			<u> </u>			
APPLIC	CATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED	
	I	1	Preliminary	8/12/78	END	
		2	Preliminary Revised	2/20/79	FLD	
		3	Preliminary Revised	3/15/79	She.	

### **PRELIMINARY**

NOTE — NUMERICAL REVISION DESIGNATION INDICATES THAT THIS DRAWING IS NOT RELEASED FOR PRODUCTION

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UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC- DECIMALS ANGLES	CONTRACT NO.			MI	CR	ROP(	<u> </u>	TM
TIONS .XX .XXX ± ± ± ± material	CHK BY					ON - 1200 DRIVES	SERIES	
FINISH	FMD 2.	ву -20-79	SIZE	CODE IDEN	IT NO.	DWG NO.	198	Rev.
DO NOT SCALE DRAWING			SCALE	·			SHEET 1	of 26

#### 1.0 Introduction

This specification describes the Micropolis Model 1200 series of 8" rigid disk drives. These units are intended for mini and microcomputer applications which require high speed random access disk storage at low cost.

The unit can incorporate up to 3 platters and utilizes a Minchester type head/media technology similar to that used in IBM 3350 type disk drives.

The unit outline dimensions fit within the envelope of a Shugart 8" floppy disk and the unit requires only D.C. voltages for operation. These are chosen to be compatible with those used by the Shugart floppy disk drive.

Table 1. Basic Model Numbers

Mode 1	Platters/Drive	Heads/Drive	Data Surfaces/Drive	Tracks/Inch
1201-I	1	2	1	478 TPI
1202-I	2	4	3	478 TPI
1203-I	3	6	5	478 TPI

Each unit consists of a drive mechanics assembly and a PCBA package which provides a flexible interface for attachment to a formatter/controller. The interface allows up to 4 drive units to be daisy chained to a single formatter/controller.

Since no encoding/decoding circuits are incorporated in the drive, format and encoding schemes are determined by the formatter/controller (although there are some boundary conditions imposed by the drive, eg. upper and lower flux reversal densities and number of sectors per track.).

The design of the drive unit also allows the addition within the drive envelope of either:

(a) An option PCBA which provides encoding/decoding circuitry operating with an MFM coding scheme. Interface to this board is radially orientated and utilizes an NRZ type data interface. Characteristics of the option board is the subject of specification 100291.

or

(b) A Micropolis designed formatter which utilizes a GCR technique allowing a substantially higher data packing density. It also incorporates the capability of "on the fly" error correction. In a multi drive system this board is housed in one of the drives. Characteristics of the formatter/controller is the subject of specification 100292.

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#### 2.0 General Description

The 1200 series of rigid disk drives consists of a drive mechanics assembly and a PCBA package. These combine to perform the following functions:

Interpret and generate control signals

Provide the necessary sequencing to bring the drive to the Ready state Position the read/write head/heads on the desired track Read and Write Data

#### 2.1 Disk Drive Mechanics

This consists of a die cast deck whose lower half is devoted to the recording heads, platters and the voice coil motor components. This lower half is sealed and air is circulated throughout the area by disk rotation induced flow. This flow is directed through a 0.3 micron absolute filter. The sealed area breathes to the outside via a similar filter.

There are no active electronic parts in the "clean" area and electrical connection is made between this area components and the electronics package via a PCB, which also seals the "clean" area from the rest of the casting.

#### 2.2 Drive Motor

Rotational drive for the platters is provided by a direct coupled brushless D.C. motor. This combination provides a very low profile allowing 3 platters to be packaged in an envelope only 4.62" high. Switching information for the electronic commutator is supplied by 3 photo transistor/LED combinations attached to the motor control PCBA.

#### 2.3 Positioner System

The positioner is a balanced swing arm mechanism supported on two preloaded bearings which reference to a stub shaft rigidly attached to the casting. The system is designed to accept between 2 and 4 arms depending on the model number. The voice coil is attached to the system on the opposite side of the bearings from the heads and the whole mechanism is statically balanced. The magnet is of the short coil long magnet type and utilizes a Ferrite magnet. Position reference is made to tracks recorded on a dedicated surface on the platter nearest the deck. These tracks are recorded with position information in the "Modified Dibit" format.

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#### 2.4 Read/Write Head

This consists of a single gap slider assembly of the Winchester type with the slider surface modified to run at 3600rpm.

#### 2.5 Electronics Package:

Three boards are normally packaged within the drive envelope. [Options have been referenced in 1.0]

(a) Preamplifier PCBA

This provides the following functions:

- ° Selection of 1 through 5 heads
- ° Read'Preamplification
- ° Servo Preamplification
- ° Write Current Drives
- ° Fault Detection circuitry

Interconnect between the "clean area" components and the electronics package

(b) Motor Control PCBA

This provides the following functions:

- ° Electronics including photo sensors and power amplifiers related to the drive motor function
- $^{\circ}$  Speed Control circuits which control the drive speed to  $\pm 0.5\%$
- ° Positioner power amplifier circuits
- ° Servo preamplifier and compensation circuits
- ° Power sensing circuits

#### (c) Device Electronics PCBA

This provides the following functions:

- ° Mrite Logic circuit
- ° Read amplifier AGC equalizer and peak detection circuits
- ° Servo electronics, including signal amplifier AGC, and modified dibit demodulator
- Microprocessor based control logic including drive sequencing, velocity profile generation and bad cylinder reallocation circuits
- ° Interface drivers and receivers

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#### 3.0 Controls and Indicators

#### None

When power is applied to the drive and the power sense circuit determines that all the voltages are within limits, the initial load sequence occurs. This consists of running the spindle up to operating speed and positioning the heads over cylinder  $\emptyset$ .

#### 4.0 Format

There are no inherent restrictions to the type of format that can be used. A jumper optioned sector counter is provided in the drive electronics which is operated from the servo clock.

The servo clock consists of 6000 pulses per disk revolution. The jumper optioned counter can provide any count of these pulses up to 4096. (see Section 6.1.4 for further description)

This system provides sector pulses and an index pulse and allows hard and soft sectoring schemes to be used. Also the long term speed variation of the drive is  $\pm 0.5\%$ . This allows the write clock to be derived from an external crystal without significant loss of capacity. The write clock can also be derived by phase lock techniques from the servo clock.

#### 5.0 Specifications

#### 5.1 Performance Specifications

#### Unformatted Capacity

MODEL	MODEL	1201-I	MODEL	1202-1	MODEL	1203-I
CODE	MFM	GCR	MFM	GCR	MFM	GCR
K Bytes Per Track	11745	15475	11745	15475	11745	15475
M Bytes Per Surface	6.81	8.975	6.81	8.975	6.81	8.975
M Bytes Per Model	6.81	8.975	20.44	26.93	34.06	44.87
Transfer Rate/ M Bits sec.	5.64	7.43	5.64	7.43	5.64	7.43

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#### 5.1 (Continued)

#### Formatted Capacity (GCR code)

MODEL	NO. OF SECTORS PER SURFACE	<u>1201-I</u>	1202-1	<u>1203-I</u>
128 Byte Sector	72	5.35	16.03	26.73
256 Byte Sector	42	6.24	18,71	31,18
512 Byte Sector	24	7.13	21.38	35.64
1024 Byte Sector	12	7.13	21.38	35.64

Average Latency = 8.33ms.

#### Access Time

Track to Track

4 millisecs.

Average (1/3 stroke) 34 millisecs.

Settling

8 millisecs.

#### 5.2 Functional Specifications

MODEL NO.	120	<u>1 - I</u>	120	<u>2-I</u>	120	<u>3-I</u>
Platters	1	1	2	2	3	3
Data Surfaces	1	. 1	3	3	5	5
Data Heads	1	1	3	3	5	5
Recording Density bpi	6640	8750	6640	8750	6640	3750
Flux Density frpi	6640	5833	6640	5833	6640	5333
Encoding Method	MFM	GCR	MFM	GCR	MFM	GCR
Spindle Speed rpm	3600	3600	3600	3600	3600	3600
Speed Variation %	±.5	±.5	±.5	±.5	±.5	±.5
Track Density tpi	478	478	478	478	478	478
Available Tracks	580	580	580	580	580	580

Media Oxide coated disks [IBM 3350 technology]

Outside Diameter Inside Diameter

200mm 2.5"

Thickness

0.075"

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#### 5.3 Physical Specifications

#### 5.3.1 Mechanical Dimensions (see Figure 11)

Depth

14.25"

Midth

8.55"

Height

4.62"

Weight

Less than 22 lbs.

#### 5.3.2 Environmental

Ambient Temperature Range: 10°C to 40°C

Relative Humidity: 10% - 80% non condensing

#### 5.3.3 <u>Dissipation</u>

Total Dissipation including positioning: 75 watts

Dissipation in Clean Area including positioning: 30 watts

#### 5.3.4 Reliability Specifications

Soft Read Errors

 $1 \text{ in } 10^{10}$ 

Hard Read Errors

 $1 \text{ in } 10^{12}$ 

MTBF (Total Unit)

10,000 hrs.

MTBF "Clean" Area

Components

.

25,000 hrs.

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#### 6.0 Electrical Interface

#### 6.1 Signal Interface

Signal Connectors Jl and J2 provide the interface between the disk drive and the host controller.

#### 5.1.1 J1 Connector

J1 is a 50 pin PCBA edge connector which provides for control, data and status signals. Up to four drives may be daisy-chained on this interface.

Either flat cable or twisted pair may be used with a maximum cable length of 20 feet. The mating connector for flat cable is Scotchflex 3415-0001 or equivalent. The connector is keyed between pins 4 and 6 and between pins 8 and 10.

Figure 2 lists the interface lines and Figure 3 provides a summary of the electrical characteristics of the interface.

Termination resistor networks are provided where required on the drive electronics PCBA. In multiple drive systems they should be installed in the last drive only.

The J1 Connector provides 15 input lines and 8 output lines. All lines except servo clock and data are low true TTL compatible signals with the following logic levels:

The servo clock and data signals are transmitted via balanced line differential interface circuits.

#### 6.1.2 J2 Connector

J2 is a 10 pin strip line connector which provides for radial status signals. The host controller must provide separate cable drivers and receivers for each drive.

Signals on J2 are not conditioned by ENABLE or drive selected.

Either flat cable or twisted pair may be used with a maximum cable length of 20 feet. The mating connector for flat cable is Scotchflex P/N 3473-0000 or equivalent.

Figure 2 lists the interface lines and Figure 3 provides a summary of the electrical characteristics of the interface.

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The J2 connector provides 4 output lines. All lines are low true TTL compatible signals with the following logic levels:

True =  $\emptyset$ - $\emptyset$ .4V False = 2.5 - 5.25V

#### 6.1.3 Input Lines

#### a) ENABLE Interface Enable

A false level on this line inhibits all drives connected to the interface from responding to any other interface lines.

This signal may be used as a power fail signal to prevent drives from responding to spurious signals when the host controller is powered up or down.

A true level on this line enables the drive specified by the drive select lines to respond to the interface.

#### b) DSØ, DS1 Drive Select Ø,1

These two lines specify the address of the drive which is actively connected to the controller. The drive address  $\emptyset$ -3 is represented by a binary number  $\emptyset$ -3 with DSØ as the least significant bit.

The address of each drive is determined by a jumper connection on the drive electronics PCBA. In a multiple drive system, each drive must be jumpered for a unique address.

When selected, a drive responds to signals on the input lines and provides signals on the output lines. All interface lines on Connector Jl are conditioned by drive selected. Lines on Connector J2 are enabled irrespective of the state of drive select or ENABLE.

#### c) BAØ, BAI Bus Address Ø,1

Control information is transferred from the host controller to the drive via an 8 bit input bus. The two bus address lines are used to route the input Bus contents to the appropriate register in the drive electronics.

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The register address  $\emptyset$ -3 is represented by a binary number  $\emptyset$ -3 with BA $\emptyset$  as the least significant bit. The drive registers which may be selected are:

<u>BA1*</u>	<u>BAØ</u> *	REGISTER
Ø	Ø	Ø - (Not Used)
Ø	1	1 - Head/cylinder address register 4 MSB
1	Ø	2 - Cylinder address register 8 LSB
1	1	3 - Control register

\*  $\emptyset$  = False

1 = True

#### d) BUSEN Bus Enable

This line coordinates the exchange of information between the host controller and the drive over the 8 bit input bus.

When this line is asserted, the contents of the input bus will be applied to the drive register selected by the bus address lines. If the head or cylinder address registers are selected, the bus contents will be latched into the selected register on the true to false transition (trailing edge) of BUSEN. If the control register is selected, the bus contents are applied directly to the drive control logic as long as BUSEN is true. The control information is not latched in the drive.

The bus address lines must be stable during the time that BUSEN is true. Detailed timing is given in Figure 4.

#### e) BUSØ - BUS7 Drive Input Bus Ø-7

The 8 input bus lines are used to transfer control information into the drive. When the bus contents represent a binary number, BUSØ is the least significant bit and BUS7 is the most significant bit.

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The meaning assigned to each bus line is a function of the register selected by the bus address. The bus assignments associated with each drive register are as follows:

Bus Address Ø - Not assigned

Bus Address 1 - Head/cylinder address 4 MSB

			bus				
7	6	5	4	3	2	1	Ø
С	С	С	С	Н	Н	Н	Н
11	10	9	8	3	2	1	Ø

HØ-3 - Head address

C8-11 - Most significant 4 bits of cylinder demand address

On the true to false transition (trailing edge) of BUSEN, the contents of BUSD-3 are transferred to the head address register and the contents of BUS4-7 are transferred to the most significant 4 bits of the cylinder demand address register.

The head address selects the surface to be used in subsequent read/write operations.

Bus Address 2 - Cylinder address 8 LSB

				ous				
Ī	7	6	5	4	3	2	1	Ø
	С	С	С	С	С	С	С	С
L	7	6	5	4	3	2	1_	Ø

CØ-7 - Least significant 8 bits of cylinder demand address

On the true to false transition (trailing edge) of BUSEN, the contents of BUS&-7 are transferred to the 8 least significant bits of the cylinder demand address register. Seek complete status is cleared, thereby initiating a seek operation to the specified cylinder.

If the specified cylinder address is invalid, the drive will terminate the operation by setting illegal cylinder status and seek complete status true.

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>

If the specified cylinder address is valid, the drive will position the heads over the desired cylinder and terminate the operation by setting seek complete status true. Illegal cylinder status is reset at the time the cylinder address is validated.

#### Bus Address 3 - Control register

	`

1	7	6	5	4	3	2	1	Ø
	//	R	/	Ŀ	т	T	/	W
	,	T	,	R	ó	Ó	/	E
	/		, , , , , , , , , , , , , , , , , , ,	S	М	Р	1	N
	/	R	1	T				

When BUSEN is true these lines are applied to the drive logic to perform control functions. These lines are effective until BUSEN is made false.

The control functions are as follows:

#### WEN - Write enable

This line controls the read/write mode of the selected drive. The write circuits are enabled when WEN is true providing the drive is ready and no write unsafe condition exists. Data signals appearing on the WDA pair are recorded on the selected surface. On conclusion of a write operation, setting WEN false disables the write circuits and enables the read circuits.

#### TOP - Track offset plus

When this line is asserted the heads are positioned off of the nominal cylinder position by 1/4 track in a direction toward the center of the disk. Seek complete status is not affected. The host controller must wait at least TBD msec after changing the state of this line before attempting to read. If offset is changed from plus or minus to an offset in the other direction, the host must wait at least TBD msec before attempting to read.

#### TOM - Track offset minus

When this line is asserted the heads are positioned off of the nominal cylinder position by 1/4 track in a direction away from the center of the disk. Seek complete status is not affected. The host controller must wait at least TBD msec after changing the state of this line before attempting to read. If offset is changed from plus or minus to an offset in the other direction, the host must wait at least TBD msec before attempting to read.

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#### FRST - Fault reset

When this line is pulsed true for a minimum of 250nsec, the fault status latch in the drive is cleared.

#### RTR - Restore

When this line is pulsed true for a minimum of 250nsec, seek complete status is cleared and a restore operation is initiated. The drive re-calibrates the positioner servo, positions the heads over cylinder  $\emptyset$  and terminates the operation by setting seek complete status true. Illegal cylinder status is cleared.

#### f) WDA+, WDA- Write data

This balanced pair carries encoded write data to be recorded on the disk. The encoded data consists of a sequence of pulses of TBD nsec to TBD nsec in width. The false to true transition (leading edge) of each pulse causes the current through the write head to be reversed, thereby recording a flux transition on the disk. WDA is enabled when WEN is true providing the drive is ready and no write unsafe condition exists.

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#### 6.1.4 Output Lines

#### a) RDY Drive ready status

This line indicates the operational status of the selected drive. It is true when the drive has completed the initial load sequence and no fault condition exists. When false, writing and seeking are inhibited.

The initial load sequence occurs when power is applied to the drive. The sequence consists of running the spindle up to operating speed and positioning the heads over cylinder  $\emptyset$ .

#### b) FLT Fault status latch

This status line is asserted whenever a fault condition occurs. It remains set until cleared by a fault reset or removal of power.

The following fault conditions are detected:

- 1) <u>DC power</u> one or more DC voltage is low
- 2) Spindle servo fault operating speed cannot be reached or maintained
- 3) <u>Positioner fault</u> a positioner servo fault prevents completion of a seek, restore or initial load
- 4) Read/write fault -
- 5) Write unsafe a write is attempted when drive is not ready or heads are not positioned over the nominal cylinder position

If fault conditions 1,2,3 or 4 are detected the heads are moved out of the data area and the spindle is disabled. If fault status is cleared the drive will attempt a load sequence.

#### c) <u>ILLADR</u> Illegal address status

This line is asserted whenever the host controller commands a seek operation to a cylinder address which is invalid. It remains true until a restore or a seek to a valid address is performed.

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#### d) SKCMP Seek complete

The false to true transition of this line indicates the completion of a seek, restore or initial load sequence. Once a load sequence is complete, this line will go false if a seek or restore is initiated or a fault condition is detected which causes the drive to unload.

A seek, restore or read/write operation must not be attempted unless this line is true.

#### e) IDX Index pulse

This line is pulsed true once each revolution of the disk to indicate the beginning of the track. Timing is given in Figure 7.

#### f) SECP Sector pulse

This line is pulsed true to indicate the beginning of each sector. Sector pulses are generated by a programmable counter which counts servo clocks.

The counter is programmed by means of a jumper platform on the drive electronics PCBA. The number of servo clock periods between sector pulses are equal except for the last sector, which may be greater than one sector time but less than two sector times.

The pulse for sector Ø occurs coincident with index or may be optionally omitted.

Index and sector timing are given in Figure 7.

#### g) SCLK+, SCLK- Servo clock

This balanced pair carries a continuous clock signal derived from the servo track. Nominally 6000 pulses per revolution of the disk are provided.

This signal may be used to frequency lock a VFO in the host controller to provide a write clock which is slaved to the rotational speed of the disk.

The pulse period corresponds to 32 bit cells for a nominal recording period of TBD BPI with timing given in Figure 8.

#### h) RDA+, RDA- Read data

This balanced pair carries composite read data from the drive to the host controller. The data consists of a series of pulses; one for each flux transition recorded on the disk. The false to true transition (leading edge) of each pulse should be used as the time reference.

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**APPLICATION** 

**REVISIONS** 

Read data is inhibited during a write operation and is invalid for  $10\mu$ sec after WEN is made false. It is also invalid for  $10\mu$ sec after head selection and when seek complete is false.

#### 6.2 DC Power Requirements

DC power is applied to the disk drive via a 10 pin AMP connector J3. Pin assignments are given in Figure 10. The mating connector is AMP  $1-87159-\emptyset$ .

DC power requirements are:

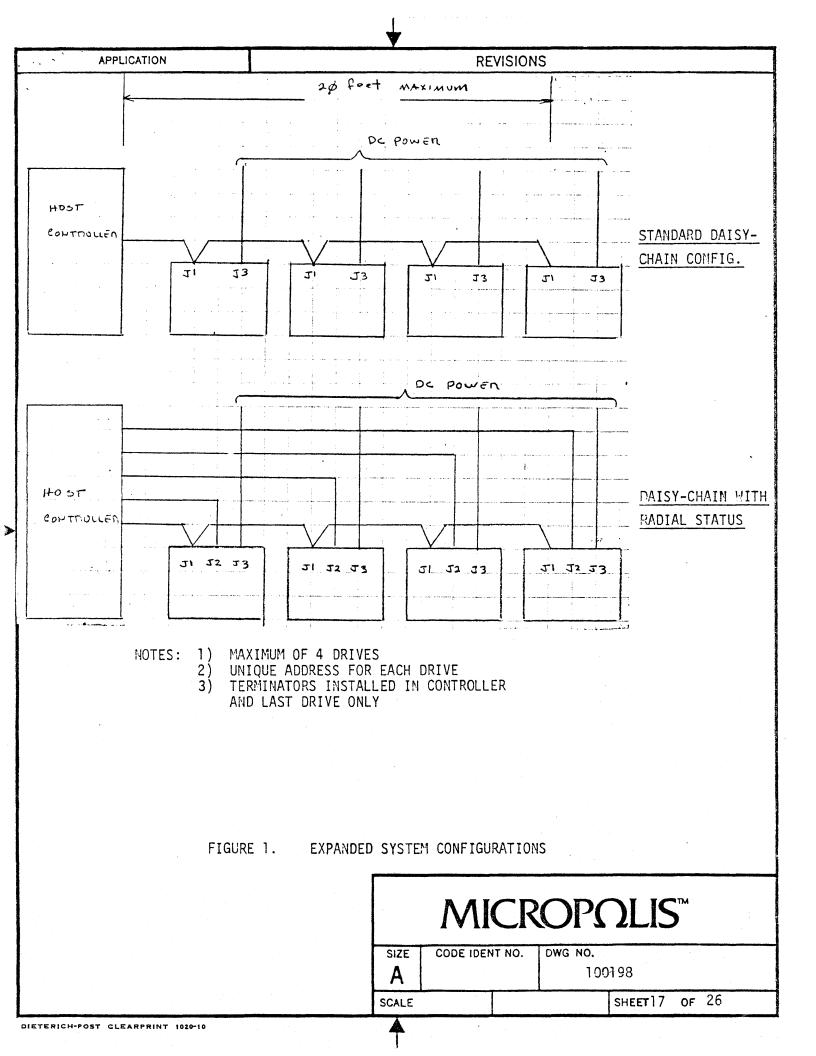
	CURR	FNT
<u>VOLTAGE</u>	AVERAGE	PEAK
+24V ±5%	2.5	4,5
+ 5V ±5%	2,25	2.25
-12V ±5%	.5	,5

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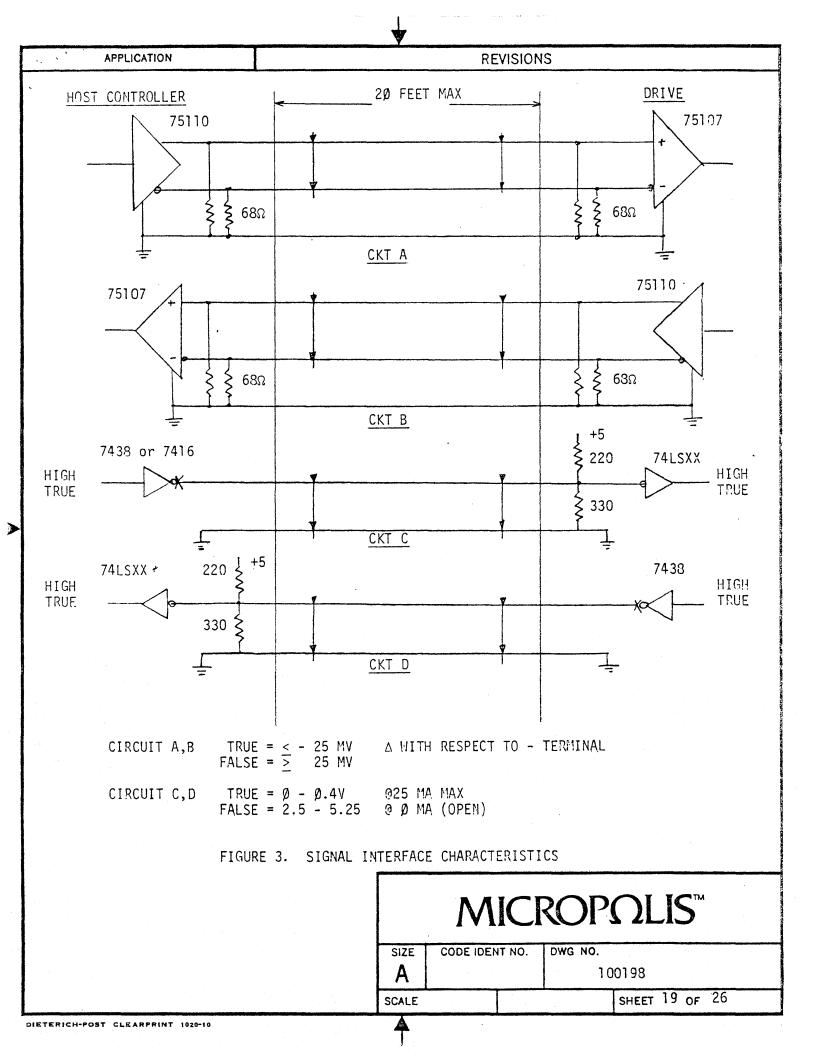
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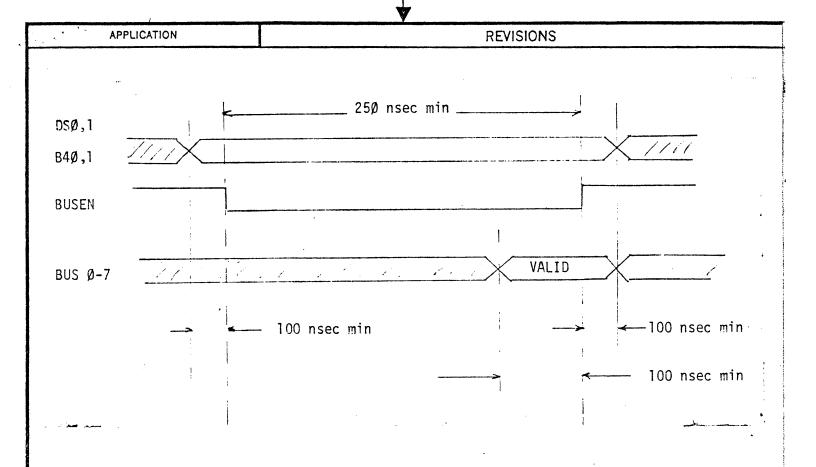


APPLICATION			REVISIONS	
Jl Connector				
<u>RETURN</u> SIGNAL	NAME	DESCRIPTION		<u>DIRN</u>
TBD	DS1 DSØ BUSEN BA1 BAØ ENABLE BUS7 BUS6 BUS5 BUS4 BUS3 BUS2 BUS1 BUSØ RDY FLT ILLADR SKCMP IDX SECP	DRIVE SELECT (DSØ is LSB) BUS ENABLE BUS ADDRESS (BAØ is LSB) INTERFACE ENABLE  DRIVE INPUT BUS (BUSØ is LSB)  DRIVE READY STATUS FAULT CONDITION STATUS ILLEGAL ADDRESS STATUS SEEK COMPLETE STATUS INDEX PULSE SECTOR PULSE		IN OUT OUT OUT OUT
	SCLK+ SCLK-	SERVO CLOCK (BALANCED PAIR)		OUT
	RDA+ RDA-	READ DATA (BALANCED PAIR)		OUT
	WDA+ WDA-	WRITE DATA (BALANCED PAIR)	•	I i j
J2 Connector  RETURN SIGNAL  TBD	NAME RDY SKCMP IDX SECP <spare></spare>	DESCRIPTION  DRIVE READY STATUS SEEK COMPLETE STATUS INDEX PULSE SECTOR PULSE		DIRN OUT OUT OUT OUT

FIGURE 2. SIGNAL INTERFACE J1:J2

	MIC	CR	OP	DLIS	тм	
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- NOTES: 1) TIMING AS OBSERVED AT DRIVE INTERFACE
  - 2) BUS Ø-7 TIMING SHOWN FOR LOADING HEAD/CYLINDER REGISTERS
  - 3) TIMING FOR INDIVIDUAL BUS BITS WHEN CONTROL REGISTER SELECTED DEPENDS UPON FUNCTION PERFORMED

FIGURE 4. GENERAL BUS TIMING

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APPLICATION REVISIONS

TBD

FIGURE 5. WRITE DATA

TBD

FIGURE 6. READ DATA

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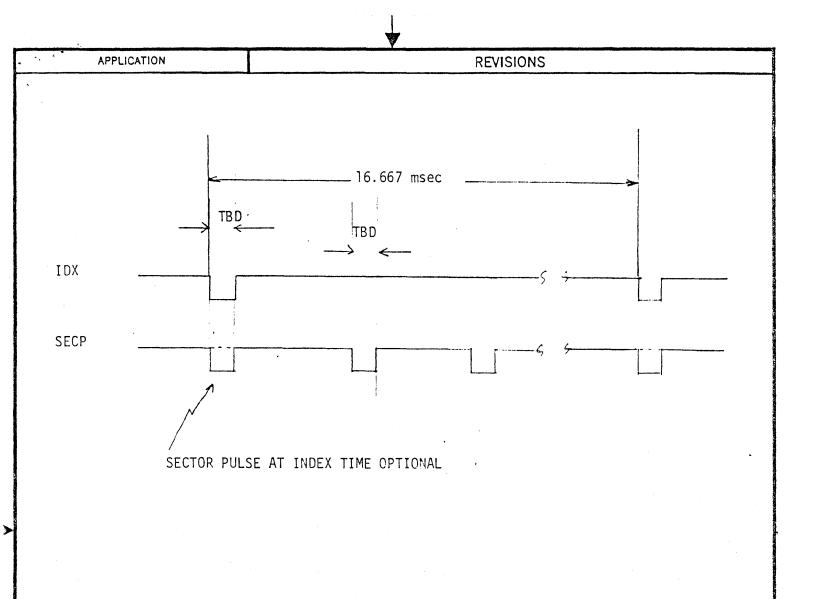


FIGURE 7. SECTOR PULSE/INDEX TIMING

	M	CF	ROP	<b>DLIS</b>	Sm		
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TBD

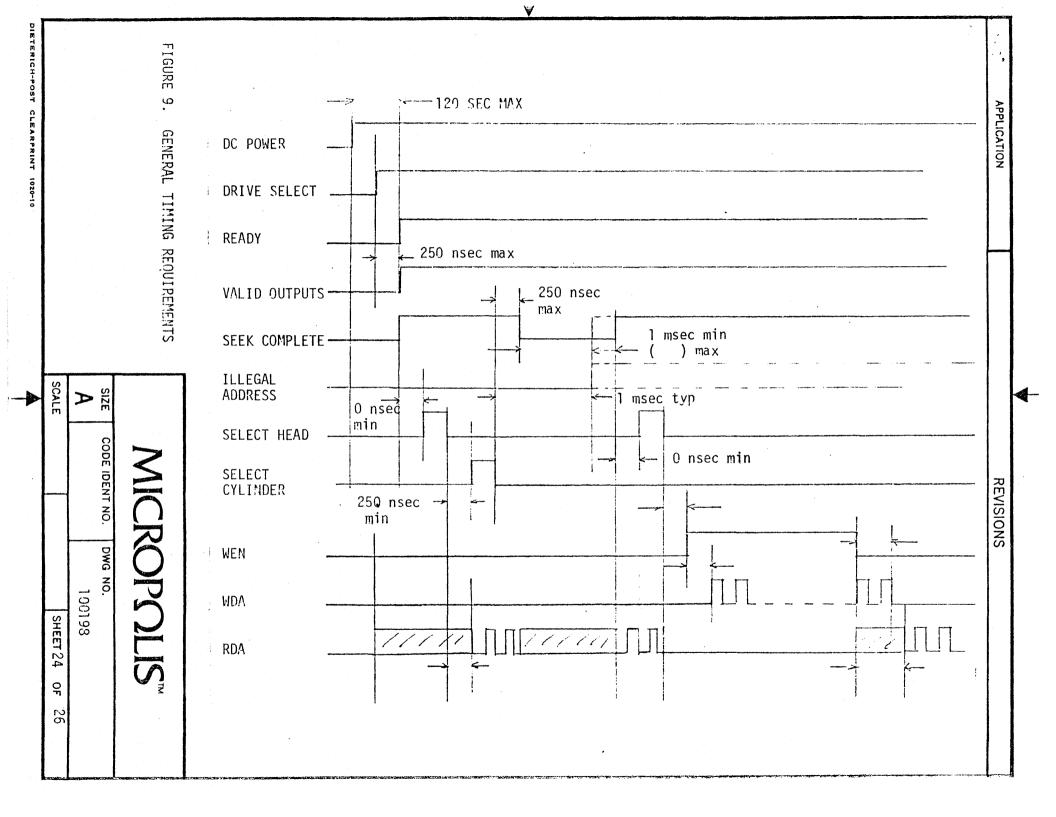
FIGURE 8. SERVO CLOCK TIMING

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**APPLICATION REVISIONS** PIN VOLTAGE 1 +24V SENSE GND 2 3 -12V SENSE +5V SENSE 5 GND 6 GND +5V -12V 9 GND +24V 1Ø

FIGURE 10. POWER CONNECTOR J3

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