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2.0	APPLICABLE DOCUMENTS	
	The following documents form a part of thi to the extent specified herein.	s specification.
	Any conflicts between applicable documents document shall be referred to the cognizan group for interpretation, clarification, a	and/or this t engineering nd resolution.
2.1	Functional Specification	
	882052 Integrated File Adapter	
	882053 Integrated Communications Adapter	
	882046 Integrated Line Printer Adapter (S/N 4 thru 11)
	882067 Integrated Card Reader Adapter (S	/N 4 thru 11)
	882045 Integrated Reader-Punch Adapter	
	882076 Integrated Card Reader Adapter (S	/N 12 and beyond)
· . ·	882051 Basic Data Channel	
	882059 Power System	
	882068 7300 Main Storage	
2.2	Other Reference Documents	
	881803 TTL High Speed Ground Rules	
	881805 TTL Medium Speed Ground Rules	
	881828 TTL1-TTL2 Interface Ground Rules	
	881879 Final Assembly, Type MSC70 Module	
•	881986 Printed Circuit Board Design Guide	e
	882019 A.C. Power Requirements for Equips	ment
	882020 Environmental Requirements for Equ	uipment
	890500 7200/7300 Processor Machine Featu	re Index
	882038 7300 Processor Test Specification	
	Midwest Operations Quality Assura	nce Manual
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3.0 REQUIREMENTS

Equipment Group

The 7300 Processor shall meet the requirements as stated within this Section.

The 7300 Processor shall support the Main Storage facility referenced in Section 2.1 and shall conform to the Address, Data and Control Signal conventions as described within that applicable document.

3.1 General Description

The Memorex 7300 Processor shall be defined as a micro-program controlled, I/O oriented, Business Data Processor as shown in Figure 1.

The Central Processing Unit shall provide "multi-state" processing and shall consist of five functional units designated as Control Storage, Arithmetic Logic Unit, Register File, Register Option and Timing/Control. Operations within the CPU shall be performed, primarily, in 16-bit parallel mode.

The 7300 Processor cabinet shall house the processor elements which, in addition to the Central Processing Unit and Main Storage, shall include Integrated Adapters for communicating with Disc Drives, Line Printers, Card Equipment, and various Terminal devices with the latter including a Keyboard/Printer for manual entry and "hard copy" display of data. Binary data entry and display shall also be possible from the 7300 System Control Panel which shall be mounted on the front of the 7300 Processor Cabinet.

Communications with Disk Drives and Terminal devices shall be handled by the Integrated File Adapter (IFA), and the Integrated Communications Adapter, (ICA), respectively. Communication with other types of I/O equipment shall be effected by means of I/O Channel(s), either via adapters within the 7300 Processor cabinet or through compatible external controllers.

See Figure 1 for the 7300 Processor Block Diagram.

See Figure 2 for the approximate placement of Processor elements within the 7300 Cabinet.

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	nt Group	ATION	Sheet 11 of
3.1.1	Processor Organization		
	The Central Processing Unit shall b any one of ten unique "states" as d output of a Resource Allocation Net	e capab letermin work.	le of assuming ed by the
	Eight of these Processor States, de shall be unique by means of the ass within the Register File. This ass shall be accomplished such that nor execution in one of these Processor affect the contents of those regist remaining Processor States. Thus, of Processor States 0 through 7 sha primarily by means of partitioning For each of these eight Processor S assigned, and normally reserved exc shall be referred to as "Dedicated resources within the CPU for which are made, shall be commonly availab Processor States and shall be refer Resources".	signate ignment ignment mal Mic States ers ass the imp ill be a the Reg tates, lusivel Resource no excl le to a red to	d 0 through 7, of registers of Registers ro-command shall not igned to the lementation ccomplished ister File. the registers y for their use, es". All other usive assignments 11 these as "Common
	Figure 3 depicts the fundamental pa Register File.	rtition	ing of the
	The ninth state of the Central Proc Console State, shall be unique as a assignment to a portion of Control State shall access its assigned por in conjunction with certain switch System Control Panel. In addition, Timing/Control area shall be reserv usage in the case of operations whi command controlled, namely Control Storage Write operations.	essing result Storage tion of settings logic v ed for (ch shal Storage	Unit, designated of functional . The Console Control Storage s on the /300 within the Console State l not be Micro- Read and Control
	The tenth state of the Central Proc Null State, shall be unique to the control CPU operation in the absenc on the part of the other nine Proce Null State shall require usage of t only, for the purpose of resynchron ment requests for Processor States Console State.	essing l extent 1 e of res ssor Sta he Timir izing re 0 throug	Unit, designated that it shall source utilization ates. The ng/Control logic esource require- gh 7 and the

The minimum duration of any one Processor State shall be an 800 n/s interval during which the execution of a maximum of eight micro-commands shall be possible. This interval shall be referred to as a "major cycle". (The number of Micro-commands which may be executed during a major cycle shall be dependent on the nature of the Micro-command_ themselves, up to a maximum of eight).

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		The dete util and Proc maxi be e maxi acco whet when asso cons dura 100 poss cond	maximum rmined ization the abi essor s mum dur qual to mum dur rding t her the a Main ciated ecutive tion of n/s inc itions	dura accor requ lity tate ation ation o whe Erro Stor Proce cycl one remen dete	tion ding ests (und to u of ther r Co age ssor e op majo ts f rmin ousl	of to , th er M tili any rach a M rrec Sta erat r cy rom ed b y me	any the ie p ficro ze one num iain tin tin tin tin tin tin tin tic tic to tic tic tic tic tic tic tic tic tic tic	one occi riori conse Proc Stor g Coc ce oc ias m . As shal n/s coned	Proc urrent ty control current	cesso of al l con ve m r St ijor sha refe CC) and 1.2 ugh atio as d	r Sf f re l su trol ajon ate cycl ll b renc Feat whe ht, t u/s l/2 sepic	tate sour ich r) of cyc shal e is ure ther rite he m , wi u/s) of ted	sha ce u a less 1 a th terr is th tria axi th bei th in	all be mests, . The lways e mined quirec preser e for mum all ng e the	; 1, 1t
			ECC F Main Conse Total	eatur Stora cutiv Majo	e Pr ge R e Cy r Cy	esen efer cle cle	nt rence Mode Inte	e e erval							
	Io No	No	EU EI	E2	E3	E4	E5	E 6	E 7				•.		3 u/s
N	Io No	Yes	E0 E1	E2	E 3	E 4	E5	E6	E7	E8	E9]		1.0) u/s
·N	lo Ye	s No	EO EO	E1	E2	E 3	E4	E5	E6	E7				.9	u/s
N	lo Ye	s Yes	E0 E0	(E1	E2	E 3	E4	E 5	. E6	E7	E 8	E9		1.1	u/s
Y	'es Ye	s No	EO EO	E0″	E1	E2	E 3	E 4	E5	E6	E 7	1		1.0	u/s
Y	'es Ye	s Yes	EO EO	É0″	E 1.	E2	E 3	E4	E5	E6	E 7	E 8	E9] 1.2	u/s
NOTE	:S: 1 2 3 4 5	. E0 in . E0 . E8 . Con . E0 . E0 . Sto . Sto . Fe	, E0', tervals throug and E9 nsecuti provid orage r provid orage r ature.	EO", of 1 prov ve Cy es a 1 eferen es a 1 eferen	and 1 00 n prov ide 1 cle 1 hardu nce 4 hardu	El t /s e ide hard Mode ware cycl ware cycl	chrou each. Mich ware ope idl es. idl es. idl	igh E ro-cc e ope erati ler a ler a n th	9 re mman rati ons. ssoc ssoc e pr	pres d ex ons iate iate esen	ent ecut asso d wi d wi ce o	mino ion. ciat th M th M f th	r c ed ain ain e E	ycle with CC	

Figure 4 depicts the fundamental timing sequence involved in a Multi-State Operation involving Processor States 0 through 7, without priority, and using minimum interval major cycles each.

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3.1.2 Register F	ile	ی۔ بینی اور بینی اور	
The Registed designated	er File shall be divided into fo as follows:	ur ma	jor groups
Basic Regis Extended Re Extended Re Extended Re	ster File egister File, Group I egister File, Group II egister File, Group III		
Three of the for the put to Processo Register F	hese major groups shall be furth rpose of creating dedicated reso or States O through 7. For a di ile organization, see Figure 3.	er pa urces agram	rtitioned corresponding depicting
a. The Bas registe command divided to the Logical of 8 cc shall to Process command Mode" s the reg	sic Register File shall consist ers which are general purpose an d control only. These 256 regis d into 8 sets of 32 registers ea 8 Processor States having 32 Re 11y, these registers shall be ar olumns by 32 rows. Normal Micro be confined to the column corres sor State of the CPU. A special d execution referred to as "Boun shall permit any Processor State gisters in other Processor State	of 25 d und ters ch, c giste range -comm pondim mode dary to ru colum	6 16-bit er Micro- shall be orresponding rs each. d in a matrix and execution ng to the of Micro- Crossing eference mns.
b. The Ext 16 18-b under H Eight o to Proce as "F H used. be read a Proce shall b the com Process remaini one ead designa appropri in a mat the F H	tended Register File, Group I, s bit registers which are special hardware as well as Micro-comman of these registers shall be allo cessor States 0 through 7 and sh <u>Registers</u> " with only the right-m The contents of the appropriate d in advance of the major cycle(s essor State, shall be available cation during the major cycle(s) essor State and, if altered by M be updated in the appropriate F mpletion of the major cycle allo sor State, all under hardware con ing eight of these Registers sha ch to Processor states 0 through ated as " <u>Pu Registers</u> ". The con- riate Pu Register shall be hardw anner similar to that previously Register.	hall purpo nd cor cated all be ost le F Re s) al for M allo icro- cated ntrol ll be 7 and tents are co desci	consist of se and ntiol. , one each e designated 6-bits being gister shall located to icro-command cated to command, ter after to a . The allocated, d shall be of the ontrolled ribed for



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However, the purpose of the Pu Register shall be related to Control Store Address, Overflow/Link status and Skip/Control Store Parity Error Status. For a diagram depicting the timing relationships of the hardware controlled sequences for F and Pu, see Figure 4. Logically, the registers within this Group are arranged in a matrix of 8 columns by 2 rows. Normal Micro-command execution shall be confined to the column corresponding to the Processor State of the CPU. A special mode of Microcommand execution referred to as "Boundary Crossing Mode" shall permit any Processor State to reference a single register in other Processor State columns per major cycle.

NOTE: Special conventions shall apply when addressing Pu by means of Micro-commands. Moreover, the left-most 2 bit positions of Pu which relate to Skip/Control Storage Parity Error status shall be reserved primarily for hardware control.

- c. The Extended Register File, Group II shall consist of 10 16-bit registers commonly available to all Processor States. Two of these registers, designated "<u>Tie Breaker (T)</u>", and "<u>Privileged Mode, (PM)</u>", shall be under Micro-command control only and shall serve as general purpose, common resource registers. The remaining eight of these registers shall be under hardware as well as Micro-command control and shall serve as varying, special purpose, common resource registers. Micro-command control of the special purpose registers within this group must meet special conventions as determined by the varying hardware controlled functions performed at the inputs and/or outputs of these registers.
- The Extended Register File, Group III shall consist of d. a maximum of 64 16-bit registers, architectually a part of the Register File but physically a part of the Integrated Adapters and I/O Channels within the 7300 (It is not within the scope of this document Processor. to describe the actual numbers, widths or functions of the registers within this Group. Such information shall be provided by the appropriate documents in Section 2.1). For the directly addressable maximum, these 64 registers shall be divided into 4 sets of 16 registers each, corresponding to Processor States 0 through 3, having 16 registers each. Logically, these registers shall be arranged in a matrix of 4 columns by 16 rows. Microcommand execution shall be unconditionally confined to the column corresponding to the Processor State of the CPU.

NOTE: The Register Address, Data and Control signal conventions for communicating with the Extended Register File, Group III are provided in Section 3.2.4.

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Equipm	ent Group	CATION Sheet 15 of
3.1.3	Register Option	
	The Register Option shall provide the 7300 Processor by accomodatin Register Features:	the means for enhancing <u>c</u> the following <u>Selectable</u>
	Relocation and Protection Feature Basic Storage Protection Feature Job Accounting Feature Error Correction Code Feature (Re	gister Set)
	Each of these Selectable Register within the Register Option throug separate group of special purpose Relocation and Protection Feature Protection Feature shall be mutua	Features shall be supported h the implementation of a registers. However, the and the Basic Storage lly exclusive.
	As a result of the highly special functional requirements on the pa features, the operations within the occur primarily under hardware con access to the registers within the be effected only by means of spec cycles and shall be allowed for a	ized and dynamic rt of all of these he Register Option shall ntrol. Micro-command e Register Option shall ial Main Storage reference 11 Processor States.
	a. The Relocation and Protection a Segment Tag File, a Segment Matrix and an Address-Mode Re	Feature shall consist of Table, a Protection gister.
	The Segment Tag File shall con Registers corresponding to le all 256 registers in the Basic the Parity Error (PE), Console Console Data (CD) Registers in File, Group II. The Segment expansion of Main Storage Add 65,536 bytes to 1,048,576 byte	nsist of 259 4-bit Tag ft-most extension to c Register File and e Address (CA), and n the Extended Register Fag File shall provide ress capabilities from es.
	The Segment Table shall consist containing 32 bits of logical Table entries shall provide Ma relocation and Main Storage pr partitioning of Main Storage	st of 16 registers, each significance. Segment ain Storage Address rotection based on the into a maximum of 16

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	roup	Sheet 16 of
	The Access Protection Matrix shall con 16-bit registers and shall provide rea protection for each Main Storage segme Processor State basis.	nsist of 16 ad and write ent on a
	The Address-Mode Register shall be a and shall provide controls for both th and protection mechanisms on a Process	l6-bit register he relocation sor State basis.
b.	The Basic Storage Protection Feature s 3 16-bit registers referred to as "Bou This option shall provide Main Storage Pages of 256 bytes each, during Main S operations on the part of Processor S	shall consist of unds Registers". e Protection,in Storage write tates 5, 6, and 7.
c.	The Job Accounting Feature shall const registers corresponding to Processor S During each major cycle allocated to Processor States, the contents of the S2-bit register shall be incremented b	ist of 8 32-bit States 0 through 7. one of these associated by one.
d.	Error Correction Code Feature (Registe	er Set)
	The Error Correction Code Feature shall within Main Storage and shall be descr appropriate document listed in 2.1.	ll be implemented ribed by the
	The Register Set, associated with ECC as a part of the Register Option shall 16-bit quantities relevant to the serv and availability aspects of Main Stora presence of the ECC Feature.	but accessed l provide 4 viceability age in the



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Equip	ment	Gro	úρ

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f.

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D Register: 16-bit Register providing data to Main Storage during word and byte write operations.

g. Shift Network: Left shifter, 32 bits wide, 0 to 15 bit positions per pass, end-off left-most, zeros in right-most, Au/Bu format.

h. Adder: 16-bit parallel, full add, four 4-bit Groups with inter-Group carries Micro-command conditioned for decimal arithmetic.

- i. <u>ALU Status:</u> Overflow, Link, Au = Zero, Au = Bu, Au>Bu algebraic, Au>Bu logical, Au<Bu algebraic, Au<Bu logical.
- j. Bit Sense: Au set or clear on bit position basis and Au set or clear, left to right scan including a Bu adder for scan result addition.
- k. <u>Constant Generator</u>: Immediate operand generator, (including Processor State number).
- 1. <u>ALU Fan-In</u>: Multi-input, multi-format multiplexer providing data to the Register File during write operations, (includes Boolean functions for Au/Bu).

m. <u>D Fan-In</u>: Three-input, 16-bit parallel multiplexer providing the data path from Main Storage, the D Register, and the Register Option to Au and the ALU Fan-In.

See Figure 5 for a Block Diagram of the ALU.

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Equipment Gr		Sheet 19 of
3.1.5 Contro	l Storage	
The Co major the "A	itrol Storage facility shall be di areas referred to as "Control Stor Idress Table".	vided into two age proper" and
a. <u>Cc</u> <u>16</u> tr 09 st	trol Storage proper shall consist 384, 14-bit words, (These 14-bit ated as 16-bit quantities in which and 10 shall be unused and always ate).	of a maximum of words shall be h bit positions in the clear
Co	trol Storage proper shall be addre address register referred to as "	essed by means of Su".
Wh re 16 bu cc ho cc in Pa	en the contents of Control Storage ad, translated, and executed as Mic- bit registers referred to as "Full ffer the output of Control Storage mands shall be duplicated in Ful rizontal parity checking shall be p itents of Fu2. Within Fu2, an even the set state shall constitute a rity Error with respect to Micro-co	proper are to be cro-commands, two " and "Fu2" shall proper. Micro- and Fu2 and performed on the h number of bits Control Storage ommand translation.
Co 4 wh as Pa Ho as "1 Fo CO	trol Storage proper shall be divid roups of 4096 words each. Console the shall be performed under Micro- selected and initiated at the 7300 tel shall be confined to the first vever, locations in Control Storage "RNIO", RNI1", "RNI2", "CS-PE", "M legal Address" shall be defined with a definition of all hardware gene stants, see 3.5.	ded into a maximum of s State operations -command control O System Control t of these four groups e proper referred to MS-PE" and ithin all 4 groups. erated, address
Wh re <u>St</u> Fi pr pu pr 25 pa nu bi	in the contents of Control Storage id but not treated as Micro-command orage Scan (CSS) Register within th e, Group II shall buffer the output oper. When such operations are per pose of hardware controlled checking oper shall be divided into a maximum words each. Withir each 256 word ity checking shall occur. Within ber of bits in the set state in an position columns shall constitute	proper are to be ds, the <u>Control</u> he Extended Register it of Control Storage erformed for the ing, Control Storage im of 64 pages of d page, longitudinal each page an even hy of the 14 individual e a Control Storage

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	Group	ENGINEER	ING SPECIFICAT	TION	Sheet 2	2.0 of	
b.	The Add 10-bit	ress Table words.	shall consist	of a ma	aximum	of 10	24,
	When the under M be addre D Fan-In Address checked of a pa buffere	e contents icro-commar essed by me n Network o Table loca for odd ho rity error, d into a re	of the Address ad control, the eans of decoding of the ALU. The ation thus refer rizontal parity the right-most gister referred	Table Addres g the c e conte renced y and i t 9 bit d to as	are to s Tab output nts of shall n the s shal "Pp"	o be ro le sha of the f the be absend 11 be	e ad 11 e ce
	After contents contents the app this man utilize without on the p	ompletion of s of the Pp ropriate Pr nner, the a the Addres affecting part of any	f the associate Register shall ocessor State's forementioned M s Table to per- access to Contr other Processo	ed majo 1 be wr s Pu Re Micro-c form a rol Sto or Stat	r cycl itten gister ommand Decode rage p e.	le, the into r. In 1 shall 2 Brand 5 oroper	e 1 ch
	When the read und be addre operation Address Register Panel and parity.	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan	of the Address e control, the ans of the Su H formed, the din l be transmitten ndicators on th eously checked	Table Addres Registe rect ou ed to t he 7300 for od	are to s Tabl r. Wh tput o he Con Syste d hori	b be le shall of the isole I em Cont zontal	11 ch Data trol 1
	When the read und be addre operation Address Register Panel an parity. For a de	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan etailed des	of the Address e control, the ans of the Su H formed, the din l be transmitten ndicators on the eously checked cription of the	Table Addres Registe rect ou ed to t he 7300 for od ese seq	are to s Tabl r. Wh tput o he Con Syste d hori uences	b be le shal of the isole I m Cont zontal	11 ch Data trol 1 3.5.
	When the read und be addre operation Address Register Panel and parity. For a de For a Bi	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan etailed des lock Diagra	of the Address e control, the ans of the Su H formed, the din l be transmitte ndicators on th eously checked cription of the m of Control St	Table Addres Registe rect ou ed to t he 7300 for od ese seq torage,	are to s Tabl r. Wh tput o he Con Syste d hori uences See F	b be le shall of the isole I em Cont zontal s, see Figure	11 ch Data trol 1 3.5. 6.
	When the read und be addre operation Address Register Panel and parity. For a de For a B	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan etailed des lock Diagra	of the Address e control, the ans of the Su H formed, the din l be transmitten ndicators on the eously checked cription of the m of Control St	Table Addres Registe rect ou ed to t he 7300 for od ese seq torage,	are to s Tabl r. Wh tput o he Con Syste d hori uences See F	b be le shal of the isole I m Cont zontal s, see Figure	11 ch Data trol 1 3.5. 6.
	When the read und be addre operation Address Register Panel and parity. For a de For a B	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan etailed des lock Diagra	of the Address e control, the ans of the Su H formed, the din l be transmitte ndicators on th eously checked cription of the m of Control St	Table Addres Registe rect ou ed to t he 7300 for od ese seq torage,	are to s Tabl r. Wh tput o he Con Syste d hori uences See F	b be le shall of the isole I em Cont zontal s, see figure	11 ch Data trol 1 3.5. 6.
	When the read und be addre operation Address Register Panel and parity. For a de For a B	e contents der hardwar essed by me ons are per Table shal r Display i nd simultan etailed des lock Diagra	of the Address e control, the ans of the Su H formed, the din l be transmitte ndicators on th eously checked cription of the m of Control St	Table Addres Registe rect ou ed to t he 7300 for od ese seq torage,	are to s Tabl r. Wh tput of he Con Syste d hori uences See F	b be le shall of the isole I em Cont zontal s, see figure	11 ch Data trol 1 3.5. 6.

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MEMOF	ENGINEERING SPECIFICATION	Number 882000
3.1.6 Main	Storage	
Main desc	Storage facilities for the 7300 Proces ribed by the appropriate document lis	ssor shall be ted in 2.1.
In a sign app1 7300	ddition to the conventional Address, D al requirements, the following general y to the CPU/Main Storage relationship Processor.	ata and Control statements shall within the
а.	Word (16-bit) and byte (8-bit) operations supported, including the means for error (and error correction in the presence (Feature).	ons shall be or checking of the ECC
b.	In the absence of the Relocation and P Feature, the CPU shall address a maximu bytes.	rotection um of 65.536
с.	In the presence of the Relocation and I Feature, the CPU shall address a maximu 1,048,576 bytes.	Protection um of
d.	References to Main Storage Addresses no present in the Main Storage facility shin an "Out of Range" condition and sha CPU to perform a hardware trap of the a Processor State. See 3.5.2, item e.	ot physically nall result ll cause the associated
e.	The CPU shall provide allowances within Resource Allocation Network for "Refres requirements on the part of the Main S	n the sh" cyclc torage facility.
f.	No minimize the impact of Refresh requinants CPU operation, the Main Storage facility capable of performing Refresh cycles in of, and in parallel with, CPU major cycles such major cycles do not involve Main S on the part of the CPU.	irements on ty shall be idependently tles whenever Storage references

MEMO	REX	ENGINEERING SPECIFICAT	ION	Number 8	82000
Equipmen	t Group			Sheet 22	d
3.1.7 M	icro-Comma	nd Repertoire			
T M C	The Micro-c Micro-comma classes.	ommand Repertoire shall c nds catagorized into the	onsist followi	of 65 b ng func	asic tional
R R P I S S S S C	Register Fi Register Fi Register Fi Register Fi Immediate C Shift Sense Skip Branch Control	le Read le Write le Read, Main Storage Rela le Write, Main Storage Rel perand	ated lated		
a	A. The Reg Micro-c true an manipul complem each re	ister File Read class shal ommands including data tra d l's complement states. ation shall be used in ord ent operations). These Mi quire 1 minor cycle for ex	ll prov ansfers (Force der to icro-co xecutio	ide 7 b in bot d Carry effect mmands n.	asic h the Register 2's shall
b	The Reg Micro-c transfe micro-c executi compara propaga executi cycles control	ister File Write class sha ommands including direct or r, Boolean and additive op ommands shall each require on except for those cases tive operations in which A tions, respectively, have on of a previous Micro-com for execution shall be pro-	all pro data tr peratio e 1 min of add Adder a not ov nmand(s povided	vide 10 ansfer, ns. The or cycle itive and nd Comp er-lappe) and 2 under ha	basic status ese e for nd arator ed the minor ardware
C	The Reg shall p one min the pro Additio control Micro-c an impr operati	ister File Read, Main Stor rovide 11 basic Micro-comm or cycle for execution pro per minor cycles within a nal minor cycles shall be so as to result in proper ommands are translated dur oper timing relationship w ons.	rage Re mands, ovided major c allowe rexecu- ing min vith Ma	lated c each rec they occ cycle. d under tion whe nor cyc in Stora	lass uiring cur on hardware en such les having age
• d	The Reg shall p a minim same ha previou Storage	ister File Write, Main Sto rovide 2 basic Micro-comma um of 1 minor cycle for ex rdware controls for timing sly described for the Regi Related class.	orage Ro inds, ea cecution ; adjust ster F	elated o ach requ h with t tments a ile Read	class uiring che us L, Main

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Equipment	Group	ENGINEERIN	ig specificat		Sheet	23	
e.	The Im Micro-c nybl ar each re	nediate Operan commands inclu id bit format equire 1 mino	nd class shal uding immedia s. These Mic r cycle for e	l provi te oper ro-com xecutio	ide 6 b rands i nands s on.	asic n byte, hall	
f.	The Shi involvi These M for exe	ft class sha ng the use of ficro-commands cution.	ll provide 4 f Au/Bu and t s shall each	basic M he Shi require	licro-c Et Netw 2 min	commands ork. or cycles	te e la
g.	The Sen involvi the Bu 2 minor	se class sha ng the use of adder. These cycles for e	ll provide 4 f Au/Bu, the e Micro-comma execution.	basic N Au Sens nds sha	ficro-c e Netw 11 eac	ommands ork and h require	
h .	The Ski includi well as Au and 1 minor and 2 m	p class shall ng zero, non- logical cor Bu. These Mi cycle for en inor cycles f	l provide 8 b -zero, and bi nparisons bet icro-commands xecution when for execution	asic Mi t sensi ween shall a skip when a	cro-co ng in each r is no skip	mmands Au as equire t performed is performe	d.
i.	The Bra includi Constan Except brancte cycle w a major other t (Addres branche cycle i minor c	nch class sha ng Function I t and Partial for the Forma s, these Mich hen executed cycle and 2 ime in the ma s Table) and s shall requi n which they ycles).	all provide 6 Decode, Forma L Address bran at Decode and ro-commands s during the 1 minor cycles ajor cycle. Address Cons tre the remain are read for	basic t Decod nch cap Addres hall re ast min if exe The For tant (R nder of execut	Micro- le, Add abilit s cons quire or cyc cuted mat De NI are the m ion, (commands ress ies. tant 1 minor le of at any code _) ajor 1 to 8	
j .	The Con of vary command Timing, Mode Mi	trol class sh ing complexit s within this Input/Output cro-command c	all provide y and execut class shall Termination control.	7 basic ion tim provid and Bo	Micro es. T e the undary	-commands he Micro- means for Crossing	



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Sheet 24

3.1.8 Resource Allocation

Processor State determination shall be performed on a major cycle basis by means of a Resource Allocation Network. Thus, utilization of shared resources on the part of dedicated resources within the 7300 Processor shall be based on the inputs to, and subsequent outputs from this Resource Allocation Network for each major cycle interval.

Without considering priorities, the Resource Allocation Network receives resource requests (and allocates resource utilization equally for these requests) from the following areas:

Main Storage: Refresh

Processor State 0: Busy Flip/Flop, Bit 00 of B/A Register Processor State 1: Busy Flip/Flop, Bit 01 of B/A Register Processor State 2: Busy Flip/Flop, Bit 02 of B/A Register Processor State 3: Busy Flip/Flop, Bit 03 of B/A Register Processor State 4: Busy Flip/Flop, Bit 04 of B/A Register Processor State 5: Busy Flip/Flop, Bit 05 of B/A Register Processor State 6: Busy Flip/Flop, Bit 06 of B/A Register Processor State 7: Busy Flip/Flop, Bit 07 of B/A Register

Console State: Console Request Hlip/Flop

Note: The B/A Register referred to as containing the Busy Flip/Flops for Processor States 0 through 7 shall be a special purpose, common resource register within the Extended Register File, Group II as previously designated in 3.1.2.

Each Main Storage Refresh request shall have unconditional priority over all other resource requests and shall result in a major cycle Null State, 800 n/s in duration. This Null State shall also result from the absence of all resource requests as listed above.

Priority allowances shall be made within the Resource Allocation Network for Processor States 0, 1, 2, and 3 only, with priority occurring in that order. Thus in priority mode, any two Processor states within this group shall be capable of obtaining equal utilization of the shared resources to the exclusion of all other Processor States (except Main Storage Refresh requests).



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Equipme	nt Group	Sheet 26 of
	c. The Maintenance Group, in conjunction Group, shall provide the means for con monitoring fault isolation procedures within the 7300 Processor.	with the Program itrolling and and operations
	d. The Communications Activity Display Gr the means for monitoring the activitie the Communications Channels within the	coup shall provide s performed by 7300 Processor.
	Throughout the remainder of this specifica System Control Panel shall be referred to for the sake of brevity.	ition, the as the Console,
3.1.10	Implementation	
	The 7300 Processor shall utilize Transisto Logic (TTL), and both bipolar and metal-ox memories. Except for MOS Main Storage, al in the machine shall be silicon devices. medium (MSI) and large (LSI) scale integra used.	or-Transis or ide-semiconulators 1 semiconductors Small (SSI), ation shall be
	The design of the machine shall utilize co case design rules and modular construction reliability, availability, and serviceabil	nservative worst to enhance ity.

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		Number concord
	ORIEX ENGINEERING SPECIFICATION	Sheet 2.7
Equipme	nt Group	-
3.2	Register File	
	The addressing mechanism for the Register have the potential for directly addressing However, the implementation of the address shall confine the 7300 Processor to address of 346 unique registers within the Registe Despite the restriction of Extended Regist Group III addressability to only the assoc States 0 through 3, all registers within t File shall be numerically designated in he notation conforming to "Boundary Crossing	File shall 512 ₁₀ registers. ing mechanism sability r File. er File, iated Processor he Register xadecimal Mode" format.
	00 06 07 08 09 10 11 12 1	3 14 15
	NOT USED E STATE REGIST	ER
	Bits 00 through 06 shall not be used but sireferred to as being in the clear state fo of 16-bit hexadecimal notation.	hall be r the purpose
	Bit 07 in the clear state shall specify the Register File and in the set state shall specify Extended Register File.	e Basic pecify the
	Bits 08, 0° and 10 shall specify the Proces number when applicable.	ssor State
	Bits 11, 12, 13, 14 and 15 shall specify the number within the Basic or Extended Group by Bit 07 and for the appropriate Processon specified by bits 08, 09 and 10 where applications.	he Register as specified r State as icable.
	The storage facilities within the Register volatile in nature, i.e. the contents of the File shall be lost when power is removed. contents of the Register File shall be unprundefined after power is applied except for affected by the System Reset associated with sequence. With the exception of the Extend Group III, the effects of System Reset on the File are described in 3.10.3.8. For the effected in 3.10.3.8.	File shall be the Register Moreover, the redictable and r those registers th the Power-on ded Register File, the Register ffects of System III, see the
	Where Register File characteristics are ass particular Micro-commands, these Micro-comm referenced by mnemonics. Each mnemonic is with an individual Micro-command as describ through 3.8.12.	sociated with only nands shall be associated bed in 3.8.3

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	OREX Int Group	ENGINEERING	SPECIFICATION	Number 892000 Sheet 28
3.2.1	Basic Regis	ter File		
	The Basic R registers, 7, using th	egister File sh 32 registers ea e following her	hall consist of 2 ach for Processor xadecimal notatio	56 16-bit States 0 through n, inclusively:
	Processor S 0 1 2 3 4 5 6 7	tate Regi 000 002 004 006 008 004 006 006	ister Numbers $00 \rightarrow 001F$ $20 \rightarrow 003F$ $40 \rightarrow 005F$ $50 \rightarrow 007F$ $80 \rightarrow 009F$ $A0 \rightarrow 00BF$ $C0 \rightarrow 00DF$ $E0 \rightarrow 00FF$	
	The registe registers un the appropri	rs within this nder Micro-comm iate Processor	group represent mand control only States as shown.	general purpose , dedicated to
	For the purp Micro-comman the left-mos File may be	pose of recording ad control (CMI st 8-bits of ar written withou	ing status condit P, CMU, RNI1 and ny register in th nt affecting its	ions under RNI2 Micro-commands) e Basic Register right-most 8-bits.
	System Rese Basic Regis	t shall not a ff ter File.	fect the register	s within the
	For each Pro Basic Regis their direc (LS1, LS2, H during the within the H Main Storage	ocessor State, ter File shall t Micro-command LSE, LSF) shall associated majo Register Option	Registers 1E and be special to the l use in addressing l result in hardway or cycle such tha h shall be referen	lF within the e extent that ng Main Storage are operations t registers nced in lieu of
3.2.2	Extended Reg	gister File, Gr	coup I	
	The Extended 18-bit regis 0 through 7 F and Pu for following he	l Register File sters, 2 regist These regist r Processor Sta exadecimal nota	Group I shall contents each for Pro- ters shall be des ites 0 through 7 wittion:	onsist of 16 cessor States ignated as using the
	Processor S1 0 1 2 3 4 5 6 7	tate F Regi 0100 0120 0140 0160 0180 01A0 01C0 01E0	ster Pu Registe 0101 0121 0141 0161 0181 01A1 01C1 01E1	er

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	MOEY		Number 882000
Equipment Group		ENGINEERING SPECIFICATION	Sheet 29 of
3.2.2.1	F Register		
	The left-mo shall be un	st 2 bits of each of these 18-1 used.	oit Registers
•	a. The con read in Process control these P cycles,	tents of the appropriate F Reg advance of the major cycles a or States 0 through 7 by means led minor cycle referred to as rocessor States utilizes consec the R1 operation shall not be	ister shall be llocated to of a hardware R1, (When one cutive major performed).
	b. Once re shall b resourc Control	ad, the contents of the approprie e held throughout each major cy e register, also referred to as section of the 7300 Processor	riate F Registe vcle in a commo s F, in the Tin Thus the

egister common he Timing/ he contents of the appropriate F Register within the Extended Register File, Group I shall be immediately available for Micro-command modification during each of the minimum 8 minor cycles comprising a major cycle (referred to as E0 through E7). The contents of the common resource F Register shall be capable, under Micro-command control, of direct participation in the formation of register numbers, shift counts, branch addresses, and bit position values as described in In addition, the contents of the common resource 3.8.1. F Register shall be capable of modifying the bit position within the adder from which the Link status bit is derived as described in 3.4.7.2.

Micro-commands which address the F Register in Normal Mode, (Not Boundary Crossing Mode) shall utilize the common resource F Register. Any such Micro-commands performed for the purpose of writing the F Register, (such as CLR, RNI1, and RNI2), should not be performed during the first minor cycle, E0, of a major cycle since such operations may lead to machine malfunctions in the course of executing hardware controlled multi-state sequencing.

Micro-commands which address the F Register in Boundary Crossing Mode shall utilize the appropriate F Register within the Extended Register File, Group I, provided such Micro-commands are executed during minor cycles E3 or E4. Any such Micro-commands executed in minor cycles other than E3 or E4 shall not be hardware supported and may lead to invalid results.

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Equipment Group		
c. For the involve the con Group after to Proo be per cycle	ose major cycles in which Micro- es the writing of the common res ntents of the associated Extende I, F Register shall be appropria the completion of such major cyc cessor States 0 through 7. This formed by means of a hardware co referred to as W1.	command execution source F Register, ed Register File, ately updated cles allocated s operation shall ontrolled minor
3.2.2.2 Pu Register	r - Charles and Charle	
Each of the	e 8 Pu Registers shall be format 00 01 02 0 L Control Storage Addre	ted as follows:
The left-ma bits relati conditions shall be in except in t for the pur Boundary Ch both of the	ost 2 bits shall be hardware con ing to Control Storage Parity Er , designated E and S, respective naccessible for Micro-command Co the case of Micro-commands which rpose of performing write refere rossing Mode. Such Micro-comman ese status bits.	trolled status for and Skip ly. These bits ntrol purposes address Pu nces in ds shall clear
Bit position status, res in 3.4.7.	ons 00 and 01 shall provide Over spectively, and are arithmetical	flow and Link ly defined
Bit positio Storage Add	ons 02 through 15 shall provide dress for Control Storage proper	a Control only.
a. The con be read Process control one of major c minor c Registe cycle c CIO2 Mi of Pp).	ntents of the appropriate Pu Reg in advance of the major cycles for States 0 through 7 by means led minor cycle referred to as these Processor States utilizes cycles, the R0 operation shall b cycle E8 and shall use the conte er in lieu of Pu, provided the p lid not involve the execution of cro-command which resulted in t	ister shall allocated to of a hardware RO. (When consecutive e effective during nts of the Pp revious major a CIO1 or he suppression
UI FPJ.		



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	c. The contents of the associated Extended Group I Pu Register shall be appropriate after the completion of each major cycle to Processor States 0 through 7 by mean ware controlled minor cycle referred to WO operation shall not be performed and involving the execution of a CIO1 or Command which resulted in the suppress	ed Register File, ately updated cle allocated ans of a hard- to as WO. (The fter major cycles CIO2 Micro- ssion of Pp).	
	Micro-commands which address the Extended Group I, F and Pu Registers shall be limit STA, STB and AND when performed in Boundar	Register File, ed to CLR, ry Crossing Mode.	
3.2.3	Extended Register File, Group II.		
	The Extended Register File, Group II shall 16-bit registers representing common resou for the Console State as well as Processor The State number portion of the Boundary C address format shall not be applicable for since any combination of these 3 bits shal However, for the sake of simplicity these treated as being in the clear state for th providing the following numerical designat notation.	consist of 10 rce facilities States 0 through 7. rossing Mode these registers 1 be allowed. bits are e purpose of ions in hexadecimal	
	Register NameRegister NumberBusy Active (B/A)0102Real Time Clock (RTC)0103Tie-Breaker (T)0104Parity Error (PE)0105Control (C)0106Privileged Mode (PM)0107Boundary Crossing (BC)0108Control Storage Scan (CSS)0109Console Address (CA)0108Console Data (CD)0108		
	NOTE: The Busy/Active (B/A) Register shal by numbers 0122, 0142, 0162, 0182, 01A2, 0 equivalent addressing anomaly shall also e remaining 9 registers within this group.	ll also be addressed DIC2 and DIE2. The exist for the	
	Read references to the ALU under Micro-comm shall be provided for all the registers with Write references from the ALU under Micro- shall be provided for all the registers with except the Parity Error (PE), Real Time Clu Control Storage Scan (CSS) Registers.	mand control thin this group. command control thin this group ock (RTC), and	

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Eduibilie	ent Group				
3.2.3.1	Busy/Active	Register (B/A)			
	This 16-bit Busy and Ac Processor S	register referred to tive status indication tates 0 through 7.	as B/A sh s for eac	all provide h of the	
Bit Positio Processor State	n 00 01 02 03 0 1 2 3	04 05 06 07 08 09 10 4 5 6 7 0 1 2	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	<u>14 15</u> 6 7	
Processor Status	KBU	sy	-ACTIVE		
	a. The set most by provide in the Process	outputs from the bit te of the B/A Register inputs to the Resourc form of resource reque or States 0 through 7.	position (Busy Fl e Allocat sts on th	in the left- ip/Flops) shall ion Network e part of	
	The Busy be cond Network as desc	y Flip/Flop for Proces itioned at the input t by a disable associat ribed in 3.10.3.18.	sor State o the Res ed with B	4 shall ource Allocation reakpoint stop	
	The set Registe to the describe	outputs of the 16 bit r shall be available f Console Data Register ed in 3.10.3.7.	position or select Display i	s of the B/A ion as inputs ndicators as	
	<pre>b. The input left-most condition be cond bits in Flip/Floon 0 through</pre>	uts from the ALU to the st byte of the B/A Reg oned for Processor Sta itioned on a bit-by-bi the right-most byte o ops) in the following m gh 4:	e bit pos ister sha tes 5, 6, t basis b f the B/A anner for	itions in the 11 not be hardwa and 7 but shall y the state of t Register (Activ Processor State	re he s
	For Pro Flip/Fl state un cycle in set sta	cessor States 0 and 4 op shall not change fronder Micro-command con n which the associated te.	the appro om the se trol duri Active F	priate Busy t to the clear ng any minor lip/Flop is in th	he
•	For Proc Flip/Flo state un cycle in the set	essor States 1, 2, and op shall not change fro ider Micro-command cont which the associated state.	1 3 the ap om the cle crol durin Active F1	propriate Busy ar to the set g any minor ip/Flop is in	
	c. The Busy provided Real Tim	Flip/Flop for Process with a set input for Clock (RTC) Register	or State each incr as descr	4 shall be rement of the ibed in 3.2.3.2.	
•	ананан сайта. Алаган			· · · · · · · · · · · · · · · · · · ·	



d.

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Each of the Busy Flip/Flops for Processor States 0 through 7 shall be provided with set inputs which shall be appropriately Console switch controlled as described in 3.10.3.19 and 3.10.3.20.

Each of the Busy Flip/Flops for Processor States O through 3 shall be provided with set inputs which shall be enabled by the appropriate Request signal supplied by Extended Register File, Group III controls as described in 3.2.4.9, conditioned by the corresponding Processor Control Select switch as described in 3.10.3.18 and disabled during minor cycles E6/E7 and E8/E9 associated with Consecutive Cycle operations.

Each of the Busy Flip/Flops for Processor Cirtes 1, 2 and 3 shall be provided with set inputs which shall be enabled by the appropriate Attention signal supplied by Extended Register File, Group III controls as described in 3.2.4.10, enabled by the cleared state of the appropriate Active Flip/Flop, conditioned by the Processor Control Select switches described in 3.10.3.18, and disabled during minor cycles E6, E7, E8 and E9.

Each of the Busy Flip/Flops for Processor States 5, 6 and 7 shall be provided with clear inputs which shall be enabled at the beginning of minor cycle E4 by the clear state of the appropriate Active Flip/Flop. These clear inputs shall clear the appropriate Busy Flip/Flop provided Micro-command execution begins at Control Store Address $X00X_{16}$ for the major cycle allocated to the associated Processor State. This clear input shall also clear the appropriate Busy Flip/Flop when Cycle Step operation is selected by means of the Console control described in 3.10.4.27.

Each of the Busy Flip/Flops for Processor States 0 through 4 shall be provided with clear inputs for Stop/Step operations which shall be Console switch controlled as described in 3.10.3.18 and 3.10.4.27.

Each of the Busy Flip/Flops for Processor States 0 through 7 shall be provided with clear inputs for Breakpoint operations which shall be Console switch controlled as described in 3.10.3.15 through 3.10.3.18.



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Each of the Busy Flip/Flops for Processor States O and 4 shall be provided with clear inputs which shall be enabled by the clear state of the appropriate Active Flip/Flop when the execution of CIO1 and CIO2 Micro-commands on the part of the associated Processor State results in the suppression of the Pp Register as described in 3.8.12.5.

Each of the Busy Flip/Flops for Processor States 1, 2, and 3 shall be provided with clear inputs which shall be enabled when the execution of CI01 and CI02 Micro-commands on the part of the associated Processor State results in the suppression of the Pp Register as described in 3.8.12.5.

The inputs from the ALU to the bit position in the right-most byte of the B/A Register (Active Flip/Flops) shall be under Micro-command control only.

Bit positions 13, 14 and 15 of the B/A Register, corresponding to Processor States 5, 6, and 7 Active Flip/Flops, shall be provided with set and clear inputs for Processor Run and Step/Stop operations which shall be Console switch controlled as described in 3.10.3.18 through 3.10.3.20.

3.2.3.2 Real Time Clock (RTC)

The contents of this register shall be incremented by one under hardware control every 1.6384 m/s. Each increment operation shall be synchronous to the extent that it shall occur only during minor cycle E7.

The contents of this register may be read but not written under Micro-command control. Attempts to write this register by means of Micro-command control shall result in no operation, (other than the clocking of the Pp Register for Blockpoint purposes). Upon completion of the power-on sequence the contents of this register shall begin incrementing from an unpredictable initial count, not affected by System Reset.

For every tenth increment operation performed on the contents of the RTC Register a set input shall be provided to the Busy Flip/Flop for Processor State 4. This set input shall be conditioned by the Console Executive Disable control described in 3.10.4.26 and the sequence described in 3.10.2.4 relative to Autoload and System Reset.

The set outputs of the 16 bit positions of the RTC Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10 3.7.

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3.2.3.3 Tie-Breaker (T)

This 16-bit common resource register contained within the Extended Register File, Group II shall be under Micro-command control only.

3.2.3.4 Parity Error (PE)

The contents of this 16-bit register shall be under Micro-command control for read but not write references.

Attempts to write this register under Micro-command control shall result in no operation (other than the clocking of the Pp Register for Blockpoint purposes).

Hardware control of this register shall be such that, in the event of detected addressing or data errors associated with Main Storage references, the contents of this register shall provide the Physical Main Storage address of the last such error to occur.

The input to this 16-bit register shall consist of a Main Storage Address only. This register shall be clocked under hardware control when each of the conditions described by items a through c have been satisfied and any one or more of the conditions described by items d through f have been simultaneously met.

- a. Minor cycle E7 of any major cycle in which a Main Storage reference is performed, and
- b. The state of the Console control described in 3.10.4.16 is such that Storage Parity is not disabled, and
- c. The address to which the Main Storage reference is performed is not "Out of Bounds" as determined by either the Basic Storage Protection Feature or the Relocation and Protection Feature, and
- d. The address to which the Main Storage reference is performed is not physically present in the System, (Out of Range), or
- e. The Main Storage reference cycle is a read operation in the absence of the ECC Feature, and invalid parity is detected in either the left-most or rightmost data byte, or
- f. The Main Storage reference cycle is a read operation in the presence of the ECC Feature, and an uncorrectable error is detected in either the left-most or rightmost data byte.
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|--|--|---|
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| The set out
shall be av
Address Reg
3.10.3.4. | tputs of the 16-bit positions of
vailable for selection as inputs
gister Display indicators as des | E the PE Register
to the Console
cribed in |
| NOTE: The
always be a
the absence
Feature and
in 3.10.3.1
the Relocat
Register wi
most 4-bits
Physical Ma
as previous | address clocked into the PE Reg
a Physical Main Storage Address
e or presence of the Relocation
d regardless of the Console cont
2 and 3.10.3.14. However, in t
tion and Protection Feature, the
thin the Register Option shall
s required to completely define
ain Storage Address at which the
sly defined in items a through f | gister shall
regardless of
and Protection
rols described
the presence of
PE Segment Tag
contain the left-
the 20-bit
error occurred |
| 3.2.3.5 Control (C) | | |
| This 16-bit
conditionin
and enablin
0 through 7 | t register shall provide the con
ng Priority Modes for Processor
ng Consecutive Cycle Modes for P
7. | trols for
States 0 through 3
rocessor States |
| Bit Position 00 01 02
Processor 0 1 2
State | 03 04 05 06 07 08 09 10 11 12 1 3 0 1 2 3 0 1 2 3 4 | 3 14 15 5 6 7 |
| ENALLE
Control PRIORITY | INVOKE CONSECUT
PRIORITY CYCLE EN | IVE
ABLE |
| | | |
| The content
control for
operations | ts of this register shall be und
the purpose of performing read
from the ALU. | er Mic.o-command
and write |
| In addition
this regist
section of
and Consecu
Processor S | the set outputs of the 16-bit
ter shall be interpreted by the
the CPU for the purpose of prov
tive Cycle Modes of operation f
states. | positions of
Timing/Control
iding Priority
or the associated |
| a. The Inv
be cond
Network
B/A Reg
are coi
potenti
common | roke Priority outputs of the C R
litioned at the input to the Res
by the appropriate set state o
sister. Processor States for wh
ncident after resynchronization
al for disproportionately great
resources. See 3.9. | egister shall
ource Allocation
utputs of the
ich these signals
shall have the
er use of the |
| | | |



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3.2.3.7 Boundary C	rossing (BC)	
This 16-bit for read as	t register shall be under Micro- nd write references from the ALU	command control
The set sta shall be in execution of The general in 3.2.	ate outputs from the 9 right-mos nterpreted under hardware contro of Nicro-commands in Boundary Cr 1 format for the BC Register is	t bit positions of during the cossing Mode. described
The set out shall be an Data Regist	tputs of the 16 bit positions of vailable for selection as inputs ter Display indicators as descri	the BC Register to the Console bed in 3.10.3.7.
During the Boundary Cr shall parti	execution of Micro-commands per rossing Mode, the contents of th cipate as follows:	formed in e BC Register
a. The Bas Process (Bits 0 from th the Mic 15), pr and the	sic Register File shall be addre for State designated by the BC R 08 through 10), at the register 10 "inclusive or" of the BC desi 10 cro-command designated register, 10 croided both the BC Register, (B 10 cro-command, (Bit	ssed for the egister, number resulting gnated register and (Bits 11 through it 07 clear), s 06 and 07
b. The Ext during by the be set BC Regi this gr	designate the Basic Register Fi tended Register File, Group I sh ninor cycles E3 and E4 at the a contents of the BC Register, (B and bits 11 through 14 shall be ster to effect the selection of roup, Bits 08 through 10 designa	all be addressed ddress designated it 07 slall clear within the a register within ting Processor State.
c. The Ext indepen registe the BC designa the BC (Bit 07 command When um and F) be supp registe operati	ended Register File, Group II s dently of Processor State design r number resulting from the "in designated register and the Mic ted register, (Bits 12 through Register specifies the Extended set), and both the BC Register designators, (Bit 11 clear), sp assigned registers within this are referenced for read operation lied. No operation shall occur rs within this group are referen- ons.	hall be addressed, nators, at the clusive or" of ro-command 15), provided Register File, and the Micro- pecify Group II. group (C, D, E, ons, zeroes shall when unassigned nced for write

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d. The Extended Register File, Group III shall be addressed for the Processor State, 0 through 3, performing the operation at the register number resulting from the "inclusive or" of the BC designated register and the Micro-command designated register, (Bits 12 through 15), provided the Micro-command designators specify this Group, (Bit 06, 07, and 11 set). The 3C Register does not participate for this operation in bit positions 07 through 11 and the term "Boundary Crossing Mode" becomes somewhat of a misnomer.

Boundary Crossing operations not described in items a through d shall be undefined. Moreover, write references which address the BC Register in Boundary Cross. Mode shall not be hardware supported and may result in machine malfunction.

3.2.3.8 Control Storage Scan (CSS)

The contents of this 16-bit register shall be under Microcommand control for read and write operations. However, all Micro-commands, with the exception of ROM, which address the CSS Register for the purpose of performing write operations shall result in clearing it. The ROM Micro-command shall clock the output from Control Store proper into the CSS Register in a J-K fashion, i.e. for each bit position having a set data input the clock shall cause the associated Flip/Flop to assume the set state when previously clear or the clear state when previously set; for each Flip/Flop having a clear data input the clock shall have no effect on the state of the associated Flip/Flop. The data inputs to the CSS Register in the bit 09 and 10 positions shall be confined by hardware means to the clear state.

The CSS Register shall be hardware controlled for clearing and clocking purposes during Control Storage Read Operations performed by means of the Console controls as described in 3.10.3.11. Moreover, the set outputs of the CSS Register in all bit positions except 09 and 10 shall be hardware translated for the purpose of detecting invalid longitudinal parity as required by Console initiated operations described in 3.10.3.11.

The set outputs of the 16 bit positions of the CSS Register shall be available for selection as inputs to the Console Data Register Display indicators as described in 3.10.3.7.

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3.2.3.9 Console Address (CA)					
This 16-bit register shall be under Micro-progra for the purpose of performing read and write ope from the ALU.	am control erations				
Each of the 16 bit positions of the CA Register provided with a set input under Console control described in 3.10.3.2.	shall be as				
Each of the 16 bit positions of the CA Register s provided with a clear input under a single Conso as described in 3.10.3.3.	shall be ble control				
The set outputs of the 16 bit positions of the C shall be available for selection as inputs to th Address Register Display indicators as described	CA Register ne Console 1 in 3.10.3.4.				
NOTE: When the CA Register is used under Micro- in conjunction with the set and clear inputs ava the Console controls, allowances for switch cont must be made in or by means of the Micro-command sequences as required.	command control ailable to tact bounce l timing				
3.2.3.10 Console Data (CD)					
This 16-bit register shall be under Micro-progra for the purpose of performing read and write ope from the ALU.	nm control prations				
Each of the 16 bit positions of the CD Register provided with a set input under Console control described in 3.10.3.5.	shall be as				
Each of the 16 bit positions of the CD Register provided with a clear input under a single Conso as described in 3.10.3.6.	shall be le control				
The set outputs of the 16 bit positions of the C shall be available for selection as inputs to th Data Register Display indicators as described in	D Register e Console 3.10.3.7.				
NOTE: When the CD Register is used under Micro- control in conjunction with the set and clear in available to the Console controls, allowances fo contact bounce must be made in or by means of th command timing sequences as required.	command puts r switch e Micro-				



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3.2.4.4	4 Extended Register Write	
	This single control signal from the CPU sha +ERFG3WR and shall indicate the execution o Micro-command designating the Extended Regi III,for the purpose of performing a write r	11 be abbreviated f each Format 1 ster File, Group eference.
	This write control signal shall be shared by 0 through 3 and shall be active during all which an AND, CER, EOR, IOR, SDB, SDW, STA command is executed for which the Extended is designated according to 3.2.3.7, item d c, for Boundary Crossing and Normal Modes, in the case of SDB and SDW Micro-commands, to minor cycle E5 during major cycles in whi or Register Option read references are perfo signal shall not assume the active state un	y Processor States minor cycles in or STB Micro- Register File and 3.8.1.1, iten respectively. However, translated for the ich Main Storage ormed, this til minor cycle E5.
	For timing relationships, see Figure 7.	
3.2.4.5	6 Clocks	
	These five control signals from the CPU shal +CLOCK-00, +CLOCK-20, +CLOCK-40, +CLOCK-60 shall provide the means for establishing fiv times during every minor cycle.	ll be abbreviated and +CLOCK-80 and ve unique phase
	These five timing control signals shall be s Processor States 0 through 3 and shall have state leading edges separated by intervals e of the duration of the minor cycle as design aforementioned abbreviations. Thus, the lea +CLOCK-00 shall occur at the beginning of ea +CLOCK-20 shall occur after 20% of each minor expired, +CLOCK-40 shall occur after 40% of cycle has expired, etc. After the leading e clock signal shall remain active for an inter to 30% of the minor cycle duration, subject of ±5% of the minor cycle duration.	shared by their active equal to 20% nated by their ading edge of ach minor cycle, or cycle has each minor edge, each erval equal to variations
3.2.4.6	System Reset I/O	
	This single control signal from the CPU shal +SR-IO and shall provide the means for estab operating states for control and data mechan within the Extended Register File, Group III	l be abbreviated lishing initial isms as required facilities.

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	This control line shall assume the active s completion of each power-on sequence, durin of each Reset/Load sequence provided the Co Maintenance Mode, during the initialization sequence and during the depression of the Co Reset switch as described in 3.10.3.8. The Out signals described in 3.2.4.3 shall be in minimum of 300 n/s prior to the active stat Reset I/O signal and shall remain inactive of 300 n/s after the System Reset I/O signal the active to the inactive state. Once act Reset I/O signal shall remain active for a	state ig the onsole Consol E Exte inact: te of for a il has cive, minin	unti e is each le Sy endec ive f the mirs cha the num c	il the itialization not in Auto-load ystem Register for a System imum anged from System of 2 u/s.		
	All output signals from the CPU shall be in the occurrence of the System Reset I/O with of the Clock signals described in 3.2.4.5.	activ the	re di exce	ring ption		
3.2.4.7	Extended Register In			• •		
	These 64 data signals to the CPU shall be of sets of 16 parallel signals each, with each to one of the Processor States 0 through 3. associated with Processor State 0 shall be +ERI0-00 through +ERI0-15. The remaining 3 similarly abbreviated such that the first m correspond to the Processor State (throug second and third numerics shall correspond position (00, left-most through 15, right-m set. These input signals shall provide the forming data transfers from the Extended Re Group III to the ALU under Format 1 Micro-c	livide set abbre sets umeri h 3) to th most) mean giste comman	d in corr set viat sha c sh and te bi with s fo r Fi d co	to 4 responding ed all be all the t in each or per- le, ontrol.		
	During all major cycles allocated to Process through 3, the appropriate set of 16 signal selected from these 64 input data signals a transferred to the ALU under Formal 1 Micro when read references are performed with the Register File, Group III designated accordi Item d and 3.8.1.1, Item c for Boundary Cro Normal Modes, respectively. For timing requirements, see Figure 7.	sor S s sha nd sh comm Exte ng to ssing	tate 11 b al1 nded 3.2 and	s 0 e be control .3.7,		
3.2.4.8	Extended Register Read	i a				
	This single control signal from the CPU sha +ERFG3RD and shall indicate the execution o Micro-command designating the Extended Regi III for the purpose of performing a read re	11 be f eac ster feren	abb h Fo File c e .	reviated rmal 1 , Group		
			a di A			

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This read control signal shall be shared by Processor States 0 through 3 and shall be active during all minor cycles in which a CLA, LAB, LAW, LAW, LBL, LBW, LBW, LDB, LDW, or LDW\ Micro-command is executed for which the Extended Register File is designated according to 3.2.3.7, item d and 3.8.1.1, item c, for Boundary Crossing and Normal Modes, respectively.

For timing relationships, see Figure 7.

3.2.4.9 Request

These 4 control signals to the CPU shall be abbreviated -REQ-0 through -REQ-3, individually corres onding to Processor States 0 through 3. These signals wall provide the means for accomplishing resource utilizatio. requests as originated on a Processor State basis within the Extended Register File, Group III control logic.

These control signals shall be accommodated at the set inputs of the associated Busy Flip/Flops in the B/A Fegister as described in 3.2.3.1, item c. These set inputs shall be resynchronized to the extent that they shall be disabled during minor cycles E6, E7,E8, and E9.

When the associated Processor State, 0 through 3, requires a major cycle, the appropriate Request signal shall be active until a major cycle is allocated as indicated by the active state of the associated Execute signal described in 3.2.4.1. When the corresponding Request and Execute signals are simultaneously active, the allocation of an additional major cycle for the associated Processor State shall depend on the timing of their simultaneity with respect to resynchronization of the B/A Register as described in 3.9 and Micro-command control effecting the contents of the B/A Register during the current major cycle as established by firmware conventions for each of the Processor States, 0 through 3.

3.2.4.10 Attention

These 3 control signals to the CPU shall be abbreviated -ATTN-1, -ATTN-2 and -ATTN-3 corresponding to Processor States 1, 2, and 3, respectively. These signals shall provide an additional means for accomplishing resource utilization requests as originated on a Processor State basis within the Extended Register File, Group III control logic for Processor States 1, 2, and 3.



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These control signals shall be accommodated at the set inputs of the associated Busy Flip/Flops in the B/A Register as described in 3.2.3.1, item c. These set inputs shall be resynchronized to the extent that they shall be disabled during minor cycles E6, E7, E8, and E9.

When the associated Processor State, 1 through 3, requires a major cycle, the appropriate Attention signal shall be active (but enabled at the set input to the associated Busy Flip/Flop only when the corresponding Active Flip/ Flop is in the cleared state as described in 3.2.3.1, item c) until a major cycle is allocated as indicated by the active state of the associated Execute signal described in 3.2.4.1. When the corresponding Attention and Execute signals are simultaneously active in the presence of the cleared state of the associated Active Flip/Flop, the allocation of an additional major cycle for the associated Processor State shall depend on the timing of their simultaniety with respect to resynchronization of the B/A Register as described in 3.9 and Micro-command control affecting the contents of the B/A Register during the current major cycle as established by firmware conventions for each of the Processor States, 0 through 3.

3.2.4.11 Priority

These 4 control signals to the CPU shall be abbreviated +PRI-0 through +PRI-3, individually corresponding to Processor States 0 through 3. These signals shall provide the means for accomplishing disproportionately greater use of the common resources on the part of Processor States 0 through 3 by means of establishing Priority Modes of operation on their behalf. These signals shall be originated on a Processor State basis within the Extended Register File Group III control logic but shall be individually conditioned under Micro-command control only, by means of the associated Enable Priority Flip/Flops in the C Register as described in 3.2.3.5, item b.

The active state of these Priority signals shall be effective only when the associated Processor State has both its Busy and Enable Priority Flip/Flops in the set state. The coincidence of these conditions shall be resynchronized for each Processor State 0 through 3, at the inputs to the Resource Allocation Network as described in 3.9.

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3.2.4.12 End of Transfer

These 4 control signals to the CPU shall be abbreviated -EOT-0 through -EOT-3, individually corresponding to Processor States 0 through 3. In the active state, these signals shall provide the means for accomplishing an I/O Exit during the execution of CIO1 and CIO2 Micro-commands as described in 3.8.12.5. These signals shall be originated on a Processor State basis within the Extended Register File, Group III control logic.

During each major cycle allocated to Processor States 0 through 3, the state of the associated E. 4 of Transfer signal must be stable during, and for 200 n/2 prior to, the execution of CIO1 and CIO2 Micro-commands 1. order to obtain predictable results. When the associated signal is not synchronous to the extent just described, the execution of CIO1 and CIO2 Micro-commands may result in machine malfunction.

3.2.4.13 I/O Exit

This single control signal from the CPU shall be abbreviated +IOEXIT and shall be shared by Processor States 0 through 3.

This output control signal shall be active during the execution of CIO1 or CIO2 Micro-commands only, under the conditions described in 3.8.12.5.

For timing relationships, see Figure 7.

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Equipment Group	
3.3 Register Option	
The Register Option shall be functionally four parts as related to the following Se Features: The Relocation and Protection Feature The Basic Storage Protection Feature The Job Accounting Feature The ECC Feature (Register Set)	divided into lectable Register
The Relocation and Protection Feature and Protection Feature shall be mutually exclu	Basic Storage usive.
The registers and networks within each of shall provide the means for accomplishing operations as described in 3.3.1 through majority of these operations shall be under control as specified herein and shall be a dynamically as required. When registers we features must be referenced under Micro-con- for the purpose of transferring data betwee the Register Option, a major cycle shall be similar to Main Storage references. Register references under Micro-command control shall differentiated from Main Storage references in 3.8.5.1. Register Option read reference differentiated from write references under control in the same manner as for Main Storage as described in 3.8.5.2.	these features the associated 3.3.4. The er hardware accomplished within these ommand control een the CPU and be required ster Option all be es as described ces shall be r Micro-command orage references
During all Register Option references, the S Register in the ALU section of the CPU s the register number according to the follo	e contents of the chall designate owing format:
00 01 02 03 04 05 06 07 08 09 10 11 12 1	3 14 15
(S) = NOT USED FEATURE STATE REGI	STER
a. Bits 00 through 03 shall not be used b referred to as being in the clear stat of 16-bit hexadecimal notation.	ut shall be e for the purpose
b. Bits 04 through 07 shall specify the f set within a feature, according to the hexadecimal notation.	eature, or register following
0: Relocation and Protection Feature 1: Relocation and Protection Feature 2: Relocation and Protection Feature Table	: Segment Tag File : Protect Matrix : Segment Relocation

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- 3: Relocation and Protection Feature: Address-Mode Register
- 4: Relocation and Protection Feature: Parity Error Tag Register
- 5: Basic Storage Protection Feature: Bounds Registers
- 6: Job Accounting Feature: Job Accounting Registers 7: Not Used.

8/9: ECC Feature: Main Storage Data Register

- A/B: ECC Feature: Log Register
- C/D: ECC Feature: Generated Check Bits
- E/F: ECC Feature: Read Check Bits
- c. Bits 08 through 10 shall specify a Processor State when referencing the Segment Tag File, the Protection Matrix, the Bounds Registers and the Job Adminting Registers. For all other Register Option references these bits shall be unused but shall be referred to as being in the clear state for the purpose of 16-bit hexadecimal notation.
- d. Bits 11 through 15 shall specify a register number (1 of 32) when referencing the Segment Tag File. Bits 11 through 14 shall specify a double-word register number when referencing the Segment Relocation Table with bit 15 specifying the left-most word when in the clear state and the right-most word when in the set state. Bit 15 shall also be used to specify the leftmost word in the clear state and the right-most word in the set state when referencing the double-word registers within the Job Accounting Feature. Finally bit 15 in the clear state shall specify the Write Restriction bits and in the set state shall specify the Read Restriction bits when referencing the Protection Matrix. For all cases just described in which bits 11 through 14 are unused, and for all cases in which bits 11 through 15 are unused, they shall be referred to as being in the clear state for the purpose of hexadecimal notation.

Number 882000 ENGINEERING SPECIFICATION Sheet of 51 Equipment Group 3.3.1 Relocation and Protection Feature The Relocation and Protection feature shall expand the Main Storage Address capabilities of the 7300 Processor. from 65,536 bytes to 1,048,576 bytes. In addition, this feature shall provide the facilities for dynamically performing Main Storage Address relocation and Main Storage protection on a Processor State basis. The expansion of Main Storage Addresses shall be a. accomplished for Processor States 0 through 7 through the implementation of a Segment Tag File containing 256 4-bit entries. These 4-bit values, referred to as Segment Tags, shall serve as left-most extensions to each of the corresponding 256 16-bit registers comprising the Basic Register File within the CPU. The 20 bit Main Storage Address thus provided shall be referred to as the System Address. Address expansion shall be accomplished with respect to 7300 Console operations by means of Segment Tag additions to the associated CA and CD Registers. Likewise, a Segment Tag addition shall be provided for the PE Register such that a 20-bit Main Storage Address may be recorded during each Main Storage reference for which a Main Storage Parity Error Trap occurs. For purposes of performing relocation and protection, the System Address shall be divided such that the left-most 4-bits shall represent a Segment Tag and the right-most 16-bits shall represent a Displacement. This 16-bit Displacement shall be further divided, into bytes, such that the left-most 8-bits shall be referred to as a Page Displacement and the right-most 8-bits shall be referred to as a Byte Displacement. The Byte Displacement shall not participate in Main Storage Address relocation and Main Storage protection operations. Relocation shall be performed on a Main Storage page Ь.

Relocation shall be performed on a Main Storage page basis for which each page shall consist of 256 bytes. (Thus, Physical Main Storage Addresses shall be capable of expressing 4096 pages). Relocation shall be accomplished through the implementation of a Segment Relocation Table containing 16-24-bit entries in a 32bit format for which 8 bits shall be defined as being in the clear state. The 4-bit Segment Tag portion of the 20-bit System Address described in item a, shall be used to reference 1 of the 16 entries in the Segment Relocation Table. The Page Displacement Portion of the 20-bit System Address shall be added (right-justified, zeroes extended) to the right-most 12-bit output of the Segment kelocation Table.

			್ಯಾತ್ ಕಾರ್ಯಕ್ರಮಕ್ಕೆ ಮತ್ತು ಮತ್ತು ಸ್ಥೇತ್ರ.	NUMBER OF STREET OF		and the second	an a
	MEMOR	NEX	ENGINEERI	NG SPECIFICA	TION	Number Shad	882000
	Equipment C	Group	e corage f	er Which dea	P. Baal Ric . e.	Short []]	51: been
	C. C.	Thus, a to Main perform operati designa of a ma see 3, 3 checks Storage checks in each hardwar page nu of each Page Di by mean Write m Matrin For cla accompa violati trap se end of states has bee 0 throu Storage	a 20-bit Phy Storage fo ed for the ons shall b tion of 1 o ximum of 25 .1.2., and it Protection of performia involving th Segment Re e checks in mber (also Selaret Re splace. It sof haru, estriction 1 on a Anoces rification, 1 on a Anoces rification, 1 on a Anoces rification, 1 on through 12. n performed gho7, furthe Addressing Pero-command	sical Address rwhich dynam left-most 12-1 e based on the f 16 Main Sto 6 pages each. s accompanying shall be accompanying shall be accompanying shall be accompanying shall be accompanying shall be accompanying state accompanying location rable of relocation location rable of relocation rable of signated will boation of the schecks invo- state and see 3.3.1.2 a ans All Mai tected, shall inol Storage A major cycle a once the ha for the assoc t operations violation sha t control begi 016.	shall ic relo bits e Syste g diagr omplish by me it cont e entry omparis thin, the e system olving l within Segmen and 3.3 in Stor result ddress allocate indware iated I relation	be pro cation These m Addr clarif cla	Jin peen Vided has been relocation ess comprised ication in the berdware left most hardware hardware hardware hardware hardware hardware hardware hardware hardware hardware hardware hardware hardware he maximum most vorc the maximum hotection dand if and if an
	а 	Main St shall n	orage_protec	tion during C leftion operation recessor State	Console fions si basis	State	operations
	d.	Relocat conditi of ian A loshit relocat	datess-fode iom and -prog oned on a Bi ddress flade Address Mode ion nor prot	Register. The Register shares for the second	ie contra jons sh basis ie contra ill spectation co	by meants of hall.be by meants of ify;ne only, o	the ther fs the the ther r
		Velhcat Statete State of Witheres Registed State of means of describe	ion and prot brough 7 perations in fpeks torrel rafunction s perations in f the Consol ad in 3 10 3	ection fornea volvide Main ocation contr hall be accom volving Main e Main Storag	sora Sora ols, the plished Storage e, Reloc	Lor C Addre Addre For C refer ate/Of	Processor ences by solution phones by ences by f switch
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·	Equipment Group	ENGINEERING SPECIFICATION	Sheet 53 of					
	3.3.1.1 Segment Ta	gs						
	259 Segmer Relocation 4-bit, let shall be u described Segment Ta	t Tag Registers shall be provided and Protection Feature, not inc t-most extension to the S Registen nder Load S Micro-command contro in 3.8.5.1 for the purpose of acc g values.	d by the luding the er which l as commodating					
	a. The Se Regist regist	gment Tag File shall consist of 2 ers with one-for-one corresponder ers within the Basic Register Fil	256 4-bit nce to the le.					
	During in whi the Se Micro- as des Micro- Regist Segmer 3.8.5. commar Regist of the approp File, associ X00X16 Micro-	each minor cycle associated with ch a Register Option reference is gment Tag File shall be addressed commands identically to the Basic cribed in 3.8.1.1, item c. Morec commands shall be implicitly capa er File read and write references t Tag File shall participate as of 1 and 3.8.5.7. Likewise, all For ds which perform write references er File, shall implicitly transfe 4-bit S Register Segment Tag Ext riate register number within the whenever Micro-command execution ated major cycle begins at Contro , (RNI), or when immediately prec command as described in 3.8.5.7.	n a major cycle s not performed, d by Format 1 c Register File over, Format 1 able of performing s in which the described in rmat 1 Micro- s to the Basic er the contents tension to the Segment Tag for the ol Storage Address ceded by an IDX					
	During refere be add most 1 hexade Proces	each major cycle for which a Reg nce is performed, the Segment Tag ressed according to the contents 5 bits of the S Register using th cimal notation: Sor State Register Num	gister Option g File shall of the right- ie following					
	FIUCES	sol state Register Au						
		$\begin{array}{cccccccccccccccccccccccccccccccccccc$)1F)3F)5F)7F)9F)BF)DF)DF					

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MEMOR	DIEV			ľ	lumber	882000	
Equipment	Group	ENGINEERIN	g specificat		Sheet	54	
	With re write r make us positio referen zeroes 12 bit 4 bit p	spect to 16-b eferences to e of the outp ns of the D R ces from the to the D Fan- positions, Se ositions.	it data paths the Segment T uts from the egister and F Segment Tag F In Network in gment Tag dat	5, Regis Fag File right-r Register File sha the le ta to th	ster e sha nost r Opt all t eft-m ne ri	Option 11 only 4 bit ion read ransfer ost ght-most	
b.	The CA a Console and 3.10	nd CD Segment ' controls to 0.3.5, respec	Tag Registers the extert de tively.	shall scribed	be s l in	ubject to 3.10.3.2	÷
	Implici registe for imp in 3.10 include	t Micro-comman rs shall be 1 lementation of .3.11, item incremental	nd control of imited to the f the Console d, f, and capabilities.	these extent operat g, and	Segme t required tions shal	ent Tag uired described 1 not	
	The mean under Mi CA and G	ns for perform icro-command CD Segment	ning Register control shall Tag Registers	Option not be	refe prov	erences vided for 1	the
с.	The PE S to the H to Micro hardward	Segment Tag Re PE Register de o-command cont e controls.	egister shall escribed in 3 trolled write	operat .2.3.4 refere	e ide with nces	entically respect and all	
	The PE S command reference Register such ref describe zeroes i Tag data	Segment Tag Re control only ces for which r are equal to ferences shall ed for the Seg in the left-mo a in the right	egister shall by means of the right-mo 0 040016. Th conform to gment Tag Fil ost 12 bit po c-most 4 bit	be rea Registe st 16 b e data that pr e in it sitions positio	d und r Opt its of forma eviou em a, , Seg ns.	der Micro- tion read of the S at for usly namely, gment	
					. •		
					•) - -
							• •



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a. For the p tion and the conte shall be	Main Storage protection on a se ents of each entry in the Segmen specifically utilized as follow	ge Add gment, t Relo s:	iress reloca- /page basis, ocation Table
When the cleared s Bits 08 t Page Disp Storage A	"V" designator (Word 0, Bit 00; state or when the "Maximum Page" through 15) is exceeded in value placement portion of the System Addressing violation shall be de	valio fielo (unsi Addres tecteo	lity) is in the 1 (Word 0, Igned) by the ss, a Main 1.
The Reloc be added of the Sy the Physi Relocatio right-jus	ation Constant (Word 1, Bits 04 in 2's complement to the Page D stem Address to provide the lef cal Address. (With respect to on Consult, the Page Displaceme stified, with reconstance.).	throu isplac t-most the 12 nt sha	agh 15) shall cement portion t 12 bits of 2-bit allbe added
The "P", 03) along 04 throug unused.	"U", and "L" designators (Word with the two fields of zeroes h 07 and Word 1, Bits 00 throug	0, bit (Word h 03)	ts 01 through 0, Bits shall be
b. For the p under Mic shall be Register SEGMENT R Double Wo	arpose of performing Register 0 ro-command control, the Segment addressed by the right-most 16-1 according to the following hexa ELOCATION TABLE REGISTER NUL rd Entry Word 0 / N 0 0200 / N 1 0202 / N 2 0204 / N 3 0206 / N 4 0208 / N 5 020A / N 6 020C / N 7 020E / N 8 0210 / N 9 0212 / N A 0214 / N B 0216 / N 0218 / N 0214 / N	Reloc Reloc bits c decima MBER Word 1 0201 0203 0205 0205 0207 0209 0208 0200 0205 0207 0209 0208 0207 0209 0205 0207 0209 0205 0207 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0205 0205 0205 0205 0205 0207 0201 0201 0201 0201 0201 0201 0205 0205 0205 0205 0205 0205 0207 0201 0201 0201 0201 0201 0201 0205 0205 0205 0205 0205 0205 0205 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0205 0205 0205 0205 0205 0205 0205 0205 0205 0205 0205 0205 0205 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0201 0205 0205 0205 0205 0211 0215	ation Table of the S 1 notation:
The Segme in"fields Word 1, B erences w within th these fie for these performed	E 021A / (021C / (021E / (nt Relocation Table shall not be of zeroes"positions (Word 0, Bi its 00 through 03) and Register hich transfer non-zero values to e Segment Relocation Table shall lds. Likewise, zeroes shall alw fields when Register Option rea from the Segment Relocation Tab	21D 21F phys t 04 Option thes have vays b d ref	ically present through 07 and n write ref- e bit positions no effect on e obtained erences are

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b. For the purpose of performing Register Option references under Micro-command Control, the Protection Matrix shall be addressed by the right-most 16 bits of the S Register according to the following hexadecimal notation.

Processor	State		Regist	er Numb	er
		Write	Restrictio	on/Read	Restriction
0			01	00/0101	
1			01	20/0121	
2			01	40/0141	
3			010	50/0161	
4			01	80/0181	ter ter anna an tha
5			01/	A0/01A1	
6		and the second	010	CO/01C1	
7 · · · · · · · · 7			011	E0/01E1	

3.3.1.4 Address-Mode Register

The Address Mode Register shall consist of 16-bits and shall provide the means for conditioning dynamic relocation and protection operations on a Processor State basis.

The Address-Mode Register shall contain an "R" designator bit for each Processor State, 0 through 7, in the left-most byte and a "D" designator bit for each Processor State, 0 through 7, in the right-most byte in the following format.

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
"R" Designators							יםיי	' De	esi	gnat	tors	5				

During each Main Storage reference on the part of Processor States 0 through 7 the appropriate " \mathbb{R} " and "D" designators shall be hardware interpreted for the associated Processor States as follows:

- a. When the "R" designator is clear, neither relocation nor protection shall be performed. The 20-bit System Main Storage Address shall be used directly as the Physical Main Storage Address. The detection of Main Storage Address violations shall have no effect.
- b. When the "R" designator is set and the "D" designator is clear, dynamic Main Storage Address relocation shall occur. The 20-bit System Address shall be converted to a 20-bit Physical Address as described in 3.3.1.2. The detection of Main Storage Address violations shall have no effect except when the "V" designator is clear for the associated Segment Relocation Table entry in which case a hardware trap sequence shall be performed and Main Storage write operations shall be disabled.

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	ent Group	ENGINEERING SPECIFICAT	ION Sheet	59 01
	c. When th Main St detecti result write o	e "R" and "D" designators orage Address relocation s on of any Main Storage Add in a hardware trap sequenc perations disabled.	are both set hall occur a ress violati e with Main	, dynamic nd the ons shall Storage
	The Add Micro-c Option of the	ress-Mode Register shall b ommand control only by mea references for which the S Register are equal to 03	e referenced ns of Regist right-most 1 00 ₁₆ .	under er 6-bits
	The con cleared	tents of the Address Mode by System Reset as descri	register sha bed in 3.10.	11 be 3.8.
3.3.2	Basic Stora	ge Protection Feature		
	The Basic S bit registe provide the protection, Processor S provided on 256 bytes e	torage Protection Feature rs, referred to as Bounds means for accomplishing d during write references of tates 5, 6, and 7. This p the basis of Main Storage ach.	shall consis Registers, a ynamic Main nly, on the rotection sh pages consi	t of 3 16- nd shall Storage part of all be sting of
	a. Each of States	the 3 Bounds Registers as 5, 6, and 7 shall be forma	sociated wit tted as foll	h Processor ows:
	00 01	02 03 04 05 06 07 08 09 10	11 12 13 14	15
	Upp	er Bounds L	ower Bounds	
	The Upp Storage designa	er Bounds field shall desi page number and the Lower te a minimum Main Storage p	gnate a maxi Bounds fiel page number.	mum Main d shall
	When the Storage Storage Processe Registe be disa the asse	e Upper and Lower Bounds f write references shall be page as performed on the p or State. When the conten r are equal to FF00 ₁₆ , Main bled for write references p ociated Processor State.	ields are eq confined to part of the ts of any Bo n Storage properformed on	ual, Main that Main associated unds otection shall the part of
	b. During the part the app left-mos Registes field of Address	each Main Storage write re- t of Processor States 5,6, ropriate bounds Register sh st 8 bits (page number) cor r are greater than the asso r less than the Lower Bound ing violation shall be dete	ference, per and 7, the nall be read ntained in the ociated Upper is field, a here ected. A Ma	formed on contents of . When the he S r Bounds Main Storage in Storage
	Address hardware at the e	ing violation thus detected e trap sequence (Control St end of the major cycle and	d shall resu torage Addres shall disab	lt in a ss X010 ₁₆) le the
			•	
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	NREY			Number	88200 0
	ent Group	ENGINEERING	SPECIFICATION	Sheet 60	fo
	Main St sequent State 5	corage write ref te has been perf 5, 6, or 7, the	erence. Once to ormed for the a Main Storage Ac	the hardwa associated ldressing	re trap Processor violaticn
	shall b beginni	e considered to ing at Control S	tally under Mic torage Address	x010 ₁₆ .	d control
	c. For the under M be addr accordi	purpose of per licro-command co essed by the ri ng to the follo	forming Registent ntrol, the Bound ght-most 16 bit wing hexadecime	er Option ids Regist is of the il notation	references ers shall 5 Register h:
	Process	or State	Register N	lumber	
		5 6 7	0 5 A 0 0 5 C 0 0 5 E 0)	
3.3.3	Job Account	ing Feature		• .	
	The Job Acc correspondi provide the allocated t	ounting Feature ng to Processor means for acco o these process	shall consist States 0 throu unting for all or states on an	of 8 32-bi ngh 7 and s major cycl individua	it registers shall les sl basis.
	a. During 0 throu Account during Feature	ing Register sh Register Option itself.	e allocated to nts of the appr all be increase references to	the Job Ac	b except counting
	b. For the under M shall b Registe notatio	purpose of per licro-command con- e addressed by r according to n:	forming Registe ntrol, the Job the right-most the following h	r Option a Accounting 16-bits of exadecimal	eferences Registers the S
	Job Acc Pro	ounting Registe cessor State	r Regis Word	ter Number 0 / Word 1	•
		0 1 2 3 4	06 06 06 06 06	00 / 0601 20 / 0621 40 / 0641 60 / 0661 80 / 0681	
		5 6 7	06 06 06	A0 / 06A1 C0 / 06C1 E0 / 06E1	

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	When the Job Accounting feature is addr command control for the purpose of perf Option write references, the entire 32- left-most 16-bits and Word 1, right-mos cleared within the appropriate Job Acco regardless of the Word 0/Word 1 designa S Register) and irrespective of the co Register.	essed under Micro- orming Register bit contents (Word 0, t 16-bits) shall be unting Register tion (Bit 15 of the ntents of the D
3.3.4	ECC Feature (Register Set)	
	The Register Set associated with the EC of 4 16-bit quantities for which the fo are described by the applicable documen	C Feature shall consi rmat and function t listed in 2.1.
	ant from the CDH for the mensors of the	ncforming the
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register	nsferring the Storage to the CPU. r shall address the read references notation. Numbers
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register Main Storage Data Register 0800 Log Register 0400	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0800
	set from the CPU for the purpose of traassociated 16-bit quantities from Main SThe right-most 16-bits of the S RegisteECC Register Set during Register Optionaccording to the following hexadecimalECC Register SetRegister SetMain Storage Data RegisterLog RegisterOA00Generated Check BitsOE00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0B00 or 0D00 or 0F00
	set from the CPU for the purpose of traassociated 16-bit quantities from Main SThe right-most 16-bits of the S RegisteECC Register Set during Register Optionaccording to the following hexadecimalECC Register SetRegister SetMain Storage Data RegisterLog RegisterOA00Generated Check BitsOE00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0B00 or 0D00 or 0F00
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register Main Storage Data Register 0800 Log Register 0A00 Generated Check Bits 0C00 Read Check Bits 0E00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0B00 or 0D00 or 0F00
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register Main Storage Data Register 0800 Log Register 0A00 Generated Check Bits 0C00 Read Check Bits 0E00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0B00 or 0D00 or 0F00
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register Main Storage Data Register 0800 Log Register 0A00 Generated Check Bits 0C00 Read Check Bits 0E00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0800 or 0000 or 0F00
	set from the CPU for the purpose of tra associated 16-bit quantities from Main S The right-most 16-bits of the S Registe ECC Register Set during Register Option according to the following hexadecimal ECC Register Set Register Main Storage Data Register 0800 Log Register 0A00 Generated Check Bits 0C00 Read Check Bits 0E00	nsferring the Storage to the CPU. r shall address the read references notation. Numbers or 0900 or 0B00 or 0D00 or 0F00

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Fauina	nent (Group

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3.4 ALU

The Arithmetic Logic Unit (ALU) shall consist of those registers and logical networks required for implementation of the Micro-command repertoire.

3.4.1 Au Register

The Au Register shall consist of 16-bits, designated 00 through 15 from left to right. During operations with signed magnitudes, the left-most bit, 00, shall be treated as the sign bit position.

a. The Au Registrr shall accommodate the following inputs:

Register File (True and 1's complement states) Shift Network (Left-most output, 16 bits) Bit Sense (1 of 16 code) D Fan-In Network (True and 1's complement states)

b. The Au Register shall provide outputs to the following:

Shift Network (Left-most input, 16 bits) Bit Sense (Bit multiplex and bit scan) ALU Fan-In Network (Direct) ALU Fan-In Network (Additively combined with Bu) ALU Fan-In Network (Logically combined with Bu) Compare (Compared with Bu and with zero)

The Au Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d.

The Au Register shall be set by means of the Console control described in 3.10.4.20, item a.

The contents of the Au Register shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7. Bu Register

3.4.2

The Bu Register shall consist of 16 bits, designated 00 through 15 from left to right. During operations with signed magnitudes, the left-most bit, 00, shall be treated as the sign bit position.

a. The Bu Register shall accommodate the following inputs:

Register File (True and 1's complement states) Shift Network (Right-most output, 16 bits) Bit Sense (Bu Adder) Constant Generator

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b. The Bu	Register shall provide outputs	to the following:
Shift Bit Se ALU Fa ALU Fa ALU Fa Compar	Network (Right-most input, 16 bit nse (Bu Adder) n-In Network (Direct) n-In Network (Additively combine n-In Network (Logically combined e (Logically and Algebraically w	s) d with Au) with Au) ith Au)
The Bu of a S	Register shall be cleared by th System Reset as described in 3.10	e occurrence .3.8, item d.
The Bu contro	Register shall be set by means 1 described in 3.10.4.20, item b	of the Console •
The co at the select 3.10.3 3.4.3 Force Carr	ntents of the Bu Register shall Console Data Register Display i ed by means of the Console Contr 5.7. y Register	be available ndicators when ol as described in
The Force accommodat Micro-comm Register s bit, 15, o	Carry Register shall consist of ing set, clear and Link Status B and control. The output from th hall serve as a carry input to th f the Adder described in 3.4.5.	a single Flir/Flor it inputs under he Force Carry he right-most
The Force of a Syste	Carry Register shall be cleared I m Reset as described in 3.10.3.8	by the occurrence , item d.
The Force carry inpu set state Console con	Carry Register shall not be set, t to the Adder it shall appear to during the simultaneous selection ntrols as described in 3.10.4.20	but at the o be in the of the , item c.
3.4.4 Inner Carry	y Register	
The Inner carry inpu Adder shal 0, 1, 2, an propagated These groun transferred the execut 3.8.4.8.	Carry Register shall consist of a ts from the Adder only. These in 1 consist of group carry signals and 3 corresponding to carries ger through bits 00, 04, 08 and 12 m o carry signals from the Adder sh d (clocked) to the Inner Carry Re ion of DSUM Micro-commands as des	4 Flip/Flops with puts from the designated merated from or respectively. hall be egister during scribed in
The outputs individual such a way inputs to t Micro-comma	s from the Inner Carry Register s ly translated within the Constant as to provide corresponding n/bl the Bu Register as described for and in 3.8.7.6.	shall be t Generator in L (4-bit group) the CORC

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3.4.5 Adder

The Adder shall consist of an additive network for arithmetically combining the contents of the Au and Bu Registers. The Adder shall also accommodate the output of the Force Carry Register as a carry input to the right-most bit position, 15.

The inner carry mechanism within the Adder shall be based on 4-bit groups providing carry translations to the inputs of the Inner Carry Register. Likewise, the inner carry mechanism shall accommodate a disabling input such that inter-group carry inputs shall be in the cleared state only, following the execution of DIG and CORC Microcommands as described in 3.8.7.5 and 3.8.7.6, respectively.

The output of the Adder sn. 1 be available to the ALU Fan-In Network for selection during write references to the Register File under Micro-command control.

The output of the Adder shall be available at the Console Data Register Display indicators when selected by means of the Console Control as described in 3.10.3.7.

3.4.6 Shift Network

The Shift Network shall provide the means for implementing the Shift class of Micro-commands described in 3.8.8.

Within two minor cycles, the Shift Network facilities shall be capable of selecting a Shift-count, performing a 2's complement of the shift count as Micro-command designated, and shifting the 32-bit combined contents of the Au/Bu Registers 0 to 15₁₀ places left, end-off, zeroes inserted.

3.4.7 ALU Status

ALU Status facilities shall consist of the means for translating Overflow, Link and Au Register comparison conditions.

3.4.7.1 Overflow

Overflow status shall be transferred to the Su Register, bit 00 position, by means of SUM and DSUM Micro-commands as described in 3.8.4.7 and 3.8.4.8, respectively.

Overflow shall be defined as occurring whenever the contents of the Au and Bu Registers have the same sign, but produce at the output of the Adder an oppositely signed Sum; Augo \neq Sum₀₀ and Sum₀₀ \neq Bu₀₀.



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3.4.8	Bit Sense	
	Bit sense logic within the ALU shall provi for testing the contents of the Au Registe command control relative to the state of a bit position (bit multiplex) or with respe to right search (bit scan) in which case t scanning Au shall result in an addition to of the Bu Register.	de the means r under Micro- in individual ect to a left the result of the contents
3.4.8.1	Au Bit	•
	The output of the Au Register shall be bit the purpose of implem_ring the SKB and SK described in 3.8.10.3 and 9 10.4, respec	multiplexed for B\ Micro-commands tively.
3.4.8.2	Au Scan	
	The output of the Au Register shall be sca scan result encoded for the purpose of imp Bit Sense class of Micro-commands describe	nned and the lementing the d in 3.8.9.
3,4.8.3	Bu Adder	
	The Bu Adder shall provide the means for a of the Au scan operation to the contents o Register. According to the first bit posi Au as described in 3.8.9, the following va hexadecimal notation shall be correspondin the contents of the Bu Register.	dding the result f the Bu tion sensed in lues in gly added to
	Au Bit Position Detected Bu Add	end
	01 0001 02 0002 03 0003 04 0004 05 0005 06 0006 07 0007 08 0008 09 0009 10 0000 12 000C 13 000D 14 000E 15 000F	

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3.4.9 Con	istant Ge	nerator			
The the of Mic	Constan Bu Regi Micro-co ro-comma	t Generator shall ster as required b nmands described in nds described in 3	provide immedi y the Immediat n 3.8.7 as wel .8.5.1.	ate opera e Opera 1 as th	erands to and class ne Load S
3.4.10 ALU	Fan-In	Network			
The ALU Mic NuJ for Reg des	ALU Fan J data to ro-comma 1 State, selectin ister Di cribed in	-In Network shall be transferred to nd control. Durin the ALU Fan-In Ne ng ALU data to be splay indicators un 1 3.10.3.7.	the Register the Register g major cycles twork shall pr transferred to der Console s	ans for File un alloca covide to the Co witch c	r selecting ider ated to the the means onsole Data control as
The pro	output vide the	of the ALU Fan-In ! following:	Network shall	selecti	vely
Au Bu D F D F D F Sum Exc Inc Log Com ALU Zer	Register Register an-In Net an-In Net of Au ar lusive On lusive On ical Proc pare Stat Status o oes	twork (Full Word) twork (Byte 0) twork (Byte 1) ad Bu of Au and Bu of Au and Bu luct of Au and Bu tus of Au and Bu (1) of Overflo, and Lir	left-most byte ak (left-most) byte)	
3.4.11 S R	egister				
The Mai	16-bit S n Storage	Register shall pre- and the Register	ovide the mean Option.	ns for	addressing
The Reg in	input to ister Fil 3.8.5.1.	the S Register sh e under Load S Mic	all be provid ro-command co	ed from ntrol a	the s described
The Sto Pro In for ite Reg Con	output f rage by w tection f addition, Breakpoi m a, and ister Dis sole cont	rom the S Register ay of the Register eature or Relocati the output of the nt stop operations shall be available play indicators wh rol as described i	shall be pro Option, (Bas on and Protec S Register sl as described to the Conso en selected by n 3.10.3.4.	vided t ic Stor tion Fe hall be in 3.1 le Addr y means	o Main age ature). used 0.3.13, ess of the
In the as	the prese S Regist described	nce of the Relocat er shall be left-π in 3.3.1.1.	ion and Prote lost extended l	ction F by 4 bi	eature, t positions
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UVIL_UVIL_VIL_ANENGINEERING SPECIFICATIONJavet 68 eff3.4.12D RegisterThe 16-bit D Register shall provide the means for transferring data to Main Storage and the Register Option.The io-bit D Register shall be provided from the Register File under Micro-command control.The only from the D Register shall be provided to Main Storage by way of the Register Option, (Basic Storage Protection Feature). During Main Storage references purforming partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the left- most byte position as 2-*cribed in 3.8.5.4.In addition the output of the J Register shall be provided to the D Fan-In Network.Micro-command states in the Storage such that the right-most byte shall be duplicated in 3.8.5 and 3.8.6, including timing constraints.The D Register shall be set by means of the Console controls described in 3.10.3.8, item d.The contents of the D Register (by way of the D Fan-In and ALU Pan-In Network)The One dister Shall be set by means of the Console controls described in 3.10.4.20, item c.The contents of the D Register of the D Fan-In and ALU Pan-In Network)The Solution way of the D Fan-In and ALU Pan-In NetworkThe Contents of the D Register of the Solution, and the D Register ball be available at the Console control as described in 3.10.3.7.3.4.13D Fan-In NetworkThe Contents of the A Register and the All Pan-In Network, <th></th> <th>AREY</th> <th>Number 882000</th>		AREY	Number 882000
 3.4.12 D Register The 16-bit D Register shall provide the means for transferring data to Main Storage and the Register Option. The input to the D Register shall be provided from the Register File under Micro-command control. The output from the D Register shall be provided to Main Storage by way of the Register Shall be provided to Main Storage by way of the Register option, (Basic Storage Protection Feature). During Main Storage references performing partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the leftmost byte position as*cribed in 3.8.5.4. In addition the output of the J Register shall be provided to the D Fan-In Network. Micro-commands related to the D Register are described in 3.8.5 including timing constraints. The D Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d. The D Register shall be cleared by the ocnole controls described in 3.10.4.20, item c. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Diplay indicators when selected by means of the Console control as described in 3.10.3.7. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5.4. 		ent Group	Sheet of
 The 16-bit D Register shall provide the means for transferring data to Main Storage and the Register Option. The input to the D Register shall be provided from the Register File under Micro-command control. The output from the D Register shall be provided to Main Storage by way of the Register Option, (Basic Storage Protection Feature). During Main Storage references performing partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the leftmost byte position as 1.5 cribed in 3.8.5.4. In addition the output of the J Registers shall be provided to the D Fan-In Network. Micro-commands related to the D Register are described in 3.8.5 and 3.8.6, including timing constraints. The D Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register to the Au Register and the ALU Fan-In Network. J Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. J Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 	3.4.12	D Register	
 The input to the D Register shall be provided from the Register File under Micro-command control. The output from the D Register option, (Basic Storage Protection Feature) or Relocation and Protection Feature). During Main Storage references preforming partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the leftmost byte position as 2-scribed in 3.8.5.4. In addition the output of the D Register are described in 3.8.5 and 3.8.6, including timing constraints. The D Register shall be set by means of the Console controls described in 3.10.3.8, item d. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Network) shall be available at the Console Data Register to the ALD Fan-In Network. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the ALU Fan-In Network. In addition, the output of the D Fan-In Network. In addition, the output of the D Fan-In Network. In addition, the output of the D Fan-In Network. In addition, the output of the D Fan-In Network. In addition, the output of the D Fan-In Network. In addition, the output of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network output). 		The 16-bit D Register shall provide the me data to Main Storage and the Register Option	ans for transferring on.
 The output from the D Register shall be provided to Main Storage by way of the Register Option, (Basic Storage Protection Feature). During Main Storage references performing partial (byte) write operations under Micro-command control, the output from the D Register shall be sent to Main Storage such that the right-most byte shall be duplicated in the leftmost byte position as 2~cribed in 3.8.5.4. In addition the output of the J Registers shall be provided to the D Fan-In Network. Micro-commands related to the D Register are described in 3.8.5 and 3.8.6, including timing constraints. The D Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d. The D Register shall be set by means of the Console controls described in 3.10.4.20, item c. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the AlU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Addressi mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 		The input to the D Register shall be provi Register File under Micro-command control.	ded from the
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 Micro-commands related to the D Register are described in 3.8.5 and 3.8.6, including timing constraints. The D Register shall be cleared by the occurrence of a System Reset as described in 3.10.3.8, item d. The D Register shall be set by means of the Console controls described in 3.10.4.20, item c. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 		In addition the output of the D Registers s to the D Fan-In Network.	shall be provided
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 The D Register shall be set by means of the Console controls described in 3.10.4.20, item c. The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 		The D Register shall be cleared by the occu System Reset as described in 3.10.3.8, it	urrence of a tem d.
 The contents of the D Register (by way of the D Fan-In and ALU Fan-In Networks) shall be available at the Console Data Register Display indicators when selected by means of the Console control as described in 3.10.3.7. 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 		The D Register shall be set by means of the controls described in 3.10.4.20, item c.	e Console
 3.4.13 D Fan-In Network This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift-count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5. 		The contents of the D Register (by way of and ALU Fan-In Networks) shall be available Data Register Display indicators when select Console control as described in 3.10.3.7.	the D Fan-In e at the Console cted by means of the
This 16-bit fan-in shall provide the means for transferring data from Main Storage, the Register Option, and the D Register to the Au Register and the ALU Fan-In Network. In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift- count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5.	3.4.13	D Fan-In Network	
In addition, the output of the D Fan-In Network shall be provided to the Shift Network for selection as a shift- count (Bits 12 through 15) and shall be provided to the Address Table addressing mechanism, in lieu of Su, for the purpose of executing FRJ Micro-commands (Bits 00 through 08 and bit 12 of the D Fan-In Network output). Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5.		This 16-bit fan-in shall provide the means data from Main Storage, the Register Option Register to the Au Register and the ALU Fan	for transferring 1, and the D 1-In Network.
Timing constraints with respect to hardware control of the inputs to the D Fan-In Network are described in 3.8.5.		In addition, the output of the D Fan-In Net provided to the Shift Network for selection count (Bits 12 through 15) and shall be pro Address Table addressing mechanism, in lieu for the purpose of executing FRJ Micro-comm 00 through 08 and bit 12 of the D Fan-In Ne	twork shall be a as a shift- ovided to the of Su, nands (Bits etwork output).
		Timing constraints with respect to hardware of the inputs to the D Fan-In Network are d	e control lescribed in 3.8.5.
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3.5	Control Sto	orage	
	Control Sto referred to	rage shall be divided into two as Control Storage proper and	functional areas the Address Table.
	Control Sto Micro-comma hardware co	rage proper shall provide the nds to be read, translated and ntrol.	means for storing executed under
	The Address Control Sto may perform purposes.	Table shall provide the means rage Addresses such that FRJ M high speed branch operations (See 3.8.11.2).	for storing licro-commands for decoding
	All Control performed f command exe 7300 Proces operations, from the Co Read and Co in 3.10.3.1	Storage references, read and or purposes not directly relat cution shall be associated wit sor maintainability and availa performed under hardware cont nsole, shall be referred to as ntrol Storage Write operations 1, items h and i, respectively	write, which are ed to Micro- h provisions for bility. Such rol as initialized Control Storage as described
3.5.1	Su		
	The Su Reginal addressing not involvin Storage Rea the Su Reginal addressing	ster shall provide the only me Control Storage proper. Durin ng Micro-command execution, (n d and Control Storage Write, C ster shall provide the only me the Address Table.	ans for directly g all operations amely, Control onsole operations), ans for directly
	a. During have th by the selecte	Micro-command execution, the S e following format and shall b Console Address Register Displ d according to 3.10.3.4.	u Register shall e displayed as such ay indicators when
	00 01 0	2 03 04 05 06 07 08 09 10 11 1	2 13 14 15
	0 L	CONTROL STORAGE PROPER, ADD	RESS
		ink (See 3.4.7.2)	
	Over	flow (See 3.4.7.1)	
· · · · ·			

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b. Durin have descr is no Regis	g Micro-command execution, the Su the following format for Breakpoin ibed in 3.10.3.13, item b, provide t selected as the input to the Con ter Display indicators.	Regist nt purp ed the nsole A	er shall oses as Su Register ddress
00 01	02 03 04 05 06 07 08 09 10 11 12	13 14	15
0 0	CONTROL STORAGE PROPER,	ADDRES	S
c. During State Contro forma	g Control Storage references perfo for the express purpose of readin of Storage, L- Su Register shall t and Micro-comm. 4 execution shall	ormed b ng or w have t ll be e	y the Console riting he following xcluded.
00 0	02 03 04 05 06 07 08 09 10 11 12	2 13 14	15
ER AT	7	· · · · ·	
	ADDRESS TABLE ADDRES	SS	- N
	.0: Control Storage Proper		
	1: Address Table		
Bun the	est Check Error indication, when s termination of a Deadstart Seque	et fol ence.	lowing
Control St command ex States and constants	corage proper shall be addressed s ecution shall begin, for the appr l under the designated conditions, as follows:	opriate at the	at Micro- e Processor e address
a. Contro addres notati in a c genera	ol Storage proper shall be referrences of the set of th	d to as hexade 1 be de be hard 10.4.18	s RNIO at ecimal esignated lware 8.
b. Contro at add notati in a c genera 3.8.11	ol Storage proper shall be referre lresses 0002, 1002, 2002 and 3002 on. These address constants shal combined form as X002 ₁₆ and shall ted under Micro-command control a .5.	d to as in hexa 1 be de be expl s desci	s RNI1, adecimal esignated licitly ribed in

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- c. Control Storage proper shall be referred to as RNI2 at addresses 0009, 1009, 2009 and 3009 in hexadecimal notation. These address constants shall be designated in a combined form a X009₁₆ and shall be explicitly generated under Micro-command control as described in 3.8.11.6.
- NOTE: The RNIO, RNII and RNI2 addresses shall be hardware translated at the beginning of each major cycle for Breakpoint purposes as described in 3.10.3.13 through 3.10.3.17, for Stop/Step operations as described in 3.10.3.18, and for implicit Segment Tag write transfers as described in 3.3.1.1, item a.
- d. Control Storage proper shall be referenced during Illegal Address trap sequences at addresses 0010, 1010, 2010, and 3010 in hexadecimal notation. These address constants shall be designated in a combined form as X010₁₆ and shall be hardware generated as a result of Main Storage Address violations detected and enabled as described in 3.3.1 and 3.3.2.
- Control Storage proper shall be referenced during Main е. Storage Parity Error trap sequences at addresses 0018, 1018, 2018, and 3018 in hexadecimal notation. These address constants shall be designated in a combined form as X01816 and shall be hardware generated for Processor States 0 through 7 as described in 3.10.4.4 with the exception that "Out of Range" addresses shall be included with the detection of Parity Errors during Main Storage read references in the absence of the ECC Feature as well as the detection of non-correctable data errors during Main Storage read references in the presence of the ECC Feature. The occurrence of all hardware controlled trap sequences to addresses X018₁₆ shall be conditioned by the state of the Storage Parity Disable switch described in 3.10.4.16. Once this trap sequence has occurred for the associated Processor State, further operations relative to the Main Storage Parity Error shall be considered totally under Microcommand control.
- f. Control Storage proper shall be referenced during Control Storage Parity Error trap sequences at addresses 0028, 1028, 2028 and 3028 in hexadecimal notation. These address constants shall be designated in a combined form as X028₁₆ and shall be hardware generated, for Processor States 0 through 7 only, as described in 3.10.4.5. Likewise, the occurrence of trap sequences to addresses X028₁₆ shall be conditioned by the state of the Storage Parity Disable switch described in 3.10.4.16. Once this trap sequence has occurred for the associated Processor State, further operations relative to the Control Store Parity Error shall be considered under Micro-command control.

			Number
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NOT	The order of precedence be: Control Storage F Error and Illegal Addu and d, respectively. not be checked when Ma are detected as descri	te for the transverity Error, la ress as describ However, Main in Storage Ad bed in 3.3.1	p sequence shall Main Storage Parity bed in items f, e, Storage Parity shal dress violations and 3.3.2.
	For items a through f of the 14-bit address designated, the value be derived identically 3.8.11, item b.	in which the constants are of the left-me to the manne	left-most 2-bits not specifically ost 2-bits shall r described in
	Trap Sequences, items cycle E7 and shall set associated Processor S control. Thus, Proces stopped at the end of trap conditions are ha operation is expected major cycle through th Busy Flip/Flop, whethe control on the part of or by means of the ass described in 3.10.3.18	d, e, and f, s the Busy Flip tate through sor States 0 any major cyc trdware detected to be achieved to be achi	shall occur on minor p/Flop for the h 7, under hardware through 7 may not be le in which such ed, when the stop d during that the associated Micro-command Processor State, le controls as
g.	Control Storage proper sh Console State operations a and g.	all be address as described :	sed at 0100 ₁₆ for in 3.10.3.11, items
h.	Control Storage proper sh Consolc State operations b and f.	all be address as described i	sed at 0103 ₁₆ for in 3.10.3.11, items
i.	Control Storage proper sh Console State operations item c.	all be address as described i	sed at 0106 ₁₆ for in 3.10.3.11,
j.	Control Storage proper sh Console State operations item d.	all be address as described i	sed at 010C, for in 3.10.3.11,
k .	Control Storage proper sh Alternate Autoload sequen in 3.10.2.4 and 3.10.2.5.	all be address ce initializat	ed at 0112 ₁₆ for tion as described
1.	Control Storage proper sh Primary Autoload initiali and 3.10.2.5.	all be address zation as desc	ed at 0113 ₁₆ for ribed in 3.10.2.4

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Equipment Gro	oup	F NGIN	IEERING	SPECIF	ICATION	Sheet	73 이	
3.5.3 Addres	s Tab	1e				с 1997 г. – Фелл	· · ·	
The Address Table shall consist of a minimum of 256 10-bit words. Address Table sizes of 512, 768, and 1024 10-bit words shall be possible on an optional basis.								
a. The con Con Mi	e 256 ntent nsole cro-c	word A s of Su State ommand	ddress as des read an executi	Table si cribed d write on.	hall be in 3.5.1 referen	address , item ces not	ed by c, dur invol	the ing ving
The ou cy de: fre in bi	The 256 word Address Table shall be addressed by the output of the D Fan-In Network for a minimum of 2 minor cycles prior to the execution of the FRJ Micro-command described in 3.8.11.2. Bits 00 through 08 and bit 12 from the D Fan-In Network shall be encoded from 10 bits into 8 address bits substituted for the right-most bits from Su as follows:							
D FAN-IN	<	S u	SUBSTI	TUTE TO	THE ADD	RESS TA	BLE —	>
00 through 07	08	09	10	11	12	13	14	15
2X, 3X, AX, BX	0	0	DF00	DF ₀₃	XB or XC-XF	XA or XC-XF	DF ₀₈	DF ₁₂
6X, 7X	0	1	0	DF ₀₃	DF ₀₄	DF ₀₅	DF ₀₈	DF ₁₂
0X,1X,4X,5X 8X,9X,CX,DX	0	1	1	DFOU	DF ₀₁	DF ₀₃	df ₀₄	DF05
EX	1	0	DF ₀₄	DF ₀₅	DF ₀₆	df ₀₇	DF ₀₈	DF ₁₂
FX	1	1	DF04	DF ₀₅	DF06	df ₀₇	DF ₀₈	DF ₁₂

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		ent Group	Sheet 7.4 ef
		The data output from the Address Table to Register Display indicators shall be in th during Console read operations.	the Console Data ne following forma
		00 01 02 03 04 05 06 07 08 09 10 11	12 13 14 15
	Parity	P 0 0 1 DF ₀₃ ADDRESS TABLE	.E DATA
		The data input to the Address Table from a Register shall be in the same format shown exception of bits 01 through 06 which shall Console write operations.	the Console Data above with the ll be unused durin
		The data output from the Address Table, the positions 04 through 15 of the The Register tion of FRJ Micro-commands, shall up approximation bit positions 04 through 15 also shown in	ransferred to bit r during the execu ond to the associa the above format.
		Horizontal parity for the Address Table, or read operations and FRJ Micro-command exect valid when the total number of bits in the for bit positions 00 and 07 through 15 on respect to the state of bits 01 through 06	during both Consol cution, shall be set state is odd by, i.e. without
14 		b. The 512 word Address Table is undefine address and data conventions at the pr	ed with respect to resent time.
		c. The 768 word Address Table is undefine address and data conventions at the pr	d with respect to resent time.
		d. The 1024 word Address Table is undefin address and data conventions at the pr	ed with respect tesent time.
	3.5.4	Control Storage, Read/Write	
		The means for performing Control Storage F Storage Write operations under hardware co provided in a manner mutually exclusive wi execution. Such operations shall be select through the use of the Console switches as 3.10.3.9 through 3.10.3.11.	Read and Control ontrol shall be th Micro-command ted and controlled described in
	3.5.5	Control Storage Read	
		The Console State shall be used to impleme Read operations under hardware control as 3.10.3.11, item h.	nt Control Storage described in
	3.5.6	Control Storage Write	
		The Console State shall be used to impleme Write operations under hardware control as 3.10.3.11, item i.	nt Control Storage described in
		Reset/Load sequences shall simulate Consol the extent described in 3.5.7.3, 3.5.8.2,	e operations to and 3.5.9.2.

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3.5.7	Reset/Load Sequence	e et al.		
	The Reset/Load Sequence shall be initiated three sources.	l from	one of	
	a. The trailing edge of Power-On System R completion of a power-up sequence.	leset a	t the	
	b. The Reset/Load Switch as described in	3.10.2	.12.	
	c. The presence of a Restart Reset/Load s in 3.5.8.5.	ignal	as described	
	The Reset/Load sequence shall consist of t described in 3.5.7.1 through 3.5.7.5.	hose o	perations	
3.5.7.1	Reset/Load System Reset			
	A System Reset shall be performed for a mi and a maximum of .6 m/s. For a descriptio of Reset Load, see 3.10.3.8.	nimum n of t	of .4 m/s he effects	
3.5.7.2	Reset/Load Pause			
	The trailing edge of System Reset shall ge of 2.5 u/s minimum to 3.5 u/s maximum, to to stabilize.	nerate allow	a pause IFA logic	
3.5.7.3	Reset/Load Initialization			•
	Upon completion of the pause, the Reset/Lo set, and force the following conditions:	ad Fli	p·Flop shall	
	a. Reset/Load Initiate, see 3.5.8.1.			
	b. Control Storage Write; this signal is and performs the same function as the Write Operation selected from the Cons This signal shall be disabled when the Maintenance Mode. Thus, Control Stora shall be selected by means of the Cons Switch only, when the Console is in Ma	in par Contro ole, (Conso ge Wri ole Mo intena	allel with 1 Storage See 3.10.3.11 1e is in te Operations de Select nce Mode.	L).
	c. Console Stop; this signal is in parall performs the same function as the Cons Select switch, Stop/Step position, (Se	el with ole Con e 3.10	h and ntrol .3.9).	
3.5.7.4	Reset/Load Data Transfer			
	a. Upon receiving the Reset/Load Initiate Integrated File Adapter or Integrated determined by the state of the Primary cribed in 3.5.8.3, shall transmit Data 3.5.8.8, and 3.5.9.8, with Data Strobe	signa Card Ad Source as de s as de	l, the dapter, as signal des- scribed in escribed	

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	b. The Reset/Load sequence shall write da Storage proper until all addresses pre written, (16,384 words maximum, 1024 w and shall then write data into the Add all addresses present have been writte maximum, 256 word increments). The si Storage proper and the Address Table m maximums of 4096 words and 256 words, means of the Select CS Minimum control 3.10.4.19.	ata into Control sent have been ord increments), ress Table until n (1024 words zes of Control ay be selected for respectively, by as described in
3.5.7.5	Reset/Load Termination	
	Termination of the Reset/Load shall be acc clearing of the Rese 'Load Flip/Flop, thro following means.	omplished by the ugh one of the
	a. Generation of the End Out Signal as de with the Load Select Switch in the Pri	scribed in 3.5.8.7, mary position.
	b. Generation of the End In signal as des with the Load Select Switch in the Alt	cribed in 3.5.9.5, ernate position.
	c. The occurrence of a System Reset.	
3.5.8	Primary Loader	
	The Primary Loader Logic shall utilize the to interface the ALU and the Integrated Fi in order to accomplish a Control Storage (Address Table) Reset/Load.	following signals le Adapter (IFA), including the
3.5.8.1	Reset/Load Initiate	
	A level from the loader logic which, in th shall indicate a Reset/Load is to be initi source specified by the state of the Disc described in 3.5.8.3.	e high state, ated from the Source signal
	The leading edge and trailing edge of this be generated by the setting and clearing, the Reset/Load Flip/Flop described in 3.5.	signal shall respectively, of 7.3.
3.5.8.2	Primary Data Strobe	
	A pulse from the IFA which, in the low stat that 16 bits of input Data are available or Source Data Lines described in 3.5.8.8.	te, shall indicate n the Primary

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This pulse shall initiate a sequence which clears the Console Data Register, strobes the Primary Source Data Lines into the Console Data Register, and generates a Console Run signal. This Run signal shall be in parallel with and shall perform the same function as, the Console Run Control described in 3.10.3.10.

See Figure 8 for timing relationships.

3.5.8.3 Primary Source

A level from the Loader Logic which, in the high state, shall indicate that the Primary Load Source is to be used for the Reset/Load.

This level shall be generated by the Load Select switch described in 3.10.2.5.

3.5.8.4 Maintenance Out

A level from the Loader logic which, in the high state, indicates the Console is being operated in Maintenance Mode.

This signal shall be generated by the Maintenance Mode Switch described in 3.10.4.1.

3.5.8.5 Restart Reset/Load

A 50 n/s minimum width pulse from the IFA which, in the low state, shall indicate that a burst check error has been detected during a Control Storage Load, or shall indicate that a Control Storage Load Command has been issued to the IFA by means of a Micro-command routine.

This signal reinitiates the Reset/Load sequence if not disabled by means of the Restart Reset/Load Disable described in 3.5.8.6.

3.5.8.6 Restart Reset/Load Disable

A pulse from the IFA, which shall occur 50 n/s before and shall remain for 50 n/s after the Restart Reset/Load pulse for the purpose of disabling the restart operation.

This signal shall disable the Restart Reset/Load signal when a burst check error has been detected and the Console is in Maintenance Mode.

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3.5.8.7 End (ut		
A pul shal Addre	se, from the Loader Logic indicate that Control Sto ss Table) has been complet	which, in the hi rage, (Including ely loaded.	gh state, the
This after retur word shall	signal shall assume the hi the next to the last word n to the low state from 1 is transferred. Minimum h be 3 u/s	gh state from 1 is transferred to 2 u/s after t igh state pulse	to 2 u/s and shall he last width
3.5.8.8 Prima	ry Source Data Lines		
Sixte shall for t	en (16) levels .'-om the IF provide Primary . urce in he duration of the . 'mary	A which, in the 1 put data (true s Data Strobe sign	high state, tate) nal.
See I	igure 8 for timing relatio	nships.	
3.5.9 Alter	nate Loader		
The A signa Adapt (incl	lternate Loader logic shal ls to interface the CPU an er, (ICRA), in order to ac uding the Address Table) R	l utilize the fo d the Integrated complish a Contro eset/Load.	llowing Card Reader ol Storage
NOTE :	The Alternate Loader sha a Main Storage Load when ance Mode and the Consol the MS-WR position, (See	11 be capable of the Console is 0 Operation Selec 3.10.3.11).	performing in Mainten- ct switch is
3.5.9.1 Alter	nate Reset/Load Initiate		
See 3	.5.8.1		
3.5.9.2 Alter	nate Data Strobe		
A pul that Sourc	se from the ICRA which, in 4 bits of input data are a e Data Lines as described	the low state, s vailable on the A in 3.5.9.8.	shall indic ate Alternate
This Conso Lines Conso with, Run C	pulse shall initiate a seq le Data Register, strobes into the Console Data Reg le Run signal. This Run s and shall perform the sam ontrol described in 3.10.3.	uence which clean the Alternate Sou ister, and genera ignal shall be in e function as, th 10.	rs the irce Data ates a i parallel ie Console
See F	igure 8 for timing relation	nships.	

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3.5.9.3	Alternate Source	
3.5.9.4	The Primary Source signal described in 3.5 state, shall indicate that the Alternate L be used for the Reset/Load. Maintenance Out	.8.3, in the low oad source is to
	See 3.5.8.4.	
3.5.9.5	End In	
	A 50 n/s minimum width pulse from the ICRA low state, shall indicate that the ICRA ha data transfer, (See 3.5.7.6, for Reset/Loa	Which, in the as completed its d Termination).
3.5.9.6	Nybl Zero	
	A pulse from the ICRA which, in the low st that the Alternate Source Data Lines corre left-most 4 bits, (Nybl Zero), of a 16-bit	cate, shall indicate espond to the ; word.
•	See Figure 8 for timing relationships.	
3.5.9.7	Nybl Three	
	A pulse from the ICRA which, in the low st that the Alternate Source Data Lines corre right-most 4 bits, (Nybl Three), of a 16-b	ate, shall indicate spond to the it word.
	See Figure 8 for timing relationships.	
3.5.9.8	Alternate Source Data Lines	
	Four (4) levels from the ICRA which, in th shall provide Alternate Source input data for the duration of the Alternate Data Str Each 4-bit input received on these lines s as a nybl and shall be assembled into a 16 working from left to right, in the Console	e high state (true state) obe signal. hall be treated -bit word, Data Register.
	See Figure 8 for timing relationships.	



provide the output from the ECC associated Register

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	· .	Set whe in 3.6.	n address 1, item c	ed by .).	means	of the si	gnals	described	
3.6.3	Con	trol	• • • •						
	Con Mai	trol sig n Storag	nals shal e as foll	l be e ows:	exchang	ed betwee	n the	CPU and	
	a.	A singl Storage for Mai	e Clock s and shaJ n Storag	ignal prov oper:	shall vide the ations.	be suppli e CPU tim	ed to ing re	Main ference	
	b.	A singl Main St for a M	e Acce s orage for ain Stora	Enable the p ge re	e signa purpose ference	l shall b of desig on the p	e supp nating art of	lied to the need the CPU.	
	с.	A singl Storage major c shall n Null St	e Refresh for the ycles wit ot occur ate.	signa purpos hin th during	al shal se of a ne CPU. g major	l be rece llocating Main St cycles a	ived Null orage llocat	from Main State references ed to the	•
	d.	A singl Main St referen Address Process	e Out of orage for ces on th es not ph or.	Range the p e part ysical	signal ourpose t of the lly pres	shall be of detec CPU to l sent with	recei ting M Main S in the	ved from lain Storag torage 7300	e
	e.	In the signal horizon be disa from Ma	presence shall be tal parit bled with in Storeg	of the receiv y chec in the	e ECC For yed from cking of e CPU and cating	eature an Main St Main St Id the EC	assoc orage orage C Erro	iated such that dat. shall or signal le data	•

error shall be enabled within the CPU.

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3.7 Basic Tim	ing	
With resp of the CP	ect to Multi-State capabilities, U shall be performed as shown in	the basic timing Figure 4.
With resp major cyc in Figure	ect to Single-State operations us les, the basic timing departure 4 is described in 3.7.1, item b	sing consecutive from that shown
3.7.1 State Ini	tialization	
State ini cycle all and shall	tialization shall occur prior to ocated to Processor States other occur under hardware control.	every major than the Null State
a. When cycle alloc shall with	Processor States 0 through 7 are s such that consecutive major cyc ated to the same Processor State occur during minor cycles R0 and E6 and E7, respectively.	allocated major cles are not , initialization d R1 in parallel
RO sh Pu Re to th	all transfer the contents of the gister from the Extended Register e Su Register.	appropriate r File, Group I
Rl sh Store trans from resou minor	all access Control Store proper a Address contained in Su. In add fer the contents of the appropria the Extended Register File, Group rce F Register, (Clocked at the b cycle E0).	at the Control dition, R1 shall ate F Register o I, to the common beginning of
b. When conse initi E9, a	Processor States 0 through 7 are cutive major cycles for the same alization shall occur during mino ppended to the major cycle as ill	allocated Processor State, or cycles E8 and Lustrated in 3.1.1.
Minor exten descr E9. 1 after conse 0 thr	cycle R1 shall be suppressed and ded to occur in parallel with E6 ibed in item a, as well as minor Minor cycles E8 and E9 shall occu E7 and prior to E0 for the purpo cutive major cycles for the same ough 7.	RO shall be as previously cycles E7 through ar, in that order, ose of implementing Processor State,
Minor Regist as des the co Extend when in 3.1	cycle E8 shill transfer the cont ter to Su when the operation has scribed in 3.8.12.5. Minor cycle ontents of the appropriate Pu Reg ded Register File, Group I, to th the Pp Register has been suppress 8.12.5.	ents of the Pp not been suppressed E8 shall transfer gister from the e Su Register ed as described

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Minor cycle E9 shall access Control Store proper at the Control Store Address contained in Su. At the end of E9, a major cycle shall begin on minor cycle E0 with the execution of the Micro-command thus accessed, on the part of the appropriate Processor State, provided the associated Busy Flip/Flop has remained in the set state. When the associated Busy Flip/Flop is in the clear state during minor cycle E8, minor cycle E9 shall cause a Null State major cycle to begin on the following minor cycle E0.

c. For all major cycles allocated to the Console State for the purpose of erforming operations under Microcommand control, m² or cycle RO shall transfer an address constant to Su according to 3.5.2 and minor cycle Rl shall clear the common resource F Register in addition to accessing Control Store proper. RO and Rl shall occur in parallel with E6 and E7, respectively, during the initialization of major cycles thus allocated to the Console State.

3.7.2 State Execution

Once initialized as described in 3.7.1, Processor States 0 through 7 and the Console State shall be capable of executing one Micro-command during each of the eight minor cycles beginning with E0 and continuing through E7. The actual number of Micro-commands executed during one major cycle shall depend on the nature of the Micro-commands themselves, up to a maximum of eight.

Note: As a result of the "Su+1" inputs to the Su and Pp Registers, (in conjunction with the compensation provided by the P_b, ("P buffer"), Register as required for the RO/R1 look-ahead utilization of the Su Register), Branch Micro-commands providing less than 14-bits of branch address shall have the anomalous characteristics as described in 3.8.11.

3.7.3 State Housekeeping

State housekeeping shall occur after every major cycle allocated to Processor States 0 through 7 under hardware control.

Housekeeping operations shall occur during minor cycles W0 and W1 in parallel with E0 and E1, respectively.



WO shall transfer the contents of the Pp Register to the appropriate Pu Register within the Extended Register File, Group I, provided the transfer has not been suppressed as described in 3.8.12.5. The WO operation shall update both the Arithmetic status (Bits 00 and 01) and the Control Store Address (Bits 02 through 15) portions of the appropriate Pu Register unless suppressed as described in 3.8.12.5 in which case the entire contents of the appropriate Pu Register shall be left unchanged, (including the "E" and "S" hardware controlled status bits as described in 3.2.2.2).

WI shall appropriately update the associated F Register within the Extended Register File, Group I, provided the F Register was designated by one or more Micro-commands for the purpose of performing a write reference during the preceding major cycle.

NOTE: As a result of the W1 timing equivalence to minor cycle E1, in conjunction with the compensation provided by the F_b , ("F buffer"), Register as required for the E7 to E0 timing transition, the restricted addressability for F Register write references shall exist during minor cycle E0 as described in 3.8.2.4, item b.

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3.8	Micro-comma	nd Repertoire	
	The Micro-c Nicro-conna grouped int	ommand Repertoire shall consist nds. These 65 basic Micro-comm o 10 classes as described in 3.	t of 65 basic mands shall be .8.3 through 3.8.12.
	Each of the 14-bit code bit positio state.	basic 65 Micro-commands shall s, arranged into a 16-bit forma ns 09 and 10 are unused and alv	consist of at such that ways in the clear
	Micro-comma and tempora registers r Control sec commands th translated the next 'li hardware co	nds shall be read from Control rily stored, i duplicate, by referred to as ul and Fu2 within tion of the CPU. The duplicate us contained in the Ful and Fu2 and executed, in parallel with cro-command, in an iterative far ntrol.	Storage proper means of in the Timing/ ed Micro- Registers are the access for ashion under
3.8.1	Format		
	Micro-comma Micro-comma a result of possible wi File refere bit positio are describ these capab	nd formats are shown for each on nds in 3.8.3 through 3.8.12. H the Micro-command modification th respect to register number f nces, bit position for Skin ope n for Immediate Operand entries ed in 3.8.1.1 through 3.8.1.3 r ilities.	of the 65 basic lowever, as is which are for Pegister rations and s, separate formats relative to
	Micro-comma of the bit common reso Register sh beginning o in 3.2.2.1.	nd modifications shall be based positions of the right-most byt urce F Register. The contents all be influenced by hardware c f each major cycle to the exten	l on the state e of the of this F control at the t described
3.8.1.1	Register Nu	mber	
	Micro-comma modified sh as Format 1	nds for which the register numb rll have the following format,	er may be referred to
	00 01 02 03	04 05 06 07 08 09 10 11 12 13	14 15
•	f	$\mathbf{s}_{0} \mathbf{s}_{1} \mathbf{a} \mathbf{b} \mathbf{p} 0 0 \mathbf{x}$	

 $t \in \mathbb{C}^{n}$

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	MEMO	REX	ENGINEEDING	OPECIEICATION	Number 8820	00
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	а.	The 4-b the fun	it "f" field (1 damental funct:	Bits 00 through ion code.	03) shall pr	ovide
	b.	The "so respect	" and "\$1" des: ively) shall p	ignators (Bits rovide the sub-	04 and 05, function code	•
	с.	The "a" respect registe referen	and "b" design ively) shall de r number is for cing the Regist	nators (Bits 06 etermine the main rmed for the putter File:	and 07, nner in which rpose of	the
		When "a shall b by the item f.	" and "b" are o e referenced at "x" field (Bits	clear, the Basi t the register t 11 through 15	c Register Fi number descri) as defined	le bed in
		When "a File sh describe performa field an F Regis	" is set and "h all be reference ed by the "x" f ed between bits nd bits 09, 10, ter.	" is clear the ted at the regis field after an ' 13, 14, and 19 , and 11 of the	Basic Regist ster number "inclusive or 5 of the "X" common resou	er " is rce
		When "a File sn describe performe and bit Registe	" is clear and all be reference ed by the "x" f ed between bits s 13, 14, and 1 r.	"b" is set, the ced at the regis field after an ' 13, 14 and 15 5 of the common	e Basic Regis ster number 'inclusive or' of the "X" f n resource F	ter " is ield
		When "a' shall be by the '	" and "b" are s referenced at "x" field.	et, the Extende the register r	ed Register F number descril	ile bed
	d.	The "P" horizon in the contents Micro-co	designator (bi tal parity when set state is od s of the Fu2 Re ommands.	t 08) shall pro the total numb ld for the entin gister and appl	ovide valid ber of bits te 16-bit lies to all	
	e.	The two in the o	unused bit pos clear state for	itions (Bits 09 all Micro-comm) and 10) shall ands.	ll be
	f.	The 5-bi the regi reference "inclusi and "b"	it "x" field (B lster number (1 ling the Regist lve or" operati are unlike.	its 11 through of 32) for the er File, subjec ons described i	15) shall pro purpose of t to the n item c when	ovide 1 "a"
L	Ferm 4002-2A					
						·

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When bit 11 is set, Group III shall be selected. When Format 1 Micro-commands are executed in Boundary Crossing Mode, the register number is determined as described in 3.2.3.7.

14 are set, in any combination, Group II shall be selected.

3.8.1.2 Bit Position Skip

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Micro-commands for which a bit position skip may be modified shall have the following format, referred to as Format 2.

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15

			1			
•						
I	S0' S1	a	PU	0 52	X	.
			1 1	1		

- a. The 4-bit "f" field (Bits 00 through 03) shall provide the fundamental function code for all Micro-commands.
- b. The "so", "s1", and "s2" designators (Bits 04, 05 and 11, respectively) shall provide the sub-function code.
- c. The "a" and "b" designators (Bits 06 and 07, respectively) shall determine the manner in which the bit position is formed for the purpose of selecting a bit within the Au Register as a Skip parameter.

When "a' and "b" are clear, the selected bit position in Au shall be described by the "x" field (Bits 12 through 15) as defined in item f.

When "a" is set and "b" is clear, the selected bit position in Au shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 08 through 11 of the common resource F Register.

MENM	NDIEW			Number 882000	
	nt Group	ENGINEERING SP	ECIFICATION	Sheet 88	
	When "a positic after a field a F Regis	" is clear and "b n in Au shall be n "inclusive or" nd bits 12 throug ter.	" is set, the described by is performed 1 h 15 of the co	selected bit the "x" field between the "x" ommon resource	
	When "a in Au s "inclus bits 08 and bit Registe	" and "b" are set hall be described ive or" is perfor through 11 of th s 12 through 15 o r.	, the selected by the "x" f med between th e common reson f the common r	d bit position ield after an ne "x" field, urce F Register, resource F	
	d. The "P" zontal state i Fu2 Reg	designator (Bit parity when the t s odd for the ent ister and applies	08) shall prov otal number of ire 16-bit cor to all Micro-	vide valid hori- E bits in the sentents of the -commands.	t
	e. The two shall b	unused bit posit e in the clear st	ions (Bits 09 ate for all Mi	and 10) Lcro-comands.	
	f. The 4-b the bit Au, sub in item	it "x" field (Bit position (1 of 1 ject to the "incl c when "a" and/o	s 12 through 1 6) to be selec usive or" open r "b" are set.	15) shall provid ted within tations describe	e d
3.8.1.3	Bit Positio	n Imm ediate Opera	nđ		
	llicro-comma may be modi referred to	nds for which a b fied shall have t as Format 3.	it position In he following f	umediate Operand Format,	· · · ·
	00 01 02 0 f	3 04 05 06 07 08 so s ₁ a b P	09 10 11 12 13 0 0 x	3 14 15	
	a. The 4-b the fun	it "f" field (Bit: damental function	s 00 through 0 code for all	3) shall provid Micro-commands.	e
	b. The "so respect	" and "s _l " design ively) shall prov	ators (Bits 04 ide the sub-fu	and 05, nction code.	
	c. The "a" respect bit pos bit (or Operand	and "b" designate ively) shall dete ition is formed fo bits) within the entry.	ors (Bits O6 a rmine the mann or the purpose Bu Register f	nd 07, er in which the of selecting a or Immediate	
	When "a' in Bu sl	" and "b" are cleanall be described	ar, the select by the "x" fi	ed bit position eld (Bits 12	

through 15) as defined in item f.

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When "a" is set and "b" is clear, the selected bit position in Bu shall be described by the "x" field after an "inclusive or" is performed between the "x" field and bits 08 through 11 of the common resource F Register.

When "a" is clear and "b' is set, the selected bit position in Bu shall be lescribed by the "x" field after an "inclusive or" is performed between the "x" field and oits 12 throu h 15 of the common resource F Register.

When "a" and "b" are s t, the bit position selected in the left-most byte position of the Bu Register shall correspond to the Processor State, 0 through 7, which performs the Micro-command. This "1 of 8" bit entry performed for the left-most byte position of the Bu Register shall be duplicated in the right most byte position of Bu. This operation shall occur independently of the value of the "x" field.

- d. The "P" designator (Bit 08) shall provide valid horizontal parity when the total number of bits in the set state is odd for the entire 16-bit contents of the Fu2 Register and applies to all Micro-commands.
- e. The two unused bit positions (Bits 09 and 10) shall be in the clear state for all Micro-commands. The undesignated bit position (Bit 11) shall have no effect on Micro-command execution except to the extent that it shall participate in the formation of valid L. rizontal parity as described in item d.
- f. The 4-bit "x" field (Bits 12 through 15) shall provide the bit position (1 of 16) to be selected within Bu except when "a" and "b" are set and subject to the "inclusive or" operations described in item c when "a" and "b" are unlike.

	MEM	OREX		Number 882060
į		ent Group	ENGINEERING SPECIFICATION	Sheet 90
	3.8.2	Characteris	tics	
		With respec characteris Register Fi are provide	t to each of the 65 basic Micr tics related to Mnemonic, Form le Addressability and Timing r d in Figure 9.	o-commands, at, Blockpoint, equírements
		The signifi described i	cance of each of these charact n 3.8.2.1 through 3.8.2.4.	eristics is
	3.8.2.1	Mnemonics		
		Mnemonics s and are sho Complementa special cha	hall consist of 3 or 4 alpha-n wn in Figure 9 in alpha-numeri ry operations are denoted by u racter, .	umeric characters c order. use of the
	3.8.2.2	Format		
		Formats 1, are shown i Mnemonics a	2, and 3 as described in 3.8.1 n Figure 9 for each of the 65 s applicable.	.1 through 3.8.1.3 Micro-command
	3.8.2.3	Blockpoint		
		When the "mu of the 7300 made for the rajor cycles Micro-commar cycle shall common resou execution of major cycle Thus the fin shall make m contents of ALU whenever i.e. the pr Processor St	alti-state" processing capabil: Processor are utilized, allowa e execution of Micro-commands is for each of the Processor Stands executed during the course not base their execution on the ince registers within the ALU ex- previous Micro-commands within has influenced the state of su st Micro-command executed in ex- o assumptions whatsoever with the common resource registers "multi-state" processing may revious major cycle was allocat ate than the current major cycle	ities characteristic nces must be in non-contiguous ates involved. All of each major he state of the except where the in the same ach registers. each major cycle respect to the within the have occurred, ted to a different
		A convention as Blockpoin command sequ during "mult designated a Address of t to as the Pp operations d	, using the Micro-commands sho ts, shall facilitate the codin ences such that valid results i-state" operations. Micro-co s Blockpoints shall record the he next Micro-command in a reg Register, in addition to perf escribed in 3.8.3 through 3.8.	own in Figure 9 og of Micro- shall be obtained ommands Control Storage ister referred orming the 12.



As previously described in 3.2.2.2, Micro-command execution for each major cycle allocated to Processor States 0 through 7 shall begin at the Control Storage Address designated by the contents of the associated Pu Register. Likewise, upon completion of each major cycle allocated to Processor States 0 through 7 the associated Pu Register shall be updated (written) to r flect the contents of the Pp Register (unless suppressed by execution of a CI01 or CI02 Micro-command). Thus, each major cycle allocated to Processor States 0 through shall involve the execution of at least one Blockpoint Mic o-command. Moreover, the Micro-commands following a Ble kpoint Micro-command shall make no assumptions relative ... the contents of the common resource registers in the ALU unless such Micro-commands are known to occur within the same major cycle as the last Blockpoint Micro-command. When the last Blockpoint occurs on a minor cycle other than E7 for any major cycle allocated to Processor States 0 through 7, the Micro-commands executed after the last Blockpoint shall be repeated during the next major cycle allocated to the associated Processor State.

NACAN		Number 882000
	UNEX ENGINEERING SPECIFICATION	Sheet 92
7 0 3 4		
3.8.4.4	Register File Addressability	
	for the purpose of performing read and wri to the Extended Register File, access shal to those registers and groups for the Micr shown in Figure 9.	te references 1 be allowed o-commands as
	The general addressability indications pro apply to the associated Micro-commands when Normal Mode only and are subject to specif described in 3.2. Boundary Crossing Mode is likewise described in 3.2.	vided in Figure 9 n executed in ic constraints addressability
	a. Where addressability shall be provided Register File group, addressability of Register File shall be possible for the commands as shown in Figure 9.	for any Extended the Basic e same Micro-
	b. Extended Register File, Group I address be indicated uniquely for the F and Pu shown in Figure 9.	sability shall Registers as
	Micro-commands for which F Register add be provided, should not occur for the p forming write operations during minor d operations shall not be hardware support result in machine malfunction.	dressability shall purpose of per- cycle EO. Such rted and may
	Micro-commands for which Pu Register ac shall be provided shall reference the A of the Pp Register and Arithmetic Statu the Su Register during read operations. for which Pu Register addressability sh shall reference the applicable bit posi Address portions only, of the Pp and Su write operations as specifically descri and 3.8.11.	Idressability Address portion is portion of Micro-commands hall be provided itions, in the Registers during ibed in 3.8.4
	c. Extended Register File, Group II address be provided for those Micro-commands sh subject to the constraints described in	sability shall Nown in Figure 9, 1 3.2.3.
	d. Extended Register File, Group III addre be provided for those Micro-commands sh subject to the constraints described in documents listed in 2.1.	ssability shall own in Figure 9, the associated
·		

MEN	MREY	Number 882000
	ent Groud Engineering Specification	Shoet 93 of
3.8.2.5	Timing	
	Micro-command execution times shall be pro in terms of the number of minor cycles req (minimum) and worst (maximum) cases.	vided by Figure 9 uired in the best
	In addition to the minimum, minor cycles s inserted as required for the following con	hall be hardware ditions:
	a. Additive Micro-commands SUN and DSUM a Micro-commands CMP and CMU shall requi minor cycle when adder and comparator respectively, have not ove lapped the or more previous Micro-con mands, (Bloc deferred until the second sycle when a	nd comparative re one additional propagations, execution of one kpoint shall be pplicable.
	b. Main Storage Related Micro-commands sh appropriate number of additional minor minor cycle in which they are translat does not correspond to the timing requ Storage.	all require an cycles when the ed for execution irements of Main
	c. Branch Micro-commands capable of reference applicable bit positions in the Address Su Register shall require one additions when executed in any minor cycle other JMP, and AND, CLR, STA, STB when the Pr designated).	encing the s portion of the al minor cycle than E7. (FNJ, u Register is
	d. Branch Micro-commands capable of references of the second state	encing the appli- tion of the Pp dditional minor FRJ, FZ, with and RNI2).
	e. Control Micro-commands CI01, CI02, ROM require as many additional minor cycles the major cycle.	and SYNC shall s as remain in
	NOTE: With respect to Micro-command contro asynchronous signals are read, resolve time before any actions dependent on the state of are taken. When input signals are subject the minor cycle in which they are read, set n/s must be allowed. For example, if an LA designating the Extended Register File Groups	ol and timing, wh e must be allowed of such signals to change during thing time of 20 W Micro-command up II CA Register
	command such as STA designating Pu) is performed and any skip micro-command (of n/s, such Micro-command may result in machi This resolve time requirement must be accom Micro-command control and in the case of th consist of, immediately following the LAW,	Formed within 200 ne malfunction. modated under is example could two NØPs or an S
	and LAW combination specifying an otherwise within the Register File or, an SHF designa zero, etc. Such precautions are particular the Extended Register File, Group III facil	unused register ting a shift of ly applicable to ities.
1		

MEM	OREY		Number 882000
	ent Group	XN	Sheet 94
3.8.3	Register File Read Micro-commands		
	The Micro-commands in this class shall for performing Register File read refe unrelated to Main Storage operations.	pro pronc	vide the means es which are
3.8.3.1	Load Au Word		
·	00 01 02 03 04 05 06 07 08 09 10 11 1	2 13	14 15
LAW	1 1 0 1 0 0 a b P 0 0	x	
	This Format 1 Micro-command shall tran the Register File to the Au Register w for the read reference designated acco	sfer ith rdin	the output from the register number g to 3.8.1.1.
3.8.3.2	Load Au Complement		
LAWN	00 01 02 03 04 05 06 07 08 09 10 11 1 1 0 1 0 1 a b P 0 0	12 1 x	3 14 15
	This Format 1 Micro-command shall tran of the output from the Register File t with the register number for the read according to 3.8.1.1. In addition, th Register shall be set.	sfer o the refe e For	the l's complement e Au Register rence designated rce Carry
3.8.3.3	Load Bu Word		
· · ·	00 01 02 03 04 05 06 07 08 09 10 11 1	2 13	14 15
LBN	0 1 1 0 0 0 a b P 0 0	X	
	This Format 1 Micro-command shall tran the Register File to the Bu Register w number for the read reference designate 3.8.1.1. In addition, the Force Carry be cleared.	sfer ith f ed ac Regi	the output from the register cording to ister shall

MEM	DREX		Number 882000
Equipme	nt Group	ENGINEERING SPECIFICATION	Sheet 95
7074	Lood Dy Co	mu 14ma 4	
3.9.3.4	Load bu CC	mp rement	
	00 01 02	03 04 05 06 07 08 09 10 11 12 1	3 14 15
LBWN	0 1 1	0 0 1 a b P 0 0 x	C
			· · · · · · · · · · · · · · · · · · ·
· · ·	This Forma	t 1 Micro-command shill transfe	r the 1's File to the Bu
	Register w	ith the register num er for the	read reference
	designated Force Carr	according to 3.8.1 In addi y Register shall be set.	tion, the
3.8.3.5	Load Au an	d Bu	
	00 01 02		3 14 15
TAD			
LAB	1 1 0		
	This Forma	t 1 Micro-command shall transfe	r the output of
· · ·	the Regist	er File to both the Au and Bu R	legisters with
	the regist according	er number for the read referenc to 3.8.1.1. In addition. the F	e designated orce Carry
	Register s	hall be cleared.	
3.8.3.6	Clear Au		
	00 01 02	03 04 05 06 07 08 09 10 11 12 1	3 14 15
CLA	1 1 0	1 1 1 a b P 0 0 x	
	L	<u></u>	
	This Forma	t 1 Micro-command shall transfe	r the output
	of the Reg	ister file to the Bu Register w	ith the signated
	according	to 3.8.1.1. In addition, the A	u Register
	shall be c set.	leared and the Force Carry Regi	ster shall be

.

MEMOREX	Humber 882000
Equipment Group	Sheet 96
3.8.3.7 Load Bu Link	
00 01 02 03 04 05 06 07 08 09 10 11	12 13 14 15
BL 0 1 1 1 1 a b P 0 0	x
This Format 1 Micro-command shall tra of the Register File to the Bu Regist register number for the read reference according to 3.8.1.1. In addition, t Link status bit shall be transferred Status portion of Su to the Force Car	nsfer the output er with the e designated he state of the from the Arithmetic ry Register.
3.8.4 Register File Write Micro-commands.	
The Micro-commands in this class shal for performing Register File write re are unrelated to Main Storage operati	l provide the means ferences which ons.
NOTE: The CLR, STA, STB and AND Micr effect a Branch operation when is designated.	o-commands shall the Pu Register
3.8.4.1 Clear Contents of Register (Designate	d by x)
00 01 02 03 04 05 06 07 08 09 10 11	12 13 14 15
CLR 0 0 0 1 0 0 a b P 0 0	
This Format 1 Micro-command shall cle the Register File at the register num according to 3.8.1.1. (See 3.8.2.4, it	ar the contents of ber designated em b restriction).
3.8.4.2 Store Au	
00 01 02 03 04 05 06 07 08 09 10 11	12 13 14 15
STA 0 0 0 1 0 1 a b P 0 0	x
This Format 1 Micro-command shall tran of the Au kegister to the Register Fi register number for the write reference according to 3.8.1.1.	nsfer the contents le with the ce designated

1

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MEMO	REX	ENGI	NEERING	SPECIFICATION	Rumber	882000	
Equipmen	t Group				Sheet 9	7	
3.8.4.3 S	tore Bu				· · ·		
	00 01 02	2 03 04	05 06 07	08 09 10 11 12	13 14 19	5	et i
STB	000) 1 1	0 a b	P 0 0	x		
T	his Forma	at 1 Mi	cro-comm	and shal' trans:	fer the d	contents	•
o n 3	f the Bu unber for .8.1.1.	Register r the wr	r to the ite refe	Register File w rence disignated	vith regi 1 accordi	ister ing to	
3.8.4.4 L	ogical Pi	roduct,	Au and B	u			
	00 01 02	2 03 04 (05 06 07	08 09 10 11 12	13 14 15	5	
AND	0 0 0	1 1	1 a b	P 0 0	x		
TI p tl	his Forma roduct of he Regist	t 1 Mici the cor er File designat	ro-commantents o with the	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1	Register r for th	ogical s to ne write	
TI p tl re TI b fe	his Forma roduct of he Regist eference ne logica it positi ollowing	t 1 Mich the cor er File designat 1 produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able.	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	er the lo Register er for th erformed ding to	for each	
TI p tl re TI b fe	his Forma roduct of he Regist eference he logica it positi ollowing Au Bu	t 1 Mich the cor er File designat 1 produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be pe Registers accor	er the lo Register er for th erformed ding to	for each	
Ti p tl rd Ti b fd	his Forma roduct of he Regist eference he logica it positi ollowing Au Bu	t 1 Mich the cor er File designat 1 produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be be Registers accor	r the lo Register r for th rformed ding to	for each	
T p tl rd T b f	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 0 1	t 1 Mich the cor er File designat 1 produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the lo Register r for th rformed ding to	for each	
T p tl rd T b f	his Forma roduct of he Regist eference he logica it positi ollowin Au Bu 0 0 1 0 1	at 1 Mich the cor er File designat al produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0 0	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the ic Register r for th rformed ding to	for each	
T p tl rd T b f	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 0 1 0 1 1	at 1 Mich the cor er File designat al produc on of Au truth ta	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the lo Register r for th rformed ding to	for each the	
T p tl rd f	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 1 0 1 1	at 1 Mich the cor er File designation of Au truth ta Log	ro-commantents o with thated acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the 10 Register r for th rformed ding to	for each	
T p t t r c T b f c	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 1 0 1 1	at 1 Mich the cor er File designation of Au truth ta Log	ro-commantents o with thated acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the ic Register r for th r rformed ding to	ogical es to e write for each the	
T p tl rd T b f f	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 1 1 0 1 1	at 1 Mich the cor er File designat 1 produc on of Au truth ta Log	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be pe Registers accor	r the lo Register r for th rformed ding to	for each the	
T p t r r T b f c	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 1 1 0 1 1	tt 1 Mich the con er File designat 1 produc on of Au truth ta Log	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be no Registers accor	r the 10 Register r for th rformed ding to	ogical s to he write for each the	
Ti p tl rd fd	his Forma roduct of he Regist eference he logica it positi ollowin, Au Bu 0 0 1 1 1 0 1 1	at 1 Mich the cor er File designat 1 produc on of Au truth ta Log	ro-commantents o with the ted acco ct opera u and Bu able. gical Pro 0 0 1	nd shall transfe f the Au and Bu e register numbe rding to 3.8.1.1 tion shall be pe Registers accor oduct	er the lo Register er for th erformed ding to	for each the	

MEMOREX	Number 882000
Equipment Group	Sheet 98
3.8.4.5 Inclusive Or, Au and Bu	
00 01 02 03 04 05 06 07 08 09 10 11 12 1	13 14 15
IOR 0 1 0 0 1 0 a b P 0 0 x	· · · · · · · · · · · · · · · · · · ·

This Format 1 Micro-command shall transfer the inclusive or of the contents of the Au and Bu Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

The inclusive or operation shall be performed for each bit position of the Au and Bu Registers according to the following truth table.

Au	Bu	Inclusive Or
0	0	0
0	1	1
1	0	1
1	1	1
	Au 0 0 1 1	Au Bu 0 0 0 1 1 0 1 1

3.8.4.6 Exclusive Or, Au and Bu

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
EOR	0	1	0	0	1	1	а	b	P	0	0			x		

This Format 1 Micro-command shall transfer the exclusive or of the contents of the Au and Bu Registers to the Register File with the register number for the write reference designated according to 3.8.1.1.

The exclusive or operation shall be performed for each bit position of the Au and Bu Registers according to the following truth table.

Au	Bu	Exclusive Or
0	0	0
0	1	1
1	0	1
1	1	0

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	MEM	OREX	Number 882000					
	Equipme	nt Group	Sheet 99					
	3.8.4.7	Sum, Au and Bu						
		00 01 02 03 04 05 06 07 08 09 10 11 12 13	14 15					
	SUM	0 0 1 0 0 0 a b P 0 0 x						
		This Format 1 Micro-command shall transfer	the sum of					
		the Au (16 bit ^c), Bu (16 bits) and Force Ca right justified) Registers to the Register	rry (1 bit, File with the					
		register number for the write reference des	ignated					
		according to 3.8.1.1.						
		In addition, the Overflow and Link status of relative to the current sum shall be transf	conditions Ferred to the					
		Arithmetic status portion of Su provided th	le left-most					
		equal to 50, 51, 52, or 53 in hexadecimal n	otation					
		and provided the Au or Bu Registers have be set. or clocked since the last execution of	en cleared, E a DIG or					
		CORC Micro-command.						
	3.8.4.8	Decimal Sum, Au and Bu						
		00 01 02 03 04 05 06 07 08 09 10 11 12 13	14 15					
	DSUI	0 0 1 0 0 1 a b P 0 0 x						
		L	I					
		This Format 1 Micro-comman. shall transfer Au (16 bits), Bu (16 bits) an. Force Carry justified) Registers to the Reg. ter File w register number for the write reference des to 3.8.1.1. The carry outputs from each of groups (4-bit nybls) shall be transferred t Carry Register.	the sum of the (1 bit, right ith the ignated according the adder o the Inner					
		In addition, the Overflow and Link status c	onditions					
		Arithmetic status portion of Su provided th	e Au or Bu					
		Registers have been cleared, set, or clocke last execution of a DIG or CORC Micro-comma	d since the nd.					
		NOTE: The Link status bit shall be derived output from the right-most byte of the adde of the left-most byte of the adder, wheneve most byte of the common resource F Register 50, 51, 52 or 53 in hexadecimal notation.	at the carry r, instead r the left- is equal to					
L.	Ferm 4002-2A							
:								
1.1.1								

Equipment C		NGINEERIN	IG SPEC	FICATION	Number 8820 Sheet 100 ef	UO
3.8.4.9 Sign	ind Magni	i tude Compa	re			
0	01 02 03	3 04 05 06	07 08 0	9 10 11 12 .	13 14 15	
СМР	0 1 0) 1 0 a	b P	0 0	x	
This (sig to t File be do	Format 1 (d), and (content) (here the (ignated)	Micro-comm logical (u ts of the A register according	and sha nsigned u and B number to 3.8.	11 transfer), compare s u Registers, for the writ 1.1.	the algebra tatus, rela to the Reg e reference	lic ltive lister shall
When throu acco table	he Basic h 07 of ling to t	: Register the approp he left-mc	File is riate r st byte	designated, egister shal position of	only bits 1 be writte the follow	00 n, ing
When addre provi as fo	he Exten sability ed, the lows:	ded Regist of the de full 16-bi	er File signate t compa	is designat d register i re status sh	ed and s specifica all be prov	llv ided
ALGEBRAIC LOGI	L 100 01	02 03 04 0	5 06 07	08 09 10 11	12 13 14 1	5
(A) >(B) (A) >	B) 0 1	0 0 0	100	1	······································	1
(A) > (B) (A) <	B) 0 1	0 0 0	010	1		1
(A) < (B) (A) <	B) 0 0	1 0 0	0 1 0	1	>	1
(A) < (B) (A) >	B) 0 0	1 0 0	100	1		1
(A) = (B)	0 0	0 1 0	0 0 1	1	>	1
						1

MEM) REX	·			Number	882000
Equipmer	nt Group	ENGINE	EERING SP	PECIFICATION	Sheet 10	1 of
7 9 <i>1</i> 10 W	(amituda C	000000				
J.O. 4.10 19						
	00 01 02	03 04 0	5 06 07 0	8 09 10 11 12	13 14 15	
CMU	0 0 1	0 1	1 a b 1	P 0 0	x	
			•			
T	his Format unsigned)	1 Micro compare	-command status, re	shall transfer elative to the	the logi contents	cal of
ť	he Au and	Bu Regis	ters, to	the Register F	ile where	the
d	lesignated	accordin	g to 3.8.	1.1.		
W	hen the Ba	sic Regi	ster File	is designated	, only bi	ts
0 W	0 through ritten acc	07 of the ording t	e appropri o the left	iate register t-most byte po	shall be sition of	the
f	ollowing t	able.				
W	hen the Ex	tended R	egister is	s designated a	nd addres	sability
0 1	f the desi 6-bit comp	gnated rear	egister is us shall b	s specifically be provided as	provided follows:	, the full
-				· · · · · · · · · · · · · · · · · · ·		· · · ·
	00 01 02	03 04 05	06 07 08	09 10 11 12 1	3 14 15	
Au) > (Bu)	0 1 0	0 0 1	0 0 1.		→ 1	
Au) < (Bu)	0 0 1	0 0 0	1 0 1.		→ 1	
Au) = (Bu).	0 0 0	1 0 0	0 1 1.		> 1	
. · · ·	<u>↓</u> -				d	
		· .		· · · ·		
.* ·	•					
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an taon 1997. An taona						· · ·
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Equipment	Group _	CHOINEERIN	IU JEUR		Sheet	192	
					· · ·		٦
3.8.5 Reg	ister Fil	e Read, Mai	n Storage	Related	Micro-o	commands.	
The for rel Reg LS2 Sto and	Micro-co performi ated to, ister Opt and LSE rage (or LDB Micr	mmands in t ng Register or may be r ion) operat shall be un Register Op o-commands	his class File rea elated to ions. Mi condition tion) ope shall be	shall pr d referen , Main St cro-comma ally rela rations. Main Stor	ovide (ces whi orage (nds LS1 ted to The LI age (or	the means ch are or , LSF, Main DW, LDWN, Register	
opt cvc LSI A11 Sto aft or Mai	lon) rela le El imm , LSF, LS other Mi rage (or er, but w LSE Micro n Storage	ted only who ediately fo 2 or LSE Mic cro-commands Register Opt ithin the sa -commands es (or Regist	en they a llowing th cro-comman s in this tion) rela ame major xecuted for ter Option	re execut he execut hd at min class sh ated when cycle as or the pu h) read op	ed duri ion of or cycl all be they o LS1, L rpose o peratio	ng minor an e EO. Main ccur SF, LS2 f performing ns.	
The the thi	selection ALU shal s class in	n of an inpu 1 be conditu n the follow	ut to the ioned by ving manne	D Fan-In the Micro er:	Networ -comman	k within ds within	
а.	During M Main Sto from min	ain Storage rage shall b or cycle E4	Read oper be selected through n	rations, ed at the minor cyc	the dat D Fan- le E7.	a from In Network	
ь.	During Ro Register Network	egister Opti Option shal from minor c	ion Read o 11 be sele cycle E4 1	operations ected at through mi	s, the the D F inor cy	data from the an-in cle E7.	•
¢.	For the p Register Register be treate	ourpose of m Option Read set associa ed as Main S	naking D H l operation ited with Storage Re	Fan-In Net ons which the ECC l ad operat	twork s specif Feature tions.	election only y the shall	· ,
d.	During a items a, at the D	ll minor cyc b, and c, f Fan-In Netw	the D Regiver,	than the ster shall	ose des L1 be s	cribed in elected	
3.8.5.1 Loa	đS						
00	01 02 03	04 05 06 07	08 09 10	11 12 13	3 14 15		
LS1 0	0 1 1	0 0 a b	P 0 0	x	- <u> </u>	7	
LSF	0 1 1	0 1 a b	PO 0	x	······································	- 1	
	0 1 1	1 0 a b	TPIO 0	x	······	-	
	0 1 1	1 I a b	P O O	x			Ì
· · · · · · · · · · · · · · · · · · ·	·····	k k k				• • •	
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These Format 1 Micro-commands shall transfer the output from the Register File to the S Register, when executed on minor cycle EO, with the register number for the Register File read reference designated according to 3.8.1.1.

- a. When executed during minor cycle E0 on the part of Processor States 0 through 7 with bits 11, 12, 13 and 14 set (register number 1E or 1F) or when executed during minor cycle E0 on the part of the Console State with the Console Operation Select switch in the RO-RD or RO-VR position (See 3.10.3.11), these Micro-commands shall cause hardware interpretation of the remainder of the appropriate major cycle to be associated with a Register Option reference.
- b. Shen executed during minor cycle E0 on the part of Processor States 0 through 7 with bits 11, 12, 13 or 14 clear in any combination (not register number IE or 1F) or when executed during minor cycle E0 on the part of the Console State with the Console Mode Select switch in any applicable position other than RO-RD or RO-WR (See 3.10.3.11), these Micro-commands shall cause hardware interpretation of the remainder of the appropriate major cycle to be associated with a Main Storage reference.
 - . When executed during minor cycle E0, in the presence of the Basic Storage Protection Feature, the Relocation and Protection Feature or the ECC Feature, these Micro-commands shall require an additional minor cycle referred to as E0. When executed during minor cycle E0, in the presence of the Basic Storage Protection and ECC Features or the Relocation and Protection and ECC Features, these Micro-commands shall require two additional minor cycles referred to as E0'and E0". Minor cycles E0' and E0" shall be hardware inserted.
- d. When executed during any minor cycle other than E0, the contents of the S Register shall not be affected by these Micro-commands. Moreover, the nature of each major cycle with respect to its association with Register Option or Main Storage references shall be hardware interpreted during minor cycle E0 only and shall not be altered by the execution of these Micro-commands during minor cycles other than E0. When executed during any minor cycle other than E0, the associated Load S Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle. Thus, each Load S Micro-command occurring on minor cycles other than E0, must be immediately preceded by a Blockpoint Micro-command for Processor States 0 through 7.



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These Format 1, Load S Micro-commands shall transfer the output of the Register File to the Au Register, regardless of the minor cycle in which they are executed, with the register number of the Register File Read reference designated according to 3.8.1.1. Likewise, the Bu and Force Carry Registers shall be affected according to the following:

e. The LS1 Micro-command shall cause 0000_{16} to be transferred to the Bu Register and the Force Carry Register shall be set.

- f. The LSF Micro-command shall cause FFFF16 to be transferred to the Bu Register and the Force Carry Register shall be cleared.
- g. The LS2 Micro-command shall cause 0001₁₆ to be transferred to the Bu Register and the Force Carry Register shall be set.
- h. The LSE Micro-command shall cause FFFE16 to be transferred to the Bu Register and the Force Carry Register shall be cleared.

In the presence of the Relocation and Protection Feature, Load S Micro-commands executed during minor cycle E0 shall result in the transfer of the Segment Tag, associated with the designated register number, to be transferred to the left-most 4-bit extension of the S Register as contained within the Relocation and Protection Feature.

Although the Load S Micro-commands shall be capable of execution in a single minor cycle, E0, as reflected by Figure 9, the following restrictions shall apply:

- i. In the presence of the Basic Storage Protection or the Relocation and Protection Features, the Load S Microcommands shall require 2 minor cycles, the second consisting of a special hardware inserted cycle referred to as E0⁴.
- j. In the presence of one of the features described above and in the additional presence of the ECC Feature, the Load S Micro-commands shall require 3 minor cycles, the second and third consisting of special hardware inserted cycles referred to as E0'and E0", respectively.

8.5.2	2	Loa	d D	Wo	rd			•										
•		00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	
	LDW	0	1	1	1	0	:0	a	b	P	0	0			x]
	2			-														

3.

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	OREX ENGINEERING SPECIFICATION	Sheet 105 of
	This Format 1 Micro-command shall transfer the Register File to the D Register with t number for the Register File read referenc according to 3.8.1.1.	the output from he register e designated
	When executed during minor cycle E1, immed an LS1, LSF, LS2 or LSE Micro-command at m this Micro-command shall result in a Main Option write reference involving a full tr Register output. In such cases, alteratio of the D Register by means of Micro-comman cycles E2 through E7, may result in machin The word locations of the write reference Storage, or within the Register Option, sh by the contents of the S Register (Bit 15 for Breakpoint) and shall be subject to ap validity checks on the part of the Basic S or Relocation and Protection Features. Wr thus performed shall involve 16 data bits addressed.	iately following inor cycle EO, Storage or Register ansfer of the D n of the contents ds during minor e malfunction. within Main all be designated irrelevant except propriate hardware torage Protection ite references when validly
3.8.5.3	Load D Complement	
LDW	00 01 02 03 04 05 06 07 08 09 10 11 12 13 0 1 1 0 1 a b P 0 0 x	14 15
	This Format 1 Micro-command shall transfer of the output from the Register File to the the register number for the Register File designated according to 3.8.1.1. For a description of the relationship of the to Main Storage and Register Option write the comments in 3.8.5.2.	the l's complement e D Register with read reference his Micic-command references see
3.8.5.4	Load D Byte	
	00 01 02 03 04 05 06 07 08 09 10 11 12 13	14 15
LDB	0 1 1 1 1 0 a b P 0 0 x	
	This Format 1 Micro-command shall transfer from the Register File to the D Register w number for the Register File read reference according to 3.8.1.1.	the output ith the register e designated

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When executed during minor cycle E1, immediately following an LS1, LSF, LS2, or LSE Micro-command at minor cycle EO, this Micro-command shall result in a Main Storage write reference involving a partial transfer of the D Register output for which the right-most byte shall be duplicated in the left-most byte position, (the D Register output to the D Fan-In Network shall not be affected). 'In such cases, alteration of the contents of the D Register by means of Micro-commands during minor cycles E2 through E7, may result in machine malfunction. The byte location of the write reference within Main Storage shall be designated by the contents of the S Register and shall be subject to appropriate hardware validity checks on the part of the Basic Storage Protection or Relocation and Protection Features. Write references thus performed shall involve the transfer of only the left-most data byte where bit 15 of the S Register is clear or the transfer of only the right-most data byte where bit 15 of the S Register is set, when validly addressed.

3.8.5.5 D To Au, True

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15

DTA

1

1 0 0 0 0 a b P 0 0 x

This Format 1 Micro-command shall transfer the output from the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1. In addition, this Micro-command shall transfer the output from the D Fan-In Network to the Au Register and shall clear the Force Carry Register.

When initially translated on minor cycle El, E2, or E3 during any major cycle in which a Main Storage or Register Option read reference is performed, this Micro-command shall be held in the Ful and Fu2 Registers and repeatedly executed during each minor cycle up to and including E4, under hardware control. MEMOREX Equipment Group 882000 107

3.8.5.6 D to Au, Complement

00	01 02	03 04	05 06	07 08	09 10	11 12	13 14 15

DTA	1	1	0	0	Û	1	a	Ь	P	0 0	•	3	•	
					ليبرص حف	ښمينا								i

This Format 1 Micro-command shall transfer the 1's complement of the output from the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1. In addition, this Micro-command shall transfer the output from the D Fan-In Network to the Au Register and shall set the Force Carry Register.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.

3.8.5.7 Index

 00
 01
 02
 03
 04
 05
 06
 07
 08
 09
 10
 11
 12
 13
 14
 15

 IDX
 1
 1
 0
 1
 0
 a
 b
 P
 0
 0
 x

This Format 1 Micro-command shall transfer the output from the Register File to the Bu Register provided the resultant register number for the Register File read reference does not have the 3 right-most bits (13, 14 and 15) in the clear state when designateu according to 3.8.1.1.

This Micro-command shall simply clear the Bu Register provided the resultant register number for the Register File read reference has the 3 right-most bits (13, 14 and 15) in the clear state when designated according to 3.8.1.1.

In addition, this Micro-command shall unconditionally transfer the output of the D Fan-In Network to the Au Register and shall clear the Force Carry Register.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.



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In the presence of the Relocation and Protection Feature, the IDX Micro-command shall also serve as the implicit Micro-command control mechanism for dynamic Segment Tag write references. Each IDX Micro-command shall allow the next Register File write reference, performed under Micro-command control, to occur such that the associated Segment Tag shall also be written. The Segment Tag value so written shall correspond to the Segment Tag value read during the last LS1, LSF, LS2, or LSE Micro-command, whenever the associated IDX Micro-command simply cleared the Bu Register. Alternatively, the Segment Tag value read during the associated IDX Micro-command whenever this associated IDX Micro-command whenever this associated IDX Micro-command whenever this associated IDX Micro-command a transfer of the Register File output to the Bu Register.

3.8.5.8 D False to Au

	00	01	02	03	04	05	06	07	0.8	0.9	10	11	12	13	14	15	
DFA	1	1	0	0	1	1	a	b	Р	0	.0			x			}

This Format 1 Micro-command shall transfer the output of the Register File to the Bu Register with the register number for the Register File read reference designated according to 3.8.1.1.

In addition the 1's complement of the output from the D Fan-In Network shall be transferred to the Au Register and the Force Carry Register shall be set.

During Main Storage and Register Option read references, hardware controlled timing constraints shall be exercised as described in 3.8.5.5.

Register File Write, Main Storage Related Micro-commands.

The Micro-commands within this class shall provide the means for performing Register File write references which may be related to Main Storage or Register Option read operations.

The Micro-commands within this class shall be Main Storage or Register Option related when they occur after, but in the same major cycle as LS1, LSF, LS2, or LSF Micro-commands which are executed for the purpose of performing Main Storage or Register Option read operations as defined in 3.8.5.1 through 3.8.5.4.

3.8.6
MEM	NREY				Number 882	000	
	int Group	ENGINEERING	g specific	ATION	Sheet 109		
	When initia during any Option read shall be he executed du under hardw	ally translate major cycle is reference is ld in the Ful ming each min ware control.	d on minor n which a l performed and Fu2 Re or cycle uj	cycle El Main Stor these ' gisters to and	, E2, E3 age or Re licro-comm and repeat including	or E4 gister ands tedly E5,	
3.8.6.1	Store D Wor	d	÷.				
	00 01 02	03 C4 05 06 0	7 08 09 10	11 12 13	14 15	•	
SD	W 0 1 0	0 0 0 a 1	b P 0 0	x			
	This Format of the D Fa the registe designated	1 Micro-comm n-In Network r number for according to	and shall to to the Registe the Registe 3.8.1.1.	ransfer ster Fil r File w	the output e with rite refea	rence	
3.8.6.2	Store D Byt	e					
•	00 01 02	03 04 05 06 0	7 08 09 10	11 12 13	14 15		
SD	3 0 1 0	0 0 1 a t	P 0 0	x			
	This Format most byte o Fan-In Netw of the S Re byte positi position. write refer	1 Micro-comma r left-most by ork (as detern gister)to the on, along with The register n ence shall be	and shall to the from the nined by the Register H in zeroes in number for determined	ransfer e output e state ile in t the lef the Regi accordi	the right of the D of bit 15 he right- t-most oyt ster File ng to 3.8.	lost e 1.1.	
	When bit 15 the left-mo selected at File and ze Register Fi	of the S Regist byte of the the right-mos roes at the le le.	ister is in e D Fan-Out st byte ing eft-most by	the cle Network ut to th te input	ar state, shall be e Register to the		
• • • •	When bit 15 the right-me selected at File and ze Register Fi	of the S Regi ost byte of th the right-mos roes at the le le.	ster is in the D Fan-Ou the byte inp tt-most by	the set t Networ ut to th te input	state, k shall be e Register to the		
				• * *. • • .			
				•		•	
				· · · · · · · · · · · · · · · · · · ·			
		والمراجعة والمراجعة والمراجعة والمراجعة والمراجع والمراجع والمراجعة والمراجعة					

MAGNA	ADEY'	Number 882000
	nt Group	Sheet 110
3.8.7	Immediate Operand Micro-commands.	
	The Micro-commands within this class shall means for transferring immediate operands Register. These immediate operands shall within the Micro-commands themselves, with of CORC and special cases of the LBB and	l provide the to the Bu- be contained the exception LBB\ Micro-commands.
	Undesignated bit positions within these is shall have no effect on Micro-command exec to the extent that they shall participate of valid parity.	icro-commands cution except in the formation
3.8.7.1	Enter Bu Upper	
	00 01 02 03 04 05 06 07 08 09 10 11 12 1	3 14 15
EBU	J 1 0 1 0 NO P 0 0 N-	
3.8.7.2	to the left-most byte position of the Bu H right-most byte position of the Bu Registe unchanged. Enter Bu Lower	Register. The er shall remain
		7 1A 35
EBL		1
	The N_0/N_1 fields of this Micro-command sha to the right-most byte position of the Bu addition, the left-most byte position of t shall be cleared.	ll be transferred Pegister. In he Bu Register
3.8.7.3	Load Bu Bit	
•	00 01 02 03 04 05 06 07 08 09 10 11 12 13	14 15
LBE	0 1 1 0 1 0 a b P 0 0 x	
	This Format 3 Micro-command shall transfer immediate operand to the Bu Register.	a 16-bit
· · · · · · · · · · · ·		
· · ·		

MEMOREX		Number 882000
Equipment Group		Sheet 111
When the "a immediate o state with bit positio 3.8.1.3.	a" and "b" designators are not soperand shall consist of a sing the remaining 15 bits in the control to be set shall be designated	set, the 16-bit le bit in the set lear state. The 1 according to
When the "a operand sha one in each in the clea set shall o in which th byte shall as describe	a" and "b" designators are set, all consist of two bits in the s byte position, with the remain ar state. The left-most bit pos- correspond to the Processor Stat Micro-command is executed and be duplicated in the right-most ed in 3.8.1.3.	the 16-bit set state, ning 14 bits sition to be te, 0 through 7, 1 the left-nost t byte position
In addition	, the Force Carry Register sha	ll be cleared.
3.8.7.4 Load Bu Bit	Complement	
00 01 02	03 04 05 06 07 08 09 10 11 12 1	13 14 15
LBB\ 0 1 1	0 1 1 a b P 0 0	c
This Format immediate c When the "a immediate o clear state The bit pos according	3 Micro-command shall transfer perand to the Bu Register. " and "b" designators are not s perand shall consist of a singl with the remaining 15 bits in ition to be cleared shall be de to 3.8.1.3.	et, the 16-bit tet, the 16-bit te bit in the the set tate. esignated
When the "a operand sha one in each in the set cleared sha through 7, the left-mo byte positi	" and "b" designators are set, 11 consist of two bits in the c byte position, with the remain state. The left-most bit posit 11 correspond to the Processor in which the Micro-command is e st byte shall be duplicated in on as described in 3.8.1.3.	the 16-bit lear state, ing 14-bits ion to be State, 0 xecuted and the right-most
in addition	, the Force Cary Register shall	l be set.

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Equipment Group	ENGINEERING	SPECIFICATION	Sheet 112
3.8.7.5 Digit Dupli	cation		
00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15
DIG 1 1 1	1 1 0	P 0 0 x	
The "x" fie to each nyb In addition	ld of this Mic l (4-bit group , the Force Ca	ro-command shall) position of the rry Register shal	be transferred Bu Register. 1 be cle ared.
Execution of carry mechan nybl may be in the cleat Overflow and of the Su Re of this Mich effect until clocked by M	f this Micro-c nisms within t independently r state. Like d Link conditi egister shall ro-command. T l the Au or Bu Micro-commands	ommand shall inhi he adder such tha added with group wise, the clockin ons within the Ar be inhibited by t hese disables sha Registers are cl other than DIG a	bit the group at each 4-bit carry inputs g of the ithmetic portion the execution all remain in eared, set or and CORC.
3.8.7.6 Correct Code	9		
00 01 02 0	03 04 05 06 07	08 09 10 11 12 1	3 14 15
CORC 1 1 1 This Micro-c	1 1 1 command shall	P 0 0 transfer a 16-bit	inmediate
operand to nybl (4-bit by the state Inner Carry	the Bu Registe group) shall e of the assoc Register.	r where the value be independently iated bit positio	of each determined n in the
Where the bi are set, the 3 in hexaded	it positions in associated n cimal notation	n the Inner Carry ybls shall have t •	Register he value of
Where the bi clear, the a hexadecimal	it positions in associated nyb notation.	n the Inner Carry ls shall have the	Register are value of D in
In addition,	, the Force Ca	rry Register shal	l be cleared.
Execution of carry mechan nybl may be in the clear and Link con Su Register Micro-comman until the Au by Micro-com	f this Micro-consists within the independently r state. Likew nditions within shall be inhile nd. These disa or Bu Register mands other the	ommand shall inhi he adder such tha added with group vise, the clockin h the Arithmetic bited by the exec ables shall remain ers are cleared, han DIG and CORC.	bit the group t each 4-bit carry inputs g of the Overflow portion of the ution of this n in effect set or clocked

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	mant Group	ENGINEERING	SPECIFICATIO	N Sheet	113
3.8.8	Shift Micr	o-commands			
	The Micro- means for Shift coun in true or binary pla be end-off shifted in the right-	commands within left shifting t ts of 4 bits sh 2's complement ces. Bits shif , (lost).Bits f to the Au Regis most bit positi	this class s he contents o all be Micro- form, for sh ted from the rom the Bu Re ter with zero ons of the Bu	hall prov f the Au/ command d ifts from Au Regist gister s es insert Register	ride the Ju Register lesignated 1 0 to 1510 er shall hall be red into
	Undesignat shall have to the ext of va lid p	ed bit position no effect on M ent that they s arity.	s within thes icro-command hall particip	e Micro-c execution ate in th	ommands except e formation
3.8.8.1	Shift Left			e San an	
	00 01 02	03 04 05 06 07	08 09 1 0 11	12 13 14	15
	This Micro Registers by the "x"	-command shall left the number field.	shift the con of bit posit	tents of ions desi	the Au/Bu gnated
3.8.8.2	Shift Righ	t	•		
	00 01 02 (03 04 05 06 07	08 09 10 11 1	2 13 14 1	5
	SHR 1 1 1	0 0 1	P 0 0 0	x	
	.		I I		
	This Micro Bu Register by the 2's	-command shall rs left the numl complement of	shift the con ber of bit po the "x" field	tents of sitions d •	the Au/ esignated
3.8.8.3	This Micro Bu Registe: by the 2's Left Shift	-command shall rs left the num complement of (Dependent Cour	shift the con ber of bit po the "x" field nt).	tents of sitions d •	the Au/ esignated
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02	-command shall rs left the numl complement of (Dependent Cour 03 04 05 06 07	shift the con ber of bit po the "x" field nt). 08 09 10 11	tents of sitions d 12 13 14	the Au/ esignated 15
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02 DLS 1 1 1	-command shall rs left the numl complement of (Dependent Coun 03 04 05 06 07 0 1 0	shift the conder of bit pothe "x" field nt). 08 09 10 11 P 0 0 0	tents of sitions d 12 13 14	the Au/ esignated 15
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02 DLS 1 1 1	-command shall rs left the numl complement of (Dependent Coun 03 04 05 06 07 0 1 0	shift the con ber of bit po the "x" fieldnt).08 09 10 11 P 00	tents of sitions d 12 13 14	the Au/ esignated
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02 DLS 1 1 1	-command shall rs left the numl complement of (Dependent Coun 03 04 05 06 07 0 1 0	shift the con ber of bit po the "x" field nt). 08 09 10 11 P 0 0 0	tents of sitions d 12 13 14	the Au/ esignated 15
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02 DLS 1 1 1	-command shall rs left the numl complement of (Dependent Coun 03 04 05 06 07 0 1 0	shift the con ber of bit po the "x" field nt). 08 09 10 11 P 0 0 0	tents of sitions d 12 13 14	the Au/ esignated
3.8.8.3	This Micro Bu Registe by the 2's Left Shift 00 01 02 DLS 1 1 1	-command shall rs left the numl complement of (Dependent Coun 03 04 05 06 07 0 1 0	shift the con ber of bit po the "x" field nt). 08 09 10 11 P 0 0 0	tents of sitions d 12 13 14	the Au/ esignated

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	This Mic::o- Au/Bu Regis designated	command shall ters left the by the shift c	shift the number of count.	contents o bit positi	of the lons
	The shift c 08 through bit positio is set.	ount shall be 11 of the comm n 01 of this c	obtained f non resourc common reso	rom bit po e F Regist urce F Reg	ositions er when gister
	The shift c D Fan-In Me 15) when bi is clear. or Register input to the Register to data inputs DLS Micro-c these condi- when execute	ount shall be twork in the r t position 01 During major c Option read r e D Fan-In Net the Main Stor , respectively ommands which tions, shall p ed during mino	obtained f ight-most of the com ycles whic eference, work shall age data o , during m obtain the rovide unp r cycles E	rom the ou bit positi mon resour h perform the select change fr r Register inor cycle shift cou redictable 4/E5.	tout of the ons (12 thr ce F Registe a Main Stor ion of the com the D Option E4. Thus mt under results
3.8.8.4	Right Shift	(Dependent Co	unt)		
an da sur tari Si	00 01 02	03 04 05 06 07	08 09 10	11 12 13 1	4 15
DR	S 1 1 1 This Micro- Au/Bu Regis designated 1	0 1 1 command shall ters left the by the 2's com	P 0 0 shift the number of 1 plement of	0 contents o pit positi the shift	f the ons count.
	The shift co as previous in 3.8.8.3.	o unt shall be ly described f	obtained in or the DLS	n the same Micro-com	manner mand
3.8.9	Bit Sense M	icro-commands.			
	The Micro-comeans for so left to right bit position by the associated sha as specified A value corr through 1510 Register. detection of added to the	ommands within canning the co ht, for the pu h in the set o ciated Micro-c all be cleared d by the SR1 a responding to), shall be ad when the entir f a bit in the e contents of	this class ntents of rpose of de r cleared s ommand. Bi or set wit nd SSO Micr the bit pos ded to the e Au Regist specified the Bu Regist	s shall pr the Au Reg etecting t state as s it positio thin the A ro-command sition det contents ter is sca state, 16 lster.	ovide the ister, from he first pecified ns thus u Register s, respectiv ected, 00 of the Bu nned without 10 shall be
	Undesignated shall not a extent that	l bit position ffect Micro-co they shall na	s within th mmand execu rticipate i	nese Micro ation exce In the for	-commands pt to the mation of

MEMOREY			Number 882000
Equipment Group	ENGINEERING	SPECIFICATION	Sheet 115
3.8.9.1 Sense for 2	lero		
00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15
SR0 1 1 1	0 0 0	P 0 0 1	
Le construction de la constructi			
This Micro- of the firs increase th result of t	<pre>command shall : t bit position e contents of t he scan.</pre>	scan the Au Regis in the clear sta the Bu Register a	ter for detection te, and shall ccording to the
The content	s of the Au Reg	gister shall rema	in unchanged.
3.8.9.2 Sense for O	ne		
00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15
SSI 1 1 1	0 0 1	P 1	
	, <u></u>		
detection o and shall i according t The content	f the first bit ncrease the cor o the results o s of the Au sha	t position in the stents of the Bull of the scan.	set state Register ged.
3.8.9.3 Sense and S	et for Zero		
00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15
SS0 1 1 1	0 1 0	P 0 0 1	
••••••••••••••••••••••••••••••••••••••			
This Micro- of the firs increase th to the resu	command shall s t bit position e contents of t lts of the scan	can the Au Regist in the clear stat he Bu Register ac	ter for detection te and shall ccording
The Au Regi detected in Au Register	ster shall be s the clear stat are not equal	et in the first b e when the conter to FFFF ₁₆ .	oit position hts of the

· · ·

	OREX nt Group	ENGINEERING SPECIFICATION	Number 882000 Sheet 116
3.8.9.4	Sense and R	eset for One	
	00 01 02	03 04 05 06 07 08 09 10 11 12 1	3 14 15
SI	R1 1 1 1	0 1 1 P 1	
	This Micro- detection o and shall in according t	command shall scan the Au Regis f the first bit position in the ncrease the contents of the Bu o the results of the scan.	ter for the set state Register
	The Au Regin position de of the Au Re	ster shall be cleared in the fi tected in the set state when th egister are not equal to 0000 ₁₆	rst bit le contents
3.8.10	Skip Micro-	commands	
	The Micro-c means for si Micro-comman Au Register one minor c cycle to ac Micro-comman Skip Micro- are met as shall skip minor cycle cycle.	ommands within this class shall kipping the execution of the ne nd when the specified condition are met. These Micro-commands ycle for translation and an add complish the skipping of the ne nd when the specified condition commands for which the specifie initially translated during min the next successive Micro-comma E0 of the next appropriately a	provide the ext successive as within the shall require litional minor ext successive as are met. d conditions for cycle E7, and during llocated major
	NOTE: When logically as signals into without an malfunction Micro-comman	the contents of the Au or Bu R mbiguous as a result of transfe o them, the execution of Skip M allowance for resolve time may in the form of undefined and u and execution. See 3.8.2.5.	egisters are rring asynchronous licro-commands result in machine npredictable
	Undesignated shall have n to the exten of valid par	d bit positions within these Mino effect on Micro-command exec not that they shall participate rity.	cro-commands ution except in the formation
3.8.10.1	Skip if Au	is Zero	
	00 01 02 0	3 04 05 06 07 08 09 10 11 12 13	14 15
SKZ	0 1 0	1 0 0 P 0 0 0	
F	This Micro- successive M Register are	command shall skip the execution ficro-command when the contents equal to 0000_{15} .	n of the next of the Au

• • • • • • • • • • •

MEM	OREX	ENGINEERING	SPECIFICATION	Number 88200	0
Equipme	ent Group			Sheet 117	
3.8.10.2	Skip if Au	is Non-Zero			
	00 01 02	03 04 05 06 07	08 09 10 11 12	13 14 15	
SX		1 0 1		-	
	This Micro- successive	command shall Micro-command	skip the execution when the contents	on of the nex s of the Au	t
n an Ar An Aragana	Register ar	e not equal to	0000 ₁₆ .		
3.8.10.3	Skip if Au	Bit is a One.			
	00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15	
SY				~~~	
21	B U I U		PUUU	X	
		a 1/1		· .	
	the next su	2 Micro-comma ccessive Micro	nd shall skip the -command when the	e execution o content of	£
	the Au Regi	ster is in the	set state at the	bit positic	n
	designated	according to 5	• 0 • 1 • 4 •		
3.8.10.4	Skip if Au	Bit is a Zero.			
an a	00 01 02	03 04 05 06 07	08 09 10 11 12 1	3 14 15	
SK	B 0 1 0	1 1 1 a b	P 0 0 0	x	
	1				
а 1. т. – С.	This Format	2 Micro-comma	nd shall skip the	execution o	e i i
	the next su	ccessive Micro	-command when the	content of	the state
	designated	according to 3	.8.1.2.	it position	
3.8.10.5	Skip if Au)	Bu			N 2
	00 01 02 0	7 04 05 06 07	00 00 10 11 12 17	14 15	
4 ¹		3 04 03 00 07			
SK	G 0 1 0	1 0 0	P 0 0 1		
*	This Micro-	command shall	skin the executio	n of the next	
	successive Register ar	Micro-command v e logically (u	when the contents nsigned) greater	of the Au than the cont	ents
	of the Bu R	egister.			
				· . ·	
\$				· · · · ·	
		•			
			·····	-	
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MEMORE	37		Number 882000
Equipment Gro	Dup	SPECIFICATION	Sheet 118
3.8.10.6 Skip i	f Au < Bu		
000	1 02 03 04 05 06 97	08 09 10 11 12 1	3 14 15
SKL 0	1 0 1 0 1	P 0 0 1	
This M next s the Au conten	icro-command shall uccessive Micro-com Register are logic ts of the Bu Regist	skip the executio mand when the con ally (unsigned) 1 er.	on of the tents of ess than the
3.8.10.7 Skip i	f Au = Bu		
00 0	1 02 03 04 05 06 07	38 09 10 11 12 1	3 14 15
SKE 0	1 0 1 1 0	P 0 0 1	
This M succes Au Reg Registe	icro-command shalls sive Micro-command ister are equal to er, bit-for-bit.	kip the execution when the contents the contents of t	of the next of the he Bu
3.8.10.8 Skip i	f Au ≠ Bu		
_00 0	1 02 03 04 05 06 07	08 09 10 11 12 1	3 14 15
SKEN 0	1 0 1 1 1	P 1	
This M Micro- not equ	icro-command shall command when the co ual to the contents	skip the execution ntents of th e Au of the Bu Registe	n of the next Register are er, bit-for-bit.

MEMOREX		Number	832000	
Equipment Group	ENGINEERING SPECIFICATION	Sheat	119	

3.8.11 Branch Micro-commands

In addition to the CLR, STA, STB and AND Micro-commands which shall effect a Branch operation when the Pu Register is designated as described in 3.8.4, the six Micro-commands in this class shall explicitly provide the means for performing branch operations.

As opposed to the implicit Micro-commands previously mentioned and described in 3.8.4, the explicit Microcommands in this class shall be capable of only partial write references to the right-most address portions of the Su and Pp Registers as follows:

a. The JMP Micro-command shall write only Bits 08 through 15 of the Su and/or Pp Registers. Bits 02 through 07 shall be under hardware control and shall be incremented by one when JMP Micro-commands occur at Control Storage Addresses XXFF₁₆. Likewise, bits 02 through 07 shall be incremented by one when JMP Micro-commands occur at Control Storage Addresses XXFE₁₆ during any minor cycles other than E6 and/or E7.

The FNJ, FRJ, FZJ, RNI1 and RNI2 Micro-commands shall write only Bits 04 through 15 of the Su and/or Pp Registers. Bits 02 and 03 shall be under hardware control and shall be incremented by one when these Microcommands occur at Control Storage Addresses XFFF₁₆. Likewise, bits 02 and 03 shall be incremented by one when these Micro-commands occur at Control Storage Addresses XFFE₁₆ during any minor cycles other than E6 and/or E7.

Execution of RNI1, RNI2 and FZJ Micro-commands shall be additionally dependent on the state of the Instruction Repeat switch as described in 3.10.4.18, to the extent that the branch addresses associated with these Micro-commands may be altered from values of X002₁₆ and X009₁₆ to a value of X000₁₆.

Undesignated bit positions within these Micro-commands shall have no effect on Micro-command execution except to the extent that the/ shall participate in the formation of valid parity.

INCLEMANDLE AND ENGINEERING SPECIFICATIONStreet 120Equipment Group00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15FNJ0 0 0 0 0 1 I I 0 P 0 0 IThis Micro-command shall transfer a 12-bit branch address to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 04 through 15.This 12-bit branch address shall be based on the I, Io and I Micro-command designators as well as the contents of the common resource P Register, (for which bit positions shall be referred to as F00 through F15).a. When the I designator (bit 06) is clear, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address at the designator (bit 06) is set, the 12-bit branch address to 11 12 13 14 15IoIoIoPR0 0 10 2 03 04 05 06 07 08 09 10 11 12 13 14 15FRJ0 0 10 2 03 04 05 06 07 08 09 10 11 12 13 14 15FRJIoP0 0This Micro-command shall transfer a 12-bit br	плепл	MORY	7			Number 8	82000
3.8.11.1 Function Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FNJ 0 0 0 0 1 1 1 10 P 0 1 1 This Micro-command shall transfer a 12-bit branch address to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 04 through 15. This 12-bit branch address shall be based on the I, I ₀ and I ₁ Micro-command designators as well as the contents of the common resource F Register, (for which bit positions shall be referred to as F ₀₀ through F ₁₅). a. When the I designator (bit 06) is clear, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 F04 F05 F06 F07 0 0 b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 1 0 0 F08 1 0 0 5.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 1 0 0 1 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for addressing the Address Table and formatting its output are described in 5.5.3. Once read, this Micro-command shall be held in the Ful and FUZ Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.				g specific	ATION	Sheet 12	0 01
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	3.8.11.1	Function	Decode Jump	an a		· · · ·	
FNJ 0 0 0 0 1 1 1 10 P 0 11 This Micro-command shall transfer a 12-bit branch address to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 04 through 15. This 12-bit branch address shall be based on the 1, 10 and 11 Micro-command designators as well as the contents of the common resource F Register, (for which bit positions shall be referred to as F00 through F15). a. When the I designator (bit 06) is clear, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 11 F04 F05 F06 F07 0 0 b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 11 0 0 F08 1 0 0 S.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 0 1 0 1 0 1 0 F08 1 0 0 This Micro-command shall transfer a 12-bit branch address to the P Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for address Table Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the P7 Register occurring only during the first minor cycle of its execution.		00 01 0	2 03 04 05 06 0	7 08 09 10	11 12 13	14 15	
This Micro-command shall transfer a 12-bit branch address to the Su Register, (except during minor cycles E6 and E7), and the Pp Register, in bit positions 04 through 15. This 12-bit branch address shall be based on the I, I ₀ and I ₁ Micro-command designators as well as the contents of the common resource F Register, (for which bit positions shall be referred to as F ₀₀ through F ₁₅). a. When the I designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 11 F_{04} F_{05} F_{06} F_{07} 0 0 b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 11 0 0 F_{08} 1 0 0 Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 11 0 0 F_{08} 1 0 0 3.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 0 F 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for address Table (9 bits of address, 1 bit for parity) and inserting the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the P7 Register occurring only during the first minor cycle of its execution.	FN	1 0 0 C		P 0 0	I ₁		
This 12-bit branch address shall be based on the I, I ₀ and I ₁ Micro-command designators as well as the contents of the common resource F Register, (for which bit positions shall be referred to as F ₀₀ through F ₁₅). a. When the I designator (bit 06) is clear, the 12-bit branch address at the designated inputs to the Su and PP Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 1 10 1 1 10 1 12 13 14 15 10 1 1 10 1 1 10 1 12 13 14 1510 1 1 1 10 1 12 13 14 1510 1 1 10 1 12 13 14 1510 1 1 10 1 12 13 14 1510 1 1 10 1 12 13 14 1510 1 1 10 1 1 12 13 14 1510 1 1 10 1 1 10 1 12 13 14 1510 1 1 10 1 1 10 1 12 13 14 1510 1 1 1 10 1 10 1 12 13 14 1510 1 1 1 10 1 10 1 12 13 14 1510 10 102 03 04 05 06 07 08 09 10 11 12 13 14 $15FRJ 0 0 0 1 0 10 10 10 10$		This Micr to the Su and the P	o-command shall Register, (exce p Register, in b	transfer a pt during pit positio	12-bit minor cy ns 04 th	branch cles E6 rough l	address and E7), 5.
a. When the I designator (bit 06) is clear, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 1 F_{04} F_{05} F_{06} F_{07} 0 0 b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 0 0 F_{08} 1 0 0 3.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 0 P 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The conventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fuz Registers for the remainder of the main for addressing the Address Table to the Pp Register occurring only during the first minor cycle of its execution.		This 12-b I1 Micro- common res referred	it branch addres command designat source F Registe to as F ₀₀ throug	s shall be cors as wel r, (for wh gh F ₁₅).	based o 1 as the ich bit	n the I conten position	, I ₀ and ts of the ns shall be
10 + 03 + 05 + 06 + 07 + 05 + 10 + 11 + 12 + 13 + 14 + 13 $10 + 11 + 12 + 13 + 14 + 13$ $10 + 11 + 12 + 13 + 14 + 13$ $10 + 11 + 12 + 13 + 14 + 13$ $10 + 11 + 12 + 13 + 14 + 13$ $10 + 11 + 12 + 13 + 14 + 15$ $10 + 11 + 12 + 14 + 14 + 14$ $10 + 12 + 14 + 14 + 14 + 14 + 14 + 14 + 14$		a. When addres shall	the I designator ss at the design have the follow	(bit 06) ated input ving format	is clear s to the :	, the 12 Su and	2-bit branch Pp Registers
b. When the I designator (bit 06) is set, the 12-bit branch address at the designated inputs to the Su and Pp Registers shall have the following format: 04 05 06 07 08 09 10 11 12 13 14 15 10 1 1 0 0 F_{08} 1 0 0 3.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 0 P 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and FuZ Registers for the remainder of the major cycle, with the transfer from the Address Table to the PP Register occurring only during the first minor cycle of its execution.			$1 \frac{1}{1}$	F04 F05	F ₀₆ F ₀	$\frac{3}{7}$ 14	0
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		b. When the address Regist	the I designator ss at the design ters shall have	(bit 06) ated input the follow	is set, s to the ing form	the 12-1 Su and at:	oit branch Pp
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		04	4 05 06 07 08 09	10 11	12 13	14 15	-
 3.8.11.2 Format Decode Jump 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 0 P 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The conventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution. 		I		0 0 F	08 1	0 0	
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 FRJ 0 0 0 1 0 P 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.	3.8.11.2	Format Dec	code Jump			.* 	
FRJ 0 0 0 0 1 0 P 0 0 This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The conventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.	· · · · ·	00 01 02	2 03 04 05 06 07	08 09 10	11 12 13	14 15	
This Micro-command shall transfer a 12-bit branch address to the Pp Register in bit positions 04 through 15. (The output of the D Fan-In Network must be stable 200 n/s prior to the execution of this Micro-command). This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.	FRJ	1 0 0 0		P 0 0			
This 12-bit branch address shall be obtained by reading the output of the Address Table (9 bits of address, 1 bit for parity) and inserting 3 hardware translated bits. The con- ventions for addressing the Address Table and formatting its output are described in 3.5.3. Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.		This Micro the Pp Reg of the D H execution	o-command shall gister in bit po Fan-In Network m of this Micro-c	transfer a sitions 04 ust be stal ommand).	12-bit through ble 200	branch a 15. (1 n/s pric	ddress to he output or to the
Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle, with the transfer from the Address Table to the Pp Register occurring only during the first minor cycle of its execution.		This 12-bi output of parity) an ventions f output are	it branch addres the Address Tab nd inserting 3 h for addressing t described in 3	s shall be le (9 bits ardware tra he Address .5.3.	obtained of addra anslated Table an	d by rea ess, 1 b bits. nd forma	ding the it for The con- itting its
		Once read, Fu2 Regist transfer f only durin	, this Micro-com ers for the rem from the Address ng the first min	mand shall ainder of 1 Table to 1 or cycle of	be held the major the Pp Re f its exe	in the r cycle, egister ecution.	Ful and with the occurring

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MENM	NREM				Number	882000
	nt Group	ENGINEEI	RING SPEC	FICATION	Sheet 12	21
3.8.11.3	Zero Jump					
	00 01 02	03 04 05 0	6 07 08 09	10 11 12	13 14 15	
F7 1						7
1 20						
	This Micro- of 00916 to 15 on the f	command sh the Pp Re irst minor	all transf gister in cycle in	er a 12-b bit posit which it	it branch ions 04 t is execut	address hrough ed.
	When the co 000016, no part of thi proceed to as availabl	ntents of further op s Micro-co the execut e at the o	the Au Reg erations s mmand, and ion of the utput of C	ister are hall be p hardware next Mic ontrol St	not equa erformed control s ro-comman orage pro	l to on the hall d p er .
	When the co the Ful and the remaind shall be pe State with	ntents of Fu2 Regis er of the rformed on respect to	the Au Reg ter clocks major cycl the part Micro-com	ister are shall be e and no of the cu mand exec	equal to disabled further o rrent Pro ution.	0000 ₁₆ , for perations cessor
3.8.11.4	Jump					
	00 01 02	03 04 05 0	6 07 08 09	10 11 12	13 14 15	
JMP	1 0 0	1 N	0 P 0	0	Nl]
	This Micro- address con (except dur Register, i	command sh sisting of ing minor n bit p osi	all transf the N ₀ /N ₁ cycles E6 tions 08 t	er an 8-b fields t and E7), hrough 15	it branch o the Su and the P ₁	Register,
	Thus, this bran ch oper Control Sto 3.8.11, ite	Micro-comm ations wit rage prope m a.	and provid hin 256-wo r, with th	es the me rd page b e excepti	ans for pe oundaries ons noted	erforming of in
3.8.11.5	Read Next I	nstruction	1			•
	00 01 02	03 04 05 0	6 07 08 09	10 11 12	13 14 15	
RNI1	1 0 0	0 0 0	a b P O	0	x]
	This Micro- of 002 ₁₆ to on the firs	command sh the Pp Re t minor cy	all transf gister in l cle in whi	er a 12-b bit posit ch it is	it branch ions 04 th translated	address brough 15 l.
	*		·			

	NDEY	Number 882000	
	ent Group	Shoot 122	
	In addition, this Format 1 Micro-command the Overflow and Link bits from the Arithm portion of Su to the Basic Register File of number for the partial write reference des to 3.8.1.1. This transfer shall be confin Basic Register File as a result of disable operation when the "a" and "b" designators command are both in the set state and conse exception to Format 1 Micro-command addres The Basic Register File shall be written 8 bit positions such that Overflow shall be to bit 00, bits 01, 02 and 04 through 07 s and Link shall be transferred to bit 03. 8-bits shall remain unchanged.	shall transfer metic status with the register signated according ned to the ing the write s for this Micro- stitutes an ssability. in the left-most be transferred hall be cleared, The right-most	
	Once read, this Micro-command shall be hel	ld in the Ful	
3.8.11.6	Read Next Instruction 2	e major cycle.	
	00 01 02 03 04 05 06 07 08 09 10 11 12	13 14 15	
RN I	2 1 0 0 0 0 1 a b P 0 0	x	
	This Micro-command shall transfer a 12-bit of 009_{16} to the Pp ¹ Register in bit position 15 on the first minor cycle in which it is	t branch address ons 04 through s translated.	
	In all other respects, this Micro-command identically to the RNII Micro-command as o	shall execute lescribed in	
	3. 0. 11. 3.		
		··· · · · · · · · · · · · · · · · · ·	
			t y l 'ar i s
			-

	MEMOREX ENGINEERING SPECIFICATION	Number 382000
	Equipment Group	123
	3.8.12 Control Micro-commands	
	The Micro-commands within this class shall for performing Timing, Input/Output Termin: Boundary Crossing Mode operations.	provide the means ation and
	Undesignated bit positions within these Mic have no effect on Micro-command execution extent that they shall participate in the valid parity.	cro-commands shall except to the formation of
	3.8.12.1 No Operation	
	00 01 02 03 04 05 06 07 08 09 10 11 12 1	3 14 15
	NOP 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
	This Micro-command shall not influence CPU the minor cycle during which it is containe and Fu2 Registers.	operations for ed in the Ful
	3.8.12.2 Resynchronize	
I	00 01 02 03 04 05 06 07 08 09 10 11 12 13	3 14 15
	SYNC 1 1 1 1 0 0 P 0 0 1	
	ttttt	
	This Micro-command shall transfer the Contr Address of the next successive Micro-commar positions 02 through 15 of the Pp Register minor cycle in which it is executed.	rol Storage nd to bit on the first
	Once read, this Micro-command shall be held and Fu2 Registers for the remainder of the	l in the Ful major cycle.
	Thus, the execution of a SYNC Micro-command in the establishment of minor cycle E0 for of the next successive Micro-command during major cycle allocated to the associated Pro	the execution the next cessor State.
	3.8.12.3 Invoke/Revoke Boundary Crossing Mode	
	00 01 02 03 04 05 06 07 08 09 10 11 12 13	5 14 15
	RVK 1 1 1 1 0 1 P 0 0 0	
ľ		

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During all minor cycles following the execution of an IVK Micro-command, up to and including the minor cycle in which an RVK Micro-command is executed, Boundary Crossing Mode shall be in effect with respect to the designation of register numbers on the part of all Micro-commands performing Register File references.

The Boundary Crossing Mode of designating register numbers by means of the contents of the BC Register is described in 3.2.3.7 including timing constraints where applicable.

The Normal Mode of designating register numbers by means of Format 1 Micro-commands only, is described in 3.8.1.1.

3.8.12.4 Read Control Memory

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	
rom	1	. 1	1	1	0	0			Р	0.	0	0					

This Micro-command shall transfer the Control Storage Address of the next successive Micro-command to bit positions 02 through 15 of the Pp Register on the first minor cycle in which it is executed.

Control Storage proper shall be read referenced at the address contained in the Bu Register and the output of Control Storage proper shall be subsequently transferred to the CSS Register (J-K inputs as described in 3.2.3.8) on the second minor cycle involved in the execution of this Micro-command.

Once read, this Micro-command shall be held in the Ful and Fu2 Registers for the remainder of the major cycle. ROM Micro-commands which begin execution on minor cycles E6 or E7 shall be undefined with respect to the data transfer to the CSS Register. Thus, meaningful execution of each ROM Micro-command shall require that an allowance be made for a minimum of 3 contiguous minor cycles in the same major cycle as shown in Figure 9. This allowance must be provided under Micro-command control.

3.8.12.5 Compare I/O

	00	01	02	03	04	05	06	07	08	09	10	11 12	13	14	15
CI01	1	0	0	0	1	0	1	1	Р	0	0				
	<u>L.</u>			l	l]		1		l	· · · · ·			
CI 02	1	0	0	0	1	1	1	1	Р	0	0				
	L	_									l				



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These Micro-commands shall transfer the Control Storage Address of the next successive Micro-command to bit positions 02 through 15 of the Pp Register on the first minor cycle in which they are executed.

Once read, these Micro-commands shall be held in the Ful and Fu2 Registers for the remainder of the major cycle.

Operations performed in the further execution of these Micro-commands shall be dependent upon the comparison of the contents of the Au and Bu Registers as well as the state of the appropriate End of Transfer signal when performed for Processor States 0 through 3. See 3.2.4.12 for a description of the End of Transfer signals.

- a. When the contents of the Au Register are equal to the contents of the Bu Register, bit-for-bit, or in the presence of the appropriate End of transfer signal when applicable, the CIO1 Micro-command shall provide an I/O Exit signal as described in 3.2.4.13 at the end of the first minor cycle of execution only.
- b. When the contents of the Au Register are not equal to the contents of the Bu Register, bit-for-bit, or in the presence of the appropriate End of Transfer signal when applicable, the CIO2 Micro-command shall provide an I/O Exit signal as described in 3.2.4.13 at the end of the first minor cycle of the execution only.

When these Micro-commands provide an I/O Exit signal at the end of the first minor cycle of their execution, no other operations shall be performed.

When these Micro-commands do not provide an I/O Exit signal at the end of the first minor cycle of their execution, the transfer of the contents of the Pp Register to the appropriate Pu Register (to the Su Register during consecutive major cycles for the same Processor State) which would otherwise occur during minor cycle WO, shall be suppressed. In addition, a pulse shall be applied to the clear input of the appropriate Busy Flip/Flop in the B/A Register for Processor States 0 through 4 at the end of the first minor cycle of execution of these Micro-commands in which an I/O Exit signal is not provided, as described in 3.2.3.1, item d.

Execution of these Micro-commands beginning on minor cycle E7 shall not be hardware supported and may result in machine malfunction.

MEMO	REX				Number	882000	
Equipment	Group		SPECIFICATI	ON	Sheet 12	6	
3.9 Re	source Allo	cation			•		
Re b a ge	source allo sis by mean nerally des	cation shall s of the Reso cribed in 3.1	be accompl urce Alloca .8.	ished tion N	on a ma etwork	ijor cycle as	4
Th re an eq	e Resource source requ d the Conso uivalent to	Allocation Ne ests from Pro le State, dur CLOCK-60 as	twork shall cessor Stat ing minor c defined in	resyn es 0 t ycle E 3.2.4.	chroni; hrough 1 at a 5.	ze all 7 time	
Th an re:	e Refresh ro d shall havo source reque	equest from M e uncondition ests.	ain Storage al priority	shall over	occur all oth	s ynchro no 1er	us 1 y
3.9.1 No	n-Priority 1	Mode		5			
In Al cyc al the or	the absence location Ne cles to the location of e Processor der:	e of Priority twork shall p requesting P major cycles States invol	Mode opera roportionate rocessor St shall occu ved, in the	tions, ely al ates. r repe follo	the Re locate This e titious wing se	source major qual ly, for quential	
		PROCESSOR PROCESSOR PROCESSOR PROCESSOR PROCESSOR PROCESSOR PROCESSOR PROCESSOR CONSOLE ST.	STATE 0 STATE 1 STATE 2 STATE 3 STATE 4 STATE 5 STATE 6 STATE 6 STATE 7 ATE				
Whe (a) acc the Rec	en more thar fter the Mai counted for) e following Total Numb questing Pro	n one of thes In Storage Re , resource a manner. er of ocessor State	e resource f fresh requin llocation sh s Alloc	reques rement: hall ta Resou cation	ts occu s have ake pla urce per St	r, been ce in ate	
	2 3 4 5 6 7 8 9			50.0 33. 25.0 20.0 16.0 14.2 12.5) % 3 %) % 5 % 2 % 5 %		
					-		

MEM	OREX				Number	382000
Equipme	ent Group	ENGINEERIN	ig specific	ATION	Sheet 12	7
	•			· · · ·	- 	
3.9.2	Priority Mod	de	· .	• • • •		•
	The Resource resynchronia 0 through 3 associated 3.2.3.5 and the associat described in resynchronia minor cycle	e Allocation ze all resour , relative to Invoke Priori relative to ted Enable Pr n 3.2.3.5 and zation activi El at a time	Network sha ce requests their coir ty signals their combi- ciority and 3.2.4.11, ties shall equivalent	11 addi from P cidence as desc ned coin Priority respect occur du to CLOO	tionally rocesso with th ribed in ncidence y signa ively. uring ev CK-60 as	r States ne with ls as These very
	defined in Each Priorit 0 through 3 Non-Priority Mode request following on	5.2.4.5. ty Mode reque shall have u Mode reques ts occur, pri rder:	est on the p incondition ts. When n ority shall	art of l 1 prior 1 ore than 1 be gran	Processo ity ove n two P nted in	or States r all riority the
	PI PI PI	ROCESSOR STAT ROCESSOR STAT ROCESSOR STAT ROCESSOR STAT	YE 0 YE 1 YE 2 YE 3		· · · · · · ·	
	In the absen Mode request Refresh requ of the resou State so req When three of Priority Mod having highe cases, these utilization other Process as a result	nce of Consec ts shall resu urements hav urce utilizat questing, up or four Proce de requests, est priority two Process of the resou ssor States, of Main Stor	utive Cycle ilt, (after e been acco ion allocat to a maximu ssor States only the tw shall be re or States s irces to the (except for age Refresh	operati the Main unted for ed to ea m of two have ma o Proces cognized hall equ exclusi Null St request	ions, Prins or), in ach Proc such S ade simu ssor Sta 1. In s ually sh ion of a cates pe	riority ge 50% cessor States. States. States such sare 111 rformed
3.9.3	Non-Consecut	tive Cycle Mo	de		•	р.
	Without resp Cycle Mode s a single Pro resource uti	bect to Prior shall affect bcessor State llization in	ity Mode op resource al , 0 through the absence	erations location 7, is r of all	s, Non-O only w requestiother n	Consecutive hen ng equests.
	an a	CHAN'S BE CHIL PROVIDED		1		
FAR 4003.04	and a second	ana ana amin'ny faritr'o amin'ny faritr'o amin'ny faritr'o amin'ny faritr'o amin'ny faritr'o amin'ny faritr'o a Amin'ny faritr'o amin'ny				N 1997

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Thus, major cycles shall be alternately allocated between the single requesting Processor State and the Null State unless the appropriate Consecutive Cycle Enable is set as described in 3.2.3.5.

3.9.4

Consecutive Cycle Mode

Without respect to Priority Mode operations, Consecutive Cycle Mode shall affect resource allocation only when a single Processor State, 0 through 7, is requesting resource utilization in the absence of all other requests.

Thus, major cycles shall be consecutively allocated to the single requesting Processor State when the appropriate Consecutive Cycle Enable is set as described in 3.2.3.5. Consecutive Cycle Mode shall be accomplished by means of basic timing modifications as described in 3.8.1, item b.

NOTE: The Console State shall be unconditionally capable of utilizing consecutive major cycles without the basic timing modifications which shall be required for Processor States 0 through 7. See 3.7.1, item c.

3.9.5 Priority with Consecutive Cycle Mode

> When both Priority and Consecutive Cycle Modes of operation are correspondingly specified for one or more Processor States, the highest priority Processor State thus requesting resource utilization shall obtain exclusive allocation of the resources, (with the exception of the Null State resulting from Main Storage Refresh requests).

NOTE: Each major cycle performed in this combined Priority and Consecutive Cycle Mode of operation shall be unconditionally followed by a Null State major cycle when the associated Busy Flip/Flop is cleared. See 3.7.1, item b.

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Equipm	ent Group	Shoet 129 of	
3.10	System Control Panel (Console)		
	The Console description within this Section to the Console as implemented for Serial 8	shall apply and beyond.	· · ·
	Controls and indicators on the 7300 Console arranged in four major groups as follows:	shall be	
	Operator Group (See Figure 10) Program Group (See Figure 11) Maintenance Group (See Figure 12) Communications Activity Display Group (See	Figure 13)	
 	The relative positions of these groups is s Figure 14.	hown in	
3.10.1	Mechanical		
	The Console Control Panel shall be approxim 22"W, 11.5"D and positioned at the front of Processor cabinet. For maintenance purpose and indicator portions of the panel shall b of being pivoted 90 degrees into a mechanic position so as to be easily accessed from the module (card) side of the 7300 Processor cal	ately 28" H, the 7300 s, the control e capable ally locked he P. C. binet.	
3.10.2	Operator Group		
	With the exception of the Power On and Powe as described in 3.10.2.2 and 3.10.2.3, resp Operator Group of controls shall be enabled This group of controls shall provide the op the basic means for control of the 7300 Pro-	r Off switches ectively, the at all times. erator with cessor.	
3.10.2.1	Emergency Pull		
	This control shall be a latching pull switch a mechanical reset shall be required. The mechanism shall be located behind the Conso Panel such that it is accessible only by ope Console Control Panel enclosure.	h. Once pulled, resetting le Control ening the	
	When pulled, this switch causes all A.C. and to drop immediately, by-Fissing the normal p sequence. This action shall be referred to Power Off (EPO).	d D.C. power power-down as Emergency	
	CAUTION: OPERATION OF THIS CONTROL MAY RESIDENTION: DAMAGE TO THE SYSTEM.	ULT IN PHYSICAL	



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3.10.2.2 Power On

This control shall be a momentary push-button switch with an indicator.

The effect of this switch shall be conditioned by the Local/ Remote Control described in 3.10.4. In Remote Control Mode the Power On switch shall have no effect. In Local Control Mode the depression of the Power On switch shall initialize the power-up sequence.

The indicator shall be on when the power-up sequence is initialized and shall remain on until a power-down sequence has been completed, i.e. during power sequencing and when power is on.

NOTE: Upon completion of the power-up sequence, a Reset/ Load sequence shall be automatically initialized. Moreover, upon completion of the Reset/Load sequence, an Autoload sequence shall be automatically initialized provided the Maintenance Group controls have not been enabled. For a description of the Reset/Load and Autoload sequences, see 3.10.2.12 and 3.10.2.4, respectively.

3.10.2.3 Power Off

This control shall be a momentary push-button switch with an indicator.

The effect of this switch shall be conditioned by the Local/ Remote Control as described in 3.10.4. In Remote Control Mode, the power off switch shall have no effect. In Local Control Mode, the depression of the Power Off switch shall initialize the power-down sequence.

The indicator shall be on <u>unless</u> one of the following conditions exist:

a. No primary power is available.

b. The Main Disconnect switch is off.

- c. An EPO (Emergency Power Off) has occurred.
- d. Power is on, i.e. that period between the completion of the power-up sequence and the initialization of the power-down sequence.

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3.10.2.4 Autoload		
This contro	ol shall be a momentary push-but	ton switch with

an indicator. When depressed, this switch shall initialize an Autoload sequence, and the indicator shall be on until the switch is released. The Autoload sequence shall consist of the following:

- a. A System Reset shall be performed for a minimum of .4 m/s and z maximum of .6 m/s. For a description of the effects of System Reset, see 3.10.3.8.
- b. Upon completion of the System Reset, the Busy F/F for Processor State 4 (Bit 04 of the Busy/Active Register) shall be set. This setting input shall be removed at the beginning of the first major cycle allocated to Processor State 4.
- c. On the first major cycle allocated to Processor State 4, the Control Storage address shall be forced such that micro-code execution begins at address 0112_{16} or 0113_{16} as determined by the Load Select switch described in 3.10.2.5.
- NOTE: At this point, the Autoload sequence shall be considered totally under micro-code control.
- d. Real Time Clock increment pulses shall be enabled at the set input of the Busy F/F for Processor State 4. This enable shall exist until a System Reset occurs. These increment pulses shall be further conditioned by the Executive Disable switch as described in 3.10.4.27.

3.10.2.5 Load Select: Primary/Alternate

This control shall be a toggle switch.

This switch shall determine the state of the right-most bit of the Control Storage Address generated during the Autoload sequence. In the Primary, (down) position, the right-most bit shall be set, resulting in a Control Storage Address of 0113_{16} . In the Alternate, (up) position, the right-most bit shall be clear, resulting in a Control Storage Address of 0112_{16} .

This switch shall also determine the device interface selected within the Control Storage Loader logic during the Reset/Load sequence. In the Primary, (down) position, the Control Storage Loader shall interface Integrated File Adapter-type (IFA) signals. In the Alternate, (up) position, the Control Storage Loader shall interface Integrated Card Adapter-type (ICA) signals.

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Equipm	ent Group	Sheet	132	
3.10.2.6	Speaker Volume			
	This control shall be a one-turn potentioned controls the potential volume level of the loudspeaker. Rotation of this control full clockwise shall reduce speaker volume to ir Rotation of this control fully clockwise sh the potential for maximum speaker volume.	eter wh Consol ly coun naudibi nall pr	nich le nter- llity. rovide	
	For a description of the digital inputs and effects on the console speaker's frequency see 3.10.3.5.	d their and vo	r relative olume	
3.10.2.7	Processor Fault		· · · · · · · · · · · · · · · · · · ·	
	This control shall be a momentary push-but an indicator.	ton swi	itch with	
	The indicator shall be on when any of the processor faults occur.	followi	ing	
	a. Control Storage Parity Error.			. · · · .
	b. Main Storage Parity Error	1. s		
	c. D.C. Fault			
	d. Over-Temperature Condition.	· ·		
	Depression of the Processor Fault switch sh correct nor initialize recovery activities these faults.	all n e for an	ither y of	
	When the indicator is on as a result of Con Storage Parity Error faults, depression of cause the indicator to be off. The indicat off until the switch is released and no fur Errors occur.	trol o the sw or sha ther P	or Main itch shal 11 remain arity	.1
	When the indicator is on as a result of a D or an Overtemperature Condition, the Proces switch shall have no effect.).C. Fa sor F	ult ault	
	Each of these Processor Faults shall have i indicators within the Maintenance Group con described in Section 3.10.4.	ndivid trols	ual as	
Form 4002-2A				/



3.10.2.8 I/O Fault

This control shall be a momentary push-button switch with an indicator.

The indicator shall be on when any of the following I/O faults occur.

a. Channel 1 Transmission Parity Error

b. Channel 2 Transmission Parity Error

c. Channel 1 Control Check Error

d. Channel 2 Control Check Error

e. Burst Check Error (during a Reset/Load sequence involving a File-type device only).

f. Failure of an IFA attached File to retract heads during the power down sequence.

Depression of the I/O Fault switch shall neither correct nor initialize recovery activities for any of these errors.

Depression of the I/O Fault switch shall cause the indicator to be off. The indicator shall remain off until the switch is released and no further I/O Faults occur.

Each of these I/O Faults shall have individual indicators within the Maintenance Group controls as described in Section 3.10.4.

3.10.2.9 Lamp Test

This control shall be a momentary push-button switch with an indicator.

When depressed, this switch shall cause all Console indicators to be on. When released, all Console indicators shall be off to the extent of the effects of this switch i.e. indicators shall remain on wherever the conditions for the on state otherwise exist.

When depressed, this switch shall also cause the Alarm to be audible. When released, the same effect for Alarm operation applies as for indicator operation as previously described.



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3.10.2.10 Alarm

The Alarm shall be an audible signal only. The Alarm shall be on when the Lamp Test Switch is depressed or when any of the following conditions exist within the System.

- a. Blower failure within the Processor, (interpreted as an over-temperature condition).
- b. A D.C. Fault.
- c. Failure of an IFA attached File to retract heads during the power-down sequence.

Each of these conditions could result in physical damage within the System. When blower failure or D.C. Fault conditions persist for approximately 60 seconds, the power-down sequence shall be automatically initialized. When the heads fail to retract during the power-down sequence, D.C. power within the Processor shall be removed but the power-down sequence shall be suspended at that point for as long as the heads remain extended.

3.10.2.11 Alarm Disable

This control shall be a momentary push-button switch with an indicator.

When the Alarm is audible, depressing the switch shall cause the Alarm to be off (disabled) and the Alarm Disable indicator to be on. When the switch is released and the condition(s) which cause the alarm no longer exists, the alarm shall be enabled (but inaudible unless and until fault conditions reoccur) and the Alarm Disable indicator shall be off.

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3.10.2.12 Reset/Load

This control shall be a momentary push-button switch with an indicator.

Depression of this switch shall initialize a Deadstart sequence, and the indicator shall be on until the switch is released. The Reset/Load sequence shall consist of the following:

- a. A System Reset shall be performed for a minimum of .4 m/s and a maximum of .6 m/s provided the Maintenance Group Controls have not been enabled. When the Maintenance Group Controls have been enabled, this System Reset shall be omitted from the Reset/Load sequence. For a description of the effects of System Reset, see 3.10.3.8.
- b. Upon completion of the System Reset when applicable, the Control Storage Loader shall transfer data into Control Storage using either a Primary or Alternate device adapter as the source, where the selection is determined by the state of the Load Select switch described in 3.10.2.5. For a description of the Primary and Alternate sequences and signal conventions, see 3.5.8 and 3.5.9, respectively.
- c. The Reset/Load sequence shall write data into Control Storage proper until all addresses present have been written, (16,384 words maximum, 1024 word increments), and shall then write data into the Address Table until all addresses present have been written (1024 words maximum, 256 word increments). The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.
- d. Upon completion of the Reset/Load Sequence, an Autoload sequence shall be initialized provided the Maintenance Group Controls have not been enabled.

For additional details concerning the Reset/Load Sequence, see 3.5.7, 3.5.8, and 3.5.9.

	OREX ENGINEERING SPECIFICATION	Nui
3.10.3	Programmer Group	
	This group of controls shall be enabled onl Console is in Program Mode or Maintenance M Console is not in Program Mode and not in M the switches within this group shall have n However, indicators within this group shall all times.	y lodd lain .o d
3.10.3.1	Program Mode	
	This control shall be a push-on, push-off s indicator. The indicator shall be on only Console is in Program Mode, i.e. the indic off when the Console is in Maintenance Mode	wi whe
	Depression of the Program Mode switch to th shall enable all controls in the Program Gr	e o ouj
	Depression of the Program Mode switch to th shall disable all controls in the Program G the Maintenance Mode switch is also off.	e (roi
	Note: Program Mode and Maintenance Mode sh exclusive and Maintenance Mode shall have p both selections are made simultaneously.	all rec
3.10.3.2	Console Address Register Display (20 bits)	
	These 20 controls shall be momentary, push- with indicators. These switches and indica horizontally positioned as 5 groups of 4 bi the left-most group, bits shall be individu from left to right, X0 through X3. Within 4 groups, bits shall be individually design to right, 00 through 15.	but to all the ate
	a. Console Address Register Display: X0 -	X3
• • •	These switches and indicators shall not unless the Relocation and Protection Fea in the 7300 Processor.	be atu
	In the presence of the Relocation and Pr and when enabled, depression of these sw cause corresponding bits to be set in th Portion of the Console Address Register indicators shall be on for corresponding that are set and off for corresponding by that are clear in the Segment Tag portion Console Address and PE Registers as det	rot wit on g b oit
• • •	Console Address Register Select describe	ed.

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3.1

when the e. When the ntenance Mode; effect. e enabled at

3.1

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tch with an en the or shall be

on position p.

off position up provided

1 be mutually cedence when

3.10

tton switches rs shall be each. Within ly designated e right-most ed from left

e functional ure is present

tection Feature, tches shall Segment Tag nly. The pit positions positions s of the S, rmined by the in 3.10.3.4.

	ENGINEERING SPECIFICATION	Number 882000 Sheet 137 of
	b. Console Address Register Display: 00 -	- 15
	When enabled, depression of these switc corresponding bits to be set in the Con Register only. The indicators shall be ponding bit positions that are clear in Address, and PE Registers as determined Address Register Select described in 3.	ches shall cause nsole Address e on for corres- n the Su, S, Console l by the Console .10.3.4.
3.10.3.3	Clear Address	
	This control shall be a momentary push-butt	ton switch.
	When enabled, depression of this switch sha bit positions of the Console Address Regist clear signal resulting from the depression shall continue until the switch is released	all clear all ter only. The of this switch l.
3.10.3.4	Console Address Register Select	
	This control shall be a rotary switch with designated positions. In a clockwise direc positions of this switch shall be designate Address, and PE.	4 panel tion, the ed Su, S,
	The Su and PE positions of this switch shal only when the Console is in Maintenance Mod in 3.10.4.1.	l be enabled le as described
	When enabled, the position of this switch d Su, S, Console Address, or PE Register cont mitted to the Console Address Register Disp In the presence of the Relocation and Prote the S position of this switch shall be furt by the System/Physical control described in	etermines whether ents are trans- lay indicators. ction Feature, her conditioned 3.10.3.14.
	The Console Address Register Select switch ridden by CS-RD and CS-WR selections at the Select switch as described in 3.10.3.11.	shall be over- Console Mode
	NOTE: When controls within the Programmer otherwise influence the selection of the Re contents are transmitted to the Console Add Display indicators, the contents of the Con Register shall be selected.	Group do not gister whose ress Register sole Address
. · ·		



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3.10.3.5 Console Data Register Display (20 Bits)

These 20 controls shall be momentary push-button switches with indicators. These switches and indicators shall be horizontally positioned as 5 groups of 4 bits each. Within the left-most group, bits shall be individually designated from left to right X0 through X3. Within the right-most 4 groups, bits shall be individually designated from left to right, 00 through 15.

a. Console Data Register Display: XO-X3

These switches and indicators shall not be functional unless the Relocation and Protection Feature is present in the 7300 Processor.

In the presence of the Relocation and Protection feature, and when enabled, depression of these switches shall cause corresponding bits to be set in the Segment Tag portion of the Console Data Register only. The indicators shall be on for corresponding bit positions that are set and off for corresponding bit positions that are clear in the Segment Tag portions of the Console Data Register only.

b. Console Data Register Display: 00 - 15

When enabled, depression of these switches shall cause corresponding bits to be set in the Console Data Register only. The indicators shall be on for corresponding bit positions that are set and off for corresponding bit positions that are clear at Fu2, Fu1, RTC, CSS, B/A, Console Data, D, Au, Bu, SUM or BC outputs as determined by the Console Data Register Select described in 3.10.3.7.

The digital inputs to the Console Data Register Display lamp drivers in bit positions 13, 14, and 15 shall also be used as inputs to the Console Speaker drivers. Bit 15 shall have minimum control on Speaker coil current, bit 14 shall have approximately twice the control of bit 15 (+3 decibels), and bit 13 shall have approximately four times the control of bit 15 (+6 decibels).

3.10.3.6 Clear Data

This control shall be a momentary push-button switch.

When enabled, depression of this switch shall clear all bit positions of the Console Data Register only. The clear signal resulting from the depression of this switch shall continue until the switch is released.

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3.10.3.7 Console Data Register Select

This control shall be a rotary switch, with 11 panel designated positions. In a clockwise direction the positions of this switch shall be designated Fu2, Fu1, RTC, CSS, B/A, Data, D, Au, Bu, SUM, and BC.

The Fu2, Fu1, RTC, CSS, D, Au, Bu, SUM and BC positions of this switch shall be enabled only when the Console is in Maintenance Mode as described in 3.10.4.1.

When enabled, the position of this switch determines whether Fu2, Fu1, RTC, CSS, B/A, Console Data, BC, or the output from the ALU shall be transmitted to the Console Data Register Display indicators. In the D, Au, Bu, and SUM positions, the output of the ALU shall be selected. The output of the ALU shall be controlled by micro-command except during Null State cycles. Thus, when enabled, and during Null State cycles, switch positions of D, Au, Bu, and SUM shall be effective in selecting these outputs for transmission to the Console Data Register Display indicators.

The Console Data Register Select switch shall be over-ridden by CS-RD and CS-WR selections at the Console Mode Select switch as described in 3.10.3.11.

NOTE: When Controls with the Programmer Group do not otherwise influence the selection of the Register whose contents are transmitted to the Console Data Register Display indicators, the contents of Console Data Register shall be selected.

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3.10.3.8	System Reset	
	This control shall be a momentary push-butt an indicator.	ton switch with
	When enabled, depression of this switch sha System Reset sequence and the indicator sha switch is released. The System Reset seque of the following:	all result in a all be on until the ence shall consist
	a. The output of the ALU shall be driven to state.	to the clear
	b. The eight (8) Pu Registers within the E File, Group I, shall be cleared.	Extended Register
	c. The B/A, T, G, PM, BC, CSS, Console Add Data Registers within the Extended Regi shall be cleared.	lress and Console ster File, Group II
	d. The Au, Bu, D and Forced Carry Register shall be cleared.	s within the ALU
	e. A reset signal shall be transmitted to Register File, Group III. (For the eff signal within the integrated adapters, appropriate document listed in 2.0).	the Extended ects of this see the
	f. The Resource Allocation Network shall b issue Null cycles only.	e forced to
	g. The timing mechanism shall be forced to minor cycles per major cycle, (E0 throu	issue ten(10) gh E9).
	h. The Su, Ful, and Fu2 Registers at the p Control Storage shall be cleared.	eriphery of
	i. The RTC Increment pulses shall be disab input of the Busy Flip-Flop for Process 04 of the Busy/Active Register).	led at the set or State 4, (Bit
	j. The logical inter-lock which is set by Stop operation with Processor State 4, disables the output of the Busy Flip/Fl State 4 from appearing at the input of Allocation Network), shall be cleared.	a Breakpoint (and when set, op for Processor the Resource
	k. In the presence of the Relocation and P Feature, the Addressing Mode Register s	rotection hall be cleared.
	The System Reset sequence resulting from th this switch shall continue until the switch	e depression of is released.

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3.10.3.9 Console Control Select: Stop/Step, Normal, Breakpoint

This control shall be a 3 position toggle switch.

When enabled, the position of this switch shall determine the mode in which Console Operations are performed. (Console Operations shall be selected by means of the Console Mode Select switch described in 3.10.3.11 and initialized by means of the Console Run Switch described in 3.10.3.10).

NOTE: Some Console Operations shall stop, despite the position of this switch, when error conditions occur as described in 3.10.3.11.

a. Stop/Step

In the Stop/Step, (up), position, this switch shall cause the Console Request Flip/Flop to clear at the beginning of E4 during all major cycles allocated to the Console State.

As a result, when Console Operations are already occurring, and this switch is moved to the Stop/Step position, the Console Operation shall stop, i.e. Stop Mode. For each initialization of Console Operation with this switch already in the Stop/Step position, a single major cycle shall be allocated to the Console, i.e. Step Mode. (Console Operation shall be initialized by means of the Console Run switch described in 3.10.3.10).

b. Normal

In the Normal, (center), position, this switch shall have no effect on the Console Request Flip/Flop, i.e. once initialized, Console Operation shall be performed continuously.

c. Breakpoint

In the Breakpoint, (down), position, this switch shall cause the Console Request Flip/Flop to clear at the beginning of E4 during all major cycles allocated to the Console in which a Breakpoint Comparison occurs and is applicable. (Console Operations for which Breakpoint stops are applicable are described in 3.10.3.11).

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3.10.3.10 Console Run

This control shall be a momentary push-button switch with an indicator. The indicator shall be on during all major cycles allocated to the Console State.

When enabled, depression of this switch shall result in a single pulse, approximately 100 n/s in duration at the set input to the Console Request Flip/Flop.

As a result, each depression of this switch, when enabled, shall initialize a Console Operation provided the Console Mode Select switch, as described in 3.10.3.11, is also in an ena ed position.

3.10.3.11 Console Mode Select

This control shall be a rotary switch with 9 panel designated positions. In a clockwise direction, the positions of this switch shall be designated RO-WR, RO-RD, RF-WR, RF-RD, OFF, MS-RD, MS-WR, CS-RD, and CS-WR.

The CS-RD and CS-WR positions of this switch shall be enabled only when the Console is in Maintenance Mode as described in 3.10.4.1.

When enabled, the position of this switch shall select the type of Console Operation to be initialized when the Console Run Switch is depressed.

a. RO-WR

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0100_{16} .

Micro-command sequences which would otherwise result in Main Storage Write operations shall be altered by hardware control into Register Option Write Operations.

Clocks shall be disabled at the micro-command translations for the Console Address Register .

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Equipment	Group ENGINEERING SPECIFICATION	Sheet 143 of
b.	RO-RD	
	This position of the Console Mode Sele have the following effects during all allocated to the Console State.	ct switch shall major cycles
	Micro-command execution shall be force Control Storage Address 0103 ₁₆ .	d to begin at
	Micro-command sequences which would ot Main Storage Read operations shall be hardware control into Register Option	herwise result in altered by Read Operations.
	Clocks shall be disabled at the Micro- for the Console Address Register.	command translations
c. ′	RF-WR	
	This position of the Console Mode Sele the following effects during all major to the Console State.	ct switch shall have cycles allocated
	Micro-command execution shall be force Control Storage Address 0106 ₁₆ .	d to begin at
	In the presence of the Relocation and I Feature, Micro-command sequences which Register File Write operations in Bound Mode shall be supplemented by hardware include participation of the Segment Ta Basic Register File.	Protection perform dary Crossing control to ags for the
d.	RF-RD	
	This position of the Console Mode Selechave the following effects during all rallocated to the Console State.	ct switch shall major cycles
	Micro-command execution shall be forced Control Storage Address 010C ₁₆ .	d to begin at
	In the presence of the Relocation and H micro-command sequences which perform H Read operations in Boundary Crossing Mo supplemented by hardware control to inc of the Segment Tags for the Basic Regis	Protection Feature, Register File ode shall be clude participation ster File.



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e. OFF

This position of the Console Mode Select switch shall cause a clear signal at the Console Request Flip/Flop. This clear signal shall continue until the switch is moved from the OFF position.

NOTE: A Clear signal shall also be provided to the Console Request Flip/Flop during the time the Console Operation Select switch is between positions. Thus a change in Console Operation Selection while the Console is running shall result in stopping the Console Operation.

f. MS-RD

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This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 0103_{16} .

The Console Request Flip/Flop shall be cleared at the beginning at E7 when the Micro-command sequence performs a Main Storage Read and a Parity Error occurs, (an additional Main Storage reference for the Console shall not occur). This Parity Error stop shall be conditioned by the Storage Parity Disable control as described in 3.10.4.16.

The Console Request Flip/Flop shall be cleared at the beginning of E4 when the Micro-command sequence performs a Main Storage reference, the Main Storage Address compares bit- f_0 r-bit with the Breakpoint Address selection, and the Console Control Select switch is in the Breakpoint position.

The right-most 16-bits of the Console Address Register shall be cleared during E7 when the Micro-command sequence performs a Main Storage reference at an address which is not physically present, (Out of Range).

When the right-most bit (bit 15) of the Main Storage Address Register, S, is set, clocks shall be disabled at the Micro-command translations for the Console Address Register.
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NOTE: In the presence of the Relocation and Protection Feature, the contents of the Main Storage Address Register, S, shall be interpreted as either a System. or a Physical Main Storage Address as determined by the position of the Console Main Storage, Relocate/Off switch described in 3.10.3.12. Likewise, in the presence of the Relocation and Protection Feature, the Main Storage Address which is compared with the Breakpoint Address selection shall be either a System or Physical Main Storage Address as determined by the position of the System/Physical switch described in 3.10.3.14.

g. MS-WR

This position of the Console Mode Select switch shall have the following effects during all major cycles allocated to the Console State.

Micro-command execution shall be forced to begin at Control Storage Address 010016.

The Console Request Flip/Flop shall be cleared at the beginning of E4 when the Micro-command sequence performs a Main Storage reference, the Main Storage Address compares bit-for-bit with the Breakpoint Address selection, and the Console Control Select switch is in the Breakpoint position.

The right-most 16-bits of the Console Address Register shall be cleared during E7 when the Micro-command sequence performs a Main Storage reference at an address which is not rhysically present, (Out of Range).

When the right-most bit (bit 15) of the Main Storage Address Register, S, is set, clocks shall be disabled at the Micro-command translations for the Console Address Register.

NOTE:

In the presence of the Relocation and Protection Feature, the contents of the Main Storage Address Register, S, shall be interpreted as either a System or a Physical Main Storage Address as determined by the position of the Console Main Storage, Relocate/Off switch described in 3.10.3.12 Likewise, in the presence of the Relocation and Protection Feature, the Main Storage Address which is compared with the Breakpoint Address selection shall be either a System or Physical Main Storage Address as determined by the position of the System/Physical switch described in 3.10.3.14.



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CS-RD

This position of the Console Mode Select switch shall provide the means for selecting Control Storage Read operations to be performed under hardware control.

During Control Storage Read operations as initiated from the Console, the associated hardware sequences shall be mutually exclusive with Micro-command execution on the part of any Processor State.

This position of the Console Mode Select switch shall over-ride the Console Address Register and Console Data Register Select switches. The Console Address Register Display indicators shall be used in the right-most 16-bit positions to display the Control Storage address as contained in Su. The Console Data Register Display indicators shall be used in the right-most lo-bit positions to display Control Storage data as contained in the CSS Register for Control Storage proper, and as available at the input to the Pp Register for the Address Table.

During Control Storage Read operations, the contents of the Su Register shall be incremented by one at the beginning of each major cycle allocated to the Console State except on the first cycle following System Reset. Thus, the data indicated by the Console Address Register Display shall correspond to the contents of the Control Storage address indicated by the Console Address Register Display at the end of each major cycle allocated to the Console State.

In Stop/Step Mode, Control Storage Read operations shall reference a single Control Storage Address for each depression of the Console Run switch.

In Normal Mode, Control Storage Read operations initialized by depression of the Console Run switch shall attempt to scan all Control Storage locations physically present in the 7300 Processor. Longitudinal parity shall be checked for Control Storage proper and horizontal parity shall be checked for the Address Table. In the event of a Parity Error, the operation shall stop unless disabled by the Storage Parity Disable control described in 3.10.4. In the absence of a Parity Error stop, the complete scan shall occur repeatedly, including parity checking, until manually stopped from the Console.



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In Breakpoint Mode, Control Storage Read operations initialized by depression of the Console Run switch shall attempt to scan all Control Storage locations physically present in the 7300 Processor. In the event that the Control Storage address contained in Su compares bit-for-bit with the Breakpoing Address selection, the operation shall stop. If the operation stops in Control Storage proper, the Console Data Register Display shall indicate the cumulative longitudinal check word for the associated page of 256 words, up to and including the address indicated by the Console Address Register Display. In the absence of a Breakpoint stop, a complete scan shall occur repeatedly until manually stopped from the Console.

The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.19.

i. CS-WR

This position of the Console Mode Select switch shall provide the means for selecting Control Storage Write operations to be performed under hardware control.

During Control Storage Write operations as initiated from the Console, the associated hardware sequences shall be mutually exclusive with Micro-command execution on the part of any Processor State.

This position of the Console Mode Select switch shall over-ride the Console Address Register and Console Data Register Select switches. The Console Address Register Display indicators shall be used in the right-most 16-bit positions to display the Control Storage Address as contained in Su. The Console Data Register Display indicators shall be used in the right-most 16-bit positions to display data to be written into Control Storage as contained in the Console Data Register.

During Control Storage Write operations, the contents of the Su Register shall be incremented by one after the data transfer is performed during each major cycle allocated to the Console State. Thus, the data indicated by the Console Data Register Display shall correspond to the data to be written at the Control Storage address, indicated by the Console Address Register Display at the beginning of each major cycle allocated to the Console State.

In Stop/Step Mode, Control Storage Write operations shall write at a single Control Storage Address for each depression of the Console Run switch.



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In Normal Mode, Control Storage Write operations initialized by depression of the Console Run switch, shall attempt to write all Control Storage locations physically present in the 7300 Processor. Once initialized, a complete write operation shall occur repeatedly until manually stopped from the Console.

In Breakpoint Mode, Control Storage Write operations initialized by means of the Console Run switch shall attempt to write all Control Storage locations physically present in the 7300 Processor. In the event that the Control Storage address contained in Su compares bit-for-bit with the Breakpoint Address selection, the operation shall stop prior to writing at that address. In the absence of a Breakpoint stop a complete write operation shall occur repeatedly until manually stopped from the Console.

The sizes of Control Storage proper and the Address Table may be selected for maximums of 4096 words and 256 words, respectively, by means of the Select CS Minimum control as described in 3.10.4.19.

3.10.3.12 Console Main Storage, Relocate/Off

This control shall be a 2 position toggle switch.

In the absence of the Relocation and Protection Feature this switch shall have no effect.

When enabled and during major cycles allocated to the Console State for the purpose of referencing Main Storage, the position of this switch shall determine whether the contents of the S Register shall be interpreted as a System or Physical Main Storage Address. In the Relocate (up) position, the contents of the S Register shall be interpreted as a System Main Storage Address and shall be converted by the relocation mechanism into a Physical Main Storage Address. In the Off (down) position, the contents of the S Register shall be directly interpreted as a Physical Main Storage Address and shall by-pass the relocation mechanism.

3.10.3.13 Breakpoint Address Select

Each of these 5 controls shall be a 16-position rotary switch.

In the absence of the Relocation and Protection Feature, the left-most switch shall have no effect.

These switches shall supply a 20-bit Breakpoint Address selection, expressed as 5 digits in hexadecimal notation.



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	OREX ENGINEERING SPECIFICATION	Numbor Sheet	882000 150 •	
3.10.3.14	Breakpoint Mode Select: System/Physical			2
	This control shall be a 2-position toggle s	witch	•	
	In the absence of the Relocation and Protecthis switch shall have no effect.	tion	Feature	
	In the presence of the Relocation and Prote position of this switch shall determine whe Physical Main Storage Addresses shall be co Breakpoint Address selection. Likewise, th switch shall determine whether System or Ph Addresses shall be transmitted to the Conso Display indicators when the Select switch is the S position. System Main Storage Address selected as described when this switch is end System (up) position. Physical Main Storage be selected as described when this switch is the Physical (down) position.	ection ompare pos vysica ole Ad ses s enable ge Add s dis	Feature, System or d with th ition of 1 Main St dress Reg bled and hall be d and in resses sha abled or	the this orage ister in the all in
3.10.3.15	Breakpoint Mode Select: Read Instr/Øff This control shall be a 2-nosition toggle s	witch		
	When enabled and in the Read Instr (up) pos shall <u>enable</u> a Breakpoint stop for Processo 7 during major cycles which perform a Main by beginning Micro-command execution at Con Address X00X ₁₆ , i.e. RNIX, see 3.5.2.	ition r Sta Stora trol	• , this sw: tes 0 thro ge referen Storage	itch bugh ice
	In the Off (down) position, this switch sha Breakpoint stop enable just described.	11 no	t provide	the.
3.10.3.16	Breakpoint Mode Select: Read Data/Øff		· · ·	
	This control shall be a 2-position toggle s	witch	•	
	When enabled and in the Read Data (up) posi shall <u>enable</u> a Breakpoint stop for Processo 7 during major cycles which perform a Main reference by beginning Micro-command execut Storage Addresses other than X00X ₁₆ , i.e. n	tion, r Sta Stora ion a ot RN	this swit tes 0 thro ge <u>read</u> t Control IX, see 3.	ch bugh

In the Off (down) position, this switch shall not provide the Breakpoint stop enable just described.

3.10.3.17 Breakpoint Mode Select: Write Data/Øff

This control shall be a 2-position toggle switch.

When enabled and in the Write Data (up) position, this switch shall enable a Breakpoint stop for Processor States 0 through 7 during major cycles which perform a Main Storage write reference by beginning Micro-command execution at Control Storage addresses other than X00X16, i.e., not RNI, see 3.5.2.

In the Off (down) position, this switch shall not provide the Breakpoint stop enable just described.





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Note: When a Breakpoint Stop is performed for Processor State 4, the output of the Busy Flip/Flop for this Processor State shall be disabled at the input to the Resource Allocation Network. Independent of its Busy Flip/Flop, major cycles shall not be allocated to Processor State 4 until this disable is removed by restarting Processor State 4 through the use of the Processor Run and Select Controls described in 3.10.3.19 and 3.10.3.20, respectively, or until the occurrence of a System Reset as described in 3.10.3.8.

3.10.3.19 Processor Run

This control shall be a momentary push-button switch with an indicator. The indicator shall be on when the switch is enabled and depressed, and remain on until the switch is released or disabled.

When enabled, depression of this switch shall result in a single pulse at the set input of each Busy Flip/Flop in the B/A Register. This pulse shall be further conditioned at these set inputs, by the position of the Processor Select control described in 3.10.3.20.

The leading edge of the Run pulse shall occur upon depression of the Run switch and the trailing edge of the Run pulse, independent of the Run switch, shall occur at the beginning of the major cycle allocated to the Processor State selected by means of the Processor Select Control described in 3.10.3.20.

3.10.3.20 Processor Select

This control shall be a rotary switch with 8 manel designated positions. In a clockwise direction, the positions of this switch shall be designated 0 through 7.

The position of this switch shall enable the Run pulse described in 3.10.3.19 at the set input of an individual Busy Flip/Flop, corresponding to the Processor State number 0 through 7 selected.

3.10.3.21 Processor State Display

This Display shall consist of 8 indicators designated from left to right as 0 through 7.

During each major cycle allocated to Processor States 0 through 7, the corresponding indicator shall be on.



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3.10.4 Maintenance Group

Controls within this group shall be enabled only when the Console is in Maintenance Mode unless otherwise specified. However, indicators within this group shall be enabled at all times.

3.10.4.1 Maintenance Mode

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on only when the Console is in Maintenance Mode.

Depression of the Maintenance Mode switch to the on position shall place the Console in Maintenance Mode. All controls in the Maintenance and Program groups shall be enabled and the Program Mode indicator shall be off.

Depression of the Maintenance Mode switch to the off position shall remove the Console from Maintenance Mode. All controls in the Maintenance Group shall be disabled unless otherwise specified. All controls in the Program Group shall be restored to dependency on the state of the Program Mode switch, including the state of the Program Mode indicator.

3.10.4.2 MS Parity Byte 0

This control shall consist of an indicator only.

In the absence of the ECC Feature, this indicator shall display the state of the parity bit associated with the left-most byte of data as supplied by Main Storage. The indicator shall be on when the parity bit is set and off when the parity bit is clear.

In the presence of the ECC Feature, this indicator shall be off.

3.10.4.3 MS Parity Byte 1

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This control shall consist of an indicator only.

In the absence of the ECC Feature, this indicator shall display the state of the parity bit associated with the right-most byte of data as supplied by Main Storage. The indicator shall be on when the parity bit is set and off when the parity bit is clear.

In the presence of the ECC Feature, this indicator shall be off.



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3.10.4.4 MS Parity Error

This control shall consist of an indicator only.

This indicator shall display the state of the Main Storage Parity Error Flip/Flop. The indicator shall be on when the Main Storage Parity Error Flip/Flop is set and off when the Main Storage Parity Error Flip/Flop*is clear.

In the absence of theECC Feature, this Parity Error Flip/Flop shall set during Main Storage read references in which the total number of bits in the set state, including the parity bit, is even for either the left-most or right-most byte positions.

In the presence of the ECC Feature, this Parity Error Flip/Flop shall set during Main Storage read references in which non-correctable data errors are detected by the ECC Feature.

The Main Storage Parity Error Flip/Flop shall not set during Main Storage references to "Out of Range" or "Out of Bounds" addresses but shall set independently of the Storage Parity Disable control described in 3.10.4.16.

Once set, the Main Storage Parity Error Flip/Flop shall be cleared only by means of a System Reset or operation of the Processor Fault control described in 3.10.2.7.



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3.10.4.5 CS Parity Error

This control shall be an indicator only.

This indicator shall display the state of the Control Storage Parity Error Flip/Flop. The indicator shall be on when the Control Storage Parity Error Flip/Flop is set and off when the Control Storage Parity Error Flip/Flop is clear.

The Control Storage Parity Error Flip/Flop shall set for each of the following:

- a. When a Micro-command as contained in the Fu2 Register consists of an even number of bits in the set state for any Processor State other than the Null State.
- b. When the longitudinal check character as contained in the CSS Register reflects an even number of bits in any bit position column on a 256 word Page basis, during Control Storage Read operations initiated from the Console in Normal Mode (for Control Storage proper, only).
- c. When the output of the Address Table, whether referenced by Micro-command or by hardware Control Storage Read operation, contains an even number of bits in the set state.

The Control Storage Parity Error Flip/Flop shall set independently of the Storage Parity Disable Control described in 3.10.4.16.

Once set, the Control Storage Parity Error Flip/Flop shall be cleared only by means of a System Reset or operation of the Processor Fault Control described in 3.10.2.7.

3.10.4.6 D.C. Fault

This control shall be an indicator only.

This indicator shall be on when any D.C. power supply within the 7300 Processor is not within its associated allowable output range for normal operation. The indicator shall remain on for as long as such a condition persists.



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3.10.4.7 Overtemperature

This control shall be an indicator only.

This indicator shall be on as a result of either a blower failure or an overtemperature condition within the 7300 cabinet. These conditions shall result in an audible Alarm and in the event that they persist for approximately 60 seconds, a power-down sequence shall be initialized. See 3.10.2.10.

3.10.4.8 Heads Extended

This control shall be an indicator only.

This indicator shall be on when the heads in one or more IFA attached Files fail to retract during a powerdown sequence. This condition shall result in an audible Alarm and suspension of the power-down sequence as described in 3.10.2.10.

3.10.4.9 Burst Check

This control shall be an indicator only.

This indicator shall be on when a Burst Check Error is detected during a Reset/Load sequence involving a File as the input device.

Once detected, the Burst Check Error indicator shall remain. on until a System Reset occurs, (a System Reset shall occur during the initialization of a Reset/Load sequence when the Console is not in Maintenance Mode.

3.10.4.10 Channel 1 Data Check

This control shall consist of an indicator only.

This indicator shall display the state of the Channel 1, Transmission Check Flip/Flop/ The indicator shall be on when the Transmission Check Flip/Flop is set and off when the Transmission Check Flip/Flop is clear.

The Channel 1 Transmission Check Flip/Flop shall set when the I/O Channel detects a parity error on incoming data, i.e. a byte of data from an adapter in which the total number of bits in the set state, including the parity. bit, is even.

Once set, the Channel 1 Transmission Check Flip/Flop shall be cleared only under Micro-command control or by means of a System Reset.



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Channel 1 shall be associated with Processor State 1 and shall provide the corresponding Extended Register, Group III facilities as described by the appropriate document listed in 2.0.

In the absence of Channel 1 this indicator shall be off. 3.10.4.11 Channel 1 Control Check

This control shall consist of an indicator only.

This indicator shall display the state of the Channel 1, Control Check Flip/Flop. The indicator shall be on when the Control Check Flip/Flop is set and off when the Control Check Flip/Flop is clear.

The Channel 1 Control Check Flip/Flop shall set when the I/O Channel detects concurrence of more than one Tag In Line (Address In, Service In, Data In and Status In; or Select In and Operational In) or concurrence of Command Out and Service Out.

Once Set the Channel 1 Control Check Flip/Flop shall be cleared only under Micro-command control or by means of a System Reset.

In the absence of Channel 1 this indicator shall be off.

3.10.4.12 Channel 2 Data Check

This control shall consist of an indicator only.

This indicator shall provide a display for Channel 2, associated with Processor State 2, equivalent to the Channel 1 Data Check described in 3.10.4.10.

3.10.4.13 Channel 2 Control Check

This control shall be an indicator only.

This indicator shall provide a display for Channel 2, associated with Processor State 2, equivalent to the Channel 1 Control Check described in 3.10.4.11.



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3.10.4.14 Select Even Parity, Byte 0

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

In the presence of the ECC Feature, this switch shall have no effect.

In the absence of the ECC Feature, when enabled, and when depressed to the on position, this switch shall cause the parity bit associated with the left-most 8 bits of data transmitted to Main Storage to be generated such that the total number of bits in the set state, including this parity bit, is even. Thus all Main Storage write references performed under these conditions shall result in Main Storage Parity Error detection during subsequent Main Storage read references at the affected Main Storage Addresses.

When disabled or depressed to the off position, this switch shall have no effect.

3.10.4.15 Select Even Parity, Byte 1

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

In the presence of the ECC Feature this switch shall have no effect.

In the absence of the ECC Feature, when enabled, and when depressed to the on position, this switch shall cause the parity bit associated with the right-most 8 bits of data transmitted to Main Storage to be generated such that the total number of bits in the set state, including this parity bit, is even. Thus, all Main Storage write references performed under these conditions shall result in Main Storage Parity Error detection during subsequent Main Storage read references at the affected Main Storage Addresses.

When disabled or depressed to the off position, this switch shall have no effect.





3.10.4.19 Select CS Minimum/Off

This control shall be a push-on, push-off switch with an indicator. The indicator shall be on when the switch is enabled and depressed to the on position. The indicator shall be off when the switch is disabled or depressed to the off position.

When enabled and in the Select CS Minimum (up) position, this switch shall select Control Storage sizes of 4096 words maximum for Control Storage proper and 256 words maximum for the Address Table.

NOTE: Hardware control information relative to the sizes of Control Storage proper and the Address Table shall be effective only during Console Control Storage Read, Console Control Storage Write and Reset/Load operations.

When disabled or depressed to the off position, this switch shall have no effect.

3.10.4.20 Set D, Set Au, Set Bu

These controls shall consist of 2 push-on, push-off switches with individual indicators. The left-hand switch shall be additionally designated "Set Au" and the right-hand switch shall be additionally designated "Set Bu". For each of these switches, the indicator shall be on when the switches are enabled and the associated switch is depressed to the on position.

- a. When enabled and depressed to the on position, the Set Au switch shall result in the setting of the 16-Flip/ Flops comprising the Au Register during every minor cycle the switch remains in the enabled on position.
- b. When enabled and depressed to the on position, the Set Bu switch shall result in the setting of the 16 Flip/ Flops comprising the Bu Register during every minor cycle the switch remains in the enabled on position.
- c. When both the Au and Bu switches are enabled and depressed to the on positions simultaneously, the 16 Flip/Flops comprising the D Register shall be set for every minor cycle these switches remain in the enabled on positions. Likewise, a carry shall be forced into the right-most bit position of the Adder.

When disabled or depressed to the off position, these switches shall have no effect.

PAISMA	OREX	ENGINEEDING ODEOLEICATION	Number 882000
'Equipme	ent Group	ENGINEERING SPECIFICATION	Sheet 161 of
3.10.4.21	Time Meter		
	This control	. shall be a 7 decimal digit m	neter.
	This meter s which logic The meter sh and shall op	hall provide the total accumu power has been applied to the all provide this reading in h perate independently of Consol	ulated time during 7300 Processor. nundredths of hours Le Maintenance Mode.
3.10.4.22	Voltmeter		
	This control independent1	shall be a linear scale mete y of Console Maintenance Mode	er and shall operate
	This meter s in per cent at scale cen low voltage indicate hig or negative the Voltage	hall provide power supply vol deviation from nominal values ter. Meter deviations to the magnitudes and deviation to t h voltage magnitudes regardle character of the voltages sel Select control described in 3	tage measurements , with 0% deviation e left shall indicate the right shall ess of the positive ected by means of 5.10.4.23.
3.10.4.23	Voltage Sele	ct	
	This control designated p of this swit +19.8, +12,	shall be rotary switch with ositions. In a clockwise dir ch shall be designated OFF, + +5A, +5B, +5C, +3, -3, -5, -1	14 panel ection the positions 28, +24, +23.3, 2 and OFF.
	The numerica select the a Voltmeter de	lly designated positions of t ssociated voltage for measure scribed in 3.10.4.22.	his switch shall ment by means of the
	When in the reading at t	Off position, this switch sha he Voltmeter.	ll select a 0%
3.10.4.24	Logic A, Log	ic B, Main Storage Adjusts	
	These contro Each of thes	ls shall consist of 3 ten-tur e potentiometers shall be scr	n potentiometers. ew driver adjustable.
	These contro "Logic A", " the means fo of Console M	ls shall be designated from 1 Logic B", and "Main Storage" r adjusting the associated vo aintenance Mode.	eft to right, and shall provide ltages independently

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3.10.4.25 Power Mode, Remote/Local

This control shall be a 2-position toggle switch and shall operate independently of Console Maintenance Mode.

In the Remote (up) position, this switch shall place the 7300 Processor power system in Remote Control Mode. For a description of Remote Control Mode, see the appropriate document listed in 2.1.

In the Local (down) position, this switch shall place the 7300 Processor power system in Local Mode, under control of the Power On and Power Off switches described in 3.10.2.2 and 3.10.2.3 respectively.

The position of this switch shall not effect the operation of the Emergency Pull control described in 3.10.2.1.

3.10.4.26 Executive Disable/Off

This control shall be a 2-position toggle switch.

When enabled and in the Executive Disable (up) position, this switch shall disable a set input to the Busy Flip/Flop for Processor State 4 (Bit 04 of the B/A Register). The set input disabled by this switch shall occur for each increment of the RTC Register provided the additional enable described in 3.10.2.4 is satisfied.

In the Off (down) position, this switch shall have no effect.

3.10.4.27 Cycle Step/Off

This control shall be a 2-position toggle switch.

When enabled and in the Cycle Step (up) position, this switch shall enable a clear input to the appropriate Busy Flip/Flop in the B/A Register at the beginning of E4 for each major cycle allocated to Processor States 0 through 7.

This clear input to each of the Busy Flip/Flcps shall be further conditioned on an individual basis by the Stop/Step (up) position of the appropriate Processor Operation Mode control as described in 3.10.3.18.

In the Off (down) position, this switch shall have no effect.



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Sheet 164

3.10.5.4 Data Set Ready (CC)

When on, the indicators within this row shall indicate that the associated Channel is connected to a Communication line and has completed the transmission of the answer tone.

3.10.5.5 Secondary Received Line Signal Detector (SCF)

When on, the indicators within this row shall indicate that the associated Channel has properly received the Secondary Channel Line signal where applicable.

NOTE: This signal shall be used to indicate circuit assurance status and thus, signal the interrupt condition.

3.10.5.6 Received Line Signal Detector (CF)

When on, the indicators within this row shall indicate that the associated Channel modem is receiving a signal which meets its suitability criteria for demodulation, and in the case of half duplex Channels, that the Line Adapter is in receive mode.

3.10.5.7 Clear to Send (CB)

When on, the indicators within this row shall indicate that the associated Channels are in a transmit condition.

3.10.5.8 Transmitted Data (BA)

When on, the indicators within this row shall indicate that the associated Channels are in the spacing condition, binary zero.

When off, the indicators within this row shall indicate that the associated Channels are in the marking condition, binary one.

3.10.5.9 Received Data (BB)

When on, the indicators within this row shall indicate that the associated Channels are in the spacing condition, binary zero.

When off, the indicators within this row shall indicate that the associated Channels are in the marking condition, binary one.

NOTE: Depending on the Transmission Facility utilized by each Communications Channel, certain Status Indicators as described in 3.10.5.1 through 3.10.5.9 may not be applicable.

MEM	OREX	Number	882000
	ent Group	Sheet	165 of
3.11	Reliability, Availability, Serviceability		
	The design parameters described in 3.1.10 the implementation of the 7300 Processor, sufficient reliability characteristics as the MTBF goal described in 3.11.1.	with restant	espect to contribute ed to achieve
	Console capabilities described in 3.10.2 th as well as modular packaging of the 7300 P shall contribute sufficient serviceability as required to achieve the MTTR goal, desc provided such hardware characteristics are means of exerciser, fault detection and fau procedures, including software/firmware roo	hrough rocesso charao ribed comple ult iso utines	3.10.4, or elements, cteristics in 3.11.2, emented by olation
3.11.1	MTBF	•	
	The mean time between failure goal for the the 7300 Processor shall be 4,000 hours (Fa. 25/1000 hours).	CPU po ailure	ortion of Rate =
3.11.2	MTTR		
	The mean time to repair goal for the 7300 be 2 hours.	Process	sor shall
3.12	Mechanical		
	The 7300 Processor cabinet, including the (be physically dimensioned according to Figu (Conceptual cabinet sketch is provided by) reference only).	Console ure 15 Figure	e, shall and 16. 17 for
	Maximum weight shall be 1350 lbs.		
3.13	Environmental		
	The Memorex 7300 shall conform to 882020 wi exception:	th the	following
	Acoustical Noise; Noise shall not exceed 35	db.	
3.14	Power System	1. 	
	The 7300 Processor power system shall confo with input voltages of 208/230V, 50 or 60 H	orm to Iz.	882059

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ME	EMO	REX
Equi	ipment	Grou

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Sheet 166 of

4.0 QUALITY ASSURANCE PROVISIONS

This section establishes requirements and procedures implemented to produce a product with maximum performance and reliability.

4.1 Components

In the context of this section, components shall be construed to include all piece parts from which the Processor is constructed.

All components shall be documented and controlled to a sufficient degree to assure proper form, fit, and function.

Components which significantly affect performance and reliability, and which are purchased by Memorex for use in the product shall be procured only from sources which have been determined to be acceptable by Component Engineering.

All components shall be purchased and inspected in accord with all applicable documentation. Components which do not meet all requirements shall not be used without the prior written authorization of the cognizant engineering group.

4.2 Construction

The machine shall be constructed and inspected in accordance with all applicable engineering drawings and specifications. Construction processes and techniques shall be such that no damage or subsequent degradation results to any component.

Prior to shipment, each machine shall be operated for at least 50 hours (power-on time) under the approved Final System Inspection procedure. This inspection shall verify all mechanical and electrical operations of the machine. The machine shall be powered by an A-C input which is equivalent to the destination requirements. During this inspection, each machine shall be exercised with appropriate software to demonstrate, with the highest possible confidence level, the software execution required by the particular configuration.

4.4 Qualification Testing

A complete qualification test in accord with 882038 shall be run periodically to assure conformance with all provisions of applicable specifications.

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4.3

	NREY	Number 882000
Equipmer	t Group	Sheet 167 of
5.0 F	PREPARATION FOR DELIVERY	
2 (Shipment of the machine shall require separ Console Table from the Main Cabinet. Disco Shall be clearly labeled to facilitate rapi in the field.	ration of the onnected wiring id reconnection
1 1 0	All doors and removable panels shall be see shut by tape or strapping. Particular care taken not to scratch or mar painted surface bend any sheet metal. No straps shall be p cross the console panel to prevent damage to	curely fastened e shall be es, or to permitted to to the controls.
S I 1 C	Standard shipment shall be by electronic particle of the standard shipment shall be designed for optimum protections mode of transportation. Special cratical special to meet the requirements for air starts for alternate methods of surface shipment.	added van, and otection under ing shall be shipment and
I I S C S I I I	Prior to packing, Quality Assurance shall or required inspection has been performed. An check during packaging to insure that appro- pecifications are followed and that extern of the packages is correct and legible. The chall check the units on the van to insure the downs and blocking are used, and shall the shipment when all requirements are met.	verify that all n inspector shall oved packing nal marking ne inspector that adequate only release
		:

			Number 88200C
		ENGINEERING SPECIFICATION	Sheet 168 ef
6.0	NOTES		
	With respec have been u	t to the 7300 Processor the fused inter-changeably:	ollowing terms
	Console Add	lress Register - M Register	
	Console Dat Logical One Logical zer Read Instr Read Data -	a Register - N Register - "1", high, set. o - "0", low, clear - RNI (Read Next Instruction) ROP (Read Operand)	
	Reset - Cle Reset/Load	ar , - Deadstart	
	Run - Go, (Selectable	Processor States 0 through 7) Register Features - Register	Option .
	Store Data System Cont	- STO (Store Operand) rol Panel - Console	
	System Rese	t - Master Clear	
	· · · ·		
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MEMOREX
Equipment Group

Number 882000

MEMONTC	FORMAT	BLOCK-	PEGI CPOU	STER	FILE ADDR	ESSABILITY	MINOR	CYCLES
MARMONIC	FUNIAI	FUINI	F	Pu	II	III		
AND	1	x	X	x	x	X	1	1
CIOI		X	+	<u> </u>			1	8
CI02		X	1		· ·		1	8
CLA	1	1	X	X	X	Х	1	1
CLR	1	X	X	X	<u> </u>	X	1	1
CMP	1	X	X		Х		1	2
CHU	1	X	X		Х		1	2
CORC			1				1	1
DFA	. 1		X	X	X		1	4
DIG	1						1	1
DLS	1		1				2	2
DRS			1				2	2
DSUM	1	Х	X		Х		1	2
DTA	1		X	X	X		1	4
DTAN	1		X	X	Х		1	4
EBL	:						1	1
EBU				ŀ			1	1
EOR	1	Х	X		X	X	1	1
FNJ		Х	T	X			1	2
FRJ		Х		X			1	8
FZJ		X		X			1	8
IDX	1		X	X	<u>х</u> .		1	4
IOR	1	X	X		X	X	1	1
IVK							1	1
JMP		X	li .	X	-		1	2
LAB	1		X	X	Х	X	1	1
LAW	1		X	X	X	Х	1	1
LAW	1		X	X	X	X	1	1
LBB	3						1	1
LBB	3		1				1	1
LBL			X	X	Х	X	1	1
LBW	1		X	Y	X	X	1	1
LBW	TI		XI	IXI	X	Х	1	1

FIGURE 9: MICRO-COMMAND CHARACTERISTICS

NOTE: Minor cycle minimums and maximums do not account for special minor cycles of E0", E0", E8 and E9.

MEM	OREX	7 ENGI	NEEDI	NCC	DEMEICATI	<u></u>	Numbo	882000)
Equipme	nt Group		NEEMI		rewritmin		Sheet	178	
وروار المرافقة والمتكارية الموجوع والموارية والمراجعة		1	REGIS	TER	FILE ADDRE	SSÁBI	LITY	INNOR	CYCLES
MNEMONIC	FORMAT	BLOCK- POINT	GROU F	JP I Pu	GROUP I I	GRC II	UP I	MIN.	MAX.
LDB	1		x	x	X	X	[1	1
LDW	1	1	X	X	X	X		I	
LDW	1		X	X	X	X		1	I
LSE	1		X	X	X			1	7
LSF	1		X	Х	X			1	7
LS1	1	· .	<u>X</u>	X	X			1	7
LS2	1	1	<u> </u>	X	X			1	7
NOP			2					1	1
RNI1		<u>X</u>	<u> </u>	<u>X</u>	Χ			11	<u> </u>
. <u>RNI2</u>		χ	<u>X</u>	<u>X</u>	<u>X</u>			1	<u> </u>
ROM		<u>X</u>	,					3	8
RVK								<u>i 1</u>	i
SDB	1	<u>X</u>	X		<u> </u>	<u> </u>		1	5
<u>SDW</u>	1	X	<u>X</u>		X	X	(1	5
SHF			1	L				2	2
SHR		1	1			L		2	2
SKB	2	X	<u> </u>	-				<u> 1</u>	2
SKB	2	X		L				<u>i 1</u>	2
SKE		<u> </u>						1	2
SKE		X						1	2
SKG		<u>X</u>		<u> </u>				1	2
SKL		X						1	2
SKN		<u>X</u>						1	2
SKZ		X						1	2
SRO								2	2
SR1				·				2	2
SSO								2	2
SS1		-						2	2
STA	1	X	X	X	X	X		1	2
STB	1	X	X	X	X	X		1	2
SUM	1	X	X		X			1	2
SYNC		X						1	8
	:						· ·	•	

FIGURE 9: (CONTINUED) MICRO-COMMAND CHARACTERISTICS

NOTE: Minor cycle minimums and maximums do not account for special minor cycles of E0', E0", E8 and E9.






N CAR		Nun" er 882095
Equipment an	aroup	
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		•••
REC	EIVED DATA	9 10 11 12 13 14 15
COMMUNICATIONS CLE	AR TO SEND	
ACT ITY RUN DISPLAY SEC GROUP DE	RCVD LN SIG	
DAT	A SET READY	
RIN	G INDICATOR	
¥		

FIGURE 13: 7300 CONSOLE COMMUNICATIONS ACTIVITY

Frim ADA27A

DISPLAY GROUP







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