7300022

RGB -GRAPH

Color Graphics Controller

MANUAL NO. 167MO-05A-1

matrox
electronic systems

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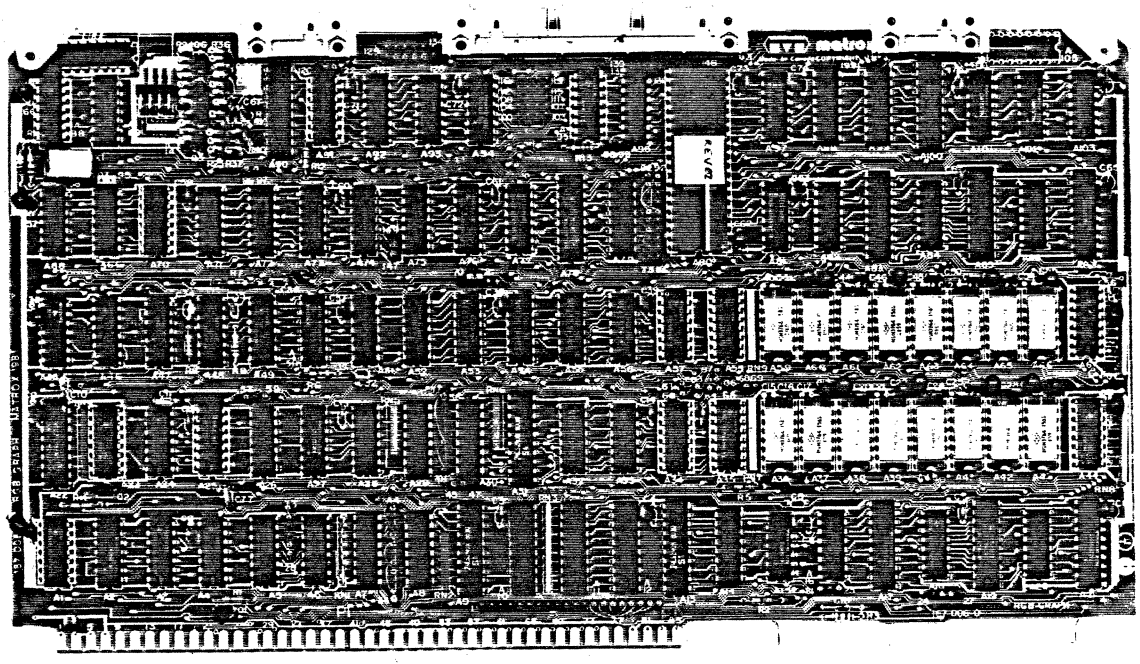
Color Graphics Controller

MANUAL NO. 167M0-05A-1

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

FEATURES

- 512 x 512 x 4 or 1024 x 512 x 2 SOFTWARE SELECTABLE RESOLUTION
- MULTIBUS® PLUG-IN
- 4 BIT PLANES
- PAN and SCROLL
- VECTOR PLOT
- EXPANDABLE
- SCREEN PRESET
- BIT PLANE WRITE ENABLE
- INDEPENDENT X and Y ZOOM
- DMA TRANSFERS
- HARDWARE CLIPPING
- VIDEO BUS
- LIGHT PEN INTERFACE
- VIDEO OUTPUT ENABLE
- PROGRAMMABLE DISPLAY FORMAT



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1.0 SPECIFICATIONS:

Bus:

- Multibus plug-in.
- 8 or 16 bit CPU.

Resolution:

- RGB-Graph/16-1. 256 pixels x 256 pixels x 1 bit
- RGB-Graph/16-4. 256 pixels x 256 pixels x 4 bits
- RGB-Graph/32-1. 512 pixels x 256 pixels x 1 bit
- RGB-Graph/32-4. 512 pixels x 256 pixels x 4 bits
- RGB-Graph/64-1. 512 pixels x 512 pixels x 1 bit*
- RGB-Graph/64-4. 512 pixels x 512 pixels x 4 bits*
- The horizontal resolution of the -4 models can be doubled by sacrificing two bit planes.

*On 480 pixels of the 512 pixel vertical resolution are displayed at any given time.

Display Memory Access:

- Normal: programmed I/O via X and Y address registers and data port.
- DMA: occupies 1K of system memory space.
- Access Time from CMD to XACK/:
  - 500 ns to Address Register, Data Register, Status Register, and Vector Register.
  - 50 ns to all other locations (DMA included) if no internal cycle resulting from a previous access is in process; if a subsequent access is made while an internal cycle is still in process, XACK/ will not be generated until that cycle is ended. See Table 1.1 for access cycle times.

RGB-GRAPH	X-Y ZOOM	CYCLE TIME (10.000MHz XTAL)		
		BEST TIME	AVERAGE	WORST TIME
/16	X1	800ns	1460ns	2.4us
	X2	800ns	1230ns	2.4us
	X4	800ns	1020ns	2.4us
/32 AND /64	X1	400ns	730ns	1.2us
	X2	400ns	615ns	1.2us
	X4	400ns	510ns	1.2us

Table 1.1 - CYCLE TIMES

Special Functions:

- Independent X and Y Zoom:
  - X-Zoom by 1,2,3,4,5,6,7, or 8
  - Y-Zoom by 1,2, or 4
- Scroll and Pan:
  - horizontal pan with single pixel precision
  - vertical scroll with 8 pixel precision
- Fast preset of display to value in data port.
- DMA access to the Display Memory.
- Light Pen Register.
- Vector Plot.
- Access to each bit plane can be independently software disabled.

1.0 SPECIFICATIONS (Cont'd):

- The video output from each bit plane can be independently software disabled.
- The TTL video outputs can be put in high impedence mode by software.
  - Allows several RGB-Graphs to occupy the same position on the video bus.
  - Allows more than one RGB-Graph to use the same monitor.
- The fourth bit plane can be superimposed on the others.
- Single or continuous frame grab with external frame grabber.
- Clipping of X and Y Registers.
- Grey scale DAC (functional only on boards with 4 bit planes).

Video Bus:

- 16 bits of graphics video
- 8 bits of frame grab data
- Sync and control signals
- Allows use of the RGB-Graph in groups of up to 4 (16 bits/pixel).
- Allows use of the RGB-Graph with the RGB-Alpha alphanumeric controller.
- Allows use of the RGB-Graph with the VAF board.

I/O:

- Occupies 16 I/O locations
- 8 or 12 bit I/O addresses
- Board I/O space can be strap-positioned on any 16 address boundary.

T.V. Standard:

- European (50 Hz) or American (60 Hz) operation.
- Fully functional with 10 MHz RGB monitor.
- Grey scale functions with 10 MHz black and white monitor.
- Functional with standard and direct drive monitors.

Connectors:

- P1, standard Multibus 86 pin edge connector: bus signals.
- J1, 10 pin right angle header AMP # 87578-2: composite video.
- J2, 10 pin right angle header AMP # 87578-2: outputs for direct drive monitors.
- J3, 50 pin right angle header MOLEX # 10-55-3505 (# 6874): video bus.
- J4, 10 pin right angle header MOLEX # 10-55-3103 (# 4700): light pen signals.

1.0 SPECIFICATIONS (Cont'd):

Power Requirements:
- RGB-Graph/16-1:
  . +5V 5% @ 1.5A
  . +12V 5% @ 35mA
  . -12V 5% @ 30mA
- RGB-Graph/16-4:
  . +5V 5% @ 1.8A
  . +12V 5% @ 128mA
  . -12V 5% @ 30mA
- RGB-Graph/32-1: +5V 5% @ 2.0A
- RGB-Graph/32-4: +5V 5% @ 2.25A
- RGB-Graph/64-1: +5V 5% @ 2.5A
- RGB-Graph/64-4: +5V 5% @ 0.3A

Dimensions:
- Standard Multibus card size: 12 inches (30.48 cm) wide by 6.75 inches (17.15 cm) high by 0.5 inches (1.25 cm) thick.

Environmental:
- Operating temperature: 0 to 55 C
- Relative humidity 0% to 90% non condensing.

2.0 FUNCTIONAL DESCRIPTION:

The RGB-Graph is a Multibus compatible color graphics video controller board for use with RGB monitors. It is available in several models with maximum resolutions ranging from 256 pixels by 256 pixels by one bit plane to 512 pixels by 512 pixels by four bit planes. The 4 bit plane models can merge bit planes to double the horizontal resolution. The display format is set by the user during the programmed I/O initialization of the board.

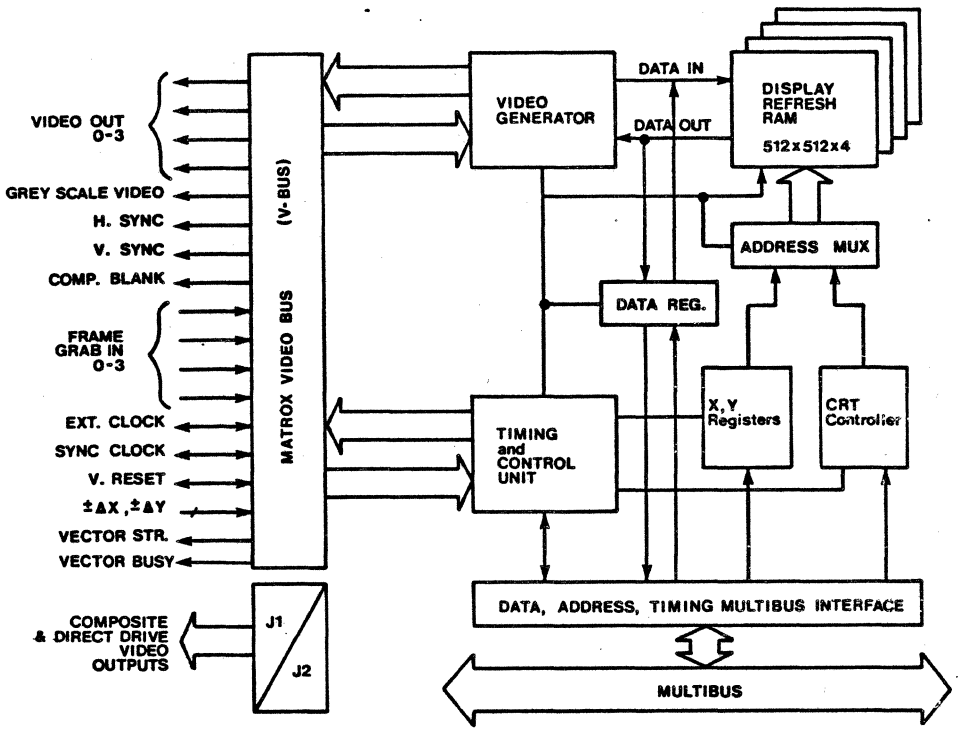


Figure 2.1 - RGB-GRAPH BLOCK DIAGRAM

2.1 DISPLAY MEMORY ACCESS:

The RGB-Graph's display memory is normally accessed by programmed I/O: Display Memory locations corresponding to pixels are pointed to by the X and Y registers, and are accessed through the Data Register. The X and Y Registers, which contain the pixel's horizontal and vertical coordinates respectively, can be accessed by direct I/O or their contents can be modified via the Vector Register. Depending on the command loaded into it, the Vector Register increments or decrements, independently, the X and Y registers, and it can be commanded to automatically write the contents of the Data Register into the Display Memory. The Vector Register is used to rapidly draw horizontal, vertical or angular lines.

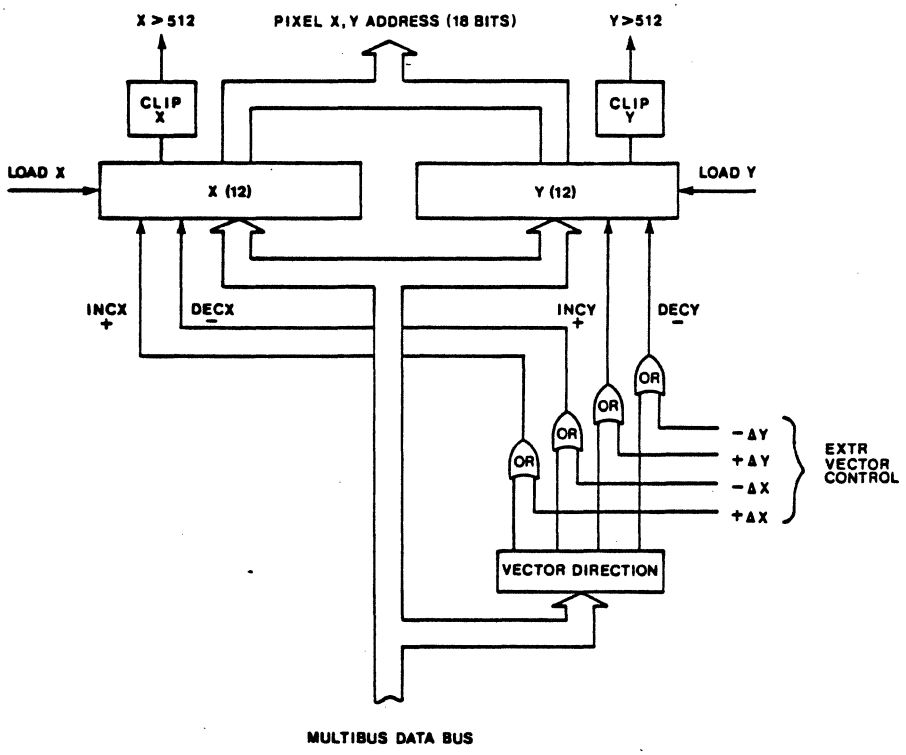


Figure 2.2 - X AND Y REGISTERS

The Display Memory can also be accessed by an external DMA controller. When the RGB-Graph is used in DMA mode, it occupies 1K of system address space, that is positioned via straps. The DMA controller does each block transfer into this same 1K address block which is mapped into different areas of the Display Memory by the X and Y Registers. As the transfer proceeds, the X and Y Registers are automatically incremented.

The RGB-Graph also has a fast preset function which uses one command to fill the entire Display Memory with the data contained in the Data Register. Similarily, provision has been made for the Display Memory to be loaded from an external frame grabbing A to D converter. Both operations are completed in one frame period.

When the RGB-Graph is not in DMA Mode, the X and Y Registers are clipped so that any data written to pixels outside the display format will not wrap around on the Display. This provides a total working area, displayed and non-displayed, of 4096 pixels by 4096 pixels for all formats (see figure 2.3).

2.1 DISPLAY MEMORY ACCESS (Cont'd):

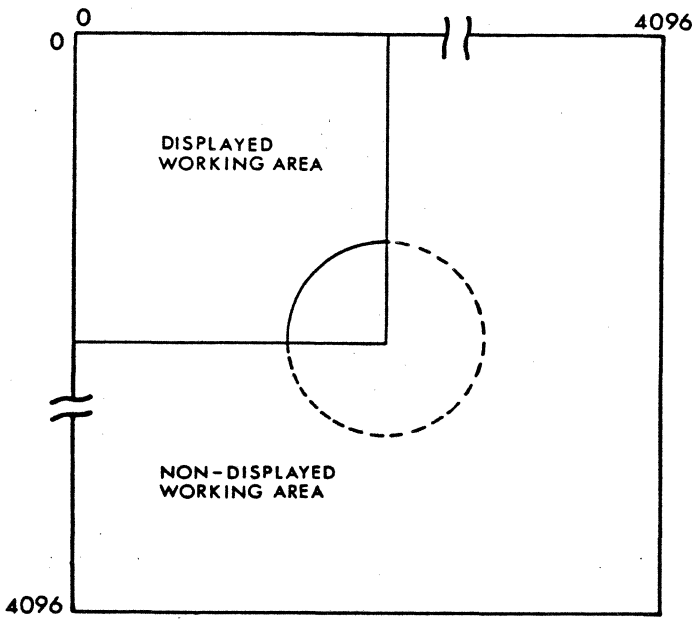


Figure 2.3 - NON-DISPLAYED WORKING AREA

If the user wants the image to wrap around he can put the board in DMA mode, and use the usual I/O access to the Display Memory.

Normally all bit planes are written to simultaneously; however, the RGB-Graph has a mask register which allows write access to be interdicted to any or all of the bit planes.

2.2 DISPLAY MANIPULATION:

The RGB-Graph allows the user to zoom into the display. That is to say, a portion of the display can be selected and expanded to replace the original image from which it was taken. Horizontal expansion (x-zoom) and vertical expansion (y-zoom) are independently controlled allowing the user to make distorting as well as non-distorting zooms. Horizontal zooms can be made by factors of 1, 2, 3, 4, 5, 6, 7 and 8; vertical zooms can be made by factors of 1, 2, and 4.

The display can be panned horizontally with single pixel precision in both directions, and it can be vertically scrolled with 8 pixel precision in both directions.

A series of light pen registers are provided which allow the CPU to determine the position of a light pen to within one pixel.

2.3 VIDEO:

The RGB-Graph has three composite video outputs for color (red, green and blue). One of these outputs (nominally green) can be intensity controlled by a 2 bit D/A converter connected to bit planes 2 and 3. A 4 bit D/A converter supplies another composite video output for grey scale applications. Each bit plane also has two separate TTL video outputs: one for direct drive monitors and one for the video bus connector. The video bus is a connection system that allows the RGB-Graph to be used with other video control products from Matrox (see section 9).

The video outputs can be controlled via a video mask register and by a video enable bit in Control Register No. 1. The video mask register allows the user to individually disable output from any of the bit planes: the disabled outputs, TTL and composite video, go to black. The video enable bit disables all of the outputs together: the composite outputs go to black and the TTL outputs go to high impedence mode (tri-state). The high impedence mode allows more than one RGB-Graph to share the same direct drive monitor and it allows several boards to occupy the same position on the video bus.

If required, the video from bit plane 4 can be disconnected from the 2 bit color output and used to overlay the video from bit planes 1, 2, and 3: this can be an AND, NAND, OR, or XOR operation. The overlay allows the fourth bit plane to be used for alphanumeric or similar data.

3.0 START-UP PROCEDURE:

The following familiarization procedure will not be valid if the as-shipped strap configuration is changed or if a direct drive monitor is used.

1. Visually inspect the board for any shipping damage.

2. Plug the board into a Multibus system and connect an R.G.B. monitor. The video connections will depend on the monitor used; however, section 7 shows where to find any of the video or sync signals that might be required. If one of the RGB-Graph-1 models is being used it will only have one bit plane which should be connected to a monochrome monitor via the red composite video output.

3. Use the procedure in table 3.1 to initialize the display. It will establish the maximum single density format for the particular RGB-Graph model being used.

3.0 START-UP PROCEDURE (Cont'd):

STEP	DATA						I/O LOCATION	COMMENTS
	/16		/32		/64			
	60 HZ	50 HZ	60 HZ	50 HZ	60 HZ	50 HZ		
1	20H	20H	20H	20H	20H	20H	A6H	Control Register No. 1 is initialized; video enabled, single density, no DMA, no frame grab, no preset. Note that two identical outputs are required to initialize this register.
2	20H	20H	20H	20H	20H	20H	A6H	
3	3FH	3FH	3FH	3FH	3FH	3FH	A7H	Control Register No. 2 is initialized; X-Pan=0, X-Zoom=1, Y-Zoom=1.
4	0FH	0FH	0FH	0FH	0FH	0FH	A8H	Control Register No. 3 is initialized; all video outputs are enabled.
5	00H	00H	00H	00H	00H	00H	AAH	Control Register No. 4 is initialized; access to all bit planes is enabled.
6	00H	00H	00H	00H	00H	00H	ACH	The horizontal total minus one is written to CRTC-R0.
7	27H	27H	4FH	4FH	4FH	4EH	AEH	
8	01H	01H	01H	01H	01H	01H	ACH	The format width, in cells, is written to CRTC-R1.
9	20H	20H	40H	40H	40H	40H	AEH	
10	02H	02H	02H	02H	02H	02H	ACH	The horizontal sync position is written to CRTC-R2.
11	21H	21H	45H	45H	45H	45H	AEH	
12	03H	03H	03H	03H	03H	03H	ACH	The horizontal and vertical sync widths are written to CRTC-R3.
13	33H	33H	36H	36H	36H	36H	AEH	
14	04H	04H	04H	04H	04H	04H	ACH	The vertical total minus one is written to CRTC-R4.
15	1FH	26H	1FH	26H	3FH	4DH	AEH	
16	05H	05H	05H	05H	05H	05H	ACH	The vertical adjust parameter is written to CRTC-R5.
17	04H	00H	04H	00H	04H	00H	AEH	
18	06H	06H	06H	06H	06H	06H	ACH	The format height, in cells, is written to CRTC-R6.
19	1EH	20H	1EH	20H	3CH	40H	AEH	
20	07H	07H	07H	07H	07H	07H	ACH	The vertical sync position is written to CRTC-R7.
21	1FH	24H	1FH	24H	3DH	4BH	AEH	
22	08H	08H	08H	08H	08H	08H	ACH	CRTC-R8 is programmed for row and column addressing & to appropriate interlace mode
23	04H	04H	04H	04H	07H	07H	AEH	
24	09H	09H	09H	09H	09H	09H	ACH	The No. of scan lines/field per cell row minus one is written to CRTC-R9.
25	07H	07H	07H	07H	07H	07H	AEH	
26	0CH	0CH	0CH	0CH	0CH	0CH	ACH	The starting address is set to row zero column zero.
27	00H	00H	00H	00H	00H	00H	AEH	
28	0DH	0DH	0DH	0DH	0DH	0DH	ACH	
29	00H	00H	00H	00H	00H	00H	AEH	
Following the above steps in order, output the 50 or 60Hz data that corresponds to the board's model No. (/16-/64) to the I/O location indicated.								

Table 3.1 - DISPLAY INITIALIZATION

4. The display should now be showing random data. Clear the display by outputting 00H to the Data Register at A4H then outputting A0H to Control Register no. 1 at A6H.

5. Enter and run the following program, which will fill an RGB display with vertical color bars. On a monochrome monitor, it will be seen as a series of vertical bars at different positions across the screen.

3.0 START-UP PROCEDURE (Cont'd)

COLOR BARS

ADDRESS	OP-CODE	MNEMONIC	ADDRESS	OP-CODE	MNEMONIC
100	3E	LD, A, 0F	11A	A3	
101	0F		11B	7B	LD A, E
102	D3	OUT A8, A	11C	D3	OUT A4, A
103	A8		11D	A4	
104	01	LD BC, 01, FF	11E	79	LD A, C
105	FF		11F	A7	AND A
106	01		120	C2	JP NZ, 0114
107	21	LD HL, 0000	121	14	
108	00		122	01	
109	00		123	05	DEC B
10A	1E	LD E, 3F	124	F2	JP P, 0114
10B	3F		125	14	
10C	16	LD D, 08	126	01	
10D	08		127	23	INC HL
10E	7D	LD A, L	128	01	LD BC, 01FF
10F	D3	OUT A0, A	129	FF	
110	A0		12A	01	
111	7C	LD A, H	12B	15	DEC D
112	D3	OUT A1, A	12C	C2	JP NZ, 010E
113	A1		12D	0E	
114	0D	DEC C	12E	01	
115	79	LDA, C	12F	1D	DEC E
116	D3	OUT A2, A	130	F2	JP P, 010C
117	A2		131	0C	
118	78	LD A, B	132	01	
119	D3	OUT A3, A	133	76	HALT

4.0 PROGRAMMING:

The RGB-GRAPH is initialized and controlled by programmed I/O to a series of registers. There are 15 directly accessed registers plus 14 CRTC registers that are indirectly accessed through an address register and data port. Section 4.3 contains detailed descriptions of the directly accessed registers and the CRTC data sheets in Section 12 contain descriptions of the CRTC registers. Table 4.1 gives a brief overview of the directly accessed registers.

Because the CRTC was intended for use with alphanumeric displays, the data sheets refer to characters and the character clock; however, as far as the RGB-GRAPH is concerned, the user should read "8 x 8 pixel graphics cell" instead of "character", and "cell clock" instead of "character clock".

The display format is established during the initialization routine by writing the format parameters to Control Register No. 2 and certain CRTC registers. Table 4.1 shows which parameter must be written to which register to establish the standard maximum density format for the particular model of RGB-GRAPH that is being used. The user may, however, wish to establish a non-standard format to facilitate some graphics applications. If this is the case, the format parameters can be calculated using the formula given in Section 4.2.

Note that section 4.4 has been dedicated to the zoom function.

4.0 PROGRAMMING (Cont'd):

RELATIVE LOCATION	DIRECTION	NAME	FUNCTION
00_H	WRITE ONLY	X-Register LOW	Pixel X-coordinate (X0-X7)
01_H	WRITE ONLY	X-Register HIGH	Pixel X-coordinate (X8-X11)
02_H	WRITE ONLY	Y-Register LOW	Pixel Y-coordinate (Y0-Y7)
03_H	WRITE ONLY	Y-Register HIGH	Pixel Y-coordinate (Y8-Y11)
04_H	WRITE READ	Data Reg. LOW	Data registers contain pixel data (color). From 4 bits/pixel (1 x RGB-GRAPH) to 16 bits/pixel (4 x RGB-GRAPH) user strappable.
05_H	WRITE READ	Data Reg. HIGH	
06_H	READ ONLY	Status Register	CLEAR/, PRESET/, Frame Grab Flag
06_H	WRITE ONLY	Control Register Number 1	Video Enable, Double Resolution, DMA Mode, Continous Frame Grab, Display Preset Control.
07_H	WRITE ONLY	Control Register Number 2	X-Pan, X-Zoom, Y-Zoom
08_H	READ ONLY	Aux. Light Pen Register	Light Pen Pixel Position
08_H	WRITE ONLY	Control Register Number 3 LOW	Video enable register (Video Mask) From 4 bits/pixel (1 x RGB-GRAPH) to 16 bits/pixel (4 x RGB-GRAPH) user strappable within two bytes.
09_H	WRITE ONLY	Control Register Number 3 HIGH	
$0A_H$	WRITE ONLY	Control Register Number 4 LOW	Bit plane write enable register (Preset Mask) From 4 bits to 16 bits, user strappable within two bytes
$0B_H$	WRITE ONLY	Control Register Number 4 HIGH	
$0C_H$	READ ONLY	CRTC Status Register	Vertical Blanking Flag Light Pen Register Full Flag
$0C_H$	WRITE ONLY	CRTC Address Register*	Address for CRTC's Internal Reg.
$0E_H$	WRITE READ	CRTC Data Register*	Data Port for CRTC's Internal Reg.
$0F_H$	WRITE ONLY	Vector Register	Increment/decrement control for X,Y registers for vector plots

* These two registers indirectly access 14 more registers within the CRTC, specifying such video parameters as horizontal and vertical Sync, Blanking, Frequency Format, etc.

Table 4.1 - DIRECTLY ACCESSED REGISTER-OVERVIEW

4.1 FORMAT PROGRAMMING TABLES

The following table shows which format parameters must be written to which registers to establish the standard maximum density formats. Note that there is a column of American parameters (60Hz) and a column of European (50Hz) parameters for each model of the RGB-Graph. Note that for American Standard displays, only 480 pixels of the 512 vertical resolution are visable at any time. The non-displayed portion can be scrolled onto the screen.

RGB-GRAPH		/16		/32		/64	
SINGLE DENSITY FORMAT		256 x 256		512 x 256		512 x 512	
AMERICAN/EUROPEAN		60HZ	50HZ	60HZ	50HZ	60HZ	50HZ
Control Register No. 2		3FH	3FH	3FH	3FH	3FH	3FH
H. Total	R0	27H	27H	4FH	4FH	4FH	4FH
H. Displayed,	R1	20H	20H	40H	40H	40H	40H
H. Sync. Position,	R2	21H	21H	45H	45H	45H	45H
V. & H. Sync Width	R3	33H	33H	36H	36H	36H	36H
V. Total,	R4	1FH	26H	1FH	26H	3FH	4DH
V. Adjust,	R5	04H	00H	04H	00H	04H	00H
V. Displayed,	R6	1EH	20H	1EH	20H	3CH	40H
V. Sync. Position,	R7	1FH	24H	1FH	24H	3DH	4BH
Mode Control,	R8	04H	04H	04H	04H	07H	07H
Scan Line	R9	07H	07H	07H	07H	07H	07H
Display Start High	R12	00H	00H	00H	00H	00H	00H
Display Start Low	R13	00H	00H	00H	00H	00H	00H

Table 4.2 - STANDARD FORMATS

4.2 FORMAT PARAMETER CALCULATIONS:

The RGB-GRAPH's format is set by the X and Y zoom factors in Control Register No. 2 and by format parameters written to registers in the board's CRTC. Because the CRTC, an LSI video controller chip, was designed primarily to refresh alphanumerics displays, it sees the display as a field of graphics cells equivalent to characters and it refreshes the display at that level. Each of these graphics cells is 8 pixels by 8 pixels in size; display refresh at the pixel level within the cells is taken care of by circuitry external to the CRTC. Because the format is programmed in the CRTC, which operates at the cell level, the number of pixels in the X or Y axis of any format must be a multiple of 8. If the user conforms to this restriction, he can use the formulas in this section to calculate the parameters for a large number of different formats. The only other restriction, of course, is that the number of pixels in the format times the number of bit planes used must not exceed the capacity of the Display Memory.

In some cases, the user may find that the display does not cover as much of the CRT as might be wished. If such is the case he still has the option of changing the crystal to a lower frequency.

The following is a list of formulas that can be used to calculate the format parameters for irregular formats or the parameter changes required for zoom operations:

4.2 FORMAT PARAMETER CALCULATIONS:

FORMAT PARAMETER FORMULAS

1. Dot Clock = $\frac{\text{Crystal Freq.}}{\text{X-Zoom Factor}}$

2. Cell Clock = $\frac{\text{Dot Clock}}{8}$

   The Cell Clock is the same as the character clock referred to in the CRTC data sheets.

3. HORIZONTAL TOTAL = $\frac{\text{Monitor Spec. Horiz. Scan Period}}{\text{Cell Clock Period}}$

   Choose the nearest integer minus one. This value is written in HEX format to R0.

4. HORIZONTAL DISPLAYED = $\frac{\text{Total X-Axis Pixels}}{8}$

   This is the number of graphics cells in the X-AXIS of the format and is written in HEX to R1.

5. HORIZONTAL SYNC. POSITION H. Displayed + $\frac{\text{(H. Total - H. Displayed)}}{2}$

   This value may require adjustment. It is written in HEX to R2

6. ACTUAL HORIZONTAL SCAN PERIOD = $\frac{\text{Horizontal Total}}{\text{Cell Clock}}$

7. CELL ROW PERIOD = Y-Zoom Factor x 8 x Actual Horizontal Scan Period

8. VERTICAL TOTAL = $\frac{\text{Vertical Scan Period}}{\text{Cell Row Period}}$

   This value minus one is written in HEX to R4. The vertical scan period is 16.667ms on American systems and 20.000ms for European systems.

9. VERTICAL TOTAL ADJUST = $\frac{\text{(Vertical Scan Period -(V. Total x Cell Row Period))}}{\text{Actual Horizontal Scan Period}}$

   Choose the nearest integer. This value is written in HEX to R5.

10. VERTICAL DISPLAYED = $\frac{\text{Total Y-Axis Pixels}}{8}$

    This value is written in HEX to R6.

11. VERTICAL SYNC. POSITION V. Displayed + $\frac{\text{(V. Total -V. Displayed)}}{2}$

    Adjust the value as required. It is written in HEX to R7.

12. SCAN LINE = 8 x Y ZOOM FACTOR
    This value minus one is written in HEX to R9.

13. HORIZONTAL SYNC. WIDTH = $\frac{\text{Monitor Spec. H. Sync. Width}}{\text{Cell Clock Period}}$

    Choose the nearest integer. This value goes to bits 0-3 of R3.

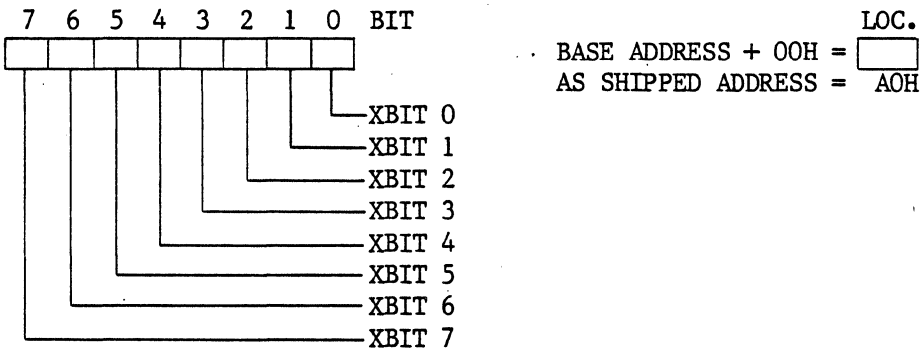
14. VERTICAL SYNC WIDTH = $\frac{\text{Monitor Spec. V. Sync. Width}}{\text{Actual Horizontal Scan Period}}$

    Choose the nearest integer. This value goes to bits 4-7 of R3.

4.3 REGISTERS:

4.3.1 X-REGISTER LOW:

WRITE ONLY

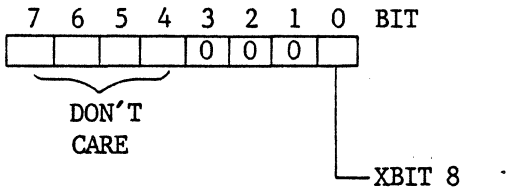


LOC.
BASE ADDRESS + 00H = [ ]
AS SHIPPED ADDRESS = A0H

This register holds the lower 8 bits of the X coordinate of the display memory location that is to be accessed.

4.3.2 X-REGISTER HIGH:

WRITE ONLY

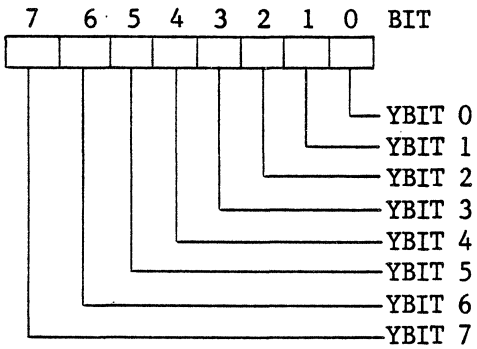


LOC.
BASE ADDRESS + 01H = [ ]
AS-SHIPPED ADDRESS = A1H

This register holds the 9th bit of the X coordinate for the RGB-GRAPH/32 and the RGB-GRAPH/64. If a One is written to any of bits 1-3 the clipping circuit will interdict memory access. This also applies to Bit 0 on the RGB-GRAPH/16.

4.3.3 Y-REGISTER LOW:

WRITE ONLY

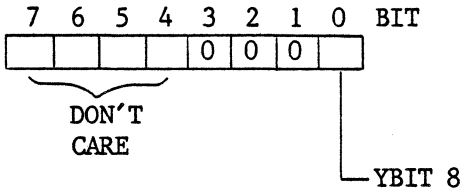


LOC.
BASE ADDRESS + 02H = [ ]
AS-SHIPPED ADDRESS = A2H

This register holds the lower 8 bits of the Y coordinate of the display memory location that is to be accessed.

4.3.4 Y-REGISTER HIGH:

WRITE ONLY

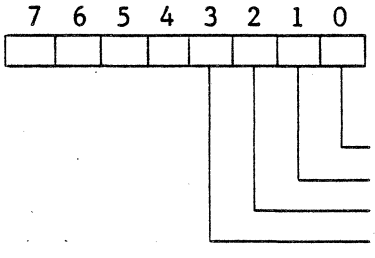


BASE ADDRESS + 03H = LOC.
AS-SHIPPED ADDRESS = A3H

This register holds the 9th bit of the Y coordinate for the RGB-GRAPH/64. If a One is written to any of Bits 1-3 the clipping circuit will interdict memory access. This also applies to Bit 0 on the RGB-GRAPH/16 and RGB-GRAPH/32.

4.3.5 DATA REGISTER LOW:

READ/WRITE



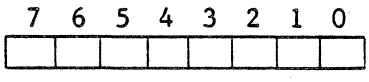
BASE ADDRESS + 04H = LOC.
AS-SHIPPED ADDRESS = A4H

As Shipped Configuration

Any four bits of this register can be used as a data port to the Display Memory if the appropriate straps are installed (see Section 5.2). When the board is shipped, straps are installed which allow the display memory to be accessed through the four least significant bits of this register, as shown above. Bits not selected for use are don't care for write and zero for read.

4.3.6 DATA REGISTER HIGH:

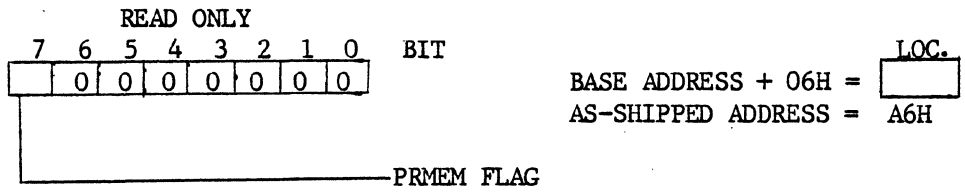
READ/WRITE



BASE ADDRESS + 05H = LOC.
AS-SHIPPED ADDRESS = A5H

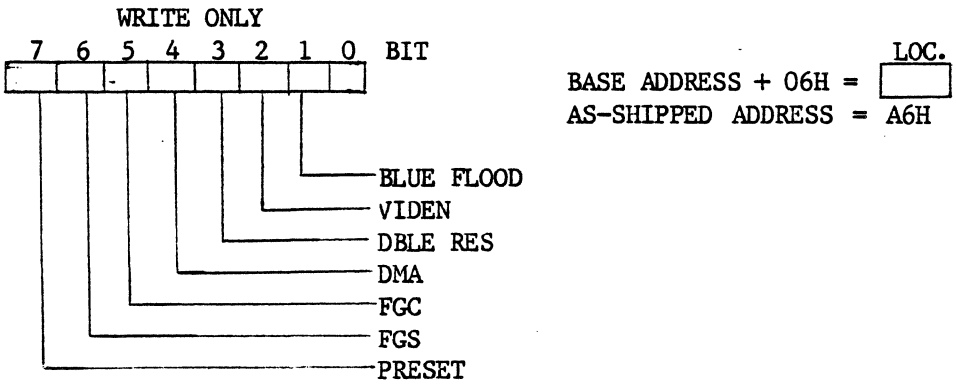
As in the case of the Data Register Low, any four bits of this register can be used as a data port to the Display Memory if the appropriate straps are installed (see Section 5-3). Any bits not selected are "don't care" for write and zero for read.

4.3.7 STATUS REGISTER:



Bit 7: PRMEM FLAG. When this bit is one, the memory is being preset or a frame grab is in process. When this bit is zero, the memory is neither being preset nor is a frame grab in process.

4.3.8 CONTROL REGISTER NO. 1



BIT 1: BLUE FLOOD. When this bit is zero, operation is normal. When this bit is one, the Blue output is driven on during active video. BLUE FLOOD is used to provide a visible raster to trigger the light pen. When activated, it is only generated on the composite video output; the TTL output are not affected.

Bit 2: VIDEN. When this bit is zero, TTL video is enabled. When this bit is one, TTL video is in high impedence (tri-state) mode.

Bit 3: DBLE RES. When this bit is one, bit planes 0 and 2 are multiplexed together and bit planes 1 and 3 are multiplexed together to provide twice the X-AXIS resolution. Note however, that the bits per pixel are halved. When this bit is zero, resolution is normal and there are four independent bit planes.

Bit 4: DMA. When this bit is one, the Display Memory can be accessed by DMA. All DMA transfers are made at the same 1K block of system address space, the base address of which, is set by straps (see Section 5.4). This system address space is mapped into different areas of the Display Memory, before the block transfer, by loading the X and Y Registers with the transfer's Display Memory starting address minus one. As the transfer proceeds, the X and Y Registers are automatically incremented before each byte transfer. When several 1K blocks are sequentially transferred to or from contiguous Display Memory, the X-Y starting address need only be loaded before the first block transfer.

When bit 4 is zero the RGB-GRAPH's Display Memory is accessed normally and the X and Y registers must be loaded with a new set of coordinates before each byte or word transfer.

4.3.8 CONTROL REGISTER NO. 1 (Cont'd):

Bit 5: FGC. When this bit is 0, the RGB-GRAPH operates in continuous frame grab mode. If a frame grabber is connected, the board will continually grab and display sequential frames: in effect, it will display what the camera sees. When the bit is 1, the RGB-GRAPH will freeze the frame that was in the display memory at the time the bit changed state. The user can watch the action, then freeze it.

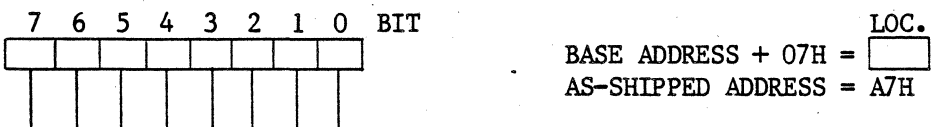
Bit 6: FGS. This bit is also provided for frame-grabbing operations. If a one is written to FGS , the RGB-GRAPH will grab and hold a single frame of video information. It will continue to display the information until one is again written to FGS, at which time a new frame will be grabbed. If a zero is written to this bit, it will have no effect.

Bit 7: PRESET. When a one is written to this bit, the Display Memory will be preset to the value in the Data Register. If a zero is written to this bit, it will have no effect.

NOTE: During initialization, the output operation to this register must be repeated twice. After initialization, one output is enough to load the register.

4.3.9 CONTROL REGISTER NO. 2:

WRITE ONLY



HORIZONTAL SYNC. DELAY	0 DOTS	1 DOTS	2 DOTS	3 DOTS	4 DOTS	5 DOTS	6 DOTS	7 DOTS
XPAN 0	1	0	1	0	1	0	1	0
XPAN 1	1	1	0	0	1	1	0	0
XPAN 2	1	1	1	1	0	0	0	0

ZOOM FACTOR	1	2	3	4	5	6	7	8
XZOOM 0	1	0	1	0	1	0	1	0
XZOOM 1	1	1	0	0	1	1	0	0
XZOOM 2	1	1	1	1	0	0	0	0

ZOOM FACTOR	1	2	4
YZOOM 0	0	1	0
YZOOM 1	0	0	1

NOTE: X zooms of greater than 4 are not possible when using the 256 x 256 format.

4.3.9 CONTROL REGISTER NO. 2 (Cont'd):

Bit 0-2: XPAN0-XPAN2. These three bits are used in conjunction with the CRTC starting address registers (R12 and R14) to horizontally pan the display. XPAN0-XPAN2 can be set to delay the horizontal sync. pulse by 1 through 7 dots (see Table above). A pan is accomplished by sequentially incrementing this delay until it reaches 7 dots then resetting XPAN0-XPAN2 and incrementing the CRTC starting address registers during vertical blanking. This operation is repeated at a rate that will give the required pan speed.

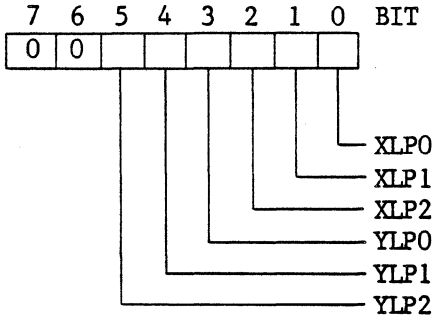
Bit 3-5: XZOOM0-XZOOM2. These three bits are used in conjunction with several CRTC registers (R0, R1, R2, R3, R12, R13) to expand the display along the horizontal axis (see Section 4.4).

Bit 6 & 7: YZOOM0 and YZOOM1. These two bits are used in conjunction with several CRTC registers (R3, R4, R5, R6, R7, R9, R12, R13) to expand the display along the vertical axis (see Section 4.4).

NOTE: For a normal display, X and Y zoom factors of one must be loaded.

4.3.10 AUXILIARY LIGHT PEN REGISTER:

READ ONLY



LOC.

BASE ADDRESS + 08H = ☐

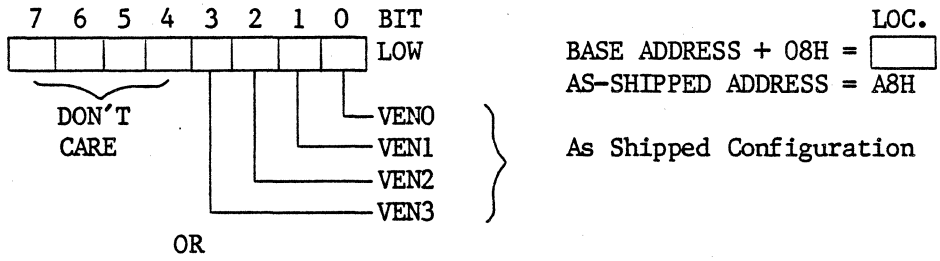
AS-SHIPPED ADDRESS = A8H

Bits 0-2: XLP0-XLP2. These bits are the three least significant bits of the light pen X coordinate. The most significant bits are provided by CRTC R17: bits 0-4 represent XLP3-XLP7 for 256 x 256 formats and bits 0-5 represent XLP3-XLP8 for 512 x 512 formats. Note that the data from CRTC R17 must be shifted to the left three bits before they can be combined with XLP0-XLP2 from this register. Unused bits in CRTC R17 are zero.

Bits 3-5: YLP0-YLP2. These bits are the three least significant bits of the light pen Y coordinate. The most significant digits are provided by CRTC R16: bits 0-4 represent YLP3-YLP7 for 256 x 256 formats and bits 0-5 represent YLP3-YLP8 for 512 x 512 formats. Note that the data from CRTC R16 must be shifted three spaces to the left before it can be combined with YLP0-YLP2 from this register. Unused bits in CRTC R16 are zero.

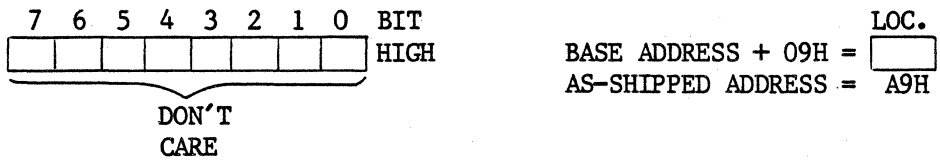
4.3.11 CONTROL REGISTER NO. 3:

WRITE ONLY



OR

WRITE ONLY



The four video enable bits can be strapped to any four bits in the two I/O locations shown above (see Section 5.4), and must be strapped to the same four bits that are used by the data port (see Section 4.3.5). The as-shipped configuration is shown here.

Bit 0: VEN0. When this bit is one, video from bit plane 0 is enabled. When this bit is zero, video from bit plane 0 is disabled.

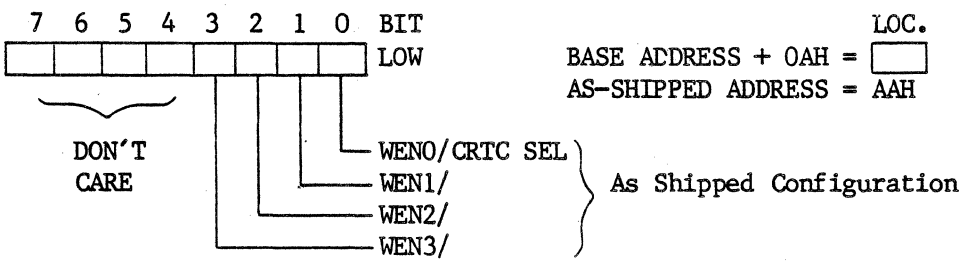
Bit 1: VEN1. When this bit is one, video from bit plane 1 is enabled. When this bit is zero, video from bit plane 1 is disabled.

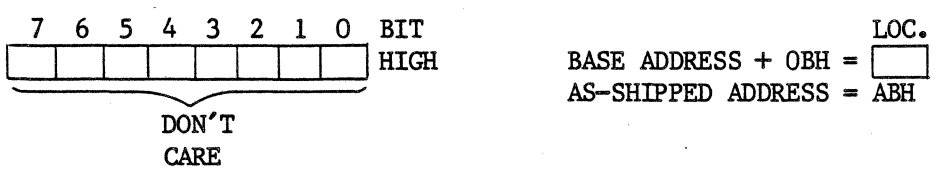
Bit 2: VEN2. When this bit is one, video from bit plane 2 is enabled. When this bit is zero, video from bit plane 2 is disabled.

Bit 3: VEN3. When this bit is one, video from bit plane 3 is enabled. When this bit is zero, video from bit plane 3 is disabled.

4.3.12 CONTROL REGISTER NO. 4:

WRITE ONLY





4.3.12 CONTROL REGISTER NO. 4 (Cont'd):

The four bits of Control Register No. 3 can be strapped to any four bits in the two I/O locations shown above (see Section 5.4) and must be strapped to the same four bits that are used as the data port. The as-shipped configuration is shown here.

Bit 0: WEN0/CRTC SEL/. When this bit is zero, bit plane 0 and the CRTC can be written to. When this bit is one, bit plane 0 and the CRTC cannot be written to. The CRTC SEL/ function is required for master slave configurations where the CRTCs of two or more boards at the same address are programmed differently.

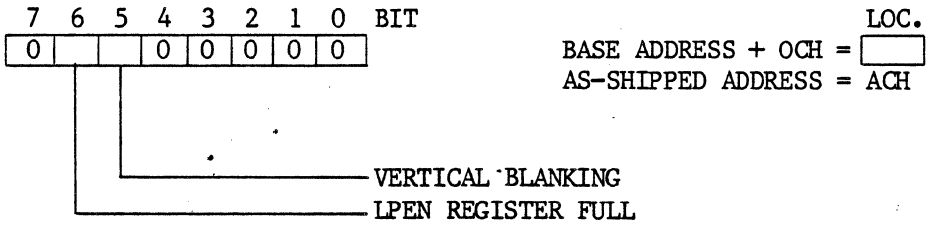
Bit 1: WEN1/. When this bit is zero, bit plane 1 can be written to. When this bit is one, bit plane 1 cannot be written to.

Bit 2: WEN2/. When this bit is zero, bit plane 2 can be written to. When this bit is one, bit plane 2 cannot be written to.

Bit 3: WEN3/. When this bit is zero, bit plane 3 can be written to. When this bit is one, bit plane 3 cannot be written to.

4.3.13 CRTC STATUS REGISTER:

READ ONLY

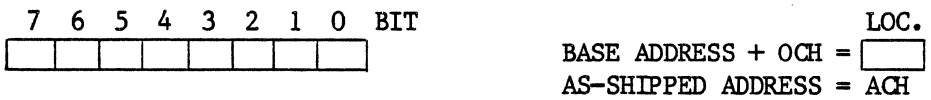


Bit 5: VERTICAL BLANKING. When this bit is one, the scan is in vertical blanking. When this bit is zero, the scan is not in vertical blanking.

Bit 6: LPEN REGISTER FULL. This bit goes to one whenever a light pen strobe occurs. This bit goes to zero whenever either CRTC R16 or R17 are read.

4.3.14 CRTC ADDRESS REGISTER:

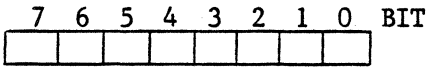
WRITE ONLY



When one of the CRTC registers is to be accessed, its address is placed in this register, then data is input or output through the CRTC Data Register. Addresses and descriptions for the CRTC registers are found in the CRTC data sheets.

4.3.15 CRTC DATA REGISTER:

READ/WRITE

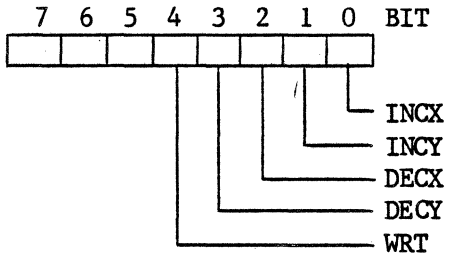


BASE ADDRESS + OEH = LOC.
AS-SHIPPED ADDRESS = AEH

This location is the data port to and from the CRTC.

4.3.16 VECTOR REGISTER:

WRITE ONLY



BASE ADDRESS + OFH = LOC.
AS-SHIPPED ADDRESS = AFH

BIT 0: INCX. When a one is written to this bit, the X-Register is incremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 1: INCY. When a one is written to this bit, the Y-Register is incremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 2: DECX. When a one is written to this bit, the X-Register is decremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 3: DECY. When a one is written to this bit, the Y-Register is decremented. Writing a zero to this bit has no effect on the X-Y coordinates.

Bit 4: WRT. When this bit is zero, the contents of the Data Register are automatically written to the Display Memory when the Vector Registor is loaded. When this bit is one, data is not automatically written to the Display Memory when the Vector Register is loaded.

NOTE: The Vector Register will not function properly if the RGB-GRAPH is in DMA mode.

Figure 5-1 shows the direction that the graphics trace will take when different values are written to the Vector Register.

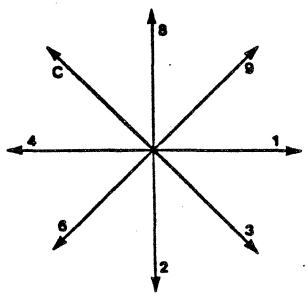


Figure 4.1 - VECTOR DIRECTION (BIT 0-3)

4.4 THE ZOOM FUNCTION::

The zoom function allows the user to select a portion of the display and enlarge it to replace the original image from which it was taken. Resolution in the enlarged section is not affected, since it contains the same number of pixels before and after the zoom. Horizontal expansion (X zoom) and vertical expansion (Y zoom) are independently controlled by the user. It can be expanded vertically by factors of 2, 3, 4, 5, 6, 7, and 8 in the 512 x 512 and 512 x 256 formats, and by 2, 3, and 4 in the 256 x 256 format. Since identical horizontal and vertical zoom factors are required to maintain correct image proportions, the horizontal zoom factors of 2 and 4 are the most useful. The remaining horizontal zoom factors should not, however, be ignored since they can be used for controlled distortion of an image.

When considering the zoom function, the display should be considered as a field of graphics cells, each of which is composed of 8 x 8 pixels in a normal resolution display or 16 x 8 pixels in a double resolution display.

The number of these cells in the display depends on the type of RGB-GRAPH used: 32 columns by 32 rows for the RGB-GRAPH/16, 64 columns and 32 rows for the RGB-GRAPH/32, and 64 columns and 64 rows for the RGB-GRAPH/64. The zoom window (the area to be enlarged) is defined in terms of these cells. Integer values must be used.

The size of the zoom window should be selected so that the actual display is the same size before and after the zoom. The post zoom display can, if necessary, be smaller; however, if it is larger, it will most likely overshoot the CRT and there may be problems programming the CRTC. The best way to determine the size of the zoom window is to divide the times one format X and Y axes, in cells, by the zoom factors to be used. If the result is not an interger value, choose the next lower integer. For example, if a times two X and Y zoom was made into the display of a RGB-GRAPH/64 (64 x 64 cells), the area to be enlarged would be 32 cells x 32 cells. If a distorting zoom of 4 times on the Y axis and 3 on the X axis was made into the same display, the area to be enlarged would be 21 cells (X axis) by 16 cells (Y axis). Table 4.2 gives the sizes, in cells, of zoom windows to be enlarged for X-Y zooms of 2 and 4.

RGB-GRAPH	/16		/32		/64	
AXIS	X	Y	X	Y	X	Y
TIMES 2	16 Cells	16 Cells	32 Cells	16 Cells	32 Cells	32 Cells
TIMES 4	8 Cells	8 Cells	16 Cells	8 Cells	16 Cells	16 Cells

Figure 4.2 - THE MOST USED ZOOM WINDOW SIZES

When doing a zoom, the user first decides the X and Y zoom factors to be used, and then, knowing the times 1 format, he determines the size of the zoom window. He then places an imaginary frame the size of the zoom window around the part of the image to be enlarged. The row and column numbers of the cell in the upper left hand corner of that frame are then written to CRTC register R12 and R13 respectively. Finally, the zoom factors are written to Control Register No. 2 (see Section 4.3.9) and the format parameters in the CRTC Registers are adjusted to accommodate them. This adjustment is necessary because the Dot Clock is set by the X zoom factor and the number of scan lines per pixel is set by the Y-zoom factor.

4.4 THE ZOOM FUNCTION (Cont'd):

Table 4.3 shows the CRTC register values for non-distorting times 2 and times 4 zooms. When other zoom factors are used, the adjusted CRTC register values can be calculated using the formulas found in section 4.2.

RGB-GRAPH	/ 16				/ 32				/ 64			
ZOOM FACTORS	2 X 2		4 X 4		2 X 2		4 X 4		2 X 2		4 X 4	
AMERICAN / EUROPEAN	60HZ	50HZ	60HZ	50HZ	60HZ	50HZ	60HZ	50HZ	60HZ	50HZ	60HZ	50HZ
CONTROL REGISTER NO. 2	77H	77H	A7H	A7H	77H	77H	A7H	A7H	77H	77H	A7H	A7H
HORIZONTAL TOTAL	13H	13H	09H	09H	27H	27H	13H	13H	27H	27H	13H	13H
HORIZONTAL DISPLAYED	10H	10H	08H	08H	20H	20H	10H	10H	20H	20H	10H	10H
H. SYNC POSITION	10H	10H	08H	08H	23H	23H	11H	11H	23H	23H	11H	11H
V. AND H. SYNC WIDTH	32H	32H	31H	31H	33H	33H	32H	32H	33H	33H	32H	32H
VERTICAL TOTAL	0FH	12H	07H	08H	0FH	12H	07H	08H	1FH	26H	0FH	12H
VERTICAL ADJUST	04H	08H	04H	18H	04H	08H	04H	18H	04H	00H	04H	08H
VERTICAL DISPLAYED	0EH	10H	07H	05H	0EH	10H	07H	05H	1EH	20H	0EH	10H
V. SYNC POSITION	0FH	11H	07H	07H	0FH	11H	07H	07H	1EH	24H	0FH	11H
MODE CONTROL	04H	04H	04H	04H	04H	04H	04H	04H	07H	07H	07H	07H
SCAN LINE	0FH	0FH	1FH	1FH	0FH	0FH	1FH	1FH	0FH	0FH	1FH	1FH

Table 4.3 - FORMAT PARAMETERS FOR NON-DISTORTING ZOOMS

Figure 4.2 represents a 256 x 256 display and shows three areas (A, B and C) that might be zoomed into using X and Y zoom factors of 4. Note that where the zoom window overshoots the display it wraps around.

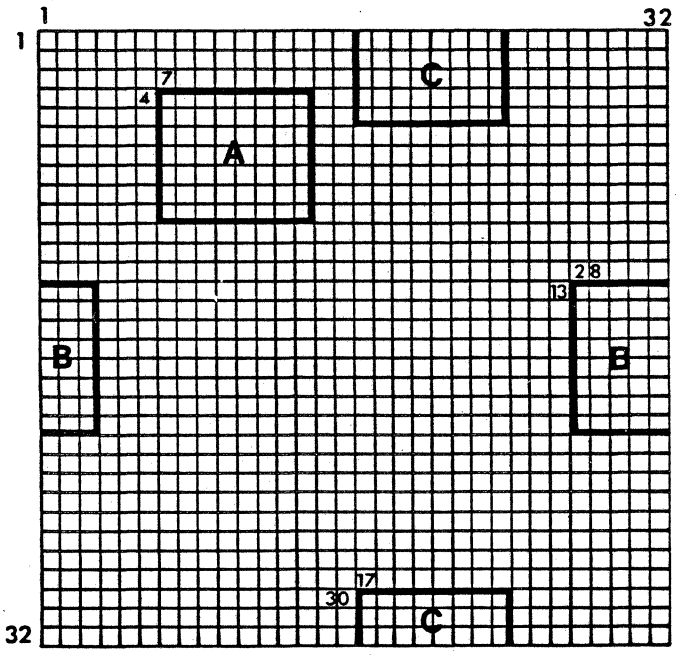


Figure 4.2 - TYPICAL ZOOM AREAS IN A 256 X 256 FORMAT

5.0 STRAPS:

Strap options on the RGB-Graph are implemented by interconnecting numbered wire wrap pins. In this manual, straps between any two wire wrap pins are referred to in the following ways:

14-15 IN indicates that wire wrap pin 14 is connected to wire wrap pin 15.
14-15 OUT indicates that wire wrap pin 14 is not connected to wire wrap pin 15.
14 ←→ 15 indicates that wire wrap pin 14 is connected to wire wrap pin 15.

5.1 I/O BASE ADDRESS STRAPS:

ADDRESS BIT	ADR8	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4
CORRESPONDING STRAP	*49-56	*50-56	*54-56	*53-56	52-56	48-56	55-56	51-56
BIT = ZERO	OUT	OUT	IN	IN	IN	IN	IN	IN
BIT = ONE	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT
*Not used with 8-bit I/O address	Also Strap 45-46 IN 46-47 OUT For 8-Bit Address 45-46 OUT 46-47 IN For 16-Bit Address							

Table 5.1 - I/O BASE ADDRESS STRAPS

5.2 DATA STRAPS:

Table 5.2 shows how the RGB-Graph's 4 bit data port can be strapped to ay 4 bit nibble in the Multibus's 16 bit data bus.

INTERNAL DATA BUS	PIN	AS-SHIPPED STRAPS	PIN	BUS DATA BUS
MD0 RED	20		16	DAT 0
			12	DAT 4
			8	DAT 8
			4	DAT 12
MD1 BLUE	19		15	DAT 1
			11	DAT 5
			7	DAT 9
			3	DAT 13
MD2 GREEN	18		14	DAT 2
			10	DAT 6
			6	DAT 10
			2	DAT 14
MD3 OVERLAY	17		13	DAT 3
			9	DAT 7
			5	DAT 11
			1	DAT 15

Table 5.2 - DATA STRAPS

5.2 DATA STRAPS (Cont'd):

The nibble selected must be completely within either the high byte or the low byte, and depending on which byte it occupies one of the two following two strap configurations must be implemented.

DATA PORT IN LOW BYTE (AS-SHIPPED) = 32-33 IN 28-29 IN
DATA PORT IN HIGH BYTE = 31-32 IN 29-30 IN

5.3 DMA BASE ADDRESS:

Table 5.3 shows the straps used to set the base address of the 1K block of system address space used for DMA transfers.

ADDRESS BIT	ADI3	ADI2	ADI1	ADIO	ADRF	ADRE	ADRD	ADRC	ADRB	ADRA
CORRESPONDING STRAP	36-44	39-44	43-44	42-44	35-44	34-44	38-44	40-44	41-44	37-44
BIT = ZERO	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
BIT = ONE	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN

Table 5.3 - DMA BASE ADDRESS STRAPS

5.4 STRAPS FOR CONTROL REGISTERS 3 AND 4:

Bits 0-3 of Control Register 3 and 4 must be strapped to the same Multibus data lines used by bits 0-3 of the data port (see table 5.4).

REGISTER BIT	PIN	AS-SHIPPED STRAPS	PIN	BUS DATA BIT
VEN 0 and WEN 0	96		80	DAT 0
			91	DAT 4
			78	DAT 8
			94	DAT 12
VEN 1 and WEN 1	86		81	DAT 1
			79	DAT 5
			90	DAT 9
			93	DAT 13
VEN 2 and WEN 2	85		92	DAT 2
			87	DAT 6
			83	DAT 10
			89	DAT 14
VEN 3 and WEN 3	95		82	DAT 3
			77	DAT 7
			84	DAT 11
			88	DAT 15

* For high byte access strap 159-158 IN, 159-160 OUT, 159-161 OUT.
For low byte access strap 159-160 IN, 159-158 OUT, 159-161 OUT.
For word access strap 159-161 IN, 159-158 OUT, 159-160 OUT.

Table 5.4 - MASK REGISTER STRAPS

5.5 FRAME GRAB STRAPS:

Each of the RGB-Graph's bit planes can be strapped to any of the 8 data lines on the video bus (J3). Table 5.5 shows the appropriate straps.

BIT PLANE	PIN	AS-SHIPPED STRAPS	PIN	J3-PIN
0	151		141	29
			145	33
1	150		143	30
			146	34
2	149		142	31
			140	35
3	148		144	32
			147	36

Table 5.5 - FRAME GRAB STRAPS

None of these straps are installed when the board is shipped.

5.6 TTL VIDEO STRAPS:

The RGB-Graph's 4 TTL video signals can be strapped on any one of the 16 lines on the video bus (J3). Table 5.6 shows the wire wrap pins used to accomplish this.

TTL VIDEO	PIN	AS-SHIPPED STRAPS	PIN	J3 PIN
0	123		112	12
			117	16
			122	20
			127	24
1	118		111	13
			116	17
			121	21
			126	25
2	113		110	14
			115	18
			120	22
			125	26
3	108		109	15
			114	19
			119	23
			124	27

Table 5.6 - TTL VIDEO STRAPS

NOTE: None of the TTL video straps are installed when the board is shipped.

5.7 SYNC AND BLANKING STRAPS:

Table 5.7 shows how the horizontal and vertical sync. (positive and inverted can be connected to J2 and J1.

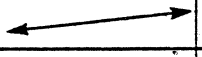
SOURCE	PIN	STRAPS	PIN	DESTINATION
H. Sync	128		129	J2-Pin 1
H. Sync/	130			
V. Sync	133		132	J2-Pin 9
V. Sync/	131			
H. Sync/	136		137	J3-Pin 8
V. Sync/	138		139	J3-Pin 9
C. Blank/	135		134	J3-Pin 10
Note: Straps should not cross the horizontal lines in the center column.				

Table 5.7- SYNC AND BLANKING STRAPS

5.8 REGISTER READ DISABLE STRAPS:

When 2, 3 or 4 RGB-Graphs are used in parallel, it is necessary, on all but one board, to disable read access from all registers except the Data Register. This is done by installing the straps shown below:

REGISTER ACCESS (AS-SHIPPED) = 73 - 72 IN
NO REGISTER ACCESS = 72 - 71 IN

5.9 V RESET/STRAP:

When the RGB-Graph is used with another RGB-Graph or its sister alphanumeric controller, the RGB-Alpha, it must generate a vertical reset pulse to synchronize the two boards. A strap between wire wrap pin 106 and wire wrap pin 107 will cause this pulse to be generated on pin 6 of the video bus (J3). This strap must be out when the RGB-Graph is in a single board configuration. (see section 9)

5.10 CHARACTER CLOCK STRAP:

When the strap between wire wrap pin 100 and wire wrap pin 101 is removed, the internal Character Clock is disable and must be supplied from some external source at pin 4 of J3. This configuration is used when the board is operating as a slave (see section 9). Normally this strap is installed and will be installed when the board is shipped.

5.11 MASTER SLAVE STRAPS:

The straps given in table 5.8 are used to configure the RGB-GRAPH as a master, a pseudo master, or a slave. Also see section 9.0.

	98-97*	100-101	106-107	156-155	156-157	134-135	138-139	136-137	73-72	72-71	162-163
MASTER	IN	IN	IN	IN	OUT	IN	IN	IN	IN	OUT	IN**
PSEUDO MASTER	OUT	IN	OUT	IN	OUT	IN	IN	IN	IN	OUT	IN**
SLAVE	OUT	OUT	OUT	OUT	IN	OUT	OUT	OUT	OUT	IN	OUT

* Substitute 99 for 97 when RGB-GRAPH/16 IS USED.
** Necessary only when RGB-Alpha is in the system.

NOTE: 106-107 must be out for stand alone board.

Table 5.8 - MASTER SLAVE STRAPS

5.12 BIT PLANE CONTROL STRAP:

The fourth output channel can be disconnected from the green and grey scale drivers, and can be connected to overlay the other three video channels. The overlay can be an OR, EXCLUSIVE OR, AND, or NAND function depending on the I.C. used for A91 (see table 5.9).

OVERLAY LOGIC FUNCTION	A91	
OR	74LS32	AS-SHIPPED
EX OR	74LS86	
AND	74LS08	
NAND	74LS00	

Table 5.9 - OVERLAY I.C. SELECTION

The straps that must be implemented are as follows:

OVERLAY = 103-104 IN, 102-105 IN
NO OVERLAY (AS-SHIPPED) = 102-103 IN, 104-105 IN

5.13 LIGHT PEN STRAPS:

If one of the following straps is installed, a light pen hit will generate a hardware interrupt to the CPU.

153 - 152 IN INTERRUPT ON 41 - P1 INT 0/
153 - 154 IN INTERRUPT ON 42 - P1 INT 1/

6.0 CIRCUIT DESCRIPTION:

The following circuit description should help the user to understand some of the more involved sections of the RGB-Graph's logic. While reading it the user should refer to the schematics at the back of this manual. Where more than one gate is found in an i.c., individual gates are referred to by their output pin: thus A10-1 is the gate in A10 that has its output at pin 1 of the I.C. package.

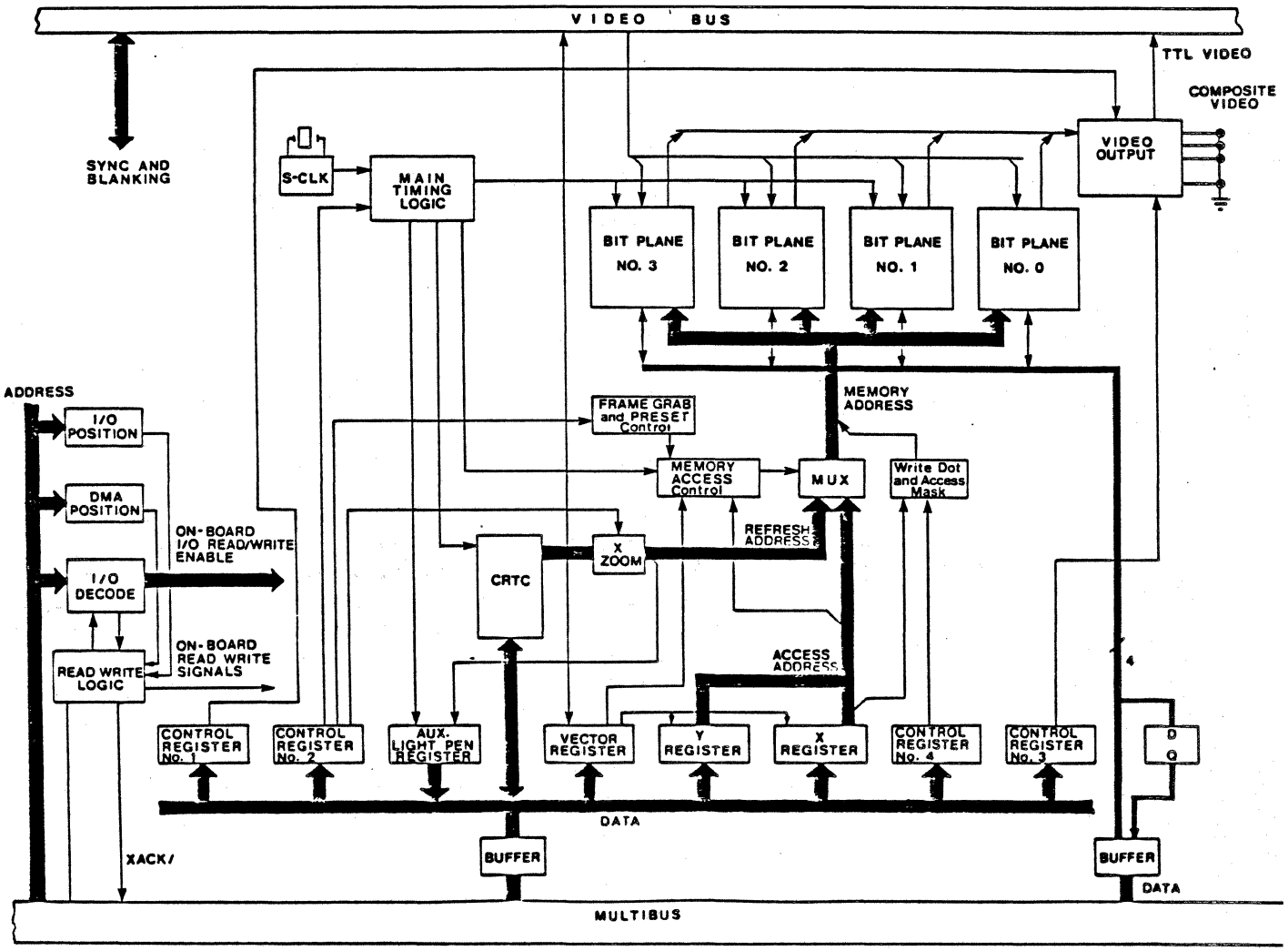


Figure 6.1 - BLOCK DIAGRAM OF RGB-GRAPH

6.1 BIT PLANE:

Figure 6.2 is a block diagram of bit plane zero and its associated data access chips. The RGB-GRAPH can have up to four circuits like this. The display memory for each bit plane is composed of four RAMs. When the memory is read; all four RAMs are accessed simultaneously, providing four bits corresponding to four consecutive pixels in the display. If the access is part of a display refresh operation, the four bits are latched into A85, then loaded into A83 and shifted out as serial video data. If the access is a read to the Multibus , multiplexer A84 allows only the bit addressed by X0 and X1 from the X-Register to go to the data port register (A14). Data enters the bit plane via the multiplexer A82 which selects either the data port or the frame grabber port as the data source. When the source is the data port, the data bit is presented to the inputs of all four RAMs and only the write enable line of the RAM containing the bits' destination is activated (see section 6.5). When the source is the frame grabber port, incoming serial data is first converted to parallel data in the right half of A83, then four bits are simultaneously written into the bit plane: one bit to each of the RAMs. Note that when the RGB-Graph is operating in continous frame grab mode, the video data continues through A83 to the video output section.

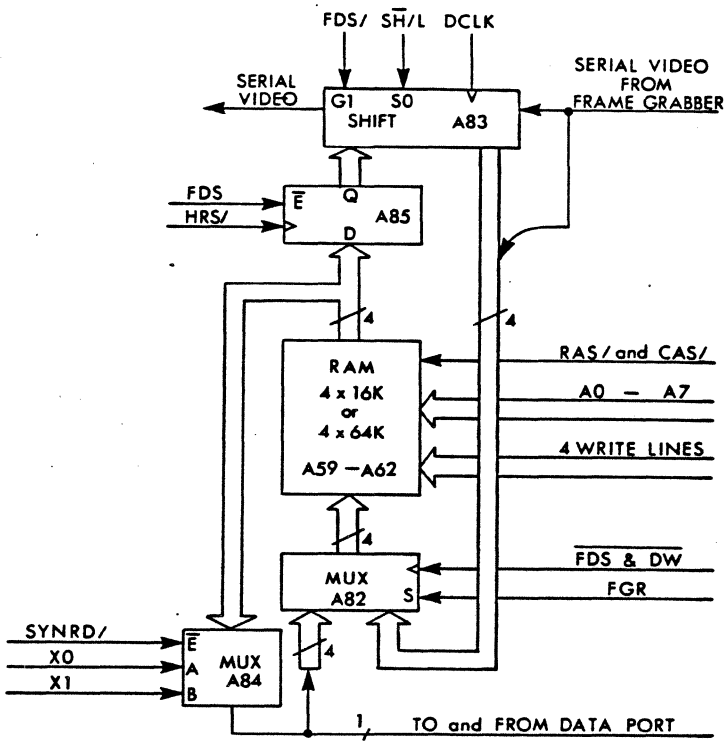


Figure 6.2 - BIT PLANE NO. 0

6.2 CENTRAL TIMING:

Figure 6.3 is a block diagram of the RGB-Graph's central timing section. It generates most of the board's timing signals and is controlled principally by CTL23-CTL25 (the X-zoom factor), which set the divisor used by the Dot Clock (A70), the Load Clock (A71), and the Cell Clock (A72). A divisor of one is used for zoom by one, a divisor of two is used for zoom by two, and so on. A46 enables the Load Clock every 4 SCLK Cycles and enables the Cell Clock (CCLK) every 8 SCLK cycles. Figures 6.4 and 6.5 show the timing of A70-A72 for zoom times one and zoom times two.

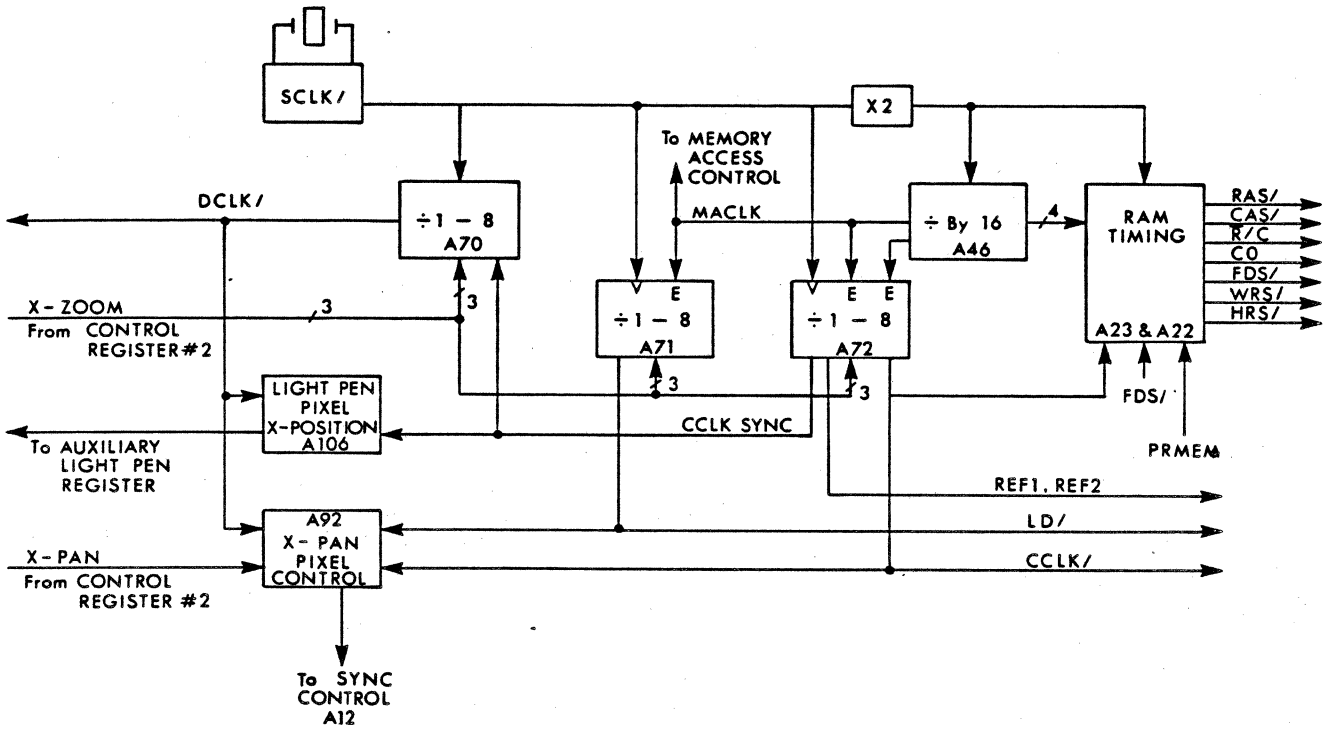


Figure 6.3 - TIMING SECTION BLOCK DIAGRAM

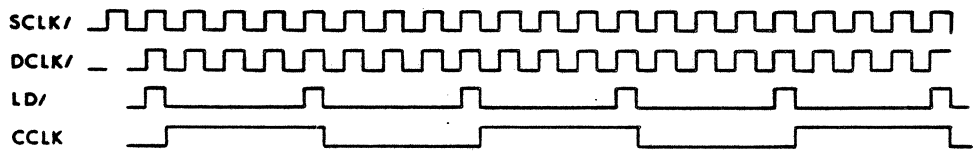


Figure 6.4 - X-ZOOM BY ONE TIMING

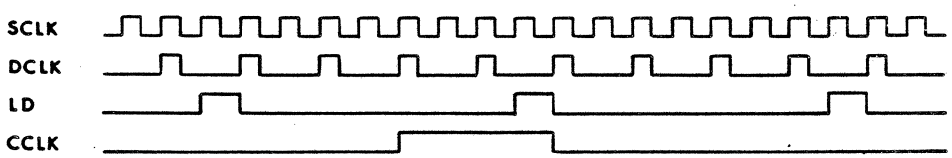


Figure 6.5 - X-ZOOM BY TWO TIMING

6.2 CENTRAL TIMING (Cont'd):

The three least significant outputs of A46 are used to address a PROM (A23) which generates a series of timing signals for the memory. The relation of these signals to several other timing signals is shown in figure 6.6. Note that the form of the signals depends on the state of CCLK and PRMEM which are also connected to the PROM's address lines. Also note that the display is refreshed when CCLK is high and that there are two memory reads during that period (CAS goes low twice); four bits are read out of each bit plane when CO is low and another four bits are read out when CO is high. The period during CCLK low is reserved for accesses from off-board. PRMEM goes high for both frame grab and preset memory operations and the only difference in timing between these operations is that FDS/ is gated on by FGR/ during frame grab.

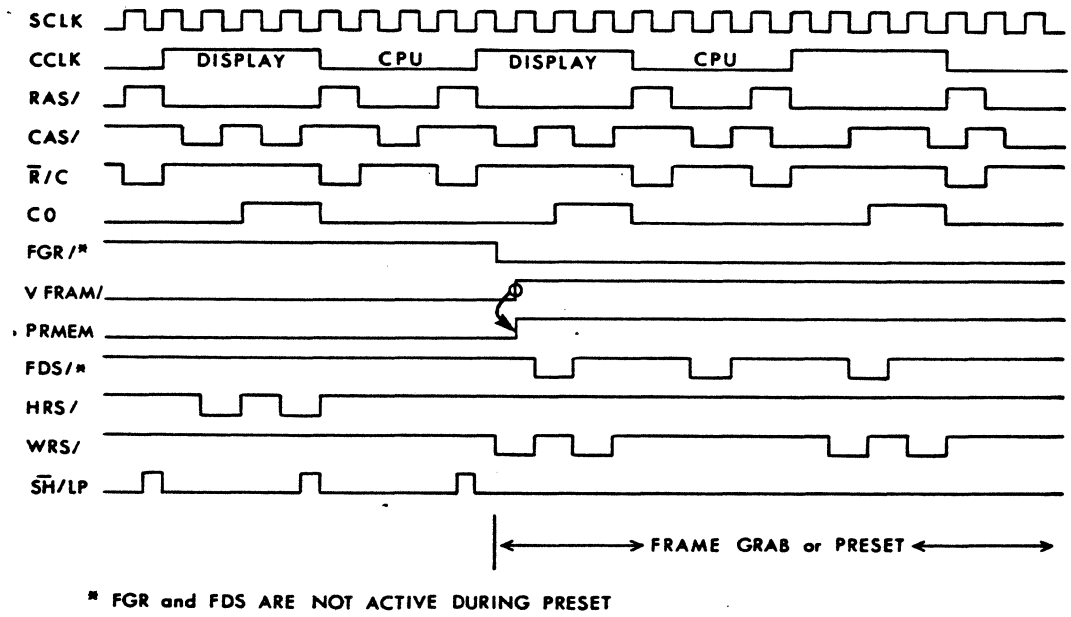


Figure 6.6 - MEMORY TIMING (X-ZOOM BY ONE)

The central timing section also controls the light pen and the X-pan functions at the pixel resolution level. A106 holds the position of the scan as it moves through each cell and provides this information to the Auxiliary Light Pen Register. A92 sets the position of the horizontal sync pulse in response to the CTL20-CTL22 (X-PAN) from Control Register No. 2.

6.3 FRAME GRAB AND PRESET CONTROL:

Figure 6.7 shows a simplified version of the circuit used to control frame grab and memory preset operations. The circuit synchronizes these operations with the VFRAM signal which indicates the start of each new frame. The two flip flops, A96-5 and A 4-5, are part of Control Register No. 1 and hold bits 6 and 7 respectively. Note that PRMEM, which goes to the memory timing PROM (A23), goes high when either a frame grab or a memory preset operation is initiated. Also note that the Q output of A4-5 is read as bit 7 of the Status Register.

6.3 FRAME GRAB AND PRESET CONTROL (Cont'd):

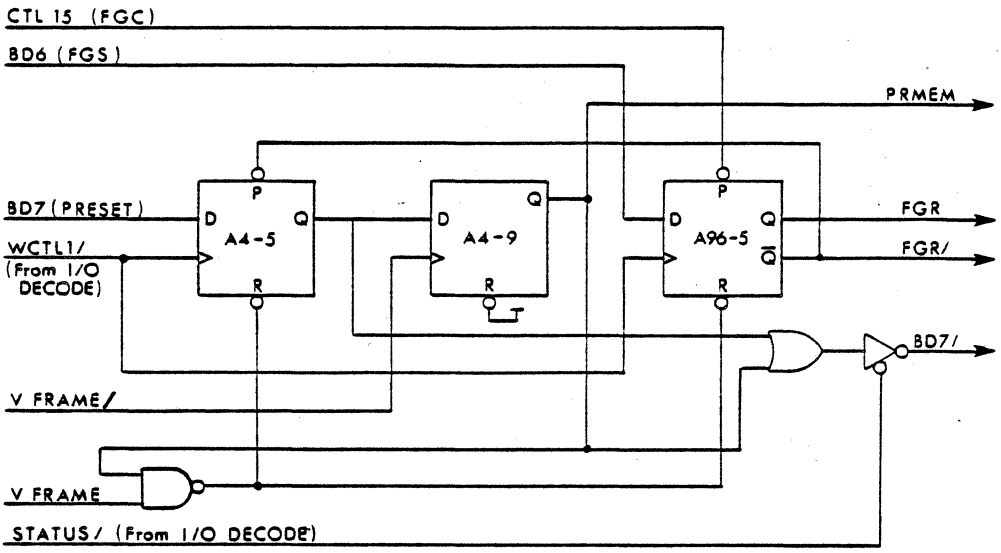


Figure 6.7 - FRAME GRAB AND PRESET CONTROL

6.4 MEMORY ACCESS CONTROL:

The RGB-Graph's display memory can be addressed by either the CRTC or the X and Y Registers. The CRTC does so to refresh the display or to do frame grab or preset operations; the X and Y Registers do so when there is an external access from the system CPU or a DMA controller. Since refresh is an on-going process it takes precidence, and the four multiplexers, A34, A35, A57, A58 (see schematic), normally connect the memory address lines to the CRTC. When an external access occurs the address multiplexers are switched to the X and Y Registers by BCLE from the circuit shown in figure 6.8. This circuit arbitrates conflicts between external and internal accesses of the display memory.

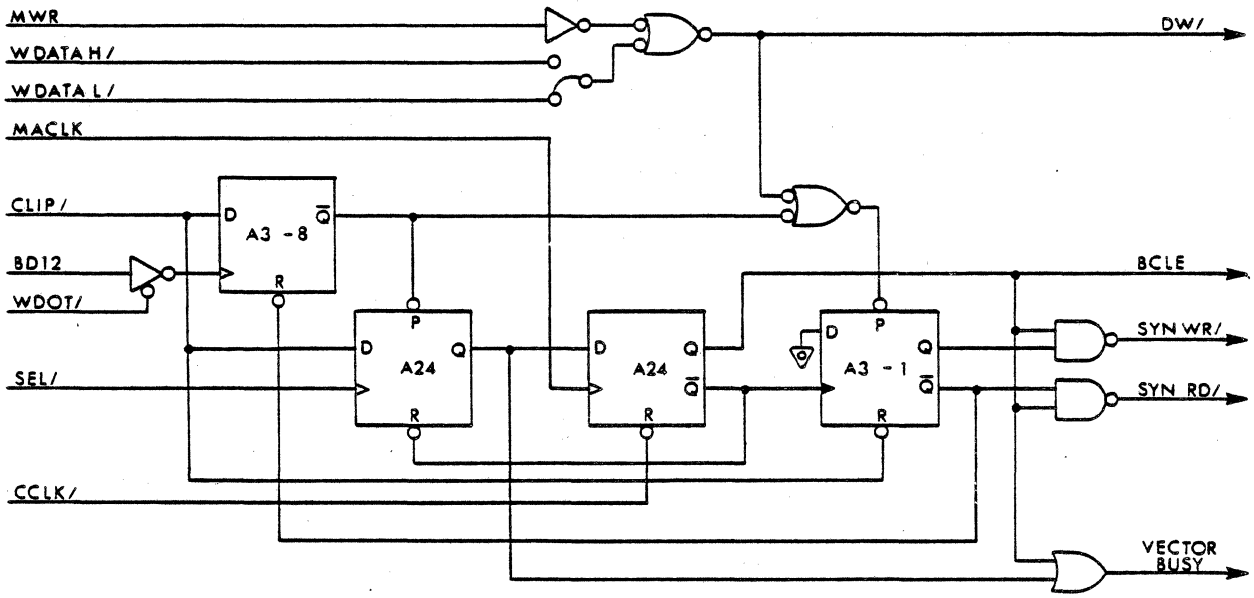
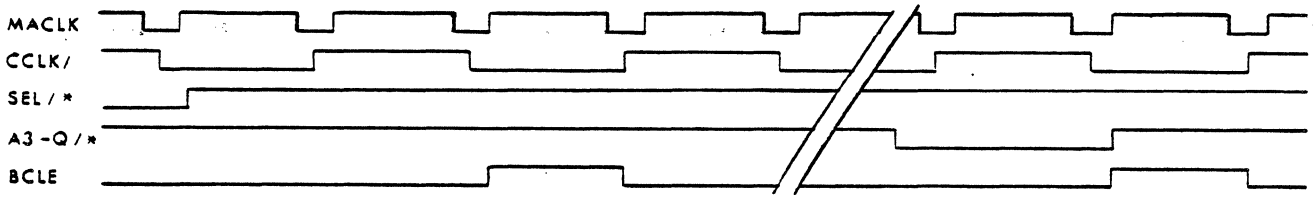


Figure 6.8 - MEMORY ACCESS ARBITRATION LOGIC

6.4 MEMORY ACCESS CONTROL (Cont'd):

The CRTC accesses the display memory only when the CCLK is high, at which time the accessed data is latched into A83 and A85 which mask the display from the display memory. Because of this, the CCLK low period is available for external access. The circuit in figure 6.8 delays any external access until the start of the CCLK low period at which time BCLE is generated and the access is made. Figure 6.9 shows the timing involved in this procedure.



* SEL/ AND A3-Q/ ARE INITIATED BY AN EXTERNAL ACCESS AND THEIR POSITIONS IN THIS DIAGRAM ARE ARBITRARY WITH RESPECT TO THE OTHER TIMING SIGNALS.

Figure 6.9 - BCLE TIMING (ZOOM BY ONE)

Note that BCLE will be generated by either the trailing edge of SEL/ initiated from the Multibus or a A3-Q/ initiated from the video bus. A3-Q/ signals a write operation resulting from an access to the Vector Register (BD12=WRT).

When the CLIP/ signal is low, it indicates that there is an overflow condition in the X and Y Registers and it will inhibit BCLE, preventing any externally initiated access. Note that CLIP/ does not go low when there is an overflow during a DMA transfer.

6.5 DISPLAY MEMORY WRITE ACCESS:

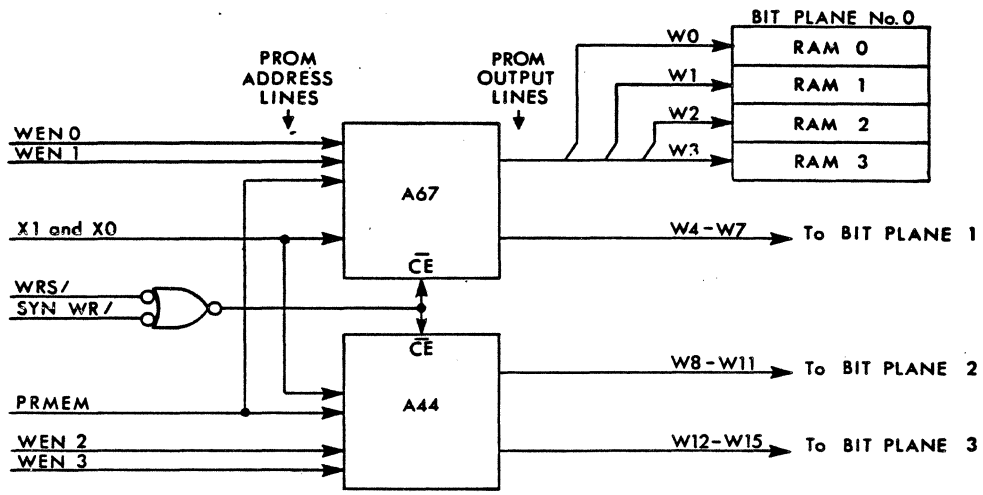


Figure 6.10 - DISPLAY MEMORY WRITE ACCESS LOGIC

6.5 DISPLAY MEMORY WRITE ACCESS (Cont'd):

Figure 6.10 shows how the two PROMs, A67 and A44, control the write enable signals for the Display Memory. When there is a frame grab or a memory preset operation the PROMs are enabled by WRS/ from the memory timing PROM (see section 6.2); when there is a write access from off-board, the PROMs are enabled by SYNWR/ from the memory access section (see section 6.4). The PROMs have been programmed to enable the memory write lines (W0-W15) according to the requirements defined by the signals addressing the PROMs. For example if X0 and X1 are low and all the other addresses lines are high, W0 will be pulled low, allowing a write to RAM 0 of bit plane 0. If a WEN line is low access to the corresponding bit plane in interdicted.

6.6 REFRESH ADDRESSING:

Figure 6.11 shows how the Display Memory refresh address is taken from the CRTC. Note that the RAM row address (R0-R7) is contained within the least significant part of the CRTC generated address to assure that the RAMs are refreshed within the required time limit. The Y-zoom multiplexer selects different bits of the scan line counter (RA0-RA4) as RAM row address, R4-R6, depending on the Y-zoom factor. This is done to allow for the fact that the number of scan lines per pixel changes with the y-zoom factor. The two Exclusive OR GATES, A45-6 AND A45-8, are used to assure that all of the RAM columns get refreshed when the larger x-zoom factors are used. In such a case, REF2 and REF3 are automatically pulled high following each display refresh cycle, RAS/ and CAS/ are generated (see figure 6.6), and the unused rows are refreshed without their contents being displayed. In some cases 64K RAMs requiring 256 refresh addresses will be used in the RGB-Graph. When this occurs, the positions of R7 and C2 will be interchanged within the CRTC generated address to assure proper RAM refresh.

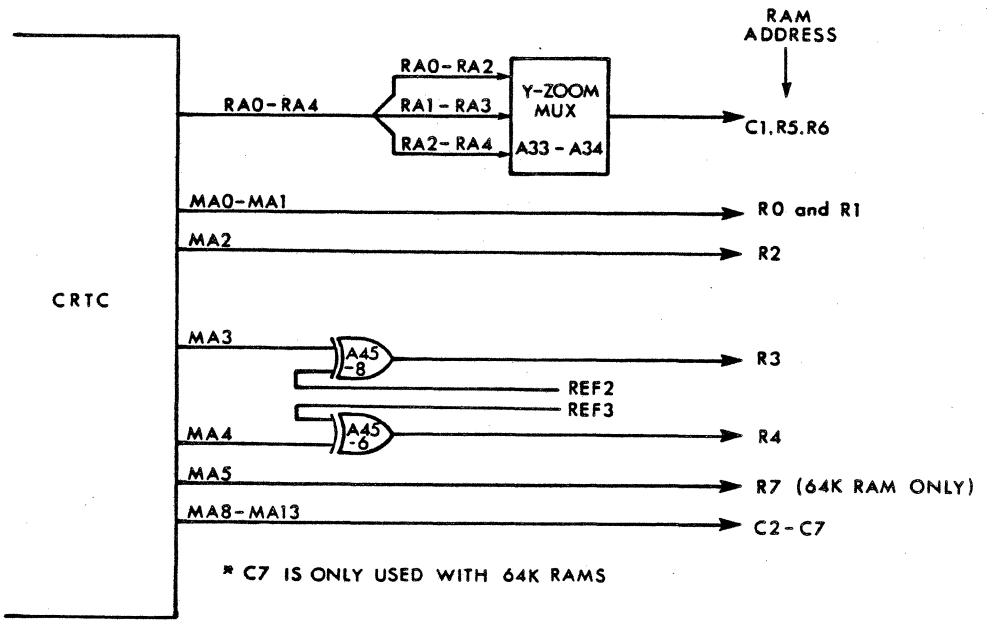


Figure 6.11 - RAM REFRESH ADDRESS

6.7 VIDEO OUTPUT:

Figure 6.12 shows a block diagram of the video output section. The double resolution function is implemented in A94 by multiplexing the four bit planes onto two video output channels with the dot clock. The video mask logic is a set of AND gates which allow VEN 0-3 to disable selected video channels. The contents of the overlay logic can be changed by the user but is shipped with OR gates which allow channel 4 to be superimposed on the other video outputs. The video disable block (A90) provides a synchronization function and allows one control bit to put the TTL outputs into a high impedance state.

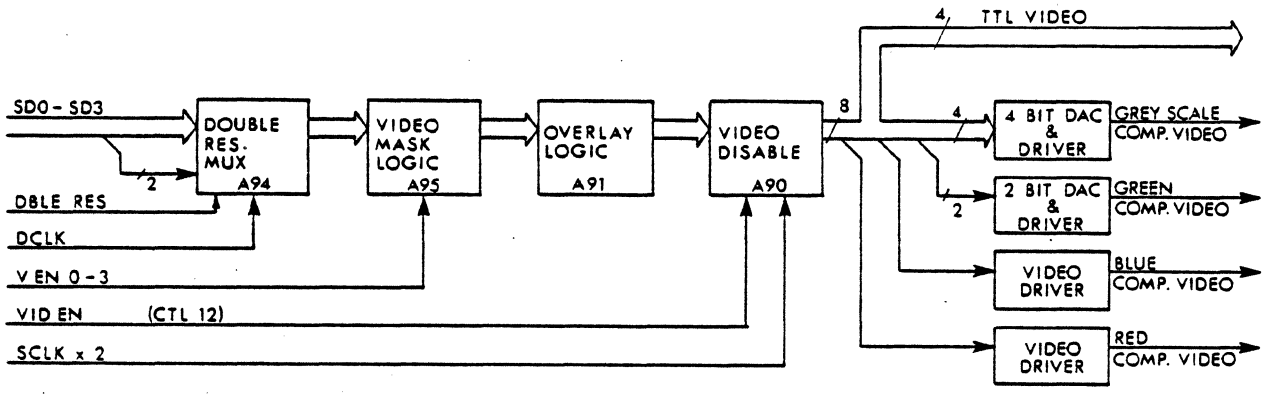


Figure 6.12 - VIDEO OUTPUT SECTION

7.0 CONNECTORS:

7.1 P1 (BUS CONNECTOR):

P1 is the standard 86 pin edge connector (.156 IN. centers) used with the Multibus. Table 7.1 shows the pin assignments.

	(COMPONENT SIDE)			(CIRCUIT SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Sig GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7	+12V	+12Vdc	8	+12V	+12Vdc
	9	N.C.		10	N C	
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	N.C.		14	INT/	CRTC RESET
	15	N.C.		16	N. C.	
	17	N.C.		18	N. C.	
	19	MRDC/	Mem Read Cmd	20	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	N C	
BUS CONTROLS AND ADDRESS	25		Reserved	26	N.C.	
	27	BHEN/	Byte High Enable	28	AD10/	
	29	N.C.		30	AD11/	Address
	31	N.C.		32	AD12/	Bus
	33	N.C.		34	AD13/	
INTERRUPTS	35	N.C.		36	N.C.	
	37	N.C.		38	N.C.	
	39	N.C.		40	N.C.	
	41	INT0/		42	INT1/	
ADDRESS	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/	Address	48	ADRB	Address
	49	ADR8/	Bus	50	ADR9/	Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/	Data	64	DATB/	Data
	65	DAT8/	Bus	66	DAT9/	Bus
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved	78		Reserved
	79	-12V	-12Vdc	80	-12V	-12Vdc
	81	+5V	+5Vdc	82	+5V	+5Vdc
	83	+5V	+5Vdc	84	+5V	+5Vdc
	85	GND	Signal GND	86	GND	Signal GND

Note that -12V is required only with /16 models

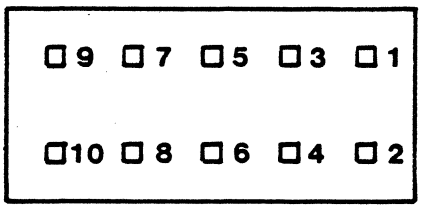
7.2 J1 (COMPOSITE VIDEO):

J1 is a 10 pin right angle header (0.100 IN.) that mates with the AMP # 87922-1 or equivalent. It is used for the composite video outputs. Note that coaxiale cable can be attached to this connecter.

PIN	SIGNAL	PIN	SIGNAL
1	GREY SCALE	6	GROUND
2	GROUND	7	BLUE VIDEO
3	RED VIDEO	8	GROUND
4	GROUND	9	N.C.
5	GREEN VIDEO	10	GROUND

* The Red output is used for monochrome monitors when only one bit plane is used.

Table 7.2 - J1 PIN ASSIGNMENT



PIN CONFIGURATION LOOKING INTO J1 OR J2

FIGURE 7.1 - PIN CONFIGURATION J1, J2

7.3 J2 (DIRECT DRIVE OUTPUTS):

J2 is a 10 pin right angle header (0.100 IN.) that mates with the AMP. 87922-1 or equivalent. It provides the signals required by direct drive monitors.

PIN	SIGNAL	PIN	SIGNAL
1	HORIZONTAL DRIVE/	6	GROUND
2	GROUND	7	TTL VIDEO BLUE
3	TTL VIDEO RED	8	GROUND
4	GROUND	9	VERTICAL DRIVE/
5	TTL VIDEO GREEN	10	GROUND

Table 7.3 - J2 PIN ASSIGNMENT

7.4 J3 (VIDEO BUS):

J3 is a 50 pin right angle header (0.100 IN.) that mates with the MOLEX 15-25-4505 (#4700) or equivalent. It is the connector for the Matrox Video Bus.

7.4 J3 (VIDEO BUS) Cont'd):

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	26	VIDEO DATA E
2	EXTERNAL CLOCK	27	VIDEO DATA F
3	GROUND	28	GROUND
4	EXTERNAL CCLK SYNC/	29	FRAME GRAB 0
5	GROUND	30	FRAME GRAB 1
6	V RESET	31	FRAME GRAB 2
7	GROUND	32	FRAME GRAB 3
8	HORIZONTAL SYNC/	33	FRAME GRAB 4
9	VERTICAL SYNC/	34	FRAME GRAB 5
10	COMPOSITE BLANKING	35	FRAME GRAB 6
11	GROUND	36	FRAME GRAB 7
12	VIDEO DATA 0	37	GROUND
13	VIDEO DATA 1	38	RED TTL VIDEO - RGB-Alpha
14	VIDEO DATA 2	39	GREEN TTL VIDEO - RGB-Alpha
15	VIDEO DATA 3	40	BLUE TTL VIDEO - RGB-Alpha
16	VIDEO DATA 4	41	BG TTL VIDEO
17	VIDEO DATA 5	42	GROUND
18	VIDEO DATA 6	43	INC X
19	VIDEO DATA 7	44	DEC X
20	VIDEO DATA 8	45	INC Y
21	VIDEO DATA 9	46	DEC Y
22	VIDEO DATA A	47	WR7
23	VIDEO DATA B	48	GROUND
24	VIDEO DATA C	49	VECTOR BUSY'
25	VIDEO DATA D	50	CRTC Reset/
Also see Sections 5.5 and 5.7			

Table 7.4 - J3 PIN ASSIGNMENT

7.5 J4 (LIGHT PEN):

J4 is a 10 pin right angle header (0.100 IN.) that mates with the Molex 15-25-5103 # 4700 or equivalent. It is used for light pen signals.

PIN	SIGNAL	PIN	SIGNAL
1	LP ENABLE	5	+ 5V
2	N.C.	6	N.C.
3	LP STROBE	7	GROUND
4	N.C.	8	GROUND

Table 7.5 - J4 PIN ASSIGNMENT

Note: Pins 9 and 10 are not connected.

8.0 READ/WRITE TIMING:

8.1 DMA ACCESS TIMING:

PARAMETER	DESCRIPTION	MIN.	MAX.	UNITS
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold-Time	0		ns
t_{ACK}	Acknowledge Time	80	1100*	ns
t_{TO}	CMD ↑ To XACK ↑		50	ns
t_{DS}	Write Data Set-Up Time	0		ns
t_{DHW}	Data Hold Time For Write	0		ns
t_{ACC}	CMD To Data Valid (Read)	40	40	ns
t_{DHR}	Read Data Hold Time	0	10	ns
t_{DXL}	Read Data Set-Up to Xack	80	1100*	ns

* From previous CMD (2.2 us for RGB-GRAPH/32 or /16

Table 8.1 - READ/WRITE TIMING PARAMETERS

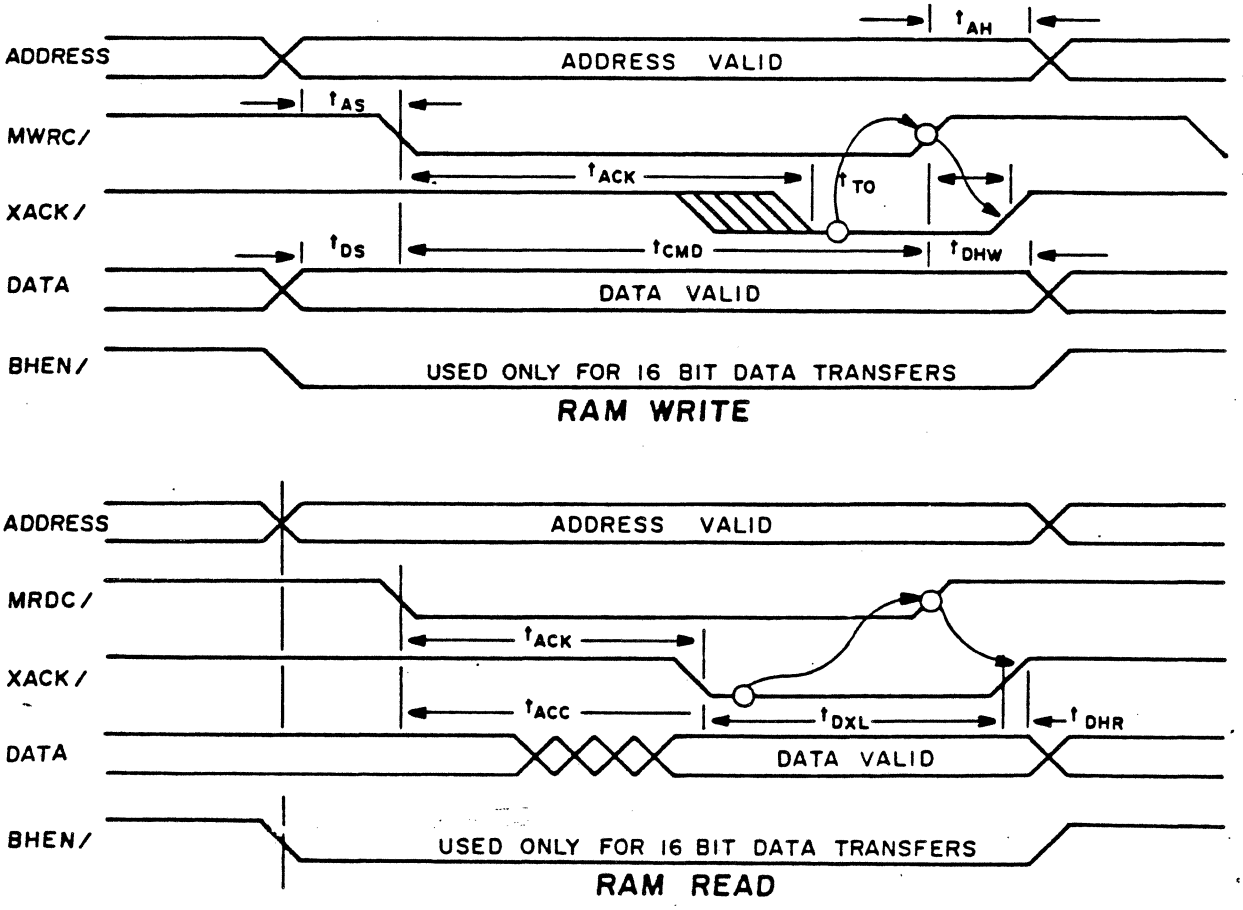
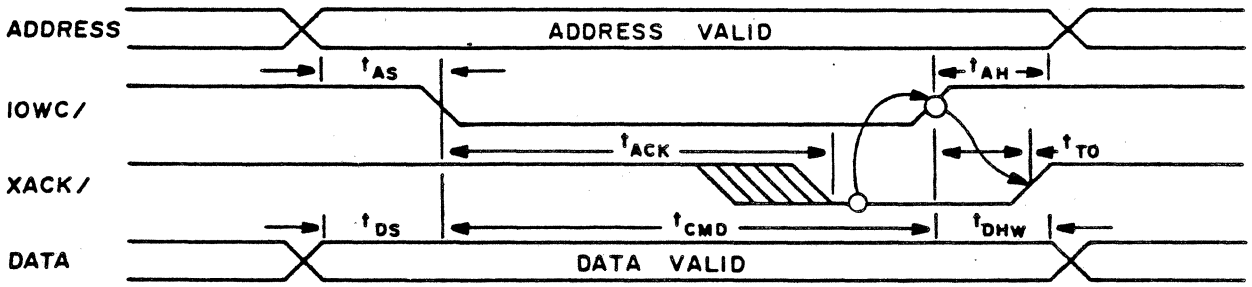


Figure 8.1 - READ/WRITE TIMING

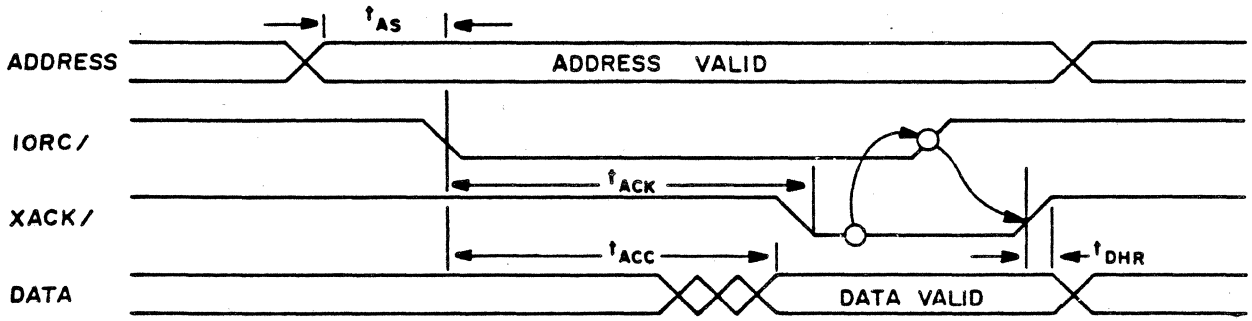
8.2 I/O ACCESS TIMING:

PARAMETER	DESCRIPTION	MIN.	MAX.	UNITS
t_{AS}	Address Set-Up Time	0		ns
t_{AH}	Address Hold Time	0		ns
t_{ACK}	Acknowledge Time	80		ns
t_{TO}	CMD↑ To XACK↑	80		ns
t_{DS}	Write Data Set-Up Time	0		n
t_{DHW}	Data Hold Time For Write	0		n
t_{ACC}	CMD To Data Valid (Read)	0	60	n
t_{DHR}	Read Data Hold Time	30	60	n

Table 8.2 - CONTROL REGISTER READ/WRITE TIMING PARAMETERS



(A) WRITE TO CONTROL REGISTER



(B) READ FROM CONTROL REGISTER

Figure 8.2 - CONTROL REGISTER READ/WRITE TIMING

9.0 APPLICATIONS:

9.1 COMBINED RGB-GRAPH AND RGB-ALPHA:

The RGB-Graph and the RGB-Alpha can be synchronized and their video outputs can be mixed to provide a combination alphanumerics and graphics display. This is accomplished by simply interconnecting the two boards as illustrated in figure 9.1 and programming their CRTC's to conform to the constraints imposed by formulas 1 through 8.

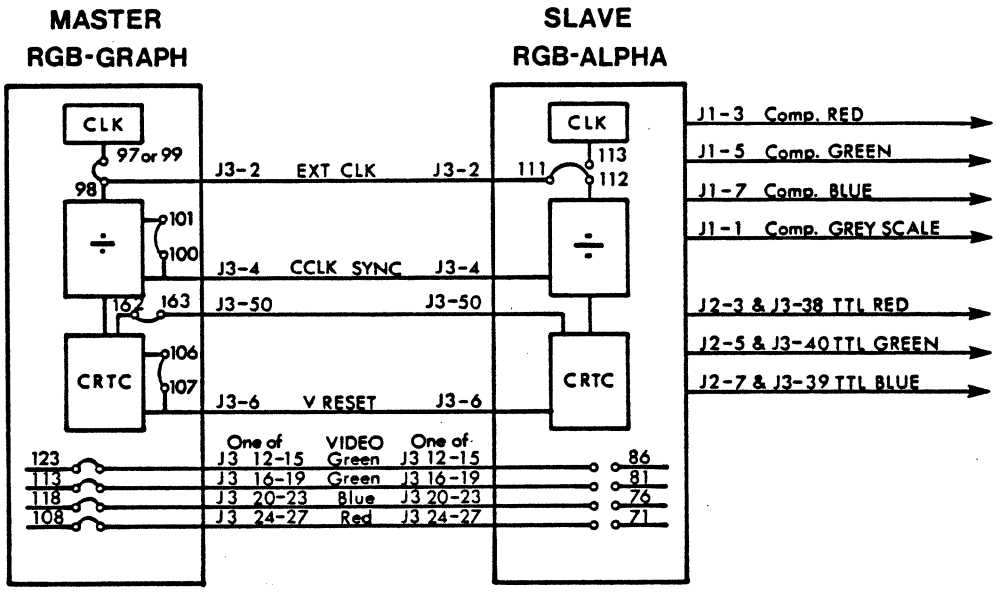


Figure 9.1 - RGB-GRAPH WITH RGB-ALPHA

PROGRAMMING FORMULAS FOR COMBINED RGB-GRAPH AND RGB-ALPHA

1. H. TOTAL x H. DOTS/CELL [GRAPH] = H. TOTAL x H. DOTS/CELL [ALPHA]
2. H. SYNC POSITION [GRAPH] = (H. TOTAL - 1) - (3 CHAR) [GRAPH]
3. V. SYNC WIDTH + V. SYNC POSITION [GRAPH] = (V. TOTAL - 1) + V. ADJUST [GRAPH]
4. V. SYNC WIDTH [GRAPH] = AN ODD NUMBER
5. H. SYNC WIDTH [GRAPH] = 1
6. V. TOTAL [GRAPH] = V. TOTAL [ALPHA]
7. V. ADJUST [GRAPH] = V. ADJUST [ALPHA]
8. V. SYNC POSITION [GRAPH] = V. TOTAL [GRAPH]

Note that when these two boards are combined the RGB-Alpha can not have character cells 11 dots wide and its cursor blink function will not work in non-interlaced displays.

These programming formulas are also used when two RGB-Graph boards are used together.

9.2 VAF-512:

Figure 9.2 shows one application where the RGB-Graph is used with Matrox's new VAF-512, which will be available in the second half of 1981. A more complete block diagram is given in figure 9.3 and a preliminary data sheet for the VAF-512 is also included in this section.

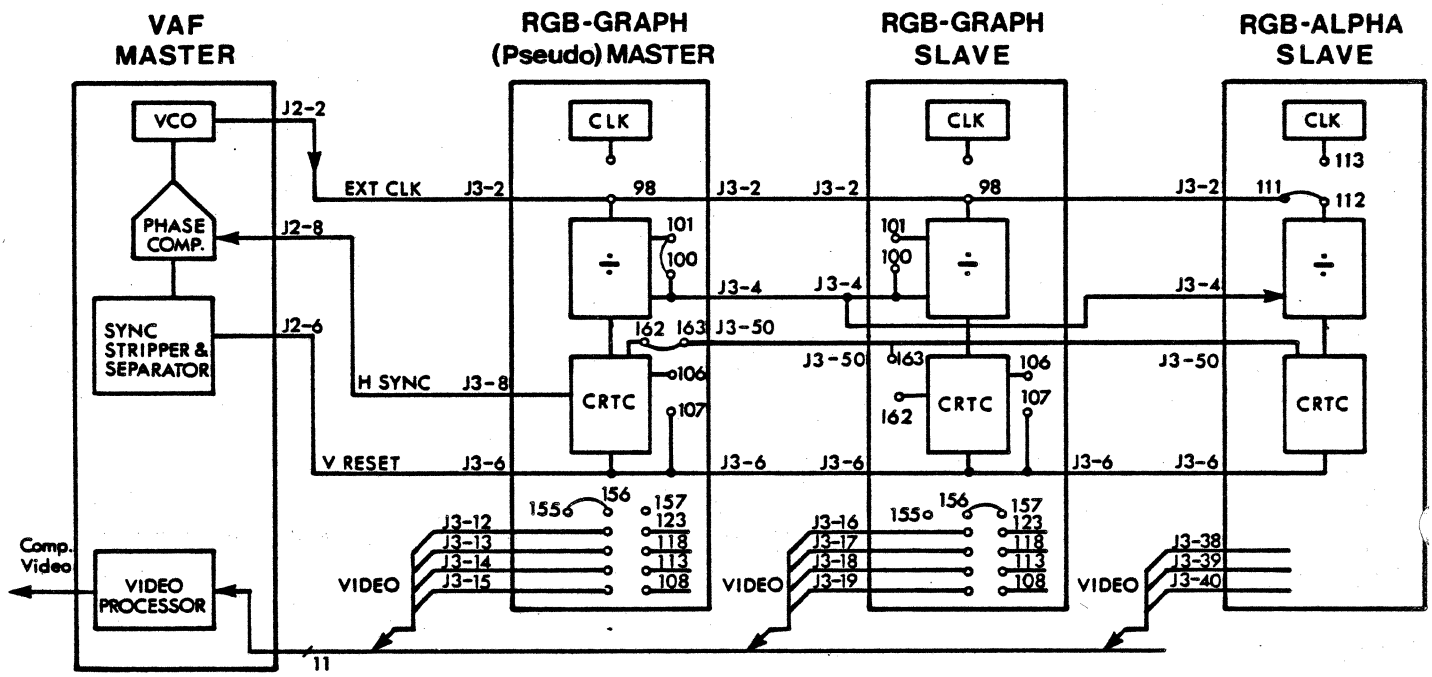


Figure 9.2 - RGB-GRAPH, RGB-ALPHA, VAF COMBINATION

9.0 APPLICATIONS (Cont'd):

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL. 514—735-1182 TELEX: 05-825651

VAF-512

VIDEO PROCESSOR BOARD For RGB-GRAPH FAMILY

* Adds high speed video processing to the RGB-GRAPH board
* Real time frame grabber with 8 bits/pixel (B/W) or 12 bits/pixel (color)
* 512x512 or 512x256 resolution
* 4 video inputs video switcher with 60dB channel isolation
* Built-in phase lock loop and video separator
* Video look-up table with over 16 million displayable colors
* System CPU can read/write video look-up table
* On-board bipolar bit-slice CPU provides high-speed hardware vector generation
* High level graphics primitives such as vectors, circles, area fills and polygons are executed by hardware vector generator
* Drawing speed of 700ns/pixel
* Multibus* compatible, LSI-11/PDP-11 plug-in versions available soon

FUNCTIONAL DESCRIPTION

The VAF-512 board is a high speed video processor board designed to enhance the performance of Matrox color graphic systems (RGB-GRAPH). It plugs into any standard Multibus* backplane and interfaces with the RGB-GRAPH (or up to 3 RGB-GRAPH boards and one RGB-ALPHA) via a single 50-pin ribbon cable. The VAF-512 consists of three independant functional blocks; video digitizer (VD), video look-up processor (VP) and a vector generator (VG).

VIDEO DIGITIZER (VD)- contains a high-speed, low-noise video switcher which enables the CPU to connect up to 4 analog video inputs (either composite video from four different TV cameras or Red, Green and Blue camera outputs) to the 35MHz 8-bit A/D converter. A phase lock loop and video separator locks to the external sync provided by the camera and syncronizes the RGB-GRAPH boards. By digitizing R, G and B signals separately, significantly higher color image quality can be reproduced.

VIDEO LOOK-UP PROCESSOR (VP)- has a three channel (one for each color) high-speed color map RAM (3x256x8, 40ns). By mapping the video outputs from the RGB-GRAPH and RGB-ALPHA boards into Look-up RAM outputs and then converting them into analog video signals by 3 high-speed 8-bit D/A converters, a much higher range of colors (2^{24} = 16,777,216) can be displayed.

VECTOR GENERATOR (VG)-

SYSTEM FLEXIBILITY

The VAF-512's main functional blocks, video digitizer, video look-up processor and video generator, are completely independant of each other with all of the IC's in sockets. This means that the VAF-512 can be optimized for the customer's specific requirements. For example system designs which do not require frame grabbing will use VAF-512 with vector generation and look-up sections incorporated, but without the video digitizer, therefore lowering the price of the board. The same applies for the video generator and look-up processor.

ORDERING INFORMATION

VAF-512 can be ordered with any combination of VD, VP and VG incorporated on the board. In addition the VD can be specified with either a 6 or 8-bit A/D converter.

Ordering No.: VAF-512 - - - / -
- 6 or 8-bit A/D converter
- D - Video digitizer incl.
- P - Video processor incl.
- G - Vector generator incl.

Example: VAF-512 PD/6 contains a video digitizer with a 6-bit A/D converter and video look-up processor but no vector generator.

FEBUARY 1981 · MATROX products covered by Canadian and foreign patent and/or patent pending. PRINTED IN CANADA

9.0 APPLICATIONS (Cont'd):

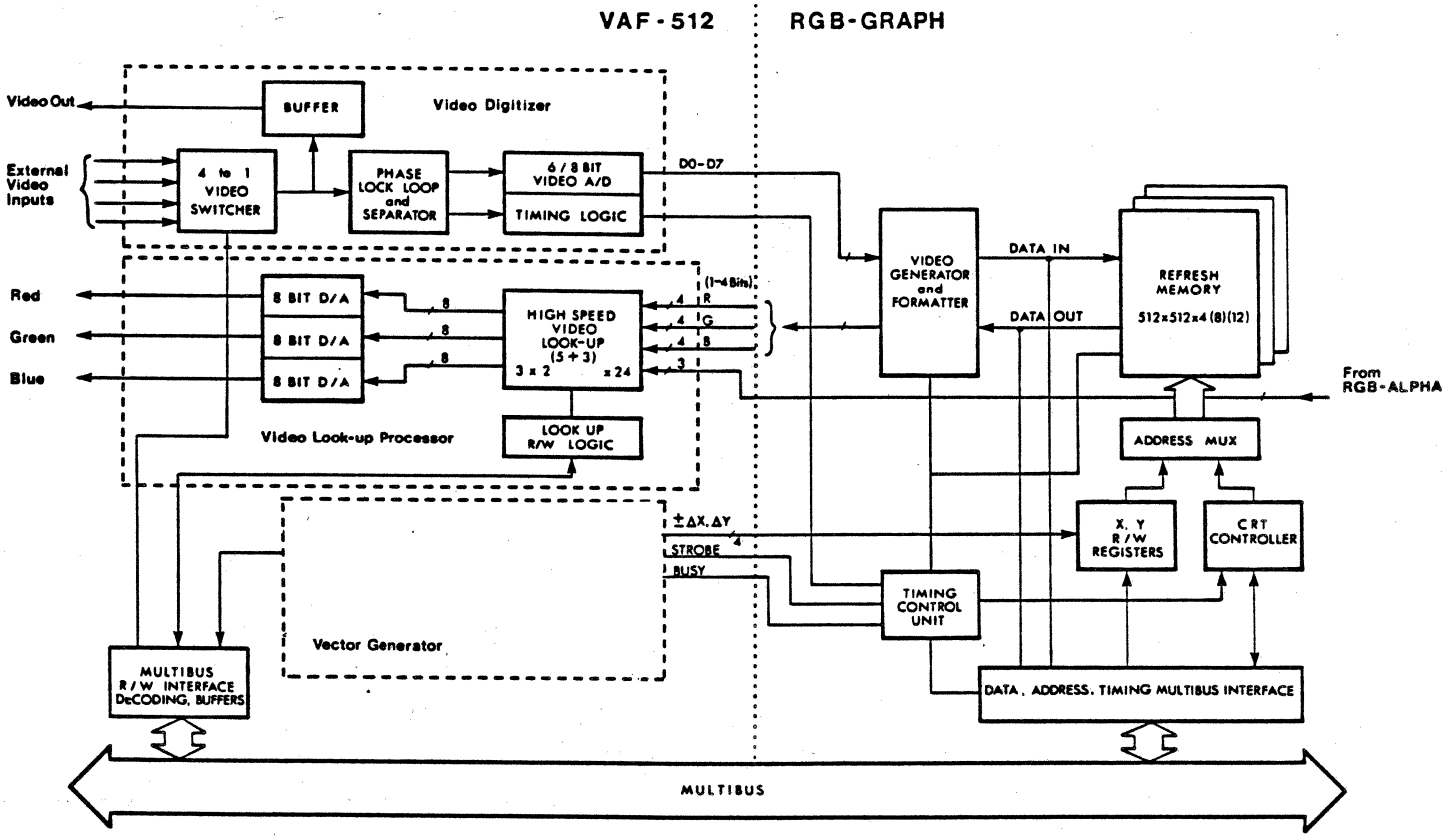


Figure 9.3 - BLOCK DIAGRAM OF VAF-512

10.0 MAINTENANCE AND WARRANTY:

Matrox products are warranted against defects in materials and workmanship for a period of 180 days from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damages.

U. S. customers are to return their products to our U. S. warehouse, at the following address: Matrox International Corporation, Trimex Building, Mooers, N. Y. 12958.

11.0 ORDERING INFORMATION:

The RGB-Graph can be ordered directly from Matrox Electronic Systems Limited or from its worldwide network of distributors.

CRT Controller

SY6545

Synertek® INCORPORATED

MICROPROCESSOR PRODUCTS

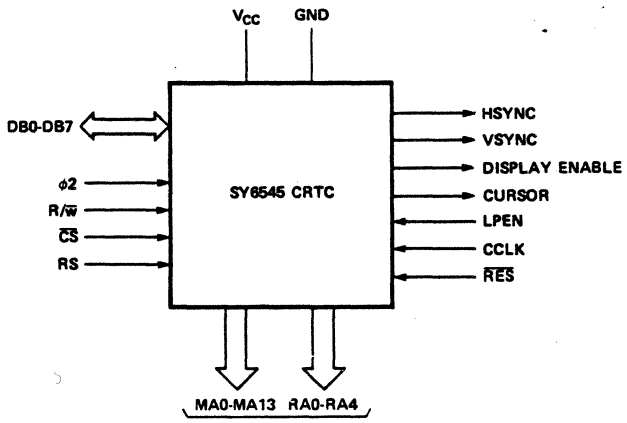
Preliminary

OCTOBER 1979

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6545.
- Internal status register.

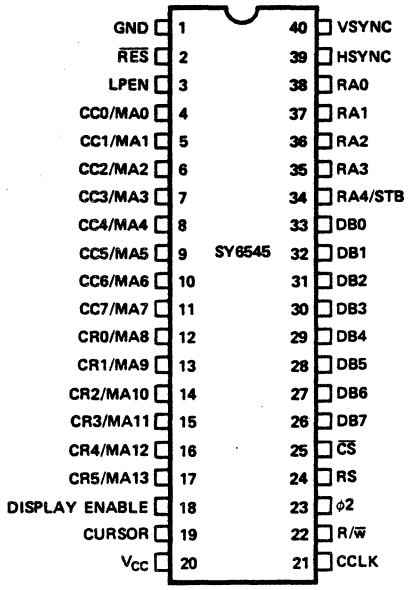
The SY6545 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

INTERFACE DIAGRAM



VIDEO DISPLAY RAM AND CHARACTER ROM

PIN DESIGNATION



ORDERING INFORMATION

Part Number	Package	Clock Rate
SYC6545	Ceramic	1 MHz
SYP6545	Plastic	1 MHz
SYC6545A	Ceramic	2 MHz
SYP6545A	Plastic	2 MHz

MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

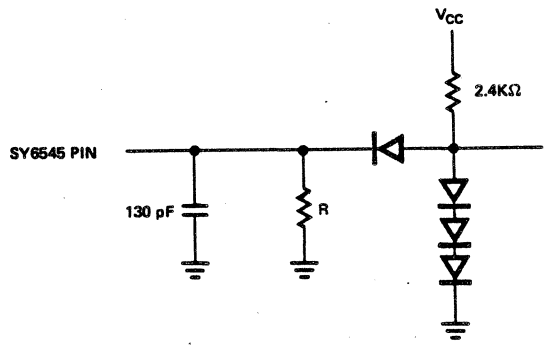
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–	2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	–	10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = 205μA (DB0-DB7) I_{LOAD} = 100μA (all others)	2.4	–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–	0.4	V
P_D	Power Dissipation	–	800	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –	10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–	10.0	pF

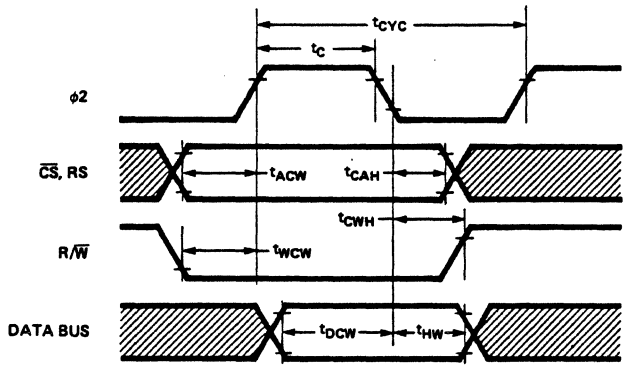
TEST LOAD



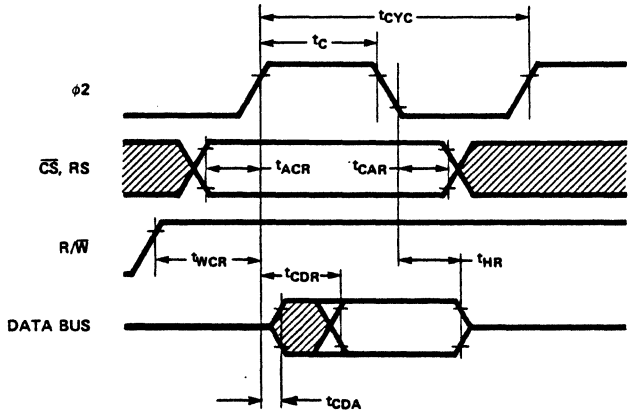
R = 11KΩ FOR DB_0-DB_7
= 24KΩ FOR ALL OTHER OUTPUTS

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

Symbol	Characteristic	SY6545		SY6545A		
		Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACW}	Address Set-Up Time	180	–	90	–	ns
t_{CAH}	Address Hold Time	0	–	0	–	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
t_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
t_{HW}	Data Bus Hold Time	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

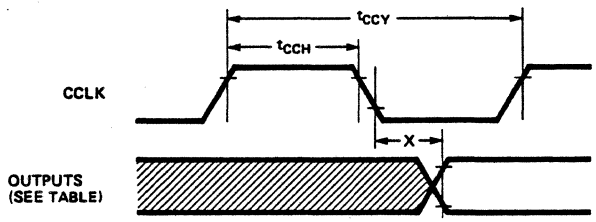
Symbol	Characteristic	SY6545		SY6545A		
		Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACR}	Address Set-Up Time	180	–	90	–	ns
t_{CAR}	Address Hold Time	0	–	0	–	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CDR}	Read Access Time (Valid Data)	–	395	–	200	ns
t_{HR}	Read Hold Time	10	–	10	–	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

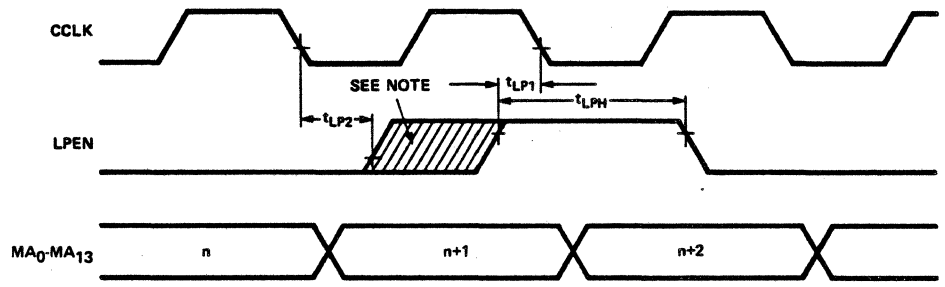
SYSTEM TIMING



Output	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	μs
t_{CCH}	Character Clock Pulse Width	200	—	200	—	ns
t_{MAD}	MA0-MA13 Propagation Delay	—	160	—	160	ns
t_{RAD}	RA0-RA4 Propagation Delay	—	160	—	160	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	—	300	—	300	ns
t_{HSD}	HSYNC Propagation Delay	—	300	—	300	ns
t_{VSD}	VSYNC Propagation Delay	—	300	—	300	ns
t_{CDD}	CURSOR Propagation Delay	—	300	—	300	ns

LIGHT PEN STROBE TIMING



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{LPH}	LPEN Strobe Width	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	120	—	120	—	ns
t_{LP2}	CCLK to LPEN Delay	0	—	0	—	ns

t_r, t_f = 20 ns (max)

MPU INTERFACE SIGNAL DESCRIPTION

$\phi 2$ (Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6545. Since there is no maximum limit to the allowable $\phi 2$ cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6545 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6545; a low on the R/$\overline{W}$ pin allows a write to the SY6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6545 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6545. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6545 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0–MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0–MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0–MA7 function as column addresses CC0–CC7, and MA8–MA13, as row addresses CR0–CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0–CC7 and CR0–CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6545 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0–MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6545 with only a small amount of external circuitry.

DESCRIPTION OF INTERNAL REGISTERS

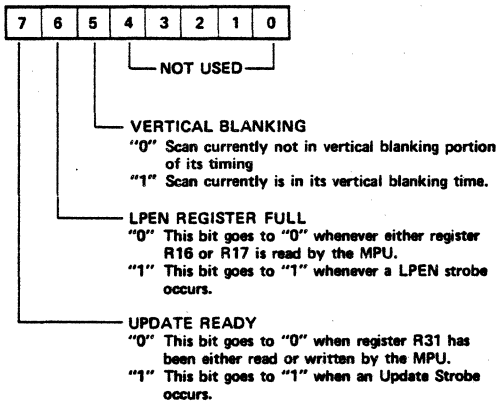
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6545 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6545 data transfers to and from the system MPU. Its contents is the number of the desired register (0–31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

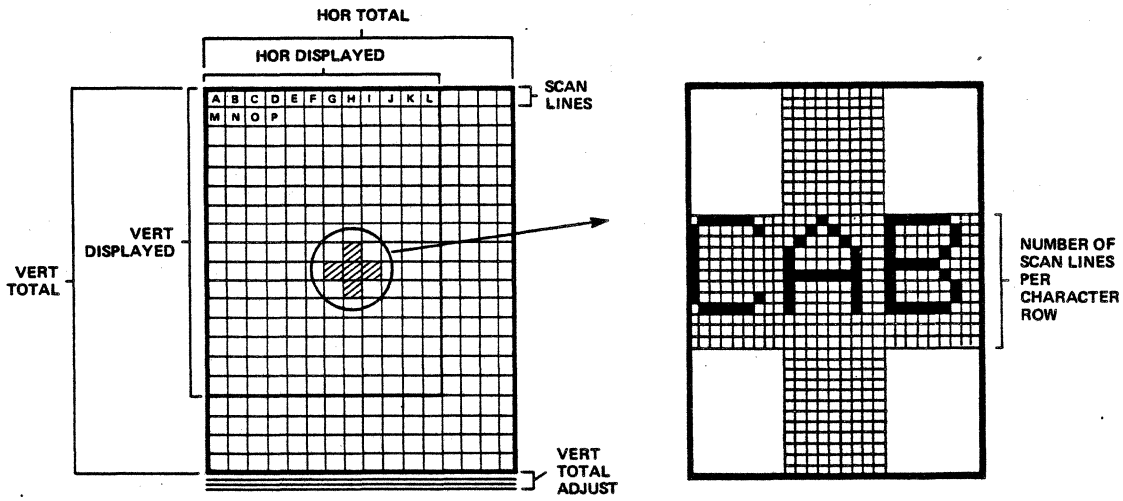


Figure 1. Video Display Format

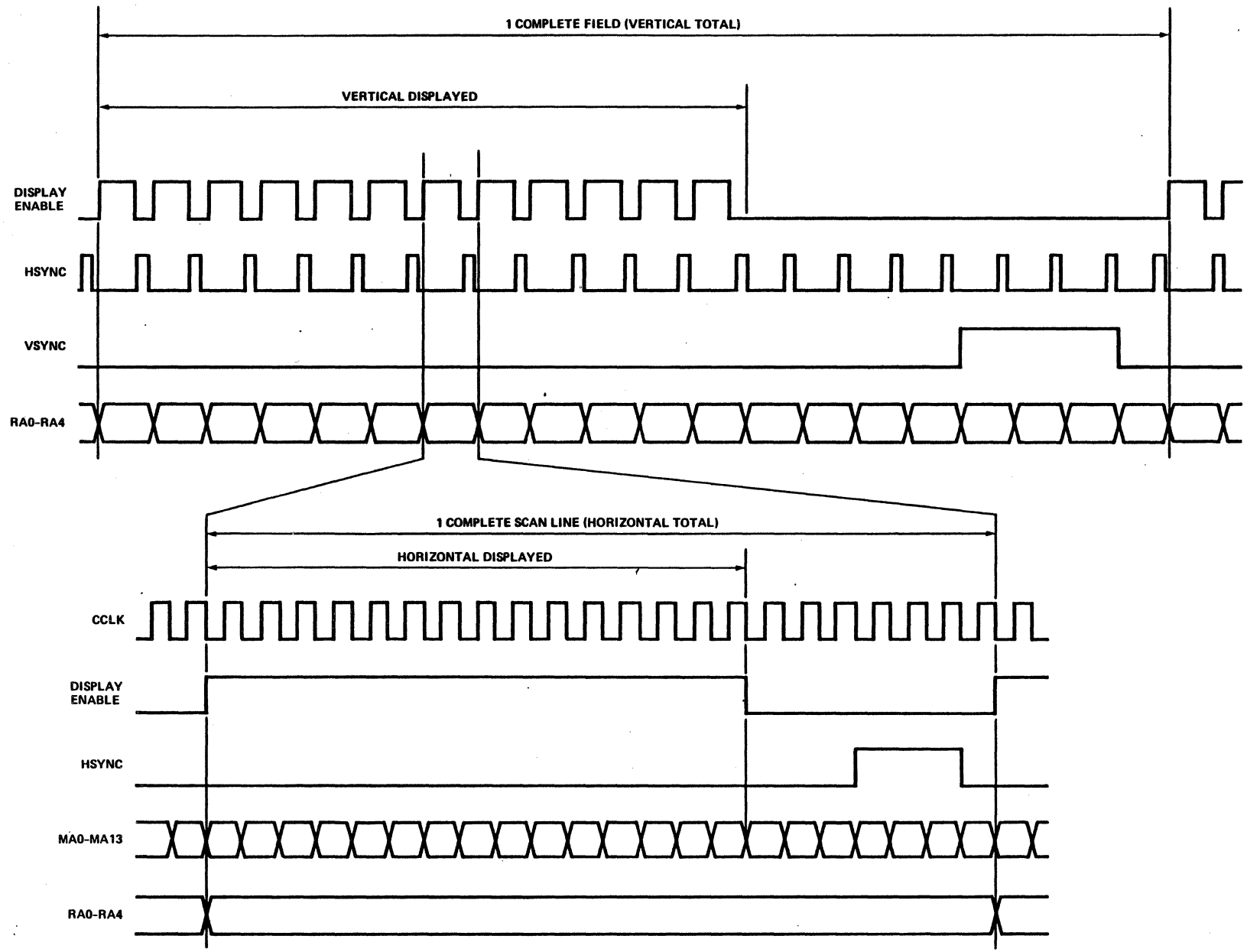
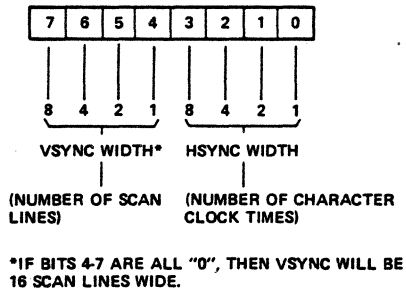


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6545 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0		0	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0		0	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√				●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

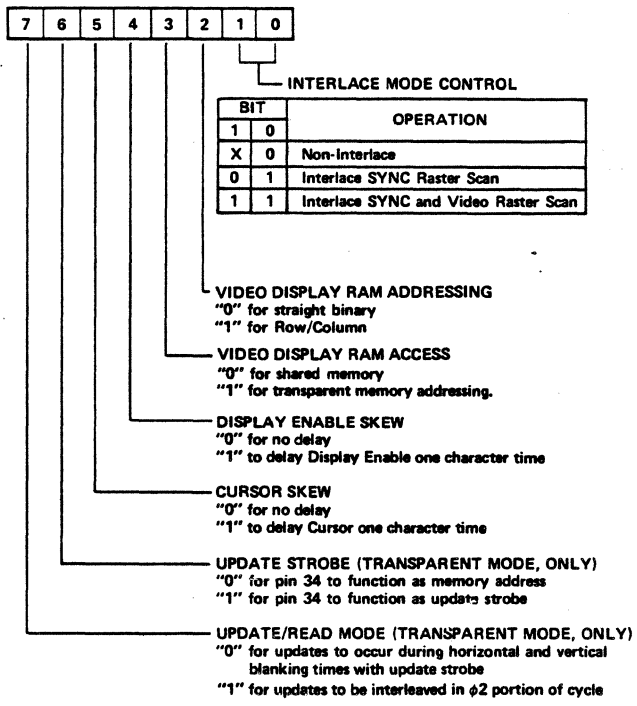
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6545 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	0	1	2	---	---	77	78	79	80	81	---	89
1	80	81	82	---	---	157	158	159	160	161	---	169
2	160	161	162	---	---	237	238	239	240	241	---	249
	⋮							⋮				⋮
	⋮							⋮				⋮
	⋮							⋮				⋮
21	1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
22	1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
23	1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
24	2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
	⋮							⋮				⋮
33	2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	---	---	77	78	79	80	81	---	89
1	256	257	258	---	---	333	334	335	336	337	---	345
2	512	513	514	---	---	589	590	591	592	593	---	601
	⋮							⋮				⋮
	⋮							⋮				⋮
	⋮							⋮				⋮
21	⋮							⋮				⋮
22	5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
23	5888	5889	5890	---	---	5965	5966	5967	5968	5969	---	5977
24	6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
25	6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
	⋮							⋮				⋮
33	8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6545 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6545 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6545. All MPU accesses are made via the SY6545 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

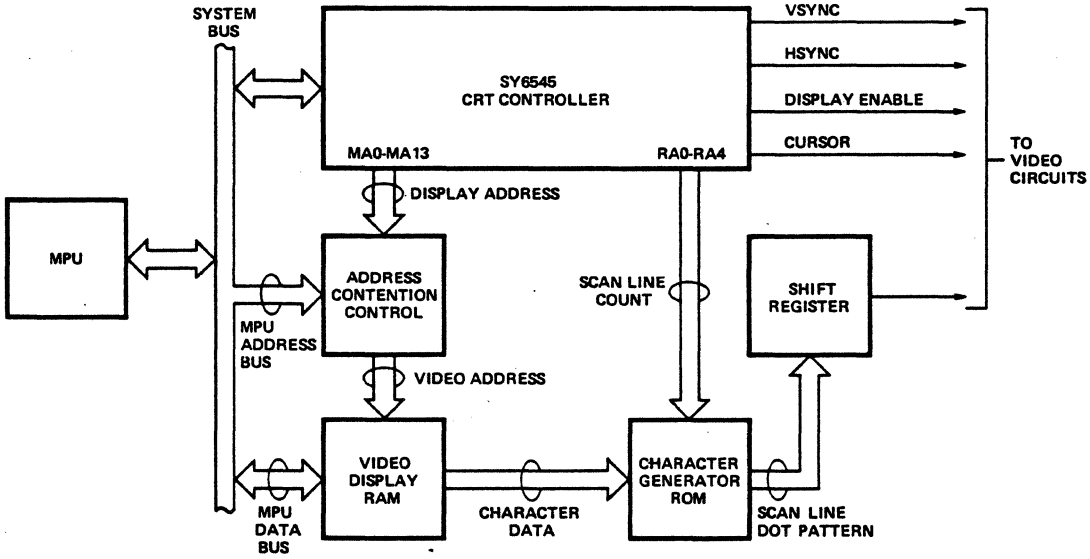


Figure 5. Shared Memory System Configuration

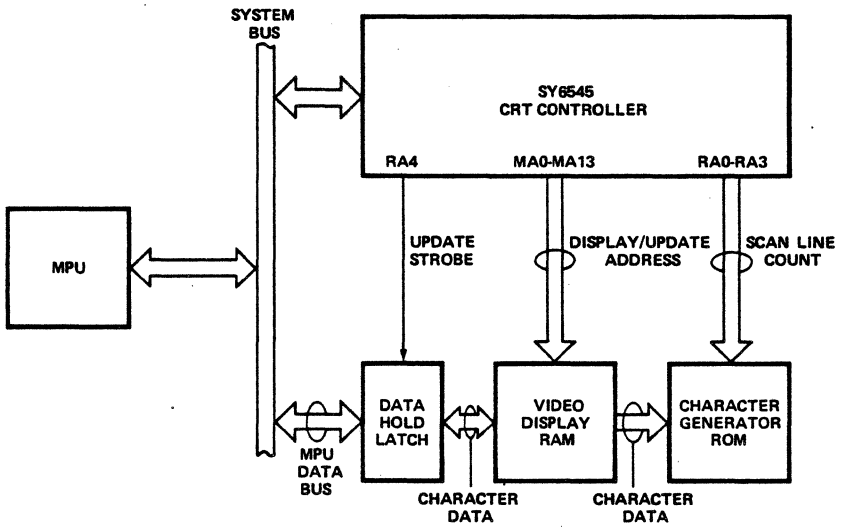


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the SY6545 and the system MPU must be capable of addressing the video display memory. The SY6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6545 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6545 and the MPU has immediate access.

- $\phi1/\phi2$ Memory Interleaving

  This method permits both the SY6545 and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when $\phi2$ is low), the SY6545 address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the SY6545 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

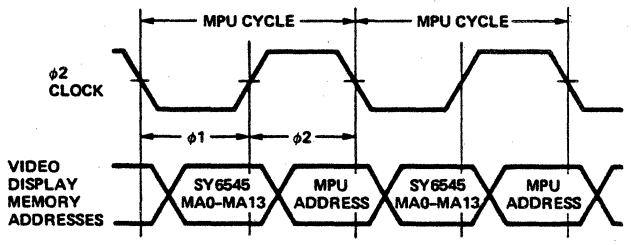


Figure 7. $\phi1/\phi2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6545. In effect, the contention is handled by the SY6545. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi1/\phi2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6545. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi2$. Figure 8 shows the timing.

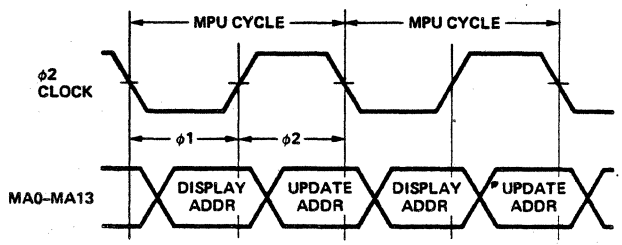


Figure 8. $\phi1/\phi2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in a related Technical Note available from Synertek.

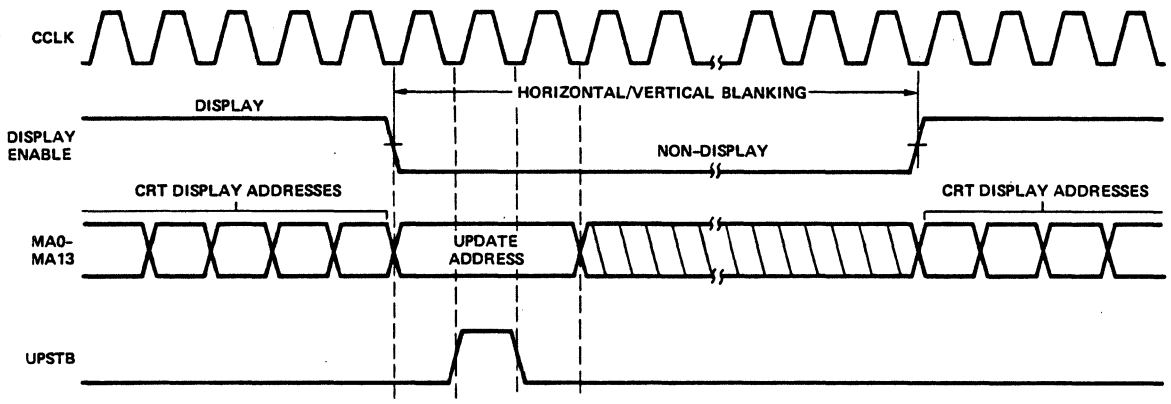


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6545 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered. Figure 12 illustrates the timing.

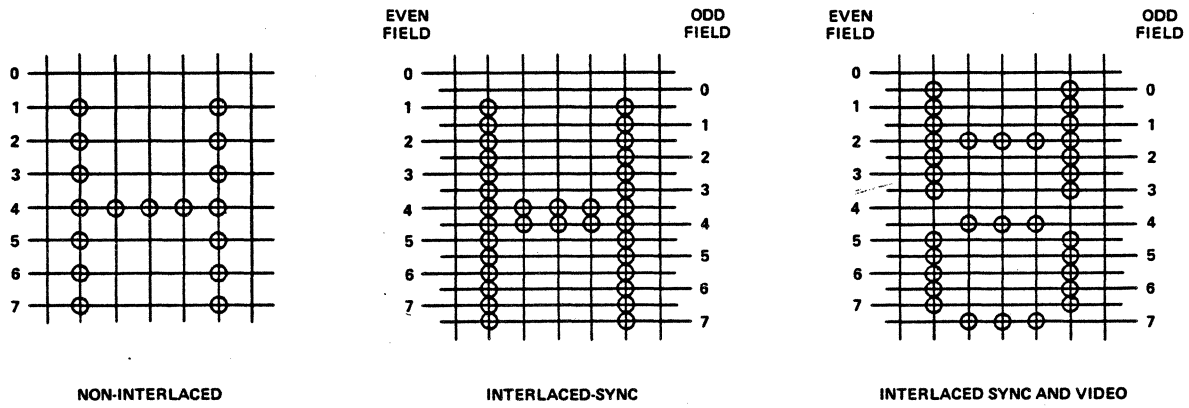


Figure 10. Comparison of Display Modes.

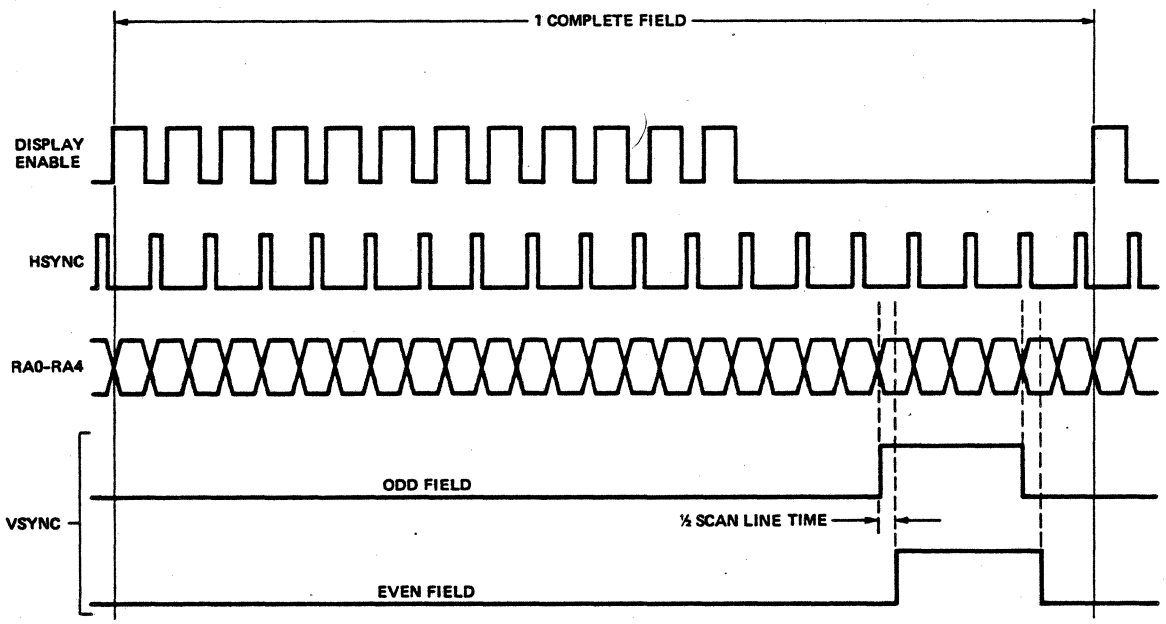


Figure 11. Interlace-Sync Mode Timing

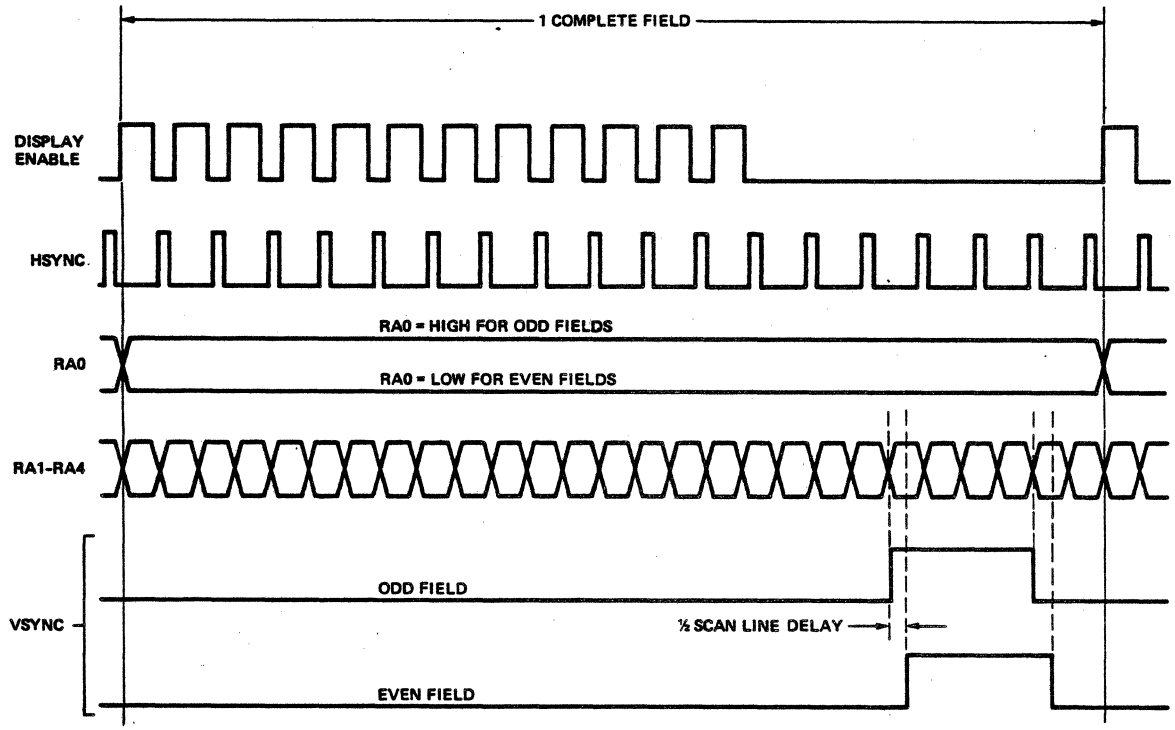


Figure 12. Interlace-Sync-and-Video Mode Timing

Some restrictions on interlace modes of operation are:

a) The Horizontal Total Character count (register R0) must be odd, in order to represent an even number of character times.

b) For Interlaced Sync and Video mode, only, the following registers must be programmed in a non-standard fashion:
   - R4 (Vertical Total) must be programmed to one-half the actual number desired, minus one. For example, for a total of 24 characters high, R4 must contain 11 (decimal).
   - R6 (Vertical Displayed) must be programmed to one-half the actual number desired. For example, for 16 displayed characters high, R6 must contain 8 (decimal).
   - R7 (Vertical Sync Position) must be programmed to one-half the actual number desired.

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 13 illustrates the effect of the delays.

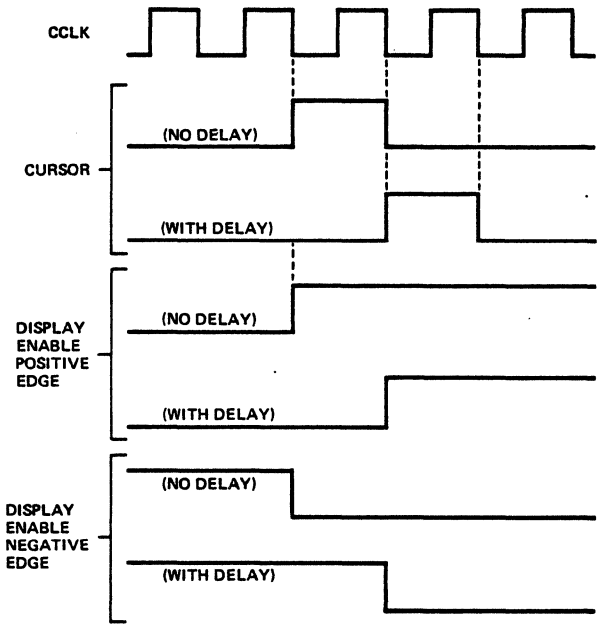


Figure 13. Cursor and Display Enable Skew

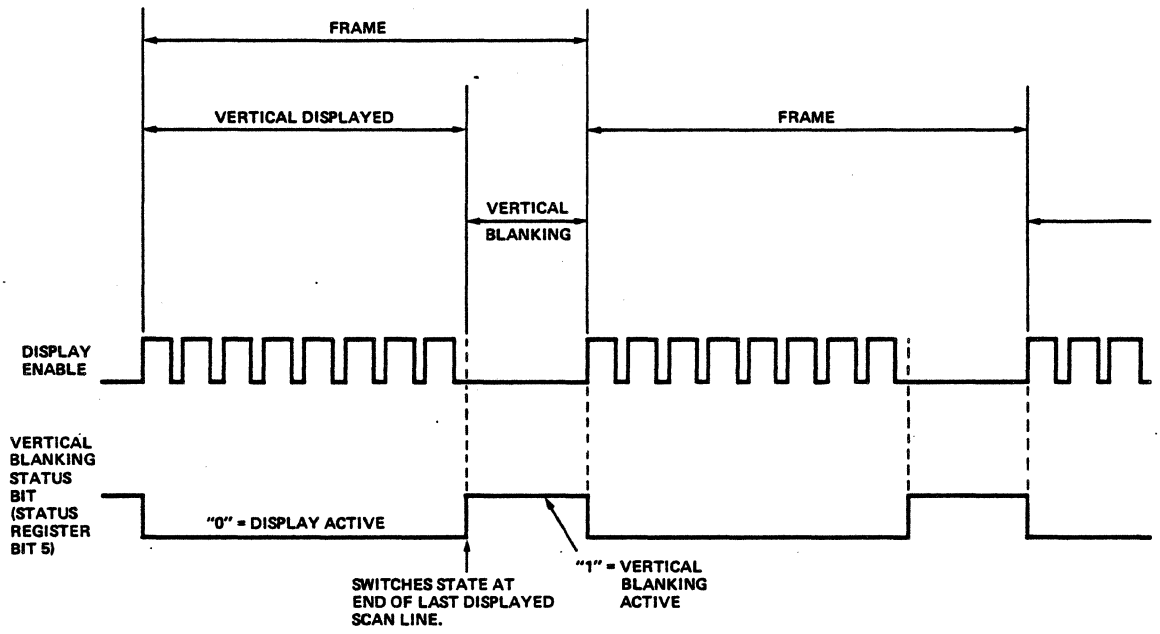
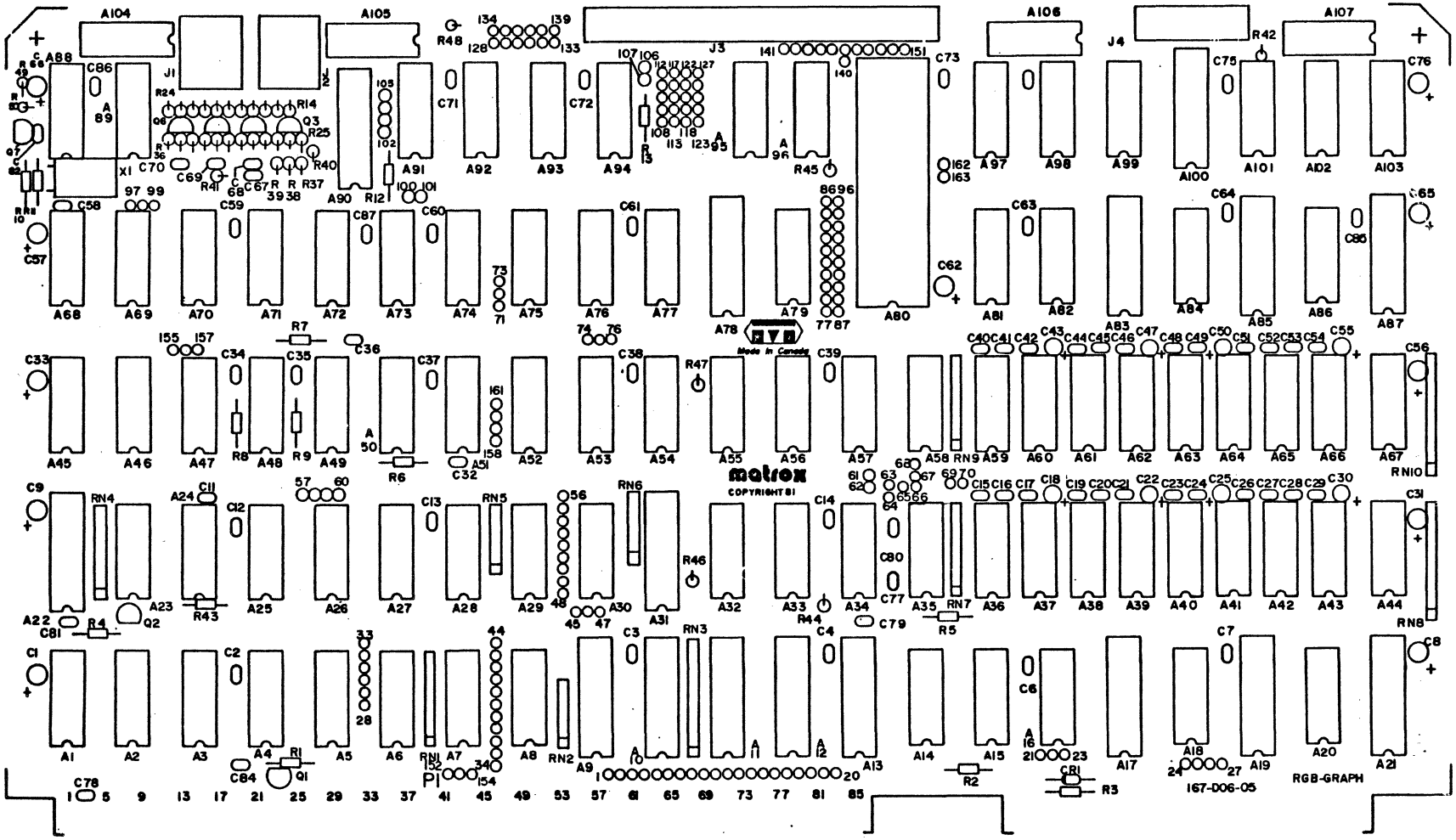
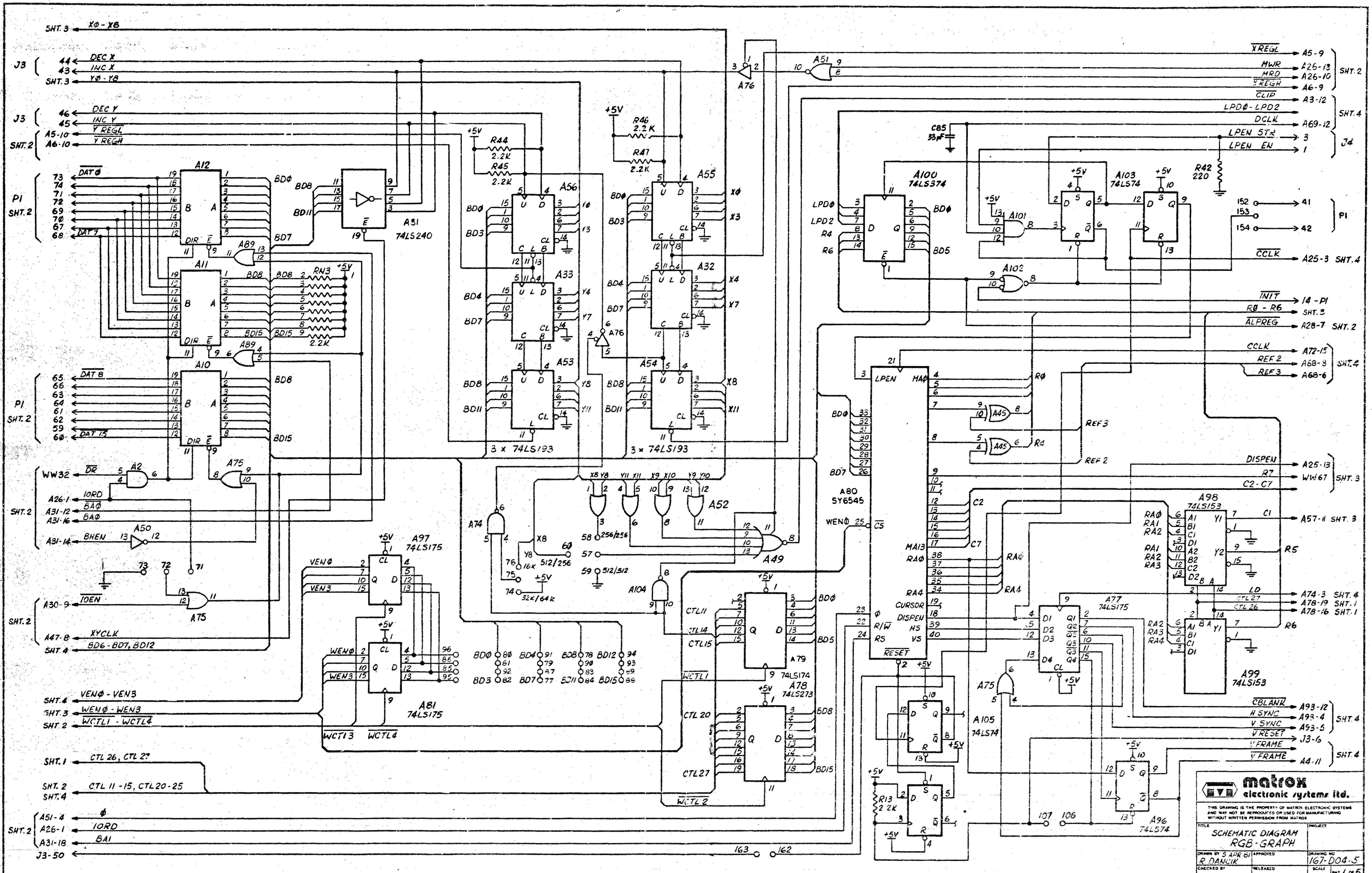


Figure 14. Operation of Vertical Blanking Status Bit

13.0 SCHEMATICS AND PARTS LAYOUT



PARTS LAYOUT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SHT 1 of 5
A12
A11
A10
A31 74LS240
A56
A33
A53
3 x 74LS193
A55
A32
A54
3 x 74LS193
A76
A51
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A74
A104
A2
A75
A89
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A97 74LS175
A81 74LS175
A79 74LS174
A78 74LS273
A100 74LS374
A101
A102
A103 74LS74
A80 SY6545
A45
A98 74LS153
A99 74LS153
A77 74LS175
A105 74LS74
A96 74LS74
R44 2.2K
R45 2.2K
R46 2.2K
R47 2.2K
R42 220
R13 2.2K
RN3 2.2K
C85 33pF
+5V
X0 - X8
DEC X
INC X
Y0 - Y8
DEC Y
INC Y
Y REGL
Y REGH
XREGL
MWR
MRD
Y REGH
CLIP
LPD0 - LPD2
DCLK
LPEN STR
LPEN EN
CCLK
INIT
R0 - R6
ALPREG
CCLK
REF 2
REF 3
DISPEN
R7
C2 - C7
LD
CTL 27
CTL 26
CBLANK
H SYNC
V SYNC
V RESET
V FRAME
V FRAME
WW32
DR
IORD
BA0
BHEN
IOEN
XYCLK
BD6 - BD7, BD12
VEN0 - VEN3
WEN0 - WEN3
WCTL1 - WCTL4
CTL 26, CTL 27
CTL 11 - 15, CTL20 - 25
IORD
BAI
J3
SHT. 2
SHT. 3
SHT. 4
SHT. 1
P1
J4
LPEN
MA0
MA13
RA0
RA4
CURSOR
DISPEN
HS
VS
RESET
R/W
RS
WEN0
CS
256/256
512/256
512/512
16K
32K/64K

SHT. 1 A89-13 BAØ
34 ADI3
32 ADI2
30 ADII
28 ADIØ
44 ADF
43 ADE
42 ADD
41 ADC
45 ADB
48 ADA
47 BAA
P1
A9 74LS240
50 ADI9 → BA9
49 52 51 54 53 56 55 ADI2
1 19
A31 74LS240
58 ADI 2 4 6 → BAØ
57 ADØ 16 14
27 BHEN 18 1
SHT. 1 A50-13 BHEN
A79-12 CTL14
A75-12 IOEN
SHT. 4 VECTOR BUSY
J3-49
P1
21 IORC
22 IOWC
19 MRDC
20 MWTC
A26
SHT. 1 A51-9 MWR
A51-8 MRD
IORD
A49
SHT. 4 A24-3 SEL
P1-23 VACK
Q1 2N3904
C84 100pF
R1 3.3K
A51
R7 470
C36 100pF
SHT. 1 A31-19 XYCLK
SHT. 4 A76-10 WDOT
SHT. 1 A89-5 BAØ
+5V
R43 2.2K
A7 DM8131
A8 DM8131
RN1 2.2K
RN2 2.2K
BAI3
BAE
BAD
BAA
44
A50
+5V
R9 10K
C35 100pf
A48 9602
A29 DM8131
A30 DM8131
RN5 2.2K
RN6 2.2K
BAB BAA BA9 BA8
BA7 BA4
56
A28 74LS155
BA1 BA2 BA3
A50
A27
A31
A45
BA2 BAØ BAØ
BAØ
A47
A74
161 160 159 158 157 156 155
BA3 BAØ
MDØ MD3 MDØ MD3
A14 74LS174
A15
A13 74LS240
A102
A1
A107
WCTL3 WCTL4
RDATAH RDATAL
A27
A47
CRTCA CWTCD
R6 470
A48 9602
C34 220pf 2.2K +5V R8
C32 100pf
A51
BA1 BA2
A5 74LS155
BAØ BA3 BA1 BA2
A6 74LS155
MDØ-MD3 → SHT 3
DATØ 73
DAT4 69
DAT8 65
DAT12 61
DAT1 74
DAT5 70
DAT9 66
DAT13 62
DAT2 71
DAT6 67
DAT10 63
DAT14 59
DAT3 72
DAT7 68
DAT11 64
DAT15 60
P1
DR → A2-5 SHT. 1
DW → A102-11 SHT 4
SYNRD → A25-8 SHT 4
CAS → A25-6 SHT 4
WCTL3-WCTL4 → SHT. 1
ALPREG → SHT. 1
Ø → A80-23 SHT. 1
BAI → A80-24 SHT. 1
STATUS → A76-13 SHT. 4
X REGL → SHT. 1
Y REGL → SHT. 1
WDATAL → WW 28 SHT 4
WCTLI → SHT. 4, SHT. 1
X REGH → A54-11 SHT. 1
Y REGH → A53-11 SHT. 1
WDATAH → WW 30 SHT 4
WCTL2 → A78-11 SHT. 1

matrox electronic systems ltd.

TITLE: SCHEMATIC DIAGRAM RGB-GRAPH
PRODUCT:
DRAWN BY: S. APR. 81
R. DANCIK
APPROVED:
CHECKED BY:
RELEASED:
DRAWING NO: 167-004-5
SCALE:
SHT 9 OF 5

J3
32 36 31 35 30 34 29 33
147 148 140 149 146 150 145 151
SDI3
SDIØ
SDIØ SDI1 SDI2 SDI3
SDOØ-SDO3
DCLK → A69-12 SHT. 4
SH/L → A15-6
A22-16 HRS
A1-8 RAS
A25-6 CAS
A24-9 BCLE
A22-6 R/C
SHT. 4
A57 74S153
A34 74S153
A58 74S153
A35 74S153
SHT. 1
A80-4 RØ
A22-9 CØ
A55-7 X3
A55-6 X2
A80-5 R1
A98-7 C1
A32-3 X4
A56-3 YØ
RN9 33 AØ A1
A45-6 R2
A80-12 C2
A32-2 X5
A56-7 Y3
A45-8 R3
A80-13 C3
A32-6 X6
A33-3 Y4
RN7 33 A2 A3
A45-6 R4
A80-14 C4
A32-7 X7
A33-2 Y5
A98-9 R5
A80-15 C5
A56-2 Y1
A33-6 Y6
RN9 33 A4 A5
A99-7 R6
A80-16 C6
A56-6 Y2
A33-7 Y7
A80-9 R7
C7
A80-17 X8
A54-3 Y8
A53-3
RN7 33 A6 A7
C80 22pF
C77 470pF
R2 33
R5 33
A83 74LS299
A85 74LS374
A107
A87 74LS299
A17 74LS299
A19 74LS374
A21 74LS299
A19 74LS374
RDØØ RDØ3 RDIØ RDI3
RDØ4 RDØ7 RDI4 RDI7
RDØ8 RDØ11 RDI8 RDI11
RDØ12 RDØ15 RDI12 RDI15
A59 A60 A61 A62
A63 A64 A65 A66
A36 A37 A38 A39
A40 A41 A42 A43
WØ W3
W4 W7
W8 W11
W12 W15
+5V
-12V
-5V
+12V
R 220
CR1 IN751A
A82 74LS399
A2
A86 74LS399
A16 74LS399
A20 74LS399
A84 74LS253
A84 74LS253
A18 74LS253
A18 74LS253
MDØ MD1 MD2 MD3
SHT. 4 A96-5 FGR
A25-8 SYNRD
SHT. 1 A55-3 XC
A55-2 X1
SHT 2 MDØ-MD3
SHT. 4 A1-11 FDS
A102-11 DW
SHT. 4 A4-3 PRMEM
RN10 1.0K
A67 74S288
A44 74S288
RN8 1.0K
WENØ WEN1 WEN2 WEN3
SHT. 1 WENØ-WEN3
SHT. 4 A4-9 PRMEM
SHT 1 A80-18 DISPEN
SHT 4 A22-15 WRS
A25
A15
SHT. 4 A73-12 SYNWR

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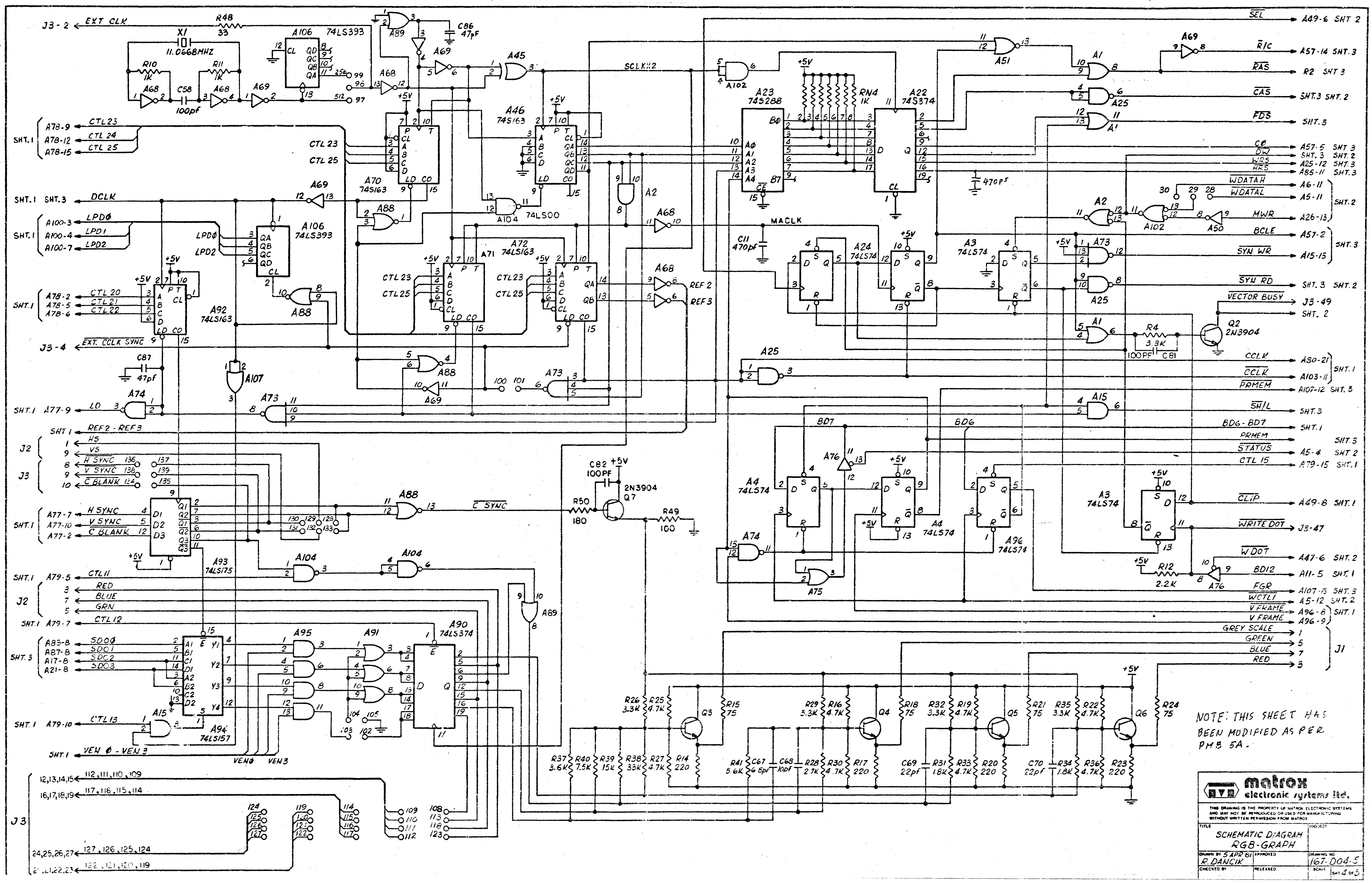
TITLE: SCHEMATIC DIAGRAM RGB-GRAPH
PROJECT:
DRAWN BY: R. DANCIK 5 APR 81
APPROVED:
DRAWING NO: 167-004-5
CHECKED BY:
RELEASED:
SCALE:
SHT 3 OF 5



J3-2 EXT CLK
R48 33
X1 11.0668MHZ
R10 1K
R11 1K
C58 100pf
A106 74LS393
A89
C86 47pF
A45
SCLKX2
A46 74S163
A70 74S163
CTL 23
CTL 24
CTL 25
SHT.1 SHT.3 DCLK
LPD0
LPD1
LPD2
A104 74LS00
A88
A71
A72 74LS163
A92 74LS163
CTL 20
CTL 21
CTL 22
J3-4 EXT. CCLK SYNC
C87 47pf
A107
A74
A73
A68
REF 2
REF 3
SHT.1 REF2 - REF3
HS
VS
H SYNC
V SYNC
C BLANK
A93 74LS175
C SYNC
CTL 11
RED
BLUE
GRN
CTL 12
SD00
SD01
SD02
SD03
A94 74LS157
CTL 13
A95
A91
A90 74LS374
VEN 0 - VEN 3
VEN0
VEN3
C82 100PF
2N3904 Q7
R50 180
R49 100
A2
MACLK
C11 470pf
A23 74S288
RN4 1K
A22 74S374
A102
A51
A1
A25
A69
SEL A49-6 SHT.2
R/C A57-14 SHT.3
RAS R2 SHT 3
CAS SHT.3 SHT.2
FDS SHT.3
C0 A57-5 SHT.3
DW SHT.3 SHT.2
WRS A25-12 SHT.3
HRS A85-11 SHT.3
470pF
WDATAH A6-11
WDATAL A5-11 SHT.2
MWR A26-13
A50
BCLE A57-2
SYN WR A15-13 SHT.3
SYN RD SHT.3 SHT.2
VECTOR BUSY J3-49
SHT.2
A24 74LS74
A3 74LS74
R4 3.3K
100PF C81
Q2 2N3904
CCLK A80-21 SHT.1
CCLK A103-11
PRMEM A107-12 SHT.3
A15
SH/L SHT.3
BD7
BD6
BD6-BD7 SHT.1
PRMEM SHT.3
STATUS A5-4 SHT.2
CTL 15 A79-15 SHT.1
A4 74LS74
A76
A96 74LS74
A3 74LS74
CLIP A49-8 SHT.1
WRITE DOT J3-47
W DOT A47-6 SHT.2
R12 2.2K
BD12 A11-5 SHT.1
A75
FGR A107-13 SHT.3
WCTL1 A5-12 SHT.2
V FRAME A96-8 SHT.1
V FRAME A96-9
GREY SCALE
GREEN
BLUE
RED
J1
Q3
Q4
Q5
Q6
NOTE: THIS SHEET HAS BEEN MODIFIED AS PER PMB 5A.
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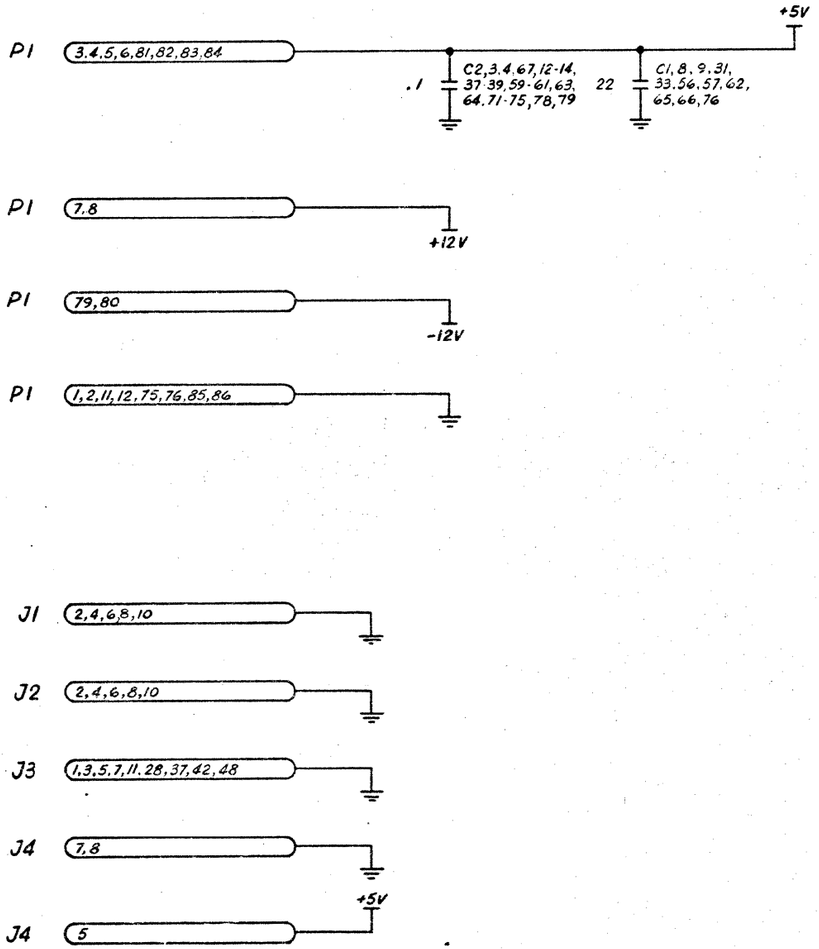
TITLE
SCHEMATIC DIAGRAM
RGB-GRAPH
DRAWN BY 5 APR 81
R. DANCIK
APPROVED
CHECKED BY
RELEASED
DRAWING NO 167-D04-5
SCALE
SHT 4 OF 5



PARTS #	IC REFERENCE	+12V	-12V	+5V	-5V	GND
74S00	A25			14		7
74LS00	A74, 104			14		7
74S02	A88			14		7
74LS02	A26, 51			14		7
74LS04	A50, 68			14		7
74LS08	A2, 15, 95, 102			14		7
74LS10	A73			14		7
74LS21	A27, 101			14		7
7425	A49			14		7
74S32	A1			14		7
74LS32	A37, 52, 75, 89, 91, 107			14		7
74LS74	A3, 4, 24, 96, 103, 105			14		7
74S86	A45			14		7
74LS125	A76			14		7
74LS153	A98, 99			16		8
74S153	A34, 35, 57, 58			16		8
74LS155	A5, 6, 28			16		8
74S157	A94			16		8
74S163	A70, 46			16		8
74LS163	A71, 72, 92			16		8
74LS174	A14, 79			16		8
74LS175	A77, 81, 93, 97			16		8
74LS193	A32, 33, 53-56			16		8
74LS240	A9, 13, 31			20		10
74LS253	A18, 84			16		8
74LS273	A78			20		10
74S288	A23, 44, 67			16		8
74LS299	A17, 21, 87			20		10
74LS374	A19, 85, 90, 100			20		10
74LS393	A106			14		7
74LS399	A16, 20, 86			16		8
DM8131	A7, 8, 29, 30			16		8
DM8303	A10, 11, 12			20		10
SY6545	A80			20		1
9602	A48			16		8
4164-150	A36-43, 59-66					16
74S04	A69			14		7
74S374	A22			20		10

PARTS #	IC REFERENCE	SPARES
74S04	A69	1

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   - ALL RESISTANCES ARE IN OHMS 1/4W, 10%.
   - ALL CAPACITORS ARE MICROFARAD.

matrox electronic systems ltd.

TITLE: SCHEMATIC DIAGRAM RGB-GRAPH

PROJECT:

DRAWN BY: 5 APR 81 R. DANCIK

APPROVED:

DRAWING NO: 167-D04-5

matrox
electronic systems ltd.
5800 ANDOVER AVE., T.M.R., QUE., H4T 1H4, CANADA
TEL.: 514—735-1182 TELEX: 05-825651

PRODUCT FAILURE REPORT

If you are returning one of our products for repair, you must fill out this form and return it with the defective unit. The information so provided is necessary for us to provide a high standard of service.

COMPANY NAME AND ADDRESS: _____

_____

NAME OF UNIT: _____

MODEL NO.(on silkscreen): _____ SERIAL NO.(on label): _____

DATE UNIT RECEIVED: _____ DATE UNIT FAILED: _____ OR DEAD ON ARRIVAL [].

MEMORY BASE ADDRESS USED: _____ I/O BASE ADDRESS USED: _____

PLEASE DESCRIBE THE SYSTEM THAT THE UNIT IS USED IN (CPU,BUS,MEMORY,ETC.): _____

_____

_____

_____

UNIT CONFIGURATION (50 or 60 Hz, attributes used, display resolution selected, etc.): _____

_____

_____

_____

_____

FAULT IS CONSTANT [] FAULT IS INTERMITTENT []

PLEASE DESCRIBE THE FAULT: _____

_____

_____

_____

_____

_____

_____

THE FOLLOWING SPACE IS FOR FACTORY USE ONLY

CORRECTIVE STEPS TAKEN: _____

_____

_____

_____

_____

_____

_____

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TEL.: (514) 735-1182 TELEX: 05-825651