

DESIGN IMPROVEMENTS IN ALWAC III-E

The system of numbering the half-word cells in working storage has been modified for ALWAC III-E:

ALWAC III	ALWAC III-E
00 01 02 03 04 05 06 07	00 80 01 81 02 82 03 83
08 09 0a 0b 0c 0d 0e 0f	04 84 05 85 06 86 07 87
10 11 12 13 14 15 16 17	08 88 09 89 0a 8a 0b 8b
18 19 1a 1b 1c 1d 1e 1f	0c 8c 0d 8d 0e 8e 0f 8f
20 21 22 23 24 25 26 27	10 90 11 91 12 92 13 93
28 29 2a 2b 2c 2d 2e 2f	14 94 15 95 16 96 17 97
30 31 32 33 34 35 36 37	18 98 19 99 1a 9a 1b 9b
38 39 3a 3b 3c 3d 3e 3f	1c 9c 1d 9d 1e 9e 1f 9f

In ALWAC III the pattern in which instructions are picked up is 00, 08, 10, 18, etc. The pattern in ALWAC III-E is 00, 80, 04, 84, 08, 88, etc. In III-E, both instructions in a word are picked up at once and the second is executed as soon as the first is finished. If the addresses in the two instructions are in ascending order, this leads to a fifty-per-cent reduction in access time. If the addresses in such instructions are randomly assigned, the double pickup still leads to a reduction in access time of approximately twenty-five per cent.

ALWAC III in SHIFT operations a0, a2, a4, and a6, can shift up to 31 places; III-E shifts up to 63 places in these operations.

ALWAC III's a8 operation, SCALE, has been eliminated from the III-E.

In ALWAC III's FLOATING POINT SHIFT, the double-length register AB is shifted right or left as required to obtain a 1 as the left-hand bit of B and all 0's in A. If A is not zero, such a shift will be to the right; if A is zero and the left-hand bit of B is 0, such a shift will be to the left. The number of places shifted is stored in the D register, positive for right shifts and negative for left, and the overflow is turned on if both A and B were clear. In ALWAC III E's FLOATING POINT SHIFT, A and B are shifted left until the left-hand bit of A is 1, and the number of places shifted is stored in D with a positive sign. The overflow is turned on and D is cleared if both A and B were clear.

In ALWAC III, operation code 4c, COPY ADDRESS to W, makes the bit in W immediately to the left of that address correspond to the sign of A. (Plus is 1, minus is 0.) In ALWAC III-E, 4c changes nothing but the address in W.

In ALWAC III-E, operation code f8, SIGN INPUT, sets the sign of A to correspond to the right-hand bit of the computer code for the key struck on the FLEXOWRITER.

In ALWAC III-E, if any add operation or the roundoff operation causes overflow, the carry from the left end of A is held, and may be shifted back into A by either of the SHIFT RIGHT operations. This bit is cleared out of its storage by any operation which changes any bit of A, including shifting and clearing.

In ALWAC III, operation codes beginning with 0, 2, or 3 can accommodate a second operation code (one not requiring an address) in the address syllable. When such a second operation occurs, the code for the first operation must be increased by 1. In ALWAC III-E, operations (not requiring addresses) which can accommodate a second operation in the address syllable have odd-number codes in normal use and must be reduced by 1 when the address syllable is to be used for another operation.

The NEXT ORDER ADDRESS register of ALWAC III becomes the INSTRUCTION ADDRESS register of ALWAC III-E. When ALWAC III-E is stopped by moving the NORMAL, STOP, ONE-STEP switch to STOP, the control panel shows the operation code which is about to be carried out, the address of the operand on which it will operate, and the address from which both were picked up.

ALWAC III-E has a STOP operation, code 1a, and a START button. After operation 1a, the INSTRUCTION ADDRESS register does not show the address from which the STOP instruction was picked up. The computer may be started again by pressing the START button. The STOP operation is a form of jump. When the START button is pressed, control jumps to the cell specified by the address with the STOP operation.

ALWAC III-E has three other new operations: e2, copy E to W; c4, copy B to W; and c6, copy D to W. Two of the ALWAC III operations have been eliminated from the III-E: 08, copy E to B; and 0a, copy E to D.

In ALWAC III-E, the E register is only a half word, the left-hand 16 bits. In $E \rightarrow A$, $E \rightarrow W$, and $A \rightarrow E$, the right-hand 16 bits and the sign of A and W are left unchanged. The modification of an instruction address by E is accomplished by adding 1 to the related operation code, which is normally an even number. Changing such an operation code to the next higher odd number subtracts the E register (modulo 256) from the address. In its use as a tally, the E register is counted down, so that the effect of the subtraction is to assign successive addresses to repetitive operations in ascending order. For example, if the basic form of an instruction calls for adding cell 28, and E contains 28, the instruction operates, when augmented by 1, on cell 00 because of the subtraction of E from the address. When E is now counted down, the next occurrence of the same instruction, because 27 is now subtracted from the address, will operate on cell 01. It should be noted that because of the renumbering of half-word cells (as mentioned earlier), 00 and 01 in ALWAC III-E are the addresses of successive full words, not of successive half words as in ALWAC III.

The following example shows the kind of economy in coding that can be effected by the E register's address modification. The results of the two codes are identical: the summation of eight numbers from consecutively numbered memory cells. As noted earlier, the sequence of storage addresses is different for each code.

ALWAC III

Stored Data

In 3e, 00000008

In 2e, 00020000

Storage Address of Instruction	Instruction and Address	Effect
00	56 3e	Puts contents of 3e into E register.
08	28 --	Clears A register.
10	→ 60 40	Adds contents of 40 into A register.
18	68 10	Swaps contents of 10 and A: 10 now contains the first sum and A now contains the ADD instruction, which is to be modified.
20	62 2e	Adds 00020000 to instruction in A, changing it to 60 42.
28	68 10	Swaps 10 and A, putting the instruction in place to be carried out again, and returning sum to A for further addition.
30	← 16 10	Counts E down 1 (to 00000007), jumping to 10 if E is not zero.
38	etc.	

ALWAC III-E

Stored Data

In 1f, 00000008

00	56 1f	Puts contents of 1f into E register.
80	28 --	Clears A register.
04	→ 61 28	Adds contents of 20 into A register. (Since the operation in 04 is 61, E register is subtracted from 28.)
84	← 16 04	Counts E down 1 (to 00000007), jumping to 04 if E is not zero. (The next 61 operation will be carried out on the contents of 21.)
08	etc.	

In addition to eliminating three instructions out of five by means of the E register, ALWAC III-E code, as noted earlier, offers a speed advantage by means of the double pickup of instructions.