LAWRENCE RADIATION LABORATORY
Livermore, California

Preliminary
Specification
LES 11868
October 12, 1964

PARALLEL NETWORK DIGITAL COMPUTING SYSTEM

1.0 PURPOSE

1.1 The purpose of the computing system described in this specification is to complement the existing computing equipment at the Lawrence Radiation Laboratory. In particular, the system shall be especially useful in the solution of certain mesh type nuclear research problems.

2.0 FUNCTIONAL CHARACTERISTICS

2.1 The computing system herein described in detail shall generally consist of a number of identical parallel arithmetic processors operating simultaneously on instructions issued by a central control unit.

2.2 The system shall be capable of executing many of the problems currently being done on conventional digital computers at the Lawrence Radiation Laboratory at a speed considerably greater than is presently being attained.

2.3 The system shall be capable of operating as an independent digital computing system, as well as interacting with a conventional digital computer which could provide additional I/0 capabilities.

3.0 EQUIPMENT

The system shall include the following major sections: (See Figure 1)

3.1 The Processor Network and the Processor Memories.

3.2 The Network Program Memory.

3.3 The Processor Control Unit.

3.4 The Input-Output Section.

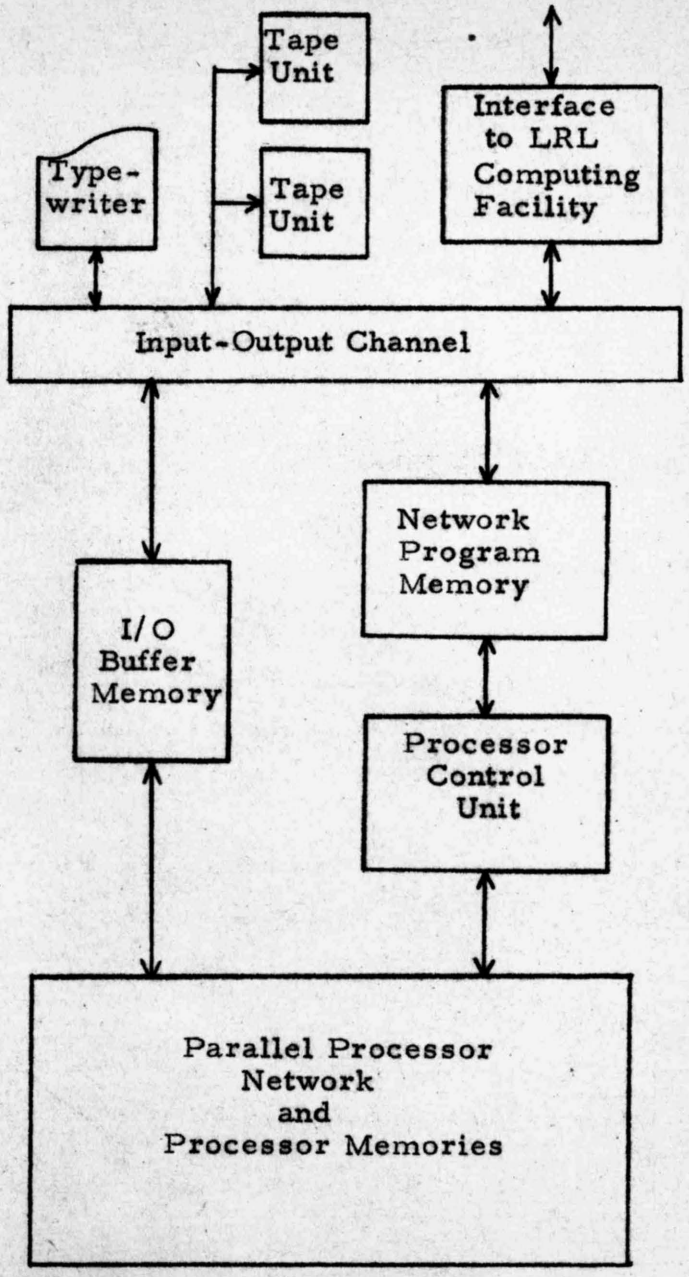
3.4.1 I/0 Buffer Memory.

3.4.2 Console typewriter.

3.4.3 Two magnetic tape units.

3.4.4 Interface to LRL computing facility.

TITLE **Parallel Network Digital Computing System**



SUGGESTED SYSTEM ORGANIZATION

FIGURE 1

4.0 DESIGN FEATURES & OPERATIONAL CHARACTERISTICS OF THE MAJOR SECTIONS

4.1 Processor Network and Processor Memories

4.1.1 It is not the intent of this specification to state the exact number of processors best suited for the system, however, a minimum qualification shall be that the average instruction execution time in microseconds calculated from the results of the coding to be done in paragraph 8.1, when divided by the proposed number of processors yields a quotient less than 0.05 μs. The number of processors shall be chosen by the seller to optimize cost, instruction execution speed, and general capability.

4.1.2 The Processor Network and its memories shall be modular and expansible wherever practicable.

4.1.3 All processors shall be capable of simultaneously processing identical instructions issued by a centralized Processor Control Unit.

4.1.4 Each processor shall possess arithmetic and logical capabilities and have its own Random Access Memory.

4.1.5 In addition to performing operations on operands in its own memory each processor shall have the capability of fetching operands from, or operating on operands fetched from the memory of its nearest orthogonal neighbors within the network; that is, a given processor operation shall be capable of being accomplished between an operand contained in an accumulator register of any base processor with an operand contained in the memory of any of its four nearest neighbors; North, South, East, West. The availability of operands from other neighbors is also desirable.

4.1.6 In addition to normal data communication paths between a processor and its neighbors, each processor shall have another neighbor which is common to all processors in the network. This neighbor shall be referred to as the Manifold Register. It may be loaded from the Program Memory and the contents sent to all processors.

4.1.7 The processors shall also be capable of selecting operands from the I/0 Buffer Memory.

4.1.8 It is desirable to make the nearest neighbor connectivity in such a way as to form the network into a vertical cylinder, a horizontal cylinder, a torus (combination of previous two connections), a helix, and no connections (plane).

4.1.9 Control shall be provided within each processor to give it the capability of not executing a given instruction. This control shall be referred to as "mode control". Each processor shall have a Mode Register and be capable of being in any one of several mode states. Each processor instruction shall specify the particular mode states in which action is required. Any combination of the several states shall be possible in the instruction, i.e. several bits are necessary to designate the states. A zero in a particular position of these bits commands all processors in the corresponding mode state to remain inactive during the execution of that instruction.

4.1.10 A second form of control over the activity of the processors shall be provided which is independent of the instruction being executed. This control shall be applied to the network on the basis of its spatial arrangement, and shall be controlled by bits in a register or registers which correspond to the spatial relationship. These shall be referred to as Space Activity Registers. A zero in any bit position of the register(s) shall make all processors in the corresponding space inactive.

4.1.11 A processor shall be active only when it is in the mode specified by the instruction and lies in an active space.

4.1.12 Both active and inactive processors shall supply operands to their neighbors. Only active processors shall compute results with the operands they receive. When results are stored in memory they shall be stored in the memory of the base processor only.

4.1.13 The processor network memory shall consist of at least eight million bits of Random Access Memory divided equally among the processors.

4.1.14 Transfer of data to and from the processor memories shall be routed through a memory called the I/O Buffer Memory.

4.1.15 Each processor in the network shall be capable of executing the type of instructions listed in Appendix A, which is a part of this specification. The seller shall propose those instructions which he feels will optimize capability commensurate with cost.

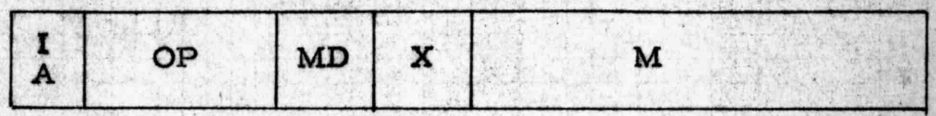
4.2 Network Program Memory

4.2.1 The Network Program Memory shall be a random access memory. The size of the memory shall be determined on the basis of instruction length, the power of the instructions, and compatibility with the size of the processor data word. In general the memory shall be capable of holding at least 16000 instructions of the type listed in Appendix B, and of the format shown in paragraph 4.3.2.

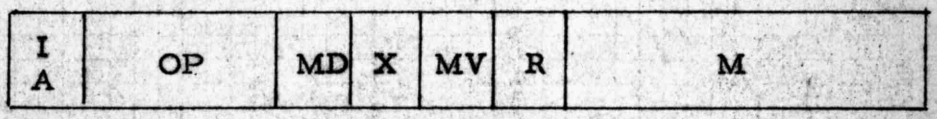
4.3 Processor Control Unit

4.3.1 The main function of the Processor Control Unit (PCU) shall be to provide the Processor Network with finalized instructions taken from the Network Program Memory, and control the sequence of these instructions.

4.3.2 The instruction formats for the PCU and processor instructions shall include the following fields:



PCU



PROCESSOR NETWORK

Where:

IA = Indirect Address Indicator
OP = Operation
MD = Mode
X = Index
MV = Mode Value
R = Routing (Internal, N, S, E, W, Manifold, I/O Buffer)
M = Memory Location

4.3.3 The Processor Control Unit shall obtain instruction words from the Network Program Memory and decode these for both the Processor Network and PCU. The operation field shall identify the instruction as a PCU or a processor type and specify the operation to be executed.

4.3.4 The PCU shall have the ability to initiate Input-Output commands as well as the ability to modify its instructions and operate on data for processor operation.

4.3.5 The instruction format for the PCU shall provide for the indication of operands which are direct addresses, immediate addresses, indexed addresses or indirect addresses.

4.3.6 The PCU shall contain at least seven Index Registers to allow modification of the memory field of the instruction word.

4.3.7 The PCU shall be capable of executing the type of instructions listed in Appendix B, which is a part of this specification. The seller shall propose those instructions which he feels will optimize capability commensurate with cost.

4.4 The Input-Output Section

4.4.1 Data channels shall be provided to transmit data between the Network Program Memory and the following devices:

4.4.1.1 I/O Buffer Memory.

4.4.1.2 Input-Output console typewriter.

4.4.1.3 Two IBM 729 MOD VI magnetic tape units, or equivalent.

4.4.1.4 An interface to the LRL computing facilities.

4.4.2 Space and terminal facilities shall be provided to allow for the addition of data channels at a future time which are compatible with conventional peripheral devices such as printer, card reader and punch, drum or disc file, etc.

5.0 CONSTRUCTION, POWER, AND UTILITIES

5.1 The electronic portions of this System shall be constructed of solid-state circuit components and mounted on printed-wiring modular plug-in units wherever practical. The circuit boards shall be flame retardant.

5.2 All equipment shall be so constructed and fabricated as to permit accessibility to any and all component parts for ease of maintenance and replacement -- without disconnecting any cables.

5.3 All construction and fabrication shall be of the highest quality according to electronic industry standards. The seller shall have an Engineering and Manufacturing Standards Manual acceptable to LRL. All construction and adjustment procedures shall adhere to these standards.

5.4 The System shall be completely assembled. LRL shall in no way provide any equipment such as -- but not limited to -- racks, cabinets, vacuum pumps, generators, power supplies, etc. Equipment shall be constructed so as to be compatible with LRL buildings and building services.

5.5 All interconnections shall be made by cables with LRL approved connectors at terminations.

5.6 All terminals, plugs, connectors, circuit wiring, etc., shall be uniquely labeled on the equipment and referenced to a set of system drawings.

5.7 Each subassembly of the System shall pass through a door opening which is 7' high by 5' wide. An estimate of the physical size and shape of the System shall be submitted with the proposal.

5.8 Adequate interlocks and safety devices shall be installed wherever necessary to ensure the safety of personnel and equipment. All such safety devices shall comply with published State of California Codes and LRL Electronics Engineering Safety Standard (LE 3088-14 attached).

5.9 The operating line voltage for the System shall be taken from commercially available power at LRL. This power is 117v/208v single phase or 208/440 v, 4-wire wye-connected three phase. The frequency is 60 cycles per second ±2 cycles. The system shall operate over an input voltage fluctuation of ±10% of normal. If a motor generator is used its primary power shall be as specified above.

5.10 The System shall operate as specified within a room temperature range of ±55°F to +100°F. Any internal cooling requirements shall be supplied by the seller.

5.11 Provisions shall be made to prevent improper distribution of air and improper cooling if one or more devices or modules are removed from the System for prolonged periods of time.

5.12 The noise generated by the equipment of this specification shall not increase the noise level more than one db above the average noise level in the three octave-bands of the speech interference range: 600-1200, 1200-2400 and 2400-4800 cps. The average level over these three bands, for the environment in which the equipment is to be placed, shall be taken at 60 db. (Reference: Handbook of Noise Measurement, General Radio Company.)

6.0 TESTS

6.1 A test to be negotiated at time of final contract shall be performed to demonstrate to members of the Lawrence Radiation Laboratory that the System meets the design features and operational characteristics stipulated in Section 4.0.

6.2 The test shall require approximately 8 hours per day for 3 consecutive days.

6.3 The test shall be performed and passed at the seller's plant before shipment may be made.

6.4 The test shall be performed again after installation at LRL. Passage of the test at LRL shall constitute preliminary acceptance of the System.

7.0 PERFORMANCE FOR ACCEPTANCE OF THE SYSTEM

7.1 The system shall be designed and constructed such that the total preventive and non-scheduled maintenance time does not exceed 4 hours for each 40 hours of time that the system is in operation. The system will be operated on a 24 hrs per day, 7 days per week basis.

7.2 Final acceptance of the system shall occur when the system has operated under the maximum allowable down time (10% per 40 hours) for a period of 4 consecutive weeks (28 calendar days).

8.0 SPECIAL REQUIREMENTS

8.1 The set of equations shown in Appendix C, which is a part of this specification, shall be hand coded using applicable Processing Element instructions. The listing shall be submitted with the seller's proposal as an accurate evaluation of the potential speed of the system.

8.2 The seller shall install the machine at LRL, Livermore.

8.3 The seller shall supply 25 copies of a preliminary programmer's manual and system description at least 90 days prior to the shipment of the system to LRL. The seller shall also supply 50 copies of a complete, accurate and adequate programmers' manual and system description at the time of the delivery of the system to LRL.

8.4 It is desirable that a certain amount of computer time, to be negotiated at the time of the final contract, be made available to LRL programmers prior to shipment of the system to Livermore.

8.5 The seller shall instruct LRL maintenance personnel, a maximum of six persons, in the logic, electronics and mechanics of the entire system.

8.6 The seller shall supply five complete sets of instruction manuals, adequate for operation and maintenance and servicing of the equipment. The seller shall also supply five complete sets of circuit schematics, logic drawings, and wiring diagrams for the entire system. In no case shall any drawing be larger than an LRL size 4 engineering drawing. One set shall be reproducable.

8.7 The seller shall supply a complete Recommended Spare Parts List.

8.8 The seller shall supply all spare parts prior to final acceptance.

8.9 As an alternative to paragraph 8.5 through 8.7; the seller may submit a proposal for a Maintenance Contract which includes spare parts.

8.10 To permit a fair and adequate evaluation of proposal received, sellers shall submit a list, correlated with the paragraphs of this specification, containing itemized descriptions and thorough explanations of the following:

8.10.1 All exceptions or alternatives to any paragraph of this specification.

8.10.2 Specifications exceeded and degree to which exceeded.

8.10.3 Specifications not met.

8.10.4 Additional features which are provided at no additional cost to LRL.

8.10.5 Sellers suggestion which would make the system more versatile or reliable.

APPENDIX A

Instruction List for Processors

The Processors shall be capable of executing a comprehensive complement of the following types of instructions.

1. **Transfers**

   (a) Transfers of operands from the processor accumulators, generally referred to as "A" to the processor memory.

   (b) Transfers of operands from the routing field, R, to A.

2. **Transfers with I/O Buffer**

   (a) Transfer of operands in the I/O buffer to the network memory under spatial control.

   (b) Transfer of operands in the network memory to the I/O buffer under spatial control.

3. **Addition and Subtraction**

   (a) Floating point and/or fixed point addition or subtraction of an operand in the accumulator, requestor, A, to or from an operand designated by R.

   (b) The absolute value of A may be used.

   (c) Results go to A.

   (d) Provision shall be made to handle overflow.

4. **Multiplication**

   (a) Floating point and/or fixed point multiplication of the operand in A by the operand designated by R.

   (b) Provision shall be made to handle overflow.

5. **Division**

   (a) Floating point and/or fixed point division of the operand in A by the operand designated by R.

   (b) Provision shall be made to handle overflow.

6. **Sign Operations**

   (a) The sign of the operand in A may be set positive, negative or opposite.

7. Shifts

(a) A shift of the operand in A may be made to the left, right; signed or unsigned.

(b) The operand in A may be shifted circularly.

8. Boolean Operations

(a) With the operand in A as the first operand a Boolean AND, OR, or Exclusive OR is performed. The operand designated by the routing field is the second operand.

(b) The operation NOT may be performed on an operand in A or R.

9. Mode Set

(a) The Mode Register may be set to the value of the Mode Value portion of the instruction.

(b) The set may be unconditional.

(c) The set may be conditional on the result of a comparison of an operand in A and an aperand designated by R. The test may be for equality, inequality, greater than, less than, greater than or equal, less than or equal, A equal to zero or A equal to one.

10. Miscellaneous Sets

(a) The Mode Register may be set from a pair of bits in A.

(b) The Mode Register contents may be transfered to a pair of bits in A.

(c) The Spatial Control Registers may be set from processor conditions.

APPENDIX B

Instruction List for Processor Control Unit

The Processor Control Unit shall be capable of executing a comprehensive complement of the following types of instructions.

1. **Transfers**

   (a) **Transfers of operands from the Program Memory to the various registers of the PCU, including such registers as the Manifold Register, Space Activity Registers, Mode Register and Index Registers.**

   (b) **Transfers of operands between the various registers and accumulator.**

   (c) **Transfers of operands between the Program Memory and the I/O Buffer Memory.**

2. **Addition and Subtraction**

   (a) **Floating point and/or fixed point addition or subtraction of an operand designated by the M field of an instruction or the actual contents of the M field (immediate operand) to or from the contents of an index register, with overflow detection.**

   (b) **Floating point and/or fixed point addition or subtraction of an operand (memory or immediate) to or from the value in the accumulator, with overflow detection.**

3. **Shifts**

   (a) **A shift of the operand in the accumulator to the left, right, circularly; signed or unsigned.**

4. **Boolean Operations**

   (a) **The following Boolean operations are desirable: And, Negated Co-implication, Negated Implication, Exclusive OR, Negated Or, Equivalence, Implication, Co-implication, Negated And, and Not.**

5. **Jumps**

   (A jump causes a new sequencer of instructions to be established.)

   (a) **Jumps which modify index registers.**

   (b) **Jumps which test index registers.**

   (c) **Jumps which test the accumulators.**

   (d) **Jumps on overflow.**

   (e) **Jumps on certain indicators having to do with manual switches and network states of activity.**

6. Indicator Sets

(a) Sets indicator on Index Comparison.

(b) Sets indicator on Boolean Comparisons.

7. Miscellaneous

(a) Halt.

(b) No operation.

(c) Input-Output initiation.

(d) External Signal sensing and emitting.

APPENDIX C

Equations To Be Hand Coded

Consider the memory of each of the processors to contain a number of sequences of the variables designated by the following letters: P, Q, R, Z, M, U, V. The problem is to calculate new variables R', Z', U', V' from the equations shown below and store them in place of the old variables R, Z, U, V.

Calculation of the new variables shall be coded in two distinct ways: (1) All variables considered as double precision words, and, (2) All variables as single precision words. The instructions which are necessary and sufficient to calculate the results shall be written in the form of a mnemonic assembly language with annotations concerning the mnemonics. A timing diagram or list shall accompany the coding showing the proposed speed of each instruction in the sequence and a total time shall be given for each of the two variations requested.

$$A = [P(NE) + Q(NE) - P(N) - Q(N)]\,[R + R(N)]/[M(N) + M(NE)]$$

$$B = [P(N) + Q(N) - P - Q]\,[R + R(W)]/[M + M(N)]$$

$$U' = U + s\,\{-A(N)\,[Z - Z(N)] + A[Z - Z(S)] - B[Z - Z(W)] + B(E)[Z - Z(E)]\}$$

$$V' = V + s\,\{-A(N)\,[R - R(N)] + A[R - R(S)] - B[R - R(W)] + B(E)[R - R(E)]\}$$

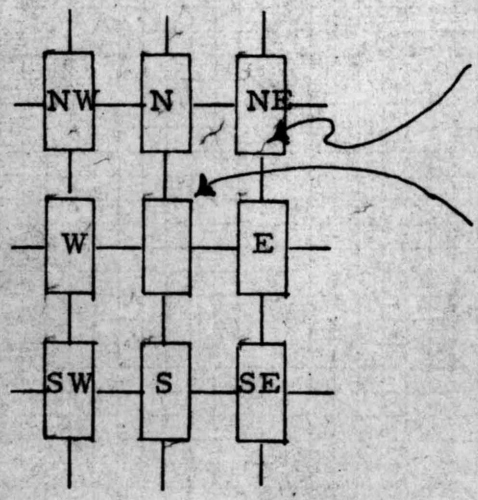
$$R' = R + t \cdot U' \quad \text{(s and t are given constants which are the same for all processors.)}$$

$$Z' = Z + t \cdot V'$$

All variables shall be considered as indexed quantities within each processor memory.

Square and curly brackets are used to designate arithmetic expressions.

All quantities in parenthesis refer to the neighbor relationship shown in the following diagram:



For example: P(NE) refers to the variable P located in the memory of the Northeast neighbor of the base processor.

BASE Processor (variables with no parenthetic expression reside here).

Ignore boundary connectivity.

Note: This diagram is not intended to convey any fixed organizational arrangement.