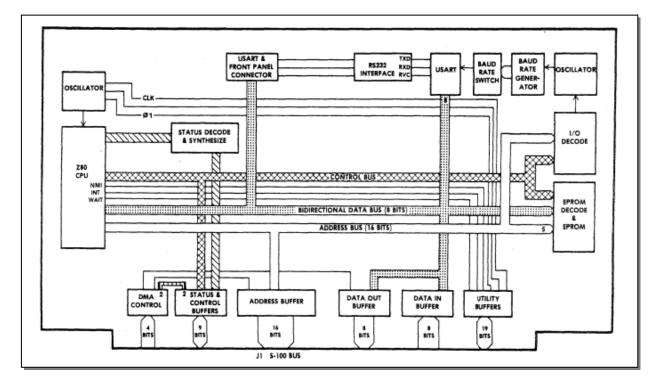
Jade Computer Products

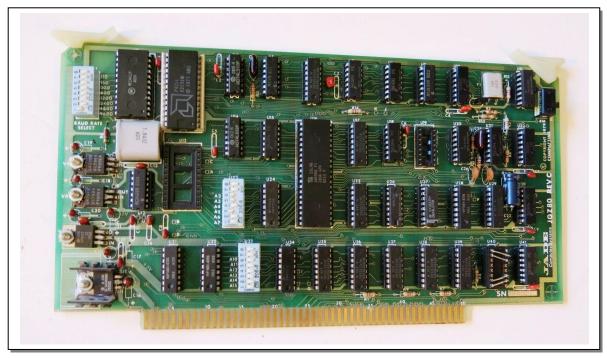
The Big Z Revision C

The Jade Big Z CPU board is a Z80 Main processor card for the S-100 computer bus system developed around 1980. The board was developed before the IEEE-696 standards were put into effect so there are a few complications when using this card with more modern S-100 systems.

The card was known as "The Big Z" or the "JGZ80" board and had revisions A through C with the C version being the final version produced. The board offers the following features...

- Zilog Z-80 CPU
- EPROM onboard accessed on 1K, 2K or 4K boundaries (2708, 27C16 or 27C32)
- POJ power on jump to EPROM at boot
- one M1 wait state
- 8251 USART onboard for RS-232 communication to another Host or Terminal/Console
- CPU speed selectable between 2Mhz and 4Mhz
- Front Panel DIP connector to enable using a front panel (IMSAI)
- Fully buffered S-100 address and data lines
- Voltage regulators for all onboard voltages





The Jade Big-Z revision "C"

The Jade board was engineered before the IEEE specifications were finalized and therefore some incompatibilities exist.

- sXTRQ* Pin#58 is not implemented on the Big Z (16 bit wide I/O request)
- pSTVAL*- Pin#25 is not implemented (signals when address and status lines are valid)
- SIXTN* Pin#60 is not implemented (this is an acknowledgement to the sXTRQ* signal)
- RFSH* Pin#66 is implemented by the Big Z on undefined S-100 pin#66 (Memory Refresh)
- MRQ Pin#65 is implemented by the Big Z on undefined S-100 pin#65 (Memory Request)
- pWAIT- Pin#27 is implemented by the Big Z on undefined S-100 pin#27 (Wait signal)
- DMA0* Pin#55 is not implemented (temporary bus master signal)
- DMA1* Pin#56 is not implemented (temporary bus master signal)
- DMA2* Pin#57 is not implemented (temporary bus master signal)
- DMA3* Pin#14 is not implemented (temporary bus master signal)
- GND Pin#20 is not implemented
- GND Pin#53 is not implemented
- GND Pin#70 is not implemented
- CLOCK1 or PHI 1 Pin#25 is implemented and in violation of IEEE standards The Pin#9 on U29 has been bent out to disconnect this line from the S-100 Bus S-100 Pin#25 should be pSTVAL* and is not implemented, could cause problems.

NOTE: If the "S100Computers.com" System Monitor Board V2 or later is used, U29 should remain intact. The SMB requires pSTVAL* to operate but an inverted PHI 1 on S-100 Bus Pin#25 will enable the SMB Address Display to function (pSTVAL* hack for slower boards).

• SSWDSB*- Pin#53 is implemented and in **violation of IEEE standards** (Sense switch disable) The S-100 bus Pin#53 is a GND line. On the Jade Big Z, the S-100 bus pin#53 has been cut at pull-up resistor pack U31 pin#8.

It has been noted that the Jade Big Z does not work with all memory cards. Most reliable operation of the Jade Big Z will be accomplished using Static RAM memory cards with 8 Data lines and 16 Address lines. Dynamic RAM boards work, but may require rebooting a few times before stable (ie...Jade Memory Bank). So, memory boards that have been used and verified working with the Jade Big Z are the "S100Computers.com" 4MB memory card, Jade Memory Bank, Static Memory Systems "The Last Memory Board" and the Compupro RAM-20. There should be many more boards that work but these are the ones available for testing. The Jade can access 64K of RAM but has no provision for memory paging or extended addressing (A16-A23).

EPROM INTERFACE:



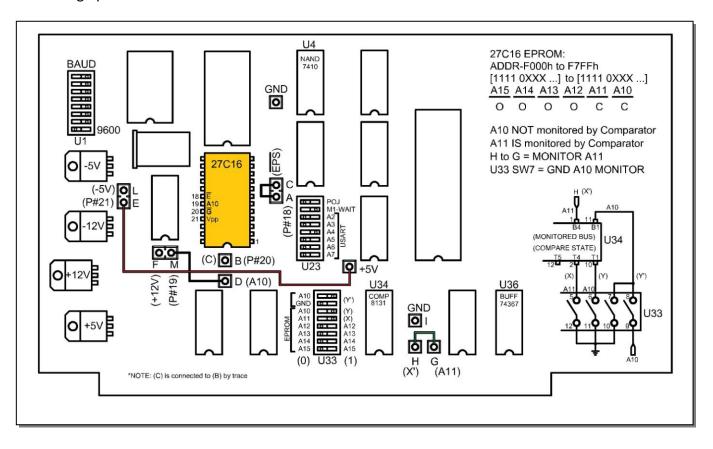
- Use only single voltage EPROM or EEPROM
- Voltage +5V DC
- Cut trace L to E on Big Z to isolate (-5V) Note: **Remove C12** as it interferes with A11
- Cut trace F to M on Big Z to isolate (+12V)
- Cut trace G to H on Big Z to isolate (A11)

The Jade Big Z will accommodate three types of EPROM's (2708, 27C16 or 27C32). The board is originally configured for the 2708 EPROM but due to it's small 1K size and limited supply, it was never used. There are jumpers on the board to configure the card for the other two EPROM types. In fact, there are just two wires to connect for Pin#21 on the EPROMS (either Vpp or A11). All other connections remain the same for the 27C16 and the 27C32. EEPROMS such as the Atmel AT28C16 can also be used in place of a 27C16 EEPROM. There is no counterpart for the 27C32 though.

The EPROM is first accessed at power on (if the POJ option is enabled) by starting at address 0000H and moving upward in address space until the address space set for the EPROM is reached. When this happens, the EPS* signal becomes active low, and the EPROM is enabled.

Code in the EPROM is then read and acted upon by the Z80 CPU. Typically this is where the Monitor Program for the Jade Board would reside in EPROM at a high address range such as E800H, F000H or F800H (more on this later).

The DIP Switch U33 is used to select the address for the EPROM. The Big Z is capable of utilizing "Shadow EPROM" mode that will enable the EPROM on boot-up, but thereafter will not be seen by the system. This might be useful for a boot to Disk System (refer to the users manual for details).



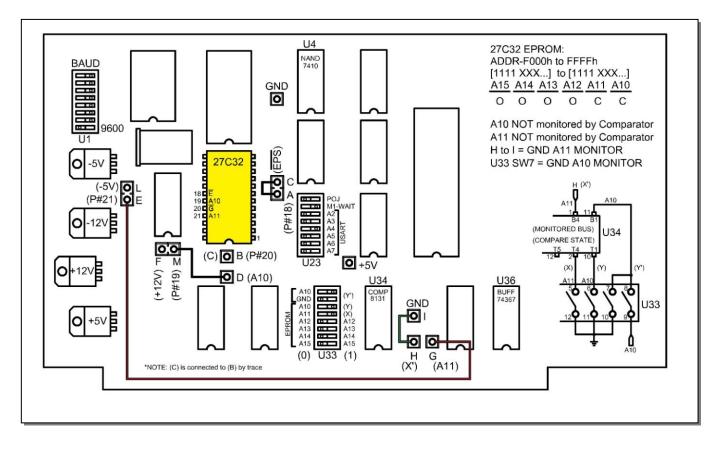
Wiring up a 27C16 EPROM is as follows...

Wiring the 27C16 only requires running a wire-wrap wire from Point (E) to Point (+5V), this routes +5V to Pin#21 on the EPROM which is Vpp that needs to be High to operate. Then run a wire-wrap wire from Point (H) to Point (G) thereby routing the A11 comparator bus sense input to A11. That's it as all other wires are already attached.

- Wire (E) to (+5V)
- Wire (H) to (G)
- Wire (C) to (A)

The DIP Switch address for the EPROM has to be set using the U33 DIP Switch. See the section below on how to do this.

Wiring up a 27C32 EPROM is as follows...



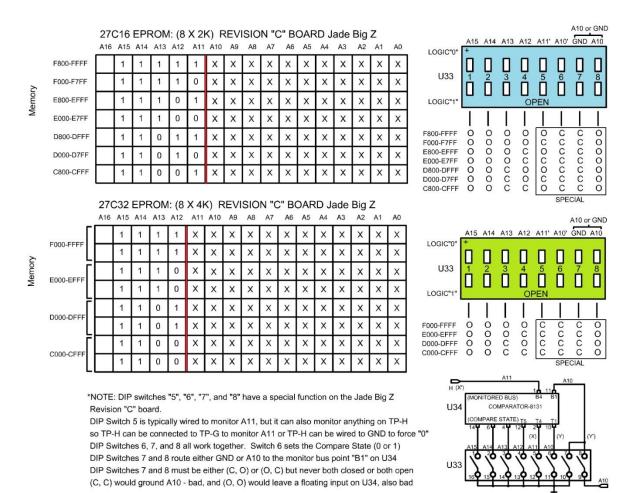
Wiring the 27C32 only requires running a wire-wrap wire from Point (E) to Point (G), this routes address line A11 to Pin#21 on the EPROM which is A11. Then run a wire-wrap wire from Point (H) to Point (I) thereby grounding the A11 comparator bus sense input. That's it as all other wires are already attached.

- Wire (E) to (G)
- Wire (H) to (I)
- Wire (C) to (A)

The DIP Switch address for the EPROM has to be set using the U33 DIP Switch. See the section below on how to do this.

EPROM ADDRESS SELECTION:

The EPROM address is selected by using U33 to enter the required address to activate the EPS* signal for the EPROM enable. The chart below illustrates some possible locations in High Memory for the EPROM to reside (27C16 or 27C32). Since the 27C16 is a 2Kx8 device there are smaller memory blocks allocated to it. The larger 27C32 is a 4Kx8 device and therefore fewer choices. The bits to the left of the red line are bits that identify memory blocks. These can be entered into the DIP switch by using an "open switch" as a logic 1 and a "closed switch" as a logic 0. A11 is special and A10 is not used unless a lower memory address is used. By "special", this means the Jade Big Z has added a complicated way to represent these two bits. This is to allow more versatility for address selection to the board.



Note the drawing on the lower right of the DM8131 comparator and DIP Switch. For a 27C32 the A11 line is routed to the EPROM via point (G) and the S5 switch is simply set O or C as shown in the charts. A10 on the other-hand is hard-wired to the DM8131 and it's selection is accomplished by using three switches S6, S7 and S8.

The A10 logic state is selected by DIP S6 and will select the logic level to be compared as described above. S7 and S8 will route either A11 or GND (logic 0) to the bus comparator circuit side of the DM8131. S7 is the GND signal line and S8 is the A10 signal line. Either of these signals can be routed to the DM8131 but not both. Refer to the diagram above to clarify.

In the example chart shown above, the 27C32 does not use the A11 or A10 to enable the EPROM.

- Point (H) is tied to (GND) physically on the board with wire-wrap thereby setting the bus comparator sense input to "0" taking it out of the picture (not used).
- A11 DIP S5 is closed or "0" thereby making it match the unchanging bus comparator input and taking it out of the picture (not used).
- DIP S7 is closed "0" and DIP S8 is open not allowing A10 to reach the comparator input and taking it out of the picture (not used)
- A10 DIP S6 is closed or "0" thereby making it match the unchanging bus comparator input and taking it out of the picture (not used).

The same process is used for the 27C16 except A11 is used and only A10 has to be adjusted using DIP S6, S7 and S8 to get it out of the picture.

- DIP S7 is closed "0" and DIP S8 is open not allowing A10 to reach the comparator input and taking it out of the picture (not used)
- A10 DIP S6 is closed or "0" thereby making it match the unchanging bus comparator input and taking it out of the picture (not used).

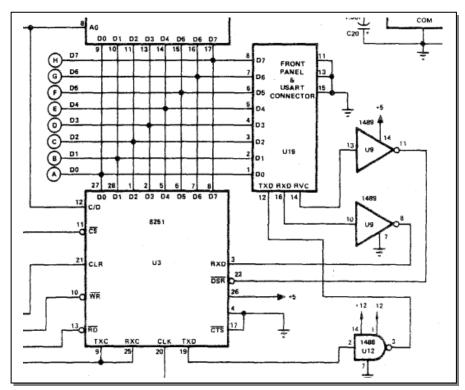
This is how the address is set for the EPROM. There are charts in the Jade Big Z manual that just give the "O" or "C" positions of the U33 DIP switch, but there are errors in the chart depending upon which revision of the board is being used. The above information describes how the DIP switch is set for any address and applies to the revision "C" version of the board.

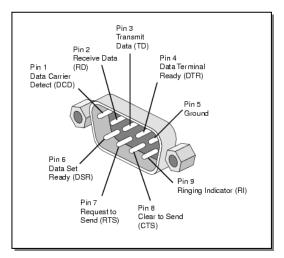
Remember that capacitor C12 is installed for filtering the surge current when using the -5 volt supply on a 2708 EPROM. This capacitor appears to attenuate or distort the A11 signal to a 2732 EPROM making the EPROM incapable of being accessed. This may be due to bad capacitors used on the Jade Board as some of the .1mfd monolithic capacitors have been found to be shorted out. In any case, if not using the 2708 EPROM it is a good idea to remove the C12 capacitor located directly below the 1.8432 MHz crystal.

8251 USART:

The Jade Big Z has an onboard 8251 USART to be primarily used as a console input/output allowing the Jade to communicate to the outside world. The USART could also be used as an RS-232 serial port but there are better dedicated cards that perform this function so this limits the USART to console I/O.

The connector for the USART is the DIP socket U19 on the Jade board. One side of this socket is used for the RS-232 communication and the other side can be used for a front panel connection. **NOTE PIN#1 LOCATION ON U19! DON'T INSERT PLUG BACKWARDS!**





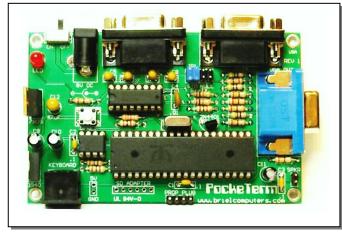
A DB-9 (RS-232) cable can be constructed by wiring the following pins...

- TXD (Pin12) to RD (Pin2)
- RXD (Pin16) to TD (Pin3)
- GND (Pin15) to Ground (Pin5)

That's it, no handshaking required

There is a "Reverse Channel" signal line provided by the Big Z on Pin#14 of U19. RVC can be used as a "Busy" or "Data Not Ready" signal from the Host Equipment to the Jade Big Z USART. This would be accomplished by wiring U19 Pin#14 (RVC) to Pin#6 (DSR).

In practice, for console I/O, this signal was not needed as the Big Z controlled all communication and would be fast enough to loop waiting for a keyboard input from the USART and then sending output back at such a slow data rate (9600 baud) that both Host and Jade had no problem keeping up. The other end of the cable should be connected to a RS-232 (VT-100) capable terminal (+/- 12VDC). A PC running emulation software. A laptop or any other terminal device can be used. One option is to use the Propeller driven "Pocket Term" by Briel Computing.

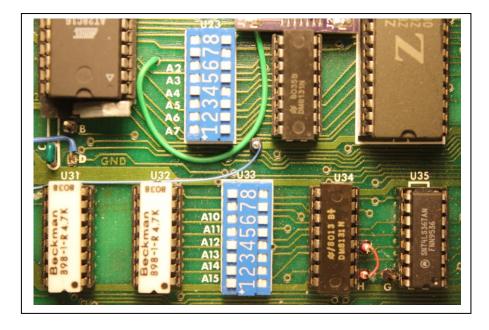


A VGA Monitor is connected to the "blue" connector in the picture above. The Big Z RS-232 cable is connected to the "HOST" connector (one of two on back) and an IBM keyboard is connected to the PS/2 connector on the front of the board. The (2) jumpers in the middle may have to be switched (they act as gender changers). When working, the following is displayed...

CSCCSRUE CROCLORD CUOCUER CUOUSER CXOCSYNC (YOCRDJ CBOTARB CEOUERSA # M 00000 R R R R R R R R R R R R R R R 1000 R R R R R R R R R R R R R R R	CKOMEN
9899 R R R R R R R R R R R R R R R R	
(R)HHOB (B)HDUMP (G)RUN (P)PORT (G)HHOUE (T)MTEST (F)MFILL (M)HHAP ((S)CSRUE (R)CLOND (U)CUER (U)USER (X)CBYNC (V)CRDJ (B)TARB (E)UERSA (J U	SOMWRT Comenu
Baud Rate: 9608 Color PC Port: OFF Force 7 bit: NO Cursor CR V/L	F: YES

Address for the 8251 USART:

The USART is accessed as one of 255 Ports available to the Z80 CPU. The address of the USART Port is set by using DIP Switch U23 (S1-S6). The USART appears to the Z80 as two consecutive port I/O address. U24 on the Big Z decodes a group of four consecutive addresses and the two lower addresses are used for USART communication. An "ODD" address will select the "Status Port" and an "EVEN" address will select the "Data Port".



U23 is used to set the Port Address for the USART. In this example, the USART has been assigned Port 10H and Port 11H as Data Port and Status Port.

10H = [0001 0000]B 11H = [0001 0001]B

<u>A7</u>	A6	A5	A4	A3	A2	
0	0			0	0	
		OF	२			
۸7	٨٥	Λ5	Λ.Λ	٨2	Δ2	

<u>A7</u>	A6	A5	A4	A3	<u>A2</u>
С	С	С	0	С	С

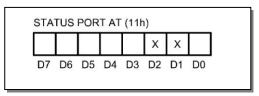
So this is what is entered into the U23 DIP Switch (S1-S6).

As to the 8251 USART itself, different commands can be entered to the USART and different status bits can be used to indicate conditions within the USART itself such as "BUSY", "READY TO SEND" ect...

DATA PORT & STATUS PORT:

As mention above, the two Ports chosen for the USART communication are described as Data Port and Status Port. These are 8-bit words used to transmit data to and from the Big Z.

Х	X	X	X	X	X	X	X
7	D6	DE	D4	<u></u>	D2	D1	



In it's most simple form, the Status Port provides hand shaking control while the Data Port actually transmits and receives the 8-bit data word. A code snippet to do this is shown below...

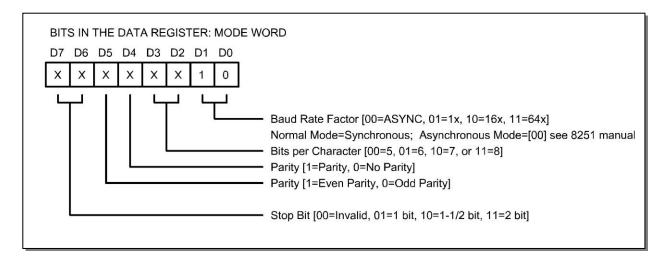
INPUT: IN	A,(11H)	;Read keyboard status [0000 00X0]	
AND	02H	; 02H = [0000 00X0] evaluate the "X"	
JP	Z,INPUT	;Loop if not ready, [0000 0010]=RDY [0000 0000]=NOT RDY	
IN	A,(10H)	;Get keyboard data	

OUTPUT:	IN	A,(11H)	;Read keyboard status [0000 0X00]
	AND	04H	; 04H = [0000 0X00] evaluate the "X"
	JP	Z,OUTPUT	;Loop if busy, [0000 0000]=BUSY [0000 0100]=NOT BUSY
	LD	A,C	
	OUT	A,(10H)	;Output character to console

This is how data gets into and out of the Jade Big Z; but before this can happen, the 8251 USART must be initialized via software. This is quite complex but offers great versatility without hard wiring the USART.

PROGRAMMING THE 8251 USART:

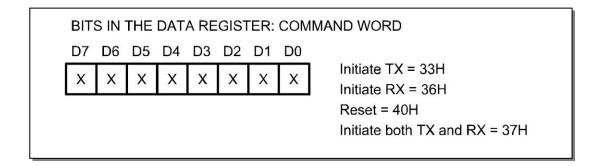
Before the 8251 USART can be used for anything, it must be initialized with word length, stop bits, parity and parity type. This is done by sending a "**MODE WORD**" to the 8251 prior to communicating with it. A MODE WORD is described as follows...



So, to initialize the 8251 USART for **8 data bits, no parity, odd parity, and 1 stop bit**, the following "MODE WORD" would be sent to the 8251 USART...

[0100 1110]B or [4E]H is the MODE WORD sent to the USART

After writing the Mode Word to the 8251, there should be a slight delay and then the "**COMMAND WORD**" would be sent. The delay is accomplished by using a "LD A" instruction followed by the Command Word. The Command Word is sent to control the transmit or receive function of the USART.



The Mode and Command Word are sent only once after a power-on sequence or reset is performed.

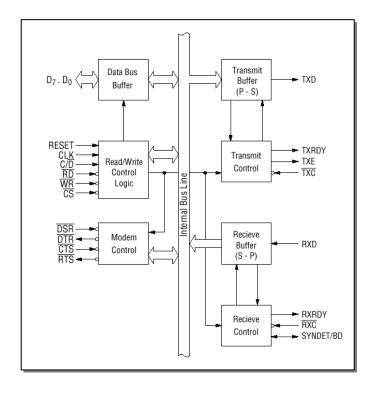
The **Status Register** of the USART is used to determine operating conditions within the 8251 USART as follows...

D7	D6	D5	D4	D3	D2	D1	D0	
Х		Х	Х	х	х	х	х	
Ĩ		Ĭ.	1			L	L	 Transmitter Buffer [1=RDY] buffer is empty & ready for more Receive Buffer [1=RDY] data is available
					L			 Transmitter Mode [1=BUSY] USART is transmitting
								 Parity Error [1=ERROR] error in Rx or Tx data parity
			_					 Overrun Error [1=ERROR] received data overrun error detected
								 Framing Error [1= ERROR] transmitted data has wrong stop bit, length or bau
L								 Reverse Channel [1= BUSY] DSR on the RS-232 connector

If the 8251 USART is used solely for console I/O, the main Status Register bits to be concerned with are D1 and D2.

INPUT PORT [00]H = 02H then **DATA RDY** from keyboard; if the Port is = 00H then **DATA NOT RDY OUTPUT PORT [00]H = 04H** then the **HOST NOT BUSY**; if the Port = 00H then **HOST BUSY**.

The other Status Register bits are useful if more advanced RS-232 data operations are being used.



Block Diagram of the

8251 USART

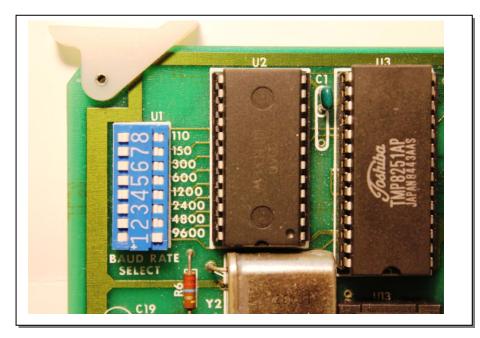
The following code snippet will initialize and set up the 8251 USART for operation...

(Note Foxit PDF reader ver 4.3.0.110 can convert this listing into ASCII text for use in a Z80 compiler)

		******	*****************************
			Asynchronous Communication Mode
			Reset
			Mode Instruction (Asych or Synch, Baud Rate, Word Length, Stop Bits, Parity)
			Mode Word (Write): D7+D6=Stop Bits,D5=E/O Parity,D4=Parity Enable,D3+D2=Char Length,D1+D0=Baud
			*Note: a different Mode Word for Asynchronous Communication is used
			Command Instruction (DTR, RTS, Hunt Mode, Xmt Enable, Rxv Enable)
			Cmd Word (Write): D7=Hunt,D6=Int Rst,D5=RTS,D4=Err Rst,D3=Snd Brk,D3=Rx Enable,D1=DTR,D0=Tx Enable
			Status Word (Read): D7=DSR,D6=Syn Det,D5=Frame Err,D4=Overrun Err,D3=Parity Err,D2=Tx Empty,D1=Rx Rdy,D0=Tx Rd
	ORG	0E000H	
ТАТ	EQU	11H	;8251 Status port
ATA	EQU	10H	;8251 Data port
RDY	EQU	01H	;TRANSMIT READY = (0000 0001) or (01)H
			initialize USART send 00H three times to guarantee device in "Command Word" mode
IT:	LD	A,00H	;initialize USART
	OUT	(SSTAT),A	
	LD	A,00H	;initialize USART
	OUT	(SSTAT),A	
	LD	A,00H	;initialize USART
	OUT	(SSTAT),A	
	LD	A,40H	;Send reset "Command Word " (0100 0000) or 40H and ready 8251 to receive a "Mode Word"
	OUT	(SSTAT),A	
			Mode word:(01)-1 stop bits (00)-parity disabled (11)-char length 8 bit (10)-baud 16X
			Mode word: (01001110) or (4E)Hex1xBaud = 153,600 1/16xBaud = 9,600 1/64xBaud = 2,400
	LD	A,4EH	;Mode register 8,1,n,9600 or 4EH
	OUT	(SSTAT),A	
			Command word:(0)-disable hunt mode (0)-do not return to mode word (1)-reset output 0
			Command word: (1)-reset all error flags (0)-normal operations (1)-receive enable
			Command word:(1)-DTR will output "0" (1)-transmit enable
			Command word: (0011 0111)Binary or (37)Hex
	LD	A,37H	Command register 37H essentially enables both transmit & recieve modes
	OUT	(SSTAT),A	
ST:	IN	A,(SSTAT)	
	AND	TXRDY	;is transmitter buffer ready (0&0=0,0&1=0,1&0=0,1&1=1)if SSTAT=1 AND TXRDY=1 the loop exits
	JP	Z,TEST	;loop until it's empty
			Output to say we reached this point "U"
	LD	A,56H	
	OUT	(SDATA),A	
	JP	TEST	
	END		

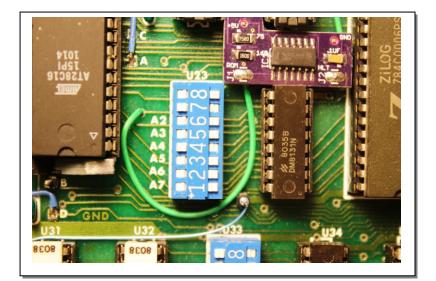
8251 USART BAUD RATE:

The Baud Rate for the 8251 is selected by using DIP Switch U1. The Baud Rates are clearly labeled on the circuit board. Rates go from 110 baud to 9600 baud. Only one switch on U1 can be closed at a time or the baud rate generator will not function.



REVISITING U23 DIP SWITCH:

The remaining two switches (S7 & S8) are option switches controlling the M1 Wait State and the (POJ) Power-On Jump to EPROM functions.

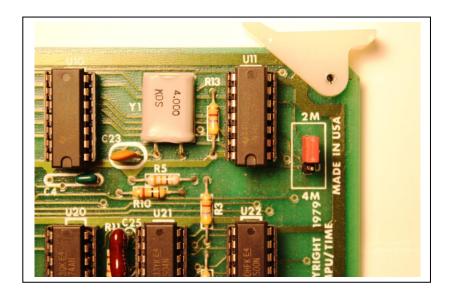


DIP Switch U23

- S7- OPEN=Wait Off
- S7- CLOSE=M1 Wait On Jumper **R** to **F**
- S8- OPEN=POJ Off
- S8-CLOSE=POJ On

BIG Z SPEED OPTION:

The Big Z CPU can operate at 2MHz or 4MHz depending upon the position of the T, V, U jumper.



Operation at 4MHz has been successful with the Jade DD Controller Card and a static RAM board but this depends on many factors and is not easy to get working. The other problem with the 4MHz operation may be due to the 8251 not being a 4MHz part. Substitution of a faster USART may resolve the issue or a USART wait state could be implemented as described in the Big Z Manual and Engineering Update #104.

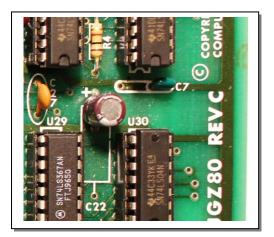
ENGINEERING UPDATES:

Engineering updates or "ECN" are listed in the back of the revision C Big Z user's manual. Most of the ECN's deal with errors in the User's Manual due to board revisions, EPROM tables, EPROM connections and errors in the program listings included within the User's Manual. In particular, the Jade Monitor listing in the manual does not work.

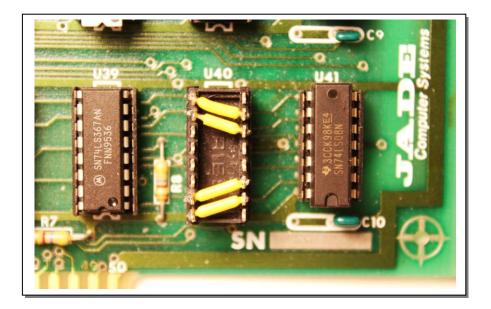
Two of the ECN's have been performed on the Jade Big Z revision C board...

- Erratic Reset ECN#101
- Status Delay Signal ECN#102

Erratic Reset Operation is caused by excessive time constant on RC network on input to U21 Pin#1. This time constant was chosen for operation with front panel systems and resulted in a delay of 470 ms after the Reset was activated. This may be too long of a delay for non-front panel systems. Capacitor C22, a 100mfd capacitor was removed and a smaller 10mfd capacitor was installed in it's place. This may have to be fine-tuned up to around 22mfd before acceptable operation is observed.

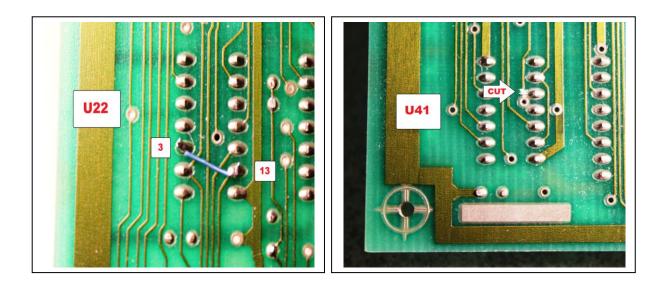


The **Status Signals** from a front panel display are latched by U40 to provide for a stable display operation of the front panel. Unfortunately, passing the status signals through U40 slows them down enough to become non-compliant with some dynamic memory boards operating at 4MHz. To correct this, U40 is removed and a jumper DIP is installed in it's place. This removes the pSYNC delay introduced by the original circuit.



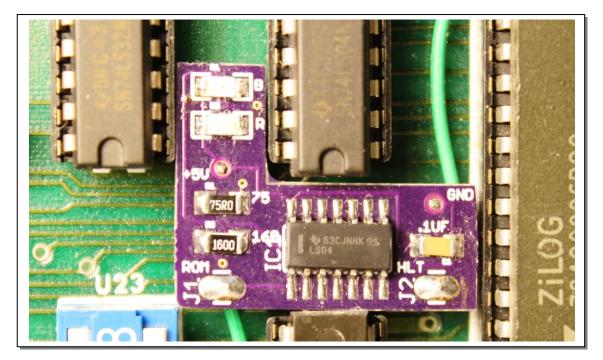
OTHER MODIFICATIONS:

If the Jade Double D Disk Controller board is used in the system, one of the Engineering Notice Bulletins #4 was for erratic operation between the Jade Big Z and the Jade DD (from the Jade DD manual) was to modify U22. Cut the trace going to pin#13 of U22 and jump pin#13 to pin#3. If the Jade DD is not used this modification is not needed.



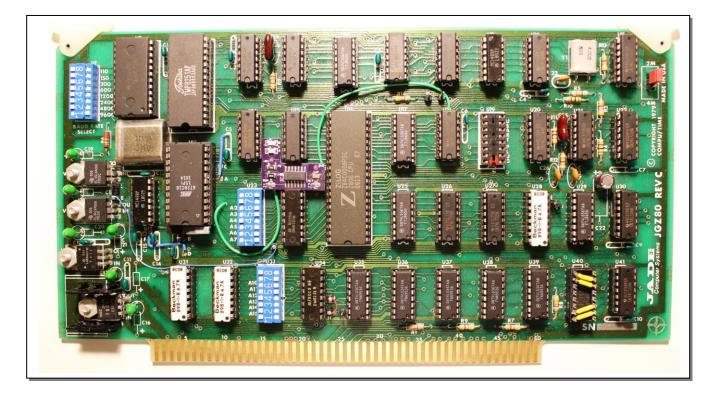
EPS & HALT:

One other modification done to the Big Z CPU board was the addition of two signal LED's to indicate when the EPROM address space is being accessed, and an LED to indicate when a software HALT instruction has been accessed by the CPU. These indicators are useful in determining if the EPROM is set up correctly and if the Big Z board is working by installing an EPROM filled with HALT instructions (76H) that will cause the processor to HALT and turn on the LED indicator.

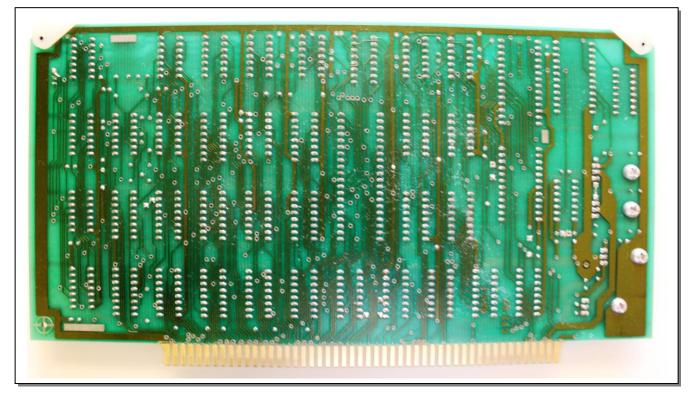


- BLUE LED: ON=EPROM being accessed EPS (within the U33 DIP switch address range)
- RED LED: ON=HALT instruction has been read by the CPU and stopped

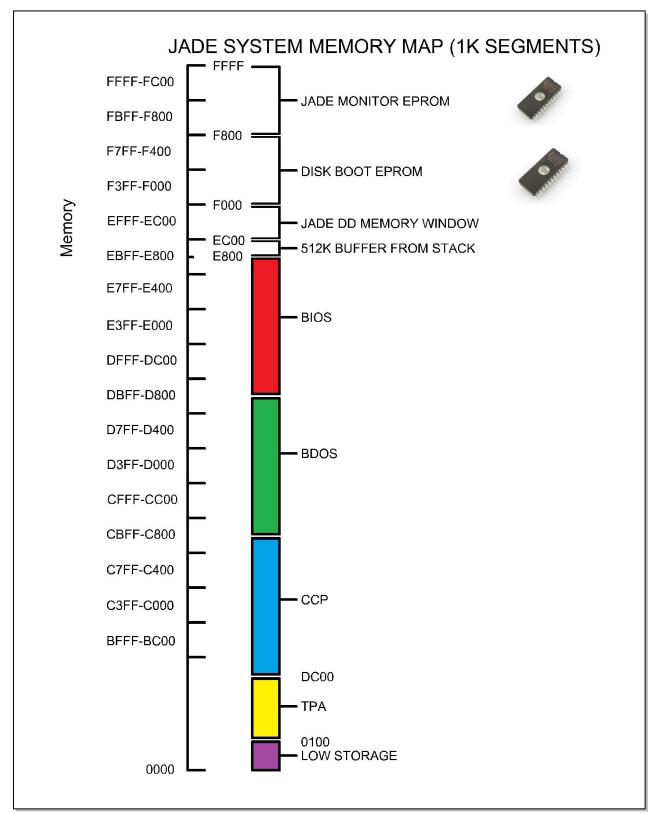
Jade Big Z Front:



Jade Big Z Back:



Jade Memory Map for Disk Based System:

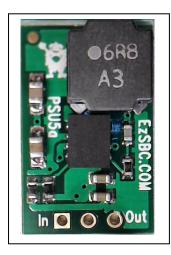


Troubleshooting and Observations:

Hot +5V Regulator Heatsink: The +5V Regulator at VR4 gets rather hot during normal operation. Other (larger heatsinks) have been tried but still, this regulator runs hot. I believe this is normal operation for this board and should not cause problems but it is undesirable. For this reason, a new switching regulator was installed that does not heat up at all. This regulator is manufactured by (EzSBC.COM) and is rated at +5V @ 3 Amps.

This is a 5V 2.5A switch-mode voltage regulator. It is a high-efficiency replacement for popular three-terminal LM323T linear regulators and it is pin-to-pin compatible with the common and now obsolete LM323T linear regulators. The mechanical design allows the PSU5a to fit anywhere where an LM323T or an LM7805 was used. The maximum continuous output current is 3A and at room temperature the PSU5a does not need a heatsink to maintain this current indefinitely. All the required capacitors are included on the module, no external capacitors are required and additional input capacitors do no harm. The output voltage guaranteed to be within +/-1% as the load varies. The original LM323T had a rather loosely specified output voltage and it could vary by as much as 250mV without load and at room temperature. The PSU5a is accurate to winthin +/-2%. The module has thermal shutdown and current limit protection. The absolute maximum input voltage is 20V.

- Drop-in replacement of the obsolete LM323T or equivalent linear voltage regulator.
- Guaranteed 3A output current.
- Input voltage range of 7.2V to 20V
- Suitable for use in Pinball machines and video game consoles
- High efficiency switching regulator design reduces power dissipation with superior voltage regulation compare to the LM323T.
- Thermal shutdown and current limit protection
- All components are mounted on one side of the PCB
- Highest component is the inductor at 5mm above the PCB.
- Available with or without pins.
- Gold plated pins and PCB to withstand harsh environments over the long term.
- Can drive inductive loads such as solenoids and DC motors.
- 500kHz Switching Frequency
- Made in the USA



PSU5a 5V 3A Regulator in TO-220 form Factor

As a side note, the previous +5V regulator was changed out with another regulator with a higher Amp rating prior to trying the EzSBC switching regulator. This regulator worked but provided an output of 4.98 volts. This caused strange behavior in the Big Z CPU board. Random crashes, random HALT's and weird operation of the front panel displays (flickering of status LED's). I can't state emphatically that the lower 4.98 volts caused this problem, but after replacing the regulator with the EzSBC switching regulator, along with the two filter capacitors C16 & C17, all problems stopped occurring. The EzSBC output voltage was 5.01 volts. Food for thought...in the future, check the voltage output of the VR4 regulator to insure it is operating at +5.00 volts.

8251 USART Port: Problems with the serial port can be hard to diagnose. The RS-232 connection from the Terminal Equipment to the Jade Big Z is through the 16-Pin DIP socket on the board U19. If the connector plug is installed backwards, +/- 12 volts is applied to the CPU data bus directly and can cause damage. Make sure the plug inserted into U19 is correctly oriented with Pin #1 closest to the Gold Fingers on the bottom of the card. Verify Pin #1! If the serial port becomes unresponsive, replace the MC1488 and MC1489 chips first as they are the interface between the RS-232 and TTL logic. If the computer is turned off, the Big Z plugged in with serial connection on, and there is a small voltage bleeding through on the +12V or -12V system rails; this may indicate failure of the 1488 and/or 1499.

System Monitor known working ... JADEV3F.BIN/JADEV3F.ASM 2K 2716 EPROM Origin= E800-EFFF 8251 Data Port=10H & Status/CMD Port=11H

SWITCH	1	2	3	4	5	6	7	8
U1=	С	0	0	0	0	0	0	0
U23=	С	С	С	0	С	С	0	С
U33=	0	0	0	С	0	С	C	0



JADE Firmware: (EPROM and/or Disk)

Big Z Monitor "A" SFX-58001020E \$29.95 Monitor program on 2708 EPROM for JADE Big Z CPU, original JADE parallel-serial I/O board, serial terminal, and Versafloppy I or Tarbell disk controller.

Big Z Monitor "B" SFX-58001025E \$29.95 Similar to version A, but uses Tarbell cassette for tape I/O.

Big Z Monitor "C"/5-1/4" SFX-58001030E \$49.95 Combination monitor and CP/M BIOS for Big Z, serial terminal, Versafloppy I, and 5-1/4" drives (2716).

Big Z Monitor "C"/8" SFX-58001040E \$49.95 Same as above, for use with 8" drives.

Big Z Monitor "D"/5-1/4" SFX-58001050E \$49.95 Combination monitor and CP/M BIOS for Big Z, serial terminal, JADE Double-D disk controller, and 5-1/4" drives.

Big Z Monitor "D"/8" SFX-58001060E \$49.95 Same as above, for use with 8" drives.

Double-D Boot SFC-58001200E \$20.00 Standard bootstrap routine for JADE Double-D disk controller (2708). (Note Foxit PDF reader ver 4.3.0.1110 can convert this listing into ASCII text for use in a Z80 compiler)

Monitor listing based on Big Z Monitor "A" and Big Z Monitor "B" Note: Cassette functions are untested on actual hardware 07/15/24 so may not work all other functions should work

BIG Z MUNTOR (2K VERSION 3.0) 9/10/79 AB VERSION: JADEV3FC.280 JUNE 25,2020 BY AD TAPE FUNCTIONS INCLUDED NOW...VERSION C BACKGROUND-THIS MONITOR CODE IS FROM THE JADE BIG Z REVISION C MANUAL 1K ROM MONITOR THE VERSION WAS 2.0 A/B FOR CASSETTE STORAGE A=JADE 251P/AND B=TARBELL FROM THE ENCINEERING NOTES, THIS VERSION WAS KNOWN NOT TO WORK AND WAS POORLY COMMENTED THE CODE WAS MODIFIED WITH THE GOAL OF KEEPING THE BASIC MONITOR FUNCTIONS INTACT AND ADDING TO THE MONITOR WITH ITMROVEMENTS AND EXTENSIVE COMMENTE OWNERE POSSIBLE BETTER MENUS & PROMPTS, DR DOBBS MEMORY MAP, PORT IDENTIFER (SLOD.COM). TAPE FUNCTIONS THAT LOAD & SAVE DATA FOR KCTAPE ARE JADE ORIGINALS W/CHECK SUMS (BUT THERE IS NO STANDARD FOR THIS SO EXAMINE THE CODE). THE TARBELL TAPE ROUTINES ARE BASED ON THE TARBELL MANUAL AND ARE NOT JADE ORIGINAL ROUTINES. THE MONITOR WENT FROM A 1K 2708 TO A 2K 2716 EPROM. ASSUMPTIONS: 8251 SERIAL PORT ON BIGZ IS SET TO PORTS 10 AND 11H OR SIGO.COM PROPELLER CONSOLE BOARD AT PORTS 00H AND 01H (SIGO.COM PROP MUST ONLY ADDRESS THE 256 PORTS FOR A PRE-IEEE696 MACHINE) TARBELL TAPE USING STANDARD TARBELL PORTS OR KC STANDARD VIA JADE SERIAL/PARALLEL CARD 251P WITH AV51013 UART SET TO PORTS 00 & 80 HEX NO MEMORY SIZE IS ASSUMED ASSUME A VT-100 SERIAL TERMINAL CONNECTED TO JGZ80 8251 USART USING VT-100 'ESC' COMMANDS PROGRAMMING THE JGZ&0 &251 UART Asynchronous Communication Mode Mode Instruction MSB(Asych or Synch, Baud Rate, Word Length, Stop Bits, Parity)LSB MODE WORD (Write): D7+D6=Stop Bits,D5=Even Parity,D4=Parity Enable,D3+D2=Char Length,D1+D0=Baud *Note: a different Mode Word for Synchronous Communication is used but not used here Command Instruction MSB(DTR, RTS, Hunt Mode, Xmt Enable, Rxv Enable)LSB COMMAND WORD (Write): D7+HUT,D6=Int RSt,D5=FK5,D4+Err Rst,D3=Snd Brk,D3=Rx Enable,D1=DTR,D0=Tx Enable STATUS WORD (Read): D7=DSR,D6=Syn Det,D5=FFrame Err,D4=Overrun Err,D3=Parity Err,D2=Tx Empty,D1=Rx Rdy,D0=Tx Rdy PROGRAMMING THE JADE 2SIP CASSETTE PORT A AY51013/TRIG02 UART (note: This board does not actually have a programmable UART; but JADE used 74L5125 & 74L597 to emulate one) DATA Ports: "FOR A" can be either (00H,04H,08H,0CH,10H,14H,18H or 1CH) ⇒ HOLDS THE DATA WORD FOR I/O CONTROL PORTS: (DATA PORT) + (80H) ⇒ WRITE ONLY MS8(NP,TSB,N82,N81,EPS,XX,XX)CSB NP=1(NO PARITY),TBS=1(2 STOP BITS),N82+N81(00=5,01=6,10=7,11=8 BITS/CHAR),EPS=1(EVEN PARITY) STATUS PORTS: (DATA PORT) + (80H) ⇒ RED ONLY MS8(TBMT,PE,FE,DAV,XX,XX,XX)LSB TMBT=1(TX BUFF EMPTY),PE=1(PARITY IS BAD),FE=1(STOP BIT IS BAD),DAV=1(RX IS READY TO READ) PROGRAMMING THE TARELL- THE TARBELL AND THE CONTROL/STATUS PORT AT "6H" THE PORT ADDRESS BIT 'AO' DIFFERENTIATES BETWEEN THE TWO. DATA PORT IS AT "6H" AND THE CONTROL/STATUS PORT AT "6H" THE PORT ADDRESS BIT 'AO' DIFFERENTIATES BETWEEN THE TWO. DATA PORT IS AT "6H" AND THE CONTROL/STATUS PORT AT "6H" THE PORT ADDRESS BIT 'AO' DIFFERENTIATES BETWEEN THE TWO. TARBEL AND TARBEL AND TO RECEIVE, TXRDY-00H TARBEL READY TO TRECEIVE, TXRDY-00H TARBEL READY TO TRECEIVE, TXRDY-00H TARBEL READY TO TRANSMIT GP OUTPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT (11) - PORT 6H MSB[X,X,X,X, D3,D2,D1,D0]LSB WRITING A 'I' TURNS BIT ON AND "0' TURNS IT OFF GP INPUT PORT AS FOUR BITS (40ma) AND "DO'' IS USED TO CONTROL CASSETTE TAPE "MOTOR-ON" FUNCTION VIA RELAY TARBELL DEFINES: [3CH]=START BYTE, [E6H]=SYNC BYTE, [FFH]=LEADER BYTE NOTHING ELS IS SPECIFICALLY DEFINED SLR SYSTEMS ASSEMBLER USED TO GENERATE HEX CODE FOR USE-(Z80ASM.COM) EXAMPLE: "Z80ASM JADEV3FC.Z80 FH" JADE MONITOR ROM HAS BEEN COMPILED TO RESIDE AT (F800H-FFFFH). THIS WAS TO ALLOW FOR A DISK BOOT ROM TO RESIDE AT (F000H-F7FFH) WITHOUT WASTING MEMORY SPACE. COMPILER: COMPILED CODE SHOULD FIT INTO A 2716 EPROM WITH 2048 BYTES AVAILABLE 1999 BYTES - PROP/TARB 2023 BYTES - SERIAL/TARB 1889 BYTES - SERIAL/JADE 1865 BYTES - PROP/JADE 1865 BYTES - PROP/JADE MENU COMMANDS: A(MMOD)-MODIFY A RANGE OF MEMORY TO THE CONSOLE G(RUN)-GOTO AND RUN A PROGRAM AT THAT ADDRESS K(MENU)-REFRESH THE MENU SELECTIONS/SCREEN C(MMOVE)-THIS ACTUALLY COPIES B BLOCK OF MEMORY TO A NEW LOCATION C(MMOVE)-THIS ACTUALLY COPIES B BLOCK OF MEMORY TO A NEW LOCATION C(MMOVE)-THIS ACTUALLY COPIES B BLOCK OF MEMORY TO A NEW LOCATION C(MMOVE)-THIS ACTUALLY COPIES B BLOCK OF MEMORY THAT SELECTED HEX CHARACTER M(MMAP)-DR DUBBS MEMORY MAPPER THAT DISPLAYS REMORY BITS THAT CAN'T BE CHANGED AS "1111111" F(MFIL)-WILL FILL A BLOCK OF MEMORY WITH A SELECTED HEX CHARACTER M(MMAP)-DR DUBBS MEMORY MAPPER THAT DISPLAYS RAM, ROM, AND MISSING MEMORY L(MWRT)-ROUTINE TO ENTER SHORT PROGRAMS INTO CONSECUTIVE MEMORY LOCATIONS (MACHINE LANGUAGE PROGRAMS) P(PORTS)-WILL SCAN THE 0-255 I/O PORTS AND DISPLAY VALUES THAT IT FINDS S(CSAVE)-SAVE A BLOCK OF MEMORY BY SPECIFIED STARTING, LOCATION IN MEMORY ((ALCAD)-LOAD FROM CASSETTE TAPE TO A SPECIFIED STARTING, ENDING, AND NEW LOCATION ADDRESS X(CSYNC)-GENERATE A SYNC STREAM TAPE USED TO ADJUST THE CASSETTE TAPE VOLUME VIA THE (CAD) ROUTINE Y(CAS)-ROUTINE TO ADJUST THE CASSETTE PLAYER VOLUME CONTROL USING A SYNC STREAM TAPE B(TARB)-TARBELL FLOPPY DISK BOOT ROM VERSAFLOPPY BOOT ROM AT FOOM AND LOZA AT DHE ON FROM THERE B(TARB)-TARBELL FLOPPY DISK NOOT ROW TARE WAITEN TO MEMORY AND THEN RUN; WORKS ON A FPO-1771; NO BOOT ROM REQUIRED E(VERSA)-TARBELL FLOPPY DISK BOOT ROM AT FOOM AND LOZA A DISK SYSTEM FROM THERE U(XPORT)-CHANGE AN I/O PORT VALUE 0-255 BY ENTERING PORT HEX NUMBER, THEN NEW HEX VALUE FOR THAT PORT CONDITIONAL ASSEMBLY PARAMETERS DEFINE VALUES OF TRUE/FALSE EQU 0FFFFH EQU 0 TRUE: FALSE: EQU EQU DEFINE CONSOLE I/O EQU FALSE EQU TRUE , UART: PROP: ; USE BIG Z ONBOARD 8251 FOR CONSOLE I/O ; USE S100.COM PROPELLER CONSOLE BOARD FOR I/O DEFINE CASSETTE TAPE SYSTEM EQU TRUE EQU FALSE , TARBEL: KCTAPE: ; USE THE DON TARBELL CASSETTE BOARD ; USE THE JADE SERIAL/PARALLEL BOARD TRUE FALSE SYSTEM EQUATES ; LOCATION OF JADE MONITOR ROM MON: ORG 0F800H ASSUME JADE BIG Z MONITOR IS AT (F800)H - (FFFF)H 2KROM ASSUME VERSAFLOPPY II BIOS ROM AT (F000)H - (F7FF)H OR OTHER FLOPPY BIOS ==(f)IF КСТАРЕ ADDE 251P BOARD SELECT PORT B KC CASSETTE 'CURRENTLY SET TO PORT OH' JADE 251P BOARD ADDRESS UART B I/O (80H + SELECT PORT) 'CURRENTLY PORT O & PORT 80' JADE 251P: TO PROGRAM THE UART OPERATION MODE LOAD THE SELECT PORT + 80 ========(f)ENDIF AS THE I/O ADDRESS THEN OUTPUT THE CONTROL WORD TO THAT ADDRESS...BAUD, PARITY,ETC THE INPUT & OUTPUT ADDRESS IS THE SAME. THE CONTROL WORD IS AN OUTPUT WHILE THE STATUS SENSE IN AN INPUT. JADE 251P CATL WORD (10110000)B = B0H => NOP,ISTOP,8DATA JADE 251P STATUS SENSE (1XXXXXXX)B = 80H => CHARACTER READY TO TRANSMIT (DAV)=1 EQU EQU ENDTE TAPE: TAPST: 00H 80H

		_	
WAIT: SECT: DCOM:	EQU EQU EQU	0FCH 0FAH 0F8H	
DDATA: DSTAT: SBOOT:	EQU EQU	0FBH 0F8H 007DH	
TARBL ;	EQU EQU	06EH	; TARBELL CONTROL/STATUS PORT
KBDST: KBDDT:	IF EQU EQU	UART 11H 10H	; ====================================
KBDIN: KBDOT:	EQU EQU	02H 01H	; 8251 RECEIVE READY = (0000 0002)B or (02)H ; 8251 TRANSMIT READY = (0000 0001)B or (01)H
;	ENDIF IF	PROP	; ====================================
KBDST: KBDDT: KBDIN:	EQU EQU EQU	00н 01н 02н	; Status port is PORT (00)H ; Data port is PORT (01)H ; RECEIVE READY = (0000 0002)B or (02)H
KBDOT:	EQU ENDIF	04H	; TRANSMIT READY = (0000 0100)B or (04)H ====================================
3			THE FOLLOWING ARE JUMP SUBROUTINES THAT CAN BE ACCESSED BY OTHER PROGRAMS FOR THIS REASON THEY ARE LISTED HERE; BUT PROGRAM FLOW ONLY USES "INIT"
	JP JP	INIT EXEC	
	JP JP JP	CONIN CONOUT HEXIN	
	JP JP	HEXOUT DHXOT	
	JP JP JP	CRLF SPACE TREAD	
	JP	TWRIT + + + +	DEFINE MESSAGES HERE + + + +
;			; MESSAGE PRINT ROUTINE [DO NOT USE COMMA AS PUNCTUATION!!!]
, MSG1:	IF DEFM	TARBEL JADE COMPUTER SYSTEMS E	
;	DEFB ENDIF	03н	; 03H=END OF TEXT(h)ENDIF
MSG1:	IF DEFM DEFB	KCTAPE 'JADE COMPUTER SYSTEMS E 03H	;(i)IF IG Z MONITOR 3.0A' : 03H=END OF TEXT
; MSG2:	ENDIF	'TOP OF RAM:'	(i)ENDIF
;	DEFB	03н	; 03H=END OF TEXT
MSG3:	DEFM DEFB DEFB	ODH,OAH 03H	RT (F)MFIL (C)MMOVE (M)MMAP (V)MVER (T)MTEST (G)RUN' ; ODH=CARRIAGE RTN OAH=LINE FEED ; O3H=END OF TEXT
; MSG4:	DEFM DEFB DEFB	'(S)CSAVE (R)CLOAD (P)PC ODH,OAH O3H	NT (U)XPORT (X)CSYNC (Y)CADJ (B)TARB (E)VERSA (K)MENU' ; ODH=CARRIAGE RTN OAH=LINE FEED ; O3H=END OF TEXT
; MSG10:	DEFM DEFB	' xxxx <cr> <bs> <xx.> c ODH,OAH,O3H ; CR LF EOT</xx.></bs></cr>	or exit'
; MSG11:	DEFM DEFB	'BAD:' 03H	: END OF TEXT '03H'
; MSG12:	DEFM DEFB	' xxxx,xxxx <cr>' ODH,OAH,O3H ; C/R L/F EC</cr>	π
; MSG13:	DEFM DEFB	' xxxx <cr> or exit' ODH,OAH,O3H ; C/R L/F EC</cr>	π
; MSG14:	DEFM DEFB	' xxxx,xxxx,xx <cr>' ODH,OAH,O3H ; C/R L/F EC</cr>	
; MSG15:	DEFM DEFB	' xxxx,xxxx,xxxx <cr>'</cr>	
; MSG16:	DEFM	ODH,OAH,O3H ; C/R L/F EC ADJ VOL GOOD(+)/BAD(\$)	,
; MSG17:	DEFB	ODH,OAH,O3H ; C/R L/F EC ' SYNC STREAM TAPE:'	л Т
; MSG18:	DEFB	ODH,OAH,O3H ; C/R L/F EC	IT IMORY: <strt>,<end>,<new>'</new></end></strt>
; MSG19:	DEFB	ODH,OAH,O3H ; C/R L/F EC	
:	DEFB	03н	; END OF TEXT '03H'
м́sg20: ;	DEFM DEFB	' xxxx <cr>' ODH,OAH,O3H ; C/R L/F EC</cr>	т
MSG21:	DEFM DEFB	' XXXX <cr> PORT VALUE' ODH,OAH,O3H ; C/R L/F EC</cr>	
м́sg22:	DEFM DEFB	' DISK BOOTSTRAP LOADER' ODH,OAH,O3H ; C/R L/F EC	
MSG23:	DEFM DEFB	' DISK BOOT ROM AT F000H ODH,0AH,03H ; C/R L/F EC	י' ד
init:			; SET UP THE UART AND THEN INITIALIZE THE STACK
	IF LD OUT	UART A,00H (KBDST),A	; ; Initialize USART send 00H three times to guarantee device in "Command Instruction"
	LD OUT LD	A,00H (KBDST),A A,00H	; INITIALIZE USART ; INITIALIZE USART
"Mode Too	OUT LD	(KBDST),A A,40H	; Send internal reset "Command Instruction" (0100 0000) or 40H and ready 8251 to recieve a
;	truction" OUT	(KBDST),A	Mode word: (01)-1 stop bits (00)-parity disabled (11)-char length 8 bit (10)-baud 16x
;	LD OUT	A,4EH (KBDST),A	Mode word: (01001110) or (4E)Hex1xBaud = 153,600 1/16xBaud = 9,600 1/64xBaud = 2,400 ; Mode register 8,1,n,9600 or 4EH
;			Command word:(0)-disable hunt mode (0)-do not return to mode word (1)-reset output 0 Command word:(1)-reset all error flags (0)-normal operations (1)-receive enable Command word:(1)-DTR will output "0" (1)-transmit enable
;	LD	A, 37H	Command word:(0)-disable hunt mode (0)-do not return to mode word (1)-reset output 0 Command word:(1)-reset all error flags (0)-normal operations (1)-receive enable Command word: (0011 0111)Binary or (37)Hex Command register 37H essentially enables both transmit & recieve modes INITIALIZE THE ONBOARD UART
;	OUT ENDIF	(KBDST),A	;()ENDIF
;			TOP OF MEMORY ROUTINE AND SETUP STACK

		- 1	
FTOP:	LD LD	B,1 HL,TRUE	; SET POINTER TO "1" ; PRELOAD MEMORY ADDRESS WITH "FFFF"
FTOP1:	INC	HL	; ADD I TO MEMORY POINTER HL (START AT "0000" GOING TO "FFFF") ; LOAD "A" WITH (HL) CONTENTS
	LD CPL	A,(HL)	; MODIFY THE MEMORY CONTENTS
	LD CP	(HL),A (HL)	; LOAD MEMORY LOCATION (HL) WITH MODIFIED CONTENT
	CPL		; SEE IF MEMORY CONTENT COULD BE CHANGED
	LD JP	(HL),A NZ,FTOP2	; IF CHANGED=RAM, IF NOT CHANGED=TOP OF RAM ; IF CHANGED=TOP OF RAM, JUMP OUT; OTHERWISE REPEAT
	LD	в,0	; SET POINTER TO "0", FOUND SOME MEMORY!
FTOP2:	JR LD	FTOP1 A,B	; LOAD "A" WITH "MEMORY POINTER"
	OR	A	:
	JP DEC	NZ,FTOP1 HL	; IF POINTER IS "1", THERE IS NO MEMORY AT THIS LOCATION, TRY AGAIN ; SUBTRACT BY 1
	DEC	HL	; SUBTRACT BY 1
	LD PUSH	SP,HL HL	; LOAD THE (SP) STACK POINTER WITH HL
	POP	IY	; SAVE STACK ADDRESS IN IY
;	CALL	CLRSCN	; CLEAR SCREEN AND MOVE CURSOR TO UPPER LEFT CORNER
	LD CALL	HL,MSG2 MARQ	TOP OF MEMORY MESSAGE - ONE TIME ONLY AT BOOT MESSAGE MARQUEE ROUTINE
	LD	HL,1	, MESSAGE MARQUEE ROOTINE
	ADD CALL	HL,SP DHXOT	; DISPLAY THE TOP OF MEMORY - HEX OUT TO CONSOLE
	CALL	CRLF	,
; INIT1:	LD	HL,MSG1	; DISPLAY THE JADE SIGN-ON MESSAGE
	CALL	MARQ CRLF	; MESSAGE MARQUEE ROUTINE
;	CALL	CKLF	
EXEC:	TF	TARBEL	; NOT SURE OF THIS ROUTINE - CHECK IF USING TARBEL ====================================
	CALL	CRLF	; CRLF TO CONSOLE
	LD SUB	SP,IY A	; LOAD SP FROM IYIY CONTAINS THE SP ?? : A=A=0
	OUT	(TARBL),A	; OUTPUT TO TARBEL STATUS PORT MSB[X,X,TXRDY,RXRDY, X,X,X,X]LSB
;	ENDIF		; =======================(d)ENDIF
,	LD	HL,MSG3	; ROUTINE TO PRINT THE TWO LINES OF MENU COMMANDS
	CALL	MARQ HL,MSG4	; MESSAGE MARQUEE ROUTINE
_	CALL	MARQ	; MESSAGE MARQUEE ROUTINE
EXEC3:			; DISPLAY MONITOR PROMPT
	LD CALL	A,'#' CRLF	; MONITOR PROMPT: # SIGN
	CALL	CONOUT	
			+ + + MENU TABLE ENTRIES + + +
, EXEC4:	CALL	CONIN	; GET CONSOLE INPUT IN REGISTER 'A'
	CP JP	21H M,EXEC4	; LOOP ON CONTROL CHARACTERS ASCII(00H-20H)
	CP	'A'	
	JP CP	Z,ALTER 'D'	; MODIFY MEMORY ROUTINE = A
	JP	Z DUMP	; DUMP MEMORY ROUTINE = D
	CP JP	'G' Z,GO	; JUMP TO ADDRESS AND RUN = G
	CP JP		; PRINT THE MENU CHOICES = K
	CP	Z,KMENU 'C'	
	JP CP	Z,COPY 'T'	; MOVE MEMORY ROUTINE = C
	JP	Z,MTEST	; TEST MEMORY ROUTINE = T
	CP JP	'F' Z,FILL	; FILL MEMORY ROUTINE = F
	CP	'M'	
	JP CP	Z,MEMMAP	; MAP RAM AREAS = M
	JP	Z,MLOAD	; WRITE DIRECT INTO MEMORY = L
	CP JP	'P' Z,PORTS	; DISPLAY AVAILABLE PORTS
	CP JP	Z, PORTS	
	CP	Z,TSAVE 'R'	; SAVE MEMORY ON CASSETTE = S
	JP CP	Z,TLOAD 'V'	; LOAD MEMORY FROM CASSETTE = R
	JP	Z,VERIFY 'X'	; VERIFY MEMORY BLOCK COPY/MOVE = V
	CP JP	7. STRM	; DO A SYNC STREAM OUTPUT = X
	CP	Z,STRM	
	JP CP	Z,TUNE 'B'	; ADJUST CASSETTE VOLUME ROUTINE = Y
	JP CP	Z,BOOT 'E'	; TARBELL BOOT ROUTINE = B
	JP	Z,BIOS	; VERSAFLOPPY II FLOPPY BIOS ROM = E
	CP JP	'U' Z,QUERY	; CHANGE PORT VALUE
;			
;	JP	EXEC4	; IF INCORRECT OR NO SELECTION IS MADE, TRY AGAIN
BIOS:	LD	HL,MSG23	; OUTPUT BRIEF INSTRUCTION ; OUTPUT TO CONSOLE
	CALL JP	MARQ 0F000H	; JUMP TO FLOPPY ROM AT FOOOH
; GO:			; JUMP TO A MEMORY LOCATION AND RUN A PROGRAM THERE
GO.	LD	HL,MSG20	
	CALL CALL	MARQ SPHIN	; OUTPUT BRIEF INSTRUCTION ; OUTPUT TO CONSOLE
	CALL	CRLF	
:	JP	(HL)	; EXECUTE A PROGRAM AT '(HL)' NO RETURN NEED RE-BOOT
ALTER:			; MODIFY OR EXAMINE MEMORY ROUTINE # A <enter> # A 0100 <cr></cr></enter>
			0100 00 <memory 0100="" displayed="" location=""></memory>
i			0100 00 FF. <memory 0100="" and="" changed="" ff="" inc="" location="" pc="" to=""></memory>
;			UIUI UU / <memory exit="" routine="" unchanged=""></memory>
2			0101 00 <cr> <memory and="" dec="" pc="" unchanged=""> 0101 00 <bs> <memory and="" inc="" pc="" unchanged=""></memory></bs></memory></cr>
;			0100 FF
	LD CALL	HL,MSG10 MARQ	; OUTPUT BRIEF INSTRUCTION ; OUTPUT TO CONSOLE
	CALL	SPHIN	,
ALT1:	CALL	CRLF DHXOT	
	CALL	SPACE	
	LD CALL	A,(HL) HEXOUT	
	PUSH	HL SPHIN	
	LD	E,L	
	POP CP	HL ODH	; ODH=CR MEANS DON'T CHANGE BUT DECREMENT TO THE NEXT LOCATION
	JP	Z,ALT3	
	CP	1	; THE '/' IS THE EXIT CHARACTER W/O CHANGE

ALT2: ALT3:	JP CP JP LD INC JR DEC JR	Z,EXEC3 NZ,ALT2 (HL),E HL ALT1 HL ALT1	: THE '.' IS THE MODIFY CHARACTER AS IN '0100 00 12.' : IF THE '.' IS DETECTED : LOAD THE VALUE IN 'E' TO MEMORY LOCATION '(HL)' : INCREMENT THE MEMORY LOCATION '(HL)' : START AGAIN AT ALT1 : DECREMENT THE MEMORY LOCATION AND START AGAIN AT ALT1
; DUMP: ; ;		HL,MSG12 MARO	; DUMP MEMORY ROUTINE # D < < < < < = < (memory location 0100 displayed> # D = # D 0100,0110 < <cr> 0100 03 03 03 03 03 <</cr>
DUMP1: DUMP2:	CALL CALL CALL LD CALL LD CALL CALL CALL	MARQ DHXIN CRLF DHXOT B,16 SPACE A,(HL) HEXOUT CMPDH	
	JP INC DEC JP JR	C,EXEC3 HL B NZ,DUMP2 DUMP1	; EXIT THE ROUTINE ; INCREMENT THE PC 'HL'
; MEMMAP:			; MEMORY MAP PROGRAM CF.DR.DOBBS VOL 31 P40 AND JOHN MONAHAN S-100.COM
MAP1A:	LD LD LD CPL LD CP CPL	HL,0 B,1 E,'R' A,(HL) (HL),A (HL)	; IT WILL SHOW ON CONSOL TOTAL MEMORY SUMMARY OF RAM, PROM, AND NO MEMORY ; PRINT R FOR RAM
MAP2A: MAP3A:	LD JP CP JP LD LD CP JP INC XOR	(HL),A NZ,MAP2A (HL) Z,PRINTA E,'p' A,OFFH (HL) NZ,PRINTA L A	
PRINTA:	CP JP LD DEC JP LD CALL	L NZ,MAP3A E,'' L,O B NZ,NLINEA B,16 CRLF	
NLINEA:	CALL LD CALL LD CALL INC JP	HXOT4 A,20H OTA A,E OTA H NZ,MAP1A	: 16 HEX CONSOL OUT ROUTINE : LOAD REG A WITH 'SPACE' (20H) ; SEND TO CONSOL WHAT'S IN REG A ; SEND TO CONSOL WHAT'S IN REG A
	CALL JP	CRLF EXEC3	
MLOAD:			; WRITE DIRECTLY INTO MEMORY ROUTINE: THIS ROUTINE WILL ACCEPT A STARTING ADDRESS FOLLOWED BY HEX DATA THAT IS PLACED CONSECUTIVELY INTO MEMORY. ENTERING AN '/' WILL EXIT THE ROUTINE. THIS COULD BE USED TO ENTER SHORT PROGRAMS INTO MEMORY TO BE RUN WITH THE 'GO' COMMAND.
3 3 3 3 3 3 3 3 3 3 3 3 3 3			ENTER HEX VALUES STARTING AT SPECIFIC MEMORY LOCATION # L <neter> # L 0100 <cr> 0100 <nemory 0100="" displayed="" location=""> 0100 AF <cr> <nemory 0100="" af="" and="" changed="" inc="" location="" pc="" to=""> 0101 <nemory 0101="" displayed="" location=""> 0101 / <nemory exit="" routine="" unchanged=""></nemory></nemory></nemory></cr></nemory></cr></neter>
ML1: ML2:	LD CALL CALL CALL CALL CALL PUSH CALL	HL,MSG13 MARQ SPHIN CRLF DHXOT SPACE HL SPHIN	; GET A MEMORY ADDRESS TO PLACE THE CODE ; GOTO A NEW LINE ; DISPLAY THE MEMORY ADDRESS ; ADD A SPACE ; REG PAIR 'HL' CONTAINS ADDRESS OF DATA LOCATION IS PUSHED ONTO STACK ; RITER SOME HEX DATA, A <cr> OR A '/'</cr>
мц3:	LD POP CP JP CP JP LD INC	E,L HL '/' Z,ML4 ODH NZ,ML3 (HL),E HL	; THE '/' IS THE EXIT CHARACTER W/O CHANGE ; EXIT TO EXEC ; <cr> = ODH ; IF THE '.' IS DETECTED ; LOAD THE VALUE IN 'E' TO MEMORY LOCATION '(HL)' ; INCREMENT THE MEMORY LOCATION '(HL)'</cr>
	CALL JR	CRLF ML2	; START AGAIN AT ML2
ML4:	CALL CALL LD CALL CALL LD CALL LD CALL	CRLF CRLF A, 'D' CONOUT A, 'O' CONOUT A, 'N' CONOUT	
	LD CALL JP	A,'E' CONOUT EXEC3	
; KMENU:	CALL JP	CLRSCN INIT1	; ROUTINE TO CLR SCREEN & HOME POSITION ; FILL SCREEN WITH BLANKS AND HOME CURSOR ; JUMP TO INITI - DISPLAY JADE SIGN-ON MESSAGE
; FILL: ; ;			; MEMORY FILL ROUTINE # F # F 0100-0150,DE ~enter> This will write "De" into all memory locations between 0100 - 0150 Only one byte "" entered is valid as the fill
,	LD CALL SUB JP PUSH CALL	HL,MSG14 MARQ DHXIN ODH Z,FILLO HL HEXIN	Only one byte "" entered is valid as the fill

FILLO: FILL1:	LD POP DEC INC LD CALL JP JP	A,L HL HL (HL),A CMPDH NC,FILL1 EXEC3		
COPY:			; COPY MEMORY FROM ONE LOCATION TO ANOTHER LOCATION # C # C 0100-0150,0200	
; COPYO:	LD CALL CALL LD LD	HL,MSG15 MARQ TRPIN CRLF A,(DE) (BC),A	; TRPIN: INPUT 3 WORDSPLACE IN [HL],[DE],[BC]ex: (hhll),(ddee),(bbcc) <cr> [HL]=END [DE]=BEG [BC]=DESTWANT TO INC DE AND BC UNTIL DE=HL</cr>	
:	CALL JP INC INC JP	CMPDH C,EXEC3 DE BC COPYO	; COMPARES [DE] TO [HL] IF EQUAL [CARRY FLAG] = 1 ; EXIT THE ROUTINE IF [CARRY FLAG] = 1	
,			MEMORY TEST ROUTINE: (64K OR LESS) # Tenter> # T 0100,0200 <enter> - WILL TEST MEMORY FROM 0100H TO 0200H - WILL RETURN NOTHING IF MEMORY IS OK OR - ADDRESS OF BAD MEMORY WITH BAD BITS</enter>	
· · · · · · · · · · · · · · · · · · ·			THIS IS A 'QUICKIE' MEMORY TEST TO SPOT HARD MEMORY FAILURES, OR ACCIDENTLY PROTECTED MEMORY LOCATIONS. IT IS NOT MEANT TO BE THE DEFINITIVE MEMORY DIACNOSTIC. IT IS, HOWEVER, NON-DESTRUCTIVE. ERRORS ARE PRINTED ON THE CONSOLE AS FOLLOWS- <addrs 00000100="" <1="" where=""> IS THE BAD BIT. BIT LOCATION OF THE FAILURE IS EASILY DETERMINED. NON-R/W MEMORY WILL RETURN WITH- 1111111</addrs>	
; MTEST:	LD CALL LD	HL,MSG12 MARQ HL,0	; INPUT TWO HEX NUMBERS IN REGISTER PAIR 'HL' AND 'DE' (XXh XXh) AND (XXh XXh) ; INITIALIZE HL TO ZERO	
MT1:	CALL CALL LD	DHXIN CRLF A, (HL)	; GET TWO PARAMETERS FROM THE CONSOL HL=(START ADDR) DE=(END ADDR) ; LOAD 'REG A' WITH BYTE (HL) ; STORE ORIGINAL BYTE (HL) TO 'REG B'	
	CPL LD XOR	B,A (HL),A (HL)	; COMPLEMENT A(INVERT A)1† 'REG A'=[11110001] => 'REG A'=[00001110] ; LOAD (COMPLEMENT'd) A TO (HL) ; XOR: (both bits same, then make '0')IF NOT '0' THEN BITS ARE STUCK, BAD OR ROM	
;	JP PUSH LD CALL LD CALL	Z, MT2 DE D, B E, A BAD A, E HISP	; IF JUMP TO MT2, NO BAD MEMORY FOUND BAD MEMORY FOUND, DISPLAY IT ON CONSOL ; SAVE END POINTER 'DE' ON STACK SO 'REG D' AND 'REG E' ARE AVAILABLE FOR USE ; LOAD 'REG D' WITH ORIGINAL BYTE (HL) THAT IS BAD ; LOAD 'REG E' WITH CMP AND XOR BYTE (HL) 7?? ; PRINT 'BAD: 'TO THE CONSOL (AF AND HL ARE UNCHANGED IN ROUTINE 'BAD') ; MAKE SURE 'REG A' IS UNCHANGED AFTER MSG ; PRINT 'HL' TO CONSOL FOLLOWED BY A SPACE ; SEND 'N BLANK TO CONSOL OUT	
	LD CALL LD CALL CALL LD POP	HLSP A, ' CONOUT A,E BITS1 CRLF B,D	; SEND ' ' BLANK TO CONSOL OUT ; CONVERT HEX TO BINARY BITS AND DISPLAY	
MT2: MND1:	LD	DE (HL),B A,H	; RESTORE SAVED BYTE (HL) ; NOW SEE IF WE REACHED THE END ; COMPARE H[XXXX]L TO D[XXXX]E	
MND2:	LD CP JP JR LD LD CP JP	C,D C,MND2 INCR1 A,L C,E C,E Z,MND3	: DOES H=D : IF H=D GOTO MND2 : H<>D GOTO INCR1 : COMPARE H[XXXX] TO D[XXXX]E : DOES L=E : IF L=E WE ARE ALL DONE SO GOTO MND3 : IF L<∞E CONTINUE TO INCR1	
; INCR1:	INC JR	HL MT1	; INC HL, THIS MOVES HL (START) CLOSER TO DE (END) ; NOT THERE YET SO GO BACK FOR MORE	
; MND3:	CALL LD CALL JP	CRLF HL,MSG19 MARQ EXEC3	; REACHED THE END LOAD MESSAGE "END " ; DISPLAY MESSAGE	
; PORTS: ;			; PORTS ROUTINE TO DISPLAY DETECTED PORTS - FROM JOHN MONAHAN \$100.COM	
	CALL LD LD LD	CRLF B,0 D,6 E,0FFH	; LOOP THROUGH ALL PORTS (0-FF) ;Display 6 ports across ;Will contain port number	
; LOOPIO:	LD LD	C,E A,E	; LOAD 'REG C' WITH OFFH ; LOAD 'REG A' WITH OFFH	
;	IN CP	A,(C) OFFH	Remember [ZASMB does not work with this opcode,SLR is OK]	
	JR LD CALL LD CALL LD CALL LD CALL	Z,SKIP H,A A,E LBYTE A,'-' CONOUT A,'>' CONOUT	: IF DATA PORT C CONTAINS (FF)H, SKIP IT DATA PORT C HAS SOMETHING SO STORE IN 'H' FOR BELOW LOAD CURRENT PORT NUMBER TO 'REG A' PRINT PORT NUMBER	
	LD CALL LD CALL	A,H LBYTE A,09H CONOUT	: GET PORT DATA STORED IN 'H' : PRINT TO CONSOL ; 09H = TAB	
	DEC JR LD	D NZ,SKIP D,6	; 6 PORTS PER LINE	
SKIP:	CALL DEC DJNZ CALL JP	CRLF E LOOPIO CRLF EXEC3	; NEXT PORT	
, QUERY:	LD CALL	HL,MSG21 MARQ	; OUTPUT VALUE TO A PORT ; GET INPUT PROMPT "XXXX <cr> PORT VALUE" EX: PORT(10)=>(FF)"10FF <cr>" SET (PORT 10) TO (FF) ; DISPLAY MESSAGE TO CONSOLE</cr></cr>	

	CALL LD LD	DHXIN C,H A,L	; GET TWO HEX VALUES [HL]; H=PORT,L=VALUE ; LOAD REG "C" WITH THE HARDWARE PORT ; LOAD REG "A" WITH THE NEW VALUE ; WRITE PORT (C) WITH VALUE "A"
;	OUT JP	(C),A EXEC3	; WRITE PORT (C) WITH VALUE "A"
;********	********		TAPE ROUTINES ************************************
;	IF	KCTAPE	; KANSAS CITY TAPE(a)IF
; TLOAD:	LD	HL,MSG20	; ROUTINE TO LOAD TAPE DATA TO MEMORY ; PREPARE CASSETTE PLAYER, ENTER <load addr="" start="">, <load addr="" end="">,<cr>, START PLAYER, ; LEADER LOADS, DATA STARTS,'S' DISPLAYED, DATA ENDS,"**" DISPLAYED IF BAD CHKSUNM ; LOAD KANSAS CITY TAPE DATA AT SPECIFIED MEMORY LOCATION ; GET STARTING MEMORY ADDRESSXXYY (CR> HL=(XX), DE=(YY)</cr></load></load>
	CALL CALL	MARQ DHXIN	; DISPLAY MESSAGE ; GET TWO HEX VALUES FROM KEYBOARD
	CALL JP	TREAD Z,EXEC3	TAPE LOAD WAS SUCCESSFUL
	CALL LD CALL	SPACE A, ' * ' CONOUT	; TAPE LOAD ERROR; SEND SPACE TO CONSOLE ; SEND "*" TO CONSOLE INDICATING A CHKSUM ERROR
	JP	EXEC3	TAPE FORMAT: [FF][FF][FF][FF][E6][DD][DD][DD][CHKSUM]
TREAD:	LD OUT LD	A,0B0H (TAPST),A HL,TRUE	: set up 251p Aў51013 ÚART ON CÁSSÉTTE PORT A ; wRITE BOH TO "CONTROL WORD PORT" MSG(NP,TSB,NBZ,NBJ,EPS,X,X,X)LSB ; BOH=(1,0,1,1, 0,0,0,0)=(NO PARITY,1 STOP BIT,8 DATA BITS,ODD PARITY) ; HL IS A DELAY SEED; TRUE = OFFFFH
TRDA:	CALL	DELAY B.4	; SET COUNTER B=4; LATER B BECOMES CHKSUM
TRDB:	CALL CP	CIN OFFH	; GET CASSETTE DATA : IF DATA IS NOT "FFH" THEN LEADER HASN'T STARTED YET NZ=FALSE
	JR DEC	NZ,TRDA B	; IF DATA IS 'FFH', FOUND LEADER SO KEEP READING CASSEITE DATA, IF 'E6H' ; DECREMENT THE COUNTER B
TRDC:	JR CALL	NZ, TRDB CIN	; GET NEXT (4) BYTES FROM CASSETTE [FF][FF][FF][FF] ; READ DATA FROM THE TAPE ; IS DATA LEADER "FFH"
	CP JR CP	OFFH Z,TRDA	: IF IT IS LEADER: START ALL OVER READING THE NEXT (4) BYTES
	JR LD	0E6H NZ,TRDA B,0	; IS BYTE "E6H"START OF DATA WITH "SYNC BYTE" ; IF IT IS NOT "E6H" SOMETHING IS WRONG SO START AGAIN ; FOUND THE "SYNC BYTE" (E6); SO SET CHECKSUM=B=0
	LD CALL	A,'\$' CONOUT	; SEND "\$" TO CONSOLE INDICATING START OF MEMORY LOAD FROM TAPE
TRD1:	DEC INC	HL HL	; INCREMENT LOAD ADDRESS HL
	CALL LD ADD	CIN (HL),A A.B	; LOAD TAPE DATA IN "A" ; WRITE "A" TO MEMORY LOCATION (HL)
	CALL	CMPDH NC,TRD1	; ADD CHKSUM TO A ; COMPARE "D" TO "H"START=END NC=FALSE
	CALL CP	CIN B	; LOAD TAPE DATA [CHKSUM] ; IF TAPE CHKSUM = B; THEN Z=TRUE
;	RET	. ()	
CIN:	IN AND JR	A,(TAPST) 10H Z.CTN	; READ "STATUS SENSE PORT" FOR 2S1P AY51013 UART ON CASSETTE PORT B ; MSB(TBMT,PE,FE,DAV,X,X,X,X)LSB 10H=(0,0,0,1, 0,0,0,0)=> DAV=0 (RX IS RDY)
	IN RET	Z,CIN A,(TAPE)	; READ DATA INTO "DATA WORD PORT"
TUNE:	LD	А, ОВОН	; ROUTINE TO ALLOW FOR ADJUSTMENT OF TAPE PLAYER VOLUME CONTROL-NEED SYNC STREAM TAPE AS INPUT ; SET UP 251P AY51013 UART ON CASSETTE PORT B ; WRITE BOH TO "CONTROL WORD PORT" MSB(NP,TSB,NB2,NB1,EPS,X,X,X)LSB
	OUT CALL	(TAPST),A CLRSCN	; B0H=(1,0,1,1, 0,0,0,0)=(NO PARITY,1 STOP BIT,8 DATA BITS,ODD PARITY)
TUN0:	LD CALL LD	B,30 HOME HL,MSG16	; B IS A LINE COUNTER TO PRINT 30 LINES TO CONSOLE ; MOVE CURSOR TO UPPER TOP LEFT OF SCREEN
	CALL	MARQ	LOAD A "SYNC STREAM TAPE" AND OBSERVE DISPLAY FOR "\$" OR "+" ADJUST THE TAPE PLAYER VOLUME TO ONLY DISPLAY "+"
TUN1:	CALL LD	CRLF H,40	; SEN CRLF TO CONSOLE ; LOAD COUNTER TO 40; PRINTS 40 "+" OR "\$" TO CONSOLE = 1 LINE
TUN2:	CALL CP JR	CIN OFFH	; INPUT TAPE DATA ; IS DATA [FF]; IF IT IS, Z=TRUE ; DATA [FF]; IF IT IS, Z=TRUE
	LD CP	Z,TUN2 L,'+' 0E6H	; DATA IS LEADER, TRY AGAINOHERWISE CONTINUE BELOW ; L="+" ; IS DATA [E6] THE SYNC BYTEIF SO, Z=TRUE
	JR LD	Z,TUN3 L,'\$'	; IF FOUND [E6] GOTO TUN3(L="+" GOOD/L="\$"BAD) ; L="\$"
TUN3:	LD CALL	A,L CONOUT	; SEND L TO CONSOLE
	DEC JR DEC	H NZ,TUN2 B	; DECREMENT COUNTER H ; IF H=0, START ALL OVER AGAIN
	JR JP	NZ,TUN1 TUN0	
;			; TSAVE ROUTINE-USED TO SAVE A BLOCK OF MEMORY TO CASSETTE TAPE
TSAVE:	LD	HL,MSG12	; CONSOLE PROMPT FOR BEGINNING AND ENDING MEMORY ADDRESS ; TSAVE XXXX,YVY <cr> STARTS THE TAPE SAVE ; FORMAT: [FF][FF]16[FF][E6][DD][DD][DD][DD][CHKSUM][CHKSUM][CHKSUM]</cr>
	CALL CALL CALL	MARQ DHXIN TWRIT	; FOKMAI: [FF][FF]ID[FF][E6][DD][DD][DD][DD][CHKSUM][CHKSUM][CHKSUM] ; GET STARTING MEMORY ADDRESSXXYY <cr> HL=(XX), DE=(YY)</cr>
TWRIT:	JP LD	EXEC3 A,0B0H	; SET UP 2S1P AY51013 UART ON CASSETTE PORT A
	OUT	(TAPST),A	; WRITE BOH TO "CONTROL WORD PORT" MSB(NP,TSB,NB2,NB1,EPS,X,X,X)LSB ; BOH=(1,0,1,1, 0,0,0,0)=(NO PARITY,1 STOP BIT,8 DATA BITS,ODD PARITY)
TWRT0:	LD LD CALL	B,16 A,0FFH COUT	; COUNTER B=16 ; LOAD A=[FF] . weiter [se] to tabe
	DEC	B NZ,TWRT0	; WRITE [FF] TO TAPE ; WRITE [FF] TO TAPE ; DECREMENT COUNTER B : KEEP GOING UNTIL 16 [FF]'S HAVE BEEN WRITTEN TO TAPE
	LD CALL	A, ÓE6H COUT	; KEEP GOING UNTIL 16 [FF]'S HAVE BEEN WRITTEN TO TAPE ; LOAD A WITH [E6] THE SYNC BYTE ; WRITE SYNC BYTE TO TAPE
	DEC LD	НL В,0	; LOAD CHKSUM B=0
TWRT1:	INC LD CALL	HL A, (HL) COUT	; INCREMENT HL ; LOAD DATA FROM (HL) TO A ; WRITE DATA TO TAPE
	ADD LD	A,B B,A	; ADD CHKSUM TO A ; SAVE SUM BACK TO CHKSUM
	CALL JR	CMPDH NZ,TWRT1	; COMPARE D TO H : KEEP WRITING DATA UNTIL NZ=FALSE
	LD CALL	A,B COUT	; LOAD THE CHKSUM TO A ; WRITE CHECKSUM ONCE
COUT:	CALL JR PUSH	COUT COUT AF	; WRITE CHCKSUM TWICE ; WRITE CHKSUM A THIRD TIME ; PUSH DATA TO BE WRITTEN ONTO AF
	IN AND	A,(TAPST) 80H	; READ STATUS PORT MSB(TBMT,PE,FE,DAV,XX,XX,XX,XX)LSB ; 80H=[1,0,0,0, 0,0,0,0] IF TBMT=1, TRANSMIT BUFFER NOT RDY
	JR POP	Z,COUT+1 AF	; IF TBMT <> 0 KEEP CHECKING ; POD DATA TO BE WRITTEN TO TAPE
	OUT RET	(TAPE),A	; WRITE DATA TO TAPE
; STRM:	LD CALL	HL,MSG17 MARQ	; STREAM ROUTINE-GENERATES A SERIES OF "FFH" AND "E6H"[FF] [E6] [FF] [E6] [FF] ; START THE ROUTINE AND RECORD THE OUTPUT TO CASSETTE TAPE ; THIS, WILL, CREATE A, "SYNC STREAM TAPE" USED TO CALIBRATE THE TAPE VOLUME
	LD	А, ОВОН	; THIS WILL CREATE A "SYNC STREAM TAPE" USED TO CALIBRATE THE TAPE VOLUME ; SET UP 251P AY51013 UART ON CASSETTE PORT A

STRM1:	OUT LD CALL	(TAPST),A A,OFFH COUT	; WRITE BOH TO "CONTROL WORD PORT" MSB(NP,TSB,NB2,NB1,EPS,X,X,X)LSB ; BOH=(1,0,1,1, 0,0,0,0)=(NO PARITY,1 STOP BIT,8 DATA BITS,ODD PARITY) ; WRITE [FF] TO TAPE		
	LD CALL	A, 0E6H COUT	; WRITE [E6] TO TAPE		
;	JR	STRM1			
;	ENDIF		; KANSAS CITY TAPE ====================================		
;	IF	TARBEL	; TARBELL TAPE ====================================		
			: TAPE FORMAT: [FF][FF][FF][5][60][00][00][00][1A][FF][CHSUM][FF][FF][FF][FF][FF] [FF][FF][FF] TAPE LEADER; [3C]=START BYTE: [66]=SYNC BYTE; [0D]=DATA BYTES; [1A]+[FF]=STOP BYTES; [CHKSUM]=CHECKSUMSIMPLE SUM OF DATA BYTES ; END OF RECORD- [IA][FF][CHKSUM]=CHECKSUMSIMPLE SUM OF DATA BYTES ; NOTE: ROUTINES ARE FROM THE DON TARBELL MANUAL WHERE POSSIBLE AS THEY SEEM MUCH BETTER ; THAN THE JADE TARBEL ROUTINESREFERENCE "WRITING PROGRAMS FOR THE CASSETTE INTERFACE", ; "CASSETTE INTERFACE INPUT ROUTINE", "CASSETTE INTERFACE OUTPUT ROUTINE"		
;			: LOAD MEMORY FROM TAPE ROUTINE-CASSETTE INTERFACE INPUT ROUTINE		
TLOAD:	LD CALL CALL DEC INC	HL,MSG20 MARQ DHXIN HL HL	GET STARTING MEMORY ADDRESSXXYY <cr> HL=(XX), DE=(YY) LOAD MESSAGE PROMPT DISPLAY MESSAGE GET STARTING MEMORY ADDRESSXXYY <cr> HL=(XX), DE=(YY)</cr></cr>		
	CALL JP CALL LD CALL CALL	TREAD Z,EXEC3 CRLF A,C CONOUT SPACE	TARBELL OUTPUT PORT J1 BIT DD=CASSETTE MOTOR CONTROL ON/OFF IF THE CHKSUM MATCHED (FLAG Z IS TRUE), THEN EXIT IF THE CHECKSUM DID NOT MATCH LOAD TAPE CHKSUM		
	LD CALL	A,B CONOUT	; LOAD THE CALCULATED CHKSUM		
	CALL LD CALL JP	SPACE HL,MSG11 MARQ EXEC3	; "BAD" MESSAGE		
TREAD:	LD OUT LD	A,11H (TARBL),A B,O	; LOAD 11H TO "A" BECAUSE WE WANT TO RESET THE INTERFACE & START THE CASSETTE MOTOR ; WRITE 11H TO THE STATUS PORT (GEH) MSB[X,X,TXRDY,RXRDY, 0,0,0,0D]LSB ; MSB[0,0,0,1, 0,0,0,1]LSB = 11H ; B=CHKSUM BYTE, SET TO "00"		
TRD0:	LD LD	C,0 A,C	; REG "C" IS USED AS PATTERN IDENTIFER=(1)[FF];(2)[3C];(3)[E6];(4)[1A];(5)[FF] following [1A]		
	CP JR CALL CP JR	3 Z,TRD1 CIN OFFH Z,IDB1	; IF Z=TRUE; [FF][3C][E6] PATTERN FOUND SO GO GET DATA [DD] ; GET CASSETTE DATA IN REG "A" ; LEADER [FF]		
	CP JR	03CH Z,IDB2	START BYTE [3C]		
	CP JR	OÉGH Z,IDB3	SYNC BYTE [E6]		
	LD JR	C,0 TRDO	RESET "C" TO 0 TRY AGAIN TO FIND PATTERN		
IDB1:	LD 1P	C,1 TRD0			
IDB2:	LD JP	C,2 TRD0			
IDB3:	LD JP	C,3 TRD0			
TRD1:	LD CALL	C,0 CIN	; TO GET HERE, THE PATTERN [FF][3C][E6] WAS FOUND"C"=3 ; RESET "C" TO 0		
	PUSH CP	HL 01AH	; PUSH [DATA] ONTO HL ; FOUND [1A], COULD BE A STOP BYTE		
	JR CP JR JP	Z,IDB4 OFFH Z,IDB5 TRD2	FOUND [FF], COULD BE "END OF RECORD"		
; IDB4:	LD	С,4	; [1A] FLAG ? ; [DATA]=[DATA1] AND IS IN HL		
	JP	(TRD1+1)	GET NEXT DATA BYTE		
IDB5:	LD CP 1P	A,C 4	; [1A][FF] FLAG ?		
	LD	NZ,TRD2 C,5	IF C=4; THEN [1A][FF] IS TRUE AND C=5		
TRD2:	LD CP	A,C 4	; GET C ; IF C=4; [1A] FLAG SET		
;	JR CP JR	z,trd4 5 z,trd5	; IF C=5; [1A][FF] FLAG SET		
trd3:	POP CALL JP	HL DATIN TRD1	; POP [DATA] FROM HL INTO "A" ; [DATA] INSERTED TO MEMORY (HL); HL INCREMENTED; CHKSUM UPDATED ; GO GET MORE DATA		
TRD4:	POP LD POP CALL LD CALL JP	HL C,A HL DATIN A,C DATIN TRD1	; TO GET HERE, END NOT FOUND AND [DATA1]=HL [DATA2]=HL ; "C" IS REUSED AS VARIABLE STORAGE; [DATA2] STORED IN "C" ; POP [DATA1] FROM HL INTO "A" ; [DATA1] INSERTED TO MEMORY (HL); HL INCREMENTED; CHKSUM UPDATED ; RESTORE [DATA2] TO A ; [DATA2] INSERTED TO MEMORY (HL); HL INCREMENTED; CHKSUM UPDATED ; GO GET MORE DATA		
; TRD5:	POP POP CALL LD LD CP JR RET	HL HL CIN C,A A,B C Z,TRD6	; TO GET HERE, "END OF RECORD" FOUND AND [DATA1]=1A, [DATA2]=FF ; STOP BYTE AND FOLLOWING FF ARE DISCARDED ; GET TAPE [CHKSUM] ; REGISTER "C" IS REUSED; STORE TAPE [CHKSUM] = C ; GET CAKCULATED [CHKSUM] = A ; COMPARE TAPE TO CALCULATED CHKSUM ; CHKSUM MATCHEDSHUTDOWN AND RETURN ; CHKSUM DID NOT MATCH, RETURN WITH CP=NZ		
; TRD6:	LD OUT CP RET	A,10H (TARBL),A A,10H	; LOAD 10H TO "A" BECAUSE WE WANT TO RESET THE INTERFACE & STOP THE CASSETTE MOTOR ; WRITE 10H TO THE STATUS PORT (6EH) MSB[X,X,TXRDY,RXRDY, 0,0,0,D0]LSB ; SET Z FLAG		
; CIN:	IN AND JR IN RET	A,(TARBL) 01h NZ,CIN A,(TARBL+1)	: READ STATUS PORT (6EH) MSB[0,0,0,1, 0,0,0,1]LSB RDY=MSB[0,0,0,0, 0,0,0,1]LSB =01H ; 01H=[0,0,0,0, 0,0,0,1]IF RXRDY=0 AND D0=0 CASSETTE MTR=ON, RXRDY=0=RDY TO RECEIVE ; LOOP WAITING FOR RXRDY=0 ; LOAD DATA WORD FROM DATA PORT (6FH)		
; DATIN:	INC LD ADD LD RET	HL (HL),A A,B B,A	; LOAD DATA INTO MEMORY, CHKSUM, AND INCREMENT HL		
TUNE:	LD OUT	A,11H (TARBL),A	; ROUTINE TO ALLOW FOR ADJUSTMENT OF TAPE PLAYER VOLUME CONTROL-NEED SYNC STREAM TAPE AS INPUT ; LOAD 11H TO "A" BECAUSE WE WANT TO RESET THE INTERFACE & START THE CASSETTE MOTOR ; WRITE 11H TO THE STATUS PORT (GEH) MSB[X,X,TROY,RXRDY, 0,0,0,0]LSB		

TUN0:	CALL LD CALL LD CALL	CLRSCN B,30 HOME HL,MSG16 MARO	: MSB[0,0,0,1, 0,0,0,1]LSB = 11H : CLEAR THE CONSOLE : B IS A LINE COUNTER TO PRINT 30 LINES TO THE CONSOLE : MOVE CURSOR TO UPPER TOP LEFT OF SCREEN : B IS A LINE COUNTER TO PRINT 30 LINES TO CONSOLE : LOAD A "SYNC STREAM TAPE" AND OBSERVE DISPLAY "+" ADJUST THE TAPE PLAYER VOLUME TO ONLY DISPLAY "+"		
T (1)1	CALL	SPACE	; ADJUST THE TAPE PLAYER VOLUME TO ONLY DISPLAY "+"		
TUN1:	CALL LD	CRLF H,40	; SEND CRLF TO CONSOLE ; LOAD COUNTER TO 40; PRINTS 40 "+" OR "\$" TO CONSOLE = 1 LINE		
TUN2:	CALL CP	CIN OFFH	; INPUT TAPE DATA ; IS DATA [FF]; IF IT IS, Z=TRUE		
	JR LD	Z,TUN2 L,'+'	; DATA IS LEADER, TRY AGAINOHERWISE CONTINUE BELOW ; L="+"		
	CP JR	0E6H Z,TUN3 L,'\$'	; IS DATA [E6] THE SYNC BYTEIF SO, Z=TRUE ; IF FOUND [E6] GOTO TUN3(L="+" GOOD/L="\$"BAD)		
TUN3:	LD LD	A,L	; L="\$"		
	CALL DEC	CONOUT H	; SEND L TO CONSOLE ; DECREMENT COUNTER H		
	JR DEC	В	; IF H=0, START ALL OVER AGAIN		
	JR JP	NZ,TUN1 TUNO			
;		;	ROUTINE TO SAVE A BLOCK OF MEMORY TO THE TARBELL TAPE		
TSAVE:	LD CALL	HL,MSG12 MARQ	; FORMAT: [FF][FF][FF][3C][E6][DD][DD][DD][DD][1A][FF][CHKSUM][FF][FF][FF] ; MESSAGE PROMPT FOR START/END MEMORY ADDRESS INPUT		
	CALL CALL	DHXIN TWRIT	; GET STARTING MEMORY ADDRESSXXXX,YYYY <cr> HL=(START ADDR), DE=(END ADDR) ; THE "TAPE WRITE" ROUTINE</cr>		
;	JP	EXEC3			
TWRIT:	LD OUT	A,21H (TARBL),A	: MSB[X,X,TXRDY,RXRDY, X,X,X,D0]LSB 21H=[X,X,1,0, 0,0,0,1]SET TXRDY=1 AND D0=1MTR ON WRITE TO STATUS PORT (GEH), THIS SHOULD RESET THE TARBELL TXRDY TO NOT RDY AND START THE MTR ; STORE HL, ON THE STACK (START ADDR)		
	PUSH LD	HL, OFFFFH ;	; LOAD DELAY SEED		
THE LEADER	CALL	DELAY ;	; WAIT A BIT, THIS ASSUMES WITH NO DIRECT OUTPUT, THE TARBELL WRITES [FF][FF][FF] TO TAPE AS		
	POP SUB	HL A	; LEADER IS FINISHED, RECOVER HL , AFTER "DELAY", REG "A" SHOULD CONTAIN (00)"A" SUB "A" = 0 ; LOAD THE CHCKSUM "B" WITH (00) ; LOAD "A" WITH THE START BYTE (3CH)		
	LD LD	в,А А,03CH	; LOAD THE CHCKSUM "B" WITH (00) ; LOAD "A" WITH THE START BYTE (3CH)		
	CALL LD	A,0E6H	; WRITE [SC] TO THE TAPE ; LOAD "A" WITH THE SYNC BYTE (E6H)		
	CALL DEC	COUT ; HL	; WRITE [E6] TO THE TAPE		
TWRT1:	INC LD	A,(HL) ;	; DECREMENT THE STARTING BLOCK OF MEMORY ADDRESS STORED IN HL ; LOAD REG "A" WITH THE BYTE OF MEMORY IN LOCATION (HL)		
	CALL ADD	COUT A,B	WRITE [(HL)] TO TAPE ; ADD "A" + CHKSUM		
	LD CALL	B,A CMPDH	; STORE RESULT TO CHKSUM ; COMPARE START ADDRESS TO END ADDRESS		
	JR LD	NC,TWRT1 A,01AH	; IF NC=TRUE, KEEP SENDING MEMORY BYTES TO TAPE ; LOAD "A" WITH FIRST PART OF STOP BYTE (1AH)		
	CALL LD	COUT A,OFFH	WRITE [1A] TO TAPE , LOAD "A" WITH SECOND PART OF STOP BYTE (FFH)		
	CALL LD	COUT A,B	WRITE [FF] TO TAPE ; LOAD REG "A" WITH THE CHECKSUM VALUE		
	CALL LD	COUT A,21H	; WRITE [CHKSUM] TO TAPE ; AGAIN SET TXRDY=1 AND D0=1		
RUNNING	OUT	(TARBL),A	; WRITE TO STATUS PORT (6EH), THIS SHOULD RESET THE TARBELL TXRDY TO NOT RDY AND KEEP MTR		
	LD CALL	HL,07FFFH ; LOAD DELAY DELAY ;	SEEDSHORTER THAN STARTING LEADER ; WAIT A BIT, THIS ASSUMES WITH NO DIRECT OUTPUT, THE TARBELL WRITES [FF][FF][FF] TO TAPE AS		
THE LEADER	LD OUT	A,00H (TARBL),A	; MSB[X,X,TXRDY,RXRDY, X,X,X,D0]LSB 00H=[X,X,0,0, 0,0,0,0]SET TXRDY=0 AND D0=0MTR OFF ; WRITE [0,0,0,0, 0,0,0,0] TO STATUS PORT; (TURN OFF CASSETTE MTR) AND SET RXRDY=TXRDY=0		
	CALL	CRLF			
	CALL	HL,MSG19 MARQ	; LOAD MESSAGE "END " ; DISPLAY MESSAGE		
; COUT:	PUSH	AF	; STORE BYTE TO BE WRITTEN TO TAPE IN AF		
	IN	A, (TARBL) 20H	READ STATUS PORT (6EH) ; MSB[X,X,TXRDY,RXRDY, X,X,X,X]LSB 20H=[X,X,1,0, 0,0,0,0]IF TXRDY=1 NOT RDY TO TRANSMIT		
	JR POP	NZ,COUT+1 AF	; TARBEL RDY TO TRANSMIT; POP DATA BYTE FROM AF		
	OUT RET	(TARBL+1),A	WRITE [DATA] TO TAPE		
; STRM:	LD	HL,MSG17 ;	; STREAM ROUTINE-GENERATES A SERIES OF "FFH" & "E6H"[FF][FF][FF][E6][E6][E6][E6][E6][E6][
	CALL LD	MARQ B,1EH	START THE ROUTINE AND RECORD THE OUTPUT TO CASSETTE TAPE THIS WILL CREATE A "SYNC STREAM TAPE" USED TO CALIBRATE THE TAPE VOLUME		
	LD OUT	A,11H (TARBL),A	; MSB[X,X,TXRDY,RXRDY, X,X,X,X]LSB 11H=[X,X,1,0, 0,0,0,1]IF TXRDY=1 NOT RDY TO TRANSMIT ; SEND TO STATUS PORT (6EH) TO RESET TARBELL AND START TAPE RECORDER MOTOR		
STRM1:	LD CALL	A, OFFH COUT	; WRITE [FF] TO TAPE		
	DEC JR	B NZ,STRM1	; DECREMENT COUNTER B ; IF NOT ZERO, CONTINUE WRITING LEADER		
STRM2:	LD CALL	A,0E6H COUT ;	; WRITE [E6] TO TAPE		
;	JR	STRM2 ;	; CONTINUE UNTIL TAPE RECORDER IS SHUT OFF		
;	ENDIF		; TARBELL TAPE ====================================		
;					
VERIFY:	LD CALL CALL	HL,MSG18 MARQ TRPIN	; VERIFY ORIGINAL MEMORY BLOCK TO COPIED/MOVED MEMORY BLOCK ; IF MISMATCH, PRINT <orig addr=""> <orig data=""> <copy data="" move=""> TO CONSOLE ; CALL TRIPLE INPUTX,Y,Z WHERE X=START ORG(HL), Y=END ORG(DE), Z=START MOVE/COPY BLOCK(BC)</copy></orig></orig>		
	EX	DE,HL	; CALL INIPLE INPUTX,Y,Z WHERE X=START UNG(HL), Y=END UNG(DE), Z=START MUVE/CUPY BLUCK(BC)		
VPEV1 -	DEC	HL BC			
VRFY1:	INC	BC ;	; INCREMENT ORIGINAL STARTING ADDRESS HL ; INCREMENT COPIED/MOVED STARTING ADDRESS BC		
	LD CP	A, (BC) (HL)	; LOAD "A" WITH COPY MEMORY DATA (BC) ; CP (BC) TO (HL); IF (BC)=(HL) Z=TRUE		
	JR CALL	Z,VRFY2 CRLF	(BC) AND (HL) MATCH, ALL IS GOOD SO CONTINUE CHECKING (BC) \Leftrightarrow (HL), ERROR EXISTS; PRINT CRLF TO CONSOLE		
	CALL CALL LD	DHXOT SPACE	; SEND CURRENT HL VALUE TO CONSOLEORIG MEMORY ADDRESS ; SEND SPACE TO CONSOLE ; LOAD "A" WITH (HL) LOCATION CONTENTS		
	CALL	A, (HL) HEXOUT SPACE	· SEND HEX VALUE (HL) TO CONSOLE		
	CALL LD	SPACE A, (BC)	SEND SPACE TO CONSOLE LOAD "A" WITH (BC) LOCATION CONTENTS SEND HEX VALUE (BC) TO CONSOLE		
VRFY2:	CALL CALL	HEXOUT CMPDH	; COMPARE START HL TO END ADDRESS DE		
	JR JP	NC,VRFY1 EXEC3	; IF START ↔ END KEEP CHECKING ; ALL DONE		
; DELAX:	FY		; DELAY USES SEED STORED IN HL AS A BASIS FOR TIME DELAY		
DELAY:	EX EX DEC	(SP),HL (SP),HL HL	; WASTE TIME FOR DELAY ; WASTE TIME FOR DELAY ; DECREMENT SEED IN Hexample 20000=HL=[4E][20]DEC HL=[4E][1F]		
	LD OR	A,L	, DECREMENT SEED IN HLexample Le[IF] REGISTER "H" AS IN HLexample L=[IF] ; REGISTER "H" AS IN HLexample H=[4E]		
	JR RET		; KEEP DECREMENTING UNTIL HL=[00][00]		
; CMPDH:	PUSH	AF ;	; COMPARE 'D' TO 'H'H[XX XX]L AND D[XX XX]E		

	LD CP JP LD CP JP	A,D H NZ,CMP1 A,E L NZ,CMP1	; IF D \Leftrightarrow H THEN GOTO CMP1, [CLEAR CARRY] AND RETURN
	JP POP SCF	NZ,CMP1 AF	; IF E ↔ H THEN GOTO CMP1, [CLEAR CARRY] AND RETURN ; H=D AND L=E [SET CARRY] AND RETURN
CMP1:	RET POP SCF CCF RET	AF	; POP WHAT WAS SAVED IN AF ; SET CARRY FLAG ; CLEAR CARRY FLAG
; DHXIN:	CALL PUSH CP CALL EX POP RET	SPHIN HL ODH NZ,HEXIN DE,HL HL	; OUTPUT A SPACE AND GET SOME CONSOL INPUT ; PUSH 'HL' ONTO THE STACK ; COMPARESUBTRACT <reg a=""> - <0D> = NZIS IT '0DH' A <carriage rtn=""> ; IF 'NOT ZERO' NOT <cr> GO GET MORE ; <cr> DETECTED SO EXCHANGE THE 'DE' AND 'HL' REGISTERS</cr></cr></carriage></reg>
			THIS IS THE MAIN "PARAMETER-GETTING" ROUTINE. THIS ROUTINE WILL ABORT ON A NON-HEX CHARACTER. IT TAKES THE MOST RECENTELY TYPED FOUR VALID HEX CHARACTERS, AND PLACES THEM UP ON THE STACK. (AS ONE 16 BIT VALUE, CONTAINED IN TWO 8-BIT BYTES.) IF A CARRIAGE RETURN IS ENTERED, IT WILL PLACE THE VALUE OF "0000" IN THE STACK.
SPHIN:	CALL CALL	SPACE SPACE	; LOAD 'A' WITH 20H 'SPACE' AND SEND TO CONSOLE OUTPUT
HEXIN: HXIN1:	CALL LD CALL CP RET CP RET CP JP	SPACE HL_0 CONIN '0' M 'F'+1 P '9'+1 M.HXIN2	; LOAD HL WITH '0'THIS ROUTINE IS FOR HEX INPUT, SO REJECTS ANYTHING ELSE ; GET CONSOL INPUT AND RETURN IN 'REG A' CAN BE '00H TO 7FH' ; COMPAREsubtract <reg a=""> - <0> = MIF NOT '0' OR LARGER RETURN ; IF 'SIGN NEG' RETURN ; COMPAREsubtract <reg a=""> - <f'+1> = PIF IT IS LARGER THAN 'F' IE NOT HEX RET ; IF 'SIGN POS' ; COMPAREsubtract <reg a=""> - <9 + 1> = MIF IT IS LARGER THAN '9' ; IF 'SIGN NEG' GOTO HIN2</reg></f'+1></reg></reg>
	CP RET	M,HXIN2 'A' M	: COMPAREsubtract <reg a=""> - <a> = MIF IT IS NOT 'A' THEN RETURN : IF 'SIGN NEG'</reg>
HXIN2:	ADC AND ADD	А,9 ОГН НL,НL	; ADD "A" + 9 + "CARRY FLAG 0 OR 1" ; MULTIPLY BY 16
	ADD ADD ADD	HL,HL HL,HL	
	OR LD	HL,HL L L,A	; 'OR' IN THE SINGLE NIBBLE
;	JR	HXIN1	; GET SOME MORE FROM CONSOL IN
TRPIN:	CALL EX CALL PUSH CALL PUSH POP POP	SPHIN DE,HL HEXIN HL HEXIN HL BC HL	; TRPIN: INPUT 3 BYTESPLACE IN [HL],[DE],[BC]ex: (hhll),(ddee),(bbcc) <cr> ; ECHANGE THE DE AND HL REGISTERS - LOAD ALL THREE PAIRS WITH HEX ; ENTRIES</cr>
; DHXOT:	RET LD CALL LD	A,H HEXOUT A,L	; DISPLAY CURRENT HL VALUE
; HEXOUT:	PUSH RRCA RRCA RRCA RRCA	AF	
нхот1:	CALL POP AND ADD CP JP ADD	HXOT1 AF OFH A,30H M,CONOUT A,7 CONOUT	
; CRLF:	JP PUSH LD CALL LD CALL POP RET	CONOUT AF A, ODH CONOUT A, OAH CONOUT AF	
; SPACE:	PUSH LD CALL POP RET	AF A,20H CONOUT AF	; PUSH CONTENTS OF AF ONTO THE STACK ; A IS LOADED WITH 20H = 'SPACE' ; A 'SPACE' IS SENT TO THE CONSOL OUTPUT ; POP FROM THE STACK BACK TO AF
; CLRSCN:			; ROUTINE TO CLEAR THE CONSOLE SCREEN AND HOME TO UPPER LEFT CORNER VT-100 'ESC' COMMANDSCLR_SCRN='ESC'[2] HOME='ESC'[H
; CLEAR: CALL	DEFB DEFB LD MARQ	1вн,5вн,32н,4ан ОЗН HL,CLEAR	; ESC=1BH [=5BH 2=32H J=4AH ; O3H=END OF TEXT
; HOME:	DEFB	1вн,5вн,48н ; ESC=10	вн [=5вн н=48н
CALL	DEFB LD MARQ RET	03H HL,HOME	; O3H=END OF TEXT
; MARQ: MAR2:	LD CALL INC	A, (HL) CONOUT HL	; MARQUEE ROUTINE TO SEND MESSAGE IN (HL) TO CONSOLE SCREEN
	CP JP RET	03H NZ,MAR2	; LOOKING FOR "03H" TO INDICATE END OF MESSAGE
; CONOUT:			; ROUTINE FOR CONSOLE OUTPUT TO DISPLAY
CONO1:	PUSH IN	AF A, (KBDST)	; ROUTINE FOR CONSOLE OUTPUT TO DISPLAY ; STORE CONTENTS OF 'A' REGISTER "OUTPUT CHARACTER" IN 'AF' REGISTER PAIR ; LOAD STATUS PORT INTO 'A' STATUS PORT-MSB[0][0][0][0][0][0][0][0]LSB MEANS DISPLAY BUSY STATUS PORT-MSB[0][0][0][0][0][0][0][0][0][0][0][0] ; 'AND' REGISTER 'A' WITH 04H=MSB[0][0][0][0][0][0][0][0][0][0]LSB
	AND JR JR	A, (KBDOT) NZ, CONO2 CONO1	; 'AND' REGISTER 'A' WITH 04H=MSB[0][0][0][0][0][1][0][0]LSB ; IF RESULT IS NOT-ZERO, JUMP OUT OF LOOP TO CONO2
CONO2:	JR POP OUT	CONO1 AF (KBDDT),A	; RESTORE "OUTPUT CHARACTER" TO REGISTER 'A' ; SEND "OUTPUT" TO (KBDDT)
;	RET	(1000.),0	

CONIN:	IN	A,(KBDST)	: ROUTINE FOR CONSOLE INPUT FROM KEYBOARD : STATUS PORT=WSB[0][0][0][0][0][0][0][0][1][0]LSB MEANS NO CHARACTER WAITING STATUS PORT=WSB[0][0][0][0][0][1][0]LSB MEANS CHARACTER IS WAITING : AND REGISTER · A WITH 02H=MSB[0][0][0][0][0][0][0][0][1][0]LSB
CONI1:	AND JP JP IN	A,(KBDIN) NZ,CONI1 CONIN A,(KBDDT)	; 'AND' REGISTER ^T A ^T WITH ÖZH -M ŚB[Ö][Ö][Ö][O][O][O][O][I][O]LSB ; IF RESULT IS NOT-ZERO, JUMP OUT OF LOOP TO CONIL ; RESULT IS ZERO, SO GO BACK AND CHECK STATUS PORT AGAIN ; INPUT FROM DATA PORT OLH FOR PROPELLER CONSOLE ; CODE BELOW FILTERS INPUT AND RETURNS
NOT ON KE	AND CP YBOARD	7ғн 61н	; ASCII RANGE ODH-7FH COVERS ALL 128 CHARACTERS; PASSES ALL ASCII UP TO 7FH, THEN 'A'= 0,1,2 ; 61H-7FH ARE LOWER CASE LETTERS; ASCII (00H-61H)=C;ASCII (62H-7FH)=NC;ASCII (80H-FFH)=C BUT
	JP CP JP SUB	C,ECHO 7CH NC,ECHO 20H	; SENDS ASCII(00H-60H) TO OUTPUT CONSOLE DISPLAY; NOTE-CARRY SET IF NEG OR GREATER THAN FF ; ONLY ASCII(61H-7FH) REMAIN; FILTER OUT ASCII < 7CH ; SENDS ASCII(7DH-7FH) TO OUTPUT CONSOLE DISPLAY ONLY ASCII(61H-7CH) REMAIN ; ONLY ASCII(41H-5CH) REMAINIE(A TO \) WHICH GO TO CONSOLE DISPLAY
ECHO:	CP JP JR	18H Z,EXEC4 CONOUT	: 18H='CAN' OR CANCEL ; FF 'A' IS 'CAN' RETURN WITH NO ACTION ; SEND 'A' TO CONSOLE OUTPUT DISPLAY
Ρ́ΤΧΤ:	LD CP RET CALL INC JR	A, (HL) 03H Z CONOUT HL PTXT	; PRINT A MESSAGE ; IF [03H], THEN END AND RETURN
нхот4:	LD CALL LD	С,Н НХО2 С,L	; 16 HEX OUTPUT ROUTINE
нхо2:	LD RRA RRA RRA RRA CALL	A,C HX03	
нхо3:	LD AND CP JP ADD	A,C OFH 10 C,HADJ A,7	
HADJ: OTA:	ADD PUSH LD	А,30Н ВС С,А	
:	CALL POP RET	CÓNOUT BC	; SEND TO CONSOL WHAT'S IN REGISTER A
; HLSP:	PUSH PUSH CALL LD CALL	HL BC LADR A, 20H CONOUT	PRINT [HL] AND A SPACE
:	POP POP RET	BC HL	
; LADR:	LD CALL	A,H LBYTE	PRINT [HL] ON CONSOL
LBYTE:	LD PUSH RRCA RRCA RRCA RRCA	A,L AF	: STORE "H" IN "AF" MSB[X000 000]LSB = MSB[0X00 0000]LSB MSB[0X00 000]LSB = MSB[00X0 0000]LSB MSB[00X0 000]LSB = MSB[000X 0000]LSB MSB[00X0 000]LSB = MSB[000X 0000]LSB
SF598:	CALL POP CALL LD JP	SF598 AF CONV A, C CONOUT	; RESTORE "H" FROM "AF"
CONV:	AND ADD	ОГН А,90Н	CONVERT HEX TO ASCII
	DAA ADC DAA LD RET	а,40н С,А	
; BITS1:	PUSH PUSH LD	DE BC E,A	; DISPLAY 8 BITS OF [A]
	CALL POP POP RET	BITS BC DE	
BITS: SF76E:	LD CALL SLA	B,08H SPACE E	; DISPLAY 8 BITS OF [E]
	LD ADC LD CALL DJNZ RET	A,18H A,A C,A CONOUT SF76E	
; BAD:	PUSH PUSH LD CALL POP POP RET	AF HL HL,MSG11 MARQ HL AF	; PRINT BAD ; SAVE ORIGINAL 'AF' AND 'HL' ; PRINT 'BAD: ' TO CONSOL ; PRINT MAQUEE ROUTINE ; RESTORE HL ; RESTORE AF
; BOOT:	LD CALL	HL,MSG22 MARQ	; OUTPUT MESSAGE ; OUTPUT TO CONSOLE
,			; THIS ROUTINE CAN ACCESS THE FLOPPY DISK CONTROLLER'S SIX I/O PORTS STARTING AT F8H IT CAN BE USED TO CREATE CBOOT CODE IN MEMORY AT LOCATION (007D)H THIS CODE SEEMS TO WORK ON WESTERN DIGITAL FD-1771 CONTROLLERS BUT MAYBE NOT LATER ONES AS THE PORT VALUES MAY HAVE BEEN CHANGED.
			(D6FAH)-OUT DISK COMMAND PORT (D6FAH)-IN DISK STATUS PORT (D6FAH)-I/O SECTOR REGISTER PORT (D6FAH)-I/O SECTOR REGISTER PORT (D6FAH)-I/O DATA PORT OPAT (D6FAH)-I/O DATA PORT OPAT (D6FCH)-IN DISK WAIT PORT (MDV/PRDY) (D6FCH)-OUT DISK DEXTEMDED COMMAND PORT
;			THE CODE APPEARS VERY SIMILAR TO THE BOOT LOADER FOR TARBELL 1011D (FD-1771) CONTROLLER IT'S PURPOSE IS TO READ THE FIRST SECTOR OF TRACK 0 INTO MEMORY AT 0000H, AND THEN EXECUTE IT
-	IN XOR	A,(WAIT) A	; WAIT FOR HOME ; COMPLETE

	LD	L,A	; SET L=0
	LD	H,A	; H=0; L=0
	INC	A	: SET A=1
	OUT	(SECT),A	SECTOR=1
	LD	A.8CH	READ SECTOR
	OUT	(DCOM),A	
RLOOP:	IN	A, (WAIT)	; WAIT FOR DRQ OR INTRQ
	OR	A	; SET FLAGS
	JP	P, RDONE	; DONE IF INTRQ
	IN	A, (DDATA)	; READ A BYTE OF DATA
	LD	(HL),A	; LOAD IT INTO MEMORY
	INC	HL	INCREMENT MEMORY POINTER
	JP	RLOOP	; DO IT AGAIN
RDONE:	IN	A, (DSTAT)	; READ DISK STATUS
	OR	A	; SET FLAGS
	JP	Z,SBOOT	; IF ZERO, GO TO SBOOT AT 007DH
	HALT		; DISK ERROR, SO HALT
;			
	END		