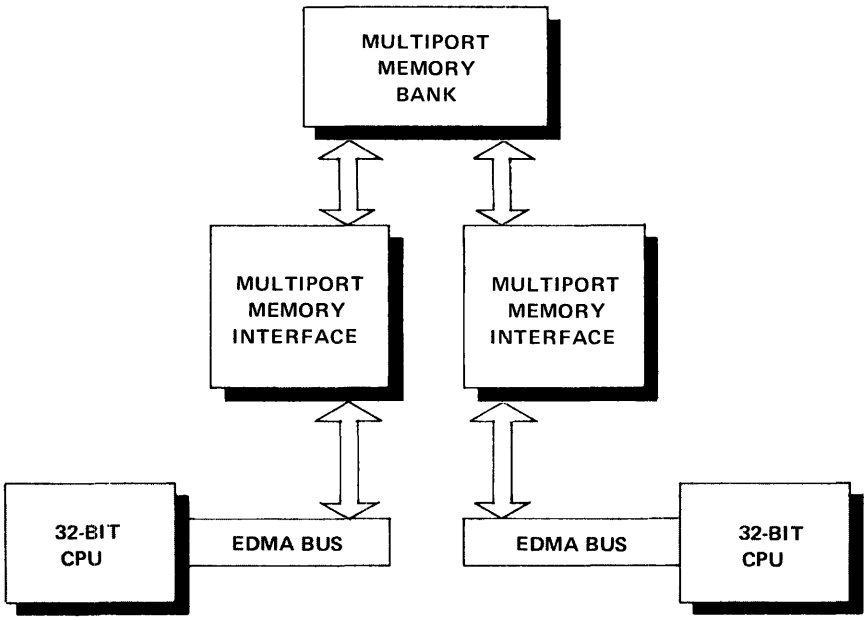
INTERDATA

PROCESSOR ENHANCEMENTS



Multiport Memory System

PRODUCT DESCRIPTION

Interdata's Multiport Memory System components provide a highly modular method of implementing small and large shared memory configurations to satisfy both the simplest and most complex multiprocessor applications.

The Multiport Memory System (MMS) is Interdata's way of sharing memory. MMS allows up to fourteen 32-bit Central Processing Units (CPU's) to share a common memory. Each CPU has direct access to a total of one million bytes (1MB) of shared plus local memory. Any Interdata 32-bit processor can access MMS by using a Multiport Memory Interface (MMI) on the Extended Direct Memory Access (EDMA) bus.

The Multiport Memory System is a multi-bank, multi-port, multi-bus system. It can achieve aggregate throughputs in excess of 20 megabytes per second in a fully expanded configuration where one megabyte of memory is distributed across an eight-bank multiport system.

Interdata's Shared Memory concept allows each processor in a multi-processor configuration to share common memory and to access its local memory for instructions and data unique to its primary task.

The Interdata 32-bit processors along with Multiport Memory open whole new vistas to users who can now divide and conquer large and complex application problems. No other method is as simple for coupling multiple computers together.

Bit serial communications, asynchronous or synchronous, are slow and impose a large overhead, both for operating system usage and communications handshaking. It is not unusual to chew up as much as 60% of the processor time in overhead. Special parallel interfaces are fast, but they also expend a large overhead to send, receive, pack and move data to its final memory destination. Traditional methods of communication produce slow total system response times. (Response time is the time a processor system takes to "see" an event, analyze it and output a response.) In most applications, system response time is a critical element.

FEATURES

- One Megabyte of Sharable Memory
- Eight Memory Banks per Multiport System
- Fourteen Access Ports per Bank
- Hardware Write Protect on 1KB Boundaries
- Sequential or Fixed Access Service Priority
- Immediate or Deferred Response Selection
- Power Fail Detection
- Twenty Megabyte Aggregate Throughput

FUNCTIONAL DESCRIPTION

A Multiport Memory System consists of two major sections: the Multiport Memory Bank (MMB) and a Multiport Memory Interface (MMI) board. The Interface is physically and electrically located between the Extended Direct Memory Access (EDMA) bus and the MMB; it acts as a buffer and allows the EDMA bus to access up to eight memory banks. Each bank operates asynchronously, all can actively service processors (or other devices) simultaneously. Each processor or special I/O device requires a multiport memory interface to gain access to a multiport memory bank.

A memory bank consists of one or two 7-inch multiport memory chassis. The actual number of chassis depends on the number of multiport memory multiplexors and/or the amount of memory in the bank. The total amount of memory in a multiport memory system that can be shared is determined by the processor in the system with the largest complement of local memory. For example: If one CPU in a three-CPU system has 256KB of local memory and the second and third CPU's each have 128KB of local memory, the total shared memory can be 744 KB (1 MB – 256 KB = 744 KB). The first CPU imposes the limitation.

A minimum memory bank system requires the following components:

- Chassis
- Power Supply
- Multiport Memory Controller (MMC)
- Multiport Memory Multiplexor (MMM)
- 32KB or 64KB Memory Module

Each bank requires one multiport memory controller. Each processor or private EDMA bus that accesses the memory system requires one Multiport Memory Interface (MMI).

The memory system is housed in one or more forced air-cooled cabinets. The memory system can be physically extended from the processor by 50-foot memory bus cables.

A fully expanded memory bank includes the following components:

- 2 Chassis
- 2 Power Supplies
- 1 MMC
- 7 MMM's (to support 14 processors)
- 512KB of Memory (64KB modules)

SYSTEM ARCHITECTURE

A typical two-processor Multiport Memory System is shown in Figure 1. Each processor accesses a multiplexor port through an interface board. A memory bank system can support up to seven multiport memory multiplexors, a memory control board, and up to eight 32KB or 64KB memory modules. Each interface board has two port buses, but only one is used in this example. (The second bus can be used to access a second memory bank.)

The MMI accepts the memory address and data from a processor's EDMA bus. The interface interprets the address and generates a bank select code to identify the bank containing the address. The memory address and data are then presented to the selected bank. Immediate or deferred access is optional. Deferred access is elected for an interface that supports a low-priority access device. The deferred response allows other EDMA activity while MMI is waiting for memory access.

The MMI can generate one or two memory bank port buses: one for the odd half-word and one for the even half-word when two buses are used. The MMI can generate a private EDMA bus. The private EDMA bus with seven ports allows the user to interface special high-speed devices with direct access to multiport memory, i.e., array processor or high-speed graphics device.

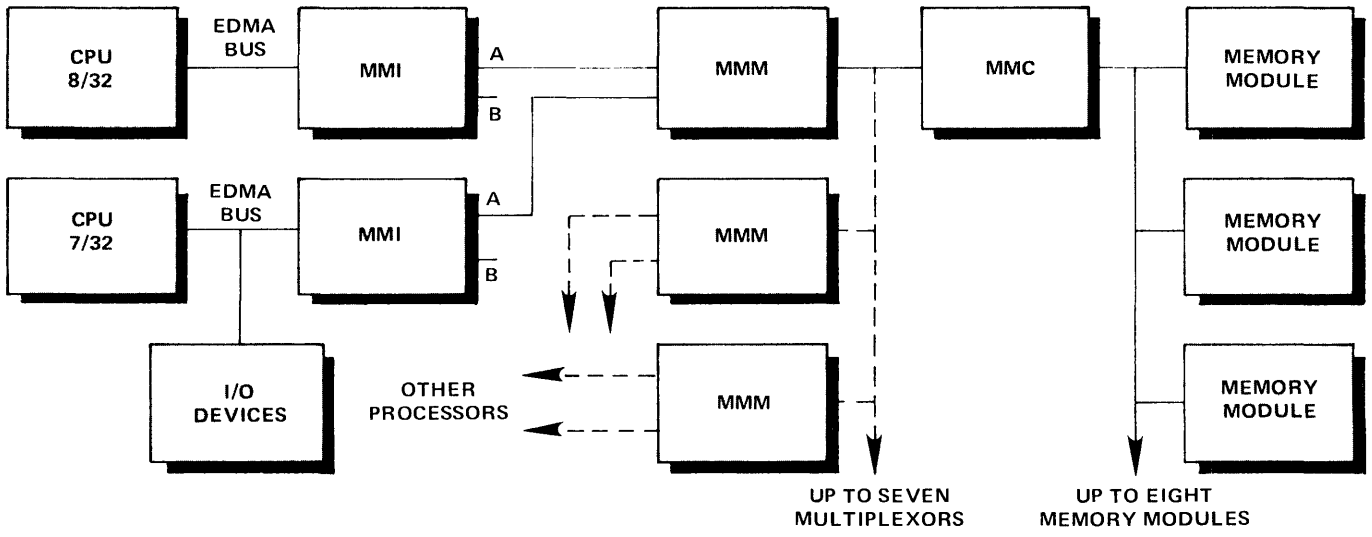


FIGURE 1. TYPICAL MULTIPORT MEMORY SYSTEM CONFIGURATION.

The MMM is a 2:1 multiplexor that resolves contention between the two access ports. It also recognizes the bank select code and communicates with two MMI port buses. The hardware write protect feature is implemented on the MMM using a pair of programmable read only memory (PROM) chips, one for each port.

The MMC controls access to memory and resolves contention among access requests from up to seven multiplexors. Fixed or sequential access priority is implemented by strap options on the MMC. Once a request is accepted, the controller manages all communications to and from the selected multiplexor. In addition, the MMC initiates the memory cycle and generates memory control and timing signals to provide a completely autonomous operation within each memory bank.

A maximum of eight 32KB or 64KB memory modules can be driven by each controller. Power fail detection is included in the MMC. In the event the power drops below a preset level, the drop is sensed by the controller and all internal sequences are stopped to prevent requests from being honored and data lost.

Figure 2 depicts two processors accessing four memory banks; each port of every interface accesses two banks. Again the total memory capacity for each processor is 1MB.

Using both interface ports to access memory allows the A port to access the even half-word and the B port to access the odd half-word. This allows higher transfer rates for full-word or burst mode operations.

OPERATING CHARACTERISTICS

The Multiport Memory on a processor system is transparent to the high-level language applications programmer. Processors share data through named global common areas located in multiport memory. The "Test and Set" instruction can be used as a user-implemented semaphore or key when accessing shared areas on the assembly language level.

Up to fifteen common areas can be declared under OS/32 MT. The user can declare 14 of the common areas in multiport memory at system generation time. The user identifies common areas with a starting address and number of locations assigned to that area. The operating system of each processor attached to the Multiport Memory system generates the same addresses in global common. The user can exclude any processor from accessing any common area by eliminating that global common address at system generation time. The Hardware Write Protect feature provides a method of establishing sharable Read Only areas or sharable Read/Write privileges for selected processors. Hardware Write Protect can be established on 1KB boundaries. The operating system also supports discontiguous memory segments. The system recognizes the difference between the declared top of local memory and the starting address or the first global common area as a "hole" in memory.

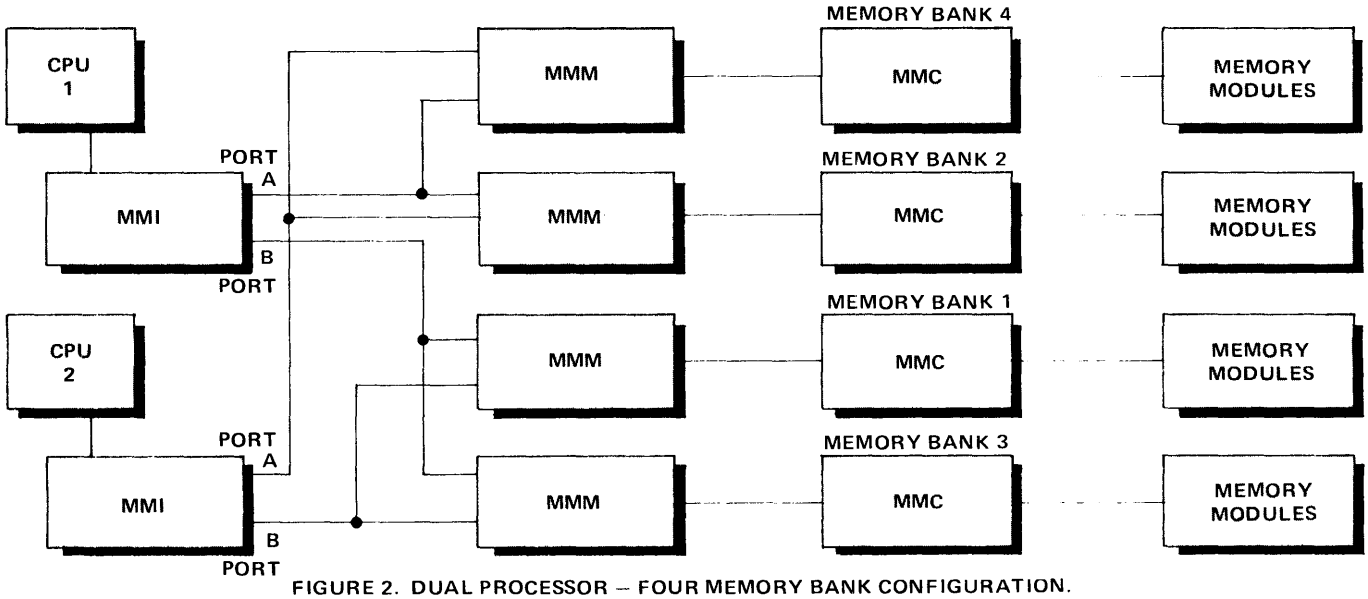


FIGURE 2. DUAL PROCESSOR – FOUR MEMORY BANK CONFIGURATION.

SPECIFICATIONS

Power Requirements

MMI – 5 VDC, 9 ampere
MMM– 5 VDC, 6.2 ampere
MMC – 5 VDC, 3 ampere
Power Supply– 115/230 VAC ± 10%
47-63 Hz
6.5/3.75 amp. max.

Dimensions

MMI – 15" x 15" multiwire board
(38.1 cm x 38.1 cm)
MMM– 15" x 15" multiwire board
(38.1 cm x 38.1 cm)
MMC – 15" x 15" multiwire board
(38.1 cm x 38.1 cm)
MMC chassis – 7" H, 19" W, 19" D
(17.8 cm H, 48.3 cm W, 48.3 cm D)
MMC power supply – 7" H, 19" W, 9" D
(17.8 cm H, 48.3 cm W, 22.9 cm D)

Weight

MMI – 3 pounds (1.5 Kg)
MMM– 3 pounds (1.5 Kg)
MMC – 3 pounds (1.5 Kg)
MMC chassis – 8 pounds (3.6 Kg)
MMC power supply – 31 pounds (14.1 Kg)

Transfer Rates (Maximum)

Half-word Mode – 1.2 MB/sec.
Full-word Mode – 2.4 MB/sec.
Burst Mode – 3.2 MB/sec.

Bank Interleaving Options

No Interleaving
2-Way Interleaving
4-Way Interleaving
8-Way Interleaving

Bus Length

50 Feet Maximum (15.2 meters)

Environmental

Temperature	0 to 50° C
Humidity	0 to 90% (non-condensing)
Storage Temperature	–55° C to +85° C

INTERDATA PRODUCT NUMBERS

M48-025	Multiport Memory Interface with 3-foot cable stubs and terminators.
M48-026	Multiport Memory Controller with power supply, 7-inch chassis and power fail function cable.
M48-027	Multiport Memory Multiplexor with quad 3-foot cable stubs.
M48-033	25-foot extension cable, maximum of two per interface. Extends memory bus between the interface and the memory bank.
M73-301	Memory Expansion Module with parity, 32,768 bytes, 750ns core cycle time.
M71-309	Memory Expansion Module with parity, 65,536 bytes, 1000ns core cycle time.

Related Documents

29-539	Multiport Memory Instruction Manual

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