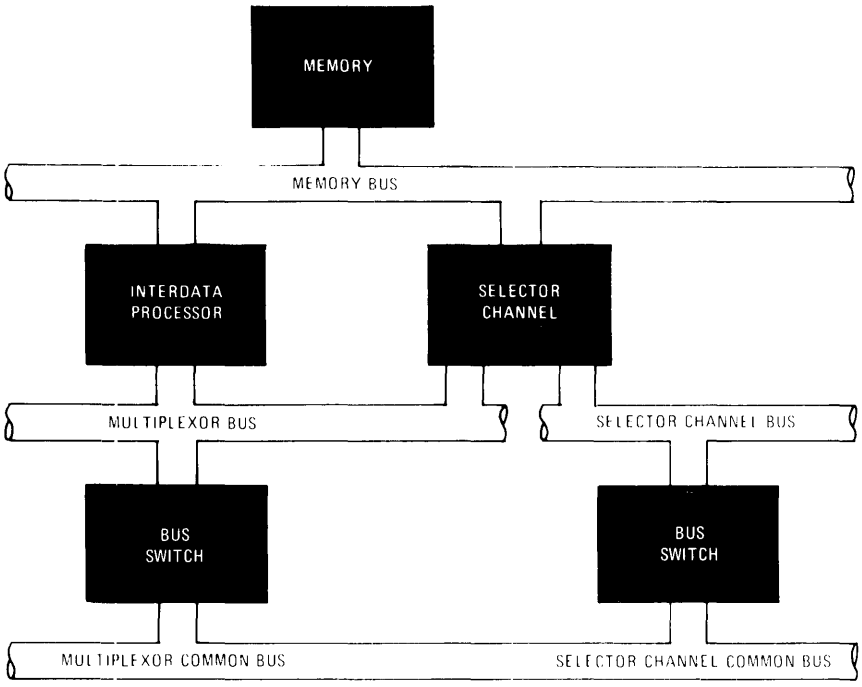
INTERDATA®

PERIPHERALS



I/O Bus Switch

PRODUCT DESCRIPTION

The I/O BUS SWITCH is a convenient and inexpensive means of providing multiple processor access to a common I/O bus or to provide an extension medium to a remotely located bus chassis.

Non-interfering multiport access to the common bus allows only one processor to have unqualified control at any one time, thus preventing simultaneous access. When the switch is employed as a bus extender, all operation is performed in a transparent mode, with programmable features inhibited.

FEATURES

- Multiprocessor Shared Bus Capability
- Up to 10 Bus Loads
- Multiplexor or Selector Channel Operation
- Programmable or Manual Control
- Transparent Extended Bus
- All Solid-State

OPERATIONAL CHARACTERISTICS

There are two 7-inch printed circuit boards in the I/O Bus Switch. One board, the MBS-A, is physically located on the processor side of the switch. The second board, MBS-B, is physically located on the switched bus side of the switch. Complete isolation is built-in to ensure that power failure or switch failure will not result in common bus interference. Light-emitting diodes are incorporated on each switch board to provide a positive visual indication of the selected switch.

When used as a bus extender, total load capability of the I/O Bus Switch common bus is 9 controllers. The addition of I/O Bus Switch (MBS B) cards constitutes one controller load for each switch card interfaced to the common bus.

The common bus is always idle unless a switch has been requested and has been granted bus control. Requests from other switches are registered within the switch for response as soon as the bus is released.

A master-slave option can be implemented, allowing one of the switches in a multiple processor application to assert unqualified control in the system. In the master mode, any request for the bus by the master switch results in de-select of the current user and an immediate seizure of the common bus by the master.

Program control is exercised via a command byte and a status byte. The command and status for the switch does not affect the controllers connected to the common bus.

BIT	0	1	2	3	4	5	6	7
COMMAND	DISABLE	ENABLE			CLEAR REQUEST	SET REQUEST	COMMAND CLEAR	
	DISARM				SET MASTER			

Command Byte Definition

Bit 0 is the Disable bit. When set, this bit prevents a processor interrupt by the switch or the common peripherals. Queuing conditions for peripherals are unaffected. Bit 1 is the Enable bit. When set, this bit permits processor interrupt

When bits 0 and 1 are set, the Disarm condition is activated. In this state, both the switch and peripheral interrupts are blocked. Previously queued switch interrupts are cleared.

Bit 4 is the Clear Request bit. When set, this bit causes the switch to relinquish control of the common bus.

Bit 5 is the Set Request bit. When set, this bit allows a normal bus request to be satisfied when the bus is idle (not under control of another bus switch).

When bits 4 and 5 are set, the set master condition is activated. If the switch has the master option installed, this condition will cause the switch to gain immediate control of the common bus and force a de-select of the previously selected switch.

Bit 6 is the Command clear bit. This bit allows the switch to activate the system clear line of the common bus. In addition, the EOM bit is set during the one-second clear time.

BIT	0	1	2	3	4	5	6	7
STATUS					BUSY		EOM	DU
					BUS BUSY			

Status Byte Definition

Bit 4 is the Busy bit. When this bit is set (set = 1) the switch is not selected (idle condition).

Bit 6 is the End of Medium bit. This bit is used in conjunction with the Busy bit as follows:

EOM = 1 and Busy = 1 signals the common bus is busy.

EOM = 1 and Busy = 0 signals a command clear interval. When operating under Selector channel control, this condition will cause a termination interrupt.

Bit 7 is the Device Unavailable bit. When this bit is set, the switch is not active, e.g.: loss of common bus power or loss of cable contact.

SPECIFICATIONS

Power Requirements

	MBS-A	MBS-B
+5 VDC ± 5%	1 Ampere	0.8 Ampere

Operating Environment

0° - 50° C operational
-40° 85° C storage
5 - 90% humidity (without condensation)

Dimensions

7 x 15-inch Printed Circuit Boards

Weight

8 pounds (2 pounds per printed circuit board)
(2 pounds per 12.5-foot cable)

INTERDATA PRODUCT NUMBERS

Two versions of manual switch control panels are available. Both incorporate positive keylock manual-auto select to prevent accidental manual over-ride intervention of program controlled system switch parameters. The Control Panel requires only 1.75 vertical inches of mounting space in a standard 19 inch rack.

M48-014 Input/Output Bus Switch. Allows a common bus between processors (one Input/Output Bus Switch required per processor sharing a common bus). Includes two 7" boards and interconnecting cables.

M48-017 Extension Cable Kit 25 feet. Provides extension of distance between I/O Bus Switch boards.

M48-018 Manual Control Panel. Allows manual override control for up to six processors sharing a simple common switched bus.

M48-019 Manual Control Panel. Allows manual override control for up to three separate common switched busses by two processors.

Printed in U.S.A.

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3-01065-1