## PERKIN-ELMER

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Product Overview

The Perkin-Elmer I/O Switch is a convenient and inexpensive means of providing multiple processor access to a common I/O bus or to provide an extension medium to a remotely located bus chassis.

Non-interfering multiport access to the common bus allows only one processor to
have unqualified control at any one time, thus preventing simultaneous access. When the switch is employed as a bus extender, all operations are performed in a transparent mode, with programmable features inhibited.

- Programmable or manual control
- Transparent extended bus


## Operational Characteristics

- Multiprocessor shared bus capability
- Up to 15 bus loads on remote bus
- Multiplexor or selector channel operation

Features

There are two 7 -inch $\times 15$-inch printed circuit boards that comprise the I/O Switch set. One board, the IOS-A, is physically located on the processor side of the switch. The second board, IOS-B, is physically located on the switched bus side of the switch. A lightemitting diode is provided to indicate loss of power on the common bus or cable disconnection between the two I/O switch boards. Light-emitting diodes are also incorporated on each switch board to provide a positive visual indication of the "selected" switch.

The new data transfer protocol allows highspeed devices to transfer data to and from memory at distances of 100 feet maximum. The transfer rate under the new protocol is limited by I/O Switch cable lengths as follows:
I/O Switch Halfword Data Transfer Rate Cable Length

| Ft. | Meters | New Protocol | Old Protocol |
| ---: | :---: | :---: | :---: |
| 25 | 7.6 | 1400 | 700 |
| 50 | 15.2 | 1200 | 600 |
| 75 | 22.9 | 1000 | 500 |
| 100 | 30.5 | 800 | 400 |

Operational Characteristics (Continued)

When used as a bus extender, the total load capability of the I/O Bus Switch common bus is 16 controllers. The addition of I/O Switch (IOS-B) card constitutes one controller load for each switch card interfaced to the common bus.
The common bus is always idle unless a switch has been requested and has been granted bus control. Requests from other switches are registered within the switch for response as soon as the bus is released.

A master-slave option can be implemented, allowing one of the switches in a multiple processor application to assert unqualified control in the system. In the master mode, any request for the bus by the master switch results in de-select of the current user and an immediate seizure of the common bus by the master:
Program control is exercised via a command byte and a status byte. The command and status for the switch does not affect the controllers connected to the common bus.

| Bit | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Command | $\underbrace{\text { Disable }}_{\text {Disarm }}$ | Enable |  |  | Clear <br> Request | Set <br> Request | Command <br> Clear |  |

## Command

## Byte

Definition

Bit 8 is the Disable bit. When set, this bit prevents a processor interrupt by the switch or the common peripherals. Queuing conditions for peripherals are unaffected. Bit 9 is the Enable bit. When set, this bit permits processor interrupt.
When bits 8 and 9 are set, the Disarm condition is activated. In this state, both the switch and péripheral interrupts are blocked. Previously queued switch interrupts are cleared.
Bit 12 is the Clear Request bit. When set, this bit causes the switch to relinquish control of the common bus.

Bit 13 is the Set Request bit. When set, this bit allows a normal bus request to be satisfied when the bus is idle (not under control of another bus switch).
When 12 and 13 are set, the Set Master condition is activated. If the switch has the master option installed, this condition will cause the switch to gain immediate control of the common bus and force a de-select of the previously selected switch.
Bit 14 is the Command Clear bit. This bit allows the switch to activate the system clear line of the common bus. In addition, the EOM bit is set during the one-second clear time.

| Bit | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| :--- | :--- | :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Status |  |  |  |  | Busy |  | $\underbrace{\text { EDM }}_{\text {Bus Busy }}$ | DU |
| EOM |  |  |  |  |  |  |  |  |

## Status

Byte
Definition

Bit 12 is the Busy bit. When this bit is set (set $=1$ ) the switch is not selected (idle condition).
Bit 14 is the End of Medium bit. This bit is used in conjunction with the Busy bit as follows:
EOM $=1$ and Busy $=1$ signals the common bus is busy.
EOM $=1$ and Busy $=0$ signals the command clear interval.

When operating under Selector Channel control, this condition will cause a termination interrupt.
Bit 15 is the Device Unavailable bit. When this bit is set, the switch is not active, e.g., loss of common bus power or loss of cable contact.

| Specifications Power Requirements | IOS-A 1 Ampere IOS-B 0.8 Ampere |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Operating Environment | $0^{\circ}$ to $50^{\circ} \mathrm{C}$ operational $-40^{\circ}$ to $85^{\circ} \mathrm{C}$ storage 5 to $90 \%$ humidity (without condensation) |  |  |  |
| Dimensions | $17.8 \times 38.1 \mathrm{~cm}(7 \times 15$-inch) <br> Printed Circuit Boards <br> The Control Panel requires only 4.4 cm (1.75) vertical inches of mounting space in a standard 482.6 mm rack. |  |  |  |
| Weight | 3.6 Kg ( 8 pounds) .9 Kg (2 pounds) per printed circuit board .9 Kg (2 pounds) per 3.8 m (12.5 foot) cable. |  |  |  |
| Product Numbers | M48-055 Input/Output Switch. Allows a common bus between processors (one Switch required per processor sharing a common bus). Includes two 178 mm boards and two 3.8 m interconnecting cables. |  | M48-018 | Manual Control Panel. Allows manual override control for up to six processors sharing a single common system I/O. |
|  |  |  | M48-019 | Manual Control Panel. Allows manual override control for three separate common system I/O's each shared by two processors. |
|  | M48-058 | I/O Switch Extension Cable, 25 feet. Using multiple cables, the I/O Switch can be shared at distances up to 30.5 max. (Transfer rate decreases as distance increases). |  |  |
|  |  |  | M48-064 | I/O Switch Panel ( $1 \times 6$ ). Allows manual override control for up to six processors sharing a single common system I/O. <br> I/O Switch Panel ( $3 \times 2$ ). Allows manual override control for up to three separate systems I/O's each shared by two processors. |
|  | Two versions of manual switch control panels are available. Both incorporate positive keylock manual-auto select to prevent accidental manual override intervention of program-controlled system switch parameters. |  | M48-063 |  |

Related
Documentation

29-616 Maintenance Manual IOS
29-617 IOS Programming Manual

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The information contained herein is intended to be a general description and is subject to change with product enhancement.

