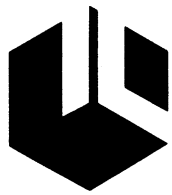


Instrumentation Laboratory

The Pixel 100/AP™ Service Manual

Theory of Operation

THE PIXEL 100/AP SERVICE MANUAL

THE PIXEL 100/AP SERVICE MANUAL

I

THEORY OF OPERATION

Part No. 160451-00 Rev. 0

CONTENTS

FIGURES

Section 1

INTRODUCTION

1.0 GENERAL

The Pixel 100/AP is a general-purpose microcomputer manufactured by the Pixel Division of Instrumentation Laboratory, Inc., One Burtt Road, Andover, Mass. 01801.

The 100/AP is illustrated in Figure 1-1.

Figure 1-1. The Pixel 100/AP

1.1 PHYSICAL DESCRIPTION

The Pixel 100/AP system consists of:

- A computer module,
- One to eight terminals, and
- Various options and peripherals.

They are discussed individually in the sections which follow.

1.1.1 Computer Module

Most of the 100/AP's circuitry is enclosed in a 20" × 21" × 26½" (50.8 × 53.3 × 67.3 cm) metal housing. A card cage mounted inside the housing holds the 10" × 12" (25.4 × 30.5 cm) printed circuit card modules which include the processor and memory boards, controllers for mass storage and I/O, and the power supply. Mass storage devices (diskette and Winchester disk drives) mount underneath the card cage.

The front panel of the computer module contains an on/off switch, power light, and the diskette drive doors.

External devices may be connected to ports on the computer module's rear panel. Ports are provided for up to eight Pixel terminals, two parallel printers, and eight RS-232C serial devices. An AC line cord is also attached to the rear panel.

1.1.2 Terminal

The terminal consists of a cathode-ray tube (CRT) display and an alphanumeric keyboard. The display and keyboard are separate units connected by a flexible coiled cable. The terminal is connected to the computer module with a cable which plugs into the back panel of the CRT display and one of the terminal ports on the computer module's rear panel.

The display unit contains a power supply, a receiver board which serves as the interface between the terminal and the computer module, and a display driver. The receiver board also drives the audible signal, or "bell."

The CRT features a direct-etched surface to reduce glare. It displays 25 eighty-character lines of 9 × 9 dot-matrix characters. A contrast control, provided under the right side of the display screen, allows the operator to adjust the brightness of the displayed characters. The operator may also adjust the angle of the display by rotating the back foot of the display.

The rear panel contains an AC power cord and a rocker-type power switch. Two connectors are provided for connecting the terminal to the computer and the display to the keyboard.

1.1.3 Optional Equipment and Peripherals

The 100/AP system may be expanded and upgraded by adding extra terminals, additional mass storage devices, more main memory, and serial or parallel communication devices to the basic system configuration.

Additional positions are available in the card cage for printed circuit modules. Mounting and panel space for up to four disk drives, of which two may be diskette drives, is available.

1.2 FUNCTIONAL DESCRIPTION

The 100/AP system was designed according to a modular philosophy. Modular design means that the machine consists of a number of sub-assemblies, each with a specific function. It simplifies maintenance and repair, since a malfunction can usually be identified as a failure within a certain module or modules. It also simplifies system upgrading and expansion.

The various modules are interconnected as shown in Figure 1-2. Many of the modules are printed circuit cards which fit into the card cage inside the computer housing:

- Input/output processor board
- Attached processor board and RAM board(s)
- Serial board
- Monochrome terminal controller board(s)
- Diskette drive controller board
- Winchester disk drive controller board (optional)
- Power supply

The machine also includes these modules:

- Terminal(s), consisting of keyboard and display
- Diskette drive(s)
- Winchester disk drive(s) (optional)
- Backplane, card cage, and housing

1.2.1 Processor/Memory Modules

The processor/memory modules include the input/output processor board and the attached processor module. The attached processor module consists of one board which contains the attached processor and associated electronics, and one to six boards containing one Megabyte of RAM each.

The input/output processor, or IOP, serves as the central control processor for the 100/AP machine. Upon powerup, it performs the system bootstrap. It also coordinates data transactions between the system modules. It is supported by 128 kilobytes of dynamic RAM memory (256 kbytes optional).

The attached processor executes instuctions and processes data. Because the attached processor is unencumbered by housekeeping and I/O functions, it is able to process larger amounts of data than would otherwise be possible.

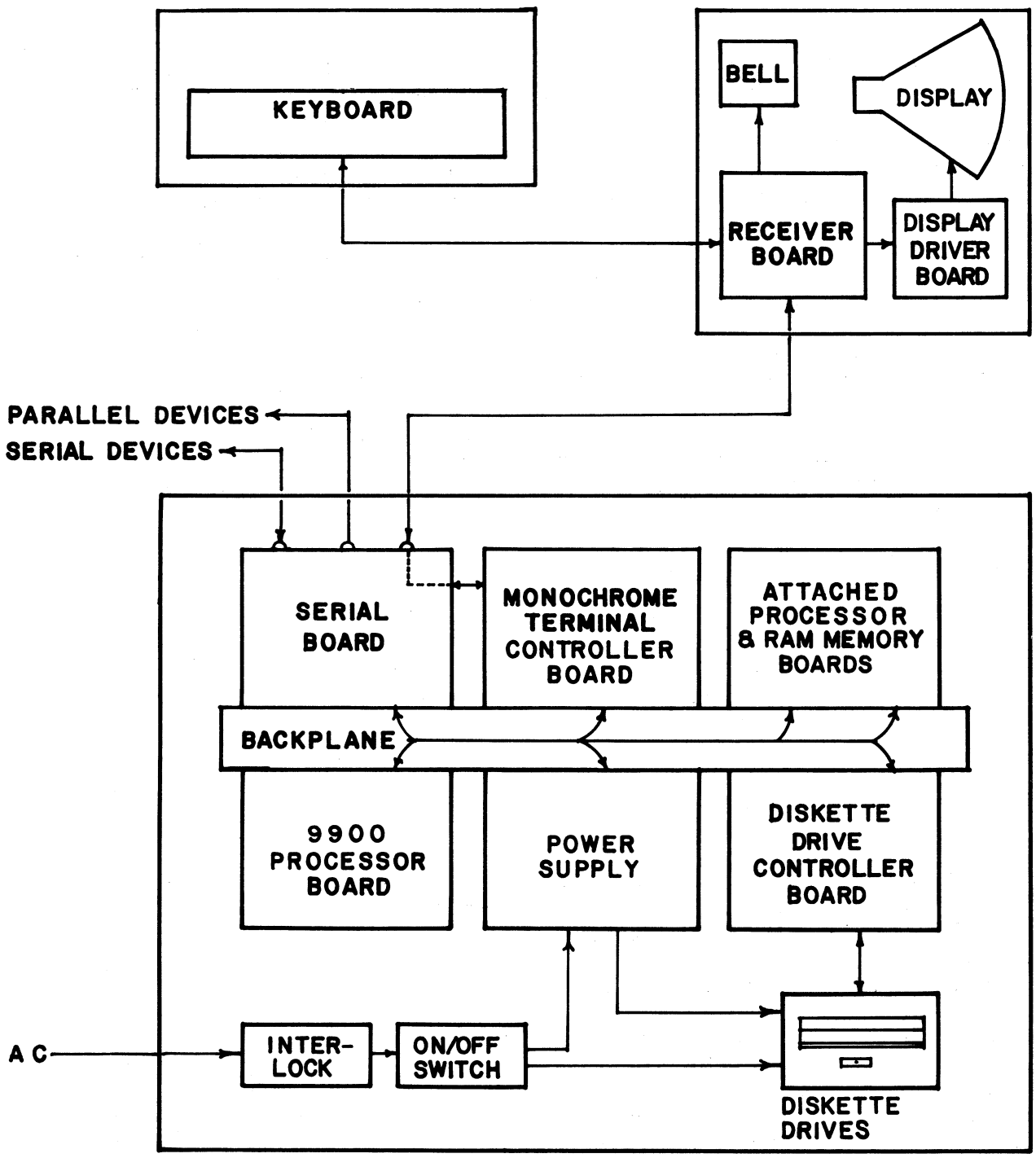


Figure 1-2. 100/AP Modules

1.2.2 I/O Interfaces and Devices

The 100/AP supports input/output ports which allow communication with up to eight Pixel terminals, eight RS-232C serial devices, and two Centronics-compatible parallel printers. These ports are mounted on the serial board; they can be accessed through a cutout on the rear panel of the computer.

Serial and parallel communications are managed by the serial board, which acts as an interface between the I/O ports and the 100/AP's internal data paths and control lines. These interfaces are programmable—parameters such as baud rate, number of bits per character, number of stop bits, and parity are set by the system software and may be changed by the user as communication requirements change.

The Pixel terminals consist of a keyboard and video display. Video and sync outputs for the video displays, and buffers and interrupt logic for the keyboard data stream are provided by the monochrome terminal controller board(s). Each monochrome terminal controller board can control up to four terminals; by equipping the system with two of these controller boards, the maximum configuration of eight user terminals can be supported.

1.2.3 Bulk Storage Devices

The 100/AP can be equipped with two different types of magnetic disk recording subsystems for bulk storage. Diskette drives record information on inexpensive, removable diskettes (also called "floppy disks"). Winchester disk drives store information on rigid, fixed disks housed in a sealed environment. Diskette drives provide 0.4 Megabytes of storage per diskette (single-density recording format); Winchester rigid disk drives are available in 5 Mbyte, 10 Mbyte, 20 Mbyte, 30 Mbyte, and 40 Mbyte nominal capacities.

A disk subsystem consists of a controller board and one or more drives. The controller board converts data from a format which can be stored on disk to a format which can be used by the processor, and vice versa. It also generates the necessary control and status signals. Controller boards plug into the computer backplane.

Drives spin the magnetic disks and locate, modify or read data with a magnetic read/write head. The 100/AP system can accomodate a total of four disk drives (diskette or Winchester).

Of these four drives, two may be diskette drives. Most systems will include diskette drives: in a small system they function as the principal drive, and in a large system equipped with Winchester disk drives they function as a software loading and archival backup unit.

1.2.4 Support Elements

Support elements include the housing (described in Section 1.1), the card cage and the power supply.

The 14-position card cage houses the printed circuit card modules and guides them into the 100-contact connectors on the backplane. The backplane includes the data and address buses, power lines, and control signals used by the printed circuit card modules.

A switching-type power supply provides regulated power for the system.

100/AP CONFIGURATIONS

CARD CAGE POSITIONS (14 total)

- Serial board (4-1-8)
  or Serial board (8-2-8)
- Power supply
- Monochrome terminal controller #0
- *Monochrome terminal controller #1*
- Input/output processor with 128K *(256K)* RAM
- Diskette drive controller *(or empty slot)*
- *Winchester disk drive controller*
- Attached processor board
- AP/memory board #0
- *AP/memory board #1*
- *AP/memory board #2*
- *AP/memory board #3*
- *AP/memory board #4*
- *AP/memory board #5*

DISK DRIVES

- Diskette drive
  or Winchester disk drive
- Diskette drive
  or Winchester disk drive
- *Winchester disk drive*
- *Winchester disk drive*

TERMINALS

- Terminal #0
- *Terminal #1*
- *Terminal #2*
- *Terminal #3*
- *Terminal #4*
- *Terminal #5*
- *Terminal #6*
- *Terminal #7*

Notes: Additions to the basic configuration are shown in italics.

1) Terminals 4-7 require the second terminal controller.

1.3 SPECIFICATIONS

Mechanical

Height:	26.5	in	67.3	cm
Width:	20.0	in	50.8	cm
Depth:	21.0	in	53.3	cm
Weight:	250	lbs	113	kg

Power Requirements

Input voltage:	85-130 or 170-260 VAC
Frequency:	47-63 Hz
Power:	1100 watts
Other:	A three-wire grounded receptacle is required for both the computer and terminal AC line cords.

Environmental Requirements

Temperature:	32-95 °F	0-35 °C
Humidity:	10-80% noncondensing	
Altitude:	10,000 ft	3050 m
RFI/EMI:	Meets FCC class A standards	

Section 2

THEORY OF OPERATION

2.0 GENERAL

This section contains functional descriptions and block-level discussions of the following modules:

Processing Modules

- I/O processor (9900) module
- Attached processor (68000) module (and RAM boards)

I/O Modules

- Serial board
- Monochrome terminal controller board
- Terminal

Disk Subsystems

- Diskette drive controller board
- Diskette drive
- Winchester disk drive controller board
- Winchester disk drive

Support Elements

- Power supply
- Backplane, card cage, and housing

Each subsection discusses one of these modules; an additional subsection describes the backplane-bus arrangement. Each subsection begins with a general overview of the module and a table of its functional characteristics; it goes on to a block-diagram and a discussion based on the block diagram. Finally, some subsections contain other information important to the understanding of the module and the machine.

2.1 INPUT/OUTPUT PROCESSOR MODULE

2.1.1 Overview

The input/output processor module, or IOP, is a single 10 × 12 inch (25.4 × 30.5 cm) printed circuit board which contains the I/O microprocessor, associated support and interface electronics, dynamic RAM, and bootstrap ROM. The I/O microprocessor serves as the central control processor for the Pixel 100/AP system. It communicates with the attached processor module and the other system components via the backplane.

The IOP performs the I/O and housekeeping functions and processes faults for the attached processor (AP), leaving the AP free for data processing. The IOP also performs the bootstrapping function upon powerup.

In the Pixel 100 system, which lacks the attached processor module, the IOP also performs the central data processing functions. Section 2.1.6 of this manual will discuss the differences in this module's operation between the 100 and 100/AP systems.

The I/O microprocessor, a TMS 9900, is a single-chip NMOS device with 64 pins. It employs a 16-bit memory word and executes an advanced instruction set. Its memory-to-memory architecture allows faster response to interrupts and increased programming flexibility.

Support and interface circuitry, including timing generation, interrupt logic, and direct memory access control, is designed around 9900-family LSI components for reliability and low cost.

The IOP is supported by 128 kilobytes of 64K × 1 dynamic RAM. An additional 128 kilobytes of RAM are available as an option. This memory is mounted on the IOP board itself, and should not be confused with the AP's 1 Megabyte RAM boards.

Bootstrap code is stored on 2 2K × 8 EPROMs.

2.1.2 Functional Characteristics

Processor

Type:	TMS 9900
Instruction types:	Data transfer Arithmetic Compare Logical Shift Branch Control and I/O
Object lengths:	16-bit word 8-bit byte
Interrupts:	16 prioritized interrupts Reset
Registers:	16 general registers Workspace register Program counter Status register
Buses:	16-bit bidirectional data bus 15-bit address bus

Memory

Type:	65,536 × 1 dynamic RAM
Board capacity:	128 kilobytes 256 kilobytes optional
Cycle time:	Access: 150 nsec. Read, modify, write: 280 nsec.
Refresh period:	2 milliseconds (128 kbytes) 4 milliseconds (256 kbytes)

2.1.3 Block Diagram

Figure 2-1 shows the principal components and interconnections of the I/O processor board. The board includes the 9900 microprocessor, support and interface components, and 128 or 256 kilobytes of RAM.

This section covers the following functional blocks and operations:

- 9900 microprocessor
- Timing generation
- Interrupt processing
- Data and address paths
- Direct memory access (DMA) control
- Communications register unit (CRU) operations

9900 Microprocessor

The 9900 is an advanced 16-bit microprocessor (also called a central processing unit, or CPU) with minicomputer-like architecture and instructions. Operations are performed with a set of dedicated registers, an arithmetic logic unit (ALU), and instruction handling circuitry. These components are shown in Figure 2-2.

The 64 pins of the 9900 processor chip include a 15-bit address bus, a 16-bit data bus, and support and control lines. Support lines include three supply voltages (+5, -5, and +12 volts), a ground reference, and four clock phases. Bus control lines include read/write and memory enable signals, as well as the three CRU signals discussed below. Interrupt control lines accept interrupt requests and a four-bit interrupt level code from the interrupt logic. Memory control lines are provided for direct memory access (DMA) control, and for memory control during read/write operations. A pin is also provided for the $\overline{\text{RESET}}$ signal.

The 9900 is programmed by storing sets of instructions in memory. Instructions specify operations and the memory locations of operands. These operations include data transfer, arithmetic, compare, logical (boolean), bit shifting, program branching, and a number of control and input/output operations.

As the processor receives clock signals from the timing generation circuitry, it fetches an instruction, executes it, stores the result, fetches another instruction, and so on. While an

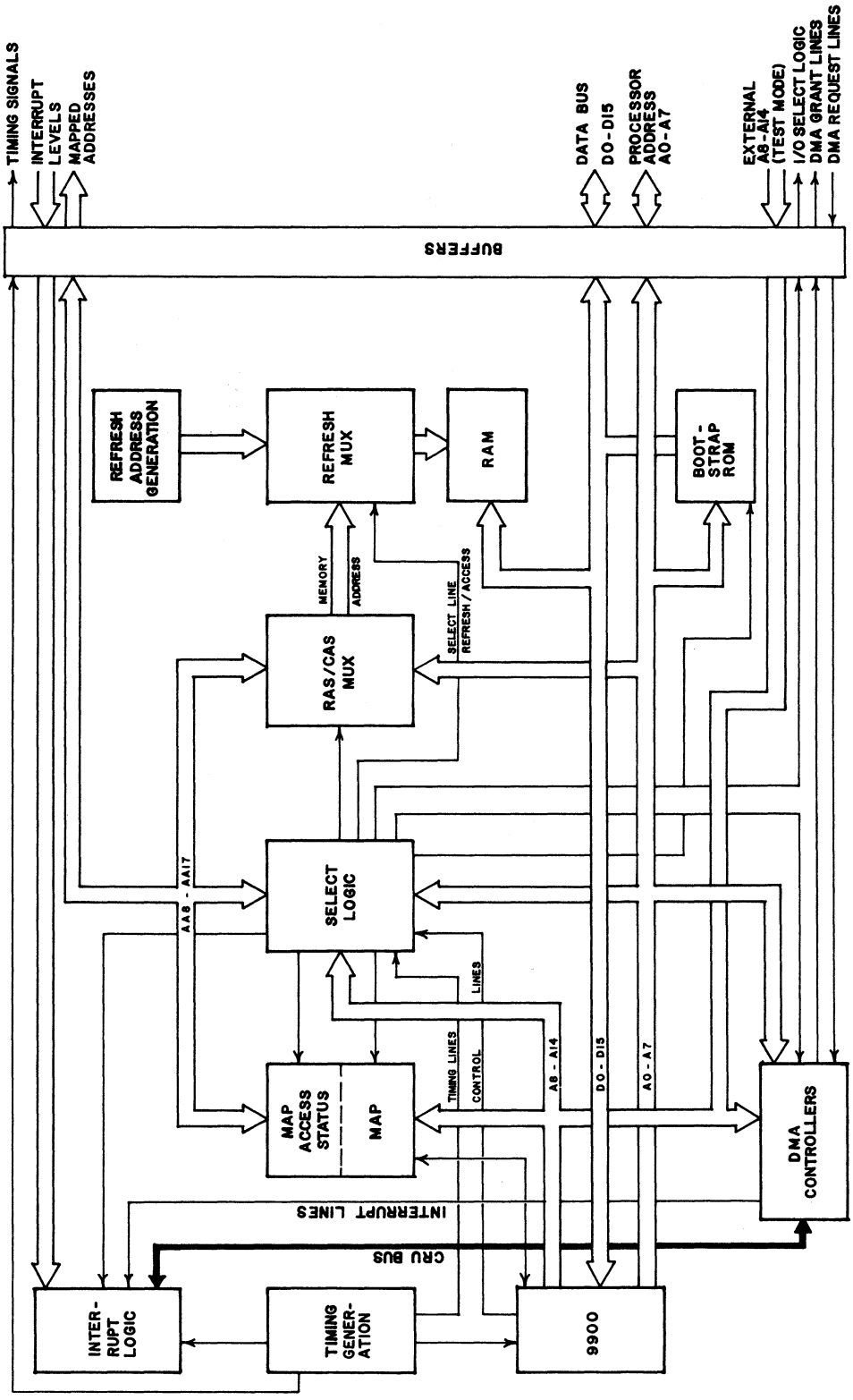


Figure 2-1. Input/Output Processor Board

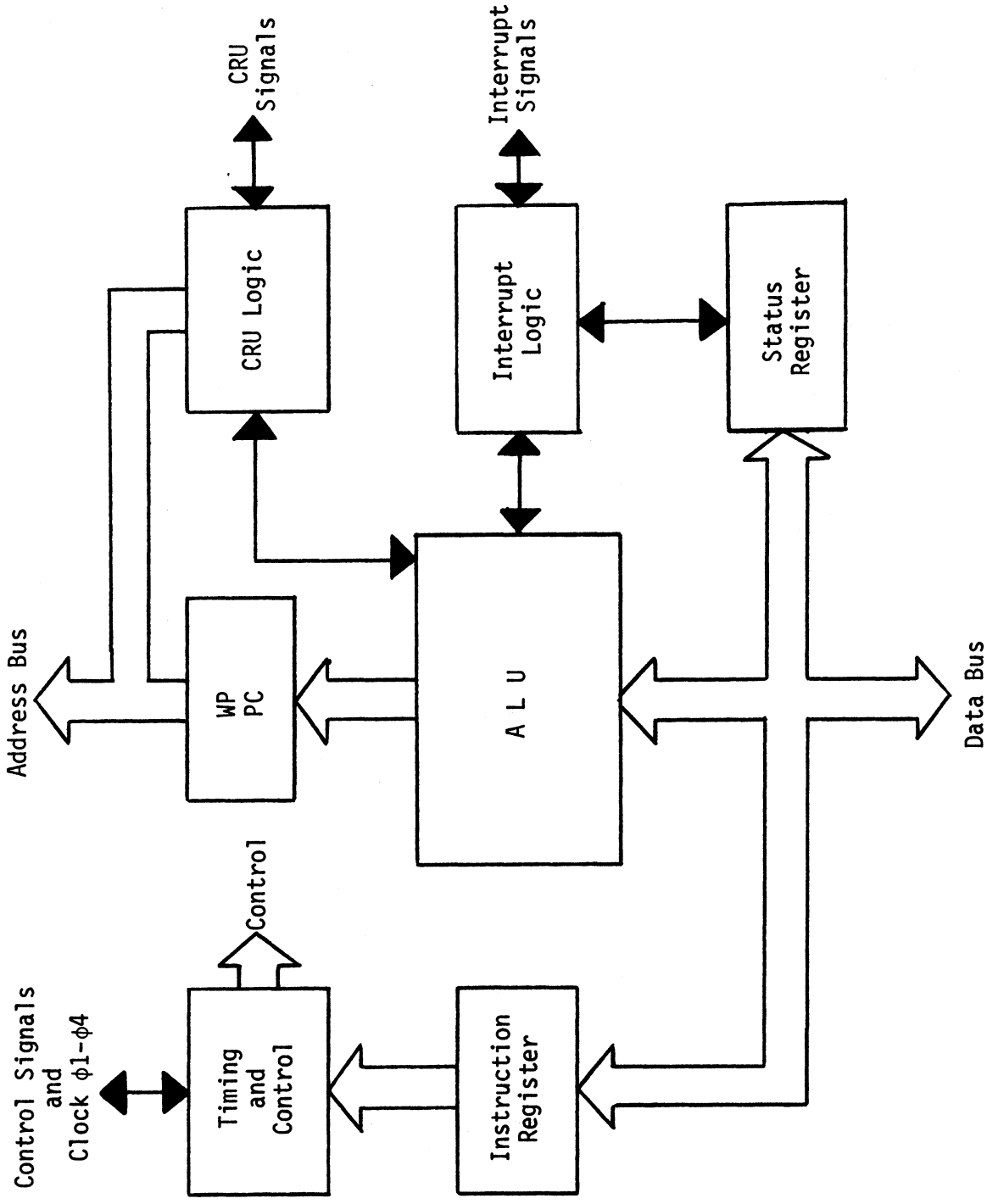


Figure 2-2. 9900 Microprocessor

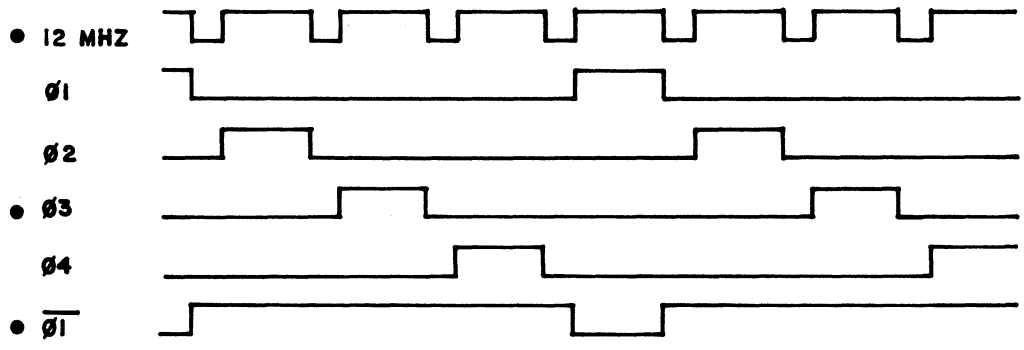
instruction is being executed it is stored in a special register called the instruction register. Decode circuitry sets up the appropriate controls based on the contents of the instruction register. After an instruction is executed, a memory write cycle is performed to store the result of the operation at the desired location in memory.

The 9900 also provides 16 general-purpose registers implemented as blocks of memory called workspaces. Three special registers are provided to manipulate these workspaces and perform other functions during the execution of a program. The workspace pointer (WP) holds the address of the first word in the current workspace. The program counter (PC) is used to locate the next instruction to be executed. The status register (ST) consists of individual bits which are used as flags. These flags are set as a result of instructions and may be used as a basis for decision making during program execution.

Timing Generation

Timing generation is performed by a TMS 9904 clock generator/ driver chip. A 48 MHz crystal-controlled oscillator is divided to generate the four-phase timing signals required by the 9900. Phases 1 and 3 of the clock and a 12 MHz oscillator signal are supplied to the backplane for synchronous operations. (Note: the attached processor and the IOP run asynchronously.)

The output of the timing generator is shown in Figure 2-3.



• BACKPLANE SIGNALS

Figure 2-3. Clock Signals

Interrupt Processing

The 9900 provides fifteen maskable interrupt levels in addition to the RESET function. An interrupt request processor chip receives the interrupt requests and signals the 9900 by asserting the interrupt request signal INTREQ. The interrupt processor provides a four-bit code corresponding to the level of the interrupt. RESET is given the highest priority, followed by interrupt requests generated by devices on the IOP board. Ten interrupt request lines corresponding to the lowest-priority interrupt requests (INT06..INT15) are provided on the backplane. Interrupt level assignments are shown in Table 2-1.

Table 2-1
I/O Processor Interrupt Levels

01	Power failure
02	Memory parity error
03	Timer
04	DMA channels 0 and 1
05	DMA channels 2 and 3
06	(reserved)
07	Winchester disk drives
08	Diskette drives
09	Communications controller
10	Serial board
11	(reserved)
12	(reserved)
13	Attached processor errors
14	Terminals
15	Attached processor service request

Data and Address Paths

The principal data path on the I/O processor board is the 16-bit bidirectional tri-state data bus. A bidirectional buffer is used to connect the on-board data bus to the backplane data bus. The two buses are connected when the processor addresses the off board memory space or when a direct memory access transfer is performed. In all other cases the two buses are isolated. The individual bits of the data bus are numbered D0 through D15. D0 is the most significant bit.

The address buses include the processor address bus and the mapped address bus; they are discussed in more detail in Section 2.1.4 under "memory mapping." The address information is supplied to the backplane through buffers.

DMA Controllers

Four direct memory access (DMA) channels are provided on the backplane. The DMA channels are used to provide a fast-response and high-transfer-rate coupling between processor RAM and certain high-speed peripheral devices (for example, diskette and Winchester disk drives).

DMA transfers are more efficient than other I/O operations because they are performed without CPU intervention. Other I/O operations usually require an interrupt routine for each word of data transferred. In a DMA transfer, the DMA controller holds the processor—causes it to stop execution and relinquish control of the data and address buses—and generates the signals necessary to transfer directly between the external device and memory.

DMA operations are controlled by two TMS 9911 DMA controller chips which provide two DMA channels each. These channels consist of request and grant lines—actual data transfers take place along the data bus. A peripheral device signals that it is ready for a transfer by asserting one of the request signals $\overline{\text{DMARQ0}}$..$\overline{\text{DMARQ3}}$. The DMA controller issues a hold signal to the CPU. At the next available non-memory cycle, the processor relinquishes control of the data and address buses and issues a hold acknowledge signal. The DMA controller then signals the peripheral device by asserting one of the grant lines $\overline{\text{DMAGR0}}$.. $\overline{\text{DMAGR3}}$. The DMA controller then supervises the direct transfer of data between the peripheral device and the processor RAM. When the transfer is complete, the DMA controller releases the hold signals and the processor resumes execution of its instructions.

DMA channel assignments are shown in Table 2-2.

Table 2-2
DMA Channel Assignments

0	Winchester disk drives
1	Diskette drives
2	(reserved)
3	Communications controller

CRU Operations

The communications register unit (CRU) is a serial communication path used by the 9900 processor for a number of I/O operations, particularly those involving slower I/O devices.

The primary advantage of the CRU is economic; its data path is one bit wide, allowing chips with lower pin counts to be used. The CRU also provides a convenient alternate address path which is described more fully in Section 2.1.4.

The CRU data field consists of up to 4096 directly addressable input bits and 4096 directly addressable output bits. These bits can be addressed individually or in groups of 2 to 16 bits. Three signal lines—CRUIN, CRUOUT, and CRUCLK—are used to read and write bits of the CRU data field. The bits are specified by a portion of the processor address bus PA03..PA14 (on the backplane, these appear as A3..A7 and CA8..CA14). The processor instructions that drive the CRU can set, reset, or read any bit in the CRU data field or transfer between external memory and the CRU data field.

CRU data is sampled on CRUIN during input operations. During output operations, CRU data appears on the CRUOUT line and is strobed by CRUCLK.

CRU addresses 000_{16} through 300_{16} are reserved for the external CRU address space under the control of the $\overline{\text{EXTCRU}}$ line on the backplane. $\overline{\text{EXTCRU}}$ is asserted whenever one of the external CRU addresses appears on the processor address bus.

2.1.4 Memory Operations

Read and Write

The processor begins a memory read or write cycle by asserting its memory enable signal, $\overline{\text{MEMEN}}$, on the second phase of a clock cycle. (On the backplane, $\overline{\text{MEMEN}}$ is called $\overline{\text{BMEMEN}}$. It is connected to the processor signal via a buffer.)

A read cycle is shown in Figure 2-4. The processor asserts $\overline{\text{MEMEN}}$ and DBIN (data bus in; on the backplane, BDBIN) on the second phase of the first clock cycle. If the memory device is ready at the first phase of the next clock cycle, the processor will read data from the data bus on the first phase of clock cycle 3. If the memory device is not ready (that is, if it has not asserted to READY signal), then the processor will enter a wait state for one clock cycle and sample READY again.

A write cycle is shown in Firgure 2-5. The processor asserts $\overline{\text{MEMEN}}$ and places a memory vector and valid data on the address and data buses respectively. At the beginning of the second clock cycle, the processor asserts $\overline{\text{WE}}$ (write enable). If the memory device is READY, then the data is written during the second clock cycle. If the device is not READY, then the processor enters a one-cycle wait state as before.

Memory Mapping

The 9900 microprocessor's fifteen-bit address bus allows it to address directly 64 kilobytes of memory. Since the actual addressing requirements of the IOP are greater than 64 kilobytes (about eight times greater), provisions must be made to expand the addressing capabilities of the microprocessor. This is accomplished with the use of a memory map, a functional block constructed of very high speed (65 nsec.) static RAMs. The memory map stores arrays of pointers, which select windows within the address space for memory operations. In effect, the memory map accepts the 9900's 15-bit address and converts it into an 18-bit mapped address.

The eighteen bit mapped address allows the 9900 microprocessor to address eight 64 kilobyte memory spaces. Four spaces are assigned to the processor RAM, while the other four are assigned to bootstrap ROM and three external memory spaces: the terminals, the attached processor, and parallel I/O devices. The allocation of the mapped memory space—or "virtual" memory space—is shown in Figure 2-6.

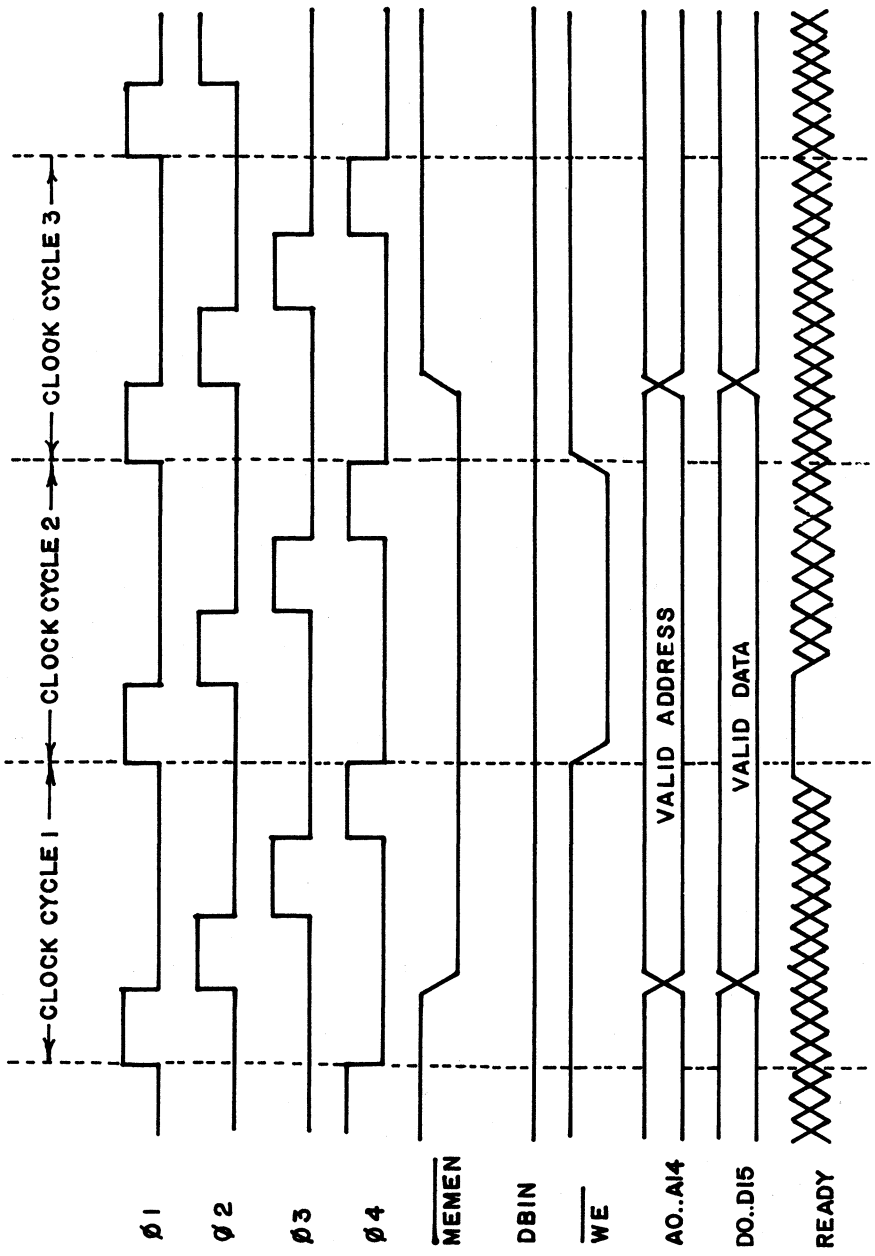


Figure 2-4. Memory Read Cycle

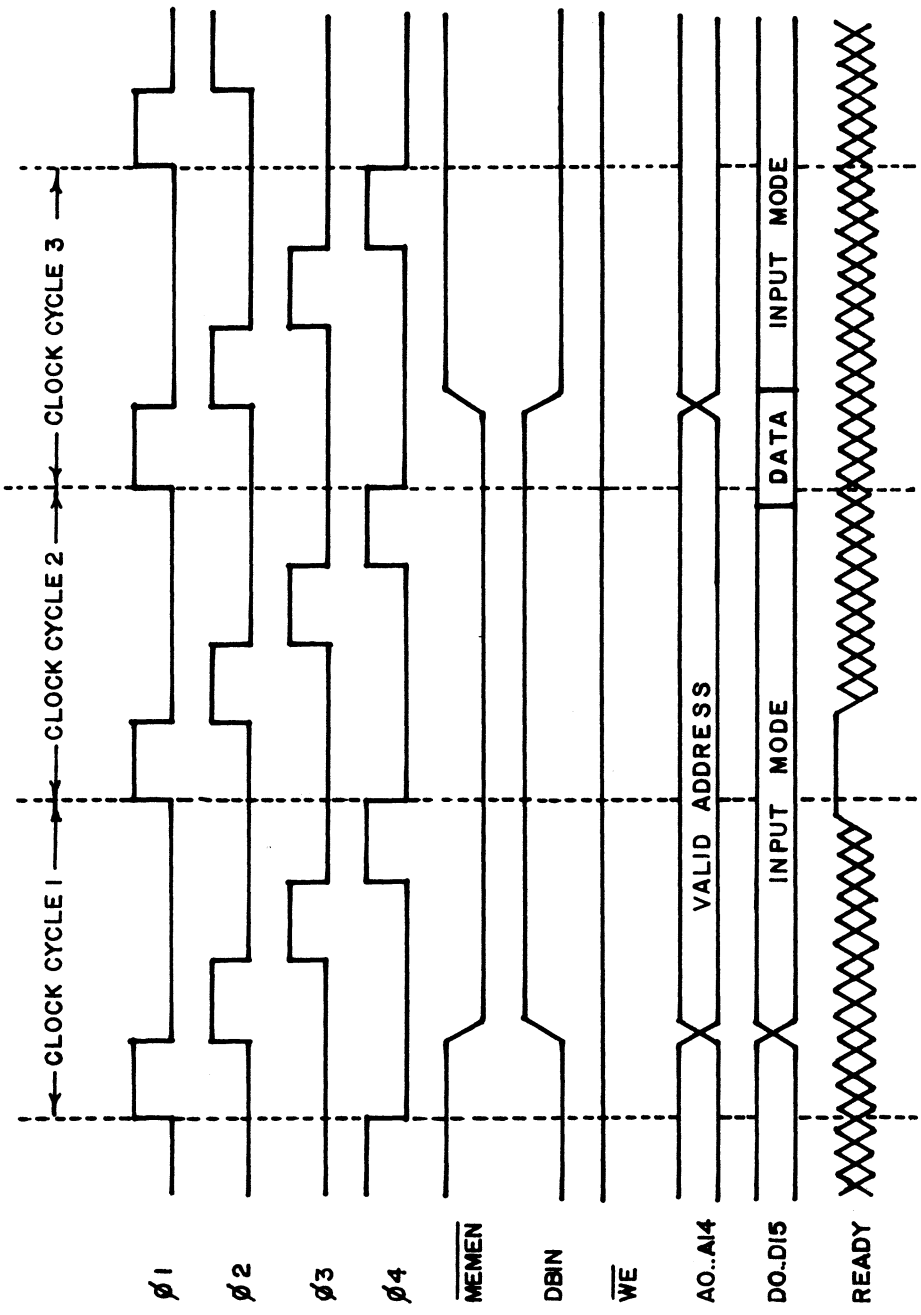


Figure 2-5. Memory Write Cycle

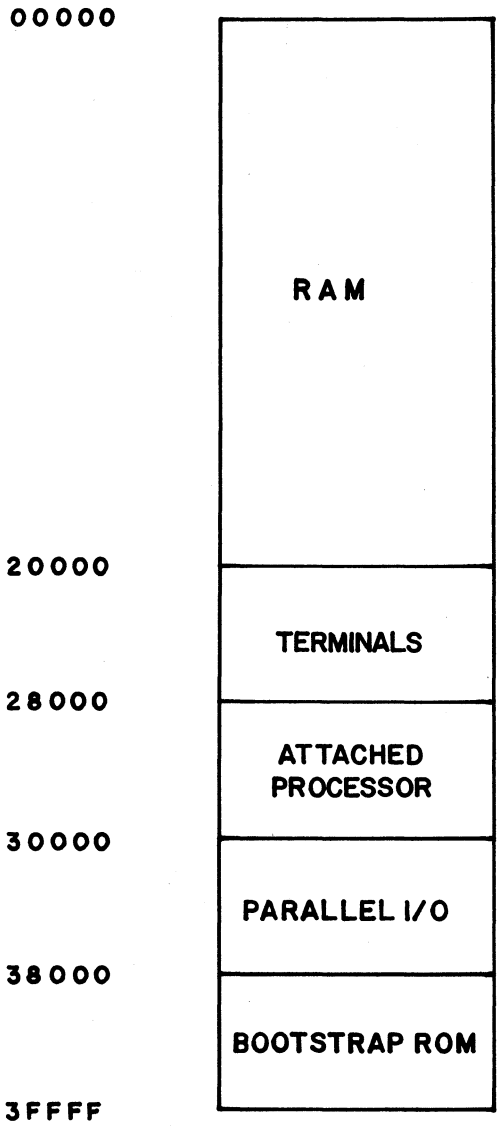


Figure 2-6. 9900 Virtual Memory Space Allocation

There are two map images. One is used for running user programs, and the other is used for DMA transfers and operating system code.

The memory-mapped design results in several different address paths on the IOP module and the backplane. These address paths, and some other important buses, are shown in Figure 2-7.

The processor address bus, that is, the fifteen lines directly connected to the microprocessor chip itself, is fifteen bits wide (PA00..PA14). Of these fifteen bits, the higher-order seven and lower-order eight are treated differently. The lower-order eight bits PA00..PA07 are the same as the lower-order eight bits of the backplane address bus A00..A07.

The higher-order seven bits PA08..PA14 are fed into the memory map. The map's output consists of ten bits AA08..AA17. The higher-order three bits of the mapped address are then decoded into column address strobes for the processor RAM, bootsrtrap ROM, and the externalmemory address select lines $\overline{\text{SCROCAS}}$ (terminals), $\overline{\text{APCAS}}$ (attached processor), and $\overline{\text{PIOCAS}}$ (parallel I/O).

The fifteen bits of the backplane address consist of

the processor addresses PA00..PA07 → A00..A07
and the mapped addresses AA08..AA14 → A08..A14.

For CRU operations, however, the unmapped processor addresses are required. The CRU address bus (CA08..CA14) on the backplane is equivalent to the higher-order portion of the processor address bus (PA08..PA14).

Thus, two complete address buses are available on the backplane: the fifteen-bit mapped address bus (A00..A14), which with the external select lines $\overline{\text{SCROCAS}}$, $\overline{\text{APCAS}}$, and $\overline{\text{PIOCAS}}$ is used for addressing external devices; and the fifteen-bit unmapped address bus (A00.A07..CA08..CA14) used for CRU operations.

2.1.5 Bootstrap Performance

When the machine is powered up, or a $\overline{\text{RESET}}$ signal is received, the IOP must perform a number of routines before loading the operating system which allows the user to use the system. This operation, bootstrapping, is executed from code stored in two 1024 × 8 EPROMs. The bootstrap code runs some diagnostics on the IOP board—it primarily makes sure that the 9900 and its

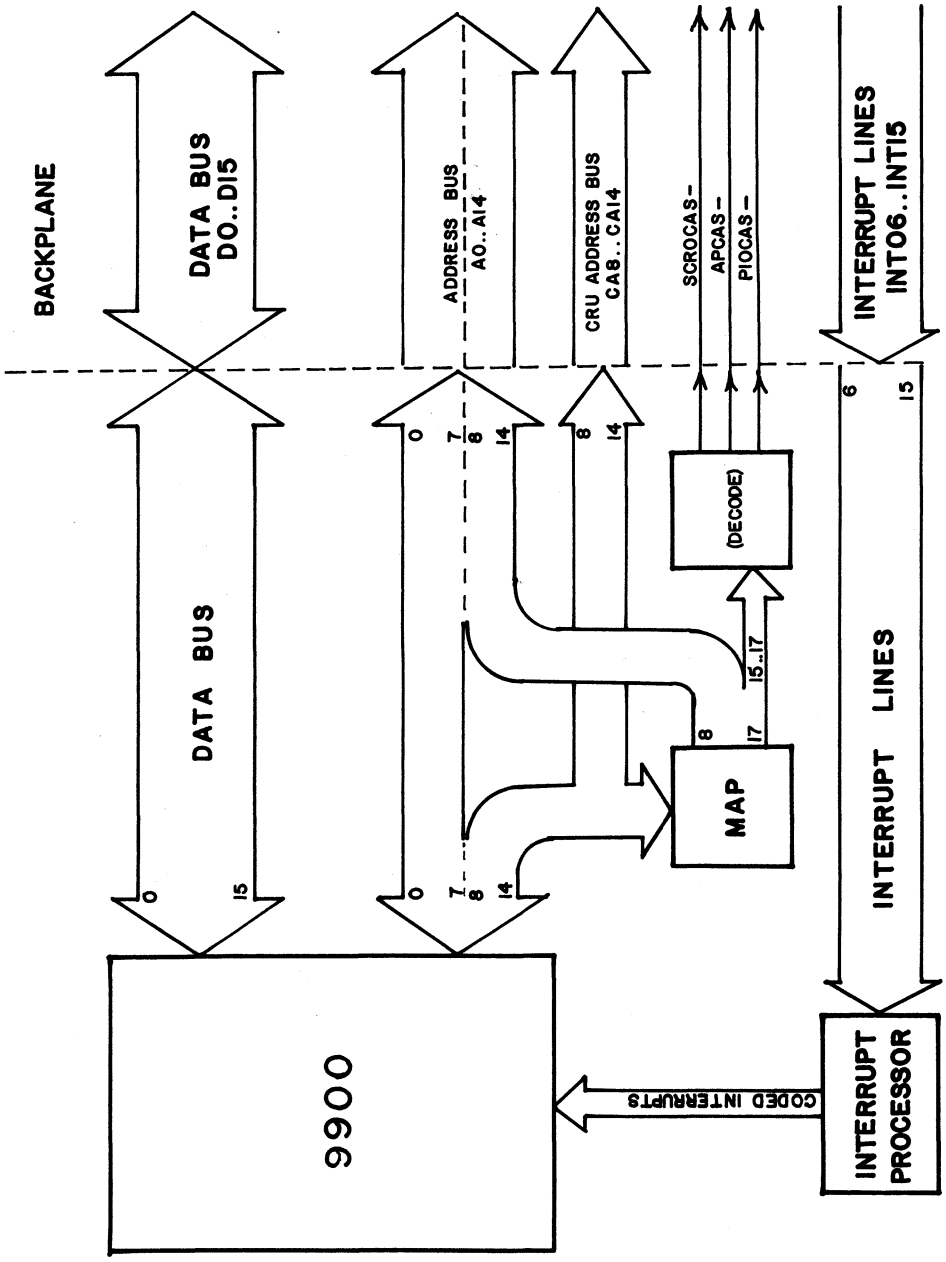


Figure 2-7. IOP Module and Backplane Buses

principal support components are operating properly—before initializing the system modules.

The reset operation which precedes bootstrapping causes the memory map to be disabled. The memory map outputs are pulled up; in other words, the map address is all ones. This address is assigned to the bootstrap EPROMs.

The 9900 fetches a reset vector from the memory map and begins to execute from the EPROMs. After the diagnostics have been run, some of the memory map is initialized to allow the EPROMs to continue to be addressed, and to set up addressing to the processor RAM. Once these initializations are complete, the map is enabled.

The diskette drive controller board, and the Winchester disk drive controller board (if present), are initialized. The system then continues to bootstrap from operating system code located on a system diskette. If an operating system diskette is not present, the system will check the Winchester drive(s) for the operating system code.

2.1.6 9900 Operations in the Pixel 100 Machine

The Pixel 100 machine differs from the 100/AP in that it does not contain the AP (attached processor) module or the RAM memory module(s) associated with the AP. It will not work with an AP operating system.

The 9900 processor module is therefore called upon to perform both control and data processing functions. From a hardware point of view, the attached processor is an external device which occupies 64 kilobytes of the virtual memory space. The only real hardware difference between the IOP's function in the two systems is the use of the memory space decoded by the $\overline{\text{APCAS}}$ line, and the operating system version.

It is possible to upgrade a Pixel 100 system by plugging the AP and AP memory boards into the extra positions in the card cage and booting an AP operating system. It is also possible to boot a Pixel 100 system operating system on a 100/AP machine; the system will simply ignore the AP and AP/memory boards. This operation is useful in isolating certain AP system failures.

2.2 ATTACHED PROCESSOR MODULE

2.2.1 Overview

The attached processor (AP) module consists of two to seven printed circuit boards. One of the boards, the "AP board," contains the attached processor and its associated support and interface circuitry. The other boards, "AP/memory boards," each contain up to one Megabyte of dynamic RAM memory.

The AP module is the principal data processor for the 100/AP system. The AP board communicates with the I/O processor via the backplane, and with the AP/memory boards through two sixty-conductor ribbon cables attached to the tops of the boards.

The attached processor is a 68000, a 64-pin single-chip microprocessor built using high-density NMOS techniques. It supports an object length of 32, 16, or 8 bits. It offers seventeen 32-bit data and address registers.

Support and interface electronics are fairly simple, since all of the input/output operations are handled by the I/O processor module.

Each AP/memory board contains 1 Megabyte of 64K × 1 dynamic RAM. The system may be expanded to a maximum of 6 Megabytes of RAM, although the power requirements at this maximum configuration may limit the number of peripherals and options the machine is able to support.

2.2.2 Functional Characteristics

Processor

Type:	68000
Instruction types:	Data transfer Integer arithmetic Logical Shift and rotate Bit manipulation Binary coded decimal Program control
Addressing:	16 Megabyte direct addressing range 14 addressing modes

Processor, cont'd

Object lengths:	32-bit long word 16-bit word 8-bit byte
Registers:	Eight 32-bit data registers Seven 32-bit address registers Two 32-bit stack pointers One 32-bit program counter One 16-bit status register
Buses:	16-bit bidirectional data bus 32-bit address bus

Memory

Type:	65,536 × 1 dynamic RAM
Board capacity:	1 Megabyte
Cycle time:	Access: 150 nsec. Read, modify, write: 280 nsec.
Refresh period:	4 millisec. maximum

2.2.3 Block Diagram

Figure 2-8 shows the principal components and data paths of the attached processor board. This board includes the 68000 microprocessor chip, some support components, the processor address and data paths, and the memory map.

This section will discuss the following:

- 68000 microprocessor
- Timing generation
- Memory operations
- Board select and control
- Data and address paths

68000 Microprocessor

68000 microprocessor operations are similar to those of the I/O processor discussed in Section 2.1.3. Like the I/O processor, the 68000 operates with a set of dedicated registers, instruction handling circuitry, and an arithmetic logic unit. It is programmed by storing instructions in memory. As clock signals are received, the 68000 will fetch an instruction, execute it, store the result, fetch another instruction, and so on.

The 68000 chip has 64 pins, which perform the following functions:

- A 23-bit address bus, which provides the address for 68000 operations.
- A 16-bit bidirectional data bus.
- Bus control signals, including the address strobe $\overline{AS}$ and a single read/write signal R/$\overline{W}$. The address strobe indicates that there is a valid address on the address bus, and R/$\overline{W}$ identifies a data bus transfer as a read or write cycle.
- Bus arbitration control signals, which permit devices to request and receive control of the 68000 processor address and data buses.
- Interrupt control signals.
- System control signals, which indicate fault conditions and $\overline{HALT}$ or $\overline{RESET}$ the 68000.

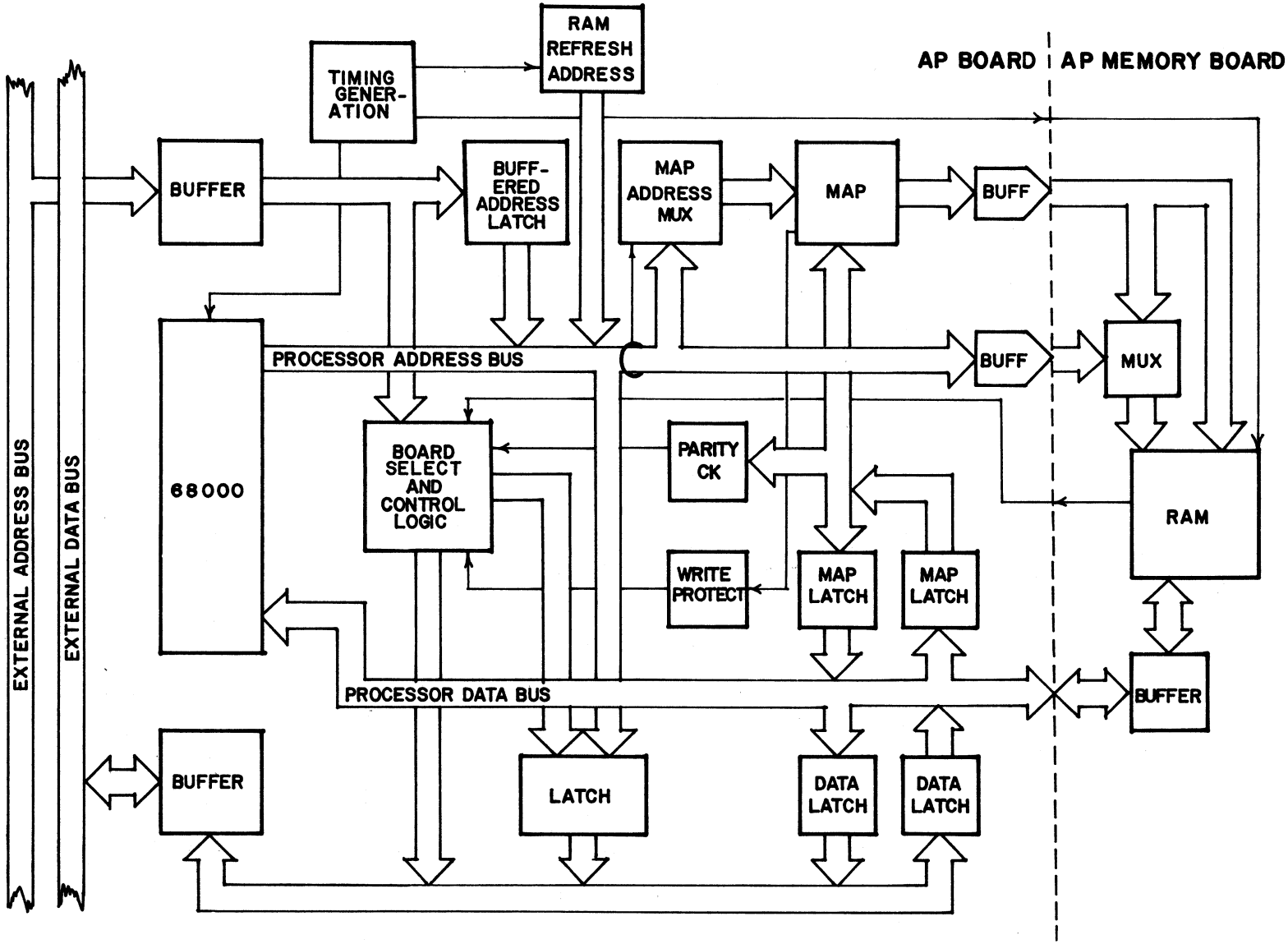


Figure 2-8. Attached Processor Module

- Processor status codes, which indicate the processor state (user, supervisor, or interrupted) and the cycle type being executed.

- Support pins, including +5V, ground, and a single-phase clock input.

The 68000 performs operations on 8-bit bytes, 16-bit words, and 32-bit long words. Some instructions contain an explicitly coded operand-size specification, while others are designed to operate on certain data types.

These three data types can be stored in one of the eight general purpose data registers. A byte will occupy the lower order 8 bits, a word will occupy the lower order 16 bits, and a long word will occupy the entire 32 bits of space in the register.

The 68000 also supports seven address registers and two stack pointers (similar to the "workspace pointers in the 9900 microprocessor). These registers are 32 bits wide. The 32-bit program counter and 16-bit status register identify instructions to be executed and provide flags for decision-making, respectively.

The instruction set, specially designed to support high-level languages and to facilitate ease of programming form a set of tools to manipulate these registers and the external AP memory. Instructions contain two kinds of information: the type of function to be performed, and the locations of data on which to perform that function. The latter infomation is referred to as addressing information. The 68000 instruction set allows the program to address data in registers, at a specific address, or in certain specialized registers. Certain addressing types direct the processor to operate on information preceding or following certain information in memory.

The instructions perform the following functions:

- Data movement. Basic transfer and storage is provided by a move instruction, which allows the manipulation of both addresses and data. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. Several special data movement instructions are also supported.

- Integer Arithmetic Operations. These include add, subtract, multiply and divide, as well as arithmetic compare, clear and negate.

- Logical Operations. These operations include and, or exclusive or, and not.

- Shift and Rotate. Shift and rotate operations in both directions are supported. Shift counts of zero to 63 bits can be specified in a data register; 1 to 7 can be explicitly coded in the instruction.

- Bit Manipulation Operations. These permit individual bits to be tested, set, cleared, or changed.

- Binary Coded Decimal Operations. These permit standard multiprecision arithmetic operations to be performed on four-bit binary-coded-decimal (BCD) data.

- Program/System Control Operations. These instructions are used to control the execution of programs and also permit the operating system to integrate the processor into a usable system.

Timing Generation

Timing signals for the 68000 microprocessor, as well as for RAM refresh, are generated by a 32 MHz crystal-controlled oscillator module. The 32 MHz signal is divided by four to provide the single 8 MHz clock signal required by the processor.

The attached processor and the I/O processor run asynchronously.

Memory Operations

The AP subsystem is supported by up to six Megabytes of dynamic RAM memory. AP/memory boards, which hold up to one Megabyte of RAM each, are connected to the AP through two 60-conductor ribbon cables which plug into connectors on the tops of the boards. Switches on each AP/memory board allow it to be identified as memoryØ through memory5.

The 68000 microprocessor is capable of addressing 16 megabytes of hardware address space. Since the AP/memory (at maximum configuration) consists of only 6 Megabytes, the 68000 processor address bus is translated through a memory map. While the I/O

processor uses a memory map to accomodate a larger address space, the AP uses a memory map to accomodate a smaller address space.

The RAM memory shown in Figure 2-8 can be addressed in one of two ways: via the 68000 processor address bus or via the memory map. Addressing via the address bus is used for refresh, performed by the RAM refresh address circuitry and the timing generation section.

The RAM is normally addressed via the memory map. An address on the 68000 processor address bus is translated by the memory map into the shorter address actually used by the RAM. The 68000 then performs a memory read or write (specified by R/$\overline{W}$) and the data are buffered onto the 68000 data bus.

The I/O processor can access a 64 kiloByte section of the AP's virtual memory space in order to transfer information from terminals, or processing state information. This memory space makes use of the AP's map to provide access to the entire memory space. Data latches permit the 68000 data bus information to be transferred onto the IOP's buffered data bus.

Data in the memory map are read or written via the map latches. A write-protect feature permits each page of the memory map to be protected against supervisor or user access, or both.

Board Select and Control

Board select and control is the general name for the various circuits which select the attached processor board, read status words, process fault conditions, and issue interrupt requests between the processors.

The principal communication paths used for these operations are the (buffered) backplane address and data buses, the AP select line $\overline{\text{APCAS}}$, and the I/O processor read signal BDBIN.

The I/O processor treats the attached processor as an external memory device. The board is selected by means of the address bus and $\overline{\text{APCAS}}$. In addition, a portion of the parallel I/O virtual memory space decoded by $\overline{\text{PIOCAS}}$ contains various control and status registers used by the IOP to control the AP. These registers include bits which give the status of some of the pins on the 68000 microprocessor chip, and are particularly useful in the case of AP faults.

The AP cannot process faults; a fault condition causes the AP to halt and set the appropriate bits of the fault words. These faults can include an error in the parity-protected RAM or memory map; page faults, which occur when the memory map output doesn't coincide with any real memory space; errors in the map's write protection system; and common errors such as spurious interrupts.

Address and Data Paths

This section reviews the various data and address paths on the AP board. Please refer to the AP block diagram, Figure 2-8.

Of the six important paths on the AP board, two are associated with the 68000 microprocessor. These are:

- The processor address bus (labeled as such in the diagram). This contains the unmapped 68000 address. It is used as an input value to the memory map for all RAM addressing operations, and it is used directly by the RAM refresh logic for refresh.

- The processor data bus. All data to and from the RAM appear on this bus. It is also used to supply data to the memory map via two map latches.

Two paths are associated with the backplane data and address lines under the control of the I/O processor. These include:

- The IOP address bus (the output of the buffer connected to the external address bus in the diagram). This is used to access the virtual memory space assigned to the AP, decoded by the $\overline{\text{APCAS}}$ line. It is also used to obtain status and control words from the board control logic; this function is decoded by the $\overline{\text{PIOCAS}}$ line.

- The IOP data bus (the in/output of the buffer connected to the external data bus in the diagram). This is used for general data transfers between the AP sub-system and the rest of the computer. It is also used for transferring control and status words to the IOP.

Two paths are associated with the AP's memory map.

- The mapped address bus (output of the map block). This contains the mapped address used by the real RAM memory.

- The map data bus (the input to the map block from the map latches). This is used to read, modify, and write data in the memory map.

2.3 SERIAL BOARD

2.3.1 Overview

The serial board is the external communications interface for the 100/AP. The serial board plugs into the rearmost position in the card cage, in such a way that the I/O ports mounted on the serial board may be accessed through a cutout in the rear panel of the computer enclosure. The serial board is available with a maximum of eight Pixel terminal ports, eight serial ports conforming to RS-232C protocol, and two Centronics-compatible parallel ports.

The serial board communicates with the I/O processor via the backplane. Parallel and serial data are received and transmitted through programmable devices—parallel interfaces and UARTs—located on the serial board.

A ribbon cable connects the top of the serial board to the monochrome terminal controller board(s). This cable carries all of the signals required by the terminals. The serial board does not process or buffer these signals—it merely makes them available at the terminal connectors. (Note: if there are two monochrome terminal controllers, two top-cables are used.)

Board control and backplane interface logic is shared among all of the serial and parallel ports. A parallel interface or UART is assigned to each port.

2.3.2 Functional Characteristics

Data ports:	Four or eight EIA RS-232C serial ports One or two parallel output ports Eight Pixel terminal connectors
Data format:	(see Section 2.3.4)
Hardware options:	4•1•8 or 8•2•8 (serial•parallel•terminal)

2.3.3 Block Diagram

Data paths and functional blocks for the serial board are shown in Figure 2-9. The serial board performs three basic functions:

- Select/internal control and CRU buffer
- Serial data transmission and reception
- Parallel data transmission

Select/Internal Control and CRU Buffer

On-board control operations are performed by a TMS 9901 programmable interface device which communicates with the I/O processor via the backplane. CRU signals, the external CRU space select line EXTCRU, and the CRU address bus are buffered and used to select individual serial board devices. The interface also services device interrupts and generates a tenth-level interrupt request on the backplane INT10 line.

The programmable interface occupies 32 bits of CRU address space, and the individual devices interfaced through the serial board occupy a total of 32 bits of CRU address space. The CRU concept and operations are described in Section 2.1.3.

Timing signals for the interface devices on the serial board is provided by dividing the backplane oscillator signal MHZ12 to 3 MHz. This signal is used by the interface devices for baud-rate timing and device operation.

Serial Data Transmission and Reception

Each serial port is controlled by a TMS 9902 universal asynchronous receiver/transmitter (UART). The transmission and reception parameters including baud rate, character size, number of stop bits, and parity are stored on programmable registers on the 9902 chip. Default parameters are set by the operating system when the machine is bootstrapped. These parameters may be changed by the user.

Buffered address lines 0 through 4 are used to select, process interrupts, and generate clear-to-send signals for each of the eight UARTs.

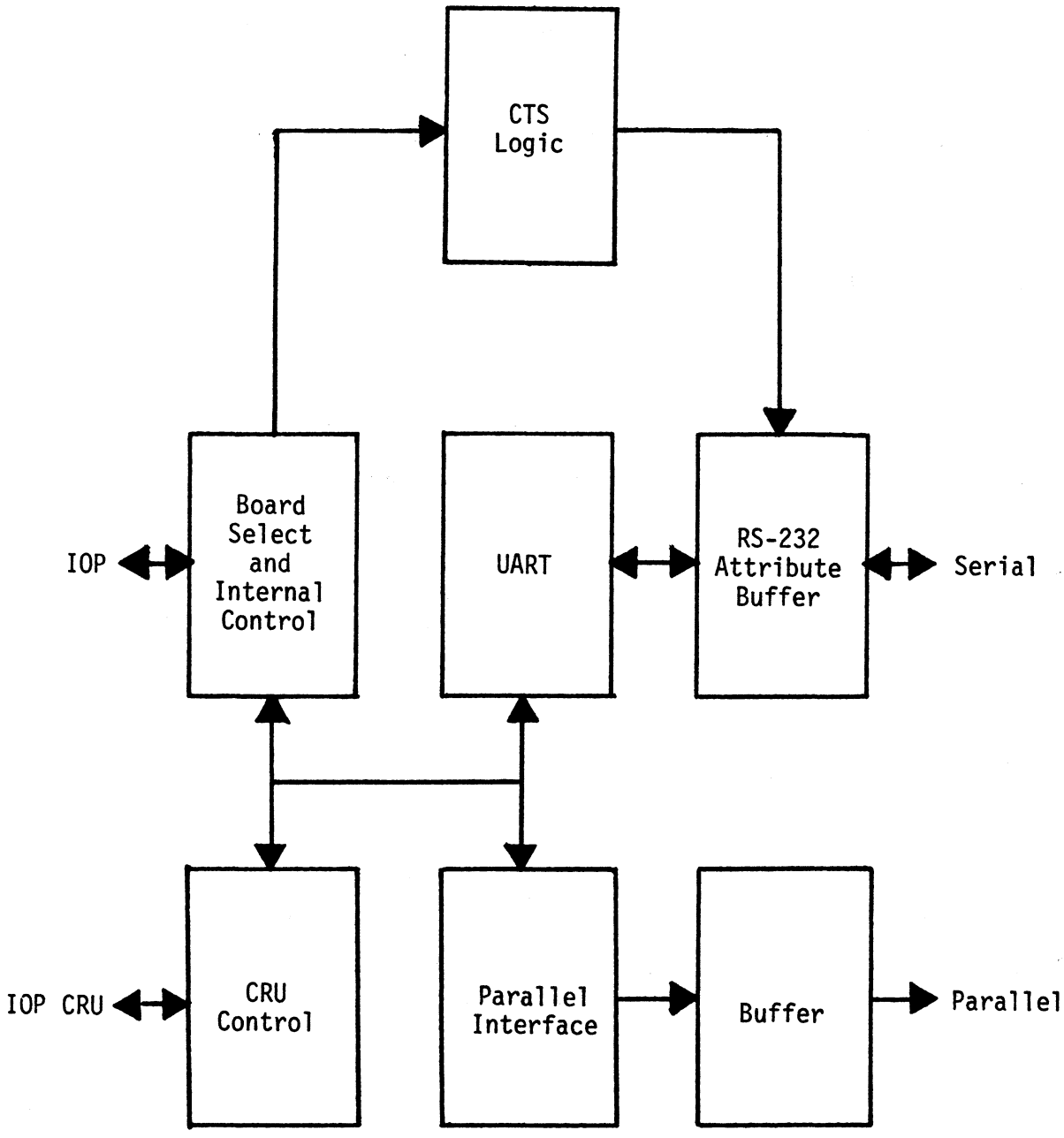


Figure 2-9. Serial Board

Parallel Data Transmission

Each parallel data port is controlled by a TMS 9901 parallel interface. Transmission rate and other parameters are programmable; as with serial transmission, the parameters are set to default values when the system is bootstrapped, and they may be changed by the user.

Buffered address lines 0 and 3 are used to select and respond to interrupts for the two interfaces.

2.3.4 Interface Specifications

RS-232C Serial Ports

Communication type:	Asynchronous, bit serial full-duplex
Xmit/receive:	Independently programmable rate 50 to 19,200 baud
Data Structure:	Start bit (logic 0) 5 to 8 character length 1, 1½, or 2 stop bits Odd, even or no parity
Line type:	EIA RS-232C protocol
Control signals:	Clear to send Request to send Data set ready Line control characters Flush buffer characters
Recommended mating connector:	Pixel p/n 160180-00 3M p/n 3485-1000

Parallel I/O Ports

Communication type:	Parallel data out, 8-bit with strobe Centronics-compatible Positive or negative data Positive or negative data strobe
Line speed:	Programmable
Control signals:	Acknowledge Busy On Line Paper Out Fault Reset
Recommended mating Connector:	Connector Pixel p/n 160131-00 AMP p/n 552138-1 Strain relief cover Pixel p/n 160135-00 AMP p/n 552073-6

Terminal Ports

Communication type:	(Refer to Sections 2.4 and 2.5.)
Recommended mating connector:	Plug Pixel p/n 160363-01 AMP p/n 205204-4 Pins Pixel p/n 160365-00 AMP p/n 66506-9

2.4 MONOCHROME TERMINAL CONTROLLER BOARD

2.4.1 Overview

The monochrome terminal controller board multiplexes video, control, and memory operations for one to four separate Pixel terminals. The controller uses a memory mapped design which allows up to eight pages of text to be shared among the terminals. Complete and separate keyboard control, character generation, and video signals are provided for each terminal.

The Pixel machine can accomodate one or two monochrome terminal controller boards. With two controller boards installed, eight terminals can be used. Controller #0 supports terminals 0 through 3, and controller #1 supports terminals 4 through 7.

Each controller board plugs into the card cage, and is connected by a ribbon cable to one of the two connectors on top of the serial board. The terminal connectors are mounted on the serial board; they are accessible through a cutout in the rear panel of the computer enclosure.

2.4.2 Functional Characteristics

Communication type:	16.2 kHz horizontal sync 50/60 Hz vertical sync 12.247 MHz video signal Bit serial data from keyboard Bell control pulse
Characters:	25 80-character line display area Complete 7-bit ASCII character set 7 × 10 character matrix Normal/reverse video User-selectable blinking cursor
Keyboard receiver:	Bit serial data, start and stop bits 8 bit word, even parity 2400 baud receive rate
Bell control:	User-selectable
Hardware options:	50 or 60 Hz operation Terminal controller #0 or #1

2.4.3 Block Diagram

A block diagram for the monochrome terminal controller board is provided in Figure 2-10. The controller is made up of five basic blocks:

- Processor interface
- Memory map and screen RAM
- Video control and addressing
- Video drive
- Keyboard receiver and bell control

Processor Interface

The processor interface includes board select, read/write control, and timing electronics. The interface controls the transfer of information between the external (backplane) and on-board buses with TTL latches.

The board is selected when the terminal external memory space select line $\overline{\text{SCROCAS}}$ is asserted and the external address bus bits 13 and 14 are zero. Address bit 12 is used to differentiate between operations involving controller board 0 and controller board 1.

When the board is selected, read/write signals from the backplane (BDBIN and $\overline{\text{WE}}$) are used to operate the address and data latches shown in the block diagram. $\overline{\text{WE}}$ is used to latch the address bus, the memory map and RAM during write operations, and BDBIN is used to latch the data bus during read operations.

Timing signals are generated by a 24.4944 MHz crystal oscillator. The oscillator signal controls a latch on a timing ROM; this is used to generate timing signals used by the various components of the board and column and row address strobes for the screen RAM.

Memory Map and Screen RAM

The terminal controller employs a memory-mapped design. The screen RAM (or display RAM) is a 16 kB × 8 array of dynamic RAM. The screen RAM stores 204 eighty-character lines of information in random order. The lines of information stored in the screen RAM are arranged by the memory map into the order in which they appear on the terminal screens.

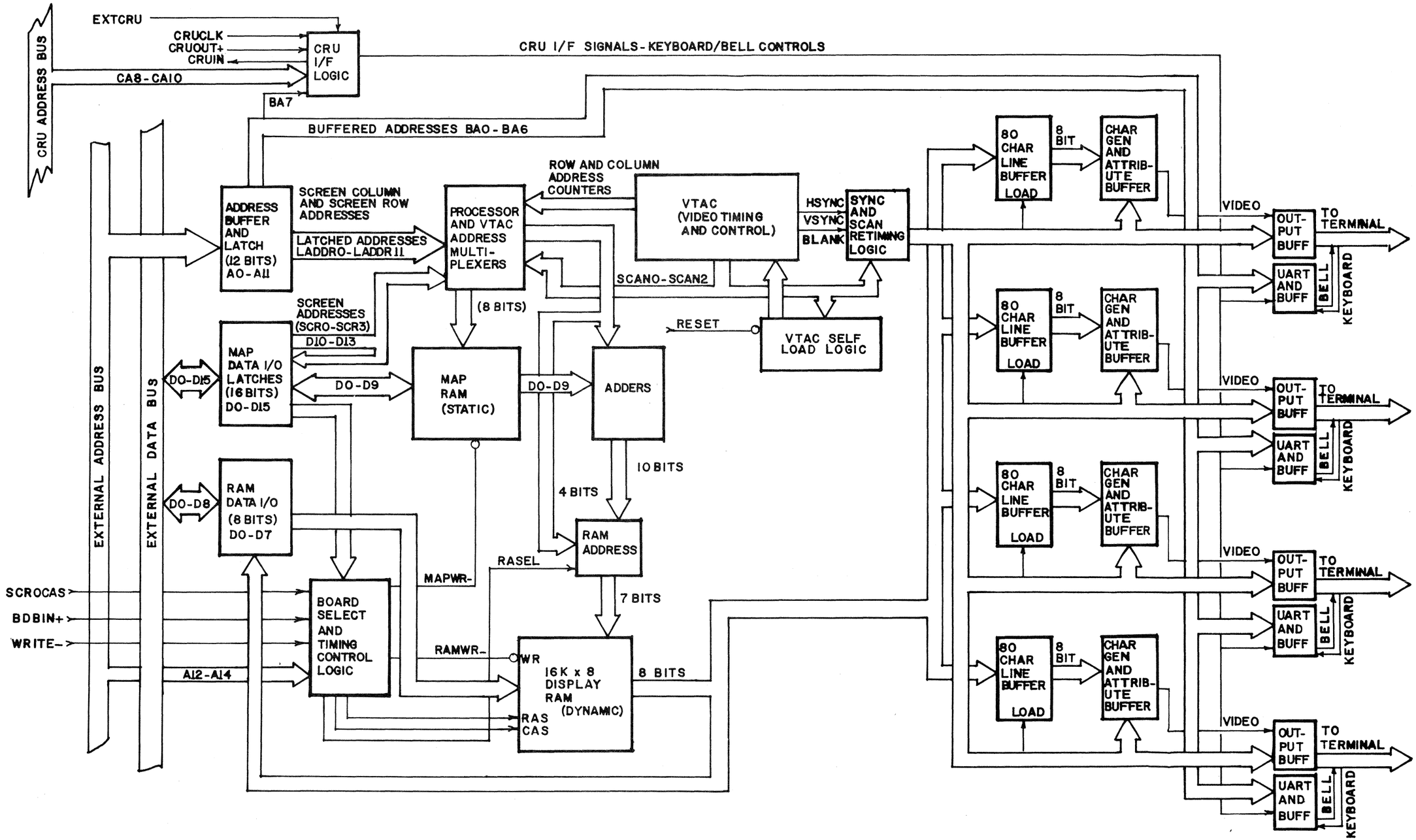


Figure 2-10. Monochrome Terminal Controller

The map is an array of static RAM. In addition to arranging the screen RAM data lines into display order, it is used for screen RAM refresh and for enabling or inhibiting actual screen display.

The map is divided into 16 sections called windows, numbered 0 through 15. Windows 0 through 3 are used for the four terminal screens. The terminal windows consist of a pointer which points to a line of blanks (used for retrace), and 25 pointers which correspond to the 25 lines of text on the display screen.

Windows 8 and 9 are used for refreshing the screen RAM. Writes to window 14 will turn the display off by disabling the horizontal sync signal, and writes to window 15 will turn the display on by enabling the horizontal sync signal. (Note: When the horizontal sync is disabled, power to the keyboard unit is disabled as well by the terminal's receiver board. Upon power-up, the horizontal sync is disabled to prevent screen trash from being displayed, and to prevent the keyboard from interfering with the system initialization.)

The other windows are reserved for future applications.

Screen RAM and map data may be modified by the I/O processor during the screen retrace; at other times the memory is busy transferring data into the line buffer and character generator for display on the user terminals.

Video Control and Addressing

The components responsible for video control and addressing include the video timing and control (VTAC) chip and its associated electronics, and the video multiplexing and RAM addressing circuitry. The purpose of these functional blocks is to transfer information from the screen RAMs to the actual screens.

The VTAC chip is a TMS 9927 video controller/timer, a programmable NMOS device. Parameters for the operation of Pixel terminals are stored on a self-load PROM; these parameters are loaded into the appropriate registers on the VTAC chip when the system is bootstrapped.

Raster-scan, row and column addresses from the VTAC are supplied to the processor and VTAC address multiplexers shown in the block diagram. This functional block generates an output character address which is sent to the adders. The line address from the map RAM is added to the character address from the

VTAC; the result is used to select the desired character code which is stored in the screen RAM.

Video Drive

The video drive processes information from the display RAMs and sync and scan information from the VTAC to generate the video signals which actually control the CRT display. The output of this section consists of horizontal and vertical sync signals, which govern the CRT's electron gun movement, and a video signal, which turns the electron gun on and off to produce white dots on the CRT screen.

The basic blocks of the video drive include an 80 × 8 shift register which serves as a line buffer, a character generator ROM which converts the character code into a dot-matrix character, and attribute buffers which generate the video signal and transmit it and the sync signals to the terminal.

Each terminal is assigned a complete and separate video drive section; there are four on each monochrome terminal controller board.

Keyboard Receiver/Bell Control

The previous sections have dealt with the video ouput sections of the terminal controller board. Each controller board also includes four entirely separate keyboard and bell control sections. These functions are performed by TMS 9902 UARTs. The UARTs receive the keyboard serial data stream and transmit the bell signal, serving as the interface between the terminal and the I/O processor.

The interface with the processor is conducted via the CRU backplane signals and the CRU address bus. Keyboard data will also generate a fourteenth-level interrupt on the backplane INT14 line.

2.5 TERMINAL

2.5.1 Overview

The terminal consists of a 25 line × 80 character cathode-ray tube (CRT) display, a typewriter-format keyboard, an audible signal (called a "bell"), and associated electronics. A cable connects the display to the computer module, and a four-conductor coiled cable connects the keyboard to the display.

A receiver board and display driver are mounted inside the display housing. The receiver board buffers the sync and video signals sent by the monochrome terminal controller and drives the bell. The display driver drives the CRT display.

The keyboard is equipped with a scanner which converts key transitions into a stream of serial data. The data stream and power for the keyboard are supplied via the four-conductor cable.

An AC line cord mounted on the back of the display supplies power to an IC-regulated power supply which powers the entire terminal unit. A rocker-type on/off switch is also mounted on the rear panel. 120 or 220 volt AC supplies are accomodated by an internal jumper.

2.5.2 Functional Characteristics

Video display:	Raster-scan monochrome display Grey phosphor Direct etched (non-glare) CRT
User controls:	Character intensity (contrast) Screen angle
Display area:	25 lines of 80 characters each
Keyboard:	Standard typewriter keyboard with additional command and function keys.
Audible tone:	User-selectable

2.5.3 Block Diagram

The main components of the terminal are the keyboard and the display, the latter consisting of a power supply, receiver board, display driver, bell, and CRT. These are interconnected as shown in Figure 2-11.

Receiver Board

The principal components of the receiver board are shown in Figure 2-12.

The receiver board buffers the sync, video, and bell signals. The buffered horizontal and vertical sync signals are sent to the display driver, while the buffered video signal is sent to the display driver through the intensity control mounted on the display housing.

The buffered bell control signal is used to control a tone generator which drives a small speaker mounted inside the display housing.

Display Driver

The principal components of the display driver are shown in Figure 2-13.

The video amplifier boosts the amplitude of the TTL-level video signal to about 30 volts; the video signal is then connected to the cathode of the CRT.

The vertical processor generates a ramp waveform synchronously according to the 50 or 60 Hz vertical sync signal. It also contains a power amplifier necessary to drive the vertical yoke of the CRT. Three potentiometers in the vertical processor section provide the standard adjustments for vertical hold, vertical size, and vertical linearity. The yoke can also be rotated by hand to level the display image.

The horizontal sync signal is first processed through a monostable multivibrator which generates a clean 25 µsec. pulse on the rising edge of the sync signal. The clean signal is applied to a horizontal output stage, the primary function of which is to supply the horizontal yoke with the proper horizontal scanning current. The size of the horizontal sweep—and thus

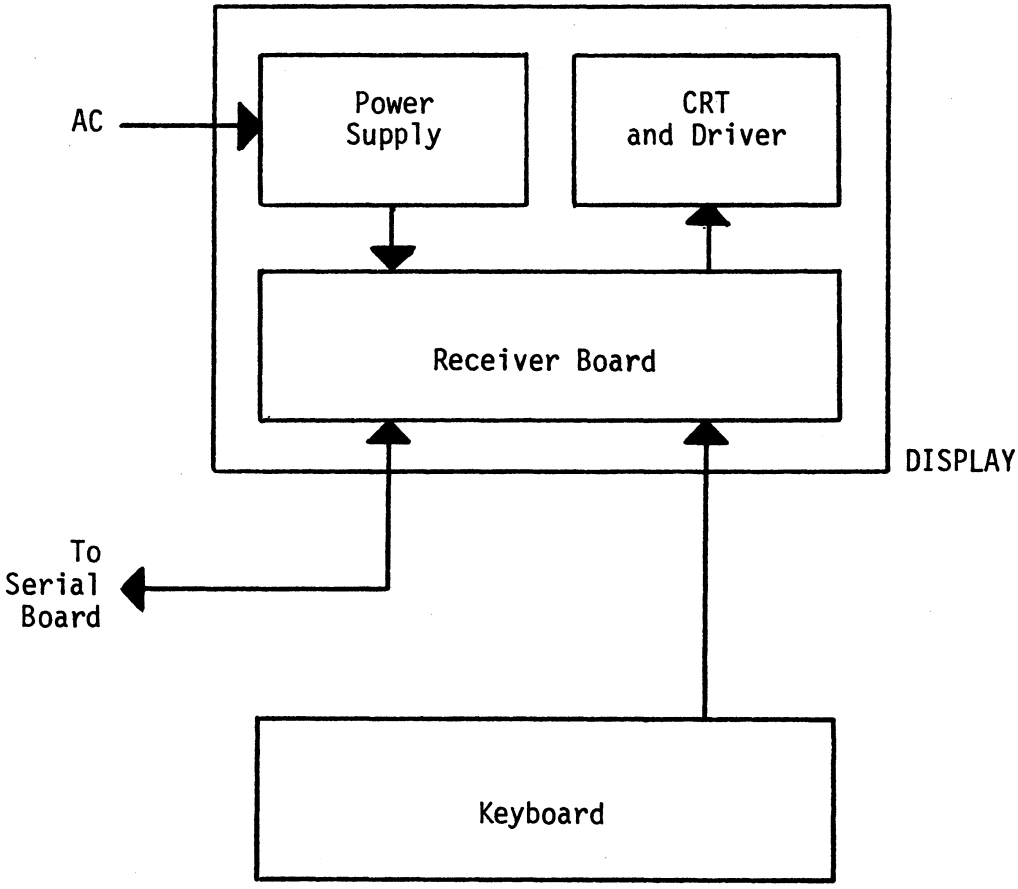


Figure 2-11. Terminal

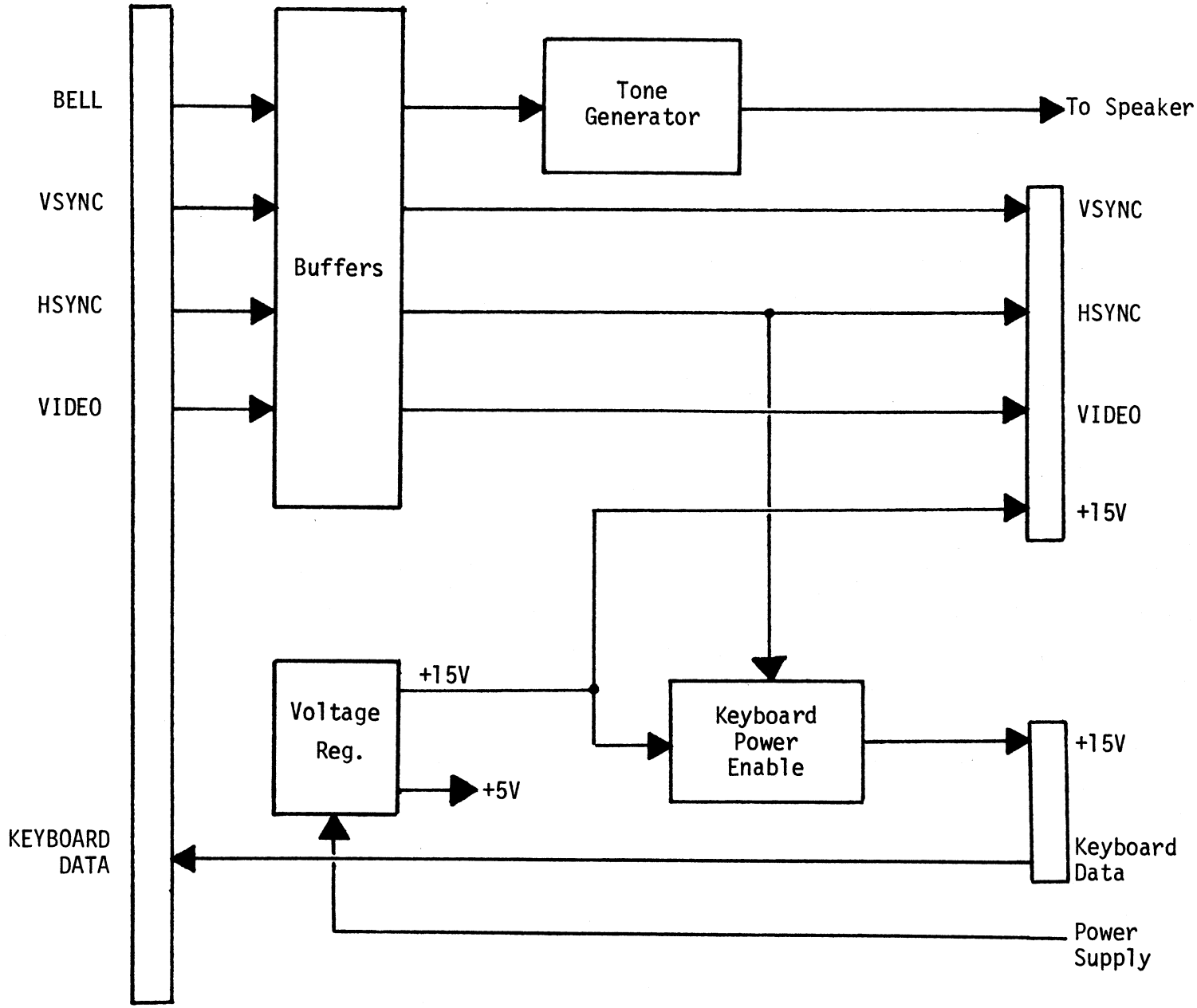


Figure 2-12. Receiver Board

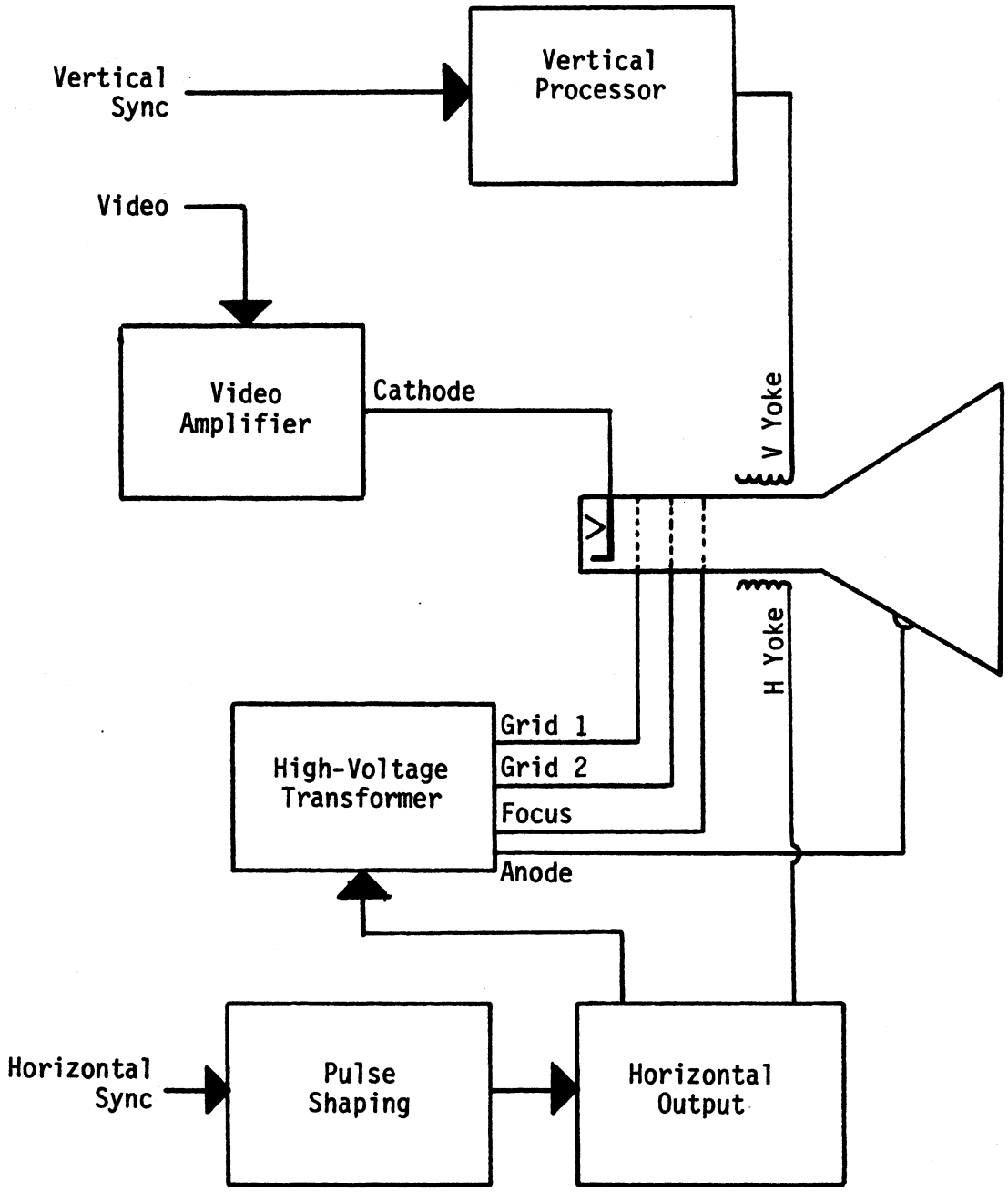


Figure 2-13. CRT and Display Driver

the width of the displayed characters—is adjusted by a slug-tuned coil.

The horizontal output section also supplies the primary of a power transformer which generates the high voltages necessary for grid bias and the anode. Grid #1 (at -150 v) regulates the overall brightness of the CRT screen; a potentiometer adjustment permits the brightmess to be controlled. Grid #2 (at +400 v) works with the cathode to draw the electron beam down the CRT. The focus grid (at +400 v) electrically focusses the beam; a potentiometer permits the focus to be adjusted.

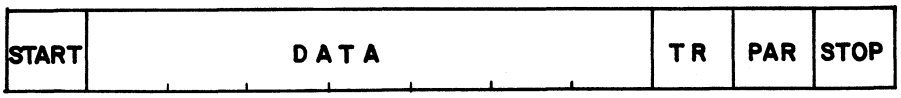
Power supply

The power supply consists of a transformer (which may be jumpered according to the input voltage), rectifier, and filter. It produces unregulated DC which is regulated to 15 volts by an IC regulator on the receiver board.

Keyboard

The keyboard contains an integral scanner which converts key transition information into serial data (in order to transmit it over a few wires).

The keyboard output is shown in Figure 2-14.



DATA: 7-bit ASCII

TR: Key transition- 0 = key down
1 = key up

PAR: Parity (even)

Figure 2-14. Keyboard Data

2.6 DISKETTE DRIVE CONTROLLER BOARD

> NOTE
>
> The diskette drive controller described in this section employs the single-density (FM) recording technique. It is expected that this module will be replaced by a controller supporting the double-density (MFM) technique in the near future.

2.6.1 Overview

The diskette drive controller board interfaces one or two diskette ("floppy disk") drives with the input/output processor and thus to the 100/AP system. The controller board allows the IOP to select a desired diskette drive, issue control signals, read status signals, and transfer data under direct memory access control. The controller board also includes bidirectional data conversion circuitry which converts the 16-bit backplane data words into the 8-bit data bytes stored on the diskettes, and vice versa.

The diskette drive controller is built around a single-chip MOS/LSI floppy disk controller. The programmable chip employs dedicated registers and data and control handling circuitry to operate the diskette drive.

One diskette drive controller board is required to interface with the one or two diskette drives used in the 100/AP system. A logic ribbon cable is connected to the top of the diskette drive controller board; the drives are then connected to this cable in "daisy chain" fashion--that is, all of the control and data signals are connected to both of the drives. The drives are selected (enabled) by asserting a drive select signal.

2.6.2 Functional Characteristics

Recording technique:	Frequency modulation (FM) Single side, single density
Diskette format:	Soft-sectored 512 bytes/sector 8 sectors/track 77 tracks Inverted data
Read/write:	Single/multiple sector Entire track Write precompensation
Registers:	Data Command Sector Track Status
Drive characteristics:	(refer to Section 2.7.2)

2.6.3 Block Diagram

The main components of the diskette drive controller board are shown in Figure 2-15. They include:

- FD1771 controller chip
- Select logic
- Data conversion circuitry
- DMA control
- Buffers

FD1771 Controller Chip

The FD1771 is a programmable interface device designed to transfer data between a floppy disk drive and a host (in this case, the IOP data bus), to issue control signals to the drive and status signals to the processor. The recording technique used is frequency modulation (FM), described in Section 2.6.4.

The FD1771 consists of a number of internal registers, a chip data bus eight bits wide called the data access lines (DAL), data separation circuitry, cyclic redundancy check (CRC)

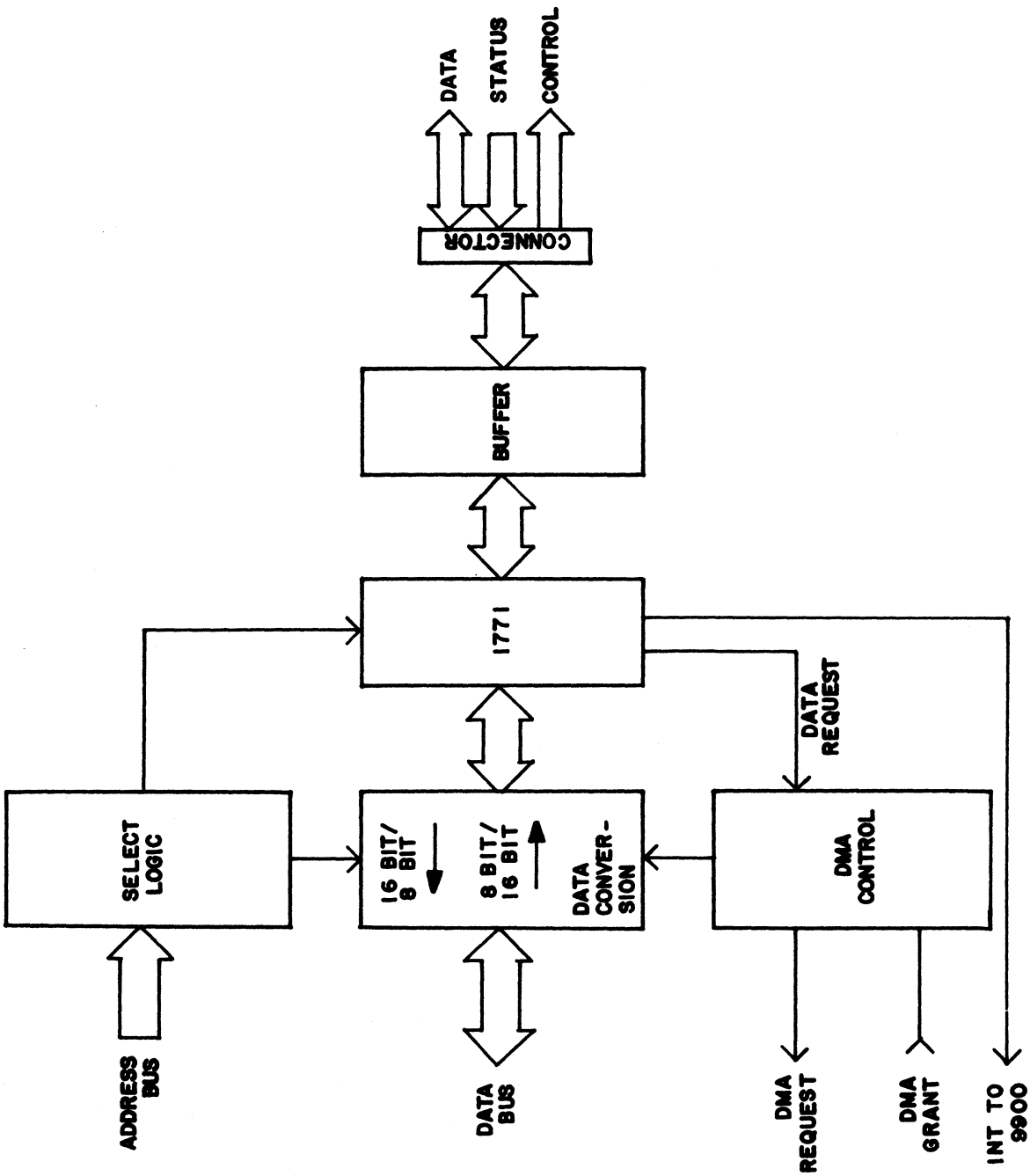


Figure 2-15. Diskette Drive Controller

character generation and detect circuitry, and timing and control logic which interprets the various signals and commands from the diskette drives and the central processor.

The on-chip registers include a command register, which accepts instructions from the IOP and performs the functions specified by the instructions. Examples of these instructions are read data, write data, step in or out, restore and seek. Sector and track registers contain the desired sector and track numbers. The controller chip compares the sector and track numbers recorded in the diskette ID fields with the numbers in these registers and moves the read/write head accordingly. The chip will also update the contents of these registers in response to specific commands such as step in or out, or seek to track 00.

A status register provides a status byte which can be read by the IOP. Individual bits of the status byte are set by the controller in response to the results of instructions or the status of the diskette drive.

The data register is used as a buffer during data transfer.

As the controller receives data or instructions, it will direct the diskette drive to move its read/write head to a desired location on the diskette, and read or write data in that location.

Registers are read and written via the eight DAL lines. The various registers are connected to the DAL lines according to a two-bit instruction on the backplane address bus (bits A0 and A1), and the value of A2, which is used to differentiate read and write operations.

Error detection is performed by checking a cyclic redundancy check (CRC) character which is recorded in each sector. The value of the CRC character is determined by dividing the data stream by the large polynomial

$$x^{16} + x^{12} + x^5 + 1.$$

The result is recorded in two CRC bytes which are checked by the FD1771 during read operations. If a CRC error is detected, the information in the status register is modified so that the system can attempt to recover the data. During write operations the FD1771 generates the proper CRC character and records it in the proper field on the diskette.

Timing and control circuitry interprets processor read and write commands, manipulates the registers described above, and

provides internal synchronization for the chip's operations based on the backplane signal MHZ12. It issues a data request signal to the DMA control interface (described below) and resets the data conversion circuitry at the beginning of data transfers. Interrupts required by the FD1771--to signal a non-recoverable CRC error, for example--are requested by the chip over the backplane line INT08.

Select Logic

The diskette drive controller board is enabled by the parallel I/O address space select line PIOCAS and an address on the IOP address bus, bits A07 through A13.

IOP address bit A03 is used to specify a control mode. When the control mode is selected, data transfers are inhibited and the low byte of the data bus (D00..D07) is used to select a drive. This drive select signal is latched until the controller board is deselected or the control mode is selected again.

Data Conversion Circuitry

In order to interface the 16-bit data word used by the processor and the 8-bit FD1771/diskette drive data byte, a data converter is used. The data converter converts the 16-bit word into two sequential bytes during write operations, and it converts the 8-bit byte into the higher or lower half of the data bus word during read operations.

Data conversion is performed with two pairs of flip-flops. One of the pairs is clocked by a high-byte enabling signal; the other is clocked by a low-byte enabling signal. One of the flip-flops in each pair is enabled during read operations and the other during write operations. The timing signals which enable the flip-flops are generated by the DMA control interface circuitry; they are reset at the beginning of data transfers.

The data conversion circuitry is disabled, and the low byte of the processor data bus connected to the FD1771 DALs when registers other than data registers (control, sector, track, and status) are being read or modified.

DMA Control

The direct memory access (DMA) control logic on the diskette drive controller board interfaces the FD1771 chip with the DMA controller on the I/O processor board.

The DMA concept, discussed in Section 2.1.3, permits the transfer of blocks of data from external storage devices (such as the diskette drive) and processor RAM memory. The DMA controllers on the processor board perform the transfer of data directly, without processor intervention.

During read and write, the FD1771 chip generates a signal when the data register is ready to receive or transmit data. The DMA control logic generates the appropriate DMA request signals, and responds to the DMA grant signals. The DMA control circuitry also generates high- and low-byte enabling signals for the data conversion circuitry.

2.6.4 Diskette Data Format

A diskette is a flexible oxide-coated recording disk mounted in a protective envelope. A diskette is illustrated in Figure 2-16.

The diskette itself includes a clamp area--where it is clamped by the motor in a disk drive and spun--and a recording area. The recording area is divided into 77 concentric rings called tracks. The track at the outermost edge of the diskette is called "track 00," and the innermost track is called "track 76."

An index hole is punched in the diskette so that when the diskette is spun, it will appear in a small hole in the jacket once per revolution.

Thus, a particular location on the diskette can be specified by a sort of polar coordinate--the distance from the center of the diskette (for example, track 39), and the amount the diskette has rotated since the index hole appeared in the opening in the jacket (for example, ninety degrees). In practice, the latter is specified either in time (microseconds), number of bit cells (locations where bits of data can be recorded), or by sector (one of eight general divisions of each track--roughly 45°, or 20,800 microseconds, or 5200 bit cells).

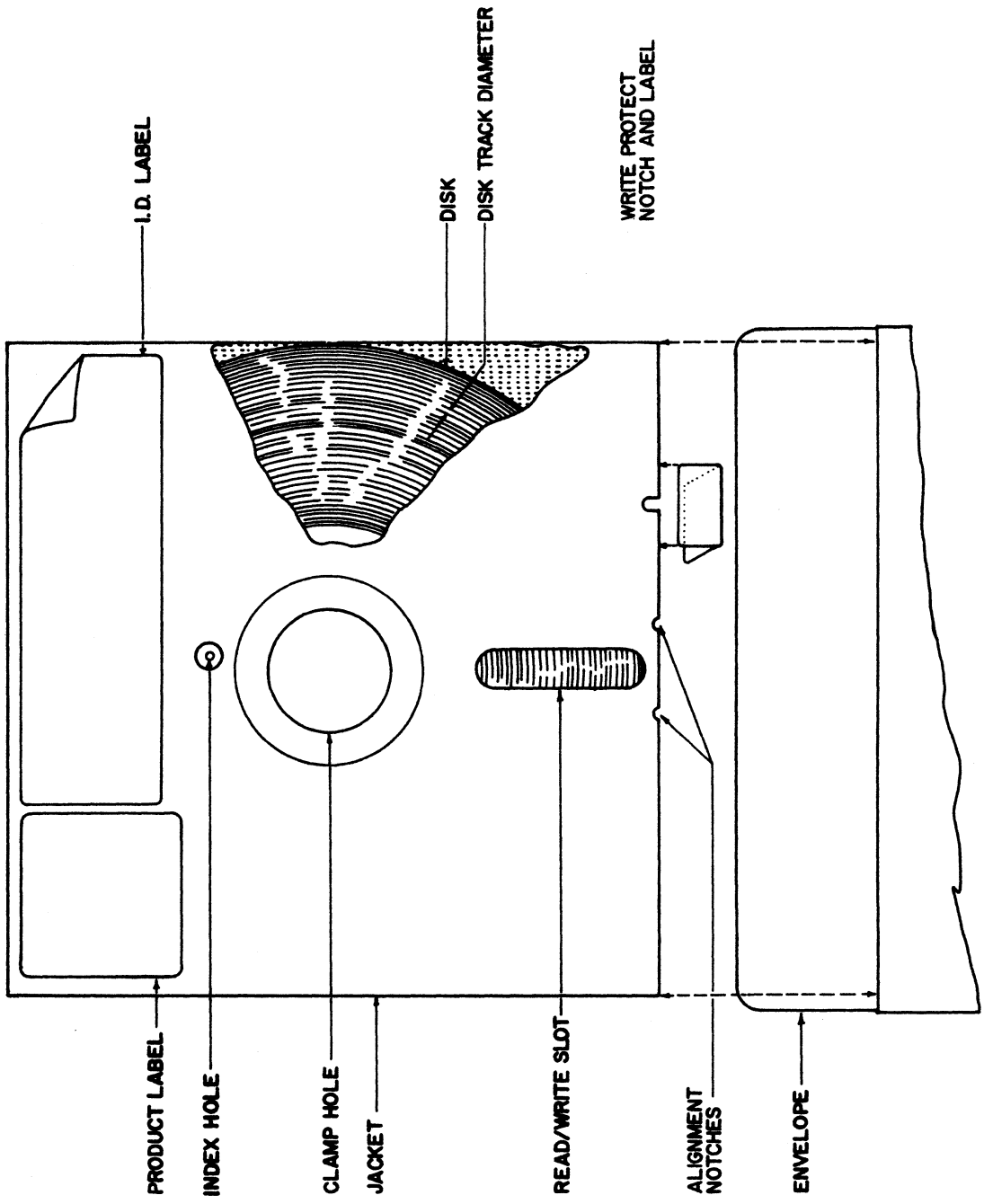


Figure 2-16. A Diskette

This section contains information on the following:

- The Frequency Modulation (FM) recording technique, which records clock and data pulses along a track to produce a self-clocking data stream, and
- The arrangement of data fields and other information on the tracks.

FM Recording

Each track consists of 41,300 bit cells, locations in which a binary number (one or zero) can be recorded. Data are recorded on the surface of the disk in pulses--tiny regions along the track where the magnetic surface of the disk is magnetized in the reverse direction. A bit cell is considered a "one" if there is a pulse in its center. If there is no pulse, then the bit cell is a "zero."

Clock pulses are also recorded on the surface of the disk. The clock pulses serve as a timing reference so that the disk drive electronics and the controller can tell where bit cells begin and end. The recording technique refers to the rules for the placement of clock and data pulses in the individual bit cells.

The FM recording technique records a clock pulse at the beginning of each 4-microsecond-wide bit cell. Data pulses, if any, are recorded in the center of a bit cell. Figure 2-17 shows how the binary number 11001010 would be recorded.

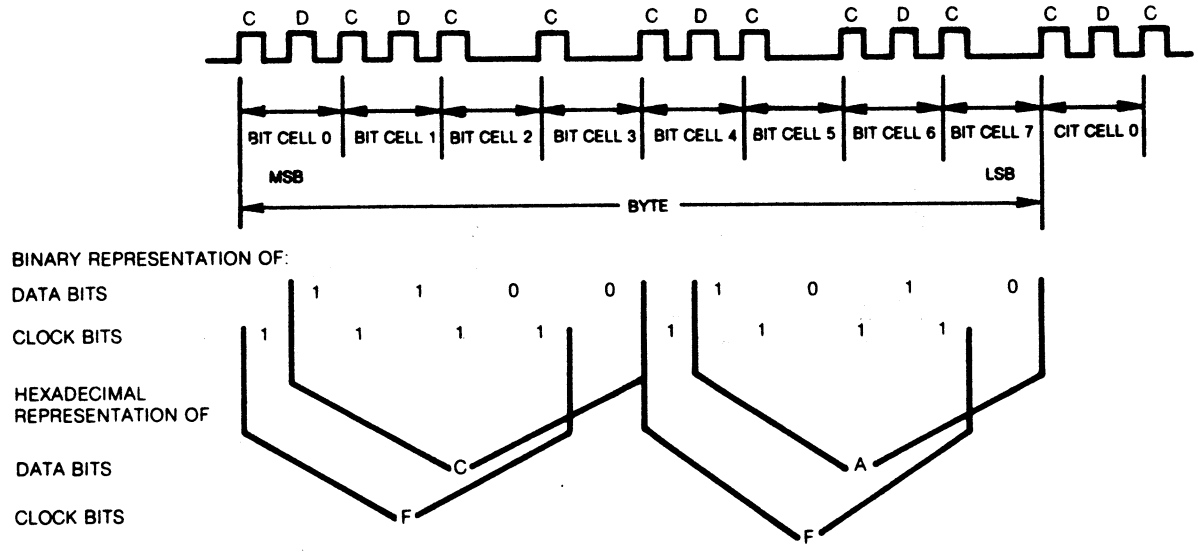


Figure 2-17. FM Recording Technique

Track Formats

In addition to user data, information is recorded on each track at the index location (the location on the track which corresponds to the index hole's appearing through the jacket opening), the track and sector number, and the two CRC check bytes. Gaps are also recorded along the track to delineate the various portions of the ID and data fields.

The format used in the 100/AP system is similar to the IBM 3740 format; Pixel, however, uses 512 byte sectors and inverted data (that is, the data recorded is the complement of the true data).

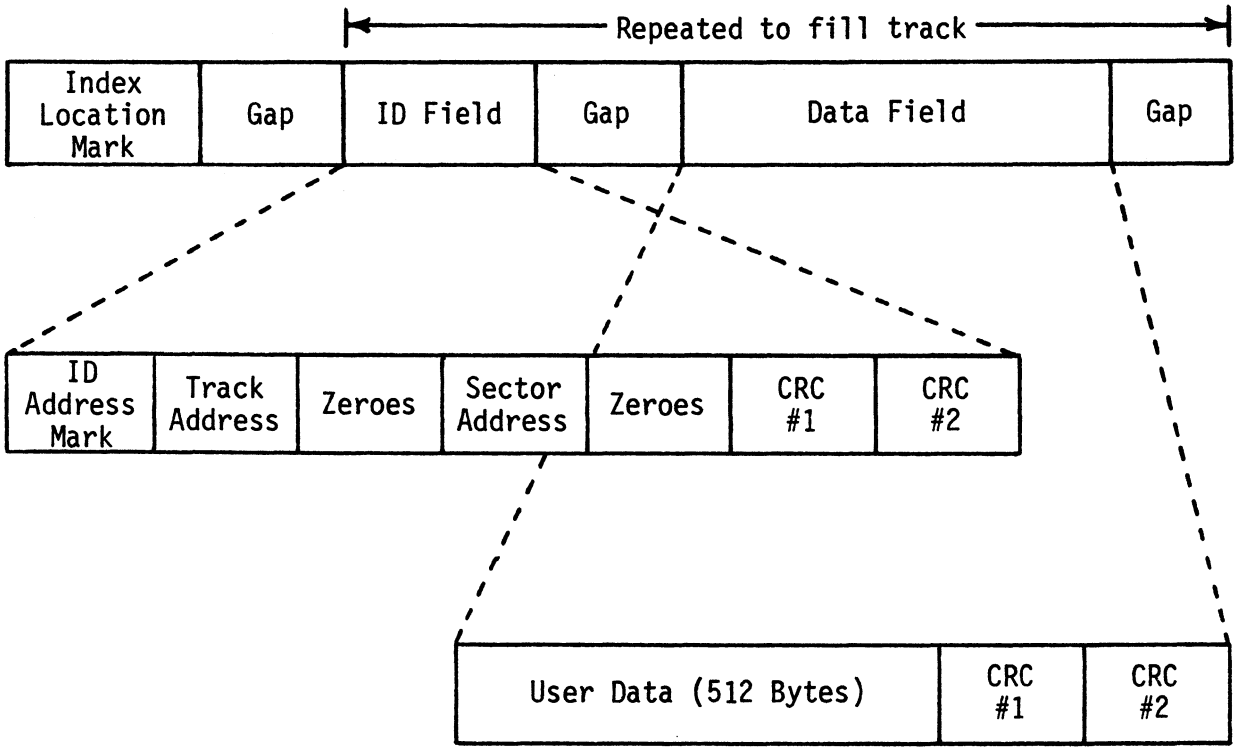


Figure 2-18. Diskette Track Format

2.7 DISKETTE DRIVE

2.7.1 Overview

The diskette drive performs the mechanical functions associated with locating, reading and writing data under the direction of the diskette drive controller described in Section 2.6.

The diskette drive includes a spring-loaded positioning mechanism which ensures that a diskette is inserted straight. The diskette is clamped to a registration hub when the drive door is closed; it is then spun at 360 rpm. A read/write head presses against the surface of the diskette for read and write operations.

Head positioning and loading commands are provided by the controller board.

The diskette drive mounts underneath the card cage in the Pixel machine so that its door is part of the lower front panel. The system may be configured with one or two diskette drives.

2.7.2 Functional Characteristics

Data format:	Single side, single density
Maximum storage:	3.2 Mbits unformatted 2.5 Mbits Pixel formatted
Transfer rate:	250 kbits/sec
Access time:	10.0 ms track-to-track 300 ms average 10.0 ms setting time
Latency:	83 ms
Head load time:	35 ms
Diskette type:	Industry standard 7.88-inch 3-mil Mylar diskette. Recommended vendors: 3M (p/n 741-5), Dysan

Functional Characteristics, cont'd.

Head type:	Ceramic single-element read/write head with straddle erase elements
Data density:	3268 bpi
Rotational speed:	360 rpm
Error rate:	Soft read errors: 1 per 10^9 bits read (software does recover) Hard read errors: 1 per 10^{12} bits read Seek errors: 1 per 10^6 seeks

2.7.3 Block Diagram

Control electronics for the diskette drive are packaged on a printed circuit board attached to the drive. This control circuitry interprets the signals sent to it by the diskette drive controller board. All of the diskette drive control signals are supplied to the diskette drives by a logic ribbon cable. Each drive is assigned a (jumper-selectable) number; the drive is selected when the drive select line corresponding to its drive number is activated.

A block diagram of the diskette drive is shown in Figure 2-19. These basic components of the drive will be discussed in this section:

- Drive system
- Stepped motor/head positioning system
- Head assembly
- Read, write, head load system
- Interlocks
- Index and Track 00 detect

Drive System

The diskette drive motor rotates a spindle at 360 rpm through a belt-drive system. A registration hub, centered on the face of the spindle, positions the diskette. A clamp that moves in conjunction with the cartridge guide fixes the diskette to the registration hub.

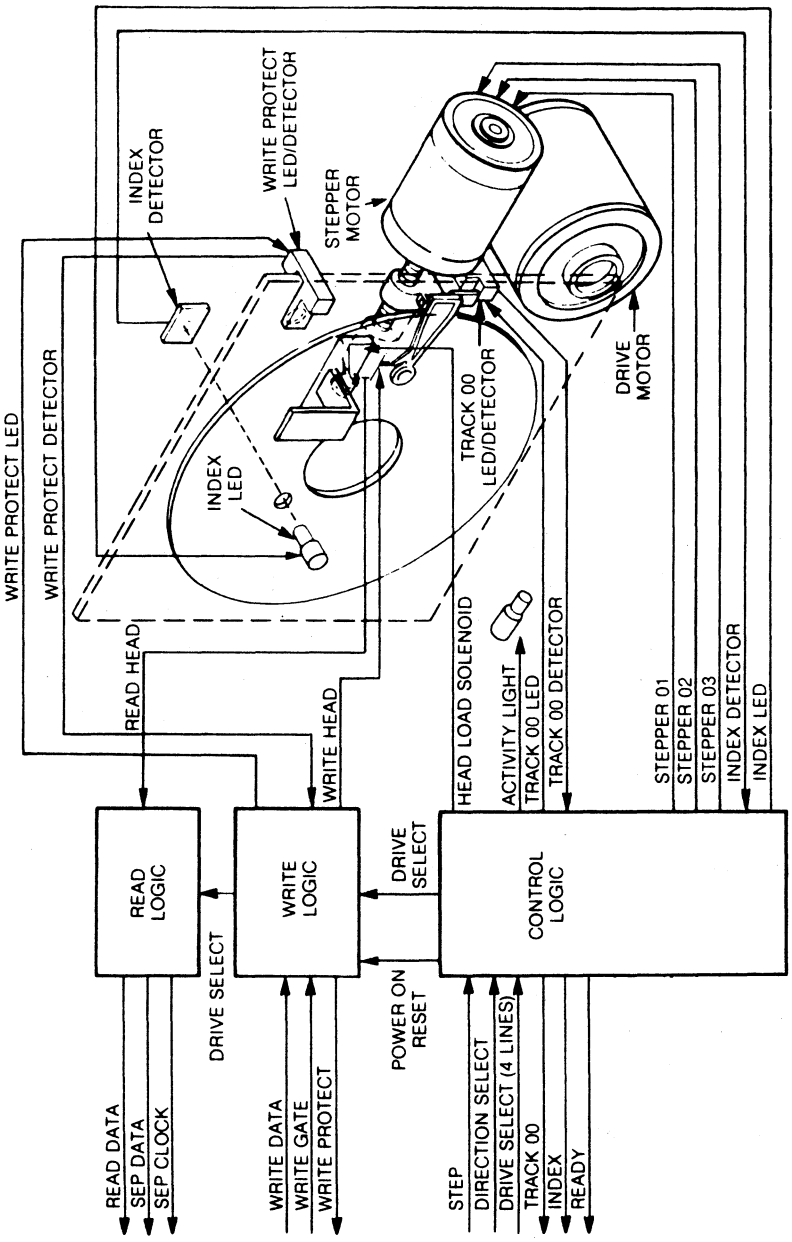


Figure 2-19. Diskette Drive

Diskette rotational speed stabilizes within 2 seconds of the application of AC power. Once the rotational speed has stabilized the disk drive can be accessed.

50 or 60 Hz line frequency is accomodated by changing the motor drive pulley and belt.

Stepper Motor/Head Positioning System

An electrical stepping motor and lead screw position the read/write head over a desired track. The stepping motor is a three-phase, 15-degree stepping motor.

The stepper motor is constructed so that its rotor turns 15 degrees in a clockwise or counterclockwise direction according to a sequence of signals applied to its windings. The drive control circuitry interprets step in/out commands and generates the proper sequence of signals. A fifteen degree rotation will move the read/write head in or out one track.

Head Assembly

The diskette drive uses a single-element read/write head with straddle erase elements which provide erased areas in between tracks. These erased areas ensure that normal interchange tolerances between diskettes and drives will not affect the readability and reliability of the diskette.

The read/write head is a ring with a gap and a coil wound around the ring. Current flowing through the coil will induce a fringe flux at the gap and magnetize the oxide recording surface in a horizontal direction. A bit is recorded by reversing the current in the coil. This causes the fringe flux to reverse and magnetize the oxide recording surface in the opposite direction. A recorded bit is shown in Figure 2-20.

During a read operation, a magnetization reversal on the diskette surface will reverse the flux direction in the gap, causing a voltage pulse to appear across the coil. The read operation is illustrated in Figure 2-21.

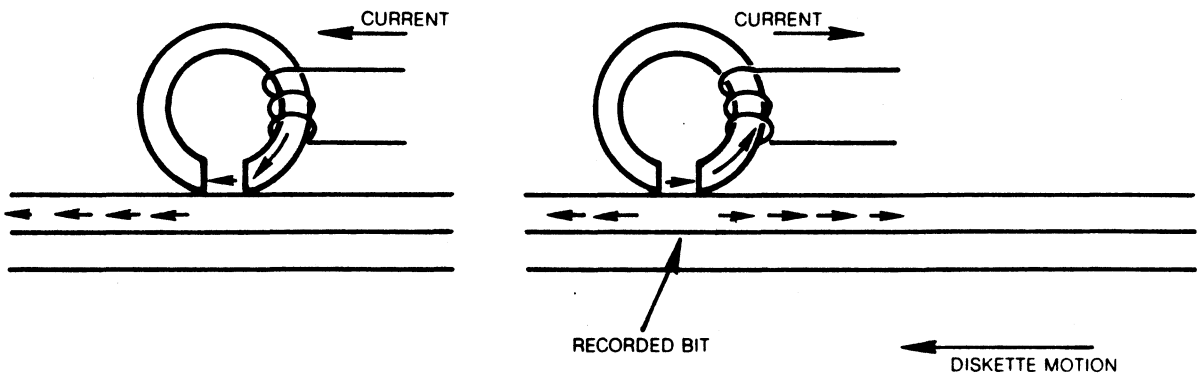


Figure 2-20. Writing a Bit

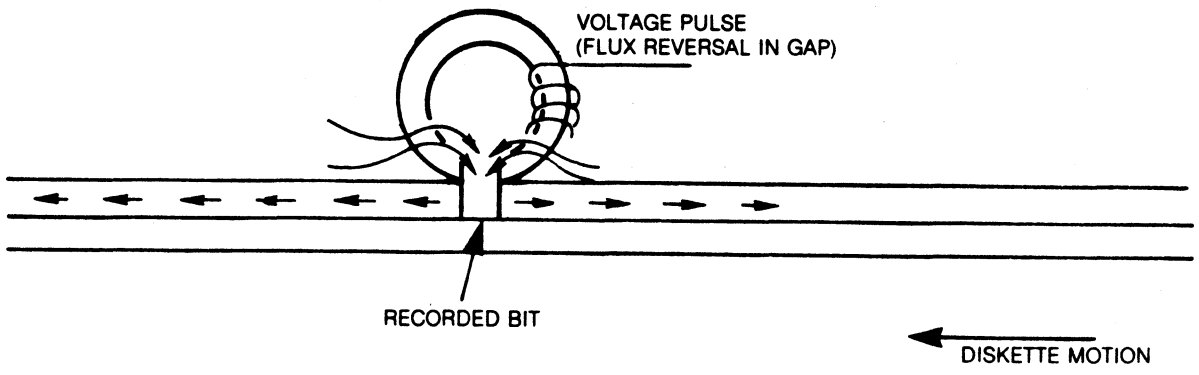


Figure 2-21. Reading a Bit

Read/Write and Head Load System

Before a diskette can be read or written, the read/write head must be loaded. The diskette drive controller issues an instruction to the diskette drive to load the head. This activates a solenoid which causes a spring loaded head load pad to press against the surface of the diskette. The head load pad and the read/write head move in tandem, with the diskette sandwiched in between.

When write data are received, the drive mixes the data with clock pulses. The result is used to trigger two write drivers which then write data on the diskette as described in the previous section. An erase driver also senses the write operation to activate the straddle erase elements.

When reading data, the read/write head generates a rough sine wave. The useful information is contained in the frequency modulation of the sine wave; although the amplitude of the wave also varies, it contains no useful information. The read signal is amplified and filtered to remove noise spikes, then fed into a differential amplifier which amplifies the read signals to even levels. A detector and pulse shaper is used to generate the clock/data stream interpreted by the diskette controller.

Interlocks

The diskette drive includes two electrical interlocks which prevent diskette damage and protect valuable data.

A door open switch prevents the drive from being in a READY condition until after the door is closed. It is operated by the mechanical operation of the door.

The write-protect detector senses the presence of a write-protect notch (used on some diskettes). If the write-protect notch is not covered, diskette write operations are inhibited. The write-protect detector consists of a light-emitting diode and a phototransistor.

Note that these interlocks do not prevent the drive from being powered up or down with a diskette mounted and the door closed; this will damage diskettes and must be avoided by the user.

Index and Track 00 Detect

The index and track 00 detector are used to identify the index radius of the diskette and the outermost data track. Section 2.6.4 describes how these reference points are used by the diskette subsystem.

Both the index detector and the track 00 detector are light-emitting diode (LED) and phototransistor assemblies. The index detector shines through the hole in the diskette jacket and generates a pulse when the index hole passes by each revolution. In addition to serving as a reference point, this also allows the diskette drive control circuitry to determine that a diskette is properly positioned and that its rotational speed is stable.

The track 00 detector senses a flag on the read/write head carriage assembly when the read/write head is at the outermost track (track 00).

2.8 WINCHESTER DISK DRIVE CONTROLLER BOARD

2.8.1 Overview

The Winchester disk drive controller board interfaces from one to four Winchester technology disk drives with the input/output processor and thus the entire 100/AP system. The controller board allows the IOP to select a particular Winchester disk drive, issue control signals, read status signals, and transfer data under direct memory access control. The controller board also includes bidirectional data conversion circuitry which converts the 16-bit backplane data words into the 8-bit data bytes stored on the Winchester drives, and vice versa.

Because of the high transfer rate of the Winchester technology drives (4.34 Megabits/second) and the complexities of data separation inherent in the MFM recording technique, the controller board contains an 8X300 central processing unit--a four million instructions per second microcontroller supported by an 8 Megahertz clock. The CPU drives an eight-bit I/O bus, over which most of the on-board data manipulations take place. Five special-function LSI chips are also utilized. These chips provide address mark detection, serial-to-parallel and parallel-to-serial conversion, CRC generation and checking, and MFM encoding and precompensation.

The Winchester controller board mounts in a single position of the card cage. A single ribbon, connected in daisy-chain fashion, supplies control signals and reads status signals for all of the Winchester drives. A separate ribbon cable is also provided to each drive for data transfer.

The Winchester controller supports one to four drives in any combination of capacities. The drives are discussed in Section 2.9.

2.8.2 Functional Characteristics

Encoding method:	Modified frequency modulation (MFM)
Drive type:	(refer to Section 2.9)
Registers:	Data Command Status Error Sector count and number Cylinder Size/Drive/Head
Commands:	Restore Seek Read sector Write sector Format track
CPU:	8 MHz 8X300
Memory:	1024 × 8 sector buffer RAM 1024 × 8 fast I/O program ROM 1024 × 16 program ROM

2.8.3 Block Diagram

Block diagrams for the Winchester disk drive controller are provided in Figures 2-22 and 2-23. (Figure 2-23 is a further breakdown of the "data separator" block shown in Figure 2-22.)

This section will consider these functions and components:

- CPU and I/O bus
- Fast I/O
- IOP interface
- Board control
- Drive control
- Data reading
- Data writing

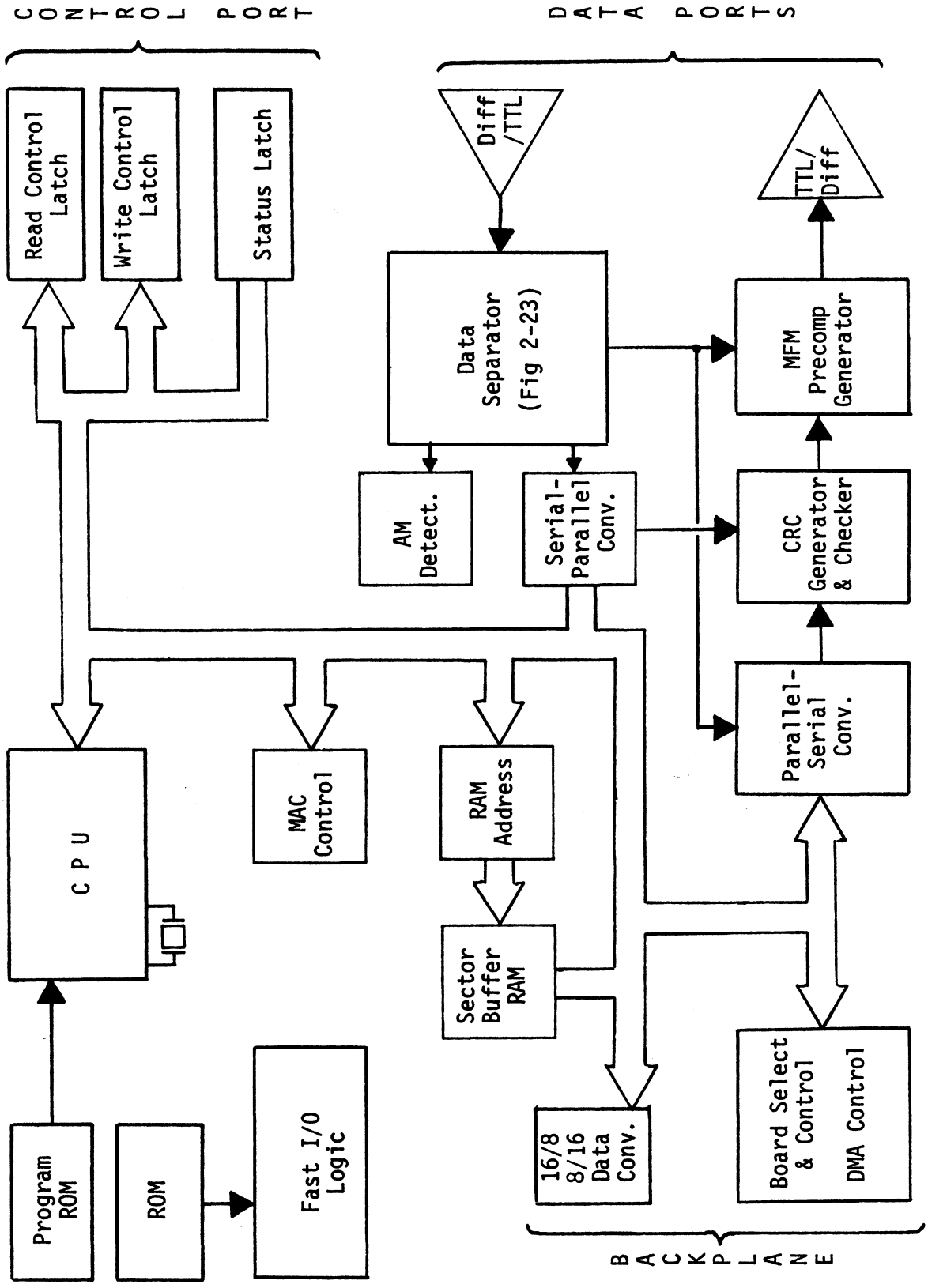


Figure 2-22. Winchester Disk Drive Controller

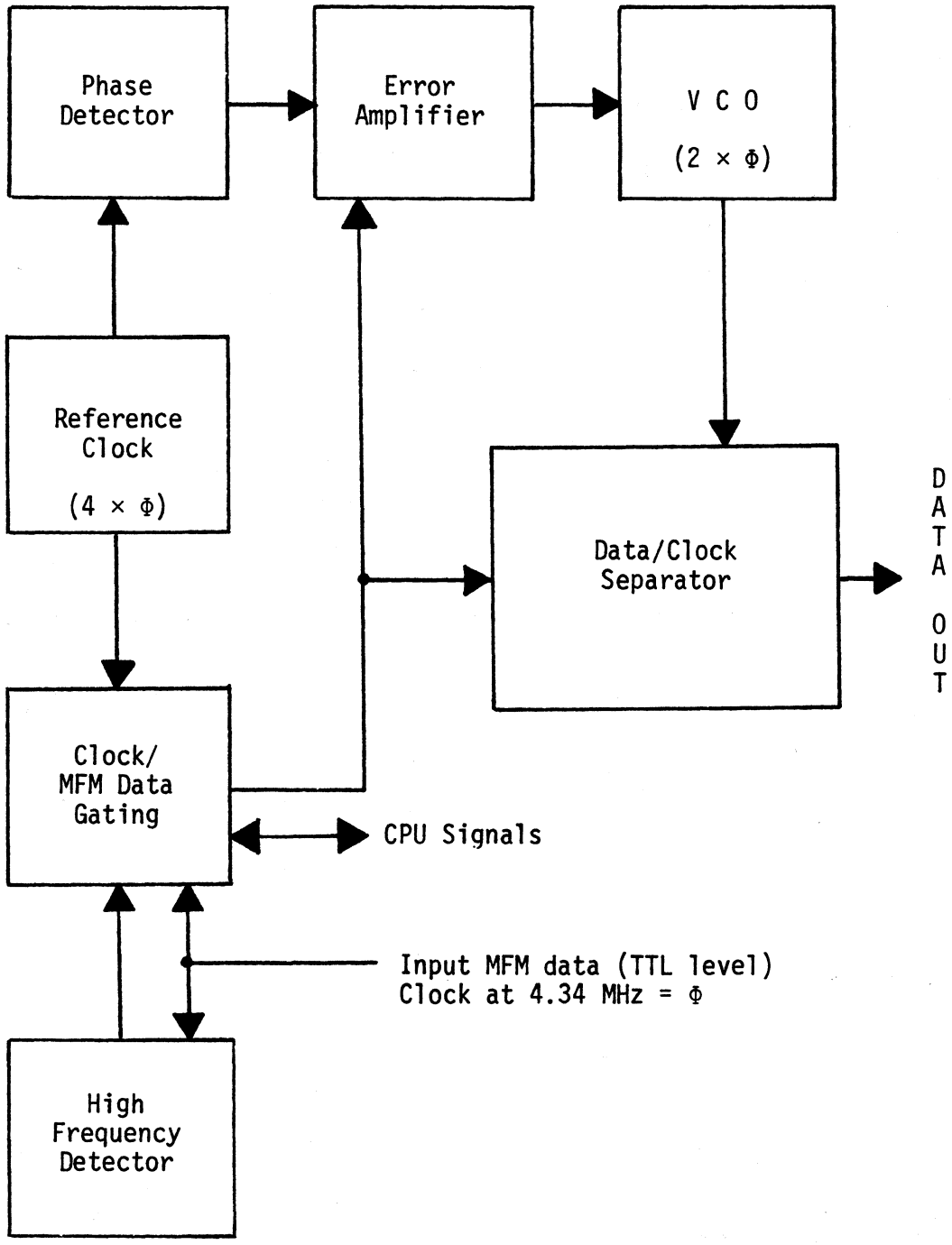


Figure 2-23. Data Separator

CPU and I/O Bus

The on-board central processor ultimately controls all of the functions of the Winchester controller board. The CPU is an 8X300, a high-speed microprocessor implemented with bipolar Schottky technology. Running on an 8 MHz clock the CPU will fetch, decode and execute instructions in 250 ns--a speed required by the high transfer rate of the Winchester drives.

The 8X300 does not support common address and data buses; rather, it supports an instruction address bus, an instruction bus, and an eight-bit I/O vector bus. The instruction address and instruction buses are connected to a program ROM. The I/O vector bus is used as the on-board I/O bus.

Bus arbitration signals are used by the 8X300 to control the transfer of data. A write control signal WC is used to determine the direction of data transfers. Select control, SC, indicates that an I/O address appears on the I/O bus. These signals are NORed to produce a composite signal which indicates an access to any port. This arrangement allows 8-bit immediate data moves within one 250 nsec instruction cycle.

The 8X300 is held on reset for approximately 40 msec after power on by an RC network and Schmitt trigger to allow the board to be properly initialized. It can also be reset by an IOP command.

Fast I/O Logic

For faster speed, and to unburden the 8X300 from a number of functions, the fast I/O logic section is used to strobe a number of functional blocks during read and write operations. The fast I/O logic is supported by ROM memory, and is clocked by a strobe signal from the 8X300 during each instruction cycle. The NORed WC/SC signal described above is used to select read strobes or write strobes.

Throughout the circuit, output ports consist of D-type latches which use one of the write strobes to latch data into the ports.

Read strobes are used to enable tri-state output devices on the I/O bus. Read strobes are also used to clock the data request and interrupt request latches, and one read strobe is left unused as a "dummy" for instructions which do not require data from a port.

IOP Interface

The IOP interface section of the Winchester controller performs several functions. It allows the IOP to select (over the address bus) registers and to read or modify them (via the data bus). It generates the DMA request signal and responds to the DMA grant. It enables the board by decoding an address in the PIOCAS address space. It also includes a data converter which converts the 16-bit backplane word into an 8-bit Winchester drive byte, and vice versa.

Instructions to the Winchester controller are sent by the IOP over the address bits A0..A2. Read or write operations are specified by the state of A3. These instructions are strobed onto the I/O bus via a latch operated by one of the fast I/O select strobes. Read/write specifications are decoded and sent to a number of functional blocks on the board. The 8X300 interprets these instructions based on the program stored on its ROM.

The IOP can also write a control byte and read a status byte on the data bus.

The DMA logic section is used to generate a DMA request signal in response to a data request signal from the 8X300. It also provides the timing signals for the data converter, which consists of two pairs of flip-flops which alternately gate the low and high bytes of the data word onto data access lines (DAL). The DALs are strobed onto the I/O bus by the Fast I/O logic.

Board Control

In addition to the basic board control signals generated by the CPU and the IOP interface logic, the board contains a dedicated 6-bit control port called MAC CNTRL. MAC CNTRL enables the functions of the WAIT control circuitry, CRC generation, the gating of read data into the data separator, selection of read or write functions, control of the CRC output, and address mark (AM) detection. MAC CNTRL values are latched into the port by a write strobe.

The functions of the MAC CNTRL signals is discussed further in the sections which consider the individual functional blocks.

Drive Control

The drive control cable is interfaced to the Winchester controller via three latches which connect the input or output information to the I/O bus when strobed by the fast I/O logic strobe signals. One latch, with the head select signals 2^0, 2^1, and 2^2 and drive select DS1 through DS4, is used to select the desired disk surface. Another latch provides the control signals WRITEGATE, RWC, STEP PULSE, and DIRECTION IN.

A third latch allows the Winchester controller to read the status signals INDEX, TRACKØØØ, SEEK COMPLETE, WRITE FAULT, and READY.

Data Reading

The Winchester controller will read a sector of data in response to the "read sector" command from the IOP. The IOP issues the appropriate commands by placing a command register request code on the address bus, and the op code for the read sector command on the data bus. These instructions will be latched onto the I/O bus by the Fast I/O select logic.

The Winchester controller will select the appropriate disk surface, position and load the head, and MFM data will appear at its MFM data input port. The data are processed through a differential-TTL demultiplexer, which converts the differential signal into a clean, TTL-level MFM signal.

The MFM data are then fed into a data separator, illustrated in Figure 2-23. At this point the clock and data signals are still mixed. (Note: If you are not familiar with MFM recording, refer to Section 2.8.4 before reading further.) The signal appears as a series of 50 nsec active high pulses spaced at 1, 1.5, and 2 times the clock period. This data is presented to the Clock/MFM Data Gating circuitry which will gate either a reference clock or MFM data into the first stage of the Error Amplifier circuitry.

The reference clock is a crystal oscillator cut to $4\times\Phi$, where Φ is the MFM clock frequency (equal to the transfer rate, 4.34 MHz). The clock is divided to provide a $2\times\Phi$ signal for read purposes and a $1\times\Phi$ signal for data writing.

The input MFM data is also fed into a High Frequency Detector, which detects the steady high frequency signal which would be produced by a stream of all ones or all zeroes.

The VCO (voltage controlled oscillator) is designed to lock on to the frequency and phase of the MFM data so that the Data/ Clock Separator section can remove the clock pulses from the MFM data stream. A voltage is applied to a hyper-abrupt tuning diode which forms part of a discrete LC oscillator. As the voltage varies, the capacitance of the diode varies, pulling the frequency up or down. Control of the VCO is performed by an error amplifier, which is fed by a phase detector. The error amplifier is a balanced differential amplifier followed by a filter stage. Whenever the VCO is running too slow, the error amplifier receives data pulses before pulses from the VCO. This causes the error amplifier to produce pump-up pulses which are integrated by the filter and adjust the voltage applied to the hyper-abrupt tuning diode. When the VCO is running too fast, pump-down pulses are fed into the filter.

The phase detector supplies the error amplifier with time windows approximately 50 nsec in length, during which the leading edges of the MFM data can be compared with the VCO. Initial oscillation of the VCO is accomplished by an oscillator set to the nominal frequency; it is then enabled by a string of ones or zeroes from the high frequency detector. The regular high frequency signal initializes the phase detector/error amp/ VCO section.

Once the VCO has been locked onto the phase of the oncoming data, the actual separation of data and clock can occur in the Data/Clock Separation section. A technique called "window extension" is used. Data bits first have their leading edges shifted into the center of the VCO half cycles; they are then latched or extended until the next rising edge of the VCO clock. Due to this extension technique, bits can be shifted approximately 1/4 of the VCO clock period without being lost.

A pair of latches are connected to the phase detector delay line to generate a delayed-data and a delayed-clock signal. These are fed into the data/clock separator as well, and are used to differentiate data from clock pulses in the MFM stream.

MFM data which has been separated to form data and clock signals are then processed by circuitry which prepares it for parallel processing by the 8X300. This circuitry is shown in Figure 2-22. It includes three LSI chips which perform the essential functions:

- Address Mark (AM) detection
- CRC checking
- Serial to Parallel conversion

Address marks are patterns of data and clock signals which cannot be recorded by MFM recording rules. AMs are used primarily to identify the byte boundaries of data, and also to confirm that the data and clock separation was performed properly.

After an address mark has been detected, the data are fed into a serial to parallel converter. The converter arranges the serial data into parallel bytes, and sets a flag to signal the processor.

The CRC checker calculates the CRC value (in the same way as the diskette drive controller, refer to p. 2-46) and compares it with the recorded CRC value, flagging the processor if an error is found.

As bytes of data are read, they are stored in the sector buffer RAM. The RAM addressing block functions as a counter and automatic address generator to allow an entire sector to be read in. The data are then DMAed into the processor memory by the DMA controllers on the IOP board.

Data Writing

Data writing is a much simpler operation that data reading. Most of the functions are performed by single-chip blocks, including:

- Parallel to Serial conversion
- CRC generation
- MFM encoding and Precompensation

Data are written to the disk, first by issuing the proper commands, and then by loading the data into the sector buffer RAM.

The parallel to serial converter takes data off the I/O bus and converts it into a serial data stream. The stream is processed by the CRC generation chip which calculates the CRC characters and writes them into the appropriate spots at the end of the serial stream.

The MFM encoder accepts the serial data stream and a 4.34 MHz write clock (an output from the reference clock in the data separation block) and converts them into an MFM data stream according to the MFM encoding rules (refer to Section 2.8.4).

The precompensation circuitry included in the MFM generator chip is designed to minimize the effects of "dynamic bit shift" on the positions of the recorded bits, particularly on the inner tracks where the greater flux density aggravates the problem.

Dynamic bit shift is caused by the magnetic effects of adjacent bits on one another. The precompensation logic examines the bits' magnetic environments and determines whether they should be written early, late, or on time in order to compensate ahead of time for the expected bit shift. The early, late, and on time outputs are shifted through delay lines to effect the precomp.

The precompensated, MFM data stream is then buffered through a TTL to differential multiplexer and sent to the disk drive for writing onto the surface of a disk.

2.8.4 Winchester Recording Format

This section contains information on the following:

- The Modified Frequency Modulation (MFM) recording technique, which records clock and data pulses along a track to produce a self-clocking high-density data stream, and
- The arrangement of data fields and other information on Winchester tracks.

MFM Recording (cf. FM RECORDING, p. 2-50)

Each Winchester track includes approximately 83,000 bit cells, locations in which a binary number (zero or one) can be recorded. Data are recorded on the surface of the disk in pulses--tiny regions along the track where the oxide surface of the disk is magnetized in the reverse direction. A bit cell is considered a "one" if there is a pulse in its center. If there is no pulse, then the bit cell is a "zero."

Clock pulses are also recorded in the bit cell, at the leading edge of the cell as in FM encoding, but only if the bit cell and the bit cell before it are both zeroes. This technique ensures that pulses along the track will never be closer than one bit cell apart; consequently, the bit cell can be made smaller.

Track Format

The Winchester track format is given below. The CRC characters and address marks (AM) are described in the previous section.

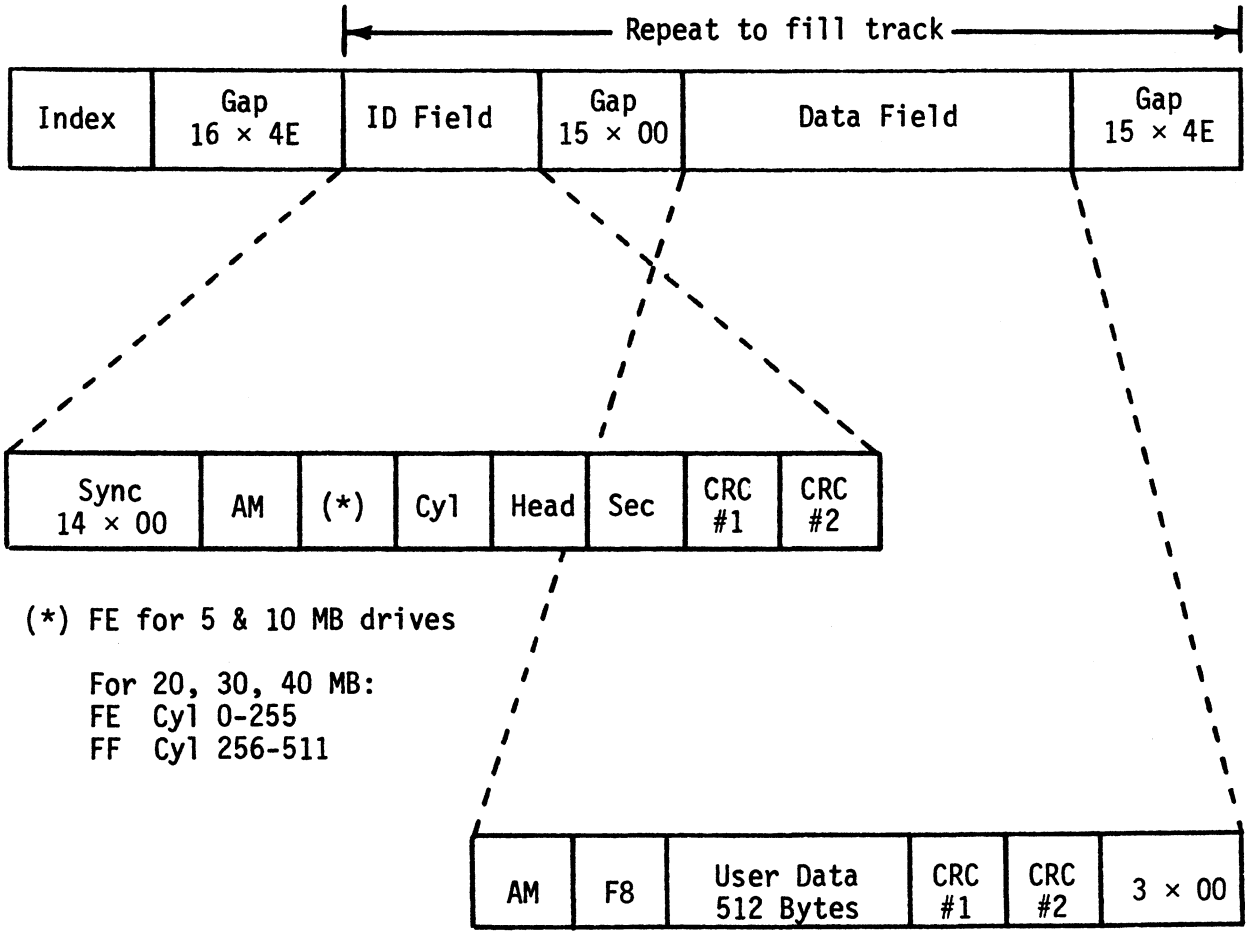


Figure 2-24. Winchester Track Format

2.9 WINCHESTER DISK DRIVE

2.9.1 Overview

The Winchester disk drive performs the mechanical functions required to locate, read, and modify data stored on rigid, non-removable disks under the control of the Winchester disk drive controller board described in Section 2.8.

The term "Winchester" refers to several features which allow data to be stored densely and recovered reliably. These features include:

- An environmentally sealed chamber for the disks and read/write heads which eliminates contamination,
- A lubricated disk surface which allows the aero-dynamically designed read/write heads to take off and land anywhere on the disk surface without damaging the heads or media,
- A head that flies 48 microns above the surface of the disk, and
- A reduced head load mass of 9.5 grams which also prevents damage to media.

The Winchester drives mount underneath the card cage in the 100/AP. Up to four Winchester drives may be installed if no diskette drives are installed; systems with one or two diskette drives can accomodate three or two Winchester disk drives, respectively. A control ribbon cable is daisy-chained to each of the drives, while a smaller data ribbon cable is provided for each drive for data transfer. The drives also accept AC power for the drive motor and DC for the logic functions.

Winchester disk drives are available in five capacities. The smaller capacity drives are avialable in 5 and 10 Megabyte nominal capacities; larger capacity drives are available in 20, 30, and 40 Megabyte nominal capacities. (The distinction between smaller and larger capacity drives is made because some of the drive attributes are different.)

2.9.2 Functional Characteristics

	5	10	20	30	40
Capacity-unformatted					
Per drive, Mbytes	5.33	10.67	21.33	32.00	42.67
Per surface, Mbytes	2.67	2.67	5.33	5.33	5.33
Per track, kbytes	10.4	10.4	10.4	10.4	10.4
Capacity-formatted					
Per drive, Mbytes	4.2	8.4	16.8	25.2	33.6
Per surface, Mbytes	2.1	2.1	4.2	4.2	4.2
Per track, kbytes	8.2	8.2	8.2	8.2	8.2
Per sector, bytes	512	512	512	512	512
Sectors/track	16	16	16	16	16
Transfer rate, Mbits/sec	4.34	4.34	4.34	4.34	4.34
Access time					
Track to track, msec	19	19	15	15	15
Average, msec	70	70	55	60	65
Maximum, msec	150	150	100	100	100
Average latency, msec	9.6	9.6	10	10	10
Rotational speed, rpm	3125	3125	3000	3000	3000
Recording density, bpi	6270	6270	6600	6600	6600
Flux density, fci	6270	6270	6600	6600	6600
Track density, tpi	172	172	345	345	345
Cylinders	256	256	512	512	512
Tracks	512	1024	2048	3072	4096
R/W heads	2	4	4	6	8
Disks	1	2	2	3	4

2.9.3 Block Diagram

This section discusses the following components of the Winchester disk drive:

- Drive mechanism
- Read/write head and disks
- Head positioning system
- Air filtration system

The following functional operations are also considered:

- Power sequencing
- Head selection
- Track accessing
- Read operation
- Write operation

Drive Mechanism (5 & 10 Mbyte Drives)

The AC drive motor rotates the spindle at 3125 rpm through a belt-drive system. 50 or 60 Hz line frequency can be accomodated by changing the drive pulley and belt.

Drive Mechanism (20, 30, and 40 Mbyte Drives)

Same as 5 & 10 Mbyte, except the rotational speed is 3000 rpm.

Read/Write Head and Disks (All Drives)

Data are recorded on a lubricated thin magnetic oxide coating on a 200 cm diameter aluminum substrate. The system employs one low load force/low mass Winchester type flying head to service the data tracks on each side of the Winchester disk. The number of disk surfaces (i.e. heads) and actual disks are listed in Section 2.9.2.

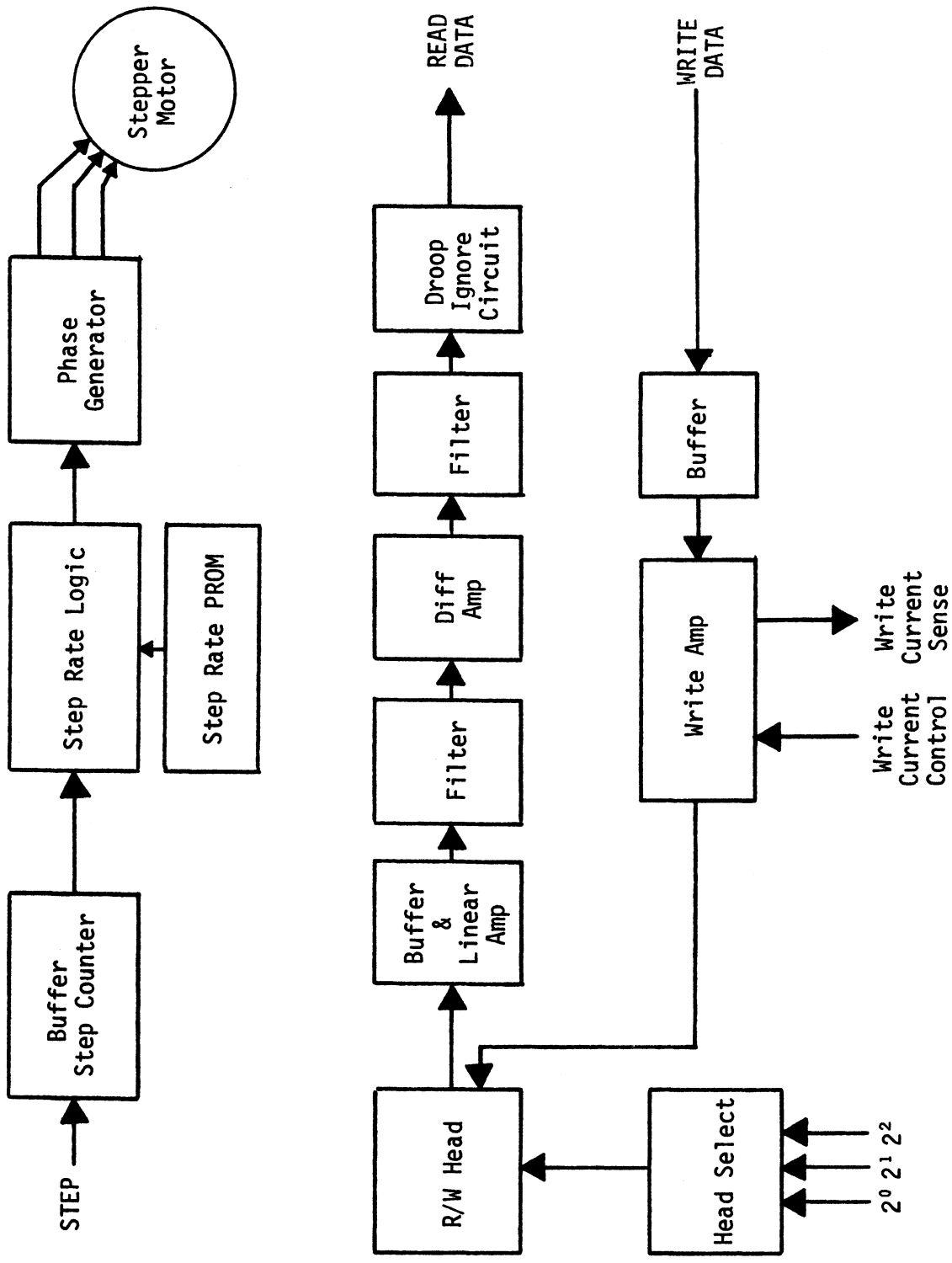


Figure 2-25. Winchester Drive Circuits

Head Positioning System (5 & 10 Mbyte Drives)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a metal band/capstan actuator. A metal band is wrapped around a drum (capstan) on the stepper motor and and fastened to the carriage in such a way that discrete small rotations of the stepper motor will cause the carriage to move in or out in discrete increments.

Head Positioning System (20, 30, and 40 MByte Drives)

The head positioning system on the larger drives is more complicated than the positioning system for smaller drives because of the greater track density (tracks are 73 microns apart v. 148 microns for the smaller drives). The positioning system consists of a rotary torque motor actuator, an optical track position encoder, and a temperature compensation servo.

The read/write heads are mounted on counterbalanced arms attached to the hub of the rotary torque motor. The configuration applies a pure torque to the rotor, which is balanced for mechanical stability and vibration resistance. The motor itself consists of a ring magnet, two flat plate pole pieces, a single plane moving coil and two bearings.

The opticaltrack position encoder consists of a photo etched glass scale, a LED light source and photodiode sensors. The encoder is mounted inside the sealed bubble. The glass scale is connected to the lowermost actuator arm; as the arm moves from track to track the graduations pass over the photodiode sensors. The system is accurate to more than ten times the track density used on the drive.

The temperature compensation (fine) servo obtains position feedboack directly from the disk surface 50 times per second. The coded information is embedded between the last gap on each track and the index pulse. The information is transparent to the Winchester controller since use of the drive is inhibited when the servo information is under the read/write heads. The disk rotation speed is 4% slower than that of the smaller drives so that the time the usable surface of the disk is under the read/write heads during each rotation is the same for both drives. (In the case of the smaller drives, the entire track is usable, while for the larger drives the entire track minus the pie-slice shaped servo area is available.)

The information from the track position encoder and the temperature servo is used by a microprocessor included in the

drive electronics. The information is used to make small adjustments in the positioning of the read/write heads over any desired track.

To further protect the information on the disks, an area inside track 511 (the innermost track) is designated as the "shipping and landing zone." During shipping, takeoff, and landing, and any time that the disks are not rotating at sufficient takeoff speed, the read/write heads are held over this zone.

Air Filtration System (All Drives)

The disk(s) and read/write heads are sealed in a module which consists of a casting and a plastic bubble, The module uses an integral recirculatory air system with an absolute (0.3μ) filter to maintain a clean environment. Another absolute filter is mounted in the bubble at the lowest pressure area in the system to allow pressure equalization with the ambient air without contamination.

Power Sequencing (5 & 10 Mbyte Drives)

The drives incorporate a speed sense circuit which prevents stepping until the disk is at the proper speed, so no power sequencing is required. Once the disk is rotating at 95% of normal speed, the drive will automatically recalibrate itself to track 000. After a 18 msec head settle time, the controller will be signalled, and normal read/write and stepping operations may be performed.

Power Sequencing (20, 30, and 40 MByte Drives)

In addition to speed sense circuitry similar to the smaller drives, the larger drives perform a recalibrate sequence which takes approximately 3 seconds to complete. The drive will seek to track 000, then seek to track 508, determine an offset value, and store it in memory. It then repeats the process for the three innermost tracks. Then, eight track locations are accessed and their offset values determined.

The procedure establishes eight zones, each with a thermal compensation value. The values are updated with every revolution of the disk to provide real-time tracking and adjustment for thermal drift.

Head Selection (All Drives)

The controller may select any one of the heads by placing that heads binary address on the head select lines. The heads will be selected as follows:

Head Select			Head Selected				
2^2	2^1	2^0	5	10	20	30	40
0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1
0	1	0	-	2	2	2	2
0	1	1	-	3	3	3	3
1	0	0	-	-	-	4	4
1	0	1	-	-	-	5	5
1	1	0	-	-	-	-	6
1	1	1	-	-	-	-	7

Track Accessing (All Drives)

Track accessing refers to the procedure by which the read/write heads are positioned over a track which contains data to be read or modified. Although the mechanical implementations are different for the smaller and larger drives, the functional operations are roughly the same.

The controller specifies a direction for stepping over the DIRECTION IN interface cable line. When DIRECTION IN is active, i.e. a logic zero, the read/write heads will move in; when the signal is inactive, the read/write heads will move out.

The read/write heads move over the tracks in the direction specified by DIRECTION IN as pulses are applied to the STEP line. Each STEP pulse moves the read/write heads one track.

There are two stepping modes: normal and buffered. The normal mode is used for moving across a small number of tracks, while buffered mode is used for moving across a large number of tracks. A block diagram of the circuitry which performs buffered stepping in the smaller drives is shown in Figure 2-25.

Normal stepping mode, used for moving a small number of tracks, causes the read/write heads to move at the rate of the pulses on the STEP line. This mode is selected automatically when the STEP line is pulsed with a minimum of 1.0 millisec between pulses.

In buffered step mode the step pulses are received at a high rate and buffered into a counter. After the last pulse is received the read/write heads will begin stepping the appropriate number of tracks, signalling the controller when the read/write heads settle at the appropriate track. This mode is selected automatically when the time between step pulses is 200 µsec or less.

The logic used to perform buffered stepping is shown in Figure 2-25. Step pulses are buffered and stored in a step counter. After the last pulse is received, the step rate logic will compare the current track location with the number of tracks to be stepped over, and select a carriage velocity from the step rate PROM. If a large number of steps are necessary, the carraige velocity will be high; if fewer steps are necessary, the carriage velocity will be low. As the carriage steps toward the destination track, the step rate logic compares the current location with the number of tracks left to be stepped over, and adjusts the velocity accordingly. The seek will therefore be damped as it approaches its destination, preventing damage or excess wear to the read/write head and carriage mechanism.

(Note: If step pulses are received at a rate which selects neither mode--that is, when the time between pulses is between 200 and 1000 µsec, the seek will be unreliable.)

Read Operation (All Drives)

In order to initiate a read operation, the drive must be selected and ready, a head must be selected, there must be no fault conditions, and the track seeking operation must have been completed.

The read operation begins with raw data flowing through the selected head. The signal is buffered onto the control PCB mounted on the side of the Winchester drive and amplified. The amplified signal is fed into a filter which removes frequencies not in the 15 kHz-5.3 MHz range. The final stage of amplification is a differential op amp which feeds another low-pass filter for further noise reduction. The droop ignore circuit creates an output window and delays erratic data long enough to prevent it from being output.

The output is MFM data, which is sent to the Winchester controller for interpretation.

Write Operation (All Drives)

In order to initiate a write operation, the drive must be selected and ready, the head selected, there must be no fault conditions, and track seeking operations must have been completed.

The write data from the Winchester controller board are buffered and fed into a write amplifier. This generates a write current sense signal used by the drive for a number of internal controls. The write current control allows the Winchester controller board to reduce the write current when recording data on inner tracks--this prevents the write operation from affecting nearby data bits. The write current is fed into the head which has been selected by the head select lines.

2.10 POWER SUPPLY

2.10.1 Overview

The 100/AP is powered by a switching-type power supply which provides the regulated DC voltages required by the system and its optional equipment. The voltages are current-limited, and an additional overvoltage protection circuit prevents the +5V logic chip supply from reaching a point where the chips could be damaged by a power supply failure.

The power supply module fits into a dedicated position in the card cage. On board connectors receive AC line power and supply DC power to the disk drives. Power is supplied to the printed circuit modules via the backplane.

2.10.2 Functional Characteristics

Outputs:	+5V at 30 amp (100 mvpp ripple) (Principal supply voltage for logic chips--reference voltage)
	+12V at 2 amp (240 mvpp ripple) -12V at 2 amp (240 mvpp ripple) (Backplane voltages--used by some larger chips)
	24V at 7 amp (480 mvpp ripple) (Disk drive DC supply)
	20V at 4 amp (400 mvpp ripple) 12V at 3 amp (240 mvpp ripple) (Current implementation--may not be included on future power supplies)
Input:	85-130V at 12 amp 170-260V at 6 amp 47-63 Hz line frequency
Protection:	Current-limiting circuitry Power supply failure will not cause +5V supply to exceed +6.2V Line fuse

2.11 BACKPLANE, CARD CAGE, AND HOUSING

2.11.1 Overview

The backplane and card cage serve to position the printed-circuit-card modules in the computer and connect them to the 100 common data, address, control, and power lines which run along the backplane (described in Section 2.12).

The backplane, card cage, and other modules mount inside the housing. The housing includes an on-off switch and mounting space for diskette drive doors on its front panel. A cutout on the rear panel allows access to the connectors mounted on the serial board. A line cord feeds through a port on the bottom of the housing; it is connected to an RFI/EMI filter and interlock before the AC power is used by the system.

Casters permit the unit to be moved easily.

2.11.2 Functional Characteristics

Card cage:	1 serial board slot 1 shielded power supply slot 12 module slots
Card dimensions:	10" × 12" (25.4 cm × 30.5 cm) 100-contact PC edge connector
Housing dimensions:	20" × 21" × 26-1/2" (50.8 cm × 53.3 cm × 67.3 cm)
Line cord:	48" (122 cm) AC line cord Standard (3-prong) grounding plug

2.12 BACKPLANE SIGNALS

Address Bus

Pin #s	Mnemonic	Function
25..39	A00..A14	15-bit address bus. The address bus contains the memory-address vector when BMEMEN is asserted and I/O bit addresses and external instruction addresses when BMEMEN is negated.
40..46	CA08..CA14	CRU address bus. The CRU address bus contains the address of the affected CRU bit during CRU operations. It also represents the unmapped I/O processor address bus for test purposes.
74	PIOCAS	Parallel I/O column address strobe. When asserted, it selects the 64 kbyte parallel I/O address space in the IOP's virtual memory.
75	SCR0CAS	Screen zero column address strobe. When asserted, it selects the monochrome terminal display address space in the IOP's virtual memory. (This line may be changed to SCRCAS in the future.)
76	APCAS	Attached processor column address strobe. When asserted, it selects the 64 kbyte address space assigned to the attached processor in the IOP's virtual memory.

Data Bus

09..24	D00..D15	16-bit bidirectional data bus. The data bus transfers data to and from the IOP when BMEMEN is asserted.

Power Supplies

Pin #s	Mnemonic	Function
01,02	GND	Ground
03,04	+5V	Common chip supply and reference voltages
05,06	+12V	
07,08	-12V	
93,94	-12V	
95,96	+12V	
97,98	+5V	
99,100	GND	Ground

Clocks

47	12MHZ	12 Megahertz crystal oscillator. Provides a rising edge on all four phases of the clock.
48	$\overline{\text{PHI1}}$	Phase 1 clock (inverted).
58	PHI3	Phase 3 clock.

Bus Control

Pin #s	Mnemonic	Function
51	$\overline{\text{PCRUOUT}}$	Same as BCRUOUT, active-low.
52	$\overline{\text{PCRUCLK}}$	Same as BCRUCLK, active low.
53	CRUIN	CRU data in. When a 9900 STCR or TB instruction is executed and $\overline{\text{EXTCRU}}$ is asserted, CRUIN is sampled for the level of the CRU input bit specified by A3..A7, CA08..CA14.
54	XCRUIN	A buffered connection to the 9900 CRUIN pin (testing).
55	$\overline{\text{EXTCRU}}$	External CRU space select. Asserted when the 9900 accesses its off-board CRU space.
56	BCRUOUT	Backplane/CRU data out. Serial I/O data appears on BCRUOUT when a 9900 LDCR, SBZ, or SBO instruction is executed.
57	BCRUCLK	Backplane/CRU clock. Indicates that serial I/O data should be sampled on BCRUOUT or that external instructions are present on A00..A02.
59	BDBIN	Backplane/Data bus in. When asserted, indicates that the 9900 will allow memory-read data on the data bus during $\overline{\text{BMEMEN}}$.
60	$\overline{\text{WE}}$	Write enable. Indicates that memory write data is available from the 9900 to be written into memory.
61	$\overline{\text{BMEMEN}}$	Backplane/Memory enable. Indicates that the address bus contains a memory address.

Memory Control

Pin #s	Mnemonic	Function
50	READY	Asserted when the current AP memory reference is complete.
65,67 69,71	$\overline{\text{DMARQ0}}$.. $\overline{\text{DMARQ3}}$	DMA request lines. $\overline{\text{DMARQn}}$ is asserted by a DMA device when it wishes to transfer data into memory.
66,68 70,72	$\overline{\text{DMAGR0}}$.. $\overline{\text{DMAGR3}}$	DMA grant lines. $\overline{\text{DMAGRn}}$ is asserted (except for the first clock cycle of each memory cycle) while the DMAC is performing a data transfer involving device n.

Timing and Control

64	$\overline{\text{BLOAD}}$	Backplane/Load. Causes the 9900 processor to execute a non-maskable interrupt and begin a load sequence. Not currently implemented.
77	$\overline{\text{EXTRESET}}$	External reset. Causes the 9900 to be reset and inhibits $\overline{\text{WE}}$ and CRU operations. When released, the 9900 initiates a zero-level interrupt routine that fetches a reset vector from the boot ROM, sets ST to zero, and begins execution. $\overline{\text{EXTRESET}}$ will also terminate an idle state. $\overline{\text{EXTRESET}}$ must be asserted for at least three clock cycles.
78	$\overline{\text{EXTCNTL}}$	External control. Causes the processor to enter a hold state following the completion of its current memory cycle. The address and data buses, $\overline{\text{WE}}$, $\overline{\text{BMEMEN}}$, BDBIN, and the CRU signals go into a high impedance state. (testing)
79	$\overline{\text{RESET}}$	A buffered output connected to the 9900 $\overline{\text{RESET}}$ pin.

Interrupt Control

Pin #s	Mnemonic	Function
83..92	$\overline{\text{INT06}}$.. $\overline{\text{INT15}}$	Interrupt lines 6 through 15. Asserting interrupt line x causes an xth level interrupt request to be sent to the IOP.

Unused

49		
62,63		
73		
80	$\overline{\text{POWERFAIL}}$	
81	$\overline{\text{SCR0AVAIL}}$	
82	$\overline{\text{SCR1AVAIL}}$	