P.V. JERMY

ISS 12

TECHNICAL SPECIFICATION OF THE I.C.T. STANDARD INTERFACE FOR PERIPHERAL DEVICES

This specification has been prepared by the Specifications Project of Engineering Division, Stevenage. The document has been approved by the Managers of Computer Systems Division, and Peripherals Division, Stevenage, Planning Division, Putney; Planning Division, Bracknell; and Computer Equipment Group, West Gorton.

PUBLISHED BY DESIGN CONTINUNCATION I.C.T. LTD.

I·C·T

I.C.T STANDARD INTERFACE SPECIFICATION

1110020

Sheet 1

Control Sheet

Issue Nº	Total Nº of Sheets	Affected Sheets and Alterations	Engineer	Design Commun.	Change Notice	Date
12	96	Revised, retyped and re-issued,	J.C. Labbett			
		sheets 81 - 96 incl. introduced	V. Klemen		2099	7.67.

PUBLISHED BY DESIGN COMMUNICATION I.C.T.(ENG) LTD.

ISS. 12

CONTENTS

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. (ENG) LTD.

ISS. 12

PART I

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. (ENG.) LTD.

ISS 12

1.0 INTRODUCTION

1.1 SCOPE

This document defines the Standard Interface to be used by I.C.T. peripherals and processors.

However it is not possible for a peripheral designer to design his equipment to this specification alone. It is necessary that the designers of the processor to which connection is desired to be made be consulted so that data width and preferred mode of operation be catered for. Similarly processor designers should consult peripheral on individual peculiarities of the peripherals it is desired to be used in the complete system.

The range of peripherals which may be connected by this interface is as follows:

Type 1	Single channel, single mechanism
Type 2	Single channel, multi mechanism
Type 3	Multi channel, multi mechanism
Type 4	Data exchange
Type 5	Single channel, multi address

The suffix A or B following the type number denotes the timing characteristics of the peripheral.

A type will operate according to the timing rules currently described in this specification and will have the 'F' line at logic 0.

B type will operate according to faster timing rules to be defined later and will have the 'F' line at logic 1.

1.2 DEFINITIONS

The following definitions are given to define the application of the terms 'CHANNEL' and 'MECHANISM' in this specification.

1.2.1 Data Block

A block of data on the interface is a group of characters associated as follows:

PUBLISHED BY DESIGN COMMUNICATION I.C.T. LTD.

ISS 12

1.2.1 Cont/d.

(i) They are transferred as the result of one command.

(ii) One block identifier is necessary and sufficient for a central processor to transfer each character to or from the correct memory location.

(iii) One block is associated with one 'TERMINATED' signal which defines its end.

1.2.2 Simultaneous Operation

If two or more data blocks are transferred over the interface such that there can exist a time when both data block transfers have been INITIATED and neither has been TERMINATED, then the transfers are SIMULTANEOUS.

1.2.3 Channel

An interface which carries one data block transfer, i.e. an INITIATED data block which is TERMINATED before a subsequent data block can exist, is a SINGLE CHANNEL interface.

An interface which carries up to N simultaneous data block transfers is an N-channel interface. In particular if N is greater than one, it is a MULTI-CHANNEL interface. As a corollary it follows that on an N-channel interface at least N distinct identifiers are required which could be used to address N buffer areas in store.

1.2.4 Mechanism

A single device handling a medium on which data is recorded or is to be recorded, is a MECHANISM.

A channel which may be switched (in between data blocks) to different MECHANISMS is a MULTI-MECHANISM CHANNEL.

The case of such a switch in the middle of a data block is not allowed for under this heading, but must use more than one CHANNEL. An interface with more than one MULTI-MECHANISM CHANNEL is a MULTI-MECHANISM, MULTI-CHANNEL INTERFACE.

In addition, some further terms are used in this document, which are defined as follows:

ISS 12

1.2.5 Peripheral

A device consisting of one or more mechanism associated with one control unit connected to a processor.

1.2.6 Irreversible

A condition which has changed due to the application of a control signal and remains in the new state after the control signal disappears.

1.2.7 Ducked

A condition which has changed due to the application of a control signal but will return to the original state after the control signal disappears.

1.2.8 Status

Status is usually a bit significant coding of the current state of a peripheral. However coding of more than one bit may occur in exceptional circumstances. Changes in the state may be signalled to the central processor where appropriate (See 3-9).

1.2.9 Unset

A condition which has ceased to exist due to the application of a control signal said to be "unset".

1.2.10 Reset

A condition which has been set again in another state is said to be "reset". This term is used for status which may in general exist in one of three states. See 7-1 and 7-3 for further remarks.

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. LTD.

ISS 12

2.0 LINES ACROSS THE INTERFACE

2.1 Types 1, 4 and 5 peripherals.

	Minimum mandatory subset	Permissible Extensions
Processor to peripheral		
Do	6 lines, 2^0 through 2^5	3 lines 2^6 2^7 + parity 2^8
A	1 line	NIL
T	1 line	NIL
C	1 line	NIL
No	NIL	1 line
L	NIL	1 line
G	1 line	NIL
Ho	1 line	NIL
Peripheral to processor		
Di	6 lines, 2^0 through 2^5	3 lines 2^6 2^7 + parity 2^8
F	1 line	NIL
R	1 line	NIL
B	1 line	NIL
J	1 line	NIL
Ni	NIL	1 line
Hi	1 line	NIL
Z	3 lines	NIL
Total - 25		9

Note: A Type peripherals will have F=0 (present timing rules)
B Type peripherals will have F=1 (fast timing rules)
rules

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. LTD.

ISS 12

2.2 Type 2 and 3 peripherals

Minimum mandatory subset		Permissible Extensions
25 lines listed in 2.1		6 lines (as listed in 2.1 except L and Ni, No)
No	1	NIL
Ni	1	NIL
L	1	NIL
Totals	- 28	6

Giving a grand total with extensions of 34

Note: A Type peripherals will have F=0 (present timing rules)
B Type peripherals will have F=1 (fast timing rules)

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. LTD.

ISS 12

3.0 FUNCTION OF LINES ACROSS THE INTERFACE

The function of each line will be described in general terms, followed by the mandatory or permissible aspects of the function.

3.1 Do - Data Out.

These lines can be used to transmit either a data character including odd parity, a control character, or a mechanism or channel identifier.

A convention is adopted whereby 2^0 signifies the lines which is equivalent to the least significant binary bit. The mandatory lines are 2^0 through 2^5. The use of the parity line (2^8) is optional. Peripherals and processors which include the line must provide a means for ignoring parity errors across the interface. Parity, if used, must be odd parity. Types 2 and 3 peripherals must accept identifiers from Do.

An extension to 7 or 8 bit characters, using lines 2^6, 2^7 is permissible only for those peripherals whose natural character width exceeds 6 bits, e.g. 7 hole paper tape, 8 bit magnetic tape. Individual agreed specifications should be consulted regarding the number of lines to be used.

3.2 A - Peripheral Addressed.

This is one line which, when in the logic 1 state, indicates that the interface is active. It exercises over-riding control, such that if A is not present, peripherals must ignore a character on the Do lines ignore C, T, L, No lines and maintain all the Di lines at logic zero.

The use of A is mandatory, If A is present peripherals must continuously present the appropriate character onto the Di lines, and peripherals must be prepared to accept a character from Do when the strobe pulse arrives.

The processor may join the A line to a common bus. (see 10-5)

The conditions under which A is raised to effect a single character transfer are described under the timing rules section, and figure 2.

No extension of A is permissible.

ISS. 12

3.3 T - Strobe

This is one line used to control transfers in conjunction with line A. It is used to make irreversible changes in the control logic in the peripheral.

The use of T is mandatory.

Processors may join the T line to a common bus (see 10-5).

No extension of T is permissible.

3.4 C - Transfer Control

This is one line which, when in the logic 1 state indicates that the character on Do is a control character.

The use of C is mandatory. The processor may join the C line to a common bus. (see 10-5)

No extension of C is permissible.

3.5 No - Identification control out.

This is one line which, when in the logic 1 state indicates:

(i) When A C = 1 1, the character on Do is a control identifier (e.g. a mechanism or channel address).

(ii) When A C = 1 0, the peripheral should place on Di the data identifier of a data character for which an 'R' request has been sent.

No is optional for type 5 peripherals. It is mandatory for types 2 and 3 peripherals. It is not used for types 1 and 4.

No extension of No is permissible.

3.6 L - Limit

This is one line used to conclude a data block transfer in conjunction with A, T and C.

The L line is optional.

If C = 0, No = 0, coincident with L, the last character of a block of data is being transmitted.

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. LTD.

ISS 12

L - Limit (Cont/d.)

In any other situation L indicates that the last character has been transferred of the block identified by the identifier being transmitted or last transmitted to the peripheral. The peripherals will suppress the R line for the appropriate channel and will proceed as follows:

If the ERROR status is already set, it will remain set.

If not set, it will take either action (a) or (b) below, following the transmission of any character read from or written onto the medium after the receipt of L.

Either (a) if the detection of errors has no significance as to the validity of data already transferred will cease to record further errors.

or: (b) if further checks are performed which may effect the validity of the data transferred will continue to record further errors. The point at which termination occurs must be specified in the individual peripheral agreed specifications.

The next READ or WRITE control code to the relevant channel will unset the error status.

No extension of L is permissible.

3.7 Di - Data In

These lines can be used to transmit either a data character including odd parity, a status character or a mechanism or channel identifier. A convention is adopted whereby 2^0 signifies the line which is equivalent to the least significant binary bit. The mandatory lines are 2^0 through 2^5. The use of the parity line (2^8) is optional. Parity, if used, must be odd parity. Type 2 and 3 peripherals must give a data identifier on Di as appropriate.

An extension to 7 or 8 bit characters using lines 2^6, 2^7 is permissible only for those peripherals whose natural character width exceeds 6 bits, e.g. 7 hole paper tape, 8 bit magnetic tape. Peripherals and processors presently designed to use 6 bit characters will continue in this mode.

ISS 12

3.8 R - Request data transfer

This is one line used in one of two ways.

The use of R is mandatory.

In the case of a read only device, or when a read/write device is in the reading states, the line is used to indicate that a character of data is available for transfer to the central processor. In the case of a write only peripheral device, or when a read/write device is in the writing state, the line is used to indicate that the device requires a data character to be transferred from the processor. The state of R has a special relationship to the speed at which data transfers may be made across the interface. This is dealt with in detail in the section concerning timing.

No extension is permissible.

3.9 B - Interrupt

This is one line used to indicate certain status changes. Such status changes will always be available to the central processor and the B line may not change for any cause other than a status change. Details of how status will affect the B line are given in Fig. 4. and Fig. 4A.

3.10 J - Direction of transfer

This is one line used by the peripheral in conjunction with the 'R' request indicating whether the request is for an input or output data character.

The use of J is mandatory, no extensions are permissible.

J = 0 = output character (WRITE)

J = 1 = input character (READ)

3.11 Ni - Identification control in

This is one line which, the logic 1 state indicates that there has been a change in the identifier associated with data transfers. Ni is optional for Type 5 peripherals. It is mandatory for types 2 and 3 peripherals. It is not used for Types 1 and 4. No extension of Ni is permissible

ISS 12

3-12 F - Fast transfer

This is one line which, when in the logic 1 state, indicates that transfers from this peripheral are controlled by faster timing rules (These rules are defined in part II of this specification.)
The use of F is mandatory, no extension is permissible.

3-13 Hi - Power present at the peripheral, information on Di is valid.

Hi is one line from the peripheral to the processor which must obey the following rules:

1. When the two wires comprising the Hi line pair are short circuited by the peripheral this indicates that all power supplies at the peripheral are within their specified limits.

2. Further, when Hi is short circuited, valid signals appear on Di, Ni, J, R, B, F in response to processor commands.

Hi is mandatory, no extensions are permissible.

3.14 Ho - Power present at the processor, information on Do is valid
Ho is one line from the processor to the peripheral which must obey the following rules:

1. When the two wires comprising the Ho line pair are short circuited by the processor this indicates that all power supplies at the processor are within their specified limits.

2. Further when Ho is short circuited, valid signals appear on Do, No, A, T, C, L.

Ho is mandatory, no extensions are permissible.

PUBLISHED BY DESIGN COMMUNICATION I.C.T. LTD.

ISS.

12 3.15 G - General Reset.

This is one line from the processor to the peripheral. The peripheral must be so designed that a logic level pulse of 100 uSec. duration is sufficient to cause a general reset.

3.15.1 If a general reset occurs when the peripheral is operable and an order is not being executed, the peripheral must enter the STOPPED 2 State, and B interrupts be inhibited.

3.15.2 If a general reset occurs when an order is being executed, R interrupts must be immediately inhibited. This may result in the rejection of any associated media (e.g. cards). The peripheral must eventually enter the STOPPED 2 state, and a B interrupt is then permissible.

3.16 Z - Ground

Z consists of 3 lines used for the 0 volt connection between the processor and the peripheral.

3.17 Identifiers.

These are characters appearing on Do or Di and indicate mechanism or channel addresses.

The specific assignment of identifiers to mechanism or channel addresses will be given in individual peripheral specifications.

Identifiers are divided into two classes, control identifiers and data identifiers.

Control identifiers are given on Do by the processor, and precede control commands, in order to identify the command with a particular channel or mechanism.

Data identifiers are <u>always</u> given on Di by the peripheral in response to A C T No = 1 0 X 1 from the processor to indicate the channel address of a data character to be transferred.

The Ni line is used by the peripheral to indicate that a <u>change</u> has occurred in the data identifier. Ni arises in conjunction with the

ISS 12

3.17 Cont'd..

data service request R and the data direction indicator J, and is unset either when:

(i) A C T No Ni = 1 0 1 1 1 or:

(ii) After the processor gives T for transfer of the first data character associated with the new identifier and before the next R interrupt occurs.

Ni will not arise with R and J, if the data character to be transferred is associated with the same data identifier as the previous character.

Processors will normally ask for data identifiers in response to R interrupts. If a data identifier request is made at other times, using T, this may cause Ni to unset prematurely and, therefore, invalidate the state of this line.

For further information on the use on identifiers, the Code of Practice document to the Standard interface may be consulted.

PUBLISHED BY DESIGN · COMMUNICATION I.C.T. LTD.