Contents

Data Communications

INTRODUCTION

Data Communications Systems

Data communications (BSC or SDLC) is an optional feature that lets System/34 function as a primary station (SDLC only) or as a secondary station on a point-to-point or multipoint network.

Up to two communications features can be installed on the system.

The data communications feature can be connected to a half-duplex or full-duplex network. However, the communications feature operates only in a half-duplex mode; that is, data is transmitted in only one direction at a time. Data is transmitted or received serially-by-bit and serially-by-character over voice-grade switched or nonswitched data communications networks, or over switched or nonswitched public or private digital data lines.

The control processor controls the communications adapter system I/O instructions. Once a transmit or receive operation starts, the control storage program and the hardware execute the specified operation.

During transmit operations, each byte to be transmitted is sent to the communications adapter where data is transmitted 1 bit at a time to the modem (modulator/demodulator) or to the digital adapter. The modem or the digital adapter, in turn, sends the bit to the receiving station over the data communications network.

During receive operations, the communications adapter receives each bit from the modem or from the digital adapter and assembles the bits into bytes. Each byte of data is sent to the control processor as the result of a character microinterrupt.

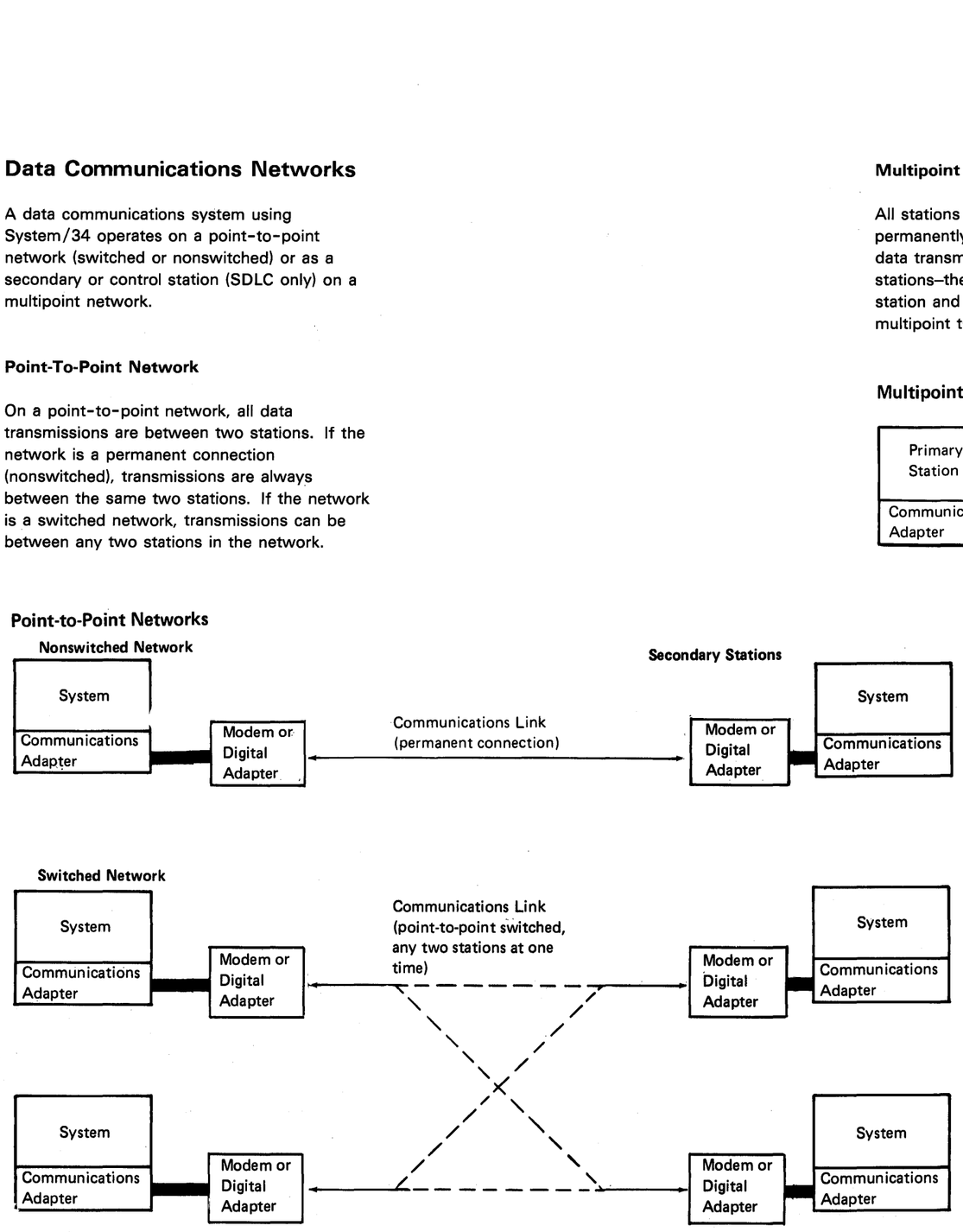
Data Communications Networks

A data communications system using System/34 operates on a point-to-point network (switched or nonswitched) or as a secondary or control station (SDLC only) on a multipoint network.

Point-To-Point Network

On a point-to-point network, all data transmissions are between two stations. If the network is a permanent connection (nonswitched), transmissions are always between the same two stations. If the network is a switched network, transmissions can be between any two stations in the network.

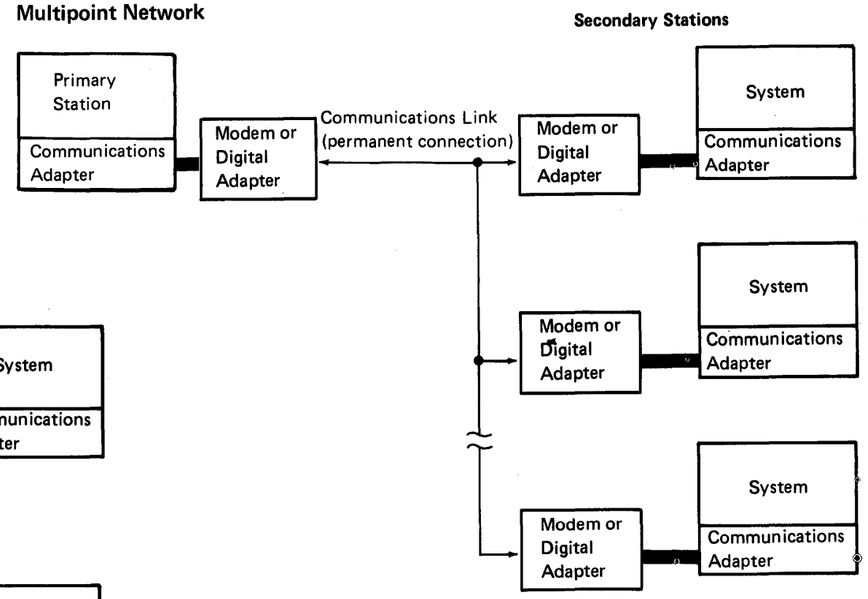
Point-to-Point Networks



Multipoint Network

All stations in a multipoint network are permanently connected (nonswitched), and all data transmissions are between two stations–the primary (or multipoint control) station and an addressed secondary (or multipoint tributary) station.

Multipoint Network

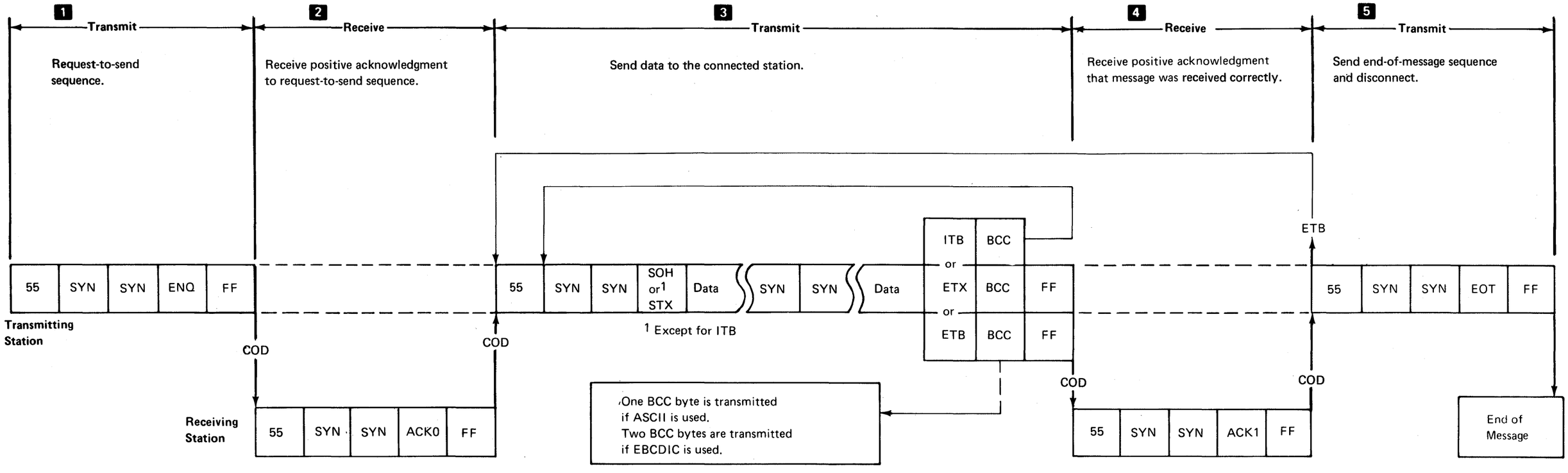


Binary Synchronous Communications

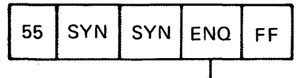
Binary synchronous communications uses a message format and line control characters for transmitting and receiving data.

BSC Message Format

The BSC feature uses line control characters to transmit information over a data link. In addition, each message starts with a hex 55 character and 2 SYN bytes, and ends with a hex FF character. Some of the line control characters are described in the following figure, which shows typical message formats for transmit and receive operations.

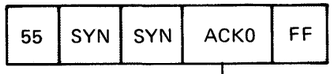


1 **Transmit**—Request-to-send sequence.



Causes a change of direction. The receiving station must respond within 2 seconds.

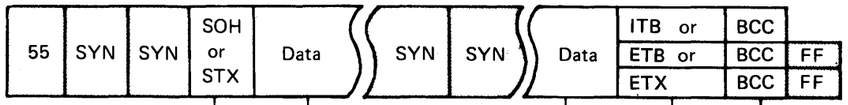
2 **Receive**—Receiving station responds to transmitted request-to-send sequence.



Indicates that the receiving station is ready to receive data.
Other responses:

- NAK—Indicates that the receiving station is not ready to receive data.
- WACK—Indicates that the receiving station is ready to receive data at a later time. (Wait before sending data.)
- No response—Receiving station did not respond to the request-to-send sequence. The transmitting station waits 3.25 seconds for a response from the receiving station.

3 **Transmit**—Send data to the connected station.



BCC—The block-check-character byte is generated by the transmitting station as the message is being transmitted. The receiving station also generates a BCC byte as the data is being received. After receiving an ITB, ETB, or ETX character, and the BCC byte, the receiving station compares the BCC byte received with the BCC byte generated. If these 2 BCC bytes compare, the message data was received correctly.

ITB—Indicates the end of an intermediate block of data. No change of direction occurs. The transmitting station sends 2 SYN characters and continues to transmit data.

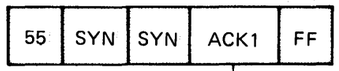
ETB—Indicates the end of a block of data in a message. The transmitting station requests acknowledgment that the message block was received correctly.

ETX—Indicates the end of text. This also requires the receiving station to acknowledge that the message was received correctly.

Data—Transmits message data.

SOH or STX—Indicates the start of a message.

4 **Receive**—Receive positive acknowledgment that message was received correctly.

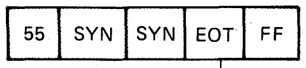


Indicates to the transmitting station that the message or block of data was received correctly.

Other responses:

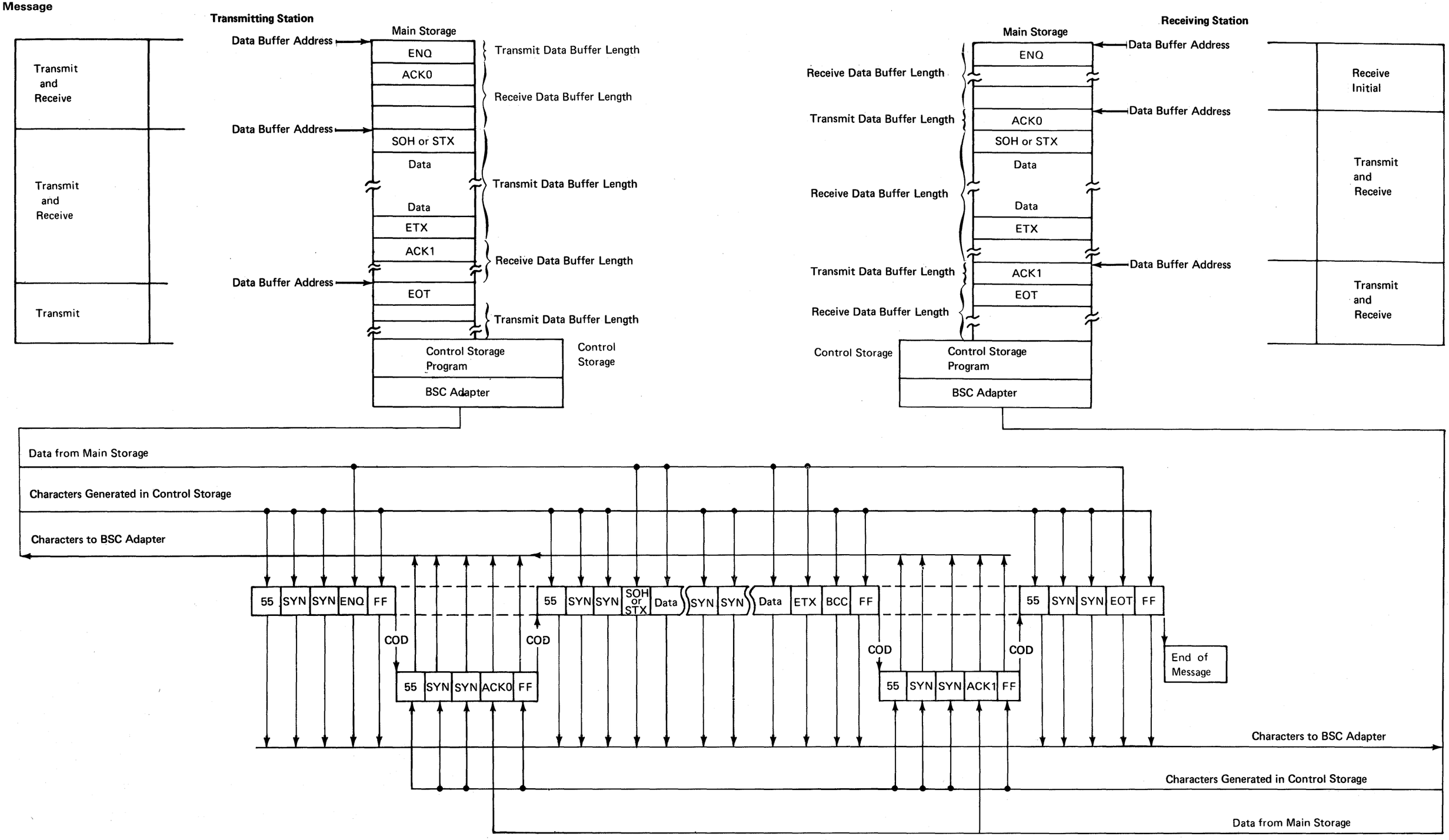
- NAK—Indicates that the block of data or the message was received incorrectly. (The 2 BCC bytes did not compare.)
- No response—The receiving station cannot receive, transmit, or did not recognize the change-of-direction character.

5 **Transmit**—Send end-of-message sequence and disconnect.



Indicates end of message. No more data is to follow. The receiving station is then disconnected from the line.

Transmit and Receive Storage Contents of Message



EBCDIC, ASCII, and Line Control Characters

The following table gives the line control character codes for the BSC feature.

Name	Mnemonic	EBCDIC	ASCII
Start of header	SOH	SOH	SOH
Start of text	STX	STX	STX
End of text block[1]	ETB	ETB	ETB
End of text[1]	ETX	ETX	ETX
End of transmission[1]	EOT	EOT	EOT
Enquiry[1]	ENQ	ENQ	ENQ
Negative acknowledgment	NAK	NAK	NAK
Synchronous idle	SYN	SYN	SYN
Data link escape	DLE	DLE	DLE
Intermediate text block	ITB	IUS	US
Even acknowledgment[1]	ACK 0	DLE (70)	DLE 0
Odd acknowledgment[1]	ACK 1	DLE/	DLE 1
Wait before transmit–positive acknowledgment[1]	WACK	DLE,	DLE;
Mandatory disconnect[1]	DISC	DLE EOT	DLE EOT
Reverse interrupt[1]	RVI	DLE@	DLE <
Temporary text delay[1]	TTD	STX ENQ	STX ENQ
Transparent start of text	XSTX	DLE STX	
Transparent intermediate text block	XITB	DLE IUS	
Transparent end of text[1]	XETX	DLE ETX	
Transparent end of text block[1]	XETB	DLE ETB	
Transparent synchronous idle	XSYN	DLE SYN	
Transparent block cancel[1]	XENQ	DLE ENQ	
Transparent TTD[1]	XTTD	DLE STX DLE ENQ	
Transparent DLE	XDLE	DLE DLE	

[1] Change-of-direction character

The following table gives the bit definitions for the EBCDIC characters.

Second Hex Digit / Bits 4, 5, 6, and 7		00				01				10				11			
		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	DS		SP	&	-						{	}	\	0
0001	1	SOH	DC1	SOS				/		a	j	~		A	J		1
0010	2	STX	DC2	FS	SYN					b	k	s		B	K	S	2
0011	3	ETX	TM							c	l	t		C	L	T	3
0100	4	PF	RES	BYP	PN					d	m	u		D	M	U	4
0101	5	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	6	LC	BS	EOB/ETB	UC					f	o	w		F	O	W	6
0111	7	DEL	IL	PRE/ESC	EOT					g	p	x		G	P	X	7
1000	8	GE	CAN							h	q	y		H	Q	Y	8
1001	9	RLF	EM						\	i	r	z		I	R	Z	9
1010	A	SMM	CC	SM		¢	!	¦	:								LVM
1011	B	VT	CU1	CU2	CU3	.	$	,	#								
1100	C	FF	IFS		DC4	<	*	%	@					∫		⌐	
1101	D	CR	IGS	ENQ	NAK	(	)	_	'								
1110	E	SO	IRS	ACK		+	;	>	=					⊎			
1111	F	SI	IUS[1]	BEL	SUB	¦	¬	?	"								EO

Bits 0, 1
Bits 2, 3
First Hex Digit

[1] IUS is the same as ITB.

The following table gives the bit definitions for the ASCII characters.

Bit Positions 7 6 5					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
4	3	2	1	Column / Row	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	! or ¦	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	⌊	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	¦
1	1	0	1	13	CR	GS	-	=	M	⌋	m	}
1	1	1	0	14	SO	RS	.	>	N	~	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

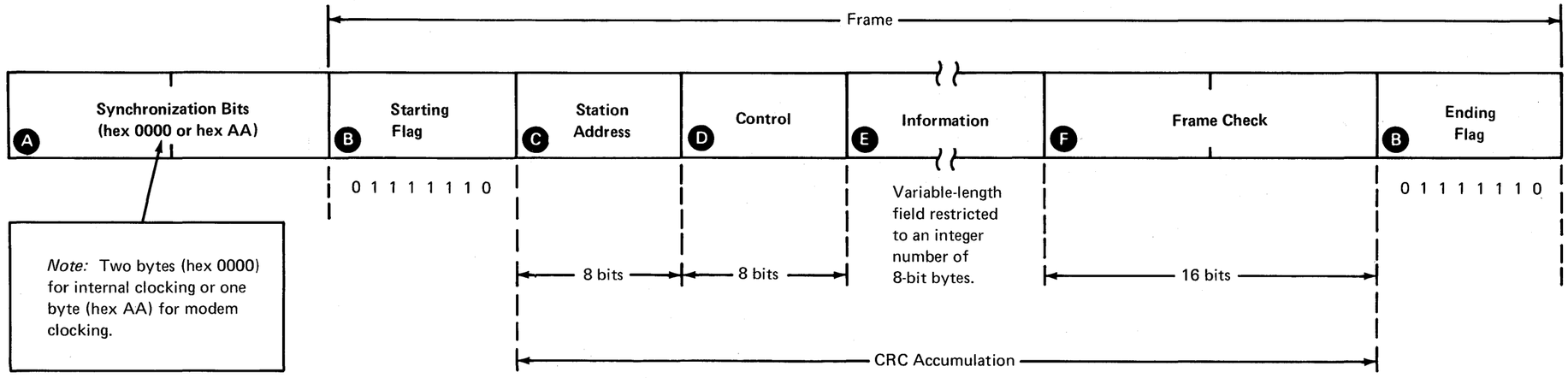
Bit 1 (the low-order bit) is transmitted first, bits 2-7 next, and a parity bit last.

Synchronous Data Link Control

Synchronous data link control uses the frame format for transmitting every command, every response, and all information over the data link.

Frame Format

Each frame contains a starting flag, a station address, a control field, an information field (optional), a frame check field, and an ending flag.



Synchronization Bits (A)

This field, although not a part of the SDLC frame, is shown here because of its relationship with the frame. When the internal clock feature is used, the SDLC adapter inserts 2 additional synchronization bytes (hex 0000) into the data stream before the starting flag sequence. These 2 bytes are used to obtain or maintain synchronization of the clock following a line turnaround.

When modem clocking is used, the SDLC adapter inserts 1 byte (hex AA) into the data stream for synchronization. NRZI (zeros-complemented transition coding) may or may not be used with modem clocking. NRZI is described later in this section.

Starting and Ending Flags (B)

In every SDLC frame, there are two flags (starting and ending) that have a binary configuration of 01111110. The starting flag starts all transmissions except when synchronization bits are needed, as described in (A). The starting flag also starts transmission error checking. The ending flag ends the frame and transmission error checking. To identify the starting flag from the ending flag, the adapter (primary and secondary) assumes that a starting flag is followed by an 8-bit sequence that is a station address. Also, secondary stations can identify the starting flag if it is followed by the general address (11111111).

When more than one frame is transmitted, the ending flag of one frame can also be the starting flag of the next frame.

Station Address (C)

The station address field is an 8-bit field that always identifies the secondary station. The primary station is never identified in the address field. If the System/34 is acting as a secondary station, in addition to recognizing its own address, it can also recognize the general address (11111111). The address field must be recognized before a frame can be received. The null address (00000000) is not a valid station address.

Control (D)

This field is used for encoding the commands and responses needed to control a data link. As a secondary station, the control field is used for supervisory and nonsequenced responses. As a primary station, it uses the control field for supervisory and nonsequenced commands. Both stations use the control field for transferring information.

The control field, using bit 7 or bits 6 and 7, can select one of three formats–the information transfer, supervisory, or nonsequenced format. Each format is described under *Control Field Formats* with its associated commands and responses.

Information (E)

This field is not necessarily included in every frame, although a frame with the information transfer format usually contains an information field. Information fields are not allowed with some control field formats.

The information field is not restricted to any bit sequence, but it is restricted to an integer number of 8-bit bytes and by the buffering limits of the stations communicating with each other.

Frame Check (F)

All frames contain 2 bytes in the frame check field for the purpose of checking transmission accuracy. The CRC accumulation, started by the starting flag and ended by the ending flag, includes all bits in the station address, control, and information fields; the flags are not included.

CRC accumulation is performed on all frames at the transmitting and receiving stations. The transmitting station sends the binary complement of the CRC accumulation. The receiving station, having processed the CRC accumulation, should show a remainder of hex F0B8 if the transmission is error free.

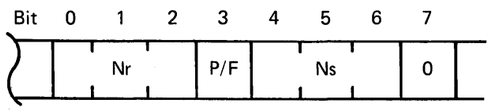
Note: Inserted zeros are not included in the CRC accumulation.

Control Field Formats

The control field uses bit 7 or bits 6 and 7 to identify the three control field formats–the information transfer, supervisory, and nonsequenced formats. All three formats use bit 3 as the poll/final (P/F) bit. A poll bit, sent by the primary station, permits the transmission of data from a secondary station. A secondary station sends a final bit when it has completed a transmission.

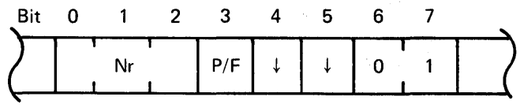
The Nr bits (bits 0 through 2 of the information transfer and supervisory formats) contain the sequence number of the next expected frame. The Ns bits (bits 4 through 6 of the information transfer format) contain the sequence number of the frames that have been sent. The remaining bits of the control field (for all three formats) are used to encode the commands and responses necessary to control a data link; the commands and responses are described on this page.

Information Transfer Format



The information transfer format is used for transferring information over a data link. The transmitting station increases its Ns count for each information frame it sends; the receiving station increases its Nr count for each valid sequenced frame it receives.

Supervisory Format



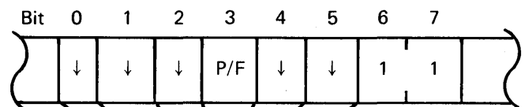
0	0	Receive Ready (RR)
0	1	Receive Not Ready (RNR)
1	0	Not used
1	1	Not used

The supervisory format is used to acknowledge information frames, to request retransmission of information frames, and to report a busy condition. The commands and responses of the supervisory format are:

- Receive Ready (RR)
  This is a command or a response (sent by a primary station or by a secondary station), indicating that the originating station is ready to receive data. Receive ready also acknowledges information frames with sequence counts through Nr minus 1.

- Receive Not Ready (RNR)
  This is a command or a response (sent by a primary station or by a secondary station), indicating that the originating station has a busy condition and cannot receive additional information frames. Frames through Nr minus 1 are received.

Nonsequenced Format



0	1	0	0	0	Disconnect (DISC)
1	0	0	0	0	Set Normal Response Mode (SNRM)
0	1	1	0	0	Nonsequenced Acknowledgment (NSA)
1	1	1	0	0	Test
1	0	0	0	1	Command Reject (CMDR)
0	0	0	1	1	Disconnected Mode (DM)
1	0	1	1	1	Exchange Station Identification (XID)
X	X	X	X	X	All remaining bit combinations are not used.

The nonsequenced format is used to perform data link control functions. The commands and responses of the nonsequenced format are:

- Disconnect (DISC)
  This command terminates normal response mode (NRM) and puts the receiving secondary station in normal disconnect mode (NDM). A System/34 that is acting as a secondary station should respond to the DISC command with an NSA (nonsequenced acknowledgment); it should then disable the adapter. No information field is permitted with the disconnect command.

- Set Normal Response Mode (SNRM)
  This command puts the secondary station in normal response mode (NRM) by placing the receiving secondary station under control of the transmitting primary station. NSA (nonsequenced acknowledgment) is the expected response from the secondary station to an SNRM command. Transmissions are not allowed from a System/34 that is a secondary and is in normal response mode until it receives a frame with the poll bit on. The primary and secondary station Nr and Ns counts are reset to 0. The secondary station remains in normal response mode until it receives a DISC command.

- Nonsequenced Acknowledgment (NSA)
  This is an affirmative response to a DISC or SNRM command; it indicates that the command has been received.

- Test
  This is a command and a response. The primary station starts one round-trip transmission of test data to which a secondary station responds. The test data sent with the command is returned in the response from the secondary station. However, if the amount of test data is more than the amount of data that can be put into the receive buffer, only the control field is returned in the test response.

- Command Reject (CMDR)
  This is a response from a secondary station in NRM to indicate that a problem has been detected in a frame received with good frame check sequence. A CMDR response includes an information field that gives the reason for the rejected command.

- Disconnected Mode (DM)
  This is a response from a secondary station, indicating that it is in a disconnected state and that it wants an online status.

- Exchange Station Identification (XID)
  The primary station uses XID as a command to request station identification from a secondary station. The primary station also has the option of giving its own identification. An XID is the expected response to the XID command.

Primary Station Commands and Secondary Station Responses

Each byte of every frame is either generated or analyzed by hardware, microcode, SDLC IOS, or SNA utility. The matrix shown at the right indicates with bullets (•) how each byte is generated or analyzed.

See the bottom of the page for bit descriptions of the nine control fields.

Typical SDLC Sequence

	SNRM	NSA	RR	Information — 2 Frames	RR	RR	DISC	NSA
Primary Station	F A C 1 FC FC F		F A C 3 FC FC F	(Note 3)	F A C 6 FC FC F		F A C 8 FC FC F	
Secondary Station	Note 1	F A C 2 FC FC F	Note 1	F A C 4 I I I FC FC F A C 5 I I I FC FC F	Note 1	F A C 7 FC FC F	Note 1	F A C 9 FC FC F
Hardware	• •	• •	• •	• •	• •	• •	• •	• •
Microcode	• • • • • •	• • • • • •	• • • • • •	• • • • • • • • • • • • • • • •	• • • • • •	• • • • • •	• • • • • •	• • • • • •
SDLC IOS	•	•	•	• •	•	•	•	•
SNA Utility				• • • • • •				

1

Bits	0	1	2	3	4	5	6	7
	1	0	0	1	0	0	1	1

SNRM command
Poll bit on
Nonsequenced frame

3

Bits	0	1	2	3	4	5	6	7
	0	0	0	1	0	0	0	1

Nr count
Poll bit on
RR command
Supervisory frame

5 (Note 2)

Bits	0	1	2	3	4	5	6	7
	0	0	0	1	0	0	1	0

Nr count
Final bit on
Ns count
Information frame

7

Bits	0	1	2	3	4	5	6	7
	0	0	0	1	0	0	0	1

Nr count
Final bit on
RR command
Supervisory frame

9

Bits	0	1	2	3	4	5	6	7
	0	1	1	1	0	0	1	1

NSA response
Final bit on
Nonsequenced frame

2

Bits	0	1	2	3	4	5	6	7
	0	1	1	1	0	0	1	1

NSA response
Final bit on
Nonsequenced frame

4

Bits	0	1	2	3	4	5	6	7
	0	0	0	0	0	0	0	0

Nr count
Final bit off
Ns count
Information frame

6

Bits	0	1	2	3	4	5	6	7
	0	0	0	1	0	0	0	1

Nr count
Poll bit on
RR command
Supervisory frame

8

Bits	0	1	2	3	4	5	6	7
	0	1	0	1	0	0	1	1

DISC command
Poll bit on
Nonsequenced frame

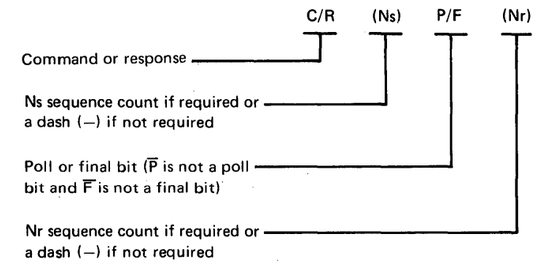
Notes:

1. System/34 microcode looks at the control byte to detect the poll/final bit only.
2. System/34 SDLC IOS turns on the final bit in the last information frame only if seven consecutive information frames are transmitted. If less than seven information frames are transmitted or a busy state exists for this line, the final bit is sent in a supervisory frame (RR or RNR) that follows the last information frame.
3. Most SNA users require that the primary station transmit the first information frame.

Examples of SDLC Commands and Responses

The examples on this page show some of the more common commands and responses between the primary and secondary stations. The examples are for either point-to-point or multipoint networks using half-duplex equipment.

The symbolic format used in the illustration is:



The starting and ending flags, the station address, and the frame check fields are not shown. The station address in every frame is always the address of the secondary station unless it is the general broadcast address (11111111).

Request for Online Status

	C/R	(Ns)	P/F	(Nr)	
The primary station polls the secondary station for transmission.	RR	(—)	P	(0) →	
	← DM	(—)	F	(—)	The secondary station requests an online status.
The primary station sets the secondary station online. The Nr and Ns sequence counts are reset to zero.	SNRM	(—)	P	(—) →	
	← NSA	(—)	F	(—)	The secondary station acknowledges the SNRM command and remains in normal response mode (online).

Secondary Station is Disconnected

	C/R	(Ns)	P/F	(Nr)	
The primary station disconnects the secondary station. (Assume that the secondary station was in normal response mode.)	DISC	(—)	P	(—) →	
	← NSA	(—)	F	(—)	The secondary station acknowledges the DISC command and the adapter is disabled.

Affirmative Response to a Poll

In this example, before the primary station sends the first RR (receive ready) command, assume that the secondary station is in normal response mode.

	C/R	(Ns)	P/F	(Nr)	
The primary station polls the secondary station for transmission.	RR	(—)	P	(0) →	
	← I	(0)	F̄	(0)	The secondary station sends an information frame followed by an RR with the final bit on.
	← RR	(—)	F	(0)	

Negative Response to a Poll

	C/R	(Ns)	P/F	(Nr)	
The primary station sets the secondary station online. The Nr and Ns sequence counts are reset to zero with the SNRM command.	SNRM	(—)	P	(—) →	
	← NSA	(—)	F	(—)	The secondary station acknowledges the SNRM command and remains in normal response mode (online).
The primary station polls the secondary station for transmission.	RR	(—)	P	(0) →	
	← RR	(—)	F	(0)	The secondary station has nothing to send but by responding with an RR, the secondary station remains in normal response mode (online).

Request for Station Identification

When operating on a point-to-point network (switched or nonswitched line), the primary station could request that the secondary stations identify themselves. The primary station transmits an exchange station identification command (XID) using the general broadcast address (11111111). Each secondary station responds with an XID and with its own station address.

	C/R	(Ns)	P/F	(Nr)	
The primary station requests identification from the secondary station.	XID	(—)	P	(—) →	
	← XID	(—)	F	(—)	The secondary station responds with an XID. (The address in the frame is the address of the responding secondary station.)

Exchange of Information Frames

This example shows what happens to the sequence count fields at both stations when information frames are exchanged between the primary station and the secondary station.

The Ns count is the sequence count of the frames that have been sent. The Nr count is the sequence count of the frames that have been received plus 1. For example, if the sequence count of the frames that have been sent (Ns) by the secondary station is 5, the Nr count of the primary station is 6.

The Nr and Ns count fields have a counting capacity of 8 and the counts can wrap around; that is, a count of 7 is sequentially followed by 0. Up to seven frames can be sent before the receiving station must report its Nr count to the transmitting station.

	C/R	(Ns)	P/F	(Nr)	
The primary station sends frames 0 and 1.	I	(0)	P̄	(0) →	
	I	(1)	P	(0) →	
	← I	(0)	F̄	(2)	The secondary station confirms frames 0 and 1 from the primary station and sends frame 0 followed by an RR with the final bit on.
	← RR	(—)	F	(2)	
The primary station confirms frame 0 and polls the secondary station for transmission.	RR	(—)	P	(1) →	
	← I	(1)	F̄	(2)	The secondary station sends four information frames followed by an RR with the final bit on.
	← I	(2)	F̄	(2)	
	← I	(3)	F̄	(2)	
	← I	(4)	F̄	(2)	
	← RR	(—)	F	(2)	
The primary station confirms frames 1-4 (Nr is now 5) from the secondary station and sends two information frames.	I	(2)	P̄	(5) →	Notice that the Nr count of the receiving station is one greater than the Ns count of the transmitting station.
	I	(3)	P	(5) →	

Systems Network Architecture

Systems network architecture (SNA) is the set of protocols (requests and responses) that is commonly understood by all the components in the network that are used to transmit and receive messages.

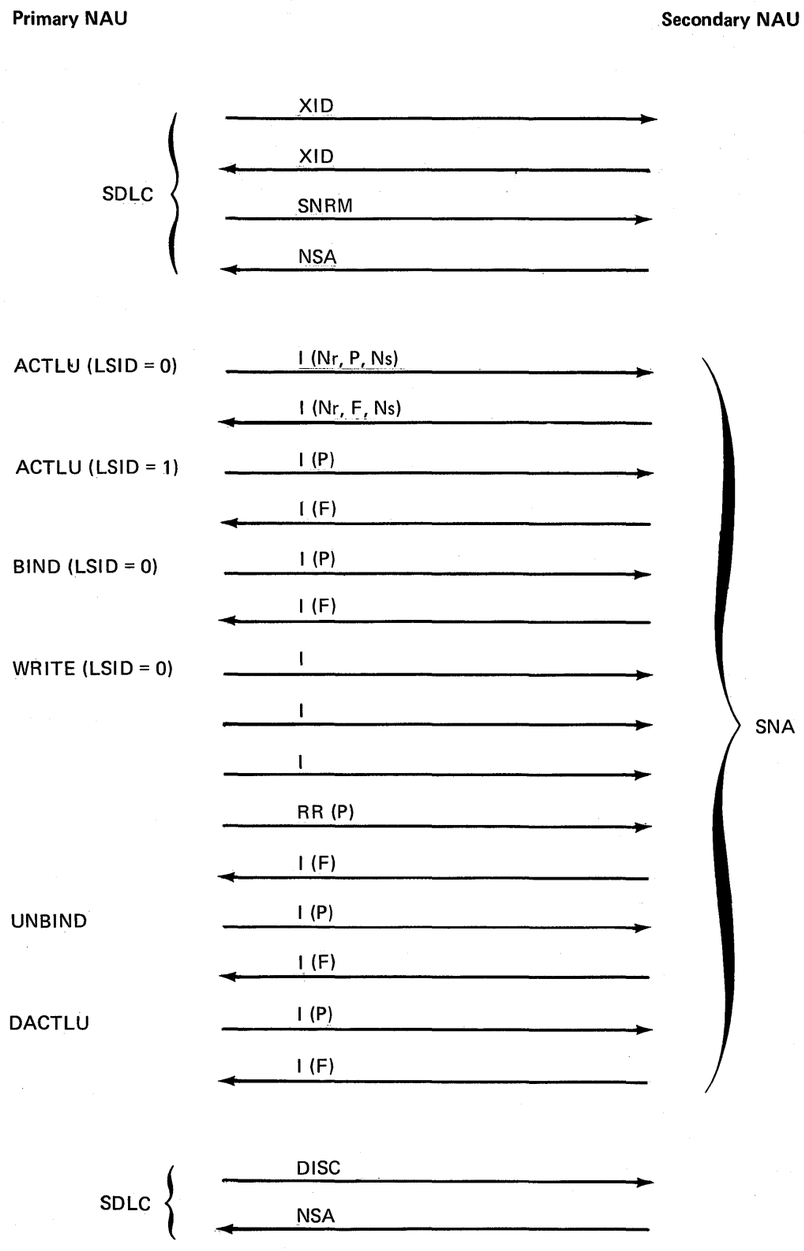
SNA provides a way to:

- Establish a communication session
- Handle a normal communication session
- Allow interrupts
- Terminate the communication session

SNA/SDLC Data Relationship

All data that is transmitted in the information field of the SDLC frame is generated or analyzed by SNA. Also, all SNA information (transmission headers, request/response headers, request units) is handled as normal data in the SDLC information field, and SDLC makes no distinction between these fields and normal data.

Typical SNA/SDLC Sequence



Types of Network Addressable Units

SNA defines three types of network addressable units (NAUs). The first type is the system services control point (SSCP). SSCP is responsible for the general management of the network (such as bringing up the network, establishing sessions, or recovering when a network component has failed to maintain contact). Some of the processes managed by SSCP are identified by commands from network operators who are responsible for the operation of the network. Other SSCP processes serve requests (for example, for sessions) from terminal operators.

The second type of NAU is the physical unit (PU). Each node in the network has an assoicated PU. (Communication controllers provide PU services for certain low-function, attached terminals as a boundary function.) The SSCP establishes a session with each PU in the network as a part of the bring-up process. This session is used to control the physical configuration and the communication system resources associated with the node and also to collect maintenance and operational statistics.

The third type of NAU is the logical unit (LU). The SSCP also establishes a session with each LU in the network as a part of the bring-up process. The LU is the port through which an end user has access to the SSCP-provided services such as session establishment. The LU is the port through which the end user also has access to presentation services provided by the communication system to support end user (or LU-LU) communication. A logical unit can support at least two concurrent sessions, one with the SSCP and one with another logical unit. Some LUs can support multiple sessions with other LUs. For example, in a remote work station environment the application program communicating with a remote 5250 is an LU capable of supporting multiple LU sessions (it can run more than one terminal).

There are three kinds of sessions among NAUs:

- LU to LU
- LU to SSCP
- PU to SSCP

Physical Configuration

The physical configuration of a network is defined in terms of four node types: host, communication controller, cluster controller, and terminal.

It should be noted that devices are physical assemblies that exist in the physical configuration. However, they do not have network addresses and do not exist in the configuration information used by the SSCP. Devices are physical resources that are controlled by the cluster controllers or terminals.

A host node is a facility that contains the system services control point in addition to executing application programs, managing data bases, and so forth.

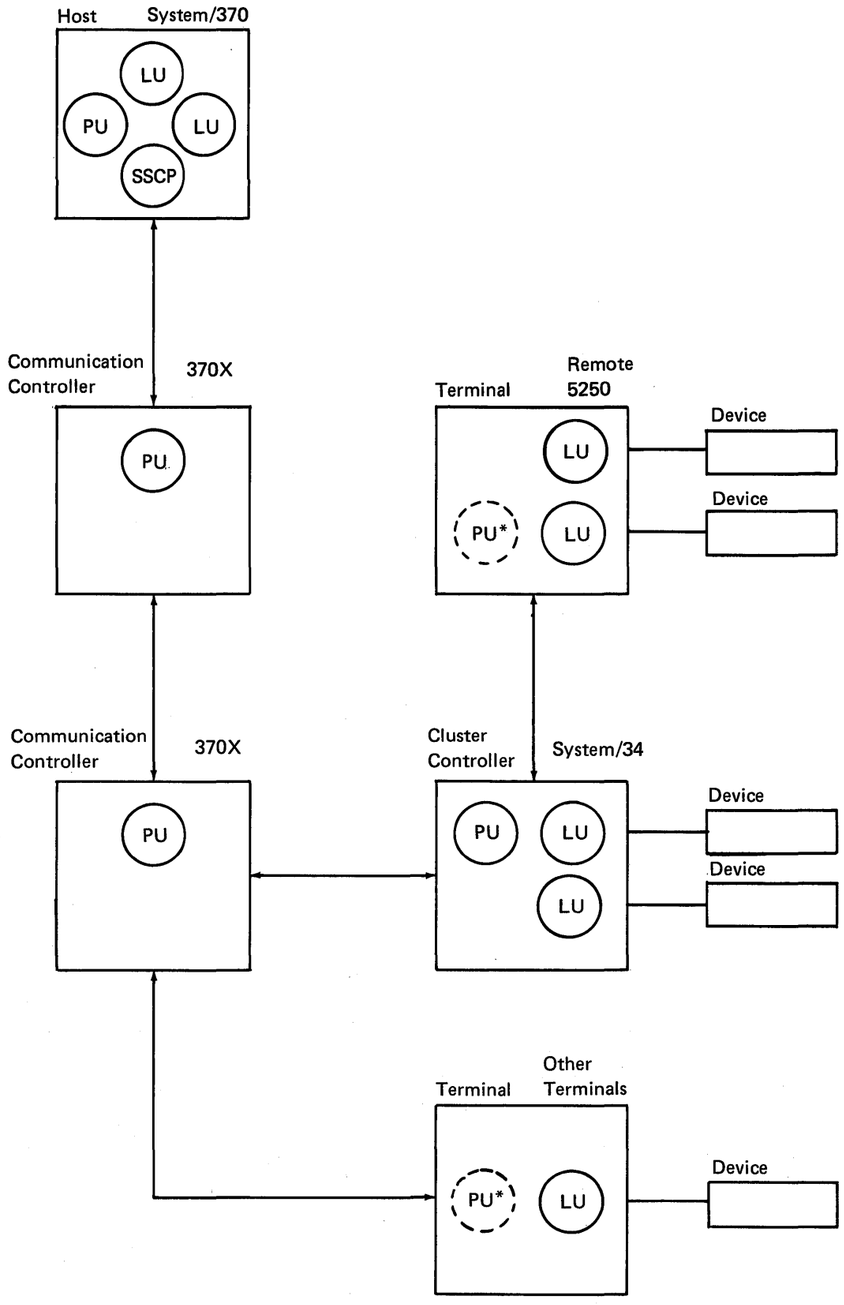
A communication controller node is dedicated to the job of controlling communication lines (and related resources such as buffers) in addition to performing the functions related to supporting one or more subareas.

Cluster controller nodes support the attachment of a wide variety of devices to satisfy the needs of a broad range of end users. Cluster controllers have less network management capability than host nodes or communication controllers.

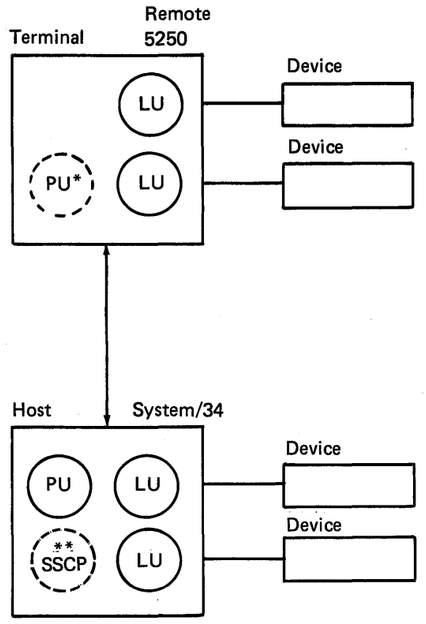
Terminal nodes have the least network management capability of all network nodes.

A communication controller node may provide two types of facilities: intermediate functions and boundary functions. A communication controller node providing an intermediate function routes messages to other subareas based on full network address processing. A communication controller node providing a boundary function converts a full network address (from the host) to a local address form for cluster controller or terminal nodes. Cluster controller and terminal nodes depend on the node to which they are attached for support in scheduling the data flow within a session.

Typical Large System Configuration



Typical System/34 Configuration



*PU services are provided by the attached controller

**SSCP services provided by a host System/34 are not the same as SSCP services provided by a host System/370 but are similar.

SNA/SDLC Buffer

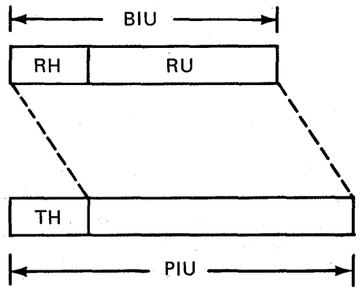
The SNA/SDLC (systems network architecture/synchronous data link control) buffer contains a transmission header (TH) field, a request/response header (RH) field, and a request/response unit (RU) field. Each field is discussed separately later in this section.

Basic Information Unit

The basic unit passed between the connection point manager (CPMGR) and path control (PC) is the basic information unit (BIU). The BIU is made up of a request/response header (RH) built by the connection point manager and attached to the request/response unit (RU).

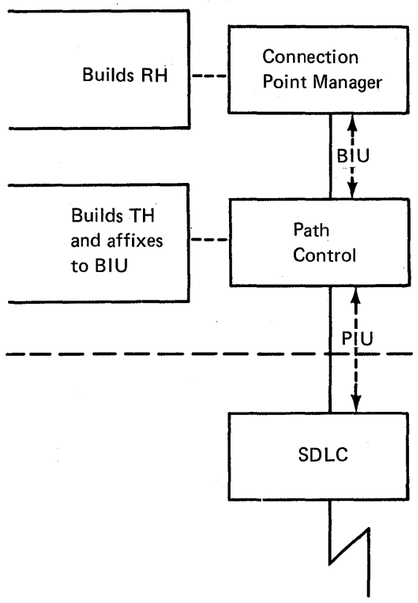
Path Information Unit

A transmission header (TH) is attached to each BIU by path control. The TH contains control information required later by path control in handling the BIU. A TH plus a BIU is a path information unit (PIU).



Basic Transmission Unit

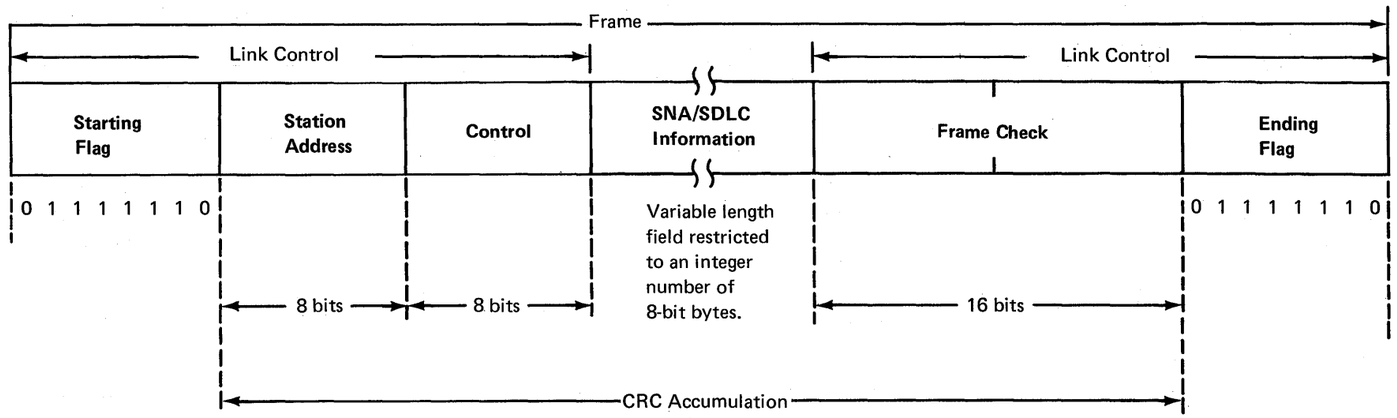
The basic transmission unit (BTU) is the fundamental unit passed between path control and data link control (DLC). A BTU is made up of one or more path information units (PIUs). The term blocking is used to describe the generation of a BTU with more than one PIU. However, blocking is not used with System/34 and is not discussed here.



Basic Link Unit

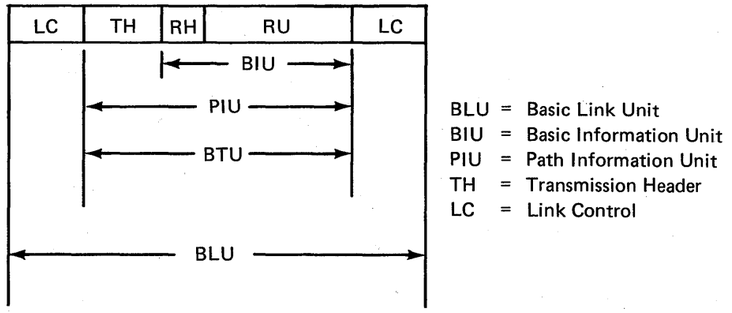
The basic link unit (BLU) is the basic unit of transmission at the data link level; that is, in SDLC the BLU is one frame with the path information unit placed in the information field.

BLU is equal to SDLC Frame is equal to F, A, C, [PIU], FC, F.



Relationship of TH, BIU, PIU, BTU, and BLU

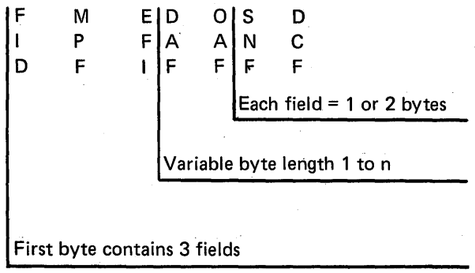
A summary of the relationship of the TH, BIU, PIU, BTU, and BLU is shown below. Link control (LC) is the control information used by the data link. In the case of SDLC, the left LC would be F, A, C, and the right LC would be FC, F.



Transmission Header

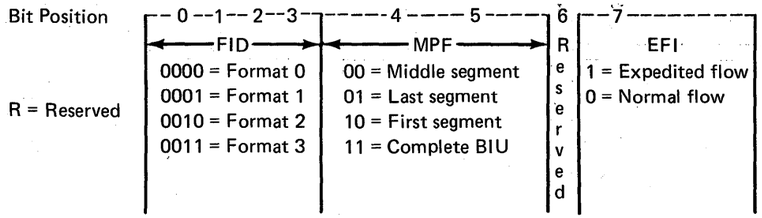
A transmission header (TH) is attached to each BIU that is handled by path control. The TH is made up of a variable number of bytes containing the format identification field (FID), the Mapping Field (MPF), and the expedited flow indicator (EFI), followed by a series of fields that define the associated BIU.

TH Format



FID = Format Identification Field
MPF = Mapping Field
EFI = Expedited Flow Indicator
DAF = Destination Address Field
OAF = Origin Address Field
SNF = Sequence Number Field
DCF = Data Count Field

The bit configuration of the first byte of the TH is:



Format Identification Field

The format identification field (FID) is the first field of the transmission header. The FID is the 4 high-order bits (0-3) of the first byte in the TH. A detailed description of the 4 TH formats is presented later in this section.

Mapping Field

The mapping field (MPF) is 2 bits (bits 4 and 5 of the first byte in the TH), which define the mapping of BIUs into PIUs for transmission.

The bit 4 and 5 settings indicate the following:

00 = Middle segment of a BIU
01 = Last segment of a BIU
10 = First segment of a BIU
11 = Complete BIU

Expedited Flow Indicator

The expedited flow indicator (EFI) determines whether the associated PIU is on the normal or expedited flow. Data on the normal flow must be processed in the order it was entered into the transmission subsystem. Data on the expedited flow may be moved ahead of data on the normal flow; however, within the expedited flow, processing order is maintained. The normal or expedited selection is made above the path control level and is passed as a parameter to path control.

The EFI is a 1-bit field, which is bit 7 of the first byte of the TH. It has the following meaning:

1 = Expedited flow
0 = Normal flow

Destination Address Field

The destination address field (DAF) contains the address of the destination network addressable unit (NAU). The address will be in the form required by the receiving path control. The DAF may be from 1 bit to several bytes, depending on the FID. The DAF is always the destination NAU, and its position in the TH is fixed for any given FID.

Origin Address Field

The origin address field (OAF) contains the address of the originating NAU. The address will be in the form required by the receiving path control. The OAF may be from 1 bit to several bytes, depending on the FID. The OAF is always the address of the originating NAU, and its position in the TH is fixed for any given FID.

Sequence Number Field

The sequence number field (SNF) provides numeric identities for the associated BIU. The content of the SNF is generated by the origin connection point manager and is passed as a parameter to path control. Although the content may be either an actual sequence number or just an identification number, path control will use the SNF only as an identification number.

Data Count Field

The data count field (DCF) contains a binary count of the number of bytes in the BIU associated with the header; the count does not include any of the bytes in the transmission header.

TH Formats

There are four TH formats:

- TH Format 0 (communication controller node)

  TH Format 0 is used between a host node and the communication controller node or between the communication controller node and pre-SNA devices. The remainder of the header fields for FID 0 are the same as those for FID 1 and are described in that section.

- TH Format 1 (communication controller node)

  TH Format 1 is used between a host node and the communication controller node or between the communication controller nodes.

FID 0: 0000
FID 1: 0001

Byte		
0	Format ID Field 1 Mapping Field Reserved Bit Expedited Flow Indicator	Reserved
2	Destination Address Field	
4	Origin Address Field	
6	Sequence Number Field	
8	Data Count Field	
10	Basic Information Unit	

- TH Format 2 (cluster controller node)

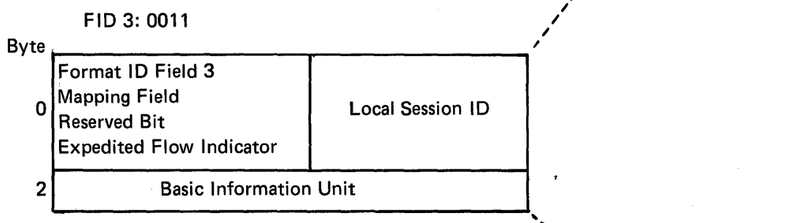
  TH Format 2 is used by path control between cluster controller nodes and the attached communication controller nodes.

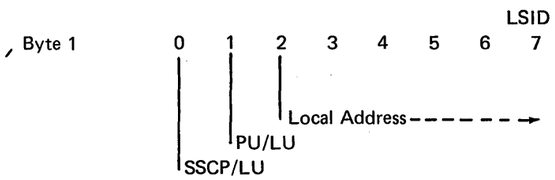
FID 2: 0010

Byte		
0	Format ID Field 2 Mapping Field Reserved Bit Expedited Flow Indicator	Reserved
2	Destination Address Field	Origin Address Field
4	Sequence Number Field	
6	Basic Information Unit	

- TH Format 3 (terminal node)

  TH Format 3 is used by path control, between terminal nodes and their connecting nodes, to provide the boundary function.





In FID 3, the DAF and OAF are replaced by 1 byte — the LSID. This replacement limits what the DAF/OAF can do.

The LSID has three parts:

- Bit 0 (SSCP/LU indicator)

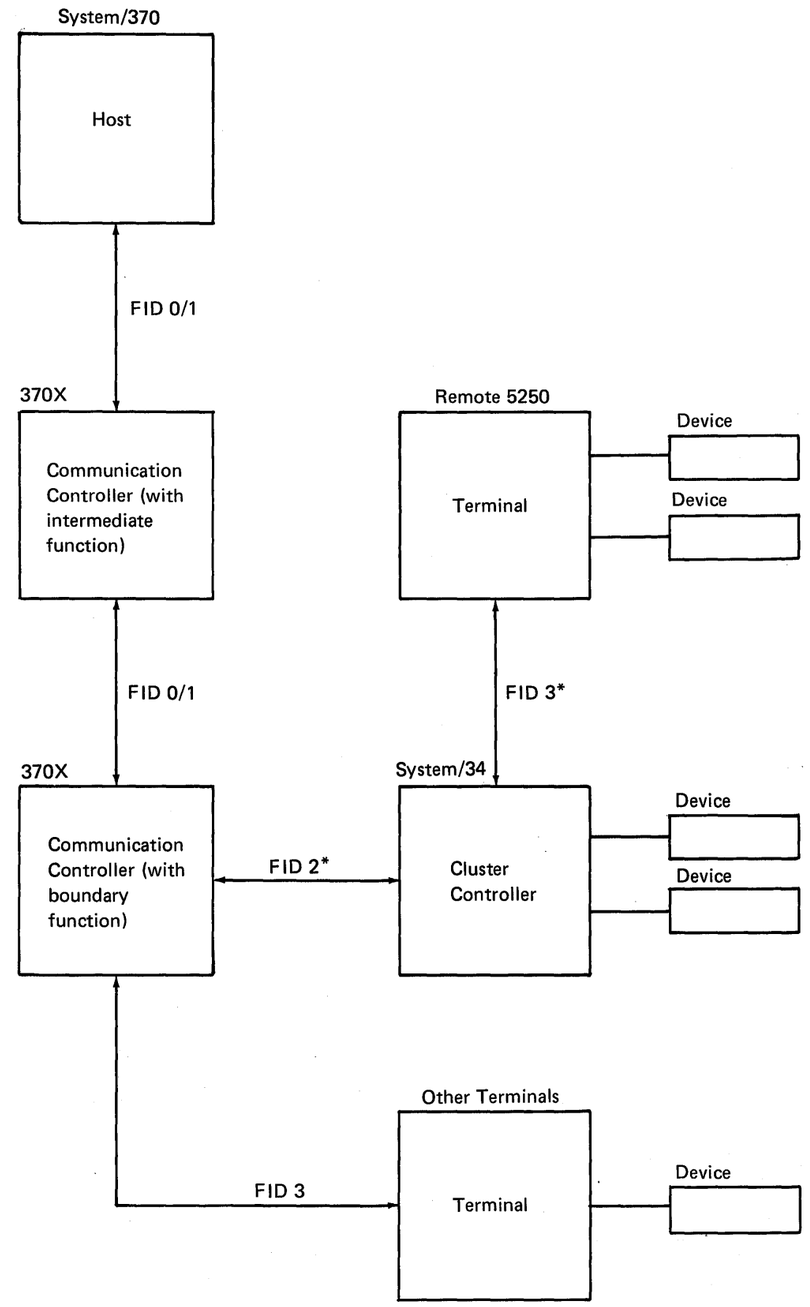
  Indicates if the FID 3 PIU is to be routed to or from the SSCP or an LU.
  0 = SSCP
  1 = LU

- Bit 1 (PU/LU indicator)

  Indicates if the local address (bits 2-7) defines the PU or an LU in the FID 3 NAU.
  0 = PU
  1 = LU

- Bits 2 through 7 (local address)

  When the PU/LU indicator equals 1 (LU), bits 2-7 select one of 64 possible LUs in the FID 3 NAU. When the PU/LU indicator equals 0 (PU), bits 2-7 are reserved and must be set to zero.



*Only FID 2 and FID 3 are used by System/34 in SNA operations.

Request/Response Header

The request/response header (RH) field is 3 bytes long and is attached to each request unit (RU) as the RU passes through the connection point manager. It is possible that the RU that the RH is to be attached to will have a length of zero.

The format of the request header differs from that of the response header. The general format of each header is shown below.

Control Fields in the Request Header Format

Byte 0	Byte 1	Byte 2
Request	Form of response requested	Change of direction control
RU type indicator	Pacing	Begin-end bracket control
Subsystem control indicator		Code selection indicator
Format indicator		
Sense data included indicator		
Chaining control		

Control Fields in the Response Header Format

Byte 0	Byte 1	Byte 2
Response	Response type	Reserved
RU type indicator	Pacing	
Subsystem control indicator		
Format indicator		
Sense data included indicator		
Chaining control		

Request/Response Unit

The request/response unit (RU) is the basic unit of information entering and leaving the transmission subsystem. It may contain commands that control the flow of data through the network, responses to commands, data, or acknowledgment of data.

There are two formats of the RU–the request format and the response format. The information that is placed in the RU and the format used are dependent on the function (command) being performed.

The RU is limited to 256 bytes in length including user data. If the RU is more than 256 bytes long, it must be divided into blocks of 256 bytes or less. This is called chaining. By setting the chain control bit in the request header (RH), SNA can determine which part is the first, middle, last, or only block of a chain.

Session Control Request Units

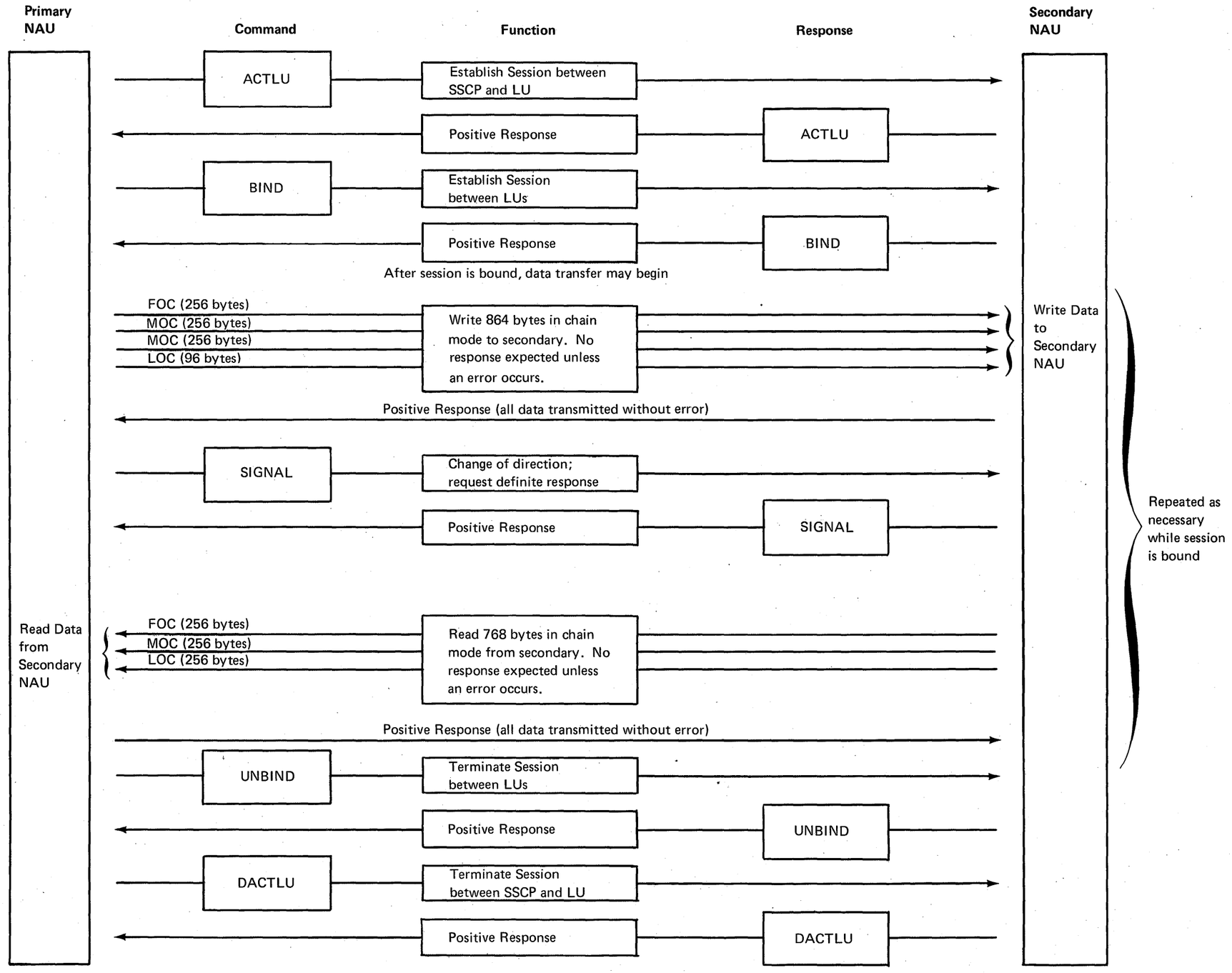
The following is a list of request/response units (commands) used with session control:

- Activate physical unit (ACTPU)
- De-activate physical unit (DACTPU)
- Activate logical unit (ACTLU)
- De-activate logical unit (DACTLU)
- Bind session (BIND)
- Unbind session (UNBIND)
- Start data traffic (SDT)
- Clear (CLEAR)
- Request recovery (RQR)
- Set and test sequence numbers (STSN)

The following is a list of special request units (commands) used with network control. These RUs are special in the sense that they are allowed (under network control) to communicate through the common network using sessions established for other purposes.

- Logic unit status (LUSTAT)
- Signal (SIGNAL)
- Cancel (CANCEL)
- Request shutdown (RSHUTD)
- Request maintenance statistics error log (REQMS)
- Request test (REQTEST)
- Auto network shutdown (ANS)
- Auto network shutdown complete (ANSC)
- Prepare to switch (PREPS)
- Switch complete (SWICOM)
- Initialization complete (INITC)

Typical SNA LU/LU Session Sequence



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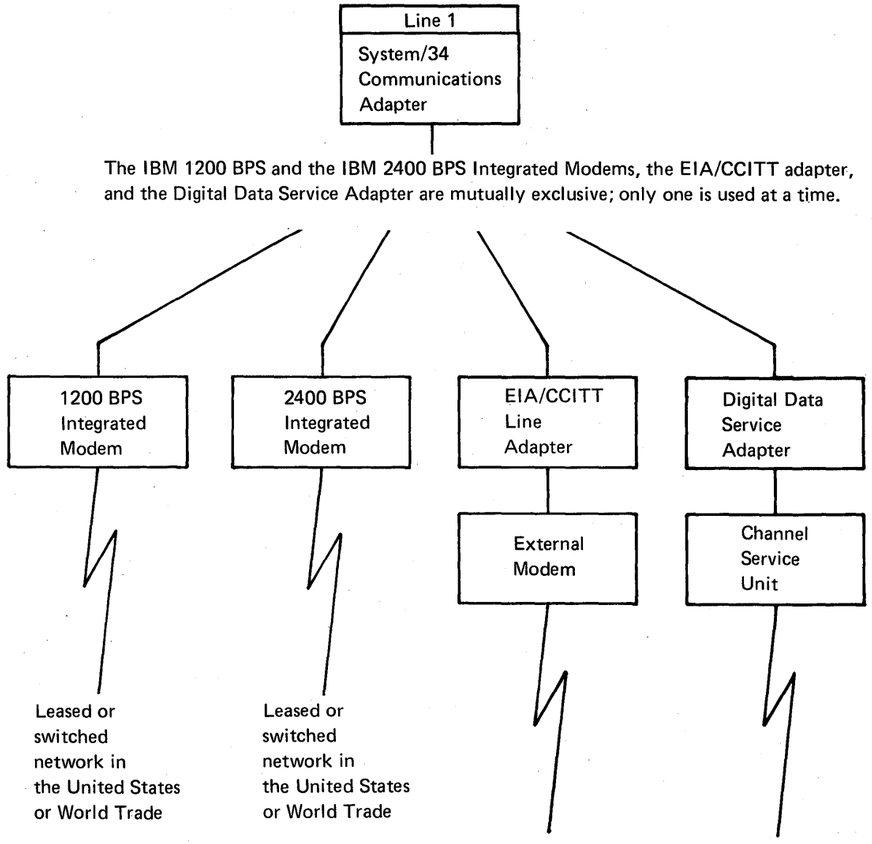
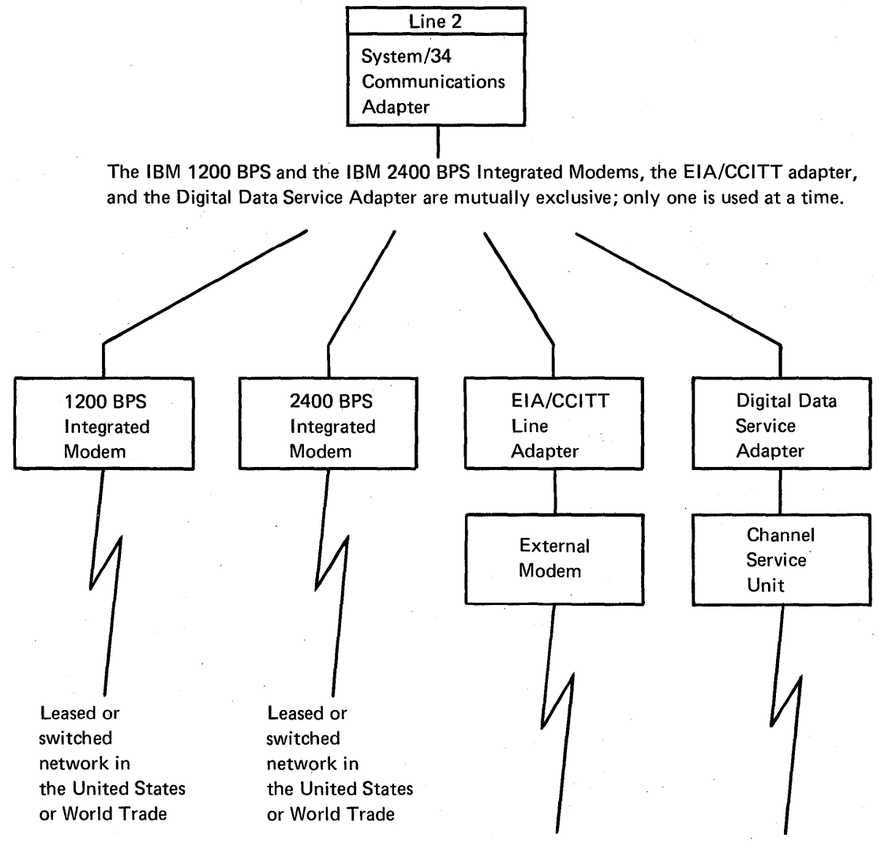
Modems and Interfaces

One of two modems (the IBM 1200 BPS Integrated Modem or the IBM 2400 BPS Integrated Modem) or the Digital Data Service Adapter can be installed in the system on each communication feature (line 1 and line 2). In addition, an external modem can be attached to the system by the EIA/CCITT (Electronic Industries Association/International Consultative Committee on Telegraph and Telephone) line adapter. All are described later in this section.

Communication lines 1 and 2 are not mutually exclusive; that is, the modem used on each line does not have to be the same type. If both adapters are operating at the same time, the sum total of the bit rate must not exceed 9,600 bps.

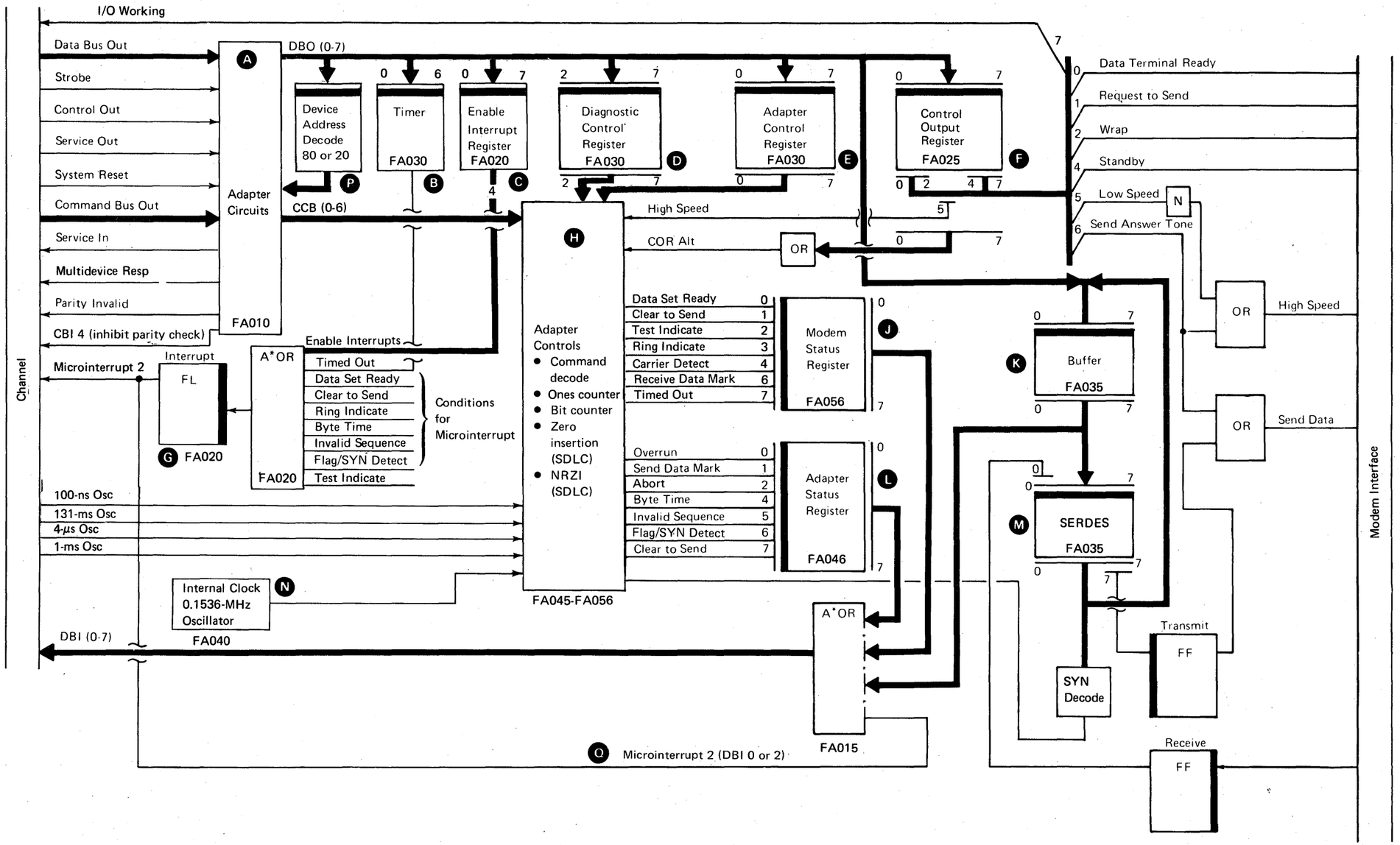




COMMUNICATIONS ADAPTER

Data Flow

The data flow figure shows the functional units of the communications adapter. All functional units that are identified by an alphabetic character are described on the following seven pages. For a logic description of the functional units, see the appropriate FSL page. For example, see FSL page FA030 for a logic description of the adapter control register (E).



Functional Units

The functional units described here are shown in the data flow figure on the preceding page. As an example for all of the registers, a second-level diagram is shown for the adapter control register (E).

Adapter Circuits (A)

The adapter circuits:

- Synchronize the adapter card with the channel
- Repower DBO
- Generate:
  - A 7-bit channel command bus (CCB)
  - Control lines used by the command decode to gate the CCB
  - CBI bit 5 (bad DBO parity)

The adapter circuits let the channel communicate with the attachment through control lines and data buses. The 'control out', 'service out', and 'strobe' lines signal the adapter circuits when data is available on DBO or should be on DBI. The 'service in' and 'multidevice resp' lines signal the channel that the data on DBO has been received or that data is available on DBI.

Data bus out (DBO) is a 9-bit bus (0 through 7 and parity) that performs one of two functions: (1) it supplies an I/O output instruction, or (2) it supplies data to the attachment during service out. On any I/O output instruction, DBO bits 4-7 contain the command modifier during control out. DBO bits 0-3 rely on the instruction type. For example, during control out of a sense microinterrupt, DBO bits 0-3 contain the attachment interrupt level address (1000). During control out of any I/O instruction other than sense microinterrupt, DBO bits 0-3 contain the attachment device address (1000).

Command bus out (CBO) is a 3-bit bus that specifies the type of I/O command to be executed. For the data communications adapter, these commands are:

000 = Not used
001 = Sense microinterrupt
010 = Not used
011 = Not used
100 = I/O load
101 = I/O sense
110 = I/O control load
111 = Not used

Timer (B)

A time-out value (maximum of 16 seconds) is loaded by an I/O control load instruction to start a time-out. A microinterrupt (level 2) occurs after the time-out to indicate that the selected time interval is complete. See *Load Time-out Clock and Registers* later in this section for a second-level diagram of the time-out register.

The following time-outs are used with BSC:

- A 1-second time-out generates an interrupt that the microcode uses to determine when 2 SYN characters are to be transmitted to maintain character phase at the receiving station.
- A 2-second time-out is used during transmit and receive operations. This 2-second time-out is provided to obtain a 2-second delay before transmitting a TTD or a WACK.

During receive operations with busy on, the operation is terminated if a 3.25-second time-out interrupt occurs when:

- Character sync is not established in 3.25 seconds.
- A continuous sync pattern is received for 3.25 seconds.
- No sync pattern is received for 3.25 seconds.

In a receive-initial, multipoint operation, the receive time-out causes the adapter to drop character phase if no sync pattern is received in 3.25 seconds.

For World Trade modems that do not generate answer tones, the BSC adapter holds a 3.25-second space condition on the 'send data' line with the 'request to send' line on. This is similar to an answer tone because it notifies the user that the connection is now complete.

The following time-outs are used with SDLC:

- Inactivity timer (secondary). A 32-second time-out to prevent long periods of inactivity that might result from an error condition.
- Idle detect and nonproductive timer (primary). The idle detect and nonproductive timer (3 seconds and 16 seconds, respectively) provide for error recovery when no response, or a response not recognized by System/34, is received to a poll.

Enable Interrupt Register (C)

Interrupts must be enabled before data is transmitted or received. The enable interrupt register is reset by the 'sense adapter status register' line. See *Sense Data, Registers, and Interrupt Conditions* later in this section for a second-level diagram of the enable interrupt register.

The microinterrupts and their associated DBO bits are:

DBO Bit	Microinterrupt Source
0	Data set ready: Indicates that the data set (modem) is ready to transmit or receive data.
1	Clear to send: Indicates that the modem is ready to transmit data to the communications network.
2	Test indicate: Indicates that the modem is in test mode.
3	Ring indicate: Indicates that the telephone is ringing.
4	Byte time: Indicates that a byte of data must be sent to the attachment during transmit operations, or that a byte of data is ready to be sent to the channel during receive operations.
5	Invalid sequence or abort: For SDLC, indicates that an invalid sequence (11111110) or an abort sequence (11111111) was received.
6	Character sync: Indicates that a SYN character has been received for BSC, or that a flag sequence (01111110) has been received for SDLC.
7	Time-out interrupt: Indicates that the specified time interval in the hardware timer ends.

Diagnostic Control Register (D)

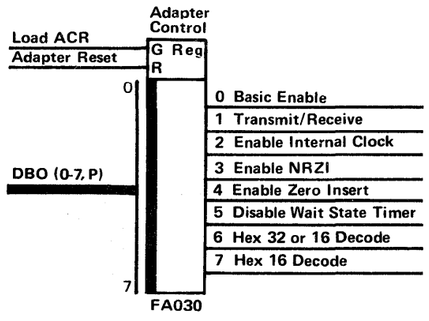
The diagnostic control register is used during problem determination to check the communication circuits between the attachment and the modem. See *Diagnostic Mode and Wrap Test* later in this section for a second-level diagram of the diagnostic control register. The diagnostic lines and their associated DBO bits are:

DBO Bit	Diagnostic Line
0	Not used.
1	Not used.
2	Gate control output register: The control output register and transmit data are gated to the modem.
3	Not used.
4	Gate internal clock oscillator: The internal clock oscillator and receive data are gated to the attachment.
5	Not used.
6	Internal clock test oscillator: A microcode-driven oscillator is supplied for testing.
7	Receive test data mark: Microcode-driven receive data is supplied for testing.

Adapter Control Register (E)

The adapter control register (ACR) is used to control the attachment. This register performs the following functions:

DBO Bit	ACR Function
0	Basic enable: Enables the circuits to transmit or receive data.
1	Transmit/receive: Causes the adapter to enter transmit or receive mode.
2	Enable internal clock: Enables the internal clock to supply transmit and receive timing pulses.
3	Enable NRZI: For SDLC, enables the NRZI circuits. The data transmitted or received is encoded or decoded in NRZI. When BSC is used, this bit disables the NRZI circuits.
4	Enable zero insert: For SDLC, lets the attachment insert a 0-bit after five consecutive 1-bits.
5	Disable wait state timer: Prevents the wait state time-out from resetting the control output register when the system clock stops.
6	If on, enables SYN decode in attachment for BSC; if off, transmits or receives flags for SDLC.
7	Select ASCII: Selects ASCII SYN (instead of an EBCDIC SYN) if SYN is selected.



Control Output Register (F)

The control output register is reset by the 'system reset' line or at the end of the wait state timer. See *Load Time-out Clock and Registers* later in this section for a second-level diagram of the control output register. This register controls the attachment operations using the following bits:

DBO Bit	Attachment Operation
0	Data terminal ready: Indicates that the attachment is enabled.
1	Request to send: Signals the modem to enter transmit mode.
2	Wrap: Permits data to be sent through an IBM modem back through the receive circuits. The received data can then be compared with the transmitted data; this permits testing of the communications adapter and the IBM modem.
3	Not used.
4	Standby: Causes IBM modems to select the switched network backup (SNBU) line.
5	Low speed: Causes the modem and the internal clock to send or receive data at half rate.
6	Send answer tone: Sends an answer tone; for modems that do not send an answer tone, forces high speed and sends data space.
7	I/O working: Informs the control processor that microinterrupts might occur.

Interrupt Latch (G)

The interrupt latch is set when the adapter needs a microinterrupt request. See *Sense Data, Registers, and Interrupt Conditions* later in this section for a second-level diagram of the interrupt latch.

Controls (H)

The controls contain the logic necessary for transmitting and receiving data. See *Adapter Controls* on the next page for a description of the control circuits.

Modem Status Register (J)

The modem status register contains the status of the modem; the status is sent to the channel. The modem status register is not a register but is shown as a register for purposes of the data flow.

Buffer (K)

The buffer contains (1) the data byte from main storage that is ready to be transmitted, or (2) the received data byte that is ready to be stored in main storage. See *Load/Sense Buffer* later in this section for a second-level diagram of the buffer.

Adapter Status Register (L)

The adapter status register contains the status of the adapter; the status is sent to the channel. The adapter status register is not a register but is shown as a register for purposes of the data flow.

SERDES (M)

During receive operations, the serializer/deserializer (SERDES) assembles the data received bit-by-bit into data bytes. During transmit operations, the SERDES sends the data byte to the transmit trigger.

Oscillator (N)

The oscillator is used by the internal clock feature. The oscillator card is located in A-A2Q2. Only one internal clock feature is required to supply internal clocking to either or both communication lines that require internal clocking.

Device Address (P)

The address switch on the adapter card is set to respond to a device address of 80 or 20. If one communication line is installed, address 80 should be used. If line 1 and line 2 are installed, and either line uses a data rate transfer speed greater than 4,800 bps, that line must use the device address of 80. The use of device address 80 by an adapter for a communication line configured as such will cause the use of the higher priority microcode and microinterrupt request bit.

Microinterrupt Bit (Q)

If device address 80 is set in the address switch on the adapter card, microinterrupt request bit 0 (DBI 0) is used. If device address 20 is set on the adapter card, microinterrupt request bit 2 (DBI 2) is used.

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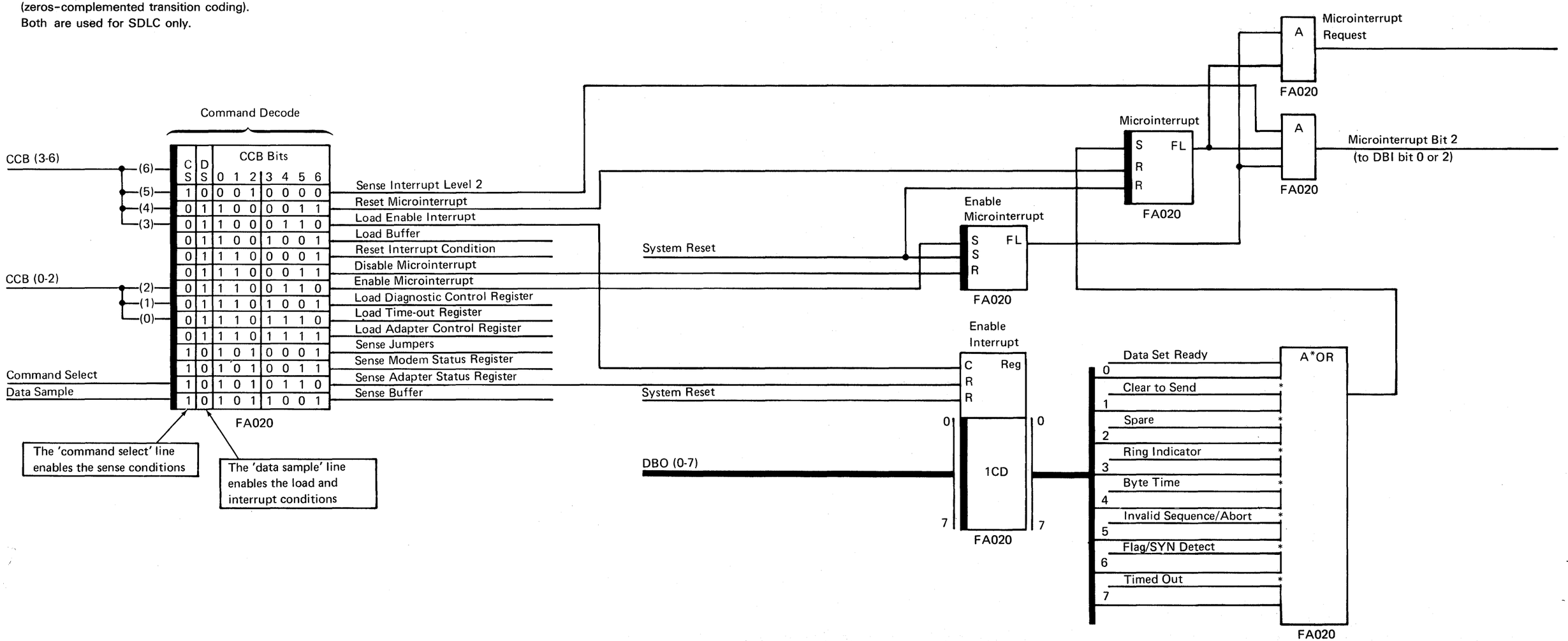
Adapter Controls

The following pages show and describe the circuits contained in the *Controls* block (H) on the data flow figure. Included in these circuits are:

- Command decode.
- Ones counter.
- Bit counter.
- Zero insertion and NRZI (zeros-complemented transition coding). Both are used for SDLC only.

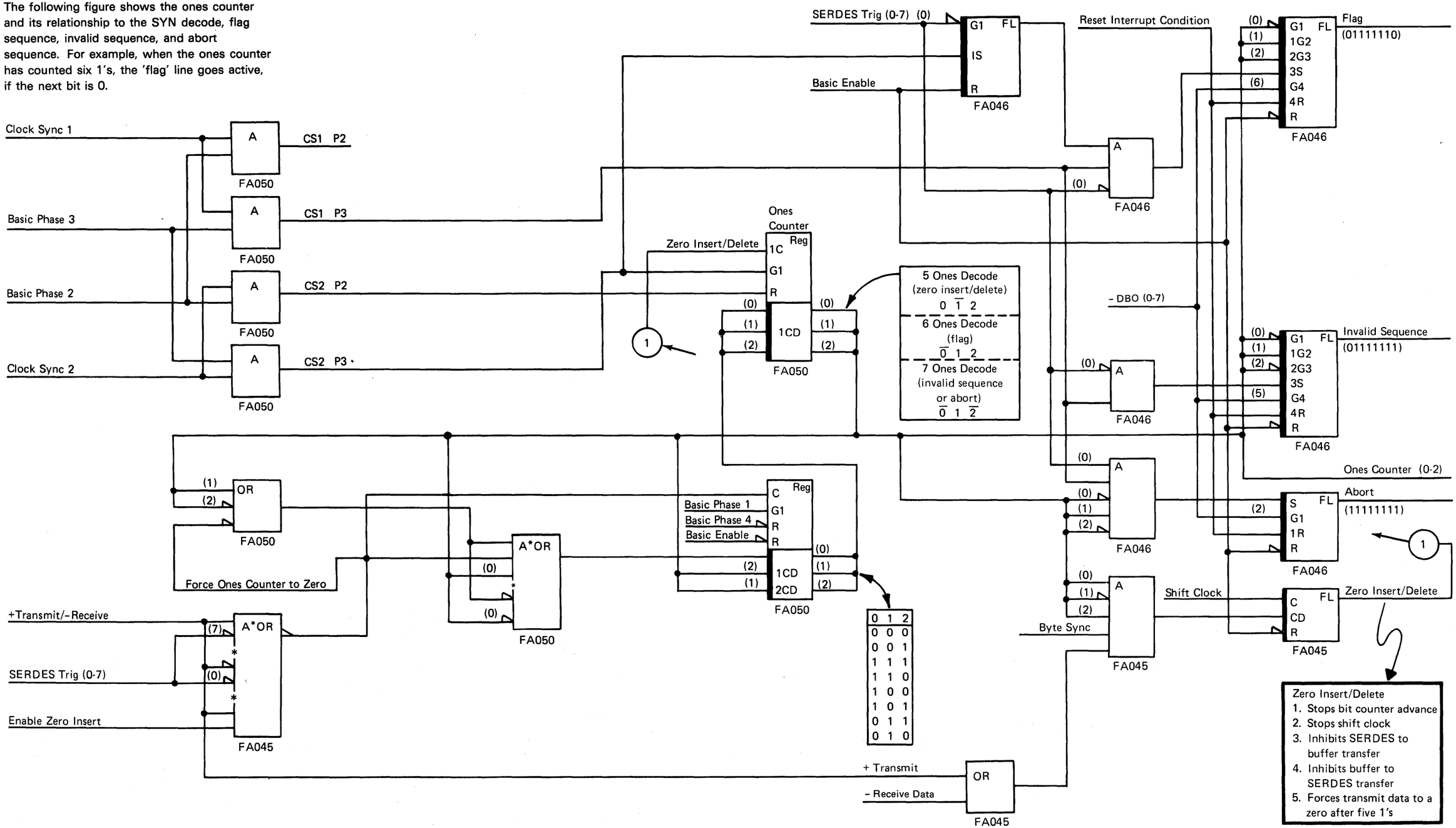
Interrupts and Command Decode

The following figure shows the interrupt and command decode logic for the communications adapter. This logic is part of the adapter control and interrupt logic shown in the data flow figure. See the command decode logic block below for definitions of the CCB bits.



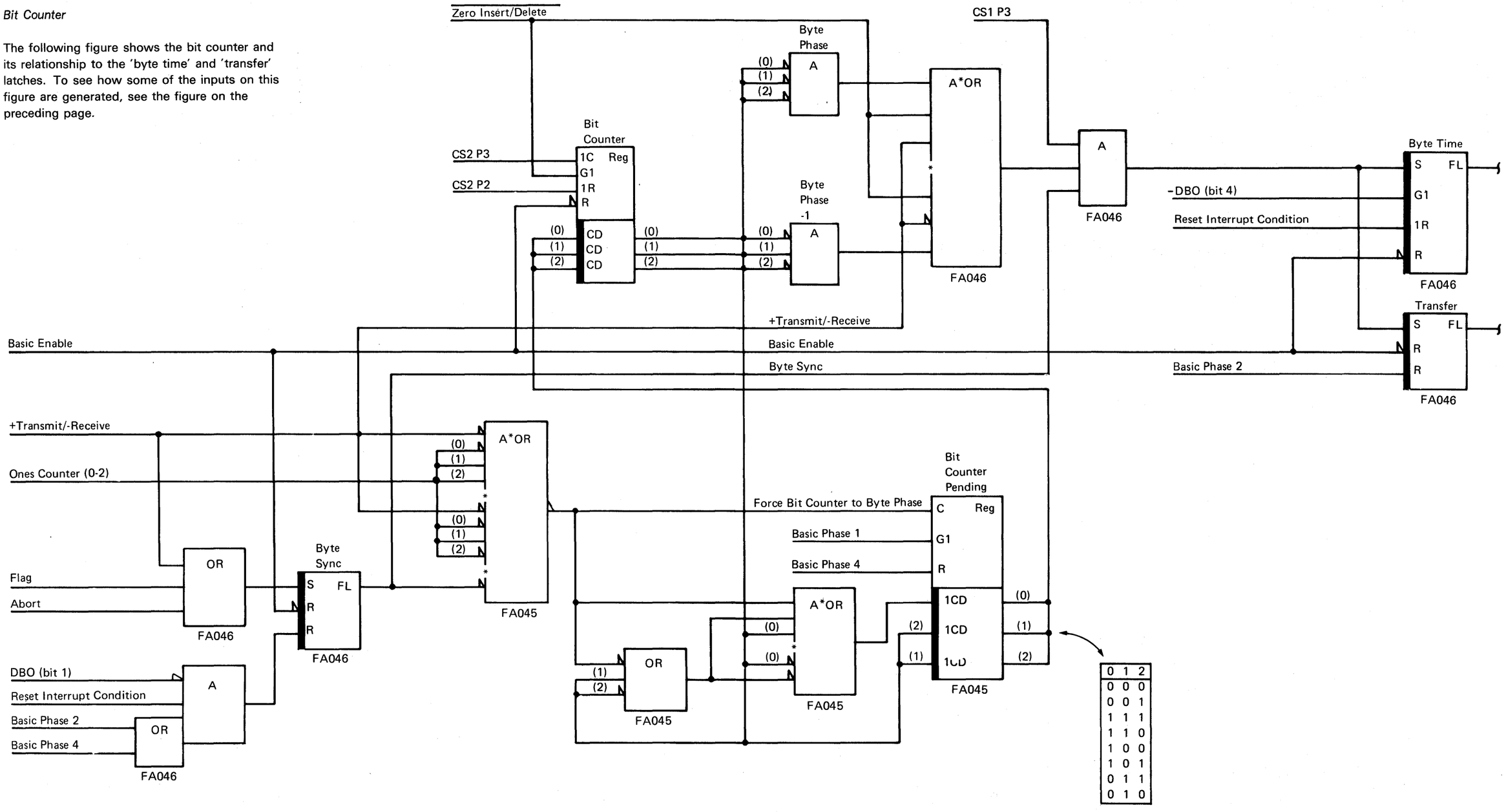
Ones Counter

The following figure shows the ones counter and its relationship to the SYN decode, flag sequence, invalid sequence, and abort sequence. For example, when the ones counter has counted six 1's, the 'flag' line goes active, if the next bit is 0.



Bit Counter

The following figure shows the bit counter and its relationship to the 'byte time' and 'transfer' latches. To see how some of the inputs on this figure are generated, see the figure on the preceding page.



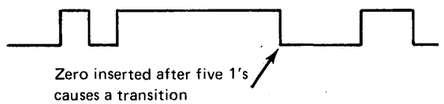
0	1	2
0	0	0
0	0	1
1	1	1
1	1	0
1	0	0
1	0	1
0	1	1
0	1	0

Zero Insertion and NRZI

In data communications (SDLC only), NRZI is a method of encoding data; it prevents extended periods of transitionless data by complementing the state of the data when transmitting a 0-bit. Also, a transition must occur after the transmission of no more than five 1-bits (zero insertion/deletion adds a 0-bit after five consecutive 1-bits). The logic diagram and the following figure show how NRZI complements the state of the data when transmitting a 0-bit; the figure also shows that zero insertion inserts a zero after five 1-bits.

Data From Buffer	1 1 0 0 0 1 1 1 1 1 1 1 0 1 0
Data After Zero Insertion	1 1 0 0 0 1 1 1 1 1 0 1 1 0 1 0

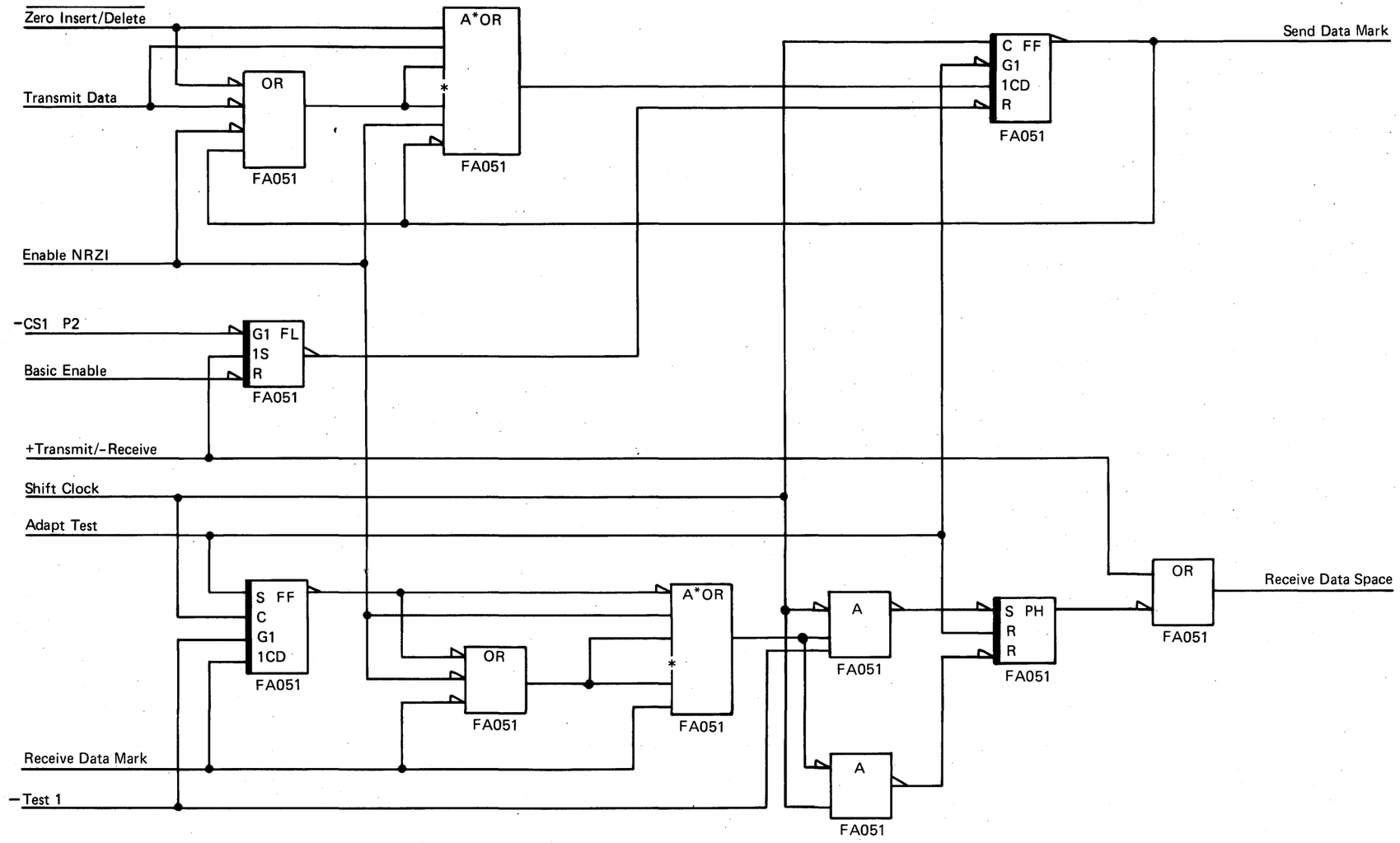
Waveshape with Zero Insertion and NRZI



To maintain bit synchronization, NRZI must be used with nonsynchronous modems (needing the internal clock) and with those synchronous modems that are sensitive to transitionless bit streams.

If a synchronous modem is being used and its sensitivity to transitionless bit streams cannot be determined, contact the IBM marketing representative.

CAUTION
All DTEs (data terminal equipment) on the same data link must use the same encoding method (NRZI or non-NRZI). There is no communication between DTEs if the same method is not used.



System Level Interface

The system level interface includes a supervisor call input/output (SVC I/O) request instruction and an associated IOB. The supervisor call input/output request instruction places commands to the communications adapter on a queue.

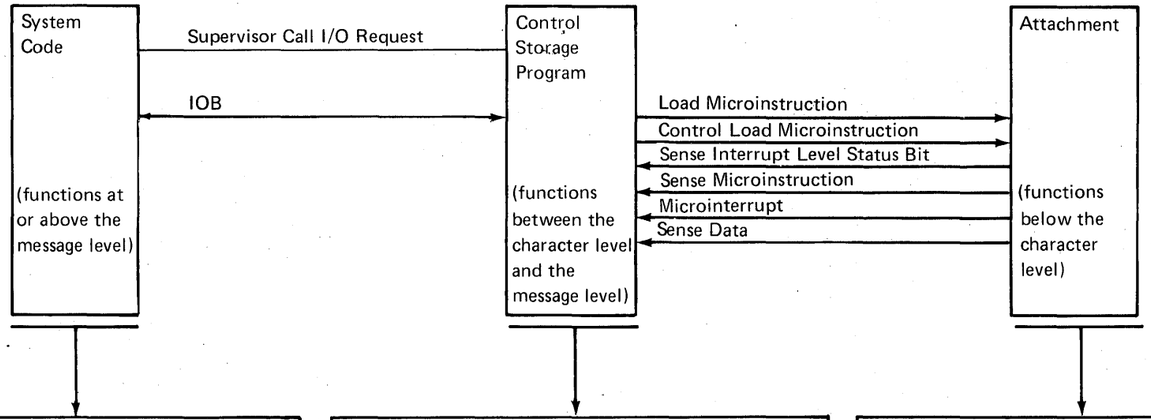
Queue

The system level interface has an assigned queue. Commands to the communications adapter are placed on this queue by the supervisor call input/output request instruction with index register 1 pointing to the IOB. The IOB is moved from the communication queue to the correct line queue (line 1 or line 2). As many commands as are needed can be placed on each line queue with an IOB associated with each supervisor call.

Input/Output Blocks

Program operation of the communications adapter is executed by the input/output block (IOB) associated with the supervisor call input/output request instruction. More than one operation can be set up by queuing the IOBs. The IOB contains all information needed to carry out the operation. At the end of each operation, the completion code is set and the next operation on the queue is started. For definitions of each byte in the BSC and SDLC input/output blocks, see the *Data Areas Handbook*.

SYSTEM LEVEL INTERFACE BETWEEN SYSTEM CODE AND ATTACHMENT



The system code:
- Uses the system level instructions during a transmit operation to format the message; the necessary control information (such as STX, ETX, and so on) is inserted into the message to be transmitted.
- Uses the system level instructions during a receive operation to process the data received.
- Is used to set up the starting conditions before issuing an SVC I/O request. The starting conditions consist of:
  - Loading the data buffer address in the IOB.
  - Issuing an SVC I/O request instruction to enable the adapter.
- Performs error recovery.

After an SVC I/O request instruction is issued, the microcode interface controls the execution of the specified operation (transmit or receive).

The control storage program:
- Performs limited control character analysis (decodes STX, ETX, EOT, ACK0, and so on). For example, 55, SYN, or SOH places the BSC adapter in data mode which enables BCC checking.
- Inserts characters (such as SYN, BCC, pad, and so on) in the message as required.
- Generates the block check character (BCC).
- Compares the received block check character with the generated block check character to determine if the data was received correctly.
- Processes microinterrupts.
- Transfers data between main storage and the adapter.
- Updates the buffer addresses.
- Checks to determine if the buffer length has been exceeded.
- Processes microinterrupts.
- Compares for station address recognition.

Note: The above examples pertain only to BSC.

The attachment:
- Establishes and maintains bit phase.
- Generates microinterrupts.
- Provides clock pulses to synchronize the attachment with the modem.
- Detects DBO parity errors and character overrun conditions.
- Transmits data (serializes data).
- Receives data (deserializes data).
- Generates character microinterrupts.

Operations

The operations for BSC and SDLC are described in Chapter 9 of the *Functions Reference Manual*. For each operation, the following paragraphs give (1) the command code (Q code), (2) the control storage objectives, and (3) the hardware objectives.

BSC Receive Only

The Q-code for a BSC receive-only operation is hex 81.

Control Storage Program Objectives

The control storage program objectives for a receive-only operation are to:

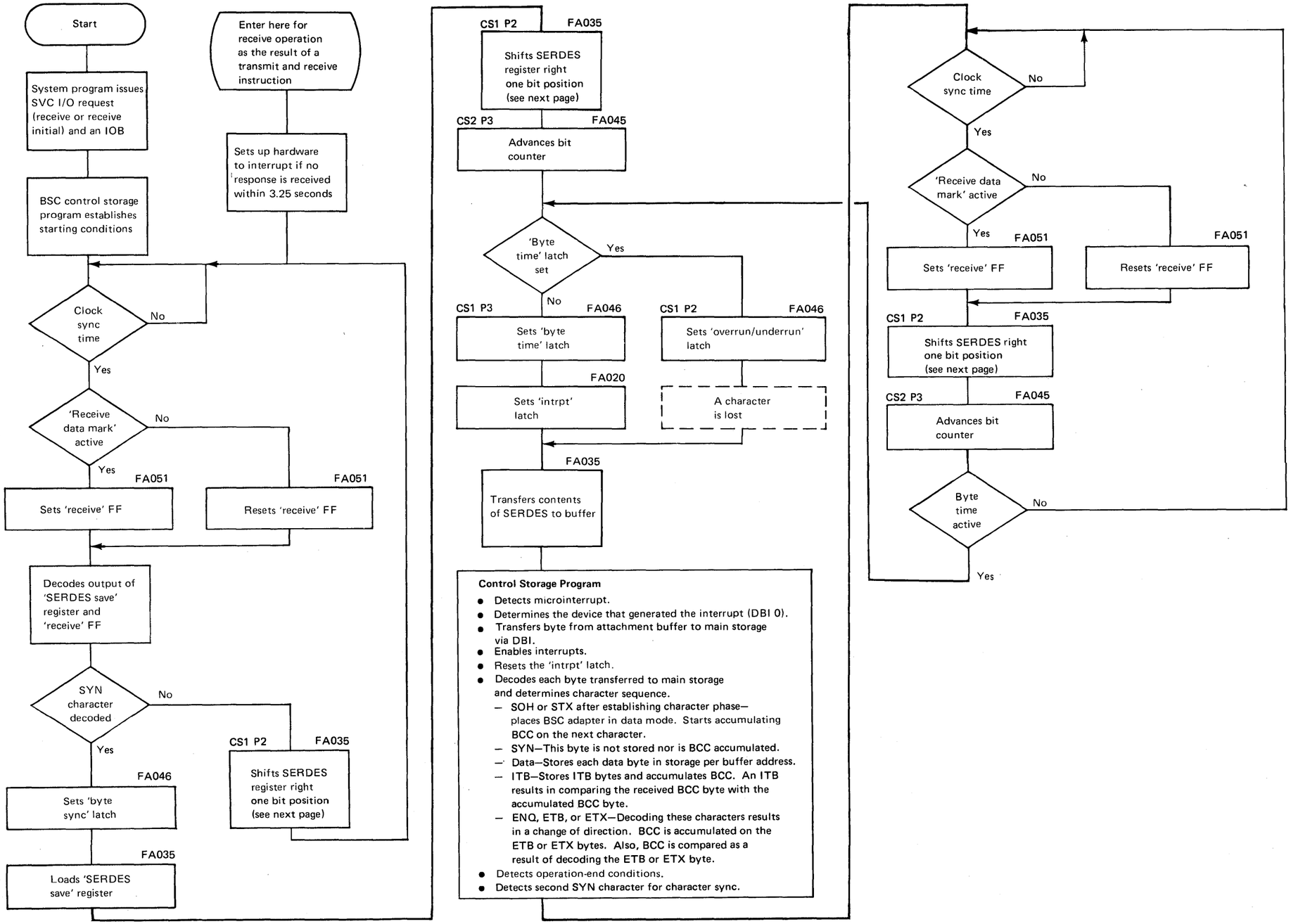
- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Sense the second SYN character to complete character phase. (The first SYN character is sensed by hardware.)
- Set up hardware to enable a microinterrupt after a 3.25-second interval.
- Store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Analyze each character to:
  - Set or reset data mode.
  - Enter transparency mode. To enter transparency mode, receive DLE, STX sequence; to exit transparency mode, receive DLE ENQ, DLE ETX, DLE ETB, or DLE ITB.
  - Sense change-of-direction character sequences.
- Decrease the receive buffer length.
- Check when the receive buffer length is 0.
- Accumulate block check character bytes.
- Compare the accumulated block checking information with the received block checking information.
- Post IOB complete when:
  - A change-of-direction character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for a receive-only operation are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is deserialized.
- Sense receive adapter checks.
- Sense the 3.25-second time-out and generate a time-out microinterrupt.

BSC Receive Flowchart

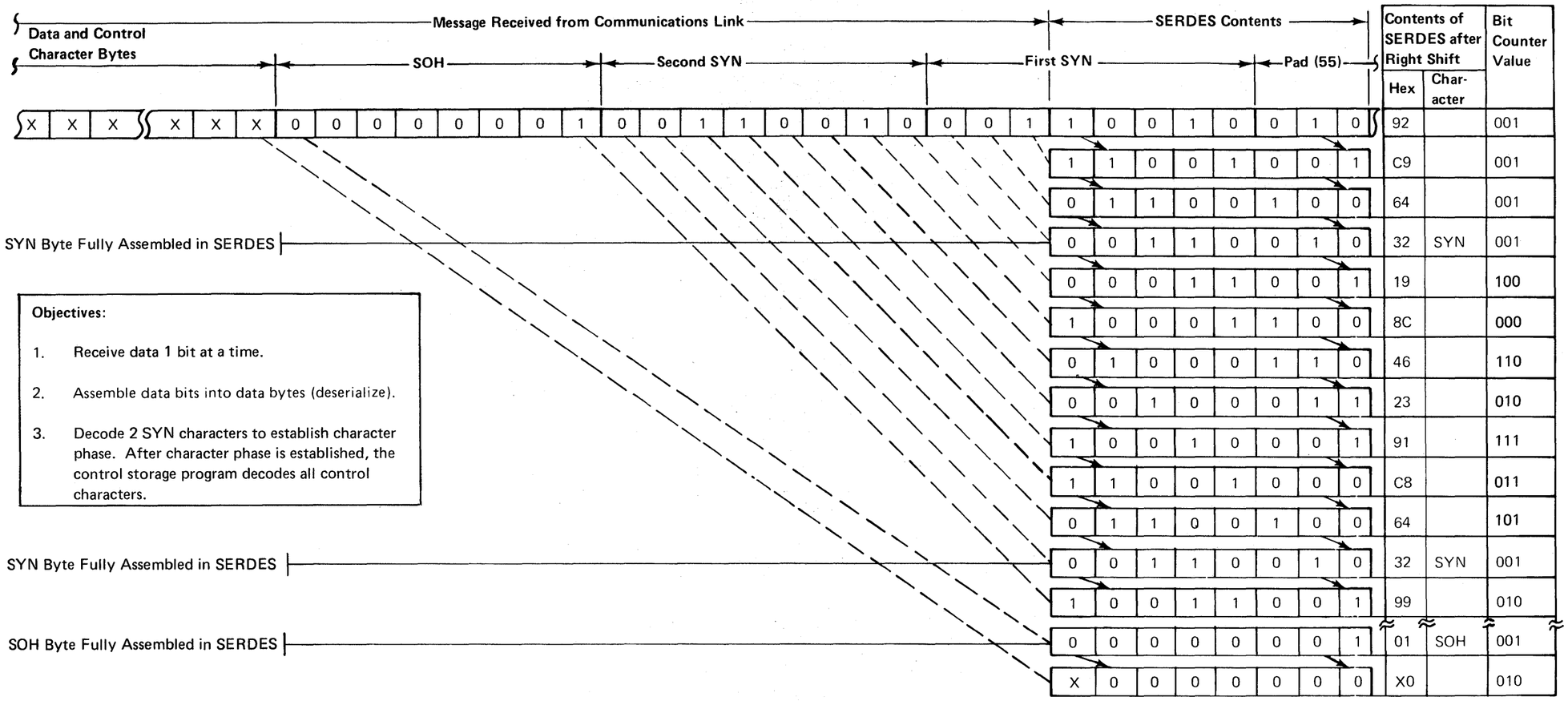


Control Storage Program

- Detects microinterrupt.
- Determines the device that generated the interrupt (DBI 0).
- Transfers byte from attachment buffer to main storage via DBI.
- Enables interrupts.
- Resets the 'intrpt' latch.
- Decodes each byte transferred to main storage and determines character sequence.
  - SOH or STX after establishing character phase—places BSC adapter in data mode. Starts accumulating BCC on the next character.
  - SYN—This byte is not stored nor is BCC accumulated.
  - Data—Stores each data byte in storage per buffer address.
  - ITB—Stores ITB bytes and accumulates BCC. An ITB results in comparing the received BCC byte with the accumulated BCC byte.
  - ENQ, ETB, or ETX—Decoding these characters results in a change of direction. BCC is accumulated on the ETB or ETX bytes. Also, BCC is compared as a result of decoding the ETB or ETX byte.
- Detects operation-end conditions.
- Detects second SYN character for character sync.

Contents of SERDES Register

The following figure shows the contents of the SERDES register after a right shift.



BSC Receive Initial Delayed (Multipoint)

The Q-code for a BSC receive-initial-delayed operation is hex 82.

Control Storage Program Objectives

The control storage program objectives for a BSC receive-initial-delayed operation are to:

- Enter receive initial delayed in control mode.
- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Sense the second SYN character to complete character phase. (The first SYN character is sensed by hardware.)
- When character phase is complete, load the time-out clock to a 3.25-second value and enable the time-out microinterrupt.
- Sense the @, @, ENQ sequence to put the adapter in addressed mode.
- In addresed mode, store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Post the IOB complete when:
  - An ENQ character is sensed.
  - The receive buffer length is 0.
- If a 3.25-second time-out microinterrupt occurs, enter receive initial delayed in control mode.

Hardware Objectives

The hardware objectives for a receive-initial-delayed operation are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is to be sent to main storage.
- Sense overrun conditions.

BSC Receive Initial (Point-to-Point)

The Q-code for a BSC receive-initial operation is hex 83.

Control Storage Program Objectives

The control storage program objectives for a BSC receive-initial operation (point-to-point) are to:

- Enable interrupts (on a switched network) to indicate when the 'data set ready' line becomes active by generating a microinterrupt.
- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Sense the second SYN character to complete character phase. (The first SYN character is sensed by hardware.)
- When character phase is complete, or on a switched network when the 'data set ready' line goes active, load the time-out clock to a 3.25-second value and enable the time-out microinterrupt.
- Store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Post the IOB complete when:
  - An ENQ character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for a BSC receive-initial operation (point-to-point) are to:

- Generate a microinterrupt when the 'data set ready' line goes active.
- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is to be sent to main storage.
- Sense overrun conditions.

BSC Receive Initial (Multipoint)

The Q-code for a BSC receive-initial operation is hex 83.

Control Storage Program Objectives

The control storage program objectives for a BSC receive-initial operation (multipoint) are to:

- Enter receive initial by sensing a SYN, SYN, EOT, PAD sequence. This sequence puts the adapter in control mode.
- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Sense the second SYN character to complete character phase. (The first SYN character is sensed by hardware.)
- When character phase is complete, load the time-out clock to a 3.25-second value and enable the time-out microinterrupt.
- In control mode, sense the @, @, ENQ sequence. This sequence puts the adapter in addressed mode.
- In addressed mode, store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Post the IOB complete when:
  - An ENQ character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for a BSC receive-initial operation (multipoint) are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is to be sent to main storage.
- Sense overrun conditions.

BSC Transmit/Receive Overlay

The Q-code for a BSC transmit/receive overlay operation is hex 84.

Control Storage Program Objectives

The control storage program objectives for the transmit portion of a transmit/receive overlay operation are to:

- Activate the 'request to send' line to the attachment, and enable the hardware to interrupt when the 'clear to send' line from the modem goes active.
- Encode BSC characters (SYNs, PAD characters, and BCC only).
- Send data characters from the main storage buffer to the BSC attachment buffer.
- Enable hardware to interrupt when another character is to be sent to the attachment.
- Load the time-out clock for a 1-second interval (half-second for the internal clock and half rate). The control storage program uses the time-out clock to determine when to insert 2 SYN characters in the data message.
- Analyze each character to:
  - Set or reset data mode.
  - Enter or exit transparency mode.
  - Sense turnaround sequences.
- Accumulate the block check character (BCC) and store it in the BCC buffer. Send the BCC character when end of transmit is sensed.
- Sense end-of-transmit operations. When the transmit buffer length is 0, the adapter updates the buffer pointer to the start of the buffer (the receive buffer overlays the transmit buffer). Then, the adapter starts to receive data. When the receive buffer length is 0, the operation ends and the IOB is posted complete.

The control storage program objectives for the receive portion of a transmit/receive overlay operation are to:

- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Set up hardware to enable microinterrupts after a 3.25-second interval.
- Store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Analyze each character to:
  - Set or reset data mode.
  - Enter transparency mode. To enter transparency mode, receive DLE, STX sequence; to exit transparency mode, receive DLE ENQ, DLE ETX, DLE ETB, or DLE ITB.
  - Sense change-of-direction character sequences.
  - Sense the SYN, SYN, EOT, PAD sequence, and start executing the receive command if the command was issued.
- Decrease the receive buffer length.
- Check when the receive buffer length is 0.
- Accumulate block check character (BCC) bytes.
- Compare the accumulated BCC with the received BCC.
- Post IOB complete when:
  - A change-of-direction character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for the transmit portion of a transmit/receive overlay operation are to:

- Activate the 'request to send' line, and generate a microinterrupt when the 'clear to send' line goes active.
- Transmit data bytes bit-by-bit (serialize).
- Generate character microinterrupts when another byte of data is to be sent to the attachment.
- Signal the program when the time interval loaded into the timer is complete.
- Sense transmit adapter checks.

The hardware objectives for the receive portion of a transmit/receive overlay operation are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is deserialized.
- Sense receive adapter checks.
- Sense the 3.25-second time-out and generate the time-out microinterrupt.

BSC Transmit/Receive Initial (Multipoint)

The Q-code for a BSC transmit/receive initial operation is hex 85.

Control Storage Program Objectives

The control storage program objectives for the transmit portion of a transmit/receive initial operation are to:

- Activate the 'request to send' line to the attachment, and enable the hardware to interrupt when the 'clear to send' line from the modem goes active.
- Encode BSC characters (SYNs, PAD characters, and BCC only).
- Send data characters from the main storage buffer to the BSC attachment buffer.
- Enable hardware to interrupt when another character is to be sent to the attachment.
- Load the time-out clock for a 1-second interval (half-second for the internal clock and half rate). The control storage program uses the time-out clock to determine when to insert 2 SYN characters in the data message.
- Analyze each character to:
  - Set or reset data mode.
  - Enter or exit transparency mode.
  - Sense turnaround sequences.
- Accumulate the block check character (BCC) and store it in the BCC buffer. Send the BCC character when end of transmit is sensed.
- Sense end-of-transmit operations. If the transmit buffer length is 0 and the receive buffer length is not 0, the adapter goes into receive-initial mode. If the transmit and receive buffer lengths are both 0, the operation ends and the IOB is posted complete.

The control storage program objectives for the receive portion of a transmit/receive initial operation are to:

- Enter transmit/receive initial by sensing a SYN, SYN, EOT, PAD sequence. This sequence puts the adapter in control mode. If bit 7 of the command modifier is on, the adapter starts a receive-initial operation.
- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Sense the second SYN character to complete character phase. (The first SYN character is sensed by hardware.)
- When character phase is complete, load the time-out clock to a 3.25-second value and enable the time-out microinterrupt.
- In control mode, sense the SYN, SYN, @, @, ENQ sequence. This sequence puts the adapter in addressed mode.
- In addressed mode, store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Post IOB complete when:
  - An ENQ character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for the transmit portion of a transmit/receive initial operation are to:

- Activate the 'request to send' line, and generate a microinterrupt when the 'clear to send' line goes active.
- Transmit data bytes bit-by-bit (serialize).
- Generate character microinterrupts when another byte of data is to be sent to the attachment.
- Signal the program when the time interval loaded into the timer is complete.
- Sense transmit adapter checks.

The hardware objectives for the receive portion of a transmit/receive initial operation are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Sense the first of 2 SYN characters. (The second SYN character is sensed by control storage.)
- Generate character microinterrupts when a byte of data is to be sent to main storage.
- Sense overrun conditions.

BSC Transmit/Receive

The Q-code for a BSC transmit/receive operation is hex 86.

Control Storage Program Objectives

The control storage program objectives for the transmit portion of a transmit/receive operation are to:

- Activate the 'request to send' line to the attachment, and enable the hardware to interrupt when the 'clear to send' line from the modem goes active.
- Encode BSC characters (SYNs, PAD characters, and BCC only).
- Send data characters from the main storage buffer to the BSC attachment buffer.
- Enable hardware to interrupt when another character is to be sent to the attachment.
- Load the time-out clock for a 1-second interval (half second for the internal clock and half rate). The control storage program uses the time-out clock to determine when to insert 2 SYN characters in the data message.
- Analyze each character to:
  - Set or reset data mode.
  - Enter or exit transparency mode.
  - Sense turnaround sequences.
- Accumulate the block check character (BCC) and store it in the BCC buffer. Send the BCC character when end of transmit is sensed.
- Sense end-of-transmit operations. If the transmit buffer length is 0 and the receive buffer length is not 0, the adapter starts to receive data. The receive buffer follows, and is contiguous to, the transmit buffer. If the transmit and receive buffer lengths are both 0, the operation ends and the IOB is posted complete.

The control storage program objectives for the receive portion of a transmit/receive operation are to:

- Set up hardware and enable microinterrupts to indicate when byte time is complete. Byte time is complete when character phase is complete (2 SYNs have been sensed) and a character has been received. Byte time occurs for each character received.
- Set up hardware to enable microinterrupts after a 3.25-second interval.
- Analyze each character to:
  - Set or reset data mode.
  - Enter transparency mode. To enter transparency mode, receive DLE, STX sequence; to exit transparency mode, receive DLE ENQ, DLE ETX, DLE ETB, or DLE ITB.
  - Sense change-of-direction character sequences.
- Store the data (including the second address byte) in main storage per the buffer address. The data is from the attachment buffer.
- Decrease the receive buffer length.
- Check when the receive buffer length is 0.
- Accumulate block check character (BCC) bytes.
- Compare the accumulated BCC with the received BCC.
- Post IOB complete when:
  - A change-of-direction character is sensed.
  - A 3.25-second time-out microinterrupt occurs.
  - The receive buffer length is 0.

Hardware Objectives

The hardware objectives for the transmit portion of a transmit/receive operation are to:

- Activate the 'request to send' line, and generate a microinterrupt when the 'clear to send' line goes active.
- Transmit data bytes bit-by-bit (serialize).
- Generate character microinterrupts when another byte of data is to be sent to the attachment.
- Signal the program when the time interval loaded into the timer is complete.
- Sense transmit adapter checks.

The hardware objectives for the receive portion of a transmit/receive operation are to:

- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Generate character microinterrupts when a byte of data is deserialized.
- Sense receive adapter checks.
- Sense the 3.25-second time-out and generate the time-out microinterrupt.

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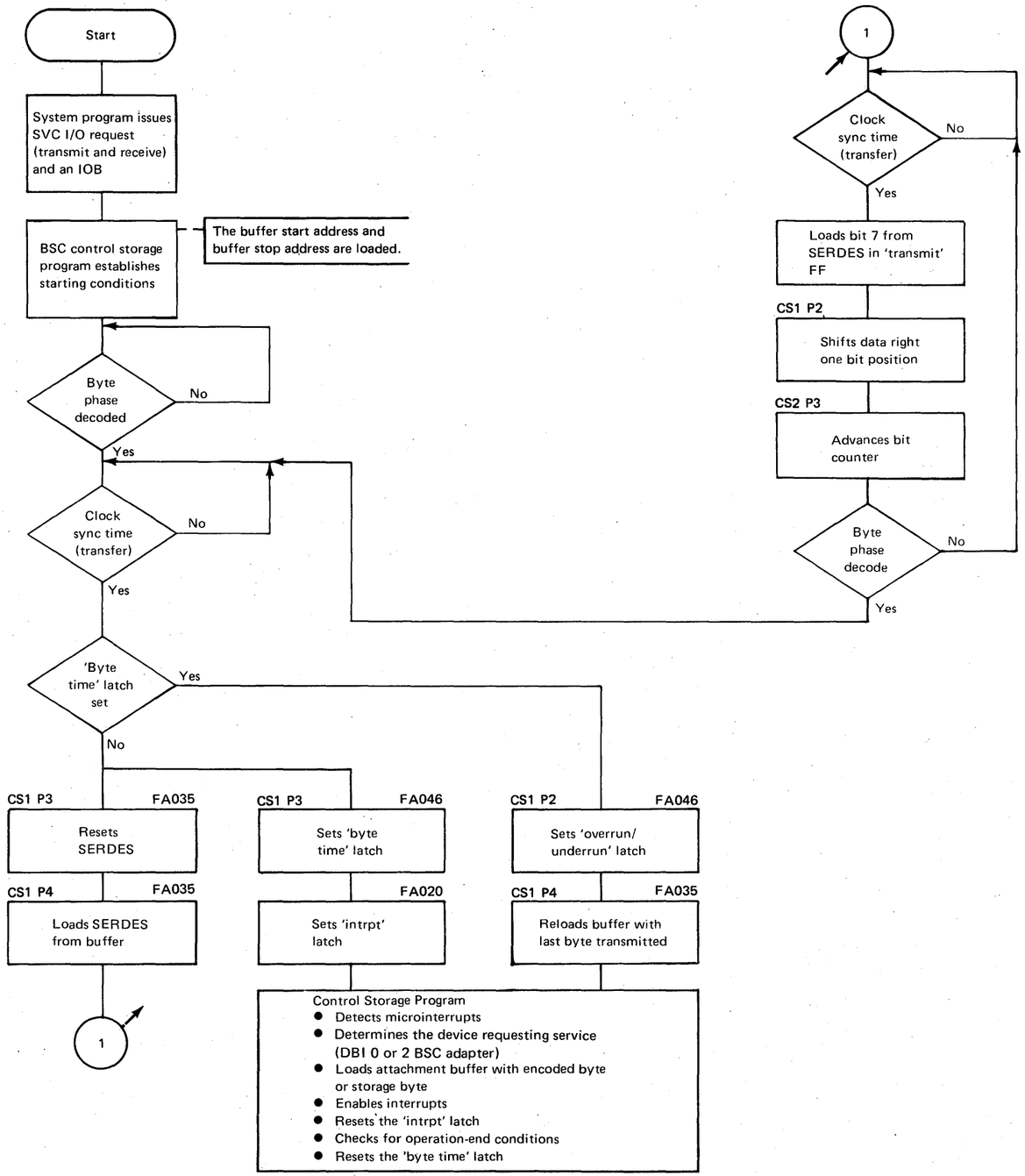
BSC Transmit Flowchart



BSC Transparent Operations

Transparent text mode operation permits any data link line control character to be transmitted and received as data. To place the BSC adapter in transparent mode, a DLE character followed by an STX character must be transmitted at the start of the message. The receive station, in turn, recognizes this sequence and also enters transparent mode.

After both stations have entered transparent mode, all characters can be transmitted as data. When a control character is needed, a DLE character followed by a data link line control character indicates a valid data link line control character. When a control character is to be sent, the control storage program inserts a DLE character before the control character. If DLE is to be sent as a data character, the control storage program inserts a DLE character before the DLE is taken from storage. After recognizing the DLE character, the receiving station checks the next character to determine what action is to be taken. This station recognizes the DLE DLE sequence. The first DLE character is ignored; the second DLE character received is stored as data.

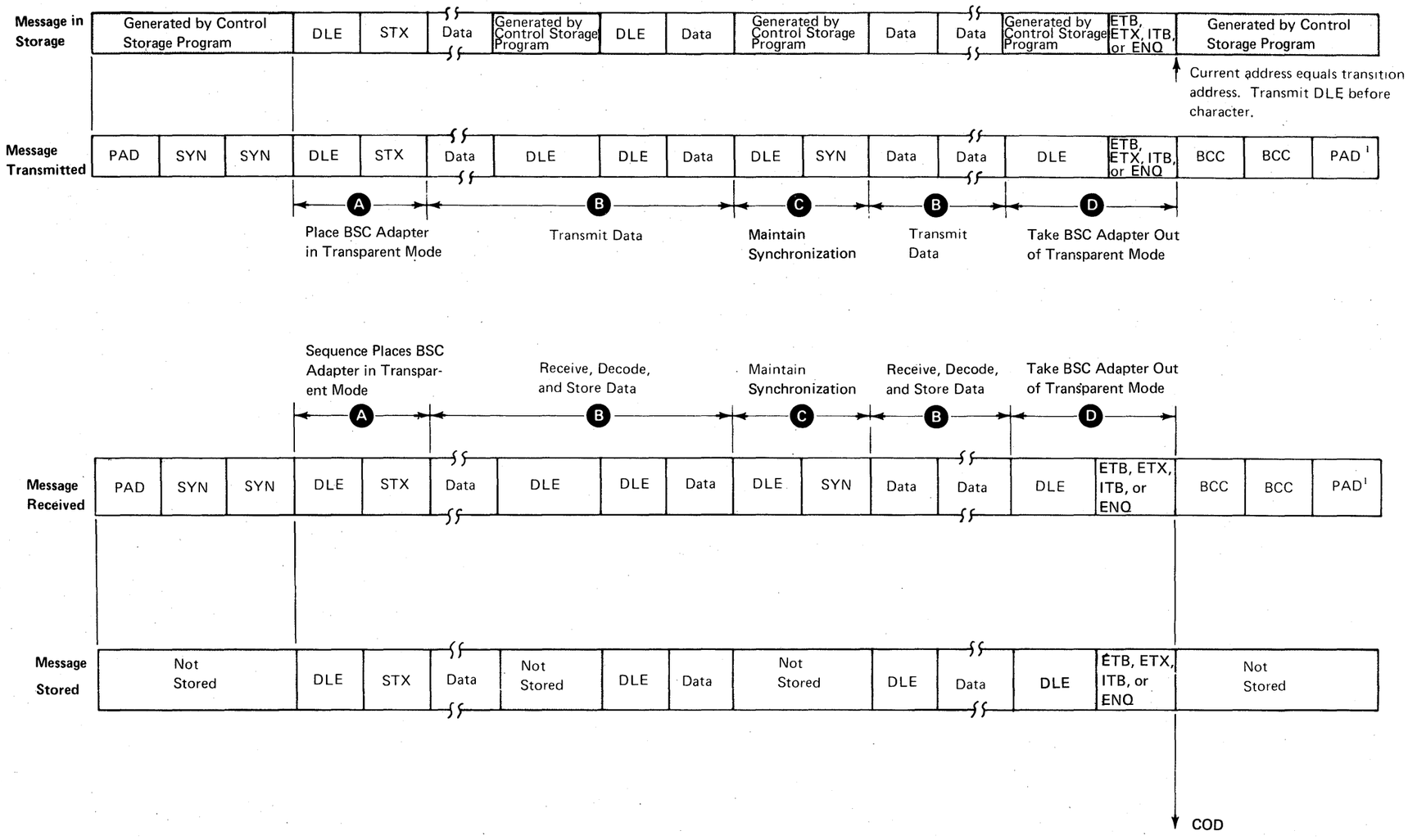
The line control characters that are identified by an alphabetic character in the figure are described in the following paragraphs.

DLE STX (A): Places the transmit and receive stations in transparent mode.

Data (B): All bytes are identified as data. For example, an extra DLE character is inserted by the control storage program after a DLE character to indicate that the inserted DLE character is data. At the receive station, the first DLE character is ignored. The second DLE character is stored as data.

DLE SYN (C): This sequence is sent at 1-second intervals to maintain character synchronization at the receiving station.

DLE followed by an ETB, ETX, ITB, or ENQ (D): DLE followed by a data link line control character indicates that the receiving station must take action as instructed by the data link line control character received.



[1] No PAD character received after an ITB.

BSC Multipoint Operations

A multipoint network has a primary station and several permanently connected secondary stations. A secondary station must be polled or addressed by the primary station before the secondary station can transmit or receive data.

At the start of a multipoint call (receive initial), the BSC adapter enters monitor mode where it monitors the first control characters. EOT resets monitor mode and starts address sensing. SOH or STX resets control mode and sets data mode. This action also resets the BCC buffer and starts BCC accumulation.

ETB or ETX resets data mode and is the last character included in BCC accumulation.

When in transmit mode, the adapter takes characters from storage and transmits them on the line. BCC accumulation, data mode, and transparent mode are set by the type of control characters taken from storage. Transmission continues until the transmit buffer length is equal to 0, which places the adapter in receive mode.

When in receive mode, the BSC adapter establishes synchronization and then sends the received characters to storage. As in transmit mode, the function of receive mode relies on the specific line control characters received.

If the secondary station is polled, it responds with its station address and with one of the following:

- EOT sequence: No data is to be transmitted by the secondary station (negative response).
- Data: Sends data to the control station (positive response).
- No response: The polled station is not online or did not receive or recognize the poll.

If the secondary station is addressed, it responds with its station address and with one of the following:

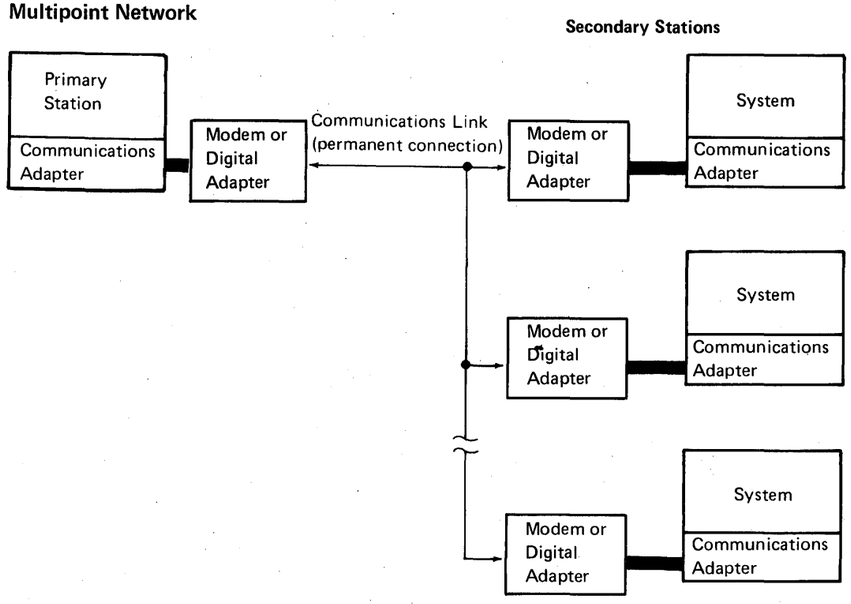
- ACK: Indicates that the secondary station is ready to receive data (positive response).
- NAK: Indicates that the secondary station is not ready to receive data (negative response).
- WACK: Indicates that the primary station should wait before sending data to the secondary station.

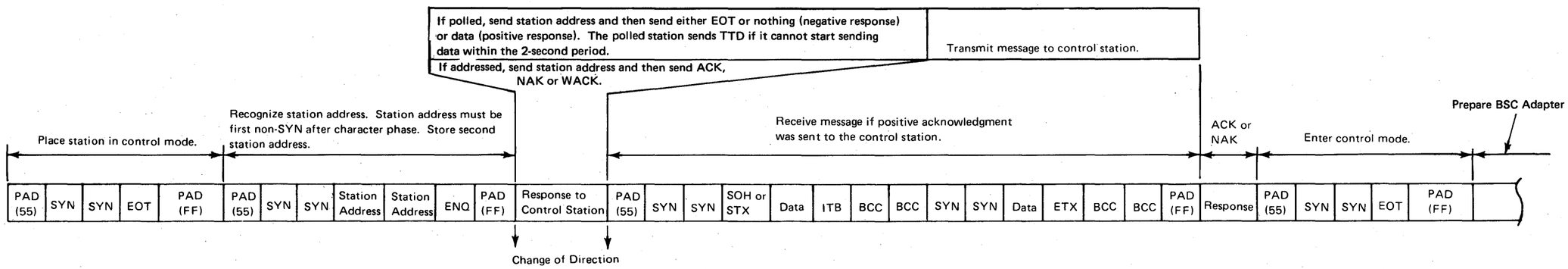
Communication between any two secondary stations must be through the primary station.

The BSC adapter is prepared for polling or selection by:

- Enabling the BSC adapter.
- Issuing a supervisor call I/O request (receive-initial) instruction and then waiting to be addressed or polled. (The secondary station address is found in the IOB.)

Multipoint Network





SDLC Transmit Operations

A supervisor call input/output request instruction (for transmit) and an associated IOB set the SDLC adapter to transmit mode. The adapter takes data from storage (during a level 2 character microinterrupt) and transmits the data on the communications line. Transmission of data continues until the transmit buffer length is equal to 0.

During transmit operations:

- Data is serialized and transmitted bit-by-bit.
- Frame checking information is accumulated and sent preceding the ending flag.
- Zero insertion/deletion inserts a binary 0-bit into the data stream after five consecutive 1-bits have been transmitted.
- NRZI changes the state of the data when transmitting a 0-bit. (This is optional and depends on the type of modem.)

The four transmit instructions are:

- Transmit/Receive: Causes the communications adapter to perform a transmit operation and dequeues the IOB from the start of the line queue (should be a receive IOB at the start of the line queue).
- Transmit Initial (primary only): The adapter waits for the 'data set ready' line and then proceeds as a transmit/receive operation. Transmit initial also generates a 3-second answer tone for World Trade switched line if it is needed.
- Transmit Final: Is used for sending the last frame of a message before disabling the adapter.
- Transmit Only: Is used for sending consecutive frames without any receive operations between frames. When the transmit operation ends, the adapter continues to hold the communications line active by sending continuous flags; flags are sent until a new transmit operation is started.

The IOB is posted complete at the end of a transmit operation, or when a transmit adapter check occurs.

Control Storage Program Objectives

The control storage program objectives for an SDLC transmit operation are to:

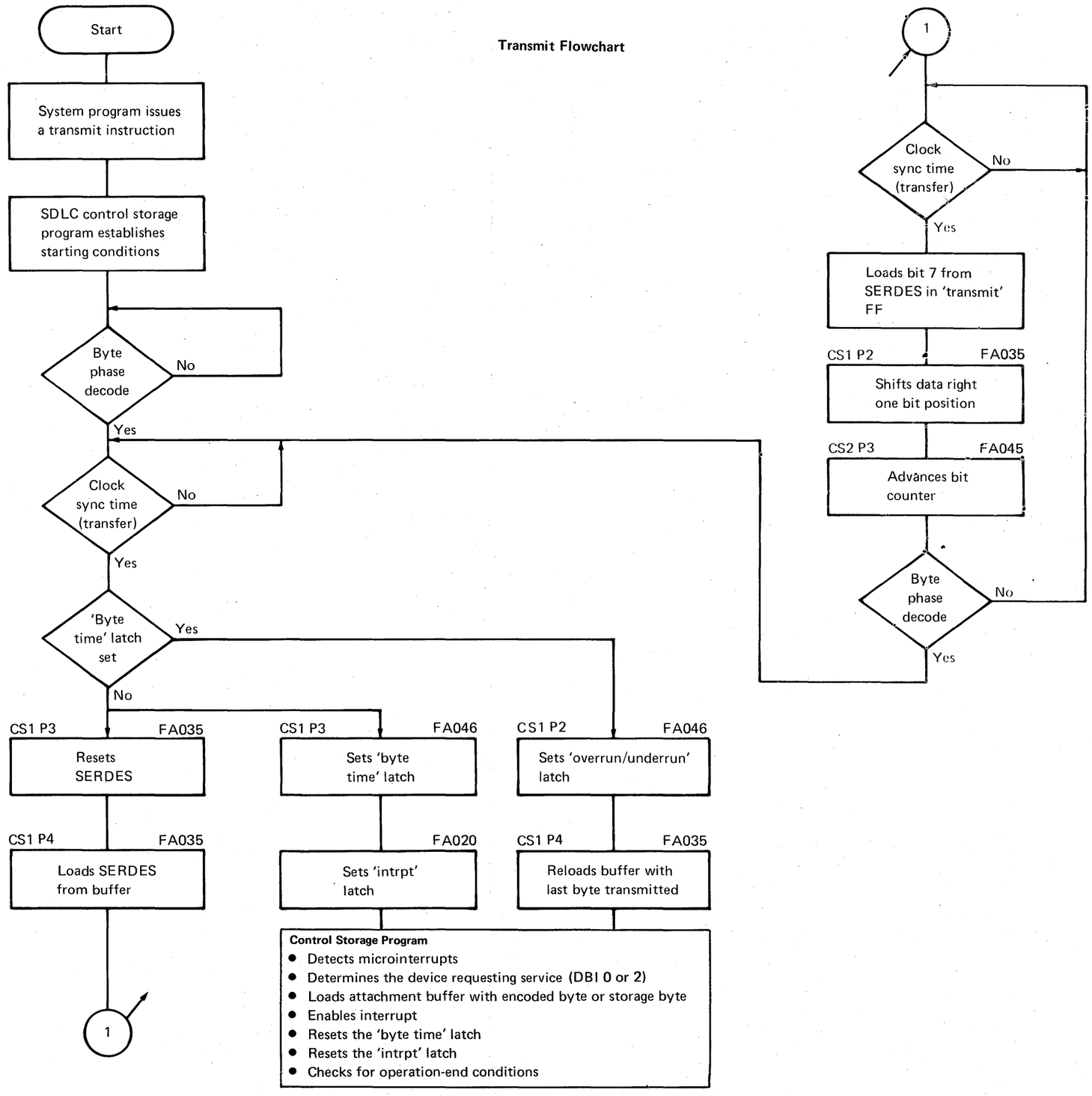
- Encode flags.
- Insert the station address. The station address is taken from the IOB.
- Transfer data from storage to the SDLC adapter.
- Decrease the transmit buffer length by 1 byte for every byte transmitted.
- Enable hardware to interrupt when another byte of information is to be sent to the adapter.
- Accumulate frame checking information.
- Sense an end-of-transmit operation when the transmit buffer length is equal to 0, and send the frame check character and ending flag. Then, depending on the type of operation, the following occurs:
  - For a transmit/receive, the IOB is posted complete and queue processing starts from the start of the line queue.
  - For a transmit only, the IOB is posted complete and flags are sent until another supervisor call I/O request instruction is issued.
  - For a transmit final, the IOB is posted complete.

Hardware Objectives

The hardware objectives for an SDLC transmit operation are to:

- Transmit data bit-by-bit (serialize).
- Generate character microinterrupts when another byte of data is to be sent to the attachment.
- Signal the control storage program when a specified time interval is completed (inactivity timer for a switched line).
- Sense character overrun conditions.
- Insert a 0-bit into the data stream after five consecutive 1-bits.
- If NRZI is installed, change the state of the data when transmitting a 0-bit.

Transmit Flowchart



SDLC Receive Operations

The receive operations for SDLC are receive only, receive delayed, and receive initial. The operations are similar except for the processing of the IOB that is put on the communications queue. For a receive-only operation, the processing starts with the first entry on the queue. The processing is delayed for the receive-delayed operation, and the processing starts with the receive-initial IOB for the receive-initial operation. Also, for the receive-initial operation, the inactivity timer is not started until the 'data set ready' line is active. During a receive operation, data is placed into the receive buffer in main storage (the receive buffer is prepared before the receive instruction is issued). Line queue processing stops when a poll/final bit is received or when the queue is empty.

During receive operations:

- Data is received bit-by-bit and deserialized.
- Incoming data is analyzed for a flag sequence.
- The first nonflag bit sequence following a flag is analyzed for a correct station address. The station address is not passed to main storage, but the control and information fields are passed to main storage.
- The zero insertion/deletion function removes a binary 0-bit from the data stream after five consecutive 1-bits have been received.
- Frame checking information is accumulated and compared with the received frame checking information.

When the receive operation ends, the IOB is posted complete and the status bytes in the IOB can be checked for status.

Control Storage Program Objectives

The control storage program objectives for an SDLC receive operation are to:

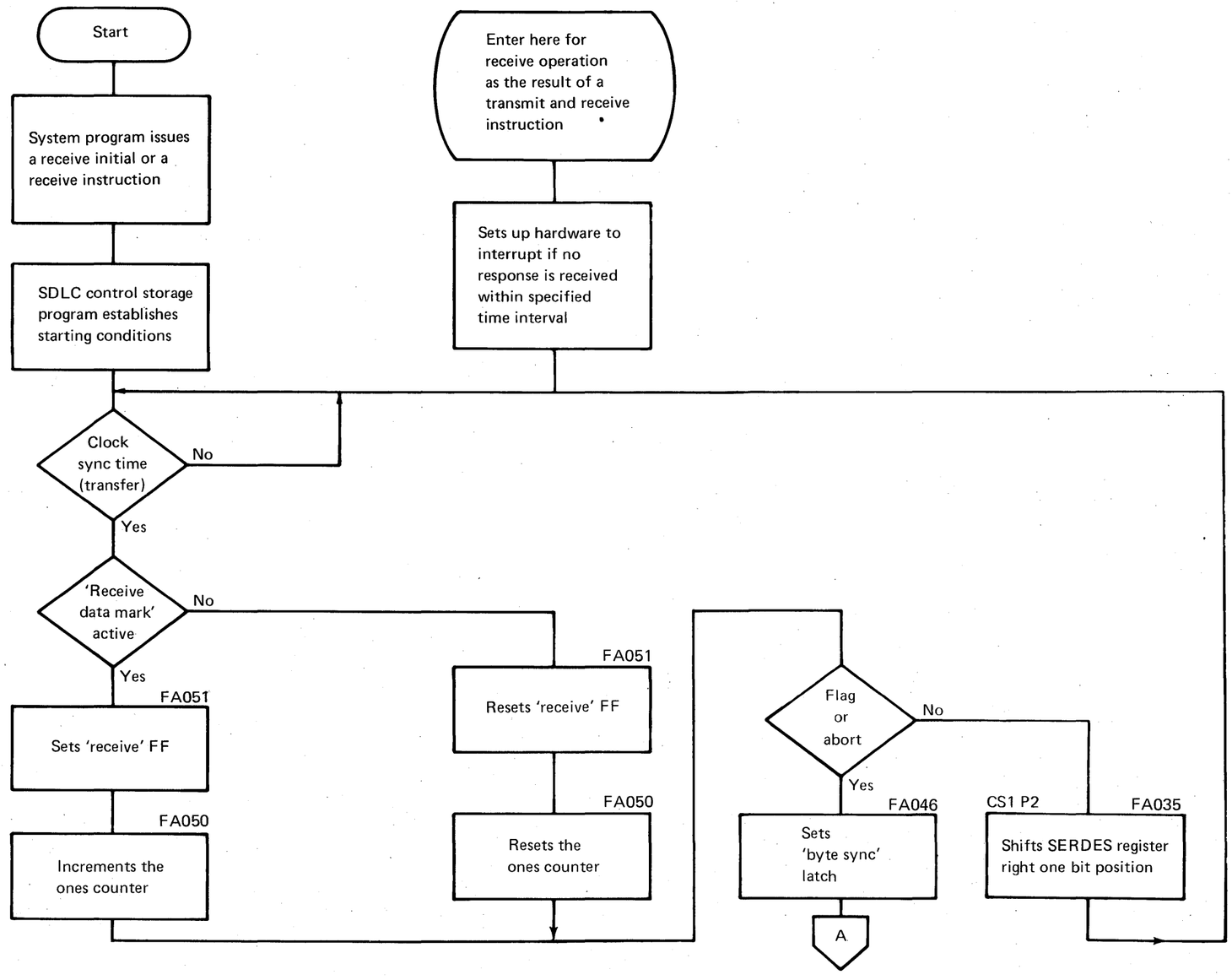
- For receive initial (on a switched network), set up the hardware to sense the 'data set ready' line and enable data set ready interrupts. Also, generate a 3-second answer tone needed by World Trade on a switched network.
- Start the inactivity timer (started twice at 16 seconds each).
- Set up hardware and enable interrupts to indicate when character sync is set (when a flag sequence is sensed).
- Transfer data from the adapter buffer to main storage.
- Store data in main storage per the buffer address.
- Decrease the receive buffer length by 1 byte for every byte received.
- Accumulate frame checking information and compare it with the received frame checking information.
- Generate a system interrupt when:
  - An ending flag is sensed.
  - An invalid frame is sensed.
  - When one of the following error conditions occurs:
    a. CRC error.
    b. Adapter check on a receive operation or on a transmit operation.
    c. Inactivity time-out.
    d. Data set ready drops (abortive disconnect for a switched line).

Hardware Objectives

The hardware objectives for an SDLC receive operation are to:

- Sense the 'data set ready' line and generate a data set ready interrupt (for receive-initial operation on a switched network).
- Establish character sync by sensing a flag sequence.
- Receive data bit-by-bit and assemble these bits into data bytes (deserialize).
- Generate a character microinterrupt when a byte of data is to be sent to main storage.
- Sense overrun, abort, and invalid sequence (seven consecutive 1-bits).
- Sense time-out condition and generate a time-out interrupt.
- Remove 0-bits from the data stream after five consecutive 1-bits have been received (zero insertion/deletion).

Receive Flowchart (Part 1 of 2)



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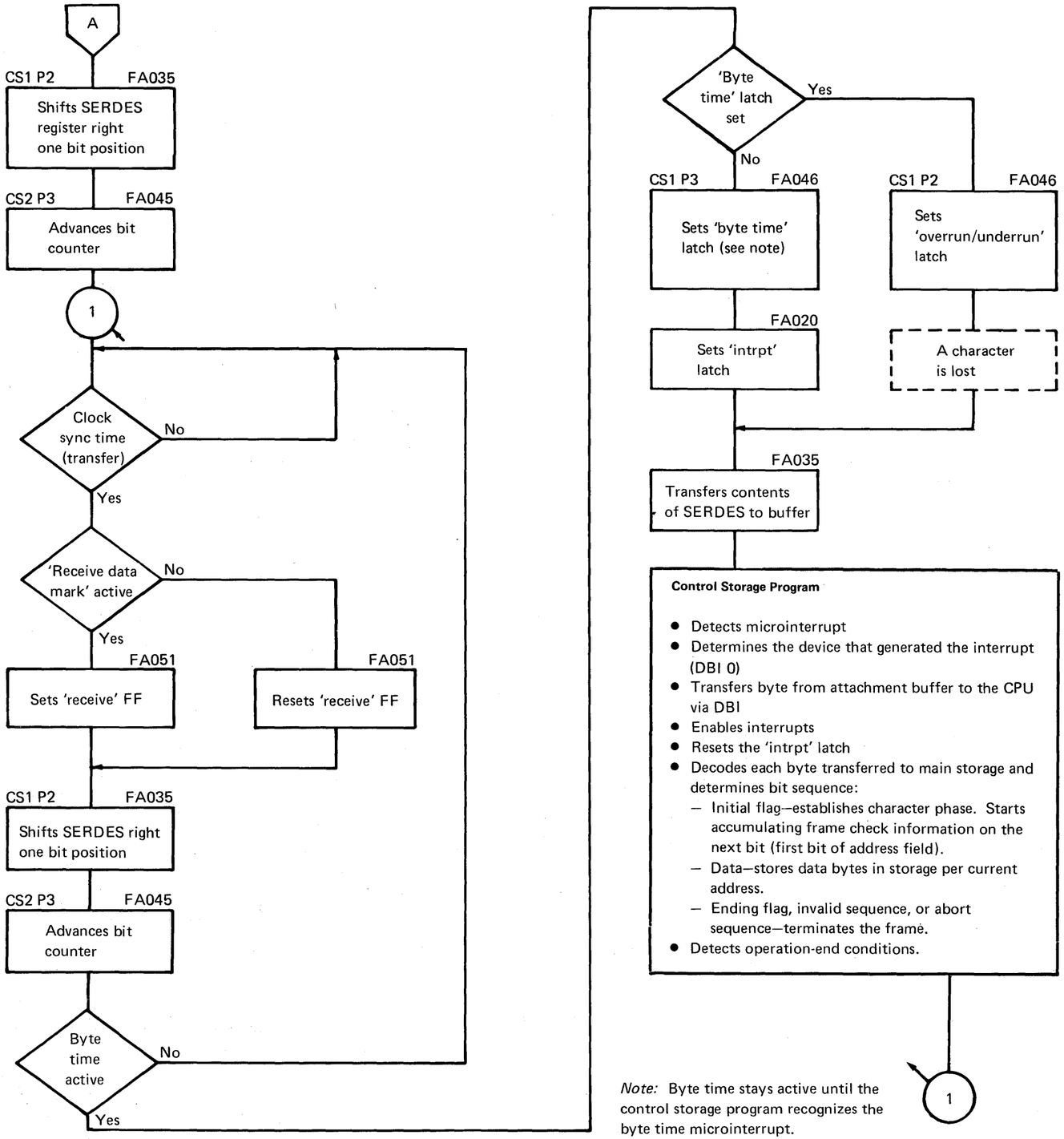
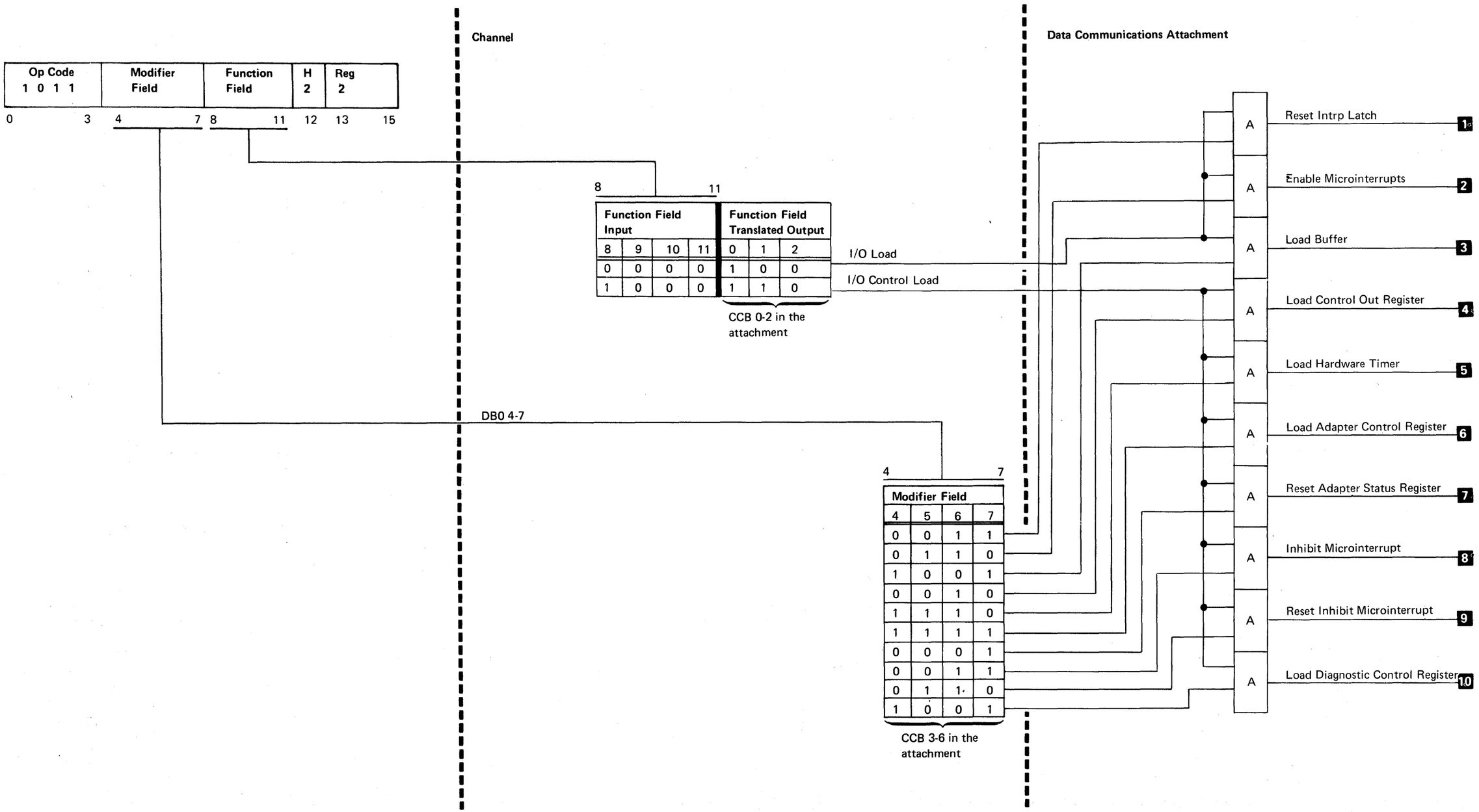
Receive Flowchart (Part 2)

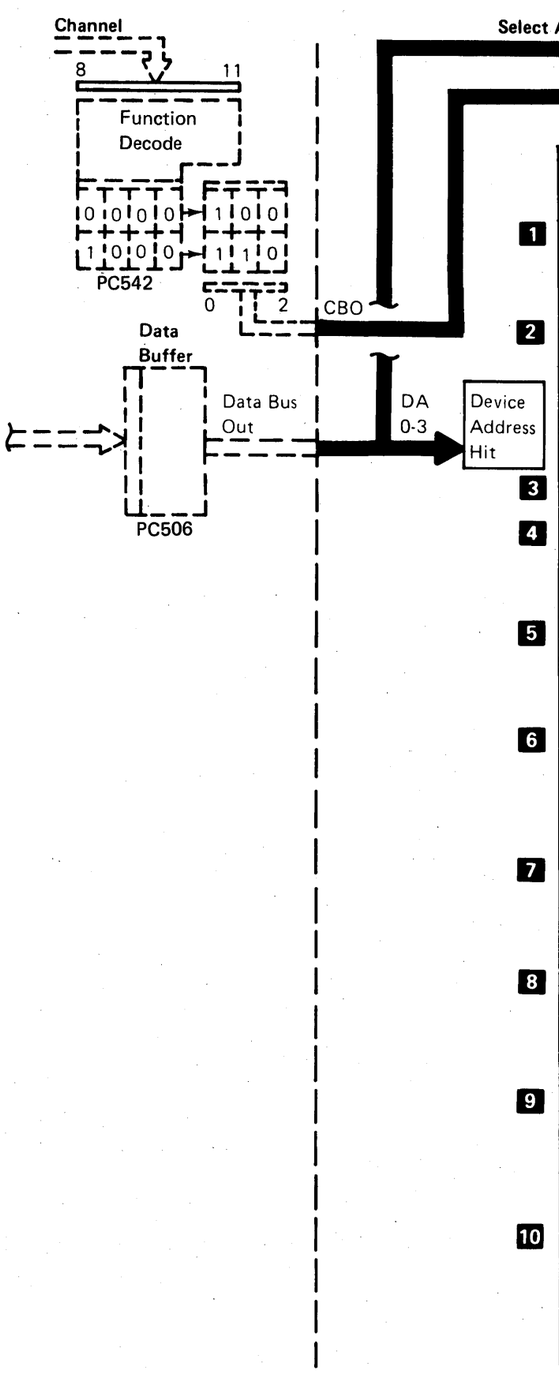


Note: Byte time stays active until the control storage program recognizes the byte time microinterrupt.

Commands

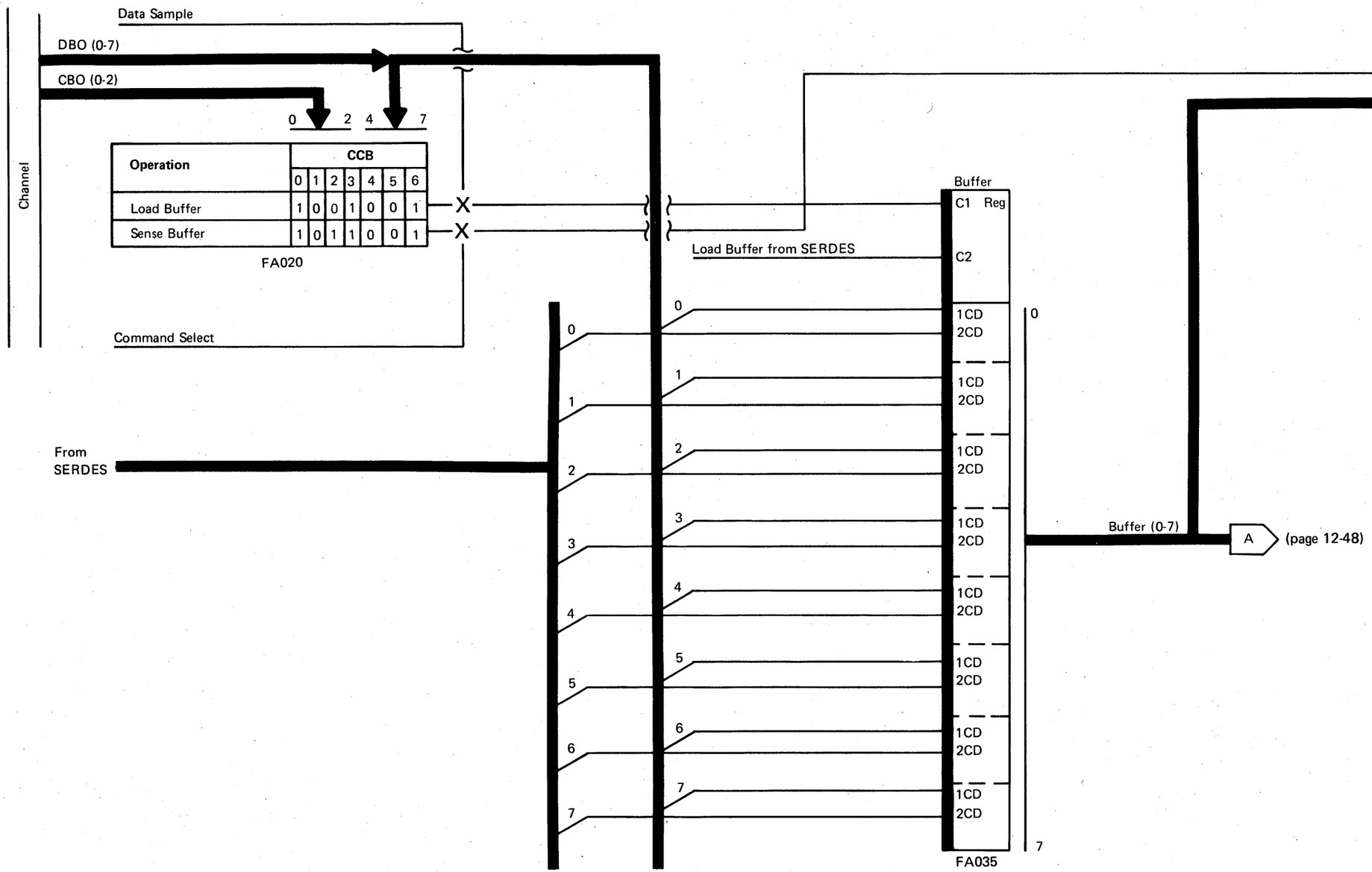
I/O Load Command–I/O Control Load Command



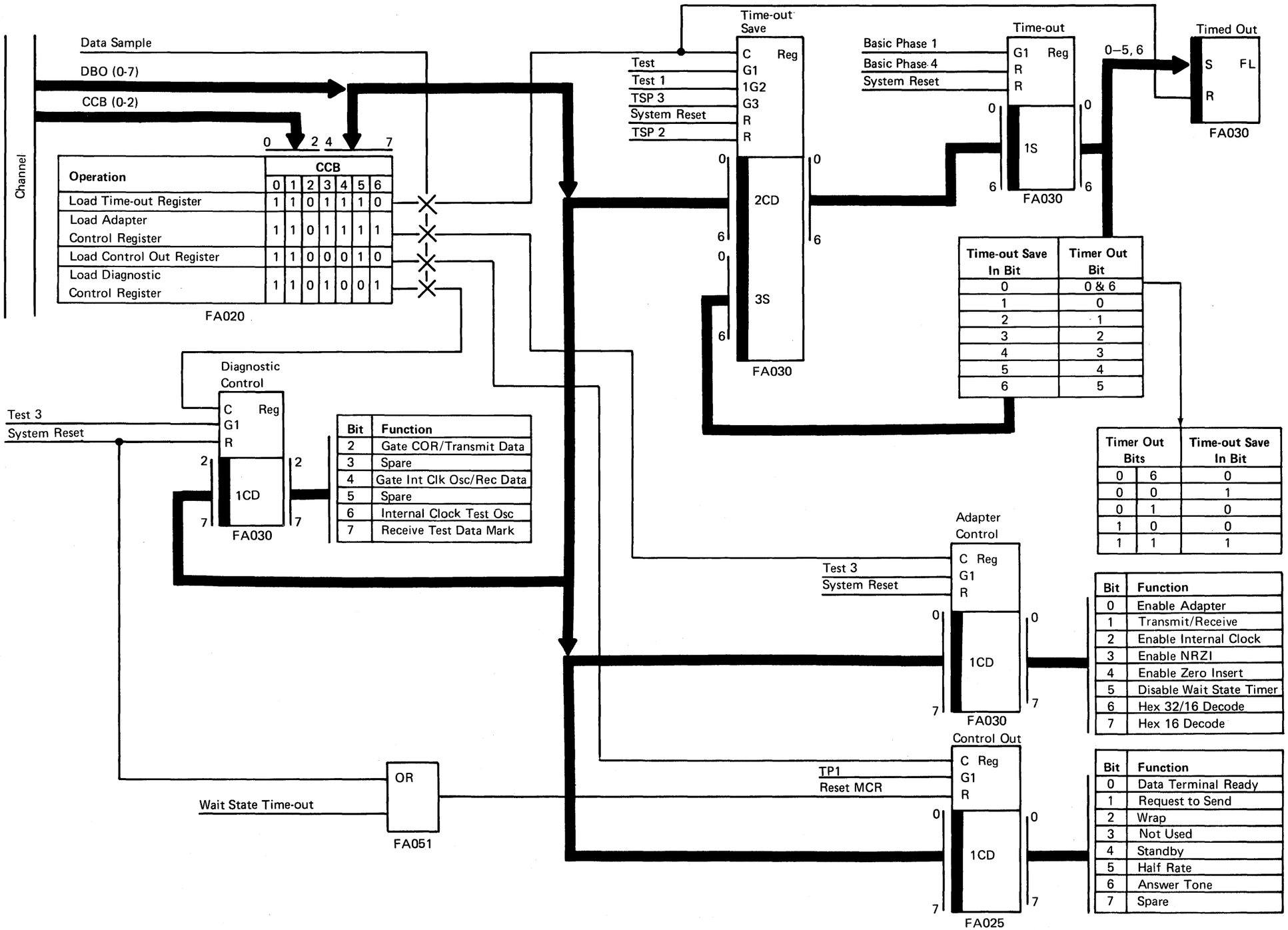


	CCB 0 1 2	CCB 3 4 5 6	Data Bus Out Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	1 0 0	0 0 1 1 Reset Intrp Latch	Reset Microinterrupts							
2	1 0 0	0 1 1 0 Enable Micro-interrupts	Data Set Ready	Clear to Send	Test Indicator	Ring Indicator	Byte Time	Invalid Sequence or Abort	Flag/SYN Detect	Timed Out
3	1 0 0	1 0 0 1 Load Buffer	DBO 0 to Buffer 0	DBO 1 to Buffer 1	DBO 2 to Buffer 2	DBO 3 to Buffer 3	DBO 4 to Buffer 4	DBO 5 to Buffer 5	DBO 6 to Buffer 6	DBO 7 to Buffer 7
4	1 1 0	0 0 1 0 Load Control Out Register	Data Terminal Ready	Request to Send	Wrap		Standby	Half Rate	Answer Tone	Adapter enabled (microcode flag)
5	1 1 0	1 1 1 0 Load Hardware Timer	Time-out Clock 0	Time-out Clock 1	Time-out Clock 2	Time-out Clock 3	Time-out Clock 4	Time-out Clock 5	Time-out Clock 6	0 = 1 ms 1 = 131 ms
6	1 1 0	1 1 1 1 Load Adapter Control Register	Enable Adapter	Transmit/Receive Operation	Enable Internal Clock	Enable NRZI	Enable Zero Insert	Disable Wait State Timer	SYN Decode	EBCDIC = 0 ASCII = 1
7	1 1 0	0 0 0 1 Reset Adapter Status Register	Adapter Check	Byte Sync	Abort		Byte Time	Invalid Sequence	Flag/SYN Detect	
8	1 1 0	0 0 1 1 Inhibit Micro-interrupt	Microinterrupts are inhibited but left pending							
9	1 1 0	0 1 1 0 Reset Inhibit Micro-interrupt	Inhibit microinterrupt is also reset by system reset							
10	1 1 0	1 0 0 1 Load Diagnostic Control Register			Gate Control Out Register and Transmit Data		Gate Internal Clock Osc and Receive Data		Internal Clock Test Oscillator	Receive Test Data

Load/Sense Buffer



Load Time-out Clock and Registers



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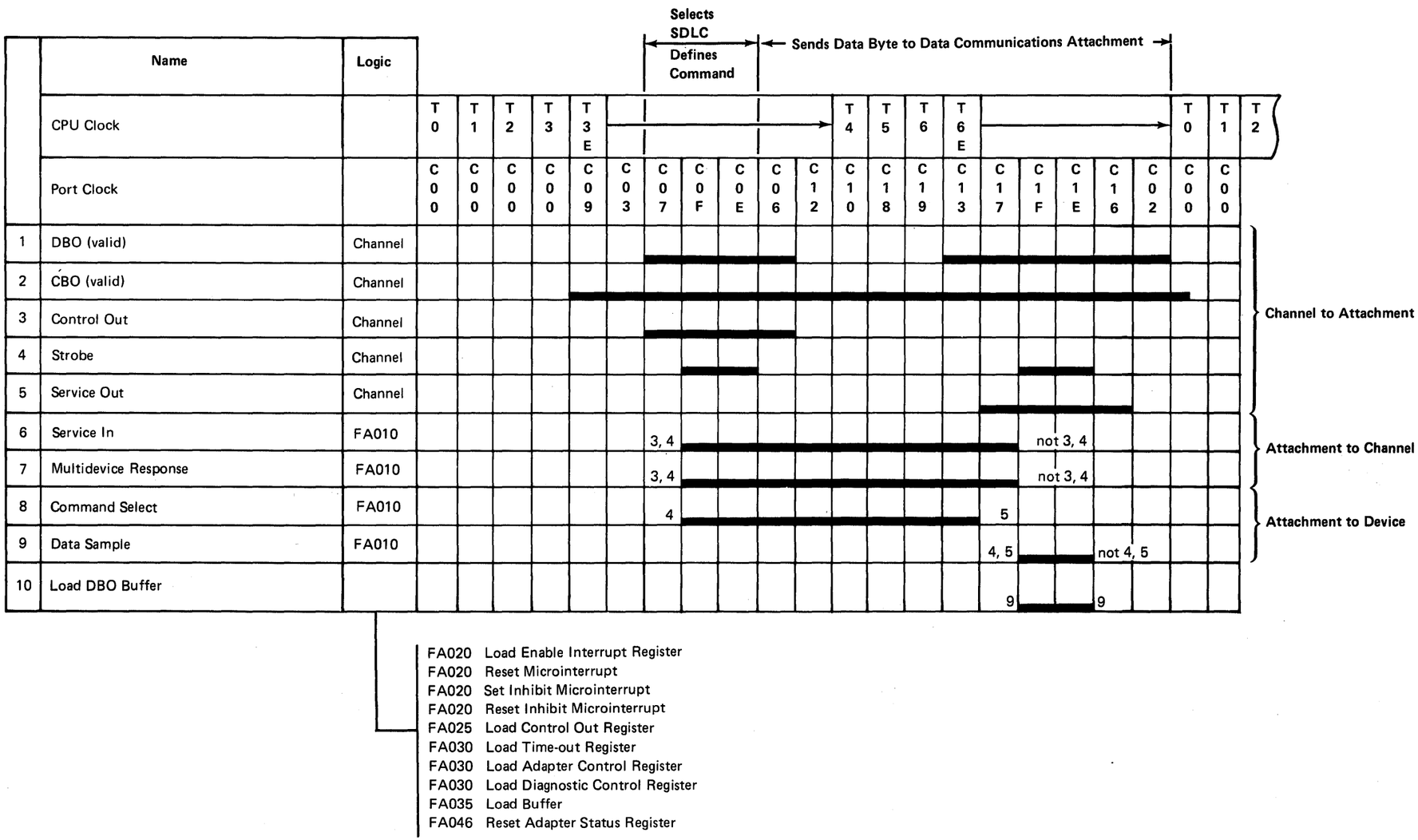
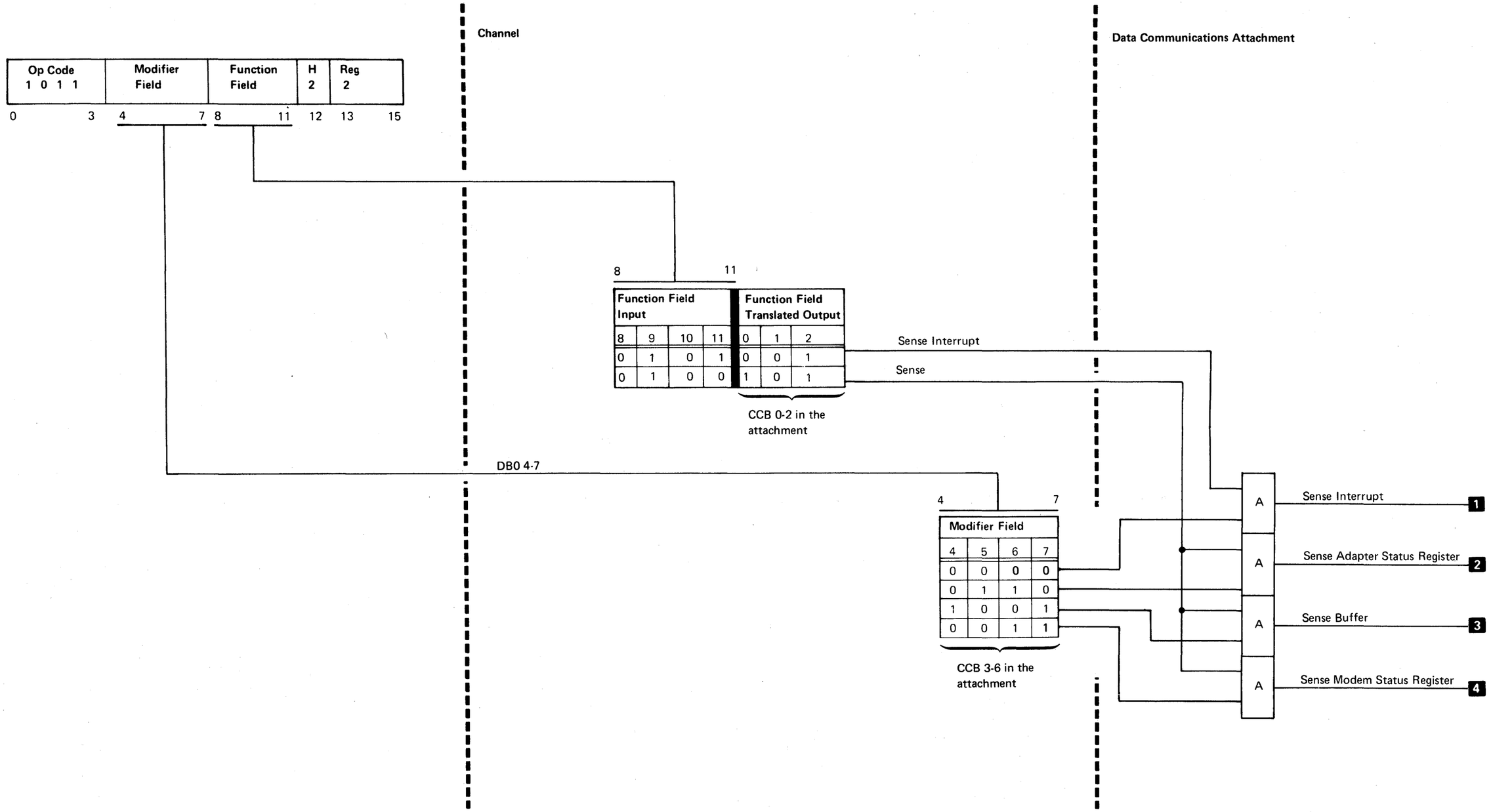
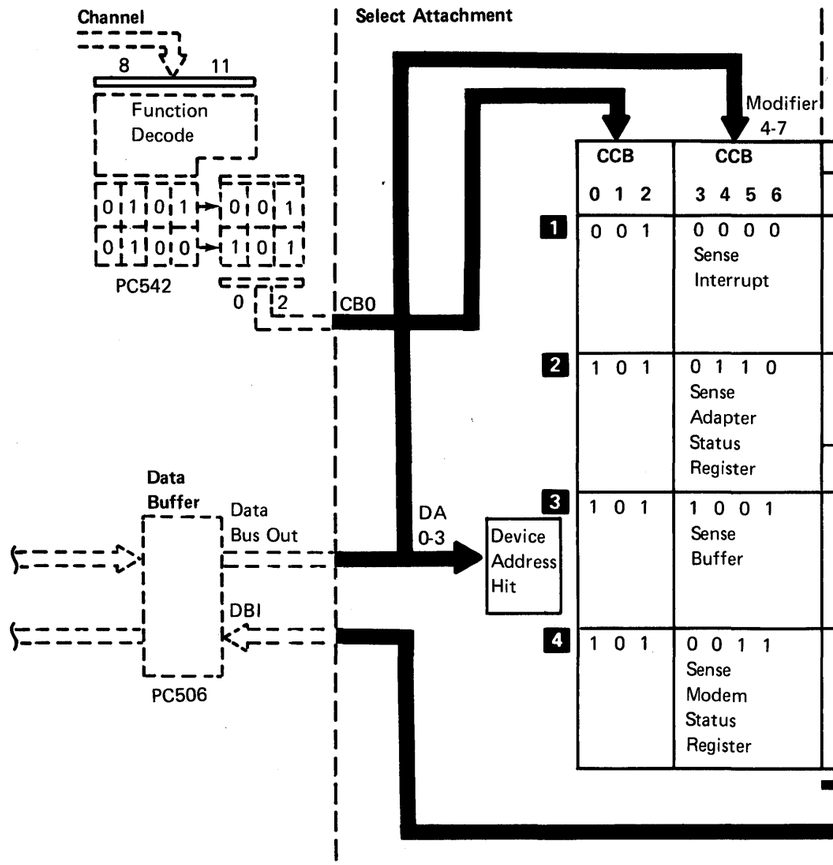
Load Timing Chart



FA020 Load Enable Interrupt Register
FA020 Reset Microinterrupt
FA020 Set Inhibit Microinterrupt
FA020 Reset Inhibit Microinterrupt
FA025 Load Control Out Register
FA030 Load Time-out Register
FA030 Load Adapter Control Register
FA030 Load Diagnostic Control Register
FA035 Load Buffer
FA046 Reset Adapter Status Register

I/O Sense Command

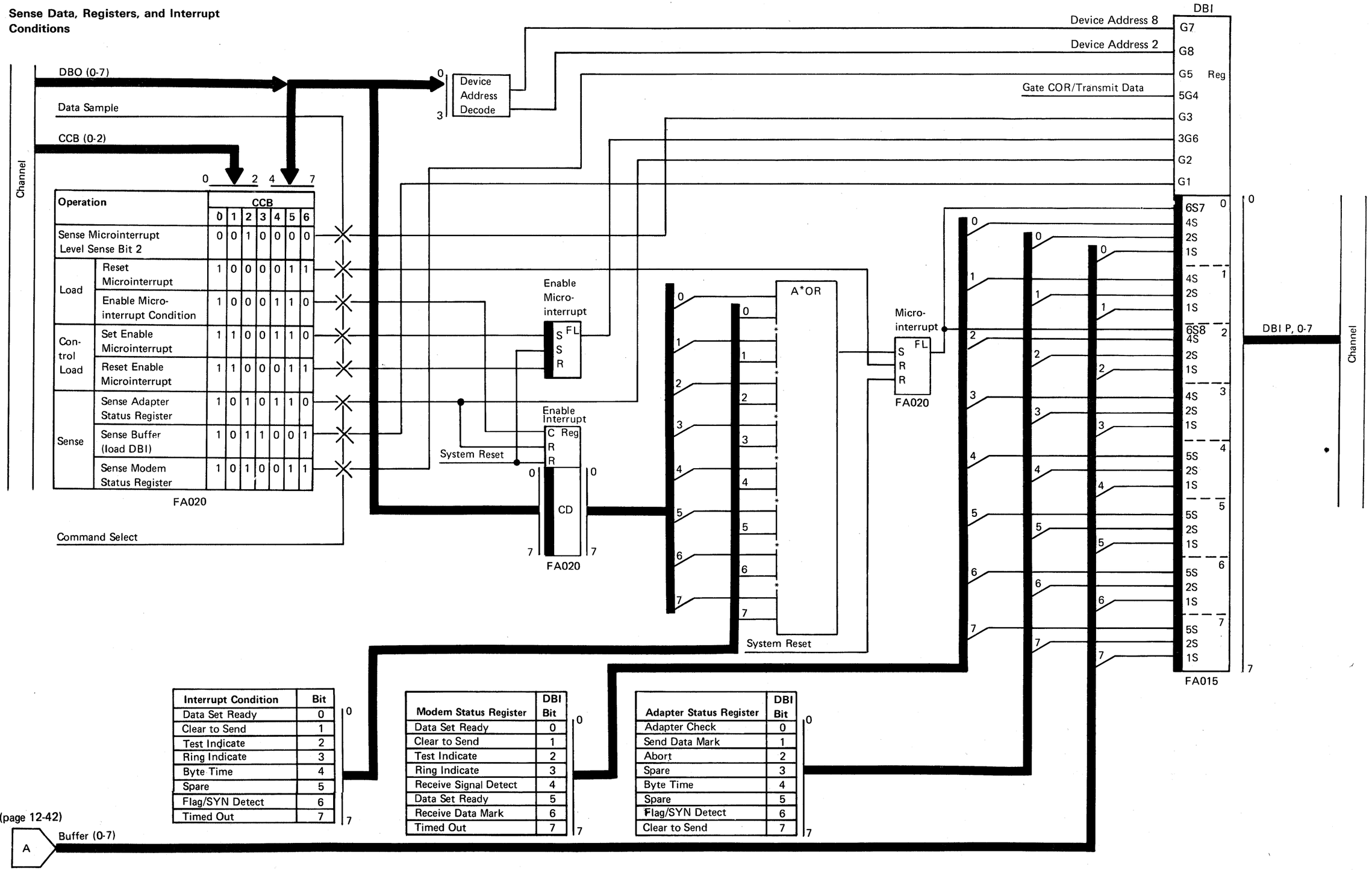




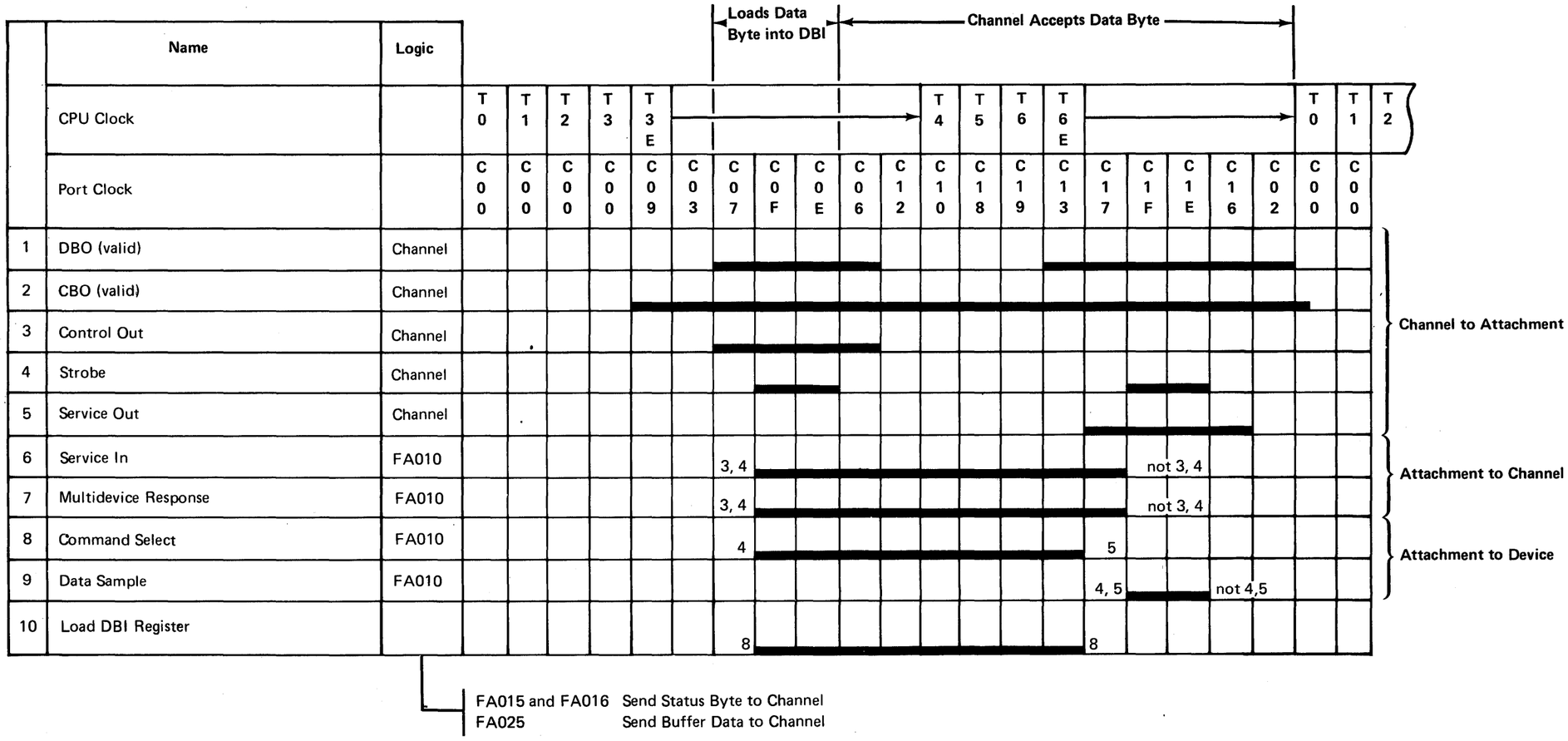
Send Data Byte to Channel

	CCB 0 1 2	CCB 3 4 5 6	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1	0 0 1	0 0 0 0 Sense Interrupt			Interrupt (interrupt level 2)					
2	1 0 1	0 1 1 0 Sense Adapter Status Register	Adapter Check	Transmit Data Mark	Abort	Data Set Ready (ungated)	Byte Time	Invalid Sequence	Flag/SYN Detect	Clear to Send (ungated)
			Resets Enable Interrupt Register							
3	1 0 1	1 0 0 1 Sense Buffer	Buffer 0 to DBI 0	Buffer 1 to DBI 1	Buffer 2 to DBI 2	Buffer 3 to DBI 3	Buffer 4 to DBI 4	Buffer 5 to DBI 5	Buffer 6 to DBI 6	Buffer 7 to DBI 7
4	1 0 1	0 0 1 1 Sense Modem Status Register	Data Set Ready	Clear to Send	Test Indicate	Ring Indicate	Carrier Detect	Receive timing	Receive Data Mark	Timed Out

Sense Data, Registers, and Interrupt Conditions



Sense Data Timing Chart



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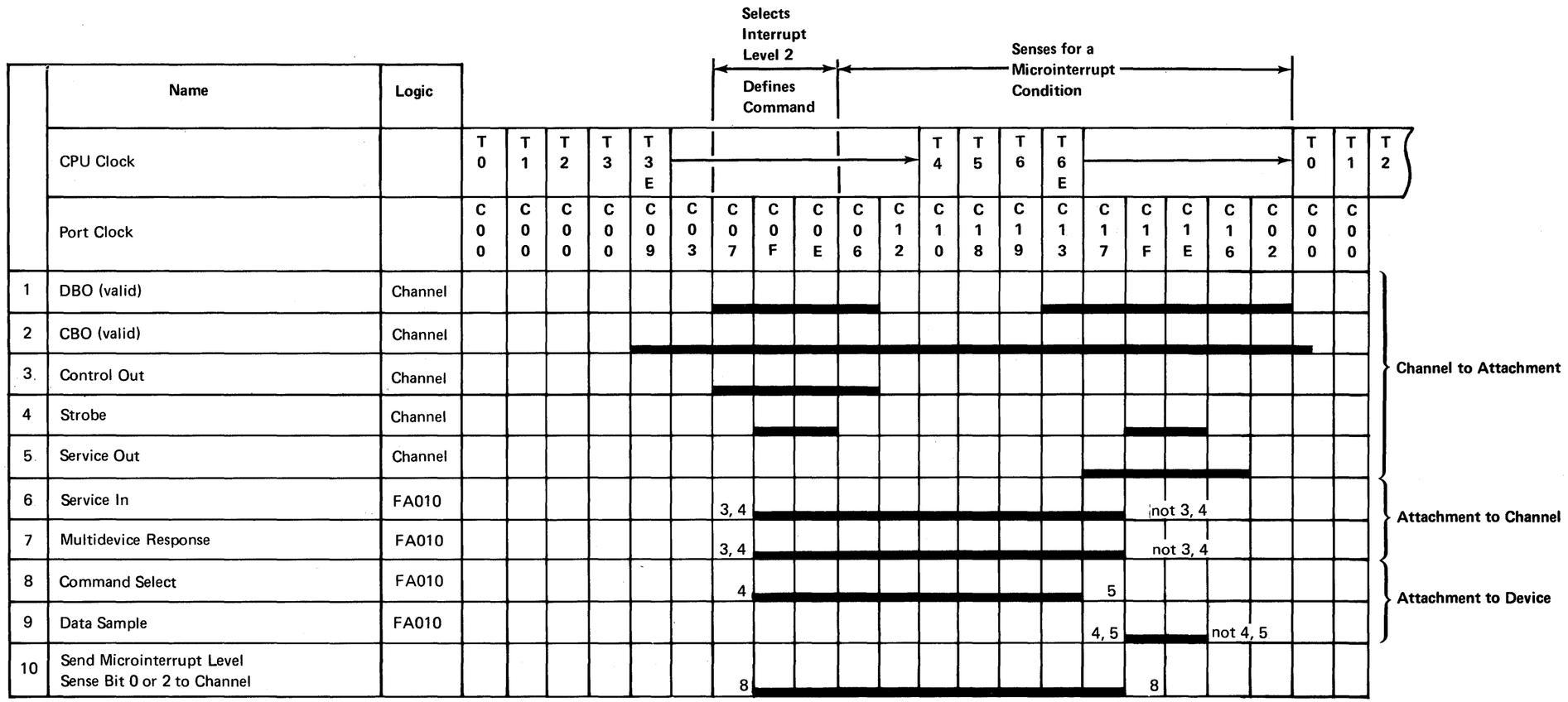
Sense Microinterrupt Level Timing Chart



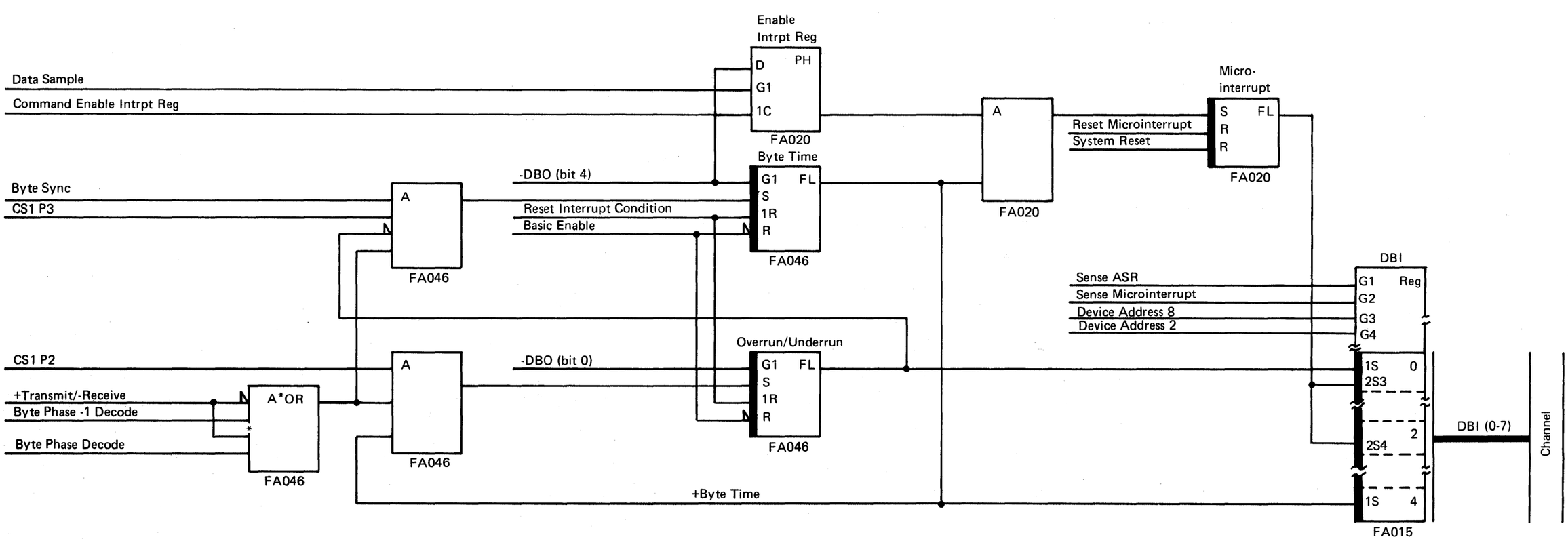
Error Conditions

Adapter Check

An adapter check is generated if a byte-time interrupt is generated while another byte-time interrupt is pending.

On a transmit operation, an adapter check occurs if it is time to transmit a character but no character has been loaded into the transmit buffer. During transmit operations, a byte-time microinterrupt is generated at byte time. At this time, data is also sent from the adapter buffer to the SERDES register. If the 'byte time' latch is not reset before the data is sent to the SERDES register, a byte-time microinterrupt is pending. Also, if the preceding microinterrupt has not been processed, the buffer is empty when the second byte-time microinterrupt is generated. Therefore, a transmit adapter check occurs, the adapter stops transmitting information, and error recovery becomes necessary. To recover from an adapter check condition, the message must be transmitted again.

On a receive operation, an adapter check occurs if another character is received before the preceding character is moved into main storage. During receive operations, a byte-time microinterrupt is generated when the data in the buffer is to be sent to main storage. At the same time, the adapter continues to receive data and fills the SERDES register. A receive adapter check occurs if the control storage program does not reset the 'byte time' latch before the second byte-time microinterrupt occurs. Because the SERDES and the buffer are both full of data and the adapter continues to gate data from the SERDES to the buffer at byte time, the data that was in the buffer is lost and recovery action becomes necessary.



Data Set (Not) Ready

The IOB is posted complete on a leased line if the 'data set ready' line is not on or does not come on in 3 seconds after a supervisor call I/O request instruction is issued.

Abortive Disconnect

The IOB is posted complete on a switched line if the 'data set ready' line comes on and then goes off (abortive disconnect).

Receive Time-out

A receive time-out occurs (for BSC only) if 2 consecutive SYN characters are not received in 3.25 seconds.

Invalid ASCII Character

For an adapter with ASCII code, this error occurs (for BSC only) if any byte taken from storage during a transmit operation contains a 1 in the high-order bit position.

Invalid Frame

After a starting flag is sensed, a microinterrupt (invalid frame) is generated (for SDLC only) if:

- A second flag appears in less than 32 bits; an address field, a control field, and a frame check field must be in every frame.
- A flag is sensed off a byte boundary.
- Seven consecutive 1-bits are received.
- An abort sequence (11111111) is sensed.
- An idle (11111111 11111111) is sensed between starting and ending flags.

Secondary SDLC Time-out (Inactivity Timer)

The inactivity time-out period is 32 seconds. The inactivity timer is used by the SDLC adapter to prevent long periods of inactivity that might result from an error condition. The IOB is posted complete at the end of the inactivity time-out period.

Note: The inactivity timer is started when a receive operation is started. It is stopped when a valid frame is received.

Primary SDLC Time-out (Idle Detect and Nonproductive Timer)

These functions are provided for error recovery when no response, or a response not recognized by the primary station, is received to a poll.

The idle timer (3 seconds) is started after the frame with the poll bit is transmitted and the receive operation is started.

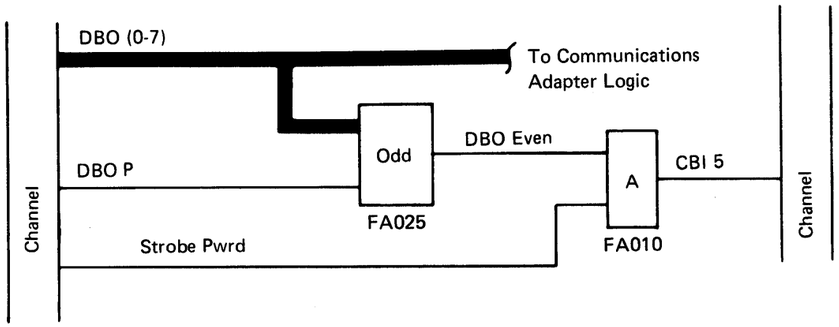
If the idle timer completes, or if a valid frame is received, the nonproductive timer (16 seconds) is started and the adapter begins monitoring for an idle condition (fifteen 1-bits). The idle monitor continues until a frame with the final bit is received. The nonproductive timer is restarted after each frame is received. If an idle condition (fifteen 1-bits) is detected, the idle detect status is posted. If the nonproductive timer completes, the nonproductive time-out status is posted.

Block/Frame Check Error

The block check characters (for BSC) or the frame check characters (for SDLC) were not correct on a received message. BSC and SDLC use CRC checking for EBCDIC, and BSC uses VRC/LRC checking for ASCII.

DBO Parity

Data on DBO is checked at strobe time to see if it is valid. If a parity check (DBO even) occurs, CBI 5 is activated to indicate a DBO parity check. A DBO parity check results in a machine check.



Diagnostics

Diagnostic Mode and Wrap Test

The diagnostic tests are used to check the control circuits, the cables to the modem, and the modem itself (if it is an IBM modem with the wrap test feature). Only the control circuits are checked in diagnostic mode. The wrap test expands the diagnostic tests to include the cables to the modem and the modem.

Diagnostic Mode

Diagnostic mode lets the control storage program test the control circuits by inhibiting or enabling selected bits (bits 2, 4, 6, and 7) of the diagnostic control register (DCR). These 4 bits are used to send data, control signals, and timing signals to the control circuits and to the modem.

Using bits 2, 4, 6, and 7 of the DCR, diagnostic mode permits the following functions to be performed:

- Bit 2 gates the control output register and 'transmit data' line to the modem.
- If bit 2 is off, the control output register is gated from the modem and put into positions 0 through 3 of the modem status register. Also, the transmit data is sent to the transmit FF at a mark level.
- If bit 4 is off, the internal clock oscillator and receive data are de-activated.
- Bit 6 supplies the internal clock oscillator for diagnostic mode. The internal clock test oscillator is used for testing purposes only.
- Bit 7 supplies data to the receive FF in diagnostic mode.

Wrap Test

The wrap test expands the diagnostic tests to include checking of the cables to the modem and the modem (if it is an IBM modem with the wrap test feature).

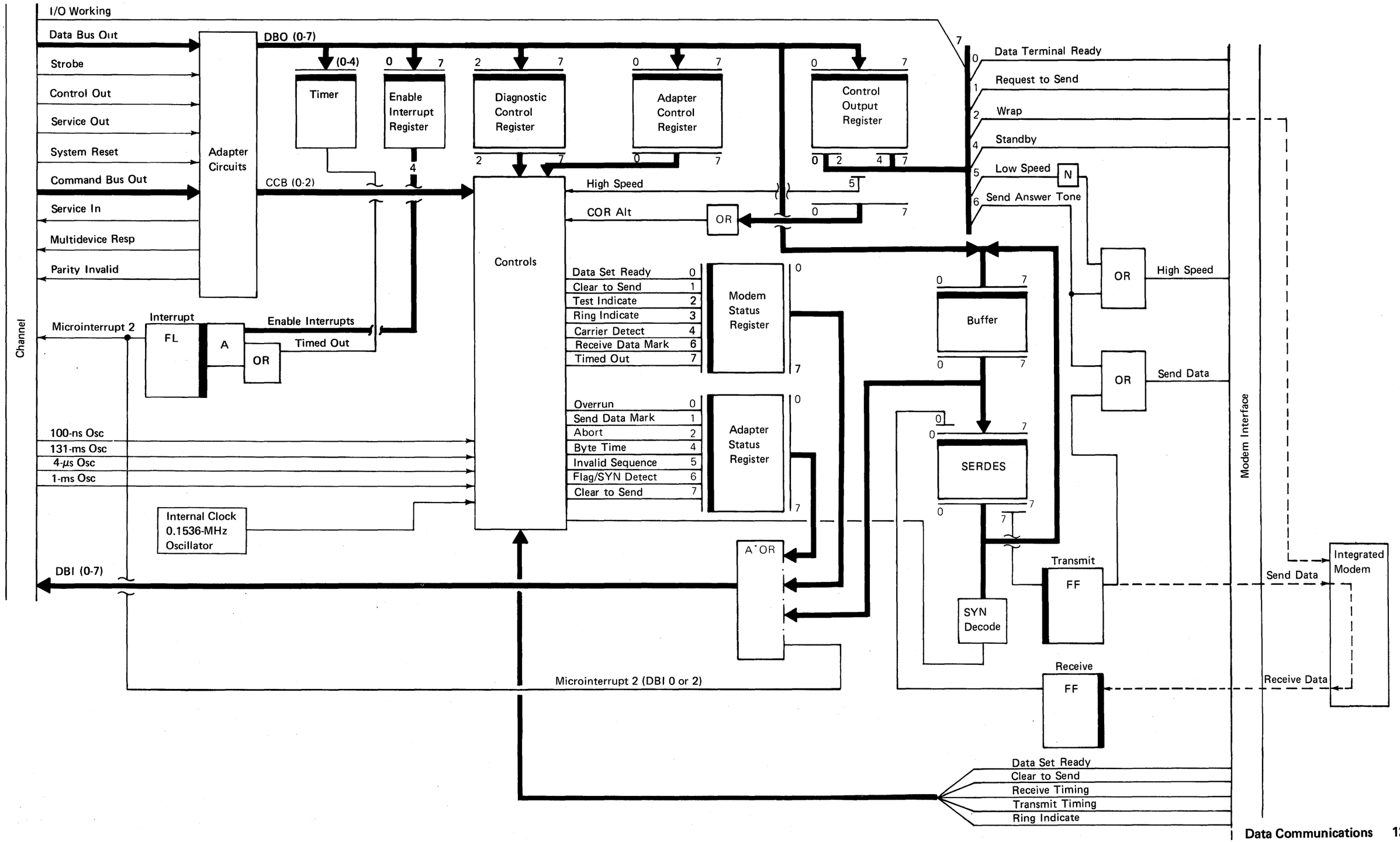
Data transmitted to the modem is sent back to the receive circuits as receive data, and the data is sensed with the modem status register (bit 6); the data received is then compared with the data transmitted. *Interface Wrap* shows the signals that are sent through the interface back to the communications adapter control circuits.

Interface Wrap

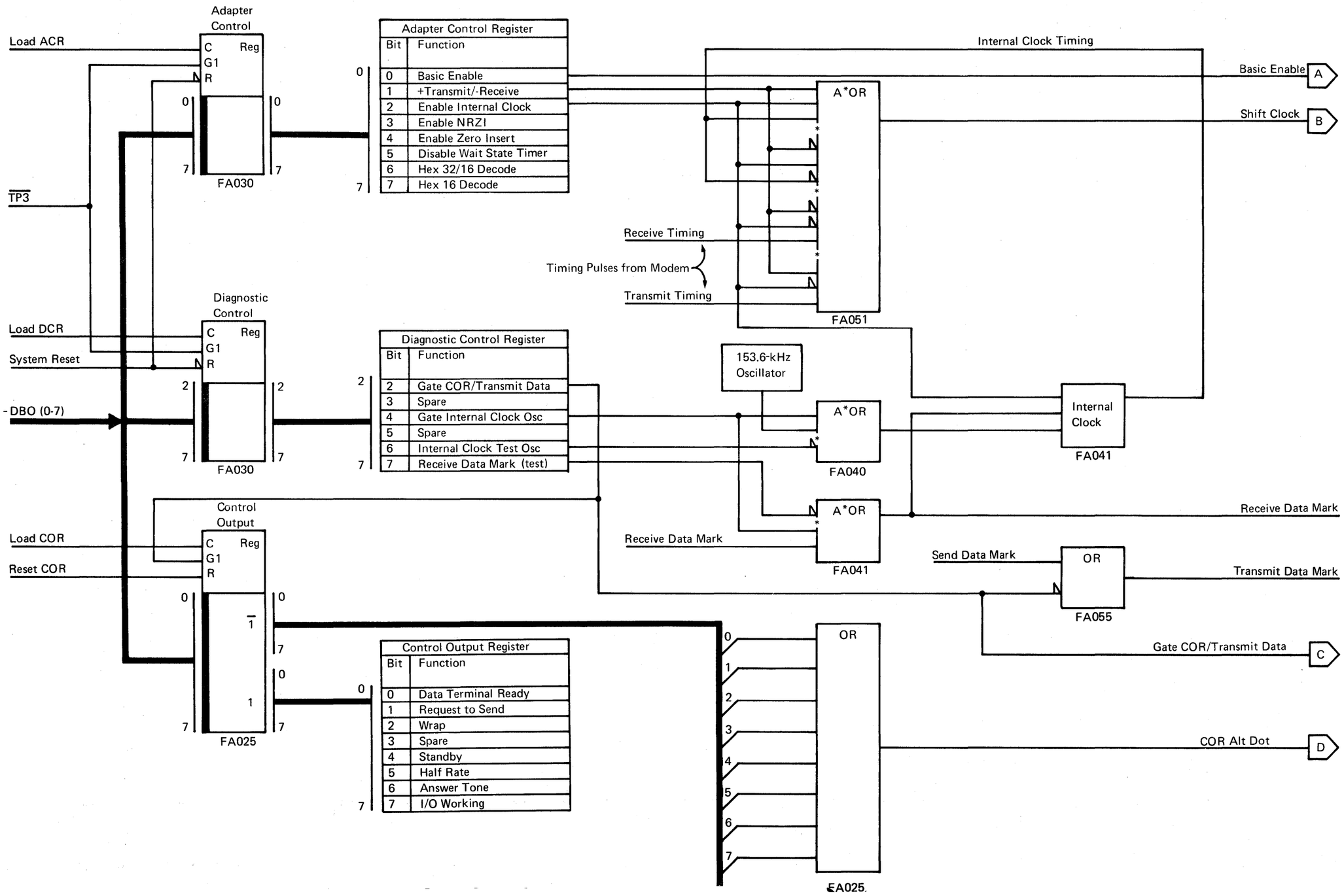
The following signals are wrapped from the EIA/CCITT card, through the exit cable to a wrap jumper assembly, and then back to the EIA/CCITT card. For the IBM 2400 BPS Integrated Modem, these same signals are wrapped from the adapter card, through the cable in B-A1U2 (line 1) and B-A2U2 (line 2) and then back to the adapter card. These cables are plugged into B-A1V2 (line 1) and B-A2V2 (line 2) for normal operation.

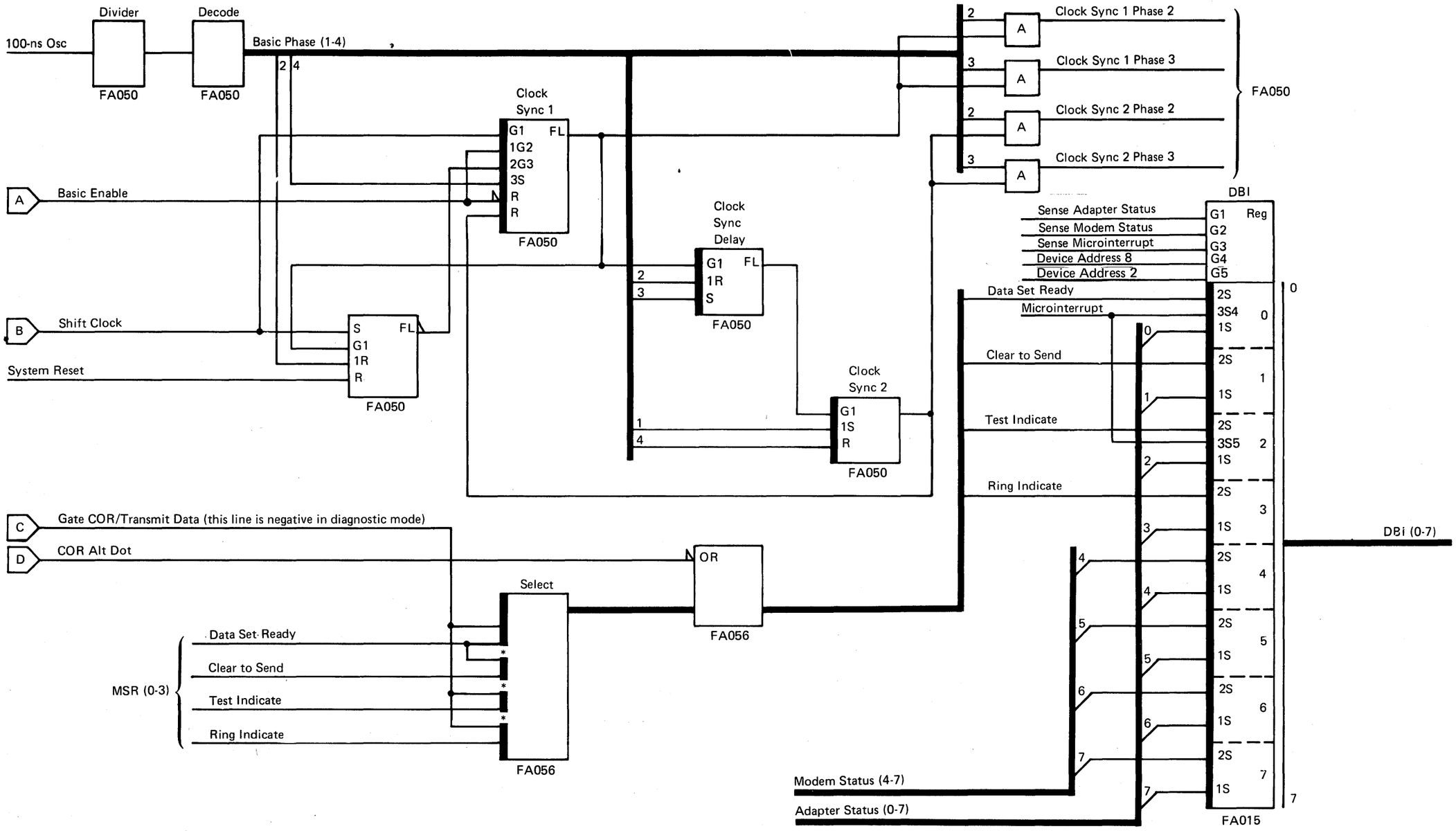
Data Terminal Ready	to	Data Set Ready
Request to Send	to	Ring Indicate
High Speed	to	Transmit Timing
Standby	to	Receive Timing
Send Data	to	Clear to Send
Wrap	to	Receive Data

Diagnostic Mode and Wrap Test Diagrams



Diagnostic Mode and Wrap Test Diagrams (continued)



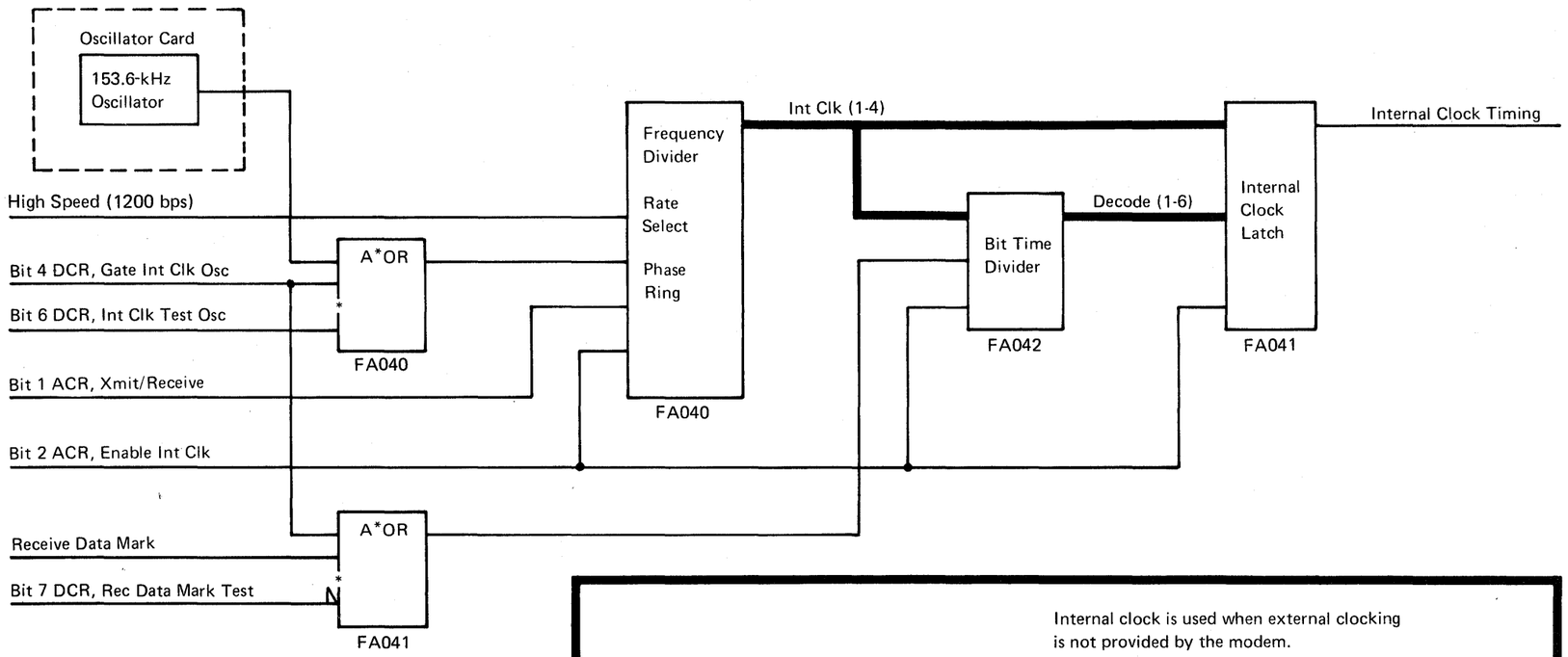

Divider
Decode
100-ns Osc
FA050
FA050
Basic Phase (1-4)
2 4
Clock Sync 1
G1 FL
1G2
2G3
3S
R
R
FA050
A
Basic Enable
Clock Sync Delay
G1 FL
1R
S
FA050
2
3
B
Shift Clock
S FL
G1
1R
R
FA050
System Reset
Clock Sync 2
G1
1S
R
FA050
1
4
2
A
Clock Sync 1 Phase 2
3
A
Clock Sync 1 Phase 3
2
A
Clock Sync 2 Phase 2
3
A
Clock Sync 2 Phase 3
FA050
DBI
Sense Adapter Status
Sense Modem Status
Sense Microinterrupt
Device Address 8
Device Address 2
G1 Reg
G2
G3
G4
G5
Data Set Ready
Microinterrupt
Clear to Send
Test Indicate
Ring Indicate
2S
3S4 0
1S
2S 1
1S
2S
3S5 2
1S
2S 3
1S
2S 4
1S
2S 5
1S
2S 6
1S
2S 7
1S
0
1
2
3
4
5
6
7
0
DBi (0-7)
7
FA015
C
Gate COR/Transmit Data (this line is negative in diagnostic mode)
D
COR Alt Dot
OR
FA056
Select
MSR (0-3)
Data Set Ready
Clear to Send
Test Indicate
Ring Indicate
FA056
Modem Status (4-7)
Adapter Status (0-7)

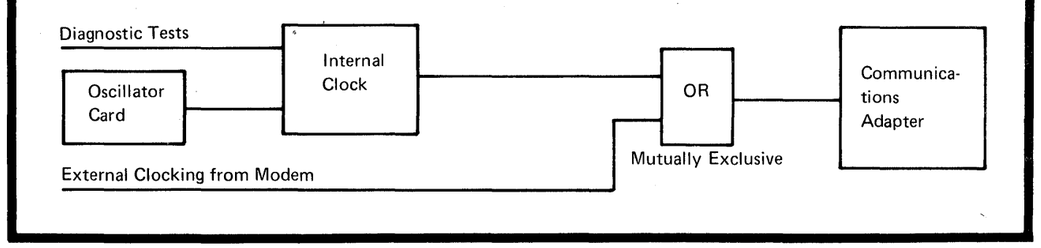
Internal Clock Feature

The internal clock feature supplies the clock pulses to the modem and to the communications adapter if the modem being used on that communication line does not supply the clocking. When the internal clock is used, an oscillator card must be installed in location A-A2Q2. The internal clock circuits are located on the adapter card in location A-A2J2 (line 1) or A-A2K2 (line 2). If internal clocking is required, one internal clock feature will furnish clocking to both communication features.

The control storage program enables the internal clock by setting bit 2 of the adapter control register. The control storage program also uses the internal clock during diagnostic mode to check the communications adapter and to transmit data. In diagnostic mode, bits 2, 4, 6, and 7 of the diagnostic control register are used to (1) reset the modem lines and internal clock oscillator, (2) gate the internal clock test oscillator, and (3) transmit or receive data.

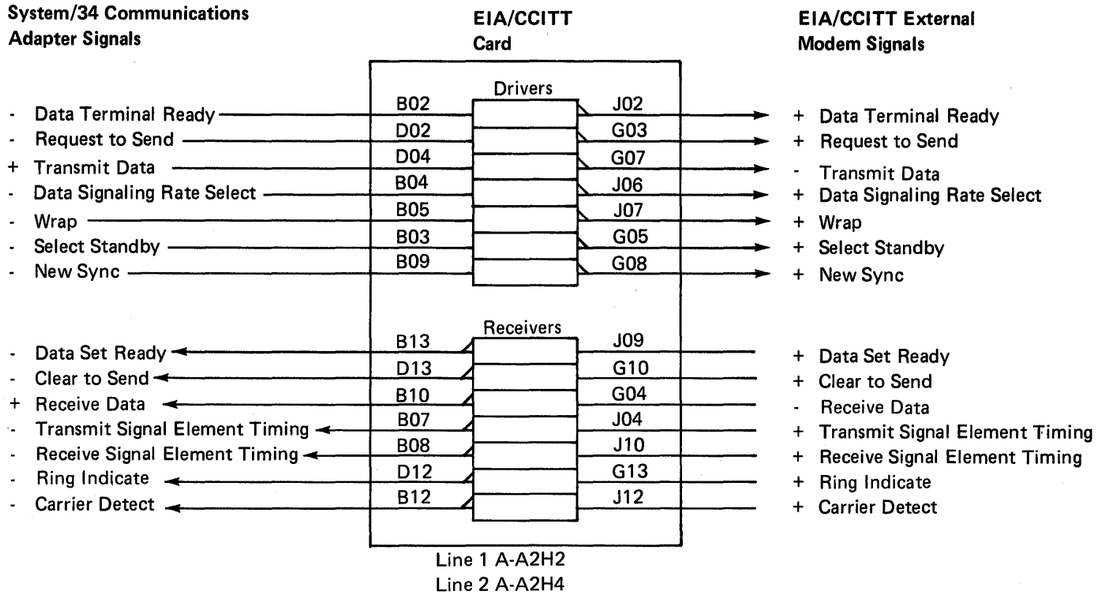
When the internal clock feature is used, the transmission rates are 1,200 bits per second (full rate) or 600 bits per second (half rate).





EIA/CCITT Line Adapter

The EIA/CCITT card located in A-A2H2 (line 1) or A-A2H4 (line 2) is a signal level convertor card that converts internal voltage levels to EIA/CCITT voltage levels specified by RS-232 and CCITT recommendations; it converts the voltage levels of the adapter card to the voltage levels needed by external modems.



MODEMS

When the data communications adapter uses clock pulses supplied by the modulator/demodulator (modem), the transmitting and receiving rates are determined by the modem used. These rates can be between 600 bits per second (bps) and 9,600 bps. However, the transmitting station and the receiving station must use compatible modems. When the internal clock is used, the rate is 1,200 bps or 600 bps when operating at half rate.

One of two IBM modems can be installed in the system:

- IBM 1200 BPS Integrated Modem
- IBM 2400 BPS Integrated Modem

For a 1200-bps integrated modem, the automatic answering and wrap features are supplied. (Both features are basic on a switched network.) This modem operates at 1,200 bps or, under control of the control storage program, at 600 bps (half rate).

For a 2400-bps integrated modem, automatic answering is basic for switched networks and optional for switched network backup (SNBU). This modem operates at 2,400 bps or, under control of the control storage program, at 1,200 bps (half rate).

A 2400-bps integrated modem operating at 1,200 bps cannot communicate with a 1200-bps integrated modem because of different modulation methods.

IBM 1200 BPS Integrated Modem

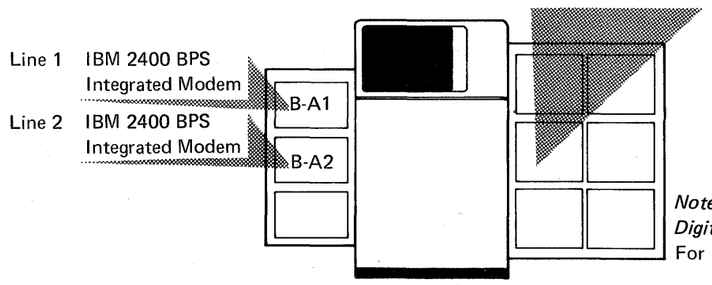
The IBM 1200 BPS Integrated Modem operates at 1,200 bps using frequency shift keying (FSK) modulation. An internal clock (oscillator card in A-A2Q2) must be installed to supply clock pulses to the modem. This modem is available in four types:

- United States nonswitched (leased)
- United States and Canada switched (using CBS coupler or a similar coupler)
- World Trade nonswitched
- World Trade public switched network (PSN)

DDSA
EIA/CCITT
IBM 1200 BPS
Integrated Modem
A-A2H2 (line 1)/A-A2H4 (line 2)

Communications Adapter
A-A2J2 (line 1)/A-A2K2 (line 2)

Internal Clock
A-A2Q2



Note: For a detailed explanation of DDSA, see *Digital Data Service Adapter* later in this section. For EIA/CCITT, see *EIA/CCITT Line Adapter.*

Nonswitched Network Interface

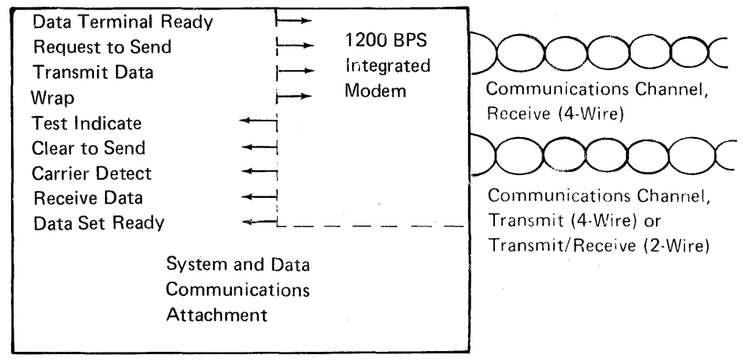
The modem is connected to the communications line by one or two twisted wire pairs; it is connected to the communications adapter by nine interface lines. The 'data set ready' line at a plus level indicates that power is on. The 'data terminal ready' line informs the modem that the terminal is ready to transmit or receive data. The 'wrap' and 'test indicate' lines are used for problem determination. To transmit data:

- The communications adapter activates the 'request to send' line.
- The modem (after the clear to send delay) activates the 'clear to send' line.
- The communications adapter puts a logical 0 on the 'transmit data' line to send a space; it puts a logical 1 on the 'transmit data' line to send a mark.

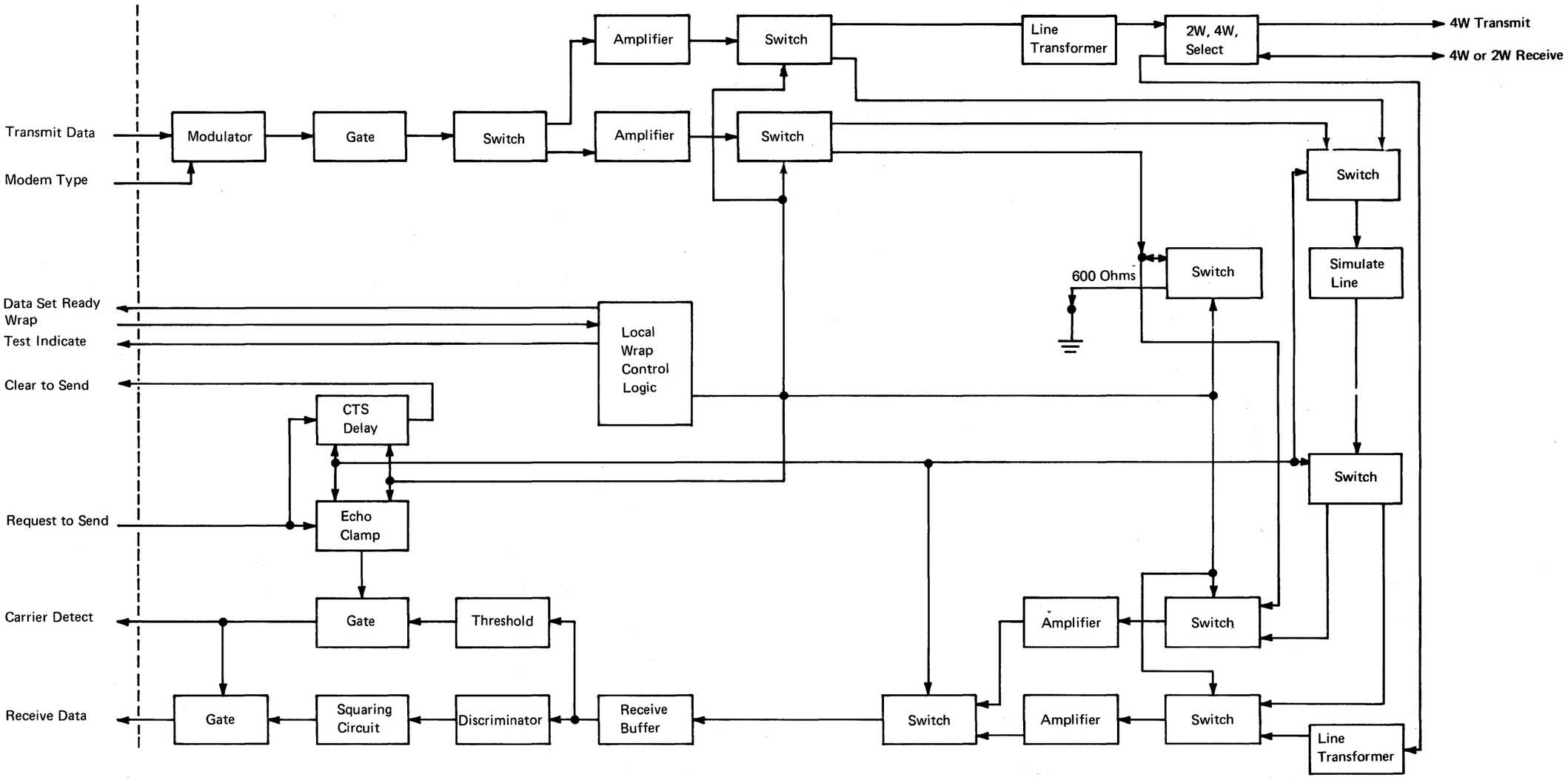
And to receive data:

- The modem receives a signal, activates the 'carrier detect' line, and unclamps the 'receive data' line.
- The communications adapter synchronizes with the signals on the 'receive data' line (logical 0 for space, logical 1 for mark) and receives data.

Nonswitched Network Interface



1200 BPS Integrated Modem with Nonswitched Network



Switched Network Interface

The purpose of the switched network 1200-bps integrated modem is to supply access to the switched networks in the United States and Canada.

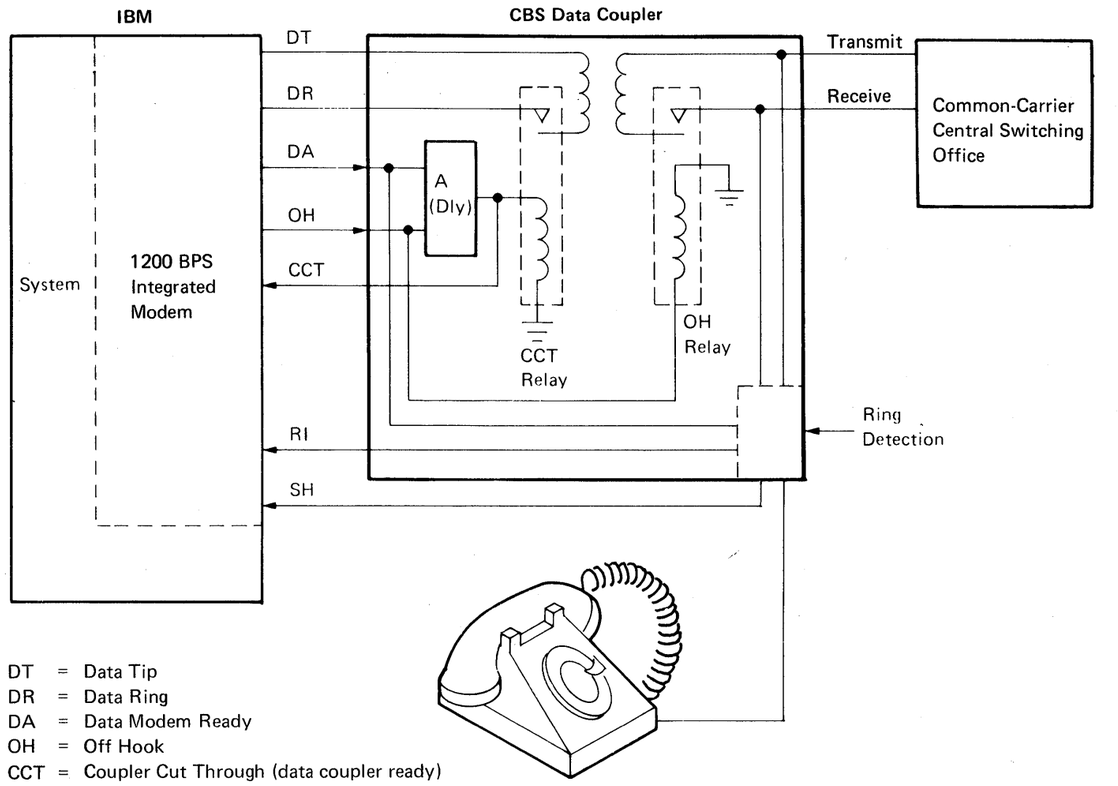
The switched network modem needs a common carrier CBS data coupler (or similar coupler) for connection to the line. The coupler supplies the status lines needed to control the automatic answering and disconnecting of a switched network connection.

The following figure shows the functions of the units in an automatically answered call. The automatic answering logic answers calls and permits the modem to use the line.

Status lines between the coupler and the business machine include: 'DA' (data modem ready); 'OH' (off hook–the handset is not on the cradle); 'CCT' (coupler cut through–the coupler has delayed long enough for automatic billing or similar equipment to function); 'RI' (ring indicate–the coupler has sensed ringing on the line); and 'SH' (switch hook–the telephone handset attached to the coupler has been lifted from the cradle and is active).

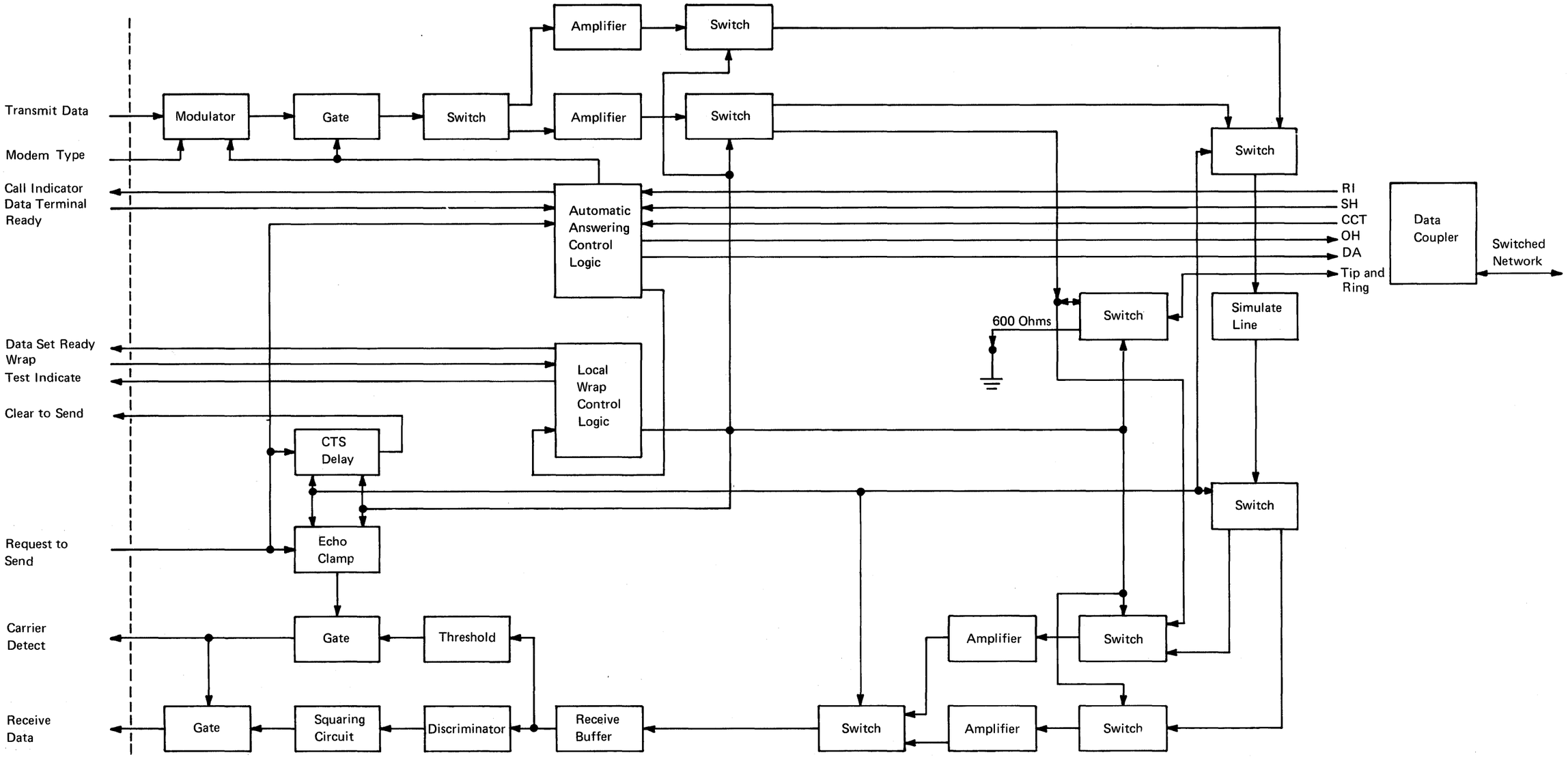
The telephone set attached to the coupler has a special pushbutton (exclusion key) on the cradle. When this pushbutton is pulled up, the handset is active and can be used for dialing a call or for voice communication.

Switched Network Interface



DT = Data Tip
DR = Data Ring
DA = Data Modem Ready
OH = Off Hook
CCT = Coupler Cut Through (data coupler ready)
RI = Ring Indicate
SH = Switch Hook

1200 BPS Integrated Modem with Switched Network



1200 BPS Transmit Operations

The 'request to send' line starts the clear-to-send delay (30 ms, 80 ms, or 230 ms for nonswitched networks and 230 ms for switched networks) that is selected when a 1200-bps integrated modem is installed. The modulator unclamps and the mark level on the 'transmit data' line causes the mark frequency to be emitted. When the 'clear to send' line becomes active, System/34 may send marks or spaces; the modulator sends the respective frequency. The transmit filter smoothes the waveshape and drives the line transformer, which couples the signal to the line.

At the end of a two-wire, half-duplex transmission, when the communications adapter turns off the 'request to send' line, the 'clear to send' line goes not active, the modulator clamps off, and the echo clamp delay starts. The purpose of the echo clamp is to prevent the receiver from sensing reflected signals; echo clamp must end before the remote modem is cleared for sending. Therefore, the echo clamp delay is always selected for a shorter delay than the remote modem's clear-to-send delay.

The transmit level is adjusted and recorded at the time of installation. (See paragraphs 31-310 and 45-730 in the *5340 System Unit Maintenance Manual*.) If the modem card is changed, adjust and record the new transmit level.

Receive Operations

The signal received from the line is coupled to the receive amplifier, which increases its amplitude. The bandpass filter blocks frequencies outside the channel range; this cleans up the signal.

The sensitivity threshold circuit (-33 decibels for nonswitched and -43 decibels for switched) senses a valid signal level and, after a delay that screens out noise hits, the 'carrier detect' line becomes active.

The discriminator recovers the data in the form of a distorted square waveshape, and the squaring circuit squares the waveshape and sends it to the communications adapter as received data. The squaring circuit output is at a mark level until the 'carrier detect' line is active.

The 'carrier detect' line is not active under two conditions:

- When the 'request to send' line drops to prevent the sensing of echo signals by the receiver.
- When a two-wire modem is transmitting.

Automatic Answering

The automatic answering logic responds to ringing by sending a 3.5-second, 2,100-Hz answer tone to the coupler. The answer tone informs the caller that the call has been answered and data can be transmitted.

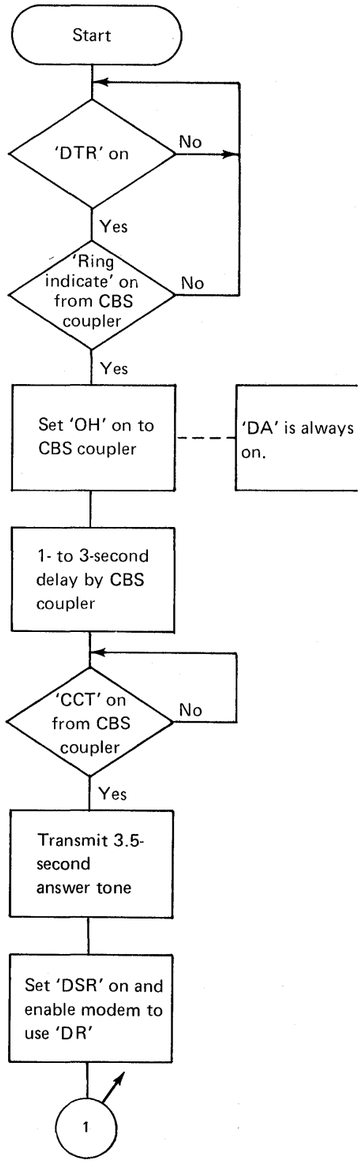
Interface

The modem interface remains the same as for a leased line except that the 'data set ready' line is controlled by the feature. This line does not go active until the answer tone has been sent and the line has been switched to the modem. The 'ring indicate' line informs the modem that a call is coming in, and the 'data terminal ready' line must be active before the feature can answer a call or maintain a switched network connection.

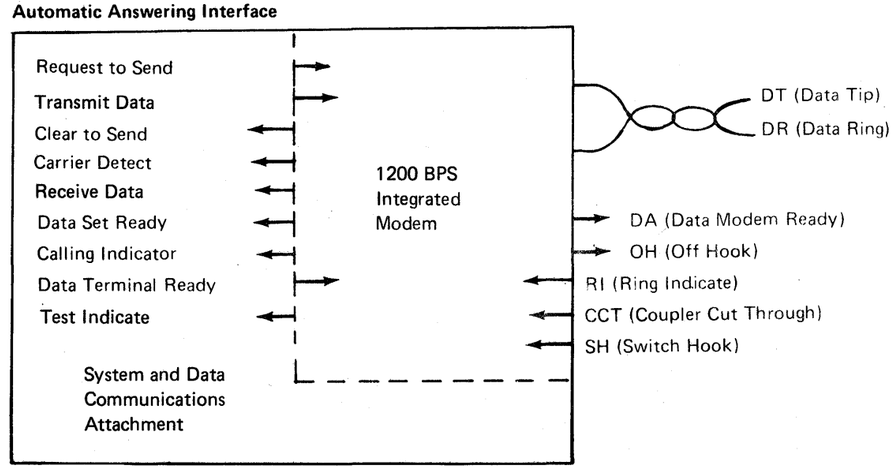
Note: Two status conditions inhibit automatic answering:

- If the 'switch hook' line is active, the telephone handset attached to the coupler is active and all calls receive a busy signal.
- If the 'data terminal ready' line is not active, the 'off hook' line is not activated and the coupler telephone rings until it is answered or until the person making the call disconnects.

Automatic Answering Operation



Automatic Answering Interface



1200 BPS Integrated Modem Tests

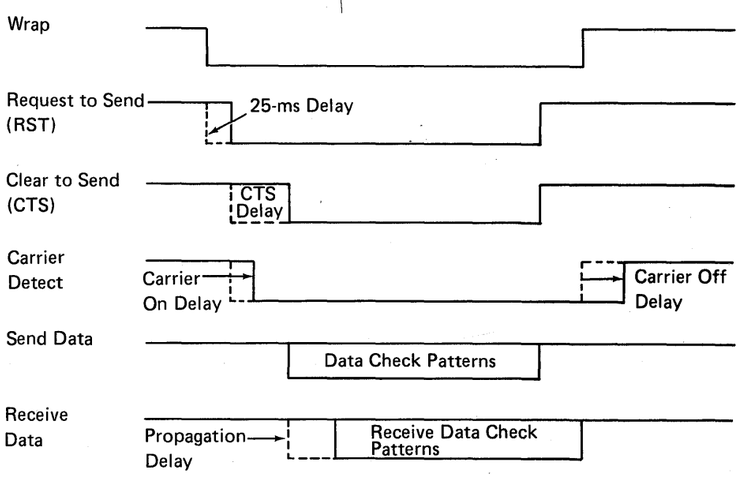
Wrap

The wrap test feature is an aid to problem determination. The *local wrap control logic* shown in the *1200 BPS Integrated Modem with Switched Network* figure is under control of the 'wrap' interface line from the communications adapter. The wrap test for a leased modem includes the *normal data flow test* only. The wrap test for a switched network modem includes the *normal data flow test* and the *automatic answer test,* as described in the following paragraphs.

Normal Data Flow Test

The communications adapter turns on the 'wrap' and 'request to send' lines and waits for the 'clear to send' and 'carrier detect' lines to come on. The adapter then sends variable data on the 'send data' line and monitors the result on the 'receive data' line after waiting for the propagation delay through the modem.

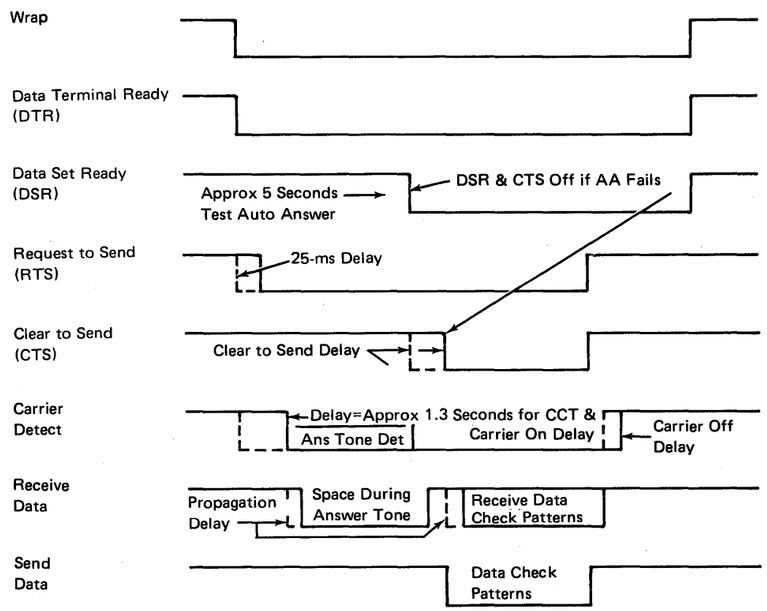
Timing Chart for Normal Data Flow Test



Automatic Answer Test

The communications adapter sets the 'data terminal ready', 'wrap', and 'request to send' lines on. When the 'wrap' line is set on, the modem simulates receiving ring indicate, waits 1.2 seconds, emits answer tone (2,100 Hz) for 3.5 seconds, checks that the 'receive data' line goes to space, and then sets the 'data set ready' line on. After the automatic answer test runs correctly, the modem automatically starts the normal data flow test.

Timing Chart for Automatic Answer Test

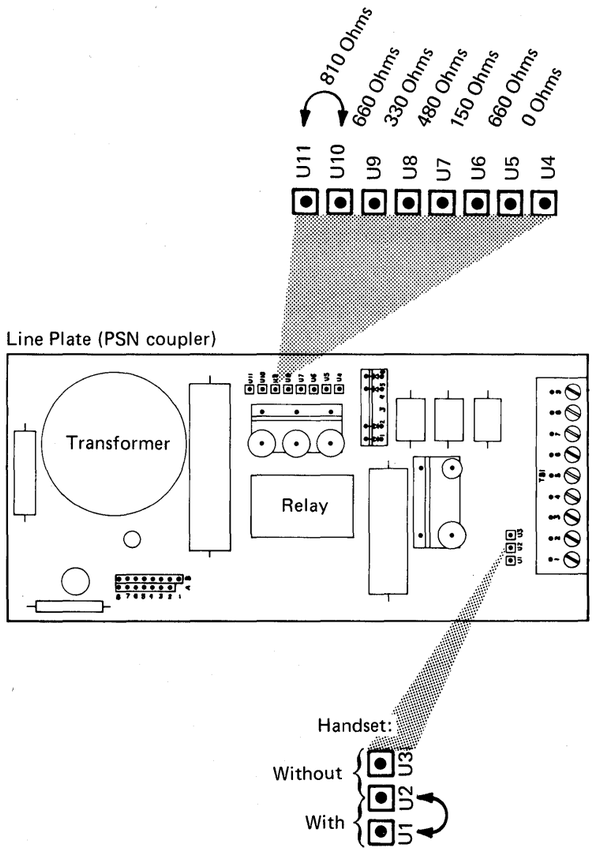


Line Plate for Public Switched Network

If a 1200-bps modem is being used on a World Trade public switched network, a line plate assembly is needed on the system to control the current from the telephone lines.

The current from the telephone lines is controlled by the 'connect data set to line' signal. If this signal is not active when the telephone rings, alternating current flows through both optical isolation diodes on the line plate. This alternating current causes the 'current detect' lines to go not active.

However, if the 'connect data set to line' signal is active when the telephone rings, the telephone lines are connected through a full-wave diode bridge and a direct current isolation transformer to the modem's transmit and receive circuits. The direct current through the primary and secondary winding of the transformer should be approximately balanced for linear alternating current operation. The transformer is balanced by adjusting the resistance on the line plate assembly using jumper locations U4 through U11. To make this adjustment, see paragraph 31-320 in the *5340 System Unit Maintenance Manual*.



IBM 2400 BPS Integrated Modem

The IBM 2400 BPS Integrated Modem converts binary data into modulated signals suitable for transmission on a communications network. The modem also collects binary data from the modulated signals.

A 2400-bps integrated modem operates with the following features:

- 2,400 bps on 3002 voice-grade communications channel or on the public switched network in the United States or Canada.
- Four-phase differential phase shift keying (DPSK) modulation.
- Own clock to maintain bit synchronization.
- Scrambler-descrambler, to prevent bit patterns sensitive to channel distortion.
- Low speed of 1,200 bps, under control of DTE interface lines.
- Modem panel status indicators; signal quality meter reads high when the signal is poor.
- Local loop test under DTE interface control.
- Multipoint tributary (receive equalization and transmit preequalization).
- Point-to-point (receive equalization; duplex or half-duplex).
- Switched network backup (automatic answering is an additional feature).
- Switched network (automatic equalization and automatic answering).

Operation

1 Transmitter

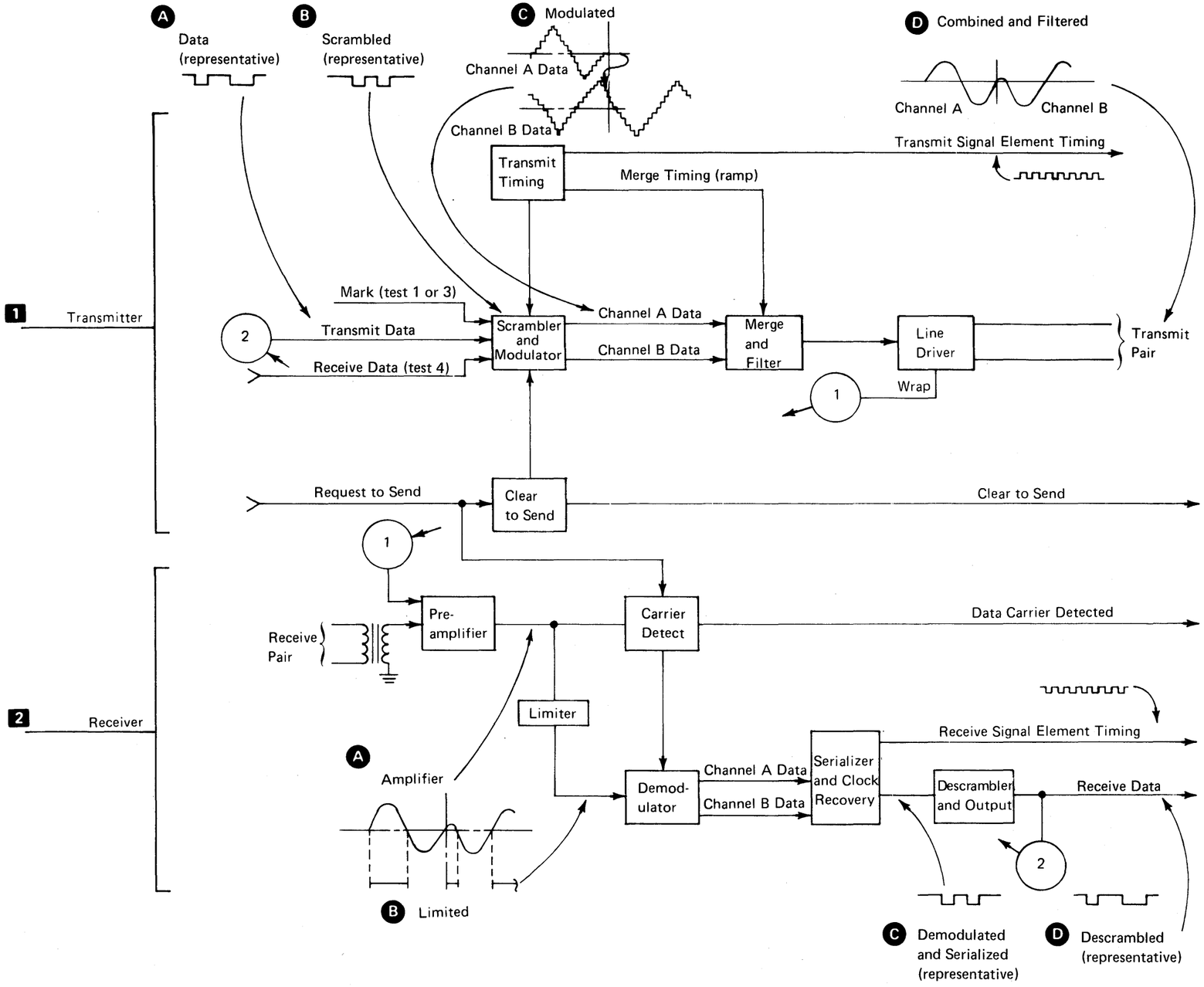
- (A) Clocks each data bit from the attached DTE device when the modem has been requested to transmit.
- (B) Forces a scramble pattern on the data to prevent long periods of sensitive data patterns that might be received in error.
- (C) Groups scrambled bits into consecutive pairs (dibits), then alternately encodes each pair as a phase shift by a digital multilevel process; one pair on Channel A data, the next pair on Channel B data, back to Channel A data, and so on (see *Modulation Theory* later in this section).
- (D) Merges and filters the encoded data from the two channels and transmits the resulting signal. Merging and filtering the data prevents the phase shift from going beyond the useful bandwidth of the communications channel (restricts the slope of the signal).

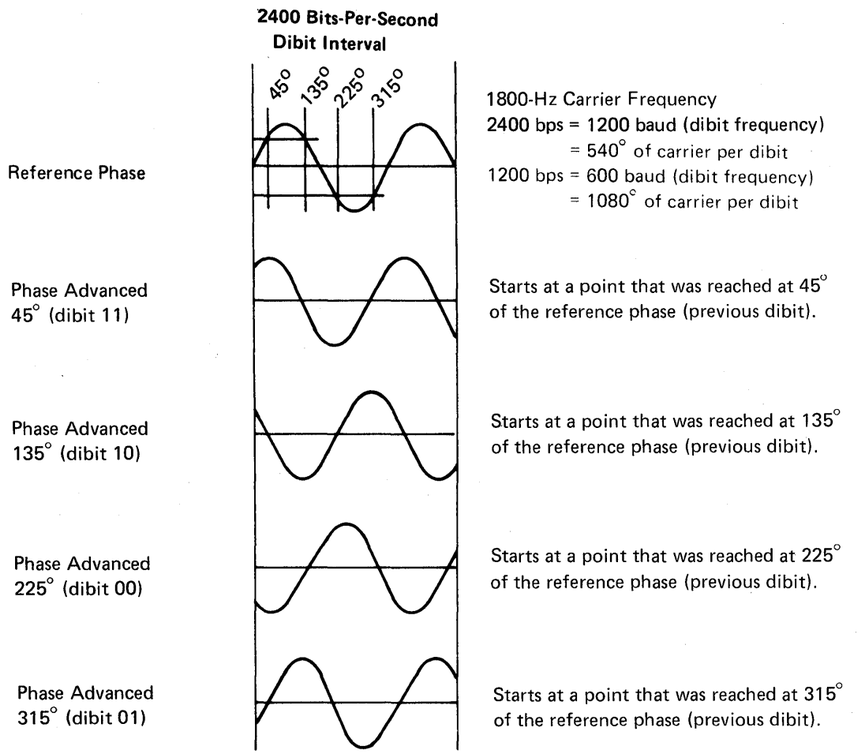
2 Receiver

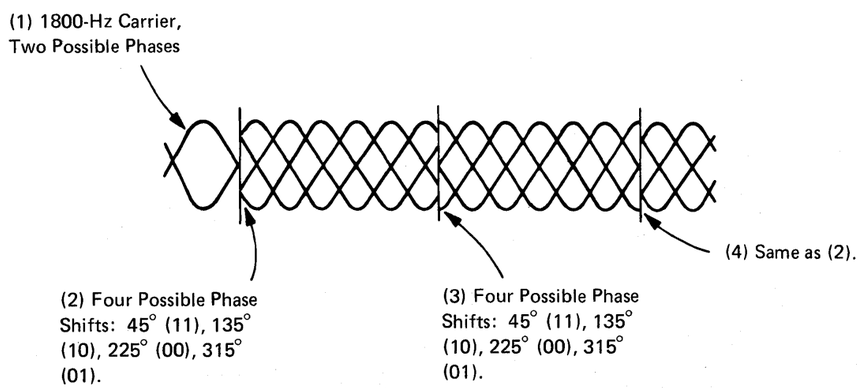
- (A) Increases the level of the signal received from the communications channel and senses the data carrier signal when it is received.
- (B) Converts the received signal into a square wave (limits the amplitude) and, by delay and comparison (see *Demodulation Theory* later in this section), derives Channel A data, Channel B data, and clock pulses from the received signal.
- (C) Alternately samples Channel A and Channel B data using a clock to serialize dibit data.
- (D) Reverses the scrambling process and sends the recovered binary data to the DTE with the clock.

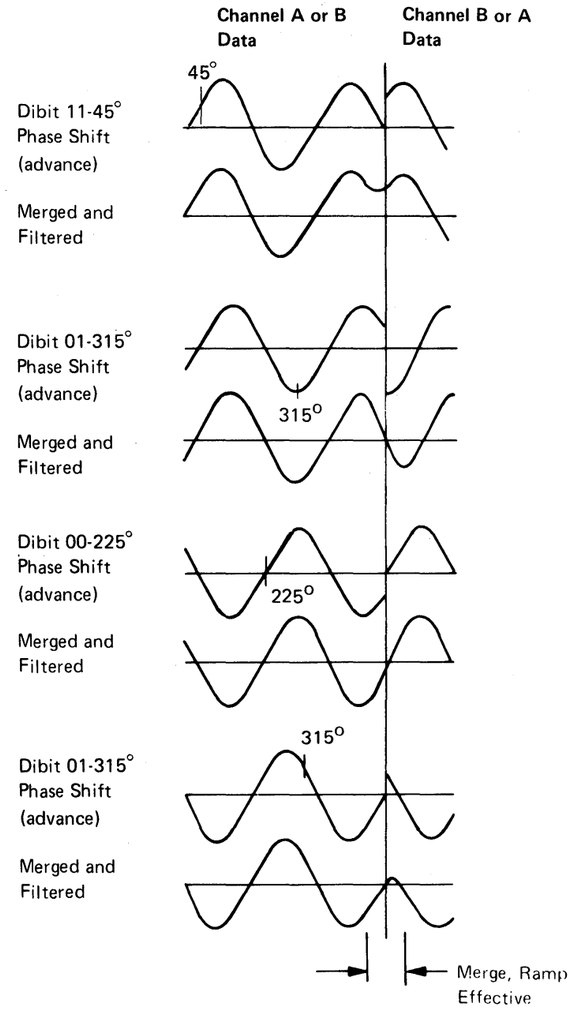
Notes:

1. DPSK (differential phase shift keying) uses the phases of each dibit as a reference for the phase shift advance of the following dibit. In demodulation, the phase of each dibit is delayed for comparison with the present dibit. (See *Modulation Theory* and *Demodulation Theory* later in this section.) It is very difficult to interpret correct encoding by looking at a modulated signal on the oscilloscope.
2. The frequency of a modulated signal is the relative steepness of the waveshape slope as seen on an oscilloscope. The reason for combining and filtering is to keep the steepness of the waveshape as close as possible to the steepness of the carrier frequency waveshapes.
3. Waveshapes of different steepness (frequency) are delayed differently by the communications channel. The function of the equalizer circuits is to compensate for the unequal delay by forcing selected delays on the waveshapes that are propagated more quickly by the communications channel.
4. The descrambler automatically recovers lost synchronization inside of 7 bits. Any error bit entering the descrambler may cause 3 output error bits, but such an error pattern falls in the 7-bit resynchronizing interval.

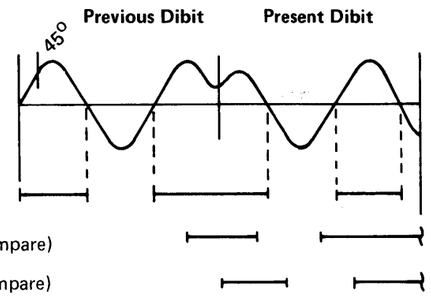

A
Data
(representative)
B
Scrambled
(representative)
C Modulated
Channel A Data
Channel B Data
D Combined and Filtered
Channel A
Channel B
Transmit Signal Element Timing
Transmit
Timing
Merge Timing (ramp)
1
Transmitter
Mark (test 1 or 3)
2
Transmit Data
Receive Data (test 4)
Scrambler
and
Modulator
Channel A Data
Channel B Data
Merge
and
Filter
Line
Driver
Transmit
Pair
1
Wrap
Request to Send
Clear
to Send
Clear to Send
1
Pre-
amplifier
Receive
Pair
Carrier
Detect
Data Carrier Detected
2
Receiver
Limiter
A
Amplifier
Demod-
ulator
Channel A Data
Channel B Data
Serializer
and Clock
Recovery
Receive Signal Element Timing
Descrambler
and Output
Receive Data
2
B Limited
C Demodulated
and Serialized
(representative)
D Descrambled
(representative)



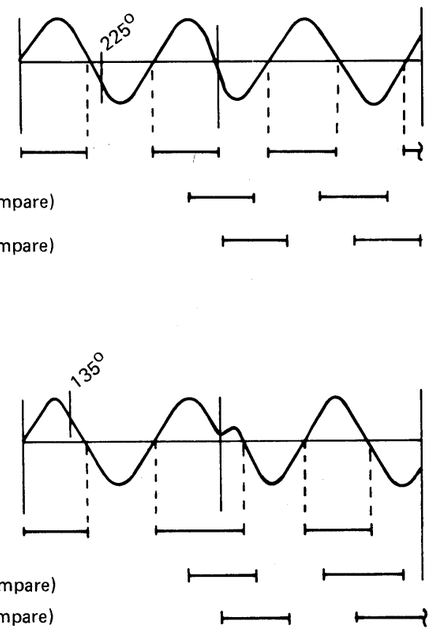




The ramp-controlled merger of Channel B or A data with Channel A or B data keeps the filtered signal slope within the optimum bandwidth.



For the present dibit, limiter output compares more in-phase than out-of-phase with the previous dibit, delayed 450°; thus, Channel A Data = 1. Limiter output also compares more in-phase than out-of-phase with the previous dibit, delayed 540°; thus, Channel B Data also = 1, and the dibit is 11.



For the present dibit, limiter output compares more out-of-phase than in-phase with the previous dibit, delayed 450°; thus, Channel A Data = 0. Limiter output also compares more out-of-phase than in-phase with the previous dibit, delayed 540°; thus, Channel B Data also = 0, and the dibit is 00.

For the present dibit, limiter output compares more in-phase than out-of-phase with the previous dibit, delayed 450°; thus, Channel A Data = 1. Limiter output compares more out-of-phase than in-phase with the previous dibit, delayed 540°; thus, Channel B data = 0, and the dibit is 10.

2400 BPS Transmit Data Flow

The transmit data flow moves from left to right in the figure. The lines named in the figure are described below.

Timing Pulses: 2,400-Hz or 1,200-Hz square waves, because of the operating speeds.

Request to Send: Activated by the DTE when it wants to use the modem to transmit data.

CSCD Timing Options: Selects the needed delay for clear to send and carrier detect after the 'request to send' line is activated.

2-Wire: Active when the modem transmits and receives on the same pair of wires connected to the communications network.

2400: Active when the modem is operating at 2,400 bps; not active at 1,200 bps.

Clamp Scrambler: Active when the 'clear to send' line is not active. Clamps scrambler output to space and unclamps the scrambler 1 bit time before the 'clear to send' line goes active.

Enable: Lets the line driver put signals on the line.

Clear to Send: Active when the modem is ready to transmit data.

2-Wire Clamp: Holds the 'receive data' line at a mark level when a 2-wire modem is transmitting.

Start Sync: Holds the 'receive data' and 'carrier detect' lines off at the DTE interface when the modem is resynchronizing.

Scrambler Input: Source of the data transmitted from the modem. It is held at a mark level for the reset, T1, and T3 positions of the Test/Operate switch but is controlled by the DTE for the Operate and T2 positions. On a 4-wire modem, the 'receive data' line goes to the scrambler for T4; a 2-wire modem set to T4 holds the scrambler input to a mark level.

Scrambler Output: A fixed pattern that repeats all bits when scrambler input is held at a mark level for the T1 and T3 positions of the Test/Operate switch.

Chan A Data and Chan B Data: Scrambler output has been converted to the stair-step waveshape shown under *Operation*. The modulator groups the scrambled data into consecutive pairs of bits (dibits). Each dibit has a phase relationship to the preceding dibit that relies on the value (00, 01, 10, or 11) of the dibit. See *Modulation Theory*.

Ramp Clock A and Ramp Clock B: 600-Hz square waves at 2,400 bps; 300-Hz square waves at 1,200 bps.

Transmit Clock: Data timing to the DTE; 2,400 Hz to 1,200 Hz because of the operating speeds.

Ramp: Upward and downward sloping signal used to smooth the signal for a phase shift. See *Modulation Theory*.

Analog Transmit Signal: Data signals from Channel A and Channel B are combined under ramp control and filtered to supply the signal that is put on the line.

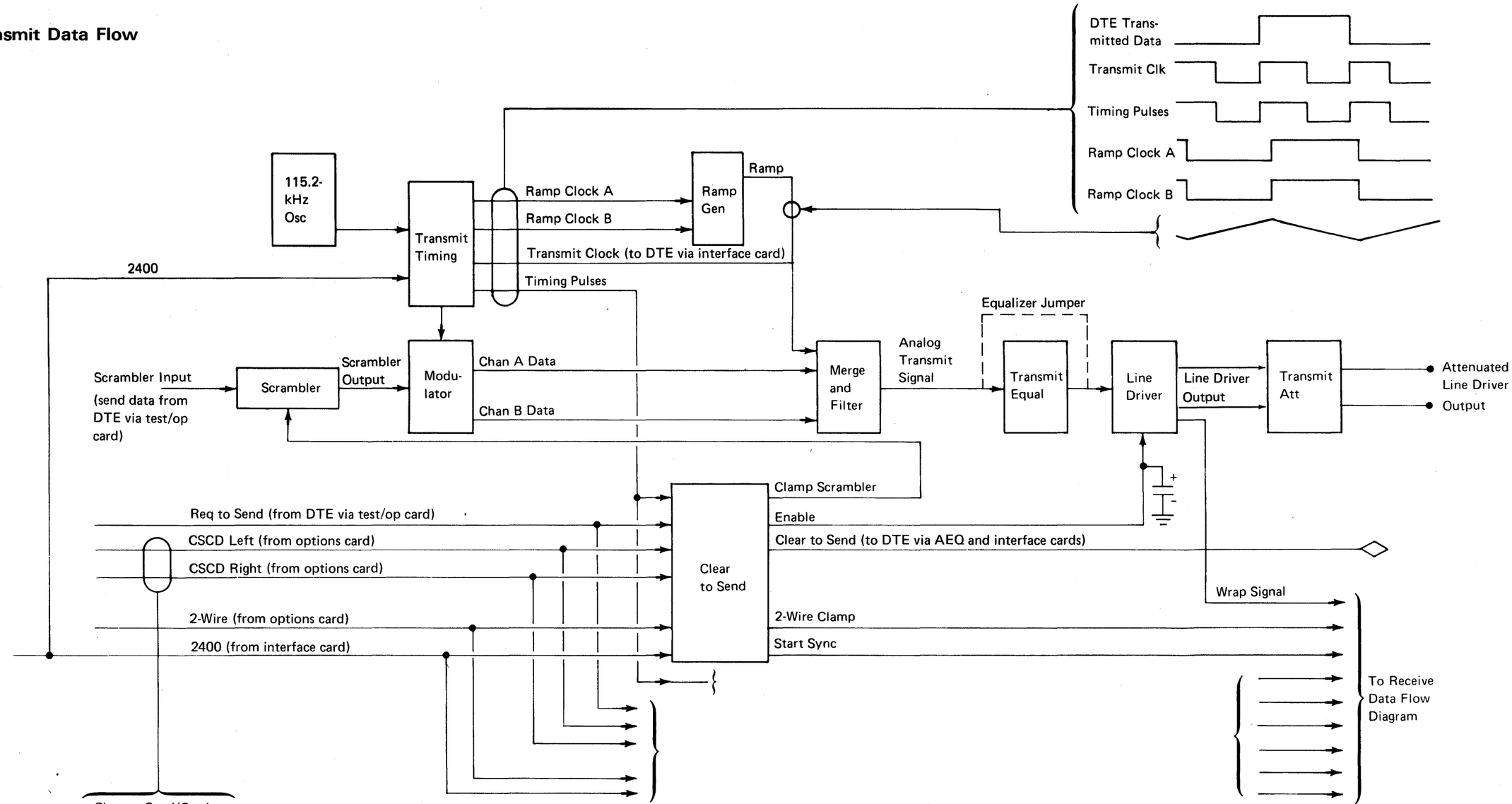
Equalizer Jumper: Supplies continuity to the line driver when transmit equalization is not needed. Equalization is usually done at a receiver to compensate for envelope delay distortion on the line, but the transmit signal from a multipoint secondary modem must be preequalized (transmit equalization) because the multipoint primary modem must receive from several secondary modems on different type lines. Equalizers are automatically disabled during local loop testing (T1, T2, or DTE test) and at 1,200 bps during down-line testing (T3 and T4).

Line Driver Output: Two lines carrying the signal that will be transmitted in a push-pull method. The capacitor is on the back panel of the logic board; it is needed for World Trade countries.

Attenuated Line Driver Output: Two lines carrying the transmitted signal with the power level decreased to the needs of the line.

Wrap Signal: Transmitted signal with the power decreased to simulate the received signal level. It is used to supply a received signal when the modem is in local loop test mode (T1, T2, or DTE test).

2400 BPS Transmit Data Flow



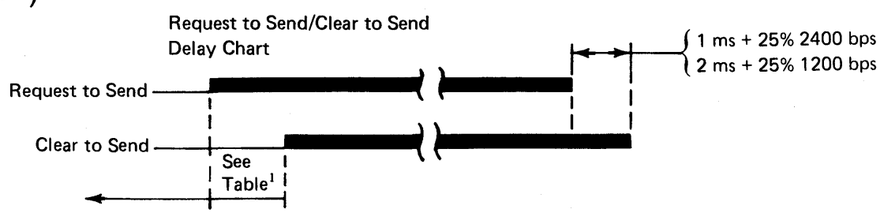
Clear to Send/Carrier Detect Strapping

CSCD	Left	Right
	Off	Off
	Off	On
	On	Off
	On	On

[1] **Clear to Send Delay (ms) Table**

2400 BPS	1200 BPS
8.3-8.8	8.3-9.2
25.0-25.4	25.0-25.8
*75.0-75.3	*75.0-75.9
*146.6-147.5	*146.6-147.5

*Add 35 ms if the switched network feature is installed.



2400 BPS Receive Data Flow

The receive data flow moves from left to right in the figure. The lines named in the figure are described below.

Wrap Signal: Transmitted signal with the power decreased to simulate the received signal level. It is used to supply a received signal during local loop test mode (T1, T2, or DTE test).

Receive Input From Line: Similar to the wrap signal but received from a remote modem. Wrap and received line signals have very low amplitude.

Preamp Output: Amplified line or wrap signal.

Minus Signal and Plus Signal: Active when the signal is more than the threshold in the negative or positive direction.

2-Wire and Request to Send: Both are active when a 2-wire modem is transmitting.

Signal Threshold: Combined plus and minus signals when both are over the threshold.

Start Sync: Holds the 'receive data' and 'carrier detect' lines off at the DTE interface when the modem is resynchronizing.

Timing Pulses: 2,400-Hz or 1,200-Hz square waves because of the operating speeds.

Clear to Send/Carrier Detect (CSCD): Selects the needed delay for clear to send and carrier detect relative to the status of the 'request to send' line and the 'signal threshold', respectively.

Internal CD: Carrier detected over the threshold and carrier detect delay timed out.

Start Resync: Lets clock recovery and demodulator circuits start operating.

Serial Data: Connects to carrier detect logic for sensing of the mark that is emitted from the scrambler of the transmitting modem just before the 'clear to send' line comes on.

Hysteresis: Increases the threshold sensor input by 3 decibels.

Carrier Detect: Active when the line signal is being received over the threshold and is being demodulated to supply valid received data to the DTE interface.

Descrambler Clamp: Active when the 'carrier detect' line is not active; holds descrambler output at the mark level.

Data Clamp: Active when the 'carrier detect' line is not active; holds the 'receive data' line to the DTE at the mark (off) level.

Equalizer Jumper: Supplies continuity of preamplifier output to the demodulator circuits when the receive equalizer is not used. Receive equalization compensates for envelope delay distortion on the line and is used when the line signal has not been preequalized (see *Transmit Data Flow*). Various applications use an automatic equalizer (switched network), a customer adjustable equalizer (leased line), or a compromise equalizer (SNBU). Equalizers are automatically disabled during local loop testing (T1, T2, and DTE test) and during down-line testing (T3 and T4) at 1,200 bps.

Limiter Output: Logic level that is active when preamplifier output is plus and not active when it is minus.

Shift Reg Clock: 115.2-kHz or 57.6-kHz square waves because of the operating speeds.

Shift Reg 80: Limiter output delayed 450° (2,400 bps) for phase comparison with the following dibit.

Shift Reg 88: Limiter output delayed 990° (1,200 bps) for phase comparison with the following dibit.

Shift Reg 96: Limiter output delayed 540° (2,400 bps) or 1,080° (1,200 bps) for phase comparison with the following dibit.

Chan A Data and Chan B Data: Intermediate demodulator outputs representing dibit values (see *Demodulation Theory*).

2400: Active when the modem is operating at 2,400 bps; not active at 1,200 bps.

Signal Quality Sample: Timing pulse that samples the demodulator B channel to determine how much noise and distortion are present in the signal.

Serial Data: Serialized dibits received from Chan A data and Chan B data; demodulation is complete.

Rcv Clock: Approximately 2,400-Hz or 1,200-Hz square waves adjusted to the timing of the 'receive data' line.

Descrambled Data: Original transmitted data recovered from serial dibit data.

Receive Data FET: Descrambled data shifted to the DTE interface 1 bit at a time.

Unclamp Demodulation Circuits

Legend

2W	2-wire
4W	4-wire
LL	Leased line
SNBU	With SNBU
$\overline{\text{SNBU}}$	Without SNBU

Modem	Echo Suppressions?	LL Clear to Send (ms)	SNBU/Sw Network Clear to Send (ms)
4WLL-$\overline{\text{SNBU}}$		8.5**	
		25	
4WLL-SNBU		8.5**	75*
			147
		25	75*
			147
2WLL-$\overline{\text{SNBU}}$	No	75***	
		147	
	Yes	75***	
		147	
2WLL-SNBU		75***	75*
			147
		147	147
Switched network			†75***
			†147
CADUCEE		25	

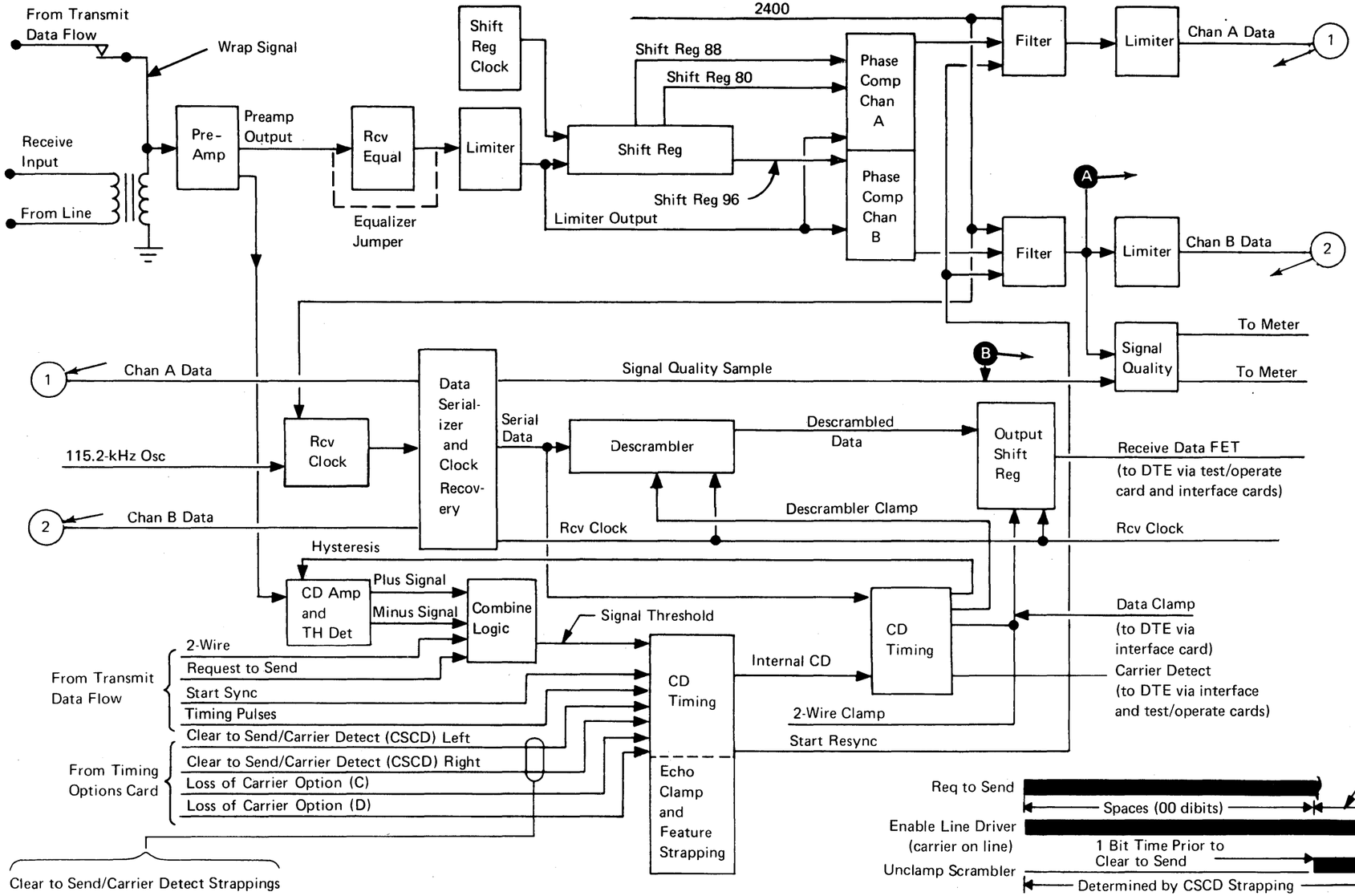
* Permissible only if SNBU operation is in the local area.

** Used only on multipoint tributary modems when new sync is used at the control station.

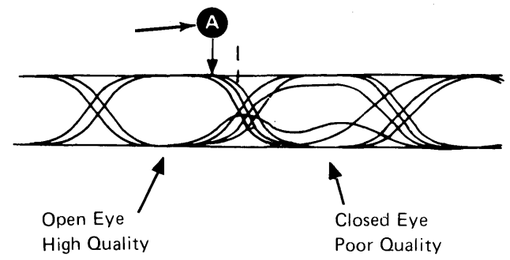
*** Used only on short lines, where turnaround is critical and the communications facility characteristics are suitable (minimum echo).

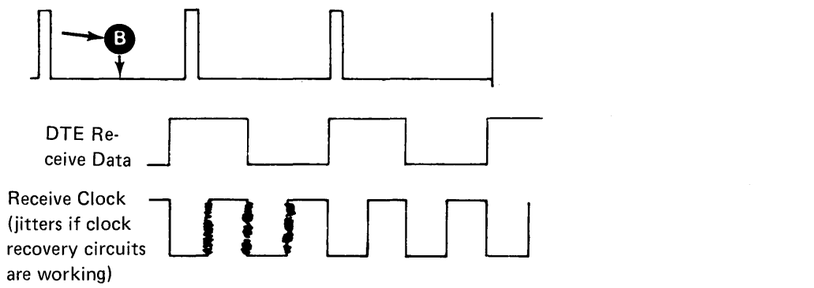
† Add 35 ms if the switched network feature is installed.

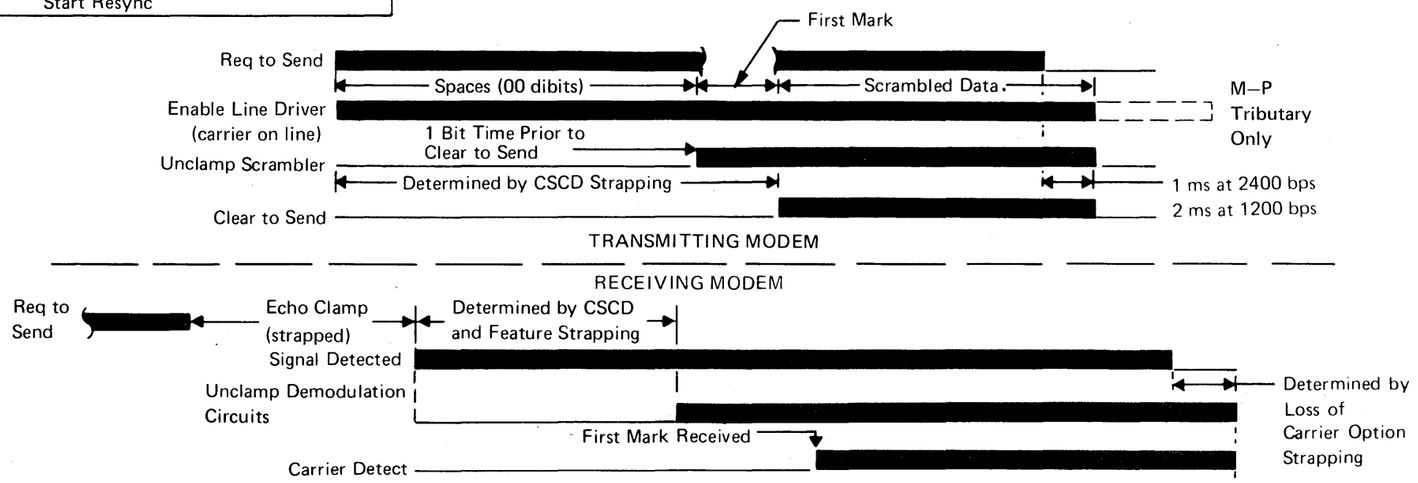
2400 BPS Receive Data Flow



Scope Presentations







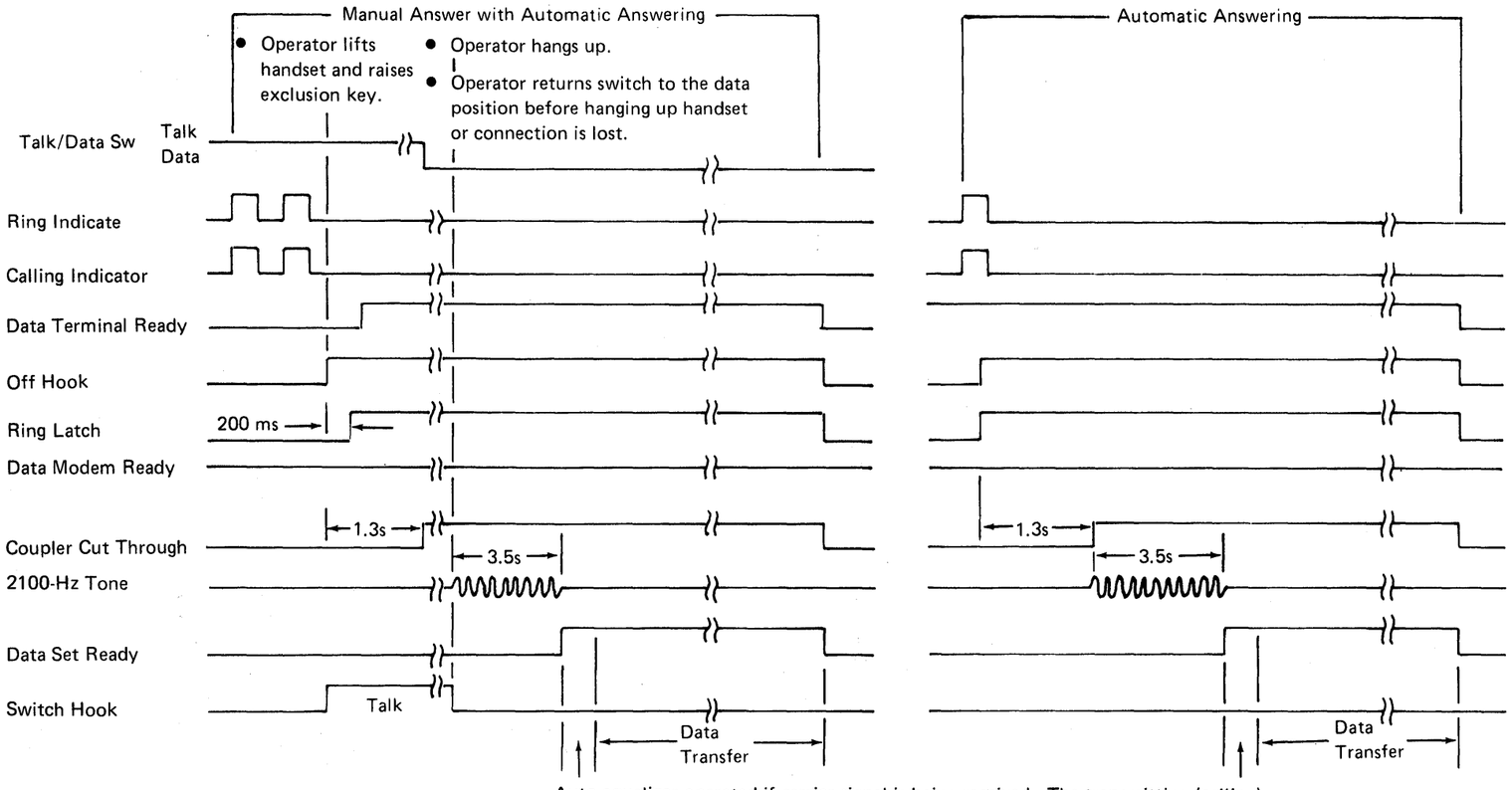
Switched Network and Automatic Answering Operation

The automatic answering feature lets the DTE automatically respond to a switched network call. Automatic answering is supplied with the switched network or as a feature with SNBU. Automatic answering is connected to the line through a CBS data coupler (or similar coupler).

Calls are answered if the 'data terminal ready' line is on and are disconnected when the 'data terminal ready' line drops. With automatic answering, the modem does not activate the 'data set ready' line to the DTE until the switched network connection is complete.

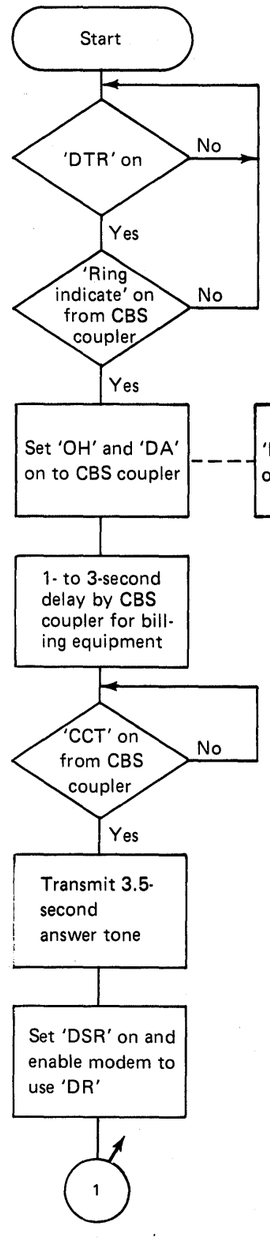
Line connections with automatic answering are different from leased line connections. Because the line is used for transmitting answer tone, the modem is excluded from the line until the 'data set ready' line turns on.

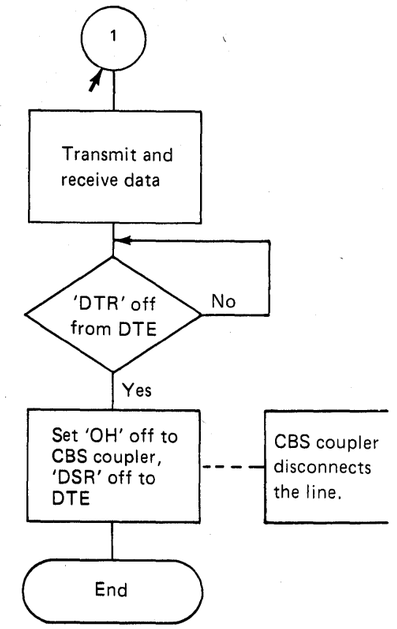
Control of the line pair with automatic answering is by analog switches. These switches permit the 'data tip' line to transmit answer tone while holding the 'data ring' line to ground. Then, the 'data ring' line is released to the modem for data while holding the 'data tip' line to ground.



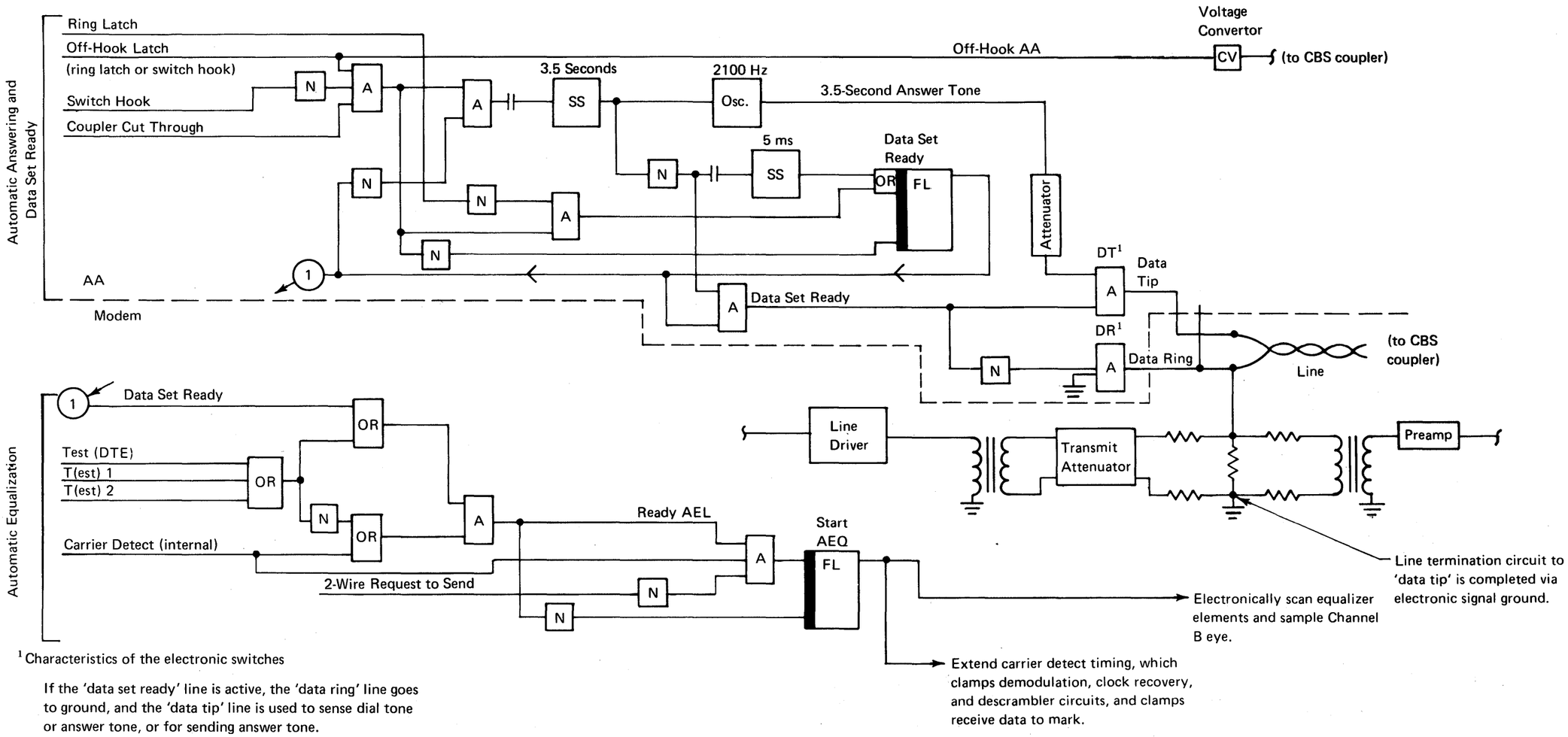
Auto equalizer operated if carrier signal is being received. The transmitting (calling) modem sends 1008 ms of scrambled mark for this purpose, during clear-to-send delay.

Automatic Answering Operation





2400 BPS Integrated Modem with Switched Network and Automatic Answering

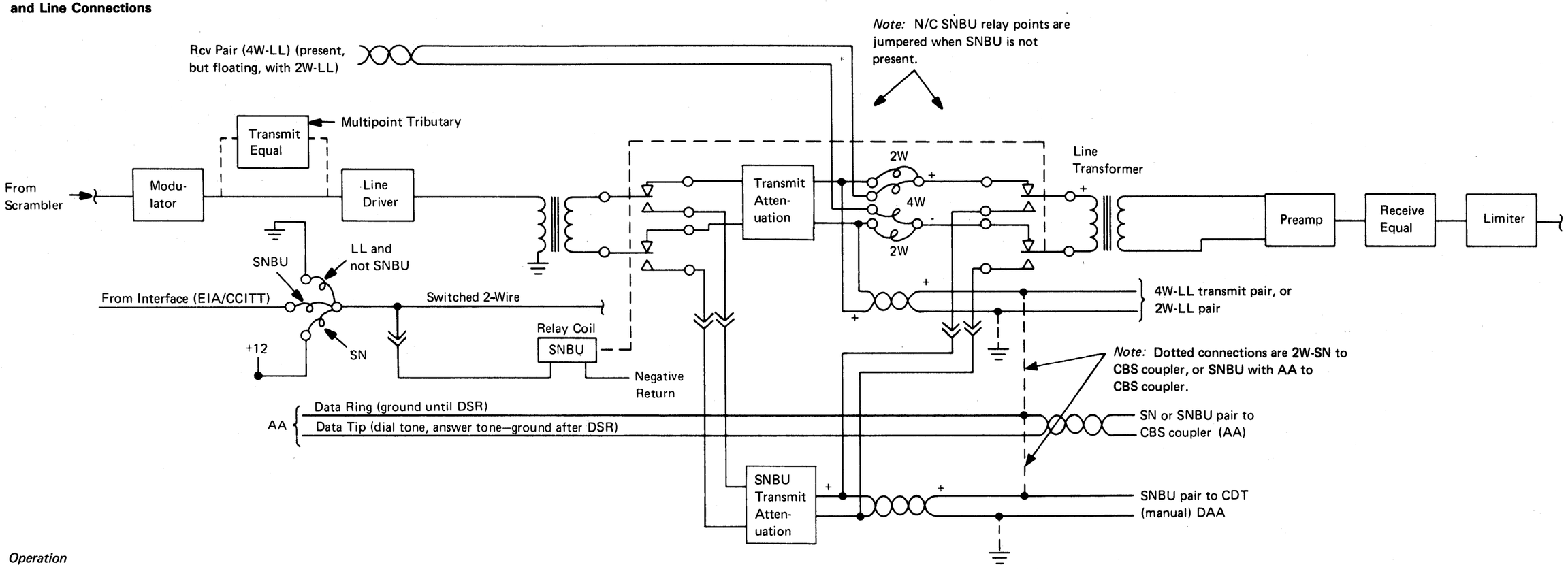


[1] Characteristics of the electronic switches

If the 'data set ready' line is active, the 'data ring' line goes to ground, and the 'data tip' line is used to sense dial tone or answer tone, or for sending answer tone.

If the 'data set ready' line is not active, the 'data tip' line goes to ground, and the 'data ring' line is used for transmitting or receiving data.

Switched Network Backup (SNBU), Wrap, and Line Connections



Operation

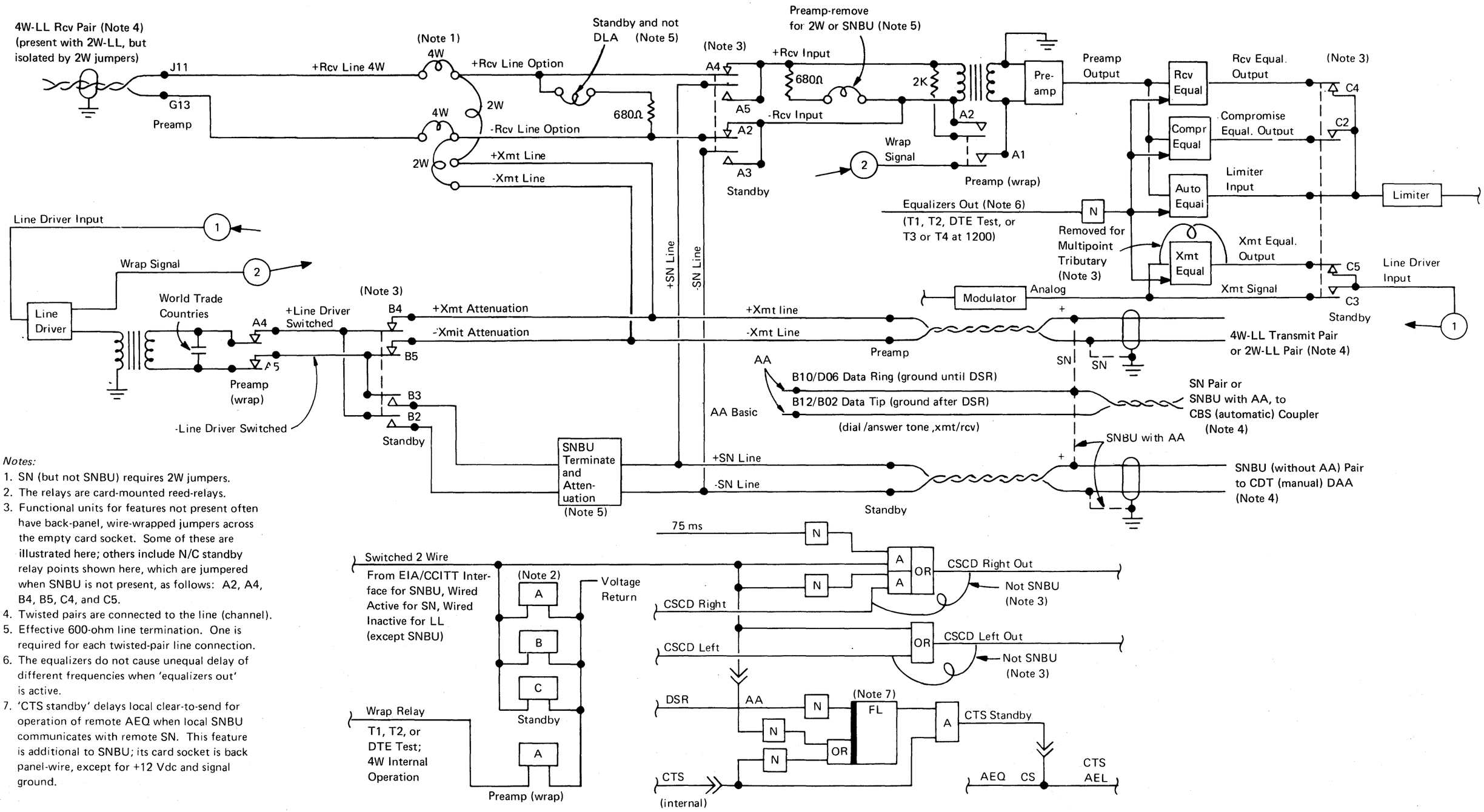
One, two, or three twisted pairs may be present because of the machine features. When SNBU is activated, it disconnects and terminates the leased line pair(s) and connects one of two possible switched network pairs to the line transformer. Which pair is used relies on if SNBU has automatic answering.

Leased line modems always have a transmit pair and a receive pair but the receive pair is not connected for 2W-LL. (SNBU and the switched network features are mutually exclusive.)

When SNBU is used, (1) the switched network receiver sensitivity (–40 db) must always be used, and (2) duplex throughput on leased line operations is done in the modem by holding 'request to send' on so that there is no 'clear-to-send' delay at turnaround. The modem permits the DTE to control 'request to send' on SNBU operations.

In addition, the clear-to-send delay for the first transmission is extended to 1,020 milliseconds so that the automatic equalizer at the receiver can complete its cycle.

Switching and Jumpers for 2W/4W, SNBU, Wrap, and Line Connections



Notes:

1. SN (but not SNBU) requires 2W jumpers.
2. The relays are card-mounted reed-relays.
3. Functional units for features not present often have back-panel, wire-wrapped jumpers across the empty card socket. Some of these are illustrated here; others include N/C standby relay points shown here, which are jumpered when SNBU is not present, as follows: A2, A4, B4, B5, C4, and C5.
4. Twisted pairs are connected to the line (channel).
5. Effective 600-ohm line termination. One is required for each twisted-pair line connection.
6. The equalizers do not cause unequal delay of different frequencies when 'equalizers out' is active.
7. 'CTS standby' delays local clear-to-send for operation of remote AEQ when local SNBU communicates with remote SN. This feature is additional to SNBU; its card socket is back panel-wire, except for +12 Vdc and signal ground.

DIGITAL DATA SERVICE ADAPTER

The Digital Data Service Adapter is an integrated adapter that lets System/34 interface to a digital data network through a channel service unit. The channel service unit is similar to the data access arrangements used with the IBM 1200 and IBM 2400 BPS Integrated Modems. The digital data network is a 4-wire, full-duplex network that operates in synchronous mode. However, operation from System/34 is half-duplex only.

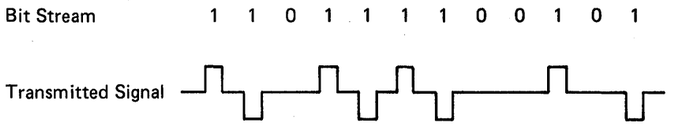
Data is transmitted serially-by-bit and serially-by-character over the digital data network. The network supplies the clock for clocking the data to and from the network.

Transmission Rates

For the Digital Data Service Adapter, the rates are 2400, 4800, or 9600 bps. Each rate is set by attaching jumpers to the Digital Data Service Adapter card in System/34. Paragraph 31-500 of the *5340 System Unit Maintenance Manual* shows where to attach these jumpers.

Transmission Signal

The signal transmitted from the Digital Data Service Adapter to the digital data network is a bipolar, return-to-zero signal. When transmitting a 0-bit, the signal is at 0 volts. However, when transmitting a 1-bit, the signal is either positive or negative, depending on the polarity of the last 1-bit transmitted. For example, if a negative 1-bit is transmitted, the next 1-bit will be positive as shown in the following figure.



Line Control Characters

The Digital Data Service Adapter uses three violation characters to control the digital data network. These characters are violation characters because two consecutively transmitted 1-bits have the same polarity (either negative or positive). The violation characters are idle, zero suppression, and out of service.

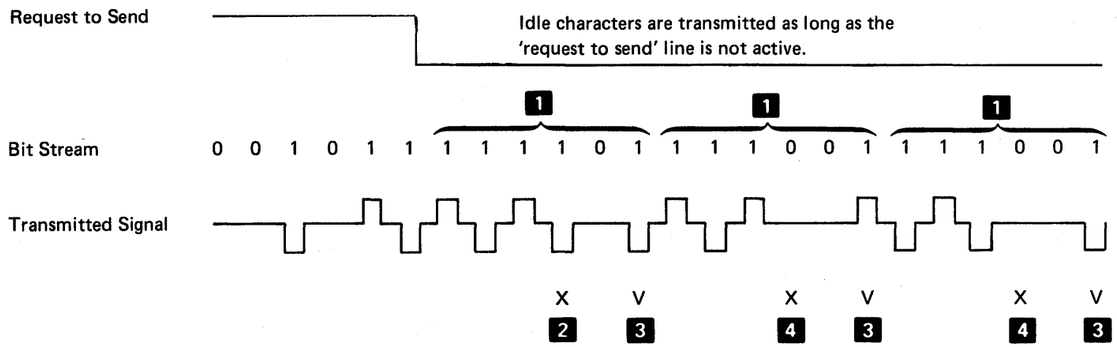
Idle

The idle character is generated and transmitted by the transmitting Digital Data Service Adapter when the 'request to send' interface line is not active from the communications adapter in System/34. This character informs the receiving Digital Data Service Adapter that the transmitting Digital Data Service Adapter is in an idle state.

The bit sequence for the idle character is 111X0V, where:

X = 0 or 1, and ensures an odd number of 1-bits since the last violation bit.

V = 1, a violation bit that ensures the same polarity as the preceding 1-bit.



1 Three transmitted idle characters.

2 First X-bit is opposite in polarity to the preceding 1-bit.

3 All V-bits are of the same polarity as the 1-bit that precedes them.

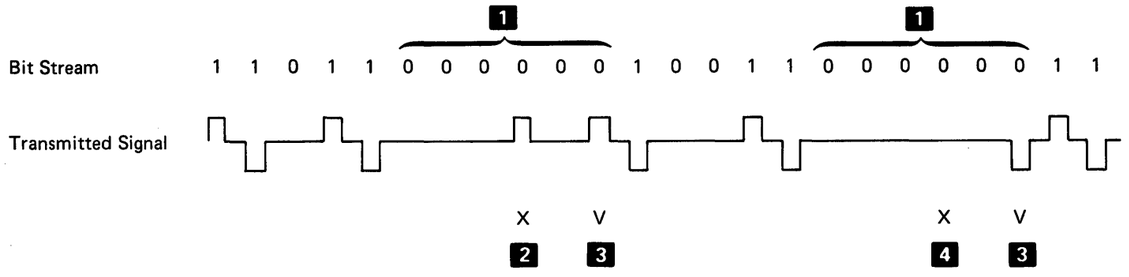
4 Both of these X-bits are at 0 volts to ensure an odd number of 1-bits since the last violation bit.

Zero Suppression

The zero suppression character is transmitted by the transmitting Digital Data Service Adapter to help maintain bit synchronization. This character ensures that at least one 1-bit gets transmitted when the data contains six consecutive 0-bits. Six consecutive 0-bits are transmitted as 000X0V, where:

X = 0 or 1, and ensures an odd number of 1-bits since the last violation bit.

V = 1, a violation bit that ensures the same polarity as the preceding 1-bit.



1 Zero suppression sequences.

2 First X-bit is opposite in polarity to the preceding 1-bit.

3 Both V-bits are of the same polarity as the 1-bit that precedes them.

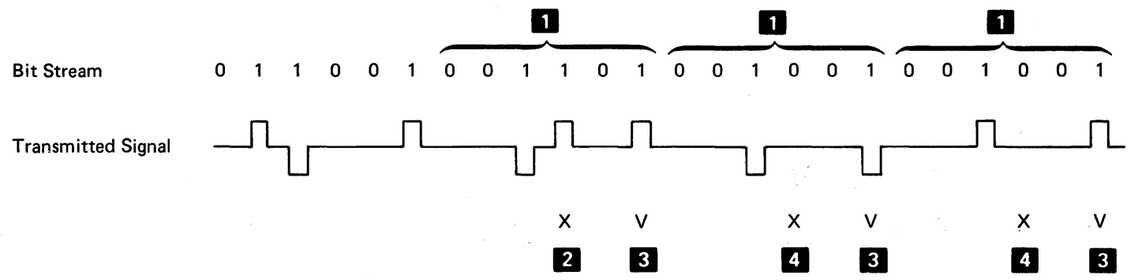
4 Second X-bit is at 0 volts to ensure an odd number of 1-bits since the last violation bit.

Out of Service

The out-of-service character is generated and transmitted by the digital data network. The character is sent to the receiving adapter and to the transmitting Digital Data Service Adapters to indicate a problem in the network. The bit sequence for the out-of-service character is 001X0V, where:

X = 0 or 1, and ensures an odd number of 1-bits since the last violation bit (see following figure).

V = 1, a violation bit that ensures the same polarity as the preceding 1-bit.



1 Out-of-service characters.

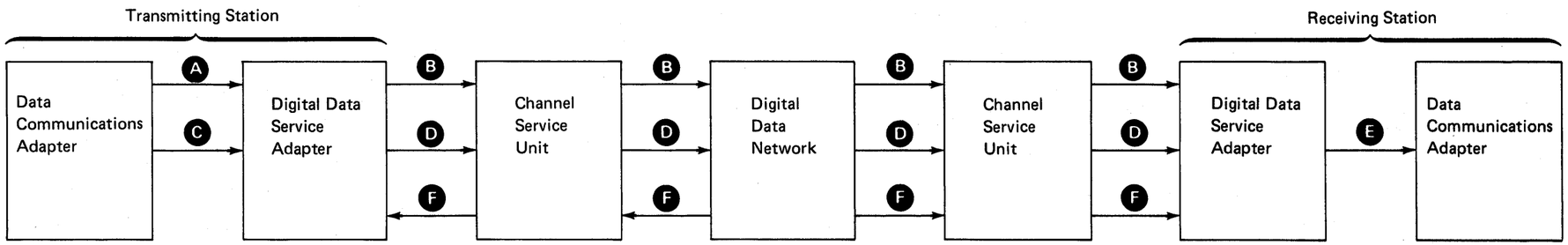
2 First X-bit is opposite in polarity to the preceding 1-bit.

3 All V-bits are of the same polarity as the 1-bit that precedes them.

4 Both of these X-bits are at 0 volts to ensure an odd number of 1-bits since the last violation bit.

Line Control Character Flow

The following figure shows the flow of the line control characters in a network. (A) and (B) are used for the idle character, (C), (D), and (E) are used for the zero suppression character, and (F) is used for the out-of-service character.



Idle

- **(A)** The 'request to send' line from the transmitting station is not active.
- **(B)** Idle characters are transmitted for as long as the 'request to send' line is not active to inform the receiving Digital Data Service Adapter that the transmitting station is in an idle state and cannot receive data.

Zero Suppression

- **(C)** The transmitted data contains six consecutive 0-bits.
- **(D)** The six consecutive 0-bits are suppressed and sent to the receiving Digital Data Service Adapter as 000X0V (see *Zero Suppression*).
- **(E)** The transmitted data (six 0-bits) is restored (from 000X0V to 000000).

Out of Service

- **(F)** An out-of-service character is sent to both Digital Data Service Adapters to inform them of problems in the network; no data can be transmitted.

Interface Lines

The following interface lines are between the data communications adapter and the Digital Data Service Adapter.

Transmit Data: Sent by the data communications adapter in sync with the clock. A mark (1-bit) is sent as a negative or positive signal, and a space (0-bit) is sent as 0 volts.

Receive Data: Activated by the Digital Data Service Adapter in response to the signal from the data communications network.

Request to Send: Activated by the data communications adapter to enable the Digital Data Service Adapter to enter transmit mode. If this line is not active, the Digital Data Service Adapter sends idle characters.

Clear to Send: Activated by the Digital Data Service Adapter in response to the 'request to send' line going active. The 'clear to send' line goes active in approximately a 20-bit interval after the 'request to send' line goes active. When the 'request to send' line goes not active, the 'clear to send' line goes not active in approximately one 1-bit interval.

When the 'clear to send' line is not active, the data communications adapter does not try to send any data to the Digital Data Service Adapter.

Carrier Detect: Activated by the Digital Data Service Adapter to indicate that the last 12-bit interval was valid data. The 'carrier detect' line goes not active if three consecutive idle or out-of-service characters are received, or if three consecutive characters containing all 0's are received.

When the 'carrier detect' line is not active, the 'receive data' line is held at a mark level (all 1's).

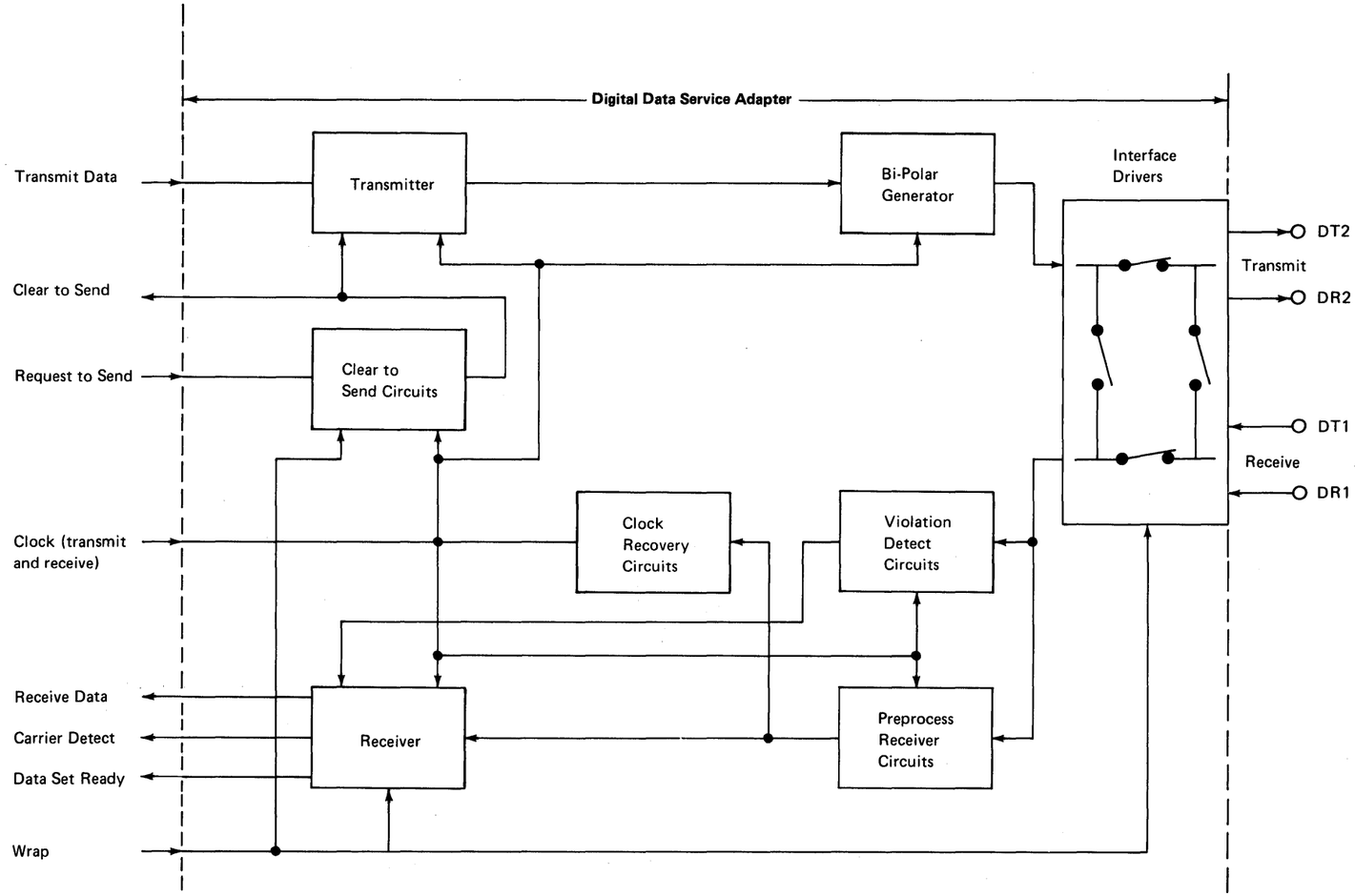
Data Set Ready: Activated by the Digital Data Service Adapter to indicate that valid data is on the communications line. The 'data set ready' line goes not active in an 18-bit interval if three consecutive out-of-service characters or three consecutive characters containing all 0's are received.

Receive Clock: Activated by the Digital Data Service Adapter to supply timing information to the data communications adapter for clocking received data.

Transmit Clock: Activated by the Digital Data Service Adapter to supply timing information to the data communications adapter for clocking transmitted data.

Wrap: Activated by the data communications adapter for local and remote error checking. For local checking, the transmitter's output in the Digital Data Service Adapter is looped back to the receiver. For remote checking, the signal from the communications line is looped back to the communications line (see the following figure).

CAUTION
Use the wrap test and turn power to the system on or off only when necessary. Up to 1 second of interference is transmitted when the Digital Data Service Adapter goes into wrap mode, or when power to the system is turned off. Up to 700 bit times of interference are transmitted when going out of wrap mode, or when turning on power to the system.



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