SY31-0458-6

IBM System/34
5340 System Unit
Theory Diagrams Manual

1 Introduction
2 Control Processor
3 Main Storage Processor
4 Interrupts and Cycle Steal Requests
5 Channel
6 Control Panels
7 62EH Disk Drive and Attachment
8 Diskette Drive and Attachment (Level 1)
9 5211 Printer Attachment
10 Attachment Controller 1
11 Work Station Attachment
12 Data Communications
13 62PC Disk Drive and Attachment
14 Diskette Drive and Attachment (Level 2)
15 3262 Printer Attachment
16 Attachment Controller 2

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5340 VOLUME A MAINTENANCE ANALYSIS PROCEDURES

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MAP'S 0000-1149

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0500-0584 POWER
0700-0782 5211 PRINTER CONTROLLER
0800-0842 3262 PRINTER CONTROLLER
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1000-1099 62PC DISK ATTACHMENT
1101-1149 WORK STATION CONTROLLER (PART 1)

5340 VOLUME A MAINTENANCE ANALYSIS PROCEDURES

S/N_____

MAP'S 1160-89XX

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S/N_____

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30-000 DATA COMMUNICATIONS (MLCA)
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45-000 INSTALLATION INSTRUCTIONS
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81-000 MAIN STORAGE PROCESSOR
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87-000 DISPLAY STATIONS
88-000 MATRIX PRINTERS
89-000 DATA COMMUNICATIONS
99-000 DIAGNOSTIC SERVICE GUIDE
PARTS CATALOG

5340 VOLUME C THEORY DIAGRAMS

S/N_____

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MAIN STORAGE PROCESSOR
INTERRUPTS AND CYCLE STEAL REQUESTS
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3262 PRINTER ATTACHMENT

5340 VOLUME D FIELD SERVICE LOGICS

S/N_____

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ACXXX PLUGCHARTS
ADXXX NET LISTS AND PIN LISTS
AEXXX SECOND LEVEL LOGIC DIAGRAMS
AFXXX VOLTAGE DISTRIBUTION
AYXXX LOGIC BLOCK SYMBOLOGY
CEXXX CE PANEL
CHXXX CHANNEL
CSXXX CONTROL STORAGE
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FBXXX DATA COMMUNICATION ATTACHMENT (MLCA)
FLXXX 72MD DSKT
FMXXX 72MD D.S.
FXXXX 72MD DRIVE
GXXXX DISK ATTACHMENT (GE, GP, AND GW PAGES)
HXXXX 62PC DISK ATTACHMENT (HA, HB, HC, HD, HE, AND HH PAGES)
MRXXX 1255 ATTACHMENT
MSXXX MSP STORAGE CTL
OPXXX OPERATOR PANEL
PAXXX DEVICE ATTACHMENTS FOR CHANNEL
PCXXX CONTROL PROCESSOR
PMXXX MAIN STORAGE PROCESSOR
PRXXX 5211 PRINTER ATTACHMENT
PSXXX PRINTER CONTROLLER
PTXXX 3262 PRINTER ATTACHMENT
PUXXX 3262 PRINTER ATTACHMENT
WCXXX WORK STATION (IDEOGRAPHIC)
WSXXX WORK STATION CONTROLLER
YAXXX POWER

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15 3262 Printer Attachment
16 Attachment Controller 2

Preface

This manual contains information about the operation of the IBM System/34. The manual is for the customer engineer who is troubleshooting a failure that the System/34 MAPs (maintenance analysis procedures) failed to isolate, or for one who wishes to improve his knowledge of System/34 operation. Each major system function is described in a separate section, as listed in the *Contents*.

Customer engineers using this manual are assumed to have been trained on System/34 as described in the *IBM System/34 Technical Service Letter*.

There are several CAUTION messages in this manual. You can use the blank lines below each message to translate the message into your own words.

Note: This manual follows the convention that *he* means *he or she*.

Related Publications

- *IBM System/34 5340 System Unit Maintenance Manual*, SY31-0457
- *IBM System/34 Control Storage Logic Manual*, SY31-0562
- *IBM System/34 Functions Reference Manual*, SA21-9243
- *IBM System/34 System Data Areas and Diagnostic Aids Manual*, LY21-0049
- *IBM System/34 Program Products and Physical Setup, Installation and Modification Reference Manual*, SC21-7689
- *IBM System/34 System Support Program Logic Manual: System*, LY21-0050
- *IBM 5211 Printer Maintenance Information*
- *IBM 3262 Printer Maintenance Information*
- *IBM System/34 Multiline Communications Adapter Theory Diagrams Manual*, SY31-0627

For systems that use the ideographic work station display, see the following manuals:

- *IBM System/34 5340 System Unit Ideographic Feature Theory Diagrams Manual Supplement*, SA09-1801
- *IBM System/34 5340 System Unit Ideographic Feature Maintenance Manual Supplement*, SA09-1014
- *IBM System/34 Functions Reference Ideographic Feature Supplement (5255 Display Station Model 1)*, SA09-1632
- *IBM System/34 Functions Reference Ideographic Feature Supplement (5255 Display Station Model 2)*, SA09-1633

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This is a major revision of, and makes obsolete, SY31-0458-5. Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change or addition. Changes are periodically made to the information herein; these changes will be reported in technical newsletters or in new editions of this publication.

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APPENDIX A. DISKETTE FORMATS A-1

GLOSSARY G-1

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List of Abbreviations and Acronyms

μA	microampere
μs	microsecond
A	add to register; AND gate
AA	automatic answering
AC	alternating current
ACE	action control element
ACK	acknowledge character
ACK0	even acknowledgment
ACK1	odd acknowledgment
ACR	adapter control register; address compare register; abandon call and retry
ACTB	alternating current terminal block
ACTLU	activate logical unit
ACTPU	activate physical unit
ACW	action control word
ACYR	add registers with carry
add/addr/ adr	address
AEQ/AEL	automatic equalizer
AFA	active format on area
AGC	automatic gain control
AI	add immediate
ALC	add logical characters
ALU	arithmetic and logic unit
AM	address mark
amp	ampere
ANS	auto network shutdown
ANSC	auto network shutdown complete
AOI	and or invert
AR	add registers; amplifier symbol
AR-DIFF	differentiator to amplifier
ARR	address recall register
ASCII	American National Standard Code for Information Interchange
asm	assembly
ASR	adapter status register
assn	assigned
ATR	address translation register
aux	auxiliary
AZ	add zoned decimal
B	branch
BAL	branch and link
BC	branch on condition; byte counter
BCC	block check character
BCD	binary-coded decimal
bfr/buf	buffer
BH	behind home
BIND	bind session
BIU	basic information unit
blk	block
BLU	basic link unit
BMR	backup mode register
BPC	block processor clock
bps	bits per second
BR	bit ring
BSC	binary synchronous communications
BSCA	binary synchronous communications adapter
BSCA TST	online test for BSCA
BTU	basic transmission unit
C	Celsius; clock pulse
CA	common adapter
CADUCEE	data communications network in France
CANCEL	cancel
CB	circuit breaker
CBI	command bus in
CBO	command bus out
CBS	data coupler for modem with automatic answering
CCB	channel command bus
CCBO	controller command bus out
CCITT	Consultative Committee on International Telegraphy and Telephony
CCR	configuration control register
CCT	coupler cut through
CD	carrier detect
CDBI	controller data bus in
CDBO	controller data bus out
CDSTL	connect data set to line
CDT	data access arrangement for manual calling
CE	customer engineer
chan	channel
CHK	check
CI	compare immediate
CKB	check byte
CLC	compare logical characters
CLEAR	clear
CLI	compare logical immediate
clk	clock
cm	centimeter
cmd	command
CMDR	command reject
CMR	control mode register
cnt	count
cntr	counter
COD	change of direction
COMM	communications
COMMST	communications test
COMP	compare
COMTB	communications terminal block
CONS	console
COR	control output register
CP	control processor
CPMGR	connection point manager
CPU	processing unit
CR	crystal rectifier
CRC	cyclic redundancy check
CRT	cathode-ray tube
CS	control storage; cycle steal
CSACK	cycle steal acknowledge
CSCD	clear to send/carrier detect
CSILSW	control storage interrupt level status word
CSIPL	control storage initial program load
CSP2	clock sync phase 2
CSP3	clock sync phase 3
CSX	clock trigger for MSP
CSY	clock trigger for MSP
CS1 P2	clock sync 1, phase 2
CS1 P3	clock sync 1, phase 3
CS2 P2	clock sync 2, phase 2
CS2 P3	clock sync 2, phase 3
CTL/cntl/ctrl	control
CTS	clear to send
cyc	cycle
DA	data modem ready; device address
DAA	data access arrangement
DAC	digital-to-analog converter
DACTLU	de-activate logical unit

DACTPU	de-activate physical unit
DAF	destination address field
DAR	data address register
dB	decibel
dBm	decibels per meter
DBI	data bus in
DBO	data bus out
DC	direct current
dcd	decode; decoder
DCE	data communications equipment
DCF	data count field
DCP	diagnostic control program
DCR	diagnostic control register
DDSA	Digital Data Service Adapter
DE	device end
DEC	decrement register by 1
demod	demodulator
det	detector
diag	diagnostic
DISC	mandatory disconnect
disp	displacement
div	division
dk	disk
DLC	data link control
DLE	data link escape
DLO	data line occupied
dly	delay
DM	disconnected mode
DPLY	display
DPSK	differential phase shift keying
DR	data ring; driver
DRAR	driver/receiver activity register
DS	data set
DSC	distant station connected
DSF	data storage facility
dskt	diskette
DSR	data set ready
DT	data tip
DTE	data terminal equipment
DTR	data terminal ready
EBCDIC	extended binary-coded decimal interchange code
EC	engineering change
ECC	emitter column counter
ED	edit
EFI	expedited flow indicator
EIA	Electronic Industries Association
EIR	enable interrupt register
ENQ	enquiry
EOF	end of file
EOT	end of transmission
ERAP	error recording analysis procedure
ERP	error recovery procedure
ESC	extended storage control
ESD	external symbol dictionary
ETB	end of text block
ETX	end of text
EWG	end write gap
ext	extended
FET	field effect transistor
FF	flip-flop
FID	format identification field
FL	flip latch
FM	frequency modulation
fms	frames
FRU	field-replaceable unit
FSK	frequency shift keying
FSL	field service logic
func/funct	function
GB	guard band
gen	generator
GND	ground
GT/gt	gate
H/L	high/low
HBN	hexadecimal branch numeric
HBZ	hexadecimal branch zone
HCP	head connector point
hd	head
hex	hexadecimal
hh:mm:ss	hour:minute:second
Hz	hertz
I-fetch	instruction fetch
I/O	input/output
IAR	instruction address register
ID	identification; identifier
IDB	identification buffer
IFP	internal fire pulse
IL	interrupt level
ILBB	interrupt level backup byte
IMPSS	impression control singleshot
INC	increment register by 1
incr	increment
INITC	initialization complete
INSN/inst	instruction
int	internal
intrpt/irpt	interrupt
IOB	input/output block
IOCH	input/output control handler
IOCL	I/O control load
IOCS	I/O control sense
IOL	I/O load
IOS	input/output supervisor; I/O sense
IPL	initial program load
IPO	immediate power off
IR	information retrieval
ITB	intermediate text block
ITC	insert and test characters
JC	jump on condition
JCB	job control block
JCY	jump on carry
JE	jump on equal
JFLG	jump on flag
JH	jump on high
JIO	jump on I/O condition
JL	jump on low
JM	jump on mixed
JN	jump on negative
JNE	jump on not equal
JNH	jump on not high
JNL	jump on not low
JNN	jump on not negative
JNP	jump on not positive
JNZ	jump on not zero
JO	jump on all ones
JP	jump on positive
JSR	jump on service request
JZ	jump on zero
K	1,024
Kana	Katakana
kbd	keyboard
kB	kilobyte
kHz	kilohertz
L	load direct to control storage; load register
LA	load address
LA1	logical/arithmetic 1
LA2	logical/arithmetic 2
LC	load from control storage; link control
LCRR	length count recall register
LED	light-emitting diode
LI	load immediate
LIO	load input/output
LL	leased line

LLB	local loop back test
LM	load from main storage
LPDA	line problem determination aid
LPDL	least positive down level
lpi	lines per inch
LPMR	load program mode register
LPUL	least positive up level
LRC	longitudinal redundancy check
LSAR	load/sense address register
LSID	local session identifier
LSR	local storage register
lth	latch
LTT	loop transmit test
LU	logical unit
LUSTAT	logical unit status
LZ	landing zone
M (mega)	million
mA	milliampere
MAB	microaddress backup register
MAP	maintenance analysis procedure
MAR	microaddress register
MB	megabyte
MC	machine check; missing clock pulse; motor connector
MCI	machine check interruption
MCR	magnetic character reader
MDI	MAP diagnostic integration
MFM	modified frequency modulation
MHz	megahertz
MIC	message identification code
MICR	magnetic ink character recognition
MLCA	multiline communications adapter
mm	millimeter
mod	modifier
modem	modulator/demodulator
MOR	micro-operation register
MPDL	most positive down level
MPF	mapping field
MPL	control processor load; main program level
MPLF	control processor load function
MPLS	control processor load special
MPS	control processor sense
MPUL	most positive up level
MPXPO	multiplexer port out
MRJE	multi-leaving remote job entry
MS	main storage
ms	millisecond
MSAR	main storage address register
MSIPL	main storage initial program load
MSP	main storage processor
MSR	modem status register
MST	monolithic storage technology
MTR	microcode trouble report
mV	millivolt
MVC	move characters
MVI	move logical immediate
MVR	move local storage register
MVX	move hexadecimal character
MZN	move zone to numeric
MZZ	move zone to zone
N	inverter symbol
N/C	normally closed
N/O	normally open
NAK	negative acknowledge character
NAU	network addressable unit
NCR	AND complement
NDM	normal disconnect mode
NR	AND register
NRF	no record found
NRM	normal response mode
NRZI	zeros complemented transition coding
ns	nanosecond
NSA	nonsequenced acknowledgment
NTF	no trouble found
O/C	over current
OAF	origin address field
OCD	off-chip driver
OCR	OR complement
OE	exclusive or
OH	off hook
op	operand; operation
osc	oscillator
P	parity; position pulse
P/F	poll/final
PAD	fill character
PC	parity check; path control
PCB	printed circuit board
PCR	processor condition register
PDTB	power distribution terminal board
PFN	print fire number
PG	parity generate; parity generator
PH	polarity hold
PIU	path information unit
PLA	programmable logic array
PLB	power logic board
PLO	phase lock oscillator
PMR	program mode register
PND	present next digit
POR	power on reset
pos	position
PP	parity predict; print position; program product
prc	processor
preamp	preamplifier
PREPS	prepare to switch
PREV	previous
PROC	processor
prtr	printer
PSN	public switched network
PSR	program status register
PSS	print subscans
PTT	Post, Telephone, and Telegraph
PTX	phototransistor
PU	physical unit
PWI	power indicator
PWR	power
pwrd	powered
R/C	resistor/capacitor
R/W	read/write
RB	request block
rcv	receive
rd	read
RDCH	read from control storage high
RDCL	read from control storage low
RDM	read from main storage
recal	recalibrate
reg	register
req	request
REQMS	request maintenance statistics error log
REQTEST	request test
resp	response
RETRN	return
RFS	ready for sending
RH	request/response header

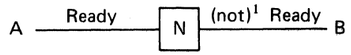
RI	ring indicate
RIB	request indicator byte
RLB	remote loop back test
RLD	relocation list directory
RMPR	sense main storage processor register
RNR	receive not ready
ROS	read-only storage
rpm	revolutions per minute
RQR	request recovery
RR	receive ready
RSHUTD	request shutdown
RST	reset
RT	receive test
RTS	request to send
RU	request/response unit
RVI	reverse interrupt
s	second
S/D	serializer/deserializer
SAR	storage address register
SBAR	storage buffer address register
SBF	set bits off; set bits off masked
SBI	system bus in
SBN	set bits on; set bits on masked
SBO	system bus out
SC	sequence counter
SCS	SNA character string
SCSID	sense cycle steal identification
SCYR	subtract with borrow
SDLC	synchronous data link control
SDR	storage data register
SDT	start data traffic
sel	select; selector
SERDES	serializer/deserializer
SG	signal ground
SH	switch hook
SI	subtract immediate
SIGNAL	signal
SILSB	sense interrupt level status byte
SILSW	system interrupt level status word
SIO	start input/output
SLC	subtract logical characters
SLL	shift left logical
SLLD	shift left logical double
SLT	solid logic technology
SNA	systems network architecture
SNBU	switched network backup (standby)
SNF	sequence number field
SNRM	set normal response mode
SNS	sense input/output
SOH	start of header
SR	subtract register
SRL	shift right logical
SRLD	shift right logical double
SS	sequential sector; singleshot
SSCP	system services control point
SSP	System Support Program Product
ST	store register; self test
STC	store to control storage
STG/STOR	storage
STM	store to main storage
STSN	set and test sequence numbers
STX	start of text
SVC	supervisor call
SW	switch
SWG	switch write gap
SWICOM	switch complete
SYN	synchronous idle
sync	synchronize; synchronization
SYS	system
SZ	subtract zoned decimal
TB	terminal block
TBF	test bits off masked
TBN	test bits on masked
TCB	task control block
TD	time delay
TH	thermal; transmission header
THP	test header point
TM	test mask
TP	test point
TPA	test point A
TPB	test point B
TP1	test point 1
TP2	test point 2
TQE	timer queue element
TR/tgr	trigger
trans	transfer
TRB	timer request block
TTD	temporary text delay
TU	test unit
TUB	terminal unit block
TWA	task work area
T1,T2,T3,T4	test 1, 2, 3, 4
UDT	unit definition table
UNBIND	unbind session
V	volts
Vac	volts, AC
Vdc	volts, DC
vert	vertical
VFL	velocity follow latch
VFO	variable frequency oscillator
VRC	vertical redundancy check
VTL	vendor transistor logic
VTOC	volume table of content
WACK	wait before transmit (positive acknowledgment)
WC	write clock
WMPR	load main storage processor register
WR	work register
wr/wrt	write
WSDM	work station data management
WSIOCH	work station input/output control handler
WT	World Trade
WTCH	write to control storage high
WTCL	write to control storage low
WTM	write to main storage
XDLE	transparent data link escape
XENQ	transparent block cancel
XETB	transparent end-of-text block
XETX	transparent end of text
xfer	transfer
XID	exchange station ID
XITB	transparent intermediate text block
xmt	transmit
XR	exclusive OR
XSTX	transparent start of text
XSYN	transparent synchronous idle
XTTD	transparent temporary text delay
yymmdd	year-month-day
ZAR	zero and add to register
ZAZ	zero and add zoned
2w	two-wire connection
4w	four-wire connection

Legend

This section describes the symbols and conventions used in System/34 maintenance documentation.

Symbols and Conventions Used in Positive-Logic Diagrams and in Field Service Logics (FSLs)

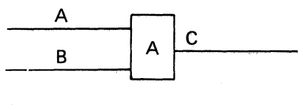
Inverter (N)



A must be active for B to be not active.

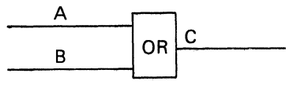
[1] Parentheses are used to enclose words that are not part of an actual line name; they are put there to help you better understand the purpose of a signal.

AND (A)



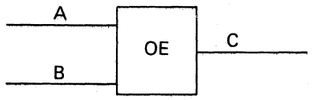
Both A and B must be active for C to be active.

OR



Either A or B must be active for C to be active.

Exclusive OR (OE)

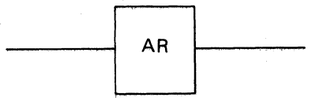


Either A or B, but not both, must be active for C to be active.

If A and B are both active, C is not active.

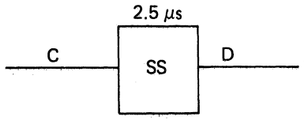
If A and B are both not active, C is not active.

Amplifier (AR)



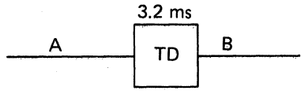
Increases the amplitude of a signal.

Singleshot (SS)



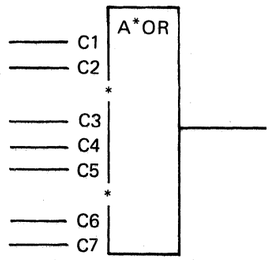
A pulse on C causes a 2.5-microsecond waveshape on D. The time that D is active (2.5 μs) is written above the symbol.

Time Delay (TD or DLY)



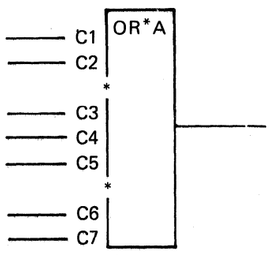
When A changes state, B changes state 3.2 milliseconds later. The length of the delay (3.2 ms) is written above the symbol.

AND-OR



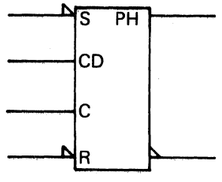
This symbol shows an OR circuit with three AND circuits as inputs. The AND circuits are separated by asterisks (*). An asterisk is a special character that separates groups of inputs in field service logics (FSLs).

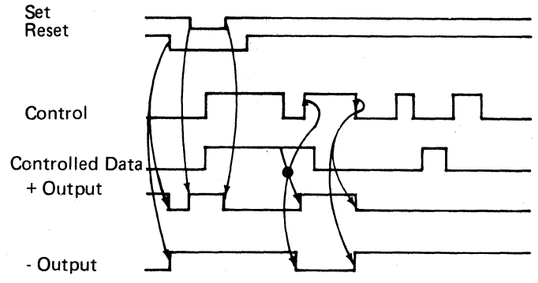
OR-AND



This symbol shows an AND circuit with three OR circuits as inputs. The OR circuits are separated by asterisks (*).

Polarity Hold (PH)

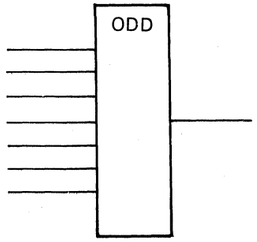




This is a polarity hold circuit with four possible inputs. When the 'control' line (C) becomes active at the same time the 'controlled data' line (CD) is active, both output lines of the PH become active and stay active for the length of the 'control' line (C).

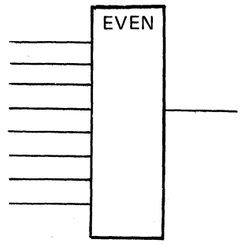
The 'set' line (S), when active, sets the '+ output' line of the PH. The 'reset' line (R), when active, resets both output lines of the PH.

Odd Count (ODD)



The output of the odd-count circuit is active only when an odd number of inputs is active.

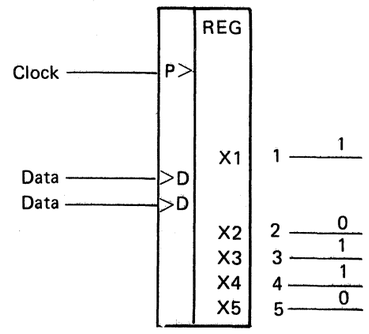
Even Count (EVEN)



The output of the even-count circuit is active only when an even number of inputs is active.

Symbols and Conventions Used in Field Service Logics (FSLs)

Shift Register (REG)



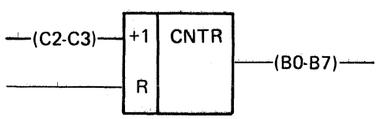
Register Trigger	X1	X2	X3	X4	X5
Initial State	1	0	1	1	0
1st Shift (D = 0)	0	1	0	1	1
2nd Shift (D = 1)	1	0	1	0	1
3rd Shift (D = 1)	1	1	0	1	0

This is an example of a shift down register. In a shift down register, the contents of the high-order position (X1) are shifted into the next lower position (X2), and so on, each time there is a clock pulse.

The greater-than symbol (>) identifies a shift down register; a less-than symbol (<) identifies a shift up register. The letter P on the 'clock' line indicates that shifting occurs on the rise of a positive clock pulse.

If either 'data' line (D) is active at shift time, the high-order position of the shift register is set to 1. If both 'data' lines (D) are not active at shift time, the high-order position of the shift register is set to 0.

Counter (CNTR)

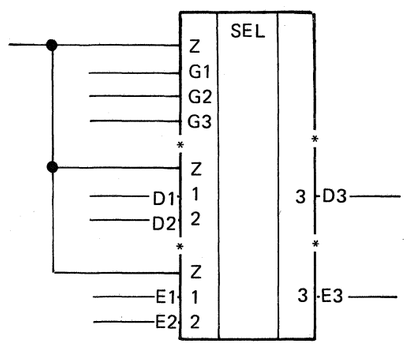


This example of a counter shows two input lines (C2 and C3) and eight output lines (B0 through B7).

The plus symbol (+) indicates that the contents of the counter are increased by 1 each time C2 or C3 becomes active. A minus symbol (-) indicates that the contents of the counter are decreased each time C2 or C3 becomes active.

When R is active, the counter is reset.

Selector (SEL)



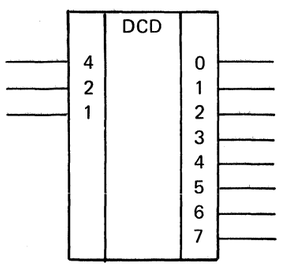
A selector is a gating circuit. The upper part of the selector symbol contains the gates (G1, G2, G3), and the lower part contains the gated data lines (D1, D2, E1, E2).

In this example, gate 1 (G1) controls input data lines D1 and E1; gate 2 (G2) controls lines D2 and E2. Gate 3 (G3) controls output data lines D3 and E3.

Thus, for data to pass through the selector, one of the input gates (G1 or G2) must be active at the same time output gate G3 is active.

This example of a selector also has a Z input. If the Z input is active at the same time gate G3 is active, output lines D3 and E3 are both active.

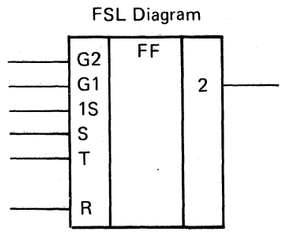
Decoder (DCD)



This example of a decoder converts the output from a 3-position binary counter into 1 of 8 decimal digits. The value of the active output line equals the sum of the active input lines. For example, when input lines 4 and 1 are active, output line 5 is active.

Flip-Flop (FF)

FSL Diagram

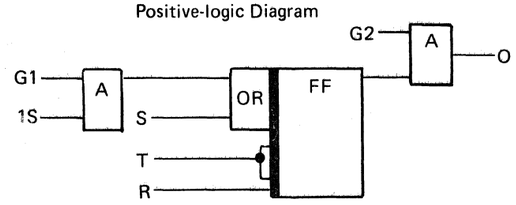


This example shows a flip-flop as it would appear in an FSL diagram, and the way the same trigger would appear in a positive-logic diagram. In this example, there are two sets (S and 1S) and one reset (R).

The trigger is turned on when S is active, or when 1S and gate 1 (G1) are active at the same time. Gate 2 (G2) must also be active for the output (O) to be active.

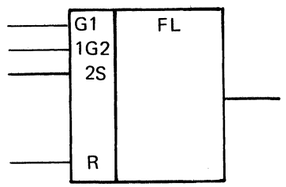
The toggle input (T) reverses the state of the trigger, turning the trigger off if it is on, or turning the trigger on if it is off. When active, the reset input (R) resets the trigger.

Positive-logic Diagram



Flip Latch (FL)

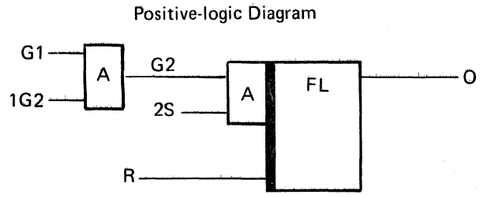
FSL Diagram



This example shows a flip latch as it would appear in an FSL diagram, and the way the same latch would appear in a positive-logic diagram. In this example, gate 1 (G1) must be active when 1G2 is active in order for gate 2 (G2) to be active.

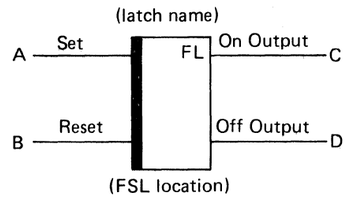
This latch is turned on if G2 is active and the set line (2S) becomes active. When active, the reset input (R) resets the latch. G2 is not shown in the FSL diagram.

Positive-logic Diagram



Symbols and Conventions Used in Positive-Logic Diagrams

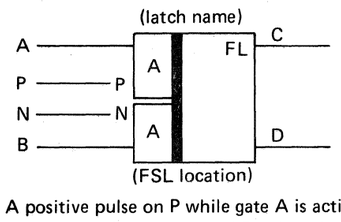
Flip Latch (FL)



If A becomes active, the latch is set to the on state (C is active and D is inactive).

If B becomes active, the latch is set to the off state (D is active and C is inactive).

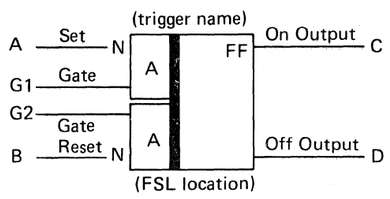
Flip Latch (FL)



A positive pulse on P while gate A is active sets the latch to the on state (C is active and D is inactive).

A negative pulse on N while gate B is active sets the latch to the off state (D is active and C is inactive).

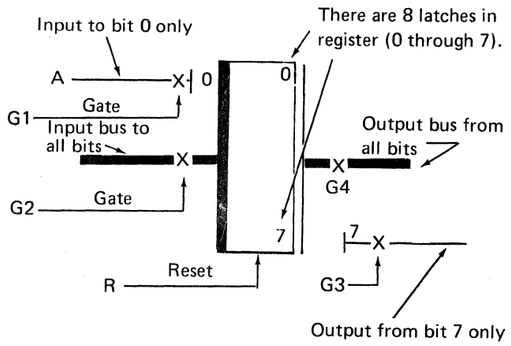
Flip-Flop (FF)



If A is active while gate G1 is active, the latch is set to the on state (C is active and D is inactive).

If B is active while gate G2 is active, the latch is set to the off state (D is active and C is inactive).

Register (Reg)



If gate G1 becomes active while input A is active, latch 0 is set to the on state (latches 1 through 7 do not change state).

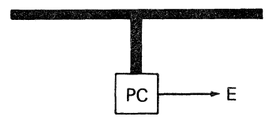
If gate G2 becomes active, latches 0 through 7 are set to the on state for each input bus line that is active.

If gate G3 is active, only the output from latch 7 is gated out.

If gate G4 is active, the output from latches 0 through 7 is gated out.

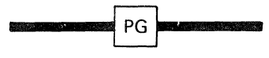
A pulse on the 'reset' line (R) resets all latches to the 0 (off) state.

Parity Check (PC)



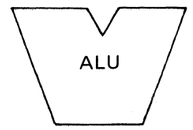
Checks the parity of a signal bus. If parity is not correct, line E becomes active to indicate an error.

Parity Generator (PG)



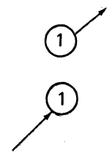
Generates the correct parity for a signal bus.

Arithmetic and Logic Unit (ALU)

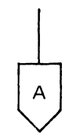


Performs arithmetic and logic operations in a processor.

On-Page Connectors

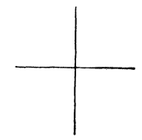


Off-Page Connector



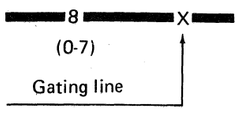
Electrical Connection

No Electrical Connection



Bus Containing 8 Lines

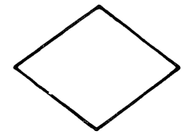
(bits 0 through 7)



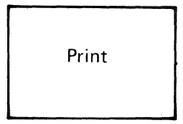
Boolean Algebra Symbols

- • In a line name means AND
- + In a line name means OR

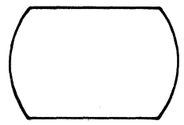
Symbols Used in Flowcharts



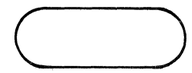
Decision block on a flowchart (asks a question)



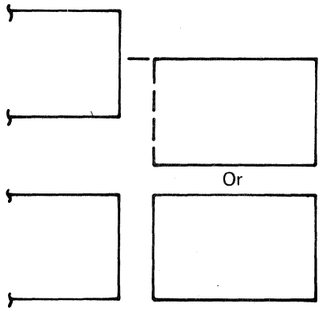
Processing block on a flowchart



Keying operation on a flowchart



Terminal on a flowchart



Note on a flowchart

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