IBM Maintenance Library

5203 Printer Attachment for System/3: Diagrams

SY31-0240-1

Preface

The diagrams in this manual are organized by operation. Thus, the details of machine operations are presented in operational flowcharts, most of which are *two-level*. The general flow path of the two-level charts (heavy line) shows the major objectives of an operation or instruction. Detailed flow paths of major objectives are located to the right of the general flow path.

Positive-logic diagrams support the operational flowcharts. They show logical circuit operation without regard to signal levels. Most of the logic diagrams in this manual are not block-for-block representations of Automated Logic Diagrams. Rather, only blocks necessary for a logical understanding of the operation are shown.

- The *IBM Maintenance Library 5203 Printer Attachment for System/3: Theory of Operation*, SY31-0245.
- The *IBM 5203 Printer, Field Engineering Theory of Operation Manual*, SY33-1045.
- The *IBM 5203 Printer, Field Engineering Maintenance Manual*, SY33-1046.
- The *IBM 5410 Processing Unit, Field Engineering Theory of Operation Manual*, SY31-0207.
- The *IBM Maintenance Library 5410 Processing Unit for System/3: Diagrams*, SY31-0202.
- The *IBM 5410 Processing Unit, Field Engineering Maintenance Manual*, SY31-0244.

Second Edition (May 1971)

This is a major revision of and obsoletes SY31-0240-0.

Changes are continually made to the specifications herein; any such change will be reported in subsequent revisions or technical newsletters.

A Reader's Comment Form is at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, Product Publications, Department 245, Rochester, Minnesota 55901.

Abbreviations

ALU	Arithmetic Logic Unit
APL	Advance Program Level
CC	Character Counter
CPU	Processing Unit
DA	Device Address
DBI	Data Bus In
DBO	Data Bus Out
EOL	End of Line
HAR	Hammer Address Register
INTF	Interface
I/O	Input/Output
LIO	Load Input/Output
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LPM	Lines Per Minute
LSR	Local Store Register
M	Mechanical Position
MAP	Maintenance Analysis Procedure
MST	Monolithic Systems Technology
PC	Print Cycle Steal
POR	Power On Reset
PSS	Print Subscan
SDR	Storage Data Register
SIO	Start Input/Output
SLD	Solid Logic Dense
SNS	Sense
SS	Single Shot
TIO	Test Input/Output
TP	Test Point
UCS	Universal Character Set
UPC	Unprintable Character
WO	With Out

Contents

Features

Special features available for the IBM 5203 Printer Attachment are:

- Dual Feed Carriage
- 120 Print Positions
- 132 Print Positions
- 200 LPM Throughput
- 300 LPM Throughput
- Universal Character Set (UCS)

All FF (Field Feature) B/Ms for the 5203 attachment must be installed along with the concurrent 5203 printer FF B/M.

DUAL FEED CARRIAGE

This feature provides simultaneous feeding of two non-overlapping sets of forms. The left carriage is standard, and the right carriage can be field installed.

Each carriage can move independently of the other. A separate SIO instruction is required for each carriage. Dual circuitry is provided for in the attachment FF B/M by adding two MST cards. These cards include an additional:

1. Carriage space-skip register
2. Carriage forms length register
3. Carriage line counter
4. Carriage space counter
5. Carriage moving counter
6. Carriage manual controls
7. Space check counter
8. Emitter generate counter

120 AND 132 PRINT POSITIONS

The standard 96 print positions can be increased to 120 or 132 print positions by installing the 120 or 132 print position feature B/M. The print operation in the attachment remains the same, except for two functions:

1. Inhibit cycle steal 2 and 3 after the hammer address register decodes the last existent hammer address in any subscan. This prevents CPU cycle steals because they are not needed.
2. Degate the hammer echo samples when the hammer address register decodes the first nonexistent hammer address. Hammer echo checks are not needed for nonexistent hammer positions.

200 LPM

The 5203 throughput can be changed from 100 LPM to 200 LPM, or from 200 LPM to 100 LPM, by changing a jumper wire and the incrementer cam.

The M position counter operates differently for 200 line per minute machines than for 100 line per minute machines. The 200 LPM machines print in both directions, whereas, the 100 LPM machines print in one direction only. Alternate lines start printing in either M1 or M4. The M position counter steps in both directions (M1, M2, M3, M4, M4, M3, M2, M1, M1, M2, etc.).

300 LPM

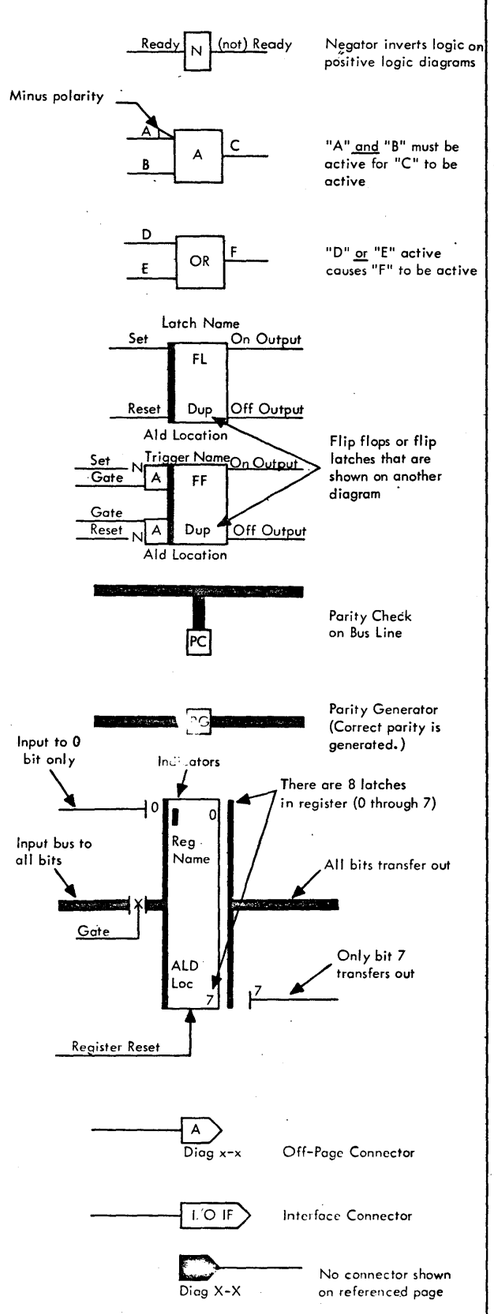
The 5203 throughput can be increased to 300 LPM by installing the 300 LPM Field Feature Bills of Material on both the printer and attachment.

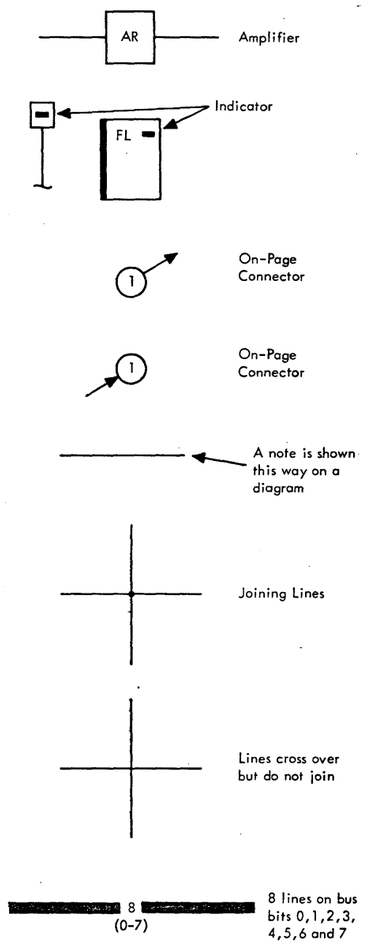
UNIVERSAL CHARACTER SET

Any character set with more than 48 different characters is defined as a Universal Character set (UCS). The UCS feature expands the 48-character set to a character set with 49 to 120 different characters.

An MST card located at B1 L4 of CPU controls the UCS in the 5203 attachment. The 5203 has an additional emitter (UCS emitter) and microswitch installed. The microswitch is activated by a stud on the UCS chain cartridge.

Legend



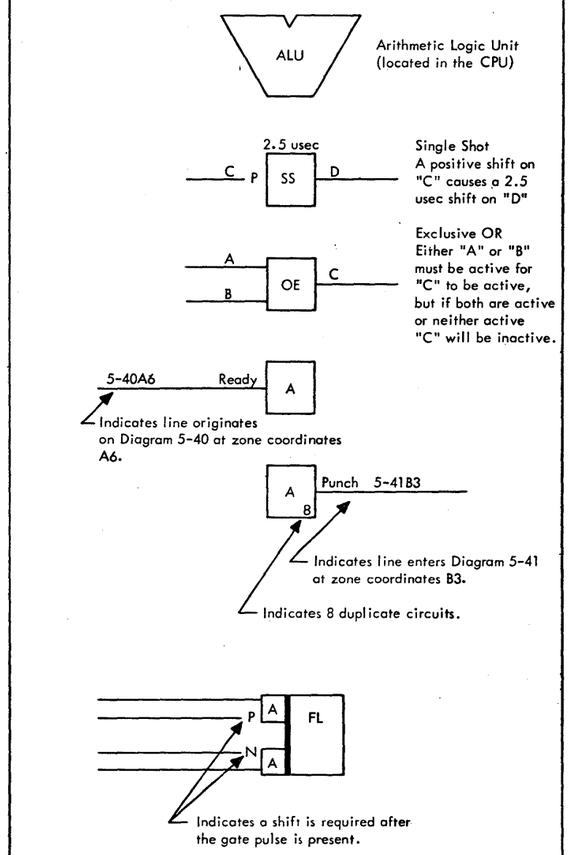


Boolean Algebra Symbols

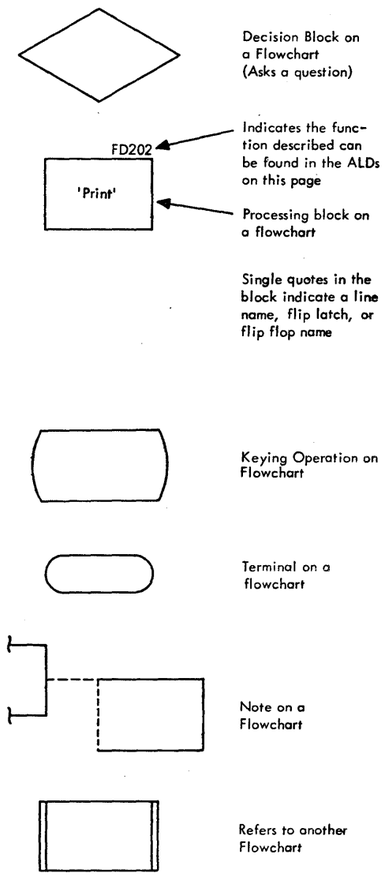
• In a line name means "And"

+ In a line name means "Or"

(xx - - - x) Indicates a line name that does not exist as an actual ALD name, but used to better explain the function of a line or block



* Indicates a point that can be probed on back-panel pins.



Clock denotes CPU clock

Figure 1-100 Diagnostic Techniques

A

B

This error condition caused by:
1. Any hammer on check
2. Hammer echo check
3. Increment or failure check

D (chain or incr sync ck)
Diag 2-120

C

G Hmr + Incr Failure Ck
Diag 2-130

B Forms + Thermal C...
Diag 2-110

This error condition caused by:
1. Carriage sync check
2. Carriage space check
3. Hmr unit thermal overload
4. Forms jam at printer

D

E

CHECK LIGHT

The check light is turned on by the system when conditions that impair print operations are detected. The printer is not ready when the check light is on. Any one, or all, of the following conditions turn on the check light:

- Carriage check.
- Forms jam (in the tractors).
- Incrementor failure check (cam clutch blocks).
- Parity check. ⎫
- Hammer echo check. ⎬ Print Check
- Any-hammer-on check. ⎭
- Chain sync check.
- Thermal overload check.

Note: Depending on the system to which the 5203 is attached, not all of these checks are necessarily implemented. For details, see the appropriate Systems Reference Library literature.

The checks are reset either manually via system reset key or via program-initiated tests. The thermal overload condition requires customer engineer attention.

OR
FP341

Check Error

EXIT
WP111

Check Light

5203

Diagram 2-100. Printer Checklight

2 3 4 5 6 7 8 9

A

B

C

D

E

'INTF FORMS JAM' LINE

This line has down level when the forms jam below the print line.

I/O IF Printer — Intf Forms Jam

Forms Jam

A forms jam below the print line or the ribbon shield is not closed.

FL FP342

Start Res + Sys Ck Res or POR

Reset Carr Ck

OR

Forms Jam → A, Diag 4-030

Forms Jam T.P. → F, Diag 4-040

B — (carr sync or space ck), Diag 2-140

OR FP342 — Forms + Thermal Ck → B, Diag 2-100

Printer hammer unit temperature too high.

I/O IF Printer — Intf Hmr Unit Thermo Overl

Hmr Unit Thermo Overl → C, Diag 4-030 4-040

C — Any Hammer On Ck, Diag 2-130

E — Hammer Echo Ck, Diag 2-130

A — Incr Failure Ck, Diag 2-130

Any Hammer On Ck

Hammer Echo Ck

Start Res + Sys Ck Res

POR

OR FL FP341

Not Print Latch

Hammer Check

Common Interlock

A OR

OR FP342 — Drop +60 Volts — CV FP211 — Intf Drop +60v — I/O IF Printer

'INTF HMR UNIT THERMO OVERL' LINE

This line has down level when the temperature in the hammer unit exceeds 134°F (57°C). The thermal-overload condition causes the CPU to raise the 'intf drop +60V' line.

Note: The thermosensor above the printer electronics board (PEB) is in series with other thermosensors in the system, and sequences system power down in cases of overtemperature.

'INTF DROP +60V' LINE

The CPU activates this line in cases of error (such as hammer drivers failing to reset) and when the rear unit interlock switch or the chute switch operates. The 60V contactor in the printer control box (PCB) then drops, causing the chain motor relay to be de-energized.

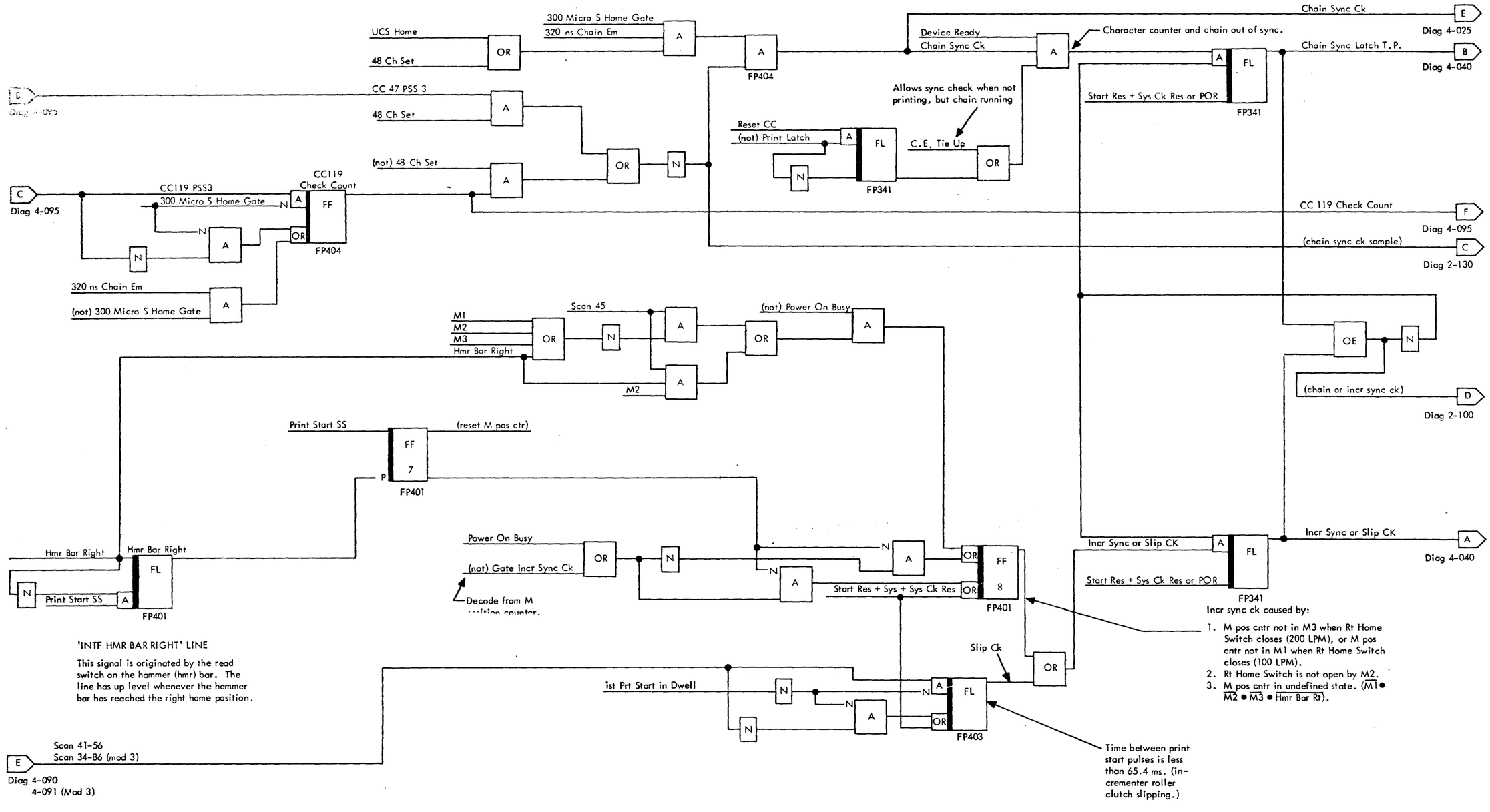


Diagram 2-120. Chain Sync Check and Increment Sync Check

2 3 4 5 6 7 8 9

A B C D E

'INTF ANY HAMMER ON' LINE

This line has up level whenever one or more hammer drivers are turned on; the signal is generated by the hammer current sense circuit in the 5203. The CPU printer logic reacts to this signal by placing up level on the 'intf reset ptr electronics' line (and/or activating the 'intf drop +60V' line) if any hammer remains on for more than one print scan (1.2 ms).

Note: The any-hammer-on condition can be simulated by operation of the CE switch (S1) on the printer control box.

'ANY HMR ON' LINE

'Any hmr on' is raised when the current in the common hammer return line exceeds 3 amperes (A).

Hammer current flowing when not printing, or any hammer on circuit not working (self-checking).

Any Hammer On

I/O IF Printer — Intf Any Hammer On

PC3

FL FP342

Start Res + Sys Ck Res + POR

PSS2

OR

(not) Print Time

A FL FP342

N

Any Hammer On Ck → C Diag 2-110

Any Hammer On Ck

Any Hmr On Ck

A FL FP341

POR

Start Res + Sys Ck Res

Any Hammer On Ck Latch T.P. → D Diag 4-045

Hmr + Incr Failure Ck → G Diag 2-100

(chain sync ck sample) — C Diag 2-120

Incr FF 1 FP404

Failure FF 2 FP404

Clock FF 3 FP404

Incr Failure Clock

Incrementer clutch was told to pick but did not.

Incr FF 1 FP501

Fail Ck FF 2 FP501

Counter FF 3 FP501

Incr Failure Ck → A Diag 2-110, 4-025, 4-030

Print Start SS

(not) Hammer Shift Clutch — C Diag 4-205

(not) Hammer Shift Clutch Sys Res or + Sys Ck Res

Incr Failure Ck

Incr Fail Ck

A FL FP341

Incr Failure Ck Latch T.P. → G Diag 4-040

POR

Start Res + Sys Ck Res

(Not) • Inhibit Echo Scan

Hammer Counter Clock

Hammer Clock 2

(Not) Feature Inhibit Echo Scan

(Mod 3)

Hammer Clock Control

Hmr Set Ctrl Gate

(not) Hammer Clock Advance

Hammer Clock 1

Inhibit Echo Scan

Feature Inhibit Echo Scan

FP333 (Mods 1 and 2)

Hammer Off Echo → B Diag 4-030

Hammer fired and no echo received, or hammer not fired and echo received.

Sample Echo Check

Hammer Off

Hammer Off Echo

OE

FP342

Hammer Echo Ck

Hmr Echo Ck

A FL FP341

POR

Start Res + Sys Ck Res

See Timing Chart 5-435

Hammer Echo Ck Latch T.P. → F Diag 4-045

Hammer Echo Ck → E Diag 2-110

Hammer Fire Bfr

HAR Set

Load HAR

FP335 FP811 (Mod 3)

I/O IF Printer — Intf Hammer Off Echo

'INTF HAMMER OFF ECHO' LINE

This line has up level each time a hammer driver is being addressed for the purpose of either setting or resetting the driver. When a hammer driver is set, the coil does not draw full current immediately and, therefore, the 'intf hammer off echo' line is at up level for 0.3 to 1.8 us; when the hammer driver is reset, the hammer-off echo appears after 5 to 30 us. The printer logic differentiates between the two echoes and recognizes only the latter one as the actual off-echo. To get a proper response, the hammer address pulses must be on for at least 30 us, even though 0.3 us is sufficient to set or reset a hammer driver.

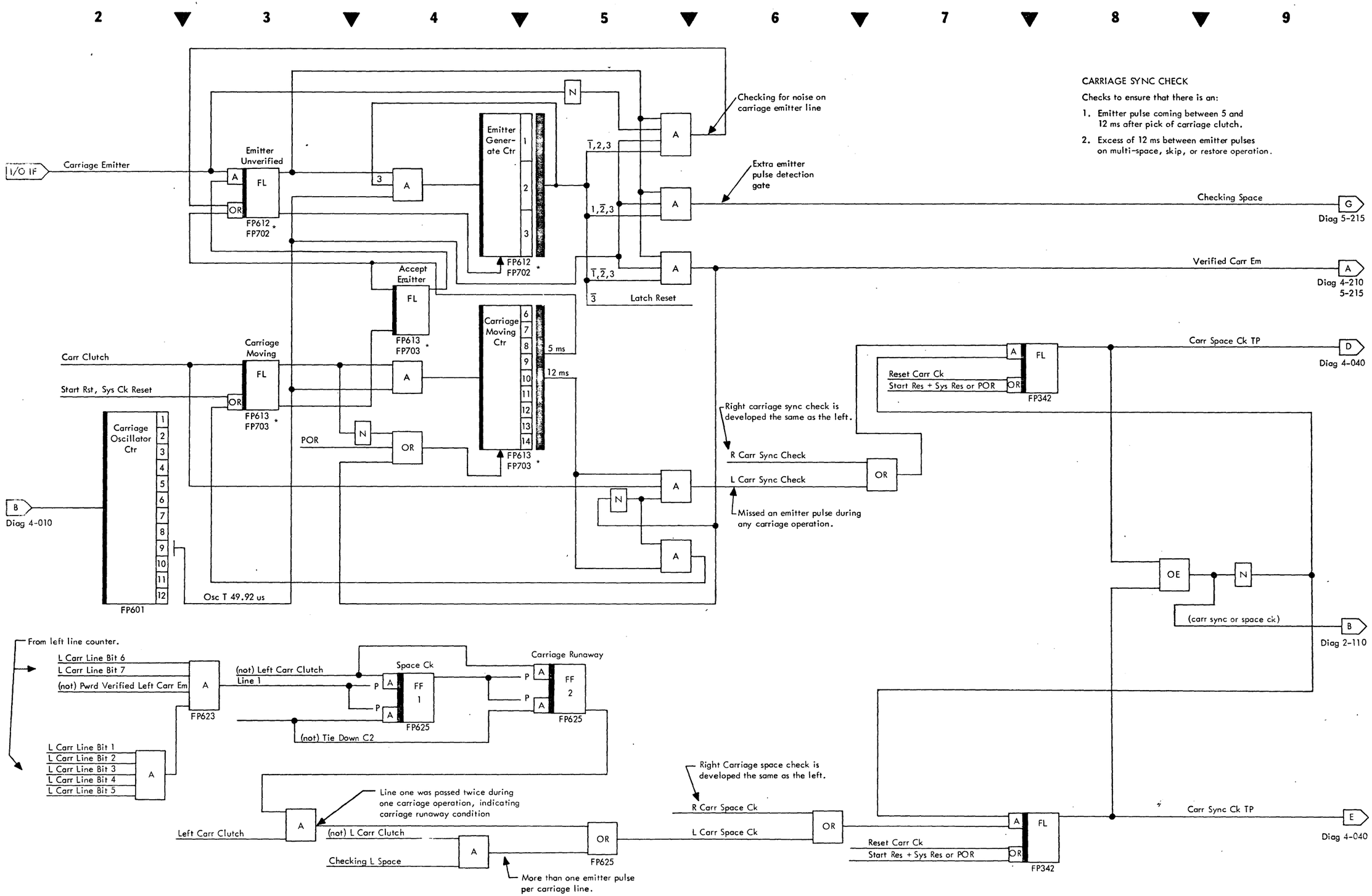


Diagram 2-140. Carriage Sync Check and Carriage Space Check

2 3 4 5 6 7 8 9

A

B

C

D

E

'INTF END OF FORMS' LINE

This line has down level when the form runs out of the forms chute. The signal is originated by the microswitch on the front apron of the forms chute.

'INTF COMMON INTERLOCK' LINE

This line has down level when either the forms chute is in the load position (pivoted up) or the rear unit is open (tilted back). A common-interlock condition causes the 5203 to lose its ready state, whereupon the CPU sends the 'intf drop +60V' signal. 'Intf drop +60V' causes the chain relay to be de-energized.

A

B

C

D

E

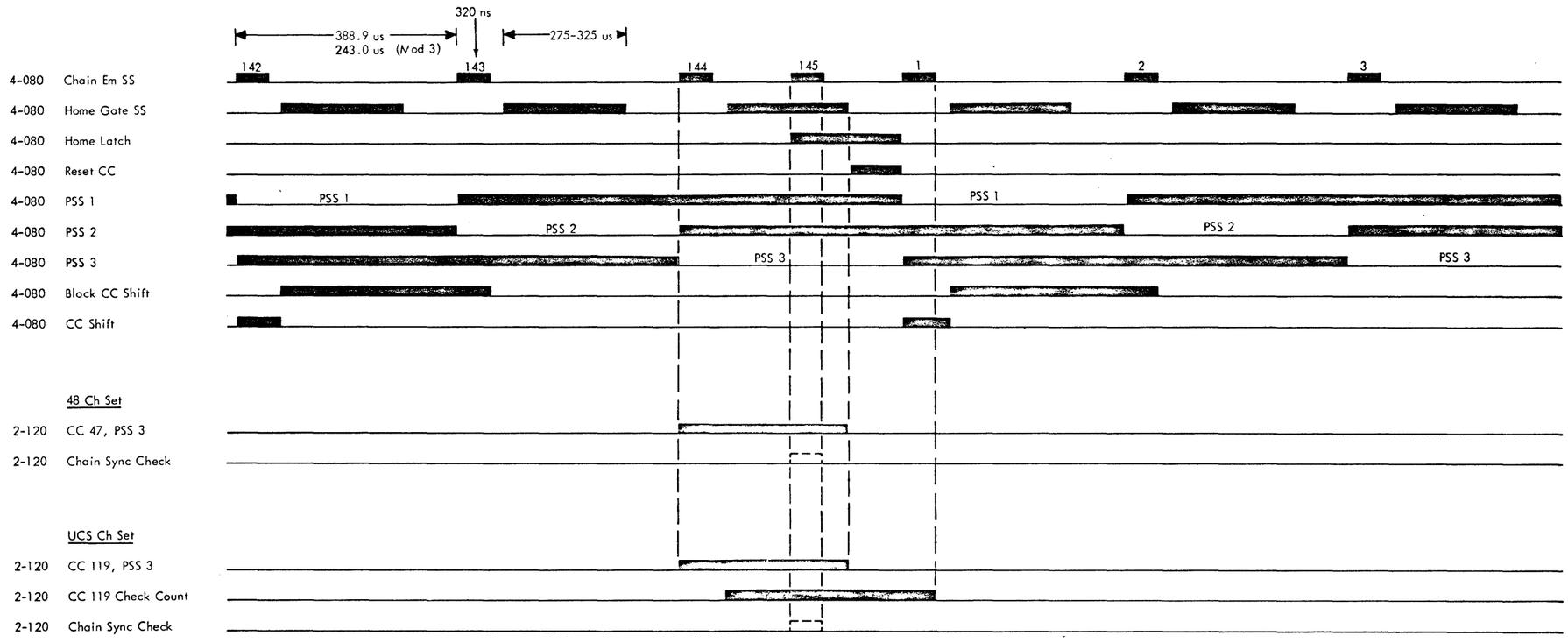


Diagram 2-160. PSS Counter Timing Chart and Chain Sync Check Timing Chart

2 3 4 5 6 7 8 9

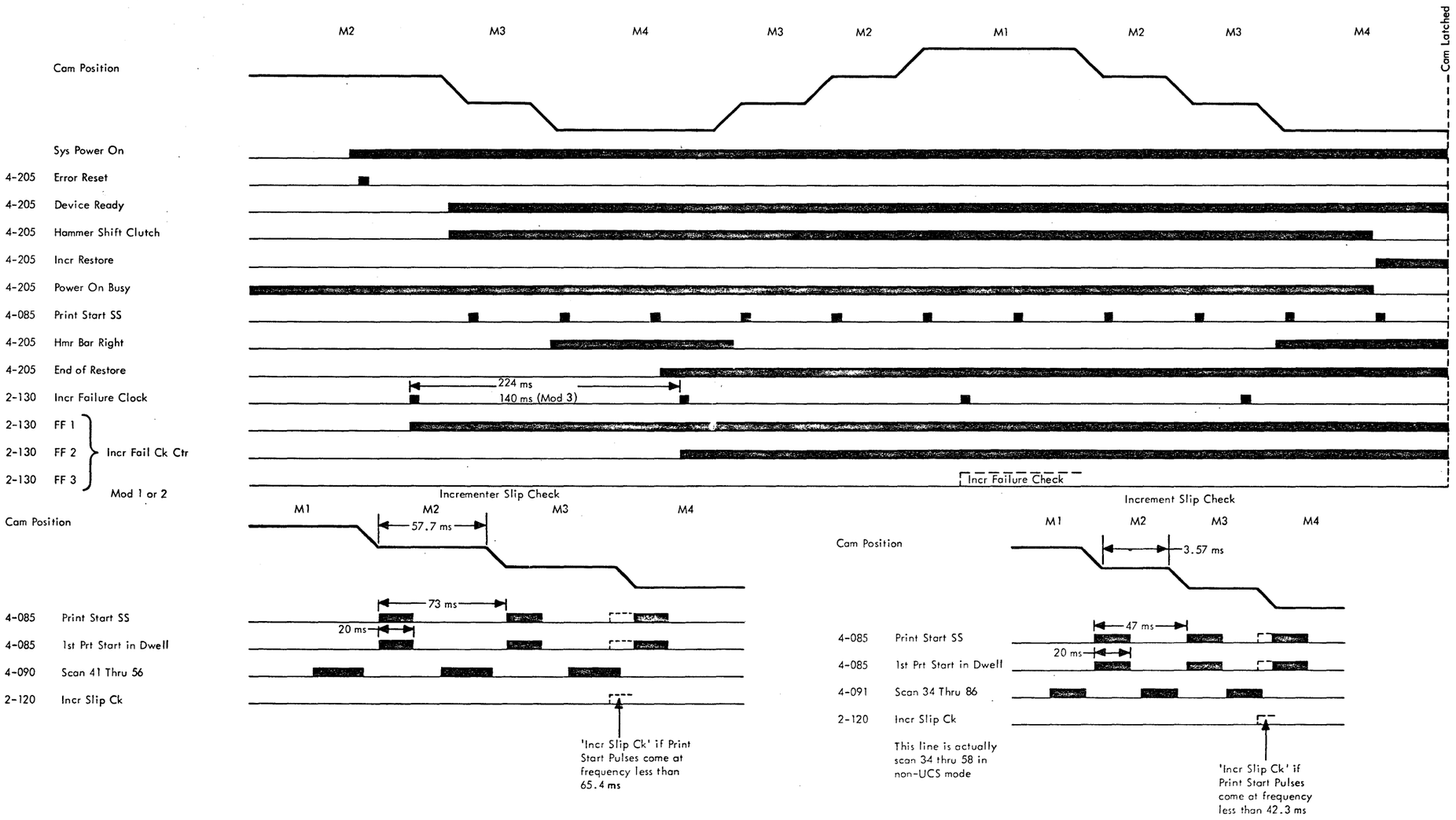
A

B

C

D

E



2 3 4 5 6 7 8 9

A

B

C

D

E

595.8 ms

M4 M3 M2 M1 M4 M3

Cam Position

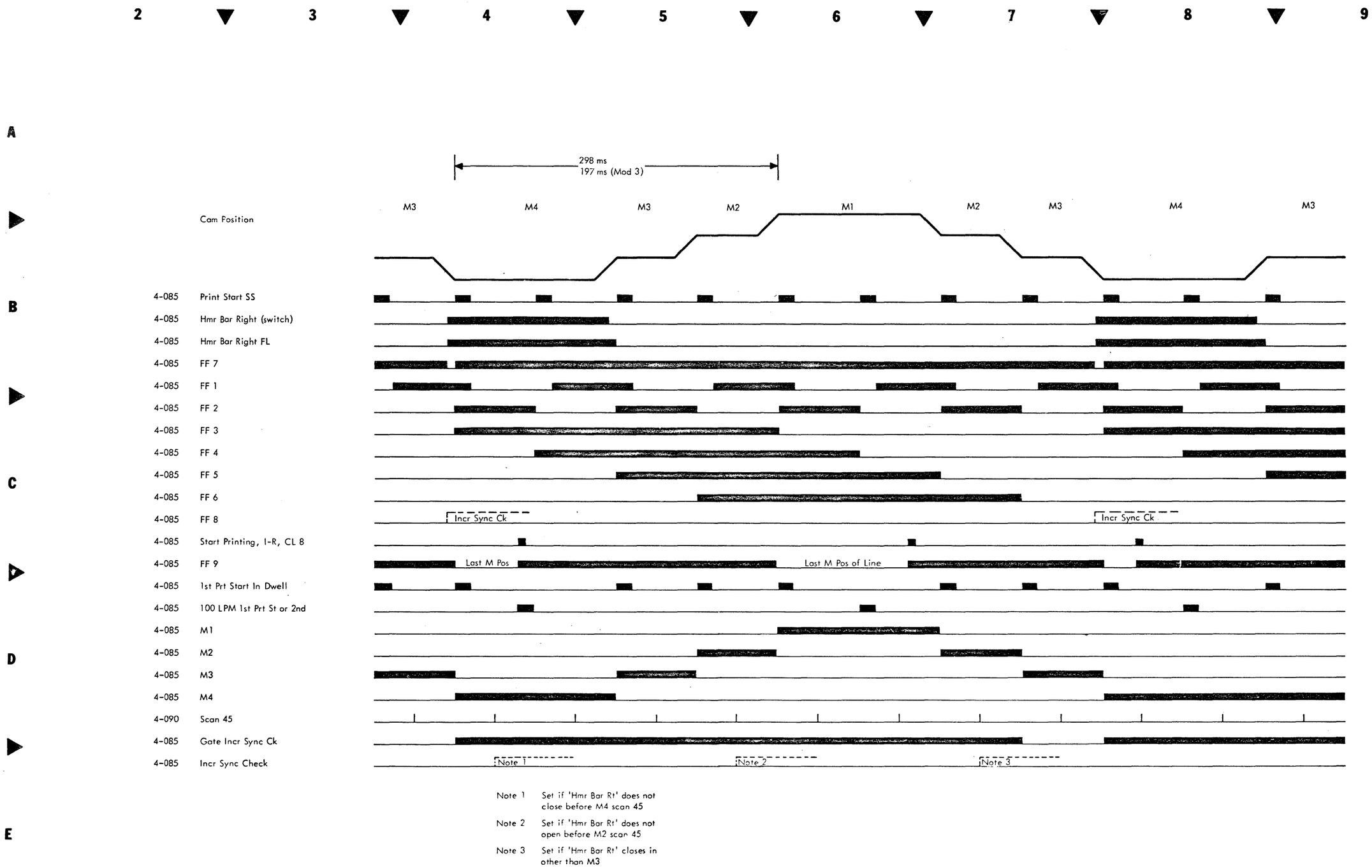
4-085 Print Start SS
4-085 Hmr Bar Right (switch)
4-085 Hmr Bar Right FL
4-085 FF 7
4-085 FF 1
4-085 FF 2
4-085 FF 3
4-085 FF 4
4-085 FF 5
4-085 FF 6
4-085 FF 8 — Incr Sync Ck — Incr Sync Ck
4-085 Start Printing, I-R, CL 8
4-085 FF 9 — Last M Pos of Line — Last M Pos of Line
4-085 1st Prt Start In Dwell
4-085 100 LPM 1st Prt St or 2nd
4-085 M1
4-085 M2
4-085 M3
4-085 M4
4-090 Scan 45
4-085 Gate Incr Sync Ck
4-085 Incr Sync Ck — Note 1 — Note 2 — Note 3

Note 1 Set if 'Hmr Bar Rt' closes in other than M1

Note 2 Set if 'Hmr Bar Rt' does not close before M4 scan 45

Note 3 Set if 'Hmr Bar Rt' does not open between M2 scan 45

Diagram 2-180. 100 LPM M Position Counter Timing Chart



Note 1 Set if 'Hmr Bar Rt' does not close before M4 scan 45

Note 2 Set if 'Hmr Bar Rt' does not open before M2 scan 45

Note 3 Set if 'Hmr Bar Rt' closes in other than M3

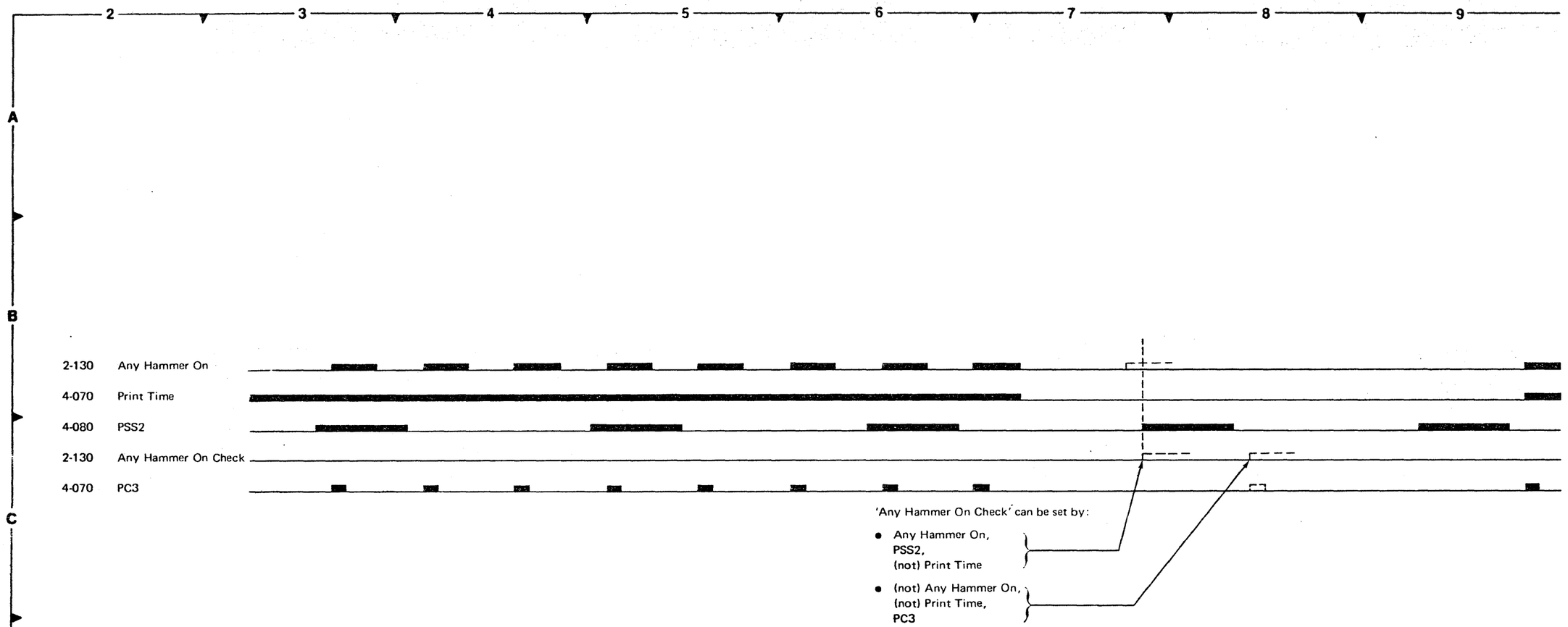
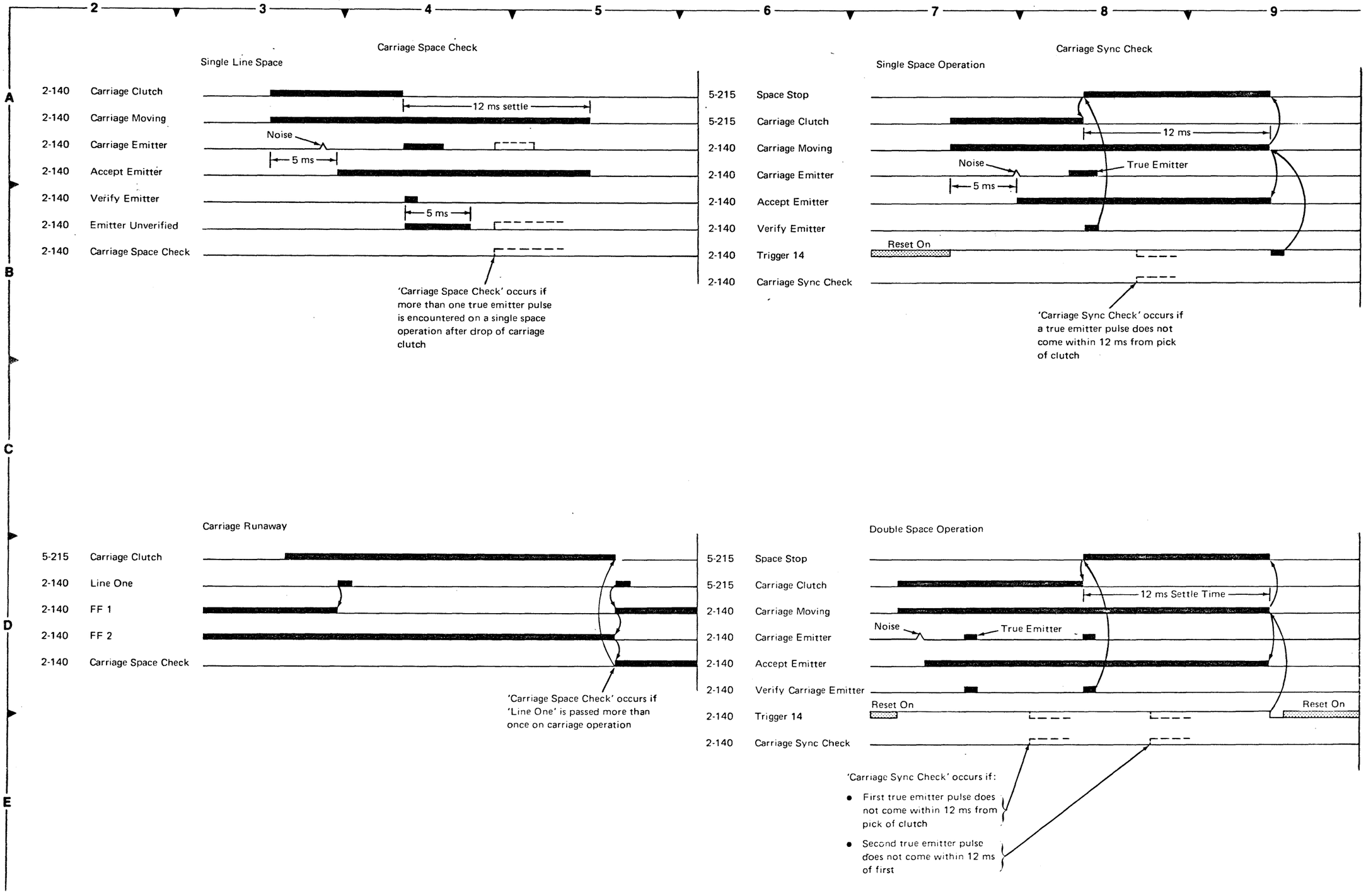


Diagram 2-190. Any Hammer On Check Timing Chart


2
3
4
5
6
7
8
9
A
B
C
D
E
Carriage Space Check
Single Line Space
2-140 Carriage Clutch
2-140 Carriage Moving
2-140 Carriage Emitter
2-140 Accept Emitter
2-140 Verify Emitter
2-140 Emitter Unverified
2-140 Carriage Space Check
12 ms settle
Noise
5 ms
5 ms
'Carriage Space Check' occurs if more than one true emitter pulse is encountered on a single space operation after drop of carriage clutch
Carriage Sync Check
Single Space Operation
5-215 Space Stop
5-215 Carriage Clutch
2-140 Carriage Moving
2-140 Carriage Emitter
2-140 Accept Emitter
2-140 Verify Emitter
2-140 Trigger 14
2-140 Carriage Sync Check
12 ms
Noise
True Emitter
5 ms
Reset On
'Carriage Sync Check' occurs if a true emitter pulse does not come within 12 ms from pick of clutch
Carriage Runaway
5-215 Carriage Clutch
2-140 Line One
2-140 FF 1
2-140 FF 2
2-140 Carriage Space Check
'Carriage Space Check' occurs if 'Line One' is passed more than once on carriage operation
Double Space Operation
5-215 Space Stop
5-215 Carriage Clutch
2-140 Carriage Moving
2-140 Carriage Emitter
2-140 Accept Emitter
2-140 Verify Carriage Emitter
2-140 Trigger 14
2-140 Carriage Sync Check
12 ms Settle Time
Noise
True Emitter
Reset On
Reset On
'Carriage Sync Check' occurs if:
• First true emitter pulse does not come within 12 ms from pick of clutch
• Second true emitter pulse does not come within 12 ms of first

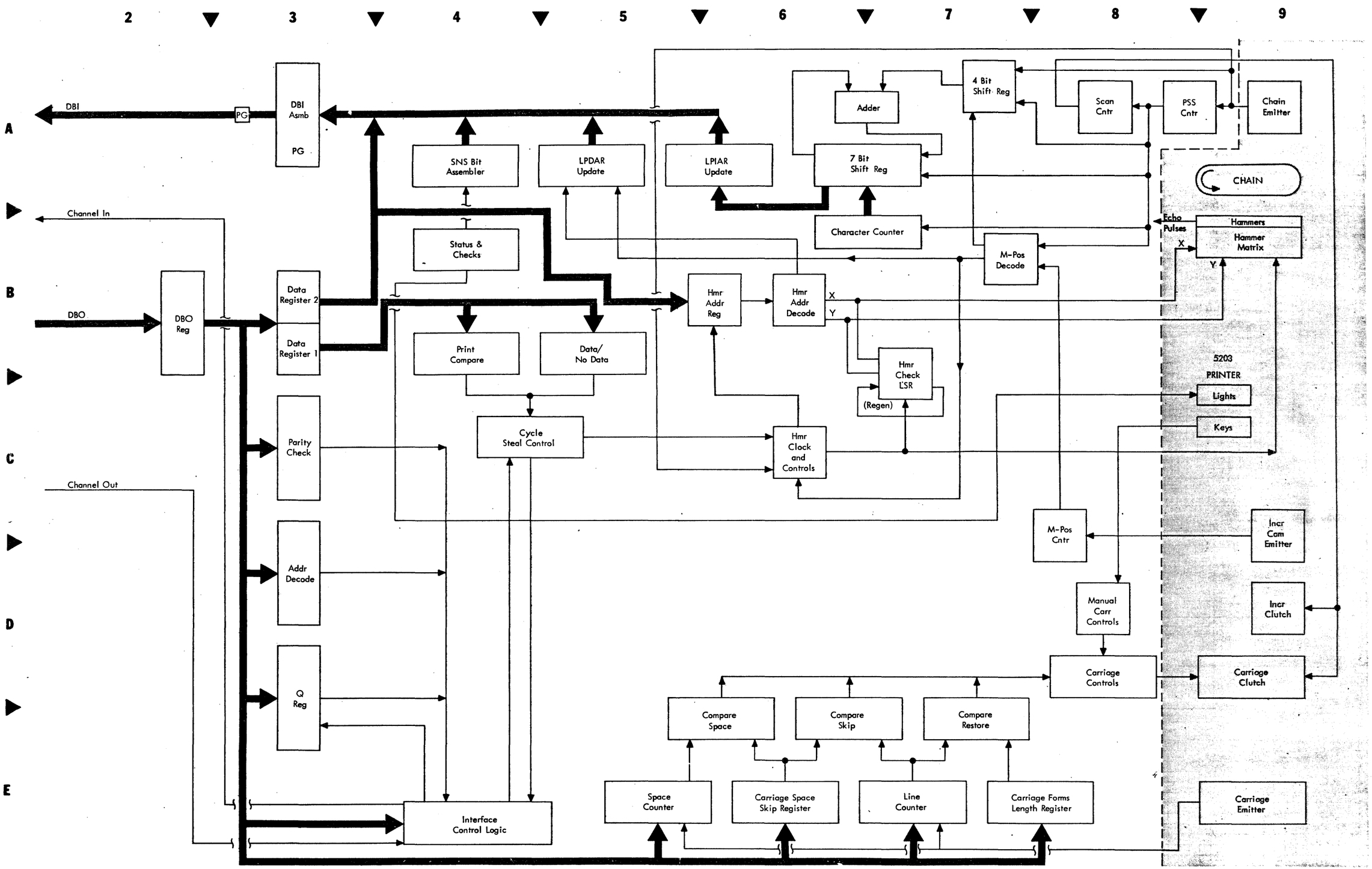
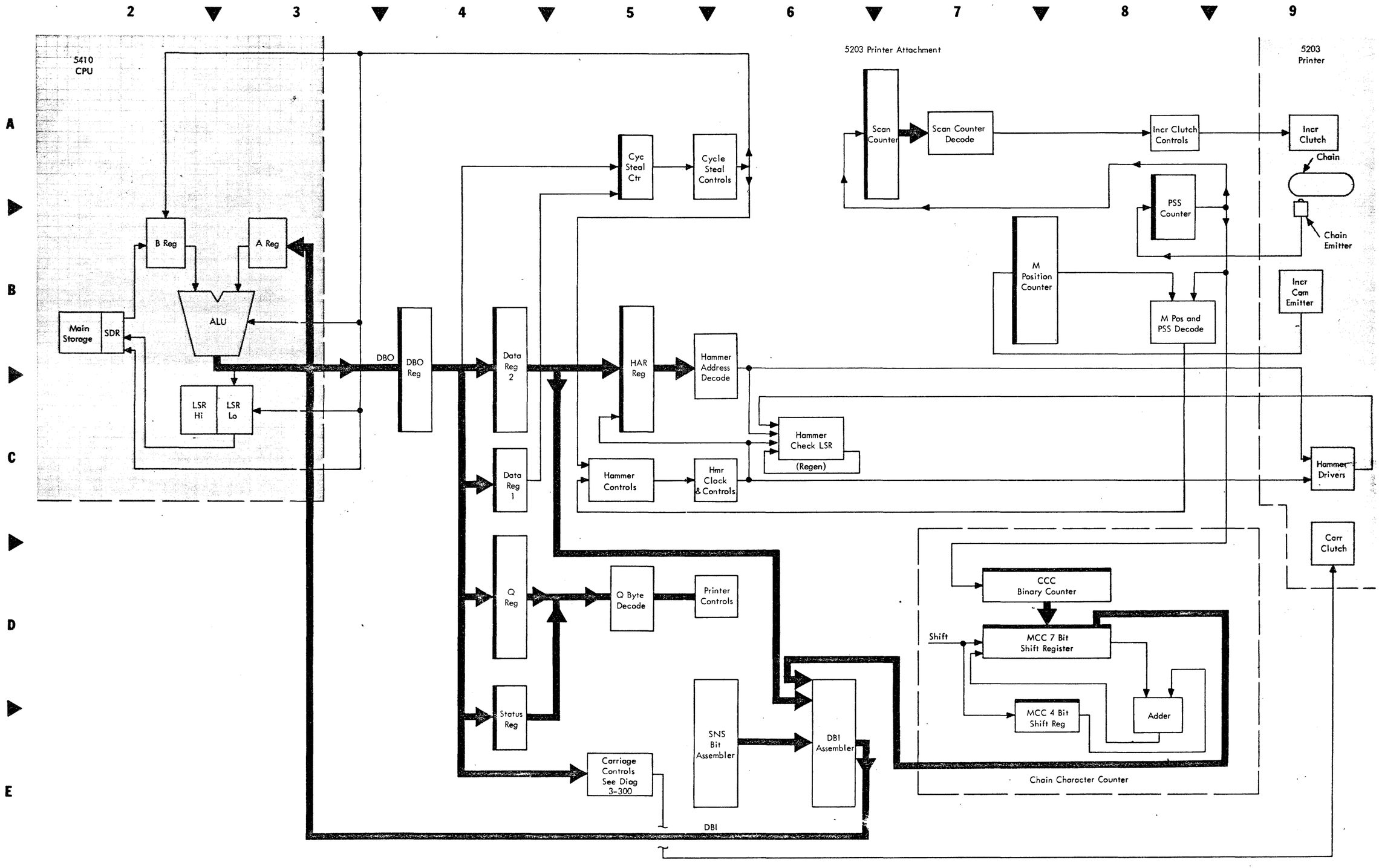


Diagram 3-100. 5203 Printer Attachment


2
3
4
5
6
7
8
9
A
B
C
D
E
5410 CPU
5203 Printer Attachment
5203 Printer
Scan Counter
Scan Counter Decode
Incr Clutch Controls
Incr Clutch
Chain
Chain Emitter
PSS Counter
M Position Counter
M Pos and PSS Decode
Incr Cam Emitter
Cyc Steal Ctr
Cycle Steal Controls
B Reg
A Reg
ALU
Main Storage
SDR
LSR Hi
LSR Lo
DBO
DBO Reg
Data Reg 2
Data Reg 1
HAR Reg
Hammer Address Decode
Hammer Check LSR
(Regen)
Hammer Controls
Hmr Clock & Controls
Hammer Drivers
Carr Clutch
Q Reg
Q Byte Decode
Printer Controls
Status Reg
SNS Bit Assembler
DBI Assembler
Carriage Controls See Diag 3-300
DBI
CCC Binary Counter
Shift
MCC 7 Bit Shift Register
MCC 4 Bit Shift Reg
Adder
Chain Character Counter

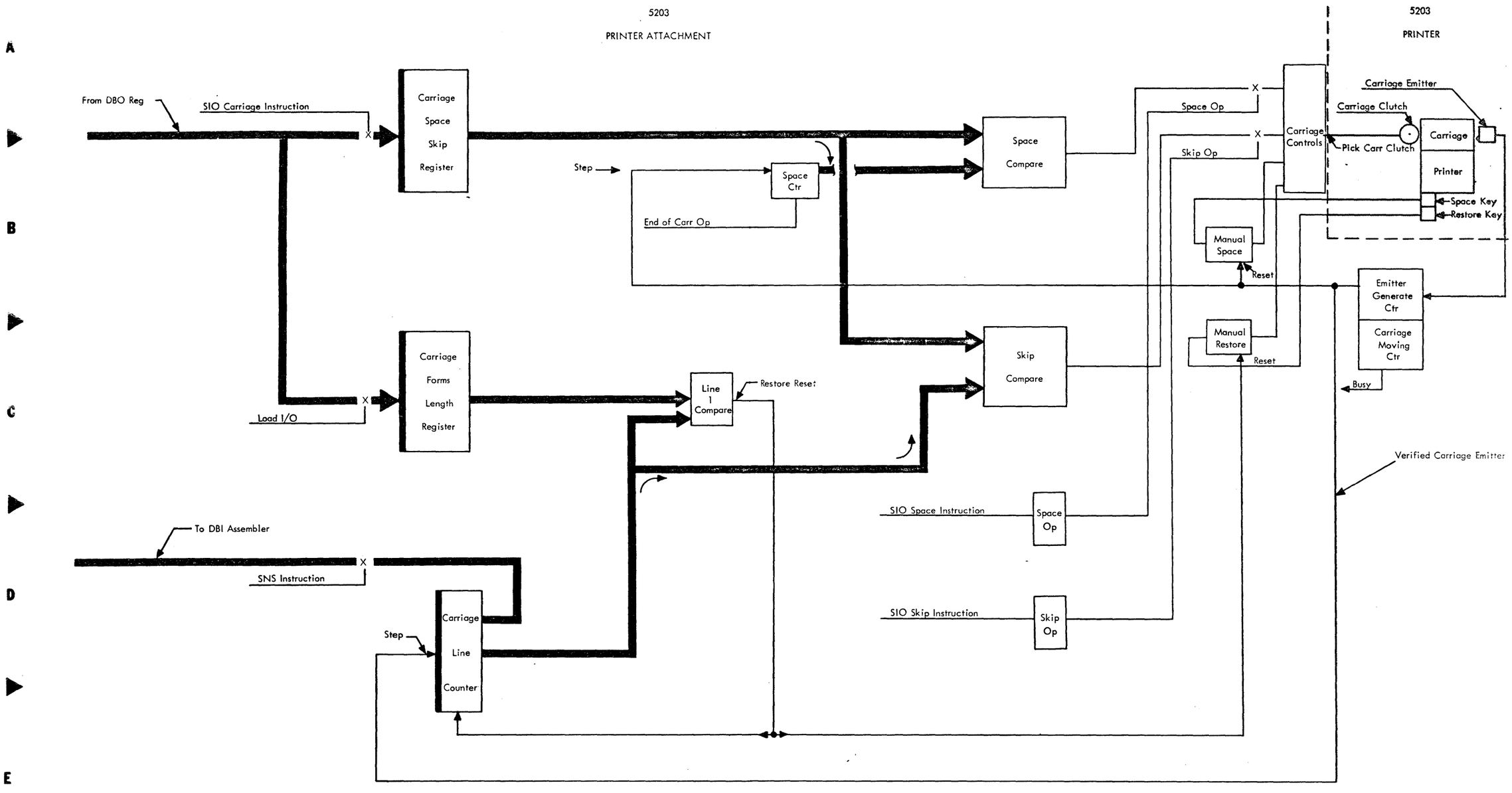
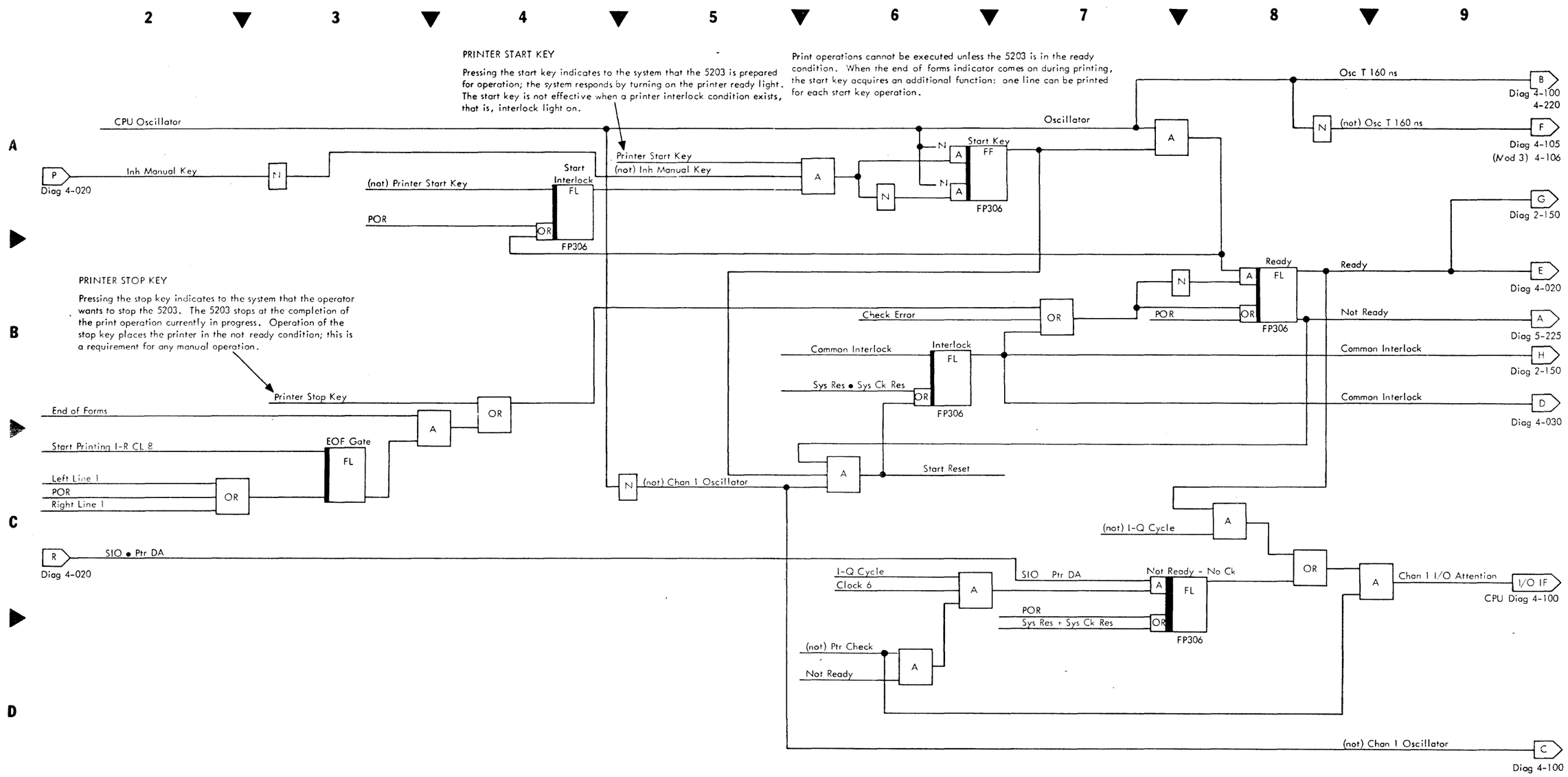


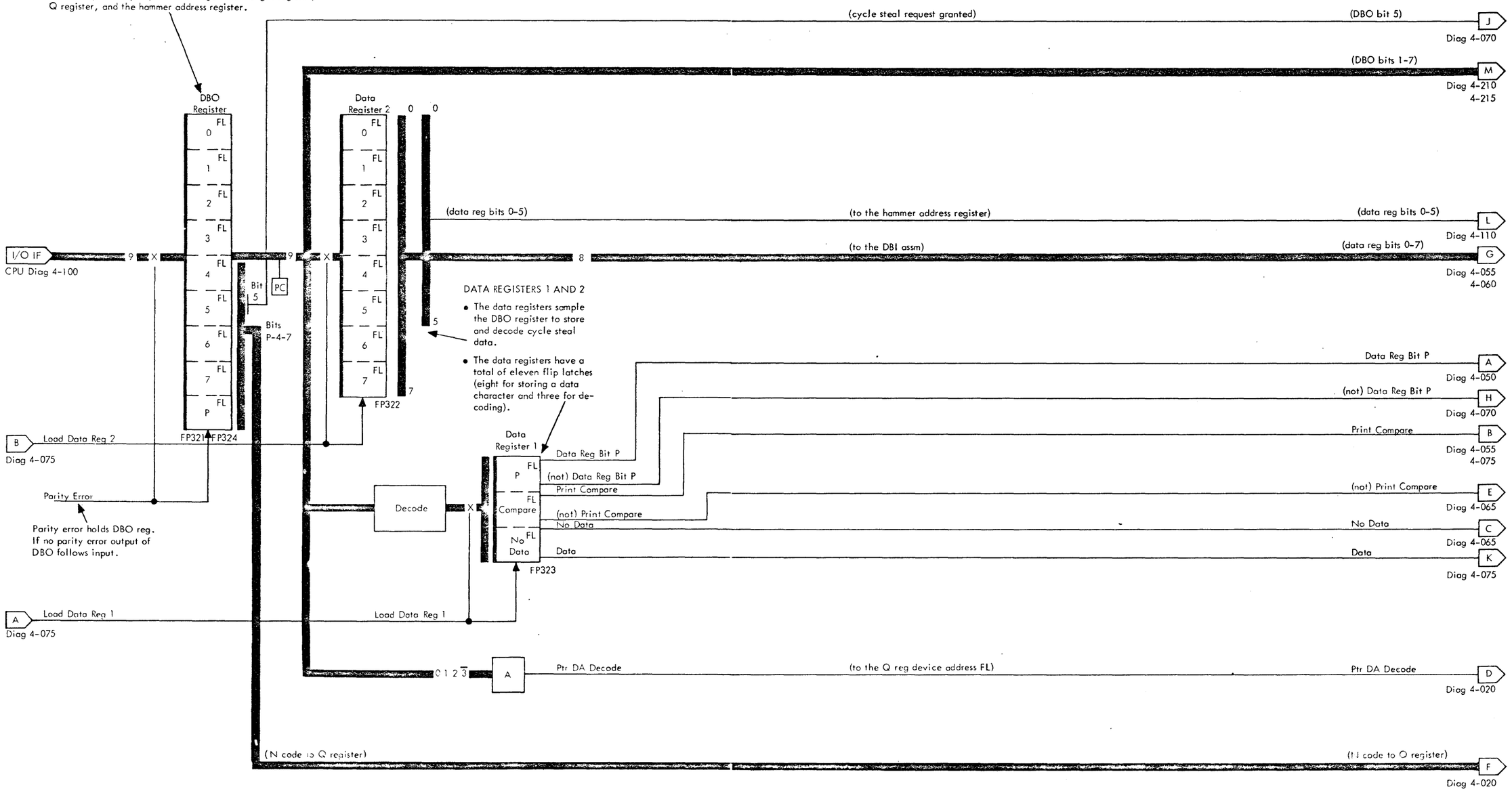
Diagram 3-300. Carriage Data Flow


2
3
4
5
6
7
8
9
A
B
C
D
E
PRINTER START KEY
Pressing the start key indicates to the system that the 5203 is prepared for operation; the system responds by turning on the printer ready light. The start key is not effective when a printer interlock condition exists, that is, interlock light on.
Print operations cannot be executed unless the 5203 is in the ready condition. When the end of forms indicator comes on during printing, the start key acquires an additional function: one line can be printed for each start key operation.
PRINTER STOP KEY
Pressing the stop key indicates to the system that the operator wants to stop the 5203. The 5203 stops at the completion of the print operation currently in progress. Operation of the stop key places the printer in the not ready condition; this is a requirement for any manual operation.
CPU Oscillator
Oscillator
Osc T 160 ns
B
Diag 4-100
4-220
(not) Osc T 160 ns
F
Diag 4-105
(Mod 3) 4-106
P
Diag 4-020
Inh Manual Key
N
(not) Printer Start Key
Start Interlock
FL
POR
OR
FP306
Printer Start Key
(not) Inh Manual Key
A
N
Start Key
FF
FP306
G
Diag 2-150
Ready
FL
FP306
Ready
E
Diag 4-020
Check Error
OR
POR
Not Ready
A
Diag 5-225
Common Interlock
Interlock
FL
Sys Res • Sys Ck Res
FP306
Common Interlock
H
Diag 2-150
Common Interlock
D
Diag 4-030
Printer Stop Key
End of Forms
Start Printing I-R CL 8
EOF Gate
FL
Left Line 1
POR
Right Line 1
(not) Chan 1 Oscillator
Start Reset
(not) 1-Q Cycle
R
Diag 4-020
SIO • Ptr DA
1-Q Cycle
Clock 6
SIO Ptr DA
Not Ready - No Ck
FL
POR
Sys Res + Sys Ck Res
FP306
OR
Chan 1 I/O Attention
I/O IF
CPU Diag 4-100
(not) Ptr Check
Not Ready
(not) Chan 1 Oscillator
C
Diag 4-100

2 3 4 5 6 7 8 9

DATA BUS OUT REGISTER

- The data bus out (DBO) register has nine flip latches.
- The latches remain set if there is a parity error, so the CE can observe the contents of the register.
- All print data from the CPU enters the attachment through the data bus out register setting the appropriate flip latches.
- Data from the data bus out register loads the data register, carriage space-skip register, carriage forms length register, Q register, and the hammer address register.



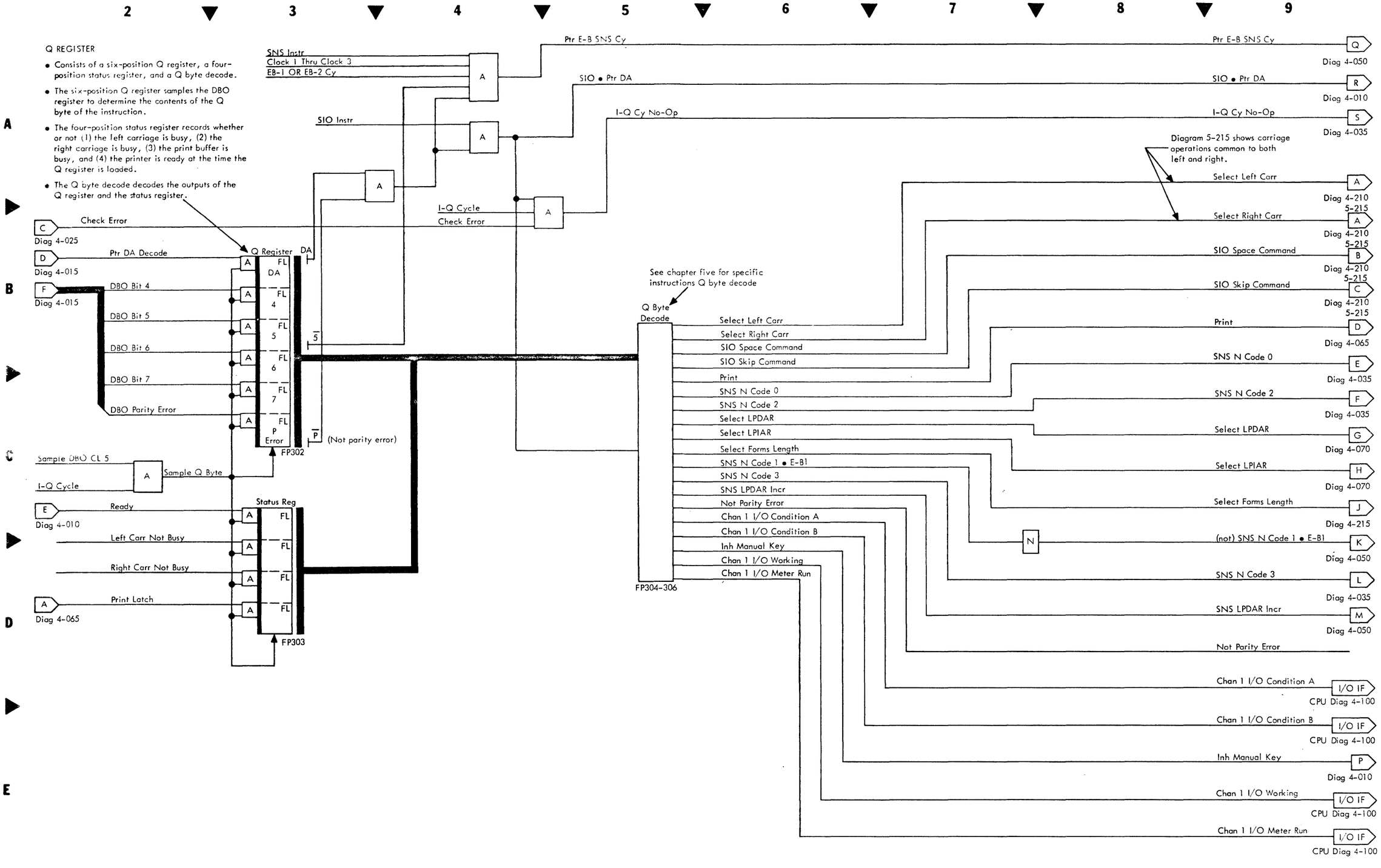


Diagram 4-020. Q Register and Decode

2 3 4 5 6 7 8 9

A
B
C
D
E

A Diag 4-085 Incr Sync Ck

A Diag 4-080 Reset CC

C Diag 4-065 (not) Print Latch

CE Tie Up

E Diag 2-120 Chain Sync Check

Device Ready

Start Res + Sys Ck Res

POR

A Diag 4-030 Forms + Thermal Ck

B Diag 4-030 Any Hammer On Ck

C Diag 4-030 Hammer Echo Ck

A Diag 2-130 Inc Failure Ck

A Diag 4-035 (not) No-Op

FP341

SENSE BIT ASSEMBLER

- The SNS bit assembler contains the status of the printer attachment logic.
- The SNS bits are placed in the DBI assembler and sent to the CPU on E-B cycles.

Chain Sync Ck

Incr Sync Ck

Allows first error to be recorded for SNS interrogation and error recovery

Start Res + Sys Ck Res Or POR

Any Hammer On Ck Latch T.P.

CE SNS Bit Latched T.P.

Hammer Echo Ck Latch T.P.

Inc Failure Ck Latch T.P.

Hammer Ck

Incr Sync Ck Latch T.P. → A Diag 4-040

Chain Sync Ck Latch T.P. → B Diag 4-040

Check Error → C Diag 4-020

Any Hammer On Ck Latch T.P. → D Diag 4-045

CE SNS Bit Latched T.P. → E Diag 4-045

Hammer Echo Ck Latch T.P. → F Diag 4-045

Incr Failure Ck Latch T.P. → G Diag 4-040

Hmr + Incr Failure Ck → H Diag 4-065

Hammer Ck → J Diag 4-030

Chan 1 I/O Check → I/O IF CPU Diag 4-100

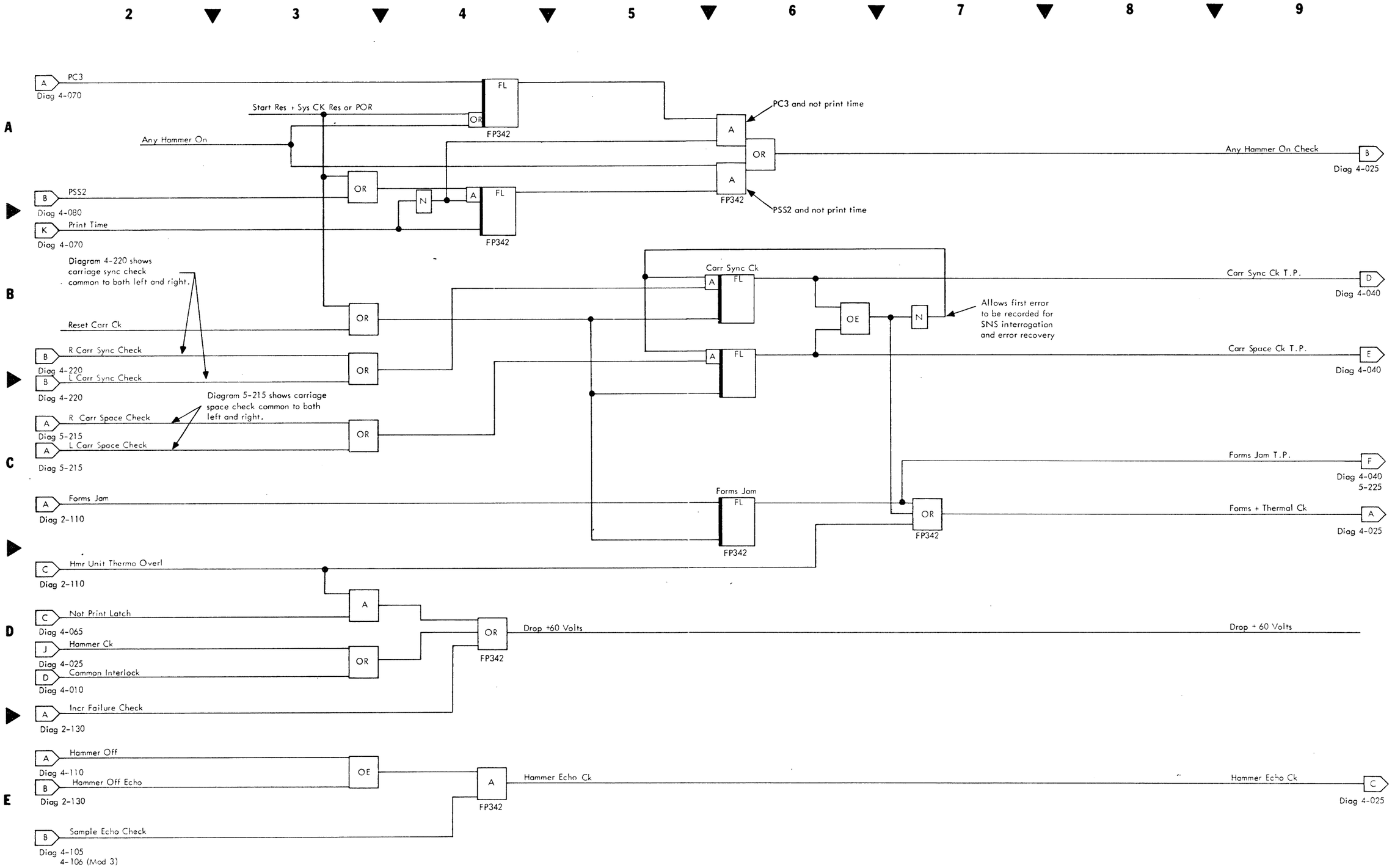
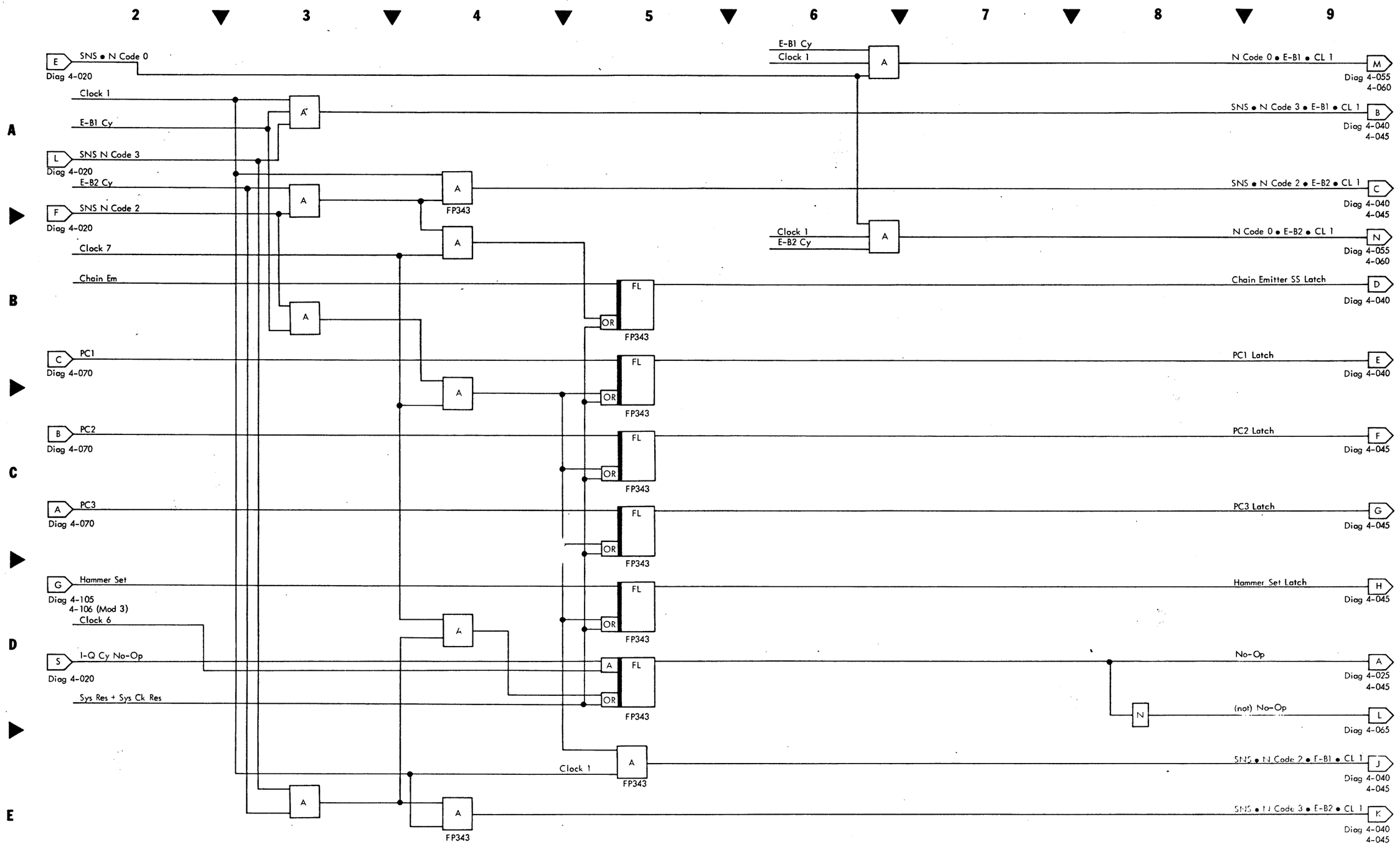


Diagram 4-030. SNS Bit Assembler Check Bit 2


2
3
4
5
6
7
8
9
A
B
C
D
E
E SNS • N Code 0
Diag 4-020
Clock 1
E-B1 Cy
L SNS N Code 3
Diag 4-020
E-B2 Cy
F SNS N Code 2
Diag 4-020
Clock 7
Chain Em
C PC1
Diag 4-070
B PC2
Diag 4-070
A PC3
Diag 4-070
G Hammer Set
Diag 4-105
4-106 (Mod 3)
Clock 6
S I-Q Cy No-Op
Diag 4-020
Sys Res + Sys Ck Res
A
FP343
FL
OR
E-B1 Cy
Clock 1
Clock 1
E-B2 Cy
Clock 1
N Code 0 • E-B1 • CL 1
M
Diag 4-055
4-060
SNS • N Code 3 • E-B1 • CL 1
B
Diag 4-040
4-045
SNS • N Code 2 • E-B2 • CL 1
C
Diag 4-040
4-045
N Code 0 • E-B2 • CL 1
N
Diag 4-055
4-060
Chain Emitter SS Latch
D
Diag 4-040
PC1 Latch
E
Diag 4-040
PC2 Latch
F
Diag 4-045
PC3 Latch
G
Diag 4-045
Hammer Set Latch
H
Diag 4-045
No-Op
A
Diag 4-025
4-045
N
(not) No-Op
L
Diag 4-065
SNS • N Code 2 • E-B1 • CL 1
J
Diag 4-040
4-045
SNS • N Code 3 • E-B2 • CL 1
K
Diag 4-040
4-045

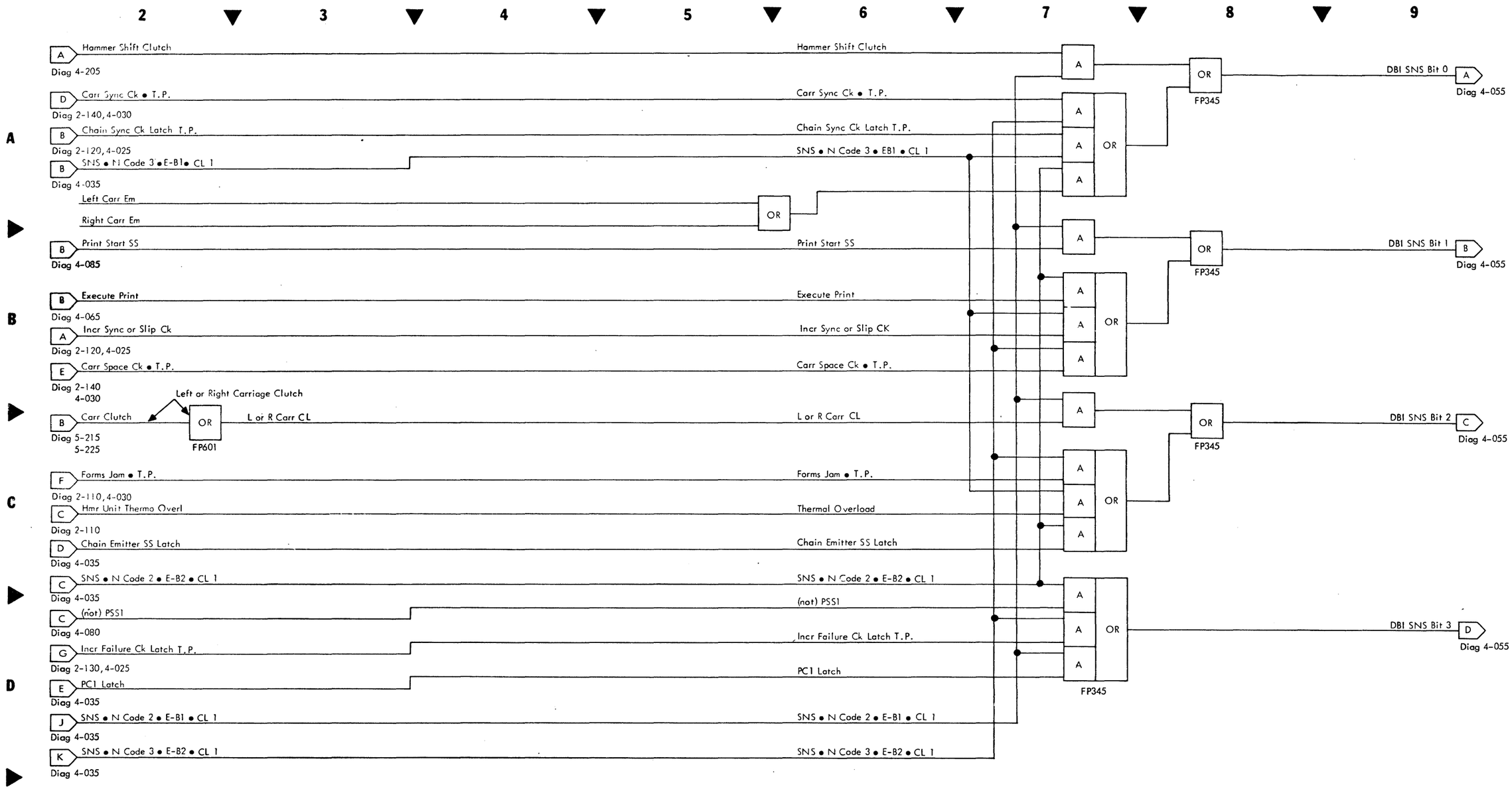
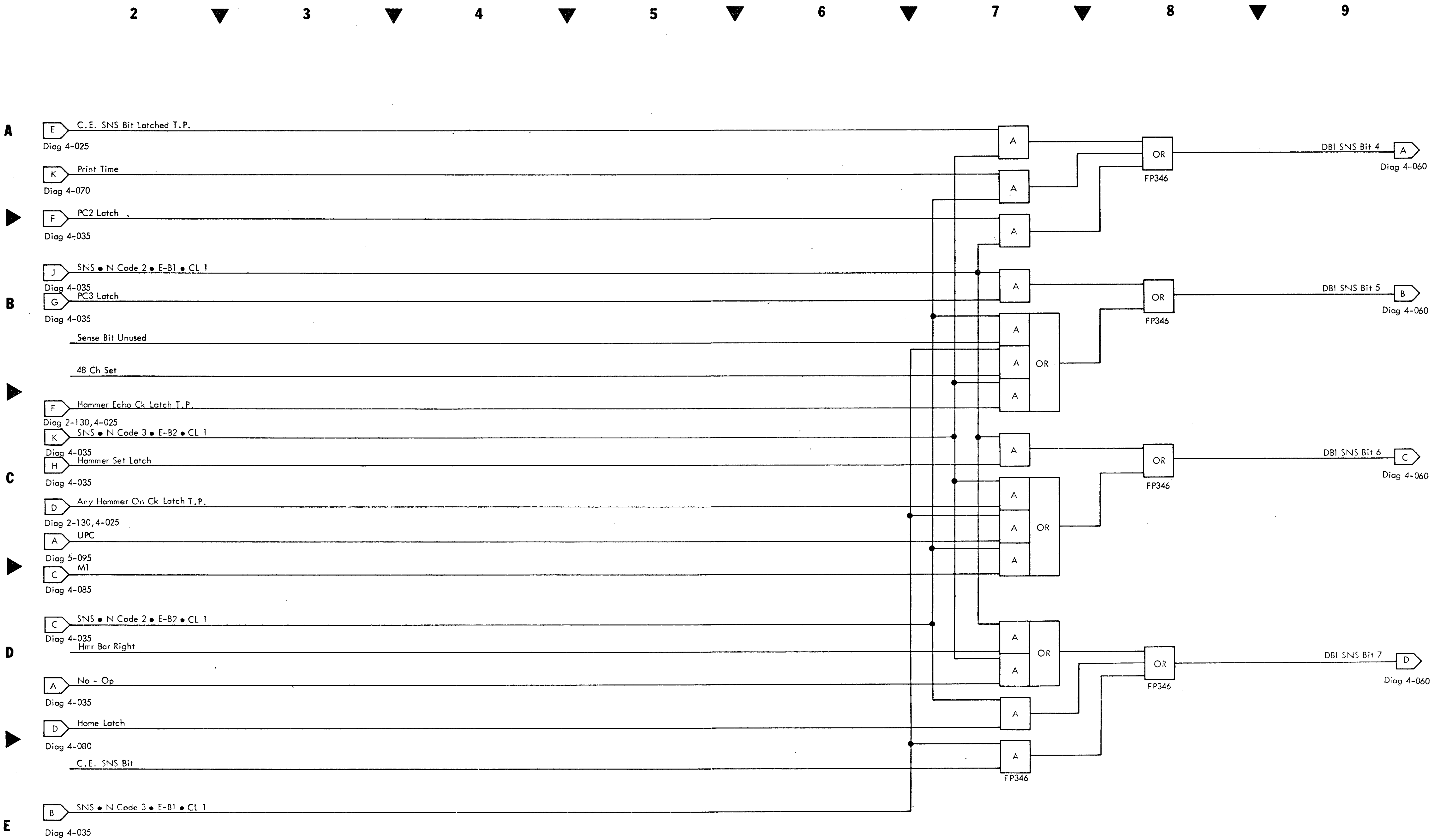


Diagram 4-040. SNS Bit Assembler Bits 0-3


2
3
4
5
6
7
8
9
A
B
C
D
E
E
C.E. SNS Bit Latched T.P.
Diag 4-025
K
Print Time
Diag 4-070
F
PC2 Latch
Diag 4-035
J
SNS • N Code 2 • E-B1 • CL 1
Diag 4-035
G
PC3 Latch
Diag 4-035
Sense Bit Unused
48 Ch Set
F
Hammer Echo Ck Latch T.P.
Diag 2-130, 4-025
K
SNS • N Code 3 • E-B2 • CL 1
Diag 4-035
H
Hammer Set Latch
Diag 4-035
D
Any Hammer On Ck Latch T.P.
Diag 2-130, 4-025
A
UPC
Diag 5-095
C
M1
Diag 4-085
C
SNS • N Code 2 • E-B2 • CL 1
Diag 4-035
Hmr Bar Right
A
No - Op
Diag 4-035
D
Home Latch
Diag 4-080
C.E. SNS Bit
B
SNS • N Code 3 • E-B1 • CL 1
Diag 4-035
A
OR
FP346
DBI SNS Bit 4
A
Diag 4-060
DBI SNS Bit 5
B
Diag 4-060
DBI SNS Bit 6
C
Diag 4-060
DBI SNS Bit 7
D
Diag 4-060

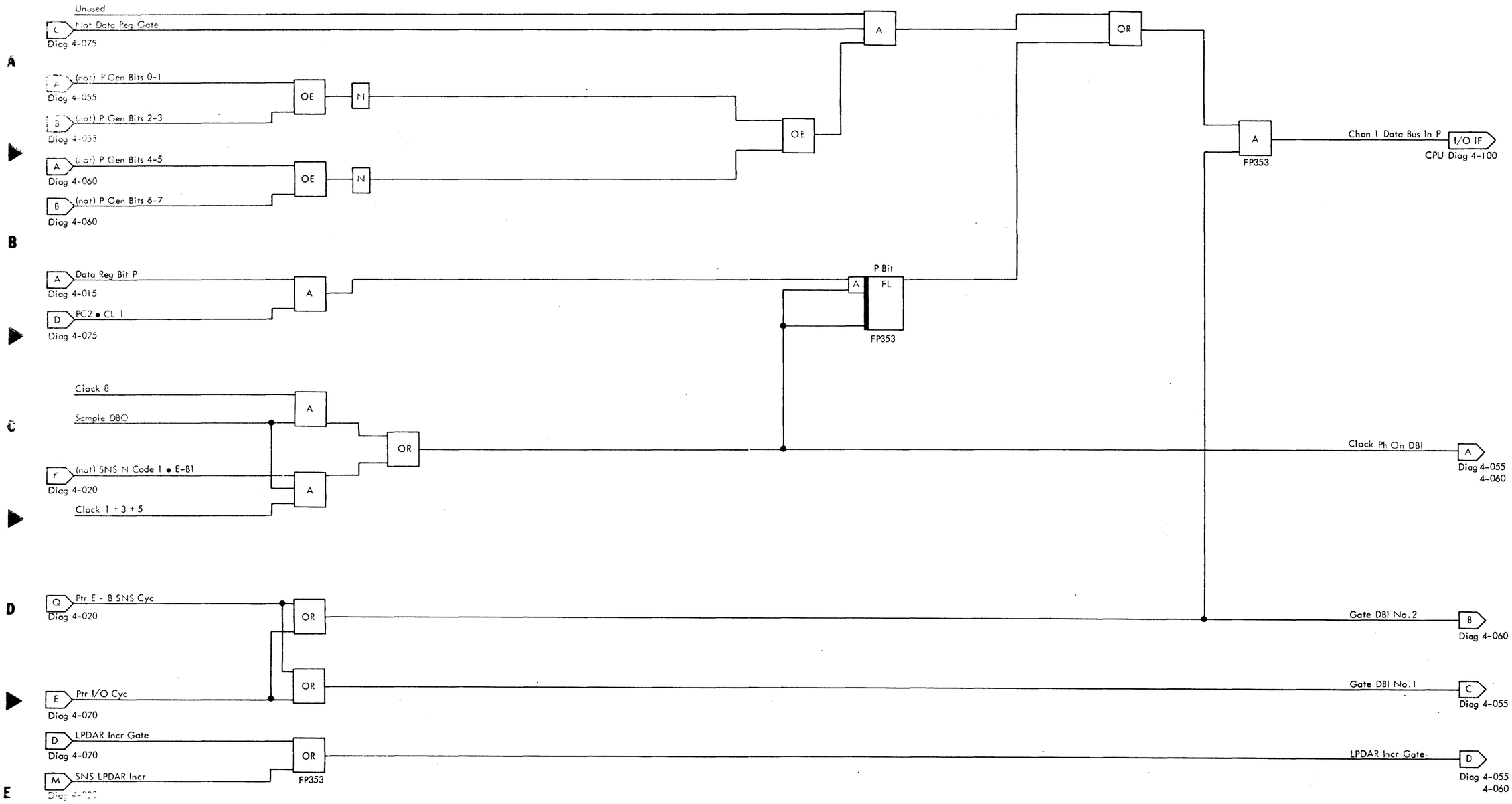
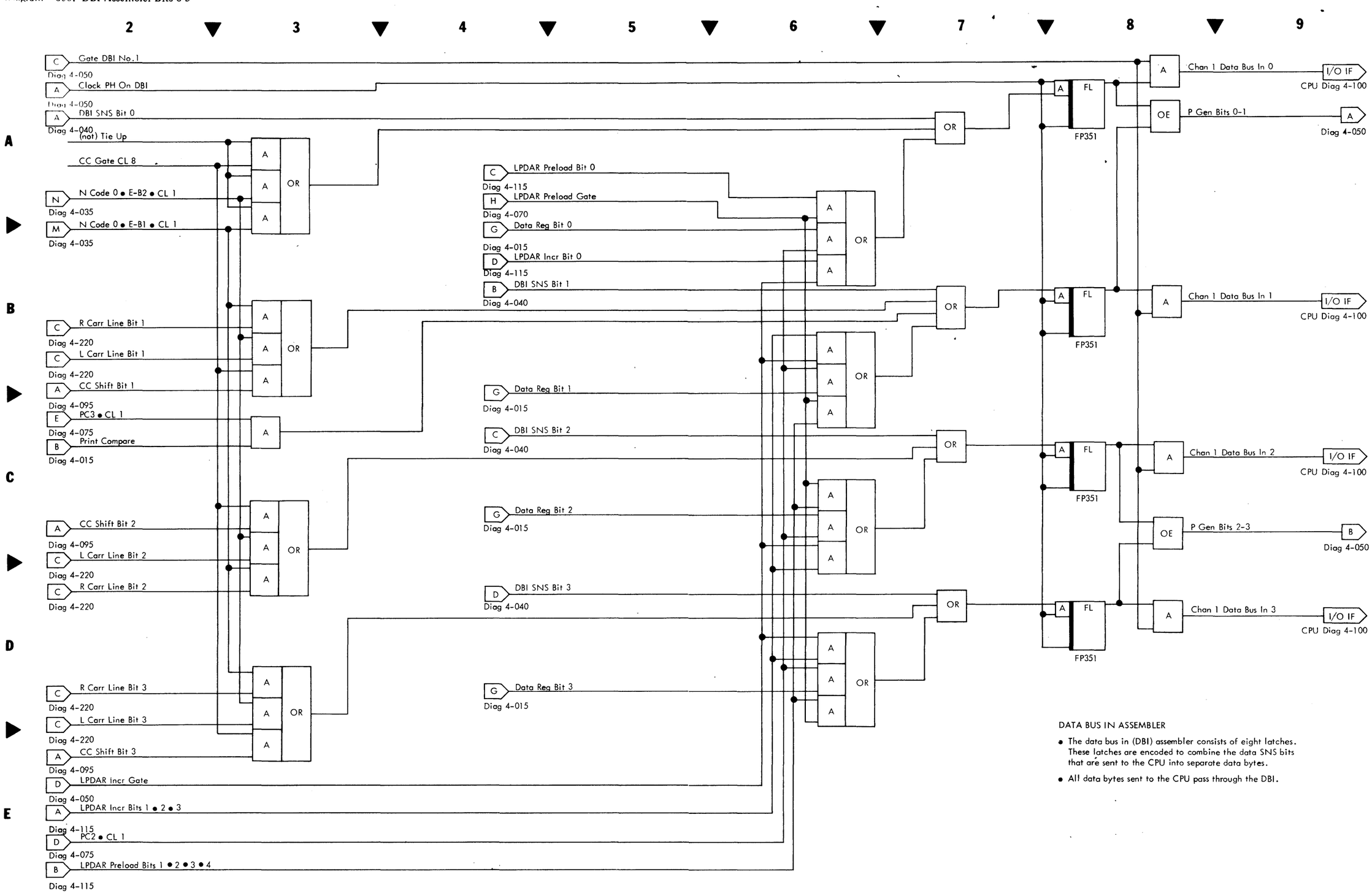


Diagram 4-050. DBI Assembler P Bit Generator-Gating



DATA BUS IN ASSEMBLER

- The data bus in (DBI) assembler consists of eight latches. These latches are encoded to combine the data SNS bits that are sent to the CPU into separate data bytes.
- All data bytes sent to the CPU pass through the DBI.

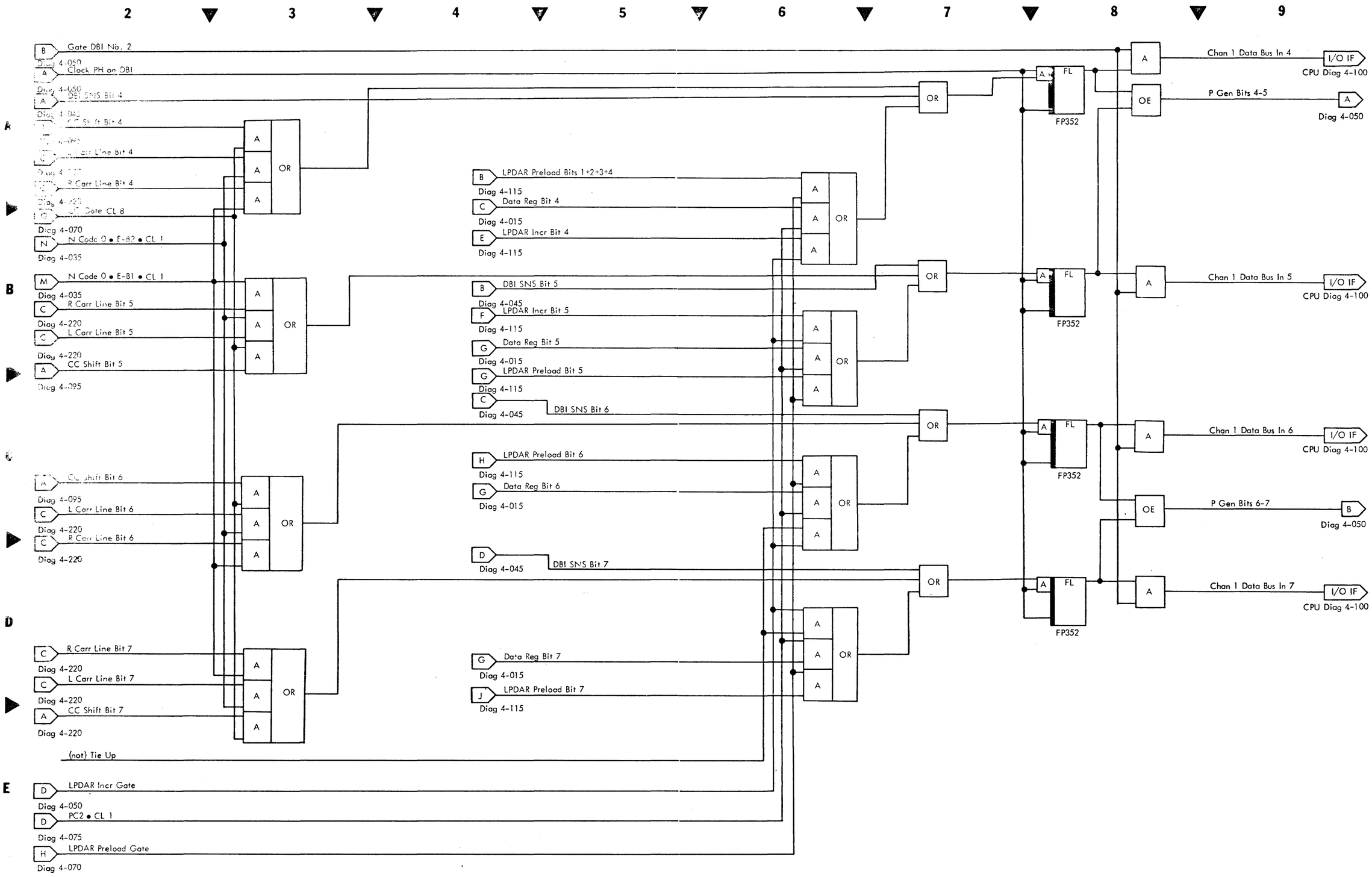
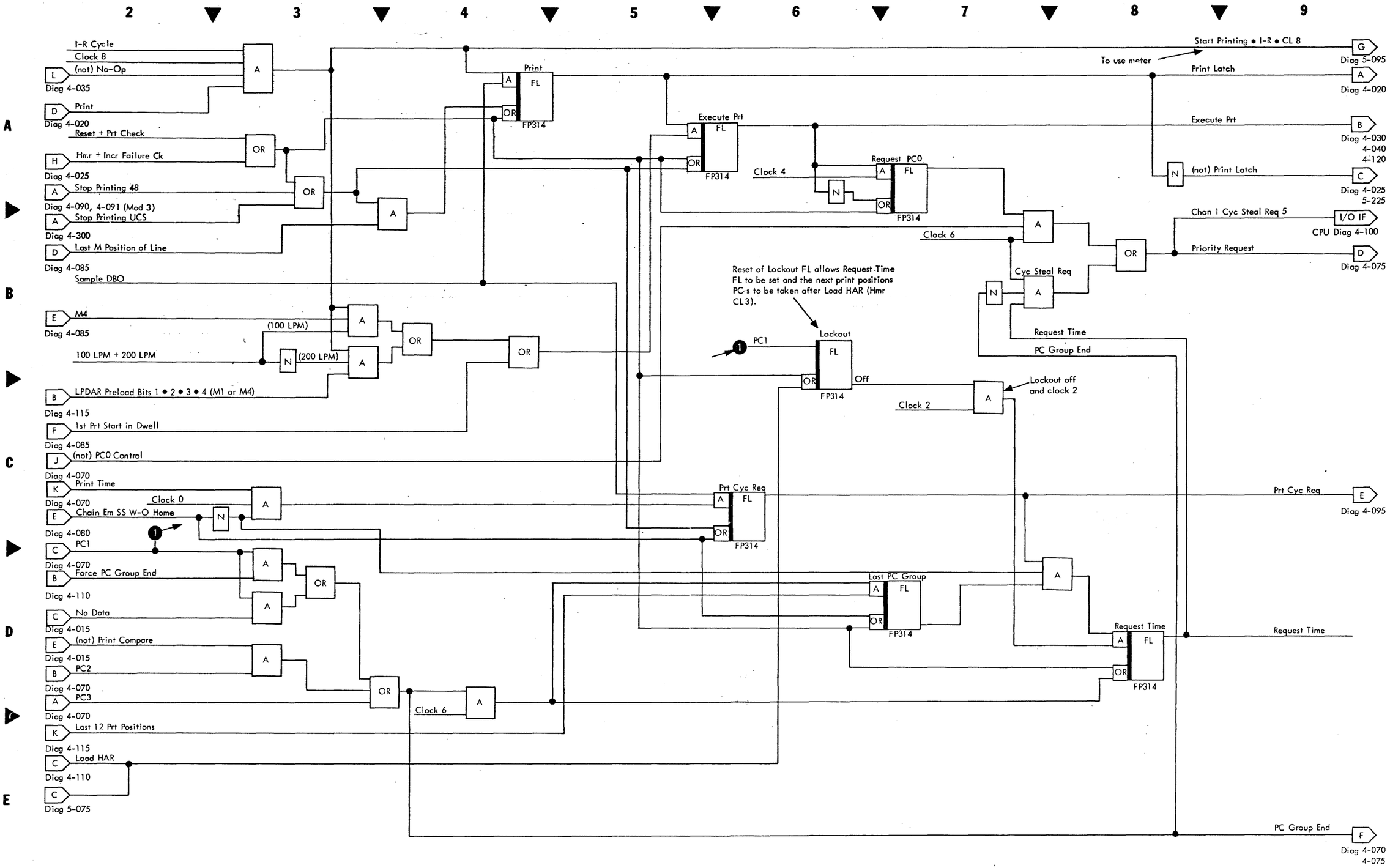
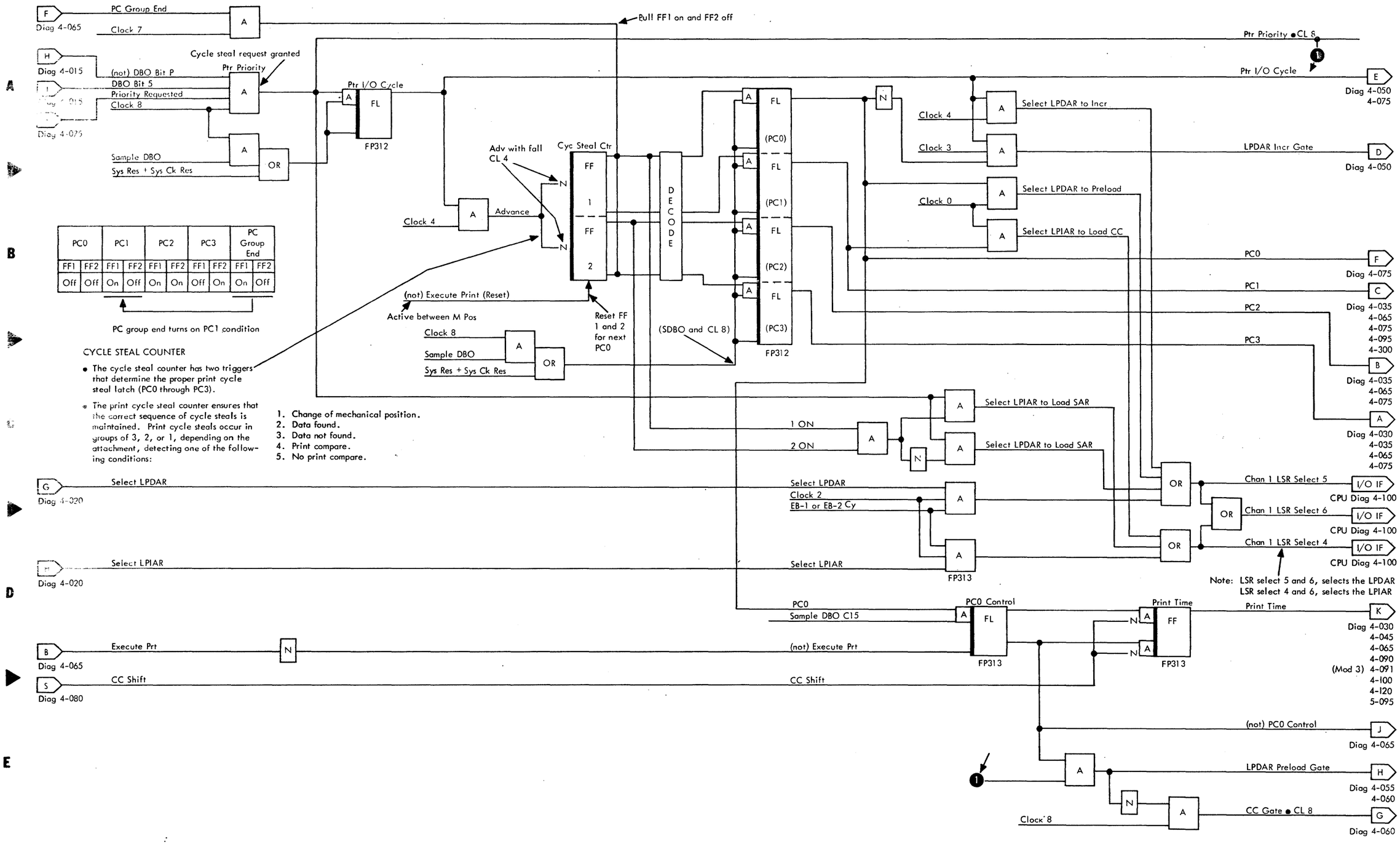


Diagram 4-060. DBI Assembler Bits 4-7


2
3
4
5
6
7
8
9
A
B
C
D
E
I-R Cycle
Clock 8
L
(not) No-Op
Diag 4-035
D
Print
Diag 4-020
Reset + Prt Check
H
Hmr + Incr Failure Ck
Diag 4-025
A
Stop Printing 48
Diag 4-090, 4-091 (Mod 3)
A
Stop Printing UCS
Diag 4-300
D
Last M Position of Line
Diag 4-085
Sample DBO
E
M4
Diag 4-085
(100 LPM)
100 LPM + 200 LPM
(200 LPM)
B
LPDAR Preload Bits 1 • 2 • 3 • 4 (M1 or M4)
Diag 4-115
F
1st Prt Start in Dwell
Diag 4-085
J
(not) PC0 Control
Diag 4-070
K
Print Time
Diag 4-070
Clock 0
E
Chain Em SS W-O Home
Diag 4-080
PC1
C
Diag 4-070
B
Force PC Group End
Diag 4-110
C
No Data
Diag 4-015
E
(not) Print Compare
Diag 4-015
B
PC2
Diag 4-070
A
PC3
Diag 4-070
K
Last 12 Prt Positions
Diag 4-115
C
Load HAR
Diag 4-110
C
Diag 5-075
A
OR
N
FL
FP314
Print
Execute Prt
Request PC0
Clock 4
Clock 6
Clock 2
Start Printing • I-R • CL 8
To use meter
G
Diag 5-095
Print Latch
Diag 4-020
Execute Prt
B
Diag 4-030
4-040
4-120
(not) Print Latch
C
Diag 4-025
5-225
Chan 1 Cyc Steal Req 5
I/O IF
CPU Diag 4-100
Priority Request
D
Diag 4-075
Cyc Steal Req
Reset of Lockout FL allows Request Time FL to be set and the next print positions PC's to be taken after Load HAR (Hmr CL3).
Lockout
PC1
Off
Request Time
PC Group End
Lockout off and clock 2
Prt Cyc Req
Last PC Group
Request Time
Clock 6
PC Group End
E
Diag 4-095
F
Diag 4-070
4-075



PC0		PC1		PC2		PC3		PC Group End	
FF1	FF2	FF1	FF2	FF1	FF2	FF1	FF2	FF1	FF2
Off	Off	On	Off	On	On	Off	On	On	Off

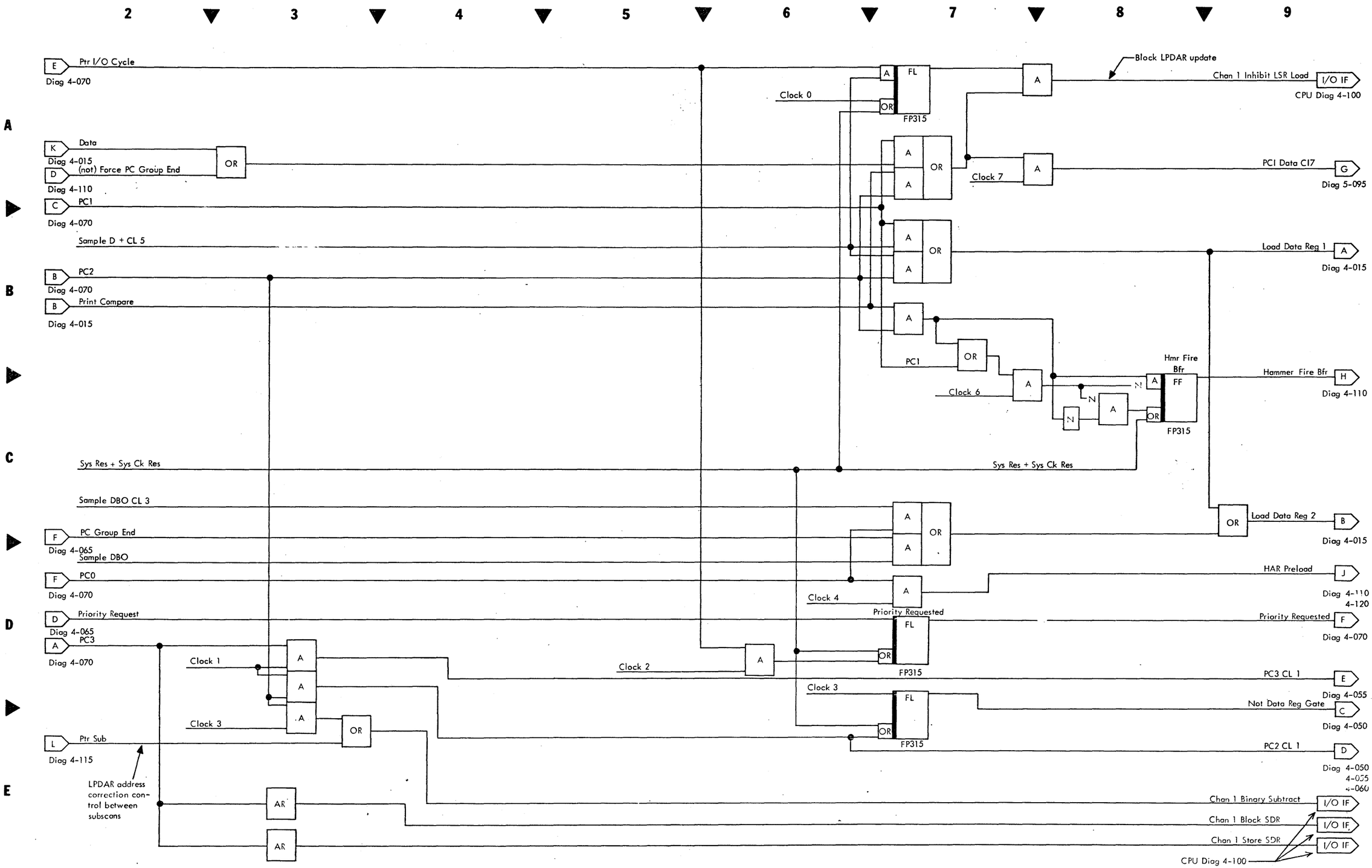
PC group end turns on PC1 condition

CYCLE STEAL COUNTER

- The cycle steal counter has two triggers that determine the proper print cycle steal latch (PC0 through PC3).
- The print cycle steal counter ensures that the correct sequence of cycle steals is maintained. Print cycle steals occur in groups of 3, 2, or 1, depending on the attachment, detecting one of the following conditions:

1. Change of mechanical position.
2. Data found.
3. Data not found.
4. Print compare.
5. No print compare.

Diagram 4-070. Cycle Steal Counter


2
3
4
5
6
7
8
9
A
B
C
D
E
Ptr I/O Cycle
Diag 4-070
Data
Diag 4-015
(not) Force PC Group End
Diag 4-110
PC1
Diag 4-070
Sample D + CL 5
PC2
Diag 4-070
Print Compare
Diag 4-015
Sys Res + Sys Ck Res
Sample DBO CL 3
PC Group End
Diag 4-065
Sample DBO
PC0
Diag 4-070
Priority Request
Diag 4-065
PC3
Diag 4-070
Ptr Sub
Diag 4-115
LPDAR address correction control between subscans
Clock 0
Clock 1
Clock 2
Clock 3
Clock 4
Clock 6
Clock 7
FL
FP315
OR
AR
PC1
Block LPDAR update
Chan 1 Inhibit LSR Load
I/O IF
CPU Diag 4-100
PCI Data CI7
Diag 5-095
Load Data Reg 1
Diag 4-015
Hmr Fire Bfr
FF
Hammer Fire Bfr
Diag 4-110
Sys Res + Sys Ck Res
Load Data Reg 2
Diag 4-015
HAR Preload
Diag 4-110
4-120
Priority Requested
Diag 4-070
PC3 CL 1
Diag 4-055
Not Data Reg Gate
Diag 4-050
PC2 CL 1
Diag 4-050
4-055
4-060
Chan 1 Binary Subtract
Chan 1 Block SDR
Chan 1 Store SDR
CPU Diag 4-100

C M1 — Diag 4-085 — M1
G M2 — Diag 4-085 — M2
H M3 — Diag 4-085 — M3
E M4 — Diag 4-085 — M4

PSS1	PSS2	PSS3	PSS1	PSS2	PSS3	CC increment bit 1 set in 4 bit shift register at PSS2
M4	M1	M3	M2	M3	M1	CC Incr Bit 2
M2	M3	M1	M3	M4	M2	CC Incr Bit 4
					M4	CC Incr Bit 8
M2	M3	M4	M3	M4	M1	Preload Hmr CL 1 or 2
M1	M2	M3	M2	M3	M4	Preload Hmr CL 1 or 4
M4	M1	M2	M3	M4	M1	Preload Hmr CL 2 or 3
M1	M2	M3	M4	M1	M2	Preload Hmr CL 3 or 4

Hmr Clk Start
Hmr

M1	SS1	4	1	M3	SS1	2	7
	SS2	3	5		SS2	1	11
	SS3	2	9		SS3	4	3
M2	SS1	1	10	M4	SS1	3	4
	SS2	4	2		SS2	2	8
	SS3	3	6		SS3	1	12

B

C Diag 4-300 — UCS Home, 48 Ch Set → OR
N Diag 4-115 — Overrun Delay
I/O IF — Chain Em pulse from 5203
See Timing Diagram 4-310 — 300 Micro S Home Gate SS, 320 Ns Chain Emitter SS

1 of 3 triggers always off. Trigger off indicates active subscan. Counter is reset to 3

PSS Counter: FF PSS1, FF PSS2, FF PSS3 — FP404
Home Latch FL — FP404
Reset
(step)
A, N

M Pos and PSS Decode — FP403

PSS1, PSS2, PSS3

C Diag 4-300 — UCS Home, 48 Ch Set → OR
N Diag 4-115 — Overrun Delay
I/O IF — Chain Em pulse from 5203
See Timing Diagram 4-310 — 300 Micro S Home Gate SS, 320 Ns Chain Emitter SS

Block CC Shift: A, FL, OR — FP404
Reset CC

CC Incr Bit 4 → F Diag 4-095
Preload Hmr CL 2 or 3 → M Diag 4-100
CC Incr Bit 2 → H Diag 4-095
Preload Hmr CL 1 or 2 → N Diag 4-100
Preload Hmr CL 3 or 4 → P Diag 4-100
CC Incr Bit 8 → K Diag 4-095
Preload Hmr CL 1 or 4 → Q Diag 4-100
N (not) PSS1 → C Diag 4-040, 4-300
PSS2 → B Diag 4-030, 4-080 4-090, (Mod 3) 4-091, 4-095
PSS3 → R Diag 4-080, 4-090 (Mod 3) 4-091 4-095
Reset CC → A Diag 4-025 4-095
CC Shift → S Diag 4-090, (Mod 3) 4-091 4-095, 4-300, 4-070
Chain Em SS W-O Home → E Diag 4-065 4-095 4-100 4-105 4-110
Home Latch → D Diag 4-045

PRINT SUBSCAN COUNTER

- The print subscan counter is a three-position trigger ring that identifies the print subscan in process.
- A chain emitter pulse from the printer advances the print subscan counter.

2 3 4 5 6 7 8 9

A B C D E

Gate Incr Sync Ck

OR

B
Power On Busy
Diag 4-205

Incr Sync Check
A
Diag 4-025

N A FF 8
Start Sys Sys Ck Res

This comes from the Printer Reed Switch

I/O IF
Hmr Bar Right
Printer

Hmr Bar Right
FL
FP401

N
A

P FF 7
FP401

Print Start SS

MECHANICAL POSITION COUNTER

- The mechanical position counter (M counter) has six triggers.
- The triggers are advanced by the 'print start' singleshot at the completion of each mechanical print position change in the printer.
- M counter output is decoded to determine the mechanical position (M position) of the incrementer cam.
- M counter output is decoded along with the print sub-scan to determine the initialization value of the four-bit shift register (see "Chain Character Counter"), and develop hammer clock times.
- The M position is decoded to determine what bit structure is to be preloaded into the LPDAR in order to determine the first print position to be optioned for printing.

Scan 45
Scan 42 (Mod 3)

Hmr Bar Right
M1
M2
M3
OR
N
A
Pull FF ON

Hmr Bar Right
M2
A

See Timing Chart
4-340
4-350

M Position Counter

FF 1 FF 2 FF 3 FF 4 FF 5 FF 6

Advance (1-2)
Advance (3-6)
N

100 LPM
200 and 300 LPM
A
A

Print Start
I/O IF
Intf Print Start Em
(Incrementer EM)
Printer
SS
FP201
Print Start SS
N

Decode
FP402

1st Prt Start In Dwell
2nd Prt Start In End Dwell
Gate Incr Sync Ck

Active at middle of M4 and M1 for 200 and 300 LPM

Active if not in M1 for 100 LPM
Active if not in M3 for 200 and 300 LPM

1st Prt Start In Dwell
F
Diag 4-065
4-300

100 LPM
A
OR
100 LPM 1st Prt St or 2nd
J
Diag 4-205

M1
C
Diag 4-045
4-080
4-115

M2
G
Diag 4-080
4-115

M3
H
Diag 4-080
4-115

M4
E
Diag 4-065
4-080
4-115

Last M Pos of Line
D
Diag 4-065

Print Start SS
B
Diag 4-040
4-090
(Mod 3) 4-091

Both AND's active for 200 and 300 LPM

200 and 300 LPM
M Pos Trig 3
M Pos Trig N4
M Pos Trig N3
M Pos Trig 4
A
A
OR
Active 100 LPM

Start Printing • I-R • CL 8
P FF 9

100 LPM

Closing Hammer Bar Rt Switch sets FF2 and FF3 on. The M position counter is advanced by a Print Start Pulse.

	FF1	FF2	FF3	FF4	FF5	FF6	Switch Closed	Switch Open
M4	x		x	x			x	
M3		x	x	x	x			x
M2	x		x	x	x	x		x
M1		x		x	x	x		x

'Last M position' is set by FF3 off and FF4 going on.

200 and 300 LPM

Closing Hammer Bar Rt Switch set FF1 on.

	FF1	FF2	FF3	FF4	FF5	FF6	Switch Closed	Switch Open
M4		x	x				x	
M4	x		x	x			x	
M3		x	x	x	x			x
M2	x		x	x	x	x		x
M1		x		x	x	x		x
M1	x				x	x		x
M2		x				x		x
M3	x							x
M4		x	x				x	

'Last M position' is set by either (1) FF4 on and FF3 going off or (2) FF4 off and FF3 going on.

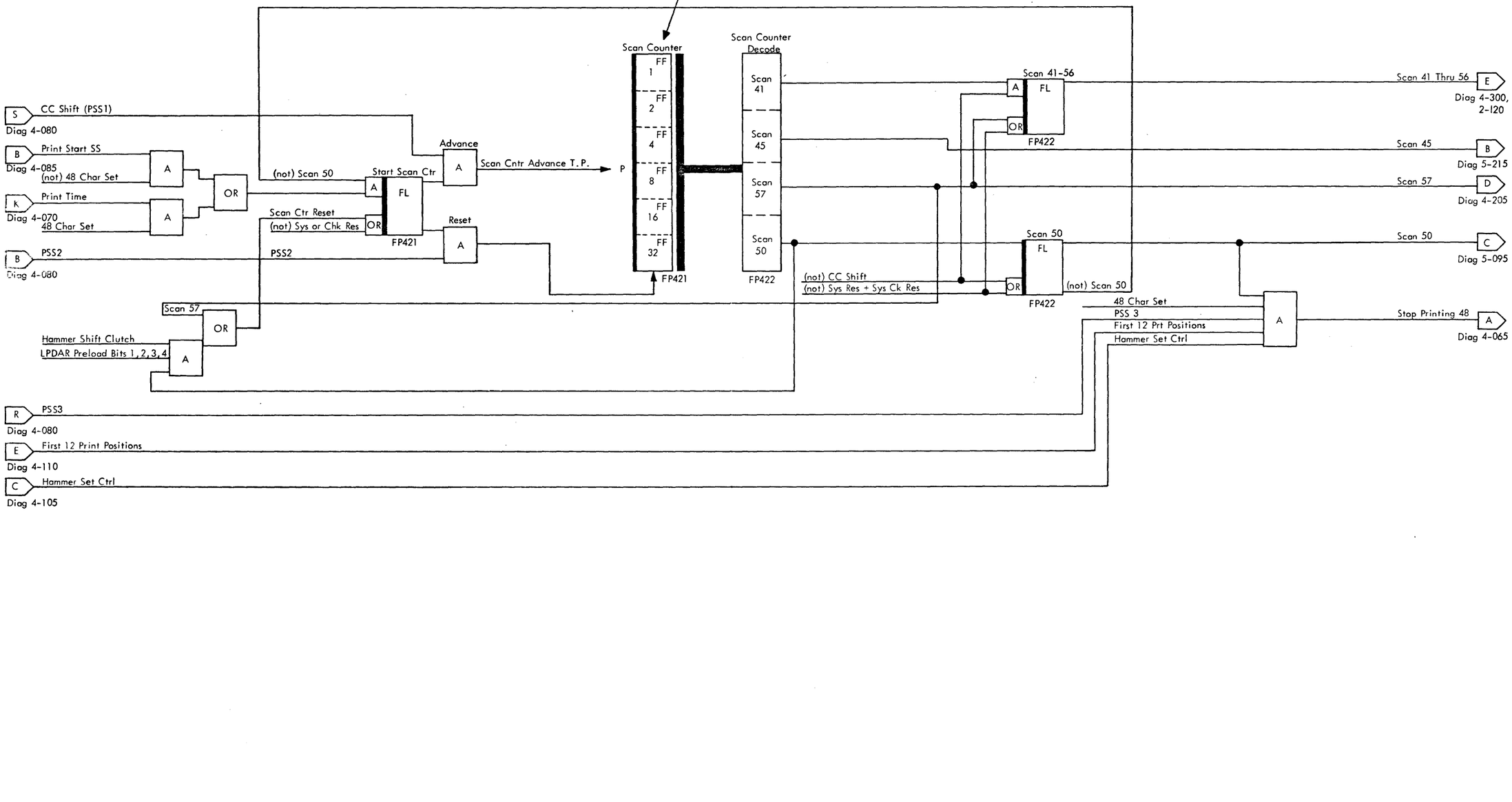
2 3 4 5 6 7 8 9

A B C D E

SCAN COUNTER

The following description of the scan counter is for the standard 48 character set only.

- The scan counter is a six-stage binary counter.
- Triggers are reset off after printing.
- A CC shift at the start of print subscan one (PSS1) advances the counter.
- The scan counter reaching 45 decodes a signal to pick the carriage clutch.
- The scan counter reaching 50 signals the end of printing for that mechanical position.
- The scan counter reaching 57 picks the incrementer clutch. (A count of 57 is reached only for the first line of printing in the last M position on a single space operation or for every line in the last M position on a double or triple space operation.)



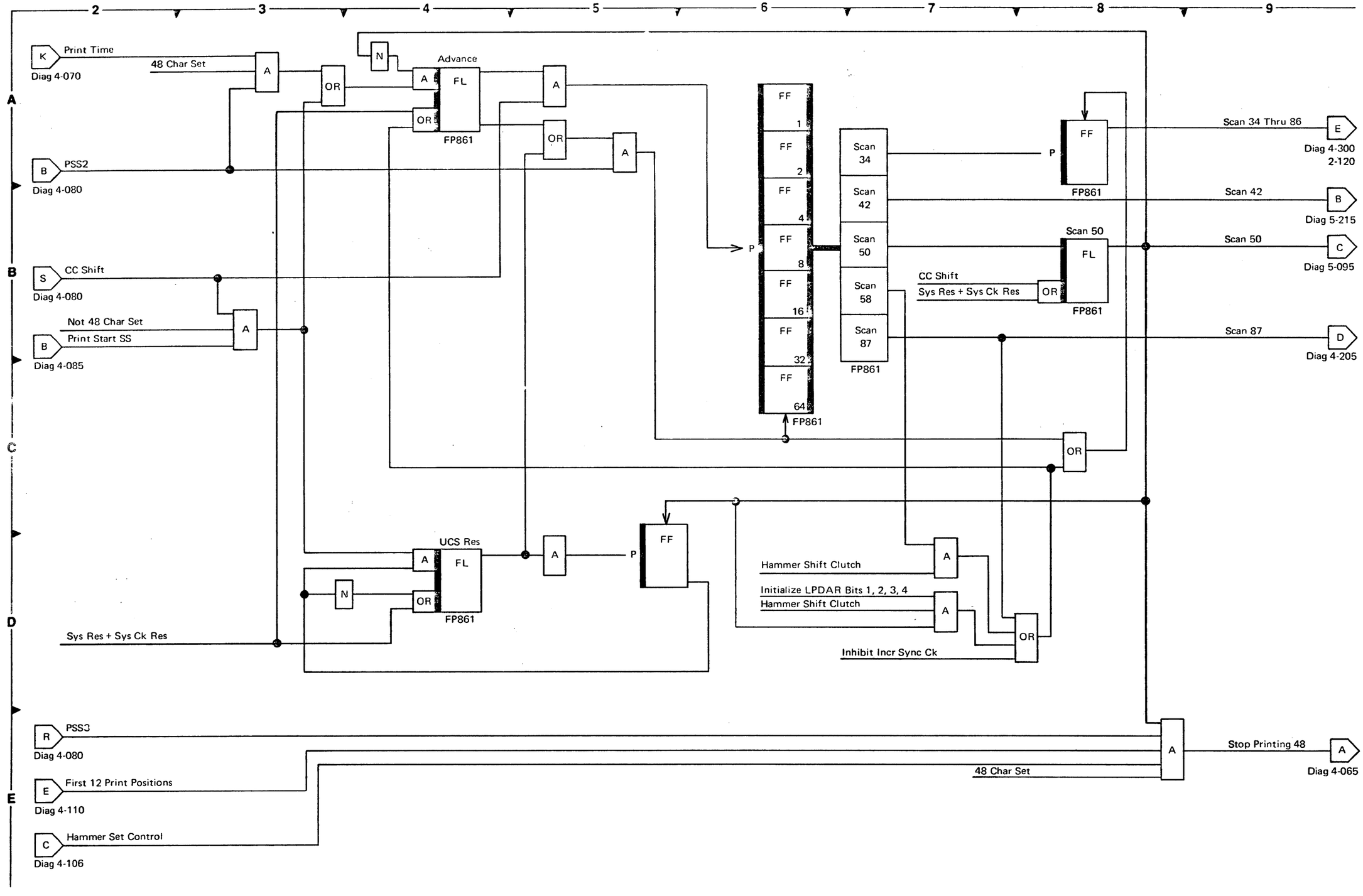
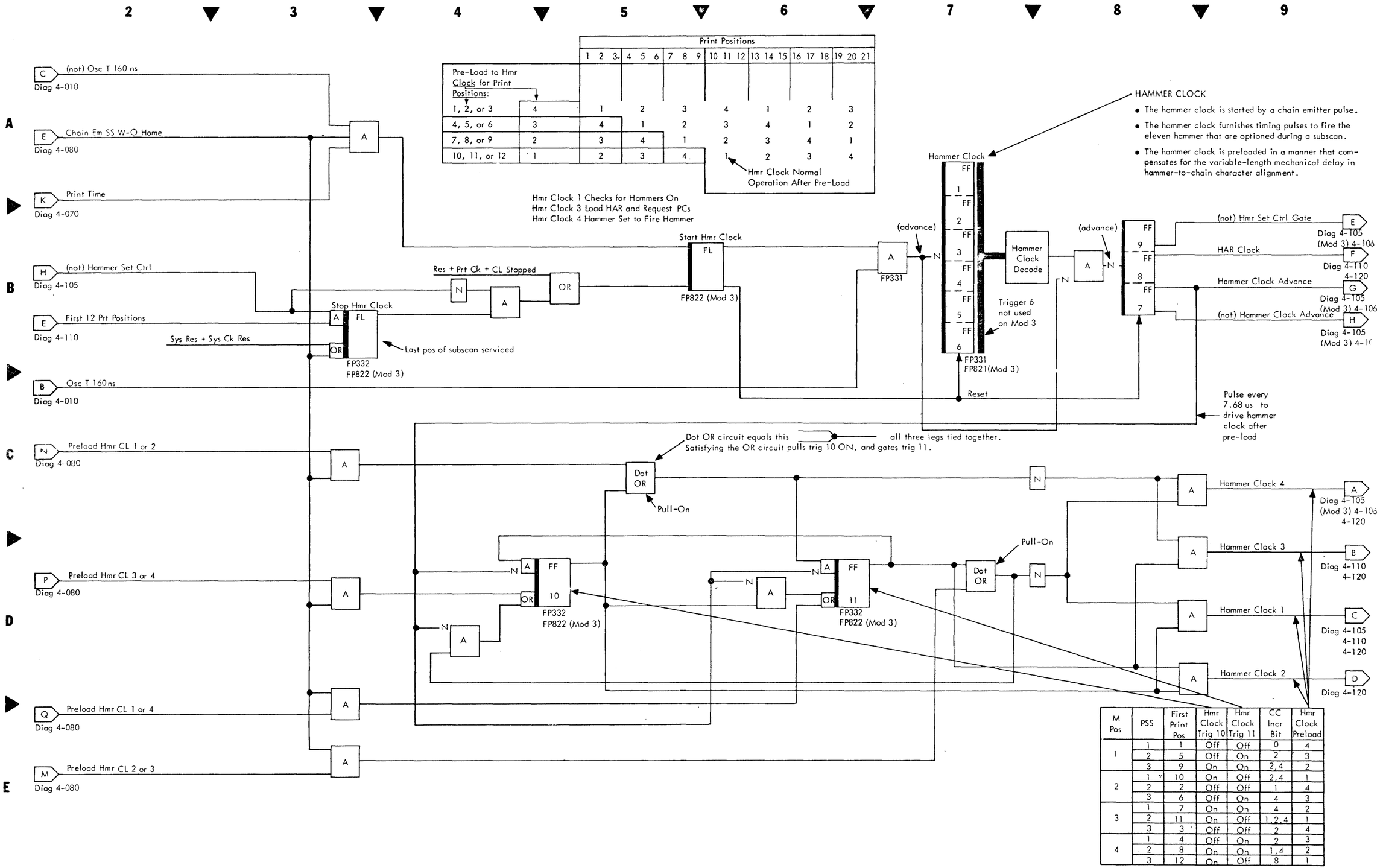


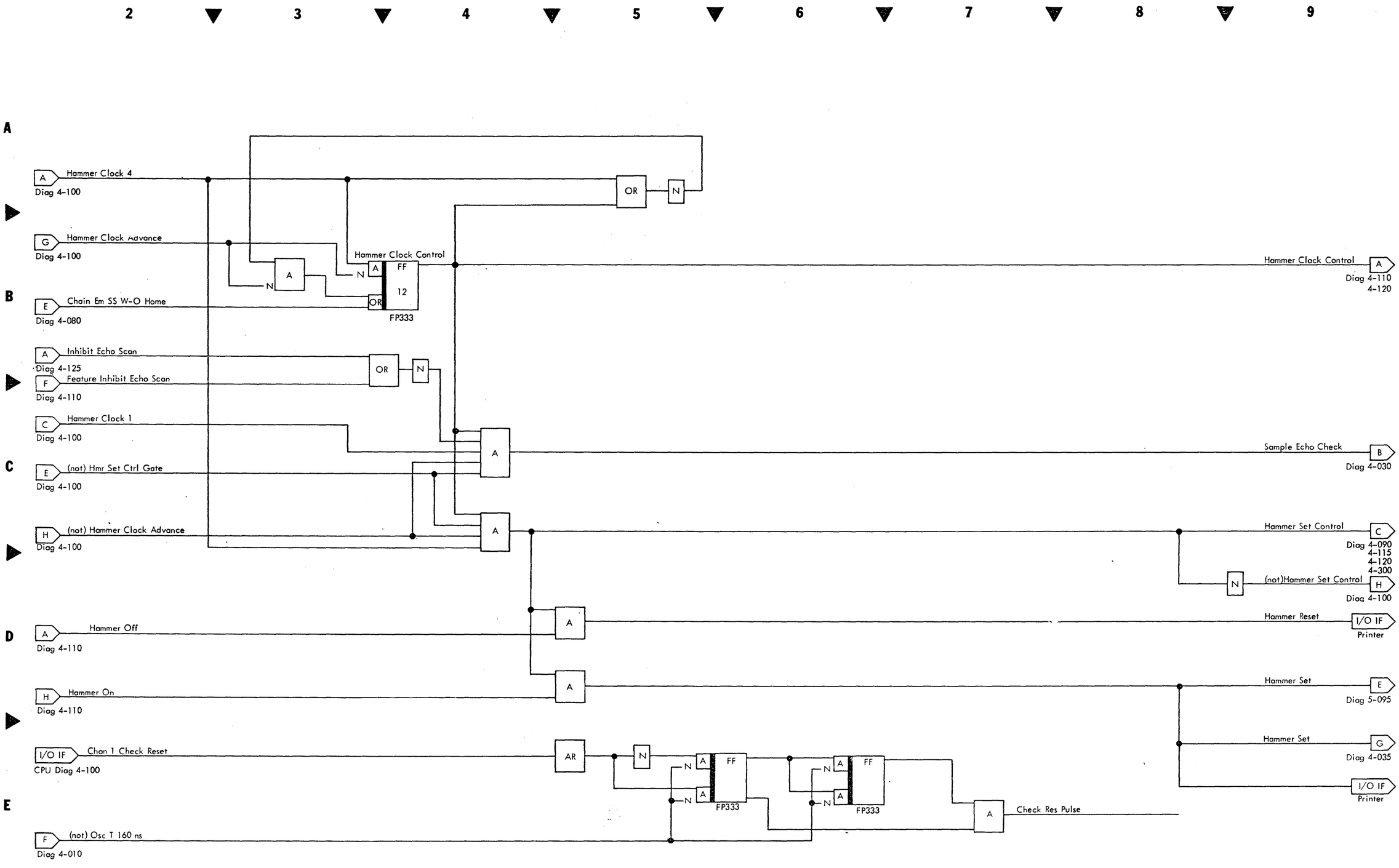
Diagram 4-091. Scan Counter and Decode–Model 3

M Pos	PSS	First Print Pos	Hmr Clock Preload	Hmr Clock Trig 10	Hmr Clock Trig 11	CC Incr Bit
1	1	1	4	Off	Off	0
	2	5	3	Off	On	1,2
	3	9	2	On	On	2,4
2	1	10	1	On	Off	2,4
	2	2	4	Off	Off	1
	3	6	3	Off	On	4
3	1	7	2	On	On	4
	2	11	1	On	Off	1,2,4
	3	3	4	Off	Off	2
4	1	4	3	Off	On	2
	2	8	2	On	On	1,4
	3	12	1	On	Off	8



M Pos	PSS	First Print Pos	Hmr Clock Trig 10	Hmr Clock Trig 11	CC Incr Bit	Hmr Clock Preload
1	1	1	Off	Off	0	4
	2	5	Off	On	2	3
	3	9	On	On	2,4	2
2	1	10	On	Off	2,4	1
	2	2	Off	Off	1	4
	3	6	Off	On	4	3
3	1	7	On	On	4	2
	2	11	On	Off	1,2,4	1
	3	3	Off	Off	2	4
4	1	4	Off	On	2	3
	2	8	On	On	1,4	2
	3	12	On	Off	8	1

Diagram 4-100. Hammer Clock and Controls


2
3
4
5
6
7
8
9
A
B
C
D
E
A Hammer Clock 4
Diag 4-100
G Hammer Clock Advance
Diag 4-100
E Chain Em SS W-O Home
Diag 4-080
A Inhibit Echo Scan
Diag 4-125
F Feature Inhibit Echo Scan
Diag 4-110
C Hammer Clock 1
Diag 4-100
E (not) Hmr Set Ctrl Gate
Diag 4-100
H (not) Hammer Clock Advance
Diag 4-100
A Hammer Off
Diag 4-110
H Hammer On
Diag 4-110
I/O IF Chan 1 Check Reset
CPU Diag 4-100
F (not) Osc T 160 ns
Diag 4-010
OR
N
A
Hammer Clock Control
FF
12
FP333
AR
Hammer Clock Control
A
Diag 4-110
4-120
Sample Echo Check
B
Diag 4-030
Hammer Set Control
C
Diag 4-090
4-115
4-120
4-300
(not)Hammer Set Control
H
Diag 4-100
Hammer Reset
I/O IF
Printer
Hammer Set
E
Diag 5-095
Hammer Set
G
Diag 4-035
I/O IF
Printer
Check Res Pulse

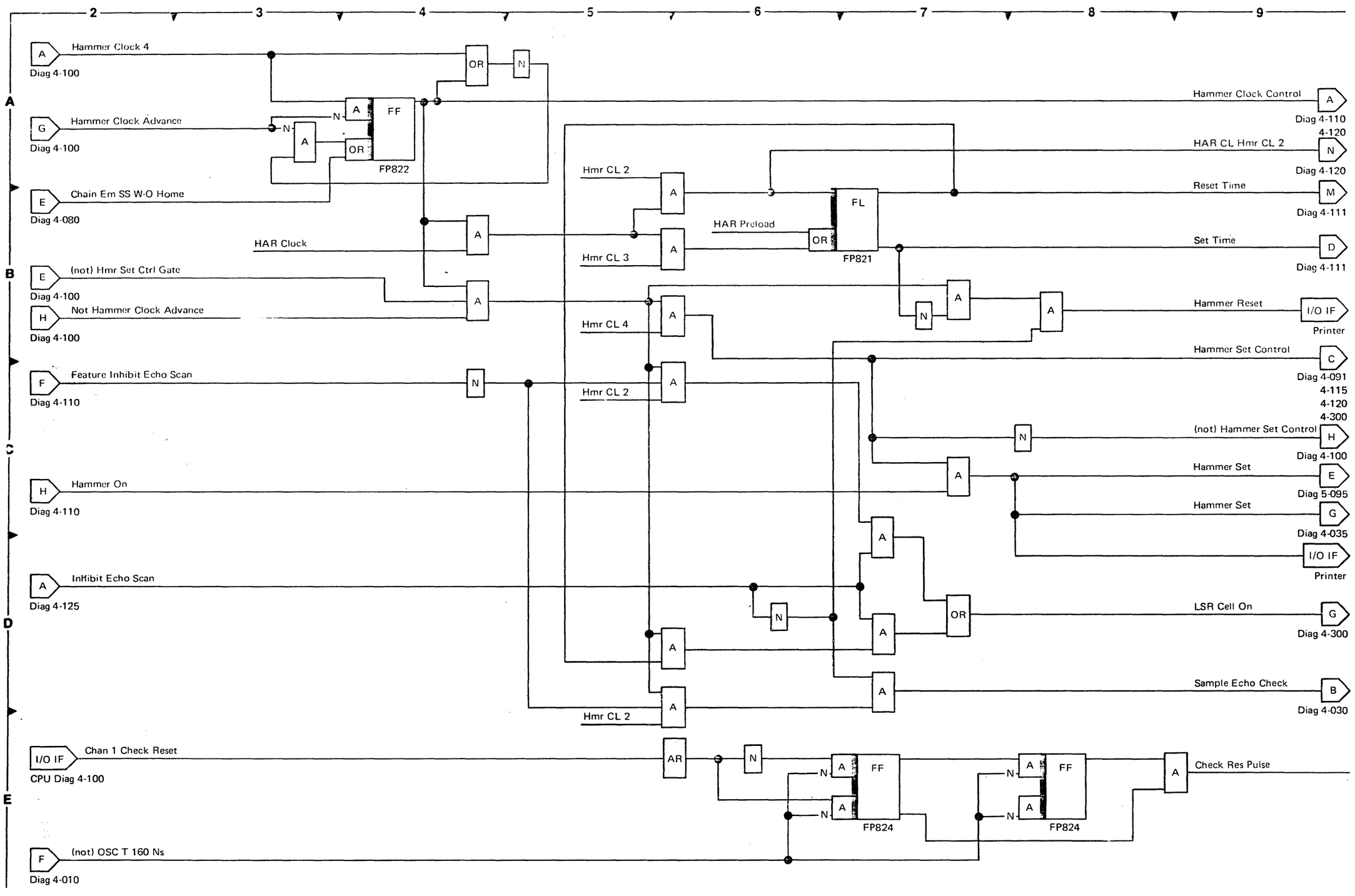
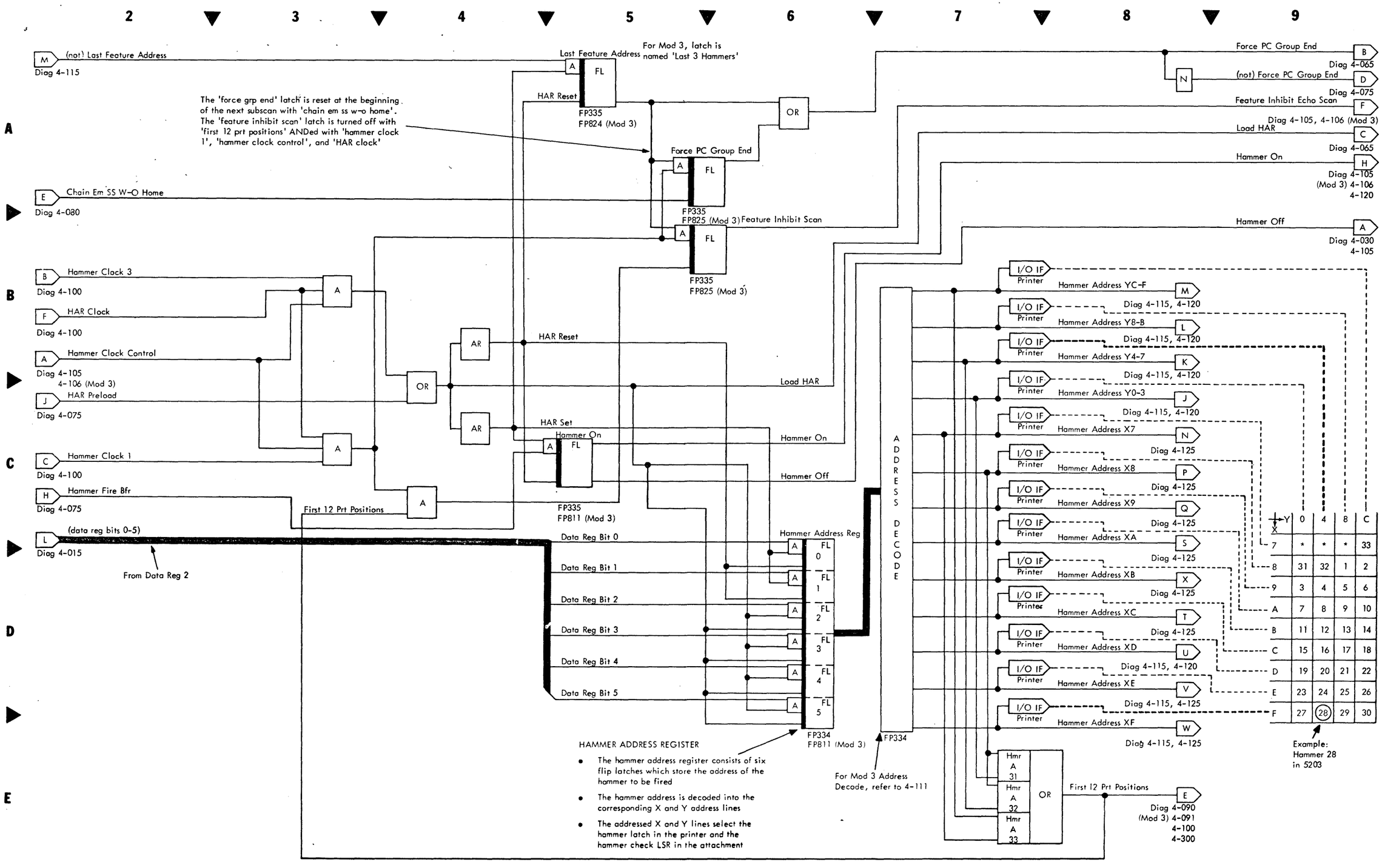
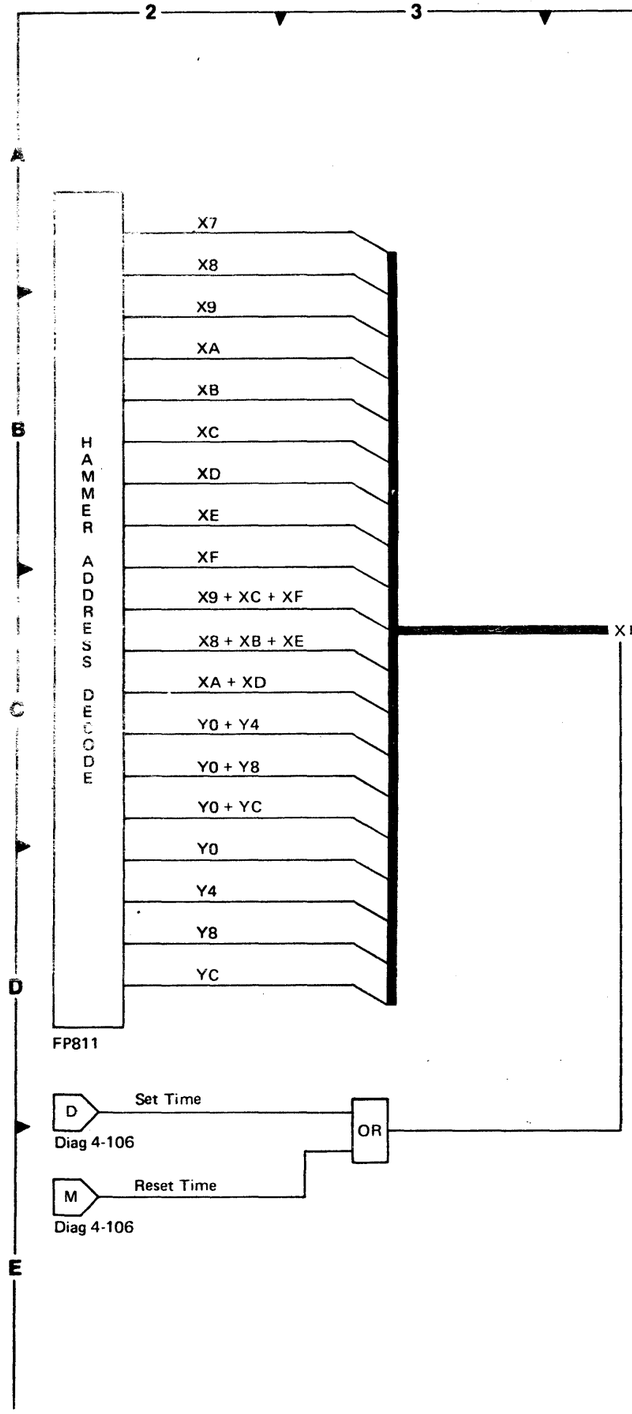


Diagram 4-106. Hammer Controls–Model 3



X \ Y	0	4	8	C
7	*	*	*	33
8	31	32	1	2
9	3	4	5	6
A	7	8	9	10
B	11	12	13	14
C	15	16	17	18
D	19	20	21	22
E	23	24	25	26
F	27	(28)	29	30



Hmr Address Set Lines	Hammer Set	Hmr Address Reset Lines	Hammer Reset
X8 • Y8	1	XA • Y4	8
X8 • YC	2	XA • Y8	9
X9 • Y0	3	XA • Y0	7
X9 • Y4	4	XB • Y0	11
X9 • Y8	5	XB • Y4	12
X9 • YC	6	XA • YC	10
XA • Y0	7	XB • YC	14
XA • Y4	8	XC • Y0	15
XA • Y8	9	XB • Y8	13
XA • YC	10	XC • Y8	17
XB • Y0	11	XC • YC	18
XB • Y4	12	XC • Y4	16
XB • Y8	13	XD • Y4	20
XB • YC	14	XD • Y8	21
XC • Y0	15	XD • Y0	19
XC • Y4	16	XE • Y0	23
XC • Y8	17	XE • Y4	24
XC • YC	18	XD • YC	22
XD • Y0	19	XE • YC	26
XD • Y4	20	XF • Y0	27
XD • Y8	21	XE • Y8	25
XD • YC	22	XF • Y8	29
XE • Y0	23	XF • YC	30
XE • Y4	24	XF • Y4	28
XE • Y8	25	X8 • Y4	32
XE • YC	26	X7 • YC	33
XF • Y0	27	X8 • Y0	31
XF • Y4	28	X9 • Y0	3
XF • Y8	29	X8 • Y8	1
XF • YC	30	X8 • YC	2
X8 • Y0	31	X9 • YC	6
X8 • Y4	32	X9 • Y4	4
X7 • YC	33	X9 • Y8	5

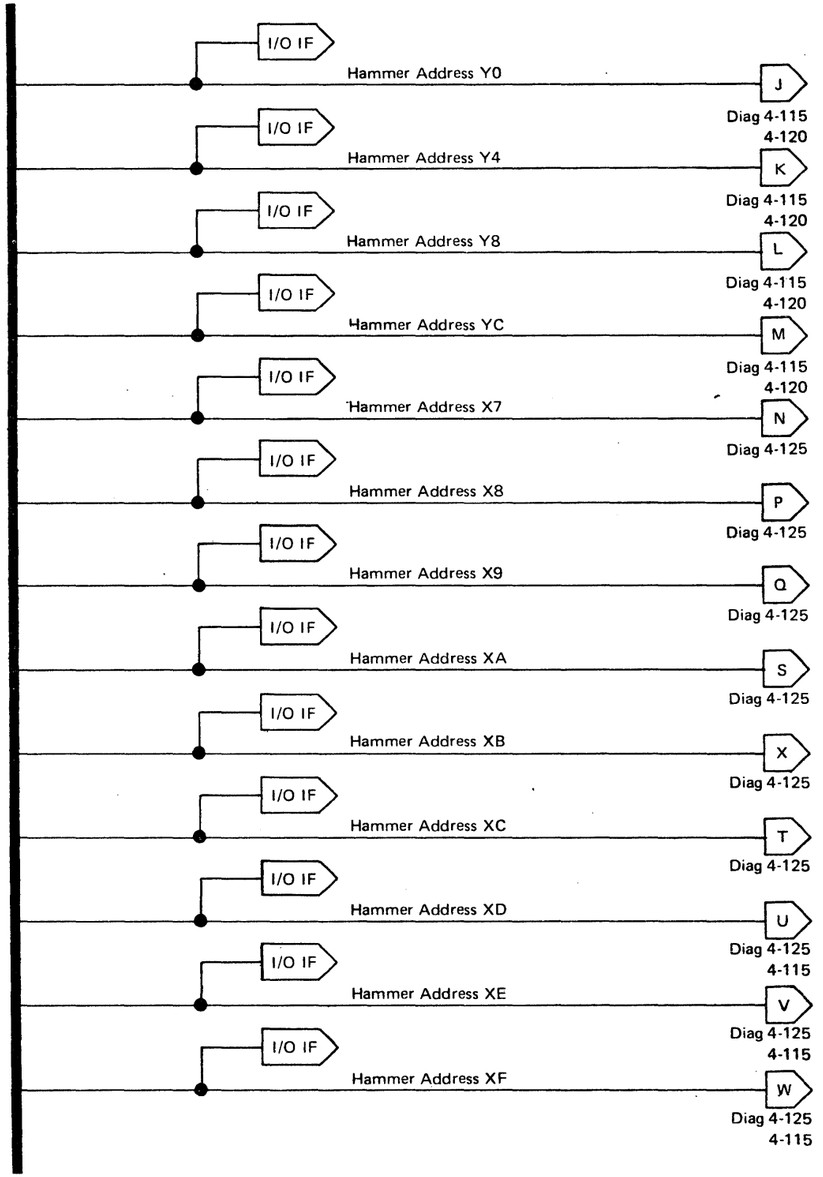


Diagram 4-111. Hammer Address Decode–Model 3

2 3 4 5 6 7 8 9

A

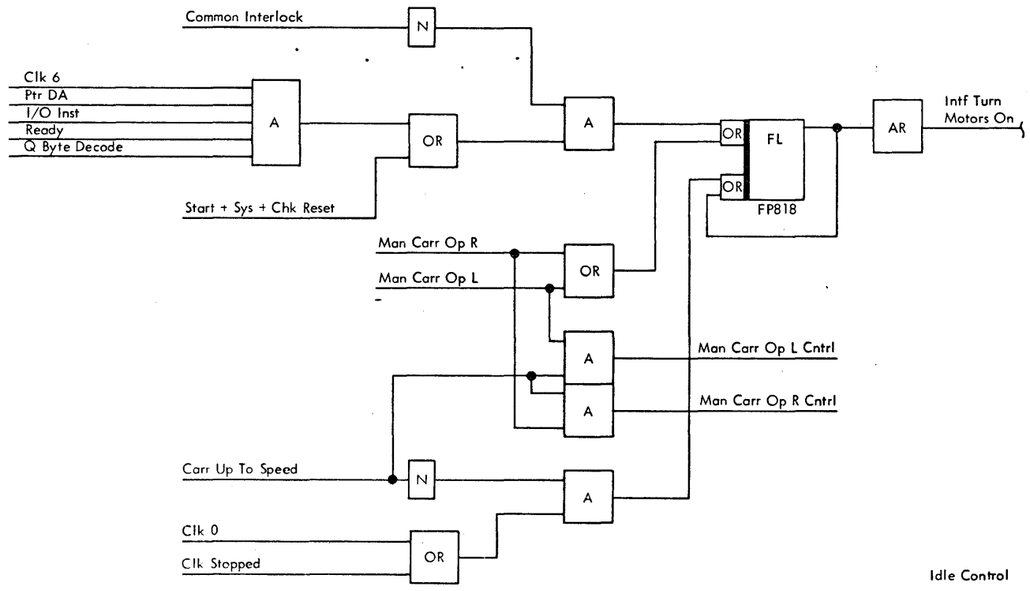
B

C

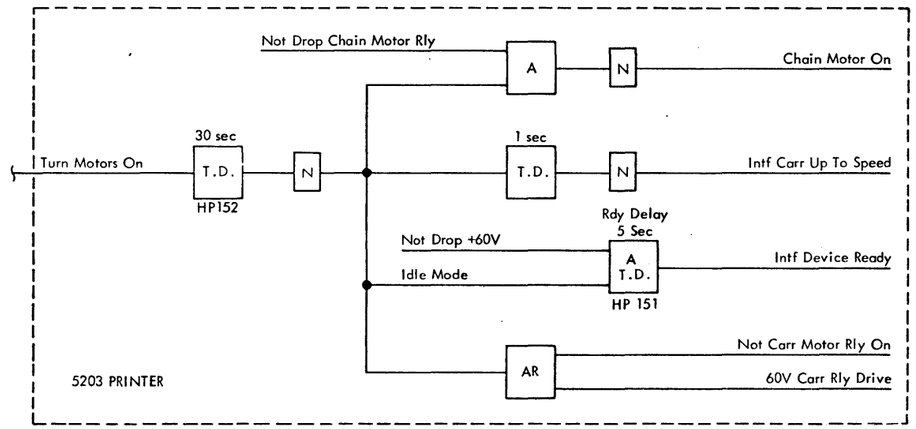
D

E

5203 ATTACHMENT



Idle Control



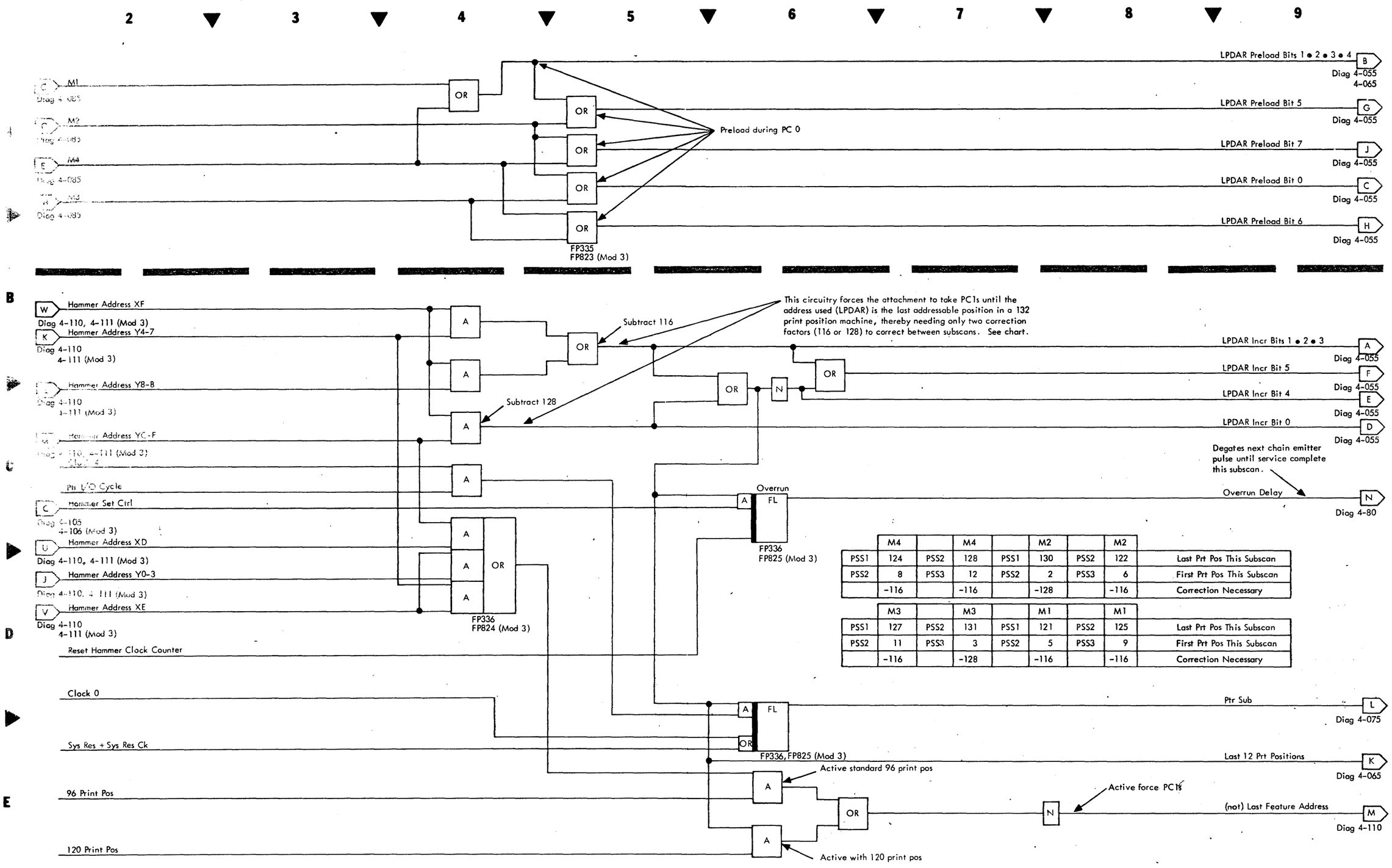
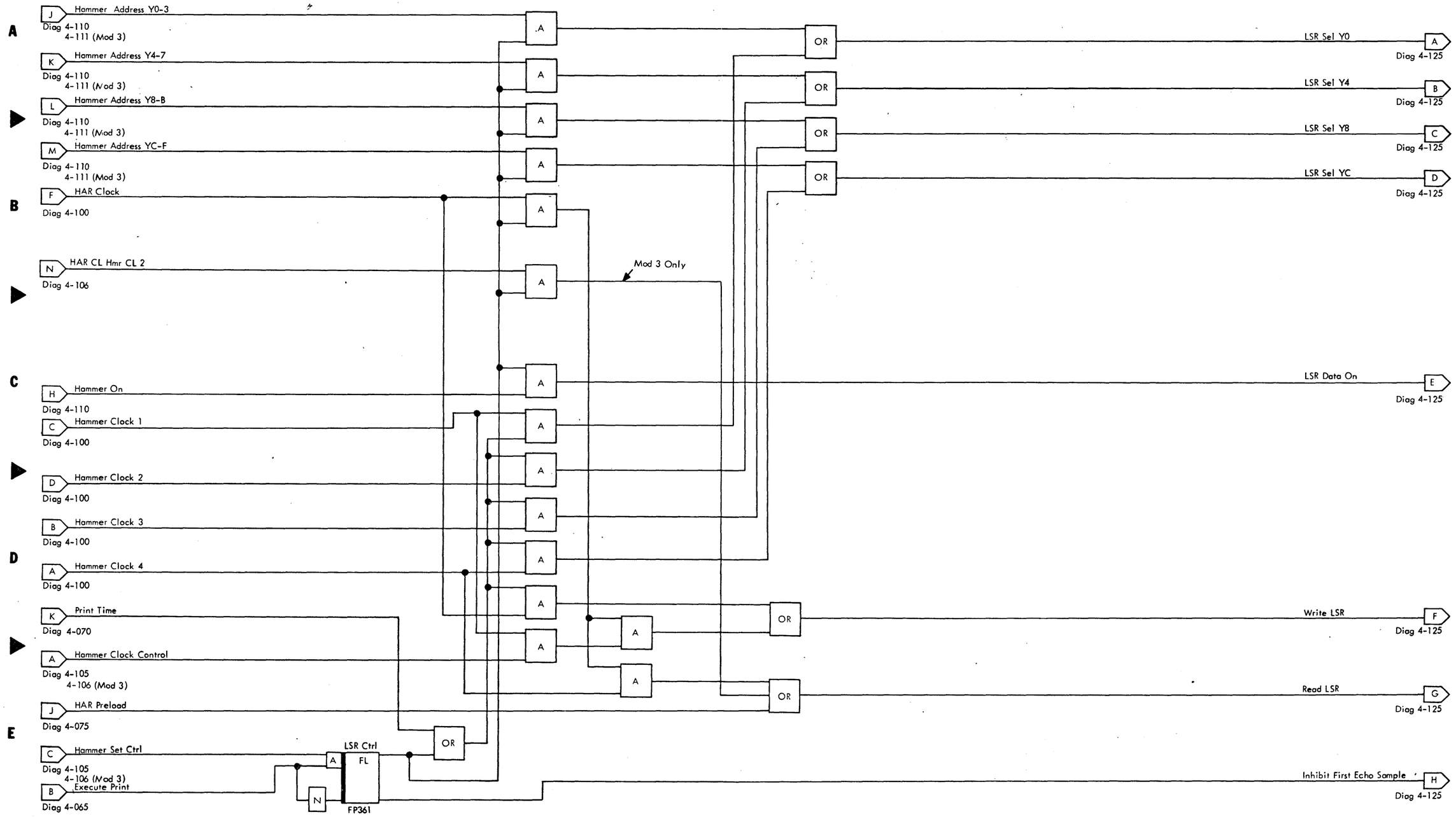


Diagram 4-115. Hammer Controls–LPDAR Preload and LPDAR Increment


2
3
4
5
6
7
8
9
A
B
C
D
E
J Hammer Address Y0-3
Diag 4-110
4-111 (Mod 3)
K Hammer Address Y4-7
Diag 4-110
4-111 (Mod 3)
L Hammer Address Y8-B
Diag 4-110
4-111 (Mod 3)
M Hammer Address YC-F
Diag 4-110
4-111 (Mod 3)
F HAR Clock
Diag 4-100
N HAR CL Hmr CL 2
Diag 4-106
H Hammer On
Diag 4-110
C Hammer Clock 1
Diag 4-100
D Hammer Clock 2
Diag 4-100
B Hammer Clock 3
Diag 4-100
A Hammer Clock 4
Diag 4-100
K Print Time
Diag 4-070
A Hammer Clock Control
Diag 4-105
4-106 (Mod 3)
J HAR Preload
Diag 4-075
C Hammer Set Ctrl
Diag 4-105
4-106 (Mod 3)
B Execute Print
Diag 4-065
A
OR
Mod 3 Only
LSR Ctrl
FL
FP361
N
LSR Sel Y0
Diag 4-125
LSR Sel Y4
Diag 4-125
LSR Sel Y8
Diag 4-125
LSR Sel YC
Diag 4-125
LSR Data On
Diag 4-125
Write LSR
Diag 4-125
Read LSR
Diag 4-125
Inhibit First Echo Sample
Diag 4-125

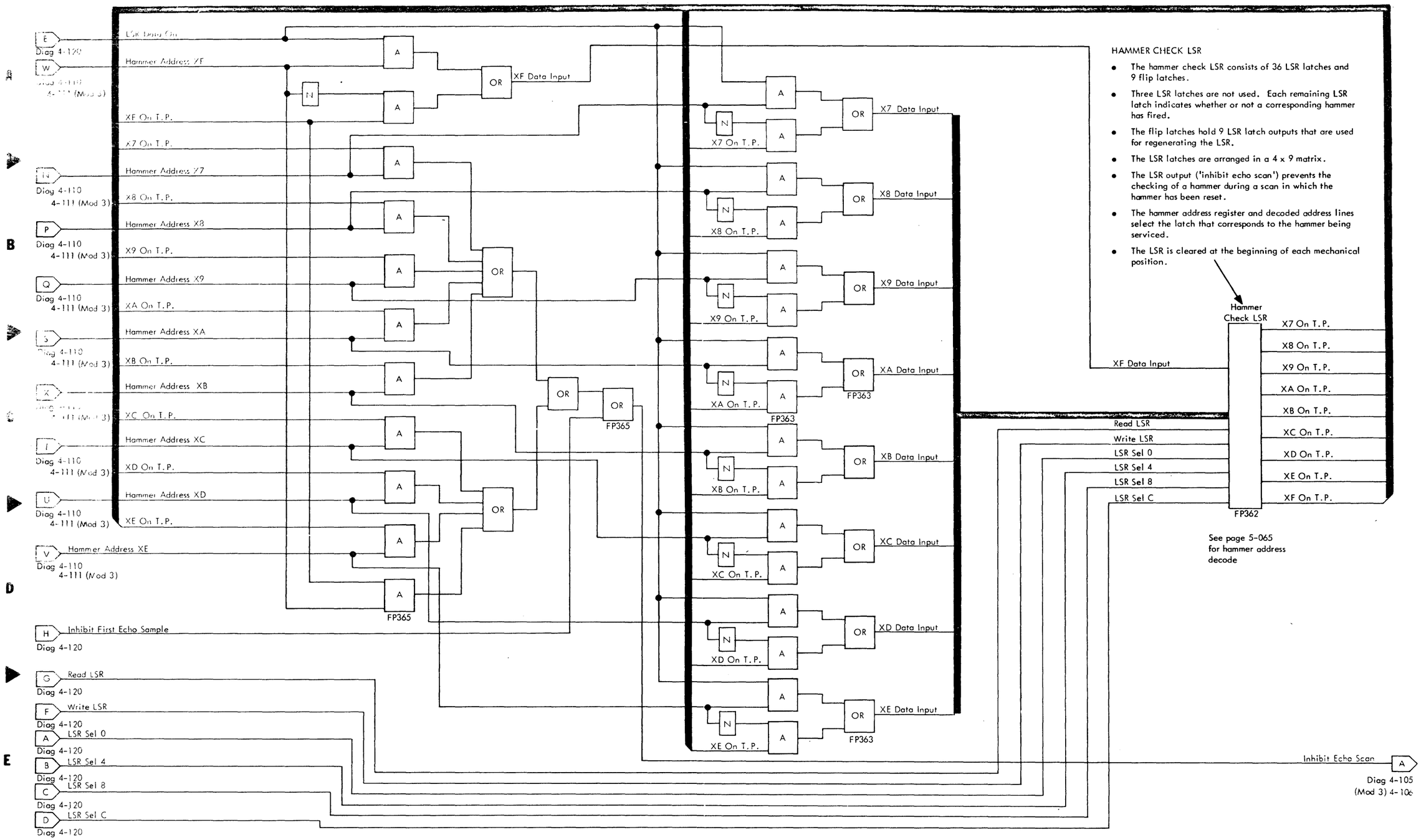


Diagram 4-125. Hammer Check LSR and Regen

2 3 4 5 6 7 8 9

A

Error Res
End of Restore
FF
Hmr Bar Right
P
This comes from the printer reed switch
FP501
A
Device Ready
A
Incr Restore
FL
Error Res
FP501
Ready applies to ready light after pressing start key
Ready
(not) Device Ready
A
OR
Power On Busy
B
Diag 4-085
Device Ready applies to the internal circuitry of the 5203

B

J
Diag 4-085
100 LPM 1st Prt St or 2nd
D
Scan 57 Scan 87 (Mod 3)
Diag 4-090
4-091 (Mod 3)
OR
N

C

B
UCS Incr Clutch Control
Diag 4-300
OR
(not) Start + Sys + Sys Ck Res
Device Ready
A
OR
A
I/O IF
Printer
Hammer Shift Clutch
A
Diag 4-090
N
(not) Hammer Shift Clutch
C
Diag 2-130

D

A
Print Latch
Diag 4-065
(not) L Carriage Moving
(not) R Carriage Moving
48 Ch Set
(not) Clock Stopped
A
N
N
A
Sys Res + Sys Ck Res
48 Incr Cntrl
A
N
FF
OR
FP501

E

M DBO Bits (1-7)
Diag 4-015

F Carr Line Bit (1-7)
Diag 4-220

A Verified Carr EM
Diag 4-220

C SIO Skip Command
Diag 4-020

A Select Carr
Diag 4-020

B SIO Space Command
Diag 4-020

A
A
OE
A

Sample DBO CL 5
1-R Cycle

A
FP625 *
FP715

A
FP624 *
FP714

Load Carr Space-Skip Register

DBO Bit 1
DBO Bit 2
DBO Bit 3
DBO Bit 4
DBO Bit 5
DBO Bit 6
DBO Bit 7
DBO Parity Error

A FL
FP621 *
FP711

OE
Carr Line Bit 1
Carr Line Bit 2
Carr Line Bit 3
Carr Line Bit 4
Carr Line Bit 5
Carr Line Bit 6
Carr Line Bit 7

A
FP621 *
FP711

Skip Stop
A
Diag 5-215

Carriage Parity Error

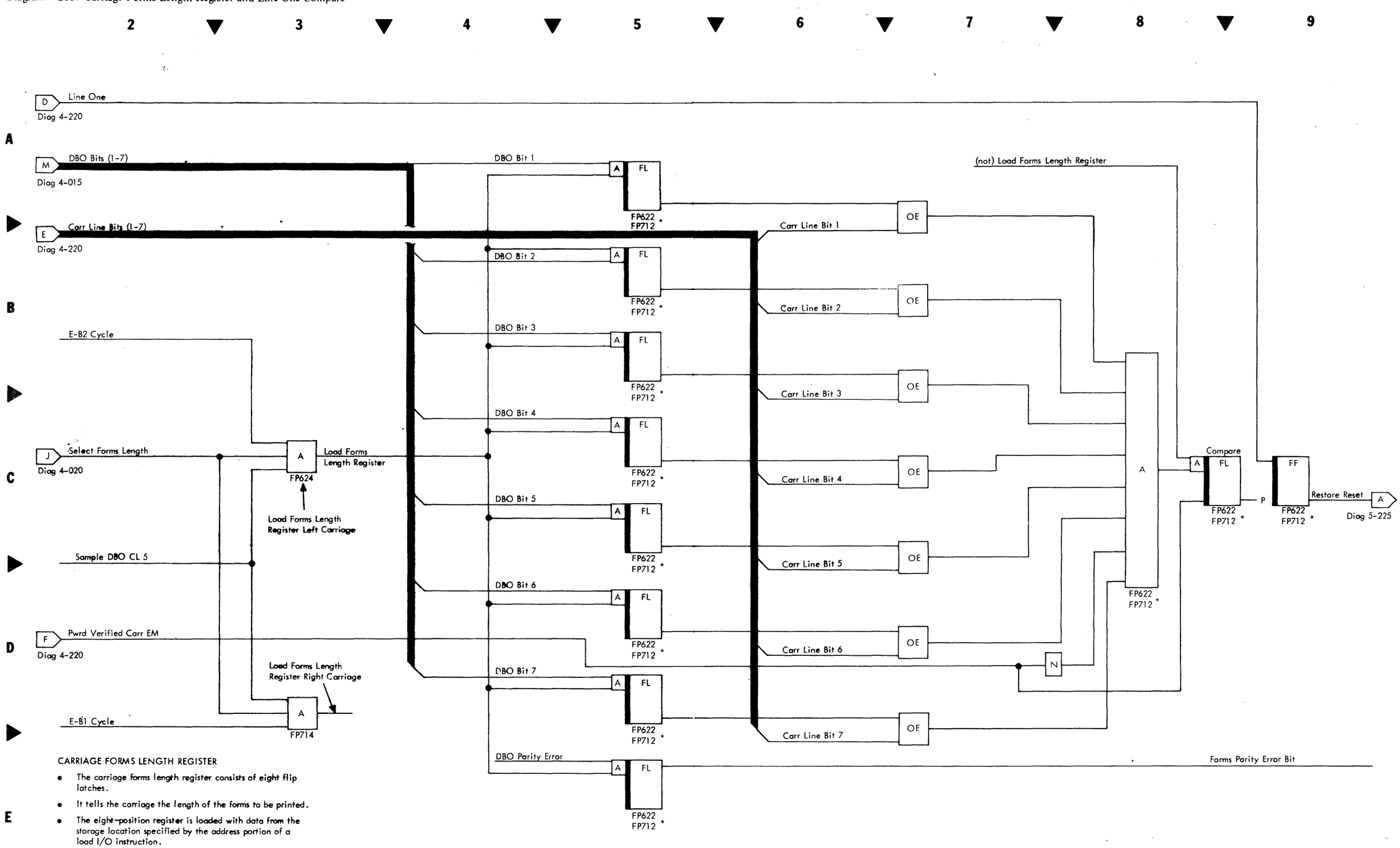
CARRIAGE SPACE-SKIP REGISTER

- The carriage space-skip register consists of eight flip latches.
- It tells the carriage how many lines to space or the line to which the carriage should skip.
- The eight-position register is set to the control field of an SIO instruction.
- Outputs are compared to the space counter to stop the printer carriage on a space operation.
- Outputs are compared to the line counter to stop the printer carriage on a skip operation.

*Left or Right Carriage

Diagram 4-210. Carriage Space-Skip Register and Line Compare

Diagram 4-215. Carriage Forms Length Register and Line One Compare



CARRIAGE FORMS LENGTH REGISTER

- The carriage forms length register consists of eight flip latches.
- It tells the carriage the length of the forms to be printed.
- The eight-position register is loaded with data from the storage location specified by the address portion of a load I/O instruction.

* Left or Right Carriage

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A

EMITTER GENERATE COUNTER

- The emitter generate counter consists of three binary triggers.
- The counter:
  1. Ignores a false carriage emitter pulse.
  2. Generates a pulse detection gate to look for an extra emitter pulse.
  3. Generates a verified carriage emitter pulse.

B

CARRIAGE MOVING COUNTER

- The carriage moving counter consists of nine binary triggers.
- It prevents printing for 12 ms after a carriage operation.
- It degates any false emitter pulse (noise) for approximately 5 ms after the carriage clutch is picked.
- It is used for every carriage operation (space, skip, restore).

C

CARRIAGE OSCILLATOR COUNTER

- The carriage Oscillator Counter converts a 160 ns input to a 49.92 us output.
- The outputs:
  1. Drive the emitter generate counter and carriage moving counter.
  2. Step the home gate singleshot reset ring.

D

CARRIAGE LINE COUNTER

- The line counter consists of seven binary triggers.
- The counter accumulates the number of lines printed, spaced, and skipped.
- The counter triggers are reset on.
- The counter advances a value of one for every carriage emitter pulse.

E

I/O IF Printer — Carriage Emitter

Emitter Unverified — FL — A / OR — FP612 FP702 *

3 — A

Reset On — Emitter Generate Ctr 1 2 3 — FP612 FP702 *

N

Checking for noise on carriage emitter line

T, 2, 3 — A — OR

Extra emitter pulse detection gate

1, 2, 3 — A — Checking Space — G — Diag 5-215

T, 2, 3 — A — Verified Carr Em — A — Diag 4-210 5-215

3 — Latch Reset

Accept Emitter — FL — FP613 FP703 *

Carr Clutch

Start + Rst + Sys Ck Reset

Carriage Moving — FL — OR — FP613 FP703 *

A

POR — N — OR

Carriage Moving Ctr 6 7 8 9 10 11 12 13 14 — 5 ms — 12 ms — FP613 FP703 *

A

N — A — Carriage Sync Check — Missed an emitter pulse — B — Diag 4-030

A

B — Osc T 160 ns — Diag 4-010

Carriage Oscillator Ctr 1 2 3 4 5 6 7 8 9 10 11 12 — FP601

Osc T 49.92 us

Pwrd Verified Carr Em — F — Diag 4-215

Reset On — Carriage Line Ctr 1 2 3 4 5 6 7 — FP612 FP702 *

(to DBI assembler carriage line bits 1-7) — C — Diag 4-055 4-060

Applies to left or right hand carriage

Carr Line Bits (1-7) — E — Diag 4-210 4-215

N

A — Restore Reset — Diag 5-225

POR — OR — (reset on)

A — FP623 FP713 * — Line One — D — Diag 4-215

* Left or Right Carriage

Diagram 4-220. Carriage Counters and Controls

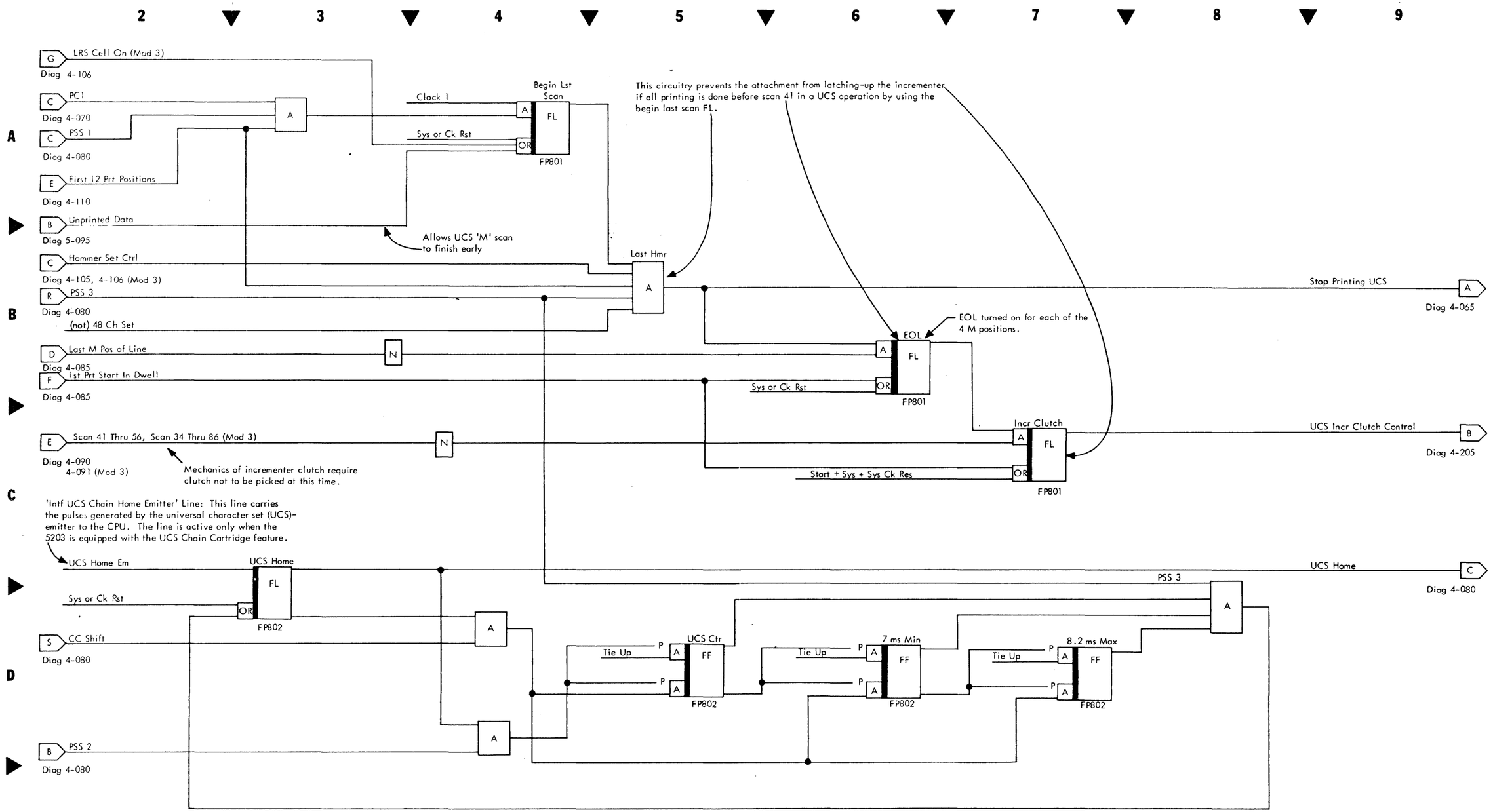


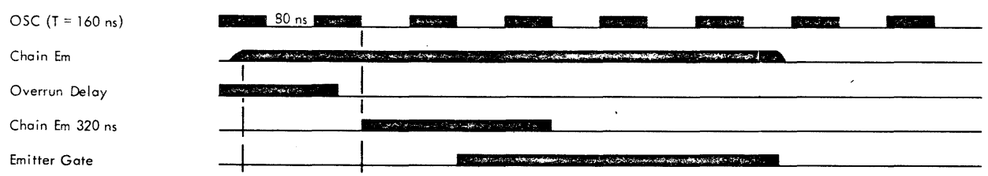
Diagram 4-300. Universal Character Set

2 3 4 5 6 7 8 9

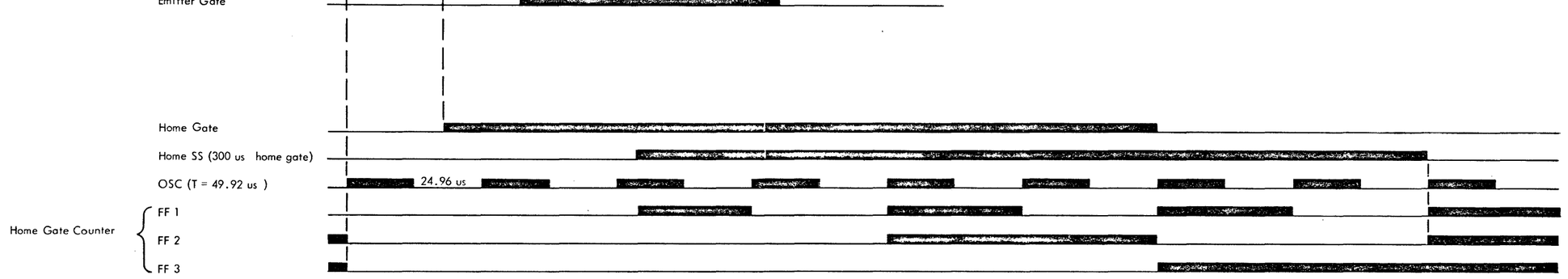
A

Assume: "Chain Em" Does Not Bounce

B



C



Note: This timing chart refers to function block at C-2 on Diag 4-080

D

E

2 3 4 5 6 7 8 9

A

B

C

D

E

	Clocks
4-065	I-R Cycle
4-065	Start Printing, I-R, CL 3
4-065	1st Prt Start In Dwell
4-065	Print
4-065	Execute Print
4-065	Request PC 0
4-070	Ptr I/O Cyc Latch
4-070	PC 0 Latch
4-070	PC 0 Control Latch
4-065	Clocks
4-065	CC Shift
4-065	Print Time
4-065	Prt Cyc Req
4-065	Last PC Group
4-065	Load Har
4-065	Req Time
4-065	Lockout

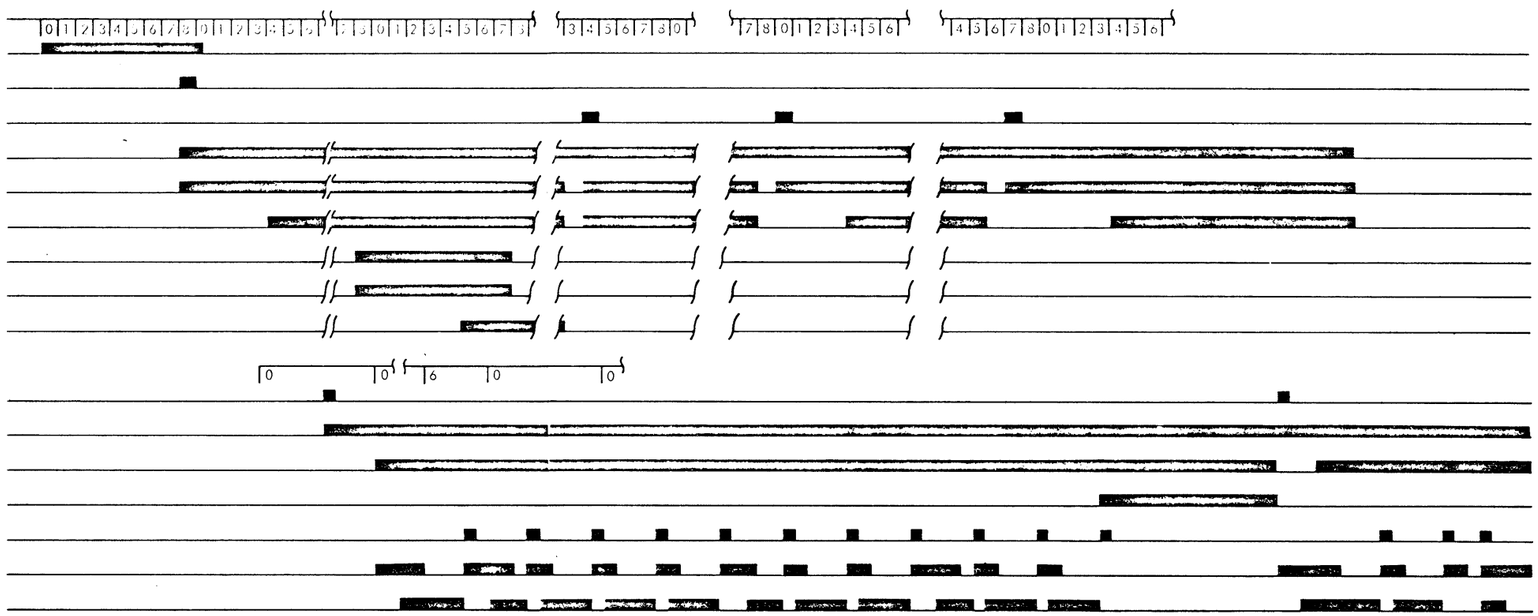
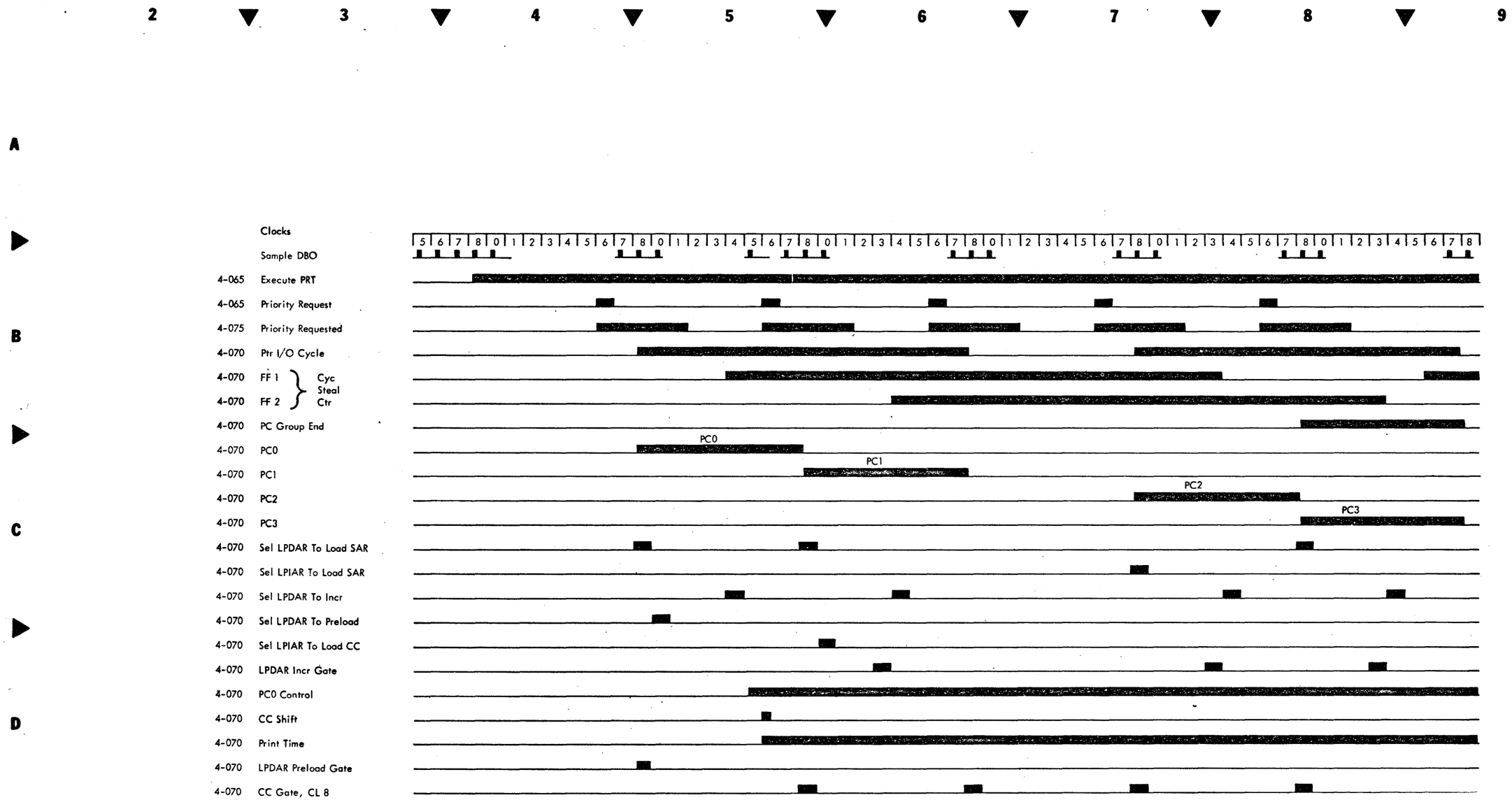
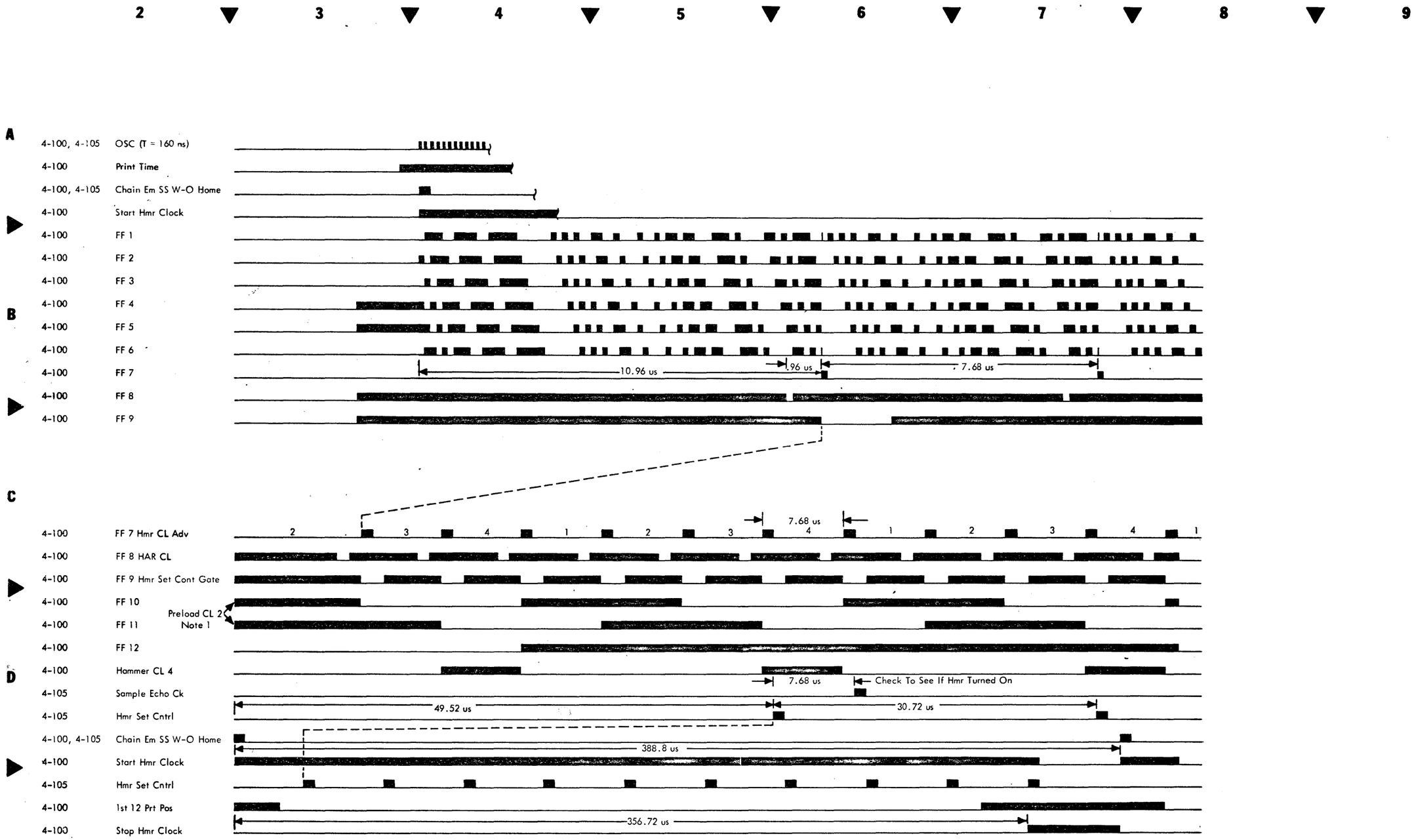


Diagram 4-320. Cycle Steal Control Timing Chart


2
3
4
5
6
7
8
9
A
B
C
D
E
Clocks
Sample DBO
4-065 Execute PRT
4-065 Priority Request
4-075 Priority Requested
4-070 Ptr I/O Cycle
4-070 FF 1
4-070 FF 2
Cyc Steal Ctr
4-070 PC Group End
4-070 PC0
4-070 PC1
4-070 PC2
4-070 PC3
4-070 Sel LPDAR To Load SAR
4-070 Sel LPIAR To Load SAR
4-070 Sel LPDAR To Incr
4-070 Sel LPDAR To Preload
4-070 Sel LPIAR To Load CC
4-070 LPDAR Incr Gate
4-070 PC0 Control
4-070 CC Shift
4-070 Print Time
4-070 LPDAR Preload Gate
4-070 CC Gate, CL 8
PC0
PC1
PC2
PC3



Note 1 Example applies for:
a) M1, PSS 3
b) M3, PSS 1
c) M4, PSS 2

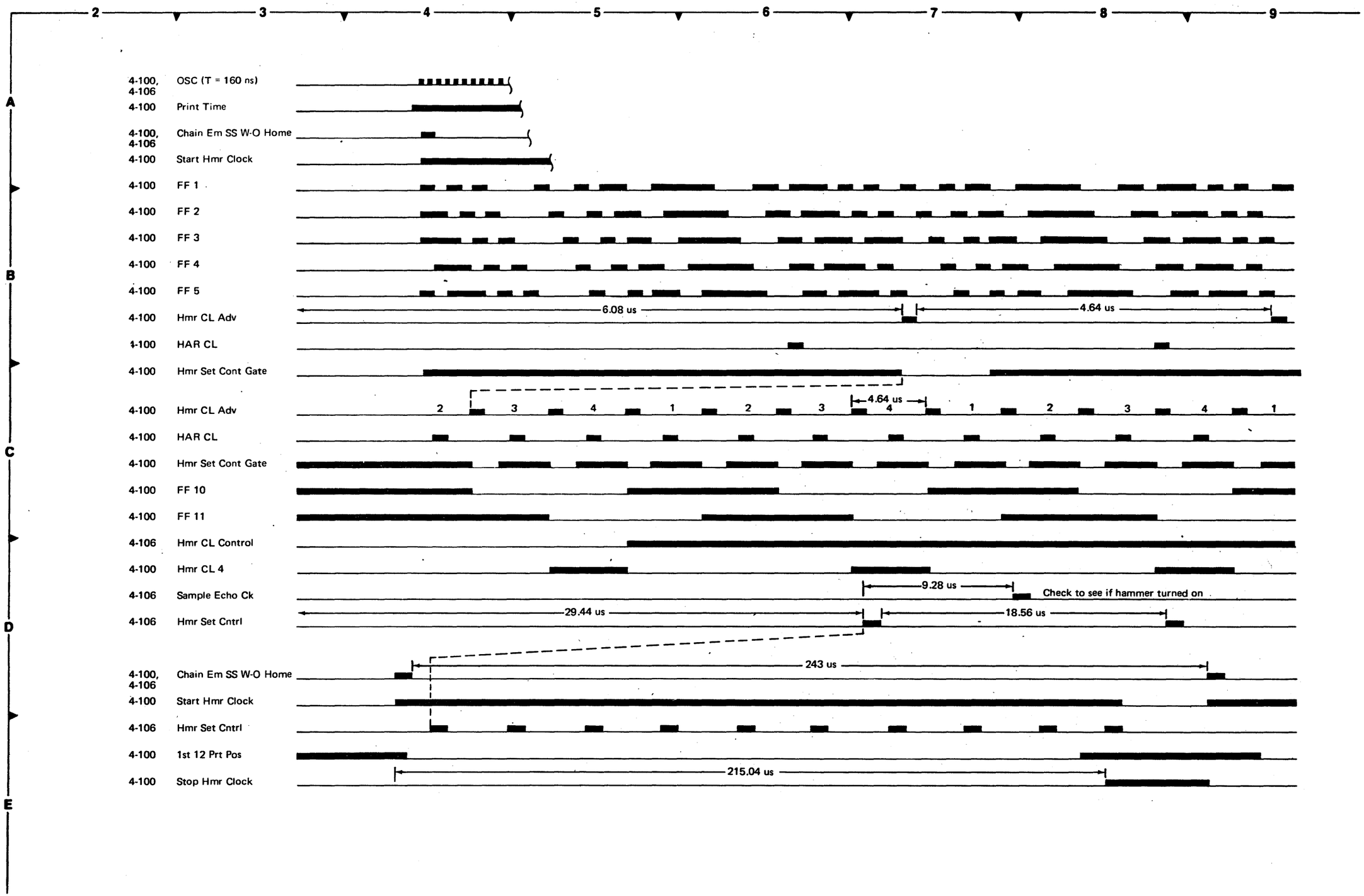
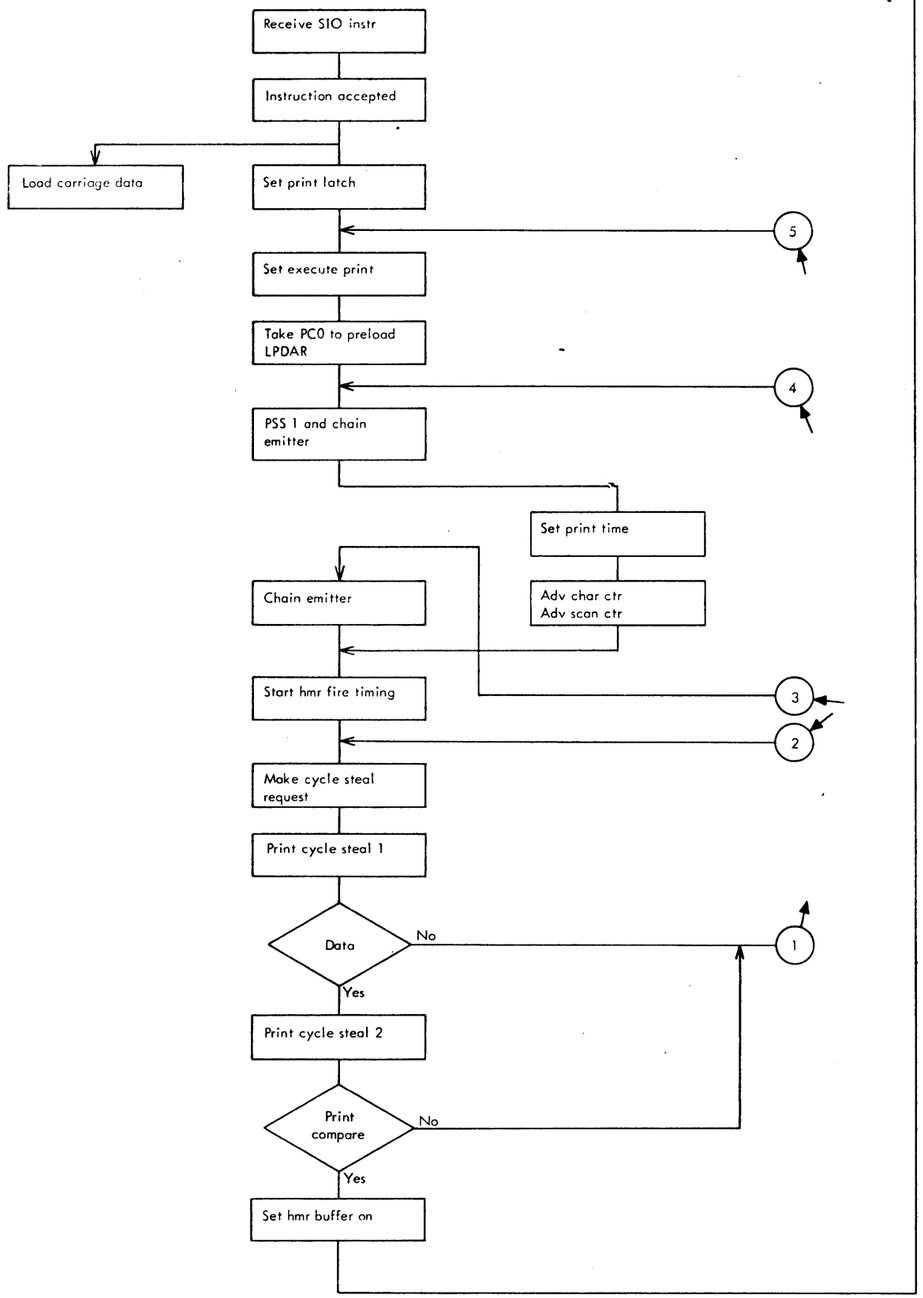


Diagram 4-361. Hammer Clock and Controls Timing Chart–Model 3



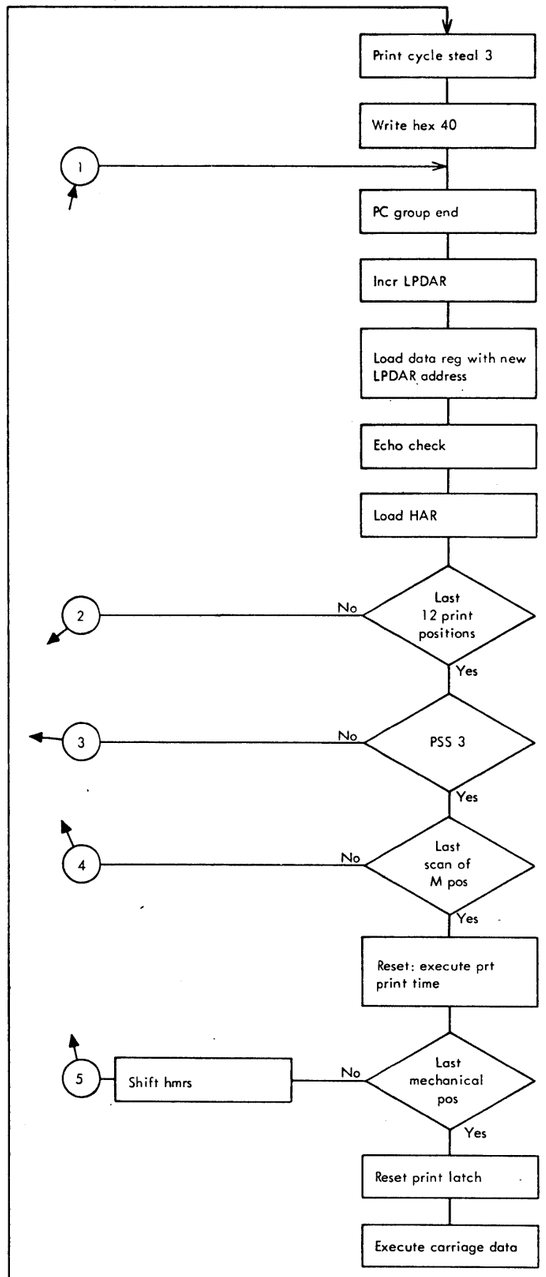
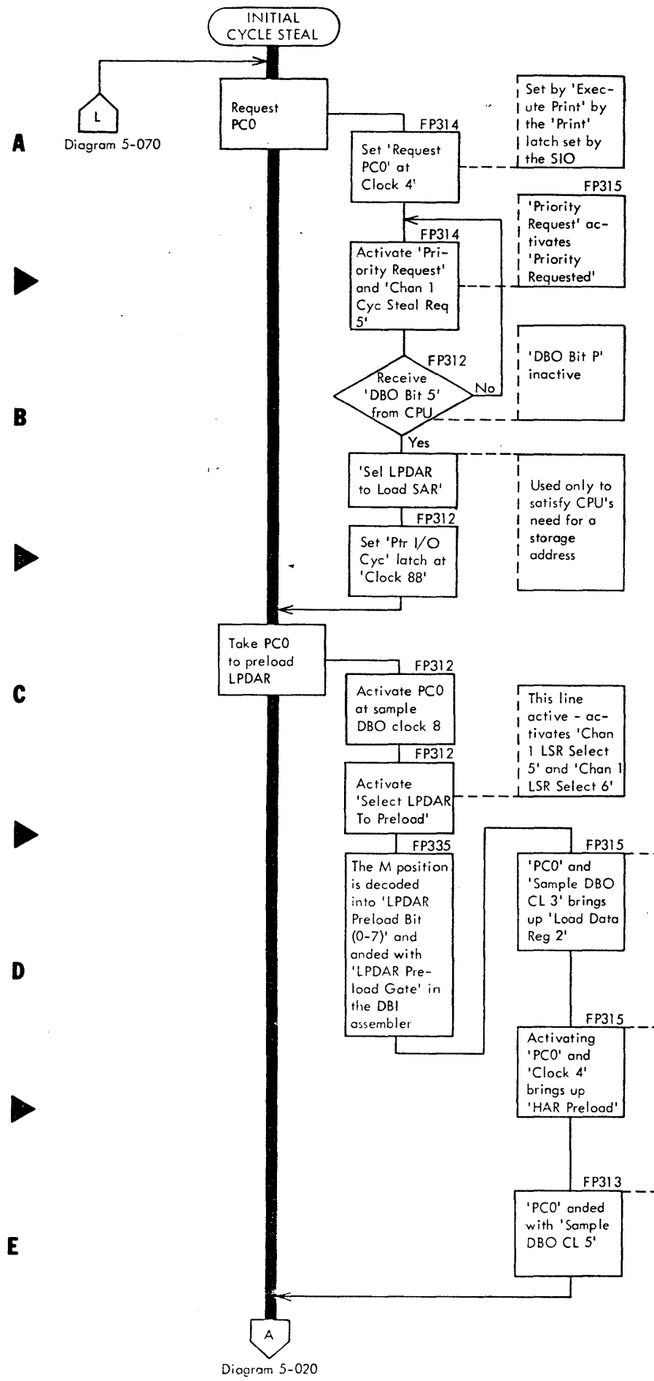
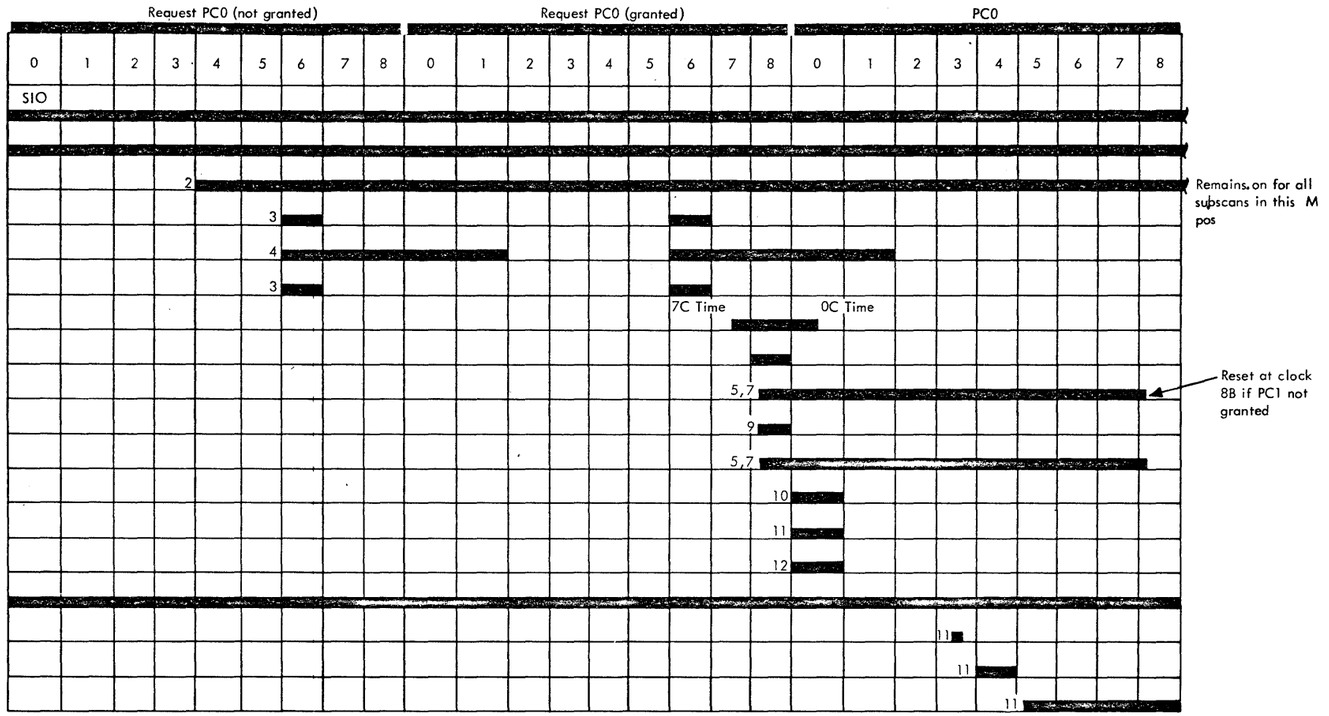
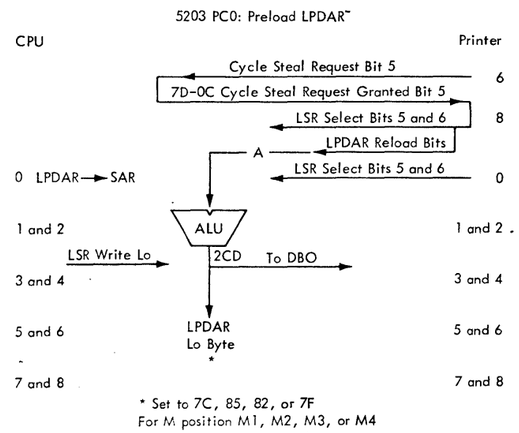


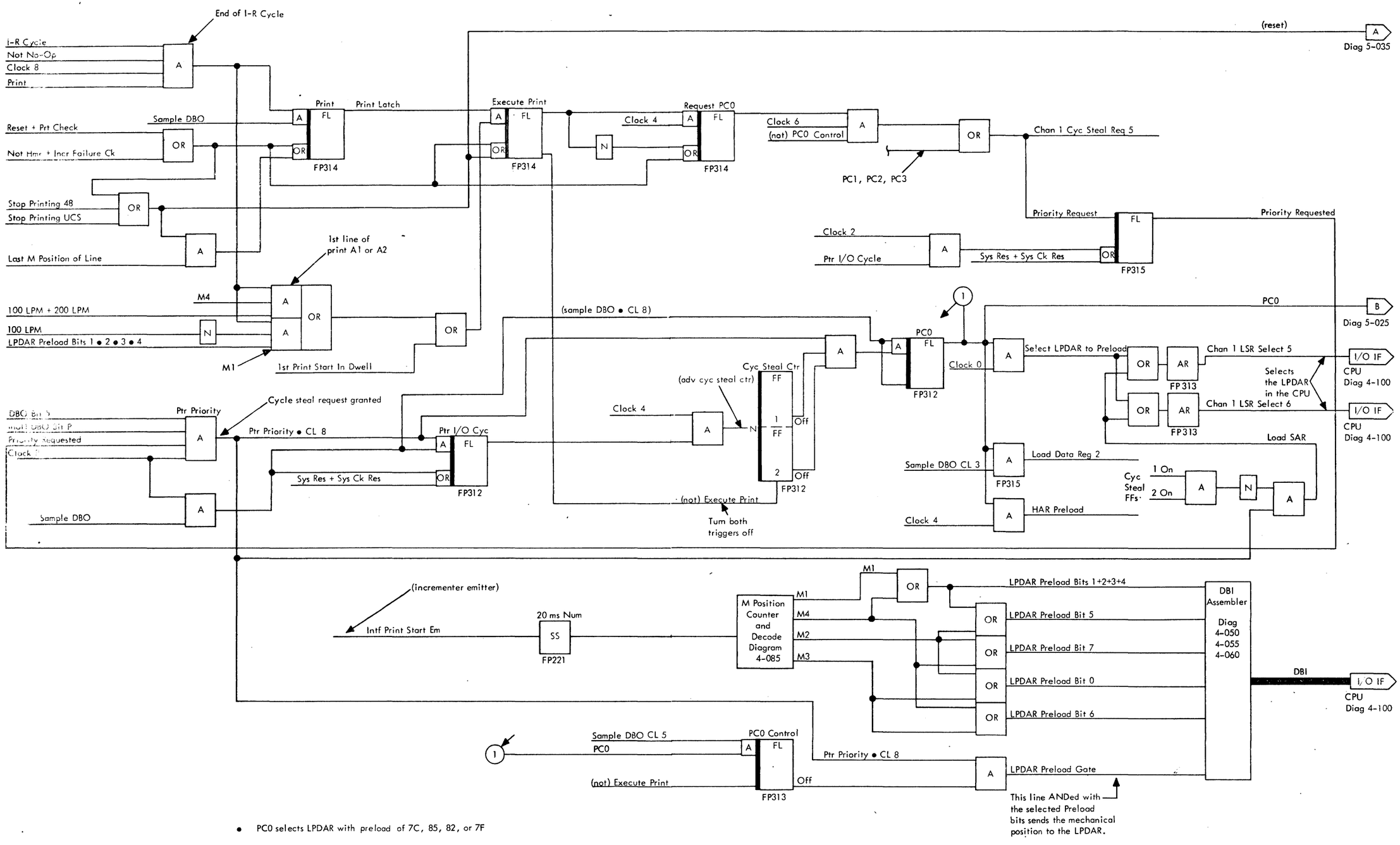
Diagram 5-005. Print Operation Flowchart



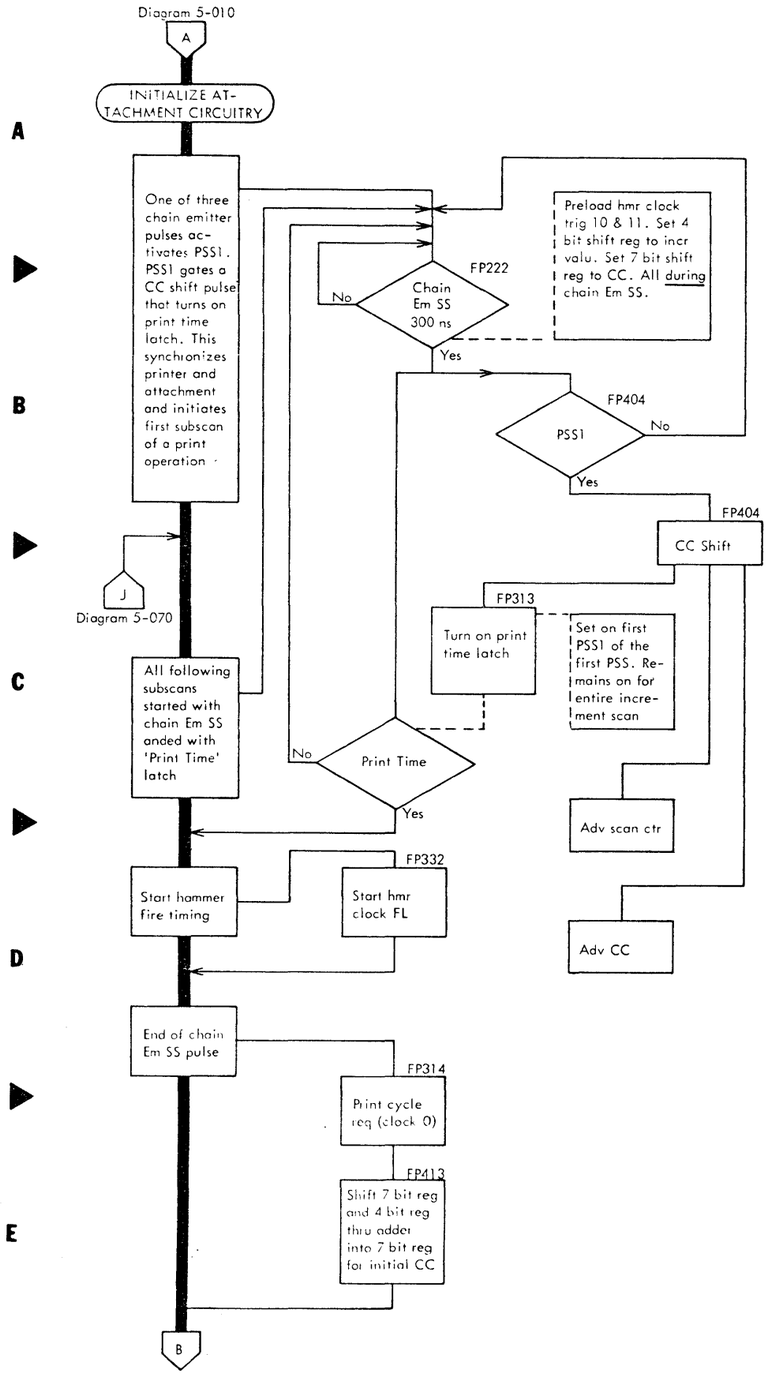
	Line Name
1	Print Latch
2	Execute Print Latch
3	Request PC0 Latch
4	Priority Request
5	Priority Requested
6	Chan 1 Cyc Steal Req 5
7	DBO Bit 5 (DBO bit P inactive)
8	Select LPDAR to Load SAR
9	Ptr I/O Cyc Latch
10	LPDAR Preload Gate
11	PC0 Latch
12	Select LPDAR to Preload
13	Chan 1 LSR Select 5
14	Chan 1 LSR Select 6
15	LPDAR Preload Bit Lines
16	Load Data Reg 2
17	HAR Preload
18	PC0 Control

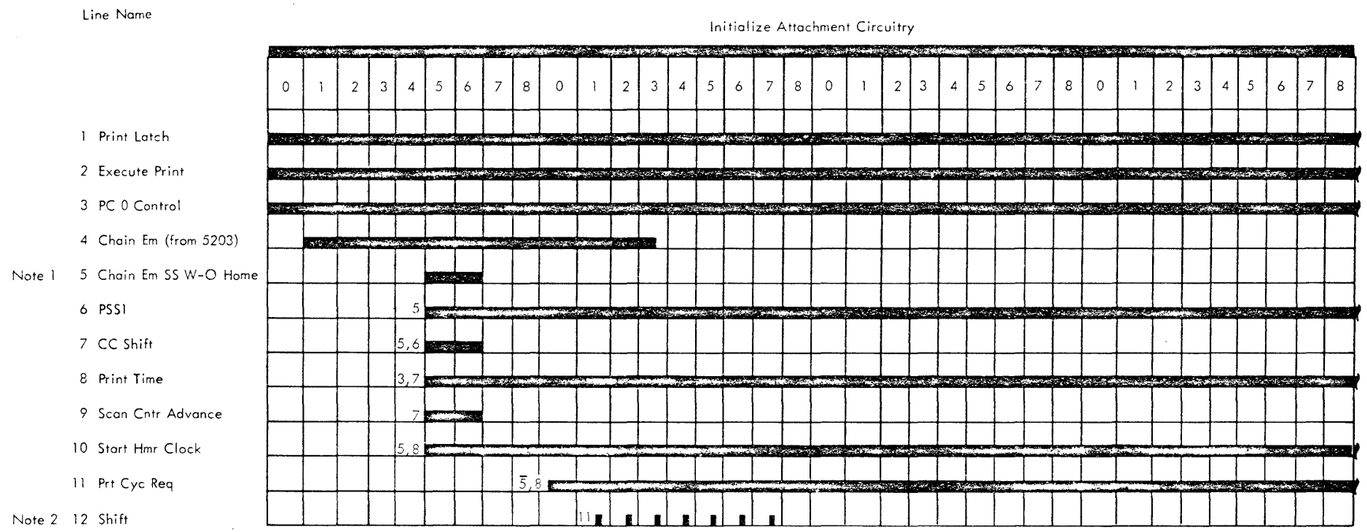






• PC0 selects LPDAR with preload of 7C, 85, 82, or 7F

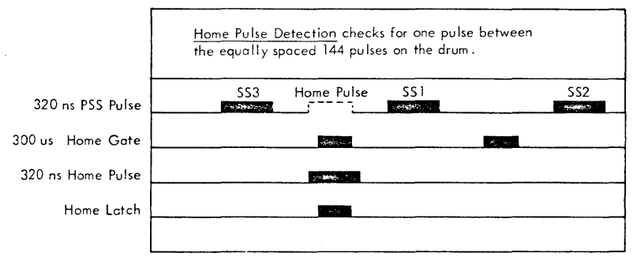


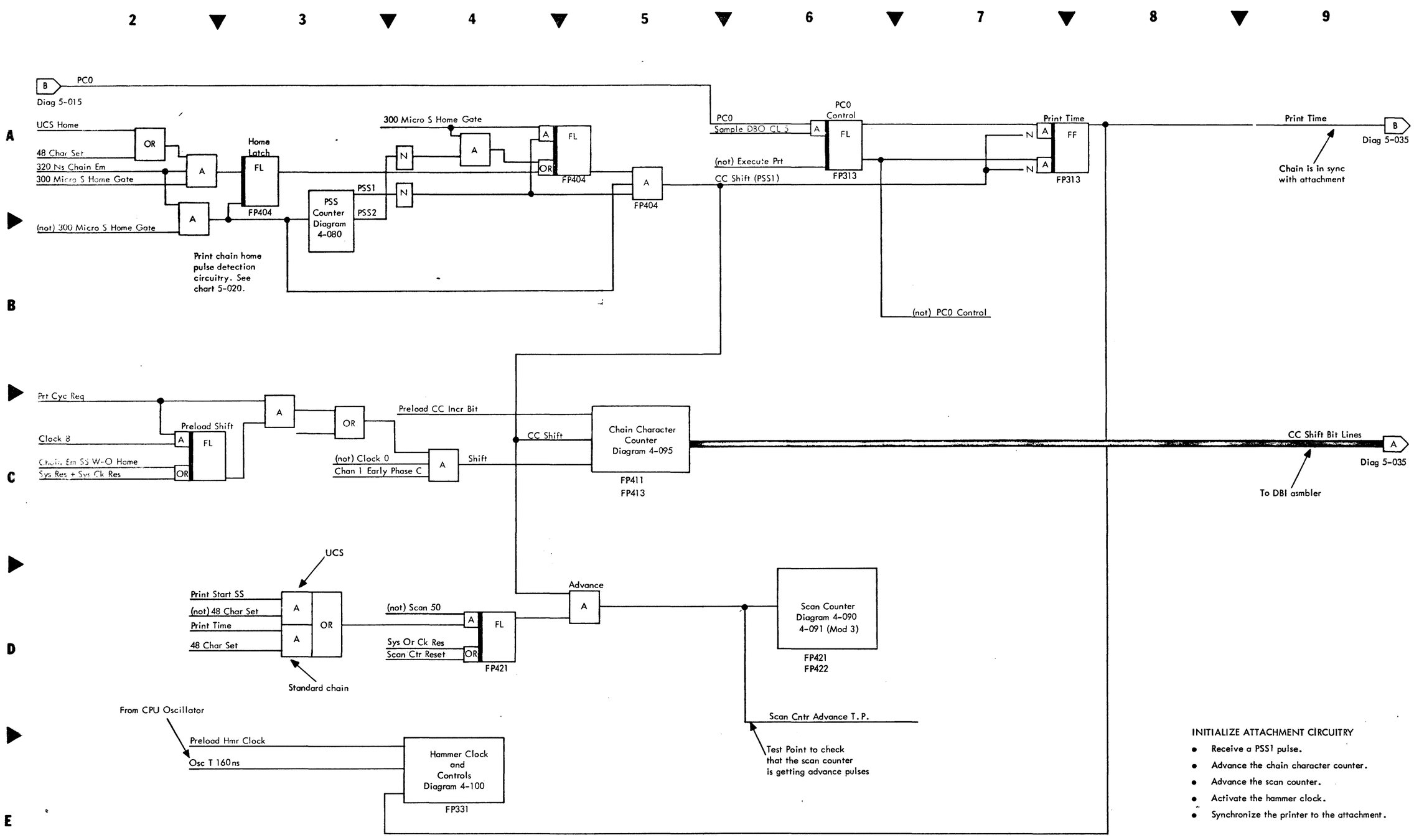


Note 1.

a. Load the character counter 4 bit shift reg with incr bits from the M pos and PSS decode
b. Load CC valu into 7 bit shift reg
c. Load trigs 10 and 11 of the hammer clock with preload bits from the M pos and PSS decode

Note 2. Shift 7 bit shift reg and 4 bit shift reg thru adder and back into 7 bit shift reg. Address of character aligned to print now in 7 bit shift reg

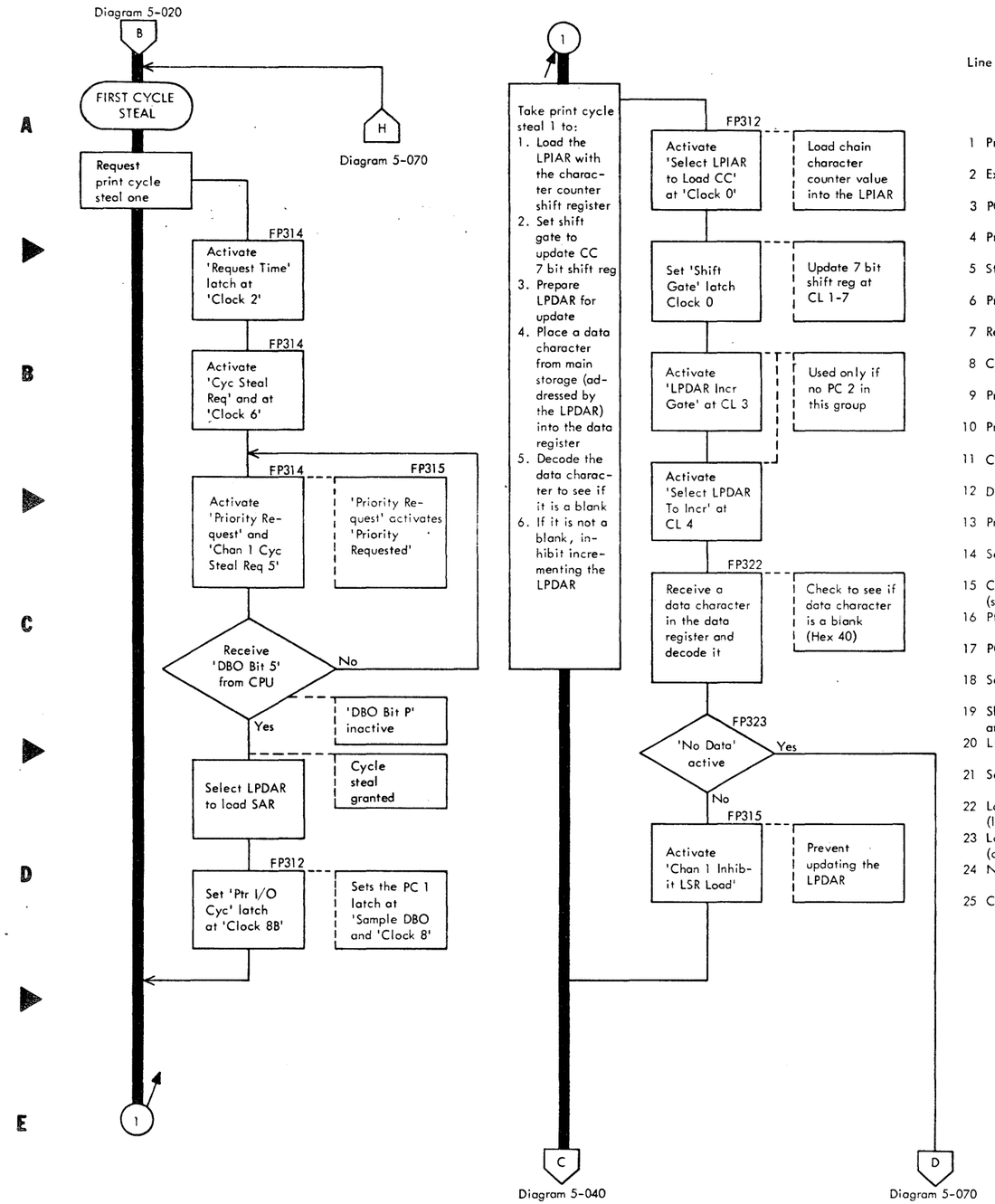




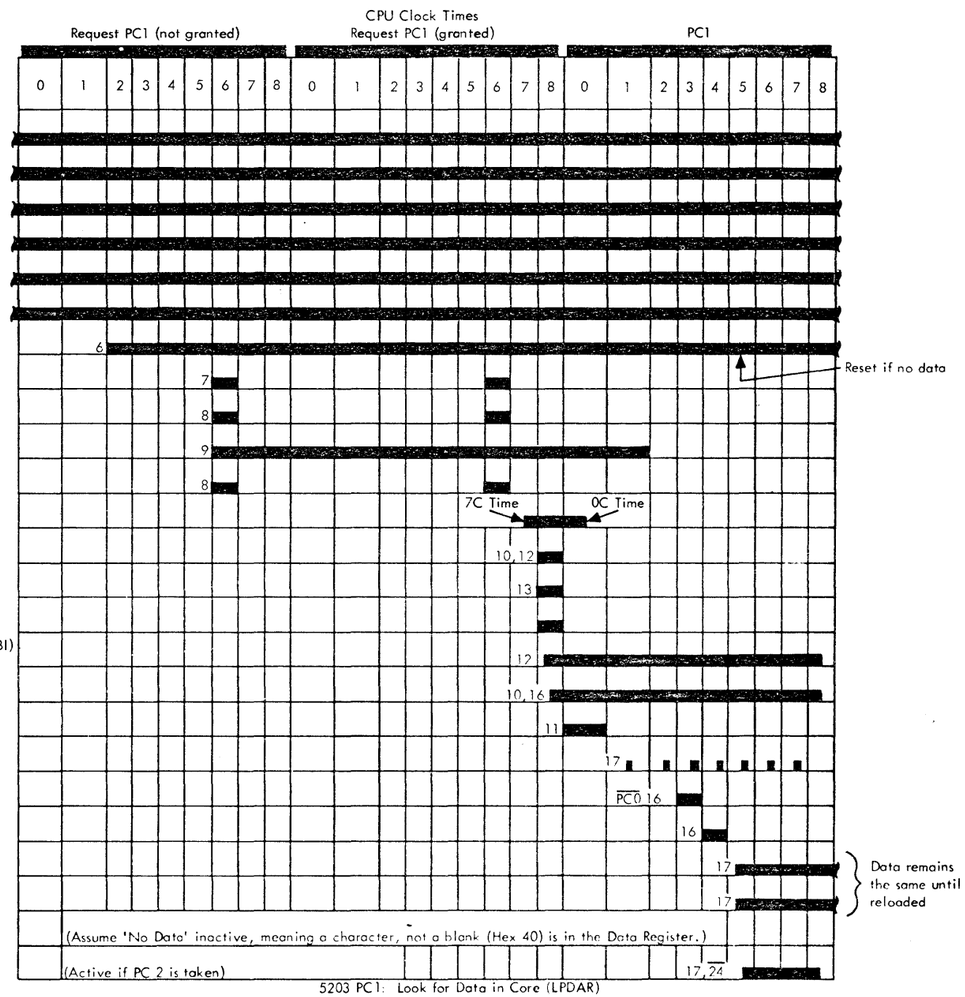
INITIALIZE ATTACHMENT CIRCUITRY

- Receive a PSS1 pulse.
- Advance the chain character counter.
- Advance the scan counter.
- Activate the hammer clock.
- Synchronize the printer to the attachment.

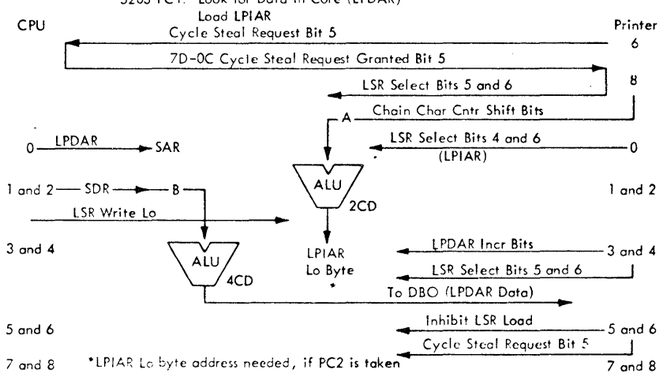
Diagram 5-025 (Part 2 of 2). Initialize Attachment Circuitry



	Line Name
1	Print Latch
2	Execute Print
3	PC0 Control
4	Print Time
5	Start Hmr Clock
6	Prt Cyc Req Latch
7	Request Time Latch
8	Cyc Steal Req
9	Priority Request
10	Priority Requested
11	Chan 1 Cyc Steal Req 5
12	DBO Bit 5 (DBO Bit P inactive)
13	Printer Priority CL 8
14	Select LPDAR To Load SAR
15	CC Gate CL 8 (send CC from 7 bit shift reg to DBI)
16	Ptr I/O Cyc Latch
17	PC1 Latch
18	Select LPIAR To Load CC
19	Shift (7 bit shift register and 4 bit shift register)
20	LPDAR Incr Gate
21	Select LPDAR To Incr
22	Load Data Reg 2 (load data character)
23	Load Data Reg 1 (check data character)
24	No Data
25	Chan 1 Inhibit LSR Load



5203 PC1: Look for Data in Core (LPDAR)



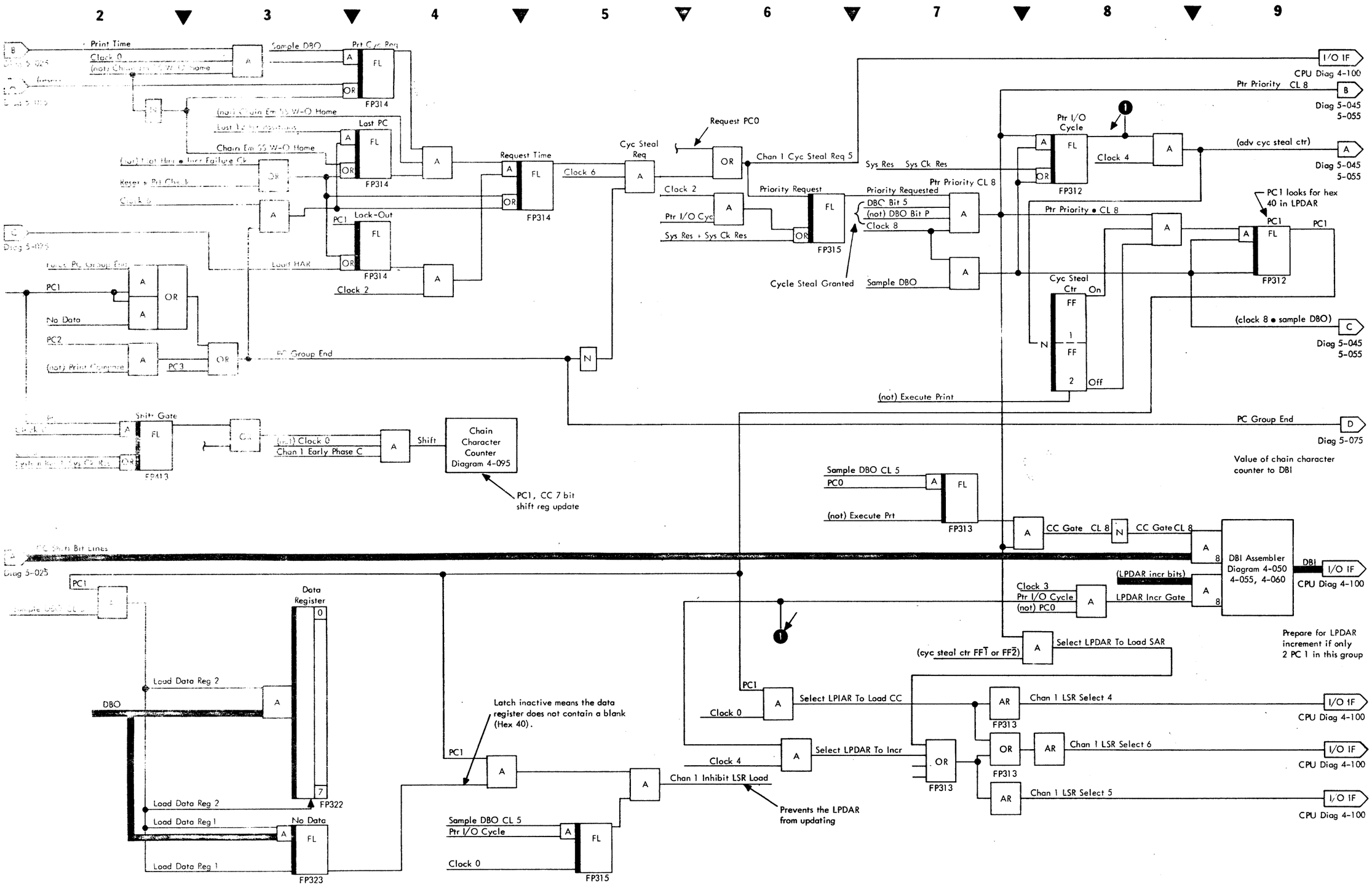
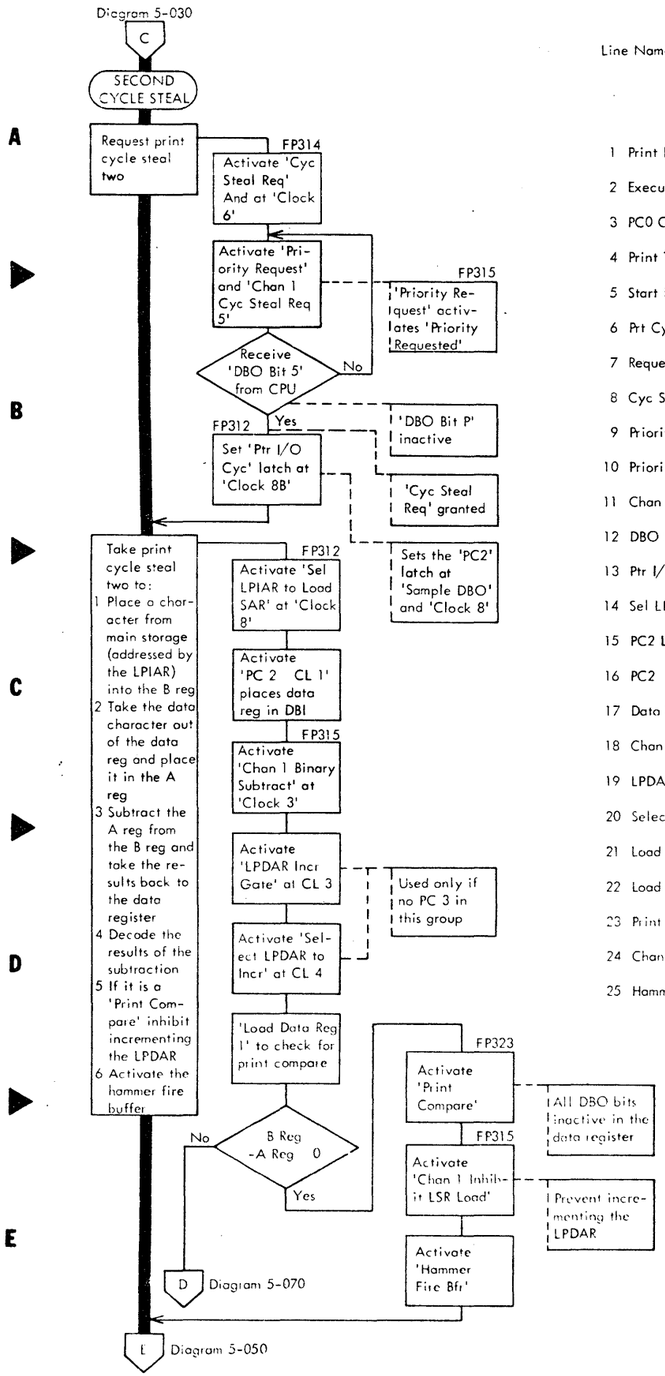
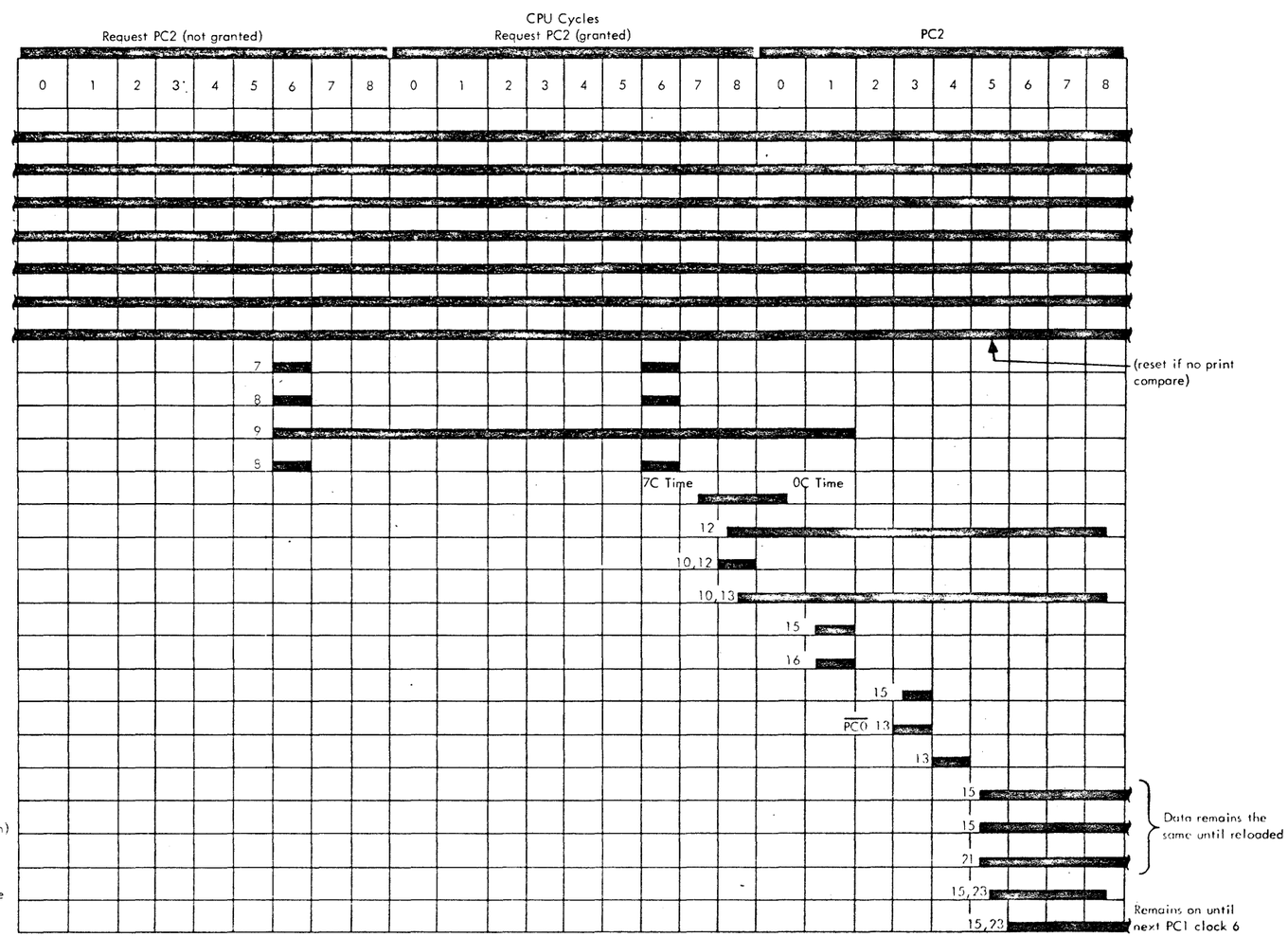


Diagram 5-035 (Part 2 of 2). First Cycle Steal–PC1

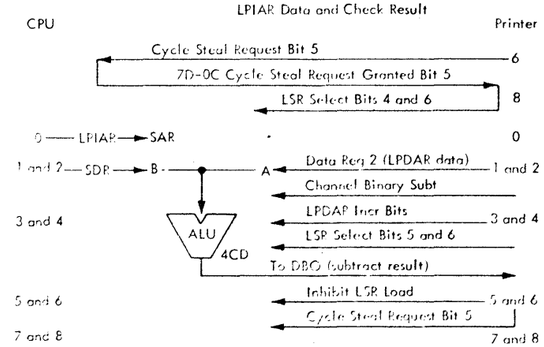


Line Name

1 Print Latch
2 Execute Print
3 PC0 Control
4 Print Time
5 Start Hmr Clock
6 Prt Cyc Req Latch
7 Request Time Latch
8 Cyc Steal Req
9 Priority Request
10 Priority Requested
11 Chan 1 Cyc Steal Req 5
12 DBO Bit 5 (DBO bit P inactive)
13 Ptr I/O Cyc Latch
14 Sel LPIAR to Load SAR
15 PC2 Latch
16 PC2 CL 1
17 Data Reg Bits (to CPU for subtraction)
18 Chan 1 Binary Subtract
19 LPDAR Incr Gate
20 Select LPDAR to Incr
21 Load Data Reg 1 (check for print compare)
22 Load Data Reg 2 (load results of subtraction)
23 Print Compare Latch
24 Chan 1 Inhibit LSR Load } Only If Compare
25 Hammer Fire Buffer



5203 PC2. Subtract LPDAR Data From LPIAR Data and Check Result



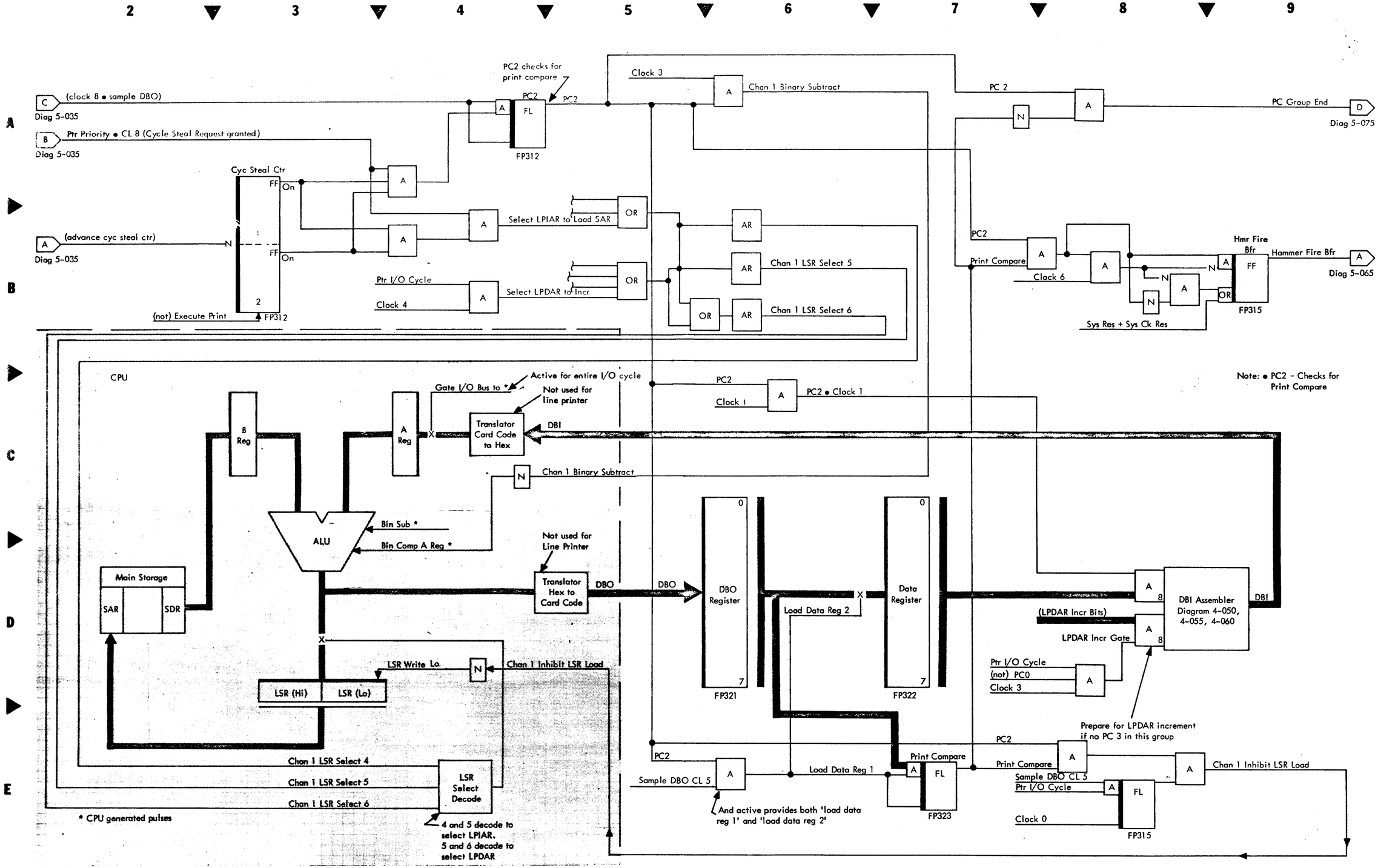
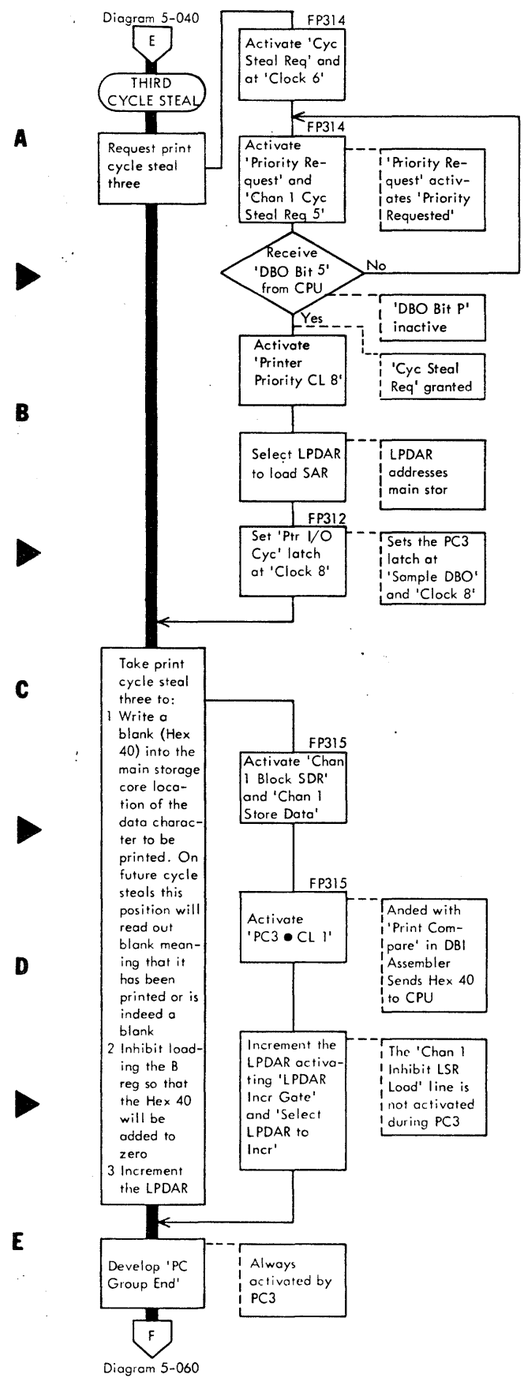
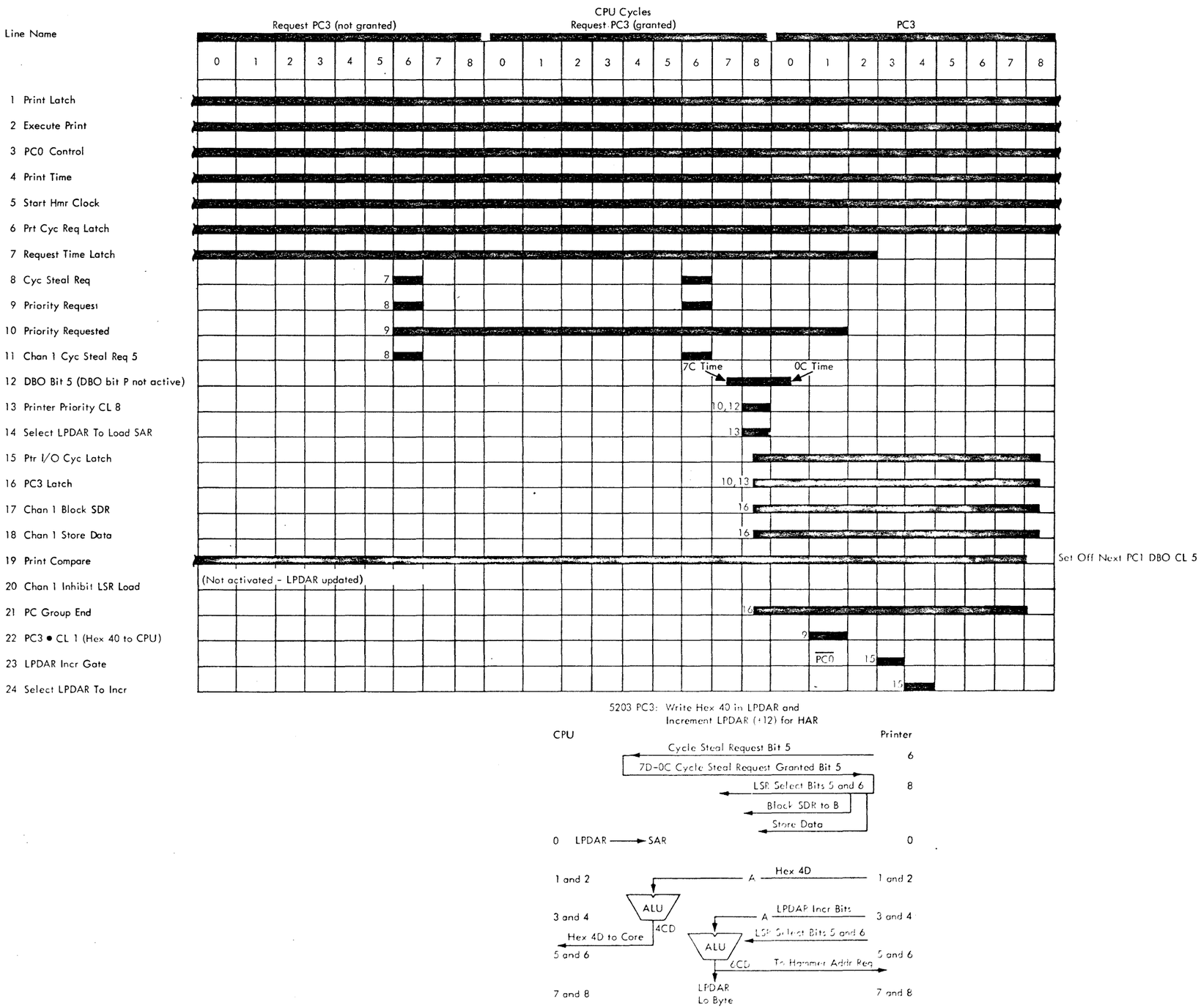


Diagram 5-045 (Part 2 of 2). Second Cycle Steal—PC2





5203 PC3: Write Hex 40 in LPDAR and Increment LPDAR (+12) for HAR

PC3 • Write Hex 40 in LPDAR
• Update LPDAR to Fire Correct Hammer

C (clock 8 • sample DBO)
Diag 5-035

PC3 PC3
A FL
FP312

AR Chan 1 BlockSDR

AR Chan 1 Store Data

B Ptr Priority • CL 8 (Cycle Steal Request granted)
Diag 5-035

A

Cyc Steal Ctr
FF
1
Off
A (advance cyc steal ctr) N
Diag 5-035
On
FF
2
FP312
(not) Execute Print

Hex 40 (blank to CPU)

Clock 1 — A — PC3 • Clock 1 — A
Print Compare

Printer I/O Cycle
(not) PC0
Clock 3 — A — LPDAR Incr Gate — A 8
(LPDAR incr bits)

DBI Assembler
Diagram 4-050
4-055, 4-060

DBI

Hex 40

OR — PC Group End — PC Group End — D Diag 5-075

CPU

Gate SDR to B N

Activate for entire I/O cycle.
Gate I/O Bus to A*

Not used for line printer.

Main Storage
SAR SDR

B Reg X

A Reg X

Translator Card Code to Hex

DBI

DBO
DBO Reg

Data Reg 2
Data Reg 2 — A

HAR
HAR Reg 0–5
A

ALU

Bin Sub *
Binary Comp A Reg*

DBO

(hex 40 = blank) X

LSR Select Decode

PC3
HAR Set

Ptr I/O Cycle
Clock 4 — A — Select LPDAR To Incr

Printer Priority CI8
(PC2) — A — Select LPDAR To Load SAR — OR — AR — AR

LSR (Hi) LSR (Lo)

LSR Write Low

N Chan 1 Inhibit LSR Load

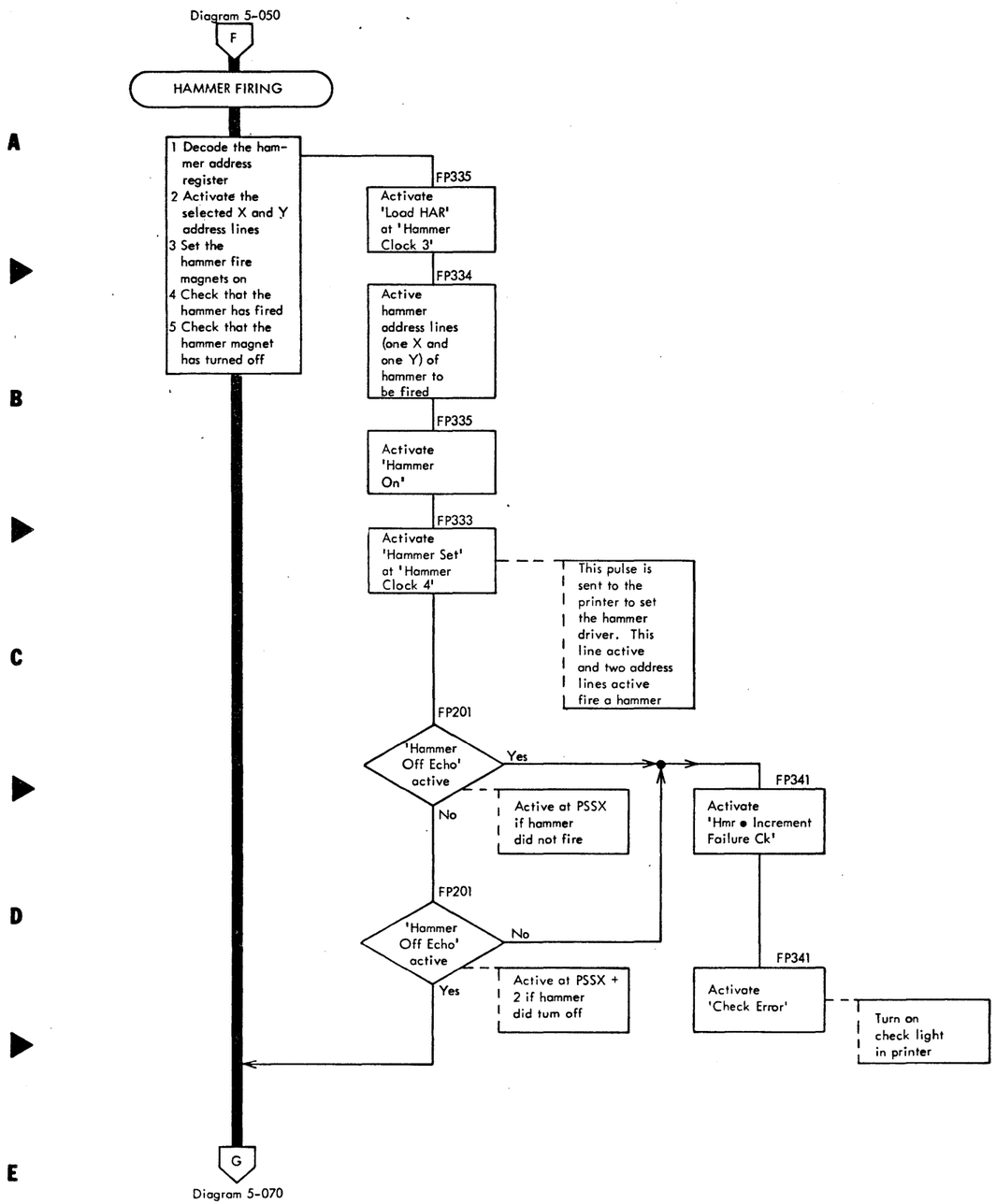
Not activated at PC3. Therefore the LPDAR is updated

Chan 1 LSR Select 5
Chan 1 LSR Select 6

(store pulse)

* CPU Generated Pulses

Diagram 5-055 (Part 2 of 2). Third Cycle Steal–PC3



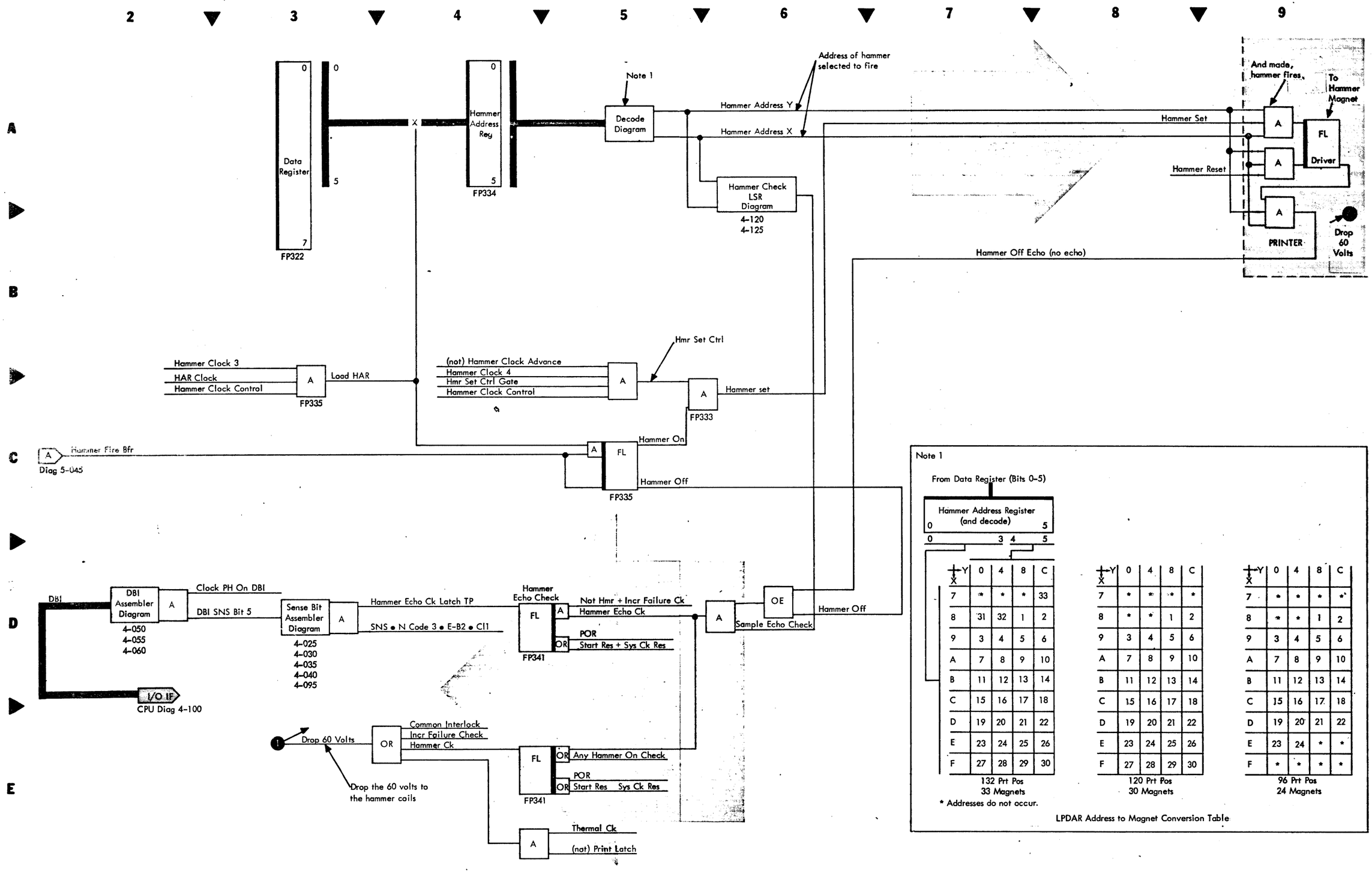
The hammer address register was loaded with the address in the LPDAR either as the result of PC0 or PC group end followed by a 'load HAR' pulse.

The address in the hammer address register is decoded into one X address line and one Y address line. The two selected address lines are taken to the printer to select a hammer driver latch and the hammer check LSR in the attachment.

At 'hammer clock 4' time in the attachment, the 'hammer set' pulse is activated if the hammer fire buffer trigger is on. The 'hammer set' pulse is taken to the printer and to all of the hammer latches. It ANDs with the latch that has the X and Y address lines active and turns on the latch. With the latch set, the hammer fires.

Each hammer driver is addressed once during every print scan. Each time it is addressed, a hammer driver is deactivated by the 'hammer reset' pulse unless a character is to be printed in that position. If a character is to be printed in that position, a hammer is activated by the 'hammer set' pulse. Two checks are made on every hammer fired: (1) a check to ensure the hammer driver turned on, and (2) a check to ensure that it has turned off. The check to see if the hammer driver turned on is made during the same print scan that sets up the hammer to print (print scan X). An inactive 'hammer off echo' line from the printer indicates the hammer driver turned on. The hammer driver is left on for that print scan (scan X). During print scan X + 1, the hammer driver is addressed again and turned off.

The check to see if the hammer driver has turned off occurs two print scans later (print scan X + 2). The check to see if the hammer has turned off cannot be made on the next print scan after the hammer driver has fired (print scan X + 1) because the response from the hammer driver that generates the 'hammer off echo' line is still on because of a long period of reset delay. If the 'hammer off echo' line is active at scan X + 2, the hammer has turned off.



Note 1

From Data Register (Bits 0-5)

Hammer Address Register (and decode)

0 3 4 5

X \ Y	0	4	8	C
7	*	*	*	33
8	31	32	1	2
9	3	4	5	6
A	7	8	9	10
B	11	12	13	14
C	15	16	17	18
D	19	20	21	22
E	23	24	25	26
F	27	28	29	30

132 Prt Pos
33 Magnets

X \ Y	0	4	8	C
7	*	*	*	*
8	*	*	1	2
9	3	4	5	6
A	7	8	9	10
B	11	12	13	14
C	15	16	17	18
D	19	20	21	22
E	23	24	25	26
F	27	28	29	30

120 Prt Pos
30 Magnets

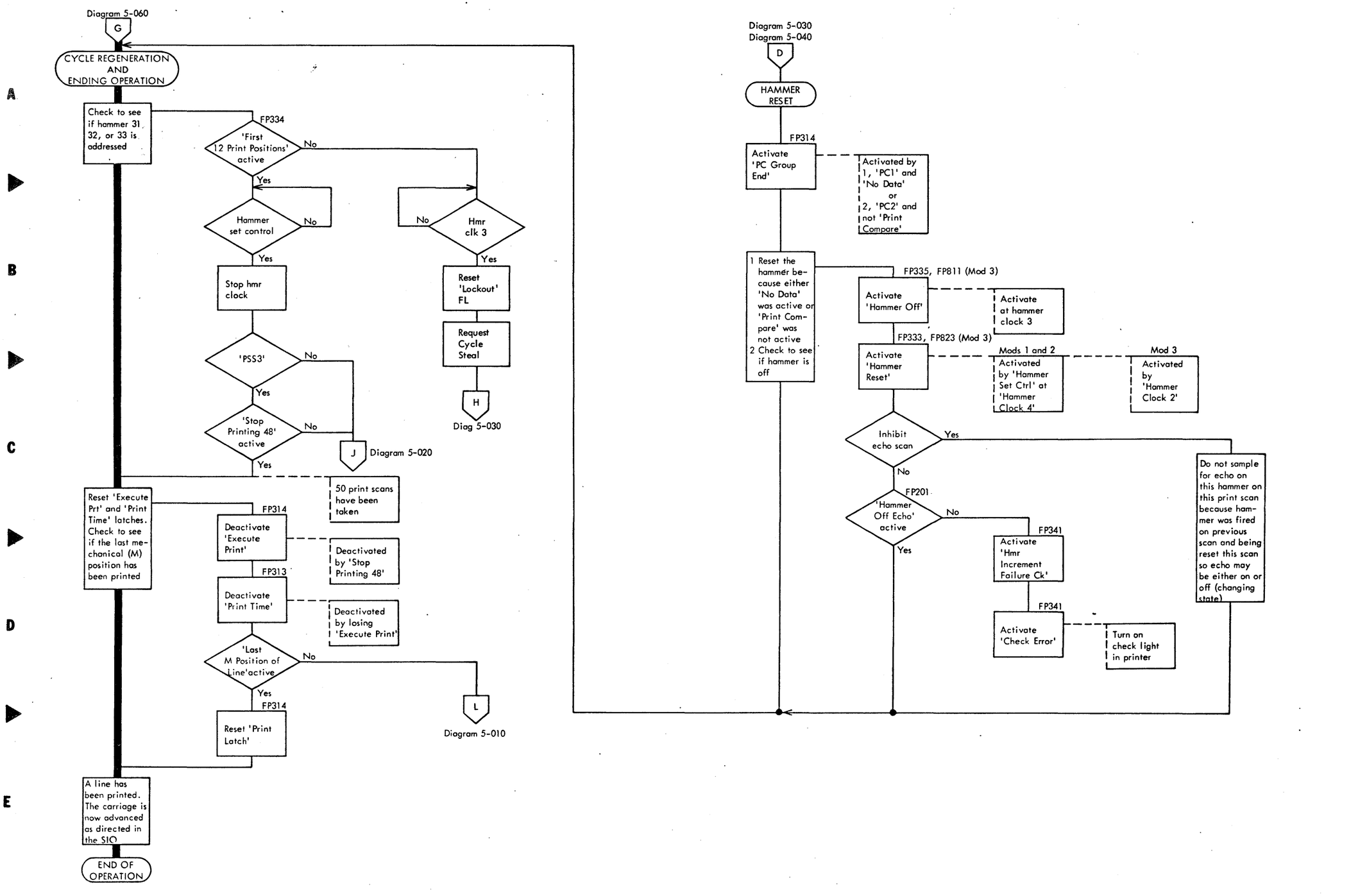
X \ Y	0	4	8	C
7	*	*	*	*
8	*	*	1	2
9	3	4	5	6
A	7	8	9	10
B	11	12	13	14
C	15	16	17	18
D	19	20	21	22
E	23	24	*	*
F	*	*	*	*

96 Prt Pos
24 Magnets

* Addresses do not occur.

LPDAR Address to Magnet Conversion Table

Diagram 5-065 (Part 2 of 2). Hammer Firing


2
3
4
5
6
7
8
9
A
B
C
D
E
Diagram 5-060
G
CYCLE REGENERATION AND ENDING OPERATION
Check to see if hammer 31, 32, or 33 is addressed
FP334
'First 12 Print Positions' active
No
Yes
Hammer set control
No
Yes
Stop hmr clock
'PSS3'
No
Yes
'Stop Printing 48' active
No
Yes
J
Diagram 5-020
50 print scans have been taken
Reset 'Execute Prt' and 'Print Time' latches. Check to see if the last mechanical (M) position has been printed
FP314
Deactivate 'Execute Print'
Deactivated by 'Stop Printing 48'
FP313
Deactivate 'Print Time'
Deactivated by losing 'Execute Print'
'Last M Position of Line' active
No
Yes
L
Diagram 5-010
FP314
Reset 'Print Latch'
A line has been printed. The carriage is now advanced as directed in the SIO
END OF OPERATION
No
Hmr clk 3
Yes
Reset 'Lockout' FL
Request Cycle Steal
H
Diag 5-030
Diagram 5-030
Diagram 5-040
D
HAMMER RESET
FP314
Activate 'PC Group End'
Activated by 1, 'PC1' and 'No Data' or 2, 'PC2' and not 'Print Compare'
1 Reset the hammer because either 'No Data' was active or 'Print Compare' was not active
2 Check to see if hammer is off
FP335, FP811 (Mod 3)
Activate 'Hammer Off'
Activate at hammer clock 3
FP333, FP823 (Mod 3)
Activate 'Hammer Reset'
Mods 1 and 2
Activated by 'Hammer Set Ctrl' at 'Hammer Clock 4'
Mod 3
Activated by 'Hammer Clock 2'
Inhibit echo scan
Yes
No
Do not sample for echo on this hammer on this print scan because hammer was fired on previous scan and being reset this scan so echo may be either on or off (changing state)
FP201
'Hammer Off Echo' active
No
Yes
FP341
Activate 'Hmr Increment Failure Ck'
FP341
Activate 'Check Error'
Turn on check light in printer

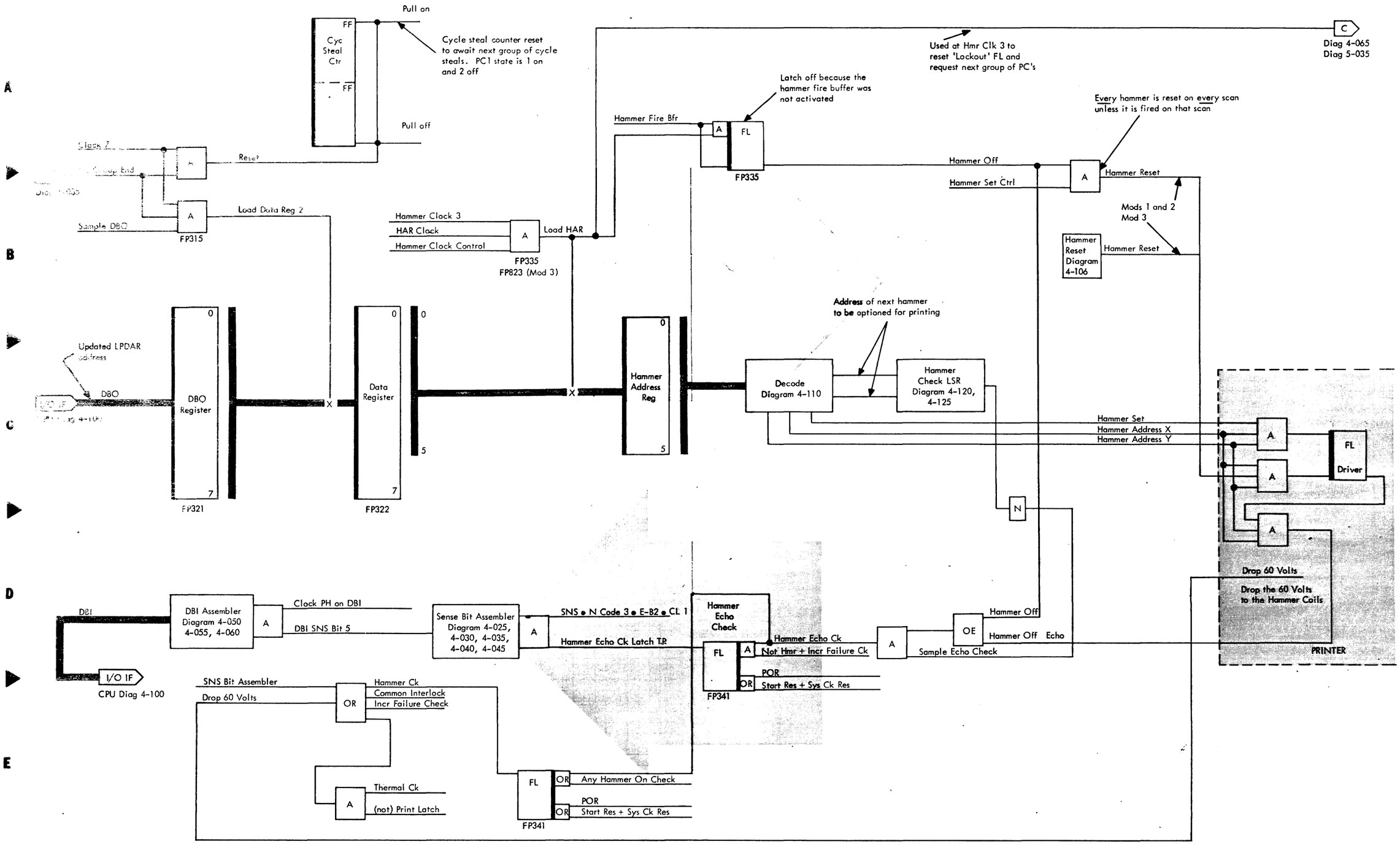


Diagram 5-075. Hammer Reset

2 3 4 5 6 7 8 9

UNPRINTABLE CHARACTER

- An unprintable character (UPC) is any character that is optioned for printing but does not appear in the chain image area in main storage.
- An unprintable character sets a sense bit in the SNS bit assembler, but will not be detected unless an SNS instruction is given.
- On machines with standard 48-character sets, there is no reduction in throughput caused by unprintable characters.

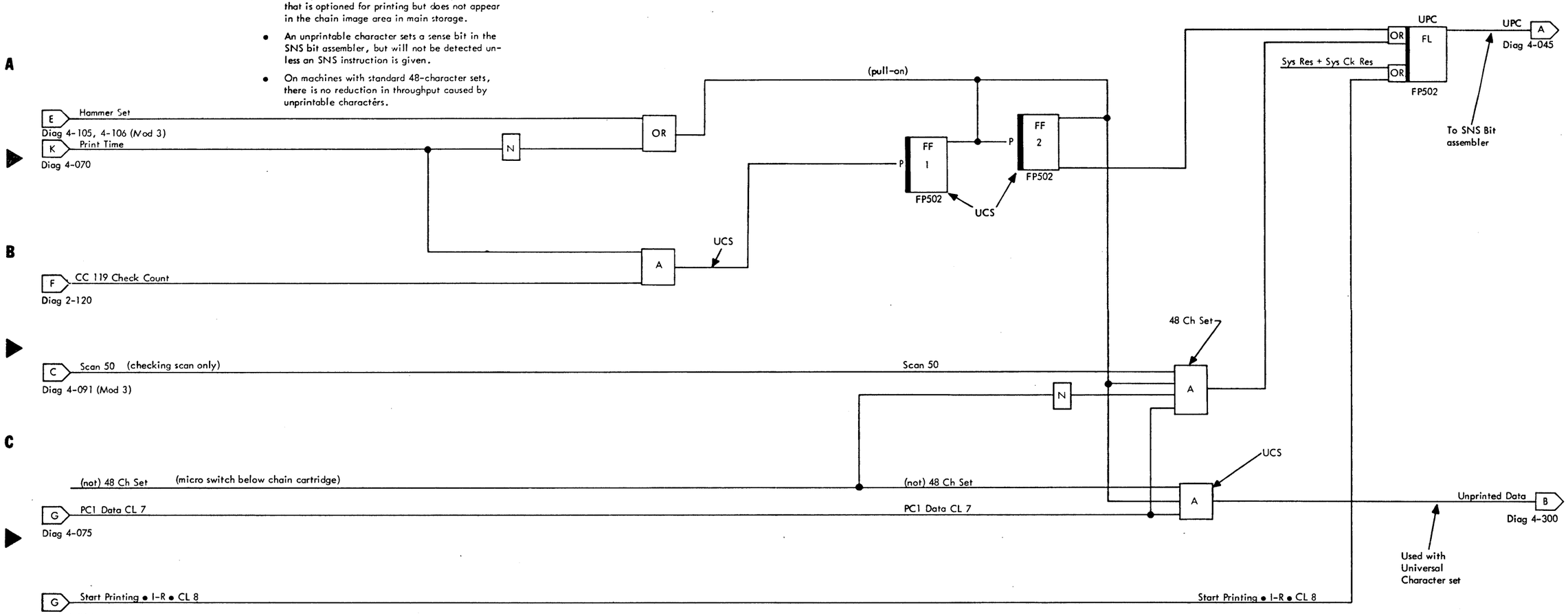
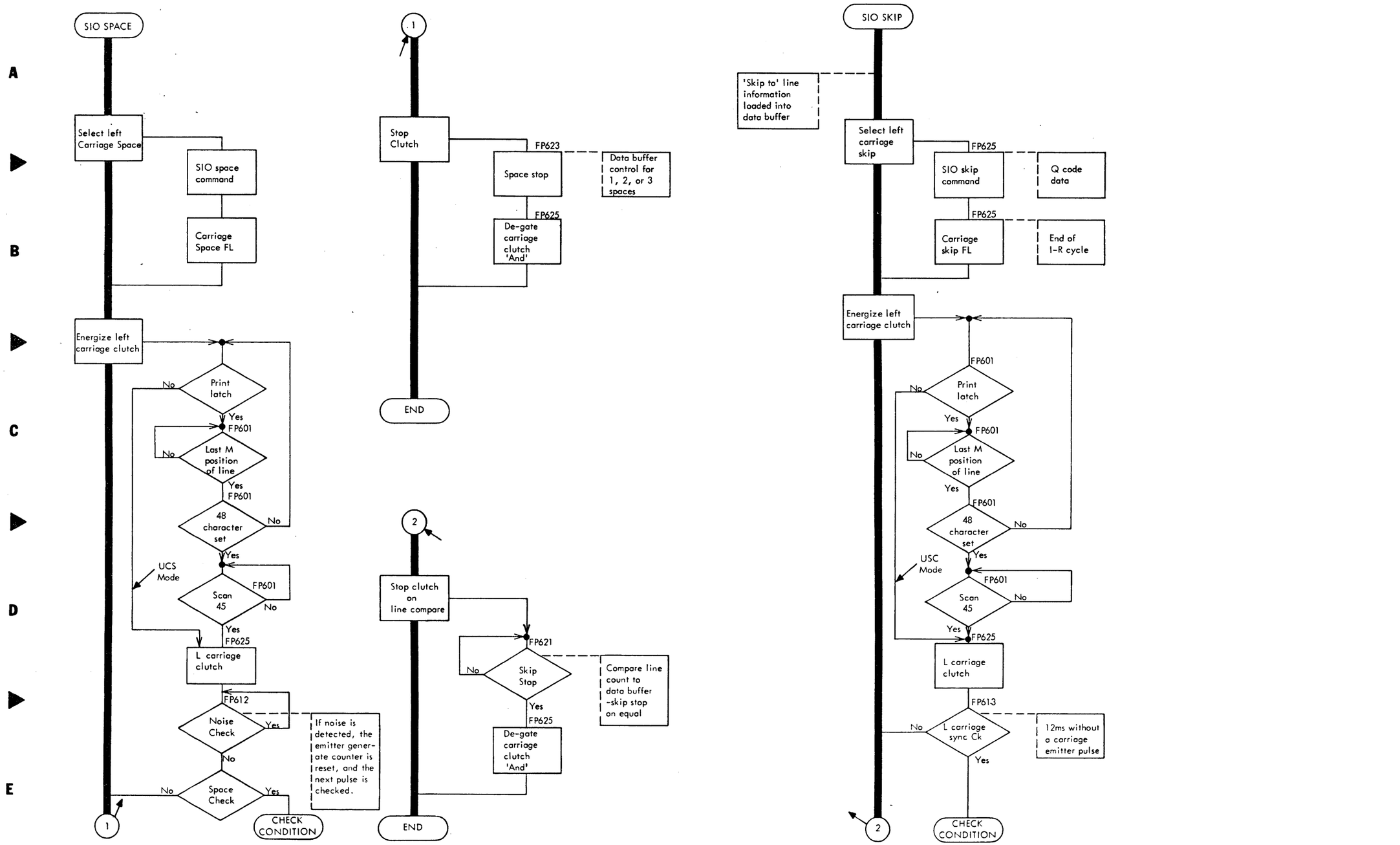


Diagram 5-095. Unprintable Character


2
3
4
5
6
7
8
9
A
B
C
D
E
SIO SPACE
Select left Carriage Space
SIO space command
Carriage Space FL
Energize left carriage clutch
Print latch
No
Yes
FP601
Last M position of line
No
Yes
FP601
48 character set
No
Yes
UCS Mode
Scan 45
FP601
No
Yes
FP625
L carriage clutch
FP612
Noise Check
Yes
No
If noise is detected, the emitter generate counter is reset, and the next pulse is checked.
Space Check
No
Yes
CHECK CONDITION
1
1
Stop Clutch
FP623
Space stop
Data buffer control for 1, 2, or 3 spaces
FP625
De-gate carriage clutch 'And'
END
2
Stop clutch on line compare
FP621
No
Skip Stop
Yes
FP625
Compare line count to data buffer -skip stop on equal
De-gate carriage clutch 'And'
END
SIO SKIP
'Skip to' line information loaded into data buffer
Select left carriage skip
FP625
SIO skip command
Q code data
FP625
Carriage skip FL
End of I-R cycle
Energize left carriage clutch
FP601
Print latch
No
Yes
FP601
Last M position of line
No
Yes
FP601
48 character set
No
Yes
USC Mode
FP601
Scan 45
No
Yes
FP625
L carriage clutch
FP613
L carriage sync Ck
No
Yes
12ms without a carriage emitter pulse
CHECK CONDITION
2

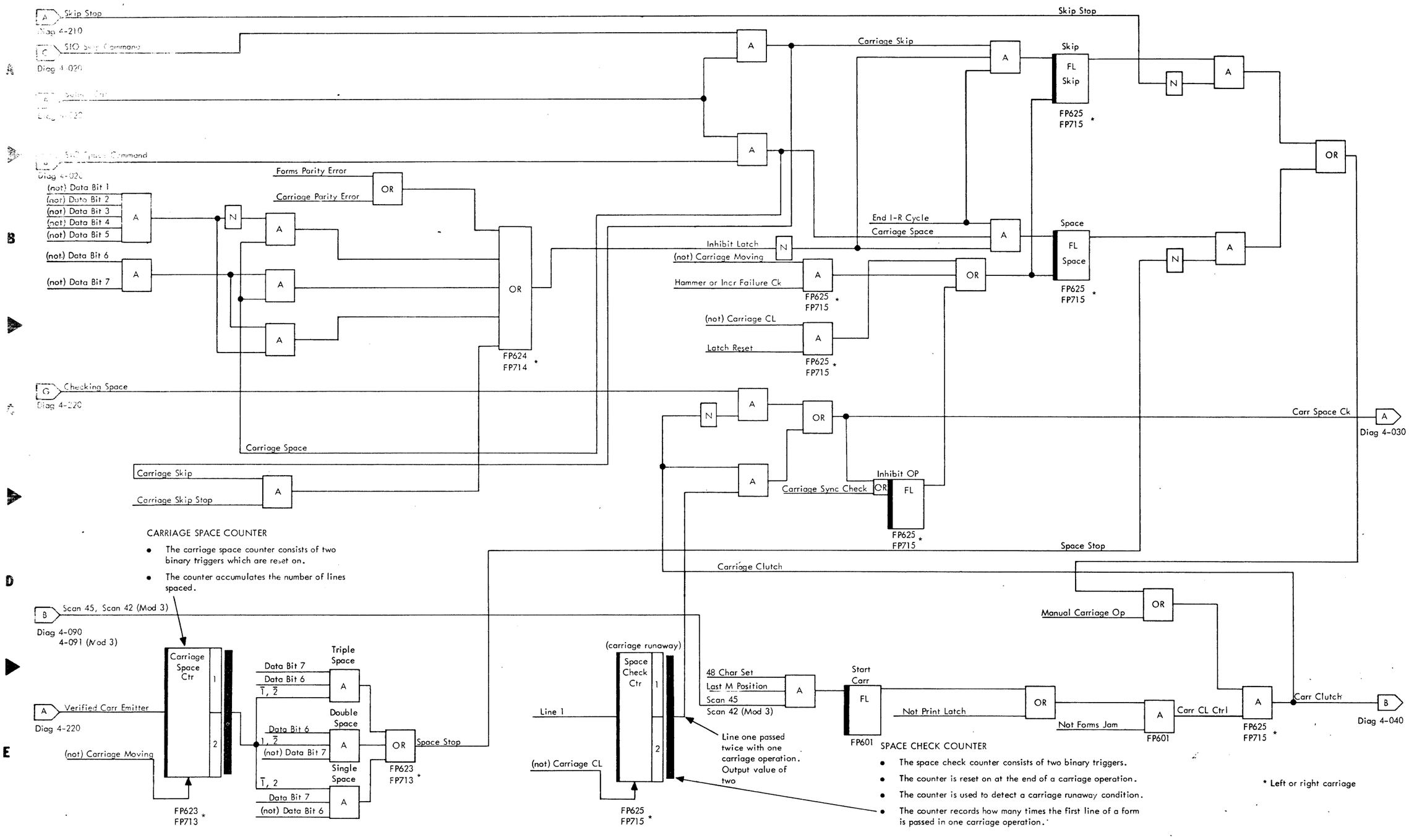
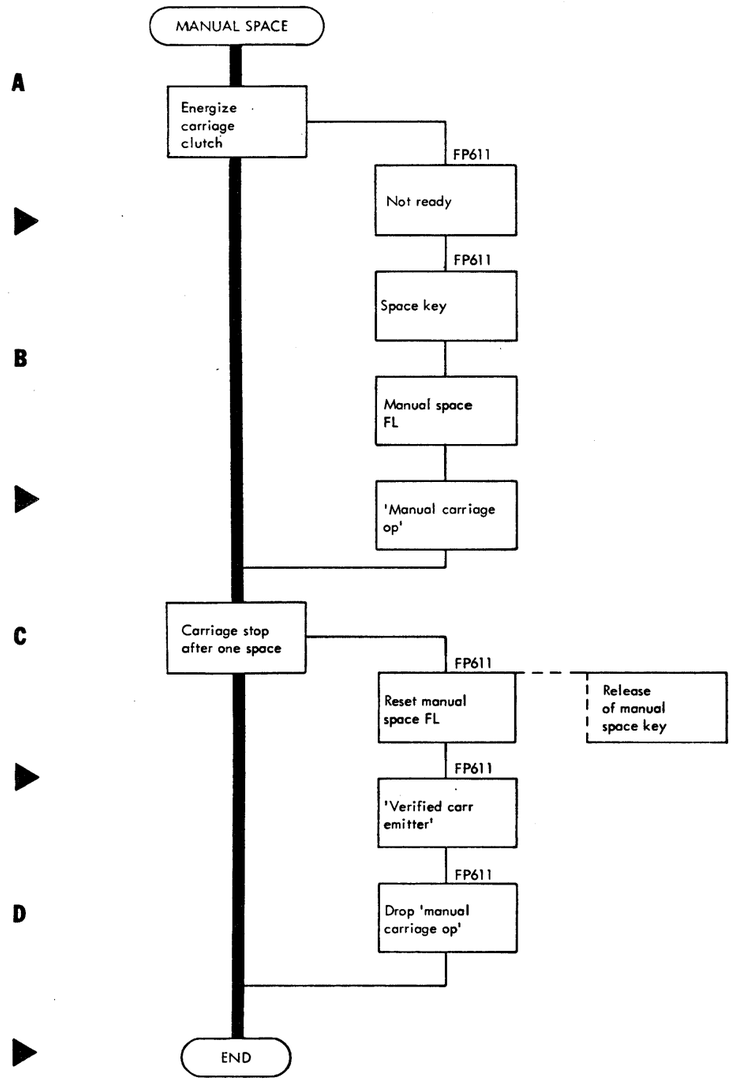
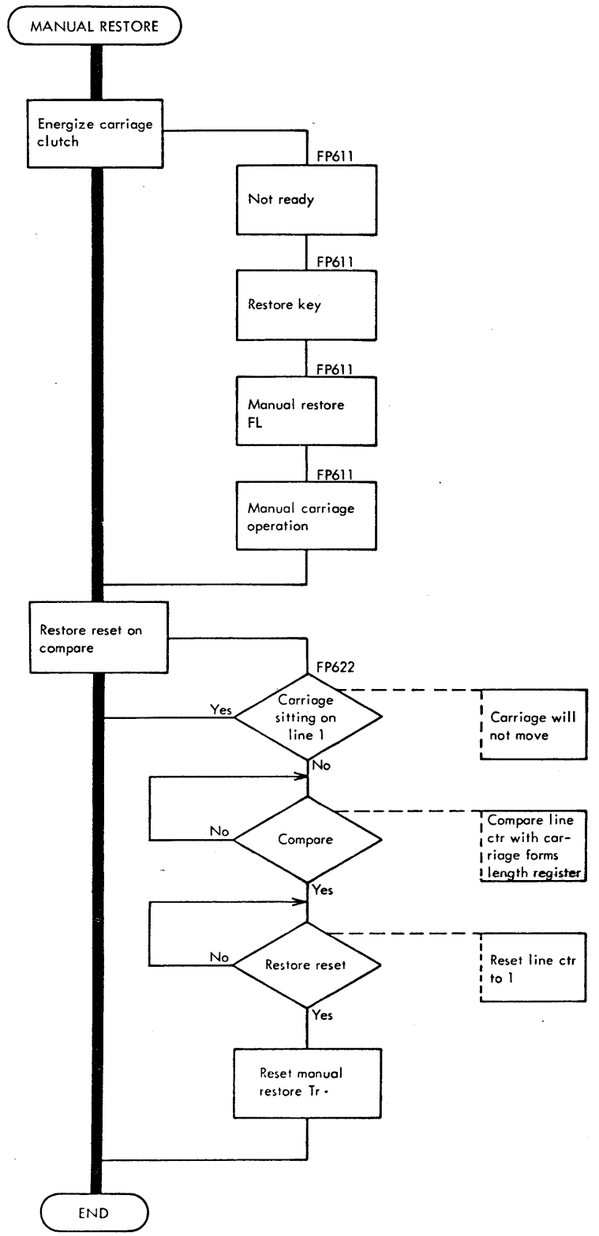
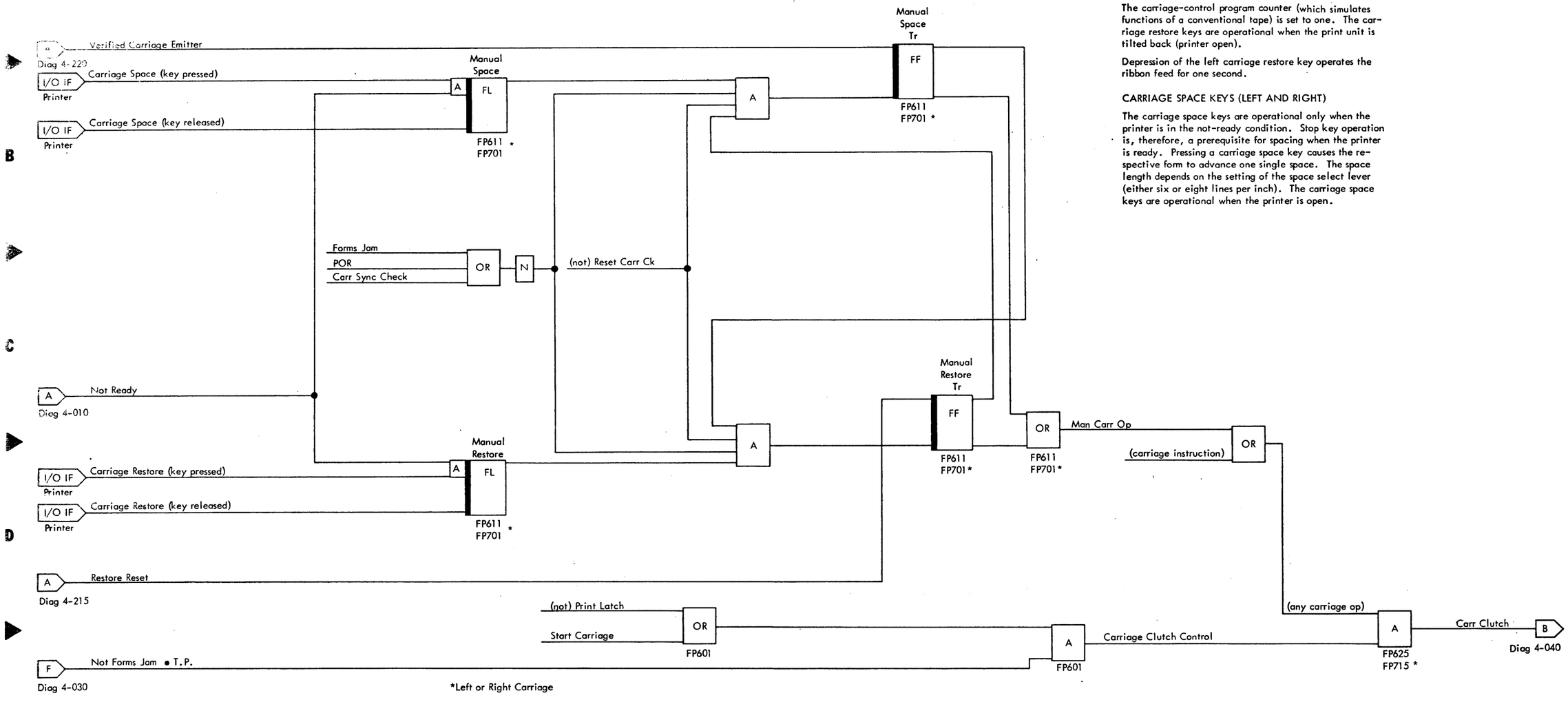


Diagram 5-215 (Part 2 of 2). Carriage Space and Skip Operation


2
3
4
5
6
7
8
9
A
B
C
D
E
MANUAL SPACE
Energize carriage clutch
FP611
Not ready
FP611
Space key
Manual space FL
'Manual carriage op'
Carriage stop after one space
FP611
Reset manual space FL
Release of manual space key
FP611
'Verified carr emitter'
FP611
Drop 'manual carriage op'
END


MANUAL RESTORE
Energize carriage clutch
FP611
Not ready
FP611
Restore key
FP611
Manual restore FL
FP611
Manual carriage operation
Restore reset on compare
FP622
Yes
Carriage sitting on line 1
Carriage will not move
No
No
Compare
Compare line ctr with carriage forms length register
Yes
No
Restore reset
Reset line ctr to 1
Yes
Reset manual restore Tr -
END



CARRIAGE RESTORE KEYS (LEFT AND RIGHT)

The carriage restore keys are operational only when the 5203 is in the not-ready condition. Stop key operation is, therefore, a prerequisite for restore operations when the 5203 is ready. Pressing a carriage restore key causes the form to advance to print line 1.

The carriage-control program counter (which simulates functions of a conventional tape) is set to one. The carriage restore keys are operational when the print unit is tilted back (printer open).

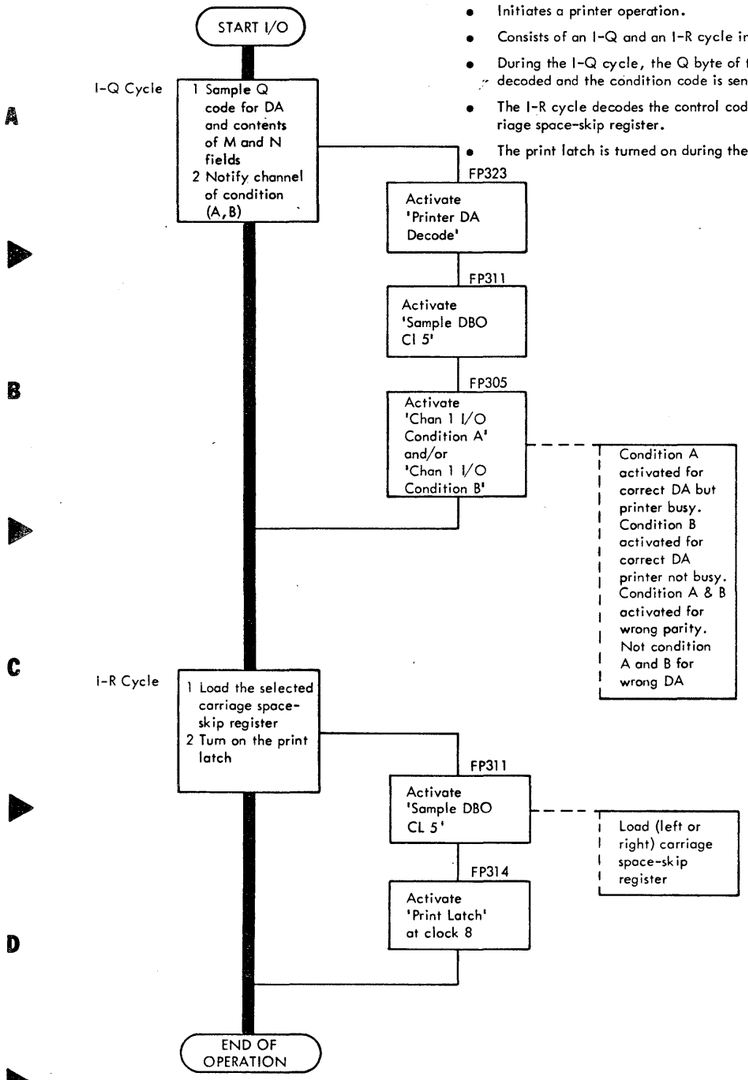
Depression of the left carriage restore key operates the ribbon feed for one second.

CARRIAGE SPACE KEYS (LEFT AND RIGHT)

The carriage space keys are operational only when the printer is in the not-ready condition. Stop key operation is, therefore, a prerequisite for spacing when the printer is ready. Pressing a carriage space key causes the respective form to advance one single space. The space length depends on the setting of the space select lever (either six or eight lines per inch). The carriage space keys are operational when the printer is open.

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

A ▶ B ▶ C ▶ D ▶ E

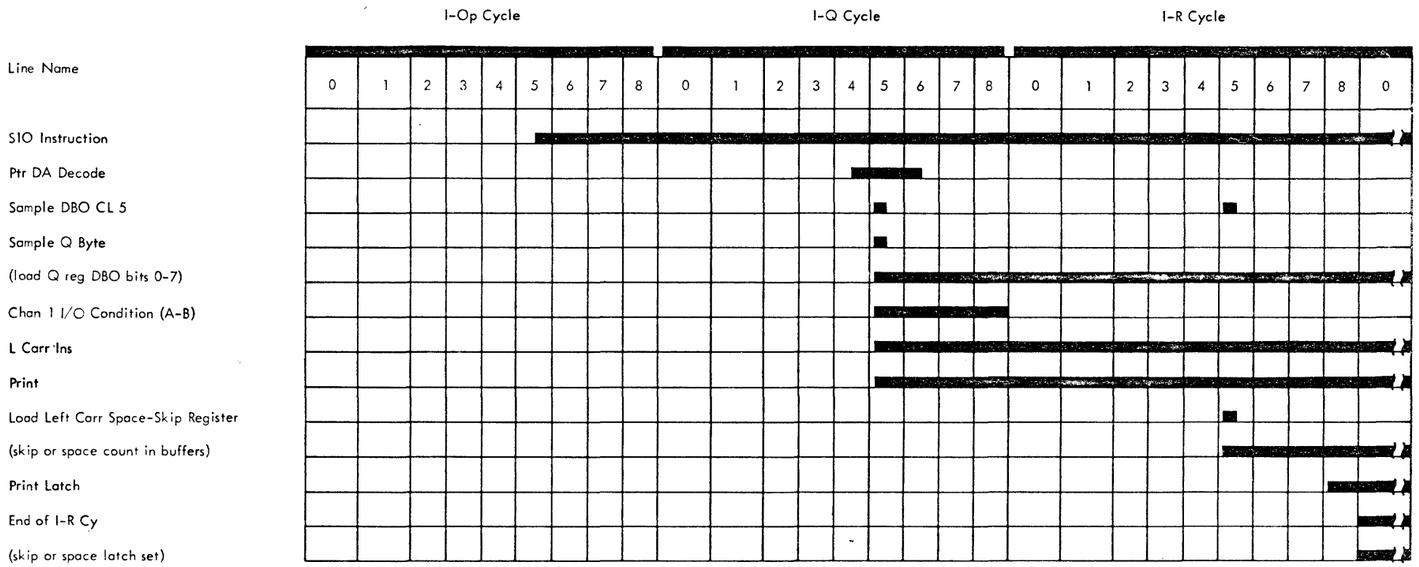


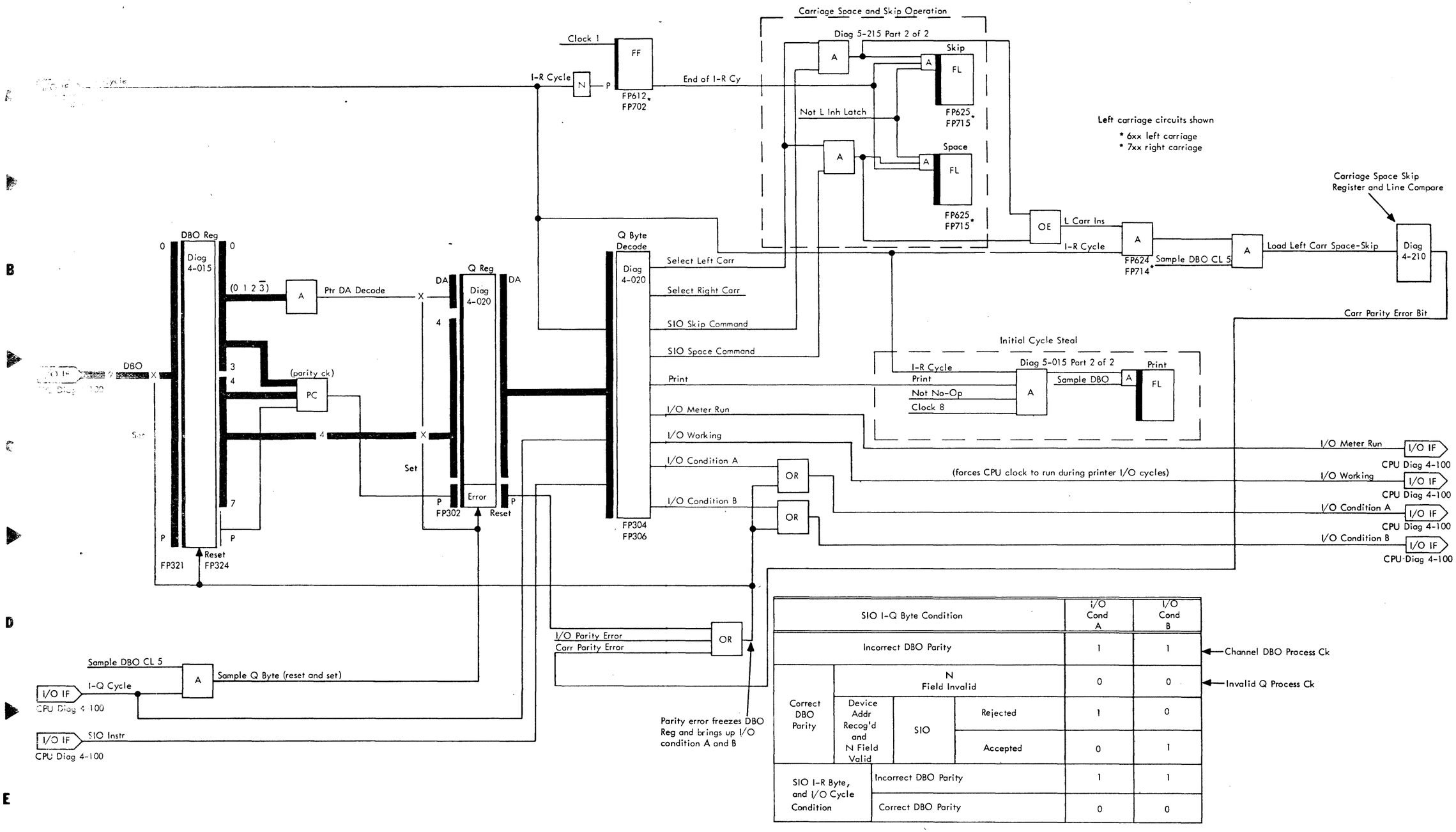
START I/O INSTRUCTION

- Initiates a printer operation.
- Consists of an I-Q and an I-R cycle in the attachment.
- During the I-Q cycle, the Q byte of the instruction is decoded and the condition code is sent back to the CPU.
- The I-R cycle decodes the control code to load the carriage space-skip register.
- The print latch is turned on during the I-R cycle.

M Field	
0	Left carriage
1	Right carriage

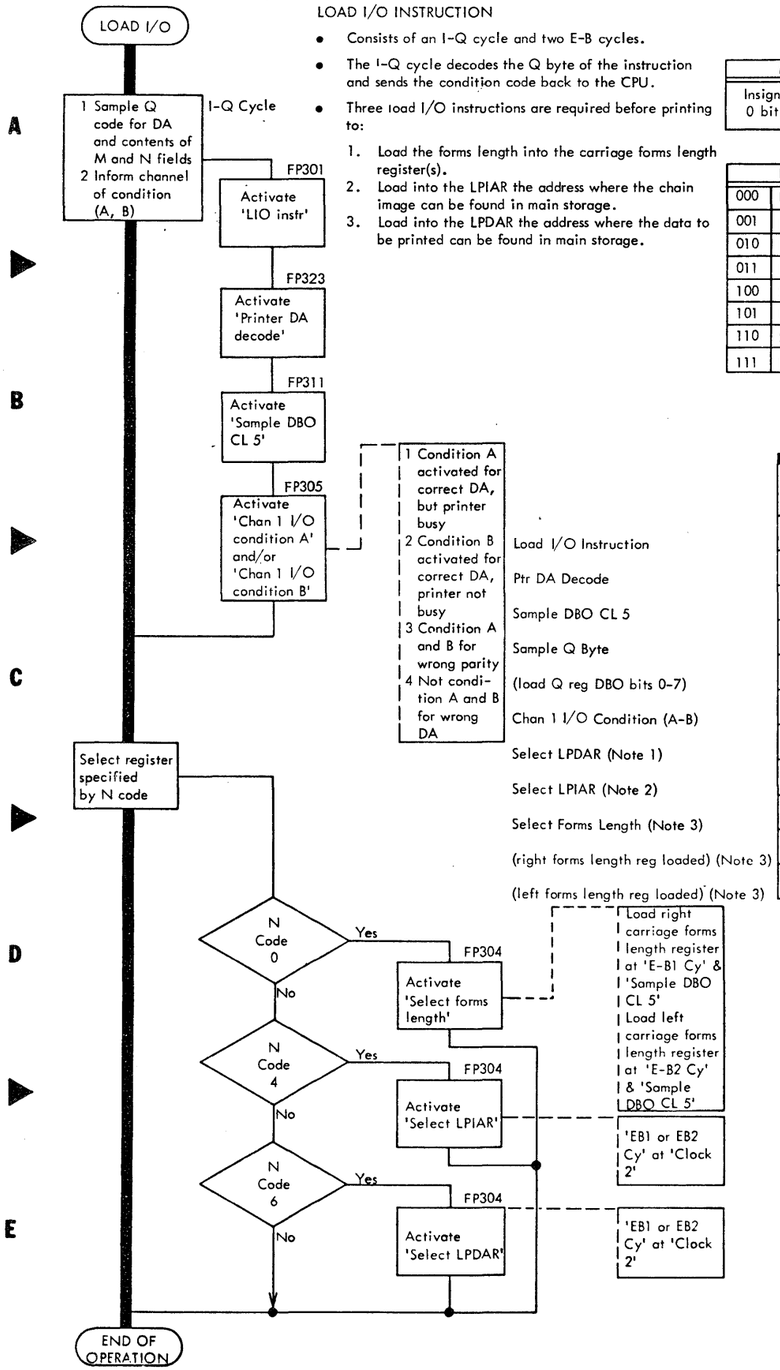
N Field	
000	Space only
001	Invalid
010	Print and space
011	Invalid
100	Skip only
101	Invalid
110	Print and skip
111	Invalid





SIO I-Q Byte Condition				I/O Cond A	I/O Cond B	
Incorrect DBO Parity				1	1	← Channel DBO Process Ck
Correct DBO Parity	N Field Invalid			0	0	← Invalid Q Process Ck
	Device Addr Recog'd and N Field Valid	SIO	Rejected	1	0	
			Accepted	0	1	
SIO I-R Byte, and I/O Cycle Condition	Incorrect DBO Parity			1	1	
	Correct DBO Parity			0	0	

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9



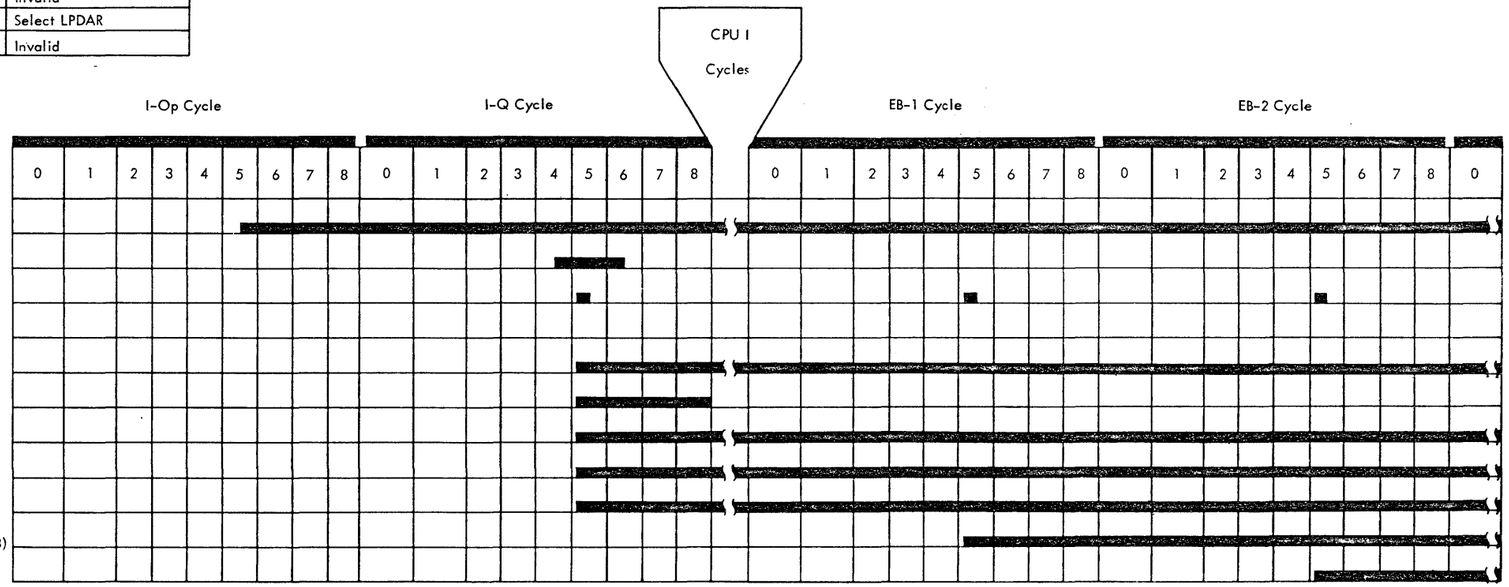
LOAD I/O INSTRUCTION

- Consists of an I-Q cycle and two E-B cycles.
- The I-Q cycle decodes the Q byte of the instruction and sends the condition code back to the CPU.
- Three load I/O instructions are required before printing to:

1. Load the forms length into the carriage forms length register(s).
2. Load into the LPIAR the address where the chain image can be found in main storage.
3. Load into the LPDAR the address where the data to be printed can be found in main storage.

M Field
Insignificant for Load I/O, 0 bit preferred

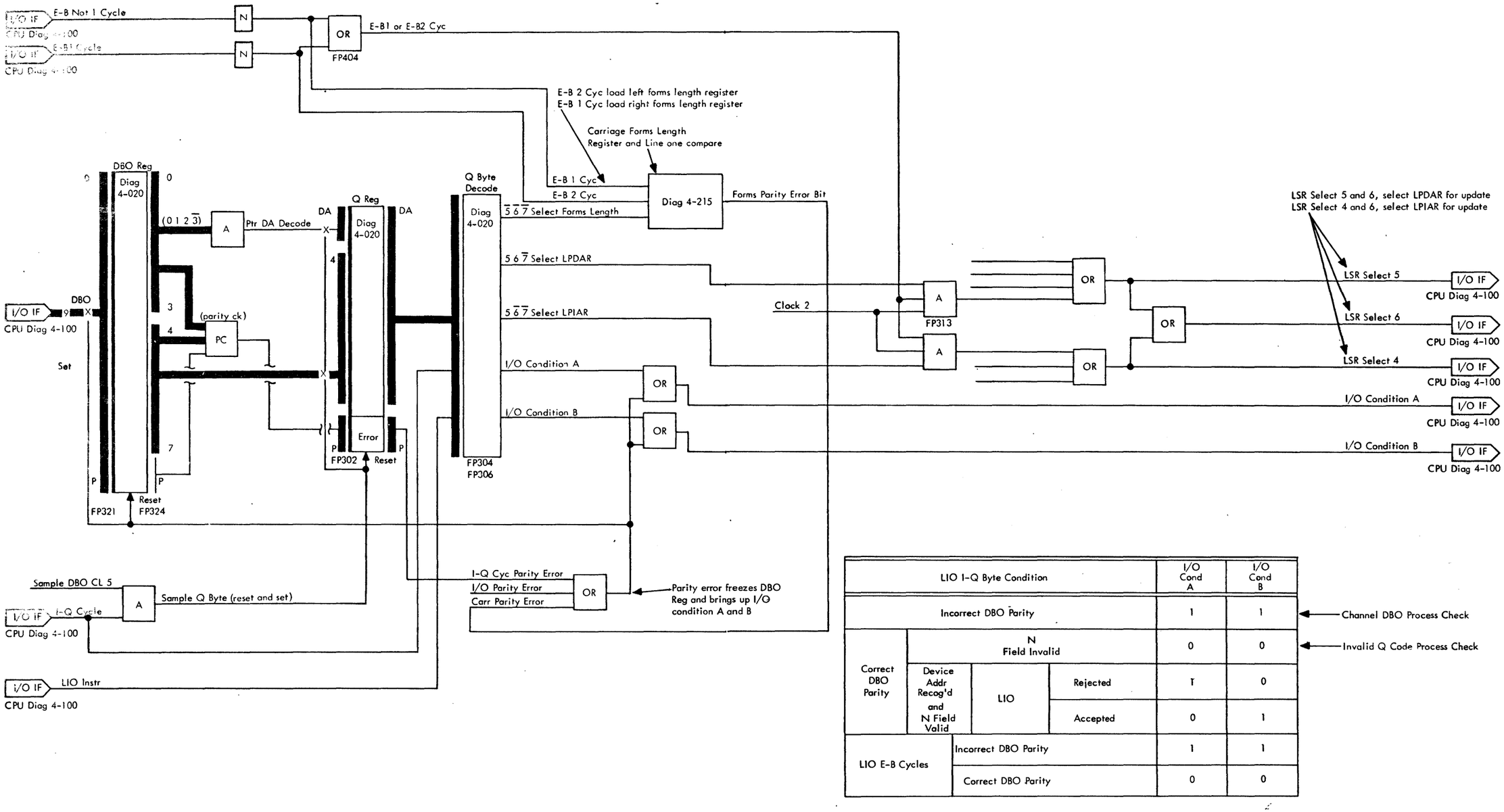
N Field	
000	Load forms length
001	Invalid
010	Invalid
011	Invalid
100	Select LPIAR
101	Invalid
110	Select LPDAR
111	Invalid



Note 1 LPDAR Selected for update if N code bits 5 6 $\overline{7}$, 'Chan 1 LSR Select 5,' and 'Chan 1 LSR Select 6' signal CPU to update LPDAR. The LPDAR will be updated to the contents of the location specified by the address portion of the LIO instruction

Note 2 LPIAR Selected for update if N code bits 5 $\overline{6}$ $\overline{7}$, 'Chan 1 LSR Select 6,' and 'Chan 1 LSR Select 4' signal CPU to update LPIAR. The LPIAR will be updated to the contents of the location specified by the address portion of the LIO instruction

Note 3 Forms length register(s) filled if N code bits $\overline{5}$ $\overline{6}$ $\overline{7}$



LIO I-Q Byte Condition				I/O Cond A	I/O Cond B	
Incorrect DBO Parity				1	1	Channel DBO Process Check
Correct DBO Parity	N Field Invalid			0	0	Invalid Q Code Process Check
	Device Addr Recog'd and N Field Valid	LIO	Rejected	1	0	
			Accepted	0	1	
LIO E-B Cycles	Incorrect DBO Parity			1	1	
	Correct DBO Parity			0	0	

2 ▼ 3 ▼ 4 ▼ 5 ▼ 6 ▼ 7 ▼ 8 ▼ 9

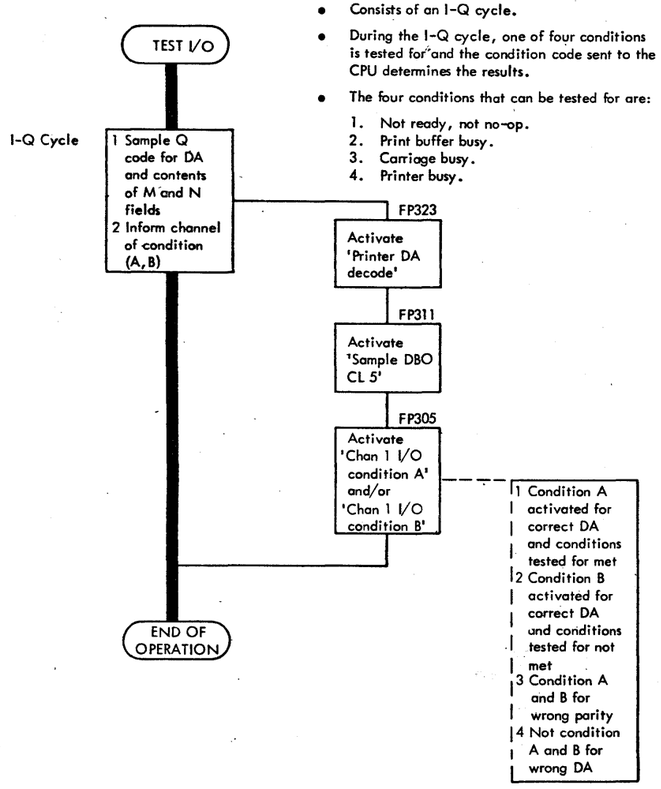
A

B

C

D

E



TEST I/O INSTRUCTION

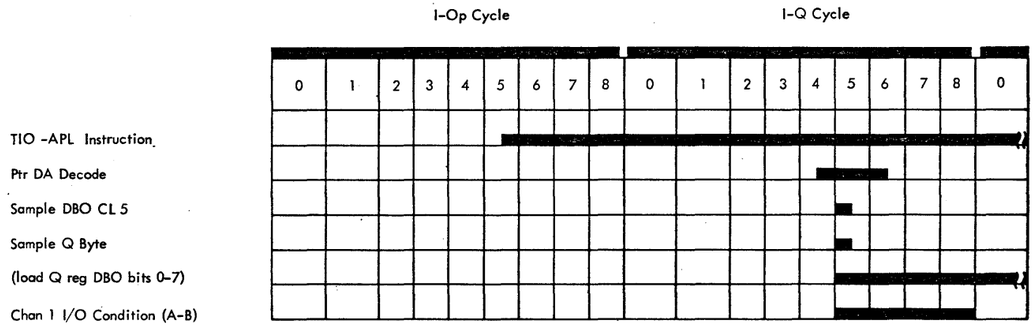
- Consists of an I-Q cycle.
- During the I-Q cycle, one of four conditions is tested for and the condition code sent to the CPU determines the results.
- The four conditions that can be tested for are:
  1. Not ready, not no-op.
  2. Print buffer busy.
  3. Carriage busy.
  4. Printer busy.

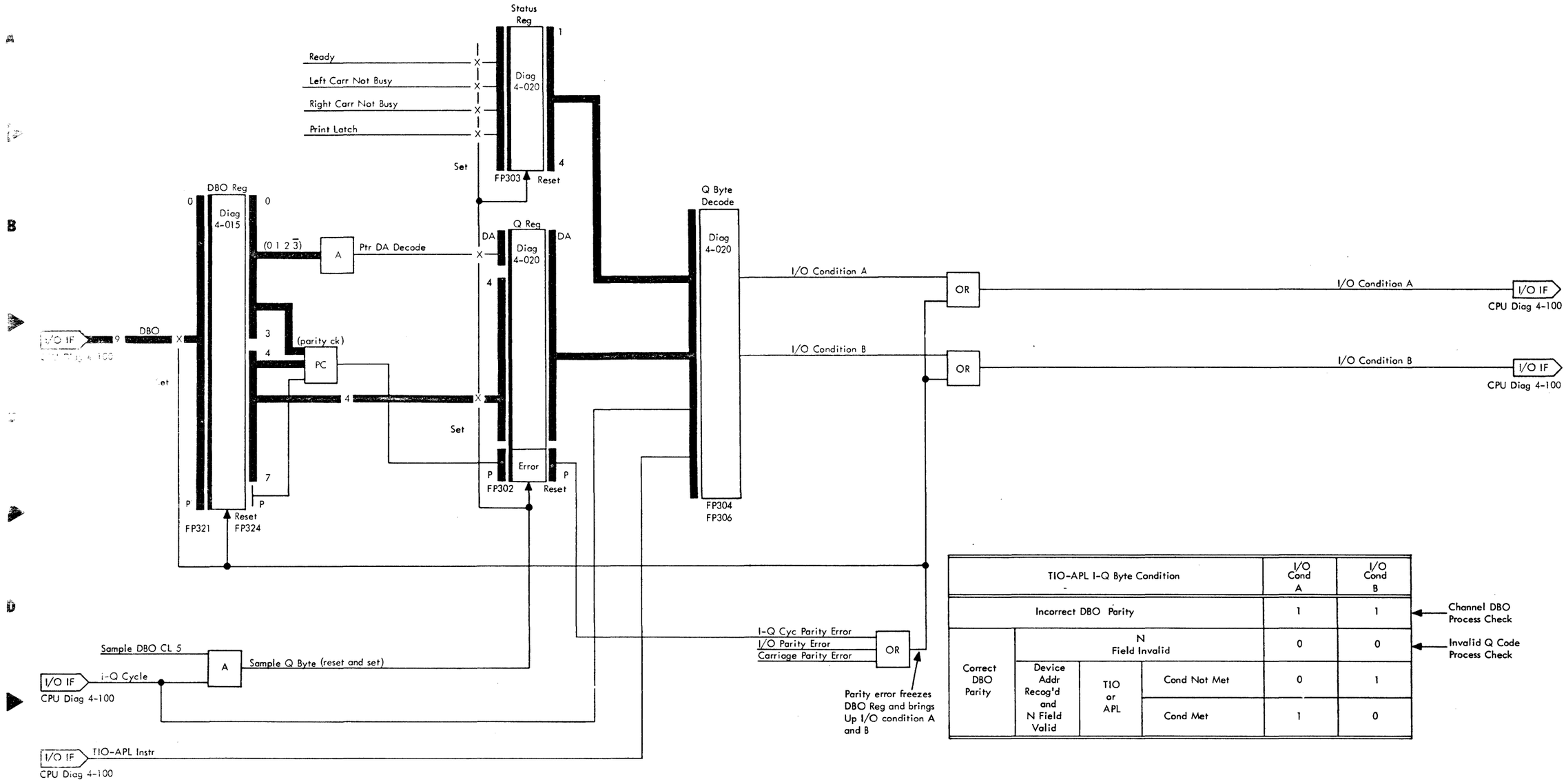
ADVANCE PROGRAM LEVEL INSTRUCTION

- Consists of an I-Q cycle.
- During the I-Q cycle, one of four conditions is tested for and the condition code sent back to the CPU determines the results.
- The four conditions that can be tested for are:
  1. Ready.
  2. Print buffer busy.
  3. Carriage busy.
  4. Printer busy.
- The Advance Program Level instruction is similar to the Test I/O instruction.

M Field	
0	Left carriage
1	Right carriage

N Field	
000	Not ready, Not no-op
001	Invalid
010	Print buffer busy
011	Invalid
100	Carriage busy
101	Invalid
110	Printer busy
111	Invalid





TIO-APL I-Q Byte Condition				I/O Cond A	I/O Cond B	
Incorrect DBO Parity				1	1	Channel DBO Process Check
Correct DBO Parity	N Field Invalid			0	0	Invalid Q Code Process Check
	Device Addr Recog'd and N Field Valid	TIO or APL	Cond Not Met	0	1	
			Cond Met	1	0	

2 3 4 5 6 7 8 9

A B C D E

SENSE I/O

I-Q Cycle

Sample Q code for DA and contents of M and N fields

FP323 — Activate 'printer DA decode'

FP311 — Activate 'sample DBO CL 5'

FP305 — Activate 'chan 1 I/O condition B'

The SNS I/O is always accepted, whether the printer is busy or not

E-B1 Cycle

Check for status specified by N code, and send sense information back on the channel

N Code 0 — Yes: FP714 Activate 'N code 0 • E-B1 CL 1'

N Code 1 — Yes: FP305 Activate 'SNS N code 1 • E-B1'

DBI assembler

N Code 2 — Yes: FP304 Activate 'SNS N code 2'

N Code 3 — Yes: FP305 Activate 'SNS N code 3'

SNS bits assembler

(1) (2)

SENSE I/O INSTRUCTION

- Interrogates the status of the printer attachment logic.
- Consists of an I-Q cycle and two E-B cycles.
- The I-Q cycle decodes the Q byte and sends a condition code of B back to the CPU.
- It is always accepted by the attachment whether it is busy or not.
- The two E-B cycles are taken to check for the condition called for in the N field of the Q byte.
- The sense information is sent back to the CPU.

(1) (2)

N Code 4 — Yes: FP304 Activate 'select LPIAR'; FP313 Activate 'chan 1 LSR select 4' & 'chan 1 LSR select 6'

N Code 6 — Yes: FP304 Activate 'select LPDAR'; FP313 Activate 'chan 1 LSR select 5' & 'chan 1 LSR select 6'

E-B2 Cycle

Check for status specified by N code, and send sense information back on the channel

N Code 0 — Yes: FP624 Activate 'N code 0 • E-B2 CL 1'

N Code 1 — Yes: FP305 Activate 'SNS LPDAR incr'

DBI assembler

N Code 2 — Yes: FP304 Activate 'SNS N code 2'

N Code 3 — Yes: FP305 Activate 'SNS N code 3'

SNS bits assembler

(3) (4)

M Field	
0	Left carriage
1	Right carriage

N Field		
	Byte 2 (E-B2)	Byte 1 (E-B2)
000	L carriage line location	R carriage line location
001	Incr factor of LPDAR	Chain character counter
010	Printer timing byte 2	Printer timing byte 1
011	Printer check status byte 2	Printer check status byte 1
100	LPIAR Hi	LPIAR Lo
101	Not used	Not used
110	LPDAR Hi	LPDAR Lo
111	Not used	Not used

(3) (4)

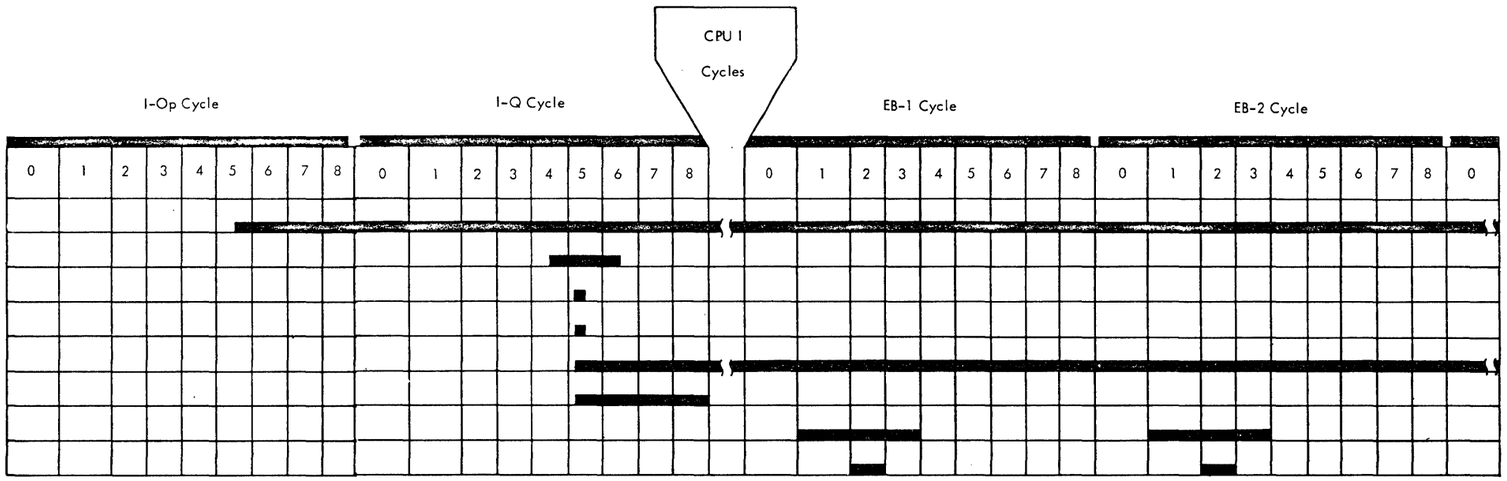
N Code 4 — Yes: FP304 Activate 'select LPIAR'; FP313 Activate 'chan 1 LSR select 4' & 'chan 1 LSR select 6'

N Code 6 — Yes: FP304 Activate 'select LPDAR'; FP313 Activate 'chan 1 LSR select 5 & 'chan 1 LSR select 6'

END OF OPERATION

A

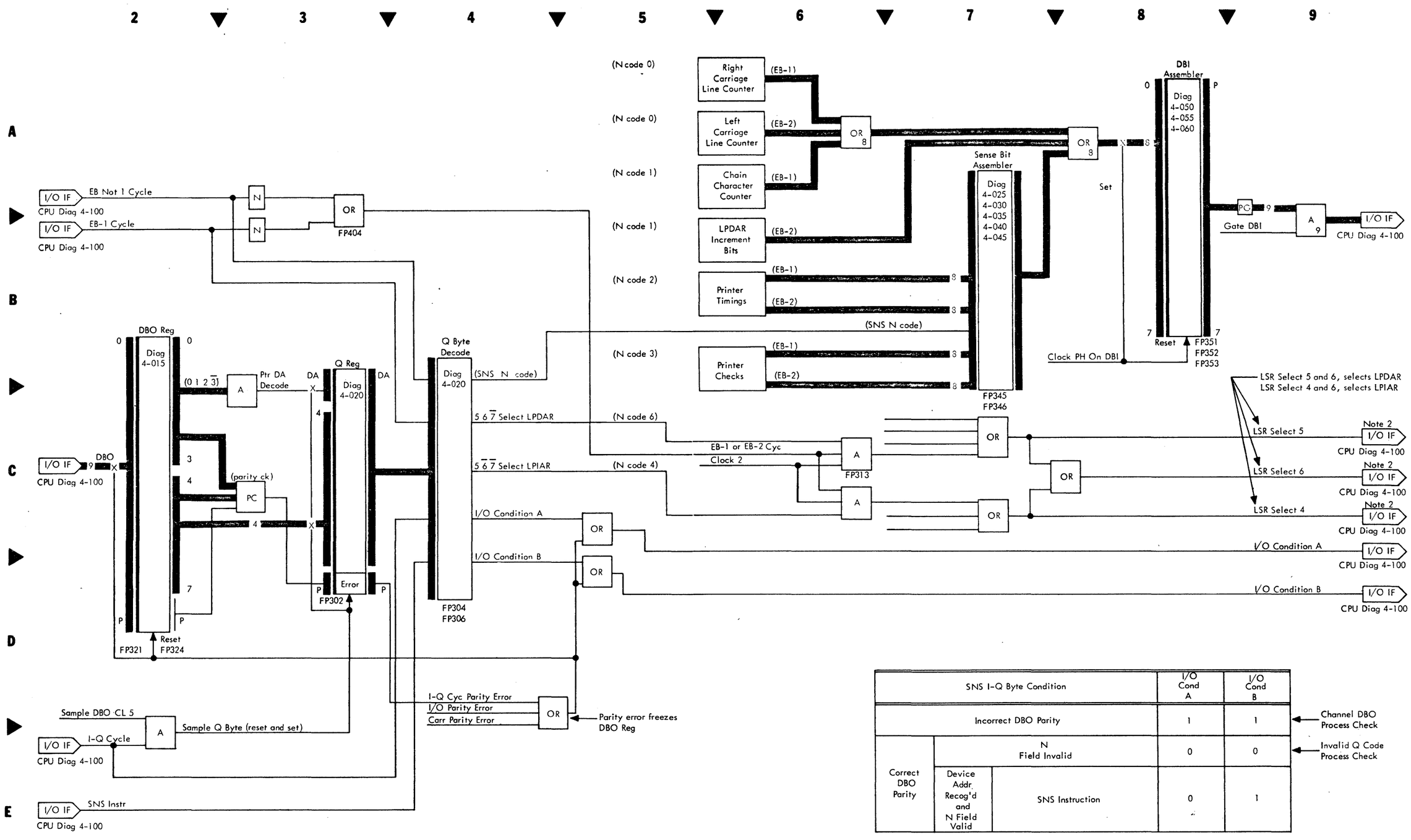
B


CPU I
Cycles
I-Op Cycle
I-Q Cycle
EB-1 Cycle
EB-2 Cycle
0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8 0 1 2 3 4 5 6 7 8 0
SNS I/O Instruction
Ptr DA Decode
Sample DBO CL 5
Sample Q Byte
(load Q reg DBO bits 0-7)
Chan I I/OCondition (A-B)
Gate DBI
(LPDAR or LPIAR select)
Refer to N field decode chart on diagram 5-370 for sense data

C

D

E



SNS I-Q Byte Condition			I/O Cond A	I/O Cond B	
Incorrect DBO Parity			1	1	Channel DBO Process Check
Correct DBO Parity	N Field Invalid		0	0	Invalid Q Code Process Check
	Device Addr Recog'd and N Field Valid	SNS Instruction	0	1	

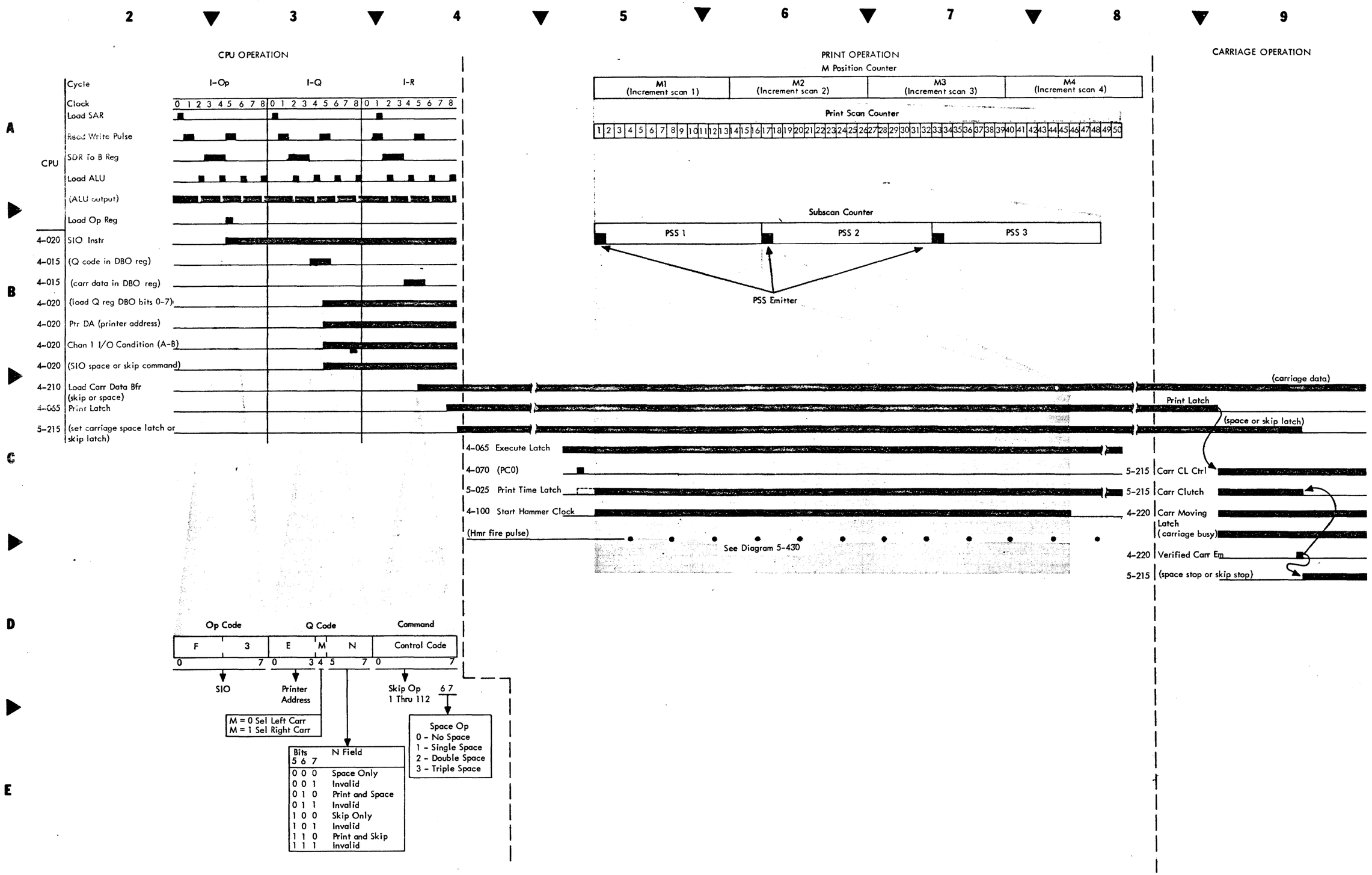
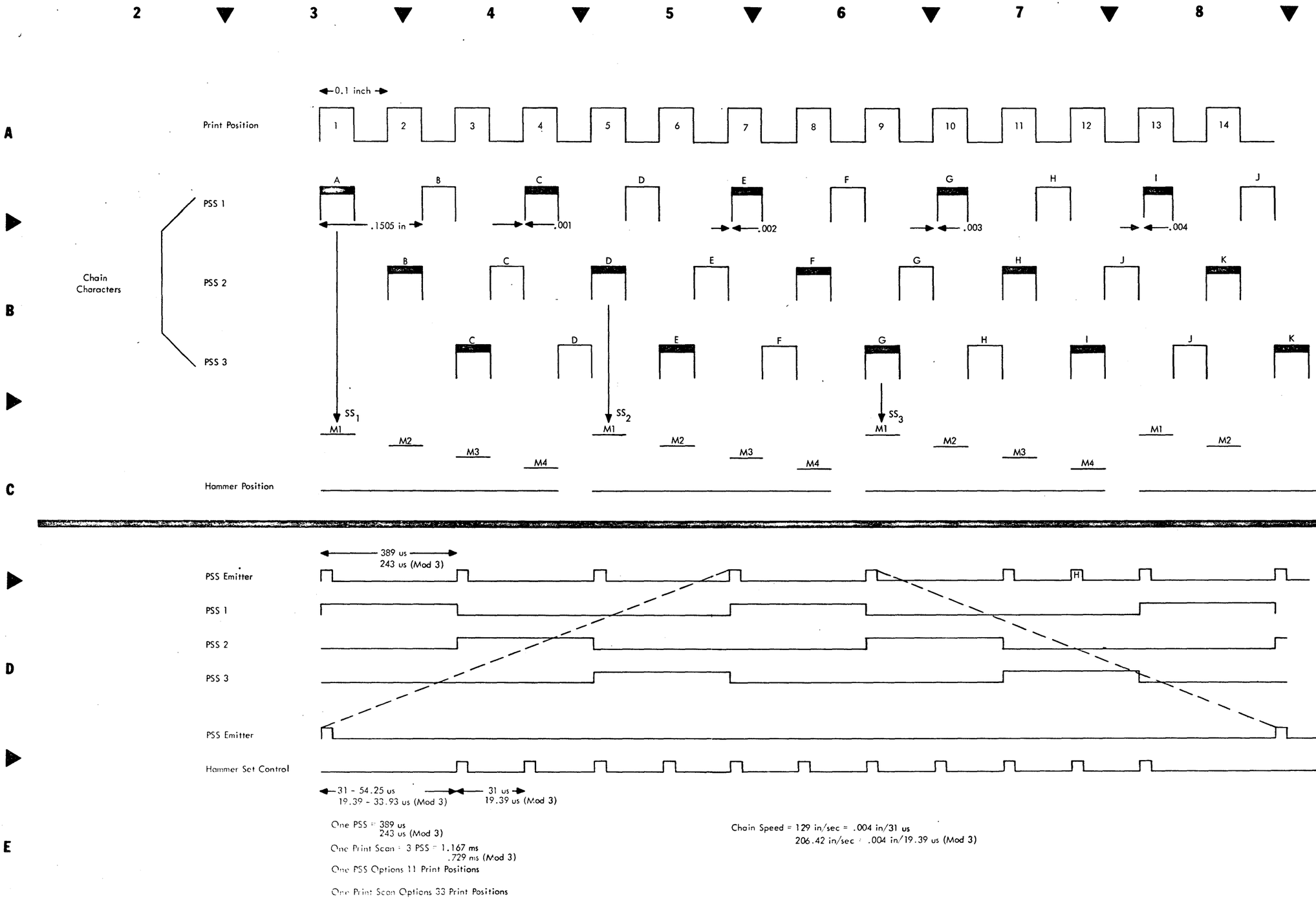


Diagram 5-410. Printer Timings


2
3
4
5
6
7
8
9
A
0.1 inch
Print Position
1
2
3
4
5
6
7
8
9
10
11
12
13
14
B
Chain Characters
PSS 1
PSS 2
PSS 3
A
B
C
D
E
F
G
H
I
J
.1505 in
.001
.002
.003
.004
K
SS1
SS2
SS3
M1
M2
M3
M4
C
Hammer Position
D
389 us
243 us (Mod 3)
PSS Emitter
PSS 1
PSS 2
PSS 3
PSS Emitter
Hammer Set Control
31 - 54.25 us
19.39 - 33.93 us (Mod 3)
31 us
19.39 us (Mod 3)
E
One PSS = 389 us
243 us (Mod 3)
One Print Scan = 3 PSS = 1.167 ms
.729 ms (Mod 3)
One PSS Options 11 Print Positions
One Print Scan Options 33 Print Positions
Chain Speed = 129 in/sec = .004 in/31 us
206.42 in/sec = .004 in/19.39 us (Mod 3)

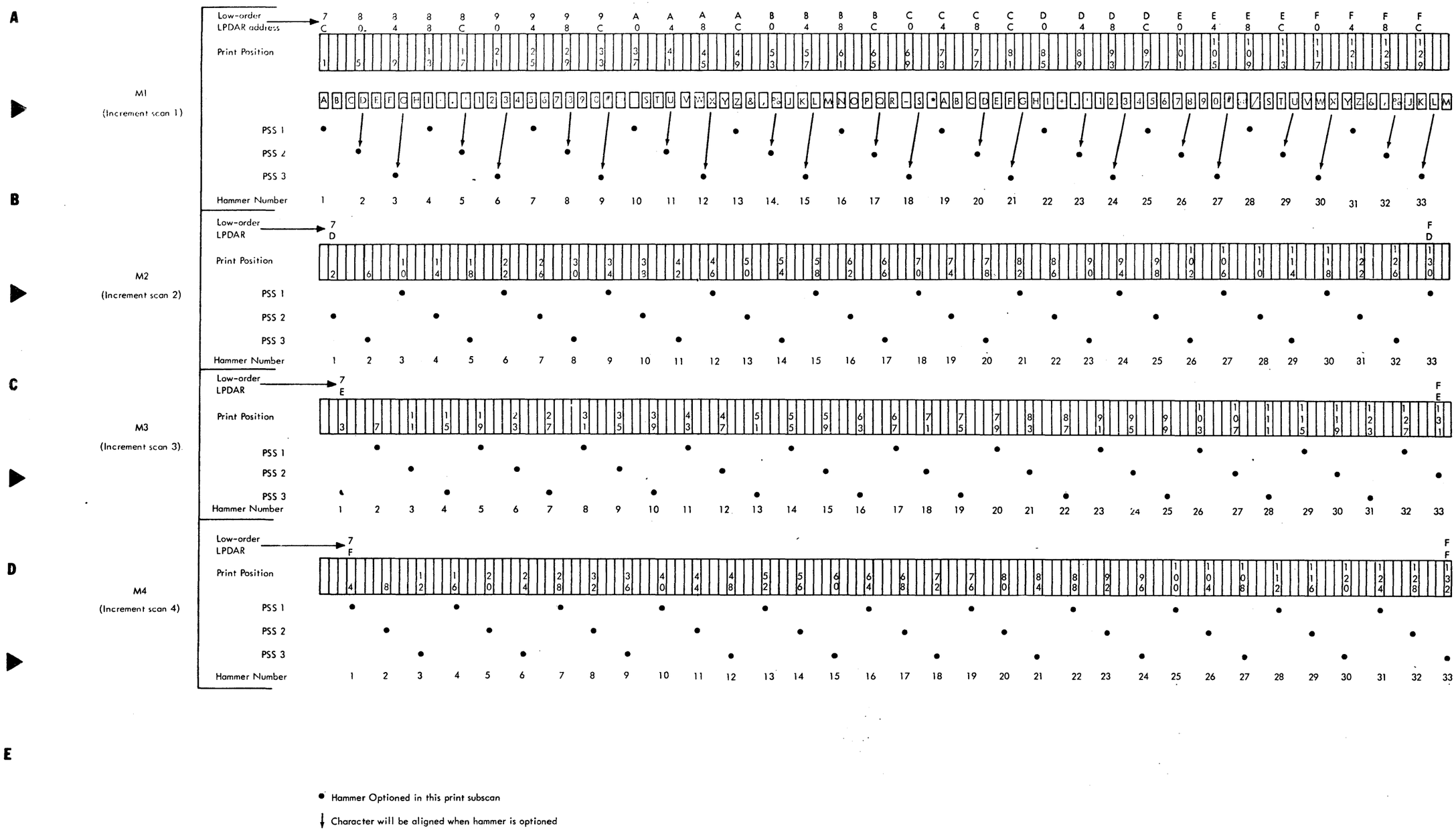


Diagram 5-420. Printing Sequence

2 3 4 5 6 7 8 9

A

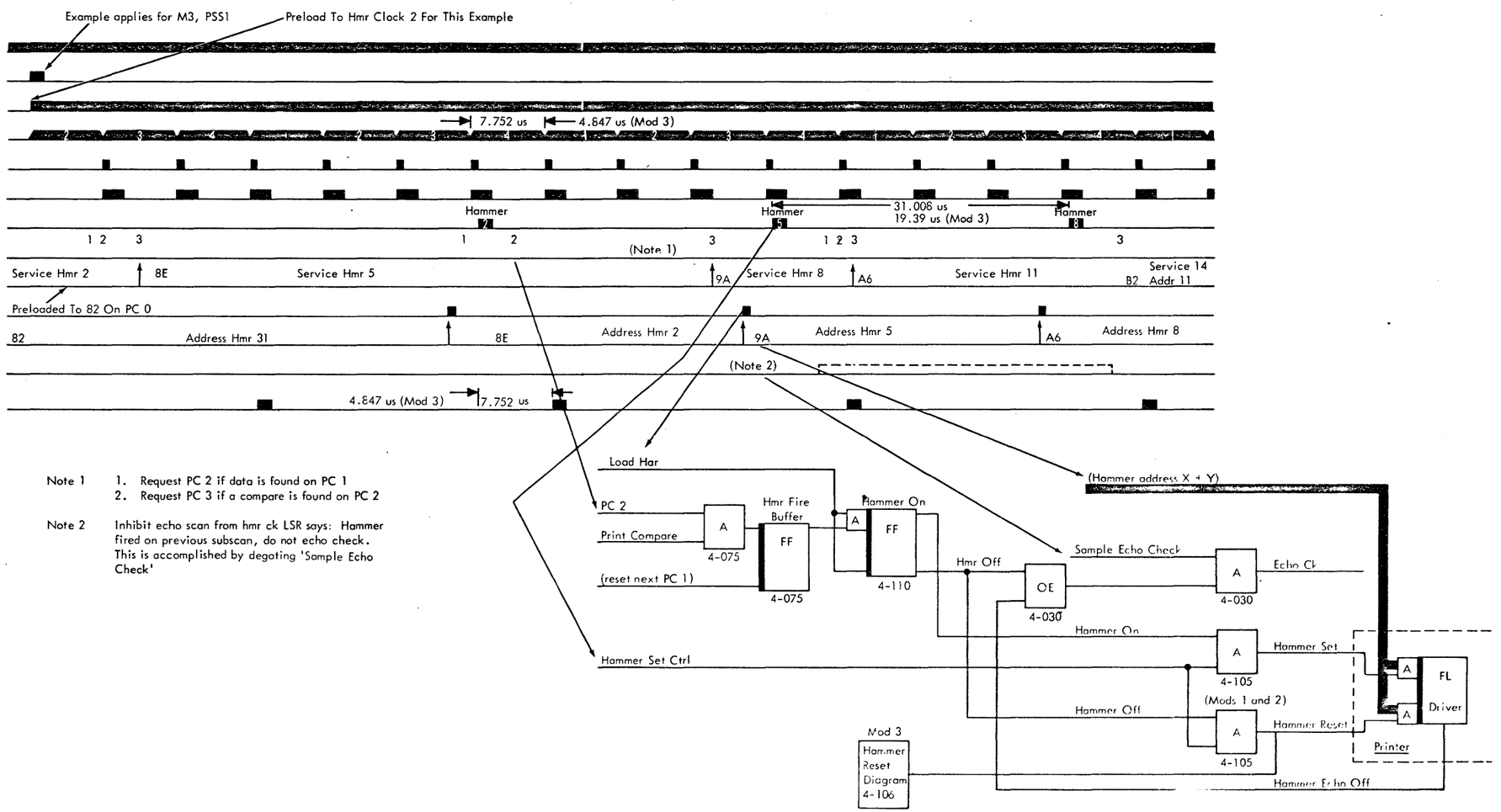
B

C

D

E

4-065 Execute Print
4-080 CC Shift
4-070 Print Time
4-100 Hammer Clocks 1,2,3, and 4
4-100 Hammer Clock Advance
4-100 Hammer Set Control Gate
4-105 Hammer Set Control
4-106 (Mod 3)
4-070 Cycle Steals
4-075 Load Data Reg With Updated Address
4-110 Load Har
4-110 Har Contents
4-125 Inhibit Echo Scan
4-105 Sample Echo Check
4-106 (Mod 3)



Note 1
1. Request PC 2 if data is found on PC 1
2. Request PC 3 if a compare is found on PC 2

Note 2 Inhibit echo scan from hmr ck LSR says: Hammer fired on previous subscan, do not echo check. This is accomplished by degating 'Sample Echo Check'

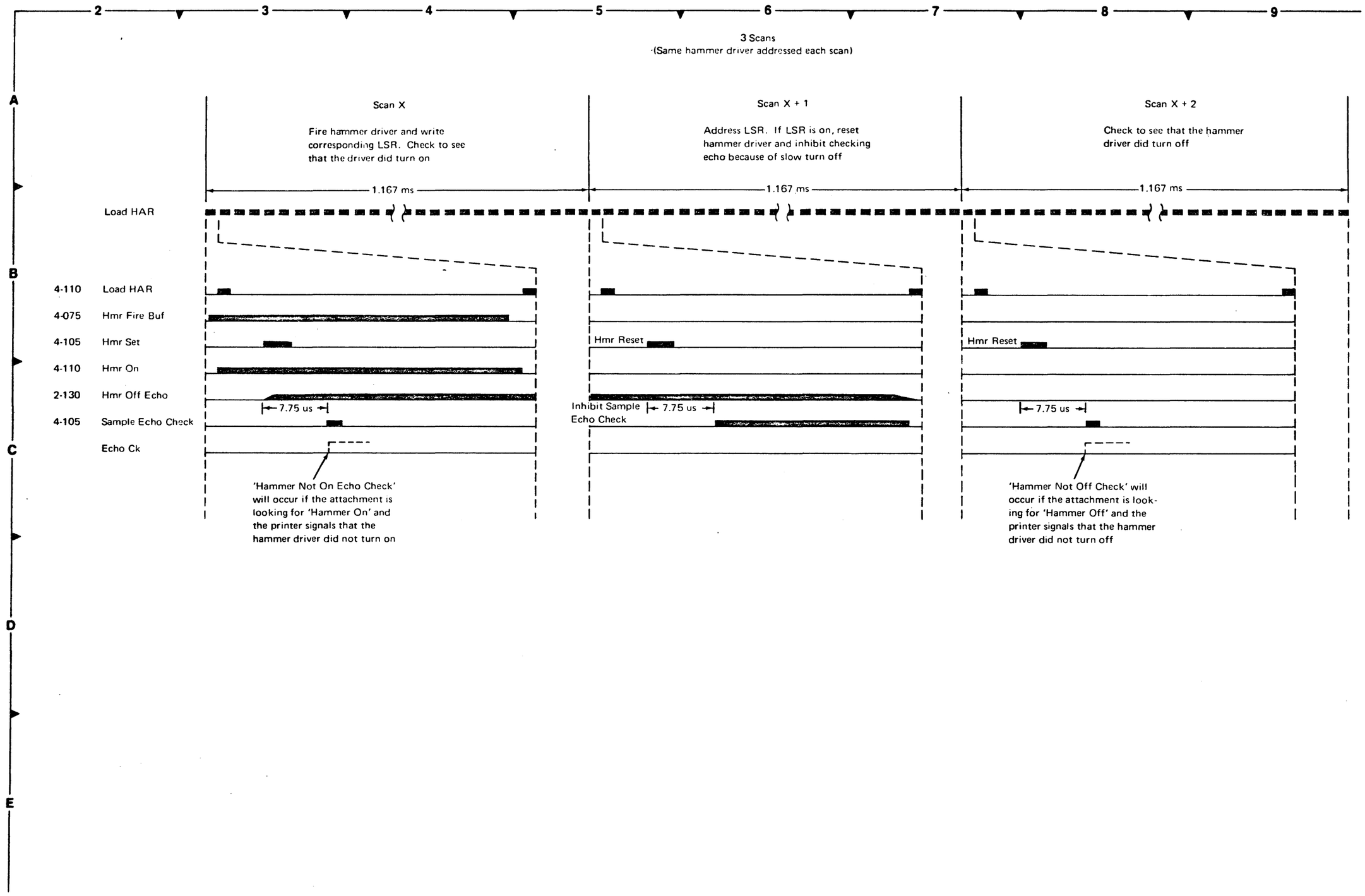
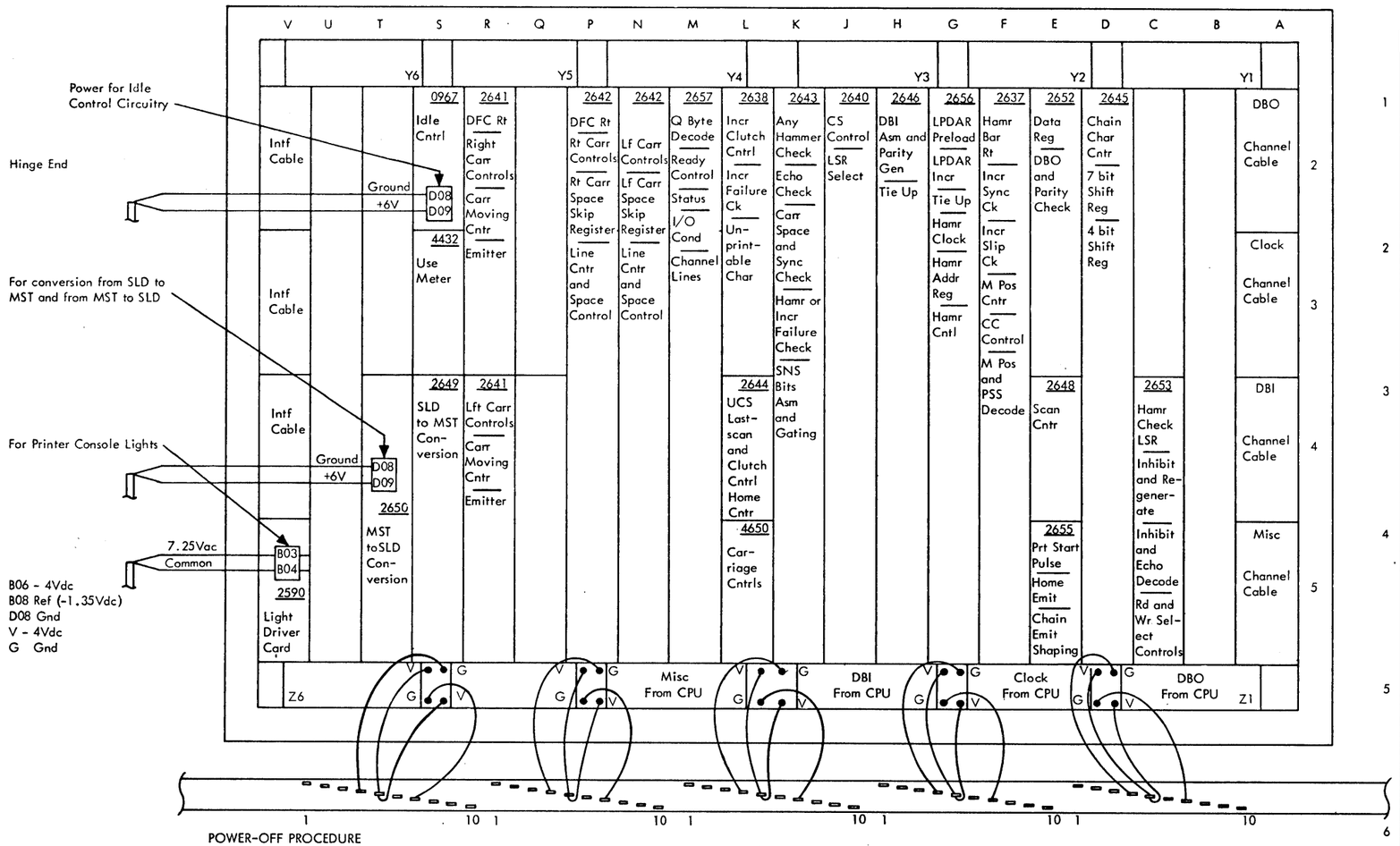


Diagram 5-435. Hammer Echo Check Timing Chart–Models 1 and 2

5203 PRINTER ATTACHMENT PANEL

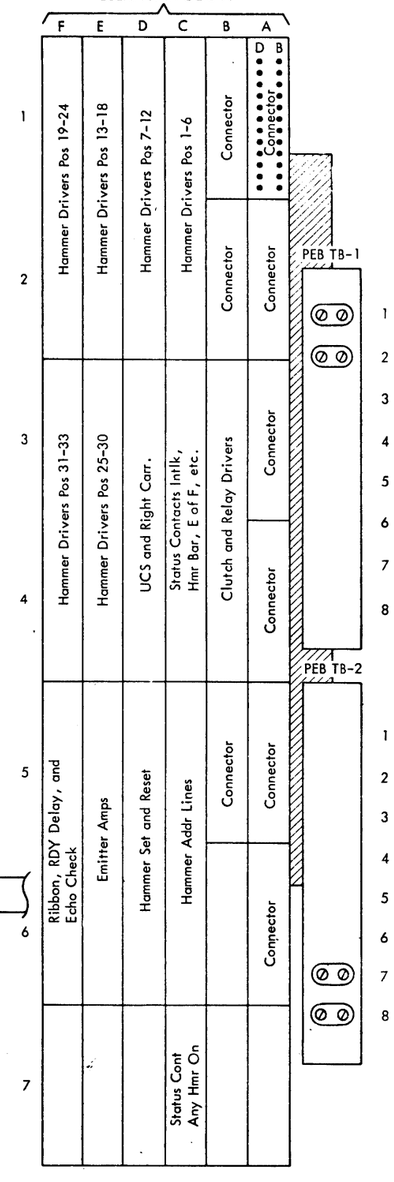
01A-B1

Pin Side View



Pin Side of Board on 5203

Board A1 in Gate A



POWER-OFF PROCEDURE

The minimum safety requirement for any maintenance activity on the 5203 is that power to all motors must be switched off. To remove power from the motors, set the motor power switch (S2) in the printer control box (rear of machine) to OFF.

DANGER

With motor power-off, the 60V power circuit in the printer control box and all terminal blocks (TB's) are still provided with primary and secondary power, and all logic voltages are still present at the printer electronics board.

To remove power completely from the 5203, switch off the system power at the CPU.

The 5203 printer attachment receives all of its logic voltages from the 5410 CPU. Four voltages are furnished by the CPU. These are:

1. -4 Vdc for control logic.
2. +6 Vdc to convert from SLD logic to MST logic.
3. Ground.
4. 7.25 Vac for printer console lights.

Voltages generated in the printer attachment are:

1. -1.35 Vdc (reference).
2. -0.9 Vdc (a plus level).
3. -1.8 Vdc (a minus level).

Diagram 6-100. Power Distribution

Index

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