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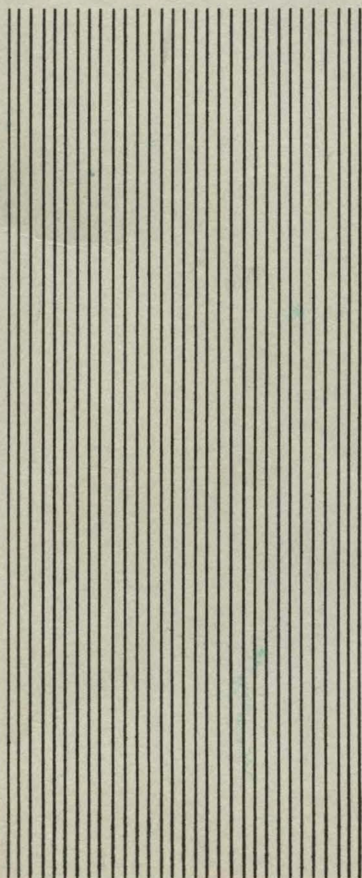
STANDARD TRANSISTORS



STANDARDS ENGINEERING

GUIDANCE INFORMATION

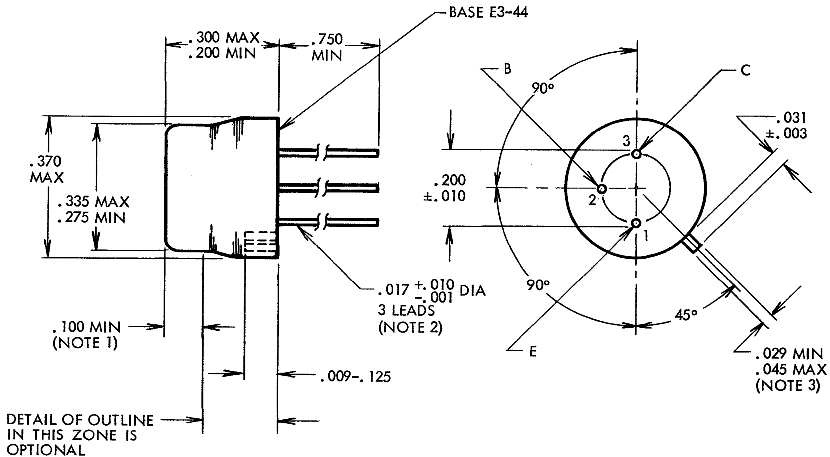
The ratings contained in Section 1 of the individual data sheets and indicated with an asterisk are absolute maximum ratings above which the performance of the devices may be permanently impaired. The remaining values are specified maximums and may possibly be exceeded in some applications without permanent damage to the transistor.

Section 2, General Characteristics, contains the specified procurement limits for the parameters indicated including EOL values where available. Design criteria should be toward the EOL values. The circuit components used for testing purposes are shown on the IBM part drawings.

The characteristic curves for the type 033 labeled "typical" should be used only as a general guide for application. They are valid only for Texas Instrument production and are taken as initial values not derated to EOL changes in vendor, material, or manufacturing processes could cause a shift in these curves.

Special circuit applications not covered by the specifications should have the approval of Semiconductor Applications Engineering.

TRANSISTOR JEDEC OUTLINE TO-5



Note 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

Note 2: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and end of lead a maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

Note 3: Measured from maximum diameter of the actual device.

1. SCOPE

1.1 USAGE. This standard gives a glossary of transistor terms in general use at IBM. These terms are applied to the transistor as a device and not to the associated circuitry.

1.2 DERIVATION OF SYMBOL. The symbols used herein are taken from IRE standards on Letter Symbols for Semi-Conductor Devices, 56IRC 28. S1. When necessary to derive symbols for parameters not listed, the rules as stated in the IRE standard should be used.

1.3 COMPATIBILITY WITH MILITARY STANDARD. Where military and commercial IBM differ in the use of a symbol, the military symbols are given in parenthesis. NOTE: In military publications and IBM military standards, subscripts are not employed on the symbols.

2. GLOSSARY

2.1 I_{CBO}, (I_{CO}) — Collector Cut-Off Current: The current which flows through the collector when the emitter is open circuited and a reverse collector to base voltage is applied.

2.2 I_{CBO*} — Reverse Biased Collector Cut-Off Current: The current which flows through the collector when the base is common and the emitter and collector are at specific reverse voltages.

2.3 I_{EBO}, (I_{EO}), I_{BEO}, (I_{BO}) — Emitter Cut-Off Current, Base Cut-Off Current: The current which flows through the emitter or base when the collector is open-circuited and a reverse emitter to base voltage is applied.

2.4 I_{CEO} — The current which flows through the collector when the base is open circuited and a reverse collector to emitter voltage is applied.

2.5 I_{CEO*}, I_{BEO*} — Reverse Biased Collector Cut-Off Current, Reverse Biased-Base Cut-Off Current: The base or collector current which flows when the emitter is common and the base and collector are at specific reverse voltages.

2.6 I_{ECO*} — Reverse Biased Emitter Cut-Off Current: The current which flows through the emitter when the collector is common and the emitter and base are at specific reverse voltages.

2.7 BV_{CBO}, BV_{CO} — The reverse voltage required between collector and base to give a specified current when the emitter is open circuited.

2.8 BV_{EBO}, BV_{EO} — The reverse voltage required between emitter and base to give a specific current when the collector is open-circuited.

2.9 BV_{CEO}, BV_{CO} — The reverse voltage required between collector and emitter to give a specific current when the base is open-circuited.

2.10 V_{CE} — Collector to Emitter Voltage: The voltage drop from collector to emitter when specific values of collector current and base current are applied.

2.11 V_{BE} — Base to Emitter Voltage: The voltage drop from base to emitter when specific values of collector current and base current are applied.

2.12 α_{FE} — The ratio of the output current (I_C) to the input current (I_B).

α_{FE} is determined by the equation

$$\alpha_{FE} = \frac{I_C}{I_B}$$

where I_B is the applied base current and I_C (the collector current) is measured in a common emitter configuration.

2.13 α_{FE*}, α_{CB} — Computed common emitter current gain. $\alpha_{FE*} = \frac{I_E}{I_{CBO} + I_B}$ where I_E (emitter current) is applied and I_B and I_{CBO} are monitored at a specific collector voltage.

2.14 h_{FE} — The static value of the forward current transfer ratio. (common emitter)

2.15 V_{PT} — Punch-Through Voltage: The maximum voltage at which the collector can be reverse-biased with respect to the base when the emitter is open-circuited, without causing a specified voltage to appear between the emitter and base.

2.16 t_r — Rise Time (See Fig. 1): The rise time of the input pulse is that time in which the amplitude of the leading edge is increasing from 10% to 90% of the maximum pulse amplitude.

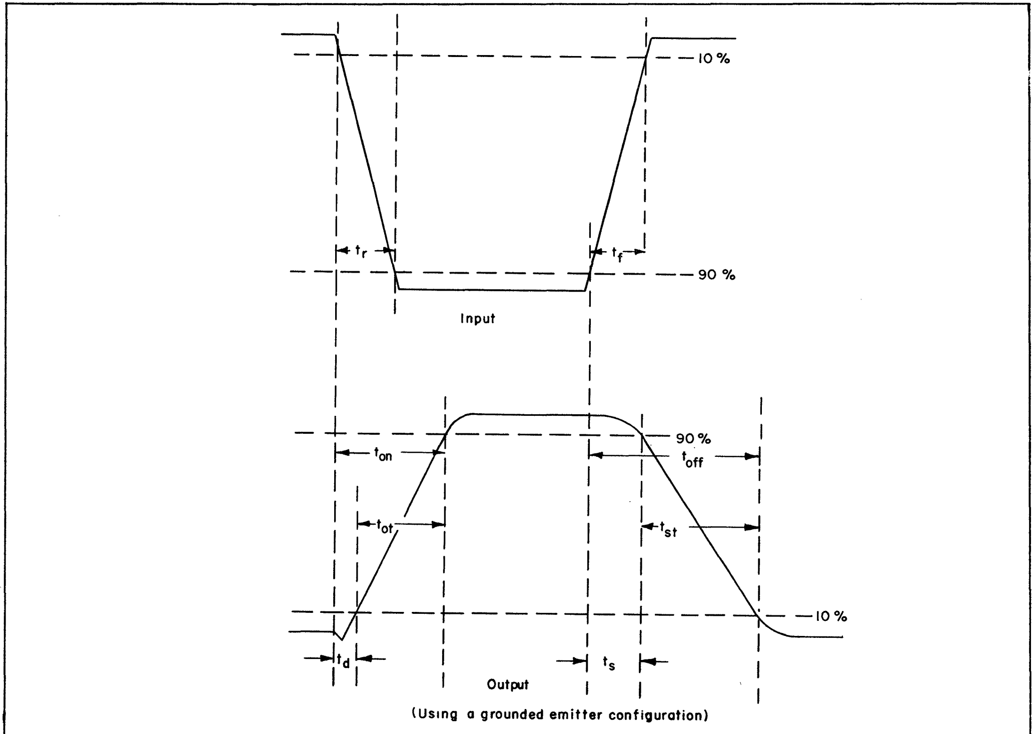


Fig. 1. PULSE RESPONSE

2.17 t_f — Fall Time: The fall time of the input pulse is that time in which the amplitude of the lagging edge is decreasing from 90% to 10% of the maximum pulse amplitude.

2.18 t_d — Turn-On Delay Time: The time interval from when the signal across the input terminals has reached 10% of its maximum amplitude change (while turning the transistor on) to when the signal across the output terminals has reached 10% of its maximum amplitude.

2.19 t_{ot} — Turn-On Transition Time: The time during which the current through the transistor is increasing from 10% to 90% of the maximum amplitude.

2.20 t_{on}, (t_o) — Turn-On Time: The sum of turn on delay and the turn on transition time of the output pulse.

2.21 t_s — Storage Time (Turn-Off Delay): The time interval from when the signal across the input terminals has reached 90% of its maximum amplitude (while turning off the transistor) to when the signal across the output terminals has reached 90% of its maximum amplitude.

2.22 t_{st} — Turn-Off Transition Time: The time during which the current through the transistor is decreasing from 90% to 10% of its maximum amplitude.

2.23 t_{off}, (t_t) — Turn-Off Time: This time is the sum of the turn off delay time and the turn off transition time of the output pulse.

2.24 C_{CB}(C_{ob}) — Collector Capacitance: The capacitance measured from collector to base at specific values of frequency, collector voltage and emitter current.

2.25	$f_{\alpha b}$, $f_{\alpha c}$, $f_{\alpha e}$	Cut-Off Frequency: The frequency at which the magnitude of the small-signal common base current ratio (α_{fb}) has fallen to .707 of the low frequency value.
2.26	R_T, K	Thermal resistance, K factor, is defined as the temperature rise of the junction per unit rise in power dissipation of the device.
2.27	P	Total Power: The total average power dissipation of a transistor.
2.28	P_c	Collector Power (P_b - Base, P_e - Emitter) : The average power dissipation of the designated electrode.
2.29	T_A	Ambient Temperature: The temperature of the medium surrounding an encapsulated transistor.
2.30	T_c	Case Temperature
2.31	T_j	Junction Temperature

TYPE 013 PT. NO. 344892 EC. 203601
DESCRIPTION Ge Alloy Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	20 V	15 V
V_{EBO}	20 V	15 V
* I_C or I_E	70 ma	
POWER @ 55°C	80 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.25	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
f αb	-5					3	25	5						Mc
I_{CBO}	-5						55					32	64	ua
I_{EBO}					-5		55					32	64	ua
I_{BEO}*														
I_{CBO}*	-5				-0.2							32		ua
h_{FE}		7.5		0.19			25	39.5						
		7.5		0.267			25		28.1					
V_{CE}		7.5		0.19			25					0.2		V
		7.5		0.267			25						0.2	V
V_{BE}		7.5		0.19			25					0.3		V
t_d, t_{ot} } t_{on}	-6						25	0.1				1.0		us
t_s, t_{st} } t_{off}														
BV_{CBO}		0.07					55	20	15					V
BV_{EBO}						0.07	55	20	15					V
BV_{CEO}														

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TYPE 015 PT. NO. 526797 EC. 203349

DESCRIPTION Ge Diffused Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	20 V	15 V
V_{EBO}	2.8 V	2.5 V
* I_C or I_E	8 ma	
POWER @ 55°C	100 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
$f_{\alpha b}$	-4					6	25	70						Mc
I_{CBO}														
I_{EBO}														
I_{BEO}*														
I_{CEO}*	-6		0.05				55					55	84	ua
h_{FE}		8		0.4			25	20						
V_{CE}		8		0.4			25					1.0		V
V_{BE}														
t_d, t_{ot} } t_{on}														
t_s, t_{st} } t_{off}														
BV_{CBO}		0.4					55	20	15					V
BV_{EBO}						0.04	55	2.8	2.5					V
BV_{CEO}														

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TYPE 016 PT. NO. 526880 EC. 203349
DESCRIPTION Ge Diffused Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	20 V	15 V
V_{EBO}	1.8 V	1.5 V
* I_C or I_E	8 ma	
POWER @ 55°C	100 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f αb	-4					6	25	70						Mc
I_{CBO}*														
I_{EBO}														
I_{BEO}*														
h_{FE}		8		0.4			25	20						
V_{CE}		8		0.4			25					1.0		V
V_{BE}														
t_d, t_{ot} } t_{on}														
t_s, t_{st} } t_{off}														
BV_{CBO}		0.4					55	20	15					V
BV_{EBO}						0.04	55	1.8	1.5					V
BV_{CEO}														

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IBM Division Standard

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TYPE 021 PT. NO. 526796 EC. 203601
DESCRIPTION Alloy Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	25 V	25 V
V_{EBO}	10 V	10 V
* I_C or I_E	70 ma	
POWER @ 55°C	80 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.25	

2. GENERAL CHARACTERISTICS

TEST CONDITIONS								D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f α b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	-6		0.2				55					26	52	ua
	-15		10				55					30	60	ua
I_{CEO}*	-25		0.2				55					30	60	ua
h_{FE}		7.5		0.19			25	39.5						
		70		2.0			25	35						
		7.5		0.25			25		30					
V_{CE}		7.5		0.19			25					0.2		V
		70		2.0			25					0.38		V
		7.5		0.25			25						0.2	V
V_{BE}		7.5		0.25			25					0.3		V
		70		2.6			25					0.48		V
t_d, t_{ot} } t_{on}	-6							0.1				1.0		us
t_s, t_{st} } t_{off}	-18		-18		-6			0.4				1.5		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 025 PT. NO. 318322 EC 203601

DESCRIPTION Alloy Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	16 V	16 V
V_{EBO}	6 V	6V
* I_C or I_E	70 ma	
POWER @ 55°C	80 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.25	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN		TYPICAL		MAX		
								INIT	EOL	INIT	EOL	INIT	EOL	
$f_{\alpha b}$														
I_{CBO}														
I_{EBO}														
I_{BEO}*	-6		0.2				55					30	60	ua
	-10		6				55					35	70	ua
I_{CEO}*	-16		0.2				55					35	70	ua
h_{FE}		7.5		0.28			25	26.8						
		20		0.71			25	28.2						
		7.5		0.34			25		22					
V_{CE}		7.5		0.28			25					0.2		V
		20		0.71			25					0.2		V
		7.5		0.34			25						0.2	V
V_{BE}		7.5		0.34			25					0.3		V
		20		0.89			25					0.35		V
t_d, t_{ot} } t_{on}	-6						25	0.1				1.5		us
t_s, t_{st} } t_{off}	-18		-18		-6		25	0.4				1.5		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 026 PT. NO. 535441 EC. 203600
DESCRIPTION Medium Power Alloy PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	45 V	45 V
V_{EBO}	15 V	15 V
* I_C or I_E	350 ma	
POWER @ 55°C	150 mw	
* T_{JCT}	85° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

TEST CONDITIONS								D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f α b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	-20		0.3				55					120		ua
	-30		15				55					200	400	ua
I_{CEO}*	-45		0.3				55					200	400	ua
h_{FE}		7.5		0.19			25	39.5						
		350		14			25	25						
		350		17.5			25		20					
V_{CE}		7.5		0.19			25					0.2		V
		350		14			25					0.35		V
		350		17.5			25						0.35	V
V_{BE}		7.5		0.25			25					0.3		V
		350		17.5			25					0.75		V
t_d / t_{ot} } t_{on}	-20		12				25					5		us
t_s / t_{st} } t_{off}														
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 033 PT. NO. 318324 EC. 203601
DESCRIPTION Alloy Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	25 V	25 V
V_{EBO}	10 V	10 V
* I_C or I_E	70 ma	
POWER @ 55°C	80 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.25	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	-6		0.2				55					26	52	ua
	-15		10				55					30	60	ua
I_{CEO}*	-25		0.2				55					30	60	ua
h_{FE}		7.5		0.19			25	39.5						
		50		2			25	25						
		7.5		0.25			25		30					
V_{CE}		7.5		0.19			25					0.2		V
		50		2			25					0.3		V
		7.5		0.25			25						0.2	V
V_{BE}		7.5		0.25			25					0.3		V
		50		2.5			25					0.48		V
t_d } t_{on} t_{ot} }	-6						25	0.1				1		us
t_s } t_{off} t_{st} }	-18		-18		-6		25	0.4				1.5		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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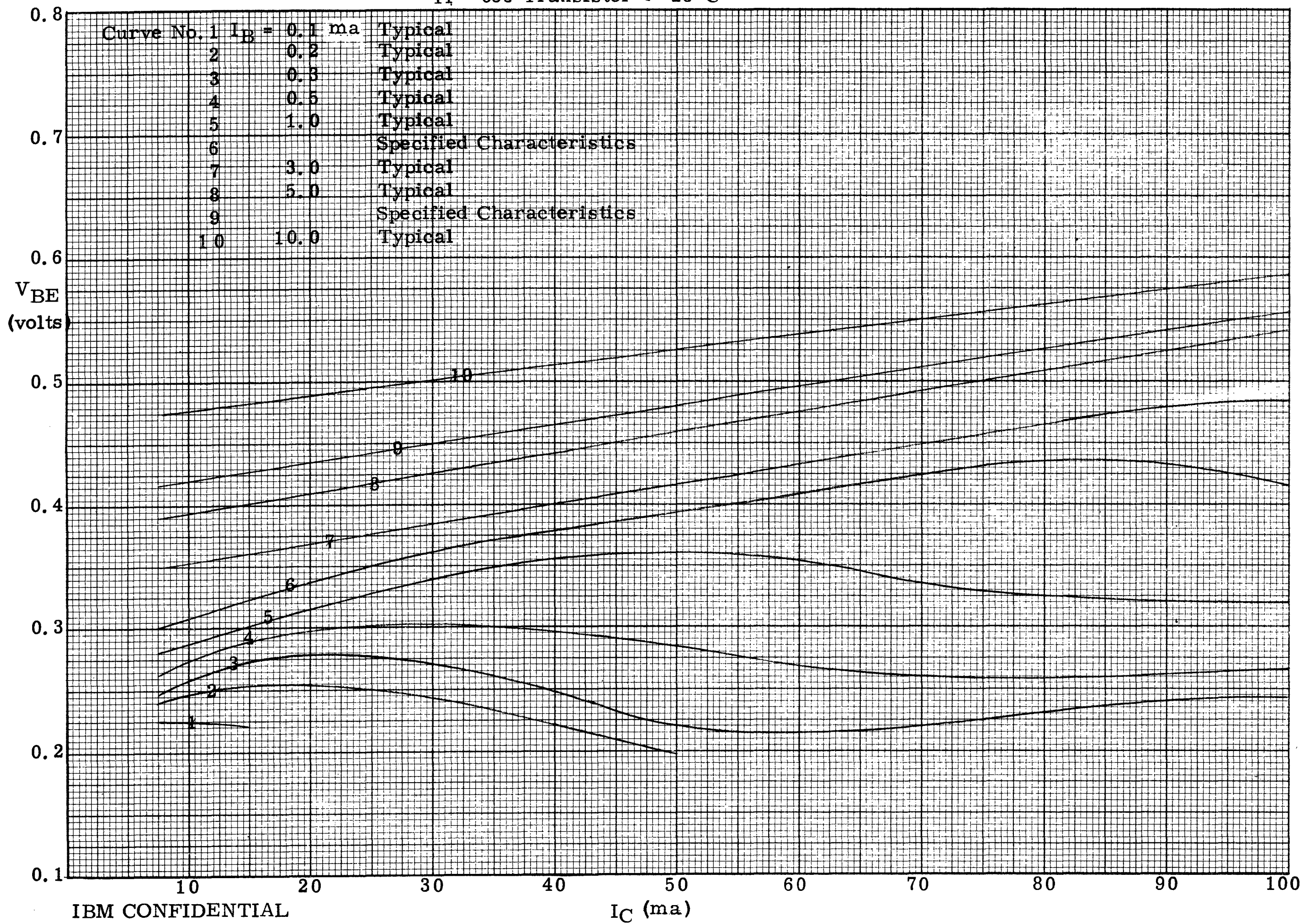
V_{BE} vs. I_C

TI - 033 Transistor @ 25°C



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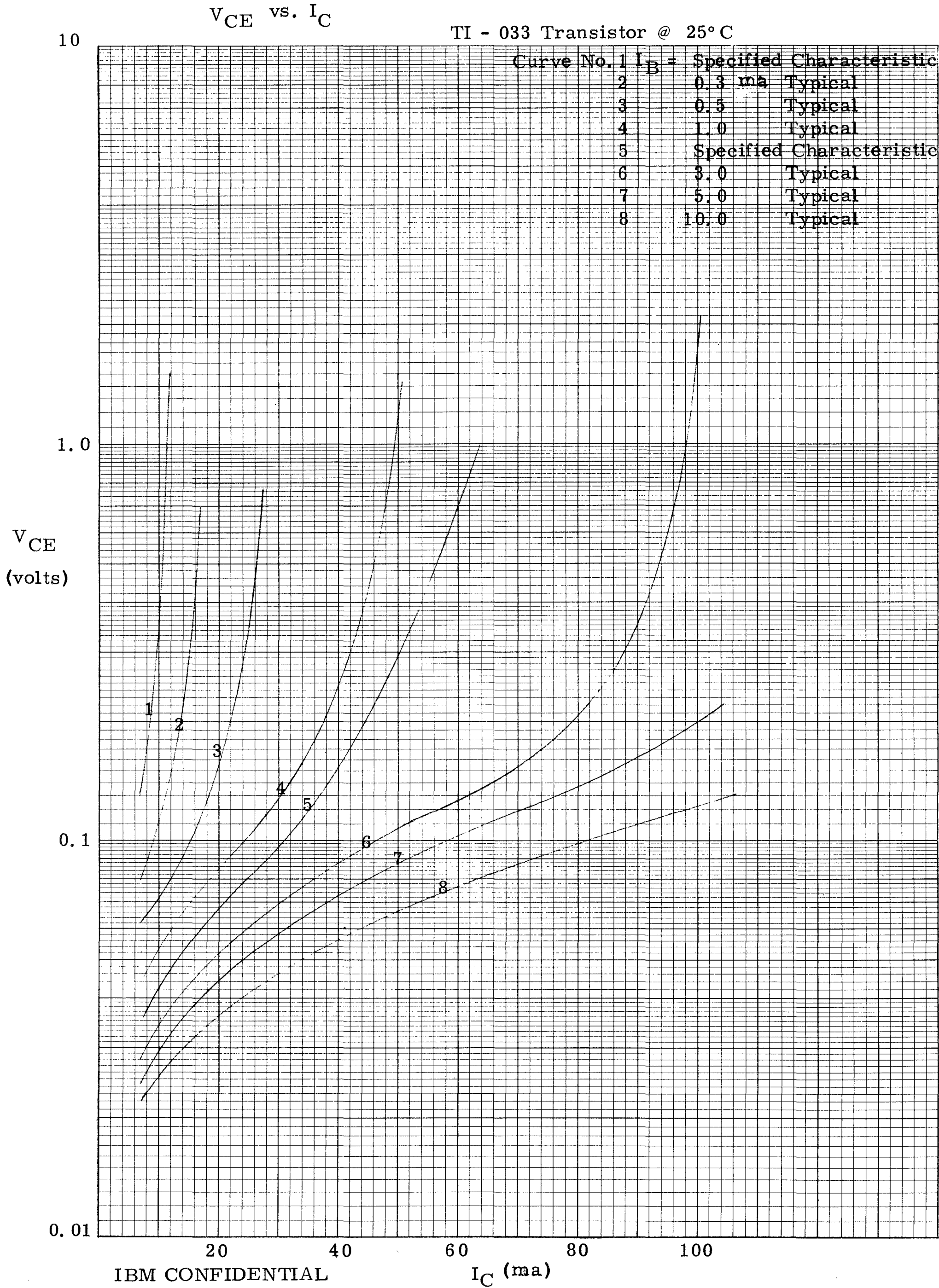
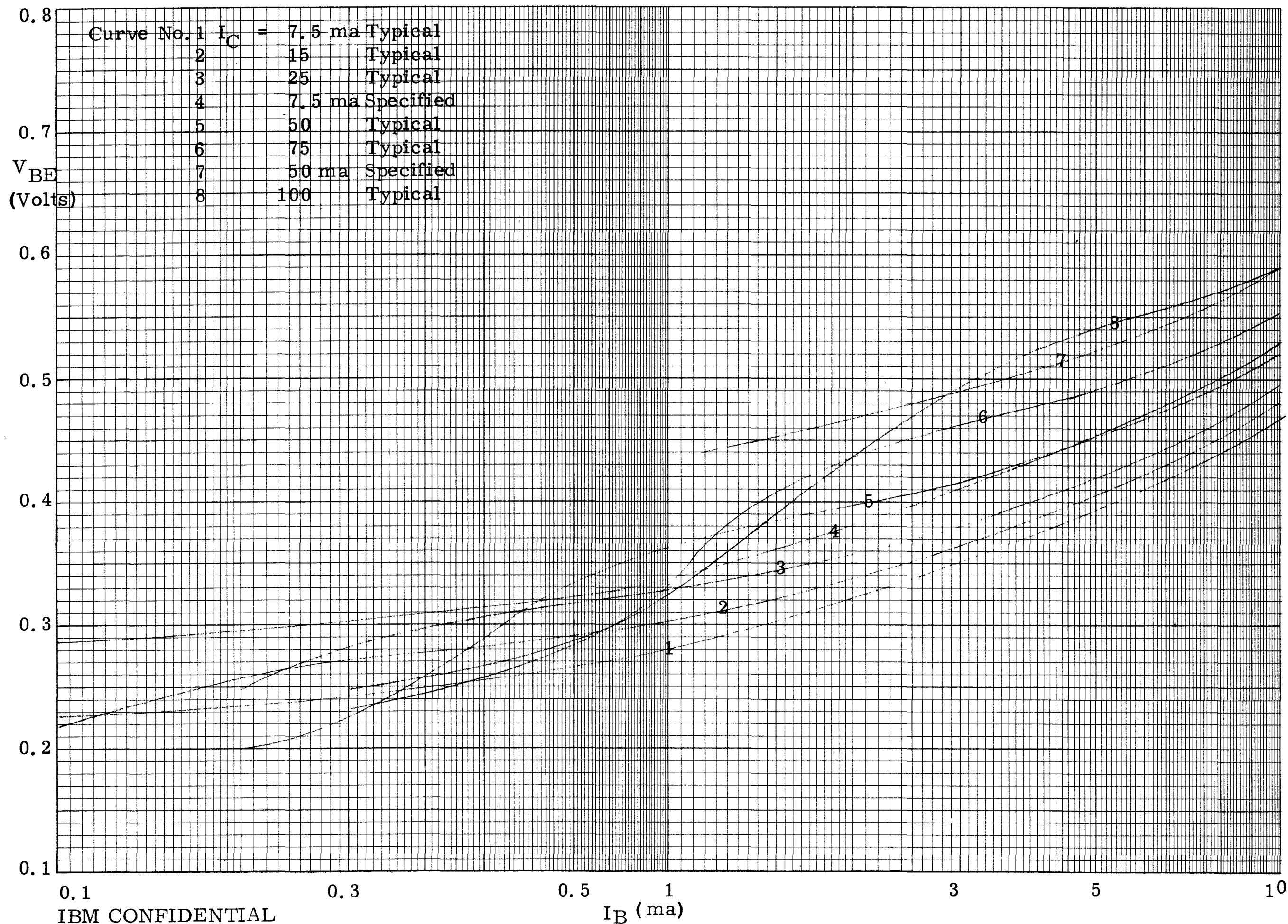
TI-033 TRANSISTOR


V_{CE} vs. I_C
TI - 033 Transistor @ 25° C
Curve No. 1 I_B = Specified Characteristic
2 0.3 ma Typical
3 0.5 Typical
4 1.0 Typical
5 Specified Characteristic
6 3.0 Typical
7 5.0 Typical
8 10.0 Typical
10
1.0
0.1
0.01
V_{CE}
(volts)
1
2
3
4
5
6
7
8
20
40
60
80
100
I_C (ma)

V_{BE} vs. I_B TI - 033 Transistor @ 25° C



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TI-033 TRANSISTOR

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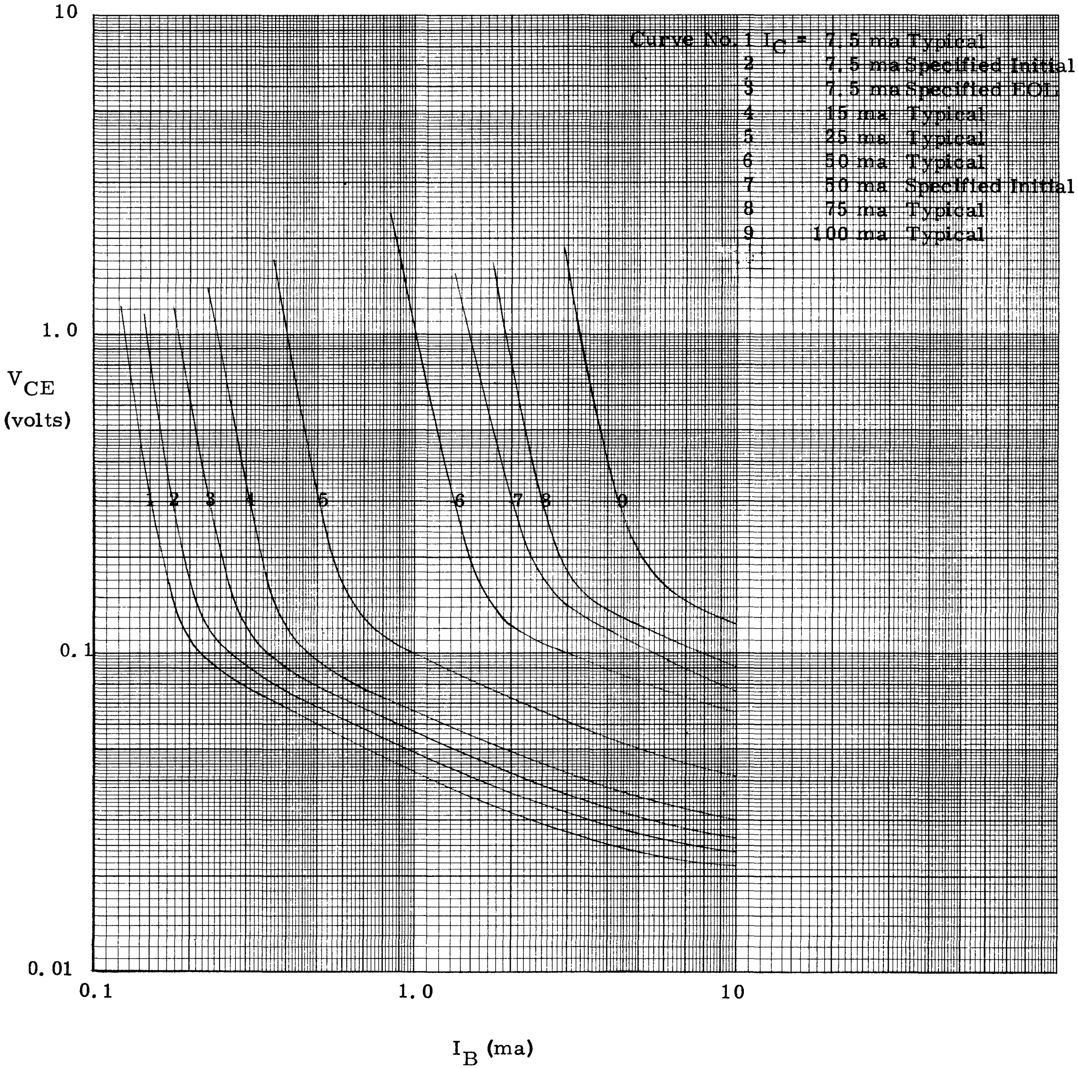
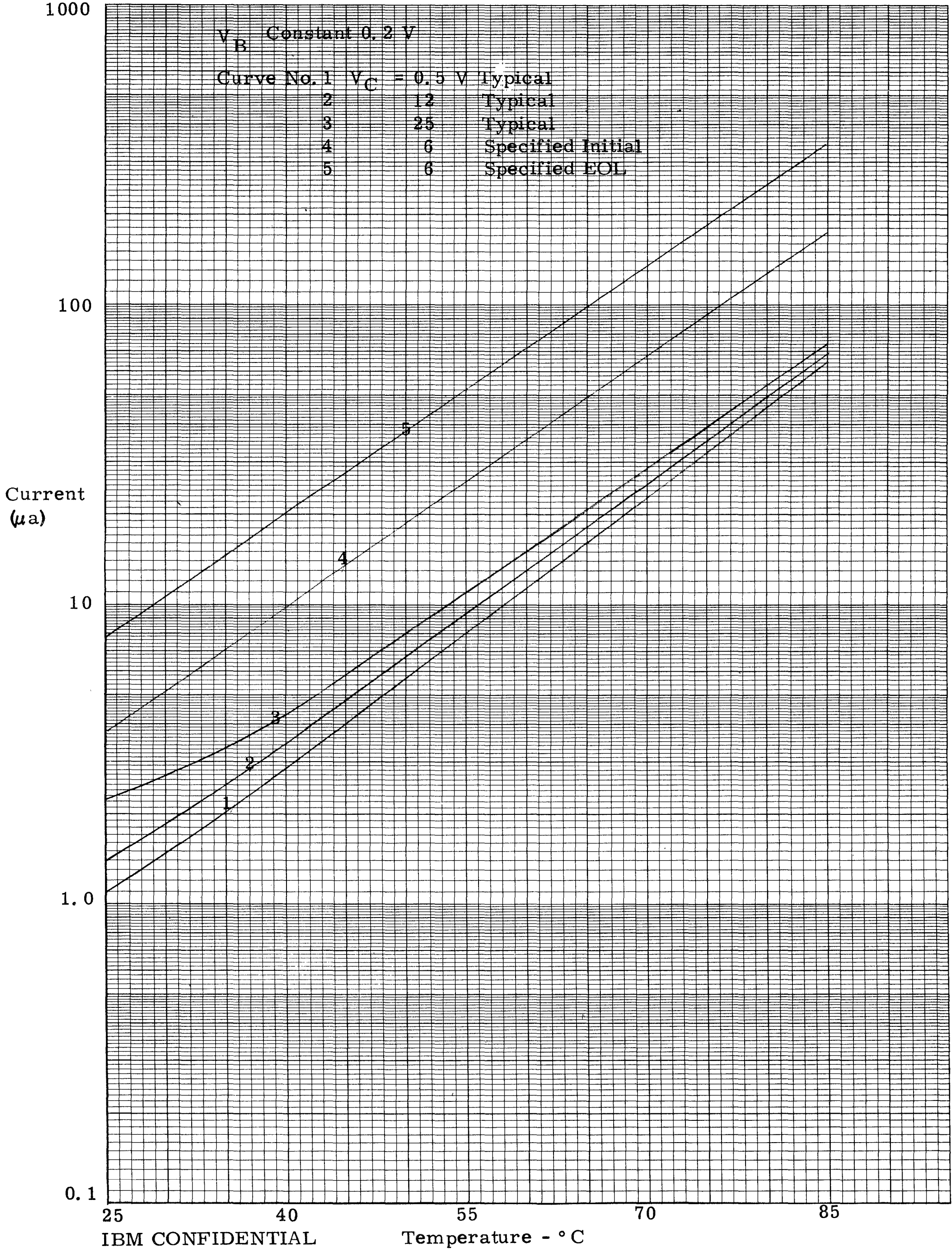
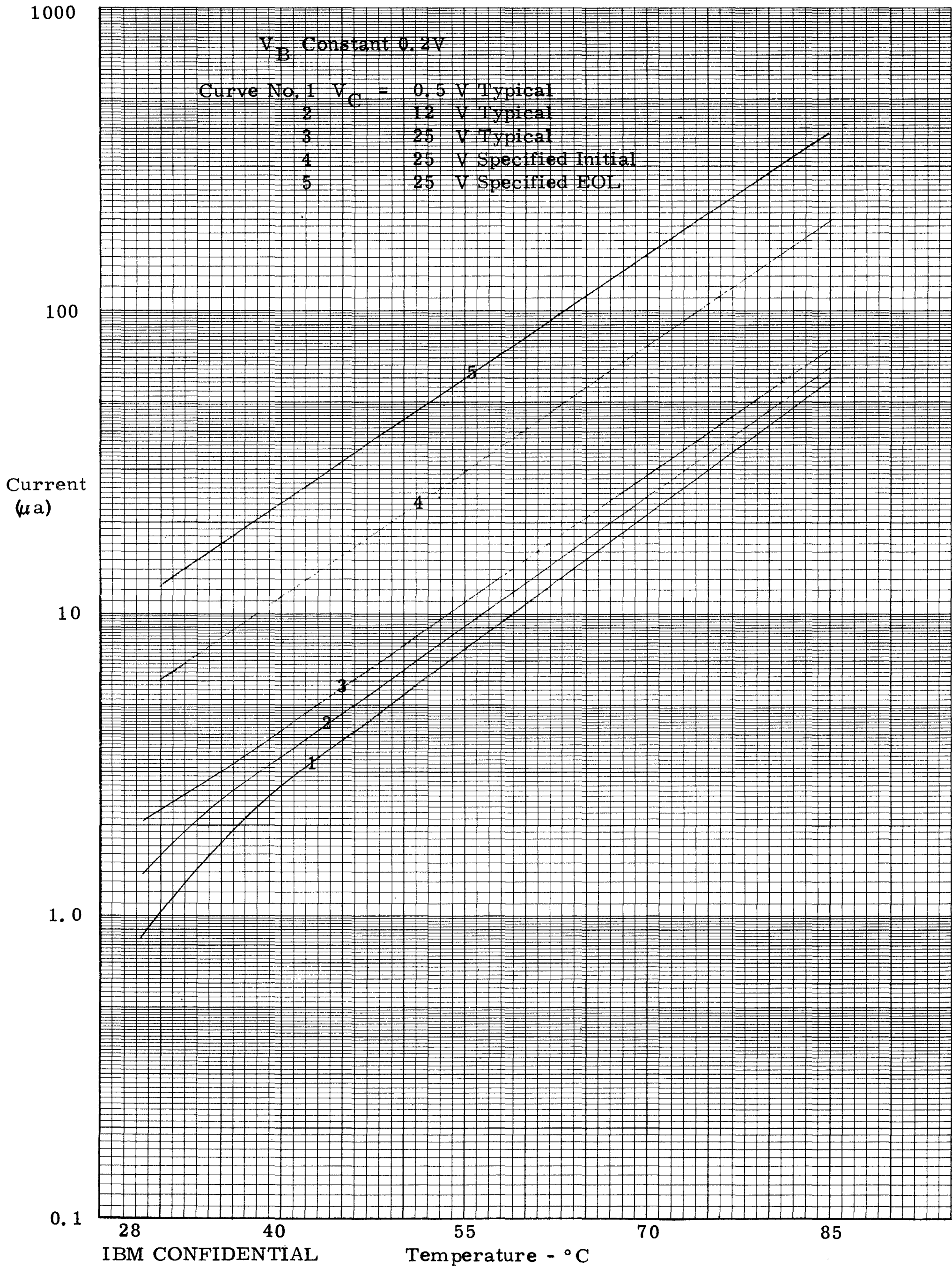

V_{CE} vs. I_B
TI - 033 Transistor @ 25°C
Curve No. 1 I_C = 7.5 ma Typical
2 7.5 ma Specified Initial
3 7.5 ma Specified EOL
4 15 ma Typical
5 25 ma Typical
6 50 ma Typical
7 50 ma Specified Initial
8 75 ma Typical
9 100 ma Typical
V_{CE} (volts)
10
1.0
0.1
0.01
1 2 3 4 5 6 7 8 9
0.1
1.0
10
I_B (ma)

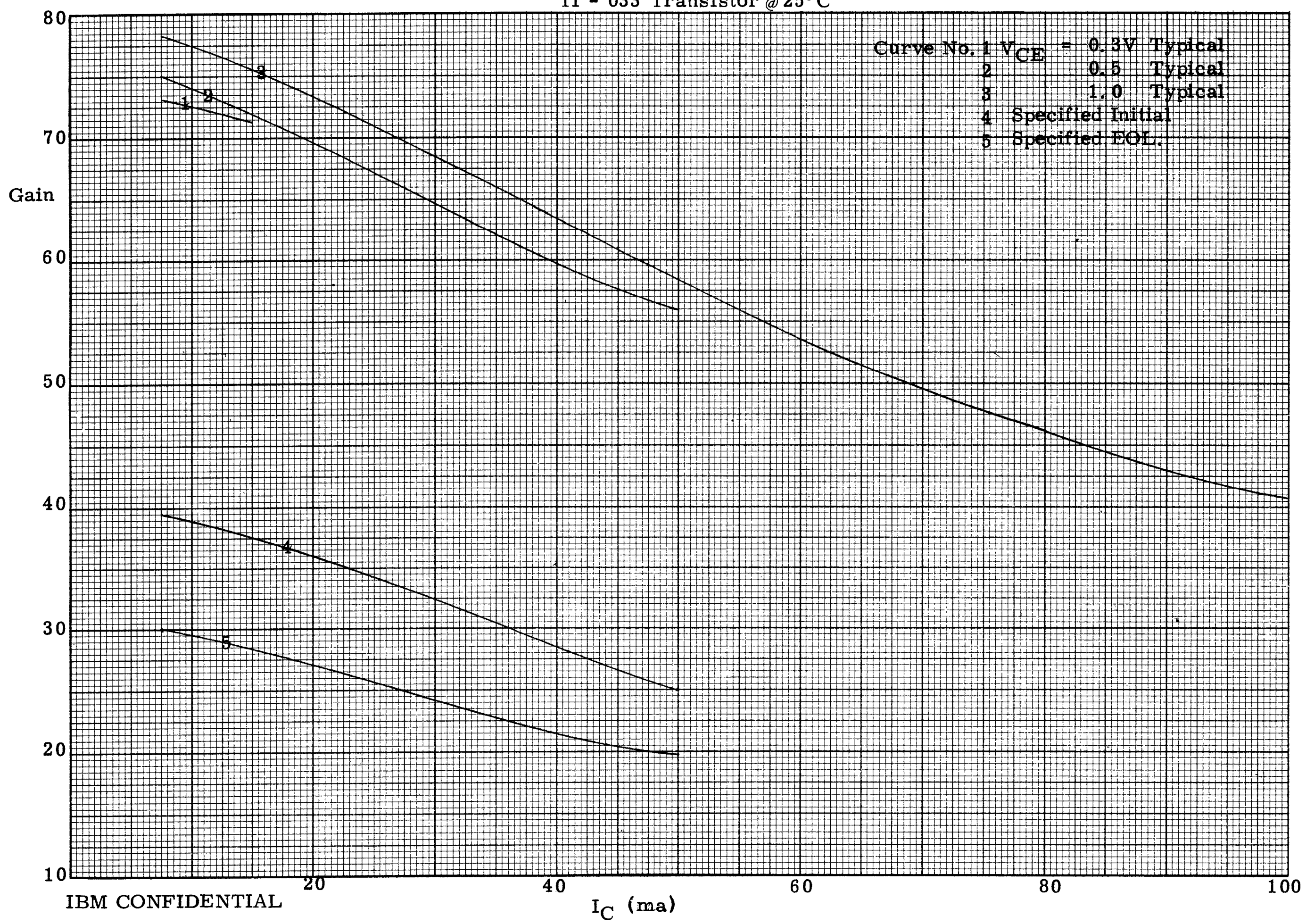

I_{BEO} * vs. Temperature
TI 033 Transistor
V_B Constant 0.2 V
Curve No. 1 V_C = 0.5 V Typical
2 12 Typical
3 25 Typical
4 6 Specified Initial
5 6 Specified EOL
1000
100
10
1.0
0.1
Current
(μa)
25
40
55
70
85
Temperature - °C
1
2
3
4
5



I_{CEO} * vs. Temperature
TI - 033 Transistor
V_B Constant 0.2V
Curve No. 1 V_C = 0.5 V Typical
2 12 V Typical
3 25 V Typical
4 25 V Specified Initial
5 25 V Specified EOL
1000
100
10
1.0
0.1
Current (μa)
28
40
55
70
85
Temperature - °C
1
2
3
4
5

h_{FE} vs. I_C

TI - 033 Transistor @ 25° C



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TI-033 TRANSISTOR

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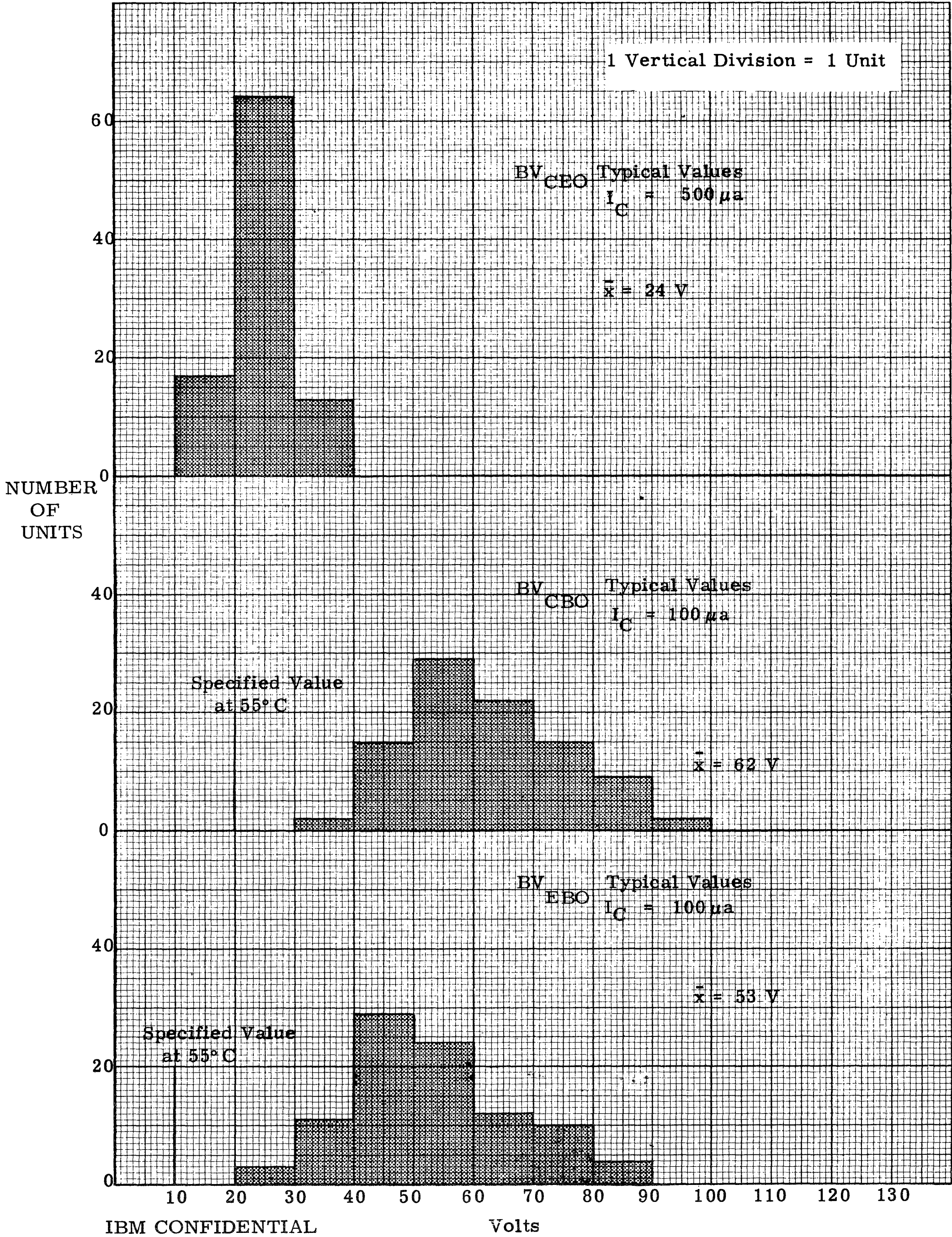
TI - 033 Transistor @ 25° C
1 Vertical Division = 1 Unit
BV_{CEO} Typical Values
I_C = 500 µa
x̄ = 24 V
BV_{CBO} Typical Values
I_C = 100 µa
Specified Value at 55° C
x̄ = 62 V
BV_{EBO} Typical Values
I_C = 100 µa
x̄ = 53 V
Specified Value at 55° C
NUMBER OF UNITS
0
20
40
60
10
20
30
40
50
60
70
80
90
100
110
120
130
Volts

IBM Division Standard

4-2-6010-0

TYPE 034 PT. NO. 535009 EC. 203601
DESCRIPTION Alloy Logic PNP

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	25 V	25 V
V_{EBO}	10 V	10 V
* I_C or I_E	70 ma	
POWER @ 55°C	80 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0. 25	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	-6		0. 2				55					26	52	ua
	-15		10				55					30	60	ua
I_{CEO}*	-25		0. 2				55					30	60	ua
h_{FE}		20		0.50			25	40						
		20		0. 69					29					
V_{CE}		20		0.50			25					0. 3		V
		20		0. 69									0. 3	V
V_{BE}		20		0. 69			25					0. 37		V
t_d, t_{ot} } t_{on}	-6						25	0. 1				1		us
t_s, t_{st} } t_{off}	-18		-18		-6		25	0. 4				1. 75		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 063 PT. NO. 344891 EC. 203348
DESCRIPTION Alloy Logic NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	20 V	15 V
V_{EBO}	20 V	16 V
I_C or I_E	50 ma	
POWER @ 55°C	100 mw	
T_{JCT}	75° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

TEST CONDITIONS								D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN		TYPICAL		MAX		
								INIT	EOL	INIT	EOL	INIT	EOL	
$f_{\alpha b}$	5					3	25	5						Mc
I_{CBO}	5						55					32	64	ua
I_{EBO}					5		55					32	64	ua
I_{BEO}*														
I_{CBO}*	5				0.2							32		ua
h_{FE}		7.5		0.19			25	39.5						
		7.5		0.267			25		28					
V_{CE}		7.5		0.19			25					0.2		V
		7.5		0.267			25						0.2	V
V_{BE}		7.5		0.19			25					0.3		V
t_d / t_{ot} } t_{on}	+6						25	0.1				1.0		us
t_s / t_{st} } t_{off}														
BV_{CBO}		0.02					25	20						V
BV_{EBO}						0.02	25	20						V
BV_{CEO}														

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TYPE 065 PT. NO. 526798 EC. 203350
DESCRIPTION Diffused Logic NPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	20 V	15 V
	V_{EBO}	2.8 V	2.5 V
*	I_C or I_E	8 ma	
	POWER @ 55°C	100 mw	
*	T_{JCT}	75° C	
	K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN		TYPICAL		MAX		
								INIT	EOL	INIT	EOL	INIT	EOL	
f αb	4					6	25	70						Mc
I_{CBO}														
I_{EBO}														
I_{BEO}*														
I_{CEO}*	6		-0.05				55					55	84	ua
h_{FE}		8		0.4			25	20						
V_{CE}		8		0.4			25					1.0		V
V_{BE}														
t_d, t_{ot} } t_{on}														
t_s, t_{st} } t_{off}														
BV_{CBO}		0.4					55	20	15					V
BV_{EBO}						0.04	55	2.8	2.5					V
BV_{CEO}														

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IBM Division Standard

4-2-6010-0

TYPE 066 PT. NO. 526881 EC. 203350
DESCRIPTION Diffused Logic NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	20 V	15 V
V_{EBO}	1.8 V	1.5 V
* I_C or I_E	8 ma	
POWER @ 55°C	100 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN		TYPICAL		MAX		
								INIT	EOL	INIT	EOL	INIT	EOL	
$f_{\alpha b}$	4					6	25	70						Mc
I_{CBO}*	+6				0.1		55					55	84	ma
I_{EBO}														
I_{BEO}*														
I_{CEO}*														
h_{FE}		8		0.4			25	20						
V_{CE}		8		0.4			25					1.0		V
V_{BE}														
t_d } t_{on}														
t_{ot} }														
t_s } t_{off}														
t_{st} }														
BV_{CBO}		0.4					55	20	15					V
BV_{EBO}						0.04	55	1.8	1.5					V
BV_{CEO}														

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TYPE 075 PT. NO. 318323 EC. 203348
DESCRIPTION Alloy Logic NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	16 V	16 V
V_{EBO}	6 V	6 V
* I_C or I_E	50 ma	
POWER @ 55°C	100 mw	
* T_{JCT}	75° C	
K - factor (Junction to Case)	0.2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
f ∝ b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	6		-0.2				55					36	72	ua
	10		6				55					45	90	ua
I_{CEO}*	16		-0.2				55					45	90	ua
h_{FE}		7.5		0.28			25	26.8						
		20		0.71			25	28.2						
		7.5		0.34			25		22					
V_{CE}		7.5		0.28			25					0.2		V
		20		0.71			25					0.2		V
		7.5		0.34			25						0.2	V
V_{BE}		7.5		0.34			25					0.3		V
		20		0.89			25					0.35		V
t_d, t_{ot} } t_{on}	6						25	0.1				1.2		us
t_s, t_{st} } t_{off}	12		12				25	0.3				1.2		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 077 PT. NO. 369067 EC. 203602
DESCRIPTION Thyratron PNPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	93 V	79 V
	V_{EBO}	13 V	13 V
*	I_C or I_E	200 ma	
	POWER @ 55°C		
*	T_{JCT}	75° C	
	K - factor (Junction to Case)		

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f ∝ b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	80		-13				55					0.5		ma
	66		-2				55					0.5	0.75	ma
I_{BE} TRIG	55						15					0.01		ma
	60						15						0.05	ma
h_{FE}														
V_{CE}		200					25					1		V
V_{BE}														
t_d, t_{ot} } t_{on}														
t_s, t_{st} } t_{off}														
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 078 PT. NO. 369068 EC. 203598
DESCRIPTION Thyratron PNPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	79 V	68 V
	V_{EBO}	15 V	15 V
*	I_C or I_E	200 ma	
	POWER @ 55°C		
*	T_{JCT}	75° C	
	K - factor (Junction to Case)		

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	64		-15				55					0.66		ma
	53		-1.5				55					0.66	1	ma
I_{BE} TRIG	35						25					0.15	0.30	ma
h_{FE}														
V_{CE}		200					25					1		V
V_{BE}														
t_d / t_{ot} } t_{on}														
t_s / t_{st} } t_{off}														
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 083 PT. NO. 318325 EC. 203348
DESCRIPTION Alloy Logic NPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	20 V	20 V
	V_{EBO}	10 V	10 V
*	I_C or I_E	50 ma	
	POWER @ 55°C	100 mw	
*	T_{JCT}	75° C	
	K - factor (Junction to Case)	0. 2	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
								MIN		TYPICAL		MAX		
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	INIT	EOL	INIT	EOL	INIT	EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	6		-0. 2				55					32	64	ua
	10		-10				55					36	72	ua
I_{CEO}*	20		-0. 2				55					36	76	ua
h_{FE}		7. 5		0. 19			25	39. 5						
		50		1. 25			25	40						
		7. 5		0. 25			25		30					
V_{CE}		7. 5		0. 19			25					0. 2		V
		50		1. 25			25					0. 3		V
		7. 5		0. 25			25						0. 2	V
V_{BE}		7. 5		0. 25			25					0. 3		V
		50		1. 7			25					0.45		V
t_d } t_{ot} } t_{on}	6						25	0. 1				0. 8		us
t_s } t_{st} } t_{off}	12		12				25	0. 3				1. 0		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 089 PT. NO. 369559 EC. 203105
DESCRIPTION Diffused Med. Power NPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	90 V	90 V
	V_{EBO}	3.5 V	3.5 V
*	I_C or I_E	600 ma	
	POWER @ 55°C	2.5 W	
*	T_{JCT}	85° C	
	K - factor (Junction to Case)	12	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f ∝ b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	50		-3.5				55					250	500	ua
I_{CEO}*	90		-0. 3				55					300	500	ua
h_{FE}														
V_{CE}														
V_{BE}														
t_d } t_{ot} } t_{on}	76		-6.				25					0. 15		us
t_s } t_{st} } t_{off}	77. 5		-5.				25					0. 08		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 091 PT. NO. 369561 EC. 203105
DESCRIPTION Diffused. Med. Power NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	90 V	90 V
V_{EBO}	3.5 V	3.5 V
* I_C or I_E	600 ma	
POWER @ 55°C	2 W	
* T_{JCT}	85° C	
K - factor (Junction to Case)	15	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	50		-3.5				55					250	500	ua
I_{CEO}*	90		-0.3				55					300	500	ua
h_{FE}		100		2.25			25	44.5						
		350		8.8			25	39.8						
		100		3.3			25		30.3					
V_{CE}		100		2.25			25					0.4		V
		350		8.8			25					0.6		V
		100		3.3			25						0.4	V
V_{BE}		100		3.3			25					0.4		V
		350		11.7			25	0.3				0.6		V
t_d, t_{ot} } t_{on}	30		-0.3				25					0.07		us
t_s, t_{st} } t_{off}	30		30				25					0.6		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 092 PT. NO 369562 EC 203105
DESCRIPTION Diffused Med. Power NPN

1. MAXIMUM RATINGS - DC

		INITIAL	END OF LIFE
	V_{CBO}	50 V	50 V
	V_{EBO}	3.5 V	3.5 V
*	I_C or I_E	600 ma	
	POWER @ 55°C	2 W	
*	T_{JCT}	85° C	
	K - factor (Junction to Case)	15	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
$f_{\alpha b}$														
I_{CBO}														
I_{EBO}														
I_{BEO}*	30		-3.5				55					500	1000	ua
I_{CEO}*	50		-0.3				55					500	1000	ua
h_{FE}		100		2.25			25	44.5						
		500		10			25	50						
		100		3.3			25		30.3					
V_{CE}		100		2.25			25					0.4		V
		500		10			25					0.6		V
		100		3.3			25						0.4	V
V_{BE}		100		3.3			25					0.4		V
		500		12.5			25					0.6		V
t_d, t_{ot} } t_{on}	30		0.3				25					0.09		us
t_s, t_{st} } t_{off}	30		30				25					0.75		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 093 PT. NO. 369560 EC. 203105
DESCRIPTION Diffused Med. Power NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	70 V	70 V
V_{EBO}	3.5 V	3.5 V
* I_C or I_E	600 ma	
POWER @ 55°C	2.5	
* T_{JCT}	85° C	
K - factor (Junction to Case)	12	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS								D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f α b														
I_{CBO}														
I_{EBO}														
I_{BEO}*	30		-3.5				55					250	500	ua
I_{CEO}*	70		-0.3				55					300	500	ua
h_{FE}														
V_{CE}														
V_{BE}														
t_d, t_{ot} } t_{on}	56		-6				25					0.15		us
t_s, t_{st} } t_{off}	57.5		-50				25					0.1		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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TYPE 094 PT. NO. 369081 EC. 203105
DESCRIPTION Diffused Med. Power NPN

1. MAXIMUM RATINGS - DC

	INITIAL	END OF LIFE
V_{CBO}	70 V	70 V
V_{EBO}	2 V	2 V
* I_C or I_E	600 ma	
POWER @ 55°C	1.2 W	
* T_{JCT}	85° C	
K - factor (Junction to Case)	25	

2. GENERAL CHARACTERISTICS

	TEST CONDITIONS							D C CHARACTERISTICS						UNITS
	V_C	I_C ma	V_B	I_B ma	V_E	I_E ma	Temp °C	MIN INIT	MIN EOL	TYPICAL INIT	TYPICAL EOL	MAX INIT	MAX EOL	
f αb														
I_{CBO}														
I_{EBO}														
I_{BEO}*	50		-2				55					250	375	ua
I_{CEO}*	70		-0.3				55					300	500	ua
h_{FE}		70		2.3			25	30.4						
		350		11.7			25	29.9						
		70		3.2			25		21.8					
V_{CE}		70		2.3			25					0.4		V
		350		11.7			25					0.6		V
		70		3.2			25						0.4	V
V_{BE}		70		3.2			25					0.4		V
		350		16			25					0.8		V
t_d, t_{ot} } t_{on}	30		-0.3				25					0.07		us
t_s, t_{st} } t_{off}	30		30				25					0.6		us
BV_{CBO}														
BV_{EBO}														
BV_{CEO}														

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NPN TRANSISTORS

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SECTION 5: GENERAL NOTES.

1. SCOPE

1.1 This specification sets forth requirements for NPN semi-conductor transistors in hermetically sealed cases. (Ref. Paragraph 4.12)

1.2 The words "component" and "transistor", shall be used hereinafter to indicate the product identified in paragraph 1.1 and described by this specification.

1.3 Transistors covered by this specification are intended to be used as high reliability components, with a useful life of the order of 20,000 hours of service when properly applied within their ratings in commercial business machines. The transistors are intended to be suitable for use in secondary circuits of equipment for which Underwriters Laboratories listing is required.

1.4 The transistors shall be suitable for storage at and between the ambient temperatures specified on the applicable IBM drawing.

2. GENERAL REQUIREMENTS AND CONSTRUCTION

2.1 APPLICABLE DRAWINGS AND SPECIFICATIONS. Components furnished under this specification shall comply with all requirements given herein and:

(a) On the applicable IBM drawing;

(b) In IBM Quality Specification No. 4015.

In case of conflict between the quality specification and this specification, except as pertaining to acceptance requirements, sampling plans, quality levels, grouping of tests and order of tests, this specification shall take precedence. In case of conflict between this specification and the draw-

ing, this specification shall take precedence unless the drawing specifically states that such requirements are modified or superseded by the requirements of the drawing.

2.2 APPLICABLE REQUIREMENTS AND TESTS. Components submitted or supplied in accordance with this specification shall be capable of meeting or passing any and all requirements or tests as follows:

Section 3: Electrical requirements and tests as specified on the applicable drawing.

Section 4: Any and all requirements or tests except those specifically designated by the applicable drawing as "Not Applicable".

2.3 ENGINEERING APPROVAL. IBM reserves the right to require that components supplied under this specification be a manufacturer's product previously approved by IBM Engineering. Such approval shall normally be given only after samples representative of the manufacturer's normal production have been examined and tested. Such approval shall not be construed to be a waiver of any requirements of this specification at any time. Engineering approval may be withdrawn or withheld if any of the following conditions exist:

(1) Performance of any test or inspection process reveals that the requirements of paragraph 2.4, "Changes in Construction" are not being met.

(2) Inspection of the manufacturer's facilities or records, in accordance with paragraphs 5.2 and 5.3, reveals conditions unsatisfactory to IBM.

(3) Long-time tests on the product or experience with the product, when properly applied within the ratings defined by the specification and part drawing, indicate that the product does not have the degree of reliability intended by this specification.

2.4 CHANGES IN CONSTRUCTION. If the manufacturer of a previously approved component desires at any time to change the material, the design, or processing, he shall submit a statement describing the proposed changes together with evidence to justify such changes. IBM reserves the right to require the manufacturer to submit samples incorporating the proposed changes for evaluation by IBM.

2.5 WORKMANSHIP. Transistors shall be processed in a careful and workmanlike manner. The manufacturer shall use good measurement and production techniques to insure the highest degree of product reliability and uniformity practicable under the present state of the art.

2.6 NO PROVISIONS or portion of this specification shall be construed to require the manufacturer to make any production or preshipment tests other than those normally performed during the manufacturing and packaging of the components described herein.

2.7 CONSTRUCTION.

2.7.1 The Transistor shall be enclosed in an hermetically sealed case. This shall form a container which is capable of protecting the transistor element under all test conditions specified herein. The active transistor element shall be completely enclosed by the case. (Ref. Paragraph 4.12)

2.7.2 The Case Material and sealing method shall be of such a nature that no loss of sealing effectiveness shall occur due to temperature variations or conditions of humidity as verified by the tests specified in paragraphs 4.4 and 4.5.

2.7.3 The Transistor shall be so constructed as to permit soldering to the leads without impairing any electrical characteristics, as verified by the Thermal Shock Test specified in paragraph 4.7. The wire leads shall be capable of withstanding the mechanical lead strength tests specified in paragraph 4.2.

2.8 MARKINGS.

2.8.1 The Transistor shall be permanently and legibly marked with its IBM type number, manufacturers identification, EIA Date code, and as specified by the applicable IBM drawing.

2.8.2 The Collector Lead shall be positively identified.

3. ELECTRICAL REQUIREMENTS AND TESTS

3.1 GENERAL.

3.1.1 Test Conditions. Unless otherwise specified, standard conditions for testing and making measurements are the following:

Barometric Pressure: 28 inches to 32 inches of mercury.

Relative Humidity: Less than 80%

Ambient Temperature as specified under "Applied Conditions" on the applicable IBM drawing + 2°C.

All voltages and current specified under "Applied Conditions" on the applicable IBM drawing shall be of at least ±2% accuracy.

All electrical components, other than transistors, shown in test circuits herein will have tolerances of ±1% unless otherwise specified.

3.1.2 When Test Conditions or measured quantities are referred to herein as "specified", it shall mean as specified on the applicable IBM drawing unless otherwise stated.

3.2 COLLECTOR CUT-OFF CURRENT, I_{CBO} :

With the emitter open circuited the specified reverse collector to base voltage V_C shall be applied. The collec-

tor current I_{CBO} shall be as specified.

3.3 REVERSE BIASED CUT-OFF CURRENTS:

3.3.1 Collector Cut-Off Current, I_{CBO*} : With the base common and the emitter and collector at the specified voltages the Collector Cut-Off Current I_{CBO*} shall be as specified.

3.3.2 Base Cut-Off Current, I_{BEO*} . With the emitter common and the base and collector at the specified voltages, the Base Cut-Off Current I_{BEO*} shall be as specified.

3.3.3 Collector Cut-Off Current, I_{CEO*}. With the emitter common and the base and collector at the specified voltages, the Collector Cut-Off Current I_{CEO*} shall be as specified.

3.4 EMITTER CUT-OFF CURRENT, I_{EBO}: With the collector open circuited the specified reverse emitter to base voltage (V_E) shall be applied. The emitter currents I_{EBO} shall be as specified.

3.5 COLLECTOR BREAKDOWN VOLTAGE, BV_{CBO}. With the emitter open circuited the specified reverse collector current I_C shall be applied. The collector voltage drop shall be as specified.

3.6 EMITTER BREAKDOWN VOLTAGE, BV_{EBO}. With the collector open circuited, the specified reverse emitter current I_E shall be applied. The emitter voltage drop shall be as specified.

3.7 PUNCH THROUGH VOLTAGE: V_{PT} With the specified reverse collector to base voltage (V_C) applied, the emitter to base voltage shall be as specified. The impedance of the emitter circuit must be equal to or greater than 1.0 megohm.

3.8 CURRENT RATIO, COMMON EMITTER, α_{FE}: When the specified values of base current and collector voltage are applied, the collector current shall be as specified.

3.9 COLLECTOR TO EMITTER SATURATION VOLTAGE, V_{CE} : With the specified values of collector current I_C and base current I_B applied in a common emitter configuration, the collector to emitter voltage shall be as specified.

3.10 BASE TO EMITTER VOLTAGE, V_{BE}: Using the circuit configurations specified in paragraph 3.9, the base to emitter voltage shall be as specified.

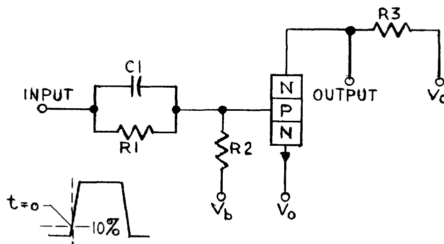
3.11 COMPUTED COMMON EMITTER CURRENT GAIN α_{FE*}: When the specified values of collector to base voltage V_C and emitter current I_E are applied, the total base current I_B shall be monitored. Under the same dissipation dondic

$$\alpha_{FE*} = \frac{I_E}{I_{CBO} + I_B}$$

Note: The sum of I_{CBO} and I_B is an algebraic sum.

3.12 EMITTER TO BASE VOLTAGE, V_{EB*} . Using the circuit configuration specified in paragraph 3.11 the emitter to base voltage shall be as specified.

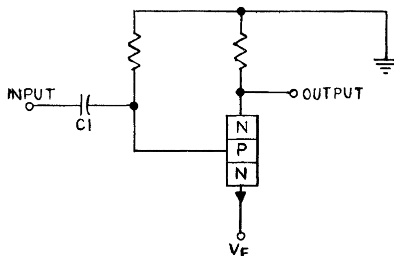
3.13 COMMON EMITTER TURN ON TIME, t_{ON}: The turn on time is defined as the time interval from t = 0 to t = T_r t = 0 is the 10% point of the input pulse . t = T_r is the point at which the output pulse (V_O) reaches the value specified. Turn on time measured in the circuit below, shall not exceed the value specified. The input pulse, R_1, R_2, R_3, C_1, V_c and V_b shall be as specified. V_E shall be ground potential unless otherwise specified. The input shall be a rectangular wave.



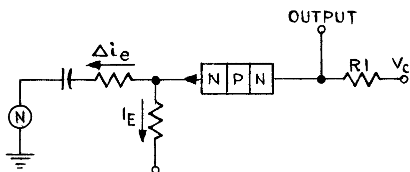
3.14 OUTPUT SHAPE AFTER TURN ON: For times greater than t = Tr, described in paragraph 3.13, the output must be a monotonically increasing function to the value of V_{ce} specified.

3.15 OUTPUT - CAPACITANCE, C_{ob}. The common collector to base capacitance shall be measured at the specified values of frequency, collector voltage, and emitter current. The collector (Output) capacitance shall be as specified on the applicable IBM drawing.

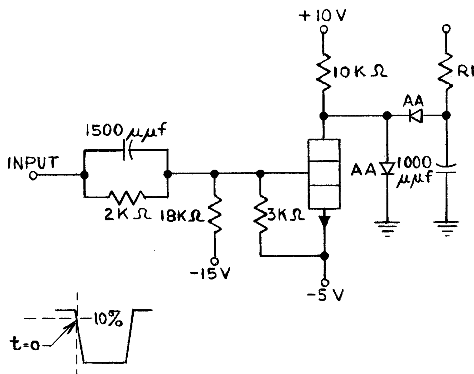
3.16 MINORITY CARRIER STORAGE, V_{st}: Minority carrier storage will be measured in the circuit below. The output pulse amplitude shall be as specified on the applicable IBM drawing. The input pulse voltage will vary between the two voltages specified in column titled "Input pulse-amplitude," The input pulse, R_1, R_2, C_1 and V_E are as specified.



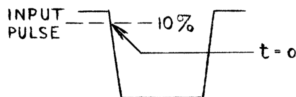
3.17 ALPHA CUT OFF FREQUENCY, f_C: Alpha cut off frequency is defined as the frequency at which the magnitude of the small signal (common base) current ratio $_{fb}$ has falled to 0.707 of its initial frequency value, and shall be measured in the circuit shown below. The initial frequency shall be 10% of the value of specified frequency cut off. V_C, I_E, Δi_e and R_1 are as specified. The measured alpha cut off frequency shall be greater than or equal to the value specified.



3.18 COMMON EMITTER TURN OFF DELAY, t_{OFF}: The turn off delay time is defined as the time interval from t = 0 to t = T_1. t = 0 is the 10% point of the fall time of the input pulse. T = T_1 is the 10% point of the change in output voltage. The delay time shall be measured in the circuit below and shall not exceed the value specified. The input pulse, and R_1 are as specified.



3.21 COMMON EMITTER TURN OFF TIME, T_{off}: The turn off time shall be measured using the circuit specified in paragraph 3.13. Turn off time is defined as the time interval from t = 0 to t = t_{off}. t = 0 is the 10% point of the input pulse. t_s t_{off} is the point at which the output pulse (V_o) reaches the value specified. The input pulse R_1, R_2, R_3, C_1, V_c and V_b shall be as specified. V_E shall be at ground potential unless otherwise specified. The input shall be a rectangular wave.



4. TESTS TO VERIFY SUITABILITY OF MATERIAL AND DESIGN

4.1 GENERAL.

4.1.1 Components to be subjected to the tests in this Section shall have been previously determined to have individually met all applicable requirements of Section 3.

4.1.2 Components subjected to any of the tests in Section 4 shall not be used in subsequent tests.

4.1.3 Unless Otherwise Specified under individual tests in this Section, a unit failing a particular test is defined as one which fails to meet any or all of the applicable requirements of paragraphs 3.2, 3.3, 3.4, 3.5, and 3.6 after completior of the test. A unit failing a particular test is defined as either a degradation failure or a catastrophic failure, depending on the amount of change in its applicable parameters.

4.1.4 A Component exhibiting a degradation failure is defined as one whose particular parameter under consideration changes from its initial value by an amount greater than either of the following, whichever is larger:

1. ±20% of its initial value if a maximum limit is specified, -20% of its initial value, if a minimum limit is for that parameter.

2. ±20% of the specified maximum initial limit, -20% of the specified minimum initial limit.

If the specified limit has both a maximum and a minimum value, the allowable change shall be ±20% of its initial value. (See Paragraph 4.8.4 for Life Test Criteria)

4.1.5 A Component considered a catastrophic failure is defined as one whose particular parameter under consideration has a final falling outside the specified 1000 hours limit(s).

4.2 LEAD STRENGTH TESTS.

4.2.1 The Transistors to be subjected to the lead strength tests shall be divided into two groups. Each group shall be subjected to one sub-test only as follows:

4.2.2 With One Axial Lead of the Transistor clamped, a force of 1 pound shall be applied without shock, at right angles to the axis of the transistor at the farthest end of the other leads in turn. A broken lead and/ or evidence of loss of seal shall be considered a failure.

4.2.3 Bend Test. Each transistor lead shall be subjected to 3 separate 90 degree bends at the base of the transistor. A broken lead and/ or evidence of loss of seal shall be considered a failure.

4.3 VIBRATION.

4.3.1 Transistors to be subjected to the vibration test shall be mounted rigidly on a vibration platform by a suitable clamp.

4.3.2 The Transistors shall be subjected to a simple harmonic motion having a total displacement of .062 inches with the frequency of motion being varied uniformly between the limits of 10 to 55 cycles per second. The entire frequency range from 10 to 55 cycles shall be traversed in not less than 1 minute.

4.3.3 The Vibrating Motions shall be applied for a period of 20 minutes along each of the three mutually perpendicular axes of the transistors.

4.3.4 A Component exhibiting either of the following shall be considered a failure:

(a) Evidence of mechanical damage, loosening of the leads or loosening of the element within the case.

(b) Electrical characteristics out of limits as outlined under paragraph 4.1.3.

4.4 TEMPERATURE SHOCK TEST. The transistors to be tested shall be subjected to five sucessive temperature cycles each of which shall be as follows:

Step	Temperature	Duration
1	Room Ambient	30 minutes (max)
2	-18° C	15 minutes (min)
3	Room Ambient	30 minutes (max)
4	As specified in para. 4.8.2	15 minutes (min)

The test may be started at any step in the cycle.

4.5 TEMPERATURE AND HUMIDITY TEST. Components to be tested shall be subjected to the following cycle:

Step	Temp. (° C)	Rel. Hum. %	Time(hrs)
Start	25° C $^{+10}_{-2}$	Existing Rel. Hum.	-------
1. Raise to	55±3	90-95	2.5 max.
2. Maintain at	55±3	90-95	3.0
3. Lower to	25$^{+10}_{-2}$	90-95	2.5
4. Maintain at	25 $^{+10}_{-2}$	90-95	0.5
5. Raise to	55±3	90-95	2.5 max.
6. Maintain at	55±3	90-95	3.0
7. Lower to	25$^{+10}_{-2}$	90-95	2.5 max.
8. Maintain at	25 $^{+10}_{-2}$	90-95	remainder of 24 hr. period.

At the completion of step 8, the cycle shall be recommenced at step 1. Four successive cycles (step 1 through 8) shall be performed.

4.6 DYNAMIC TEST.

4.6.1 Conditions of Test. A dynamic display of the voltage-current characteristics of the transistor shall be used for all dynamic tests. The test voltage shall be a continuous, half rectified 60 cps sine wave. Sensing resistor shall be of sufficient magnitude of sense specified cut off currents.

The peak reverse voltage applied across each junction shall be the value where the initiation of breakdown is observed.

Breakdown is that phenomenon occurring in a reverse biased junction, the initiation of which is observed as a transition from the region of high dynamic resistance to a region of substantially lower dynamic resistance for increasing magnitude of reverse current. In certain device types, permanent changes in the characteristics have been observed when the breakdown voltages are exceeded independent of power dissipation. In these cases the maximum instantaneous current must be limited to some value less than that which causes irreversable changes to occur in the characteristic.

4.6.2 The Dynamic Display shall exhibit little or no evidence of instabilities such as drift, hystersis, creep, flutter, etc.

4.7 THERMAL SHOCK TEST. Each lead of each transistor to be tested shall be dipped to a point 3/ 8 inch from the body of the transistor into a pot of molten solder having a temperature of 260 ± 5° C and shall remain there for approximately 3 seconds.

4.8 LIFE TEST.

4.8.1 Power Dissipation Life Test. Each transistor to be tested shall continuously dissipate in a common base configuration the power dissipation and collector current specified, for 1000 hours (without a heat sink unless otherwise specified) at the temperature specified.

4.8.2 Storage Life Test. The transistors to be tested shall be stored at the temperature specified for one thousand hours.

4.8.3 Life Test, Cut Off Condition. Each transistor to be tested shall be placed in a common emitter configuration at the specified values of Collector Voltage (V_c) and Base voltage (V_b) for 1000 hours without a heat sink,(unless otherwise specified) at the temperature specified.

4.8.4 Failure of a Transistor on life test shall be determined by the criteria stated in paragraphs 4.1.3, 4.1.4, and 4.1.5, except that the initial value referred to shall be the values measured at the 250 hour point of the 1000 hour life test. These measured values shall be taken for all parameters for which 1000 hour limits are specified on the applicable IBM drawing.

4.9 IMPACT SHOCK TEST.

4.9.1 Transistors to be subjected to the impact shock test shall be securely mounted on a rigid surface.

4.9.2 The Transistors shall be subjected to 6 blows of 2.5 x 10 - 3 LB-Sec of impulsive force to the side of the case.

4.9.3 During the Test the forward voltage vs. current characteristic of both junctions, shall be observed concurrently.

4.9.4 A Transistor failing the impact shock test is defined as one exhibiting a 1 ohm change in its forward voltage vs. current characteristics.

4.10 THERMAL RESISTANCE.

4.10.1 Thermal Resistance (R_T) shall be computed from the equation:

$$R_T = \frac{T_j - T_a}{Pav}$$

where:

T_j = specified junction temperature in °C.

T_a = ambient temperature in °C.

Pav = average power dissipation.

Pav and T_a shall be determined according to paragraph 4.10.3 or 4.10.4 whichever is specified.

4.10.2 With Each Transistor to be tested maintained at an ambient temperature equal to T_j, the collector cut-off current (I_{CBO}) shall be measured and recorded. All measurements of I_{CBO} shall be made with the specified reverse voltage (V_c) applied between the collector and base leads.

4.10.3 Method I: With the entire transistor case maintained at the specified value of T_a, the power dissipation shall be adjusted until I_{CBO} equals the value obtained in paragraph 4.10.2. In the equation above, set Pav equal to the adjusted power dissipation, and set T_a equal to the specified value.

4.10.4 Method II: T_a shall be monitored at a specified point on the transistor case while power dissipation is adjusted until I_{CBO} equals the value obtained in paragraph 4.10.2.

In the equation of paragraph 4.10.1 set Pav equal to the adjusted power dissipation, and set T_a equal to the monitored value obtained when I_{CBO} equals it specified value.

4.10.5 A Component failing the Thermal Resistance test is defined as one for which the computed value of R_T is greater than the specified value.

4.11 VISUAL EXAMINATION.

4.11.1 The Body Dimensions and lead diameter or terminal dimensions shall be as specified on the applicable IBM drawing.

4.11.2 Markings shall be as specified by paragraph 2.8.

4.11.3 Lead Length and lead or terminal construction shall be as specified on the applicable IBM drawing and by paragraph 2.7 3 Workmanship and/ or appearance shall be or must seem to be as required by paragraph 2.5.

4.12 Hermetic Sealing or Transistor Cases.

4.12.1 The Transistor shall meet the Hermetic Seal Requirements outlined in Engineering Specification No. 895874.

5. GENERAL NOTES

5.1 IBM reserves the right to subject transistors submitted or supplied in accordance with this specification to any internal or external visual inspection processes in order to verify that the electrical and mechanical properties of the transistors are consistent with their ratings and the requirements of this specification.

5.2 The manufacturer shall, on request, permit access to his manufacturing facilities and such information as may be necessary to reasonable satisfy IBM that the manufacturer is complying with the provisions and intention of this specification.

5.3 No provisions or portions of this specification shall be interpreted to mean that the manufacturer shall be required to reveal any proprietary information.

PNP TRANSISTORS

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SECTION 5: GENERAL NOTES

1. SCOPE

1.1 This specification sets forth requirements for PNP semi-conductor transistors in hermetically sealed cases. (Ref. Paragraph 4.12)

1.2 The words, "component" and "transistor", shall be used hereinafter to indicate the product identified in paragraph 1.1 and described by this specification.

1.3 Transistors covered by this specification are intended to be used as high reliability components, with a useful life of the order of 20,000 hours of service when properly applied within their ratings in commercial business machines. The transistors are intended to be suitable for use in secondary circuits of equipment for which Underwriters Laboratories listing is required.

1.4 The transistors shall be suitable for storage at and between the ambient temperatures specified on the applicable IBM drawing.

2. GENERAL REQUIREMENTS AND CONSTRUCTION

2.1 APPLICABLE DRAWINGS and SPECIFICATIONS. Components furnished under this specification shall comply with all requirements given herein and:

(a) On the applicable IBM drawings;

(b) In IBM Quality Specification No. 4014

In case of conflict between the quality specification and this specification, except as pertaining to acceptance requirements, sampling plans, quality levels, grouping of tests and order of tests, this specification shall take precedence. In case of conflict between this specification and the drawing, this specification shall take precedence unless the drawing

specifically states that such requirements are modified or superseded by the requirements of the drawing.

2.2 APPLICABLE REQUIREMENTS AND TESTS. Components submitted or supplied in accordance with this specification shall be capable of meeting or passing any and all requirements or tests as follows:

Section 3:

Electrical requirements and tests as designated on the drawing.

Section 4:

Any and all requirements or tests, except those specifically designated on the drawing as "Not Applicable".

2.3 ENGINEERING APPROVAL. IBM reserves the right to require that components supplied under this specification be a manufacturer's product previously approved by IBM Engineering. Such approval shall normally be given only after samples representative of the manufacturer's normal production have been examined and tested. Such approval shall not be construed to be a waiver of any requirements of this specification at any time. Engineering approval may be withdrawn or withheld if any of the following conditions exist:

(1) Performance of any test or inspection process reveals that the requirements of paragraph 2.4 "Changes in Construction", are not being met.

(2) Inspection of the manufacturer's facilities or records, in accordance with paragraphs 5.2 and 5.3, reveals conditions unsatisfactory to IBM.

(3) Long time tests on the product or experience with the product, when properly applied within the ratings defined by the specification and part drawing, indicate that the product does not have the degree of reliability intended by this specification.

2.4 CHANGES IN CONSTRUCTION. If the manufacturer of a previously approved component desires at any time to change the material, the design, or processing, he shall submit a statement describing the proposed changes together with evidence to justify such changes. IBM reserves the right to require the manufacturer to submit samples incorporating the proposed changes for evaluation by IBM.

2.5 WORKMANSHIP. Transistors shall be processed in a careful and workmanlike manner. The manufacturer shall use good measurement and production techniques to insure the highest degree of product reliability and uniformity practicable under the present state of the art.

2.6 NO PROVISIONS or portion of this specification shall be construed to require the manufacturer to make any production or preshipment tests other than those normally performed during the manufacturing and packaging of the components herein.

2.7 CONSTRUCTION.

2.7.1 The Transistor shall be enclosed in an hermetically sealed case. This shall form a container which is capable of protecting the transistor element under all test conditions specified herein. The active transistor element shall be completely enclosed by the case. (Ref. Paragraph 4.12)

2.7.2 The Case Material and Sealing Method shall be of such a nature that no loss of sealing effectiveness shall occur due to temperature variations or conditions of humidity as verified by the tests specified in paragraphs 4.4 and 4.5

2.7.3 The Transistor shall be so constructed as to permit soldering to the leads without impairing any electrical characteristics, as verified by the Thermal Shock Test specified in paragraph 4.7. The wire leads shall be capable of withstanding the lead strength tests specified in paragraph 4.2.

2.8 MARKINGS.

2.8.1 The Transistor shall be permanently and legibly marked with its IBM type number, manufacturers identification, EIA date code, and as specified by the applicable IBM drawing.

2.8.2 The Collector lead shall be positively identified.

3. ELECTRICAL REQUIREMENTS AND TESTS.

3.1 General.

3.1.1 Test Conditions. Unless otherwise specified, standard conditions for testing and making measurements are the following:

Barometric Pressure : 28 inches to 32 inches of mercury

Relative Humidity: Less than 80%

Ambient Temperatures as specified under "Applied Conditions" on the applicable IBM drawing ±2° C.

All voltages and current specified under "Applied Conditions" on the applicable IBM drawing shall be of at least ±2% accuracy.

All electrical components, other than transistors, shown in test circuits herein will have tolerances of ±1% unless otherwise specified.

3.1.2 When Test Conditions or measured quantities are referred to herein as "specified", it shall mean as specified on the applicable IBM drawing unless otherwise stated.

3.2 COLLECTOR CUT-OFF CURRENT, I_{CBO}

With the emitter open circuited the specified reverse collec-

tor to base voltage V_C shall be applied. The collector current I_{CBO} shall be as specified.

3.3 REVERSE BIASED CUT-OFF CURRENTS:

3.3.1 Collector Cut-Off Current, I_{CBO*}: With the base common and the emitter and collector at the specified voltages, the collector Cut-Off Current, I_{CBO*} shall be as specified.

3.3.2 Base Cut-Off Current, I_{BEO*}: With the emitter common and the base and collector at the specified voltages, the base Cut-Off Current, I_{BEO*} shall be as specified.

3.3.3 Collector Cut-Off Current, I_{CEO*}: With the emitter common and the base and collector at the specified voltages, the Collector Cut-Off Current I_{CEO*} shall be as specified.

3.4 EMITTER CUT-OFF CURRENT, I_{EBO}: With the collector open circuited the specified reverse emitter to base voltage (V_E) shall be applied. The emitter current I_{EBO} shall be as specified.

3.5 COLLECTOR BREAKDOWN VOLTAGE, BV_{CBO}: With the emitter open circuited the specified reverse collector current (I_C), shall be applied. The collector to base voltage drop shall be as specified.

3.6 EMITTER BREAKDOWN VOLTAGE, BV_{EBO}: With the collector open circuited, the specified reverse emitter current (I_E), shall be applied. The emitter to base voltage drop shall be as specified.

3.7 PUNCH THROUGH VOLTAGE, V_{PT}: With the specified reverse collector to base voltage (V_C) applied, the emitter to base voltage shall be as specified. The impedance of the emitter circuit must be equal to or greater than 1.0 megohm.

3.8 CURRENT RATIO, COMMON EMITTER, $_{FE}$: When the specified values of base current (I_b) and reverse collector voltage (V_c) are applied, the collector current shall be as specified.

3.9 COLLECTOR TO EMITTER SATURATION VOLTAGE, V_{CE}: With the specified values of collector current I_C and base current I_B applied in a common emitter configuration the collector to emitter voltage shall be as specified.

3.10 BASE TO EMITTER VOLTAGE, (V_{BE}). Using the circuit configuration specified in paragraph 3.9, the base to emitter voltage shall be as specified.

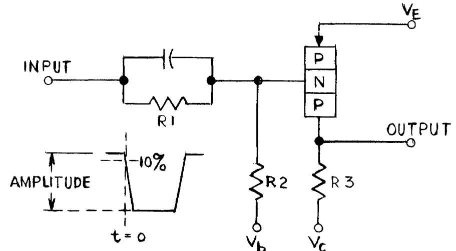
3.11 COMPUTED COMMON EMITTER CURRENT GAIN α_{FE*}: When the specified values of collector to base voltage V_C and emitter current (I_E) are applied, the total base current (I_B) shall be monitored. Under the same dissipation conditions, the collector cut-off current (I_{CBO}) shall be monitored. The computed common emitter current gain shall be as specified.

$$\alpha_{FE*} = \frac{I_E}{I_{CBO} + I_B}$$

NOTE: The sum of I_{CBO} and I_B is an algebraic sum.

3.12 EMITTER TO BASE VOLTAGE, V_{EB*}: Using the circuit configuration specified in paragraph 3.11 the emitter to base voltage shall be as specified.

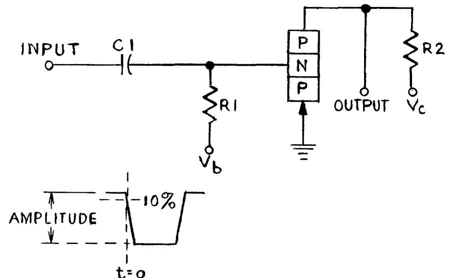
3.13 COMMON EMITTER TURN ON TIME, t_{ON}: The turn on time is defined as the time interval from t = 0 to t = Tr. t = 0 is the 10% point of the input pulse. t = Tr is the point at which the output pulse (V_o) reaches the value specified. Turn on time measured in the circuit below, shall not exceed the value specified. The input pulse, R_1, R_2, R_3, C_1, V_c and V_1 shall be as specified. V_E shall be at ground potential unless otherwise specified. The input shall be a rectangular wave.



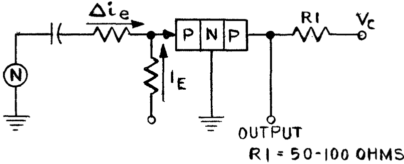
3.14 OUTPUT SHAPE AFTER TURN ON. For times greater than t = Tr, described in paragraph 3.13, the output must be a monotonically increasing function to the value of V_{ce} specified, for one cycle of input waveform.

3.15 OUTPUT CAPACITANCE, C_{OB}: The collector to base capacitance shall be measured at the specified values of frequency (f), collector voltage (V_C), and emitter current (I_E). The collector (Output) capacitance shall be as specified on the applicable IBM drawing.

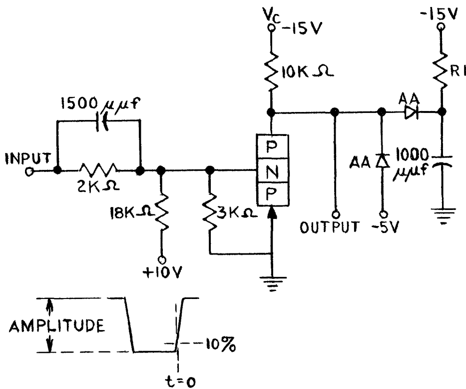
3.16 MINORITY CARRIER STORAGE, V_{st}: Minority carrier storage shall be measured in the circuit below. The output pulse shall be as specified on the applicable IBM drawing. The input pulse R_1, R_2, C_1, V_c and V_b are as specified.



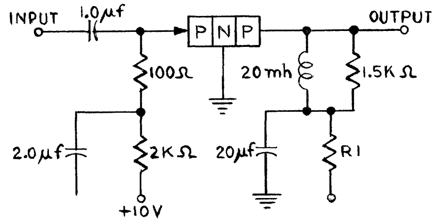
3.17 ALPHA CUT OFF FREQUENCY, $f\alpha C$: Alpha cut off frequency is defined as the frequency at which the magnitude of the small signal (common base) current, ratio . (α_{fb}) has fallen to 0.707 of its initial frequency value, and shall be measured in the circuit shown below. The initial frequency shall be 10% of the value of specified frequency cut off. V_C, I_E, Δi_e and R_1 are as specified. The measured alpha cut off frequency shall be greater than or equal to the value specified.



3.18 COMMON EMITTER TURN OFF DELAY, t_{off}: The turn off delay time is defined as the time interval from t = 0 to t = T_1. t = 0 is the 10% point of the fall time of the input pulse. t = T_1 is the 10% point of the change in output voltage. The delay time shall be measured in the circuit below and shall not exceed the value specified. The input pulse, and R_1 are as specified.



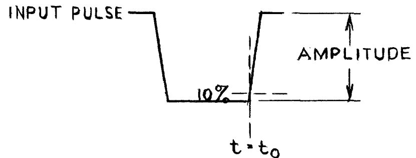
3.19 COMMON BASE SENSE AMPLIFIER. The time interval from 10% to 90% of the output rise time and the amplitude of the output measured in the circuit below shall be within specifications. The input shall be as specified on the applicable IBM drawing.



R_L = Inductor Resistance = 100 ohms maximum

$R_1 + R_L$ = 300 ±5% ohms.

3.21 COMMON EMITTER TURN OFF TIME, T_{OFF}: The turn off time shall be measured using the circuit descrived in paragraph 3.13. Turn off time is defined as the time interval from t = 0 to t = t_{off}. t = 0 is the 10% point of the input pulse. t = t_{off} is the point at which the outpulse (V_o) reaches the value specified. The input pulse R_1, R_2, R_3, C_1, V_C and V_b shall be as specified. V_E shall be at ground potential unless otherwise specified. The input shall be a rectangular wave.



4. TESTS TO VERIFY SUITABILITY OF MATERIAL AND DESIGN

4.1 GENERAL.

4.1.1 Components to be subjected to the tests in this Section shall have been previously determined to have individually met all applicable requirements of Section 3.

4.1.2 Components subjected to any of the tests in Section 4 shall not be used in subsequent tests.

4.1.3 Unless Otherwise Specified under individual tests in this section, a unit failing a particular test is defined as one which fails to meet any or all of the requirements of paragraphs 3.2, 3.3, 3.4, 3.5, and 3.6 after completion of the test. A unit failing a particular test is defined as either a degradation failure (see paragraph 4.1.4) or a catastrophic failure (paragraph 4.1.5), depending on the amount of change in its applicable parameters.

4.1.4 A Component exhibiting a degradation failure is defined as one whose particular parameter under consideration changes from its initial value by an amount greater than either of the following, whichever is larger.

(1) ±20% of its initial value if a maximum limit is specified, -20% of its initial value if a minimum limit is specified.

(2) ±20% of the specified maximum initial limit, -20% of the specified minimum initial limit.

If the specified limit has both a maximum and a minimum value, the allowable change shall be ±20% of its initial value. (See paragraph 4.8.4 for Life Test Criteria)

4.1.5 A Component considered a catastrophic failure is defined as one whose particular parameter under consideration has a final value falling outside the specified 1000 hour limit(s).

4.2 LEAD STRENGTH TESTS.

4.2.1 The Transistors to be subjected to the lead strength tests shall be divided into two groups. Each group shall be subjected to one sub-test only as follows:

4.2.2 With One Axial Lead of the transistor clamped, a force of 1 pound shall be applied without shock, at right angles to the axis of the transistor at the farthest end of the other leads in turn. A broken lead and/or evidence of loss of seal shall be considered a failure.

4.2.3 Bend Test. Each transistor lead shall be subjected to 3 separate 90 degree bends at the base of the transistor. A broken lead and/or evidence of loss of seal shall be considered a failure.

4.3 VIBRATION.

4.3.1 Transistors to be subjected to the vibration test shall be mounted rigidly on a vibration platform by a suitable clamp.

4.3.2 The Transistors shall be subjected to a simple harmonic motion having a total displacement of .062 inches with the frequency of motion being varied uniformly between the limits of 10 to 55 cycles per second. The entire frequency range from 10 to 55 cycles shall be traversed in not less than 1 minute.

4.3.3 The Vibrating Motions shall be applied for a period of 20 minutes along each of the three mutually perpendicular axes of the transistors.

4.3.4 A Component exhibiting either of the following shall be considered a failure:

(a) Evidence of mechanical damage, loosening of the leads or loosening of the element within the case.

(b) Electrical characteristics out of limits as outlined under paragraph 4.1.3.

4.4 TEMPERATURE SHOCK TEST. The transistors to be tested shall be subjected to five successive temperature cycles each of which shall be as follows:

Step	Temperature	Duration
1	Room Ambient	30 minutes (max.)
2	-18°C	15 minutes (min.)
3	Room Ambient	30 minutes (max.)
4	As specified in para. 4.8.2	15 minutes (min.)

The test may be started at any step in the cycle.

4.5 TEMPERATURE AND HUMIDITY TEST. Components to be tested shall be subjected to the following cycle:

Step	Temp(°C)	Re. Hum. %	Time(hrs)
Start	$25°C^{+10}_{-2}$	---	---
1 Raise to	55 ± 3	90-95	2.5 (max.)
2 Maintain at	55 ± 3	90-95	3.0
3 Lower at	25^{+10}_{-2}	90-95	2.5
4 Maintain at	25^{+10}_{-2}	90-95	0.5
5 Raise to	55 ± 3	90-95	2.5 (max.)
6 Maintain at	55 ± 3	90-95	3.0
7 Lower at	25^{+10}_{-2}	90-95	2.5 (max.)
8 Maintain at	25^{+10}_{-2}	90-95	remainder of 24 hour period.

At the completion of step 8, the cycles shall be recommenced at step 1. Four successive cycles (step 1 through 8) shall be performed.

4.6 DYNAMIC TEST.

4.6.1 Conditions of Test: A dynamic display of the voltage current characteristics of the transistor shall be used for all dynamic tests. The test voltage shall be a continuous half rectified 60 cps sine wave. Sensing resistor shall be of sufficient magnitude to sense specified cut off currents. The peak reverse voltage applied across each junction shall be the value where the initation of breakdown is observed.

Breakdown is that phenomenon occurring in a reverse biased junction, the initiation of which is observed as a transition from the region of high dynamic resistance to a region of substantially lower dynamic resistance for increasing magnitude of reverse current. In certain device types, permanent changes in the characteristics have been observed when the breakdown voltages are exceeded independent of power dissipation. In these cases the maximum instanteous current must be limited to some value less than that which causes irreversable changes to occur in the characteristic.

4.6.2 The Dynamic Display shall exhibit little or no evidence of instabilities such as drift, hysteresis, creep, flutter.

4.7 THERMAL SHOCK TEST. Each lead of each transistor tested shall be dipped to a point 3/8 inch from the body of the transistor into a pot of molten solder having a temperature of 260 ± 5°C and shall remain there for approximately 3 seconds.

4.8 LIFE TEST.

4.8.1 Power Dissipation Life Test. Each transistor to be tested shall continuously dissipate in a common base configuration the power dissipation and collector current specified, for 1000 hours (without a heat sink unless otherwise specified) at the temperature specified.

4.8.2 Storage Life Test: The transistors to be tested shall be stored at the temperature specified for one thousand hours.

4.8.3 Life Test, Cut Off Condition. Each transistor to be tested shall be placed inaa common emitter configuration at the specified values of collector voltage (V_c) and base voltage (V_B) for 1000 hours without a heat sink, (unless otherwise specified) at the temperature specified.

4.8.4 Failure of a Transistor on life test shall be determined by the criteria stated in paragraphs 4.1 3, 4.1.4, and 4.1.5, except that the initial value referred to shall be the values measured at the 250 hour point of the 1000 hour life test. These measured values shall be taken for all parameters for which 1000 hour limits are specified on the applicable IBM drawing.

4.9 IMPACT SHOCK TEST.

4.9.1 Transistor to be subjected to the impact shock test shall be securely mounted on a rigid surface.

4.9.2 The Transistor shall be subjected to 6 blows of 2.5 X 10-3 LB-Sec. of impulsive force to the side of the case.

4.9.3 During the Test the forward voltage vs. current characteristics of both junctions, shall be observed concurrently.

4.9.4 A Transistor failing the impact shock test is defined as one exhibiting a 1 ohm change in its forward voltage vs. current characteristics.

4.10 THERMAL RESISTANCE.

4.10.1 Thermal Resistance (R_T) shall be computed from the equation:

$$R_T = \frac{T_j - T_a}{Pav}$$

where:

T_j = specified junction temperature in °C.

T_a = ambient temperature in °C.

Pav = average power dissipation.

Pav and T_a shall be determined according to paragraph 4.10.3 or 4.10.4, whichever is specified.

4.10.2 With Each Transistor to be tested maintained at an ambient temperature equal to T_j, the collector cut-off current (I_{CBO}) shall be measured and recorded. All measurements of I_{CBO} shall be made with the specified reverse voltage (V_c) applied between the collector and base leads.

4.10.3 Method I: With the entire transistor case maintained at the specified value of T_a, the power dissipation shall be adjusted until I_{CBO} equals the value obtained in paragraph 4.10.2. In the equation above, set P_{av} equal to the adjusted power dissipation, and set T_a equal to the specified value.

4.10.4 Method II: T_a shall be monitored at a specified point on the transistor case while the power dissipation is adjusted until I_{CBO} equals the value obtained in paragraph 4.10.2. In the equation of paragraph 4.10.1 set P_{av} equal to the adjusted power dissipation and set T_a equal to monitored value obtained when I_{CBO} equals its specified value.

4.10.5 A Component failing the Thermal Resistance test is defined as one for which the computed value of R_T is greater than the specified value.

4.11 VISUAL EXAMINATION.

4.11.1 The Body Dimensions and Lead Diameter or terminal dimensions shall be as specified on the applicable IBM drawing.

4.11.2 Markings shall be as specified by paragraph 2.8.

4.11.3 Lead Length and Lead or terminal construction shall be as specified on the applicable IBM drawing and by paragraph 2.7.3. Workmanship and/or appearance shall be or must seem to be as required by paragraph 2.5.

4.12 HERMETIC SEALING OF TRANSISTOR CASES.

4.12.1 The Transistor shall meet the hermetic seal requirements outlined in Engineering Specification No. 895874.

5. GENERAL NOTES.

5.1 IBM reserves the right to subject transistors submitted or supplied in accordance with this specification to any internal or external visual inspection processes in order to verify that the electrical and mechanical properties of the transistors are consistent with their ratings and the requirements of this specification.

5.2 The manufacturer shall, on request, permit access to his manufacturing facilities and such information as may be necessary to reasonably satisfy IBM that the manufacturer is complying with the provisions and intention of this specification.

5.3 No provisions or portions of this specification shall be interpreted to mean that the manufacturer shall be required to reveal any proprietary information or any information not directly related to the procurement of components under this specification.

2.2.5.3 Criteria for Failure for transistors which are not included in 2.2.5.1 or 2.2.5.2 above or are not on the device spec. drawing, have not yet been determined. Transistors in this category are to be exempted from any Water Entry Lot-Sampling tests until their failure criteria have been determined and added to this specification or the device specification drawing.

2.2.6 Disposition of Transistor Lots which have been rejected because of Lot-Sample failure for the Water Entry Test. (Ref. Quality Control Spec. 4014 and 4015)

The transistors of Lots which fail because of the Lot-Sample Water Test must not be submitted to IBM until the IBM approved test to eliminate Gross Leak Transistors (Paragraph 2.2.7 below) has been applied to the entire lot.

2.2.7 Test for Transistors of lots which have failed the Water Entry Test. (A test to remove gross leak transistors from failed lots - Ref. Paragraph 2.2.6 above)

2.2.7.1 Transistor Lots which have failed the Lot-Sampling, Water Entry Test may be re-submitted to IBM after the following test has been performed on all the transistors which make up the lot.

2.2.7.2 The Transistors of Lots to be tested should be placed in a suitable chamber and the chamber shall be evacuated to a vacuum of 28" of Hg (or lower). The vacuum shall be maintained for a period of 5 minutes. After this period pure water shall be introduced into the chamber so that all of the contained transistors are fully submerged for 5 minutes in water which is under an exerted gage pressure of 15 lbs./sq. inch (see Paragraph 2.2.3 for definition of pure water)

2.2.7.3 All Transistors which have been subjected to the Water Test (Paragraph 2.2.7.2 above) must be tested according to the appropriate test procedure and failure criteria outlined in Paragraph 2.2.5.1 and 2.2.5.2 above. Transistors that fail must be removed from the lot.

2.2.7.4 Transistors which are removed from the lot are not eligible for further re-submission to IBM. All other transistors which make up the lot may be re-submitted to IBM for acceptance according to Quality Control Spec. 4014 and 4015.

2.3 GENERAL STATEMENT concerning the use of additional types of Water Entry tests on IBM Semi-conductor devices.

2.3.1 The Use of Any Other Form of Water Entry Test or variation thereof must not be used on Semi-conductors supplied to IBM without prior approval by IBM.

2.4 GENERAL STATEMENT concerning the use of any technique employed to fill or otherwise stop-off transistor case leaks.

2.4.1 The Use of Any Technique to fill or otherwise stop-off transistors case leaks on transistors which are to be supplied to IBM must first be approved by IBM.

3. GENERAL NOTES

3.1 IBM reserves the right to subject Semi-conductors submitted or supplied in accordance with this specification to the tests outlined herein, in order to verify that the Hermetic Seal properties of the semi-conductors are consistent with the requirements of this specification.

3.2 The manufacturer shall, on request, permit access to his manufacturing facilities and such information as may be necessary to reasonably satisfy IBM that the manufacturer is complying with the provisions and intention of this specification.

3.3 No provisions or portions of this specification shall be interpreted to mean that the manufacturer shall be required to reveal any proprietary information or any information not directly related to the procurement of components under this specification.