G320-9175-0

Circuit Board Design System 2 General Information Manual

Installed User Program

IBM

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Circuit Board Design System 2 General Information Manual

Program Numbers: 5796-PRP Circuit Pack System
5796-PRL Design Verification System

This manual provides an overview of the Circuit Board Design System as an integrated system, and includes a description of each of its component parts.

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LIST OF ILLUSTRATIONS

1. INTRODUCTION

1.1 SCOPE

This General Information Manual is an introduction to the Circuit Board Design System (CBDS). The manual provides an overview of CBDS for management, application programmers, and terminal users.

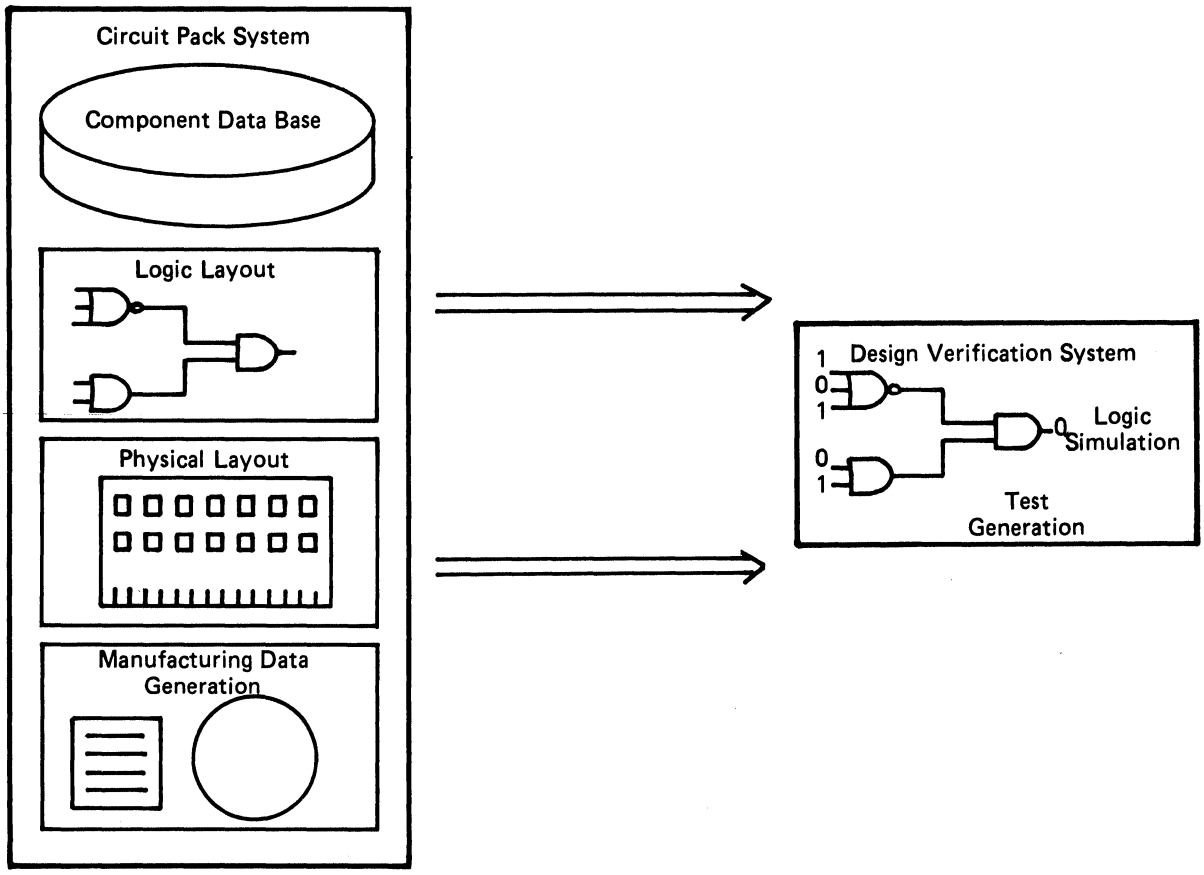


Figure 1. Circuit Board Design System

CBDS is a software system that supports all phases of the printed circuit board (PCB) design process. As shown in Figure 1, CBDS has two major elements: the Circuit Pack System (CPS), and the Design Verification System (DVS).

The **Circuit Pack System** (IUP 5796-PRP) is used for the creation of the schematic diagram, the design of the physical layout, the generation of manufacturing data and component definition and modification. CPS features an integrated design file data base and provides capabilities for both interactive graphics and automatic operating modes.

The **Design Verification System** (IUP 5796-PRL) provides functions which can enhance the accuracy and completeness of the logic design through digital logic simulation. DVS can also provide test patterns to be used with automatic test equipment.

1.2 ENVIRONMENT

1.2.1 HARDWARE

CBDS software is designed to run on the following IBM computers:

Processor: IBM 4331 Model K11
or 370/148 Model K
or IBM 3031

Also required are:

2 IBM 3310 Model 2 Direct Access Storage Devices (or equivalent)

1 9-track Tape Drive (800 bpi option may be required for plotting)

1 IBM 3277 Model 2 Display Station (with program functions keys)

1 IBM 3277 GA Graphics Attachment RPQ 7H0284 (this includes the joystick attachment)

1 Storage Display Monitor (such as Tektronix* 618)

1 IBM 3274 Display Control Unit Model D21 with RPQ 7H0289

1 IBM 3262 Model 1 Line Printer (or equivalent)

1 IBM 3278 Model 2 Display Station

* Registered trademark of Tektronix Corporation.

The IUPs are designed to operate with the minimum configuration. To take full advantage of the capabilities of the

product a:dditional work-stations, direct access storage devices, memory, or CPU power may be desirable. A plotter is recommended for hard-copy output such as schematics and artwork check-plots.

1.2.2 SOFTWARE

This IUP is coded in the languages:

- FORTRAN H Extended
- IBM Assembler

It was designed and tested in the following VM/370 CMS system environment.

- VM/370 Release 6 with BSEPP
- VM/SP Release 1

The following components are required for the Circuit Board Design System IUP's operation:

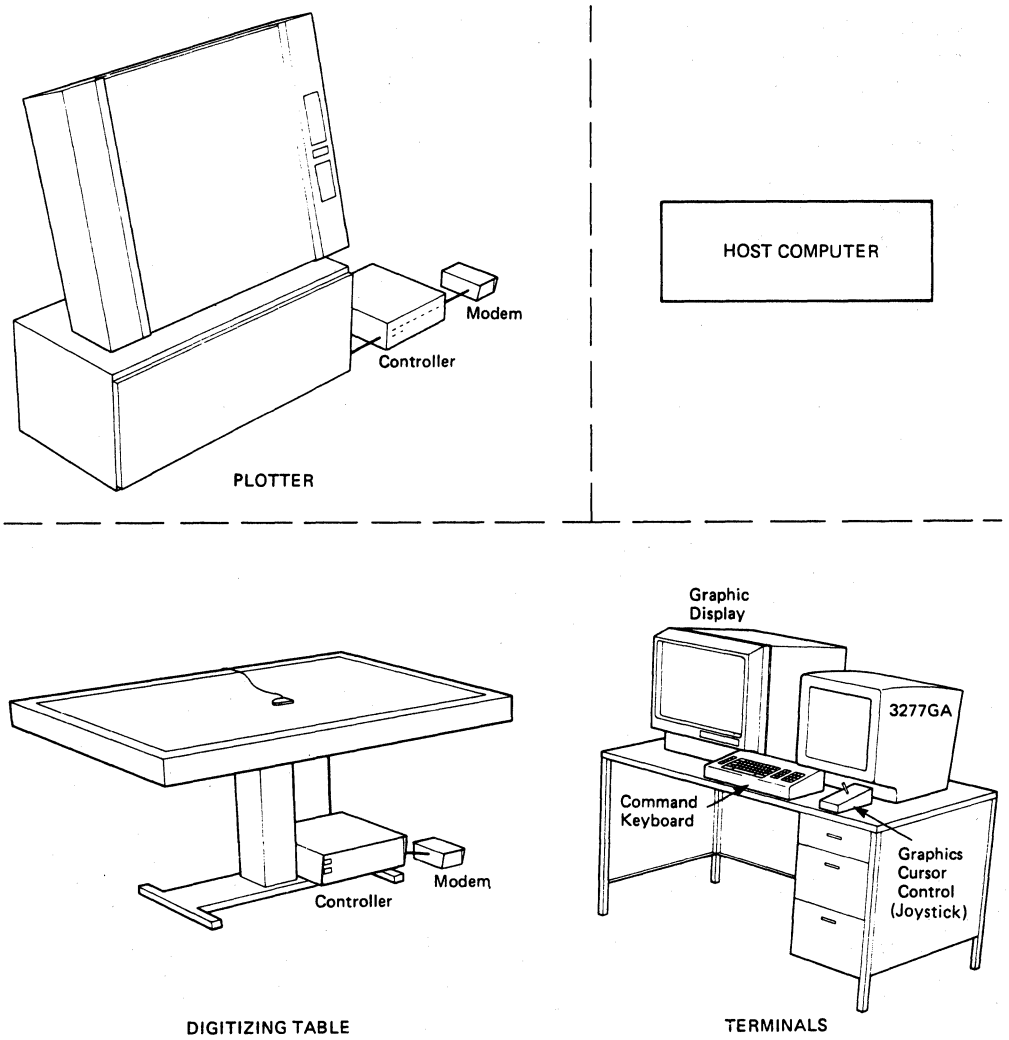
1. FORTRAN IV (5734-LM3)

   Optionally, the FORTRAN H Extended and Enhanced MOD II Library (5796-PKR) may be added.

2. IBM 3277 Graphics Attachment Support Programming for PRPQ P09013 (5799-AXX).

The basic user's workstation is illustrated in Figure 2. At this dual-screen interactive graphics workstation, the user is able to:

- capture a schematic design
- simulate digital logic for design verification and test generation
- perform PCB layout
- create data for manufacturing purposes
- store the completed design for subsequent revisions or for reference.



CBDS SYSTEM WORK STATION COMPONENTS

Figure 2. Workstation Configuration

1.3 CBDS FEATURES

CBDS is a comprehensive Computer-Aided Design/ Computer-Aided Manufacture (CAD/CAM) system which can support top management objectives with specific benefits:

Management Objectives	CBDS Can Provide
• Cost Reduction	• Improved productivity
• Product Quality	• Reduced design errors and resultant engineering changes
• Reduced Design Cycle Time	• Faster turnaround on new designs and revisions
• Increased Control	• Fewer hardware prototypes
	• Increased peak load capacity
	• Improved design level controls
	• Design standardization
	• Consistent and automated documentation
	• Ability to handle more complex designs
	• Automated manufacturing data

Automated PCB design is becoming more common in the electronic engineering community as automated PCB design systems become increasingly more cost effective. The sophistication and range of function in the Circuit Board Design System can be illustrated by some highlights of the system:

- Completely Integrated Function:
  - all key applications are linked by common design files providing enhanced data integrity
- Interactive Graphics:
  - when combined with an available storage display monitor, the IBM 3277 graphics attachment display station provides a dual-screen interactive graphic work station

- design functions, such as schematic entry, component placement, and printed wire routing, can be done in real time and viewed immediately on the graphics display

- Powerful Automatic Design Tools:

  - automatic component placement, and printed wire routing functions are completely integrated into the application to provide online design capability in concert with the interactive graphics features

- Centralized Component Data Management:

  - all physical and electronic component data and associated symbols are centrally created and controlled a starter component data base is provided containing a large number of commonly-used components

- Physical Design Flexibility:

  - physical board characteristics such as size and number of layers can be conveniently specified

  - digital, analog, or a mixture of layouts are fully supported

- Integrated Logic Design Analysis Tools:

  - online digital simulation for early design modeling is provided

  - functional test patterns for digital designs can be interactively specified and automatically evaluated

- Design Validation Functions:

  - connectivity is verified dynamically during schematic and physical layout

  - unconnected circuitry is brought to the designer's attention

  - completed layouts are checked to ensure that no manufacturing tolerances have been violated

  - the schematic can be automatically back-annotated with the PCB layout data to ensure that the schematic consistently reflects the physical layout.

1.4 RELATED DOCUMENTS

Table 1 lists the available CBDS documentation according to the function of each document.

Table 1: CBDS Documentation

Contents	Title
System overview	CBDS General Information Manual (G320-9175)
Terminal operation, basic procedures for schematic and PCB layout, manufacturing data generation and component data base administration.	Circuit Pack System Application Manual (SH20-2699)
Logic and fault simulation	Design Verification System Application Manual (SH20-2758)
Detailed function descriptions for:	
Schematic generation	Schematic Layout Subsystem Terminal User Guide (SH20-2754)
PCB layout	Physical Layout Subsystem Terminal User Guide (SH20-2755)
Manufacturing data generation	Manufacturing Data Generation Subsystem Terminal User Guide (SH20-2756)
CDB administration	Component Data Base Subsystem Terminal User Guide (SH20-2757)
Logic and fault simulation	Design Verification System Terminal User Guide (SH20-2751)
Installation instructions and application programmers' interface descriptions	CPS Program Description and Operation Manual (SH20-2698) DVS Program Description and Operation Manual (SH20-2700)

2. SYSTEM OVERVIEW

2.1 INTRODUCTION

Figure 3 shows the basic inter-relationships between the systems of CBDS. The Circuit Pack System is used to produce PCB designs, each of which is documented in the form of a design file. The design file of a PCB holds all the information related to that design; the schematic layout, the PCB layout, and the manufacturing data for PCB production. Relevant portions of the design files are used in the Design Verification System to verify logic design and to generate test data.

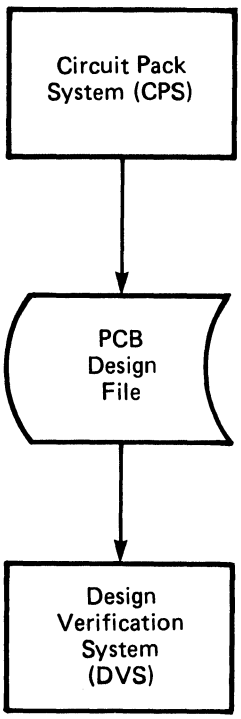


Figure 3. CBDS Systems

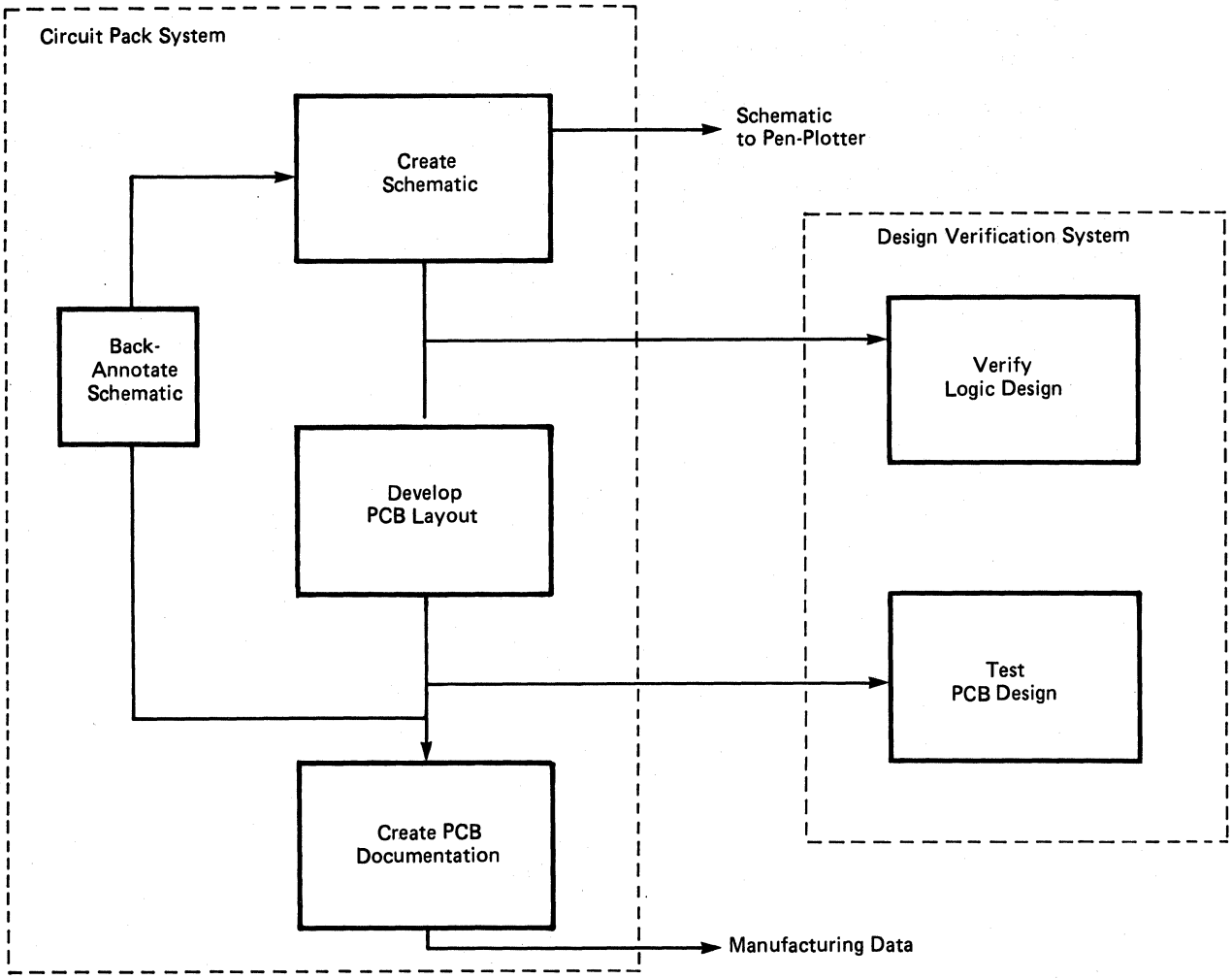


Figure 4. PCB Design with CBDS

2.2 PCB DESIGN PROCESS

The major objectives in the design of a PCB are to create a schematic of the logic design, to develop a board layout, and to generate manufacturing information for the board. Other objectives may be to verify the logic design and generate test data for the PCB, and to store the completed design. Figure 4 illustrates the basic stages in the process of creating a PCB design with CBDS.

The logic designer's sketch initiates the process. Using interactive graphics and the schematic layout capability, a user quickly and and accurately converts the sketch into a precise logic schematic on the graphics display. The captured sketch can be plotted for hard-copy reference, re-edited for engineering changes or converted into an initial design file suitable for the next design phase, physical layout.

The physical layout capability permits the user to assign logic gates to physical components retrieved from the component data base, place the components on the circuit board, and generate error-free wire routing. Either interactive graphics functions or automatic facilities can be utilized. The physical layout phase has been developed to provide a continuous and organized operator interface, in which design rule checking is an integral feature.

The schematic can be compared for inconsistencies to the physical design at its completion, in case logic design changes have been made during physical layout. Revisions can be interactively incorporated in the schematic if required at this stage. The now complete design file is ready for manufacturing data generation. A set of interactive functions are employed by the user to generate an appropriate file suitable for photoplotting, files suitable for hard-copy plots, reference listings, and numeric control drill tapes.

The Design Verification System is an optional capability. A logic designer uses the Design Verification System to evaluate the logic design. Digital logic simulation and test generation tools can be interactively controlled at the work station to set up large design problems. Simulations can be completed either interactively or as batch jobs, and the results inspected interactively.

3. SYSTEM DESCRIPTIONS

3.1 CIRCUIT PACK SYSTEM

3.1.1 INTRODUCTION

Purpose

The Circuit Pack System (CPS) contains four major subsystems, each of which is used to control one aspect of PCB design and production: the Schematic Layout subsystem, the Physical Layout subsystem, the Manufacturing Data Generation subsystem, and the Component Data Base.

The **Schematic Layout** subsystem (LOKI) allows the user at a graphics terminal to capture schematic data, edit existing schematics, plot schematics, and correlate the schematic with its corresponding PCB.

The **Physical Layout** subsystem (SPRIG) uses information from the circuit schematic as an input and provides user-controlled procedures for assigning logic gate symbols to physical components, placing components on the circuit board, and routing the corresponding connections between the various components. Facilities for verification of completed layouts are also available within SPRIG.

The **Manufacturing Data Generation** subsystem (FABRIC) generates manufacturing information from the completed board layout. This information includes a bill-of-materials, data for photoplotter transparencies for masks and silkscreening, automatic insertion data, and a numeric-control drill tape.

The **Component Data Base** subsystem (CDB) is the source of all the components and symbols used during the design of a PCB. The CDB provides graphics symbols and component data for schematic layout, physical layout, and the generation of manufacturing data. The CDB subsystem contains functions to enable the management of component data.

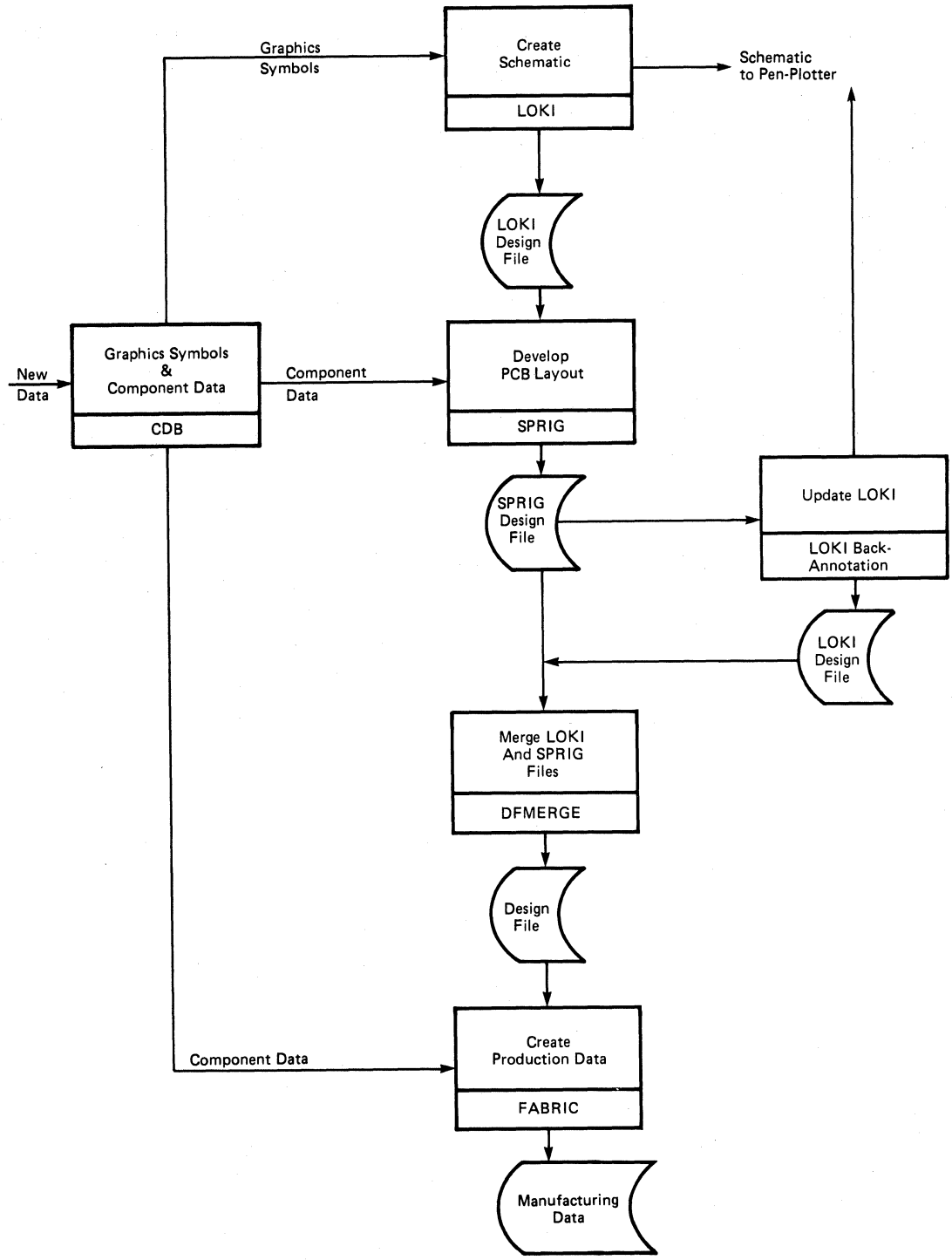


Figure 5. PCB Design in CPS

Functions

Figure 5 illustrates the overall flow of information and design activity in PCB design using CPS.

The initial design is captured and edited through LOKI, accessing the symbol libraries of the CDB for the graphics symbols. The design may be plotted and edited any number of times, and the resulting schematic is then recorded in a design file. The design file from LOKI provides the initial design and connectivity information for SPRIG. Through SPRIG, the processes of gate assignment, component placement, printed wire routing, and verification are carried out, using component data from the CDB.

Once the final board layout has been achieved using SPRIG, it is recorded in the design file. The design file is re-submitted to LOKI to add layout information from SPRIG to the schematic, as well as to record any design changes made while using SPRIG. Once this back-annotation process has been performed, the LOKI and SPRIG design files are merged using the DFMERGE facility of CPS. The resulting design file becomes the input to FABRIC, which produces manufacturing information for the PCB: a bill of materials, data for photoplotter layout and solder resist masks and silkscreens, a numeric-control drill tape, auto-insertion data, a hole and land data base, a pack usage and spare circuit report, and from/to lists sorted by signal and by component.

3.1.2 SCHEMATIC LAYOUT

Purpose

The Schematic Layout System (LOKI) is used to create and edit schematic drawings. A design may contain up to 30 schematic sheets, and the size and format of the sheets are defined by the user. Figure 6 shows a typical sheet border.

Functions

LOKI provides sets of functions that allow the user to control the design process. To use any of these functions, the user simply selects the required one from the list (or 'menu') provided on the terminal screen.

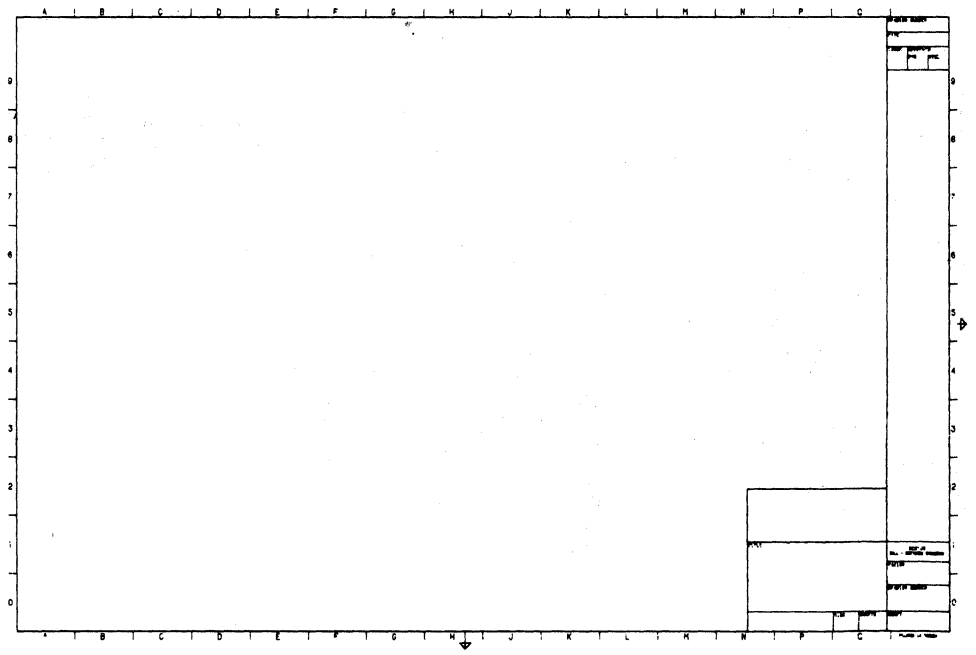


Figure 6. Typical LOKI Sheet Border

The user can call up symbols from the CDB, and position them within the schematic sheet border. Schematic symbols can be specified at both gate and component levels, as shown in Figure 7.

Once the symbols are positioned, the user may add text to the symbols (signal names, symbol designators, etc.), and may apply comment text and graphics, such as tables, wherever required. Component designators may be automatically supplied by the system, or may be placed interactively by the designer.

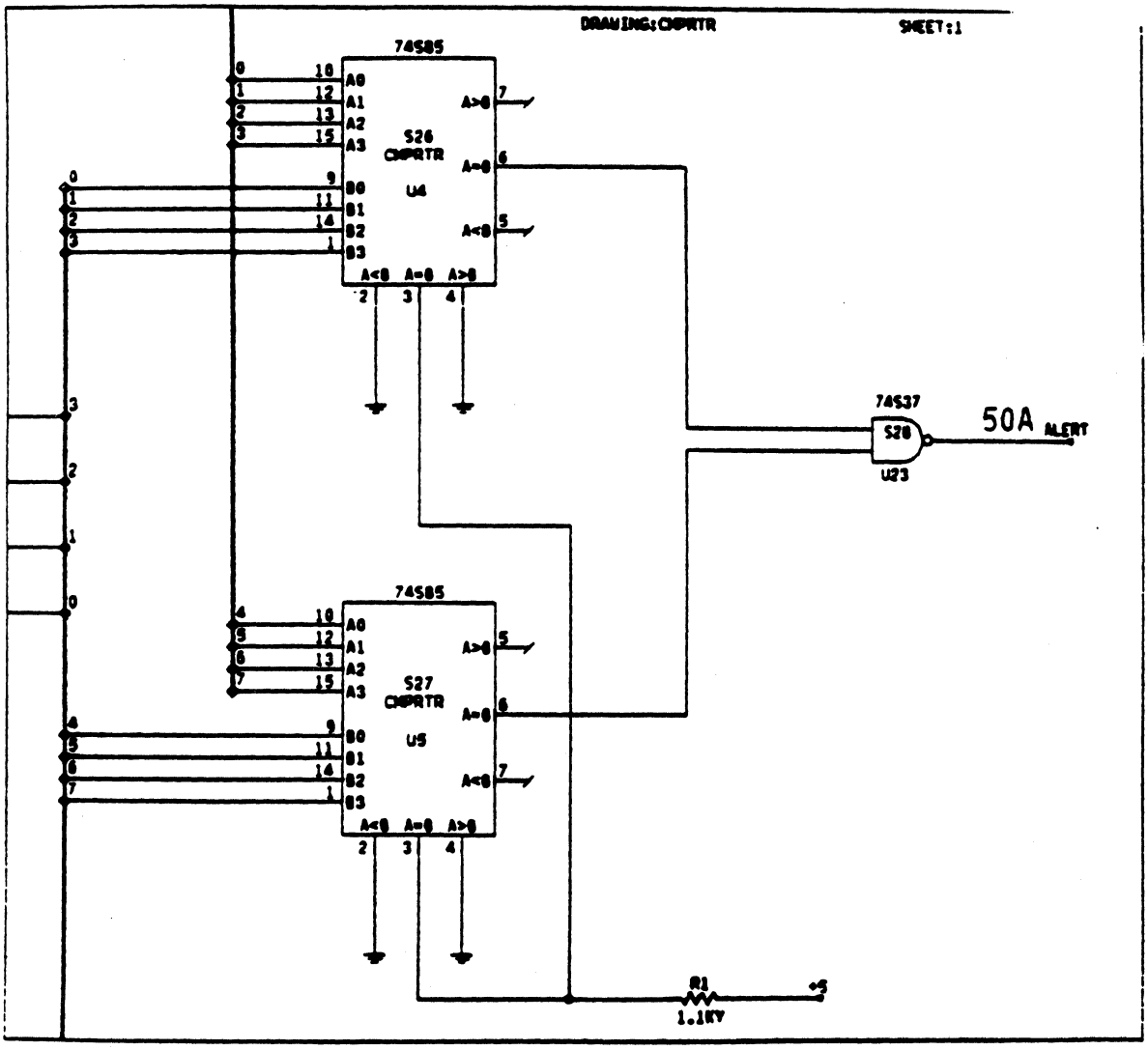


Figure 7. LOKI Schematic Symbols

At any time during the design process, the user may alter the position of schematic elements. LOKI provides functions that move gates or groups of elements, and functions that copy groups within the schematic to speed up the entry process. In Figure 8, the window shown by dashed lines has been copied onto the bottom third of the sheet. LOKI enables the user to design commonly used portions of individual schematics once, and to retrieve that schematic data as a unit for inclusion in the schematic currently being designed.

The user may connect symbols logically and graphically using interactive connection functions, or LOKI's automatic router. With either interactive or automatic facility, signal bussing is employed to make schematic diagrams more readable (as illustrated by Figure 9). LOKI automatically performs connectivity checking, as shown in Figure 10, to ensure a consistent, complete schematic.

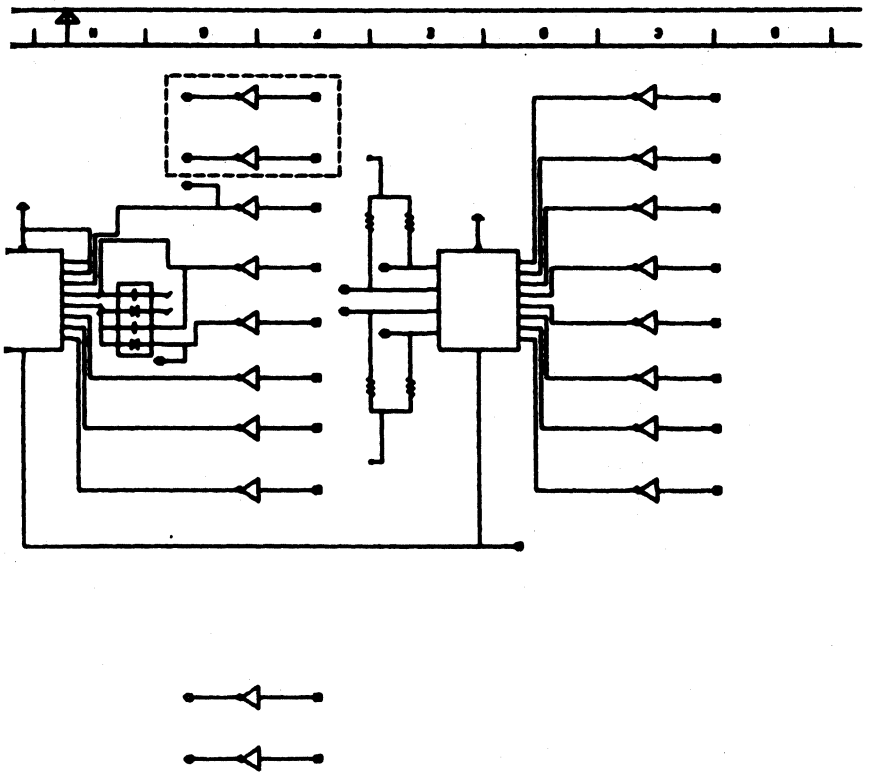


Figure 8. Schematic Move and Copy Facilities

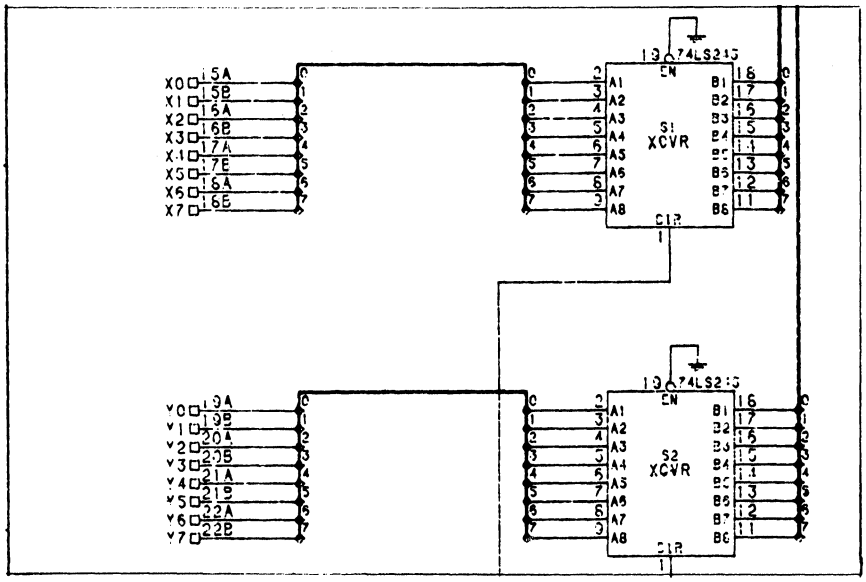


Figure 9. Signal Bussing

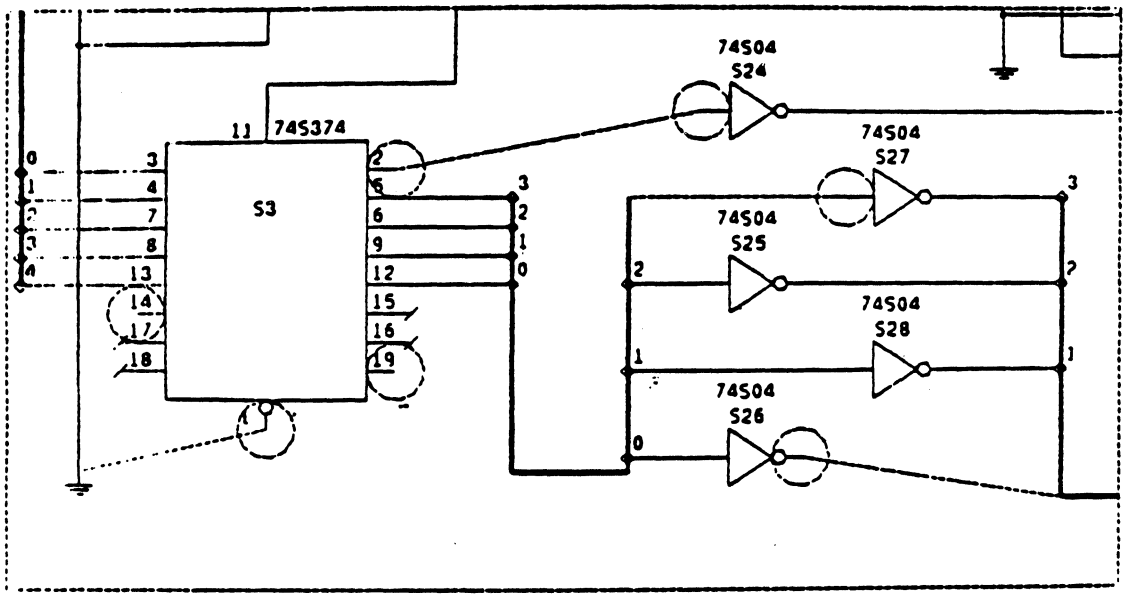


Figure 10. Connectivity Verification

Throughout the process of creating a schematic with LOKI, a set of display functions is available to provide control of the terminal screen. For example, the user may specify the size of the display elements by magnifying a portion of the schematic. Figure 11 illustrates this facility. The user can also control the type of data to be visible (e.g., symbols, lines, text, etc.).

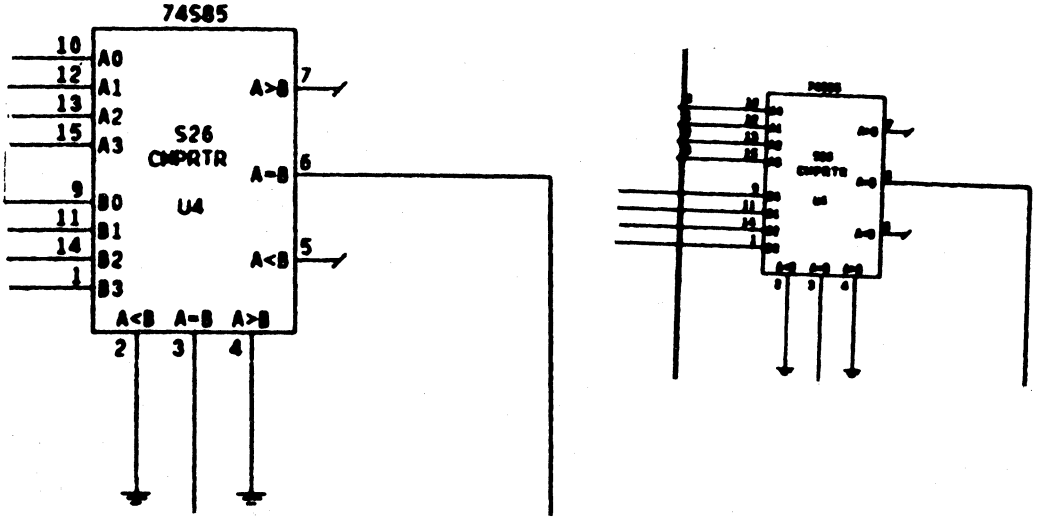


Figure 11. Display Functions

The display features of size and visible elements can also be specified for the plotting facility, which enables the user to produce hard-copy schematic drawings on a plotter.

After a design has been completed and the PCB layout developed with SPRIG, LOKI's back-annotation facility is used to produce an accurate and current schematic with component and board location data. (Refer to Figure 12.) Any differences between the schematic and the physical layout are brought to the user's attention.

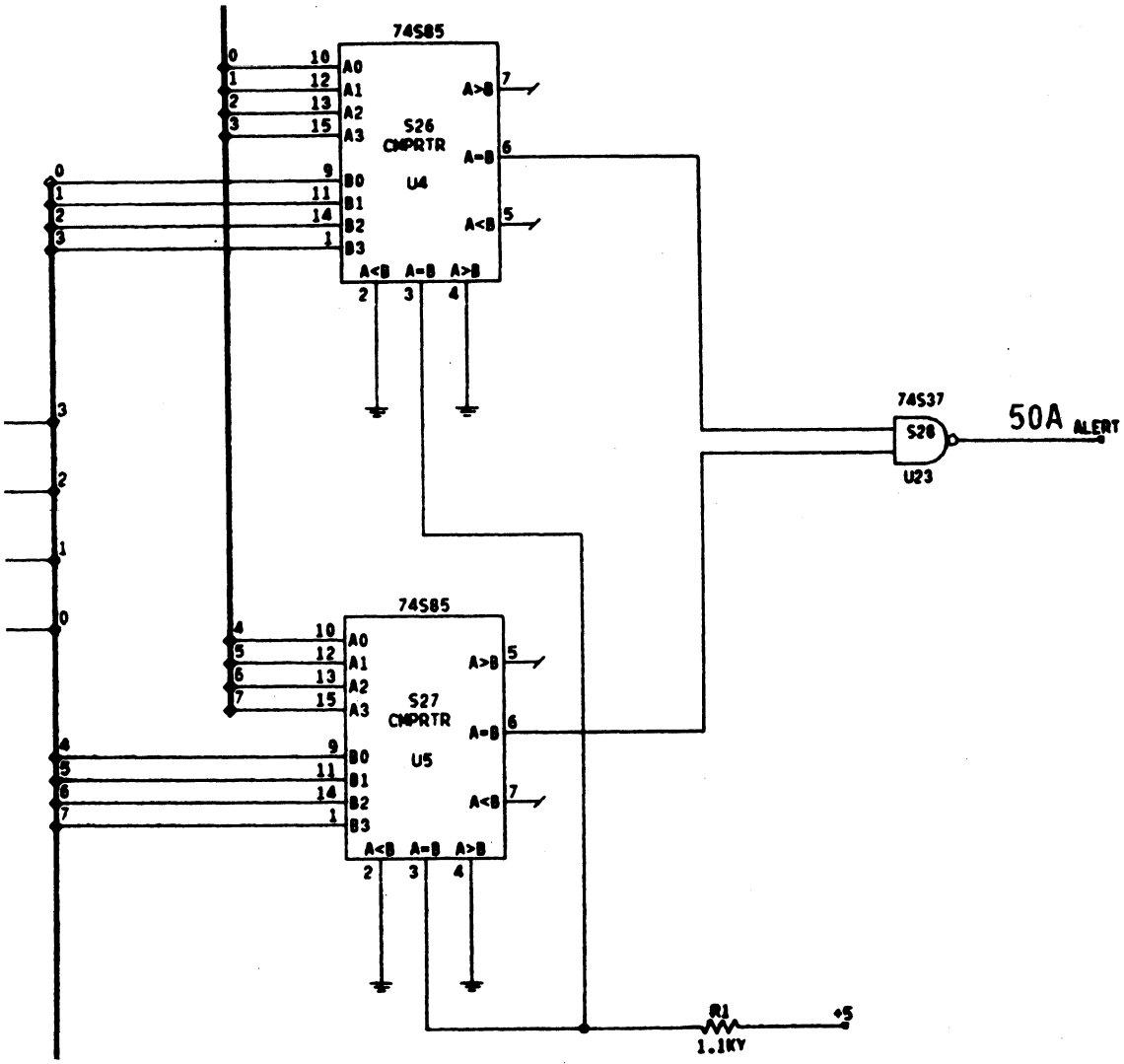


Figure 12. LOKI Back-annotation

3.1.3 PHYSICAL LAYOUT

Purpose

The Physical Layout system (SPRIG) is used to perform PCB layout design.

Functions

SPRIG provides both automatic and interactive functions to perform:

- assignment of gates to components
- component placement
- printed wire routing
- validation of PCB layout against design rules.

The automatic functions are provided to offer substantial time-saving to the designer. However, SPRIG also provides interactive functions to handle special cases and to provide editing capability. As in LOKI, the user selects automatic or interactive functions from menus displayed on the terminal screen.

Generally, the basic design information is provided to SPRIG in the form of a design file from LOKI. However, SPRIG provides interactive functions that may be used to supply this information. Alternatively, for cases in which a manual layout has already been performed, SPRIG accepts input data from a digitizing table.

In any case, the user may define the board size and shape (refer to Figure 13). Up to 16 layers can be specified for printed wire and voltage planes. Copper fill areas, board cutouts, and pad shapes are easily specified. SPRIG enables the designer to streamline this process for cases in which many boards have common basic characteristics. When this situation occurs, the information may be specified to SPRIG in the form of an input file, rather than by repetitive entry of data.

Once the basic board characteristics are defined, the automatic assignment facility may be used to allocate gates to circuit packs.

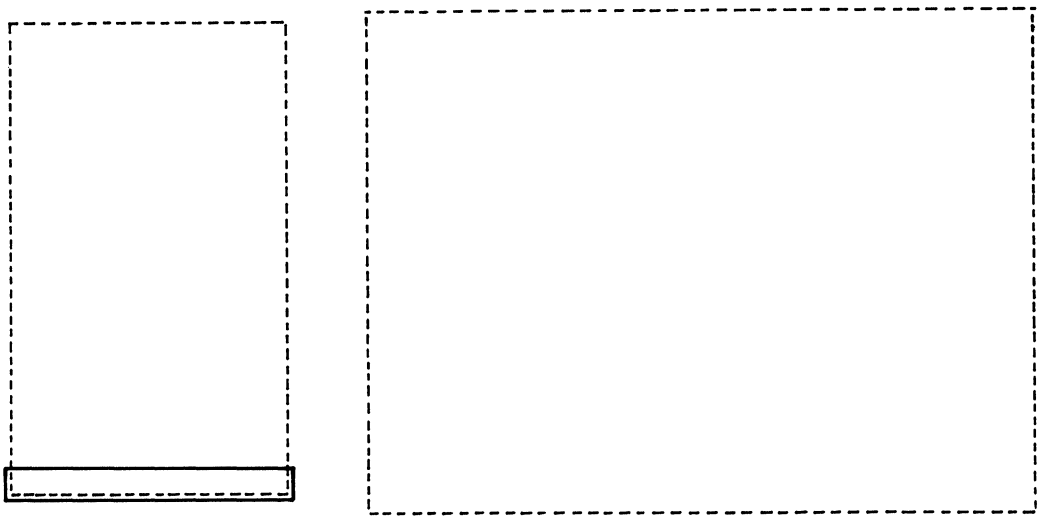


Figure 13. SPRIG Board Outline

Figure 14 illustrates a typical board layout with placed components. Automatic component placement is based on a critical cost function selected by the user: wire length, density of signals, or wire crossing count.

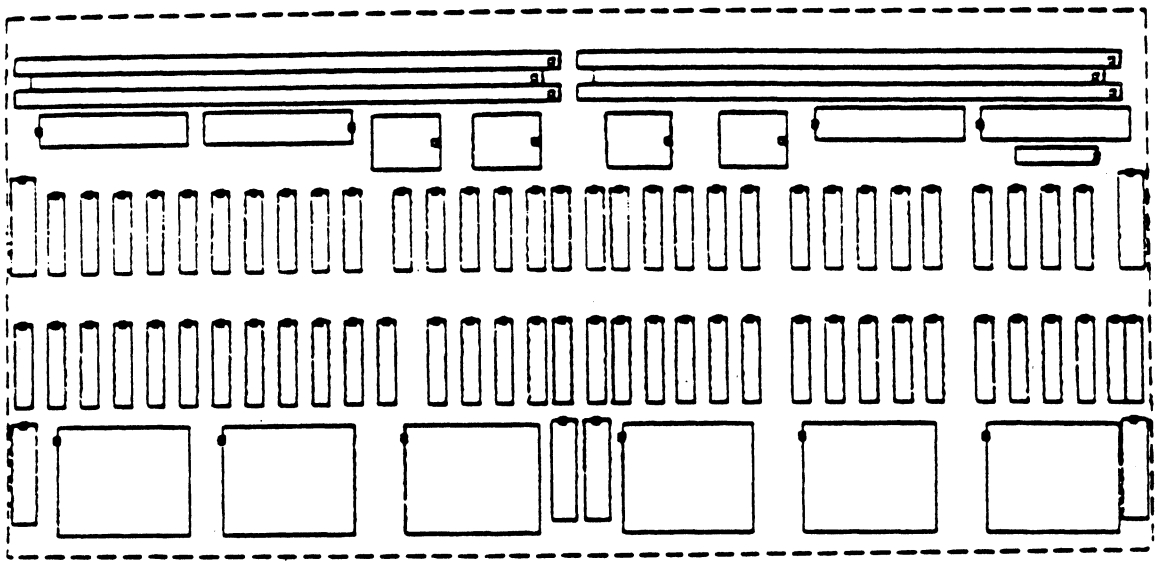


Figure 14. Placed Components

When a suitable placement is achieved, the automatic optimization of gate and pin assignment is performed. Figure 15 illustrates the logical connections among three components and a connector before and after optimization.

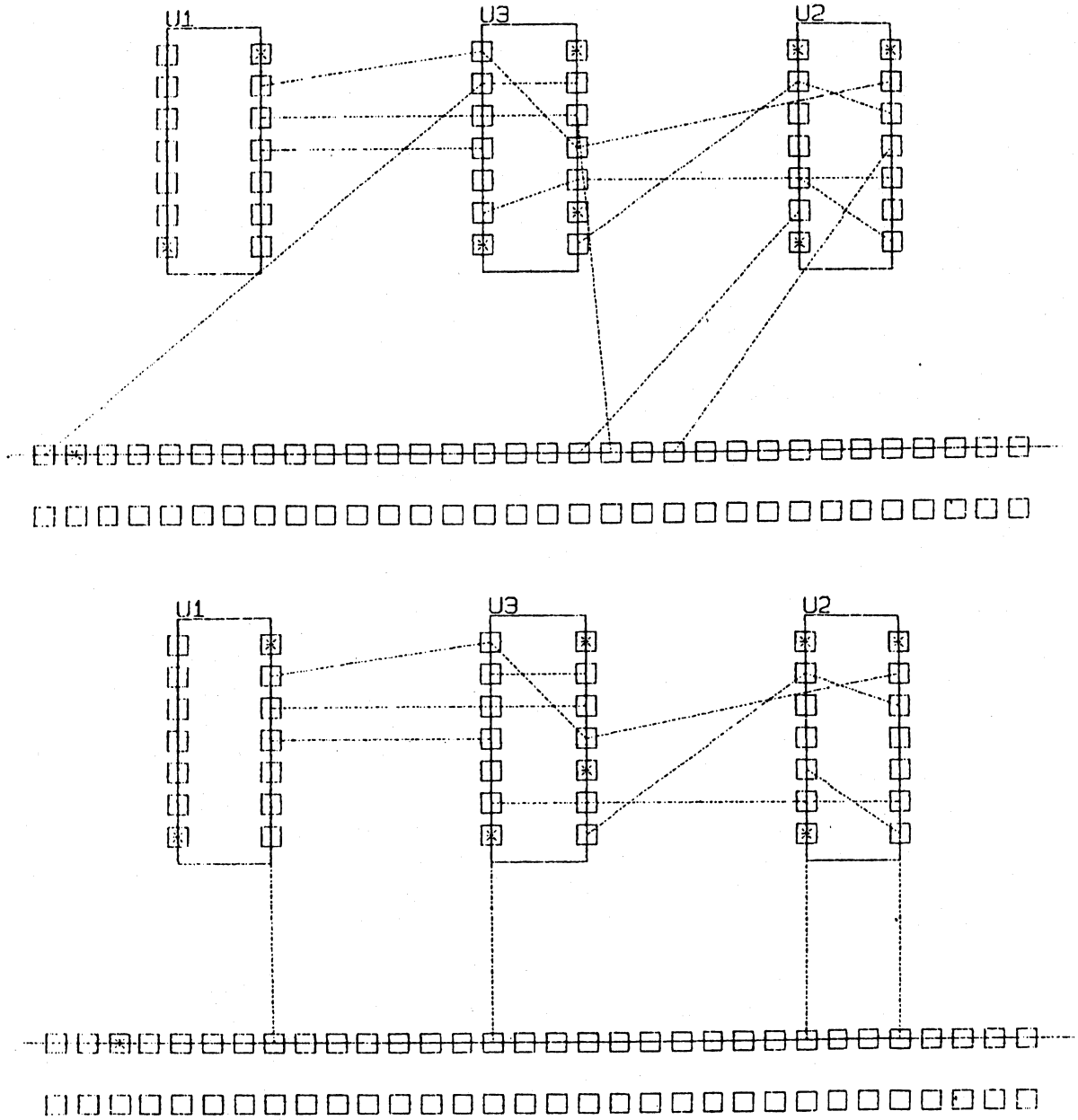


Figure 15. Optimization

Routing of connecting wires may be performed interactively or automatically. Interactive graphic routing can be on- or off-grid, with both orthogonal and 45-degree wires, as shown in Figure 16. Track width and spacing may be specified for each signal.

There are four automatic routers available to the user, which range from a very rapid router for symmetrical routing patterns to an exhaustive router for more complex boards. These routers can be controlled by the designer, who may specify the routing window, time to be spent on each connection, signals to be routed first, etc.

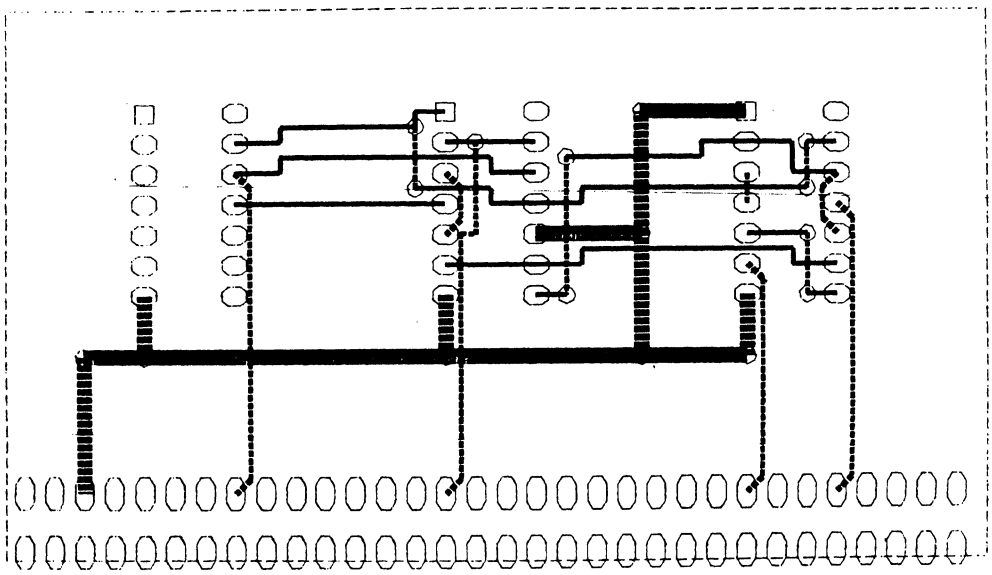


Figure 16. Printed Wire Routing

When wire routing is completed, it may be automatically tiedied to increase board reliability and manufacturability through via minimization, cutting of track bends, and banking around pins and vias. Figure 17 illustrates the same board shown in Figure 16 after the tidying facility has been used.

As in LOKI, the display screen is under the control of the user throughout the operation, so that the designer can specify the display window and the visible elements. A special feature of SPRIG enables the user to display logical connections that are not yet routed (as in Figure 15).

The completed physical design is used to update the schematic with gate and pin assignments, and component and board location data.

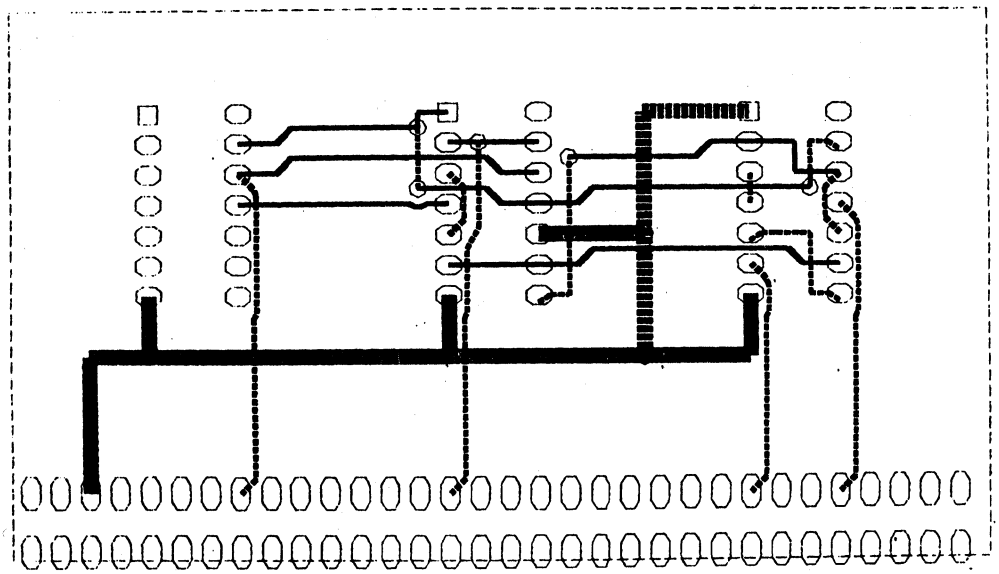


Figure 17. Tidied PCB Layout

3.1.4 MANUFACTURING DATA GENERATION

Purpose

The Manufacturing Data Generation system (FABRIC) provides files, tapes, and hard-copy output used to manufacture the PCB.

Functions

FABRIC includes a function set that enables the user to create:

- a bill of materials
- photoplotter data for circuit layout masks and solder resist masks
- photoplotter data for silkscreen layouts or assembly drawings
- numeric control (NC) drill tape data
- a hole and land data table
- automatic component insertion data
- a pack usage report and a spare circuit report
- from/to lists by signal and by component.

Each FABRIC function automatically creates a file which contains the appropriate data for the document to be produced. Once the file has been generated, the FABRIC user directs it to appropriate device (photoplotter, plotter, paper tape punch, or printer) to generate the output. The layout mask, solder mask, and silkscreen layout files are sent to the photoplotter for the production of transparencies. Layout data for the assembly drawings is directed to the plotter, and the reports are sent to the printer. When the user has created these files, the data may be examined at the workstation.

The bill of materials report provides a quantitative analysis of all the components on the PCB. This report identifies each component by product code, and provides the product description and supplier, and the quantity required of each component. (A sample bill of materials is shown in Figure 18.) This report is used to select components for manufacturing, and can provide the basis for various additional reports, such as: cost projections, availability and scheduling, automation of order processing.

STOCKLIST FOR SAMPSPBG STK GENERATED ON 24AUG82 PAGE: 1

QTY.	PCODE	CPCODE	SUPPLIER	DESCRIPTION
9	.1UF			CAP CER 0.1UF 50V 10% C1, C10, C11, C12, C5, C6, C7, C8, C9
1	1.0KY			RES 1 KOHM 1/4W 2% R1
4	2114V2			IC RAM 1K X 4 MOS 200NS U3, U4, U5, U6
1	64C-PIN			R1
2	74LS245			IC OCTAL BUS XCVR 3S U1, U2
1	74S04			IC HEX INVERTER U8
4	74S181			IC 4-BIT ALU U9, U10, U11, U12
1	74S241			IC OCT BUFFER 3-STATE U13
1	74S37			IC QUAD 2-IN NAND BUFFER U14
3	74S374			IC OCT 3-STATE FLIP-FLOP U18, U19, U20
2	74S85			IC 4-BIT COMPARATOR U15, U16
1	7407			IC HEX BUFFER OC HV U17
1	7432			IC QUAD 2-IN OR U7

Figure 18. FABRIC Bill of Materials

FABRIC produces a file that describes the copper areas of the PCB surfaces, which is used to drive a photoplotter to create circuit layout masks. (An example is provided in Figure 19.) Using a simple FABRIC function, the user can create a mask file for each layer of the board, and is able to specify the type of photoplotter to be used. Either positive or negative masks can be produced, according to the manufacturing method in use. The user is able to simulate the photoplotter output with FABRIC, and view it at the graphics terminal screen.

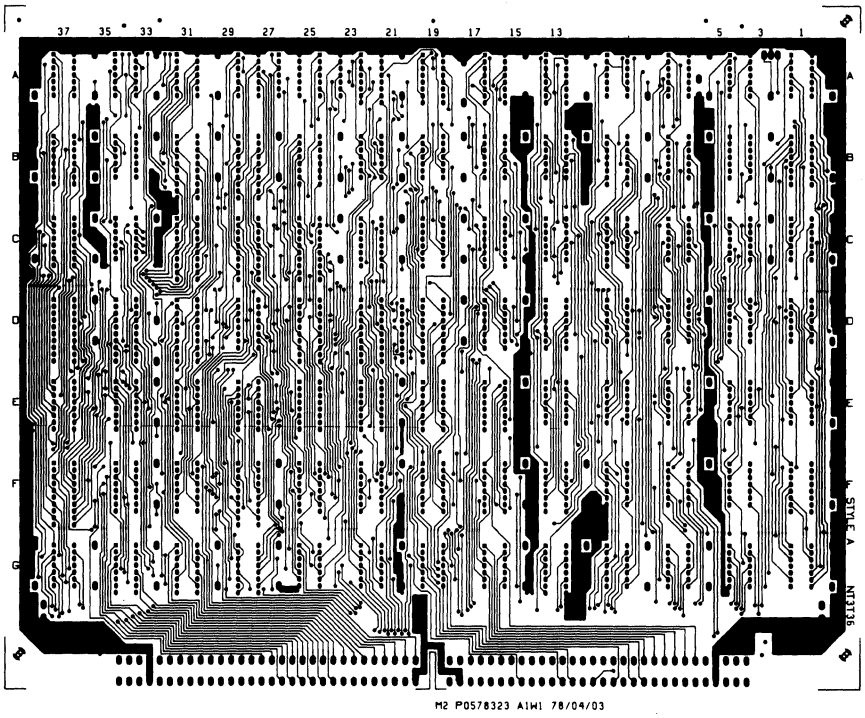


Figure 19. Circuit Layout Mask

A similar function is used to create plotter data for solder resist transparencies, such as the sample in Figure 20.

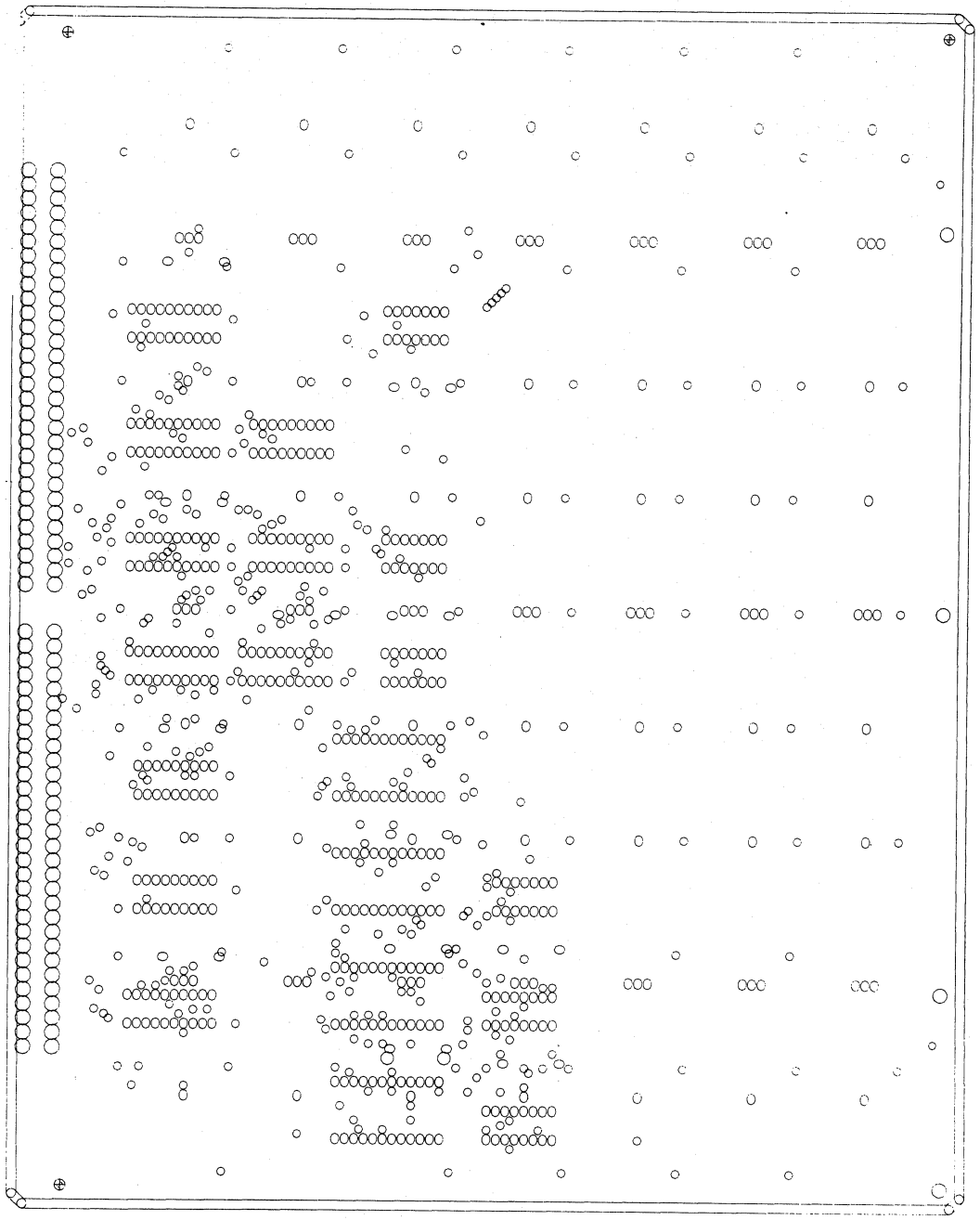


Figure 20. Solder Resist Mask

To create a silkscreen component layout or an assembly drawing, the user generates a FABRIC file that contains component outlines and codes, polarity indicators, and optional identifying artwork. (Refer to Figure 21.) When a silkscreen transparency is required, the file is processed by the selected photoplotter; when an assembly drawing is to be generated, the user directs the file to the plotter, using the CPS plotter utilities.

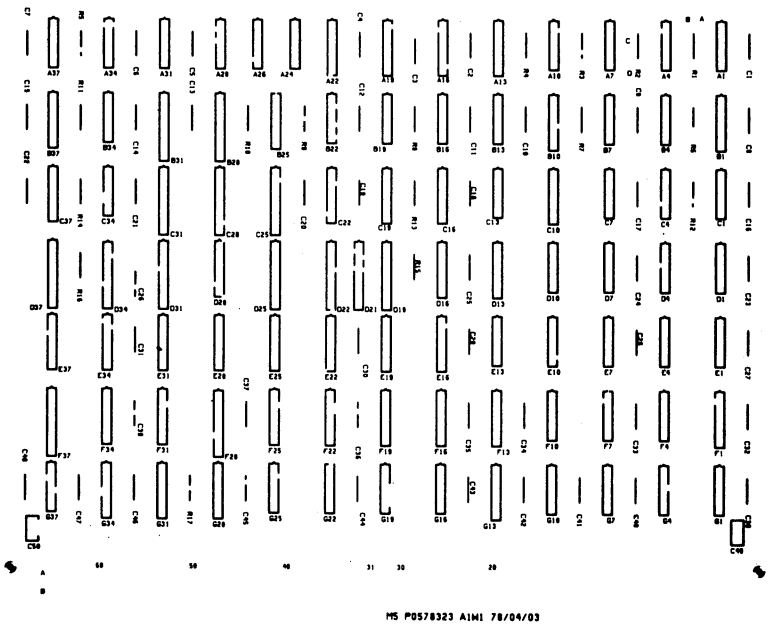


Figure 21. Silkscreen/Assembly Data

If overlapping of information occurs on silkscreen data, FABRIC's editing facility is available to correct the problem. In editing mode, the user is able to display the file and use interactive graphics to make modifications (such as moving lines or text). Figure 22 illustrates the graphics screen during the process of moving some overlapping text; the text, R1, has been positioned, and its original location indicated by a rectangle.

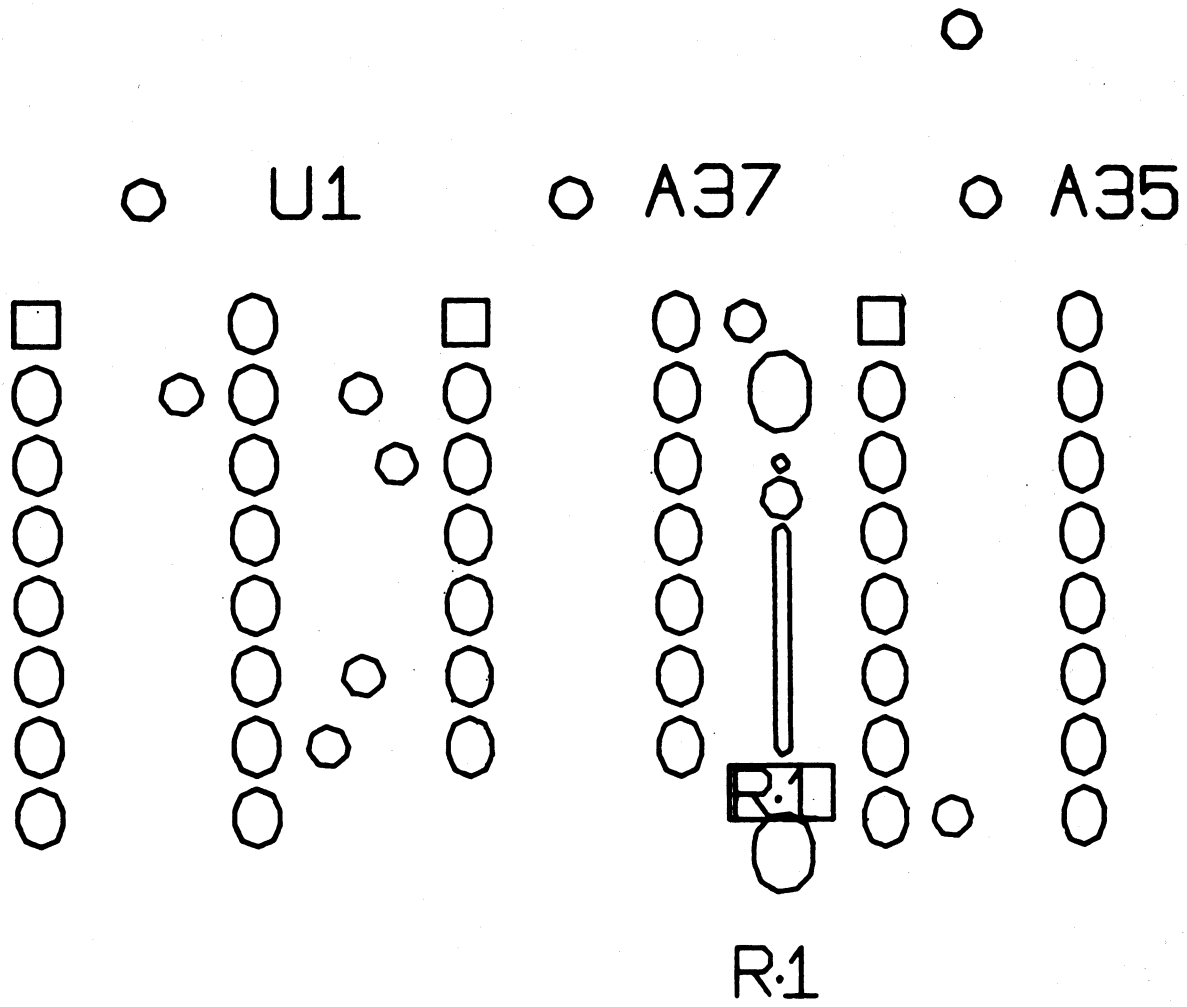


Figure 22. FABRIC Editing Mode

The NC drill file created with FABRIC is sent to a paper tape punch. The resulting tape is used to program a numerically-controlled drill machine with the positions and diameters of all holes to be drilled in the board. Alternatively, a photoplotter mask of hole locations on the board may be produced. (Figure 23 illustrates a sample drill mask.) This information can also be generated for production use in the form of the hole and land data table. This report, as shown in the sample in Figure 24, provides the x and y coordinate positions of each hole to be drilled and the land (pad) size.

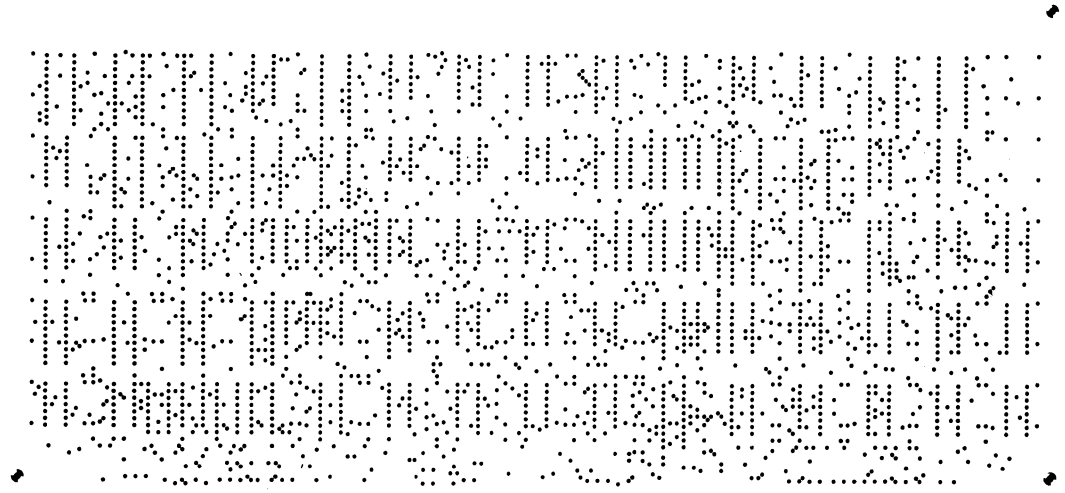


Figure 23. NC Drill Mask

PLOT DATE: 27MAY82

H O L E A N D L A N D D A T A T A B L E

BABB04

PLOT ISS :

HOLE = 0.034 DIA

LAND = 0.060 DIA

REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y
56	-1.000	2.700	57	-1.000	4.200	58	-0.400	2.700	59	-0.400	4.200	60	-0.400	5.700
61	-0.400	7.200												

HOLE = 0.044 DIA

LAND = 0.060 X 0.032 OVAL

REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y
1	-7.400	8.400	2	-7.300	8.400	3	-7.200	8.400	4	-7.100	8.400	5	-7.000	8.400
6	-6.900	8.400	7	-6.800	8.400	8	-6.700	8.400	9	-5.050	8.100	10	-5.050	8.400
11	-4.900	8.100	12	-4.900	8.400	13	-4.750	8.100	14	-4.750	8.400	15	-4.600	8.100
16	-4.600	8.400	17	-4.450	8.100	18	-4.450	8.400	19	-4.300	8.100	20	-4.300	8.400
21	-4.150	8.100	22	-4.150	8.400	23	-4.000	8.100	24	-4.000	8.400	25	-3.850	8.100
26	-3.850	8.400	27	-3.700	8.100	28	-3.700	8.400	29	-3.550	8.100	30	-3.550	8.400
31	-3.400	8.100	32	-3.400	8.400	33	-3.250	8.100	34	-3.250	8.400	35	-3.100	8.100
36	-3.100	8.400	37	-2.950	8.100	38	-2.950	8.400	39	-2.800	8.100	40	-2.800	8.400
41	-2.650	8.100	42	-2.650	8.400	43	-2.500	8.100	44	-2.500	8.400	45	-2.350	8.100
46	-2.350	8.400	47	-2.200	8.100	48	-2.200	8.400	49	-2.050	8.100	50	-2.050	8.400
51	-1.900	8.100	52	-1.900	8.400	53	-1.750	8.100	54	-1.750	8.400	55	-1.600	8.100
56	-1.600	8.400												

HOLE = 0.044 DIA

LAND = 0.112 X 0.087 OVAL

REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y	REF	X	Y
1	-8.200	7.500	2	-8.200	7.700	3	-8.200	7.900	4	-7.600	7.500	5	-7.600	7.700
6	-7.600	7.900	7	-7.000	7.500	8	-7.000	7.700	9	-6.400	7.500	10	-6.400	7.700

Figure 24. Hole and Land Data Table

The automatic insertion report lists the position of each component on the board, providing the data required to program an automatic insertion machine. Figure 25 illustrates a sample report.

DATE: 27MAY82
MINE P.C.B. ENGINEERING CODE: ABC
INSERTION REPORT ISSUE: 99
FOR IC

COMP DESIG	CPC CODE	ING CODE	DESCRIPTION	COMP VALUE	LENGTH	WIDTH /DIAM	WIRE DIAM	NUM PIN	PHS	SPAN	OR	X COORD	Y COORD	INS DEPTH	INS COD
U1			IC 4-TO-16 DECODER	QM74L154P5	1300	550	18	24	39	0	0	4000	4500	0	
U2			IC 4-TO-16 DECODER	QM74L154P5	1300	550	18	24	39	0	0	4900	4500	0	
U3			IC QUAD 2-IN OR	QM74LS32P5	770	260	18	14	39	0	0	5800	4200	0	*
U4			IC QUAD 2-IN OR	QM74LS32P5	770	260	18	14	39	0	0	3400	4200	0	*
U5			IC QUAD 2-IN OR	QM74LS32P5	770	260	18	14	39	0	0	3400	5700	0	*
U6			IC QUAD 2-IN OR	QM74LS32P5	770	260	18	14	39	0	0	4600	1200	0	*
U7			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7600	4200	0	*
U8			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7000	5700	0	*
U9			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	5200	1200	0	*
U10			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	6400	5700	0	*
U11			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7600	2700	0	*
U12			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	5200	2700	0	*
U13			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7600	1200	0	*
U14			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	8200	1200	0	*
U15			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7600	5700	0	*
U16			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	8200	5700	0	*
U17			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	1000	2700	0	*
U18			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	6400	2700	0	*
U19			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	6400	4200	0	*
U20			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	7000	4200	0	*
U21			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	5800	7200	0	*
U22			IC 2-2 AOI / 3-3 AOI	QM74LS51P5	770	260	18	14	39	0	0	2800	1200	0	*
U23			IC QUAD 2-IN NOR	QM74LS02P5	770	260	18	14	39	0	0	1000	1200	0	*
U24			IC QUAD 2-IN NOR	QM74LS02P5	770	260	18	14	39	0	0	4600	2700	0	*
U25			IC QUAD 2-IN NOR	QM74LS02P5	770	260	18	14	39	0	0	4600	5700	0	*
U26			IC QUAD 2-IN NOR	QM74LS02P5	770	260	18	14	39	0	0	3400	2700	0	*
U27			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	7000	1200	0	*
U28			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	8200	4200	0	*
U29			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	2800	4200	0	*
U30			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	2200	1200	0	*
U31			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	2200	4200	0	*
U32			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	4000	2700	0	*
U33			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	4000	7200	0	*
U34			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	1600	7200	0	*
U35			IC 4-BIT SHIFT REGISTER	QM74LS194D4	870	260	18	16	39	0	0	1600	5700	0	*
U36			IC 8-BIT PARALLEL SH REG	QM74LS165D1	870	260	18	16	39	0	0	7600	7200	0	*
U37			ANALOG A TO D CONVERTER		970	260	18	18	39	0	0	7000	7200	0	
U38			IC OP AMPLIFIER	QM308D1	400	260	18	8	39	0	0	8200	6800	0	*
U39			IC HEX INVERTER	QM74LS04P5	770	260	18	14	39	0	0	400	4200	0	*
U40			IC HEX INVERTER	QM74LS04P5	770	260	18	14	39	0	0	4000	5700	0	*
U41			IC HEX INVERTER	QM74LS04P5	770	260	18	14	39	0	0	400	2700	0	*
U42			IC HEX INVERTER	QM74LS04P5	770	260	18	14	39	0	0	5800	2700	0	*
U43			IC TRIPLE 3-IN NOR	QM74LS27P5	770	260	18	14	39	0	0	2200	2700	0	*
U44			IC QUAD 2-IN NAND	QM74LS00P5	770	260	18	14	39	0	0	2200	5700	0	*
U45			IC QUAD 2-IN NAND	QM74LS00P5	770	260	18	14	39	0	0	400	7200	0	*
U46			IC QUAD 2-IN NAND	QM74LS00P5	770	260	18	14	39	0	0	3400	7200	0	*
U47			IC QUAD 2-IN NAND	QM74LS00P5	770	260	18	14	39	0	0	400	5700	0	*
U48			IC QUAD FLIP-FLOP WITH CL BAR	QM74LS175P5	870	260	18	16	39	0	0	1600	2700	0	*
U49			IC QUAD FLIP-FLOP WITH CL	QM74LS175P5	870	260	18	16	39	0	0	3400	1200	0	*

PAGE: 2

Figure 25. Automatic Insertion Report

The component usage report and spare circuit report provide a listing of all components used in the PCB design, and a summary of spare gates, respectively. (Figure 26 provides an example of each type of report.) These reports are use-

ful for verifying the layout, and may suggest chances for reduction or substitution of components.

REPORT DATE: 24AUG82 — PAGE 1 — BOARD NAME: SAMPLOUT

PACK USAGE REPORT

DEVICE DESIGNATION	X	Y	COMPONENT CODE	LOGIC SYMBOL DESIGNATION	LOGIC SYMBOL NAME	CIRCUIT NUMBER
C1	-2.600	1.200	.1UF	C1	CAP	1
C5	-3.000	6.150	.1UF	C5	CAP	1
C6	-0.400	6.150	.1UF	C6	CAP	1
C7	-3.800	1.200	.1UF	C7	CAP	1
C8	-1.600	2.850	.1UF	C8	CAP	1
C9	-5.200	4.500	.1UF	C9	CAP	1
P1	-1.600	0.400	64C-PIN	P1	CONN	1
R1	-2.400	4.450	1.0KY	R1	RES	1
U1	-3.400	1.900	74LS245	S1	P245	1
U2	-4.800	3.550	74LS245	S2	P245	1
U3	-5.400	1.900	2114V2	S10	T2114C	1
U4	-6.000	1.900	2114V2	S11	T2114C	1
U5	-5.400	3.550	2114V2	S12	T2114C	1
U6	-6.000	3.550	2114V2	S13	T2114C	1
U7	-1.000	1.900	7432	SPAR1	OR2	1
				S14	OR2	2
				SPAR2	OR2	3
				SPAR3	OR2	4
U8	-1.000	5.200	74S04	S16	INV	1
				S18	INV	2
				S15	INV	3
				S9	INV	4
				S19	INV	5
				S17	INV	6

REPORT DATE: 24AUG82 — PAGE 1 — BOARD NAME: SAMPLOUT

SPARE CIRCUIT REPORT

LOGIC SYMBOL DESIGNATION	LOGIC SYMBOL NAME	DEVICE DESIGNATION	COMPONENT CODE	SPARE PINS
SPAR1	OR2	U7	7432	1 2 3
SPAR2	OR2	U7	7432	8 9 10
SPAR3	OR2	U7	7432	11 12 13
SPAR4	NAND2	U14	74S37	11 12 13
SPAR5	NAND2	U14	74S37	8 9 10
SPAR6	BUF	U17	7407	10 11
SPAR7	BUF	U17	7407	12 13

Figure 26. Pack Usage/Spare Circuit Report

From/to lists, such as those shown in Figure 27, are automatically ordered both by signal and by component.

REPORT DATE:
27MAY82

PAGE 1
BOARD NAME:
BABRD4

FROM TO LIST

DEVICE DESIGNATION

DEVICE DESIGNATION	SIGNAL	PHYSICAL PIN	LOGICAL PIN	LOGIC SYMBOL NAME	LOGIC SYMBOL DESIGNATION	COMPONENT CODE
C1	#15	1	5	CAP	C1	1.0UFD
	GND	2	4	CAP	C1	1.0UFD
P1	ICH1-	1A	1A	CONN	P1	CON48PIN
	ICH4-	1B	1B	CONN	P1	CON48PIN
	ICH3-	2A	2A	CONN	P1	CON48PIN
	ICH5-	2B	2B	CONN	P1	CON48PIN
	ICH2-	3A	3A	CONN	P1	CON48PIN
	ICH6-	3B	3B	CONN	P1	CON48PIN
	FLDATA	4A	4A	CONN	P1	CON48PIN
	IML0-	4B	4B	CONN	P1	CON48PIN
	ADD4	5A	5A	CONN	P1	CON48PIN
	ICH0-	5B	5B	CONN	P1	CON48PIN
	VALID	6A	6A	CONN	P1	CON48PIN
	IML2-	6B	6B	CONN	P1	CON48PIN
		7A	7A	CONN	P1	CON48PIN
	INTDATA	7B	7B	CONN	P1	CON48PIN
		8A	8A	CONN	P1	CON48PIN
	ISD10-	8B	8B	CONN	P1	CON48PIN
	IML1-	9A	9A	CONN	P1	CON48PIN
	IIUSER	9B	9B	CONN	P1	CON48PIN
	ADD1	10A	10A	CONN	P1	CON48PIN
	#63	10B	10B	CONN	P1	CON48PIN
	#64	11A	11A	CONN	P1	CON48PIN
	#62	11B	11B	CONN	P1	CON48PIN
		12A	12A	CONN	P1	CON48PIN
	ADD3	12B	12B	CONN	P1	CON48PIN
		13A	13A	CONN	P1	CON48PIN
	ADD0	13B	13B	CONN	P1	CON48PIN
	ALOGSIG	14A	14A	CONN	P1	CON48PIN
	IALOG-	14B	14B	CONN	P1	CON48PIN
		15A	15A	CONN	P1	CON48PIN
	ADD2	15B	15B	CONN	P1	CON48PIN
	GND	16A	16A	CONN	P1	CON48PIN
	#5	16B	16B	CONN	P1	CON48PIN
		17A	17A	CONN	P1	CON48PIN
	IBC0-	17B	17B	CONN	P1	CON48PIN
		18A	18A	CONN	P1	CON48PIN
	IBC1-	18B	18B	CONN	P1	CON48PIN
	IBC2-	19A	19A	CONN	P1	CON48PIN
	#65	19B	19B	CONN	P1	CON48PIN
	IBC3-	20A	20A	CONN	P1	CON48PIN
	SP	20B	20B	CONN	P1	CON48PIN
	ALOGATN	21A	21A	CONN	P1	CON48PIN

Figure 27. From/To Lists

3.1.5 COMPONENT DATA BASE

Purpose

The Component Data Base (CDB) contains all the component and symbol data required by the CPS user, and includes facilities that enable the user to control and update the data.

A starter library of approximately 1500 commonly-used components is provided with the system. New components are easily added. As shown in Figure 28, the symbol library contains both gate-level and component-level symbols. It also includes documentation-level symbols, such as sheet borders for schematics. The gate and circuit symbols are cross-mapped to the appropriate component descriptions in the data base, which include electrical and physical descriptions.

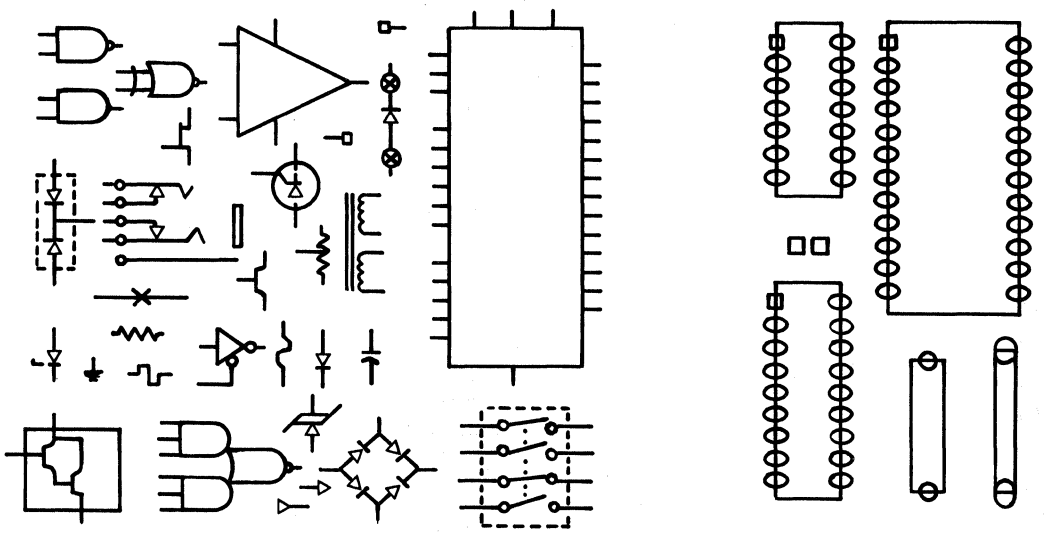


Figure 28. Component Data Base

Functions

The CDB has a flexible design that enables the user to structure it according to the requirements of the organization. The CDB is divided into a corporate data base and a project data base. Depending on the user's needs, the CDB may be further divided into project data bases and individual user data bases. Figure 29 illustrates a typical organization's data base configuration. The corporate data base is generally controlled by a corporate Data Base Administrator, and contains a pool of standard approved components common to all the organization's projects. Project data bases, of which there may be any number, typically contain components that are additional to, or alternatives to, the corporate data base components. Individual CPS users may also require their own data base, for instance during an experimental design development.

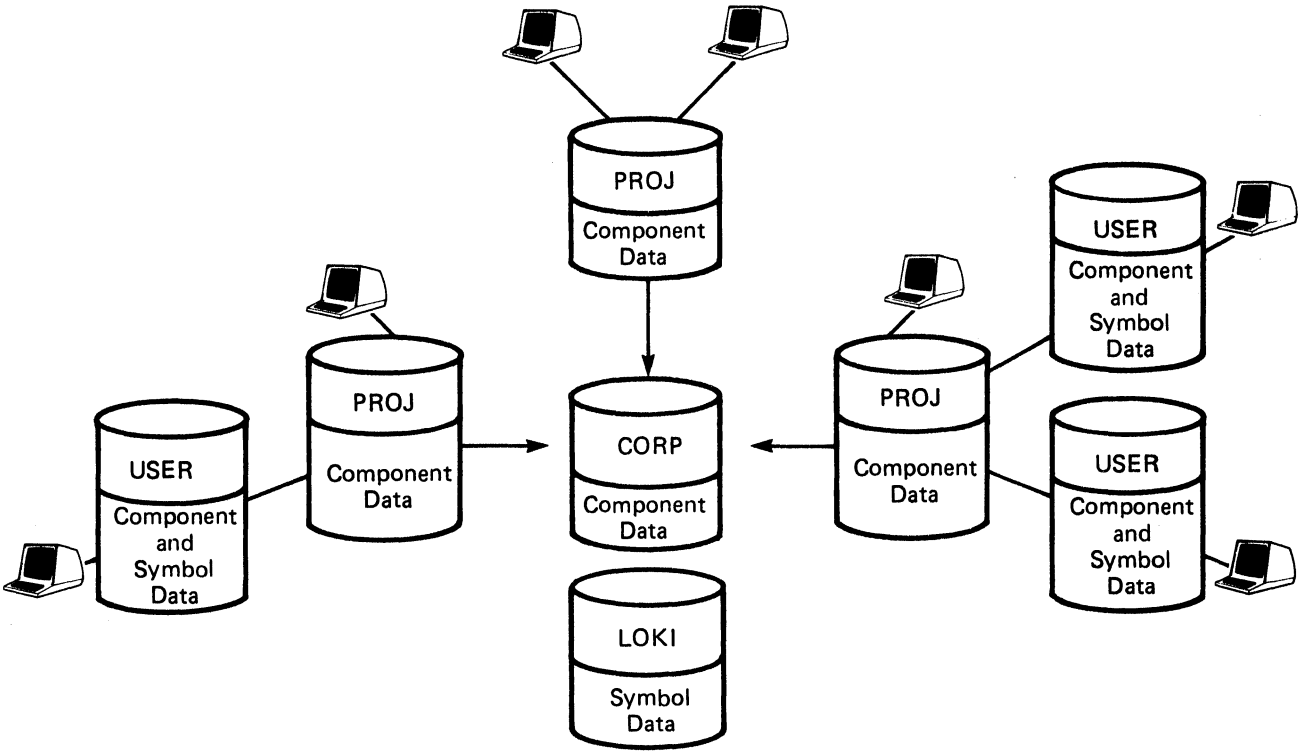


Figure 29. CDB Configuration

The CDB control facility provides the Data Base Administrator with interactive functions that enable:

- the development or modification of symbol and component data
- the control of data base access
- version control for symbols and components
- the production of reports for administrators or users.

In addition to the interactive functions, the administrator can develop sets of functions. These sets can be stored for frequent automatic execution, eliminating the repetitive tasks of data base administration.

The administrator can add new components to the data base, modify existing components, or 'retire' out-dated ones. The CDB provides functions that enable the administrator to view symbols on the graphics screen. As shown in Figure 30, special display techniques are used to identify each element of the component and the symbol. A special feature of the LOKI system enables the user to develop a new symbol using interactive graphics. Figure 31 illustrates a screen display during the process of creating symbol graphics.

Data base access can be carefully controlled, according to the requirements of the organization. The CDB maintains a concept of user privileges, so that the administrator can determine each user's level of access. For example, some users can only obtain information from the CDB, others are able to add data, etc.

Other aspects of data base usage are controlled by built-in validation facilities. For example, a LOKI user is prevented from using a schematic symbol that is invalid for the component to be used in the SPRIG PCB layout.

Version control may be applied to each component in the data base. This facility enables the user to store information related to outdated or experimental versions of a component within the same data base as the information for current versions.

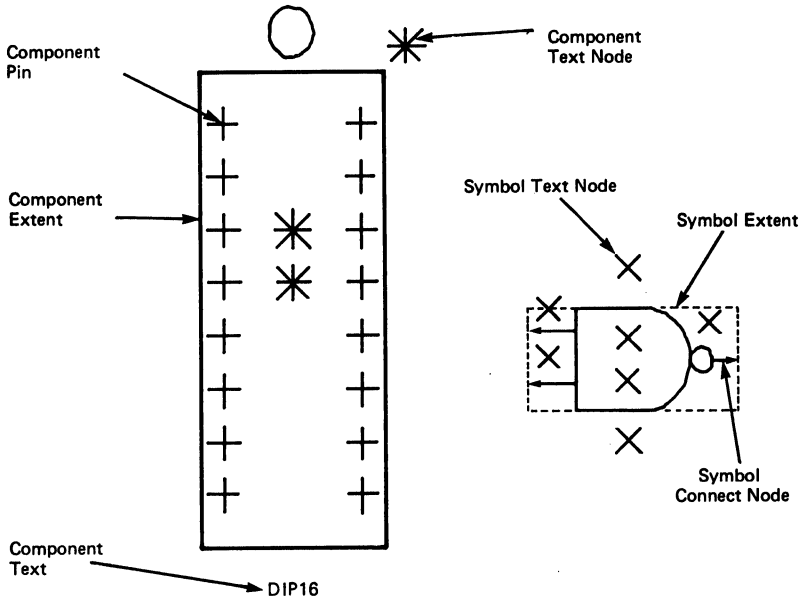


Figure 30. CDB Display Techniques

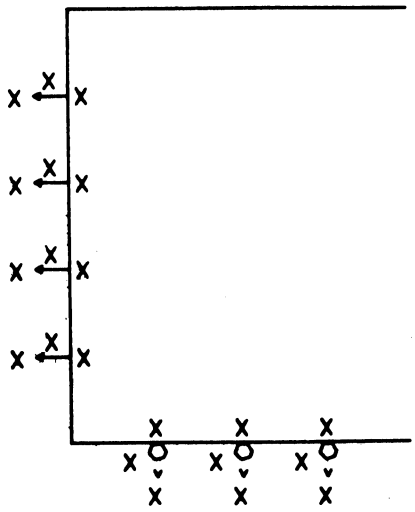


Figure 31. Symbol Development

The administrator can produce various types of reports, any of which may be created for the corporate data base or a project or user data base. These reports include:

- a listing of all the components in that data base (including each version, if the component has more than one)
- a report on the electrical/logical descriptions of each component
- a report summarizing the physical descriptions of the components in the data base.

Figure 32 illustrates a sample of a CDB component report.

```
FILE: CSCANV   PROJ     A   BNR CBDS PROJECT..VM SIPO/E                                    PAGE 001

                                        COMPONENTS IN STARTER PROJ DATABASE

CODE                    NOTETEXT
                        CPCCODE      SUPPLIER                    SUPLCODE
                VERSION VSTATUS VAPPROVE LPNTR        MPNTR      GPNTR      VERTEXT
-------------------------------------------------------------------------------------------------------

.00511UFS           --> CAP PS 5110PF 400V 2%

        VERSION       C              EQVC00080   PHYS00160   A14A       INITIAL VERSION
        VERSION 1     C              EQVC00080   PHYS00665   A13B       ALT VERSION CAP, SPAN 1300

.01UF               --> CAP CER .01UF 50V 10%

        VERSION       C              EQVC00080   PHYS00008   A065A      INITIAL VERSION
        VERSION 1     C              EQVC00080   PHYS00139   A060A      ALT VERSION CAP, SPAN 600

.01UFA              --> CAP PS .01UF 100V 1%

        VERSION       C              EQVC00080   PHYS00159   A10B       INITIAL VERSION

.01UFJJ             --> CAP PE .01UF 100V 10%

        VERSION 1     C              EQVC00080   PHYS00736   A09A       STD B214 SYMBOL CAP, SPAN 900, MTD NARROW
        VERSION 2     C              EQVC00080   PHYS00737   A09D       ALT VERSION CAP, SPAN 900, MTD WIDE

.01UFP              --> CAP PP .01UF 100V 1%

        VERSION       C              EQVC00080   PHYS00502   A10A       STD B214 SYMBOL CAP,PREF SPAN 1.000

.01UK               --> CAP CER .01UF 100V 20% (.01UFK)

        VERSION       C              EQVC00080   PHYS00008   A065A      INITIAL VERSION
        VERSION 1     C              EQVC00080   PHYS00139   A060A      ALT VERSION CAP, SPAN 600

.012MFDK            --> CAP CER .012UF 50V 10%

        VERSION       C              EQVC00080   PHYS00139   A060A      STD B214 SYMBOL CAP, SPAN 600

.015UFK             --> CAP CER .015UF 50V 10%

        VERSION       C              EQVC00080   PHYS00139   A060A      STD B214 SYMBOL CAP, SPAN 600

.0165UFA            --> CAP PS .0165UF 100V 1%
```

Figure 32. CDB Component Report

3.2 DESIGN VERIFICATION SYSTEM

3.2.1 PURPOSE

The Design Verification System (DVS) is used to evaluate logic design and to generate test data for PCBs. DVS enables users to evaluate designs rapidly and efficiently, and reduces or eliminates the need for prototype boards.

DVS can simulate digital circuits with up to 32 000 gates. The DVS libraries include a wide variety of gate primitives with which the user can generate logic circuits, ranging from simple inverters, NANDs, and NORs, to flip-flops and RAM/ROM memory elements. DVS performs its analysis in six logic states: zero, one, unknown, high impedance, rising, and falling. The designer is able to specify minimum and maximum delay values for 'rise' and 'fall' logic transitions.

3.2.2 FUNCTIONS

The designer can use DVS in four aspects of the design process:

- conceptual logic verification
- completed design verification
- fault simulation
- logic documentation.

At the initial design phase, the designer is able to check new or critical circuits by simulation, before they are incorporated into the total PCB design. At this early stage, a circuit can be redesigned and components replaced without delay or capital investment. In addition, DVS provides 'worst-case' timing simulation that enables the user to assess the circuit's ability to handle the specified processing rate. (This information cannot be directly assessed by testing a hardware prototype.)

At the second phase of design verification, circuits are assembled and components identified to form the complete design. DVS is used to simulate the inputs received by the circuit, and to monitor the resulting output responses to verify that the circuit meets design specifications. For design verification, accurate timing is essential. With

DVS, exact delays can be specified, and hazards and races are detected automatically.

At the production level, DVS produces test patterns to detect faulty components and wiring. The user may create test data interactively, or generate test patterns automatically with DVS facilities.

DVS also has a fault simulation mode that emulates potential faults and verifies that test data can detect them. Over 1000 faults can be simulated at one time due to a special parallel simulation technique designed for DVS. DVS detects and reports hazard (race) conditions, and provides reports of detected and undetected faults. (Figures 33 and 34 provide samples of these reports.)

********** HAZARD FILE **********

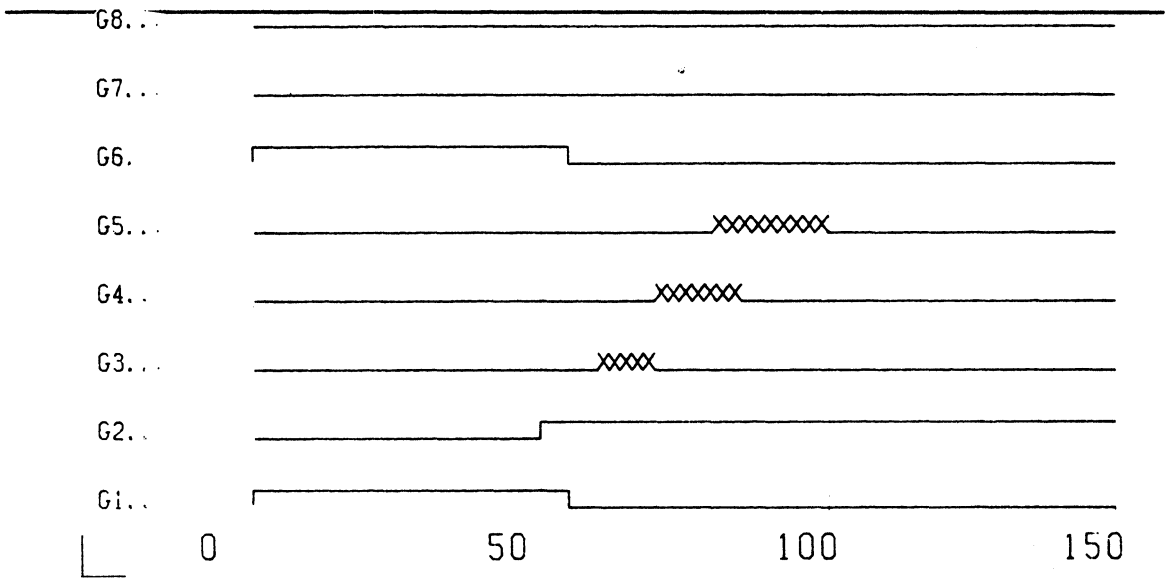
TIME	GATE TYPE	NAME
84726	NAND	#376 U57-12
94526	NAND	#1175 U54-15
347256	NAND	#1769 UD9-9
356930	NAND	#1191 U55-10
357036	NAND	#2052 UD9-5
357036	NAND	#1200 U56-10
357055	NAND	#2049 UD9-6
697176	NAND	#1769 UD9-9
706850	NAND	#1191 U55-10
706956	NAND	#2052 UD9-5
706956	NAND	#1200 U56-10
706975	NAND	#2049 UD9-6

Figure 33. Hazard Report

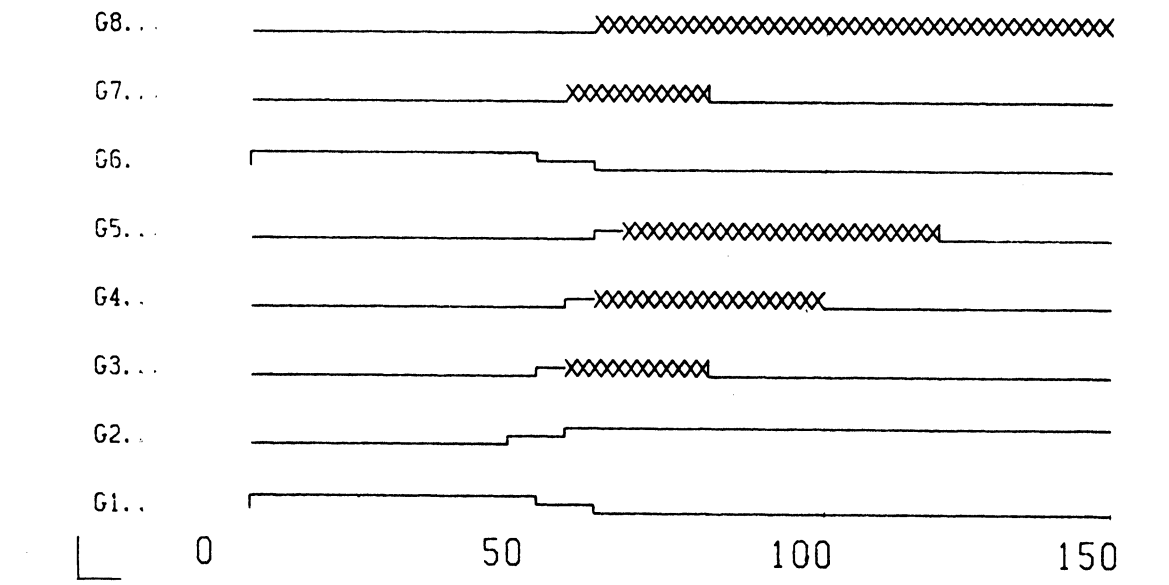
```
TIME -VECT- AIGATE -- FAULT

  1030        Q16         S1        OUTPUT SA1 DETECTED
  1030        Q16         Q16       OUTPUT SA1 DETECTED
  1030        Q15         Q15       OUTPUT SA1 DETECTED
  1030        Q14         Q14       OUTPUT SA1 DETECTED
  1030        Q13         Q13       OUTPUT SA1 DETECTED
  1030        Q12         Q12       OUTPUT SA1 DETECTED
  1030        Q11         Q11       OUTPUT SA1 DETECTED
  1030        Q10         Q10       OUTPUT SA1 DETECTED
  1030        Q9          Q9        OUTPUT SA1 DETECTED
  1030        Q8          Q8        OUTPUT SA1 DETECTED
  1030        Q7          Q7        OUTPUT SA1 DETECTED
  1030        Q6          Q6        OUTPUT SA1 DETECTED

 UNDETECTED FAULTS:

D16       OUTPUT SA1
D15       OUTPUT SA1
D14       OUTPUT SA1
D13       OUTPUT SA1
D12       OUTPUT SA1
D11       OUTPUT SA1
D10       OUTPUT SA1
D9        OUTPUT SA1
D8        OUTPUT SA1
D7        OUTPUT SA1
D6        OUTPUT SA1
D5        OUTPUT SA1
D4        OUTPUT SA1
D3        OUTPUT SA1
D2        OUTPUT SA1
D1        OUTPUT SA1
CLOCK     OUTPUT SA1
CLOCK     OUTPUT SA0
D17       OUTPUT SA1
SO        OUTPUT SA0
SO        OUTPUT SA1

TOTAL NUMBER OF FAULTS SIMULATED =   172       4 STATE
NUMBER OF FAULTS DETECTED        =   143  ( 83%)
NUMBER DROPPED FROM SIMULATION   =     0  (  0%)
NUMBER OF FAULTS UNDETECTED      =    29  ( 16%)
```

Figure 34. Fault Report

DVS adds valuable information to the design documentation through signal state tables and waveforms. Figures 35 and 36 illustrate typical examples of these outputs. The waveforms can be displayed on the graphics screen or output to a plotter.



Nominal-delay Analysis



Worst-case Analysis

Figure 35. Signal Waveforms

The signal state tables can be viewed at the terminal or printed for subsequent study.

	TIME	SWI CLOCK	SWI S1	SWI S0	QOUT			
*	0	0	0	0	XXXX	XXXX	XXXX	XXXX
	200	---1	0	0	XXXX	XXXX	XXXX	XXXX
	258	---1	0	0	0XXX	XXXX	XXXX	XXX0
	260	---1	0	0	0000	0000	0000	0000
	400	0	---1	0	0000	0000	0000	0000
	600	---1	---1	0	0000	0000	0000	0000
	670	---1	---1	0	1000	0000	0000	0001
	673	---1	---1	0	1111	1111	1111	1111
	800	0	---1	---1	1111	1111	1111	1111
	850	---1	---1	---1	1111	1111	1111	1111
	900	0	---1	---1	1111	1111	1111	1111
	950	---1	---1	---1	1111	1111	1111	1111
	1000	0	---1	---1	1111	1111	1111	1111
	1005	0	---1	---1	1111	1111	1111	1110
	1050	---1	---1	---1	1111	1111	1111	1110
	1100	0	---1	---1	1111	1111	1111	1110
	1110	0	---1	---1	1111	1111	1111	1100
	1150	---1	---1	---1	1111	1111	1111	1100
	1200	0	---1	---1	1111	1111	1111	1100
	1210	0	---1	---1	1111	1111	1111	1000
	1250	---1	---1	---1	1111	1111	1111	1000
	1300	0	---1	---1	1111	1111	1111	1000
	1310	0	---1	---1	1111	1111	1111	0000
	1350	---1	---1	---1	1111	1111	1111	0000
	1400	0	---1	---1	1111	1111	1111	0000
	1410	0	---1	---1	1111	1111	1110	0000
	1450	---1	---1	---1	1111	1111	1110	0000
	1500	0	---1	---1	1111	1111	1110	0000
	1510	0	---1	---1	1111	1111	1100	0000
	1550	---1	---1	---1	1111	1111	1100	0000
	1600	0	---1	---1	1111	1111	1100	0000
	1610	0	---1	---1	1111	1111	1000	0000
	1650	---1	---1	---1	1111	1111	1000	0000
	1700	0	---1	---1	1111	1111	1000	0000
	1710	0	---1	---1	1111	1111	0000	0000
	1750	---1	---1	---1	1111	1111	0000	0000
	1800	0	---1	---1	1111	1111	0000	0000

Figure 36. Signal State Table

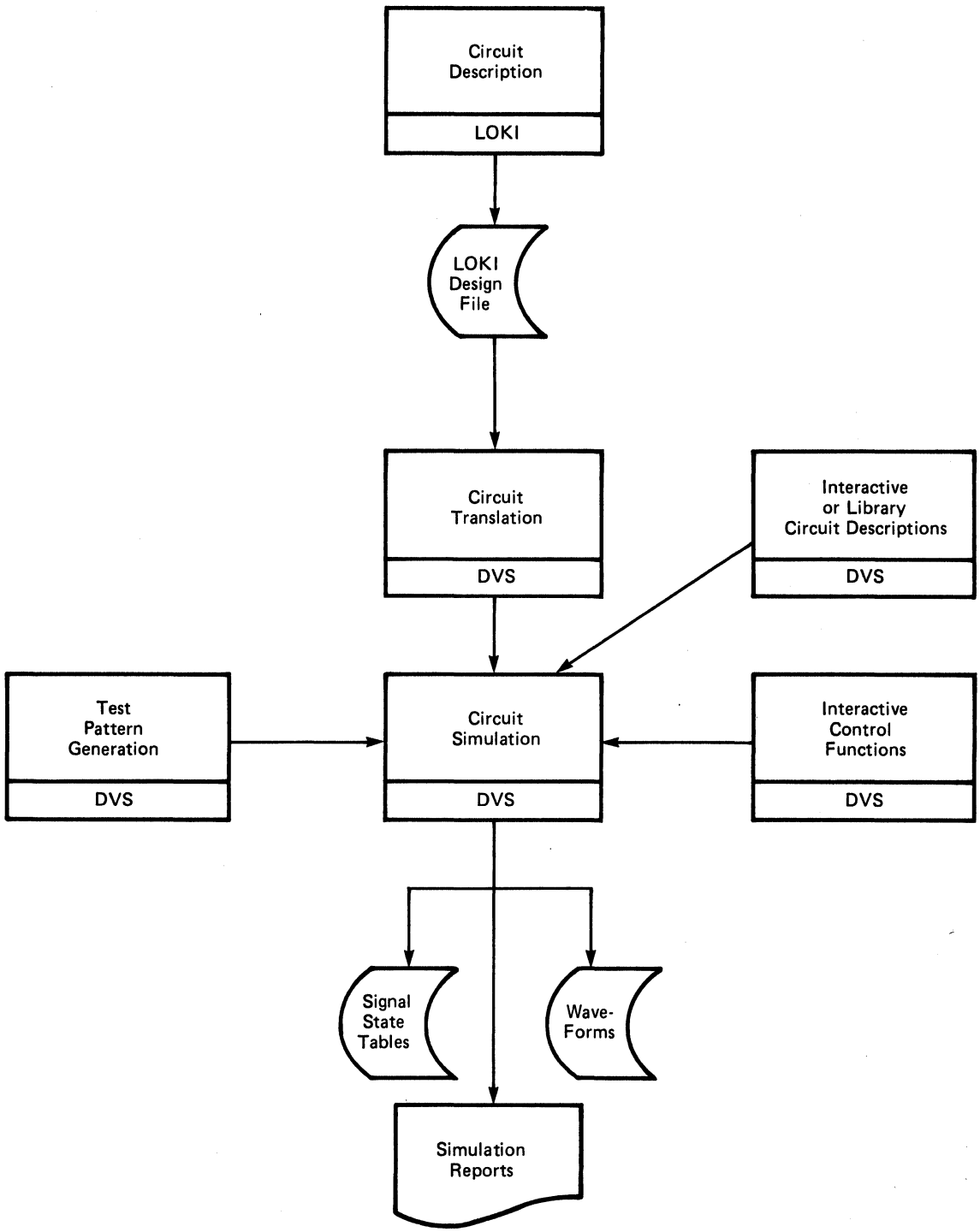


Figure 37. Simulation Process

In the process of circuit simulation, the circuit designer provides DVS with three types of information. The first is the circuit description, which can be specified through interactive functions, or by the LOKI design file. In the latter case, DVS takes the circuit layout and the component information from the LOKI design file, as shown in Figure 37.

If a LOKI design file is not available, DVS provides another method of avoiding the time-consuming process of describing the circuit at gate level. DVS contains libraries of circuit descriptions for commonly-used components, which can be easily accessed by the designer.

The second type of information produced by the designer is a set of stimulus vectors to 'drive' the circuit. The circuit is tested by applying a defined sequence of input pulses. DVS provides several methods of generating these test patterns, both interactive and automatic.

The final type of information provided by the designer is specifications to control the simulation and define the outputs required. DVS provides interactive functions that can be used to define the signals to be displayed and the time range involved. Other functions enable the designer to pre-set gates, access the libraries of circuit descriptions, specify and manipulate gate delay spreads, and interrupt the simulation process. The designer can store the status of the simulation process at any time and resume processing in a subsequent terminal session.

4. SYSTEM REQUIREMENTS

4.1 CONFIGURATION

4.1.1 BASIC REQUIREMENTS

The minimum machine requirements for CBDS are:

- IBM 4331 Model K11, 370/148 Model K, or IBM 3031
- Two IBM 3370 Model A1 direct access storage devices or equivalent
- One 9-Track Tape Drive 1600 bpi or greater (an 800 bpi option may be required to drive some photoplotters)
- One 3277 Model 2 Display Station with program function keys and the IBM 3277 Graphics Attachment RPQ 7H0284 (this includes the joystick attachment)
- one storage display monitor, such as the Tektronix* 618
- One 3274 Display Control Unit
- One IBM 3262 Model 1 Line Printer or equivalent.

4.1.2 ADDITIONAL CAPACITY

CBDS is designed to be incrementally expandable. Additional workstations, direct access storage devices, memory, or CPU power may be added as desired.

Plotter

A plotter is recommended for hard-copy output, such as schematics from the Schematic Layout system, and artwork check plots from the Physical Layout or Manufacturing Data Generation systems. Signal waveforms produced with the Design

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Verification System can also require hard-copy plotting. Direct support is provided for CalComp* model 960 (with 906 controller).

Digitizer

An organization that wishes to convert manual PCB layouts into CBDS design files can use a digitizing table to capture the existing physical data for the Physical Layout system. The current implementation of CBDS supports CalComp 9000 series* digitizers.

Photoplotter

Photoplotter output from CBDS is provided in three formats:

- ANSI/IPC-D-350B as approved by the American National Standards Institute and the Institute for Interconnecting and Packaging Electronic Circuits
- Gerber** format, conforming to EIA standard RS-274-C.

Paper Tape

Paper Tape output generated by CBDS is compatible with the REMEX+ paper tape punch. Drill tape output is according to the format described by Advance Controls Corporation in the Trudril++ Programming manual document number CSM0023. The tape code is EIA standard RS-2440.

---

* Registered Trademark of California Computer Products, Inc.
** Gerber Inc.
+ REMEX Ltd.
++ Advanced Controls Corporation (a Subsidiary of Cooper Industries)

4.2 PROGRAMMING CONSIDERATIONS

The CBDS programs are written in FORTRAN H Extended and IBM Assembler language. They were designed and tested in the following VM/370 CMS environments:

- VM/370 Release 6 with BSEPP
- VM/SP Release 1.1.

The following components are required for the system's operation:

1. FORTRAN IV (5734-LM3)

   optionally, the FORTRAN H Extended and Enhanced MOD II Library (5796-PKR) may be added.

2. IBM 3277 Graphics Attachment Support Programming for PRPQ P09013 (5799-AXX).

Subsequent versions or releases of the above IBM program offerings may affect the functioning of the CBDS programs.

4.3 CAPACITY

Table 2 provides a rough estimate of the number of users handled by various computers and memory capacities. (In all cases, the number of users may vary depending on the nature of the work being performed.)

Table 2: User Capacity

COMPUTER	NUMBER OF USERS
IBM 4331 Group 11 (2M bytes)	2
IBM 4331 Group 2 (4M bytes)	4
IBM 4341 Group 1 or 10 (4M bytes)	4-6
IBM 4341 Group 11 (8M bytes)	6-8
IBM 4341 Group 2 (8M bytes)	8-10
IBM 4341 Group 2 (16M bytes)	16-20

5. DATA MANAGEMENT

5.1 INTRODUCTION

The management of data within CBDS involves two basic types of information: component data and design data.

Component data is centrally controlled and coordinated through the Component Data Base (CDB) of the Circuit Pack System (CPS).

Design data, which is the documentation of each PCB design created with CBDS, is maintained in the form of a design file.

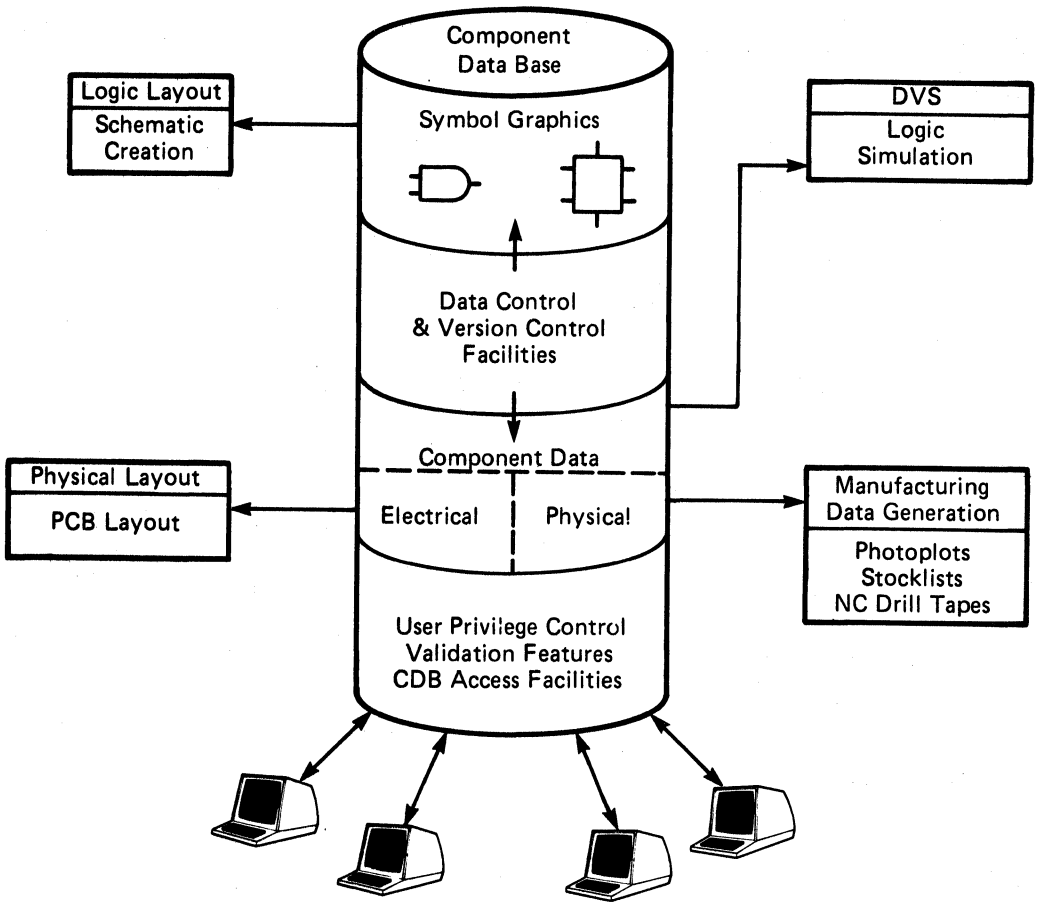

Figure 38. Component Data Management

5.2 COMPONENT DATA MANAGEMENT

5.2.1 COMPONENT DATA BASE

Component data, which includes symbol graphics as well as physical and electrical component descriptions, is centrally created and controlled with the CDB. From the CDB, symbol and component data is available to all the other systems of CPS, and the facilities of DVS that require component data. Figure 38 illustrates the access to CDB data required by CBDS modules.

The CDB combines a flexible data base structure with rigid data control facilities in an easy-to-maintain environment:

- the CDB can be divided into corporate, project, and user data bases, depending on the requirements of the organization, in order to facilitate rapid access to information
- the CDB provides version control facilities that enable simultaneous availability of out-dated, current, and experimental versions of a single component
- access to the CDB control facilities can be carefully monitored through the assignment of user priority levels
- the starter libraries provided with CBDS (approximately 1500 commonly-used symbols and components) can be easily added to, or modified, with the interactive CDB control facilities
- built-in verification features ensure that user-defined data validation rules are maintained
- the CDB provides facilities that enable the repetitive tasks of data base management to be performed automatically
- report production features can be used to provide component information for system users.

Special CDB functions are provided for application programmers who are developing software to access the CDB. These functions are particularly useful during the creation of user-defined systems tailored to interface with CBDS, or during modification of a CBDS system for a special user application.

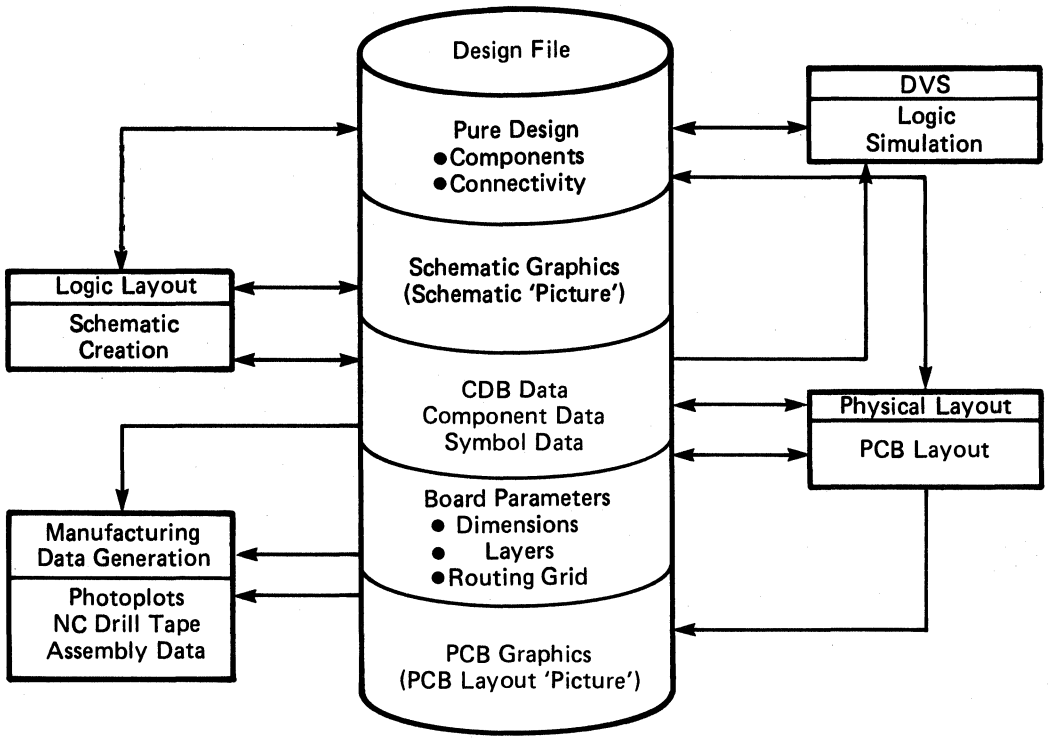

Figure 39. CBDS Design File

5.3 DESIGN DATA MANAGEMENT

5.3.1 INTRODUCTION

The basis of design data management in CDBS is the documentation of each PCB in a design file. The design file is the primary method of communication among the CBDS sub-systems, and provides the basis for the internal data base of each CPS module.

5.3.2 DESIGN FILE

The design file concept provides a fundamental method of passing PCB design information among the CBDS modular functions. Due to its computer-independent structure and content, the design file provides a software-independent format for the transfer of design data both within and outside CBDS.

Within CBDS, each function automatically extracts the data it requires from the design file and formats it into an internal data base that best suits its purpose in terms of optimization and efficiency.

Similarly, the Schematic Layout and Physical Layout systems convert the information they create into the design file format for subsequent transfer to other modules. Figure 39 illustrates the basic content of the design file and the portions of the file used and created by each CBDS module.

New user-designed modules, or interfaces with related systems, can be designed with similar techniques to take advantage of the design file's independent format.

5.3.3 MODULAR DATA BASES

Each CPS module (Schematic Layout, Physical Layout, and Manufacturing Data Generation) creates an internal base for its aspect of the PCB design. These internal data bases, which are generally referred to as work files, are based on information taken from the design file, and are added to by each system. (For example, the Physical Layout work file is based on the design file from the Schematic Layout module, and automatically accummlates the data created during PCB

layout). When the function of the system is completed, the information in the work file is converted back to design file format and passed to the next CPS system.

A special system of work file back-up is provided to protect against loss of data. This capability, which is common to all the CPS modules, ensures that the user can control the storage of work files and is able to retrieve a back-up copy of the data base if necessary.

5.3.4 DATA FILES

In addition to the design file and work files, each CBDS module produces (or uses) several data files, which have a variety of functions. Some data files may be input to a module as a rapid method of data entry. Other files are produced by the module as control or audit methods. Some are report files, and others (such as the Manufacturing Data Generation output files) provide an interface with production systems.

Circuit Board Design System 2 5796-PRP , 5796-PRL
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G320-9175-0

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