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IBM 9020D/E DATA PROCESSING SYSTEM

FACTORY AND FIELD ACCEPTANCE

TEST SPECIFICATION

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INTERNATIONAL BUSINESS MACHINES CORPORATION

INTRODUCTION

This specification is submitted to the Federal Aviation Administration by the International Business Machines Corporation in compliance with Paragraph 3.11.8 of Specification FAA-ER-606-063 and applicable amendments thereof, Specification FAA-ER-NS-100-1, and Contract No. FA64WA-5223.

The tests recommended in this specification, in conformance to the FAA approved check list, are intended to demonstrate that the equipment meets the requirements of applicable sections of the above mentioned Specifications, Amendments and Contract.

The Factory Acceptance Test will be conducted at the IBM Systems Manufacturing Division facility in Kingston, New York. The Field Acceptance Test will be conducted at the field location after equipment installation.

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1.0 SCOPE OF TESTS

The recommended Acceptance Tests are designed to demonstrate the Unit Functional, and Integrated System Functional operation of all 9020D/E System elements and units. The tests demonstrate the system capability, versatility, and support functions. The test sections are as follows:

Unit Functional Tests
Subsystem Functional Tests
System Functional Tests
Power and Battery Test
Factory Acceptance Exercise

1.1 Test Programs

The test programs used for the Acceptance Tests are, in most cases, the same programs that will be used for maintenance of the 9020D/E System. Appendix E provides a cross reference of test program numbers to test specification sections for all programs used in the Acceptance Test. The program write-up and flow diagram for all Off-Line Maintenance programs are contained in the IBM 9020D/E Data Processing System Maintenance Diagnostic Programs Manual(s) as outlined in Appendix J. Programs used for the switch demonstrations are included in the switch procedures of this specification.

1.2 Test Configuration

The various equipment configurations required for the Acceptance Tests are stated in each test description. For convenience the defined minimum is given below as a standard reference for most functional tests.

The defined minimum system configuration is as follows:

9020D
- 1 Computing Element
- 1 Storage Element
- 1 I/O Control Element
- 1 Peripheral Adapter Module with 1052 Printer Keyboard
- 1 Tape Control Unit with Tape Drives
- 1 Storage Control Unit with Disk Storage Unit

9020E
- 1 Computing Element with 1052 Printer Keyboard
- 1 Storage Element
- 1 Display Element
- 1 I/O Control Element
- 1 Tape Control Unit with Tape Drive
- 1 DAU
- 1 RCU

The defined minimum configuration does not include the redundant elements and units, System Console (9020D), Configuration Console (9020E) with 1052 Printer Keyboard, and 2821 Control Unit and Read/Punch and Printer, but these elements and units are used with the configuration as required.

All reconfiguration of equipment is done manually unless specifically stated otherwise.

To assist the FAA observers in identifying the elements and units of each test configuration, a 9020D/E System floor diagram is provided in Appendix G for the Factory Acceptance Test, and in Appendix H for the Field Acceptance Test. The use of these diagrams, in conjunction with the Equipment Identification List provided at each Acceptance Test, will give a positive identification of each 9020D/E System Element and Unit. An example of this equipment Identification List format is given in Appendix J.

1.3 Acceptance Test Schedule

The Factory Acceptance Test Schedule, Appendix A, and Field Acceptance Test Schedule, Appendix B, list the sequence and specifies the tests to be performed during the Factory and Field Acceptance Tests. However, if the next scheduled test, or portion thereof, must be delayed due to a temporary system configuration, the schedule will be changed to insure a continuous sequence of testing.

The acceptance tests will be preceded by a familiarization and orientation period to review with the FAA observers the test specification procedures and agreements, and to become acquainted with the test facility, equipment layout, and IBM personnel. Serial numbers of the equipment to be tested will be recorded at this time on the form illustrated in Appendix J.

2.0 ACCEPTANCE TEST REQUIREMENTS

Requirements of the Acceptance Test that concern personnel, test certification, quality assurance, specification changes, and allowable maintenance are described in the following sections.

2.1 General (Ref. ER 063-4.1)

All acceptance tests will be performed by IBM personnel and witnessed by the FAA; however, the FAA has the right to waive witnessing of tests or any part thereof. IBM will furnish certified test data showing the results of all such tests. The Acceptance Test Report derived from the test data sheets will be submitted to the FAA within thirty days after completion of the tests.

2.2 Quality Inspection (Ref. ER 063-4.2.2 and 4.2.2.1)

All 9020D/E System equipment and field location cables have been inspected and certified by IBM Quality Control prior to the Factory Acceptance Test. Therefore, no extensive period of time for a FAA Quality Control inspection has been included in the 9020D/E System Acceptance Test schedule. Certified IBM Quality Control reports should fulfill the acceptance test quality control requirements, however, the FAA may perform an inspection if so desired after system power has dropped in the System EPO test, Chapter 7. Quality Control personnel, upon request from the FAA, will make available for review at the Kingston plant, information regarding the quality status and/or specifications relating to the IBM 9020D/E System. Quality Control requirements not satisfied during the Factory Acceptance Test may be reinspected during the Field Acceptance Test.

2.3 Test Recording (Ref. ER 063-4.2.6)

Acceptance Test data will be recorded on the Unit Functional and System Functional Test Data Record forms. The forms permit recording of the specific test name, date, data record number, location, configuration, results, failure information, and certification. A Test Data Record Comment Sheet is used with the Test Data Record forms to provide sufficient space for test comments. An Acceptance Test Log is used to record the running time of the tests, system usage, system operation, failure data, and comments. An illustration of each form is contained in Appendix L with a brief description of each recording area. IBM will provide information as required for inclusion into these logs.

2.4 Acceptance Test Specification Changes

Changes to the FAA approved Acceptance Test Specification must have approval of the FAA. Approval of such changes is requested within two weeks after receipt of the change notice.

2.5 Scheduled Maintenance (Ref. ER 063-3.8.2.2.2.1)

The scheduled maintenance allowed during the acceptance tests will include normal preventive maintenance, normal routine maintenance and corrective maintenance. A description of each type of maintenance, and the time requirements for each during the acceptance tests, are as follows:

a) Normal preventive maintenance is the planned marginal and functional testing of the system components and control features. Since such maintenance will be performed prior to the acceptance tests, no time is requested.

b) Normal routine maintenance is the regular repair, adjustment and cleaning of system components.

c) Corrective maintenance is the repair of system components and control features during a period when the failing element or unit is not part of the active configuration, and is not available for redundancy. Corrective maintenance will, when required, utilize redundant elements and units to perform needed trouble isolation and/or repair. Corrective maintenance is requested on an as required basis.

d) Program corrective maintenance will be allowed. Scheduling of necessary time and equipment will be mutually agreed to by IBM and FAA personnel.

3.0 TEST ACCEPTANCE

The acceptance or rejection of each test shall be determined by the acceptance conditions and/or results stated in each test procedure, and the pass/fail criteria stated for the tests of that section. Refer to Section 3.1 for the test criteria of the section or sections involved.

Upon completion of each test, the FAA observer will certify the results of the test on the appropriate test data record forms. Tests which require a subsequent rerun will have an additional test data record completed for each test rerun, with a reference made to the previous data record form of that test.

By mutual agreement, the FAA and IBM may discontinue testing.

3.1 Acceptance Test Pass/Fail Criteria

3.1.1 Functional Test Criteria. The functional tests include the following sections:

5.1.1 thru 5.2.15
6.1.1 thru 6.1.4
7.1 thru 7.5

A functional test will be considered acceptable if the initial test pass is successful as given in the test description. If this initial test pass fails, the failing portions of the test will be repeated immediately to determine if the failure is a transient or a solid malfunction.

If the failure is determined to be a transient, the failing portions of the test will be repeated up to five additional passes, at the discretion of the FAA observer. The test will be considered acceptable upon the successful completion of the repeated passes.

If a malfunction has occurred, the element or unit will be repaired prior to a rerun of the failing test. At the discretion of the FAA observer, the rerun will consists of up to five consecutive passes of the failing portions of the test and any previously untested portions of the test. The test will be considered acceptable upon successful completion of the rerun passes.

3.1.2 SEVA Field Test Criteria. The SEVA field test consists of a twelve (12) hour integrated system test, Section 6.2.1.

The SEVA field test will be considered acceptable when the system configuration has successfully cycled the SEVA program for 12 hours of which a minimum of five consecutive hours must be achieved without malfunction, exclusive of certain tape drive and Disk Storage Module failures. Tape drive and Disk Storage Module failures corrected by mechanical or electrical adjustments will not be considered a disruption of the five consecutive hour criteria. At those times when redundant elements or units are not required for use as part of a maintenance subsystem, they will be included in the active system configuration; however, at any time no more than one-third (1/3) of the total number of magnetic tape drives (no less than one) and one-third (1/3) of the total number of Disk Storage Modules (no less than one) undergoing acceptance will be included in the active system configuration. At the FAA Test Director's discretion, a 1052, and a 2821 Control Unit and associated Card Reader/Punch and/or 1403 Printer may be exercised for two passes of SEVA at the beginning of every four hours and prior to the end of the test.

SEVA will be executed in the Process mode unless it is mutually agreed by the FAA and IBM to operate in the Hard Stop mode. If SEVA encounters a failure, a restart is to be tried. With proper operator intervention, five reruns of the failing pass of SEVA will be immediately tried. Successful completion of these reruns classifies the failure as a transient. The rerun time will be counted toward the required test time. An identical failure during any of these reruns causes the failure to be classified as a malfunction and necessary repair action is taken. The rerun time in this case will not be considered test time. Repair time will not start until the failing element is made available for maintenance. Should this failure recur during the test after the repaired element/unit has been returned to the system, the necessary repair action will be taken, but the failure will be classified as a transient.

For a Duplex or Triplex, if a malfunction occurs, an A-1 Equipment Mode configuration must be available for the active system for the test to continue. If a redundant element or unit is not available for reconfiguration, the 12-hour period will be restarted after the failing elements or units have been repaired.

For a Simplex, the SEVA test will be performed on the active system for a 12-hour period. If a malfunction occurs, the test will be stopped and test time will continue after the repair is completed. An element/unit requiring in excess of three hours to repair will require five consecutive malfunction free hours of operation on that element/unit after the repair.

3.1.3 Special System Test Criteria. The special system tests consisting of the Eight Timed Sample Problems, Display Instruction Performance Test, FLT Practical Demonstration, 360 Mode Recall, and System/360-9020D/E Compatibility, will be considered acceptable when the actual results obtained

and the predicted results, as specified for each test, agree. (Ref. Section 6.0).

If a failure occurs during the run or the actual results and predicted results do not agree, the test will be repeated immediately to determine if the failure was due to a malfunction or a transient.

If the failure was due to a transient condition and the results of the test agree with the predicted results, the test will be considered acceptable. However, if the failure was due to a malfunction, the element or unit will be repaired prior to a rerun of the failing test. If the rerun is successful and the results agree, the test will be considered acceptable. However, if the rerun is not successful or the results do not agree, that test will be considered as failed.

3.1.4 Factory SEVA Acceptance Exercise Criteria. The Factory SEVA acceptance exercise includes a 48 to 120 hour system test. (Section 8).

The exercise will consist of two to five consecutive 24-hour periods, during each of which SEVA will cycle in the A-1 Equipment Mode, with no more than one-third (1/3) of the total number of magnetic tape drives (no less than one) and one-third 1/3 of the total number of Disk Storage Modules (no less than one) under-going acceptance included in the active system configuration. At the FAA Test Director's discretion, a 2821 Control Unit and associated 2540 Card/Read Punch and/or 1403 Printer may be exercised for 2 passes every 8 hours, and prior to the end of the test.

The system will be operating in the A-1 Equipment Mode during the acceptance exercise periods when margins are applied. However, the total marginal check requirements of 6 hours of positive margins and 6 hours of negative margins may be an aggregate of several periods due to the scheduling of equipment periods, the unavailability of redundant elements or units, or by IBM exercising the option to remove margins.

A failure occuring during a marginal check period will be handled the same as other A-1 Equipment Mode periods, except that margins may be removed at any time, and if the system is capable of running without margins, the exercise will continue. The duration of the marginal check period prior to the failure will be counted toward the aggregate marginal check requirements.

The time to reconfigure the system during the exercise will not exceed 15 minutes and will be counted towards the 48 to 120 hour period. The time required to apply margins will be counted toward the aggregate marginal check requirements if the margins are applied within 15 minutes. However,

if the margins set up time exceeds 15 minutes, the set up time will count only towards the non-marginal requirements.

SEVA will be executed in the Process mode unless it is mutually agreed by the FAA and IBM to operate in the Hard Stop mode. If SEVA encounters a failure, a restart is to be tried. With proper operator intervention, five reruns of the failing pass of SEVA will be immediately tried. Successful completion of these reruns classifies the failure as a transient. The rerun time will be counted toward the required test time. An identical failure of any of these reruns causes the failure to be classified as a malfunction and necessary repair action taken. The rerun time in this case will not be considered test time. Repair time will not start until the failing element is made available for maintenance. Should this failure recur during the test after the repaired element/unit has been returned to the system, the necessary repair action will be taken but the failure will be classified as a transient.

3.1.4.1 Simplex System Criteria. A 120 hour SEVA acceptance exercise will be considered acceptable if under the condition stated in the preceding paragraphs the active system has not encountered an excessive number of transients or:

a. More than 10 malfunctions

b. A single malfunction requiring more than 16 hours to repair.

c. *Three malfunctions with each malfunction exceeding 8 hours to repair.

d. Or exceeding an aggregate of 12 additional hours to repair all malfunctions of duration equal to or less than 8 hours.

* If a malfunction occurs which exceeds 8 hours to repair, that 24-hour period will be restarted. If a malfunction occurs which requires 8 hours or less to repair, the 24-hour period will be continued from the time of the repair. If a second malfunction occurs which also requires more than 8 hours to repair, the test will be extended one 24-hour period.

Numbers shown in the above will be increased on a pro-rated basis depending upon the number of additional test hours required. In pro-rating, the chart below will apply.

Hour of the 24 Hour Test Period that Failure occurs or Additional Test Hours	Number of Additional Malfunctions (Step a)	Aggregate Hours (Step d)
> 0 ⩽ 6	0	0
> 6 ⩽ 12	1	1.5
> 12 ⩽ 18	1	1.5
> 18 ⩽ 24	2	3.0

Each 24-hour period will have an optional 3-hour scheduled maintenance period assigned: The option may be exercised at the end of hour 12 of each 24-hour period. If the option is exercised, this time will not count towards the 120 hour requirements. Scheduled maintenance includes routine maintenance and corrective maintenance.

The time to perform corrective maintenance on electromechanical devices or marginal check failures either off-line or during the scheduled maintenance period will not be included in any repair time totals; however, the malfunction which caused reconfiguration or removal will be counted in malfunction totals.

After the first 48 or 72 hours, the FAA Test Director may stop the test at any point and waive additional testing based on the following performance:

At the End of 48 Hours

⩽ 8 Total Transients

⩽ 4 Unrelated Transients

⩽ 2 Total Malfunctions

At the End of 72 Hours

⩽ 12 Total Transients

⩽ 6 Unrelated Transients

⩽ 3 Total Malfunctions

3.1.4.2 Duplex System Criteria. Each 24-hour period of the SEVA acceptance exercise will consist of 21 hours of A-1 Equipment Mode and 3 hours of Maintenance Equipment Mode Operation.

If a malfunction occurs in the active system, a redundant element or unit will be configured into the system in order to maintain the scheduled Equipment Mode of operation. However, if a redundant element or unit is not available, the exercise will be interrupted until the scheduled Equipment Mode can be restored.

If the first exercise interrupt does occur and the time required to effect a repair does not exceed 6 hours, that 24-hour period will be continued from the time of repair. If, however, the repair time exceeds 6 hours, that 24-hour period will be restarted.

A second exercise interrupt will require that the test be extended one twenty-four hour period.

A third exercise interrupt, or any exercise interrupt which exceeds 12 hours, will constitute a failure of the factory acceptance exercise.

A 120-hour SEVA acceptance exercise will be considered acceptable if under the condition stated in the preceding paragraphs the active system has not encountered an excessive number of transients or more than 10 malfunctions.

After the first 48 to 72 hours, the FAA Test Director may stop the test at any point and waive additional testing based on the following performance:

At the End of 48 Hours

$\leq$ 11 Total Transients

$\leq$ 6 Unrelated Transients

$\leq$ 2 Total Malfunctions

At the End of 72 Hours

$\leq$ 17 Total Transients

$\leq$ 9 Unrelated Transients

$\leq$ 3 Total Malfunctions

During this exercise, redundant elements and units will be configured periodically into the active system to allow each element and unit to be exercised for approximately the same length of time. However, each element and unit (excluding all electro-mechanical devices) must be configured into the active system for a minimum of 35 aggregate hours (120 hour test), 21 aggregate hours (72 hour test), 14 aggregate hours (48 hour test).

3.1.4.3 Triplex System Criteria. Each 24 hour period of the SEVA acceptance exercise will consist of 21 hours of A-1 Equipment Mode and 3 hours of Maintenance Equipment Mode operation.

If a malfunction occurs in the active system, a redundant element or unit will be configured into the system in order to maintain the scheduled Equipment Mode of operation. However, if a redundant element or unit is not available, the exercise will be interrupted until the scheduled Equipment Mode can be restored.

If the first exercise interrupt does occur and the time required to effect a repair does not exceed 6 hours, that 24-hour period will be continued from the time of repair. If, however, the repair time exceeds 6 hours, that 24 hour period will be restarted.

A second exercise interrupt will require that the test be extended one twenty-four hour period.

A third exercise interrupt, or any exercise interrupt which exceeds 12 hours, will constitute a failure of the factory acceptance exercise.

A 120 hour SEVA acceptance exercise will be considered acceptable, if under the condition stated in the preceding paragraphs, the active system has not encountered an excessive number of transients or more than 10 malfunctions.

After the first 48 or 72 hours, the FAA Test Director may stop the test at any point and waive additional testing based on the following performance.

At the End of 48 Hours

$\leqslant$ 15 Total Transients

$\leqslant$ 7 Unrelated Transients

$\leqslant$ 2 Malfunctions

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At the End of 72 Hours

$\leq$ 22 Total Transients

$\leq$ 11 Unrelated Transients

$\leq$ 3 Total Malfunctions

During the exercise, redundant elements and units will be configured periodically into the active system to allow each element and unit to be exercised for approximately the same length of time. However, each element and unit (excluding all electro-mechanical devices) must be configured into the active system for a minimum of 50 aggregate hours (120 hour test), 30 aggregate hours (72 hour test), 20 aggregate hours (48 hour test). When a triplex system contains element/unit types with a quantity of two, the aggregate hour requirements for those elements/units will be 35 hours (120 hour test), 21 hours (72 hour test) and 14 hours (48 hour test).

3.1.5 System EPO Criteria. The System Emergency Power Test, as specified in Section 7 is scheduled for demonstration in both the Factory and Field Acceptance Tests.

3.1.5.1 Simplex System Criteria. The System EPO Test will be considered acceptable if it demonstrates actual and indicated power loss to all elements and units, and two successful passes of SEVA can be completed within a reasonable time period after power has been restored.

If the test fails to provide the actual or indicated power loss to all elements and units, a rerun will be scheduled after the necessary corrective action has been completed.

If the rerun fails to demonstrate the proper power loss and indications, or if the SEVA checkout cannot be made, the test will be considered failed.

3.1.5.2 Duplex or Triplex Systems. The System EPO Test will be considered acceptable if it demonstrates the actual and indicated power loss to all elements and units and if the A-1 Equipment Mode can be established after a 45-minute period of system checkout.

The 45-minute checkout period will commence at the time power is restored to the system. Corrective maintenance may be performed during this period, if required.

The A-1 Equipment Mode system operation will be verified by completing two successful passes of the SEVA program on the A-1 system configuration.

If the test fails to provide the actual or indicated power loss, a rerun will be scheduled after necessary corrective action has been completed prior to system checkout.

If the rerun fails to demonstrate the proper power loss or the subsequent A-1 system operation is not verified, the test will be considered failed.

All units must be repairable within 12 hours.

3.2 Failure - Non-Deliverable Items

In the event of a failure of any of the following items the determination of whether or not the non-deliverable item caused the failure will be mutually agreed to by the FAA and IBM.

Failures determined to be caused by any of the following items will not constitute failure of the 9020D or 9020E Systems.

a. External equipment of facilities (power, simulators or environment).

b. Supply items (magnetic tape, card, etc.).

c. Those resulting from operator error, configuration error due to a manually initiated system set-up operation, or program set-up error.

d. Non-deliverable cables used in the Factory Acceptance Test.

e. Central computer complex equipment provided by the FAA.

3.3 Program Failures

Program failures will not constitute a failure of an IBM 9020D/E System Acceptance Test. However, the acceptance of the associated test will be dependent upon correction of the program failure and the successful demonstration of that test on the IBM 9020D/E Systems.

3.4 Recurring Transient Failures

Related transient failures which recur several times during the acceptance tests, and show a definite trend, will be classified as a recurring transient failure upon the mutual agreement of IBM and the FAA. IBM will submit for FAA approval, their recommended action to resolve the condition.

4.0 EQUIPMENT TEST PROCEDURES

This section describes the standard operating procedures and the initial switch settings and indications for the 9020D/E System Acceptance Tests. Frequent reference and constant adherence to these procedures and initializing conditions will greatly facilitate the resolution of any unexpected test conditions or results.

4.1 Preliminary Equipment Status

Indicated below are the initial switch settings and indicator conditions required prior to the test of the specific elements and units. Other switches and indicators are used, as directed by test operating procedures or programmed direction for manual intervention, but are not part of the preliminary status.

All Main, MACH, and Local Storage (SE, DE, CE, and IOCE) will be cleared prior to performing the Acceptance Test.

4.1.1 Compute Element

a. Manual Controls

1. Test - On
2. Scan Mode Repeat - Off
3. Scan Mode - Process
4. Defeat Interleaving - Process
5. Inhibit CE Hard Stop - Off
6. Disable Interval Timer - On
7. Storage Select - Main
8. Address Compare - Process
9. Check Control - Process
10. Pulse Mode - Process
11. Repeat Instruction - Process
12. ROS Address - Process
13. Frequency Alteration - Disable
14. Register Select - Process
15. Rate - Process

b. System Interlock - Off

c. Manual Indicator - On

d. Voltage controls at nominal values - indicators - Off

e. Main Line On indicator - On

f. Thermal indicator - Off

g. Power Check indicator - Off

h. Power Sequence Complete indicator - On

4.1.2 I/O Control Element

a. Manual Controls

1. Storage Test - Process
2. Write - Off
3. Stop On Check - Off
4. Invert SAR Bit 17 - Off
5. Bump Test - Off
6. Selector Channel Display - SC1
7. Test - On
8. Reverse Data Parity - Off
9. Storage Select - Main Storage
10. Storage Address Compare - Process
11. IAR Repeat Instruction - Off
12. ROS Address Compare - Sync
13. ROS Repeat Instruction - Off
14. Register Set - Both Off
15. Disable Interval Timer - On (Down)
16. Force Condition - Off
17. FLT Mode - Off
18. FLT Control - Process

19. Check Control - Process

20. Rate - Process

21. CTC Adapter #1 & #2 Enable/Disable - Disable

b. Manual Indicator - On

c. Voltage controls at nominal values - indicators - Off

d. Thermal indicators - Off (CLU, STOR, PDU)

e. Main Line On indicator - On

f. Open CB indicator - Off

g. Power Check indicator - Off

h. Power Sequence Complete indicator - On

4.1.3 Storage Element

a. Manual Controls

1. Marks - 0-7 to 0, P(parity) to 1

2. Address

1-4(Tag) - Reference logic KP010
5 (HI-LO) - 0
6-19 - Ripple
20 (E/O) - 1
21-23 - 0

3. Key - Set

4. Reverse Address Parity - Off

5. Data Entry - 0-7 to 0, P to 1

6. Priority (CE, IOCE) - Off

7. Reset Mode - Manual

8. Double Cycle Test Time Out - Off

9. Logout Stop - Off

10. Store/Fetch - Store

11. SCON Cont/Single - Single

12. TAS - Off

13. Cancel - Off

14. Priority/Storage - Storage

15. Single Cycle/Normal - Normal

16. Stop On Check Test - Off

17. Worst Case/Data Keys - Data Keys

18. Test/Normal - Test

19. Indicators - Normal

20. In Keys - 0-4 to 0, P to 1

b. Voltage controls at nominal values - indicators - Off

c. Thermal Check indicators - Off

d. Main Line On indicator - On

e. Power Check indicator - Off

f. Power Complete indicator - On

g. DC On indicator - On

h. SSU Power Check indicator - Off

i. Driver On indicator - Off

4.1.4 Display Element

a. Manual Controls

1. In Keys - 0-4 to 0, P to 1

2. Mark Keys - 0-7 to 0, P to 1

3. Address Keys - Ripple

4. Priority Select - CE-1 to Odd, all others to Off

5. Storage Data Entry - 0-7 to 0, P to 1

6. Log Adr Keys - 1,2 and 3 to 0

7. Store - Off

8. TAS - Off

9. Log Mode - Off

10. Auto Restart - Off

11. Key - Off

12. Priority/Storage - Storage

13. Single Cycle - Off

14. Stop On Check - Off

15. Worst Case/Data Keys - Data Keys

16. Storage Select - Main

17. Configuration Register - P0, P1, P4, P7 to 1, others to 0.

18. Test/Normal - Test

19. Indicators - Normal

20. Indicator Selection - STO

b. Voltage controls at nominal values - indicators - Off

c. Main Line On indicator - On

d. Power Check indicator - Off

e. Power Complete indicator - On

f. Thermal Check indicators - Off

g. DC On indicator - On

h. SSU Power Check indicator - Off

i. Driver On indicator - Off

4.1.5 System Console

a. Manual controls in Normal or Process position

b. Test/Operate switch - Off

c. Test Mode indicator - Off

d. System Interlock switch - Off

e. Mode of Operation indicators (red dot) - Off

f. Voltage Controls at Nominal Values - Indicator - Off

g. System Power indicators - Off

h. Main Line On indicator - On

i. Power Check indicator - Off

j. Thermal Check indicator - Off

k. Power Sequence Complete indicator - On

l. Interface Enable/Disable switch - Enable

4.1.6 Configuration Console

a. Manual controls in Normal or Process position.

b. Test/Operate switches - Operate

c. Test Mode indicators - Off

d. System Interlock switch - Off

e. Voltage controls at nominal values - indicators - Off

f. System Power indicators - Off

g. Main Line On indicator - On

h. Power Check indicators - Off

i. Thermal Check indicators - Off

j. Power Sequence Complete indicators - On

k. Interface Enable/Disable switches - Enable

4.1.7 Peripheral Adapter Module

a. Manual controls in Normal position

b. Test switch - Off

c. Test indicator - Off

d. Voltage Controls at Nominal Values - indicators - Off

e. Main Line Power indicator - On

f. Power Sequence Complete indicator - On

g. Power Check indicator - Off

h. Thermal Check indicator - Off

i. Interface Enable/Disable switch - Enable

4.1.8 Storage Control Unit

a. CE/Normal/In-line switch - CE

b. Driver Degate switch - On

c. Main Line On indicator - On

d. Power Check indicator - Off

e. Thermal Check indicator - Off

f. Power indicator - On

4.1.9 Tape Control Unit

a. Power Check indicator - Off

b. Power Sequence Complete indicator - On

c. Thermal Check indicator - Off

d. Interface Disabled indicator - Off

4.1.10 Integrated Control Unit

a. Power On indicator - On

b. CB TRIP indicator - Off

c Thermal TRIP indicator - Off

d. Interface Enable/Disable switch - Enable

4.1.11 Disk Storage Unit

a. Start/Stop switch - Start

b. Ready Indicator - On

c. Select Lock Indicator - Off

4.1.12 Printer Keyboard

a. Sense indicators - Off

b. On Line switch - On

NOTE: A full supply of 2 ply paper loaded.

4.1.13 Tape Drive Units

a. Ready indicator - On

b. File Protect indicator - On, if file reel has Write-Enable Ring removed.

c. Tape indicator - Off

d. CB indicator - Off

4.1.14 Card Read/Punch

a. Common indicators

- Power indicator - On
- Transport indicator - Off
- Stacker indicator - Off
- Fuse indicator - Off

b. Card Reader indicators

- Ready indicator - On
- Feed Stop indicator - Off
- End of File indicator - Off
- Read Check indicator - Off
- Validity Check indicator - Off

c. Card Punch indicators

- Ready indicator - On
- Feed Stop indicator - Off
- Chip Box indicator - Off
- Punch Check indicator - Off

4.1.15 High-Speed Printer

a. Print Ready indicator - On

b. Forms Check indicator - Off

c. End of Form indicator - Off

d. Print Check indicator - Off

e. Sync Check indicator - Off

NOTE: A full supply of two-ply paper loaded.
Proper carriage control tape loaded.

4.1.16 Data Adapter Unit

a. Power On and Reset indicators - On

b. Interface Enable/Disable switch - Enable

c. CB Trip indicator - Off

d. Thermal Trip indicator - Off

e. On Line Switch - On Line

f. Normal/Record Lock switch - Normal

g. Driver Degate switch - Off

h. I/O interface Disable indicator - Off

4.2 Manual Configuration Procedure

For all tests which require manual configuration or reconfiguration, the following procedures detail the steps necessary to set configuration on any given element or unit. It is assumed in all cases that any machine operation has been stopped and that the element or unit is in STATE ZERO. In the event the element or unit is not in STATE ZERO, refer to the STATE RESET PROCEDURE (4.3).

4.2.1 Compute Element

a. Set Test switch On

b. Depress Reset pushbutton

c. Set Storage Data Register keys to correspond to the desired configuration.

d. Set Register Select switch to CCR position

e. Depress Register Set pushbutton

f. Observe CCR indicators (roller 5, position 5)

g. Set the desired ATR setup in the Data Register keys

h. Set the Register Select switch to the ATR position

i. Depress the Register Set pushbutton

j. Observe the ATR indicators (roller 1 and 2, position 1)

k. Set the desired PSBAR setup in the Data Register keys

l. Set the Register Select switch to the PSBAR position

m. Depress the Register Set pushbutton

n. Observe the PSBAR indicators (roller 5, position 1)

o. Set Test switch Off

4.2.2 I/O Control Element

a. Set Test switch On

b. Depress Reset pushbutton

c. Set Storage Data Register keys to correspond to the desired configuration

d. Set Register Set switch to CCR position

e. Depress Register Set pushbutton

f. Observe CCR indicators (roller 3, position 7) to insure desired results

g. Set Test switch Off

4.2.3 Storage Element

a. Set Test switch On and Worst Case/Data keys switch to Data Keys

b. Depress Reset pushbutton

c. Set SCON Cont/Single to Single

d. Set Storage Data Entry keys to correspond to CCR-1 configuration (upper byte)

e. Set Mark switch 4 to CCR-1

f. Depress Set Configuration pushbutton

g. Observe CCR indicators to insure desired results

h. Set Mark switch 4 to zero

i. Set Storage Data Entry keys to correspond to CCR-2 configuration (lower byte)

j. Set Mark switch 7 to CCR-2

k. Depress Set Configuration pushbutton

l. Observe CCR indicators to insure desired results

m. Set Test switch Off

4.2.4 Display Element

a. Set Test switch On

b. Depress General Reset pushbutton

c. Set Configuration Register switches to correspond to the desired configuration

d. Depress Set Configuration pushbutton

e. Observe Configuration Register indicators to insure desired results

f. Set Test swtich Off

4.2.5 Reconfiguration Control Unit

a. Set Test switch On.

b. Depress Reset pushbutton

c. Depress Reset CCR pushbutton.

d. Set Address Keys 2-7 and Bus Out Keys 5-7 to the desired configuration

e. Depress Set CCR pushbutton

f. Observe Configuration Control Register to insure desired results

g. Set Test switch to Operate

4.2.6 Peripheral Adapter Module

a. Set Test switch On

b. Depress General Reset pushbutton

c. Set Data/SCON-IOCE switches to correspond to the desired configuration

0 1 2 3 4	5 6 7
P 1 2 3 4	1 2 3
SCON	*IOCE

d. Depress Set CCR pushbutton

e. Observe CCR indicators to insure desired results

f. Set Test switch Off

*Only one "1" may be set in Bits 5, 6, or 7 when setting CCR

4.2.7 Storage Control Unit

a. Set the CE/Normal/In-line switch to the CE position

b. Raise the RESET/LAMP Test switch

c. Set the CE Select switch in the ANY CE position

d. Set the CCR switches to the desired configuration

CONFIGURATION CONTROL REGISTER

STATE			SCON				IOCE			
P0	S0	S1	CE 1	CE 2	CE 3	CE 4	P3	1	2	3

e. Set the Single Step/Auto Cycle switch in the Auto Cycle position.

f. Depress the Execute pushbutton

g. Observe CCR indicators to insure desired results.

h. Set the CE/Normal/In-line switch to the Normal position.

4.2.8 Tape Control Unit

a. Insert Plug into Off Line jack. Interface disabled indicator should be - On

b. Depress Machine Reset pushbutton

c. Release A Interface

d. Plug Interface B

e. Plug Command Position #1 with Mode Set NOP command (Plug Bits P, 6 & 7) and plug a valid selection in the Address Jacks.

f. Plug Write Data Position #1 to correspond to the desired configuration as follows:

Bit	CCR Position
P	Parity #1
0	SCON 1
1	SCON 2
2	SCON 3
3	SCON 4
4	Parity #2
5	IOCE 1
6	IOCE 2
7	IOCE 3

g. Depress Start pushbutton

h. Observe CCR indicators for desired results

i. Remove Plug from Off Line jack. Interface disabled indicator should be - Off

4.2.9 Computer Oriented Peripheral Equipment. Although there is no configuration register associated with the card machines, it is necessary that they be enabled as follows:

At the System Console (9020D) or Configuration Console (9020E).

a. Select the appropriate IOCE via the I/O Select Rotary switches

b. Depress Enable pushbutton

c. Observe Enable lite to insure results

The above steps apply to System Console 1052 and/or the Read/Punch and Printer.

4.3 State Reset Procedure

For all tests which require manual reconfiguration, it will be necessary to first insure that the element or unit is in State Zero. The following procedures detail the steps necessary to obtain State Zero on any given element or unit. It is assumed in all cases that all machines operations have been stopped.

4.3.1 Compute Element

At the System Console (9020D) or Configuration Console (9020E)

a. Select the CE to be reset via the CE Select switch

b. Set the Control CE switches to correspond to the desired SCON field setting.

c. Turn System Interlock Key On.

d. Depress Activate pushbutton

4.3.2 Other Elements and Units

At the System Console (9020D) or Configuration Console (9020E)

a. Determine the Configuration Mask

NOTE: The contents of the configuration mask are loaded by the SCON instruction into the CCR of system elements and/or units.

Configuration Mask Format

9020D System

WORD 1

STATE		SCON					SE										CE					IOCE		
S_0	S_1	1	2	3	4	*	*	1	2	3	4	5	6	7	8	9	10	*	*	1	2	3	4	*	*	*	*	*	1	2	3
0	1	2			5			8									17			20			23						29		31

WORD 2

* *

0 31

9020E System

WORD 1

STATE		SCON			SE		DE			CE					IOCE		
S_0	S_1	1	2	3	4	* *	1	2	3	4	5	1	2	3	4	5	* *	1	2	3	4	* * * * *	1	2	3
0	1	2			5		8				12	13				17		20		23			29		31

WORD 2

DG																
1A	1B	2B	2C	3C	3D	4D	4A	5A	5B	6B	6C	7C	7D	8D	8A	**********
0														15		

b. Determine the Selection Mask

NOTE: The Selection Mask designates the elements or units that are to receive the data contained in the Configuration Mask. In effect, the Selection Mask is an address word for the Configuration Mask.

Selection Mask Format

9020D System

PAM			TCU				SE										CE				SCU				IOCE		
1	2	3	1	2	3	* *	1	2	3	4	5	6	7	8	9	10	* *	1	2	3	4	1	2	3	* *	1	2	3
0		2	3		5		8									17		20			23	24		26		29		31

202764

9020E System

RCU			TCU				SE					DE						CE							IOCE		
1	2	*	1	2	3	*	*	1	2	3	4	5	1	2	3	4	5	*	*	1	2	3	4	*	*	*	*	*	1	2	3
0	1		3		5			8				12	13				17			20			23					29		31

c. Turn System Interlock key On.

d. Store the following data in the given locations:

Location (Hex)	Data (Hex)
000000	00040000
000004	00000404
000400	82000000
000404	014647F0
000408	04060000
General Purpose Reg. #4 & 5	Configuration Mask
General Purpose Reg. #6	Selection Mask

e. Set IC 000400 (Hex)

f. Depress Start (Program should loop at 000406)

4.4 Diagnostic Monitor Initialization and Usage

MDM (Multiprocessing Diagnostic Monitor) and SDM (Subsystem Diagnostic Monitor) are used in the 9020D/E System Test. The following elements and units are required to initialize MDM and SDM by means of an IPL Load.

1 Systems Console (9020D) or Configuration Console (9020E)

1 Compute Element

1 Storage Element

1 Input/Output Control Element

1 Tape Control Unit

1 Tape Drive

1 Input Device (1052 or Card Reader)

1 Output Device (1052 or Printer)

Since MDM, SDM, and the test programs will normally be tape loaded from the Compute Element, with the 1052 as both the input and output device, the initialization procedure will follow this approach. However, if MDM is desired, this same load fuction may be accomplished from the System Console (9020D) or Configuration Console (9020E) during the Acceptance Test.

4.4.1 Loading Procedure. Mount the File Protected System Library Master Tape on a Tape Drive. If the Library Tape is already mounted, be sure it is at load point and made Ready.

Perform the following:

a. Manually configure all elements of the subsystem

b. At the CE, set the Main Storage Select switch to the desired element selection.

c. Set the Load Unit switches to the address of the tape unit.

d. Depress the Stop pushbutton.

e. Depress the Load pushbutton.

NOTE: Observe a Wait state with 00000A in the IAR on the SC/CC.

f. Depress the Request pushbutton on the 1052 being used as the Input device. The following messages will be printed at the 1052.

```
SDM REVISION N READY
ENTER SYSTEM ID
REPLY EITHER A,D OR E
```

g. Type the appropriate letter in lowercase or uppercase followed by a / and depress the Enter pushbutton.

h. Depress the Request pushbutton.

i. If using MDM, do the following; otherwise go to step j.

1. Type the message LMDM/.

2. Depress the Enter pushbutton.

NOTE: Observe a Wait state with 00000A in the IAR on the console.

3. Depress the Request pushbutton on the 1052. The following message will be printed.

```
MDM D/E REVISION N READY
```

j. Assign the 1403 printer (address CUU) to the Diagnostic Monitor as the primary and secondary output device by typing the following:

A63000CUU/I,,CUU,CUU,/

(Refer to Appendix M, A type message for OO options)

k. Depress the Enter pushbutton.

l. Enter all units in the maintenance subsystem, using a U message (MDM only).

m. M and S messages may be entered at this time.

n. Enter the desired task assignment.

4.4.2 Test Operating Procedure. The following procedures describe the use of the Human Interface used between the operator and MDM to specify configured elements and units, which programs to run, interventions required, and all other parameters and control input to MDM. It is also the medium by which test results and instructions to the operator are communicated. Appendix M describes the various input messages and codes of the Human Interface.

4.5 Operation Under MDM

To operate MDM in Sequential Mode utilizing only the minimum Subsystem, which MDM has assumed from the initialization, an L message followed by B/ is needed to initiate a Job Request. Depressing the Enter key signifies to MDM the end of message and must be used to terminate each input message. In the case of incorrectly entered data, the message may be cancelled by depressing the Cancel key.

The A or U message can be used to add units or elements to the System. The I message can be used to Assign or Reassign devices at any time, provided the devices were previously entered in the Unit Definition Table by MDM initialization or a U or an A message.

Options available to the operator in the form of input messages are defined in Appendix M. An input message of L1151/B/ will cause MDM to Search the Library Tape for this section, initialize the section, Print on the Output Device START D11510, execute the section and (if error free) print out a Termination message T CEN NNN D11510.

At any time during the operation of a Job Request, the operator may intervene by depressing the Request Key (1052) or Interrupt Button (System Console (9020D) or Configuration Console (9020E) depending on the specified input device, and give MDM another input message. Most input messages are dynamic in nature, meaning they may be entered anytime

and executed immediately such as Cycle, Free Section, Add Unit, etc. Load messages may be entered at any time, but the programs will not necessarily load immediately.

When a particular task has been completed, MDM will enter an idle loop enabled for interrupts and a new Sequence of Operator actions.

4.5.1 Printouts and Error Stops. MDM generated messages can be either error or operational. They are usually self explanatory but include a reference to the program listing if more detailed information is required. Reference Section 4.0 (Printouts) of the program write-ups and Section 2.2 (Output Messages) of the IBM Maintenance Diagnostic Program 9020D and 9020E System Maintenance Monitor Manual.

MDM has several places where it will branch to itself if a catastrophic error is encountered. The Instruction Counter (IC) will display the listing address where a detailed explanation will be found.

The Acceptance Tests will be run with the Check Control Switch (IOCE and CE) in the Process position and the Inhibit CE Hard Stop Switch (CE) in the Off position, unless the program write-up states otherwise.

NOTE: Hardware detected errors will result in a hard stop when Check Control switch is in the Stop position. Error indications will be determined from the display roller lamps.

4.6 SEVA Loading and Operating Procedure

The SEVA program consists of a control program, functional test programs, and a special acceptance test program. The SEVA program operates under control of MDM. After MDM has been loaded and initialized, the SEVA Control Program is loaded using a normal MDM load message. The SEVA Control Program will establish the configuration, define the system, schedule the test programs for that pass and request MDM to load and operate the scheduled programs. At the end of the pass, the SEVA Control Program is given control again and the cycle is repeated.

Refer to the SEVA program write-up in the IBM 9020D/E Data Processing System Off Line Maintenance Programs Manual for additional information concerning program operation, program options or input messages.

4.7 Switch Operating Procedure

The purpose of the manual switch demonstrations is to insure proper operation of the control panels with their associated switches. The control panels are primarily intended for use by maintenance personnel to operate and maintain elements and units in the 9020D/E System.

The testing technique for the CE and IOCE involves the use of ROS micro-orders, small program loops and the switches to initiate and control the desired switch operation. The Storage Control Unit uses ROS micro-orders and switches to initiate and control the desired switch operation. Micro-Programming then places the results in specified registers or locations for a visual indication which provides a quick method of checking proper operation of the switch being tested. The Printer Keyboard, Tape Control Unit and Integrated Control Unit output the data from the switch settings directly to indicators, magnetic tape, punched cards or printed paper, which are then checked for correct results. The switches on the PAM's, DAU's, SE's, DE's, SC or CC are checked for proper operation, utilizing indicators on each element.

Following is a list and description of the CE ROS micro-orders used during the switch demonstrations:

800 - Entry point of a ROS routine that will ripple storage with data from the Data Keys. Address switches 29 & 30 are used in conjunction with this ROS Address to designate a store operation (11) or a fetch operation (00).

F00 - Single ROS word containing all ones with good parity.

F02 - Single ROS word containing all zeroes with good parity.

Following is a list and description of the IOCE ROS micro-orders used during the switch demonstrations:

240 - Contains a micro-instruction to move the settings of the Load Unit Address switches into specified locations of the L and M registers.

29F - Address stopping on ROS Address 29F allows a visual check of the External Interrupt code set into the M register by the micro-instruction in the previous ROS Address block.

2AC - First micro-instruction of the Timer Update and External Interrupt routine.

2B0 - One of five (5) ROS Addresses (2B9, 2B0, 2A0, 2B4 and 28C) indicating that the IOCE Halt Loop has been entered.

DD6 - Contains a micro-instruction to move the settings of the Data Keys into the L register. Depressing the Start pushbutton three (3) additional times steps the micro-program through ROS Addresses D96, D56 and D16 which places the same data into the R, H and M registers.

F96 - Contains a micro-instruction which blocks the normal control panel indications.

Following is a list and description of the Storage Control Unit ROS micro-orders used during the switch demonstrations:

602 - First micro-order of a routine which tests all positions of each register and also insures that the CE decodes are functioning correctly.

6E1 - Last micro-order of the routine started at Address 602.

600 - Home address of a scan micro-program which is a sequence of two word loops, used in this case to demonstrate single step operation.

5.0 SUB-SYSTEM FUNCTIONAL TEST

These tests will consist primarily of test programs that check technical features, logic blocks, computer commands, and data transfer paths of individual elements or units. Also included in these tests are manual switch demonstrations which will be shown on all elements and units.

A single successful pass of a test program shall be considered an acceptable demonstration.

In the event that a test program or a certain routine of a test program encounters a failure caused by the element or unit being tested, that test program or routine shall be repeated immediately.

If the program or routine does not fail during the repeat pass, the failure shall be classified a transient failure and the test shall be considered acceptable.

If several transient failures are detected during a given test, the cause of such failures will be analyzed and reported to the FAA observer.

If the failure condition still exists during the repeat pass, the failure shall be classified a malfunction and necessary corrective action shall be initiated. Testing of other elements or units may proceed while repairs are accomplished on the failing element or unit. Further testing of the element or unit that failed, including a rerun of the test program or routine that encountered the failure will be completed during the time period allocated.

For either a transient failure or a malfunction from one to five passes of the program or routine that failed will be run at the discretion of the FAA observer.

The failure of an element or unit in the required configuration, other than the element or unit being tested, will not be considered a failure of the current test. A redundant element or unit will be substituted for the failing element or unit, and applicable portions of the test repeated.

Prior to any switch demonstration or switch demonstration reruns, care should be taken to assure proper element initialization and configuration.

5.1 Manual Functional Tests

The following section will be a demonstration of the manual controls and indicators on the test panels for the various elements/units.

5.1.1 Compute Element - The following section will be a manual demonstration of the Compute Element control panel switches necessary to operate a subsystem.

The CE being tested must be in state 0 with the Test switch on and configured to an available SE. (Refer to Section 4.)

a. Lamp Test

1. Depress and hold the Lamp Test Allow Ind pushbutton.

2. Observe that all but the margin, power status, and roller indicators light.

3. Test each of the sets of roller indicators by rotating the roller such that it is between normal positions. Observe that all indicators for that roller are on.

b. Repeat ROS Address switch, ROS Transfer and System Reset pushbutton.

1. Set the ROS Address switch to Rpt.

2. Depress the System Reset pushbutton.

3. Set Address Keys 8-19 to ROS Address F00.

4. Depress the ROS Transfer pushbutton.

5. Observe all ones with odd parity in ROSDR bits 2-99 (rollers 2, 3 and 4, position 4).

6. Observe that the ROS Parity Error indicators are off (roller 2, position 2).

7. Repeat steps 2 through 6 using ROS Address F02 and observe all zeroes with odd parity in ROSDR bits 0-99 (rollers 2, 3 and 4, position 4).

8. Set the ROS Address switch to Proc.

c. Store and Display pushbuttons

1. Depress the System Reset pushbutton.

2. Set all data keys to the 0 position.

3. Set Address keys 08-31 to 80 00 06_{16}.

4. Depress the ROS Transfer pushbutton.

5. Set the Storage select switch to the Local position and then return it to the Main position.

6. Depress the System Reset pushbutton.

7. Set the Check Control switch to the Stop position.

8. Set the Data keys 00-63 to 0F 0F 0F 0F F0 F0 F0 $F0_{16}$.

9. Set the Address keys 08-31 to 00 00 00_{16}.

10. Depress the Store pushbutton.

11. Observe that Check Register 2 Summary indicator does not turn on.

12. Depress the Display pushbutton.

13. Observe the Main Storage data displayed in Registers S and T (rollers 1 and 2, position 3). The data displayed should agree with the contents of the Data keys.

14. Set the Storage Select switch to the Local position.

15. Depress the Stop pushbutton.

16. Depress the Store pushbutton.

17. Depress the Display pushbutton.

18. Observe the Local Storage data displayed in Register T (roller 2, position 3). The data displayed should agree with the contents of Data Keys 32-63.

19. Return the Storage Select switch to the Main position.

d. Set IC pushbutton.

1. Set the Rate switch to the Process position.

2. Depress the System Reset pushbutton.

3. Set the Address keys 08-31 to 80 80 80_{16}.

4. Depress the Set IC pushbutton.

5. Observe that the Instruction Counter (roller 6, position 3) contains 80 80 88_{16} with odd parity.

6. Set the Address keys 08-31 to 00 00 00_{16}.

7. Depress the System Reset and Set IC pushbuttons.

8. Observe that the Instruction Counter (roller 6, position 3) contains 00 00 08_{16} with odd parity.

e. Disable Interval Timer switch and Rate switch (STEP position).

1. Set the Disable Interval Timer to the mid position.

2. Key the following into Storage:

Address	Data
000000	47F000F000000000
0000F0	47F0000000000000

3. Display the above locations to insure correct data transfer.

4. Set the Address Keys to 00 00 $F0_{16}$.

5. Depress the System Reset, Set IC and Start pushbuttons.

6. Observe the decrementing of the Interval Timer in the A register 00-23 (roller 3, position 3).

7. Set the Disable Interval Timer switch in the down position.

8. Observe that the decrementing in the A register stops.

9. Depress the Stop pushbutton.

10. Set the Rate switch to the INSN STEP position.

11. Depress the Start pushbutton several times.

12. Observe that the Instruction Counter bits 24-27 (roller 6, position 3) alternately displays 0_{16} and F_{16} as the Start pushbutton is depressed.

13. Set the Rate switch to the Process position.

f. Rate Switch (Single Cycle position)

1. Key the following into storage:

Address	Data
000100	47F0010000000000

2. Depress the System Reset pushbutton.

3. Set Address Keys to 000100_{16}.

4. Depress the Set IC pushbutton.

5. Set Rate Switch to the Sing. Cy. position.

6. Depress the Start pushbutton.

7. Observe ROS address 21C in ROSAR (roller 1, position 4).

8. Depress the Start pushbutton.

9. Observe ROS Address 107 in ROSAR.

10. Depress the Start pushbutton.

11. Observe ROS Address 724 in ROSAR.

12. Depress the Start pushbutton.

13. Observe ROS Address 9AE in ROSAR.

14. Set Rate Switch to the Process position.

15. Depress the Start and Stop pushbuttons.

g. Storage Select switch (Main Byte position)

1. Set the Storage Select switch to the Main position.

2. Set the Data keys to FF FF FF FF FF FF FF FF_{16}.

3. Set the Address keys to 00 01 00_{16}.

4. Depress the System Reset, Store and Display pushbuttons.

5. Observe that the S,T,A, and B registers contain an all ones pattern with odd parity (rollers 1 thru 4, position 3).

6. Set all Data keys to the 0 position.

7. Set the Storage Select switch to the Main Byte position.

8. Depress the Store and Display pushbuttons.

9. Observe that byte 0 of the S and A registers have cleared to zeroes with odd parity.

10. Repeat step 8 with Address key settings 00 01 01_{16} thru 00 01 03. Observe that S and A register bytes 1 thru 3 clear to zero in turn.

h. Rate Switch (Single Cycle Storage Inhibit)

1. Set the Data keys to FF FF FF FF FF FF FF FF_{16}.

2. Set the Storage Select switch to the Local position.

3. Set the Address keys to 00 00 01_{16}.

4. Depress the System Reset, Store, and Display pushbuttons.

5. Set the Storage Select switch to the Main position.

6. Key the following into Storage:

Address	Data
000100	0F 0F 0F 0F 0F 0F 0F 0F
000000	58 10 01 00 47 F0 00 00

7. Display the above locations to insure correct data transfer.

8. Set the Address keys to 00 00 00_{16}.

9. Depress the System Reset and Set IC pushbuttons.

10. Set the Rate switch to the Single Cycle Storage Inhibit position.

11. Depress the Start pushbutton six (6) times.

12. Set the Address keys to 00 00 01_{16}.

13. Set the Storage Select switch to the Local position.

14. Depress the System Reset and Display pushbuttons.

15. Observe that the T register (roller 2, position 3) contain all zeros (including parity) and that the Check Reg. 2 Ind. and LS Bus Parity (roller 6, pos. 5) are on.

16. Set the Rate switch to the Process position.

17. Depress the Start, Stop and System Reset pushbuttons.

i. Repeat Instruction Switch

1. Set the Repeat Instruction switch to the Single position.

2. Set the Check Control switch to the Disable position.

3. Set the Disable Interval Timer switch to the down position.

4. Set the Storage Select switch to the Main position.

5. Set the Data keys to FF FF FF FF FF FF FF FF_{16}.

6. Set the Address keys to 00 02 00_{16}.

7. Depress the System Reset and Store pushbuttons.

8. Set the Data keys to 58 F0 02 00 00 00 00 00_{16}.

9. Depress the Start pushbutton and observe that the System indicator turns on.

10. Depress the Stop and System Reset pushbuttons.

11. Set the Address keys to 00 00 $0F_{16}$.

12. Set the Storage Select switch to the Local position.

13. Depress the Display pushbutton.

14. Observe that Local Store register 15 as displayed in the T register (roller 2, position 3) contains all ones with odd parity.

15. Observe that the E register (roller 5, position 3) contains 58 $F0_{16}$.

16. Set the Storage Select switch to the Main position.

17. Set the Data keys to 00 00 00 00 55 55 55 55_{16}.

18. Set the Address keys to 00 0F FC_{16}.

19. Depress the System Reset and Store pushbuttons.

20. Set the Data keys to 58 F0 0F FC 47 F0 02 00_{16}.

21. Set the Repeat Instruction switch to the MPLE position.

22. Depress the System Reset pushbutton.

23. Set the Rate switch to the Instruction Step position.

24. Depress the Start pushbutton.

25. Observe that the E register (roller 5, position 3) alternately displays 58 $F0_{16}$ and 47 $F0_{16}$ for each depression of the Start pushbutton.

26. Set the Rate switch to the Process position.

27. Set the Check Control switch to Stop.

28. Depress the Start pushbutton.

29. Observe that the machine cycles error free.

30. Set the Address keys to 00 0F FC_{16}.

31. Set the Address Compare switch to the Stop position and observe that the Manual indicator turns on.

32. Set the Storage Select switch to the Local position.

33. Set the Address keys to 00 00 $0F_{16}$.

34. Depress the System Reset and Display pushbuttons.

35. Observe that Local Store register 15 as displayed in the T register (roller 2, position 3) contains 55 55 55 55_{16}.

36. Set the Address Compare switch to the Process position.

37. Set the Check Control switch to Process.

j. Test Indicator

1. Set all Manual Control switches including the Test Switch to their mid position.

2. Observe that the Test indicator turns on when any of the following switches are moved to a position other than Process or mid position: Rate, ROS Address, Repeat Instruction, Pulse Mode, Check Control, Address Compare, Disable Interval Timer, Defeat Interleaving, Scan Mode (ROS/FLT), Inhibit CE Hard Stop, and Test.

3. Return Test switch to Test and Disable Interval Timer - Down.

k. Pulse Mode Switch

1. Key the following into Storage:

Address	Data
00 00 00	00 00 00 00 00 00 02 00
00 02 00	58 20 03 00 46 20 02 04
00 02 08	47 F0 02 08 00 00 00 00
00 03 00	00 00 FF FF 00 00 00 00

2. Display the above locations to insure correct data transfer.

3. Set the Pulse Mode switch to the Count position.

4. Set the Rate switch to the Process position.

5. Set the Check Control switch to the Disable position.

6. Set the Data keys to 00 00 00 00 00 00 00 81_{16}.

7. Depress the Start pushbutton.

8. Observe that the machine cycles error free.

9. Observe that depressing the Stop pushbutton does not stop the cycling of the machine.

10. Observe that the Pulse Mode Adjust indicator (roller 3, position 1) becomes brighter as the count from Data keys 56-63 is decreased.

11. Depress the Stop and System Reset pushbuttons.

12. Set the Pulse Mode switch to the Time position.

13. Depress the Start pushbutton.

14. Observe that the machine cycles with the B register 48-63 rippling (roller 4, position 3) and the Pulse Mode Init. indicator (roller 3, position 1) is on.

15. Depress the Stop and System Reset pushbuttons.

16. Set the Pulse Mode switch to the Process position.

1. Defeat Interleaving switch

1. Depress the System Reset pushbutton.

2. Set the Data keys to FF 00 FF 00 FF 00 FF 00_{16}.

3. Set the Address keys to 00 00 08_{16}.

4. Depress the Store pushbutton.

5. Set the Defeat Interleaving switch to the No Reverse position.

6. Set the Address Keys to 02 00 00_{16}.

7. Depress the Display pushbutton.

8. Observe that the S and T registers display (roller 1 and 2, position 3) agrees with the contents of the Data keys.

9. Set the Defeat Interleaving switch to the Reverse position.

10. Set the Address keys to 00 00 00_{16}.

11. Depress the Display pushbutton.

12. Observe that the S and T registers display (roller 1 and 2, position 3) agrees with the contents of the keys.

13. Set the Defeat Interleaving switch to the Process position.

m. Log-Out pushbutton

1. Depress the System Reset pushbutton.

2. Set the Data keys to FF FF FF FF FF FF FF FF_{16}.

3. Set the Address keys to 00 10 00_{16}.

4. Depress the System Reset, Store, Display, Set IC, and Log Out.

5. Set the Address keys to 00 00 $B8_{16}$.

6. Depress the Display pushbutton.

7. Observe that the data displayed in the A and B registers (rollers 3 and 4, position 3) is all ones with odd parity.

8. Set the Address keys to 00 00 $C8_{16}$.

9. Depress the Display pushbutton.

10. Observe that the data displayed in the B register 40-63 (roller 4, position 3) is 00 10 08_{16}.

11. Set the Address keys to 00 00 $D0_{16}$.

12. Depress the Display pushbutton.

13. Observe that the data displayed in the A register 00-15 (roller 3, position 3) is FF FF_{16}.

14. Set the Address keys to 00 00 $D8_{16}$.

15. Depress the Display pushbutton.

16. Observe that the data displayed in the A and B registers (rollers 3 and 4, position 3) is all ones with odd parity.

17. Set the Address keys to 00 01 38_{16}.

18. Depress the Display pushbutton.

19. Observe that the data displayed in the A and B registers (rollers 3 and 4, position 3) is all ones with odd parity.

n. Interrupt and PSW Restart pushbutton

1. Main Stor Select switch set to the configured SE.

2. Key the following data into storage:

Address	Data
00 00 00	01 02 00 00 00 00 00 00
00 00 18	00 00 00 00 00 00 00 00
00 00 58	00 02 00 00 00 FF FF EF

3. Depress the PSW Restart pushbutton.

4. Observe that the Wait indicator is on and the Instruction Counter (roller 6, position 3) contains 00 00 08_{16}.

5. Depress the Interrupt pushbutton.

6. Observe that the Wait indicator is on and the Instruction Counter contains FF FF FF_{16}.

7. Set the Address keys to 00 00 18_{16}.

8. Depress the Stop pushbutton.

9. Depress the Display pushbutton.

10. Observe that the A register (roller 3, position 3) contains 01 02 00 40_{16}.

p. Register Select Switch and Register Set pushbutton

1. Set the Data keys 00-63 to 12 34 56 78 9A 01 23 45_{16}.

2. Set the Register Select switch to the ATR position.

3. Depress the Register Set pushbutton.

4. Set the Register Select switch to the PSBAR position.

5. Depress the Register Set pushbutton.

6. Set the Register Select switch to the CCR position.

7. Depress the Register Set pushbutton.

8. Observe that the ATR-1 (roller 2, position 1) contains 12 34 56 78_{16}.

9. Observe that the ATR-2 (roller 1, position 1) contains $9A_{16}$ with odd parity.

10. Observe that the Logical PSBAR (roller 5, position 1) contains 012_{16} with odd parity.

11. Observe that the CCR (roller 5, position 5) contains 9A 01 23 45_{16} with odd parity.

12. Restore CCR, PSBAR and ATR to original contents.

13. Set the Register Select switch to the Process position.

q. Load pushbutton

1. Depress the System Reset pushbutton.

2. Depress the Load pushbutton.

3. Observe that the Load indicator is on.

r. Scan Mode switches and Backspace FLT pushbutton

1. These switches will be demonstrated in Section 6 during the FLT Tests.

5.1.2 Input/Output Control Element. The following section will be a manual demonstration of the Input/Output Control Element Panel switches.

The IOCE which is being tested should be in State 0 with the Test switch on and be in Diagnostic Mode (not configured to any CE). The Test indicator should be on. (Refer to Spec. Section 4.1).

a. Lamp Test Switch

1. Depress Lamp Test Switch (down) and check that all indicators are lit except the Power, Marginal check, Channel to Channel and spare indicators. The Channel to Channel Adapter indicators are controlled by their Off Line/On Line switches.

b. Load Unit Address switch and Load pushbutton.

1. Enter ROS Address 240 in the data keys (position 20 to 31).

2. Set ROS Repeat Instruction switch to on (down).

3. Set Rate switch to Single Cycle and depress Load pushbutton. Load indicator should be on.

4. Set the Load Unit switches to 3 FF.

5. Depress the Start pushbutton twice and observe the following on Display 3, Roller Position 1:

L Register Position 0 to 7 should contain FF.

L Register Position 22 to 23 should contain 3.

6. Set ROS Repeat Instruction switch off.

c. Interrupt and PSW Restart pushbuttons and Disable Interval Timer switch.

1. Set Rate switch to Process.

2. Depress the Start and Reset pushbuttons.

3. Set Storage Select switch to MACH.

4. Key in the following data into Storage:

Address	Data	
0000	01 02 00 00	Initial PSW
0004	00 00 00 00	
0018	01 00 00 00	Ext. Int. Old
001C	00 00 00 00	
0050	00 FF FF 00	
0058	01 00 00 00	Ext. Int. New
005C	00 00 04 00	

5. Display the above locations to insure correct data transfer.

6. Depress the PSW Restart pushbutton. The Wait indicator should come on.

7. Set the ROS Address 2 AC in data keys (positions 20 to 31).

8. Place the ROS Address Compare switch to Stop (down).

9. Place the Disable Interval Timer switch to the Off position (up).

10. Check Display 3, Roller Position 1. The L Register which provides an indication of the Interval Timer should step each time the Start pushbutton is depressed.

11. Place the Disable Interval Timer switch to the On position (down). The Interval Timer should stop stepping after two (2) depressions of the Start pushbutton.

12. Place ROS Address Compare switch to Sync. (up).

13. Set the ROS Address 29F in Data Keys (positions 20 to 31).

14. Place the ROS Address Compare switch to Stop (down).

15. Depress the Interrupt pushbutton.

16. Check Display 3, Roller Position 3. M register, Bit 25, (External Interrupt Code), should be set.

17. Set Ros Address switch to Sync. and depress the Stop and Reset pushbuttons.

d. Reset pushbutton, Single Cycle and ROS Address Compare switches.

1. Set Rate switch to Single Cycle.

2. Enter ROS Address DD 6 in the Data keys (positions 20 to 31) and place ROS Repeat Instruction switch on.

3. Place Data keys 0 to 7 down.

4. Depress Start pushbutton twice. Place ROS Repeat Instruction switch off.

5. Depress Start pushbutton 4 times. This should load the following data into the L, R, H, and M registers: $FF000DD6_{16}$.

6. Set Rate switch to Process and depress the Reset pushbutton. Check to see that the registers R, H, and M set in Step 5 have been reset. The L register will contain the Current PSW.

7. Enter ROS Address 2B0 in Data keys (positions 20 to 31) and set Sync Box to ROS Address position and scope for a positive pulse every 2.5 microseconds.

8. Place the ROS Address Compare switch to Stop and check the current ROS Address on Display 4, Roller Position 7 for Address 2B0.

9. Place ROS Address Compare switch back to Sync.

e. Check Control switch, Store, Display, Check Reset pushbutton and Reverse Parity switch.

1. Set Storage Select to MACH Storage.

2. Set Check Control switch to Process.

3. Depress Reset pushbutton.

4. Key the following data into Storage:

Address	Data
0030	00 00 00 00
0034	00 00 00 00
0070	00 00 00 00
0074	00 00 00 00
0100	1A 12 07 F3

5. Display the above locations to insure correct data transfer.

6. Set Storage Select to Local Store. Enter the following data in Local Storage, using Address keys 22 to 27, and the Data keys.

Address	Data
17	00 00 00 00
31	00 00 00 00
32	00 00 00 00
33	00 00 01 00

7. Display the above locations to insure correct data transfer using the L Reg., Display 3, Roller position 1.

8. Set Check Control to Stop. Depress Reset pushbutton.

9. Set Address 0100 into the Address keys.

10. Depress Set IC pushbutton.

11. Depress the Start pushbutton. IOCE should run with no checks.

12. Depress the Stop pushbutton. The IAR should be setting at 0100 or 0102. The Manual indicator should be on.

13. Set Check Control switch to Disable.

14. Set Storage Select to Local Store.

15. Set Reverse Data Parity switch on (down).

16. Enter the following data into Local Store:

Address	Data
31	00 00 00 00
32	00 00 00 00

17. Display the above locations to insure correct data transfer using the L Reg., Display 3, Roller position 1.

18. Set Reverse Parity switch off (up). Depress Check Reset.

19. Enter the following data into Local Store:

Address	Data
33	00 00 01 00

20. Display the above locations to ensure correct data transfer using the L Reg., Display 3, Roller Position 1.

21. Set both Data and Address keys to zero and set Check Control switch to Process.

22. Set Storage Select switch to MACH Store.

23. Set Address 0100 into Address keys and depress Set IC pushbutton.

24. Depress Start pushbutton. Machine should run with Half Sum Checks on. Check Display 4, Roller Position 6, Half Sum Checks should be on.

25. Set Check Control switch to Disable. Machine should still run.

26. Depress Check Reset pushbutton. Half Sum Checks should go Off while the pushbutton is depressed, and they will go On when the pushbutton is released.

27. Set Check Control switch to Stop. Machine stops with IAR setting at 0100, 0102, or 0104. Master Check on.

28. Set Check Control to Process.

29. Depress Reset pushbutton, set Address 0100 into Address keys and depress Set IC and Start pushbuttons. IOCE should run with no checks.

f. Set IC pushbutton.

1. Depress the Stop and Reset pushbuttons.

2. Set any address into Address keys, positions 8 to 31.

3. Depress Set IC pushbutton. The IAR should match the Address keys.

g. Set CCR switch and Register Set pushbutton.

1. Depress Reset pushbutton.

2. Place Register Set CCR switch to CCR (down).

3. Turn roller to Display 3, Position 7.

4. Set any System Configuration in Data keys (positions 0 to 23).

5. Depress Register Set pushbutton and check that the CCR matches the Data keys.

6. Set Data keys off and depress Register Set pushbutton.

7. Set the Register Set CCR switch off.

h. Set ATR switch.

1. Depress Reset pushbutton.

2. Place ATR1/ATR2 switch to ATR1.

3. Enter 12 34 56 and 78 into Data keys and depress Register Set pushbutton.

4. Check Display 1, Roller Position 7. It should contain 12 34 and 56.

5. Place ATR switch to ATR2, and depress Register Set pushbutton.

6. Check Display 1, Roller Position 8. The register should contain $78\ 12\ 34_{16}$.

7. Set the Register Set ATR switch off.

i. Log Out pushbutton.

This pushbutton will be checked out in Spec. Section 5.2.14 which demonstrates the CE, SE, DE and IOCE log-out operation.

j. Address Compare switches (IAR and Storage)

1. Depress Reset pushbutton.

2. Set Rate switch to Process.

3. Set Storage Address Compare to Process.

4. Set the Storage switch to MACH.

5. Key the following program into Storage:

Address	Data
0000	00 00 00 00
0004	00 00 01 00
0100	82 00 04 00
0200	82 00 0F 00
0300	82 00 06 00
0400	00 00 00 00
0404	00 00 0F F0
0500	00 00 00 00
0504	00 00 03 00
0600	00 00 00 00
0604	00 00 01 00
0F00	00 00 00 00
0F04	00 00 0F FE
0FF0	82 00 05 00

6. Display the above locations to insure correct data transfer.

7. Depress the Reset pushbutton.

8. Depress the PSW Restart pushbutton.

9. Enter 0300 in Address keys. Set Sync Box to STOR ADR position and scope for a pulse 70 to 130 nsecs wide at the 1 volt level.

10. Set the Storage Address Compare switch to Stop. The Manual Indicator should be on. (IAR at 0100).

11. Set the Storage Address Compare switch to Process.

12. Set Address switches to 0200.

13. Set the IAR Repeat Instruction switch to on (down); bits 20 through 30 should be on in IAR.

14. Set IAR Repeat Instruction switch to off (up).

15. Set Rate switch to Instruction Step.

16. Depress the PSW Restart pushbutton. The IAR should indicate Address 0100.

17. Depress the Start pushbutton. The IAR should now step to 0FF0.

18. Depress the Start pushbutton once more. The IAR should now indicate Address 0300.

19. Set Rate switch back to Process.

20. Depress Reset pushbutton.

k. ROS Repeat Instruction and Force Indicator switches.

1. Set Rate switch to Process.

2. Enter ROS Address F96 into Data keys (positions 20 to 31).

3. Set ROS Repeat Instruction switch on. The Block Indicator should come on and some roller indicators should go out.

4. Set the Force Indicator switch on (down). Indicators previously out should now come on. Set Repeat Instruction switch off, and depress Reset pushbutton.

1. MACH Storage Test switches

1. Set Storage Select switch to MACH.

2. Set MACH Storage Test switch to Worst.

3. Set Write Toggle switch to Write and depress Start.

4. Set Write Toggle switch to Read (up).

5. Set Stop on Check switch to Stop on Check.

6. Storage should ripple error free.

7. Set Stop on Check switch off and depress the Stop and Reset pushbuttons.

8. Set MACH Storage Test switch to Reverse Worst.

9. Repeat Steps 3, 4, 5 and 6.

10. Set MACH Storage Test switch back to process.

11. Depress Reset pushbutton, set Stop On Check switch off.

12. Clear the MACH Storage in this IOCE.

m. Repeat the above test for each IOCE.

Upon completion of the above tests and obtaining the correct indications, the test will be considered acceptable.

5.1.3 Storage Element. This test procedure assumes that the SE under test is SE #1. When a different SE is required, TAG switches 1 through 4 should be set to a 1 (down), as shown below.

SE NO.	TAG SWITCH SETTINGS
	1 2 3 4
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0

a. Indicators Switch

1. Set Indicators Switch to Test. All panel indicators should light. Return switch to Normal.

b. Reset Pushbutton

1. Depress the Stop, then Reset pushbutton.

2. Observe that the Address Counter equals zero, with PA and PB On.

3. Observe Test Stop indicator is On.

c. Set Configuration Pushbutton

1. Set all Storage Data Entry keys to One (down).

2. Set Mark switch 4 to CCR-1.

3. Depress Set Configuration pushbutton.

4. Observe all bits On in CCR-1 (upper byte).

5. Set Mark switch 4 to Zero.

6. Set Mark switch 7 to CCR-2

7. Depress Set Configuration pushbutton.

8. Observe all bits On in CCR-2 (lower byte).

d. Storage Select

1. Set up switches as follows:

a. Stop On Chk Test switch to Stop On Chk Test position.

b. Set Key switch to Data

c. Set Hi-Lo to Lo (up)

d. Set Marks to all Ones (down).

e. Set E/O switch to Odd (down)

2. Depress Reset then Start pushbuttons.

3. Observe Address Register Odd rippling.

4. Depress Stop pushbutton.

5. Set Store/Fetch Switch to Fetch.

6. Depress the Start pushbutton.

7. Observe Fetch Odd indicator On and Address Register Odd rippling with no checks.

8. Depress Stop pushbutton.

9. Set Store/Fetch switch to Store.

10. Set E/O switch to Ø (up).

11. Depress the Start pushbutton.

12. Observe Address Register Even rippling.

13. Depress Stop pushbutton.

14. Set Store/Fetch switch to Fetch.

15. Depress the Start pushbutton.

16. Observe Fetch Even indicator on and Address Register Even Stepping with no checks.

17. Depress Stop pushbutton.

18. Set Worst Case/Data Keys to Worst Case.

19. Set E/O switch to Odd (down).

20. Set Store/Fetch to Store.

21. Repeat steps 2 through 17.

22. Return Worst Case/Data Keys to Data Keys.

23. Set Hi/Lo switch to Hi (down).

24. Set E/O switch to Odd (down).

25. Set Store/Fetch to Store.

26. Repeat steps 2 through 22.

e. Key Switch

1. Set Store/Fetch to Store.

2. Set Key Switch to Set.

3. Set In Key switches, P-off (up) and 0 thru 4 On (down).

4. Depress Reset and Start pushbuttons.

2. Depress Reset then Start pushbuttons.

3. Observe Address Register Odd rippling.

4. Set Store/Fetch switch to Fetch.

5. Observe Fetch Odd indicator On and Address Register Odd rippling with no checks.

6. Set Store/Fetch switch to Store.

7. Depress the Stop pushbutton.

8. Set E/O switch to Ø (up).

9. Depress the Start pushbutton.

10. Observe Address Register Even rippling.

11. Set Store/Fetch switch to Fetch.

12. Observe Fetch Even indicator on and Address Register Even Stepping with no checks.

13. Depress Stop pushbutton.

14. Set Worst Case/Data Keys to Worst Case.

15. Set E/O switch to Odd (down).

16. Set Store/Fetch to Store.

17. Repeat steps 2 through 13.

18. Return Worst Case/Data Keys to Data Keys.

19. Set Hi/Lo switch to Hi (down).

20. Set E/O switch to Odd (down).

21. Set Store/Fetch to Store.

22. Repeat steps 2 through 18.

e. Key Switch

1. Set Store/Fetch to Store.

2. Set Key Switch to Set.

3. Set In Key switches, P-off (up) and 0 thru 4 On (down).

4) Depress Reset and Start pushbuttons.

5. Observe Storage Protect In Key and Out Key Register indicators 0-4 On, and P Off.

6. Depress Stop pushbutton.

7. Set Key Switch to Insert.

8. Depress Start pushbutton.

9. Observe Storage Protect In Key and Out Key Register indicators 0-4 On and P Off.

10. Depress Stop. Key Switch to Data.

f. Restore good parity in Storage

1. Set the Hi/Lo switch to Ripple.

2. Set Store/Fetch to Store.

3. Set Data Entry keys P On (down) and 0 thru 7 Off (up).

4. Depress Start. Depress Stop, Set E/O switch to Even (up). Depress start.

5. Depress Stop pushbutton.

g. Priority Tests

1. Set Priority/Storage switch to Priority.

2. Set Priority switches as follows: IOCE 1, 3, CE 2, 4 Even (down). IOCE 2, CE 1, 3 Odd (up).

3. Set Single Cycle/Normal switch to Single Cycle.

4. Depress Reset pushbutton.

5. Depress Start pushbutton one time and observe indicators as follows: (1=On, 0=Off)

Priority Status Request		Priority Status Response	
IOCE	CE	IOCE	CE
011	1111	100	0000

6. Return Priority/Storage switch to Storage, Single Cycle/Normal to Normal and Depress Reset pushbutton.

h. Test and Set

1. Set TAS switch to TAS position.

2. Set Single Cycle/Normal to Single Cycle.

3. Set Stop On Check test to Off.

4. Set Store/Fetch to Fetch.

5. Set Mark switch 3 down, - all others up.

6. Set Address keys 5-19 to Force 0.

7. Depress Reset pushbutton.

8. Depress the Start pushbutton twice.

9. Observe Data Bus byte 3 (bits 24-31) all ones (all parity bits are on) and Compare Check indicator On.

10. Depress Stop pushbutton.

11. Return the TAS switch to Off.

12. Return Address keys 5-19 to Ripple.

i. Cancel Switch

1. Set all Marks to One (down).

2. Set Data Entry keys to all Ones (down).

3. Set Store/Fetch to Store.

4. Set Single Cycle/Normal to Single Cycle.

5. Set Stop On Check Test to Stop on Check Test position.

6. Set Worst Case/Data keys to Data keys.

7. Depress Reset then Start pushbuttons.

8. Observe all Data Bus indicators including Parity bits Off.

9. Set Cancel to Cancel position.

10. Set Data Entry keys 0-7 zero, P one.

11. Depress Reset and Start pushbuttons.

12. Observe all Data Bus indicators Off. (all parity bits are on).

13. Set Data Entry keys to all Ones.

14. Set Store/Fetch to Fetch.

15. Set Cancel to Off.

16. Depress Reset then Start pushbuttons.

17. Observe all Data Bus indicators On.

j. Stop On Check Test and Reverse Address Parity switches.

1. Set Store/Fetch to Store.

2. Set Single Cycle/Normal to Normal.

3. Depress Reset then Start pushbuttons.

4. While running with no checks, set Reverse Addr. Parity to PB.

5. Observe Even SAR Check and Test Stop indicators On.

6. Set Reverse Addr. Parity to Off.

7. Depress Reset then Start pushbuttons.

8. Set Reverse Addr. Parity to PA.

9. Observe Even SAR, Storage Protect Address Check and Test Stop indicators On.

10. Set Reverse Addr. Parity to Off.

11. Depress Reset, Start and Stop pushbuttons.

k. Log Out Switch Test

1. Set E/O switch to Even (Up).

2. Set all Mark keys to One (P-7 down).

3. Set Data Entry keys to all Ones.

4. Depress Reset then Start pushbutton.

5. Depress Stop pushbutton.

6. Set Log Out Stop switch to Log Out Stop.

7. Set Data Entry keys 0, 1, 2, to Zero.

8. Observe Log Stop indicator On, and all Data Bus indicators are On.

9. Set Log Out Stop switch to Off.

10. Depress Reset pushbutton.

l. Multi-Accept Check

1. Set Store/Fetch to Fetch.

2. Set TAS to ON.

3. Set Key switch to Set position.

4. Depress Start pushbutton.

5. Observe Multi-Accept indicator is On.

6. Depress Stop pushbutton.

7. Set TAS to Off.

m. Auto Mode Check

1. Set Reverse Addr. Parity to PA.

2. Set Reset Mode switch to Manual position.

3. Set Store/Fetch to Store.

4. Set Storage/Priority to Storage.

5. Set Stop On Check test Off.

6. Set Data Entry keys to all zeroes, P to one.

7. Set all Marks to One (down).

8. Set Key Switch to Data position.

9. Depress Reset Start then Stop pushbuttons.

10. Observe that the Storage Address Even and Storage Protect Address Check indicators are on.

11. Set Reset Mode switch to Auto position.

12. Observe the Even Address Register and Address Counter are rippling.

13. Set Reset Mode switch to Manual position.

14. Depress Stop pushbutton.

n. Repeat tests a through m for each SE.

Upon completion of the above test and obtaining the correct indications, the test will be considered acceptable.

5.1.4 Storage Timing and Access Demonstration. This demonstration verifies that the storage cycle time, and the basic timing source (BSM clock), of each SE operates at the required rate. This demonstration will be run using the test panel on the SE.

a. Test Panel Setup

1. Set switches according to section 4.1.3.

2. Set Key Switch to Data position.

3. Set good parity in storage. (Refer to para. 5.1.3 f).

4. Set Hi/Lo switch to Lo (Up).

5. Set Store/Fetch to Fetch, and Priority/ Storage to Priority.

6. Set Priority switches as follows:

IOCE 1, 2, 3 - Off

CE 1, 3 - Odd; 2, 4 - Even

7. Depress Start

b. Maintenance personnel will set up a scope to display the time from CE-1 Select (odd) to CE-2 Select (even). The time between the select pulses should be no greater than 400 nanoseconds.

1. Test points are as follows:

Channel 1; - Select Odd	03C-B3K4B10	MT255
Channel 2; - Select Even	03C-B3L4B10	MT254

c. Maintenance personnel will set up the scope to display the time from rise of one X gate to the next (not to exceed 800 ns), and at the same time observe the X Drive pulses occurring within the same time period that the X Gate is active.

1. Scope set up as follows:

   Channel 1 - -X Gate Ø3B-B1D2B13 MGØØ6
   Channel 2 - +X Drive Ø3B-B1E4BØ5 MDØØ4
   Sync - Int., Negative, Chan 1
   Vertical - .2V per div.
   Horiz. Sweep Time - .1 usec per div.

2. Observe waveform similar to Fig. C.

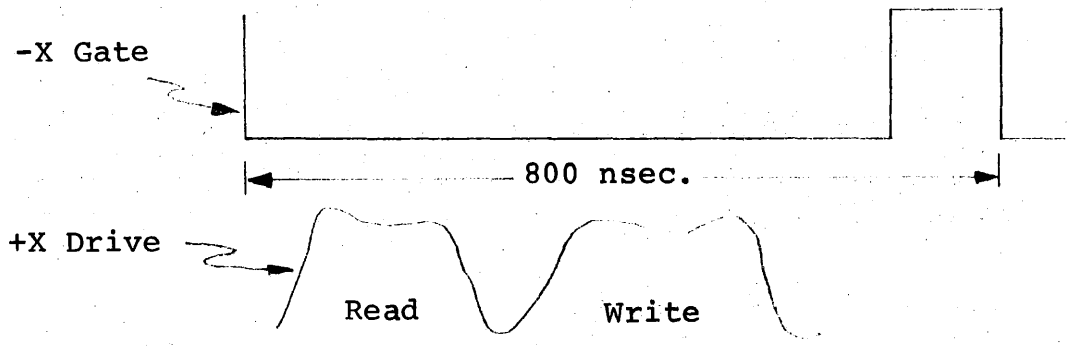

Fig. C

d. Repeat test for each SE.

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5.1.5 Display Element - The following section will be a manual demonstration of the Display Element maintenance panel switches.

The Display Element which is being tested must be in state 0 with the Test switch On. Initial switch settings should be as described in Section 4.

a. Indicator Test switch

1. Set the Indicator Test switch to the Indicator Test position.

NOTE: The switch must be held in the Test position.

2. Observe that all maintenance panel indicators are On.

3. Set the Indicator Test switch to the Inactive position.

4. Observe that all maintenance panel indicators are Off.

5. Set the Indicator Test switch to the Normal position.

b. Configuration Register switches and Set Configuration pushbutton.

1. Set all Configuration Register switches to the 1 position.

2. Depress the Set Configuration pushbutton.

3. Observe that all Configuration Register indicators and the Configuration Redundancy and Parity Check indicators are On.

4. Set all Configuration Register switches to the 0 position.

5. Depress the Set Configuration pushbutton.

6. Observe that all Configuration Register indicators are Off and the Configuration Parity Check indicator is On.

7. Set the following Configuration Register switches to the 1 position (all other Configuration Register switches to the 0 position): P_0, 1A, 2B, 3C, 4D, P_1, P_4, SCON 1-4, P_7 and CE 1-4.

8. Depress the Set Configuration pushbutton.

9. Observe that the Configuration Register indicators agree with the setting of the Configuration Register switches and the Configuration Redundancy and Parity Check indicators are Off.

c. In keys and Stop On Check switches and the Start, Stop, and General Reset pushbuttons.

1. Set the Key switch to the Set position.

2. Depress the General Reset and Start pushbuttons.

3. Observe that the Parity bits and SCON 1-4 of the Configuration Register are On.

4. Set the In Keys parity switch to the 0 position.

5. Observe that the Storage Protect Key Check indicator is On and the In Key parity indicator is Off.

6. Set the In Keys parity switch to the 1 position.

7. Set the Stop On Check switch to the Stop on Check position.

8. Set the In Keys parity switch to the 0 position.

9. Observe that the In Keys parity indicator is Off and the Storage Protect Key Check and Stop indicators are On.

10. Set the In Keys parity switch to the 1 position.

11. Set the Stop On Check switch to the Off position.

12. Depress the General Reset and Start pushbuttons.

13. Observe that the Storage Protect Key Check and Stop indicators are Off.

14. Depress the Stop pushbutton.

15. Observe that the Stop indicator is On.

16. Set the Key switch to the Off position.

d. All One's Test - Store

1. Set the switches as follows:

   Stop On Check - Stop On Check
   Mark Keys - All to 1 position
   Store - Store
   Storage Data Entry Keys - All to 1 position
   In Keys - 0-4 to 0 position, P to 1 position
   Address Keys - All to Ripple position
   Data Keys/Worst Case - Data Keys

2. Depress the Start pushbutton

3. Observe the following:

   All Check indicators are Off.
   All Odd Storage Address Register indicators are rippling.
   All Mark Odd indicators are On.

4. Depress the Stop pushbutton.

5. Set Store Switch - Off.

6. Depress General Reset and Start pushbuttons.

7. Observe the following:

   Fetch Odd indicator - On
   All Data Register indicators - On
   All Check indicators - Off

8. Set Storage Data Entry switch 3 to the 0 position.

9. Observe that the Compare Check and Stop indicators are On.

10. Return Storage Data Entry switch 3 to the 1 position.

11. Set the CE 1 Priority Select switch to the Even position and repeat steps 1-10. All observations should be made using the Even indicators.

12. Set the CE 1 Priority Select switch to the Odd position.

13. Depress the Check Reset pushbutton.

e. Data Error Test

1. Set the Stop On Check switch to the Off position.

2. Set the Store switch to the Store position.

3. Depress the Start pushbutton.

4. Set Mark Key 2 switch to the 0 position.

5. Observe that the Mark Odd 2 indicator is Off (all others On) and the Mark Odd Check indicator is On.

6. Set Storage Data Entry switch 3 to the 0 position.

7. Set Mark Key switch 2 to the 1 position.

8. Observe that all Odd Data Byte Check indicators are On and all bits of the Odd Storage Address Register are rippling.

9. Set the Stop On Check switch to the Stop On Check position.

10. Observe that the Address Register is not rippling and the Stop indicator is On.

11. Set the Auto Restart switch to the Auto Restart position.

12. Observe that all bits of the Odd Storage Address Register are rippling. (slower rate)

13. Set all Storage Data Entry switches to the 1 position.

14. Set the Auto Restart switch to the Off position.

15. Depress the Stop pushbutton.

f. All Zero's Test

1. Set the switches as follows:

   Mark Keys - All to 1 position

   Storage Data Entry Keys - 0-7 to 0 position, P to 1 position

   Store - Store

   Stop On Check - Stop On Check

2. Depress the General Reset and Start pushbuttons.

3. Observe that all Check indicators are Off.

4. Depress the Stop pushbutton.

5. Set the Store switch to the Off position.

6. Depress the Start pushbutton.

7. Observe that the Data Reg parity indicators are On and that all Check indicators are Off.

8. Depress the Stop pushbutton.

9. Set the Storage Data Entry P switch to the 0 position.

10. Depress the Start pushbutton.

11. Observe that the Compare Check indicator is on.

12. Depress the Stop pushbutton.

13. Set the CE 1 Priority Select switch to the Even position and repeat steps 1-12.

14. Set the CE 1 Priority Select switch to the Odd position.

g. Test and Set

1. Set the switches as follows:

   Mark Keys - All to 1 position

   Key - Off

   Store - Store

   Storage Data Entry Keys 0-7 to 0 position, P to 1 position.

2. Depress the General Reset, Start, and Stop pushbuttons.

3. Set the switches as follows:

Store - Off

Mark Keys - 3 to 1 position, others to 0 position.

TAS - TAS

Stop On Check - Stop On Check

4. Depress the General Reset and Start pushbuttons.

5. Observe the following:

Compare Check indicator is On.

Data Register byte 3 and all parity indicators are On and all others are Off.

Stop indicator is On.

Mark Odd indicator 3 is on and all others are Off.

Odd fetch indicator is On.

Address Register bits P_A and 14 are On in Odd SAR.

6. Set the switches as follows:

Mark Keys - All to 1 position

TAS - Off

Store - Store

7. Depress the General Reset, Start, and Stop pushbuttons.

h. Storage Address Register and Storage Address Protect Check

1. Set the Address Keys P_A, 1, P_B and 8 to the Force 1 position, and all others to the Force 0 position.

2. Depress the Start pushbutton.

3. Observe that the Odd SAR Check and Storage Protect Address Check indicators are On.

i. Storage Protect Key Check

1. Set the switches as follows:

   Stop On Check - Off

   Store - Off

   In Keys - All to 0 position

   Address Keys - All to Ripple position

   Key - Set

2. Depress the General Reset and Start pushbuttons.

3. Observe that the Storage Protect Key Check indicator is On.

4. Set In Keys P switch to the 1 position.

5. Depress the Check Reset pushbutton.

6. Observe that the Storage Protect Key Check indicator is reset.

j. BSM Worst Case Pattern Test

1. Set the switches as follows:

   Key - Set

   In Key - P to 1 position, all others to 0 position.

   Address Keys - All to Ripple position.

   Stop On Check - Off

2. Depress the General Reset and Start pushbuttons.

3. Observe that the Odd Storage Address Register bits P_A-7 are rippling and P_B is on..

4. Depress the Stop pushbutton.

5. Set the switches as follows:

   Store - Store

   Key - Off

   Data Keys/Worst Case - Worst Case

   Stop On Check - Stop On Check

   Mark Keys - All to 1 position

6. Depress the General Reset and Start pushbuttons.

7. Observe the following:

   Out Key Register parity bit is On.

   All Odd Storage Address Register indicators are rippling.

   All Check indicators are Off.

8. Depress the Stop pushbutton.

9. Set the Store switch to the Off position.

10. Depress the General Reset and Start pushbuttons.

11. Observe the following:

   Out Key Register parity indicator is On.

   Data Register parity and data bit indicators are On.

   All Odd Storage Address Register indicators are rippling.

   All Check indicators are Off.

12. Depress the Stop pushbutton.

k. Interleave Checkerboard Pattern Test

1. Set the switches as follows:

   Store - Store

   Address Keys - All to Ripple position

   Priority/Storage - Priority

   Stop On Check - Stop On Check

   Data Keys/Worst Case - Data Keys

   Key - Off

   Priority Select - CE 1 to Odd, CE 2 to Even, all others to Off

   Mark Keys - All to 1 position.

   In Keys - P to 0, 0-4 to 1.

   Storage Data Entry - P, 1, 3, 5, 7 to 1 position, 0, 2, 4, 6 to 0 position.

2. Depress the General Reset and Start push-buttons.

3. Observe that no Check indicators are On.

4. Depress the Stop pushbutton.

5. Set the Store switch to the Off position.

6. Depress the Start pushbutton.

7. Observe that Data Register indicators for parity and odd numbered bits are on in each byte and no Check indicators are On.

8. Depress the Stop pushbutton.

9. Set the Store switch to the Store position.

10. Set the Storage Data Entry switches 1, 3, 5 and 7 to the 0 position and switches P, 0, 2, 4 and 6 to the 1 position.

11. Depress the Start pushbutton.

12. Observe that no Check indicators are On.

13. Depress the Stop pushbutton.

14. Set the Store switch to the Off position.

15. Depress the Start pushbutton.

16. Observe the Storage Data Register indicators for parity and even numbered bits are on in each byte and all Check indicators are Off.

17. Depress the Stop pushbutton.

1. Local Store Test

1. Set the switches as follows:

   Storage Select - Local

   Store - Store

   Address Keys - 1-14 to Force 1, P_A and P_B to Force 0

   Priority Select - CVG 1-24 to On, CE 1-4 to Off.

2. Depress the Start pushbutton.

3. Set the Store switch to the Off position.

4. Set the Indicator Selection switch to the A position.

5. Set the Priority Selection switch for CVG 1 On and all others Off.

6. Depress the Start pushbutton.

7. Observe that the Odd Address Register indicators agree with the Address Key switches.

8. Repeat steps 1-7 using Address Keys P_A, 1, 3, 5, 7. P_B, 8, 10, 12, and 14 set to Force 1 and all others set to Force 0.

m. Log Out Pushbutton

1. Set the switches as follows:

   Store - Off

   Priority/Storage - Storage

   Data Keys/Worst Case - Data Keys

   Storage Select - Main

   Single Cycle - Single Cycle

   Key - Set

   In Keys - 0-4 to 1, P to 0

   Mark Keys - All to 1 position

   Indicator Selection - STO

   Address Keys - 1-7 and P_B to Force 1, 8-14 and P_A to Force 0

   Priority Select - CE 1 to Even, all others to Off

   Storage Data Entry Keys - All to 1

2. Depress the General Reset and Start pushbuttons.

3. Set the Key switch to the Off position.

4. Set the Store switch to the Store position.

5. Depress the Start pushbutton.

6. Depress the OBS and OTC pushbuttons which are located on the other end of the Display Element frame.

7. Set all Log Address Keys to the 0 position.

8. Set the Log Mode switch to the Log mode position.

9. Depress the Start pushbutton.

10. Observe that all Data Register indicators are On.

11. Set Log Address Key 1 to the 1 position.

12. Depress the Start pushbutton.

13. Observe that the following Data Register indicators are On: 0-15, 17-24, 32, 34, 43-47, 49-53, 59 and 60.

14. Set the switches as follows:

    Log Mode - Off

    Priority Select - CE 1 to the Odd position.

    Key - Set

    Store - Off

15. Depress the General Reset pushbutton.

16. Repeat Steps 2-6.

17. Set the switches as follows:

    Log Mode - Log Mode
    Log Address Keys - 1 and 3 to 0 position,
    2 to 1 position.

18. Depress the Start pushbutton.

19. Observe that all Data Register indicators are On.

20. Set Log Address Key 1 to the 1 position.

21. Depress the Start pushbutton.

22. Observe that the following Data Register indicators are On: 0-15, 17-24, 32 and 34.

23. Set the Log Mode switch to the Off position.

24. Depress the General Reset pushbutton.

25. Set all Configuration Register switches to the 1 position.

26. Depress the Set Configuration pushbutton.

27. Observe that the Configuration Redundancy and Parity Check indicators are On.

28. Set the Log Mode switch to the Log Mode position.

29. Set Log Address Keys 1 and 2 to the 0 position, 3 to the 1 position.

30. Depress the Start pushbutton.

31. Observe that Data Register indicators 0-31 are On.

32. Set Log Address Key 1 to the 1 position.

33. Depress the Start pushbutton.

34. Observe that the following Data Register indicators are On: 10, 16-31, 32 and 42-45.

NOTE: Bits 38-41 should reflect the DE physical address of the Display Element being tested (6_{16}-A_{16}).

35. Set the Log Mode switch to the Off position.

36. Set the Single Cycle switch to the Off position.

n. Half Word Counter Check

1. Set the Indicator Selection switch to the A Position.

2. Depress the General Reset and Stop pushbuttons.

3. Depress the Pulse DG pushbutton.

4. Observe that the Half Word Counter indicator 1 is On and indicators 2, 4 and 8 are Off.

5. Depress the Pulse DG pushbutton fourteen (14) times and observe that the Half Word Counter increments once for each depression.

6. Depress the Pulse DG pushbutton.

7. Observe that the Half Word Counter indicators are all Off.

8. Set the Priority/Storage switch to the Priority position.

9. Set the Single Cycle switch to the Single Cycle position.

10. Depress the General Reset pushbutton.

11. Observe that all Start of Display indicators are On.

12. Depress the Refresh Pulse pushbutton.

13. Observe that all Start of Display indicators are Off.

p. Repeat tests a through n for each DE. Upon completion of the above test and obtaining the correct indications, the test will be considered acceptable.

5.1.6 Display Element Timing and Access Demonstration. The following section will be a verification of the performance of the 7289-04 Display Element, as specified in 9020D/E Design Data.

5.1.6.1 Storage Section - This demonstration verifies that the storage cycle time, and the basic timing source (BSM clock), of each DE operates at the required rate. This demonstration will be run using the test panel on the D/E.

a. Test panel setup

1. Set switches according to section 4.1.4.

2. Set good parity in storage. (Refer to para. 5.1.5 F).

3. Set Store switch to Off, and Priority/Storage to Priority.

4. Set Priority Select switches as follows: CE 1 - Odd; CE 2 - Even; CE 3 and 4 Off.

5. Set Configuration Register switches P0,1A,1B,P1,P4, P7 On.

6. Depress the Set Configuration pushbutton.

7. Depress the Start pushbutton.

b. Maintenance personnel will set up a scope to display the time from CE 1 Select (odd) to CE 2 Select (even). The time between the select pulses should be no greater than 400 nanoseconds.

1. Test Points are as follows:

Channel 1 - -Select Odd 03C-B3K4B10 MT255
Channel 2 - -Select Even 03C-B3L4B10 MT254

c. Maintenance personnel will set up the scope to display the time from rise of one X gate to the next (not to exceed 800 ns), and at the same time observe the X Drive pulses occurring within the same time period that the X Gate is active.

1. Set Priority Select switches as follows:

CE 1 Odd; CE 2 and 3 Even; CE 4 Off

2. Scope set up as follows:

Channel 1 - -X Gate 03A-B1D2B13 MGØØ6
Channel 2 - + X Drive 03A-B1E4BØ5 MDØØ4

Sync - Int., Negative, Chan 1
Vertical - .1V per div.
Horiz. sweep time - .1 usec per div.

3. Observe waveform similar to Fig. A.

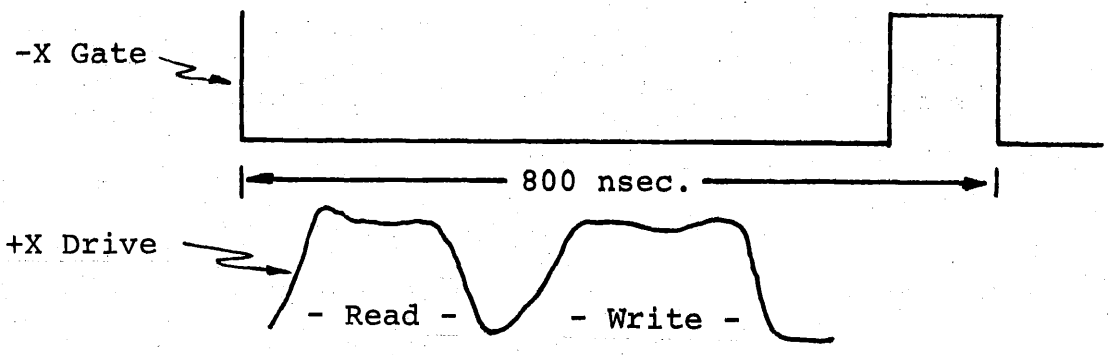


Fig. A

5.1.6.2 Controls Section - The specific performance characteristics to be tested are as follows:

1. Ability to refresh at a 55Hz rate.

2. Transfers of images that require an excess of 18.2 milliseconds will be asynchronous (no waiting for the start of the next refresh time).

3. A quadword access will be made available to each CVG once every 21.6 microseconds.

4. For a given display load, the time between successive transmissions of a given piece of data shall not vary, due to the DE, by more than ±125 microseconds.

GENERAL DESCRIPTION OF TEST:

The use of a Maintenance Subsystem is not required since the performance characteristics being tested are not controlled or affected by the operation of the other elements of the 9020E System. The test is performed in a manner that requires only the 7289-04 Display Element, an oscilloscope, and this specification. All operations required for setup of tests are performed from the Maintenance Panel of the Display Element.

a. Initial Conditions

1. Initial switch settings as specified in Section 4.

2. Set the Test/Normal switch to Test.

3. Set Configuration:

Turn on the following Configuration Register switches:

P_0,1A,2B,3C,4D,P_1,P_4,P_7

4. Depress the Set Configuration pushbutton.

5. Set all of the Address Keys to Ripple.

6. Set all of the Storage Data Entry switches to One.

7. Set all of the Mark Keys to One.

8. Set the Store switch to Store.

9. Set the Priority Select switch for CE 1 to Odd. (Set all other Priority Select switches to Off.)

10. Set the Priority/Storage switch to Storage.

11. Depress the Start pushbutton.

12. Set the Priority Select switch for CE 1 to Even.

13. Depress the Stop pushbutton.

14. Set the following Address Keys to Force 1;
P_A,5,6,8,9,10 (Set all other Address Keys to Force 0)

15. Set the Priority Select switch for CE 1 to Odd.

16. Set Mark Key 0 to One and all others Zero.

17. Set the following Storage Data Entry switches to One; P,1,5,6,7 (All others to Zero)

18. Depress the Start pushbutton.

19. Depress the Stop pushbutton.

20. Set the Store switch to Off.

21. Depress the Start pushbutton.

22. Observe a value of 47 FF FF FF FF FF FF FF_{16} with odd parity in the Data Register indicators.

23. Depress the Stop pushbutton.

24. Set the Priority/Storage switch to Priority.

25. Set the Priority Select switch for CVG 1 to On.

b. Refresh Rate Timing (55Hz)

NOTE: All Sync and scope points in the following tests will be positive.

1. Depress the Start pushbutton.

2. Scope the Refresh Pulse at 02D B3J6B10.

NOTE: Best results are obtained if the main trace is dropped below the face of the scope and the intensity level is increased.

3. Observe the time between successive Refresh Pulses of 18.2 milliseconds.

c. Asynchronous CVG Operation

1. Sync the oscilloscope on End of Display for CVG 1 at 02C-A1B6D02. (Channel 1)

2. Scope the Start of Display for CVG 1 at 02C-A1B6B04. (Channel 2)

3. Observe the time between End of Display and Start of Display does not exceed 21.6 microseconds.

d. Quadword Availability to the CVG's

1. Sync the oscilloscope on the Refresh Pulse at 02D-B3J6B10.

2. Scope the CVG Select for CVG 1 at 02C-A1D4D07.

3. Observe the period between successive CVG Selects is no greater than 21.6 microseconds.

e. Successive Transmission Stability

1. Depress the Stop pushbutton.

2. Set the following Address Keys to Force 1; P_A,5,6,P_B,8,14
(Set all other Address Keys to Force 0.)

3. Set the Store switch to Store.

4. Set the Priority Select switch for CE 1 to Odd.

5. Set the Priority/Storage switch to Storage.

6. Set Mark Key 0 to One and all others Zero.

7. Depress the Start pushbutton.

8. Depress the Stop pushbutton.

9. Set the Store switch to Off.

10. Depress the Start pushbutton.

11. Observe a value of 47 FF FF FF FF FF FF FF_{16} with odd parity in the Data Register indicators.

12. Depress the Stop pushbutton.

13. Set the Priority/Storage switch to Priority.

14. Depress the Start pushbutton.

15. Scope the End of Display for CVG 1 at 02C-A1B6D02.

16. Use the Delayed Sweep feature of the oscilloscope to display the second End of Display signal on a sweep length of 500 microseconds.

17. Observe that the End of Display signal does not drift more than ±125 microseconds.

f. Repeat tests 5.1.6.1 and 5.1.6.2 for each DE

Upon completion of the above test and obtaining the correct indications, the test will be considered acceptable.

5.1.7 System Console - (9020D). The System Console Program (D6CA4) will check all console functions except Emergency Power Off, Initial Program Load, Lamp Test and Power Supply Select.

The Emergency Power Off function will be demonstrated in Spec Section 7.0.

The Initial Program Load function will be demonstrated by many tests in that the System Console will be utilized for some program loading.

5.1.7.1 The System Console switches will be checked as follows:

a. Lamp Test

1. Depress Lamp Test pushbutton. All indicators on the Operator's panel should light except Mode of Operation, Load, Invalid Selection, Test Mode and Enable.

2. Rotate the Lamp Test Select switch through each position to check Item #1 exceptions.

b. Power Supply Select

1. Check voltage on Console Meter.

2. Drop power to the System Console by depressing Power On pushbutton.

3. Rotate A-B Select switch to the opposite position.

4. Depress Power On pushbutton.

5. Power should cycle up on the selected power supplies. Power Check indicator should turn off and Power Sequence Complete should turn on.

Upon completion of the above tests and obtaining the correct indications, the test will be considered acceptable.

5.1.7.2 System Maintenance Monitor Console (SMMC) Interface. The following test will demonstrate the SMMC) Interface requirements from the System Console.

a. Mode of Operation Indicator

1. On Maintenance and Test panel, set Mode switch to Single Byte.

2. Set Test - Operate switch to Test.

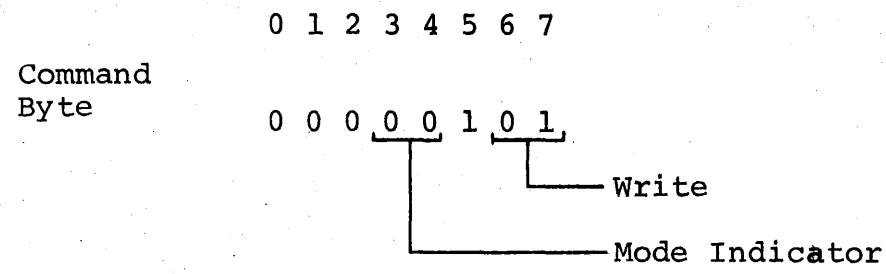
3. Set Control Unit Select switch to Console 1.

4. Depress Reset pushbutton.

5. The FAA observer may select a minimum of one alpha and a minimum of one numeric indicator to be tested.

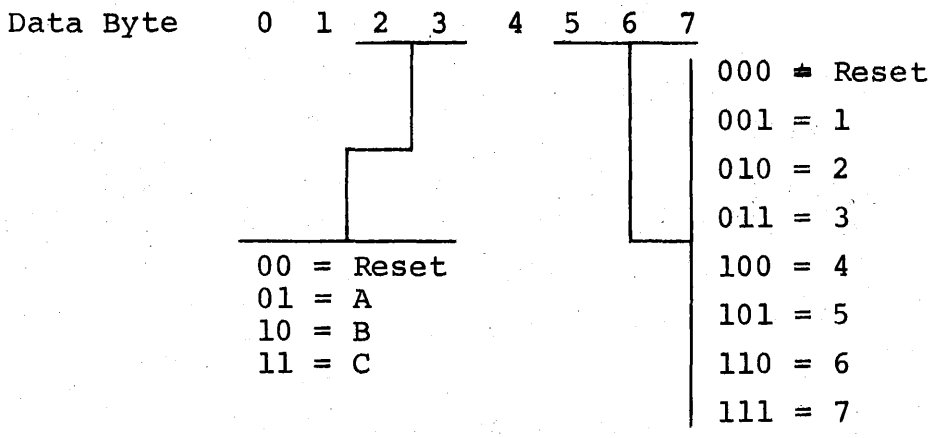
6. Using a voltmeter with a 510 ohm resistor across the meter terminals as a termination, measure the voltage at the output plug of the system console between ground and the pins for the corresponding selected indicators (use Appendix N for reference). The meter measurement should be within 0 to +.3V.

7. Place a command - write mode indicator - in the Bus Out switches. Set Parity Insert switch to Correct.



8. Depress Start pushbutton. When the operation stops, Status-In indicator should be On.

9. Place a data byte in the Bus Out switches, for the previously selected indicators.



10. Depress Start pushbutton. The Status In indicator should be On.

11. The Mode indicator, operated by the data byte in the Bus Out switches, should be On.

12. Again using the voltmeter with the termination, measure the voltage at the output plug for the selected indicators. The meter measurement should be within +4.50V to 5.75V.

b. System Configuration Registers

1. On Maintenance and Test Panel, set Mode switch to Single Byte.

2. Set Test-Operate switch to Test.

3. Set Control Unit Select switch to Console 1.

4. Depress Reset pushbutton.

5. The FAA observer may select any five configuration indicators to be tested.

6. Using a voltmeter with a 510 ohm resistor across the meter terminals as a termination, measure the voltage at the plug of the System Console, between ground and the pins for the corresponding selected indicators (use Appendix N for reference). The meter measurement should be within 0 to +.3V.

7. Place the following command byte in the Bus Out switches:

Bit 0 = 1 = Configuration Register 4
Bit 1 = 1 = Configuration Register 3
Bit 2 = 1 = Configuration Register 2
Bit 3 = 1 = Configuration Register 1
Bit 4 = 1
Bit 5 = 0 10 in bits 4, 5, = System Configuration Registers
Bit 6 = 0
Bit 7 = 1 01 in bits 6, 7 = Write

8. Depress Start pushbutton. When the operation stops, the Status-In indicator should be On.

9. Using the chart below to determine the data for the selected indicators, insert four data bytes, one at a time, into the Bus Out switches. After each insertion, depress Start pushbutton. Each time the console should stop with the Service In indicator On. (Four data bytes are needed for each system configuration register. For three configuration registers, 12 bytes are needed.)

1st Data Byte	2nd Data Byte	3rd Data Byte	4th Data Byte
Bit 0 = PAM-1	Bit 0 = SE-1	Bit 0 = SE-9	Bit 0 = not used
1 = PAM-2	1 = SE-2	1 = SE 10	1 = not used
2 = PAM-3	2 = SE-3	2 = not used	2 = not used
3 = TCU-1	3 = SE-4	3 = not used	3 = not used
4 = TCU-2	4 = SE-5	4 = CE-1	4 = not used
5 = TCU-3	5 = SE-6	5 = CE-2	5 = IOCE-1
6 = not used	6 = SE-7	6 = CE-3	6 = IOCE-2
7 = not used	7 = SE-8	7 = CE-4	7 = IOCE-3

10. The configuration indicators operated by the data bytes should be On.

11. Again using the voltmeter with the termination, measure the voltage at the output plug for the selected indicators. The meter measurement should be within +4.50V to 5.75V.

12. Depress Reset.

c. Power Check Indicators

1. The FAA observer will select a minimum of three power check indicators to be tested.

2. Using a voltmeter with a 750 ohm resistor across the meter terminals as a termination, measure the voltage at the output plug of the System Console between ground and the pins for the corresponding selected indicators (use Appendix N for reference). The meter should measure an open or ground.

3. Power will now be dropped at the selected units by the unit power On-Off switch.

4. Again using the voltmeter with the termination, measure the voltage at the output plug of the selected indicators. The meter measurement should be +24V ± 3V DC.

5. Restore power to the selected units.

6. Upon completion of the above test and obtaining the correct indicators the test will be considered acceptable.

5.1.8 Configuration Console (9020E) - The Configuration Console Program (D6CA6) will check all console functions except Emergency Power Off, Element Master Power Off, Initial Program Load, Lamp Test, and Power Supply Select.

The Emergency Power Off and Element Master Power Off functions will be demonstrated in Section 7.0.

The Initial Program Load function will be demonstrated by many tests in that the Configuration Console will be utilized for some program loading.

5.1.8.1 Configuration Console switches

a. Lamp Test

1. Depress the Lamp Test pushbutton.

2. Observe that all indicators on the Operators Panel light except Load, Enable, Invalid Selection, System Interlock and Test Mode.

3. Rotate the Lamp Test Select switch through each position to test the exceptions listed in step a.2.

b. Power Supply Select

1. Drop power to the SCCU portion of the Configuration Console by means of the Power On/Off switch.

2. Rotate the Power Supply Select switch to the opposite position.

3. Apply power by means of the Power On/Off switch.

4. Observe that the Power Check indicator is off and the Power Sequence Complete indicator is on.

5.1.8.2 System Console Control Unit (SCCU) Maintenance Panel

a. Lamp Test

1. Depress the Lamp Test pushbutton.

2. Observe that all indicators on the SCCU Maintenance Panel are on.

b. Control Unit Test Selection

1. Set the Test/Operate switch to Test.

2. Set the Control Unit Test Selection switch to the CNSL 1 position.

3. Observe that the Control Unit Test Selector Console indicator is on.

4. Repeat steps 2 and 3 for the CNSL 2 position. (and CNSL 3 position if the IOCE-3 feature is installed)

5. Set the Control Unit Test Selection switch to the 2821 position.

6. Observe that the Control Unit Test Selection 2821 indicator is on.

c. Reset

1. Set the Control Unit Test Selection switch to the CNSL 1 position.

2. Depress the Reset pushbutton.

3. Observe that the following indicators are on:

Test Control - Init Selection
Control Unit Test Selection - Console

d. Single Command

1. Set the Mode Select switch to the Single Command position.

2. Set the following Control Out switches on:
   Adr
   Sel

3. Set all Address switches to 0 with the Parity Insert switch to Correct.

4. Set all Bus Out switches to 0 with the Parity Insert switch to Correct.

5. Depress the Start pushbutton.

6. Observe that the following indicators are on:
   Control In - Sel
   Test Control - Init Sel and Adr Out Gate

7. Depress the Reset pushbutton.

8. Set Address switch 7 ON.

9. Depress the Start pushbutton.

10. Observe that the following indicators are on:
   Bus In - bit 7
   Console Control Unit ADR In, Op In and Init Sel
   Selected - 1
   Gate Ctrl - Sel.

11. Set the following Control Out switches off:
   Adr
   Sel

12. Set the Control Out Cmnd switch on.

13. Depress the Start pushbutton.

14. Observe that the following indicators are on:
   Control In - Op and Stat
   Bus In - Parity (0-7 are off)
   Console Control Unit - Status In, Op In, and Init Sel
   Selected - 1
   Gate Ctrl - Sel

15. Set the Control Out Cmnd switch off.

16. Set the Control Out Serv switch on.

17. Depress the Start pushbutton.

e. Control NOP Test

1. Set the Mode Select switch to Single Byte.

2. Depress the Reset pushbutton.

3. Set the Address switches to 01_{16} with Parity Insert Correct, then set the Bus Out switches to 03_{16} with Parity Insert Correct.

4. Depress the Start pushbutton.

5. Observe that the following indicators are on:

Bus In - P, 4, 5
Console Control Unit - Status In, Op In, and Init Sel
Status Reg. - CE/DE

6. Depress the Start pushbutton.

7. Observe that the Test Control Initial Sel indicator is Off.

5.1.8.3 Reconfiguration Control Unit (RCU) Maintenance Panel

a. Test Switch

1. Set the Test/Operate switch to Test.

2. Observe that the Test indicator is on.

b. Lamp Test

1. Depress the Lamp Test pushbutton.

2. Observe that all indicators on the RCU Maintenance Panel are on.

c. Set CCR and Reset CCR pushbuttons

1. Set the switches as follows:

Address - $3F_{16}$ with Parity Insert Correct
Bus Out - 07_{16} with Parity Insert Correct

2. Depress the Set CCR pushbutton.

3. Observe that all Configuration Control Register indicators and the Multiple IOCE Check indicator are on.

4. Depress the Reset CCR pushbutton.

5. Observe that all Configuration Control Register indicators and the Multiple IOCE Check indicator are off.

d. Test I/O Operation

1. Set the switches as follows:

Address - 21_{16} with Parity Insert Correct
Bus Out - 00_{16} with Parity Insert Correct
Mode Select - Single Cmnd
CI Select - 01
Control Out - Adr and Sel

2. Depress the Start pushbutton.

3. Observe that the following indicators are on:

Bus In - P, 2 and 7
Reconfiguration Control Unit - Adr In, Op In and Init Sel
Address Register - 7

4. Set the following Control Out switches off.

Adr
Sel

5. Set the Control Out Cmnd switch on.

6. Depress the Start pushbutton.

7. Observe that the following indicators are on:

Bus In - 7
Reconfiguration Control Unit - Status In, Op In and Init Sel
Address Register - 7
Status Reg - UE

8. Set the Control Out Cmnd switch off.

9. Set the Control Out Serv switch On.

10. Depress the Start pushbutton.

11. Observe that the Address Reg-7 indicator is on.

12. Depress the Reset pushbutton.

13. Set the Control Out Serv switch Off.

e. Write Configuration and Read Configuration

1. Set the switches as follows:

Address - 30_{16} with Parity Insert Correct

Bus Out - AF_{16} with Parity Insert Correct

Mode Select - Single Byte

2. Depress the Start pushbutton twice.

3. Depress the Reset pushbutton.

4. Set the Bus Out switches to 31_{16} with Parity Insert Correct.

5. Depress the Start pushbutton twice.

6. Set the Bus Out switches to FF_{16} with Parity Insert Correct.

7. Depress the Start pushbutton.

8. Set the Bus Out switches to 00_{16} with Parity Insert Correct.

9. Depress the Start pushbutton.

10. Set the Bus Out switches to 55_{16} with Parity Insert Correct.

11. Depress the Start pushbutton.

12. Set the Configuration Interface (CI) Single/ Cntinus switch to Single.

13. Set the Bus Out switches to AA_{16} with Parity Insert Correct.

14. Depress the Start pushbutton.

15. Observe that the CI Common Shift Register contains $FF0055AA_{16}$.

16. Set the Mode Select switch to Single Cmnd.

17. Depress the CI Clock Cycle pushbutton.

18. Observe that for each subsequent depression of the CI Clock Cycle pushbutton, the contents of the CI Common Shift Register shifts left one position with bit 0 shifting into bit 31.

19. Repeat steps a-e for the second RCU.

5.1.8.4 System Maintenance Monitor Console (SMMC) Interface - The following test will demonstrate the SMMC Interface requirements from the Configuration Console.

1. Set address switch 7 On.

2. Set all Bus Out switches Off. (Parity Insert Correct)

3. Set Mode Select switch to Single Comnd.

4. Set the following Control Out switches on:

   Adr
   Sel

5. Depress the Reset and Start pushbuttons.

6. Set the Cmnd Control Out switch on and all others off.

7. Set Bus Out switches 4 and 7 On. (Parity Insert Correct)

8. Depress Start pushbutton.

9. Set the Serv Control Out switch on and all others off.

10. Depress the Start pushbutton.

11. Set the Mode Select switch to Cntinus Trsfr.

12. Set Single/Cntinus switch to Cntinus.

13. Install terminator P/N 5805585 at location 01S-A5A and remove the plug-in relay from location 01C-C1A6.

14. Install jumper from 01D-D1D2D13 to 01D-D1D2D08.

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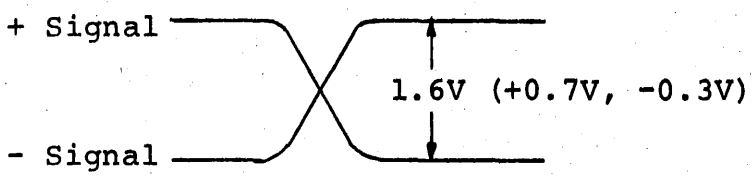
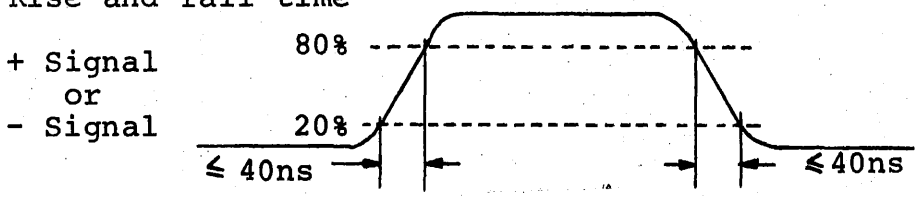
15. Scope the outputs of the data driver at locations 01D-D1L2D13 and 01D-D1L2B13. Observe the following:



Rise and fall time



16. Remove the jumper and terminator and replace the removed relay.

17. Set the Test/Operate switch to Operate.

5.1.9 Peripheral Adapter Module. This section will test the operation of the Test and Monitor functions from the Test Panel. The Test Panel provides a means to manually test the Peripheral Adapter Module.

The PAM which is being tested should be in state 0 with the Test switch on. The test indicator should be on. The PAM must be configured to its primary IOCE. (Refer to Spec. Section 4.2).

a. Lamp Test switch

1. Depress the Lamp Test pushbutton. Check to see that all of the logic indicators on the Test Panel (except spares) are on, and the State indicators on the Power Panel.

b. Select Cycle Select Out, Select Cycle Command Out, Select Out, Service Out, Address Out pushbuttons and Address switches.

1. Place the address of the Test and Monitor Adapter in the Address switches:

PAM 1	10 (Hex)
PAM 2	60 (Hex)
PAM 3	B0 (Hex)

Once address is set, do not change.

2. Place all data switches to the off (down) position.

3. Place the Parity Insert switch to the "Correct" position.

4. Place Repeat Select and Auto Transfer switches off.

5. Place Stop on Check, Suppress Out and Test Line switches to the off position.

6. Place a Test I/O Command (00) into the Command Switches.

7. Depress the following:

General Reset pushbutton
Address Out pushbutton
Select Cycle Select Out pushbutton

8. Check the Bus In indicators. Address In should be on with the Adapter address used in Step 1 displayed on Bus In.

9. Depress Select Cycle Command Out pushbutton. Status In should be On.

10. Bus In should contain the Status byte transmitted as a result of the Test I/O Command. It should contain all zeroes with correct parity.

11. Depress Select Cycle Service Out pushbutton. Status In will reset. Bus In will contain all zeroes.

c. Command and Parity Insert switches and the Execute Select pushbuttons.

1. Place the Sense Command (04) in the Command switches.

2. Depress Address Out and Select Cycle Select Out pushbutton.

3. Place the Insert Parity switch to the "Incorrect" position.

4. Depress Select Cycle Command Out pushbutton and return the Insert Parity switch to the "Correct" position. Status In, Parity Check and Command Out Indicators should be on.

5. Depress Select Cycle Service Out. The Request In indicator should be on.

6. Depress the Execute Transfer pushbutton.

7. Depress the Execute Select pushbutton. This should again execute the Sense Command and the Request In indicator should come on.

8. Depress the Transfer Cycle Select Out pushbutton. **Bus In** should contain Adapter Address and Request In indicator is reset. Address In comes on.

9. Depress Transfer Cycle Command Out pushbutton. Service In indicator should come on. Bus In will contain the first Sense byte and bit 2, (Parity Check) should be on.

10. Depress Transfer Cycle Service Out pushbutton. Service In indicator is reset. Request In indicator should come on. Bus In indicators should contain zeroes.

11. Repeat Steps 8, 9 and 10 twice. On the 1st repeat (step 9) Bus In will contain sense byte 2 which is all zeroes, and on 2nd repeat (step 9), Bus In will contain sense byte 3 which will have Bit 1 (Command Out) On.

12. All Sense bytes should be reset. Depress General Reset pushbutton.

d. General Reset and Select Reset

1. Place all Command switches off.

2. Depress Address Out and Select Cycle Select Out pushbuttons.

3. Place Parity Insert to the "Incorrect" position.

4. Depress Select Cycle Command Out pushbutton and place Parity Insert switch to "Correct" position. Command Out error, parity check and Bit 6 (Bus In) indicators should come on. Status In indicator should also be on.

5. Depress General Reset pushbutton. Checks should reset.

6. Repeat Steps 2 to 4. Depress Select Reset pushbutton. Checks should reset.

e. Suppress Out and Execute Transfer pushbutton.

1. Place a Sense Command (04) in the Command switches. Depress Execute Select pushbutton and Request indicator should come on.

2. Depress Execute Transfer pushbutton 3 times. Bus In should contain all zeroes.

3. Place the Suppress Out switch on (Up).

4. Depress Transfer Cycle Select Out and Command Out pushbuttons. Bus In should have Bits 4 and 5 (Channel End, Device End) On.

5. Depress Select Cycle Command Out and set Suppress Out switch Off (Down). Request In indicator should come On.

6. Set Suppress Out switch On. Request In indicator should go Out.

7. Depress General Reset pushbutton. Place Suppress Out switch Off.

f. Stop On Check switch.

1. Place the Stop Check switch on (Up).

2. Depress Address Out and Select Cycle Select Out pushbutton.

3. Place the Insert Parity switch to the "Incorrect" position.

4. Depress Select Cycle Command Out pushbutton, Status In indicator should be On.

5. Depress Select Cycle Service Out. Status In indicator should remain On. Request In indicator should not come On. Parity Check and Command Out indicators should be On in Sense Register.

6. Place the Stop on Check switch to the Off position (Down).

7. Place the Insert Parity switch to the "Correct" position.

8. Depress Select Cycle Service Out. Request In indicator should come On. Depress General Reset pushbutton.

g. Halt I/O pushbutton.

1. Depress Address Out and Select Cycle Select Out pushbuttons.

2. Depress Halt I/O pushbutton.

3. Depress Select Cycle Command Out pushbutton. Check to see that the operation has terminated by receiving no Status In response.

4. Depress General Reset pushbutton.

h. Command Out Stop pushbutton and Transfer Cycle Select Out, Transfer Cycle Command Out and Transfer Cycle Service Out pushbuttons.

1. Place a Sense Command (04) in the Command switches.

2. Depress Execute Select pushbutton. Request In indicator should come On.

3. Depress Transfer Cycle Select Out pushbutton. Address In indicator should be On.

4. Depress Transfer Cycle Command Out pushbutton. Service In indicator should be On.

5. Depress Transfer Cycle Service Out pushbutton. Request In indicator should be On.

6. Depress Command Out Stop pushbutton.

7. Depress Transfer Cycle Select Out pushbutton. Address In indicator should be On.

8. Depress Transfer Cycle Command Out pushbutton. Service In indicator should not come On. Request In indicator should come On. Depress General Reset pushbutton.

i. Set CCR pushbutton and Data switches.

1. Set Data/SCON-IOCE switches, postions 0, 1, 2, 3, 4, 5, 6, and 7 on (Up).

2. Depress Set CCR pushbutton. SCON and IOCE 1, 2, and 3 indicators should come On.

3. The State bits cannot be set from the Data/SCON IOCE switches.

j. Repeat the above test for each PAM.

Upon completion of the above tests and obtaining the correct indications, the test will be considered acceptable.

5.1.10 Storage Control Unit. The following section will be a manual demonstration of the Storage Control Unit test panel. The primary use of this panel will be for the maintenance and test of the SCU and its associated Disk Storage Units.

The SCU which is being tested should be in state 0 with the CE/Normal/In-line switch in the CE position. The test indicator will be On.

a. Lamp Test Pushbutton.

1. Depress the Lamp Test pushbutton.

2. Observe that all indicators on the Operator's panel are On, except thermal check and power check.

b. Data, Register Select, Enter, Display Register, and Display Switches.

1. Raise the Reset/Lamp Test switch.

2. Set the Data switches to the value of FF. (These are the two low order Start Address switches).

3. Set the Register Select switch to OP. (Black letters).

4. Raise the Enter Black switch.

5. Raise the Display Black switch. Verify that all of the Register Display and Parity lights are on.

6. Set the Data switches to the value of 00.

7. Raise the Enter Black switch.

8. Raise the Display Black switch. Verify that all of the Register Display lights are Off with exception of the Parity bit.

9. Set the Data switches to the value of 01.

10. Raise the Enter Black switch.

11. Raise the Display Black switch. Verify that the Display Register contains the value set in the Data switches with the Parity bit Off.

12. Set the Data switches to the value of FF.

13. Set the Register Select switch to DR (White letters).

14. Lower the Enter White switch.

15. Lower the Display White switch. Verify that all Register Display and Parity lights are On.

16. Set the Data switches to the value of 00.

17. Lower the Enter White switch.

18. Lower the Display White switch. Verify that all of the Register Display lights are Off with exception of the Parity bit.

19. Set the Data switches to the value of 01.

20. Lower the Enter White switch.

21. Lower the Display White switch. Verify that the Register Display contains the value set in the Data switches. The Parity bit will be Off.

c. Mode Select, Stop Address, Check Reset, and Start switches.

1. Raise the Reset/Lamp Test switch.

2. Set the Mode Select switch to the Recycle position.

3. Set the Start Address switches to 602.

4. Set the Stop Address switches to 6E1.

5. Set the Check Stop/Run/Single Step Stop switch to the Check Stop position.

6. Raise the Set Address switch.

7. Raise the Start switch. Machine Stop light will go out and remain out.

8. Verify that ROSAR is cycling and the Probe light is On.

9. Raise and release the Check Reset switch. The Probe light will go out for the duration of time which Check Reset is activated.

10. Set the Mode Select switch to Stop. Observe that the Machine Stop and Probe lights are On.

d. Start Address switches, set Address switch, and ROSAR.

1. Raise the Reset/Lamp Test switch.

2. Set the Address FFF in the Start Address switches.

3. Raise the Set Address switch. Verify that all ROSAR lights and Parity are On.

4. Set the Address 000 in the Start Address switches.

5. Raise the Set Address switch. Verify that all ROSAR lights are Off with exception of Parity.

6. Set an Address of 001 in the Start Address switches.

7. Raise the Set Address switch. Verify that ROSAR contains 001 with the Parity bit Off.

e. Single Step Operation

1. Set the Address 600 in the Start Address switches.

2. Set the Mode Select switch to the SCAN position.

3. Raise the Reset/Lamp Test switch.

4. Raise the Set Address switch and verify that ROSAR contains 600.

to the Single Step Stop position.

6. Raise the Start switch once and observe address 600 in ROSAR.

7. Raise the Start switch once and observe address 601 in ROSAR.

8. Raise the Start switch once and observe address 600 in ROSAR.

9. Raise the Start switch once and observe address 602 in ROSAR.

10. Raise the Start switch once and observe address 600 in ROSAR.

11. Raise the Start switch once and observe address 603 in ROSAR.

12. Set the Check Stop/Run/Single Step Stop switch to the Run position.

13. Raise the Start switch. Observe that ROSAR is cycling.

f. **Configuration Register switches, SET CCR Execute pushbutton, SET CCR Single Step/Auto Cycle switch, and** CE Select switch.

1. Set all Configuration Register switches to one.

2. Set the SET Single Step/Auto Cycle switch to Auto Cycle.

3. Set the CE Select switch to the ANY CE position.

4. Depress the SET CCR Execute pushbutton.

5. Observe that all bits are On in the Configuration Register except P3.

6. Set CE-1 Configuration Register switch to one, all others to zero.

7. Depress the SET CCR Execute pushbutton.

8. Observe that the CE-1 and P3 bit are On in the Configuration Register, all other bits are Off.

9. Set the CE Select switch to the CE-2 position.

10. Set all Configuration Register switches to the one position.

11. Depress the Set CCR Execute pushbutton.

12. Observe that only the CE-1 and P3 lights are On in the Configuration Register.

13. Set the CE Select switch to the CE-1 position.

14. Depress the Set CCR Execute pushbutton.

15. Observe that all bits are On in the Configuration Register except P3.

16. Raise the Reset/Lamp test switch.

17. Set the Set CCR Single Step/Auto Cycle switch to the Single Step position.

18. Set Configuration Register switches for CE-1, IOCE-1, IOCE-2, and IOCE-3 to one, all others to zero.

19. Depress the Set CCR Execute pushbutton. Observe that the SCON Cycle Select indicator is On.

20. Depress the Set CCR Execute pushbutton. SCON Cycle Select, load CCR, CE-1, IOCE-1, IOCE-2 and IOCE-3 indicators should be On with correct CCR parity.

21. Depress the Set CCR Execute pushbutton. The Load CCR light should go Off.

22. Depress the Set CCR Execute pushbutton. Observe that the SCON Cycle Select light goes Out and Channel A enable and Channel B enable lights are On.

23. Depress the Set CCR Execute pushbutton. Observe that the SCON Cycle Response light is On.

24. Depress the Set CCR Execute pushbutton four times. Observe that the SCON Cycle Response light is Out.

25. Set the Set CCR Single Step/Auto Cycle switch to the Auto Cycle position.

g. In-Line Mode Operation - The purpose of this test is to demonstrate the use of the resident diagnostic microprogram.

1. Prepare the Disk Storage Unit as follows:

   (a) Load a Scratch pack on one of the disk drives.

   (b) Insert the Spare ID can into the drive being tested.

   (c) Set the Start/Stop switch to the Start position.

   (d) Green Ready indicator will come On when drive is ready.

(e) Select Lock indicator (red) should be Off.

2. On the Storage Control Unit set the Check Stop/Run/Single Step Stop switch to the Run position and CE/Normal/In-Line switch to the In-Line position.

3. Place Mode Select switch to RTN.

4. Set 10 in Data switches.

5. Set Mode Select Switch to Load and back to RTN. Verify that Register Display is 10. In-Line routine 10 has now been loaded.

6. Set 80 in Data switches.

7. Set Mode Select switch to ERR. Verify that ROSAR is cycling.

8. Set Mode Select switch to RTN.

9. Set the CE/Normal/In-Line switch to Normal.

10. Repeat the above test for each SCU.

Upon completion of the above tests and obtaining the correct indications the test will be considered acceptable.

5.1.11 Tape Control Unit and Associated Tape Drives. The following section will be a manual demonstration of the Tape Control Unit test panel. The primary use of this panel will be for the maintenance and test of the TCU and its associated tape drives.

The TCU which is being tested should be in State 0 with the Off Line Mode plug plugged. The INTF DSBLD indicator will be On.

a. Machine Reset Pushbutton.

1. Depress the Machine Reset pushbutton. The following indicators should come On:

Op Out
1st Char.
Stop (may be on or off)
NFP
2400

2. Check for correct indications.

3. Set the Auto-Step switch to Auto.

b. Start Pushbutton.

1. Connect a 9 track drive to the TCU being tested. Plug the Address jacks to match the Physical Address setting of the TCU and tape drive. The overall parity should be Odd. Place a scratch tape on the tape drive and load (insure that tape is at Load Point). Set the Register Select rotary switch to the CRC position.

2. Plug Command jacks into Positions P of All Command Words, Interface B and CMD Word 1 Force On the test panel.

3. Depress Machine Reset and the Start pushbuttons. The tape drive being used should be selected and the following indicators should be on:

Op Out
CMND Out
Sel Out
Op In
Addr. In
1st Char.
TU Sta. A
Load Point
TI Off
NFP
Read Sta.

4. Check for correct indications.

c. CE Plugboard

1. Depress the Machine Reset and set the Raise-Lower switch to Raise.

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2. Remove Plug from Force Plug jack.

3. Make sure tape drive is in Ready and not File Protect status.

4. Plug jacks into test panel as follows:

Stop On - UC, MTE/LRC, SKEW, R/W, END/CRC and Hold Err.

Command 1 - Positions 3,4,5,6 and 7.
2 - Positions P,2,5,6 and 7.
3 - Position 6
4 - Positions 5, 6 and 7

WR Data 1 - Parity Position
2 - Parity Position
3 - Parity Position
4 - Parity Position

Rec Length - 128 (Insert proper address in all address positions).

5. Depress Machine Reset and Start pushbuttons. The tape drive should start a Write Tape Mark, Backspace Record, Read and Rewind operation.

NOTE: To check that a tape mark is being written, plug a jack into Command Counter 3, Stop Position. Tape operation will stop, tape mark indicator should be on.

d. Check Reset Pushbutton

1. Remove all jacks from the Command Counter and replug as follows:

Command 1 - Position 7
2 - Position 7
3 - Position 7
4 - Position 7

All other jacks remain the same.

2. Depress the Machine Reset and Start push-buttons. The tape drive should start a Write operation.

3. Drop Ready on the tape drive by depressing the Reset pushbutton on the tape drive. The tape drive should stop. The TCU should have the Rej. TU indicator On.

4. Depress the Check Reset pushbutton, the indicator should reset.

e. Configuration Control Register

1. Plug jacks into the test panel as follows:

Command 1 - Positions P, 6 and 7.
Data 1 - Positions 0,1,2,5,6, and 7.

2. Depress the Machine Reset and Start pushbuttons. Verify that the following indicators are on.

SCON 1
SCON 2
SCON 3
IOCE 1
IOCE 2
IOCE 3

3. Remove a jack from Data 1 position. Depress the Machine Reset and Start pushbuttons. Verify that the CCR Parity Check (SCON or IOCE) indicator is on.

4. Remove the jacks from Data 1 positions 0,1,2,5, 6 and 7.

5. Plug jacks into Data 1 positions P and 4.

6. Depress the Machine Reset and Start pushbuttons. Verify that the following indicators are Off.

SCON 1
SCON 2
SCON 3
IOCE 1
IOCE 2
IOCE 3
CCR PARITY Check (SCON and IOCE)

7. Remove all plugs.

8. Repeat the above test for each TCU.

Upon completion of the above tests and obtaining the correct indications the test will be considered acceptable.

5.1.12 2540 Read/Punch and 1403 Printer Off Line Test. The following tests will demonstrate the off line testing of the 2540 Read/Punch and 1403 Printer using the I/O Tester.

The I/O Tester may be connected to or disconnected from the 2821 without dropping power if:

1. I/O device being tested is not ready (Stop key depressed on device) or:

2. All switches on the I/O Tester are set to off.

Plug the cable connectors into the pair of receptacles provided for the I/O device being tested. (One pair for the Printer, another for the Read/Punch).

1. Install the Overlay for the I/O device to be tested.

2. Complete Step b for a 2540 and Step c for a 1403.

a. Lamp Test

1. Raise the Lamp Test Switch and observe that all but spare indicators are lit.

b. 2540 Check

1. After placing the cable connectors to the 2540, place about 100 blank cards into the Punch and depress Start, two cards should feed and the Ready light should come on.

2. Turn the Mode (rotary) switch to Storage Scan.

3. Set the Read-Punch (down).

4. Set the Data Entry switches to 5C (hex).

5. Raise and hold the Data Entry switch and raise the Start switch. This should load the Data Register to 5C. (Indicators 11, 8, and 4)

NOTE: A false Address Check is generated when the BAR advances past 89 and wraps around to 0.

6. Turn Mode (rotary) switch to Off Line Run.

7. Raise the Reset and raise the Start switch. Cards should now continue to be punched until the Tester Stop switch is turned on or the Punch hopper is empty.

8. Check a punched card to insure all 80 columns punched in rows 11, 8, and 4.

9. Remove the punched cards from the Punch Stacker, and place into the Card Reader.

10. Depress the Start pushbutton on the Card Reader. Three cards should feed and the Ready light should come on. Depress End of File.

11. Set Read/Punch switch to Read.

12. Raise the Reset and raise the Start switch. All cards punched will now be compared. When all cards have been read, Reader should stop and EOF light should be out.

13. Both Tests should run error free.

14. Before returning the 2540 on line, raise the Reset switch. This insures a Reset condition for return to On Line operation.

c. 1403 Check

1. After placing the cable connectors to the 1403, install the Forms and Carriage Tape in the 1403 and make printer ready, by raising the Start switch on the Tester.

2. Set the Mode (rotary) switch to Scan Load.

NOTE: Under no circumstances should this switch be set to the UCB Load position. This would necessitate reloading the UCB.

3. Enter F1 Hex into the Data Entry switches.

4. Set Check Stop switch on and raise the Reset switch.

5. Raise and hold the Data Entry switch and raise the Start switch. This should load the Data Register.

6. Set the Mode (rotary) switch to Print/Carr.

7. Raise the Reset switch momentarily and then raise the Start switch. This will start the Printer and printing should continue until the Stop switch is turned on at the Tester. A 1 (one) should be printed.

8. Before returning the Printer On Line, operate the Reset switch. This insures a reset conditions for return to On Line operation.

5.1.13 Printer Keyboard (1052). The following test will be a demonstration of the System Console 1052 (9020D) and 9020E 1052 Test Panels. The Test Panel controls are primarily for maintenance use as a trouble shooting aid. Insure that there is paper in the 1052.

a. Ready and Request pushbuttons.

(9020D) The Printer Keyboard switch must be in Off Line position. Then push the Enable pushbutton. The Enable indicator will come On.

(9020E) Set the 1052 I/O Interface Enable/Disable switch on the CE to the Disable position. The Disable indicator will be On.

1. Place the Contin Write/Read switch in the Read position.

2. If the CE Mode - On Line switch is in the On Line position, place it in CE Mode. If already in CE Mode, switch it to On Line and then back to CE Mode. This will reset the Control Unit. Check that the Read and Proceed lights are on.

3. Depress the Not Ready pushbutton. The Intervention Required Lamp on the 1052 should be on.

4. Depress the Ready pushbutton. The Intervention Required Lamp should go out.

5. Depress the Not Ready pushbutton. The Intervention Required Lamp should not come back on.

6. Reset the CU by throwing the CE Mode switch to On Line and back to CE Mode.

7. Again depress the Not Ready pushbutton. The Intervention Required Lamp should turn on.

8. Depress Request pushbutton. The Attention lamp should turn on.

9. Depress the Ready pushbutton. The Intervention Required Lamp should remain on.

b. Test CE Write switch.

1. Reset the Control Unit and place On-Line-CE Mode switch to CE Mode. Depress Ready pushbutton, Intervention Required light goes out.

2. Reset the CU by throwing the CE Mode switch to On Line and back to CE Mode. Place the Contin Write/Read switch to Contin Write.

3. The Write lamp should be on. The 1052 should be printing the characters which have been plugged on the logic board. The Printer Busy lamp should be blinking.

4. When the End of Line is reached, the carriage should automatically return and printing should continue after the return.

5. To stop, place Contin Write/Read switch to Read.

6. Depress the Return key.

c. Test - CE Read switch.

1. Reset the CU again with the CE Mode - On Line switch and return to CE Mode.

2. Depress and release the Shift key. The Read and Proceed lamps should be On. The Intervention Required lamp may be On or Off. Data Register indicators 3, 5, and 6 should be On. All other lamps should be Off.

3. Depress a character key. The character should print. Printer busy should be on during printing and go off again. Proceed lamp should go off and come on again. Prtr. Cycle lamp and Equipment lamp should remain off.

4. All characters and function codes can be checked this way. An upper case shift will also turn on the Upper Case lamp.

5. Lock the Keyboard in upper case and depress (ENTER). The carriage should return and Upper Case lamp should go off. Proceed lamp should go off and keyboard should lock. Verify that the keyboard is locked. (INHIB CR indicator will be on).

6. Reset the CU with the CE Mode switch.

7. Return keyboard to Lower case.

8. Depress the Cancel pushbutton. The carriage should return again and the keyboard should lock.

9. Reset the CU with the CE Mode switch.

10. Remove paper from the 1052. Intervention Required Lamp should come On.

11. Reinsert the paper, depress Ready, and place the CE Mode - On Line switch to On Line.

The following tests will demonstrate the PAM 1052 Test Panel. The CE Mode Card must be plugged into location Q2L7 in the PAM 1052 Adapter (if clearing of the alternate adapter is necessary, a controlled No-Op to the Alternate 1052 Adapter may be issued via the applicable PAM Maintenance Panel).

d. Ready and Request pushbuttons.

1. Place the Contin Write/Read switch in the Read position.

2. If the CE Mode-On Line switch is in the On Line position, place it in the CE Mode position. If already in the CE Mode, switch it to On Line and then back to CE Mode. This will reset the Control Unit. Check that the Read and Proceed lights are on.

3. Depress the Not Ready pushbutton. The Intervention Required lamp on the 1052 should be on.

4. Depress the Ready pushbutton. The Intervention Required Lamp should go out.

5. Depress the Not Ready pushbutton. The Intervention Required Lamp should not come back on.

6. Reset the CU by throwing the CE Mode switch to On Line and Back to CE Mode.

7. Again depress the Not Ready pushbutton. The Intervention Required Lamp should turn on.

e. Test CE Write switch

1. Reset the Control Unit and place the On Line CE Mode switch to CE Mode. Depress the Ready pushbutton, the Intervention Required light goes out.

2. Reset the Control Unit with the CE Mode switch.

3. Place the Contin Write/Read switch to Contin Write.

4. The Write lamp should be On. The 1052 should be printing the characters which have been plugged on the logic board. The Printer Busy lamp should be blinking.

5. When the End of Line is reached, the carriage should automatically return and printing should continue after the return.

6. To stop, place the Contin Write/Read switch to Read.

f. Test - CE Read switch.

1. Reset the CU again with the CE Mode - On Line switch and return to CE Mode.

2. If the Keyboard is locked in Upper Case, release it to Lower Case by depressing the Shift Key. All lamps should be off except Read and Proceed. The Intervention Required may be either on or off. (Data Reg indicator 3, 5 & 6 will be on.)

3. Depress a character key. The character should print. Printer busy should be on during the printing and go off and come on again. Prtr. Cycle lamp and Equipment lamp should remain off.

4. All characters and function codes can be checked this way. An upper case shift will also turn on the Upper Case lamp.

5. Lock the Keyboard in the upper case and depress (ENTER). The carriage should return and Upper Case lamp should go off and INHIB-CR will be on. The Proceed lamp should go off and the keyboard should lock. Verify that the keyboard is locked.

6. Reset the CU with the CE Mode switch.

7. Return the keyboard to Lower case.

8. Depress the Cancel pushbutton. The carriage should return again and the keyboard should lock.

9. Reset the CU with the CE Mode switch.

10. Remove the paper from the 1052. Intervention Required lamp should come on.

11. Reinsert the paper, depress Ready and the place the CE Mode On Line switch to On Line.

Upon completion of the above tests and obtaining the correct indications the test will be considered acceptable. Remove CE Mode Card from location Q2L7 in the PAM 1052 adapter.

5.1.14 Data Adapter Unit (2701) Off-Line Test. The following tests will demonstrate the off-line testing of the Data Adapter Unit (2701) using the I/O Tester.

Take 2701 Off-Line. Turn power off. Plug the cable connectors into the pair of receptacles on the 2701 and install the overlay for the 2701 on the I/O Tester. Turn power on.

NOTE: Always observe odd parity when using the Data Entry switches through this procedure.

a. Addressing:

1. Set DAU address (0100_2 or 0101_2) in Data Entry switches 0-3 and RKM address 0001_2 in Data Entry switches 4-7.

2. Raise OP Out switch.

3. Raise Address Out switch.

4. Raise Select Out/Hold Out switch.

5. Drop Address Out switch followed by Select Out/Hold Out switch.

6. The bit indicators should now reflect the contents of the Data Entry switches.

7. Drop Op Out switch.

8. Repeat steps 1 through 7 until RKM binary address 001_2-101_2 have been tested.

b. Command Reformatting

1. Repeat steps a.1 through a.6 .

2. Set a command (Refer to Fig. 5.1.13-1) into the Data Entry switches.

3. Raise then lower the Command Out Switch.

a. The Command Register should reflect the contents of the Data Entry switches.

4. Raise then lower the Service Out switch.

a. Buffer B and the Diagnostic Buffer should contain the Reformatted Command (refer to Fig. 5.1.13-1).

5. Repeat steps B.1 through B.4 until all commands referred to in Figure 5.1.13-1 have been tested.

Command Data Entry Switches									Reformatted Command Buffer B & Diagnostic Buffer								
P	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	P
1	0	1	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	0
0	1	1	0	0	0	0	1	0	1	1	0	1	1	0	0	0	1

Figure 5.1.13-1

5.2 Program Functional Tests

These tests will consist of test programs that check technical features, logic blocks, computer commands, and data transfer paths of individual elements and units.

5.2.1 Compute Element (7201-02). The Computing Element contains the facilities for addressing Main Storage for fetching or storing information, for arithmetic and logical processing of data, for sequencing instructions in the desired order and for initiating the I/O operations for communication between storage and external devices. The following test checks for proper operation of these facilities in each CE.

a. Configuration will be set for the defined minimum system (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor (See Spec. Section 4.4.)

c. Load and operate the following programs. (See Spec. Section 4.5 for loading procedures.)

Compute Element Programs

Basic (CE and Diagnose Logout) Tests

D1101
D1102
D1103
D1108

CPU Error Detection and Analysis Programs

D1111
D1112
D1113
D1114
D1115

RX Format Fixed Point Instruction Programs

D1151 D1155
D1152 D1156
D1153 D1157
D1154 D115A

RR Format Fixed Point Programs

D115C D1162
D115D D1163
D115E D1164
D115F D1165
D1160 D1166
D1161 D1167

RR, RX and RS Formats Branch Instruction Programs

D1169 D116C
D116A D116D
D116B

RX Format Half-Word Instruction Program

D116F

RS Format Single Shift Instruction Program

D1171

SI Format Instruction Programs

D1173 D1177
D1174 D1178
D1175 D1179
D1176

LM and STM Instruction Programs

D117B
D117C

RR and SI Format Status Switching Instruction Program

D117E

RR and RX Format Multiply and Divide Instruction Programs

D1180
D1181
D1182
D1183
D1184

RS Format Double Shift Instruction Program

D1186

SS Format Instruction Programs

D118A	D118E
D118B	D118F
D118C	D1190
D118D	D1191

IC/STC and ISK/SKK Instruction Program

D1192

RX and SS Format VFL Instruction Programs

D1196
D1197
D1198
D1199
D119A
D119B

Multiprocessing Instruction Programs

D119C
D119D

Floating Point Instruction Programs

D11A2	D11B0	D11C0
D11A6	D11B4	D11C2
D11A9	D11B8	D11C6
D11AC	D11BC	D11CA

Decimal Instruction Programs

D11CD	D11D4
D11CE	D11D5
D11CF	D11D6
D11D0	D11D7
D11D1	D11D8
D11D3	

RX Format Execute Instruction Programs

D11DA	D11DE
D11DB	D11DF
D11DC	D11E0
D11DD	D11E1

Program Interrupt Programs

D11E4
D11E5
D11E6
D11E7
D11E8

Invalid Operation Code Program

D11E9

Execute Program Interrupt Programs

D11EB
D11EC
D11ED
D11EE

Interval Time Program

D13A0 (NOTE: Disable Interval Timer Off-(up))

360 Mode Test

D13A5

9020 Compatibility Program

D13B0

Diagnose Instruction Program

D13BA

Display Instructions

D13C0
D13C1
D13C2 (set section sense switch 0)

Interrupt Test

D13C8

Random Instruction Program

D13CD

Direct Control Functional Program

D1DA3

Address Translation Functional Program

DD9AO

Note: Reference Program DD9A0 Documentation for proper system configuration to run this test.

d. Record results.

e. Repeat steps a through d for each CE.

5.2.2 I/O Control Element (7231) Selector Channels, Channel-To-Channel Adapter (CTC), Storage Control Units/Disk Storage Unit (2314/2312), and Tape Control Units/Tape Drives (2803/2401). The following tests will check for proper operation of the selector channels of each IOCE and proper operation of all Channel to Channel Adapters, Storage Control Units/Disk Storage Units, and Tape Control Units/Tape Drives.

5.2.2.1 I/O Control Element (7231) Selector Channels.

a. Configuration will be set for the defined minimum system (refer to Spec. Section 1.2).

b. Initialize the Multiprocessing Diagnostic Monitor. (Refer to Spec. Section 4.4).

c. Mount and ready work tape(s) (Write Enabled Ring inserted) on a Tape Drive on the Selector Channel to be tested.

d. Load and operate the following programs. (Refer to Spec. Section 4.5).

1. D3151 Selector Channel I/O Functional Program

2. D3152 Selector Channel I/O Functional Program

3. D3153 Selector Channel CCW Flag Program

4. D3154 Selector Channel Invalid Specification Program

5. D3155 Selector SPCI Functional Program

e. Record results.

f. Configure the second TCU, if available, associated with the same IOCE and repeat steps b thru e.

g. Configure a second IOCE, if available, and repeat steps b thru f.

h. Configure a third IOCE, if available, and repeat steps b thru f.

5.2.2.1.1 I/O Control Element (7231) Third Selector Channel

a. The test configuration will consist of the following:

1. 1 IOCE with RPQ F16377 (Third Selector Channel)

2. 1 TCU

3. 1 Tape Drive loaded with FLT #3 tape and ready.

b. Set Load Unit switches to the configured tape drive.

c. Set Interval Timer switch Off (down).

d. Set IOCE test switch On.

e. Set FLT Control switch on IOCE to Process.

f. Set FLT Mode switch on IOCE to Execute.

g. Set Check Control switch to Disable.

h. Set Address keys 9, 10, 22 and 23 and Data keys 0 and 6 On.

i. Depress Reset pushbutton.

j. Depress Load pushbutton.

k. Record Results.

5.2.2.2 Storage Control Units/Disk Storage Units (2314/2312).

a. Configuration will be set for the defined minimum system (Refer to Spec. Section 1.2)

b. Initialize the Muliprocessing Diagnostic Monitor (Refer to Spec. Section 4.4).

c. Mount and Ready disk packs on Disk Drive(s) to be tested, using disk packs which have been formatted by Initializer Program D8050.

d. Load and operate the following programs: (Refer to Spec. Section 4.5)

1. D8051-D8064 Storage Control Unit Functional Program

2. D8065-D8069 Disk File Diagnostic Program

e. Record results.

f. Configure the second SCU, if available, associated with the same IOCE (step a) and repeat steps b thru e.

g. Configure a second IOCE, if available, and the remaining SCU, and repeat steps b thru e. After this step all SCU's and DSU's will have been tested.

5.2.2.3 SCU Two Channel Switch Test. (Not applicable for Simplex System). Note: Refer to the Program Writeup for D80A0.

a. Configuration will be set for the defined minimum system plus the second IOCE associated with the configured SCU.

b. Initialize the Multiprocessing Diagnostic Monitor.

c. Load and operate the following program.

D80A0 SCU Dual Interface Program

d. Record results.

e. Configure the second SCU to its associated IOCE's (step a) and repeat steps b, c, and d.

f. Configure the remaining SCU, if available, to its associated IOCE's (step a) and repeat steps b, c, and d.

5.2.2.4 Tape Control Units/Tape Drives (2803/2401).

a. Configuration will be set for the defined minimum system (Refer to Spec. Section 1.2).

b. Initialize the Multiprocessing Diagnostic Monitor. (Refer to Spec. Section 4.4).

c. Mount and ready work tape(s). (Write Enabled Ring Inserted) on Tape Drive(s) to be tested.

d. Load and operate the following programs. (Refer to Spec. Section 4.5).

1. D4050-4057 Tape Drive Functional Program

2. D4060 Tape Inter Record Gap Program

e. Record results, rewind tape drives, relocate system library tape to a tested tape drive and repeat steps b, c, and d on the tape drive that had been used for the system library tape.

f. Configure the second TCU, if available, associated with the same IOCE (step a) and repeat steps b through e.

g. Configure a second IOCE, if available, and the remaining TCU and repeat steps b through e. After this step, all TCU's and tape drives will have been tested.

5.2.2.5 TCU Dual Interface Test. (Not applicable for Simplex System.)

NOTE: Refer to the Program Writeup for D46A0.

a. Configuration will be set for the defined minimum system plus the second IOCE associated with the configured TCU.

b. Initialize the Multiprocessing Diagnostic Monitor.

c. Load and operate the following program.

D46A0 TCU Dual Interface Program.

d. Record results.

e. Configure the second TCU to its associated IOCE's (step a) and repeat steps b, c and d.

f. Configure the remaining TCU, if available, to its associated IOCE's (step a) and repeat steps b, c and d.

5.2.2.6 Channel-to-Channel - This test will check the Channel-to-Channel Adapters according to its functional specifications, between two selector channels.

a. Configuration will be set for the defined minimum system. Insure that the CTC Interface is enabled.

b. Initialize the Multiprocessing Diagnostic Monitor.

c. Load and operate program DA05l.

NOTE: Only one CTC at a time can be in the system. SS0.14 must be set.

d. Record results.

e. Repeat steps a through d for each Channel-to-Channel Adapter.

f. Repeat steps a through e for each IOCE.

5.2.3 I/O Control Element (7231) Multiplexor Channel. The following test will check for proper operation of the Multiplexor Channel of each IOCE.

NOTE: Refer to the program writeups.

a. Configuration will be set for the defined minimum system plus the 2540 and 1403. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec Section 4.4.)

c. Load and operate the following programs. (See Spec. Section 4.5.)

D3051 Multiplexor Channel I/O Functional Program

D3052 Multiplexor Channel I/O Functional Program

D3053 Multiplexor Channel CCW Flag Program

D3054 Multiplexor Channel Invalid Specification Program

D3055 Multiplexor Channel SPCI Functional Program

d. Record results.

e. Repeat steps a through d for each IOCE.

5.2.4 Storage Element (7251-09). The following test will check each SE's ability to access each of its addresses, to store and retrieve data, to protect areas of storage, and recognize storage error checks.

a. Configuration will be set for the defined minimum system (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following programs. (See Spec. Section 4.5.)

D22A0 Storage Element Program
D22A4 Storage Error Check Program
D22AA Storage Protect Array Program

d. Record results.

e. Repeat steps a through d for each SE.

5.2.5 Display Element (7289-04). The following test will check each DE's ability to access each of its addresses, to store and retrieve data, to protect areas of storage, to recognize storage error checks, and determine proper operation of the DE/DG interface via the WRAP feature.

a. Configuration will be set for the defined minimum system. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following programs (See Spec. Section 4.5.)

D22A0 Storage Element Program
D22A4 Storage Error Check Program
D22AA Storage Protect Array Program
D24A0 DE/DG Interface Test Program

d. Record results.

e. Repeat steps a through d for each DE.

5.2.6 System Console (7265-02). The following test will check the functional operation of the System Console's mode of communication. Basically, the communication may be divided into operations and controls requiring operator intervention, program generated control and status alarms and displays to enable the operator to monitor the 9020D system.

a. The system configuration will consist of all available elements and units. These elements will not be functionally checked at this time, but will be used to provide status and configuration indications. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program. (See Spec. Section 4.5.)

D6CA4 - System Console Program

d. Record results.

e. Repeat steps b, c, and d for each CE.

5.2.7 Configuration Console (7265-03). The following test will check the functional operation of the Configuration Console's mode of communication. Basically, the communication may be divided into operations and controls requiring operator intervention, program generated control and status, alarms and displays to enable the operator to monitor the 9020E System.

5.2.7.1 System Console Control Unit

a. The system configuration will consist of all available elements and units. These elements will not be functionally checked at this time, but will be used to provide status, logic check and configuration indications. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program (See Spec. Section 4.5.)

D6CA6 Configuration Console Program

d. Record results.

e. Repeat steps b, c and d for each CE.

5.2.7.2 Reconfiguration Control Unit

NOTE: Refer to the Program Writeup for D9051.

a. Configuration will be set for the defined minimum system (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program (See Spec. Section 4.5.)

D9051 - Reconfiguration Control Unit Test

d. Record results.

e. Repeat steps b, c and d for each RCU.

f. Repeat steps b, c, d and e for each CE.

5.2.8 Peripheral Adapter Module (7289-02). The following test will check for proper operation of the Test and Monitor adapter and all other adapters utilizing the Test and Monitor adapter.

a. Configuration will be set for the defined minimum system. (See Spec. Section 1.2.) The PAM being tested will be the primary PAM of the configured IOCE.

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the program DCC51. (See Spec. Section 4.5.)

d. Record results.

e. Repeat steps a through d for each PAM.

5.2.8.1 PAM Dual Interface Test #1. (Not applicable for Simplex System).

a. Configuration will be set for the defined minimum system plus the secondary PAM associated with the configured IOCE. (See Spec. Section 1.2)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program. (See Spec. Section 4.5.)

DCCA0 PAM Dual Interface Program

d. Record results.

e. Configure the second IOCE to its associated PAM's (step a) and repeat steps b, c and d.

f. Configure the remaining IOCE to its associated PAM's (step a) and repeat steps b, c and d.

5.2.8.2 PAM Dual Interface Test #2 (Not applicable for Simplex System.)

a. Configuration will be set for the defined minimum system plus the second IOCE associated with the configured PAM. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program. (See Spec. Section 4.5.)

DCCA0 PAM Dual Interface Program

d. Record results.

e. Configure the second PAM to its associated IOCE's (step a) and repeat steps b, c and d.

f. Configure the remaining PAM to its associated IOCE's (step a) and repeat steps b, c and d.

5.2.9 Control Unit (2821) Read/Punch (2540) and Printer (1403). The following test will check for proper operation of the Control Unit, Read/Punch and the Printer.

a. Configuration will be set for the defined minimum system with the Read/Punch and Printer enabled to the configured IOCE (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following programs (See Spec. Section 4.5.)

D6A51	2821 Channel Register Test Section 1
D6A52	2821 Control Program for Reader, plus Punch Section 2
D6A53	2821 Buffer Addressing Test Section 3
D6A54	2821 Print Buffer Check
D6A55	2821 UCS Buffer Check
D6A56	2821 Print Buffer Data Register FLT
D6A57	2821 UCB Data Register FLT
D6A58	2821 UCB Restore Routine
D6251	2540 Read/Punch Function Program (Punch Section)
D6261	2540 Read/Punch Function Program (Read Section)
D6262	2540 Read/Punch Function Program (Read Section)
D6351	1403 Printer Functional Program
D6352	1403 Printer Functional Program (Note: When testing 2821 with TCS feature use Sense Switch 28)
D6353	1403 Printer Functional Program
D6354	1403 Ripple Print Test
D6355	1403 Buffer Restore Test
D6356	1403 Carriage Program

d. Record results.

e. Restore 2821 UCB by operating Program D6A58.

f. Repeat steps a through e if additional I/O equipment is to be tested.

5.2.9.1 Additional Tests for the 2821 with a Two Channel Switch (TCS). The following tests will check for the proper operation of the Two Channel Switch and that power sequencing does not interfere with channel operation.

a. Configuration will be set for the defined minimum system plus the additional IOCE connected to the 2821 with TCS. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate Program D6AA0. (See Spec. Section 4.5.)

d. Record results.

e. Configure the system console switchable 2821 with its associated 1403 printer to one of the IOCE's, whose interface is connected to the 2821 with TCS.

f. Throw the interface switch corresponding to the interface to which the switchable 2821 is configured, to the OFF position.

g. Initialize the Multiprocessing Diagnostic Monitor.

h. Load and operate Program D6354 on the switchable 2821.

i. With Program D6354 running, IBM personnel will remove power from the 2821 with TCS.

j. Assure that no data checks have occurred on the printout.

k. Power will then be restored on the 2821 with TCS, again assure that no data checks have occurred on the printout.

l. Record results.

5.2.10 Printer Keyboard (1052). The following test checks the functional operation of the 1052 Printer Keyboards and their associated adapters.

a. Configuration will be set for the defined minimum system. (See Spec. Section 1.2.)

b. Initialize the Subsystem Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following programs on the Printer Keyboard. (See Spec. Section 4.5.)

D6651	Console, Basic Operations and Write Tests
D6652	Console, Typewriter Mechanical
D6653	Console, Read Test

d. Record results.

e. Repeat steps b, c, and d on the other 1052 Printer Keyboards.

f. (9020D) At the SC patch panel, cable the System Console Printer Keyboard to the PAM interface. This is accomplished by interchanging the three cables that are presently routed to the System Console 1052 with the three cables that are presently routed to the PAM 1052.

g. (9020D) Repeat steps b, c and d for the new System Console 1052.

h. (9020E) At the CC patch panel, cable the CE-2 1052 to the CE-3 interface, if available, and repeat steps b, c and d.

i. (9020E) At the CC patch panel, cable the CE-2 1052 to the CE-4 interface, if available, and repeat steps b, c, and d.

5.2.11 Data Adapter Unit (2701). This test will check the functional operation of the DAU Parallel Data Adapter Unit with the multi-device attachment.

a. Configuration will be set for the defined minimum system. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following programs. (See Spec. Section 4.5.)

DB051 - 2701 Functional Program (part 1)
DB052 - 2701 Functional Program (part 2)

d. Record results.

e. Repeat steps a through d for each Data Adapter unit.

5.2.11.1 Data Adapter Unit Two Processor Switch Test

NOTE: Refer to the Program Writeup for DB0A1.

a. Configuration will be set for the defined minimum system plus the second IOCE associated with the configured DAU. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor. (See Spec. Section 4.4.)

c. Load and operate the following program. (See Spec. Section 4.5.)

DB0A1 - 2701 Functional Program
(Two Processor Switch)

d. Record results.

e. Repeat steps a through d for each Data Adapter Unit.

5.2.12 IOCE Diagnostic Mode Functional Demonstration. The following demonstration will show the IOCE's ability to operate limited diagnostic programs.

a. The configuration will consist of an IOCE, TCU, the Read/Punch and Printer (if desired), and the System Console 1052.

b. Initialize the Subsystem Diagnostic Monitor (SDM). (See Spec. Section 4.4.)

c. Load and operate the following programs. (See Spec. Section 4.5.)

D1003-D1009, D100C	RX Format Fixed-Point Programs
D1010-D101B	RR Format Fixed Point Programs
D101F-D1023	RR/RX Format Branch Programs
D1027	Halfword Instruction Program
D102A	Single Shift Instruction Program

D102D-D1032	SI Format Instruction Programs
D1037-D1038	Load and Store Multiple Instruction Programs
D103C	Status-Switching Instruction Program
D103F-D1043	Multiply & Divide Instruction Programs
D1045	Insert and Store Character Instruction Program
D1047	Double Shift Instruction Program
D104A-D1053	SS Format Instruction Programs
D105A	Convert Instructions Program
D105C-D105E	Translate and Pack Instruction Programs
D105F	Non-Decimal VFL Instruction Program
D1060	SS Format Instruction Program
D1063-D1069	Execute Instruction Programs
D106B-D106E	Program Interrupts Programs
D1071-D1072	Execute-Program. Interrupt Program
D1075	Instruction Scrambled
D1076-D1077	Basic Diagnose Kernels
D1401	IOCE Timer Program
D1403	IOCE Delay Instruction Program
D2101	IOCE Local Store Test Program
D2740	MACH Storage Test Program

d. Record results.

e. Repeat steps a through d for each IOCE.

5.2.13 I/O Control Element Processor Operation.

5.2.13.1 I/O Control Element (7231-02) Processor Operation Test. The following test will demonstrate the ability to operate functional programs under CE control in IOCE processor mode.

a. Configuration will be set for the defined minimum system (refer to Spec. Section 4.).

b. Initialize the multiprocessing diagnostic monitor (refer to Spec. Section 4.).

c. Use the MDM sense message S0.8000/ to put MDM into the multiprogramming mode.

d. Load and operate the following program:

DDDA1

e. Following successful completion of Sections B, C and E of the IOCE Processor Control Program, enter the following message to run Section D.

LDDA1/Q.D,L/B/

f. Record results.

g. Repeat steps a through f for each IOCE.

5.2.14 CE, SE, DE and IOCE Log-Out Demonstration. The following demonstration will show the practical application of the Log-Out capability of a CE, SE, DE and IOCE, The other CE's and IOCE's will have their log-out circuitry checked during the FLT demonstration and the other SE's and DE's are checked during the CE functional tests. The Diagnose, Storage Element, and Display Element programs test the log-out circuitry of the SE's and DE's.

1. CE and IOCE Pushbutton Log-Out

a. Configuration will be set for the defined minimum system. (See Spec. Section 1.2.)

b. Initialize the Multiprocessing Diagnostic Monitor (See Spec. Section 4.4.)

c. Load Program D22A0, defining the Hi ODD BSM in the "d" message, and using the "o" message to halt the program after loading.

d. At the Compute Element, set the Storage Address Compare switch to the Stop position and set the Address keys to X+Y-1000 (where X = the address of the TAG "RTN2X" in the program listing and Y = the address contained in location 244 of the PSA).

e. Enter message B/ to begin.

f. After the program stops at the selected address, depress the Start pushbutton until the contents of the D Register equals the contents of the Address keys.

g. Observe and record the contents of the following CE registers.

IC, CCR, S, and T

h. Depress the Log-Out pushbutton on the CE. Depress the Start pushbutton and place the Storage Address Compare switch to the process position to continue and observe the hard copy printout. Compare the hard copy with the data recorded in step g.

i. Repeat steps c thru f.

j. After the program stops at the selected address, observe and record the contents of the following IOCE registers.

SAR, CCR, R, L, SDR, & IAR

k. Depress the Log-out pushbutton on the IOCE. Depress the Start pushbutton on the CE and place the Storage Address Compare switch to the Process position to continue and observe the hard copy printout. Compare the hard copy with the data recorded in step j.

2. Machine Check Log-Out (CE)

a. Repeat steps a through f of #1 above.

b. Momentarily ground 02A-D3M6B04 to cause a Local Store Bus Check. Check Register 2 bit 17 will turn on.

c. Depress the Start pushbutton on the CE and place the Storage Address Compare switch to the Process position.

d. Observe the hard copy printout and record the results.

3. Machine Check Log-Out (IOCE)

a. Repeat steps a through f of #1 above.

b. Momentarily ground 01A-C2F7D11 to cause a Full-Sum Check (24-31). Bit 24 will pick.

c. Depress the Start pushbutton on the CE and place the Storage Address Compare switch to the Process position.

d. Observe the hard copy printout and record results.

4. Machine Check Log-out (SE/DE-Summary)

Note: A second SE must be configured when an SE summary is desired.

a. Repeat steps a and b of #1 above.

b. Load Program D22A0, defining the low ODD BSM for an SE test, or ODD BSM for a DE test, and using the 0 message to halt the Program after loading.

c. Repeat steps d thru f of 1.

d. Store bad parity in the SE or DE to be tested. At the time the program stops, an all ones pattern has been loaded into storage. To induce the error, alter this pattern in one segment of storage as follows:

Storage Element - At the SE maintenance panel, set the Storage Address Register switches 5, 6, and 7 to the Zero position, switch 20 to the One Position, and switches 8-19 to the Ripple position.

Display Element - At the DE maintenance panel, set the Storage Address Register switches 1 and 2 to the Zero position and all others to the Ripple position. Set the Priority Select switch for CE-1 to Odd, and set all others Off.

Set all Data keys to the Ones position except the bit selected to fail. Select the byte by means of the Mark switches. Ripple this pattern from the maintenance panel.

e. Depress the Start pushbutton on the CE.

f. Observe the summary printout which will indicate the failing bit and the failing addresses. Record results.

g. Depress the Stop pushbutton on the CE.

h. Restore good parity to the segment just tested by setting all Data keys to the One position and again rippling the pattern from the maintenance panel.

i. Repeat steps a through h for the other configured SE or DE.

NOTE: In all of the above tests, insure proper configuration and test switch setting before restarting the program.

5.2.15 FLT Functional Tests. This test will check the ability of each IOCE and CE to functionally execute its Fault Locating Tests.

5.2.15.1 IOCE FLT Tests

a. Configure a TCU and TD to the IOCE.

b. Insure that the IOCE is in State Zero, the Test switch is On, and it is in Diagnostic Mode.

NOTE: If bits 21-24 of the IOCE's CCR are off, then the IOCE is in Diagnostic Mode.

c. Load and operate the following FLT Tests (FLT #2 tape):

NOTE: Ref. IOCE Maintenance Manual and LADS page FLT02 for the procedure.

Main/MACH Storage Hard Core
ROS Hard Core
Zero Cycle
One Cycle

d. Record results.

e. Repeat steps a through d for each IOCE.

5.2.15.2 CE FLT Tests

a. Configure for the following:

1 CE
1 IOCE
1 SE
1 TCU
1 Tape Drive

b. Insure that the CE is in State Zero with the Test switch On.

c. Load and operate the FLT Tests.

NOTE: Reference the CE LADS pages for the procedure.

d. Record results.

e. Repeat steps a through d for each CE.

6.0 SYSTEM FUNCTIONAL TESTS (REF. ER 063-4.2.2.2)

System functional tests demonstrate the ability of the 9020D/E System elements and units to operate in an integrated multiprogramming, multiprocessing environment. The System functional tests contain four reconfiguration tests to demonstrate the capabilities and uses of reconfiguration, and the SEVA program, which is cycled to test the integrated operation of the 9020D or E System. Special system tests are run to verify that the 9020D/E Central Processor can adequately handle specific data processing tasks at specified rates, and demonstrate the practical tests of the FLT's and the compatibility of the System/360-9020 System.

6.1 Reconfiguration (Ref. ER 063-4.2.2.4.2)

The reconfiguration tests consist of the following:

Test A	CCR Operation and Signal Gating
Test B	DAR/DMR External Interrupt Checks
Test C	Input Message Reconfiguration Control
Test D	Failure Detection Reconfiguration Control

NOTE: Set Check Control Switch to Process on all CE's and IOCE's to be tested. The ability to reconfigure a DAU is tested in Test C.

6.1.1 Reconfiguration - Test A. Reconfiguration Test A tests the ability of the CCR circuitry to reconfigure elements and units under program control, and assures that communication can only be made between configured interfaces.

NOTE: Refer to the Program Writeup for DD8A0.

a. Set test configuration to all elements and units available in State Zero - Test switch off.

b. Initialize MDM and define the system.

c. Load and operate Configuration Control Program DD8A0.

d. When matrix printout occurs, examine the matrix for success and/or failure indications.

e. Record test results.

6.1.2 Reconfiguration - Test B. Reconfiguration Test B tests the Diagnose Accessible Register (DAR) for proper bit setting of hardware-generated external interrupts, and the DAR Mask Register (DMR) for proper masking of the interrupts.

NOTE: Refer to the Program Writeup for DD6A2.

a. Set test configuration to all elements and units available in State Zero - Test switch off.

b. Initialize MDM and define the system.

c. Load and operate DAR/DMR Functional Program DD6A2.

d. Automatic section completion indicated by:

Printout: AUTO PASS COMPLETE - START MANUAL SECTION

e. Depress Test OBS or Test OTC pushbutton on any element, or Test OTC on any unit.

f. Observe printout of tested element or unit and Test pushbutton depressed.

g. Repeat Steps e and f for all elements and units.

h. End program with input Message FD6A2.

i. Record test results.

j. Repeat Steps a through i for each CE.

6.1.3 Reconfiguration - Test C. Reconfiguration Test C tests the ability of the system to reconfigure upon a manual input message from the 1052 Printer Keyboard.

NOTE: Units or elements which are added back into the redundant system with a QE0C7 ID* message must be used in the active system on the next reconfiguration.

a. Set test configuration and include all elements and units in State Zero - Test Switch off.

NOTE: Disable Interval Timer On (down).

b. Initialize MDM and define all elements and units. (Refer to Spec. Section 4)

c. Load SEVA Control Program DE0A3, operate in acceptance test mode, and define the active minimum system. (Refer to Spec. Section 4)

d. Wait for printout "SEVA IS TESTING AND READY FOR SIMULATED FAILURES," and then enter input message QE0C7. $ID_1.ID_2$ to request a reconfiguration of the active system.

1. ID_1 - element or unit in active system that is to be placed in the redundant system.

2. ID_2 - element or unit in the redundant system that is to replace the element or unit indicated by ID_1.

NOTE: If ID_2 is a PAM, SCU, or TCU, the exchange must be capable of being made with the currently active IOCE.

e. Observe the configuration change in the CCR indicators of ID_1 and ID_2 and the printout of the element that was removed from the active system.

f. Observe the printout of the reconfiguration time, in seconds, from the receipt of the input message to full system operation with the new configuration. The time should not exceed 30 seconds.

g. Record results.

h. Repeat steps d through g for each element and unit; however, the FAA observer may stop the test sooner at his discretion.

6.1.4 Reconfiguration - Test D. Reconfiguration Test D tests under program control, the ability of the system to reconfigure, upon detection of a failing element or unit.

a. Set test configuration and include all elements and units in State Zero - Test switch off.

NOTE: Turn Disable Interval Timer On (down).

b. Initialize MDM and define all elements and units. (Refer to Spec. Section 4)

c. Load SEVA Control Program DE0A3, operate in the acceptance test mode, and define the active system. (Refer to Spec. Section 4)

d. Wait for printout "SEVA IS TESTING AND READY FOR SIMULATED FAILURES," and then depress the OTC Test pushbutton on an element or unit selected by the FAA observer.

e. Observe the reconfiguration of the selected element or unit in its CCR and the printout of the element that was placed in the failed category.

NOTE: If TCU in active system has only one active drive attached, that TCU will not be placed in the failed category.

f. Record results.

g. Repeat Steps d through f for an element and unit of each type.

6.2 Integrated System Tests

6.2.1 System Evaluation (SEVA) (Ref. ER 063-4.2.2.2). The purpose of the SEVA Program is to exercise and test elements, units and computer-oriented peripheral equipment in the maximum system configuration under control of MDM.

MDM will function as a cyclic program to control and operate SEVA test programs in a multiprogramming multiprocessing mode with periodic printouts, providing program results, error data and other pertinent information.

The maximum system configuration will be exercised for a total period of twelve (12) hours. The program may be stopped so that the tape drives and I/O equipment may be substituted into the active system. This test will be conducted only at the field installation.

a. Set the test configuration to all elements and units available in State Zero - Test switch off.

b. Enable the Interval Timer on all CE's.

c. Initialize MDM and define the system.

d. Load and operate the SEVA Program DE0A3. (Refer to Spec. Section 4)

e. Cycle the active system and observe periodic program result printouts.

f. As stated in Section 3.0, stop the SEVA program and reconfigure the tape and I/O equipment.

g. Repeat Steps c, d, and e.

The SEVA test will be considered acceptable when the maximum system configuration has successfully cycled the SEVA program for twelve (12) hours of which five (5) consecutive hours have been malfunction free. Refer to Section 3.0 for additional criteria.

6.3 Special System Tests

6.3.1 Eight Timed Sample Problems. The Eight Timed Sample Problems will be run to verify that the 9020D/E Central Processor can adequately handle specific data processing tasks at the required rates. This test, to demonstrate cable length timing differences, will be executed with three different CE to SE combinations.

a. The following procedure provides instructions for running the Eight Timed FAA Sample Problems. The following configuration will be required: (All unused elements should be in test.)

1 CE (No. 1)
1 IOCE
1 SE (No. 1)
1 1052
1 TCU
1 Tape Drive

1. "Enable" the Interval Timer on the CE.

2. Follow existing procedure to load MDM from the System Maintenance tape and define test subsystem.

3. Type LF0B0/B/ on 1052.

4. No further intervention should be required for running the Eight Sample Problems. The time required to execute each problem and the composite will be printed out on the MDM output device.

5. (9020D only) Repeat steps 1 through 4 for CE-1 and SE-6; CE-3 and SE-8.

The actual run times of the eight sample problems will be used to compute the true composite non-parallel CTAF. The result will be compared against the standard composite of:

.0740 (CE-1 to SE-1)
.0848 (CE-1 to SE-6)
.0931 (CE-3 to SE-8)

6.3.2 Display Instruction Performance Test (9020E System). The performance test for Convert and Sort Symbols, Convert Weather Lines, Repack Symbols, and Load Chain instructions will be run to verify that these instructions will perform at the required rates.

(a) The following configuration will be required for this test (all unused elements should be in test):

1 CE (No. 1)
1 SE (No. 1)
1 DE (No. 1)
1 IOCE
1 TCU
1 Tape Drive
1 MDM Output Device (1403 Printer or 1052 Typewriter)

(b) The following procedure must be followed for running the Display Instruction Performance Test.

1. "Enable" the Interval Timer on the CE Control Panel.

2. "Disable" the Frequency Alteration Switch on the CE Control Panel.

3. Follow existing procedure to load MDM from the System Maintenance tape and define test subsystem.

4. Type LFØCØ/B/ on 1052.

5. No further intervention should be required for running the Display Instruction Performance Test. The required times are printed out on the MDM output device.

   The output results obtained should be equal to or less than the indicated times listed below.

Convert and Sort Symbols	Time (usec)
Primary radar, S/S	
Instruction Overhead	5.3
Header Processing (per header)	2.3
Geographic Search (per symbol)	2.3
Search and Process (per symbol)	8.9
Beacon	
Instruction Overhead	4.6
Search (per symbol; fail altitude and type filters)	
. SB bit off	2.7
. SB bit on, IX bit off	3.6
. SB bit on, IX bit on, fail geographic filter	5.6
Process (per symbol; fail altitude and type filters, SB bit on, IX bit on, pass remaining filters, process)	12.2

SAS264

	Time (usec)
Convert Weather Lines	
Instruction Overhead	2.8
Header Processing (per header)	2.3
Search (per weather line)	
. Point 1 in sterile area 3	4.3
. Point 2 in sterile area 3, Point 1 passes all filters	6.9
. Points 1 and 2 fail geographic filter	5.1
Process (per weather line)	
. Point 1 ON, Point 2 ON	15.2
. Point 1 ON, Point 2 OFF (1 forward truncation)	16.0
. Point 1 OFF, Point 2 ON (1 forward truncation)	16.4
Truncation (per attempt)	1.4
Repack Symbols	
Instruction Overhead	24.0
Delete Descriptors	
. No match (per WCT entry)	1.6
. Match (per descriptor)	2.5
Move Descriptors	
. History/Current Descriptor	1.9
. Modified Current Radar Descriptor	
- No match (per WCT entry)	1.2
- Match (per descriptor)	3.0
Move Symbols (History, Modified Current, or Current; per symbol)	1.1
Insert	
. New Descriptor	5.8
. New Symbol	1.0
Paging Time (CSS, CVWL, or RPSB)	1.3
Load Chain	
2nd operand on doubleword boundary	2.3
2nd operand on word boundary	2.1

6.3.3 FLT Practical Test. The FLT Practical Test will demonstrate the ability of the one-cycle FLT's to detect and isolate automatically a CE or IOCE failure induced by a known error condition in a preselected location. MAIN/MACH and ROS controlled hard core tests, and zero-cycle tests are run prior to the one-cycle FLT's to detect failures in logic not under test.

The isolation and detection of the error condition is determined by the appearance of the error condition location in an indicated FLT SCOPEX LIST test stop.

a. Operating Procedures: (IOCE)

1. Set the corresponding test configuration as follows:

IOCE Test Configuration

1 IOCE (test element)
1 TCU
1 Tape Drive (FLT No. 2 Tape)

2. Set Load Unit switches to the selected configuration.

3. Set Interval Timer off (down), test element Test Switch on, and other configured equipment test switches off.

4. Load FLT tape on the selected drive and Ready.

5. Set FLT control switch on Test element to Process.

6. Set FLT Mode switch on Test element to Execute.

7. Set Check Control switch on Test element to Disable.

8. Depress Reset pushbutton.

9. Depress Load pushbutton.

10. Observe success indication stop after each hard core test, and final Stop after the last one-cycle FLT.

Success indication stop is indicated by:

SDR set to all F's with parity bits set to B.

11. Depress Start pushbutton to continue after success stop.

12. Rewind FLT tape to load point and Ready.

13. Repeat steps 5 through 9 and proceed to the success indication stop prior to the start of the zero and one-cycle FLT's.

14. IBM personnel insert the error condition in the preselected location.

15. Depress the Start pushbutton to run the one-cycle FLT's.

    One-cycle FLT failure detection stop is indicated by:

    SDR bit 7 set
    Test stop number in SDR indicator bits 16-31
    FLT Fail indicator on.

16. Reference FLT test stop number in FLT Scopex List and check the suspect location list against the location of the error condition. If no comparison is found, continue with step 17; if a comparison is found, continue with step 20.

17. Set FLT Mode switch to Force Pass.

18. Depress Start pushbutton to continue tests.

19. Repeat step 16 until the error condition location is compared, or the FLT success stop is indicated.

20. Remove the error condition from the test element. Ready FLT tape at load point, and repeat steps 5 through 12 to insure that the element is again functioning properly.

b. Operating Procedure (CE):

1. Set the test configuration as follows:

CE Test Configuration

1 CE (Test element)
1 IOCE
1 SE
1 TCU
1 Tape Drive (FLT No. 9 Tape)

2. Set appropriate Main Storage Select and Load Unit switches to the selected configuration.

3. Set Interval Timer off (down), test element Test Switch on, and other configured equipment test switches off.

4. Mount FLT tape on the selected drive and ready.

5. Set Repeat Key off (up).

6. Set Scan Mode switch on Test element to FLT.

7. Set Check Control switch on test element to Disable.

8. Depress System Reset pushbutton.

9. Set the S and T registers to all ones.

10. Depress Load pushbutton.

11. Observe success indication stop [pass trigger-On and Unconditional Terminate bit on (roller 5, position 2)] after each hard core test and Final Stop after the last one-cycle FLT.

    Final Stop is indicated by:

    S, T Registers all ones, Pass Trigger-On and Unconditional Terminate On.

12. Depress Backspace pushbutton twice and the Load pushbutton to continue after success stop.

13. Rewind FLT tape to load point and Ready.

14. Repeat steps 5 through 9 and proceed to the success indication stop prior to the start of the zero and one-cycle FLT's.

15. IBM personnel insert the error condition in the preselected location.

16. Depress the Load pushbutton to run the one-cycle FLT's.

    One-cycle FLT failure detection stop is indicated by:

    Test stop number in S Register indicator bits 0-15. FLT Fail indicator On.

17. Reference FLT test stop number in FLT SCOPEX List and check the suspect location list against the location of the error condition. If no comparison is found, continue with step 17; if a comparison is found, continue with step 20.

18. Depress Backspace twice.

19. Depress Load pushbutton to continue tests.

20. Repeat step 16 until the error condition location is compared, or the FLT success stop is indicated.

21. Remove the error condition from the test element, Ready FLT tape at load point, and repeat steps 5 through 12 to insure that the element is again functioning properly.

6.3.4 System/360-9020D/E System Compatibility. A demonstration of System/360-9020D/E System compatibility will be given during the Factory Acceptance Test. The demonstration will utilize a System/360 Basic Assembler Program.

The Basic Assembler Program is designed to translate a source program written in symbolic language into executable machine language object program. The assembled object program produced by the Assembler may be punched in cards or written on magnetic tape. This is determined by the available system configuration.

A program Wait occurs whenever the program finds it necessary to communicate with the operator. A program Wait is indicated by setting the Wait indicator on the Control panel.

When a program Wait occurs, the three low-order bytes of the Current PSW contains a three-character code. This code identifies the reason for the program Wait. This section defines all operator messages and appropriate operator intervention.

The System/360-9020D/E System Compatibility Test will require a system configuration of:

D or E System

1 CE
1 IOCE (must be IOCE No. 1)
1 SE
1 CC or SC with 1052 Printer Keyboard
1 TCU (must be TCU 1)
1 Tape Drive (9 track)(must be TD 0)
1 2821 CU
1 1403 Printer
1 2540 Read/Punch

Equipment failure will not be considered a failure of the Compatibility Program. Program reruns will be scheduled if such failures occur.

The test will be considered acceptable when it has been ascertained that the object results and predicted results agree, for the test demonstrated. The test will be run using tapes and cards, but the assembled program will be written on tape.

a. Operating Procedure:

1. Configure the required system.

2. Place Check Control switch to Stop.

3. Place the Disable Interval Timer switch to disable and depress the 360 Mode push-button.

4. Check that all other switches and keys are in normal operating positions. (See Spec. Section 4.1)

5. Remove all cards from Read/Punch and perform a Non-Process Run Out on the Card Reader.

6. Place the Source Program deck immediately following the Phase I deck in the Card Reader. Depress End of File and Start pushbuttons to make Card Reader "Ready." Place a reel of tape, with a ring in, on Tape Drive selection "0." Depress Load Rewind and Start to make the tape "Ready."

7. Select the Card Reader with the Load Unit switches and depress Load pushbutton.

8. Upon completion of Phase I, we enter the Wait state and a message "1EI" (Phase I completed, proceed with Phase II) is printed on the far left side of the printer page on the 1403.

9. Clear the Card Read/Punch by removing all cards from the machine and pressing the Start pushbuttons.

10. Place the Phase II deck in the Card Reader. Depress End of File and Start pushbuttons to make Card Reader "Ready." Place blank cards in the Punch and depress Start to make Punch "Ready."

11. Make sure all devices are "Ready" and depress Load pushbutton.

12. Upon completion of Phase II, the Printer should have printed out the program listing and an output message "2EI" (Phase II Completed) on the 1403.

b. The program which was assembled on the Tape Drive will now be punched out on the 2540. This test program sorts sixteen (16) hexidecimal characters and stores them in ascending order.

c. To Load an assembled program into storage for execution, the following items are required:

1. A self-loading Relocating Loader on punched cards.
2. Dump program.
3. The assembled program which was obtained upon completion of Phase II of the Basic Assembler. This will be on punched cards.

d. Operating procedures:

1. Perform a Non-Process Run Out of the Card Read/Punch to clear the Card Reader and to obtain the Assembled program deck from the Card Punch.

2. Clear memory and load the Reader in the following order:

- Relocating Loader
- Dump Program (Remove the last card)
- Assembled program deck
- Last card from Dump Program

3. Make the Card Reader and the Printer "Ready."

4. Set the Load-Unit switches on the CE panel with the address of the Card Reader and depress the Load pushbutton.

The printer should print "PSW's," "GREGS, and "16 numbers" in ascending order. This indicates successful run.

6.3.5 360 Mode Recall Test. The 360 Mode Recall Test will demonstrate the ability of an active operating system to recall an element operating in the 360 Mode.

a. Set test configuration and include all elements and units in Zero - Test switch off.

b. Initialize MDM and define all elements and units. (Refer to Spec. Section 4)

c. Load SEVA Control Program DE0A3, operate in acceptance test mode, and define the active minimum system. (Refer to Spec. Section 4)

d. Place a CE (other than the CE of the minimum system) in 360 Mode by depressing the 360 Mode pushbutton.

e. Wait for the printout "SEVA IS TESTING AND READY FOR SIMULATED FAILURES," and then enter input message QE0C7. $ID_1 \cdot ID_2$ where ID_1 is the identity of the CE in the minimum system, and ID_2 is the identity of the CE in 360 Mode.

f. Observe that the CE configuration changed and that the 360 Mode indicator goes off.

7.0 POWER AND BATTERY DEMONSTRATION TESTS (Ref. ER063-3.2.2 and NS100-3.8.1)

The power demonstration will test the capabilities of the elements and units of the 9020D/E System to control normal application and removal of power, circuit protection facilities, and emergency removal of power.

The battery tests will check the ability of the 9020D/E elements to detect the loss of input power and perform a subsequent switch-over to a temporary battery source.

As specified in each test, checks will be made for proper program output, if applicable, and that respective indicators are displayed correctly.

NOTE: Unload tape drives whenever power is dropped on the associated TCU.

7.1 Test A-Normal Power On/Off (Ref. ER063 - 3.8.3.2) and NS 100 - 3.4.4,3.8.1

7.1.1 Power Interlock Test. This test will demonstrate the ability of the power interlocks to prevent normal power down, unless an element or unit is configured State Zero - Test switch On.

NOTE: There is no provision for a power interlock on the DAU, System Console or SCCU portion of the Configuration Console.

a. Set the test configuration to all elements and units available in State Zero - Test switch Off.

b. Initialize MDM and define the system (Refer to Spec. Section 4.4).

c. Load CE programs D1151 through D11EE and instruct MDM to loop these programs (Sense switch #26).

d. The FAA observer may now direct IBM personnel to attempt dropping power by means of the Power On/Off switch on any element or unit in the Test Configuration. The FAA observer should note that no actual or indicated power loss has occurred, and that the program continues to cycle without interruption.

e. Repeat Step d of the procedure until all available elements and units, except the DAU's, SC and SCCU of the CC, have been tested.

This portion of the test will be considered acceptable when all elements and units have been tested and no power loss or program interruption is encountered.

7.1.2 Test State - Power On/Off Test. This test will demonstrate that normal Power On or Power Off on an inactive element or unit in test state, will not adversely affect program operation in the active system.

a. Set the configuration to the defined minimum system. All other available elements and units will be in State Zero - Test Switch On. (Do not include an RCU in the defined minimum system).

b. Initialize MDM and define the system. (Refer to Spec. Section 4.4).

c. Load CE Programs D1151 through D11EE and instruct MDM to loop these programs. (Sense switch #26).

d. The FAA observer may now direct IBM personnel to drop power by means of the Power On/Off switch on available State Zero - Test switch On, elements and units. The observer should note that the proper indicators are displayed at the System Console or Configuration Console after each element or unit is dropped and that the program cycling in the active system is not interrupted.

NOTE: Do not restore Power to tested units and elements until Spec. Section 7.1.3 is completed.

7.1.3 MPO Switch Test. This test is included under this paragraph to facilitate ease of demonstration and should not be construed to mean that this would be a normal method of removing power from an element or unit that has power applied.

The purpose of this test is to demonstrate the ability of the MPO switch to interrupt prime power in the unit or element and that once pulled, the switch cannot be reset without the services of maintenance personnel.

a. With power down on the previously tested elements and units, pull the MPO switch and attempt to restore power by means of the Power On/Off switch.

b. Attempt to reset the MPO switch.

c. The FAA observer should note that power cannot be restored and that the interlocking device prevents the MPO switch from being reset.

d. Maintenance personnel will reset the MPO switches after testing, and restore power. The FAA observer should note that as power is restored, the program cycling in the active system is not interrupted.

e. The program will then be stopped and the active system reconfigured, substituting previously tested elements and units. The formerly active units and elements will be tested for State Zero - Test switch On and MPO capabilities.

Tests 7.1.2 and 7.1.3 will be considered acceptable when normal Power On/Off and MPO capabilities have been successfully demonstrated without affecting program operation.

7.2 Test B. - Abnormal Element Power Loss and Battery Recharge

This demonstration will check the ability of all elements to detect the loss of prime power, switchover to a battery power source, and either return to normal power if input power is restored, or cycle power off after the preset battery duration has elapsed. After successfully completing an interrupt of input power, one element will be selected to demonstrate the ability to sustain another interrupt of prime power after a minimum recharge period.

a. Set the configuration to the defined minimum system. Elements and units in the configuration will be set to State Zero Test switch Off.

b. The FAA observer may now indicate on which configured element prime power is to be dropped.

c. Initialize MDM and define the system. (Refer to Spec. Section 4.4).

d. Load and cycle the program corresponding to the element selected to be tested.

Element to be Tested		Program to be Run
CE	D1151	RX Format Instruction Program
SE,DE	D22A0	Storage Element/Display Element Program
IOCE	D4050	Tape Drive Functional Program

e. While the program is cycling, drop the Input Circuit Breaker on the selected element. As soon as the On Battery indicator lights on the selected element, reset the Input Circuit Breaker.

f. The FAA observer should note the momentary lighting of the On Battery indicator, and continuous program operation.

g. With the program still cycling, drop the Input Circuit Breaker on the selected element.

h. The FAA observer should note the lighting of the On Battery indicator and that the battery duration period falls within the following specified limits:

CE - 6.5 ± 0.5 seconds
SE,DE - 5.5 ± 0.5 seconds
IOCE - 6.5 ± 0.5 seconds

NOTE: The "On Battery" duration will be measured using a stop watch and is defined as the period from when the "On Battery" indicator lights until the first visible indication of voltage decrease while viewing a voltmeter which is connected across the supply output (+6V for CE, +30V for IOCE, SE, and DE).

i. Repeat the above steps on each CE, SE, IOCE, and DE.

j. On the element selected for the recharge demonstration, the FAA observer should note the time when power has been restored to the element. Lighting of the Sequence Complete light should denote the start of the recharge period.

k. A neon indicator, which is visible through a window on the charger assembly, should be On indicating the batteries are being charged.

l. The following time period should be allowed for recharging the batteries on the selected element, to provide the minimum recharge time ratio of 300 to 1.

Element	Battery Duration	Recharge Time
CE	6.5 sec	32.5 min
SE,DE	5.5 sec	27.5 min
IOCE	6.5 sec	32.5 min

m. Prior to completion of the recharge period, do steps a, c, and d of this procedure. When the time for the recharge period has expired, continue with steps g and h.

The test will be considered acceptable after all elements have successfully demonstrated the ability to continue operation for the preset time from a temporary battery source, and to continue program operation during a momentary loss of main line power, a switch to battery power operation, and a return to main line power. The recharge portion of the test will be considered acceptable when the element successfully demonstrates its ability to again sustain operation from a temporary battery source, for the preset time.

7.3 Test C - Thermal Warning and Protection

This test will demonstrate the thermal warning and protection facilities on all of the elements, PAM's, SCU's, TCU's and SC. Heating the Thermal Sensing Circuit will result first in a Thermal warning, and as the heat application continues, a subsequent sequencing down of power on the element or unit. The thermal sensing shutdown is not interlocked and power will be removed regardless of State or Test switch status.

NOTE: Tapes should be unloaded before this test is performed.

a. Select one of the thermal sensing units on an element or unit located on the logic gates or power module compartments.

b. Direct a heating device at the selected Thermal Sensing unit in a manner that both sections of the thermal unit receive an equal amount of heat.

c. The FAA observer should note the lighting of the Thermal Check indicator on the element or unit and the Power Check indicator on the CC or SC when the warning temperature is reached. Shortly after, the FAA observer should note a power off sequence on the unit or element as the thermal protection temperature is reached.

d. After allowing sufficient time for the thermal unit to cool, perform a Thermal Reset and restore power. to the unit or element.

e. Repeat the test until all elements, PAM's, SCU's, TCU's and SC have been tested.

This test will be considered acceptable when all elements, PAM's, SCU's, TCU's and SC have given the proper warning indication and sequenced power down.

7.4 Test D - Over Voltage/Over Current and Under Voltage Protection

The Over Voltage/Over Current protection facility will be demonstrated on each element, PAM's and CC or SC. This will be accomplished by causing a power module to exceed its maximum allowable output, causing the element or unit to sequence power down.

Under Voltage protection will be demonstrated on each CE and IOCE by causing a power module output to go below its allowable limit, resulting in a sequence of power down.

7.4.1 Over Voltage Test. The following list of power modules may be used to demonstrate an over voltage condition on the respective element or unit and the approximate voltage at which a sequence down should occur.

Element/Unit	Voltage	Module	Over Voltage	Control
CE	+3	01A REG 3	+3.3 to +4.2	Local
	+6	*01A REG 7	+6.6 to +8.4	Remote
	-3	02G REG 2	-3.3 to -4.2	Local
IOCE	+30	REG 11	+34 to +37	Local
	+56	REG 9	+66 to +69	Remote
	+60	REG 5	+66 to +69	Remote
SE	+30	REG 9	+36.5 to +37.5	Local
	-23	REG 15	-24.8 to -25.2	Remote
	+ 3	REG A1	+3.3 to +4.2	Local
DE	+30	REG 6	+36.5 to +37.5	Local
	-23	REG 11	-24.8 to -25.2	Remote
	+ 3	REG A2	+3.3 to +4.2	Local
SC	+48	**PSA-2 or **PSB-2	+55 to +70	Local
CC	+ 3	**02B-B2 or **02C-B2	+3.8 to +4.2	Local
PAM	-48	PSA2	-55 to -70	Local
	+6 Spec	PSD2	+6.6 to 8.5	Local

* Requires loosening the voltage limit collars on the +6V E GT potentiometer.

** Depends on which Duplex supplies are selected on the SC Control Panel, A ro B or the CC Control Panel, B or C.

NOTE: Only modules listed for the IOCE and CE (+6) are monitored on the control panel meter. Therefore, a voltmeter must be connected across the output of the supply to determine the initial voltage reading and the voltage reading when the over voltage is activated.

The power modules to be used for this demonstration are of two types. That is, the remote control modules can be adjusted from a potentiometer located on the front control panel. The local control modules must be adjusted at the power compartment by means of a small potentiometer located on the amplified card assembly of the respective power module.

a. The FAA observer may select a power module to be adjusted for each corresponding element or unit.

b. Note the exact initial voltage reading of the module to be adjusted. If adjustment is to be made remotely, note the relative position of the control potentiometer. If the module is adjusted locally, note the number of turns and the direction adjusted.

c. Adjust the control potentiometer in a direction to cause the output of the module to increase.

d. The FAA observer should note the voltage reading as the module is adjusted to determine when the over voltage circuitry is energized and causes power to sequence down. This will cause the power check indicator on both the element or unit being tested and the CC or SC to light.

e. Return the control potentiometer as near as possible to its original position. Place the Power On/Off switch in the Off position. Depress the Over Voltage/Over Current Reset button located on the Converter/Inverter.

f. Restore power to the element or unit. After Sequence Complete is "ON", readjust the output of the module, if necessary, to read the same as noted in Step b.

g. Repeat Steps a thru f until all elements, PAM's, and CC or SC have demonstrated the ability to detect an over voltage condition.

7.4.2 Over Current Test. The modules that may be used to demonstrate an over current condition on each element or unit is listed below:

Element/Unit	Voltage	Module
CE	+6M	REG 7
	-3	REG 10
	+3	REG 12
IOCE	+18	REG 12
	- 3	REG 2
	+ 6Non	REG 1
SE	+ 6	REG 11
	-18	REG 19
	+30	REG 22

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Element/Unit	Voltage	Module
DE	+6	REG 7
	-23	REG 10
	+30	REG 14
SC	+48	*PSA 2 or *PSB 2
CC	+3	*02B-B2 or *02C-B2
PAM	-48	PSA 2
	-3	PSA 3

*Depends on which duplex supplies are selected on the SC Control panel, A or B or the CC Control Panel, B or C.

a. The FAA observer may select a module to be used for the element or unit being tested.

b. Place the Power On/Off switch to the Off position. For safety reasons, this must be done before proceeding with Step c.

c. Place a clip lead jumper across the output terminal strips so as to short circuit the power module selected.

d. Place the Power On/Off switch to the On position. Power will attempt to sequence up, however, due to the shorted output and resultant current load, the over current circuitry will interrupt the power sequence and cause power to sequence down.

e. The FAA observer should note that the Sequence Complete Indicator does not light and the Power Check indicator remains On at the element or unit and the CC or SC.

f. Place the Power On/Off switch to the Off position. Remove the shorting jumper from the supply output. Depress the Over Voltage/Over Current Reset button located on the Converter/Inverter.

g. Restore power to the element or unit. Repeat Step a through f until all elements and units have demonstrated the ability to detect an over current condition.

7.4.3 CE and IOCE Under Voltage Test

7.4.3.1 CE Under Voltage

a. Turn power off using the DC On/Off switch (do not drop the Input CB). On the CE, locate TB86 in the lower portion of the relay gate (underneath main terminal board assembly). Facing the TB86 board, locate the terminal closest to the lower-left corner of the board. Between this terminal (+)

and terminal 3 (-) record the voltage. This voltage will be re-established in later test steps and has no other test significance.

b. Power up the CE and record the output voltage of PS1 on the filter capacitor bus bars. This voltage will be re-established in a later test step. Adjust PS1 output voltage to a value between 5.9 and 5.0 volts by turning the potentiometer on the amplifier card counter-clockwise. Record this new voltage. Rotate the thumb wheel potentiometer on TB86 counter-clockwise until power drops.

c. With power remaining off and as per instructions in step (a), measure the voltage on TB86 board. The voltage measured should be between 0.20 and 0.75 volts less than the value set up on PS1 in the previous step.

d. Re-establish the original TB86 voltage that was recorded in step (a).

e. Turn power on and re-establish the original PS1 voltage that was recorded in step (b).

f. Repeat this test until each CE has demonstrated the ability to detect an under voltage condition.

7.4.3.2 IOCE Under Voltage

a. On the front panel of the IOCE, note the nominal readin~ of the +6V Non Marginal supply (Reg 1).

b. With a small screwdriver, adjust the local potentiometer located on the amplifier card assembly of the +6V Non Marginal power module so as to cause the output of the supply to decrease. Note the number of turns being adjusted.

c. The FAA observer should note that at approximately 5.2 volts, the under voltage circuit will cause power to sequence down. The Power Check indicator on the IOCE and the CC/SC should come on.

d. Return the potentiometer to its approximate initial setting by turning the adjustment screw in the opposite direction the same number of turns as noted in step b.

e. Restore power to the IOCE. After Sequence Complete, check the reading of the +6V Non Marginal voltage and adjust, if necessary, to its nominal value as noted in step a.

f. Repeat this test until each IOCE has demonstrated the ability to detect an under voltage condition.

The over voltage/over current and under voltage tests will be considered acceptable when all elements, PAMs, and CC or SC have sequenced down power and displayed the proper indication due to an over voltage/over current condition and all CEs and IOCEs have sequenced power down due to an under voltage condition.

7.5 Test E - System Main Line Power Loss

This test will demonstrate the retention of SE data and safe storage of CE registers, upon detection of a main line power loss.

When power is restored to the system, the program residing in the SE will be restarted and the safe stored CE registers displayed.

NOTE: For protection of tapes, unload tape drives before this test is performed.

a. Set the configuration to the defined minimum system State Zero - Test switch Off and all other elements and units in State Zero, Test switch On.

b. Set ATR slot 1 equal to the physical SE used to load the program. If two SE's are available, set ATR slot 2 equal to the second physical SE. If on a 9020E System, also set ATR slot 6 equal to a DE.

c. Set the Disable Interval Timer switch On (down).

d. Clear the Card Reader by pressing the Non-Process Run-Out pushbutton.

e. Place the Safe Store Data Program (DF0A1) into the Card Reader and depress the Start and End-of-File push-buttons.

f. Select the Card Reader with the Load Unit switches on the Control Panel and depress the Load Pushbutton.

When the program is loaded, it will set the contents of GPR 1, 2, 3, and 4 to all 1's except for the last four bits of byte 3, which will indicate the GPR number. The program will then printout the contents of GPR's 0-F followed by storage locations 004010, 004018, 01C010, 01C018, 044010, 044018, 05C010 and 05C018 when only one SE is available or storage locations 084010, 084018, 09C010, 09C018, 0C4010, 0C4018, 0DC010, and 0DC018 when two SE's are available. On a 9020E, the program will also print out storage locations 284010, 284018, 2A4010 and 2A4018. All storage locations printed out at this time will contain all zeros.

IBM personnel will now drop the system main line power by tripping the Input Circuit Breaker.

The elements in State Zero, Test switch Off will switch over to Battery Power for a predetermined time.

Upon detection of the On Battery signal from either the CE, IOCE, DE, or SE, the Safe Store Data Program in the SE assigned to ATR slot 1, will transfer the contents of GPR 1, 2, 3, and 4 into the SE assigned to ATR slot 2. If ATR slot 2 hasn't a SE assigned, the data will be stored in the SE assigned to ATR slot 1.

g. Reset the Input Circuit Breaker to restore system power.

h. Set the configuration to the same defined minimum system.

i. Set the Storage Select switch to the SE being used.

j. Depress the Reset pushbutton and then the PSW - Restart pushbutton to restart the program retained in the SE assigned to ATR slot 1.

k. The program will again print out the contents of all of the GPRs and the storage locations previously printed out. The contents of GPRs 1-4 will not have changed but the storage locations will now contain the same pattern as is set in GPRs 1-4.

l. Repeat the above tests once for each additional CE.

Upon successful demonstration of the following items, Power Test E will be considered acceptable.

1. Printouts of the predicted CE registers and storage locations.

2. Main line power loss.

3. Element switchover to battery power.

4. Ability to restore power and restart the stored program.

5. Printouts of the predicted CE registers containing original data and storage locations after safe storage.

7.6 Test F - System Emergency Power Off

After all other tests have been completed, the Emergency Pull switch on the System Console or Configuration Console will be tested to verify the dynamic operation of the element and unit EPO circuitry. In this test, the EPO switch will be used to remove power from all elements and units within the 9020D/E System.

a. Insure that power is applied to all elements and units.

b. Pull the EPO switch at the System Console or Configuration Console.

c. Observe that power has been removed from all elements and units and that it cannot be restored until the EPO switch is manually reset by maintenance personnel.

d. Place all element and unit test and power switches Off.

e. Maintenance personnel will reset the EPO switch. Observe that power can be restored to all elements and units by setting the power switches to the On position.

f. Initialize the Multiprocessing Diagnostic Monitor (See Spec. Section 4.4).

g. Load and operate the SEVA Control Program (DE0A3).

NOTE: Elements and units will be configured into the active system to check the status of the equipment, and establish an A-1 equipment mode system.

Power Test F will be considered acceptable if the System EPO does provide the actual and indicated power loss to all elements and units, and if the program checks after the restoration of power verify that the "A-1" equipment mode can be met by completing two successful passes of the SEVA Program on an "A-1" system configuration. (Refer to 3.1.5).

8.0 FACTORY ACCEPTANCE EXERCISE (Ref. ER063 - 4.2.2.4)

The factory acceptance exercise will test the 9020D/E System for two to five consecutive 24 hour periods, each of which will cycle the SEVA Program. The operating criteria for the factory exercise are specified in Section 3.1.4. The following are the different Equipment Mode configurations:

A-1 Equipment Mode (9020D)

Element/Unit	Triplex Number	Duplex Number	Simplex Number
CE	(C-1)	1	1
IOCE	2	1	1
SE	(S-2)**	(S-2)**	S
PAM	2	1*	1
SCU	2	1	1
DSU	1/3T	1/3T	1/3T
TCU	2	1	1
Tape Drives	1/3T	1/3T	1/3T

Where C = total no. of CE's
S = total no. of SE's
T = total no. of Tape Drives or DSU's

A-1 Equipment Mode (9020E)

Element/Unit	Triplex Number	Duplex Number	Simplex Number
CE	(C-1)	1	1
IOCE	1	1	1
SE	(S-1)	(S-1)	S
DE	(D-1)	(D-1)	D
DAU	1	1	1
RCU	1	1	1

Where C = total no. of CE's
S = total no. of SE's
D = total no. of DE's

* On those system configurations containing three PAM's, a second PAM may be added at the Test Director's discretion provided that it is not required as part of a maintenance subsystem and an interface path exists to the IOCE in the A-1 Mode.

** On those system configurations containing less than six Storage Elements, the number of on line Storage Elements will be (S-1). The minimum number of on line Storage Elements shall not be less than 2.

Maintenance Equipment Mode (9020D)

Element/Unit	Triplex Number	Duplex Number	Simplex Number
CE	(C-2)	1	Not
IOCE	1	1	Applicable
SE	(S-4)****	(S-2)****	
PAM	1	1	
SCU	1	1	
DSU	1/3T	1/3T	
TCU	1	1***	
Tape Drives	1/3T	1/3T***	

Maintenance Equipment Mode (9020E)

Element/Unit	Triplex Number	Duplex Number	Simplex Number
CE	(C-2)	1	Not
IOCE	1	1	Applicable
SE	(S-3)****	(S-2)****	
DE	(D-3)****	(D-2)****	
DAU	1	1	

*** IBM has the option of using 2 TCU's with 2 tape drives each during the Maintenance Mode.

**** On those system configurations containing less than six Storage Elements/Display Elements, the minimum number of these elements on line during the Maintenance Mode shall not be less than half the number of these elements on that system.

Simplex

The SEVA Program will be used to exercise the equipment under control of the Diagnostic Monitor. The Diagnostic Monitor will funtion as a cyclic program that will control and operate SEVA test programs and routines in a logical sequence. Periodic program results will be provided to record error data and other pertinent information.

If a malfunction of a major element or unit (i.e., CE, SE, DE, IOCE, DAU, PAM, SCU and TCU occurs, the exercise will be interrupted and IBM personnel will initiate appropriate corrective action. The exercise will be interrupted until all major elements and units have been repaired. The operating criteria for the factory exercise are specified in Section 3.

Each 24-hour period will have an optional 3-hour scheduled maintenance period assigned. The option may be exercised at the end of hour 12 of each 24-hour period. If the option is exercised, this time will not count towards the 120 hour requirements. Scheduled maintenance includes routine maintenance and corrective maintenance.

The time to perform corrective maintenance on tape drives or marginal check failures either off-line or during the scheduled maintenance period will not be included in any repair time totals; however, the malfunction which caused reconfiguration or removal will be counted in malfunction totals.

Operating procedures:

a. Set the test configuration to the scheduled A-1 Equipment Mode requirements.

b. At the SC/CC, enable the Read/Punch, Printer and Printer/Keyboard (9020D) to the system by selecting the appropriate IOCE in the I/O Select rotary switches. Depress the ENABLE pushbutton.

c. Enable the Interval Timer.

d. Initialize MDM and define the system.

e. Load and operate the SEVA Control Program (DE0A3).

f. Observe continuous operation of programs and success or failure indication printouts.

g. Record results of the active system on the System Test Data Record forms, and reference the form numbers in the Test Record Number column of the Acceptance Test Log.

Duplex and Triplex

The SEVA Program will be cycled in the A-1 Equipment Mode for 21 hours and in the Maintenance Equipment Mode for 3 hours.

The exercise periods will include the time required to reconfigure the system for substituting elements and units; apply, run and remove margins; and reconfigure the system for malfunction requirements. Periodic manual reconfiguration of redundant elements and units will be made after each 8 hour period of the exercise to allow approximately equal testing of each element and unit. This will also demonstrate the manual reconfiguration capability.

The total test time for each element and unit can be accumulated by referencing the System Functional Test Data Record forms and the Acceptance Test Logs of the exercise periods.

Operating Procedures:

a. Set the test configuration to the scheduled A-1 or Maintenance Equipment Mode requirements.

b. At the SC/CC, enable the Read/Punch, Printer and Printer/Keyboard (9020D) to the system by selecting the appropriate IOCE in the I/O Select rotary switches. Depress Enable pushbutton.

c. Enable the Interval Timer.

d. Initialize MDM and define the system.

e. Load and operate the SEVA Control Program (DE0A3).

f. Observe continuous operation of programs and success or failure indication printouts.

g. Record results of the active system on the System Test Data Records forms, and reference the form numbers in the Test Record Number column of the Acceptance Test Log.

h. When the system has been exercised for an eight hour period or scheduled for the maintenance mode period, reconfigure the active system as shown in the following schedule.

i. Repeat procedure steps a through h as required throughout the exercise.

EXAMPLE 9020D

	EXERCISE HOURS						
	0-8	9-16	17-24	25-32	33-40	41-48	49-56
A-1 MODE (TRIPLEX)							
CE-IOCE-TCU-PAM-SCU	1,2	2,3	3,1	1,2	2,3	3,1	1,2
SE	1,2,3 4,5,6	2,3,4 5,6,7	3,4,5 6,7,8	4,5,6 7,8,1	5,6,7 8,1,2	6,7,8 1,2,3	7,8,1 2,3,4
A-1 MODE (TRIPLEX) PLUS ADDITIONAL CE & SE's							
CE	1,2,3	2,3,4	3,4,1	4,1,2	1,2,3	2,3,4	3,4,1
IOCE-TCU-PAM-SCU	1,2	2,3	3,1	1,2	2,3	3,1	1,2
SE	1,2,3 4,5,6 7,8	2,3,4 5,6,7 8,9	3,4,5 6,7,8 9,10	4,5,6 7,8,9 10,1	5,6,7 8,9,10 1,2	6,7,8 9,10,1 2,3	7,8,9 10,1,2 3,4
A-1 MODE (DUPLEX)							
CE-IOCE-TCU-PAM-SCU	1	2	1	2	1	2	1
SE	1,2,3 4,5,6	2,3,4 5,6,7	3,4,5 6,7,8	4,5,6 7,8,1	5,6,7 8,1,2	6,7,8 1,2,3	7,8,1 2,3,4

NOTE* EACH 24 HOUR PERIOD WILL HAVE A 3-HOUR SCHEDULED MAINTENANCE PERIOD ASSIGNED, THIS PERIOD WILL BE EXERCISED AT THE END OF HOUR 12 OF EACH 24-HOUR PERIOD.

REPEAT THE ABOVE ROTATION SCHEDULE AS REQUIRED.

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EXAMPLE 9020E

	EXERCISE HOURS						
	0-8	9-16	17-24	25-32	33-40	41-48	49-56
A-1 MODE (TRIPLEX)							
CE	1,2	2,3	3,1	1,2	2,3	3,1	1,2
IOCE-DAU-RCU	1	2	1	2	1	2	1
SE-DE	1,2,3	2,3,4	3,4,5	4,5,1	5,1,2	1,2,3	2,3,4
A-1 MODE (TRIPLEX) PLUS ADDITIONAL CE)							
CE	1,2,3	2,3,4	3,4,1	4,1,2	1,2,3	2,3,4	3,4,1
IOCE-DAU-RCU	1	2	1	2	1	2	1
SE-DE	1,2,3	2,3,4	3,4,5	4,5,1	5,1,2	1,2,3	2,3,4

NOTE* EACH 24 HOUR PERIOD WILL HAVE A 3-HOUR SCHEDULED MAINTENANCE PERIOD ASSIGNED, THIS PERIOD WILL BE EXERCISED AT THE END OF HOUR 12 OF EACH 24-HOUR PERIOD.

REPEAT THE ABOVE ROTATION SCHEDULE AS REQUIRED.

8.1 Marginal Checking

During the SEVA Acceptance Exercise, margins will be applied on the A-1 Mode equipment for a total of 6 hours of positive excursions and 6 hours of negative excursions.

The system is most susceptible to noise at maximum margin excursions; therefore, a 12 hour check of noise susceptibility is performed during the application of maximum margins.

The time required to apply the margin voltages to the system will be counted towards the aggregate marginal checking requirement if the set up does not exceed 15 minutes. The control panel meters and voltmeters will be used to adjust the +6M voltages to the prescribed margin.

NOTE: Failures will not be counted while the marginal voltage potentiometers are being adjusted.

Operating Procedure:

a. Application of marginal voltages

1. Set the Margin Voltage Select switch to monitor the +6M voltage being adjusted.

2. Adjust the +6M voltage to the desired ±0.5 volt excursion.

3. Note that the marginal voltage indicator is On.

4. Repeat steps 1, 2, and 3 for all +6M voltages on all active element or units.

5. Check for continued proper exercise operation.

6. Record the time required to apply margins to the active system and the start time of the marginal check period.

b. Removal of marginal voltages

1. Set the Margin Voltage Select switch to monitor the +6M voltage being adjusted.

2. Adjust the +6M voltage to its nominal setting.

3. Note that the marginal voltage indicator is Off.

4. Repeat steps 1, 2, and 3 for all +6M voltages on all active elements and units.

5. Check for continued proper exercise operation.

6. Record the stop time of the marginal check period and remove margins.

APPENDIX A

FACTORY ACCEPTANCE TEST

SEQUENCE SCHEDULE

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-001	CE	SWITCH DEMONSTRATION	5.1.1
U-002	IOCE	SWITCH DEMONSTRATION	5.1.2
U-003	SE 1-4	SWITCH DEMONSTRATION	5.1.3
U-004	SE 5-8	SWITCH DEMONSTRATION	5.1.3
U-005	SE 9-10	SWITCH DEMONSTRATION	5.1.3
U-006	SE 1-4	TIMING DEMONSTRATION	5.1.4
U-007	SE 5-8	TIMING DEMONSTRATION	5.1.4
U-008	SE 9-10	TIMING DEMONSTRATION	5.1.4
U-013	SC	SWITCH DEMONSTRATION	5.1.7
U-014	SC	INTERFACE DEMONSTRATION	5.1.7
U-017	PAM	SWITCH DEMONSTRATION	5.1.9
U-018	DASF	SWITCH DEMONSTRATION	5.1.10
U-019	TCU	SWITCH DEMONSTRATION	5.1.11
U-020	I/O TESTER 2540/1403	SWITCH DEMONSTRATION	5.1.12
U-021	1052	SWITCH DEMONSTRATION	5.1.13
U-101	CE 1	FUNCTIONAL TEST	5.2.1
U-102	CE 2	FUNCTIONAL TEST	5.2.1
U-103	CE 3	FUNCTIONAL TEST	5.2.1
U-104	CE 4	FUNCTIONAL TEST	5.2.1
U-105	CE/SE/DE	ATR TEST	5.2.1
U-106	IOCE 1	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-107	IOCE 2	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-108	IOCE 3	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-109	DASF 1	FUNCTIONAL TEST	5.2.2
U-110	DASF 2	FUNCTIONAL TEST	5.2.2
U-111	DASF 3	FUNCTIONAL TEST	5.2.2

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-112	TCU 1,TD 1-4	FUNCTIONAL TEST	5.2.2
U-113	TCU 1,TD 5-8	FUNCTIONAL TEST	5.2.2
U-114	TCU 2,TD 1-4	FUNCTIONAL TEST	5.2.2
U-115	TCU 2,TD 5-8	FUNCTIONAL TEST	5.2.2
U-116	TCU 3,TD 1-4	FUNCTIONAL TEST	5.2.2
U-117	TCU 3,TD 5-8	FUNCTIONAL TEST	5.2.2
U-118	SCU	TWO CHANNEL SWITCH TESTS	5.2.2
U-119	TCU	DUAL INTERFACE TESTS	5.2.2
U-120	IOCE 1	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-121	IOCE 2	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-122	IOCE 3	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-123	IOCE 1	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-124	IOCE 2	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-125	IOCE 3	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-126	SE 1-3	FUNCTIONAL TEST	5.2.4
U-127	SE 4-6	FUNCTIONAL TEST	5.2.4
U-128	SE 7-9	FUNCTIONAL TEST	5.2.4
U-129	SE 10	FUNCTIONAL TEST	5.2.4
U-133	SC	FUNCTIONAL TEST	5.2.6
U-135	PAM	FUNCTIONAL TEST	5.2.8
U-136	PAM	DUAL INTERFACE TESTS	5.2.8
U-137	2821	FUNCTIONAL TEST, 2540, 1403	5.2.9
U-138	2821	TWO CHANNEL SWITCH TEST	5.2.9
U-139	1052	FUNCTIONAL TEST	5.2.10
U-142	IOCE 1	DIAGNOSTIC MODE FUNCTIONAL DEMO.	5.2.12
U-143	IOCE 2	DIAGNOSTIC MODE FUNCTIONAL DEMO.	5.2.12

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-144	IOCE 3	DIAGNOSTIC MODE FUNCTIONAL DEMO.	5.2.12
U-145	IOCE	I/O PROCESSOR OPERATION DEMO	5.2.13
U-146	CE/IOCE/SE/DE	LOG-OUT DEMONSTRATION	5.2.14
U-147	IOCE	FLT FUNCTIONAL TEST	5.2.15
U-148	CE	FLT FUNCTIONAL TEST	5.2.15

SYSTEM TESTS

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
S-001	SYSTEM	RECONFIGURATION TEST A	6.1.1
S-002	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-003	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-004	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-005	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-006	SYSTEM	RECONFIGURATION TEST C	6.1.3
S-007	SYSTEM	RECONFIGURATION TEST D	6.1.4
S-120	SYSTEM	EIGHT TIMED SAMPLE PROBLEMS	6.3.1
S-123	SYSTEM	360-9020 COMPATIBILITY	6.3.4
S-124	SYSTEM	360 MODE RECALL TEST	6.3.5
S-131	SYSTEM	POWER INTERLOCK TEST	7.1.1
S-132	SYSTEM	TEST STATE - POWER ON/OFF	7.1.2
S-133	SYSTEM	MPO SWITCH TEST	7.1.3
S-134	CE/IOCE/SE/DE	ABNORMAL POWER LOSS AND BATTERY RECHARGE	7.2
S-135	SYSTEM	THERMAL WARNING AND PROTECTION	7.3
S-136	SYSTEM	OVER VOLTAGE	7.4.1
S-137	SYSTEM	OVER CURRENT	7.4.2
S-138	SYSTEM	UNDER VOLTAGE	7.4.3
S-150	SYSTEM	FACTORY ACCEPTANCE EXERCISE	8.0
S-160	SYSTEM	SYSTEM EPO	7.6

9020E SYSTEM
UNIT TESTS

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-001	CE	SWITCH DEMONSTRATION	5.1.1
U-002	IOCE	SWITCH DEMONSTRATION	5.1.2
U-003	SE 1-4	SWITCH DEMONSTRATION	5.1.3
U-004	SE 5	SWITCH DEMONSTRATION	5.1.3
U-006	SE 1-4	TIMING DEMONSTRATION	5.1.4
U-007	SE 5	TIMING DEMONSTRATION	5.1.4
U-009	DE 1-4	SWITCH DEMONSTRATION	5.1.5
U-010	DE 5	SWITCH DEMONSTRATION	5.1.5
U-011	DE 1-4	TIMING DEMONSTRATION	5.1.6
U-012	DE 5	TIMING DEMONSTRATION	5.1.6
U-015	CC	SWITCH DEMONSTRATION	5.1.8
U-016	CC	INTERFACE DEMONSTRATION	5.1.8
U-019	TCU	SWITCH DEMONSTRATION	5.1.11
U-020	I/O TESTER 2540/1403	SWITCH DEMONSTRATION	5.1.12
U-021	1052	SWITCH DEMONSTRATION	5.1.13
U-022	DAU	SWITCH DEMONSTRATION	5.1.14
U-101	CE 1	FUNCTIONAL TEST	5.2.1
U-102	CE 2	FUNCTIONAL TEST	5.2.1
U-103	CE 3	FUNCTIONAL TEST	5.2.1
U-104	CE 4	FUNCTIONAL TEST	5.2.1
U-105	CE/SE/DE	ATR TEST	5.2.1
U-106	IOCE 1	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-107	IOCE 2	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-108	IOCE 3	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-112	TCU#1,TD#1-4	FUNCTIONAL TEST	5.2.2

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-113	TCU#1,TD#5-8	FUNCTIONAL TEST	5.2.2
U-114	TCU#2,TD#1-4	FUNCTIONAL TEST	5.2.2
U-115	TCU#2,TD#5-8	FUNCTIONAL TEST	5.2.2
U-116	TCU#3,TD#1-4	FUNCTIONAL TEST	5.2.2
U-117	TCU#3,TD#5-8	FUNCTIONAL TEST	5.2.2
U-119	TCU	DUAL INTERFACE TESTS	5.2.2
U-120	IOCE 1	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-121	IOCE 2	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-122	IOCE 3	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-123	IOCE 1	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-124	IOCE 2	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-125	IOCE 3	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-126	SE 1-3	FUNCTIONAL TEST	5.2.4
U-127	SE 4-5	FUNCTIONAL TEST	5.2.4
U-130	DE 1,2	FUNCTIONAL TEST	5.2.5
U-131	DE 3,4	FUNCTIONAL TEST	5.2.5
U-132	DE 5	FUNCTIONAL TEST	5.2.5
U-134	CC	FUNCTIONAL TEST	5.2.7
U-137	2821	FUNCTIONAL TEST, 2540, 1403	5.2.9
U-139	1052	FUNCTIONAL TEST	5.2.10
U-140	DAU	FUNCTIONAL TEST	5.2.11
U-141	DAU	TWO PROCESSOR SWITCH TEST	5.2.11
U-142	IOCE 1	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-143	IOCE 2	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-144	IOCE 3	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-145	IOCE	I/O PROCESSOR OPERATION DEMONSTRATION	5.2.13

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-146	CE/IOCE/SE/DE	LOG-OUT DEMONSTRATION	5.2.14
U-147	IOCE	FLT FUNCTIONAL TEST	5.2.15
U-148	CE	FLT FUNCTIONAL TEST	5.2.15

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SYSTEM TEST

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
S-001	SYSTEM	RECONFIGURATION TEST A	6.1.1
S-002	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-003	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-004	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-005	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-006	SYSTEM	RECONFIGURATION TEST C	6.1.3
S-007	SYSTEM	RECONFIGURATION TEST D	6.1.4
S-120	SYSTEM	EIGHT TIME SAMPLE PROBLEMS	6.3.1
S-121	SYSTEM	DISPLAY INSTRUCTION PERF. TEST	6.3.2
S-123	SYSTEM	360-9020 COMPATIBILITY	6.3.4
S-124	SYSTEM	360 MODE RECALL TEST	6.3.5
S-131	SYSTEM	POWER INTERLOCK TEST	7.1.1
S-132	SYSTEM	TEST STATE-POWER ON/OFF	7.1.2
S-133	SYSTEM	MPO SWITCH TEST	7.1.3
S-134	CE/IOCE/SE/DE	ABNORMAL POWER LOSS AND BATTERY RECHARGE	7.2
S-135	SYSTEM	THERMAL WARNING AND PROTECTION	7.3
S-136	SYSTEM	OVER/VOLTAGE	7.4.1
S-137	SYSTEM	OVER/CURRENT	7.4.2
S-138	SYSTEM	UNDER/VOLTAGE	7.4.3
S-150	SYSTEM	FACTORY ACCEPTANCE EXERCISE	8.0
S-160	SYSTEM	SYSTEM EPO	7.6

APPENDIX B

FIELD ACCEPTANCE TEST

SEQUENCE SCHEDULE

9020D SYSTEM
UNIT TESTS

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-001	CE	SWITCH DEMONSTRATION	5.1.1
U-002	IOCE	SWITCH DEMONSTRATION	5.1.2
U-003	SE 1-4	SWITCH DEMONSTRATION	5.1.3
U-004	SE 5-8	SWITCH DEMONSTRATION	5.1.3
U-005	SE 9-10	SWITCH DEMONSTRATION	5.1.3
U-006	SE 1-4	TIMING DEMONSTRATION	5.1.4
U-007	SE 5-8	TIMING DEMONSTRATION	5.1.4
U-008	SE 9-10	TIMING DEMONSTRATION	5.1.4
U-013	SC	SWITCH DEMONSTRATION	5.1.7
U-014	SC	INTERFACE DEMONSTRATION	5.1.7
U-017	PAM	SWITCH DEMONSTRATION	5.1.9
U-018	DASF	SWITCH DEMONSTRATION	5.1.10
U-019	TCU	SWITCH DEMONSTRATION	5.1.11
U-020	I/O TESTER 2540/1403	SWITCH DEMONSTRATION	5.1.12
U-021	1052	SWITCH DEMONSTRATION	5.1.13
U-101	CE 1	FUNCTIONAL TEST	5.2.1
U-102	CE 2	FUNCTIONAL TEST	5.2.1
U-103	CE 3	FUNCTIONAL TEST	5.2.1
U-104	CE 4	FUNCTIONAL TEST	5.2.1
U-105	CE/SE/DE	ATR TEST	5.2.1
U-106	IOCE 1	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-107	IOCE 2	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-108	IOCE 3	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-109	DASF 1	FUNCTIONAL TEST	5.2.2
U-110	DASF 2	FUNCTIONAL TEST	5.2.2

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-111	DASF 3	FUNCTIONAL TEST	5.2.2
U-112	TCU#1,TD#1-4	FUNCTIONAL TEST	5.2.2
U-113	TCU#1,TD#5-8	FUNCTIONAL TEST	5.2.2
U-114	TCU#2,TD#1-4	FUNCTIONAL TEST	5.2.2
U-115	TCU#2,TD#5-8	FUNCTIONAL TEST	5.2.2
U-116	TCU#3,TD#1-4	FUNCTIONAL TEST	5.2.2
U-117	TCU#3,TD#5-8	FUNCTIONAL TEST	5.2.2
U-118	SCU	TWO CHANNEL SWITCH TESTS	5.2.2
U-119	TCU	DUAL INTERFACE TESTS	5.2.2
U-123	IOCE 1	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-124	IOCE 2	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-125	IOCE 3	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-126	SE 1-3	FUNCTIONAL TEST	5.2.4
U-127	SE 4-6	FUNCTIONAL TEST	5.2.4
U-128	SE 7-9	FUNCTIONAL TEST	5.2.4
U-129	SE 10	FUNCTIONAL TEST	5.2.4
U-133	SC	FUNCTIONAL TEST	5.2.6
U-135	PAM	FUNCTIONAL TEST	5.2.8
U-136	PAM	DUAL INTERFACE TESTS	5.2.8
U-137	2821	FUNCTIONAL TEST, 2540, 1403	5.2.9
U-138	2821	TWO CHANNEL SWITCH TEST	5.2.9
U-139	1052	FUNCTIONAL TEST	5.2.10
U-142	IOCE 1	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-143	IOCE 2	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-144	IOCE 3	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC.REF.
U-145	IOCE	I/O PROCESSOR OPERATION DEMONSTRATION	5.2.13
U-146	CE/IOCE/SE/DE	LOG-OUT DEMONSTRATION	5.2.14
U-147	IOCE	FLT FUNCTIONAL TEST	5.2.15
U-148	CE	FLT FUNCTIONAL TEST	5.2.15

SYSTEM TEST

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF
S-001	SYSTEM	RECONFIGURATION TEST A	6.1.1
S-002	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-003	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-004	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-005	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-006	SYSTEM	RECONFIGURATION TEST C	6.1.3
S-007	SYSTEM	RECONFIGURATION TEST D	6.1.4
S-101	SYSTEM	SEVA	6.2.1
S-122	SYSTEM	FLT PRACTICAL TEST	6.3.3
S-124	SYSTEM	360 MODE RECALL TEST	6.3.5
S-131	SYSTEM	POWER INTERLOCK TEST	7.1.1
S-132	SYSTEM	TEST STATE-POWER ON/OFF	7.1.2
S-133	SYSTEM	MPO SWITCH TEST	7.1.3
S-134	CE/IOCE/SE/DE	ABNORMAL POWER LOSS AND BATTERY RECHARGE	7.2
S-135	SYSTEM	THERMAL WARNING AND PROTECTION	7.3
S-136	SYSTEM	OVER/VOLTAGE	7.4.1
S-137	SYSTEM	OVER/CURRENT	7.4.2
S-138	SYSTEM	UNDER/VOLTAGE	7.4.3
S-139	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-140	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-141	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-142	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-160	SYSTEM	SYSTEM EPO	7.6

9020E SYSTEM
UNIT TESTS

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-001	CE	SWITCH DEMONSTRATION	5.1.1
U-002	IOCE	SWITCH DEMONSTRATION	5.1.2
U-003	SE 1-4	SWITCH DEMONSTRATION	5.1.3
U-004	SE 5	SWITCH DEMONSTRATION	5.1.3
U-006	SE 1-4	TIMING DEMONSTRATION	5.1.4
U-007	SE 5	TIMING DEMONSTRATION	5.1.4
U-009	DE 1-4	SWITCH DEMONSTRATION	5.1.5
U-010	DE 5	SWITCH DEMONSTRATION	5.1.5
U-011	DE 1-4	TIMING DEMONSTRATION	5.1.6
U-012	DE 5	TIMING DEMONSTRATION	5.1.6
U-015	CC	SWITCH DEMONSTRATION	5.1.8
U-016	CC	INTERFACE DEMONSTRATION	5.1.8
U-019	TCU	SWITCH DEMONSTRATION	5.1.11
U-020	I/O TESTER 2540/1403	SWITCH DEMONSTRATION	5.1.12
U-021	1052	SWITCH DEMONSTRATION	5.1.13
U-022	DAU	SWITCH DEMONSTRATION	5.1.14
U-101	CE 1	FUNCTIONAL TEST	5.2.1
U-102	CE 2	FUNCTIONAL TEST	5.2.1
U-103	CE 3	FUNCTIONAL TEST	5.2.1
U-104	CE 4	FUNCTIONAL TEST	5.2.1
U-105	CE/SE/DE	ATR TEST	5.2.1
U-106	IOCE 1	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-107	IOCE 2	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-108	IOCE 3	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-112	TCU#1,TD#1-4	FUNCTIONAL TEST	5.2.2
U-113	TCU#1,TD#5-8	FUNCTIONAL TEST	5.2.2

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-114	TCU#2,TD#1-4	FUNCTIONAL TEST	5.2.2
U-115	TCU#2,TD#5-8	FUNCTIONAL TEST	5.2.2
U-116	TCU#3,TD#1-4	FUNCTIONAL TEST	5.2.2
U-117	TCU#4,TD#5-8	FUNCTIONAL TEST	5.2.2
U-119	TCU	DUAL INTERFACE TESTS	5.2.2
U-123	IOCE 1	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-124	IOCE 2	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-125	IOCE 3	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-126	SE 1-3	FUNCTIONAL TEST	5.2.4
U-127	SE 4-5	FUNCTIONAL TEST	5.2.4
U-130	DE 1,2	FUNCTIONAL TEST	5.2.5
U-131	DE 3,4	FUNCTIONAL TEST	5.2.5
U-132	DE 5	FUNCTIONAL TEST	5.2.5
U-134	CC	FUNCTIONAL TEST	5.2.7
U-137	2821	FUNCTIONAL TEST, 2540, 1403	5.2.9
U-139	1052	FUNCTIONAL TEST	5.2.10
U-140	DAU	FUNCTIONAL TEST	5.2.11
U-141	DAU	TWO PROCESSOR SWITCH TEST	5.2.11
U-142	IOCE 1	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-143	IOCE 2	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-144	IOCE 3	DIAG. MODE FUNCTIONAL DEMONSTRATION	5.2.12
U-145	IOCE	I/O PROCESSOR OPERATION DEMONSTRATION	5.2.13
U-146	CE/IOCE/SE/DE	LOG-OUT DEMONSTRATION	5.2.14

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TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-147	IOCE	FLT FUNCTIONAL TEST	5.2.15
U-148	CE	FLT FUNCTIONAL TEST	5.2.15

SYSTEM TEST

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
S-001	SYSTEM	RECONFIGURATION TEST A	6.1.1
S-002	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-003	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-004	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-005	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-006	SYSTEM	RECONFIGURATION TEST C	6.1.3
S-007	SYSTEM	RECONFIGURATION TEST D	6.1.4
S-101	SYSTEM	SEVA	6.2.1
S-121	SYSTEM	DISPLAY INSTRUCTION PERF. TEST	6.3.2
S-122	SYSTEM	FLT PRACTICAL TEST	6.3.3
S-124	SYSTEM	360 MODE RECALL TEST	6.3.5
S-131	SYSTEM	POWER INTERLOCK TEST	7.1.1
S-132	SYSTEM	TEST STATE-POWER ON/OFF	7.1.2
S-133	SYSTEM	MPO SWITCH TEST	7.1.3
S-134	CE/IOCE/SE/DE	ABNORMAL POWER LOSS AND BATTERY RECHARGE	7.2
S-135	SYSTEM	THERMAL WARNING AND PROTECTION	7.3
S-136	SYSTEM	OVER/VOLTAGE	7.4.1
S-137	SYSTEM	OVER/CURRENT	7.4.2
S-138	SYSTEM	UNDER/VOLTAGE	7.4.3
S-139	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-140	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-141	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-142	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-160	SYSTEM	SYSTEM EPO	7.6

APPENDIX C

ABBREVIATIONS

ATR	Address Translation Register
BSM	Basic Storage Module
CB	Circuit Breaker
CC	Configuration Console
CCR	Configuration Control Register
CCW	Channel Command Word
CE	Computing Element
CEDA	CPU (CE) Error Detection and Analysis
CLU	Common Logic Unit
CPU	Central Processing Unit (CE)
CTC	Channel-to-Channel
CU	Control Unit
DAR	Diagnose Accessible Register
DASF	Direct Access Storage Facility
DAU	Data Adapter Unit
DE	Display Element
DSU	Disk Storage Unit
EOB	End of Block
EOF	End of File
EPO	Emergency Power Off
FLT	Fault Locating Test
HEX	Hexadecimal
IAR	Instruction Address Register
IC	Instruction Counter
IOCE	Input/Output Control Element
IPL	Initial Program Load
IRG	Inter-Record Gap
KB	Kilo Byte
LPSW	Load Program Status Word
LS	Local Storage
MACH	Maintenance and Channel Storage
MDM	Multiprocessing Diagnostic Monitor
MPO	Master Power Off
MS	Main Storage
OBS	On Battery Signal
OTC	Out of Tolerance Check
PAM	Peripheral Adapter Module
PDU	Power Distribution Unit
PSA	Preferential Storage Area
PSBAR	Preferential Storage Base Address Register
PSW	Program Status Word
RCU	Reconfiguration Control Unit
ROS	Read Only Storage
RR	Register to Register Operation
RS	Register to Storage Operation
RX	Register to Indexed Storage Operation
SAR	Storage Address Register
SC	System Console
SCCU	System Console Control Unit
SCON	Set Configuration
SCOPEX	Scoping Index
SCU	Storage Control Unit
SDM	Subsystem Diagnostic Monitor
SDR	Storage Data Register

SE	Storage Element
SEVA	System Evaluation
SI	Storage and Immediate Operation
SMMC	System Maintenance Monitor Console
SPCI	Set Program Controlled Interrupt
SPCR	Storage Protect Compare Register
SPDR	Storage Protect Data Register
SS	Storage to Storage Operation
TCU	Tape Control Unit
UDT	Unit Definition Table

APPENDIX D

DEFINITIONS

Active System	Configured elements and/or units which are performing the operating program's functions.
Diagnostic Monitor	The supervisory program used to control test programs and reconfiguration programs and to handle the interrupt system, input/output facilities and communication requirements of the IBM 9020 System.
Disk Pack	Compact disk assembly composed of 11 disks mounted 1/2 inch apart on a vertical shaft.
Element	Major system components which also contain battery back-up; CE's, IOCE's, DE's and SE's.
Human Interface	The communication linkage between the Diagnostic Monitor and the program operator.
Initialization	Messages for the Diagnostic Monitor which provide unit and task assignments for the operating system.
Integrated System	Consisting of more than one subsystem.
Input Message	A standard set of messages available for communication with the Diagnostic Monitor by the operator.
Library Tape	A master tape upon which programs have been assembled.
Matrix Printout	A monitor table which is printed out defining the entire system or subsystem available for use by the Monitor.
Multiprocessing	A mode of operation which will exercise simultaneously a minimum of two CE's assigned to the maintenance tasks.
Multiprogramming	The interleaved execution of two or more programs by the same processor.
One Cycle Test	A test in which data is transferred through normal machine logic to reach the triggers being tested.
Output Message	A set of messages available for communication with the operator by the program.
Prime Power	A 208 VAC power source.

Relocating Loader	A program which will relocate programs in storage locations specified by the operator.
Scratch Tapes	A magnetic tape used for Temporary Storage.
State Zero	A state in which the test switch is operative.
Subsystem	A minimum number of elements and units required to run the desired programs.
Test Switch On	A state in which all manual controls are operative.
Unit	System components which operate mainly as I/O device control units and do not contain battery back-up.
Work Tapes	Same as Scratch Tapes.
Zero Cycle Tests	A test in which data is placed in machine triggers through direct paths and then tested.

APPENDIX E

TEST PROGRAMS

CROSS REFERENCE

TEST PROGRAMS

Section ID	Program Name	Acceptance Test Section
D0D50	Multiprocessing Diagnostic Monitor	All
D1003	LA Instruction	5.2.12
D1004	L Instruction	5.2.12
D1005	ST Instruction	5.2.12
D1006	A Instruction	5.2.12
D1007	S, C Instructions	5.2.12
D1008	CL Instructions	5.2.12
D1009	N, O, X Instructions	5.2.12
D100C	AL, SL Instructions	5.2.12
D1010	LR Instruction, Part 1	5.2.12
D1011	LR Instruction, Part 2	5.2.12
D1012	LR Instruction, Part 3	5.2.12
D1013	LR Instruction, Part 4	5.2.12
D1014	AR Instruction	5.2.12
D1015	SR, CR Instructions	5.2.12
D1016	CLR Instruction	5.2.12
D1017	NR Instruction	5.2.12
D1018	OR Instruction	5.2.12
D1019	XR Instruction	5.2.12
D101A	LPR, LNR, LTR, LCR Instructions	5.2.12
D101B	ALR, SLR Instructions	5.2.12
D101F	BCR, BC Instructions	5.2.12
D1020	BALR, BAL Instructions	5.2.12
D1021	BCT, BCTR Instructions	5.2.12
D1022	BXH, BXLE Instructions	5.2.12
D1023	Branch Instruction	5.2.12

D1027	LH, STH, AH, SH, CH Instructions	5.2.12
D102A	SRL, SRA, SLL, SLA Instructions	5.2.12
D102D	TM Instruction	5.2.12
D102E	CLI Instruction	5.2.12
D102F	MVI Instruction	5.2.12
D1030	NI Instruction	5.2.12
D1031	OI Instruction	5.2.12
D1032	XI Instruction	5.2.12
D1037	STM Instruction	5.2.12
D1038	STM, LM Instructions	5.2.12
D103C	SVC, LPSW, SPM, SSM Instructions	5.2.12
D103F	MH Instruction	5.2.12
D1040	M Instruction	5.2.12
D1041	MR Instruction	5.2.12
D1042	D Instruction	5.2.12
D1043	DR Instruction	5.2.12
D1045	IC, STC Instruction	5.2.12
D1047	SRDL, SRDA, SLDL, SLDA Instructions	5.2.12
D104A	CLC Instruction	5.2.12
D104B	CLC Instruction	5.2.12
D104C	CLC, MVC Instructions	5.2.12
D104D	NC Instruction	5.2.12
D104E	OC Instruction	5.2.12
D104F	XC Instruction	5.2.12
D1050	MVO Instruction	5.2.12
D1051	MVN Instruction	5.2.12
D1052	MVZ Instruction	5.2.12

D1053	MVW Instruction	5.2.12
D105A	CVB, CVD Instructions	5.2.12
D105C	TR Instruction	5.2.12
D105D	TRT Instruction	5.2.12
D105E	PACK, UNPK Instructions	5.2.12
D105F	PACK, UNPK	5.2.12
D1060	NC, OC, XC, MVO, MVZ Boundary Instructions	5.2.12
D1063	Small Binary Instruction Set 1	5.2.12
D1064	Small Binary Instruction Set 2	5.2.12
D1065	Small Binary Instruction Set 3	5.2.12
D1066	Standard Instruction Set, Part 1	5.2.12
D1067	Standard Instruction Set, Part 2	5.2.12
D1068	LDA, LI, TS, WRD Instructions	5.2.12
D1069	LDA, LI, TS, WRD Instructions	5.2.12
D106B	Program Interrupts, Part 1	5.2.12
D106C	Program Interrupts, Part 2	5.2.12
D106D	Program Interrupts, Part 3	5.2.12
D106E	Operation Exceptions	5.2.12
D1071	Execute Program Interrupts	5.2.12
D1072	Execute Program Interrupts	5.2.12
D1075	Pair Instruction Scrambler	5.2.12
D1076	Diagnose Kernels, Part 1	5.2.12
D1077	Diagnose Kernels, Part 2	5.2.12
D1101	Basic Compute Element Test, Part 1	5.2.1
D1102	Basic Compute Element Test, Part 2	5.2.1
D1103	Basic Compute Element Test, Part 3	5.2.1

D1108	Basic Diagnose Log-Out	5.2.1
D1111	CEDA 1	5.2.1
D1112	CEDA 2	5.2.1
D1113	CEDA 3	5.2.1
D1114	CEDA 4	5.2.1
D1115	CEDA 5	5.2.1
D1151	LA Instruction	5.2.1, 7.1.1, 7.1.2, 7.2
D1152	L Instruction	5.2.1, 7.1.1, 7.1.2
D1153	ST Instruction	5.2.1, 7.1.1, 7.1.2
D1154	A Instruction	5.2.1, 7.1.1, 7.1.2
D1155	S, C Instructions	5.2.1, 7.1.1, 7.1.2
D1156	CL Instruction	5.2.1, 7.1.1, 7.1.2
D1157	N, O, X Instructions	5.2.1, 7.1.1, 7.1.2
D115A	AL, SL Instructions	5.2.1, 7.1.1, 7.1.2
D115C	LR Instruction, Part 1	5.2.1, 7.1.1, 7.1.2
D115D	LR Instruction, Part 2	5.2.1, 7.1.1, 7.1.2
D115E	LR Instruction, Part 3	5.2.1, 7.1.1, 7.1.2
D115F	LR Instruction, Part 4	5.2.1, 7.1.1, 7.1.2
D1160	AR Instruction	5.2.1, 7.1.1, 7.1.2
D1161	SR, CR Instructions	5.2.1, 7.1.1, 7.1.2

D1162	CLR Instruction	5.2.1, 7.1.1, 7.1.2
D1163	NR Instruction	5.2.1, 7.1.1 7.1.2
D1164	OR Instruction	5.2.1, 7.1.1, 7.1.2
D1165	XR Instruction	5.2.1, 7.1.1 7.1.2
D1166	LPR, LNR, LTR, LCR Instruction	5.2.1, 7.1.1 7.1.2
D1167	ALR, SLR Instruction	5.2.1, 7.1.1, 7.1.2
D1169	BCR, BC Instructions	5.2.1, 7.1.1, 7.1.2
D116A	BALR Instruction	5.2.1, 7.1.1 7.1.2
D116B	BCT, BCTR Instructions	5.2.1, 7.1.1, 7.1.2
D116C	BXH, BXLE Instructions	5.2.1, 7.1.1, 7.1.2
D116D	Branch Instructions	5.2.1, 7.1.1, 7.1.2
D116F	LH, STH, AH, SH, CH Instructions	5.2.1, 7.1.1, 7.1.2
D1171	SRL, SRA, SLL, SLA Instructions	5.2.1, 7.1.1, 7.1.2
D1173	TM Instruction	5.2.1, 7.1.1, 7.1.2
D1174	CLI Instruction	5.2.1, 7.1.1, 7.1.2
D1175	MVI Instruction	5.2.1, 7.1.1, 7.1.2
D1176	NI Instruction	5.2.1, 7.1.1, 7.1.2
D1177	OI Instruction	5.2.1, 7.1.1, 7.1.2
D1178	XI Instruction	5.2.1, 7.1.1, 7.1.2

D1179	TS Instruction	5.2.1, 7.1.1, 7.1.2
D117B	STM Instruction	5.2.1, 7.1.1, 7.1.2
D117C	STM, LM Instruction	5.2.1, 7.1.1, 7.1.2
D117E	SVC, LPSW, SPM Instructions	5.2.1, 7.1.1, 7.1.2
D1180	MH Instruction	5.2.1, 7.1.1, 7.1.2
D1181	M Instruction	5.2.1, 7.1.1, 7.1.2
D1182	MR Instruction	5.2.1, 7.1.1, 7.1.2
D1183	D Instruction	5.2.1, 7.1.1, 7.1.2
D1184	DR Instruction	5.2.1, 7.1.1, 7.1.2
D1186	SRDL, SRDA, SLDL, SLDA Instruction	5.2.1, 7.1.1, 7.1.2
D118A	CLC, MVC Instructions	5.2.1, 7.1.1, 7.1.2
D118B	NC Instruction	5.2.1, 7.1.1, 7.1.2
D118C	OC Instruction	5.2.1, 7.1.1, 7.1.2
D118D	XC Instruction	5.2.1, 7.1.1, 7.1.2
D118E	MVO Instruction	5.2.1, 7.1.1, 7.1.2
D118F	MVN Instruction	5.2.1, 7.1.1, 7.1.2
D1190	MVZ Instruction	5.2.1, 7.1.1, 7.1.2
D1191	MVW Instruction	5.2.1, 7.1.1, 7.1.2

D1192	IC, STC, ISK, SSK Instructions	5.2.1, 7.1.1 7.1.2
D1196	CVD, CVB Instructions	5.2.1, 7.1.1 7.1.2
D1197	TR Instruction	5.2.1, 7.1.1 7.1.2
D1198	TRT Instruction	5.2.1, 7.1.1 7.1.2
D1199	PACK, UNPK Instructions	5.2.1, 7.1.1 7.1.2
D119A	PACK, UNPK Instructions	5.2.1, 7.1.1 7.1.2
D119B	Boundary Test of NC, OC, XC, MVN, MVZ, TR, TRT	5.2.1, 7.1.1 7.1.2
D119C	Functional Test of SPSB, LPSB, LI, Program Interrupts	5.2.1, 7.1.1 7.1.2
D119D	Execute and Execute Program Interrupts	5.2.1, 7.1.1 7.1.2
D11A2	LE, STE, LD, STD, CE, CD Instructions	5.2.1, 7.1.1 7.1.2
D11A6	LER, CER, LDR, CDR, LTER Instructions	5.2.1, 7.1.1 7.1.2
D11A9	LTDR, LCER, LCDR Instructions	5.2.1, 7.1.1 7.1.2
D11AC	LPER, LPDR, LNER, LNDR Instructions	5.2.1, 7.1.1 7.1.2
D11B0	AER, ADR, AE, AD Instructions	5.2.1, 7.1.1 7.1.2
D11B4	AVR, AWR, AV, AW Instructions	5.2.1, 7.1.1 7.1.2
D11B8	SER, SDR, SE, SD Instructions	5.2.1, 7.1.1 7.1.2
D11BC	SUR, SWR, SU, SW Instructions	5.2.1, 7.1.1 7.1.2
D11C0	HER, HDR Instructions	5.2.1, 7.1.1 7.1.2

D11C2	MER, MDR, ME, MD Instructions	5.2.1, 7.1.1 7.1.2
D11C6	DER, DDR, DE, DD Instructions	5.2.1, 7.1.1 7.1.2
D11CA	MER, MDR, ME, MD, DER, DDR, DE, DD Instructions	5.2.1, 7.1.1 7.1.2
D11CD	AP Instruction, Part 1	5.2.1, 7.1.1 7.1.2
D11CE	AP Instruction, Part 2	5.2.1, 7.1.1 7.1.2
D11CF	SP Instruction	5.2.1, 7.1.1 7.1.2
D11D0	CP Instruction	5.2.1, 7.1.1 7.1.2
D11D1	ZAP Instruction	5.2.1, 7.1.1 7.1.2
D11D3	MP Instruction, Part 1	5.2.1, 7.1.1 7.1.2
D11D4	MP Instruction, Part 2	5.2.1, 7.1.1 7.1.2
D11D5	DP Instruction, Part 1	5.2.1, 7.1.1 7.1.2
D11D6	DP Instruction, Part 2	5.2.1, 7.1.1 7.1.2
D11D7	ED Instruction	5.2.1, 7.1.1 7.1.2
D11D8	EDMK Instruction	5.2.1, 7.1.1 7.1.2
D11DA	Execute Small Binary Set 1	5.2.1, 7.1.1 7.1.2
D11DB	Execute Small Binary Set 2	5.2.1, 7.1.1 7.1.2
D11DC	Execute Small Binary Set 3	5.2.1, 7.1.1 7.1.2
D11DD	Execute Standard Set 1	5.2.1, 7.1.1 7.1.2

D11DE	Execute Standard Set 2	5.2.1, 7.1.1 7.1.2
D11DF	Execute Floating Point 1	5.2.1, 7.1.1 7.1.2
D11E0	Execute Floating Point 2	5.2.1, 7.1.1 7.1.2
D11E1	Execute Decimal	5.2.1, 7.1.1 7.1.2
D11E4	Program Interrupt, Small Binary Set	5.2.1, 7.1.1 7.1.2
D11E5	Program Interrupt, Standard Set	5.2.1, 7.1.1 7.1.2
D11E6	Program Interrupt, Floating Point	5.2.1, 7.1.1 7.1.2
D11E7	Program Interrupt, Decimal Set	5.2.1, 7.1.1 7.1.2
D11E8	Program Interrupt Suppression Completion	5.2.1, 7.1.1 7.1.2
D11E9	Operation Exception	5.2.1, 7.1.1 7.1.2
D11EB	Execute Program Interrupt, Small Binary Set	5.2.1, 7.1.1 7.1.2
D11EC	Execute Program Interrupt, Standard Set	5.2.1, 7.1.1 7.1.2
D11ED	Execute Program Interrupt, Floating Point	5.2.1, 7.1.1 7.1.2
D11EE	Execute Program Interrupt, Decimal Set	5.2.1, 7.1.1 7.1.2
D13A0	Interval Timer	5.2.1
D13A5	360 Mode Test	5.2.1
D13B0	SPSB, LPSB, LI, SCON, SATR, IATR, DLY, MVW Instructions	5.2.1
D13BA	Diagnose/Log-Out	5.2.1

D13C0	CSS, LC Instructions	5.2.1
D13C1	CVWL Instruction	5.2.1
D13C2	RPSB Instruction	5.2.1
D13C8	Interrupt Test	5.2.1
D13CD	Random	5.2.1
D1401	Interval Timer, IOCE	5.2.12
D1403	DLY Instruction, IOCE	5.2.12
D1DA3	Direct Control	5.2.1
D2101	Local Store, IOCE	5.2.12
D22A0	Main Storage	5.2.4, 5.2.5 5.2.13, 7.2
D22A4	Storage Error Check	5.2.4, 5.2.5
D22AA	Storage Protect	5.2.4, 5.2.5
D24A0	DE/DG Interface Test	5.2.5
D2740	MACH Storage	5.2.12
D3051	Multiplexor Channel Functional Test	5.2.3
D3052	Multiplexor Channel Functional Test	5.2.3
D3053	Multiplexor Channel Functional Test	5.2.3
D3054	Multiplexor Channel Functional Test	5.2.3
D3055	Set Program Controlled Interrupt Functional Test	5.2.3
D3151	Selector Channel Functional Test	5.2.2.1
D3152	Selector Channel Functional Test	5.2.2.1
D3153	Selector Channel Functional Test	5.2.2.1
D3154	Selector Channel Functional Test	5.2.2.1
D3155	Set Program Controlled Interrupt Functional Test	5.2.2.1

D4050	2400/2800 Tape Drive	5.2.2.2, 7.2
D4051	2400/2800 Tape Drive	5.2.2.2
D4052	2400/2800 Tape Drive	5.2.2.2
D4053	2400/2800 Tape Drive	5.2.2.2
D4054	2400/2800 Tape Drive	5.2.2.2
D4055	2400/2800 Tape Drive	5.2.2.2
D4056	2400/2800 Tape Drive	5.2.2.2
D4057	2400/2800 Tape Drive	5.2.2.2
D4060	Tape Inter Block Gap Tests	5.2.2.2
D46A0	Tape Control Unit Dual Interface	5.2.2.3
D6251	2540 Punch Functional Test	5.2.9
D6261	2540 Reader, Part 1	5.2.9
D6262	2540 Reader, Part 2	5.2.9
D6351	Printer Functional, Part 1	5.2.9
D6352	Printer Functional, Part 2	5.2.9
D6353	Printer Functional, Part 3	5.2.9
D6354	Ripple Print Test	5.2.9, 5.2.9.1
D6355	Printer Functional, Part 4	5.2.9
D6356	Sense Channel 9, 12 Test	5.2.9
D6651	Console, Basic Operations and Write Test	5.2.10
D6652	Console, Typewriter Mechanical	5.2.10
D6653	Console, Read Test	5.2.10
D6A51	2821/2540 Channel Register Test	5.2.9
D6A52	2821/2540 Control Program	5.2.9
D6A53	2821/2540 Buffer Address Test	5.2.9
D6A54	2821/1403 Print Buffer Test	5.2.9
D6A55	2821/1403 Universal Character Set Buffer Test	5.2.9

D6A56	2821/1403 Print Buffer Data Register FLT	5.2.9
D6A57	2821/1403 Universal Character Buffer Data Register FLT	5.2.9
D6A58	2821/1403 Universal Character Buffer Restore	5.2.9
D6AA0	2821 Two Tailed Switch	5.2.9.1
D6CA4	System Console, 9020D	5.1.7, 5.2.6
D6CA6	Configuration Console, 9020E	5.1.8, 5.2.7
D8050	CE Disk Pack Initializer	5.2.2.2
D8051	2314 CU Function Test	5.2.2.2
D8052	2314 CU Function Test	5.2.2.2
D8053	2314 CU Function Test	5.2.2.2
D8054	2314 CU Function Test	5.2.2.2
D8055	2314 CU Function Test	5.2.2.2
D8056	2314 CU Function Test	5.2.2.2
D8057	2314 CU Function Test	5.2.2.2
D8058	2314 CU Function Test	5.2.2.2
D8059	2314 CU Function Test	5.2.2.2
D805A	2314 CU Function Test	5.2.2.2
D805B	2314 CU Function Test	5.2.2.2
D805C	2314 CU Function Test	5.2.2.2
D805D	2314 CU Function Test	5.2.2.2
D805E	2314 CU Function Test	5.2.2.2
D805F	2314 CU Function Test	5.2.2.2
D8060	2314 CU Function Test	5.2.2.2
D8061	2314 CU Function Test	5.2.2.2
D8062	2314 CU Function Test	5.2.2.2
D8063	2314 CU Function Test	5.2.2.2
D8064	2314 CU Function Test	5.2.2.2
D8065	2314 File Diagnostic Test	5.2.2.2

D8066	2314 File Diagnostic Test	5.2.2.2
D8067	2314 File Diagnostic Test	5.2.2.2
D8068	2314 File Diagnostic Test	5.2.2.2
D8069	2314 File Diagnostic Test	5.2.2.2
D80A0	2314 Two Channel Switch Test	5.2.2.2
D9051	Reconfiguration Control Unit Test	5.2.7.2
DA051	Channel to Channel	5.2.2.4
DB051	2701 Functional, Part 1	5.2.11
DB052	2701 Functional, Part 2	5.2.11
DB0A1	2701 Functional, Two Channel Switch Test	5.2.11.1
DCC51	Peripheral Adapter Module Unit Test	5.2.8
DCCA0	Peripheral Adapter Module Dual Interface Test	5.2.8.1, 5.2.8.2
DD6A2	DAR/DMR Functions	6.1.2
DD8A0	Configuration Control	6.1.1
DD9A0	Address Translation Register Test	5.2.1
DDDA1	CE Control Program, IOCE Processor Test	5.2.13
DE0A3	SEVA Control	6.1.3, 6.1.4 6.2.1, 7.6,8.0
DF0A1	Safe Store Tests	7.5
DF0B0	Eight Timed Sample Tests	6.3.1
DF0C0	Display Instruction Performance Test	6.3.2

APPENDIX F

TEST CONFIGURATION BLOCK DIAGRAMS

Legend

Equipment Abbreviations

CE - Compute Element (7201-02)

IOCE - Input Output Control Element (7231-02)

SE - Storage Element (7251-09)

DE - Display Element (7289-04)

SC - System Console (7265-02)

CC - Configuration Console (7265-03)

PAM - Peripheral Adapter Module (7289-02)

TCU - Tape Control Unit (2803-1)

TD - Tape Drive (2401-2/3)

DAU - Data Adapter Unit (2701)

CTC - Channel To Channel Adapter

SCU - Storage Control Unit (2314-A1)

DSU - Disk Storage Unit (2312-A1)

Notes

9020D Systems

Eliminate DE and DAU from the configuration

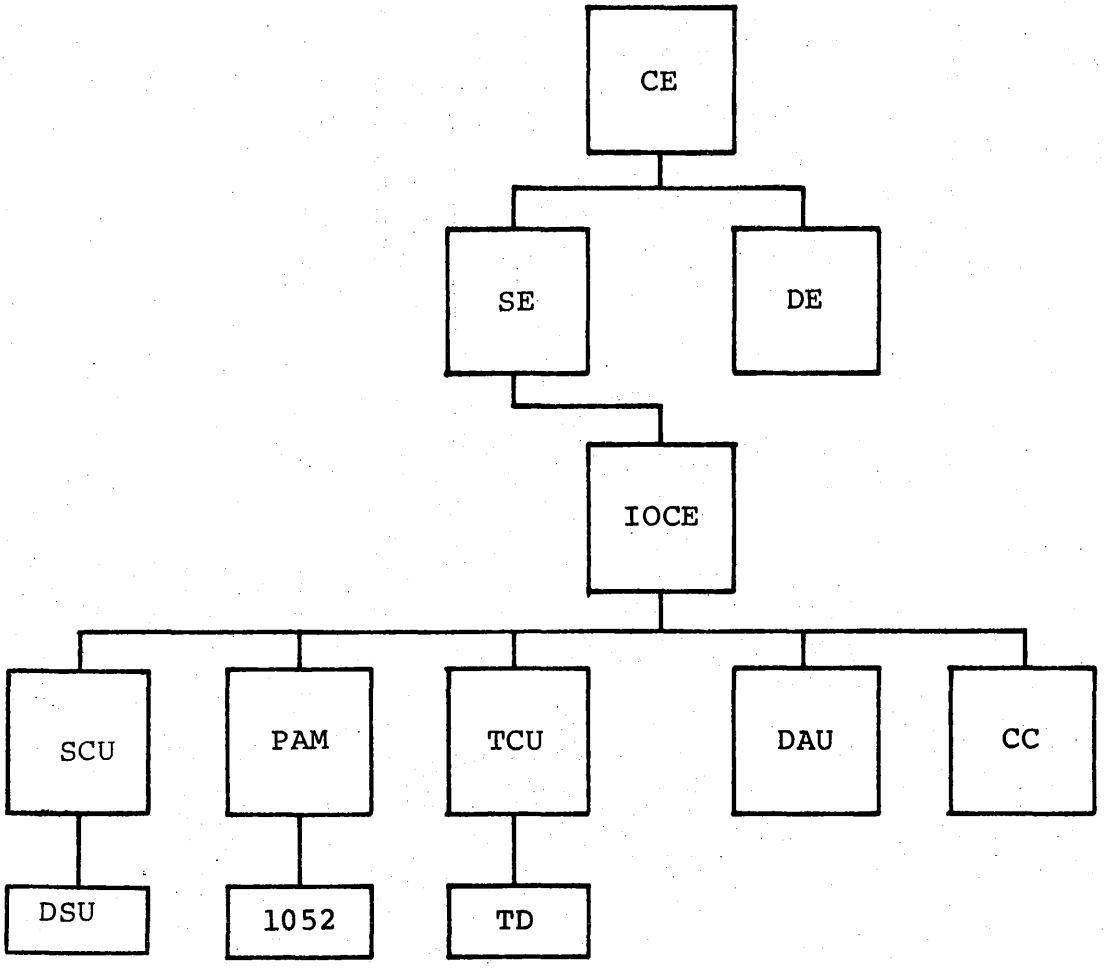
Use SC where SC/CC is shown

9020E Systems

Eliminate PAM and SCU/DSU from the configuration

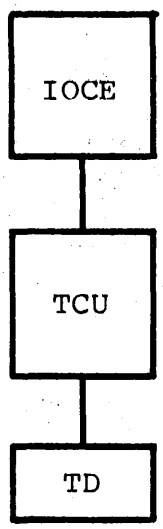
Use CC where SC/CC is shown

DEFINED MINIMUM SYSTEM



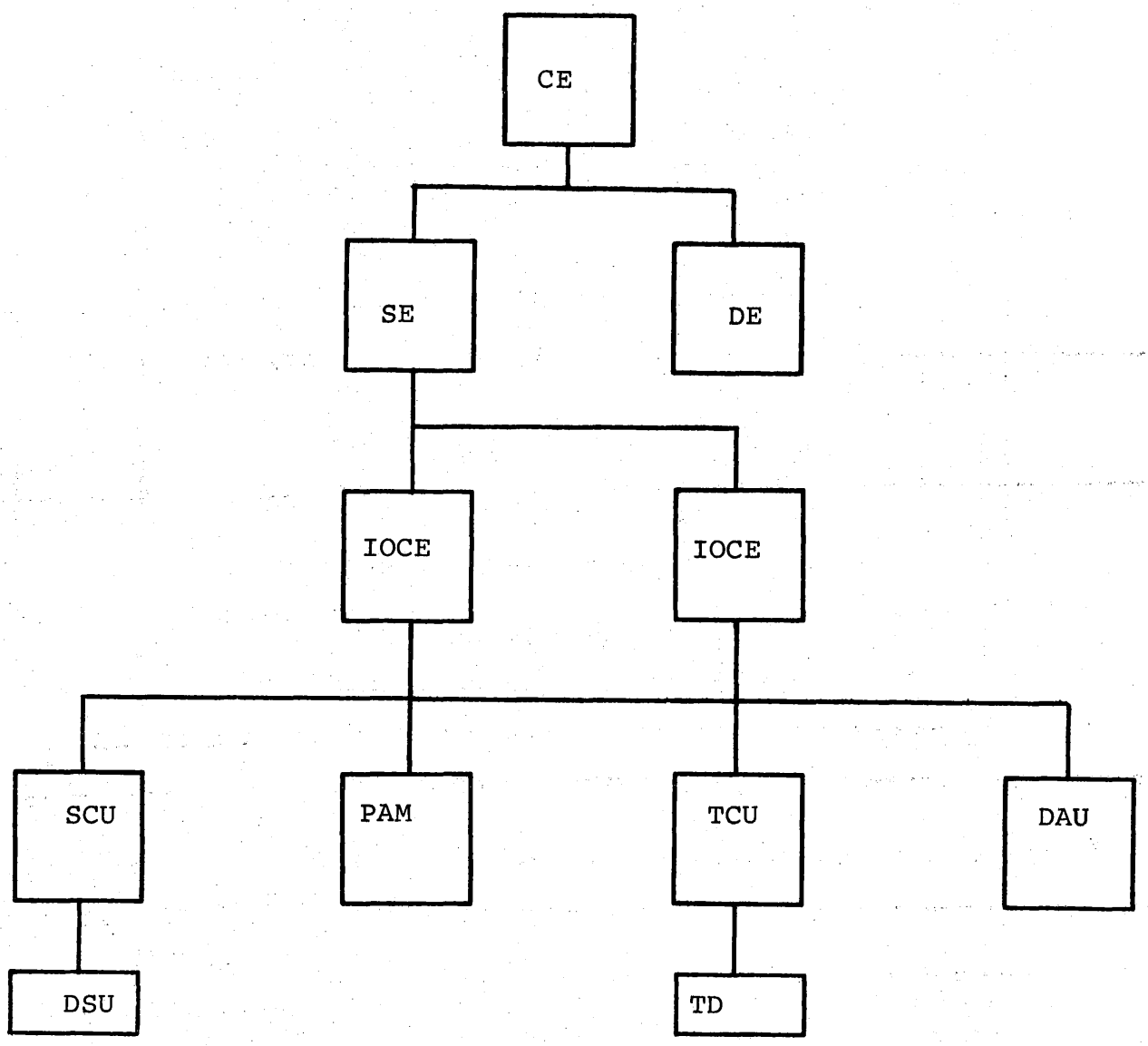
USED IN THE FOLLOWING TESTS:

5.2.1	CE FUNCTIONAL TEST
5.2.2.1	IOCE SELECTOR CHANNEL FUNCTIONAL TEST
5.2.2.2	SCU/DSU FUNCTIONAL TEST
5.2.2.4	TCU/TAPE DRIVES FUNCTIONAL TEST
5.2.2.6	CHANNEL TO CHANNEL ADAPTER FUNCTIONAL TEST
5.2.3	IOCE MULTIPLEXOR CHANNEL FUNCTIONAL TEST
5.2.4	SE FUNCTIONAL TEST
5.2.5	DE FUNCTIONAL TEST
5.2.7.2	RCU FUNCTIONAL TEST
5.2.8	PAM FUNCTIONAL TEST
5.2.10	PRINTER/KEYBOARD FUNCTIONAL TEST
5.2.11	DAU FUNCTIONAL TEST
5.2.13	IOCE PROCESSOR OPERATION
5.2.14	CE,SE,DE AND IOCE LOG-OUT OPERATION
7.1.2	TEST STATE - POWER ON/OFF TEST
7.1.3	MPO SWITCH TEST
7.2	ABNORMAL ELEMENT POWER LOSS AND BATTERY RECHARGE
7.5	SYSTEM MAIN LINE POWER LOSS



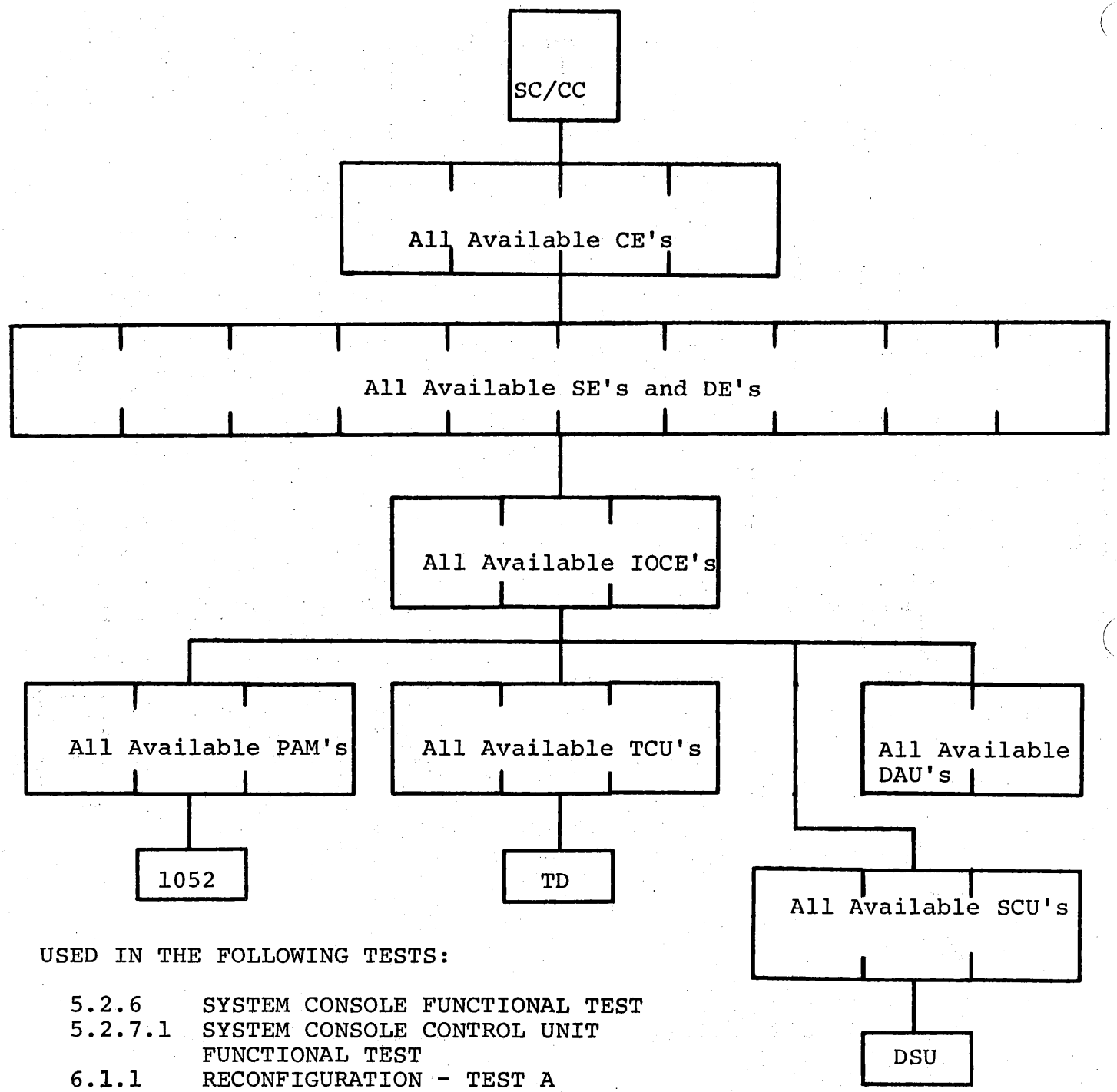
USED IN THE FOLLOWING TESTS:

5.2.2.1.1	IOCE THIRD SELECTOR CHANNEL FUNCTIONAL TEST
5.2.15.1	IOCE FLT FUNCTIONAL TEST
6.3.3	IOCE FLT PRACTICAL TEST



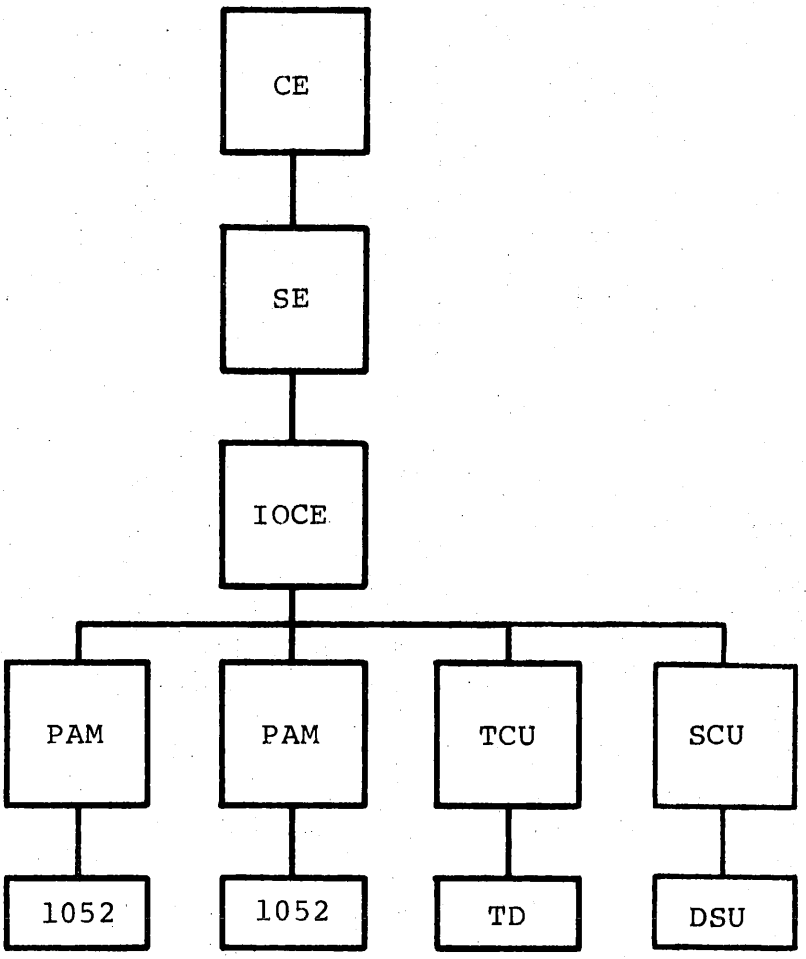
USED IN THE FOLLOWING TEST:

5.2.2.5 TCU DUAL INTERFACE FUNCTIONAL TEST



USED IN THE FOLLOWING TESTS:

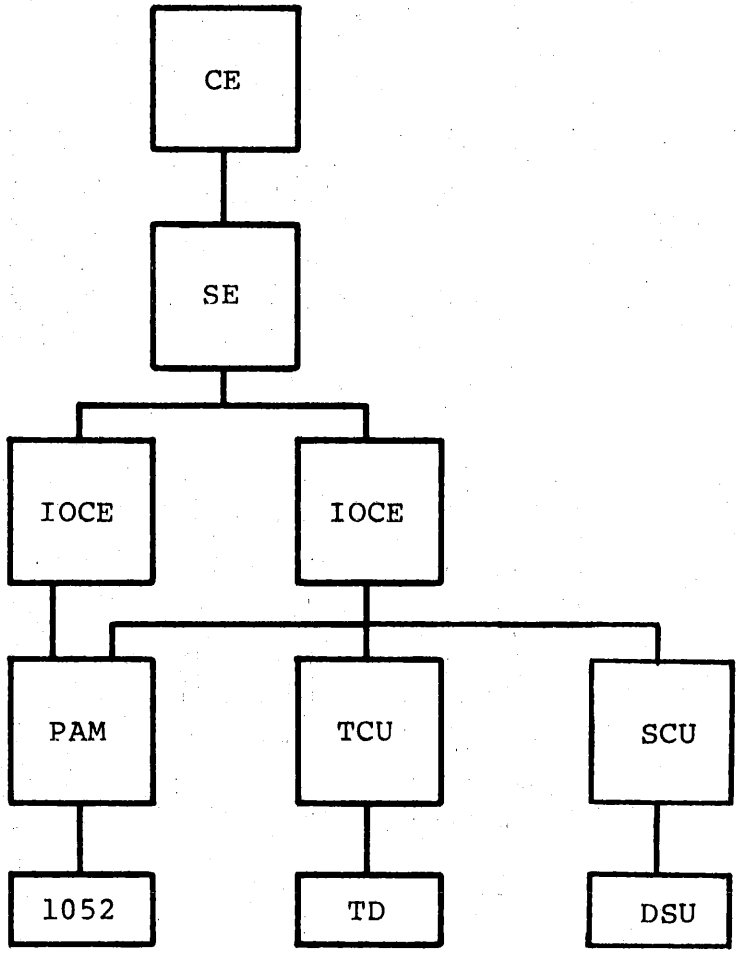
5.2.6	SYSTEM CONSOLE FUNCTIONAL TEST
5.2.7.1	SYSTEM CONSOLE CONTROL UNIT FUNCTIONAL TEST
6.1.1	RECONFIGURATION - TEST A
6.1.2	RECONFIGURATION - TEST B
6.1.3	RECONFIGURATION - TEST C
6.1.4	RECONFIGURATION - TEST D
6.2.1	SYSTEM EVALUATION (SEVA)
6.3.5	360 MODE RECALL TEST
7.1.1	POWER INTERLOCK TEST
7.3	THERMAL WARNING AND PROTECTION
7.4	OVER VOLTAGE/OVER CURRENT AND UNDER VOLTAGE PROTECTION
7.6	SYSTEM EMERGENCY POWER OFF



USED IN THE FOLLOWING TEST:

5.2.8.1 PAM DUAL INTERFACE FUNCTIONAL TEST #1

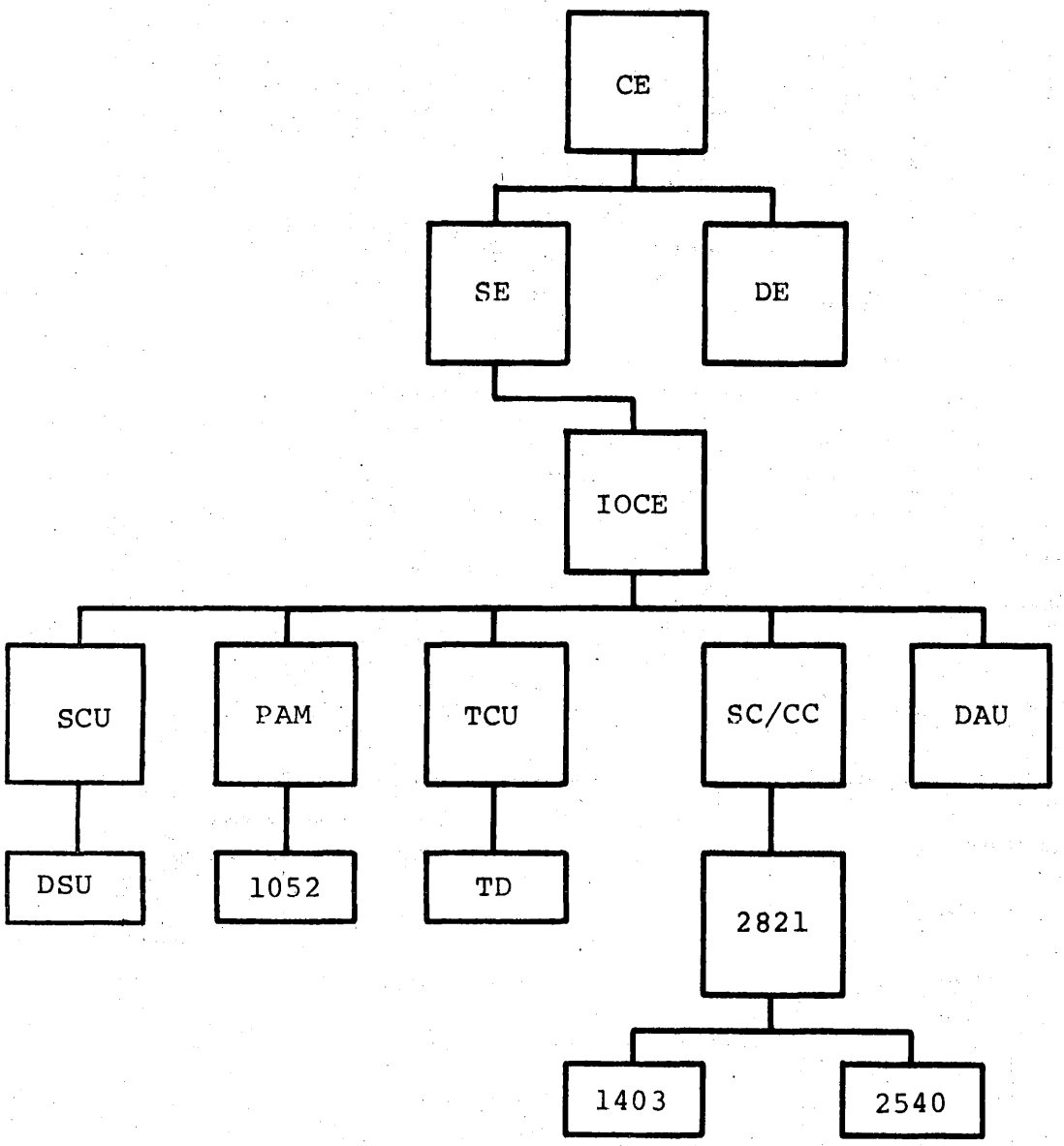
8B3764



USED IN THE FOLLOWING TEST:

5.2.8.2 PAM DUAL INTERFACE FUNCTIONAL TEST #2

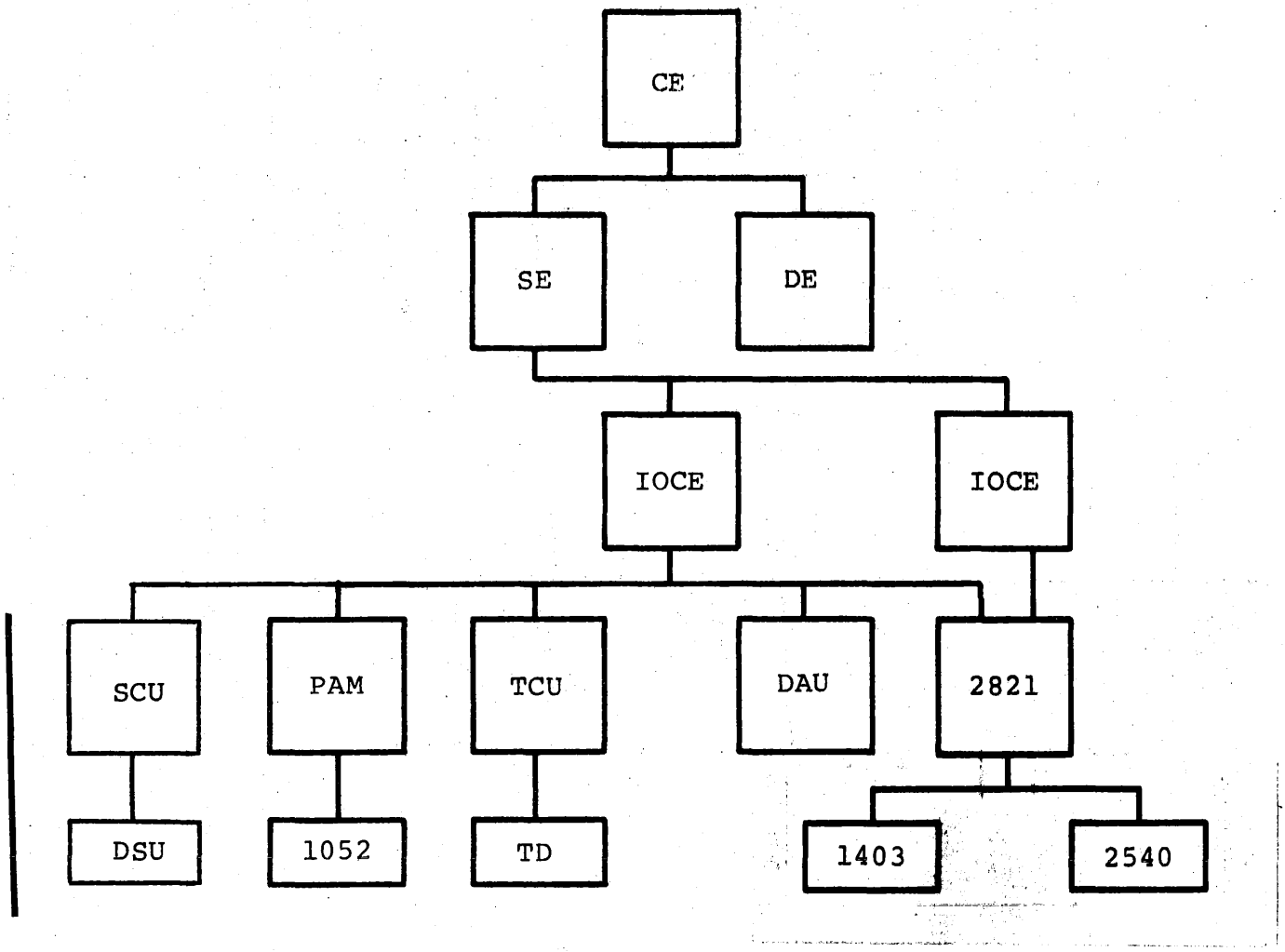
8A2764



USED IN THE FOLLOWING TESTS:

5.2.9	CONTROL UNIT (2821), READ/PUNCH AND PRINTER FUNCTIONAL TESTS
6.3.4	SYSTEM/360 - 9020D/E SYSTEM COMPATIBILITY

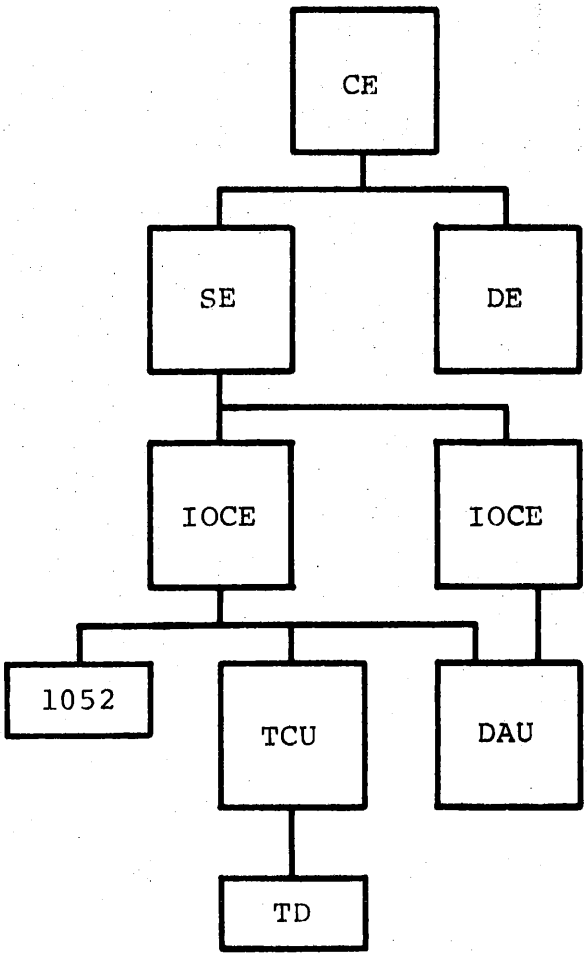
8A6764



USED IN THE FOLLOWING TEST:

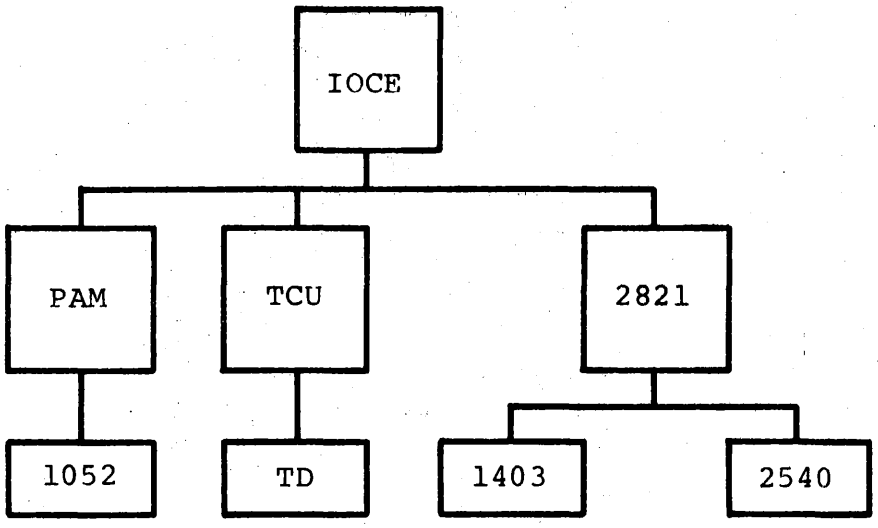
5.2.9.1 2821 TWO CHANNEL SWITCH FUNCTIONAL TEST

8B7764



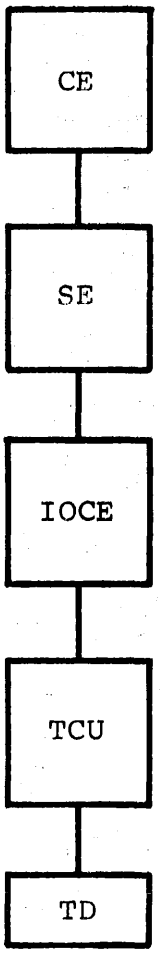
USED IN THE FOLLOWING TEST:

5.2.11.1 DAU TWO PROCESSOR SWITCH FUNCTIONAL TEST



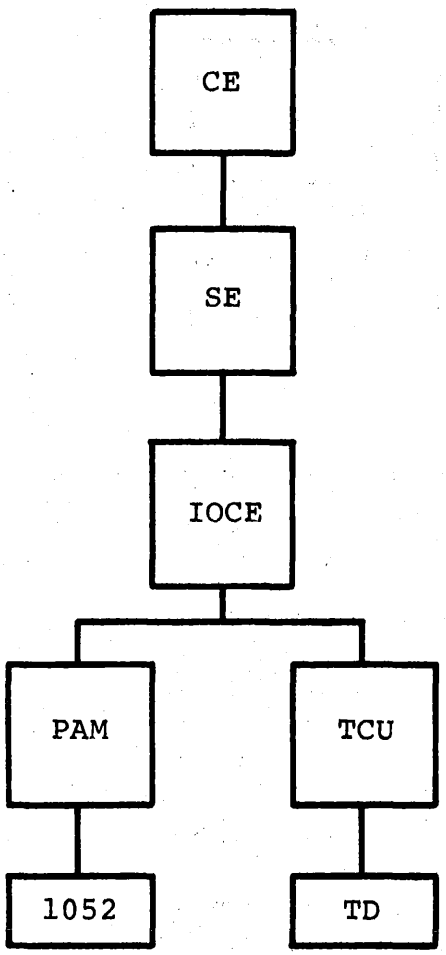
USED IN THE FOLLOWING TEST:

5.2.12 IOCE DIAGNOSTIC MODE FUNCTIONAL DEMONSTRATION



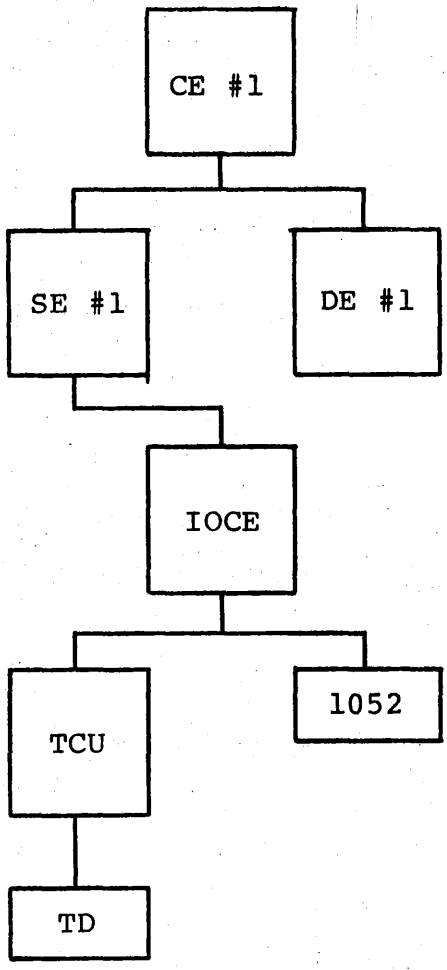
USED IN THE FOLLOWING TESTS:

5.2.15.2	CE FLT FUNCTIONAL TEST
6.3.3	CE FLT PRACTICAL TEST



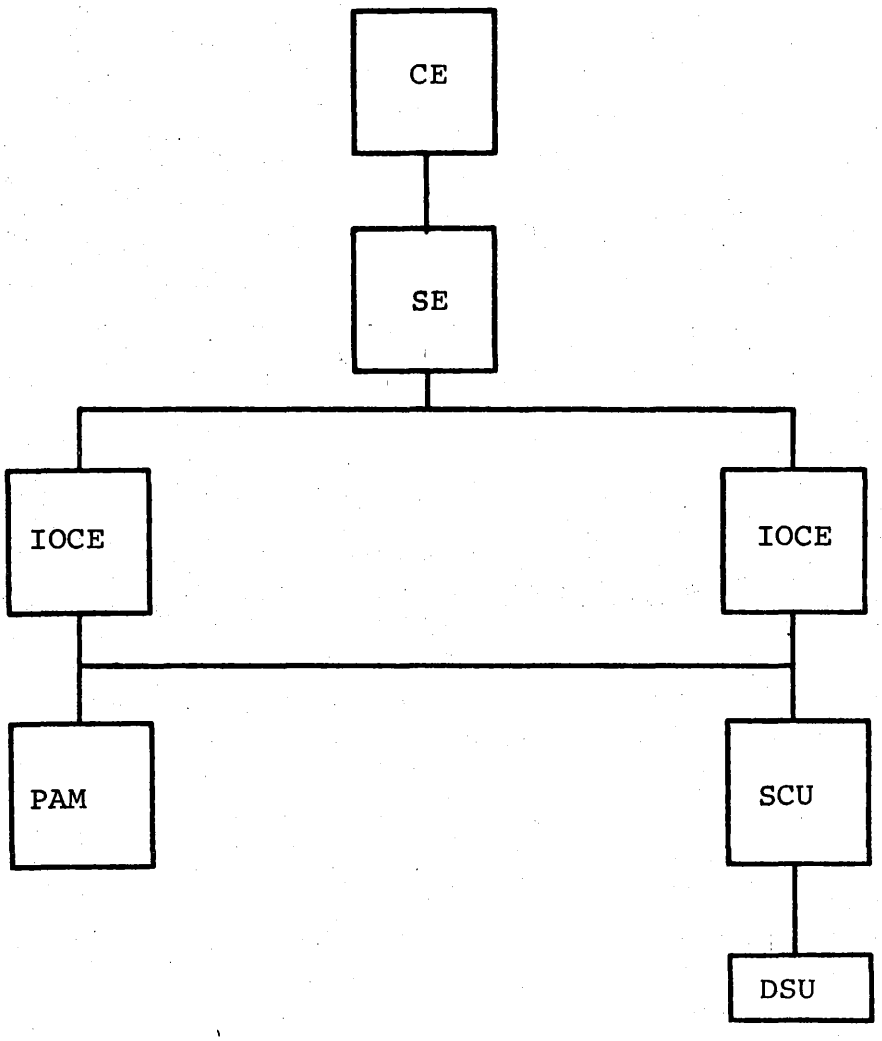
USED IN THE FOLLOWING TEST:

6.3.1 EIGHT TIMED SAMPLE PROBLEMS



USED IN THE FOLLOWING TEST:

6.3.2 DISPLAY INSTRUCTION PERFORMANCE TEST



USED IN THE FOLLOWING TEST:

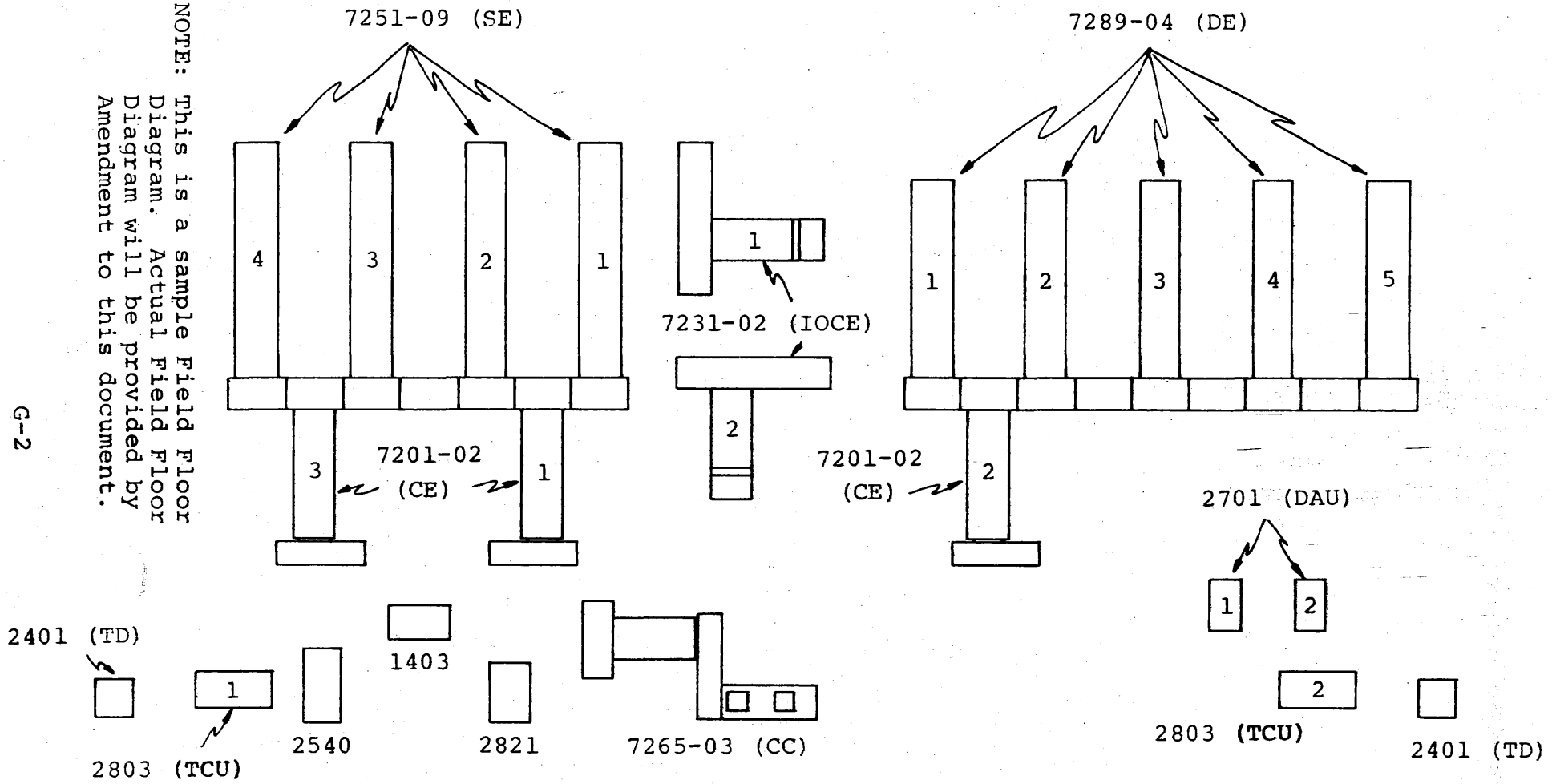
5.2.2.3 SCU TWO CHANNEL SWITCH FUNCTIONAL TEST

8A7764

APPENDIX G

FACTORY FLOOR DIAGRAM

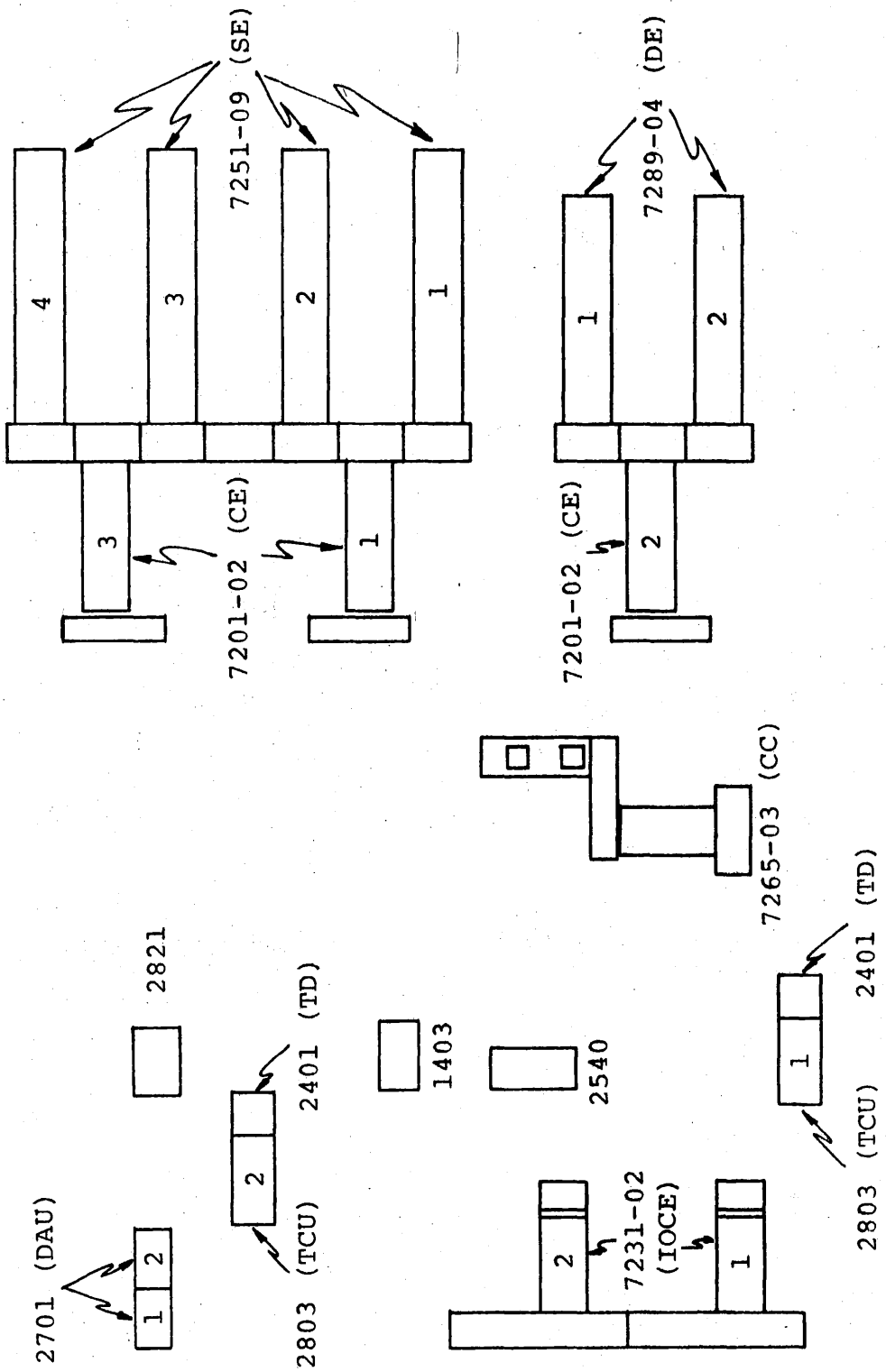
NOTE: This is a sample Field Floor Diagram. Actual Field Floor Diagram will be provided by Amendment to this document.



FACTORY FLOOR DIAGRAM

APPENDIX H

FIELD FLOOR DIAGRAM



FIELD FLOOR DIAGRAM

NOTE: This is a sample Field Floor Diagram. Actual Field Floor Diagram will be provided by Amendment to this document.

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APPENDIX J

EQUIPMENT IDENTIFICATION LIST

AND

FIELD DELIVERABLE ITEM LIST

SPECIAL FEATURES AND RPQ'S

The following features and/or RPQ's are installed on each of the units listed below:

Compute Element — 7201-02

RPQ F27061	1052 Adapter
RPQ FA0416	CCR/DAR Modification for 2314A1 Connection to 9020D
RPQ F30767	Wrap Bus Modification
RPQ FB0140	Convert and Sort Symbols/ Convert Weather Lines

Input/Output Control Element — 7231-02

RPQ F16374	Address Translation
RPQ F27112	Expanded Addressing
RPQ F21241	Processor Mode
RPQ F20974	Storage Element (64K) Interface Mod.
RPQ F26104	Channel to Channel Adapter (Sel. Ch. # 1)
RPQ F28341	Channel to Channel Adapter (Sel. Ch. # 2)
RPQ F27111	Power Mod.
RPQ F16375	SE Bus Mod.
RPQ F16377	Selector Channel

System Console — 7265-02

RPQ F16378	Single Enter-Cancel Keys
RPQ F16379	Patch Panel and Adapter Unit
RPQ F20421	SMMC Interface Mod.
RPQ F16373	Fourth CE Modification
RPQ FA0417	Configuration and State Display Modification for 2314A1 Connection to 9020D

Configuration Console — 7265-03

RPQ F28753	90 Console Expansion
RPQ F28887	3rd IOCE and 3rd TCU
RPQ F30768	Clock Pulse Modification

Peripheral Adapter Module — 7289-02

RPQ F26474	Power Mod.
RPQ F19673	Priority Two-Level Shared
RPQ FA1771	Power Mod. - 1052

Tape Control Unit		2803-A01
RPQ F12928	Switching to IOCE's	
Direct Access Storage Facility		2314-A01
RPQ FA0418	Configuration Control Modification to 2314A1 for connection to 9020A and 9020D	
Feature 8170	Two Channel Switch	
Integrated Control Unit		2821-01
Feature 8637	Universal Character Set Adapter	
Feature 9241	1403-02 Attachment	
Integrated Control Unit		2821-02
Feature 8637	Universal Character Set Adapter	
Feature 8100	Two Channel Switch	
Feature 9241	1403-02 Attachment	
Printer/Keyboard		1052-07
Feature 9572	Extended BCD Code Print Element	
Feature 9104	10 Characters/Inch Horizontal Spacing	
Feature 9509	Pin Feed Platen	
Feature 9162	Line Spacing 6 LPI, 13-1/8" Hole-to-Hole Width	
RPQ F13197	Cable and Power On Indicator	
RPQ F14713	Single Enter and Cancel Keys	
Printer		1403-02
Feature 8641	Universal Character Set	
Feature 4740	Interchangeable Chain Cartridge Adapter	
Feature 9631	PN-2 Print Arrangement	
Data Adapter Unit		2701-01
Feature 5500	Parallel Data Adapter	
RPQ F26329	PDA Multi-Device Attach.	
RPQ F26105	TPS Interface	
RPQ 858009	Two Channel Switch	

IBM EQUIPMENT IDENTIFICATION LIST

Location _____ Date _____

EQUIPMENT NAME	MODEL NO.	POSITION/ ADDRESS	SERIAL
Compute Element	7201-02	1 2 3 4	
Input/Output Control Element	7231-02	1 2 3	
Storage Element	7251-09	1 2 3 4 5 6 7 8 9 10	
Display Element	7289-04	1 2 3 4 5	
Peripheral Adapter Module Adapters- _____GPI _____GPO _____TTY _____INT. IN _____INT. OUT _____CD _____1052 _____FDEP	7289-02	1	

CONTRACT #FA64WA-5223			
AMENDMENT	ITEM	AMENDMENT	ITEM

Approval _____ Date _____

SPECIAL FEATURES AND RPQ'S (cont'd)

RPQ F30766	Address Bus Out Modify
RPQ FB0796	Receiver Modification
RPQ FB0512	Functional Modification

NOTE: This is a sample Special Features and RPQ List. Actual Special Features and RPQ list will be provided at the time of the Acceptance Test.

Approval: _____

Date: _____

Revision 7
9/17/73

IBM EQUIPMENT IDENTIFICATION LIST

Location _____ Date _____

EQUIPMENT NAME	MODEL NO.	POSITION/ ADDRESS	SERIAL NO.
Peripheral Adapter Module Adapters- _____GPI _____GPO _____TTY _____INT. IN _____INT. OUT _____CD _____1052 _____FDEP	7289-02	2	
Peripheral Adapter Module Adapters- _____GPI _____GPO _____TTY _____INT. IN _____INT. OUT _____CD _____1052 _____FDEP	7289-02	3	
System Console	7265-02	-	
Configuration Console	7265-03	-	
Storage Control Unit	2314-A1	1 2 3	
Tape Control Unit	2803-1	1 2 3	
Data Adapter Unit	2701	1 2	
Control Unit	2821-1	1	
Card Read/Punch	2540-1	03	

CONTRACT #FA64WA-5223			
AMENDMENT	ITEM	AMENDMENT	ITEM

Approval _____ Date _____ R - 5
J-5 6/23/71

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IBM EQUIPMENT IDENTIFICATION LIST

Location _____ Date _____

EQUIPMENT NAME	MODEL NO.	POSITION/ ADDRESS	SERIAL NO.
Printer	1403-2	05	
Printer/Keyboard	1052-7	02	
		3C	
Disk Storage Unit	2312-A1	1 1	
		2 1	
		3 1	
Disk Pack	2316-01		
Tape Unit	2401-	1 0	
	2401-	1 1	
	2401-	1 2	
	2401-	1 3	
	2401-	1 4	
	2401-	1 5	
	2401-	1 6	
	2401-	1 7	
	2401-	2 0	
	2401-	2 1	
	2401-	2 2	
	2401-	2 3	
	2401-	2 4	
	2401-	2 5	
	2401-	2 6	
	2401-	2 7	
	2401-	3 0	
	2401-	3 1	
	2401-	3 2	
	2401-	3 3	
	2401-	3 4	
	2401-	3 5	
	2401-	3 6	
	2401-	3 7	

NOTE: This is a sample equipment list. Actual equipment list will be provided at the time of the Acceptance Test.

CONTRACT #FA64WA-5223			
AMENDMENT	ITEM	AMENDMENT	ITEM

Approval _____ Date _____

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IBM 9020D/E DATA PROCESSING SYSTEM

DELIVERABLE ITEM LIST (TO FAA AT FIELD SITE)

_____ARTCC

	MAINTENANCE DIAGNOSTIC PROGRAMS	CERTIFICATION
1	Set Internal Specifications (Writeups, Flowcharts)	_____
1	Set Program Listing	_____
1	Reel Program Library Tape	_____
1	Set Program Object Deck	_____
5	Reels FLT Tapes	_____
2	Sets SCOPEX	_____

	ACCEPTANCE TEST PROGRAMS	
1	Set Internal Specifications (Writeups, Flowcharts)	_____
1	Set Program Listings	_____
1	Reel Program Library Tape	_____
__	Reels FLT Tapes (3 for 9020E - 2 for 9020D)	_____

	INSTRUCTION BOOKS (FE MANUALS)	
1	Set Instruction Manuals	_____
1	Set Automated Logic Diagrams Manuals	_____
1	Set Illustrated Parts Catalogs	_____

MAGNETIC TAPE - CUSTOMER REEL _____REELS _____

(One reel supplied with each new tape drive.)

Approval: _____

Date: _____

INTERNAL SPECIFICATIONS

1. Maintenance Diagnostic Programs

   a. Vol. I — Monitor Manual and Flowcharts
   b. Vol. II-V — Element, Unit, and System Programs

PROGRAM LISTINGS

1. Maintenance Diagnostic Programs

   a. Vol. VI-XXX — Program Listings

FAULT LOCATING TESTS

1. Fault Locating Tests (7231-02) Manual
2. 7231-02 FLT DUP Program Writeup, Card Deck and Listing
3. Fault Locating Tests Scopex

   a. IBM 7201-02 Vol. 1-11
   b. IBM 7231-02 Vol. 1-13

IBM 9020D/E DATA PROCESSING SYSTEM

ACCEPTANCE TEST DOCUMENTATION

ACCEPTANCE TEST CHECKLIST AND SPECIFICATION

a. Acceptance Test Checklist

b. Acceptance Test Specification

c. Amendment to Checklist and Specification (to adapt the basic checklist and specification to the specific system configuration).

INTERNAL SPECIFICATIONS

a. Maintenance Diagnostic Programs

Vol. I	Monitor Manual and Flowcharts
Vol. II-V	Element, Unit and System Programs

PROGRAM LISTINGS

a. Maintenance Diagnostic Programs

Vol. VI-XXX	Program Listings

IBM 9020D/E DATA PROCESSING SYSTEM

INSTRUCTION MANUALS

QUANTITIES:

1 PER ELEMENT/UNIT

THEORY OF OPERATION MANUALS

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SFN-0201-1	COMPUTING ELEMENT	X	X
GN31-0001	TECHNICAL NEWS LETTER TO SFN-0201-1	X	X
SN31-0020	TECHNICAL NEWS LETTER TO SFN-0201-1	X	X
SY22-2821-0	SYSTEM/360 MODEL 50, INTRODUCTION	X	X
SY22-2822-1	SYSTEM/360 MODEL 50, FUNCTIONAL UNITS	X	X
SY22-2823-0	SYSTEM/360 MODEL 50, READ ONLY STORAGE	X	X
SY22-2824-1	SYSTEM/360 MODEL 50, RR & RX INSTRUCTIONS	X	X
SY22-2825-1	SYSTEM/360 MODEL 50, RS, SI, SS INST.	X	X
SY22-2826-1	SYSTEM/360 MODEL 50, SELECTOR/COM. CHAN.	X	X
SY22-2827-0	SYSTEM/360 MODEL 50, MULTIPLEXOR	X	X
SY22-2828-0	SYSTEM/360 MODEL 50 STORAGE	X	X
SY22-6870	TECHNICAL NEWS LETTER TO SY22-2822	X	X
ZY22-6806-1	CHANNEL TO CHANNEL ADAPTER	X	X
ZZ22-2865-4	I/O CONTROL ELEMENT	X	X
ZY22-2866-1	I/O CONTROL ELEMENT, CONTROL PANEL	X	X
SFN-0301-2	STORAGE ELEMENT	X	X
SFN-0401-1	DISPLAY ELEMENT		X
SN31-0029	TECHNICAL NEWS LETTER TO SFN-0401-1		X
226-2040-3	SYSTEM CONSOLE	X	

IBM 9020D/E DATA PROCESSING SYSTEM

INSTRUCTION MANUALS

THEORY OF OPERATION MANUALS (cont'd)

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
GN31-0004	TECHNICAL NEWS LETTER TO 226-2040-3	X	
SFN-0501-1	CONFIGURATION CONSOLE		X
226-2026-3	PERIPHERAL ADAPTER MODULE	X	
SY27-2351-0	PERIPHERAL ADAPTER MODULE EXPANSION FRAME	X	
SY27-2350-0	PERIPHERAL ADAPTER MODULE TWO-LEVEL SHARED PRIORITY	X	
SY32-5001-2	TAPE CONTROL UNIT	X	X
Y22-6781-0	TAPE CONTROL UNIT	X	X
SY24-3359-4	INTEGRATED CONTROL UNIT	X	X
SY25-3479-0	INTEGRATED CONTROL UNIT, 2 CHAN. SW.	X	X
S225-3179-5	PRINTER/KEYBOARD	X	X
S23-4037	TECHNICAL NEWS LETTER TO S225-3179-5	X	X
S23-4037	SUPPLEMENT FOR #S225-3179	X	X
S225-3353-1	SELECTRIC I/O KEYBOARDLESS PRINTER	X	X
S26-3671-5	DIRECT ACCESS STORAGE FACILITY	X	
SY26-0735-0	2314 CONFIGURATION FEATURE FOR 9020 SYSTEM	X	

THEORY OF OPERATION MANUALS (cont'd)

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SY22-2819-0	TAPE DRIVE	X	X
SY31-0081-3	READER/PUNCH	X	X
Y31-0242	SUPPLEMENT FOR # SY31-0081-3	X	X
S225-6492-6	PRINTER	X	X
SFN-0901-1	DATA ADAPTER UNIT (MAINT. MANUAL INCLUDED)		X

MAINTENANCE MANUALS

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SFN-0203-2	COMPUTING ELEMENT	X	X
ZZ22-6823-0	I/O CONTROL ELEMENT	X	X
ZZ22-6886	TECHNICAL NEWS LETTER TO ZZ22-6823-0	X	X
ZZ22-6911	TECHNICAL NEWS LETTER TO ZZ22-6823-0	X	X
SY22-2832-4	SYSTEM/360 MODEL 50, 2050 PROCESSING UNIT	X	X
SFN-0303-2	STORAGE ELEMENT	X	X
SFN-0403-1	DISPLAY ELEMENT		X
226-2041-3	SYSTEM CONSOLE	X	
GN31-0005	TECHNICAL NEWS LETTER TO 226-2041-3	X	
SFN-0503-1	CONFIGURATION CONSOLE		X
226-2027-3	PERIPHERAL ADAPTER MODULE	X	
SY32-6002-2	TAPE CONTROL UNIT	X	X
SY32-5014	SUPPLEMENT FOR #Y32-6002-2	X	X
SY32-5025	SUPPLEMENT FOR #Y32-6002-2	X	X
SY24-3383-3	INTEGRATED CONTROL UNIT	X	X
S225-3207-6	PRINTER/KEYBOARD	X	X
SY22-6631-2	TAPE DRIVE	X	X

MAINTENANCE MANUALS (cont'd)

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SY31-0082-6	READER/PUNCH	X	X
S225-6493-8	PRINTER	X	X
SY26-3672-10	DIRECT ACCESS STORAGE FACILITY	X	
SY26-0736-0	2314 CONFIGURATION FEATURE FOR 9020 SYSTEM	X	

DIAGRAMS MANUALS

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SFN-0202-1	COMPUTING ELEMENT	X	X
GN31-0002	TECHNICAL NEWS LETTER TO SFN-0202-1	X	X
SN31-0021	TECHNICAL NEWS LETTER TO SFN-0202-1	X	X
SY22-2833-0	I/O CONTROL ELEMENT	X	X
Z22-2867-2	SUPPLEMENT FOR #SY22-2833-0	X	X
ZY22-6807-1	CHANNEL-TO-CHANNEL ADAPTER	X	X
SFN-0302-2	STORAGE ELEMENT	X	X
SN31-0028	SUPPLEMENT FOR #SFN-0302-2	X	X
SFN-0402-1	DISPLAY ELEMENT		X
SN31-0030	SUPPLEMENT FOR #SFN-0402-1		X
226-2042-3	SYSTEM CONSOLE	X	
GN31-0006	TECHNICAL NEWS LETTER TO 226-2042-3	X	
SFN-0502-1	CONFIGURATION CONSOLE		X
226-2028-2	PERIPHERAL ADAPTER MODULE	X	
SN31-0019	TECHNICAL NEWS LETTER TO 226-2028-2	X	
SY32-7001-1	TAPE CONTROL UNIT/TAPE DRIVE	X	X
SY24-3503-1	INTEGRATED CONTROL UNIT	X	X

DIAGRAMS MANUALS (cont'd)

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SY24-3508-1	INTEGRATED CONTROL UNIT	X	X
SY31-0168-1	READER/PUNCH	X	X
SFN-0902-1	DATA ADAPTER UNIT		X
SY26-4001-4	DIRECT ACCESS STORAGE FACILITY	X	
SN26-0740	SUPPLEMENT FOR #SY26-4001-4	X	
SY26-0737-0	2314 CONFIGURATION FEATURE FOR 9020 SYSTEM	X	

MISCELLANEOUS

QUANTITY - 3 PER SYSTEM

FORM NO.	TITLE	SYSTEM 9020D	SYSTEM 9020E
Y22-2800-3	SLT PACKAGING	X	X
SY22-2798-2	SLT COMPONENTS	X	X
SY22-2799-2	SLT POWER SUPPLIES	X	X
SFN-0105-2	POWER CONTROL AND DISTRIBUTION	X	X
SFN-0103-2	9020E SYSTEM INTRODUCTION		X
SFN-0104-2	9020D SYSTEM INTRODUCTION	X	
A27-2736-1	9020D/E OPERATORS MANUAL	X	X

IBM 9020D/E DATA PROCESSING SYSTEM
AUTOMATED LOGIC DIAGRAMS (ALD) MANUALS
AND WIRING DIAGRAMS

QUANTITIES:

1 PER ELEMENT/UNIT

ELEMENT/UNIT	# VOLUMES	SYSTEM 9020D	9020E
COMPUTING ELEMENT	31	X	X
COMPUTING ELEMENT, 1052 ADAPTER	1		X
INPUT/OUTPUT CONTROL ELEMENT	22	X	X
STORAGE ELEMENT	11	X	X
DISPLAY ELEMENT	18		X
SYSTEM CONSOLE	4	X	
CONFIGURATION CONSOLE	5		X
PERIPHERAL ADAPTER MODULE	6	X	
TAPE CONTROL UNIT	3	X	X
TAPE DRIVE	1	X	X
READER/PUNCH	2	X	X
HIGH SPEED PRINTER	1	X	X
DATA ADAPTER UNIT	2		X
INTEGRATED CONTROL UNIT	8	X	X
DIRECT ACCESS STORAGE FACILITY	9	X	

QUANTITY - 1 PER ELEMENT/UNIT

FORM NO.	ELEMENT/UNIT	SYSTEM 9020D	SYSTEM 9020E
SFN-0205-1	COMPUTING ELEMENT	X	X
S123-0428-4	I/O CONTROL ELEMENT	X	X
SFN-0305-1	STORAGE ELEMENT	X	X
SFN-0405-0	DISPLAY ELEMENT		X
SN31-0016	TECHNICAL NEWS LETTER TO SFN-0405-0		X
SN31-0011	TECHNICAL NEWS LETTER TO SFN-0405-0		X
123-0446-2	SYSTEM CONSOLE	X	
GN31-0009	TECHNICAL NEWS LETTER TO 123-0446-2	X	
SFN-0505-1	CONFIGURATION CONSOLE		X
123-0445-2	PERIPHERAL ADAPTER MODULE	X	
S123-1004-3	TAPE CONTROL UNIT	X	X
S124-0084-4	INTEGRATED CONTROL UNIT	X	X
S124-0070-6	PRINTER/KEYBOARD	X	X
S123-0461-4	DIRECT ACCESS STORAGE FACILITY	X	
S127-0916-0	DISK STORAGE UNIT	X	
SY26-0738-0	2314 CONFIGURATION FEATURE FOR 9020 SYSTEM	X	
S123-0412-4	TAPE DRIVE	X	X
S121-054506	READER/PUNCH	X	X
S124-0026-9	HIGH SPEED PRINTER	X	X
123-0423-3	DATA ADAPTER UNIT		X

APPENDIX K

TEST EQUIPMENT LIST

TEST EQUIPMENT LIST

EQUIPMENT NAME	TEST SECTION REF.
1. 453 Tektronic Oscilloscope or equivalent	5.0
2. I/O Tester - P/N 452400	5.0
3. Heating Device (i.e., Hair Dryer)	7.0
4. Stop Watch	7.0
5. Clip Lead Jumper	7.0
6. Multimeter	8.0
7. 510 Ohm Resistor	5.0
8. 750 Ohm Resistor	5.0
9. Terminator P/N 5805585	5.0

APPENDIX L

TEST RECORDING FORMS

Unit Functional Test Data Record

A. Element or Unit identification of the equipment being tested; i.e., CE #1, SE #6, TCU #3, etc.

B. A preassigned number used for record keeping purposes; i.e., U-001 - UXX

C. Location of testing; i.e,, Factory or Field location

D. Matrix used to indicate the exact configuration for re-run purposes.

E. Program Name and Section Identification; i.e., Storage Element Program - D20A1

F. Success or Failure

G. Signature of FAA observer witnessing test

H. In the event this test fails, enter the Malfunction Number assigned on the System Acceptance Test Log.

I. Yes or No

J. The Test Data Record Number (Item B) of any other forms associates, or any other pertinent comments.

K. Signature of FAA observer or authorized IBM official.

L. Test Specification Reference; copy from original form in event of reruns.

IBM 9020D/E SYSTEM

UNIT FUNCTIONAL TEST DATA RECORD

TEST NO.	ELEMENT/UNIT
1	A
2	
3	
4	

TEST DATA RECORD NO. U- B

LOCATION C

DATE

TEST SPEC. REF. L

TEST CONFIGURATION

	CE				IOCE			SE					SE/DE					DAU		PAM			SCU			TCU			SCCC	RCU	
	1	2	3	4	1	2	3	1	2	3	4	5	6/1	7/2	8/3	9/4	10/5	1	2	1	2	3	1	2	3	1	2	3	1	1	2
1																															
2																															
3																															
4																															

PROGRAM AND SECTION ID	TEST RESULT	CERTIFICATION
E	F	G

TEST NO.	MALFUNCTION NO.	RERUN REQ'D	TEST NO.	MALFUNCTION NO.	RERUN REQ'D.
1	H	I	3		
2			4		

COMMENTS

J

APPROVAL K

DATE

9C6764

System Functional Test Data Record

A. The specific system test in process (Power Test A, Reconfiguration Test D etc.)

B. A preassigned number used for recording purposes; S001 - SXXX

C. Factory or Field location

D. Matrix used to indicate the configuration at the start of the test

E. Matrix used to indicate the configuration at the time of a Failure

F. The sub-section of the system test in process

G. Matrix used to record tests performed, test, results and signature of FAA observer.

H. The Malfunction Number assigned on the System Acceptance Test Log

I. Yes or No

J. The Test Data Record Number (Item B) of any other forms associated, or any other pertinent comments

K. Signature of FAA observer or authorized IBM official.

L. Test Specification Reference; copy from original form in event of reruns.

IBM 9020D/E SYSTEM

SYSTEM FUNCTIONAL TEST DATA RECORD

TEST NAME A

TEST ITEMS

A F

B

C

TEST DATA RECORD NO. B

LOCATION C

DATE

TEST SPEC. REF. L

INITIAL TEST CONFIGURATION D

CE				IOCE			SE					SE/DE					DAU		PAM			SCU			TCU			SC CC	RCU	
1	2	3	4	1	2	3	1	2	3	4	5	6/1	7'/2	8/3	9/4	10/5	1	2	1	2	3	1	2	3	1	2	**3**	1	1	2

EQUIPMENT TEST CHECKOFF AND RESULT MATRIX G

	CE				IOCE			SE					SE/DE					DAU		PAM			SCU			TCU			SC CC	RCU	
	1	2	3	4	1	2	3	1	2	3	4	5	6/1	7'/2	8/3	9/4	10/5	1	2	1	2	3	1	2	3	1	2	**3**	1	1	2
TEST ITEM																															

S-SUCCESS

F-FAILURE

TEST CERTIFICATION CAA

FAILING TEST CONFIGURATION E

CE				IOCE			SE					SE/DE					DAU		PAM			SCU			TCU			SC CC	RCU	
1	2	3	4	1	2	3	1	2	3	4	5	6/1	7'/2	8/3	9/4	10/5	1	2	1	2	3	1	2	3	1	2	**3**	1	1	2

MALFUNCTION NO. H RERUN REQUIRED I

COMMENTS:

J

APPROVAL K

DATE

Revision 5
6/23/71

206764

System Acceptance Test Log

A. A code entered that indicates the system usage. This item will show the basic phase of testing currently being performed; i.e., UT - Unit Test, FM - Factory Exercise with Margins, ST -Reconfiguration or SEVA tests, etc.

B. A code indicating test results

C. Enter element or unit identification of the equipment that encounters a failure

D. Enter the serial number of the entry in item C.

E. Assign a number to all errors, i.e., T01, M02 where T indicates transient failures and M indicates malfunctions

F. Enter the Test Data Record number of all applicable forms.

G. Signature of IBM operator making the line entry

H. Record pertinent data for all malfunctions.

I. Signature of FAA observer or authorized IBM official.

_____ ACCEPTANCE TEST LOG

DATE			TIME		USAGE	OPER	FAILURE DATA				COMMENTS	OPERATOR
DA	MO	YR	START	STOP	CODE	CODE	UNIT OR ELEMENT	SERIAL NO.	TYPE NO.	TEST RECORD NO.		
					A	B	C	D	E	F	H	G

L-7

FAILURE TYPE: T - TRANSIENT M - MALFUNCTION

MALFUNCTION RECORD						
DA	MO	YR	NO	OPENED BY	CLOSED BY	DATE

USAGE CODES	
UT	UNIT TEST
ST	SYSTEM TEST
FE	FACTORY EXERCISE
ID	IDLE IN ORDER
SU	SETUP TIME Saw
SM	SCHED. MAINT.
UM	UNSCHED. MAINT.
~~FM~~	~~FACT. EXER. MARG.~~

OPERATION CODES	
S	SUCCESSFUL
DF	DETECTED FAILURE
PF	PROGRAM FAILURE
MF	MATERIAL FAILURE
XF	EXTERNAL FAILURE
OE	OPERATOR ERROR

APPROVAL I

DATE _____

9667-77

Test Data Record Comment Sheet

A. Comments: This form will be used in conjunction with any of the Test Data Records to provide the space necessary for any additional comments; such as, pertinent failure indications, corrective action taken on any malfunction and multiple transient failure investigation information.

B. Enter the applicable Test Data Record Number; i.e., U-001 S-005, etc.

C. Enter the malfunction or transient number; i.e., M-01 or T-01.

D. Enter the failing element or unit.

TEST DATA RECORD COMMENTS

TEST DATA RECORD NO. B DATE

TIME START	TIME STOP	UNIT OR ELEMENT	TYPE NO.	COMMENTS
		D	C	A

9A8764

UNIT TESTS

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-001	CE	SWITCH DEMONSTRATION	5.1.1
U-002	IOCE	SWITCH DEMONSTRATION	5.1.2
U-003	SE 1-4	SWITCH DEMONSTRATION	5.1.3
U-004	SE 5-8	SWITCH DEMONSTRATION	5.1.3
U-005	SE 9-10	SWITCH DEMONSTRATION	5.1.3
U-006	SE 1-4	TIMING DEMONSTRATION	5.1.4
U-007	SE 5-8	TIMING DEMONSTRATION	5.1.4
U-008	SE 9-10	TIMING DEMONSTRATION	5.1.4
U-009	DE 1-4	SWITCH DEMONSTRATION	5.1.5
U-010	DE 5	SWITCH DEMONSTRATION	5.1.5
U-011	DE 1-4	TIMING DEMONSTRATION	5.1.6
U-012	DE 5	TIMING DEMONSTRATION	5.1.6
U-013	SC	SWITCH DEMONSTRATION	5.1.7
U-014	SC	INTERFACE DEMONSTRATION	5.1.7
U-015	CC	SWITCH DEMONSTRATION	5.1.8
U-016	CC	INTERFACE DEMONSTRATION	5.1.8
U-017	PAM	SWITCH DEMONSTRATION	5.1.9
U-018	DASF	SWITCH DEMONSTRATION	5.1.10
U-019	TCU	SWITCH DEMONSTRATION	5.1.11
U-020	I/O TESTER 2540/1403	SWITCH DEMONSTRATION	5.1.12
U-021	1052	SWITCH DEMONSTRATION	5.1.13
U-022	DAU	SWITCH DEMONSTRATION	5.1.14
U-101	CE 1	FUNCTIONAL TEST	5.2.1
U-102	CE 2	FUNCTIONAL TEST	5.2.1
U-103	CE 3	FUNCTIONAL TEST	5.2.1
U-104	CE 4	FUNCTIONAL TEST	5.2.1
U-105	CE/SE/DE	ATR TEST	5.2.1

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-106	IOCE 1	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-107	IOCE 2	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-108	IOCE 3	SELECTOR CHAN. FUNCTIONAL TEST	5.2.2
U-109	DASF 1	FUNCTIONAL TEST	5.2.2
U-110	DASF 2	FUNCTIONAL TEST	5.2.2
U-111	DASF 3	FUNCTIONAL TEST	5.2.2
U-112	TCU#1,TD#1-4	FUNCTIONAL TEST	5.2.2
U-113	TCU#1,TD#5-8	FUNCTIONAL TEST	5.2.2
U-114	TCU#2,TD#1-4	FUNCTIONAL TEST	5.2.2
U-115	TCU#2,TD#5-8	FUNCTIONAL TEST	5.2.2
U-116	TCU#3,TD#1-4	FUNCTIONAL TEST	5.2.2
U-117	TCU#3,TD#5-8	FUNCTIONAL TEST	5.2.2
U-118	SCU	TWO CHANNEL SWITCH TESTS	5.2.2
U-119	TCU	DUAL INTERFACE TESTS	5.2.2
U-120	IOCE 1	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-121	IOCE 2	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-122	IOCE 3	CHAN. TO CHAN. FUNCTIONAL TEST	5.2.2
U-123	IOCE 1	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-124	IOCE 2	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-125	IOCE 3	MULTIPLEXOR CHAN. FUNCTIONAL TEST	5.2.3
U-126	SE 1-3	FUNCTIONAL TEST	5.2.4
U-127	SE 4-6	FUNCTIONAL TEST	5.2.4
U-128	SE 7-9	FUNCTIONAL TEST	5.2.4
U-129	SE 10	FUNCTIONAL TEST	5.2.4
U-130	DE 1,2	FUNCTIONAL TEST	5.2.5
U-131	DE 3,4	FUNCTIONAL TEST	5.2.5
U-132	DE 5	FUNCTIONAL TEST	5.2.5
U-133	SC	FUNCTIONAL TEST	5.2.6

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
U-134	CC	FUNCTIONAL TEST	5.2.7
U-135	PAM	FUNCTIONAL TEST	5.2.8
U-136	PAM	DUAL INTERFACE TESTS	5.2.8
U-137	2821	FUNCTIONAL TEST, 2540, 1403	5.2.9
U-138	2821	TWO CHANNEL SWITCH TEST	5.2.9
U-139	1052	FUNCTIONAL TEST	5.2.10
U-140	DAU	FUNCTIONAL TEST	5.2.11
U-141	DAU	TWO PROCESSOR SWITCH TEST	5.2.11
U-142	IOCE 1	DIAG. MODE FUNCTIONAL DEMO	5.2.12
U-143	IOCE 2	DIAG. MODE FUNCTIONAL DEMO	5.2.12
U-144	IOCE 3	DIAG. MODE FUNCTIONAL DEMO	5.2.12
U-145	IOCE	I/O PROCESSOR OPERATION DEMO	5.2.13
U-146	CE/IOCE/SE/DE	LOG-OUT DEMONSTRATION	5.2.14
U-147	IOCE	FLT FUNCTIONAL TEST	5.2.15
U-148	CE	FLT FUNCTIONAL TEST	5.2.15

SYSTEM TEST

TEST NO.	ELEMENT/UNIT	DESCRIPTION	SPEC. REF.
S-001	SYSTEM	RECONFIGURATION TEST A	6.1.1
S-002	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-003	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-004	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-005	SYSTEM	RECONFIGURATION TEST B	6.1.2
S-006	SYSTEM	RECONFIGURATION TEST C	6.1.3
S-007	SYSTEM	RECONFIGURATION TEST D	6.1.4
S-101	SYSTEM	SEVA	6.2.1
S-120	SYSTEM	EIGHT TIME SAMPLE PROBLEMS	6.3.1
S-121	SYSTEM	DISPLAY INSTRUCTION PERF. TEST	6.3.2
S-122	SYSTEM	FLT PRACTICAL TEST	6.3.3
S-123	SYSTEM	360-9020 COMPATIBILITY TEST	6.3.4
S-124	SYSTEM	360 MODE RECALL TEST	6.3.5
S-131	SYSTEM	POWER INTERLOCK TEST	7.1.1
S-132	SYSTEM	TEST STATE-POWER ON/OFF	7.1.2
S-133	SYSTEM	MPO SWITCH TEST	7.1.3
S-134	CE/IOCE/SE/DE	ABNORMAL POWER LOSS AND BATTERY RECHARGE	7.2
S-135	SYSTEM	THERMAL WARNING AND PROTECTION	7.3
S-136	SYSTEM	OVER/VOLTAGE	7.4.1
S-137	SYSTEM	OVER/CURRENT	7.4.2
S-138	SYSTEM	UNDER/VOLTAGE	7.4.3
S-139	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-140	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-141	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-142	SYSTEM	SYSTEM MAIN LINE POWER LOSS	7.5
S-150	SYSTEM	FACTORY ACCEPTANCE EXERCISE	8.0
S-160	SYSTEM	SYSTEM EPO	7.6

APPENDIX M

DIAGNOSTIC MONITOR INPUT MESSAGES

AND

SENSE SWITCH OPTIONS

INPUT MESSAGES

A (Add) Messages

Format	Purpose	Definition of Characters
APPOOØCUU/	Add I/O Unit (long format)	
Example: A4031Ø524/		
A - Add message		A - Message type
40 - Tape unit		PP - Symbolic Address of unit added (Refer to Fig. 1)
3 - Mod 3		OO - Options (Refer to Fig. 2)
1 - D. C.		Ø - Always zero
Ø - Always zero		CUU - Chan & Unit address
5 - IOCE #2, Sel. Chan. #1		/ - End of message
2 - TCU #2		
4 - TD #4		
/ - End of message		
A,CUU/	Add I/O Unit (short format)	
Example: A,211/		
A, - Add message		A - Message type
2 - IOCE #1, Chan #2		, - Must be included
1 - TCU #1		CUU - Chan & Unit address
1 - TD #1		/ - End of message
/ - End of message		

A (Add) Messages

Format	Purpose	Definition of Characters
APP/	Add element; MDM only	
Example: A12/		
A - Add message		A - Message type
12 - CE #2		PP - Symbolic address of unit (Refer to Fig. 1)
/ - End of message		/ - End of message

B (Begin) Messages

B/	Start Assigned task	
Example: B/		
B - Begin		B - Message type
/ - End of message		/ - End of message
BPPSS/	Restart task after Error Halt or operator requested halt	
Example: B4063/		
B - Begin message		B - Message type
4063 - Program number		PPSS - Program number
/ - End of message		/ - End of message

7/17/84

C (Cycle) Messages

Format	Purpose	Definition of Characters
CPPSS/	Causes designated program to be looped	
Example: C4063/ C - Cycle message 4063 - Program number / - End of message		C - Message type PPSS - Program number / - End of message
CPPSSRR/	Causes designated routine of specified program to be looped	
Example: C625104/ C - Cycle message 6251 - Program number 04 - Routine number / - End of message		C - Message type PPSS - Program number RR - Routine number (refer to particular program write-up) / - End of message
CPPSSRRHH/	Causes designated routine of specified program to be looped a specific number of times	
Example: C6251041A/ C - Cycle message 6251 - Program number 04 - Routine number 1A - Routine loops 26 times / - End of message		C - Cycle message PPSS - Program number RR - Routine number HH - Number of cycles to be looped (hex) / - End of message

D (Define Storage) Message

Format	Purpose	Definition of Characters
DPPSS.$H_1H_1H_1$.$H_2H_2H_2$/	Define storage location block	

Example: D2701.005.007/

- D - Define message
- 2701.- Program number
- 005. - 5000 (Hex) address
- 007 - 7000 (Hex) address
- / - End of message

Definition of Characters:

- D - Message type
- PPSS - Program number
- . - Must be included
- $H_1H_1H_1$ - Start location of storage block defined
- . - Must be included
- $H_2H_2H_2$ - Terminal location of storage block defined
- / - End of message

E (Enter Data) Messages

Format	Purpose	Definition of Characters
EAAAAAA.CC.HHH___ ___H/	Used to store Hex data in bytes specified (2 per byte)	
Example: E570.4.47F0B200/		
E - Enter message		E - Message type
570. - Core location first byte		AAAAAA - Absolute core location (exempt leading zero's)
4. - Number of bytes modified		. - Must be included
47 - Contents of byte 570		CC - Count in Hex of bytes to be modified starting with absolute core location
F0 - Contents of byte 571		. - Must be included
B2 - Contents of byte 572		HHH___ ___H - Hex numbers stored in bytes specified (2 per byte) in CC portion
00 - Contents of byte 573		/ - End of message
/ - End of message		

E (Enter Data) Message

Format

EAAAAAA.CC.NEEE_ _E/

Example: E4006.A.NREVISION01

- E - Enter message
- 4006. - Absolute core location
- A. - 10 characters to be entered
- N - Denotes EBCDIC characters
- R - Contents of 4006
- E - Contents of 4007
- V - Contents of 4008
- I - Contents of 4009
- S - Contents of 400A
- I - Contents of 400B
- O - Contents of 400C
- N - Contents of 400D
- 0 - Contents of 400E
- 1 - Contents of 400F
- / - End of message

Purpose

Used in Store EBCDIC data in bytes specified (1 per byte)

- E - Message type
- AAAAAA - Absolute core location (exempt leading zero's)
- . - Must be included
- CC - Count in Hex of bytes to be modi
- . - Must be included
- EEE__ __E - EBCDIC characters stored in bytes specified (1 per byte)
- / - End of message

Free Message

FPPSS/

Example: F4063/

- F - Free message
- 4063 - Program number
- / - End of message

Stop Program loaded in core

- F - Message type
- PPSS - Program number
- / - End of message

G (Define PAM) Messages

Format

G,T,1,XX__YY

Example: G,1,1,10___16/
- G, - G message
- 1, - AB PAM
- 1, - #1 type PAM message
- 10-16 - PAM adapters address 10 to 16 (Hex) will be run
- / - End of message

Purpose

Run all sequential adapters between selected address

Definition of Characters

- G - Message type
- , - Must be included
- T - PAM type (Refer to Figure 3)
- , - Must be included
- 1 - Type of G message
- XX - Start address of Adapters run
- __ - Must be included
- YY - Terminal address of Adapters run
- / - End of message

G (Define PAM) Messages

Format	Purpose	Definition of Characters
G,T,3,H/	Run all Adapters of a selected type	
Example: G,2,3,5/		
G - G message		G - Message type
2, - BC PAM		, - Must be included
3, - #3 type G Message		T - PAM type (Refer to Fig. 3)
5 - TTYLL Adapters run		, - Must be included
/ - End of message		3 - Type of G message
		, - Must be included
		H - Type of Adapter (Figure 4)
		/ - End of message

Halt Messages

H/	Halt all sections currently running in core.	
Example: H/		
H - Halt		H - Message type
/ - End of message		/ - End of message
HPPSS/		
Example: H4063/	Halt a particular section	
	MDM only	
H - Halt		H - Message type
4063 - Program number		PPSS - Program number
/ - End of message		/ - End of message

I (Initialize) Messages

Format	Purpose	Definition of Characters
I/	Completely initialize monitor and monitor tables	
Example: I/ I - Initialize message / - End of message		I - Message type / - End of message
I,CUU_1,CUU_2,CUU_3,CUU/	Assign or reassign the monitor I/O devices.	
Example: I,003,002,005,223/ I, - Initialize message 003, - 2540 Input device 002, - #1 Typewriter primary output device 005, - A 1403 secondary output device 223 - Tape 3 TCU_2 Diagnostic Loader / - End of message		I - Message type , - Must be included CUU_1 - Input device , - Must be included CUU_2 - Primary output device , - Must be included CUU_3 - Secondary output device , - Must be included CUU - Diagnostic Loader / - End of message

K (Read Input Device) Message

MDM only

Format	Purpose	Definition of Characters
K/	Loads Card from Reader	
Example: K/ K - Load Card / - End of message		K - Message type / - End of message

L (Load) Messages

L/	Informs Monitor to run all Diagnostic Programs in order of listing	
Example: L/ L - Load message / - End of message		L - Message type / - End of message
LPPSS/	Informs Monitor to run one specific program	
Example: L1151/ L - Load message 1151 - Program number / - End of message		L - Load message PPSS - Program number / - End of message

L (Load) Messages

MDM only

Format	Purpose	Definition of Characters
L,CUU/	Runs all applicable programs on specified I/O Device	
Example: L,524/ L, - Load message 524 - IOCE #2, Sel Chan #1, TCU #2, TD #4 / - End of message		L - Message type , - Must be included CUU - I/O Device / - End of message
LMPPSS/	Load the designated section into the IOCE's MACH storage, beginning at location C00000 hex.	
Example: LM4053/ L - Load Message M - MACH storage 4053 - Program number / - End of message		L - Message type M - MACH storage PPSS - Program number / - End of message
LSPPSS/	Load the designated section into Main storage.	
Example: LS4052/ L - Load message S - Main storage 4052 - Program number / - End of message		L - Message type S - Main storage PPSS - Program number / - End of message

L (Load) Messages

SDM only

LPPSS,CUU,CU,C,_,CUU/	Load a specific program to be run on specified I/O Unit, Control Unit or Channel as applicable.	L - Message type PPSS - Program number , - Must be included CUU - I/O Device , - Must be included CU - Control Unit , - Must be included C - Channel / - End of message
Example: L4050,630,52,1/ L - Load message 4050, - Program number 630, - IOCE #2, Sel Chan #2, TCU #3, TD #0 52, - IOCE #2, Sel Chan #1, TCU #2 1 - IOCE #1, Sel Chan #1, TCU #1 / - End of message		

L (Load) Messages

Format	Purpose	Definition of Characters
L0.PPSS/	Informs Monitor to sequentially run first program in a category up to a specified program.	
Example: L0.405D/ L - Load message 0 - First program in category 405D - Last program run / - End of message		L - Type of message 0 - First program in category . - Must be included PPSS - Last program run / - End of message
LPPSS.0/	Runs all programs sequentially from specified program to highest numbered program in that category	
Example: L4053.0/ L - Load message 4053. - First program run 0 - Last program in category / - End of message		L - Message type PPSS - First program run . - Must be included 0 - Last program in category / - End of message
LPPSS.PPSS/	Runs all programs sequentially from first specified to last specified.	
Example: L4050.4055.1 L - Load message 4050 - First program run 4055 - Last program run / - End of message		L - Message type PPSS - First program run . - Must be included PPSS - Last program run / - End of message

L (Load) Messages

Format	Purpose	Definition of Characters
LPPSS, CUU,CUU,----CUU/	Runs specific program on specified I/O units	
Example: L4052,525,524,224/		
L - Load Message		L - Message type
4052, - Program number		PPSS - Program number
525, - IOCE #2, Sel Chan #1, TCU #2, TD 5		, - Must be included
524, - IOCE #2, Sel Chan #1, TCU #2, TD 4		CUU - I/O Device
224 - IOCE #1, Sel Chan #2, TCU #2, TD 4		, - Must be included
/ - End of message		CUU,--CUU - I/O Device (add'l)
		/ - End of message
LPPSS.PPSS,CUU,CUU,---CUU/	Runs group of programs on specified I/O Devices	
Example: L4050, 4055, 525, 524,224/		
L - Load message		L - Message type
4050. - First program run		PPSS - First program run
4055, - Last program run		. - Must be included
525, - IOCE #2, Sel Chan #1, TCU #2, TD #5		PPSS - Last program run
524, - IOCE #2, Sel Chan #1, TCU #2, TD #4		, - Must be included
224 - IOCE #1, Sel Chan #2, TCU #2, TD #4		CUU - I/O Device
/ - End of message		, - Must be included
		CUU,--CUU - I/O Device
		/ - End of message

L (Load) Messages

SDM only

LPPSS.PPSS,CUU,CU,C,__,CUU/ — Loads a series of specific programs to be run on specified I/O Unit, Control Unit or Channel as applicable

Example: L4050.4060,630,52,1/
- L - Load message
- 4050. - First program loaded
- 4060. - Last program loaded
- 630, - IOCE #2, Sel Chan #2, TCU #3, TD #0
- 52, - IOCE #2, Sel Chan #1, TCU #2
- 1 -- IOCE #1, Sel Chan #1
- / - End of message

- L - Message type
- PPSS - First program loaded
- . - Must be included
- PPSS - Last program loaded
- , - Must be included
- CUU - I/O Device
- , - Must be included
- CU - Control Unit
- , - Must be included
- C - Channel
- / - End of message

M(Print Monitor Table) Message

M/ — Causes printing of Monitor tables and other useful data

Example: M/
- M - Print Monitor Table Message
- / - End of message

- M - Message type
- / - End of message

N (Negate) Pending Load Message

MDM only

Format	Purpose	Description of Characters
N/	Delete a load message that was previously entered but has not yet been verified	
Example: N/		
N - Negate message		N - Message type
/ - End of message		/ - End of message

O (Operator Intervention Required) Message

OPPSS/	Informs Monitor Operator intervention is needed in a specific program	
Example: O1156/		
O - Operator intervention message		O - Message type
1156 - Program number		PPSS - Program number
/ - End of message		/ - End of message

P (Print Cycle Count) Message

PPPSS/	Causes printout of amount of times a program or a routine has been cycled	
Example: P1156/		
P - Print message		P - Message type
1156 - Program number		PPSS - Program number
/ - End of Message		/ - End of message

Q (Enter Free-Form Data) Messages

MDM only

Format	Purpose	Definition of Character
Q. (Free Form)/ Example: Q.L/ Q. - Free Form Data Message L - Loop on Configuration / - End of message	Allows insertion of program option to the SEVA or Reconfiguration programs. Must be included with Load message. Refer to SEVA and Reconfiguration write-ups for codes used.	Q - Message type . - Must be included (free form) - Option characters / - End of message
QPPSS. (Free Form)/ Example: QE0C7.23/ - Free Form Data Message E0C7. - Program number 23 - SE #3 / - End of message	Allows insertion of program options to specific programs within the SEVA or Reconfiguration program.	Q - Message type . - Must be included PPSS - Program number . - Must be included (Free Form) - End of message

S (Alter Sense Switch) Messages

S0.HHHHHHHH/ — Change Monitor Sense Switches

Example: S0.0000111F/
S - Sense Switch message
0. - Defines Monitor Sense Switches
0000111F-Sense Switch Configuration
(0000 0000 0000 0000 0001 0001 0001 1111)
/ - End of message

S - Message type
0 - Monitor Sense Switc
. - Must be included
HHHHHHHH - Sense Switch Data (Refer to Fig. 5)
/ - End of message

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S (Alter Sense Switch) Messages

Format	Purpose	Definition of Characters
SPPSS.HHHHHHHH/	Change a specific program's Sense Switches	
Example: S10A1,0000 204A/		
S - Sense Switch message		S - Message type
10A1. - Program number		PPSS - Program number
0000204A - Sense Switch Configuration		. - Must be included
		HHHHHHHH - Sense Switch Data (Refer to Program Write-Ups)
		/ - End of message
SS0.DD.---.DD/	Set Monitor Sense Switches (Short Set Format)	
Example: SS0.24.28/		S - Set
S - Set		S - Message type
S - Sense Switch message		0 - Monitor Sense Switche
0. - Defines Monitor Sense Switches		. - Must be included
24. - Sense Switch #24		DD - Sense Switch (decima
28 - Sense Switch #28		.---.DD - Additional Sense Swit
/ - End of message		/ - End of message
SSPPSS.DD.---.DD/	Set a specific program's Sense Switches (Short Set Format)	
Example: SS6251.19.25/		S - Set
S - Set		S - Message type
S - Sense Switch message		PPSS - Program number
6251. - Program number		. - Must be included
19. - Sense Switch #19		DD - Sense Switch (decima
25 - Sense Switch #25		.---.DD - Additional Sense Swit
/ - End of message		/ - End of message

Format	Purpose	Definition of Characters
RS0.DD.---.DD/	Reset Monitor Sense Switches (Short Reset Format)	
Example: RS0.16.20/		
R - Reset		R - Reset
S - Sense Switch message		S - Message type
0 - Defines Monitor Sense Switches		0 - Monitor Sense Switche
16. - Sense Switch #16		. - Must be included
20 - Sense Switch #20		DD - Sense Switch (decimal
/ - End of message		.---.DD - Additional Sense Swit
		/ - End of message
RSPPSS.DD.---.DD/	Reset a specific program's Sense Switches (Short Reset Format)	
Example: RS6251.22.31/		
R - Reset		R - Reset
S - Sense Switch Message		S - Message type
6251. - Program number		PPSS - Program number
22. - Sense Switch #22		. - Must be included
31 - Sense Switch #31		DD - Sense Switch (decimal
/ - End of message		.---.DD - Additional Sense Swit
		/ - End of message

T (Type Out) Messages

Format	Purpose	Definition of Characters
TA.AAAAAA.CCCC/	Causes printout of specific amount of bytes from a specified location in core	
Example: TA.1000.10F/ T - Type message A. - Type of T message 1000. - Hex Address of first byte printout 10F1 - Number of bytes to be sequentially typed (Hex) / - End of message		T - Message type A - Type of T message . - Must be included AAAAAA - Core Address . - Must be included CCCC - Amount of bytes to be printed (hex) / - End of message
TPPSS.AAAAAA.CCCC/	Causes printout of specific amount of bytes from specified location of a program loaded in core	
Example: T1156.1000.00FF/ T - Type message 1156. - Program number 1000. - Hex Address of first byte typed 00FF - Amount of bytes typed out (hex) / - End of message		T - Message type PPSS - Program number . - Must be included AAAAAA - Absolute core location . - Must be included CCCC - Amount of bytes typed out (hex) / - End of message
TPPSS/	Types complete Diagnostic Program	
Example: T1156/ T - Type Out message 1156 - Program number / - End of message	NOTE: Section 'PPSS' must be an active section.	T - Message type PPSS - Program number / - End of message

U (Define System) Messages

Format

U--Variable----/

Purpose

Defines system available to Monitor for use or for testing against Diagnostics.

Example: U11.21.31.41,0,1,2,3.61,63,6B.C1.66/

U - Define message
11. - CE #1
21. - SE #1
31. - IOCE #1
41, - TCU #1
0, - TD #0
1, - TD #1
2, - TD #2
3. - TD #3
61, - Reader (2540)
63, - Printer (1403)
6B. - Punch (2540)
C1. - PAM #1
66 - PAM #1 Typewriter
/ - End of message

Definition of Characters

Variable
U - Message
- Define System
(Refer to Fig. #1)
/ - End of message

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U (Define System) Messages

MDM only

UA.Variable----/

Defines system available to Monitor and bypass table-clearing.

Example: Same as basic U message with addition of A.

U - Message type
A - Bypass table-clearing
Variable . - Must be included (Refer to Figure #1)
/ - End of message

USN.Variable----------/

Defines system available to Monitor and defines the maintenance system state

Example: Same as basic U message with addition of SN.

U - Message type
SN - System state (S0,S1,S
Variable . - Must be included
- (Refer to Figure #1)
/ - End of message

UASN.Variable----------/

Defines system available to Monitor, bypasses table-clearing, and defines the maintenance system state.

Example: Combination of the above two formats.

U - Message type
A - Bypass table-clearing
SN - System state(S0,S1,S2
. - Must be included
--Variable-- - (Refer to Figure #1)
/ - End of message

V (Verify Pending Load) Message

MDM only

Format	Purpose	Definition of Characters
V/	Verifies preceding Load Message and allows loading	
Example: V/ V - Verify message / - End of message		V - Message type / - End of message

W (Withdraw) Message

W,CUU/	Remove Unit from Monitor UDT	
Example: W,523/ W, - Withdraw message 523 - IOCE #2, Sel Chan #1, TCU #2, Tape Drive #3 / - End of message		W - Message type , - Must be included CUU - I/O Device / - End of message

Z (Process Select Storage)Messages

MDM only

Z.C/	Assign which CE will control program loaded in future Load Messages	
Example: Z.2/ Z. - Process Select message 2 - CE #2 / - End of message		Z - Message type . - Must be included C - CE number / - End of message

Z (Process Select Storage) Messages

MDM only

Format	Purpose	Definition of Characters
ZS/	Assigns which SE programs loaded from future Load Messages will be loaded in.	
Example: Z4/ Z - Process Select message 4 - SE #4 / - End of message		Z - Message type S - SE number / - End of message
ZS.C/	Assigns what CE will control, and which SE programs loaded by future load messages will enter.	
Example: Z2.2/ Z - Process Select message 2. - SE #2 2 - CE #2 / - End of message		Z - Message type S - SE number . - Must be included C - CE number / - End of message

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1 (Read Input Device Again) Message

Format	Purpose	Definition of Characters
1PPSS/	Request the Monitor to automatically read the input device again. (Terminates read when B/ is encountered.)	
Example: 11156/ 1 - Read Input Device Again message. 1156 - Program number / - End of Message		1 - Message type PPSS - Program number / - End of message

UNIT SYMBOLIC ADDRESSES

FIGURE #1

APPOOOCUU/ Message	U or APP/ (MDM) Message	Unit Identification
-	1X	CE X
-	2X	SE X
-	3X	IOCE X
40	-	Tape Drive
-	4X,Y,---,Y	TCU X with attached tape drives of device addresses of Y,---,and Y.
-	5X	DE X
62	62	2540 Card Reader
63	63,X	1403 Printer where X (1,2 or 3) is defined by the position of the printer in the MDM's UDT.
66	66	1052 Printer-Keyboard*
6B	6B	2540 Card Punch
6C	6C	Console
80	8X,Y,---,Y	SCU X with attached DSU's with Device Addresses of Y,---,and Y.
90	9X	RCU X. Define none or one per IOCE
A0	AX	Channel-to-Channel Adapter X
B0	BX	DAU X
CC	CX	PAM X Define none, one, or two per IOCE.

* The 1052 is attached to the preceding PAM in the U-message or, if not preceding PAM is entered, to the console.

UNIT OPTIONS

FIGURE #2

I/O Device	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Tape	USASCII Code	MODEL Number - Binary					Read While Write TCU	Data Converter
2540	USASCII Code	Card Image	Punch-Read-Feed-	51 Col. Read				
1403	USASCII Code	Selective Tape Lister	60 Char-acter Set	Universal Character Set	High Speed Version	120 Print Position	01 = PN CHAIN-NORM 10 = HN CHAIN-SPEC 11 = E PATCH INTO SECTION	
RCU								Expanded Addressing
DAU							Two Processor Switch	Multi-Device Attachment

PAM TYPE

FIGURE #3

1. = AB PAM
2. = BC PAM
3. = AC PAM

ADAPTER TYPE

FIGURE #4

1. GPI Adapter
2. GPO Adapter
3. INTI Adapter
4. INTO Adapter
5. TTYLL Adapter
6. RVDP Adapter
7. 1052 Adapter
8. Test & Monitor Adapter
9. CD Adapter
A. FDEP Adapter
B. BP Adapter

DIAGNOSTIC MONITOR SENSE SWITCH OPTIONS

Figure 5

Sense S.W. No. (Decimal)	Meaning When Clear	Meaning When Set	SDM	MDM
0-14		(For Internal DM Use Only)		
15	Allow Forced CE Errors	Inhibit Forced CE Errors	X	X
16	Set Sequential Mode	Set Multiprogramming Mode		X
17	Set Simplex Mode	Set Multiprocessing Mode		X
18		(For Internal DM Use Only)		
19	Format Logouts	Do Not Format Logouts	X	X
20	Execute Section	Wait Before Executing Section	X	X
21	Allow Manual Intervention Sections	Bypass Manual Intervention Sections	X	X
22	Print Environment On Error	Do Not Print Environment On Error	X	
23	Do Not Print Cycle Count	Print Cycle Count	X	X
24	Print Section S and T Messages	Do Not Print Section S & T Messages	X	X
25	Do Not Halt On Error	Halt On Error	X	X
26	Do Not Repeat Entire Task Request	Repeat Entire Task Request	X	X
27	Allow Printing	Inhibit All Printing	X	X
28	Print Logouts	Bypass Logout Printing	X	X
29	Allow Operational Printouts	No Operational Printout		X
30	Print Errors	Do Not Print Errors	X	X
31	Ignore Keyed-In Data Area	Data Area Contains Keyed-In Message	X	

APPENDIX N

SYSTEM MAINTENANCE MONITOR CONSOLE (SMMC)

CABLE CONNECTOR PIN ASSIGNMENTS

APPENDIX N

9020D SC to SMMC Pin Assignment

Connector #1 01S-S3-C2

Pin	Line Name	Pin	Line Name
B02	Config. Reg-1 CE-1	G02	Config. Reg-1 Storage 12
D02	Gnd Return	J02	Gnd Return
B03	Config. Reg-1 CE-2	G03	Config. Reg-1 PAM-1
D03	Config. Reg-1 CE-3	J03	Config. Reg-1 PAM-2
B04	Config. Reg-1 CE-4	G04	Config. Reg-1 PAM-3
D04	Config. Reg-1 IOCE-1	J04	Config. Reg-1 TCU-1
B05	Config. Reg-1 IOCE-2	G05	Config. Reg-1 TCU-2
D05	Config. Reg-1 IOCE-3	J05	Config. Reg-1 TCU-3
B06	Config. Reg-1 Storage 1	G06	Config. Reg-2 CE-1
D06	Config. Reg-1 Storage 2	J06	Config. Reg-2 CE-2
B07	Gnd Return	G07	Gnd Return
D07	Config. Reg-1 Storage 3	J07	Config. Reg-2 CE-3
B08	Config. Reg-1 Storage 4	G08	Config. Reg-2 CE-4
D08	Gnd Return	J08	Gnd Return
B09	Config. Reg-1 Storage 5	G09	Config. Reg-2 IOCE-1
D09	Config. Reg-1 Storage 6	J09	Config. Reg-2 IOCE-2
B10	Config. Reg-1 Storage 7	G10	Config. Reg-2 IOCE-3
D10	Config. Reg-1 Storage 8	J10	Config. Reg-2 Storage 1
B11	Config. Reg-1 Storage 9	G11	Config. Reg-2 Storage 2

Connector #1 (contd.)

Pin	Line Name	Pin	Line Name
D11	Config. Reg-1 Storage 10	J11	Config. Reg-2 Storage 3
B12	Config. Reg-1 Storage 11	G12	Config. Reg-2 Storage 4
D12	Config. Reg-1 SCU-1	J12	Config. Reg-1 SCU-3
B13	Gnd Return	G13	Gnd Return
D13	Config. Reg-1 SCU-2	J13	Config. Reg-2 SCU-1

Connector #2 01S-S3-D2

Pin	Line Name	Pin	Line Name
B02	Config. Reg-2 Storage 5	G02	Config. Reg-3 IOCE-1
D02	Gnd Return	J02	Gnd Return
B03	Config. Reg-2 Storage 6	G03	Config. Reg-3 IOCE-2
D03	Config. Reg-2 Storage 7	J03	Config. Reg-3 IOCE-3
B04	Config. Reg-2 Storage 8	G04	Config. Reg-3 Storage 1
D04	Config. Reg-2 Storage 9	J04	Config. Reg-3 Storage 2
B05	Config. Reg-2 Storage 10	G05	Config. Reg-3 Storage 3
D05	Config. Reg-2 Storage 11	J05	Config. Reg-3 Storage 4
B06	Config. Reg-2 Storage 12	G06	Config. Reg-3 Storage 5
D06	Config. Reg-2 PAM-1	J06	Config. Reg-3 Storage 6
B07	Gnd Return	G07	Gnd Return
D07	Config. Reg-2 PAM-2	J07	Config. Reg-3 Storage 7
B08	Config. Reg-2 PAM-3	G08	Config. Reg-3 Storage 8
D08	Gnd Return	J08	Gnd Return
B09	Config. Reg-2 TCU-1	G09	Config. Reg-3 Storage 9
D09	Config. Reg-2 TCU-2	J09	Config. Reg-3 Storage 10
B10	Config. Reg-2 TCU-3	G10	Config. Reg-3 Storage 11
D10	Config. Reg-3 CE-1	J10	Config. Reg-3 Storage 12
B11	Config. Reg-3 CE-2	G11	Config. Reg-3 PAM-1
D11	Config. Reg-3 CE-3	J11	Config. Reg-3 PAM-2
B12	Config. Reg-3 CE-4	G12	Config. Reg-3 PAM-3
D12	Config. Reg-2 SCU-2	J12	Config. Reg-3 SCU-1
B13	Gnd Return	G13	Gnd Return
D13	Config. Reg-2 SCU-3	J13	Config. Reg-3 SCU-2

Connector #3 01S-S3-E2

Pin	Line Name	Pin	Line Name
B02	Config. Reg-3 TCU-1	G02	Config. Reg-4 Storage 9
D02	Gnd Return	J02	Gnd Return
B03	Config. Reg-3 TCU-2	G03	Config. Reg-4 Storage 10
D03	Config. Reg-3 TCU-3	J03	Config. Reg-4 Storage 11
B04	Config. Reg-4 CE-1	G04	Config. Reg-4 Storage 12
D04	Config. Reg-4 CE-2	J04	Config. Reg-4 PAM-1
B05	Config. Reg-4 CE-3	G05	Config. Reg-4 PAM-2
D05	Config. Reg-4 CE-4	J05	Config. Reg-4 PAM-3
B06	Config. Reg-4 IOCE-1	G06	Config. Reg-4 TCU-1
D06	Config. Reg-4 IOCE-2	J06	Config. Reg-4 TCU-2
B07	Gnd Return	G07	Gnd Return
D07	Config. Reg-4 IOCE-3	J07	Config. Reg-4 TCU-3
B08	Config. Reg-4 Storage 1	G08	Mode Ind. Alpha-A
D08	Gnd Return	J08	Gnd Return
B09	Config. Reg-4 Storage 2	G09	Mode Ind. Alpha-B
D09	Config. Reg-4 Storage 3	J09	Mode Ind. Alpha-C
B10	Config. Reg-4 Storage 4	G10	Mode Ind. Numeric-1
D10	Config. Reg-4 Storage 5	J10	Mode Ind. Numeric-2
B11	Config. Reg-4 Storage 6	G11	Mode Ind. Numeric-3
D11	Config. Reg-4 Storage 7	J11	Mode Ind. Numeric-4
B12	Config. Reg-4 Storage 8	G12	Mode Ind. Numeric-5
D12	Config. Reg-3 SCU-3	J12	Mode Ind. Numeric-6
B13	Gnd Return	G13	Gnd Return
D13	Config. Reg-4 SCU-1	J13	Mode Ind. Numeric-7

Connector #4 01S-S3-B2

Pin	Line Name	Pin	Line Name
B02	Power Check CE-1	G02	Power Check PAM-1
D02	Gnd Return	J02	Gnd Return
B03	Power Check CE-2	G03	Power Check PAM-2
D03	Power Check CE-3	J03	Power Check PAM-3
B04	Power Check CE-4	G04	Power Check TCU-1
D04	Power Check IOCE-1	J04	Power Check TCU-2
B05	Power Check IOCE-2	G05	Power Check TCU-3
D05	Power Check IOCE-3	J05	Power Check SCU-1
B06	Power Check Storage 1	G06	Power Check SCU-2
D06	Power Check Storage 2	J06	Power Check SCU-3
B07	Gnd Return	G07	Gnd Return
D07	Power Check Storage 3	J07	Spare
B08	Power Check Storage 4	G08	Spare
D08	Gnd Return	J08	Gnd Return
B09	Power Check Storage 5	G09	Spare
D09	Power Check Storage 6	J09	Spare
B10	Power Check Storage 7	G10	Spare
D10	Power Check Storage 8	J10	Spare
B11	Power Check Storage 9	G11	Spare
D11	Power Check Storage 10	J11	Spare
B12	Power Check Storage 11	G12	Spare
D12	Power Check Storage 12	J12	Config. Reg-4 SCU-2
B13	Gnd Return	G13	Gnd Return
D13	Spare	J13	Config. Reg-4 SCU-3

9020E CC to SMMC Pin Assignment

Connector #1 01S-A5-A1

Pin	Line Name
B02	-Data
D02	+Data
B04	-Clock
B03	+Clock
D04	-Transfer
D05	+Transfer
B07	-Disabled
B05	+Disabled
D06	-Fault
D07	+Fault
B09	-Help
B08	+Help
D09	-Request
D10	+Request
B12	-Interlock
B10	+Interlock
D11	-Power Monitor Tripped
D12	+Power Monitor Tripped
D13	-Power Monitor Override
B13	+Power Monitor Override
D08	Ground