# 9020 D System
# 9020 E System
# Design Data

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International Business Machines Corporation

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This document is submitted to the Federal Aviation Agency by the
International Business Machines Corporation in response to Section
3.11.5 of FAA-ER-606-063 under Contract Number FA64WA-5223 and
contains Design Data for the IBM 9020D and 9020E Data Processing
Systems.  The following documents are pertinent to understanding the
design of the 9020D and 9020E Systems and the reader should
familiarize himself with them:  Amendments 65 and 66 of Contract
Number FA64WA-5223; FAA Specification FAA-ER-606-063 dated 15 October
1963, and its amendments; FAA Specification FAA-ER-NS-100-1 dated
20 February 1969; IBM 9020D and 9020E System Principles of Operation
Manual.

     This document provides detailed information for each of the
system components and for system control features, such as
configuration control, and system power.  Specifically, the infor-
mation includes block diagrams, information logic flow diagrams,
input/output details, logic diagrams, and a detailed physical
description.

     Each chapter is organized as follows:  a brief functional
description of the subject is presented, followed by design details.
The detailed interface line descriptions are presented in Chapter 13.

     Figures 1-1 and 1-2 show all system components of the basic
9020D Central Computer Complex and 9020E Display Channel Processor
Configurations, respectively.  The following equipment options are
available for the 9020D System:  addition of a fourth CE and
addition of a ninth and tenth SE.  Equipment options for the 9020E
are:  addition of a fourth CE, a fifth SE, a fifth DE, a third IOCE
and a third TCU and expansion options for the Configuration Console.
The 9020E System shown in Figure 1-2 is enclosed by dotted lines.
Equipment outside the dotted lines are Other Equipment Manufacturer's
units attachable to the system.

     The elements within the system are being designed to permit
field installation of options.  Design considerations for the various
options for the systems are described below.

9020D EXPANSION OPTIONS

7201-02 Computing Element (CE)

A fourth Computing Element may be added to the 9020D configuration
when appropriate field or factory changes are made to the IOCE's,
PAM, TCU's, and System Console.  Internal and/or external cabling
must be installed from the fourth CE to each element with which it
communicates.  Testing and checkout will require maintenance sub-
system and total system hours when this expansion is made in the
field.
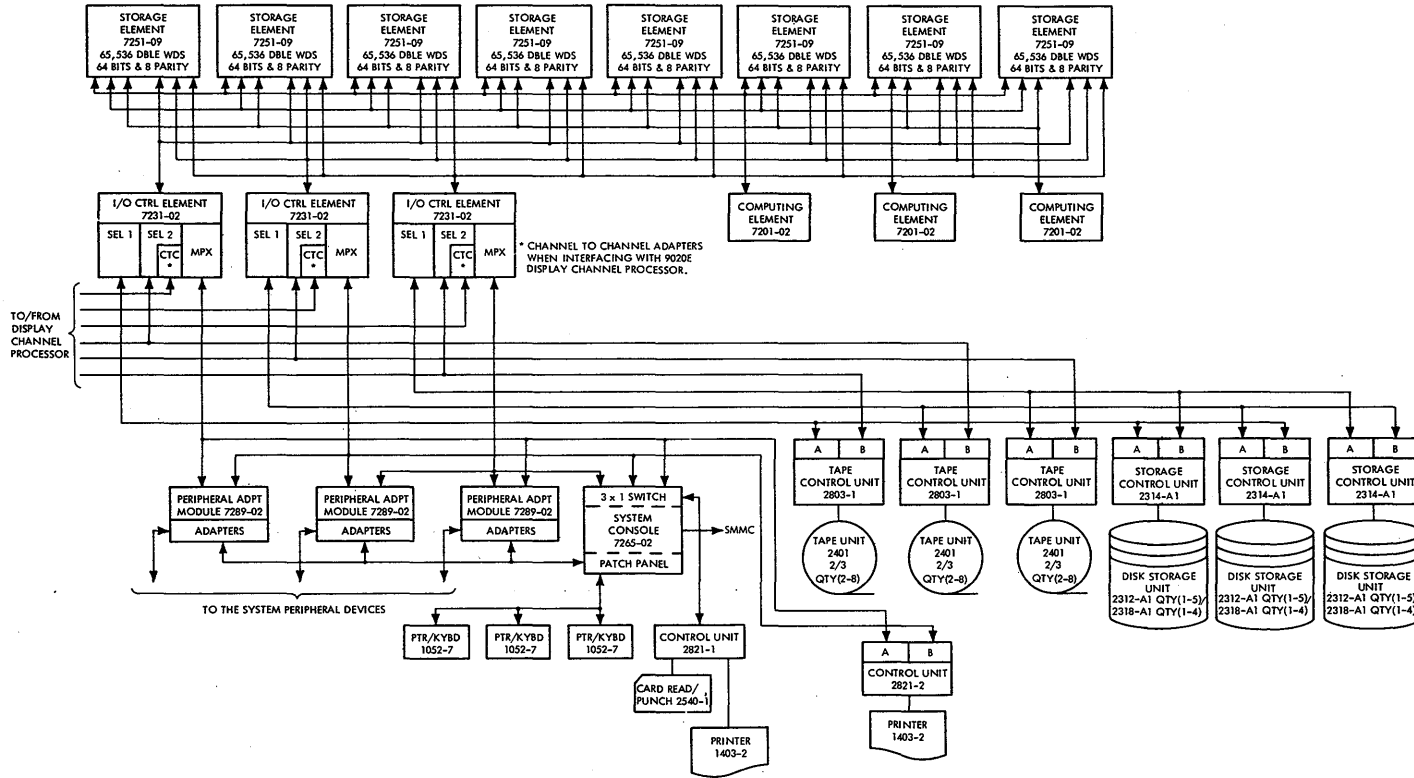
•Figure 1-1  9020D Central Computer Complex

60 PVD'S

DISPLAY GENERATOR (×12)

STORAGE ELEMENT 7251-09 65,536 DBLE WDS 64 BITS & 8 PARITY (×4)

DISPLAY ELEMENT 7289-04 32,768 DBLE WDS 64 BITS & 8 PARITY (×4)

I/O CTRL ELEMENT 7231-02
SEL 1 | SEL 2 CTC * | SEL 3 | MPX

I/O CTRL ELEMENT
SEL 1 | SEL 2 CTC * | SEL 3 | MPX

* CHANNEL TO CHANNEL ADAPTERS WHEN INTERFACING WITH CCC

COMPUTING ELEMENT 7201-02 1052-7 ADAPTER (×3)

TO/FROM CENTRAL COMPUTER COMPLEX

A | B TAPE CONTROL UNIT 2803-1

A | B TAPE CONTROL UNIT 2803-1

TAPE UNIT 2401 2/3 QTY (1)

SWITCH

CONFIGURATION CONSOLE 7265-03

PTR/KYBD 1052-7
PTR/KYBD 1052-7

PATCH PANEL

CONTROL UNIT 2821-1

CARD READ/ PUNCH 2540-1

PRINTER 1403-2

STATUS FROM AND CONFIGURATION CONTROL TO 2701'S

A | B DATA ADAPTER UNIT 2701

A | B DATA ADAPTER UNIT 2701

STATUS AND CONFIGURATION CONTROL → TO AND FROM RKM, DG

SMMC

RADAR KYBD MPLX

RADAR KYBD MPLX

RADAR KYBD MPLX

Figure 1-2  9020E Display Channel Processor

## 7251-09 Storage Element (SE)

A ninth and tenth Storage Element may be added to the basic 9020D configuration. These additions require modifications to the IOCE's and the System Console involving additional logic and internal and external cabling. Internal and/or external cabling must be installed from the ninth and/or tenth storage element to the CE's, IOCE's and existing SE's. Testing and checkout will require maintenance subsystem hours when this expansion is made in the field. Several different maintenance subsystems will be required.

## 2803-01 Tape Control Unit (TCU)

Additional Tape Control Units may be added either in the factory or the field. These additional units would be attached to the Selector Channels of the IOCE's in the manner and within the limitations imposed by Appendix D. The special modifications for attachment of two 9020D System I/O channels under control of the 9020 System. Configuration Control facilities cannot be used by these additional TCU's.

## 7231-02 Input/Output Control Element (IOCE)

Third Selector Channel

The Input/Output Control Element is capable of being expanded to contain three selector channels. A 9020D System with three IOCE's can only increase the total number of channels from nine to eleven (three multiplex and eight selector). IOCE's are designed to accommodate the expansion. The addition of a third selector channel provides the IOCE with increased addressing capability, but no increase in total aggregate data transfer capabilities of the IOCE.

Addition of a selector channel to an IOCE at the factory or at a field location involves adding a significant number of boards, cards, and internal cables followed by appropriate checkouts and confidence tests. Part of the change could be accomplished off-line during low load periods in such a manner that the IOCE could be made available and operational during peak periods. During final cabling and checkout, the IOCE would be made neither available nor recallable.

A channel-to-channel adapter may be added either in the field or the factory to each IOCE of the 9020D. An IOCE with two channel-to-channel adapters would contain one in Selector Channel 1 and one in Selector Channel 2. An IOCE can contain a maximum of two channel-to-channel adapters.

9020E EXPANSION OPTIONS

## 7201-02 Computing Element (CE)

A fourth Computing Element may be added to the basic 9020E configurations. This requires modifications to the Configuration Console, TCU's and IOCE's. Internal and/or external cabling must be installed

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from the fourth CE to each element with which it communicates. When this expansion is done in the field, maintenance subsystem and total system hours will be required for checkout and testing.

### 7251-09 Storage Element (SE)

A fifth Storage Element may be added to the basic 9020E configuration requiring modifications to the IOCE's and Configuration Console. Internal and/or external cabling must be installed from the fifth Storage Element to the CE's, CC, IOCE's and Fourth SE. Checkout and testing can be accomplished using maintenance subsystems hours. Several different maintenance subsystems will be required.

### 7289-04 Display Element (DE)

A fifth Display Element may be added to the basic 9020E configuration. Modifications would be required to the Configuration Console. Internal cabling must be installed to the CE and fourth DE. The internal cabling of the existing DE's must be modified dependent upon the DG configuration attached to the DE's. In general, adding DE's to the system will cause a reassignment of DE/DG interfaces. External cabling from the DE to the CE's, CC and DG's must be installed. The DG cables are GFE. Maintenance subsystem and total system hours would be required for checkout and testing.

### 7231-02 Input/Output Control Element (IOCE)

A third IOCE may be added to the basic 9020E configuration. This will require modifications to the Configuration Console and external cabling to all units with which the IOCE communicates. When expanding to the third IOCE, the total number of system channels must not exceed eleven (eight selector channels and three multiplex channels). Maintenance subsystem and total system hours will be required for checkout and testing when this expansion is done in the field. When expanding to a third IOCE, a third TCU must be added to the configuration for maintenance purposes.

### 7265-03 Configuration Console (CC)

The Configuration Console may be expanded from a 60-console version to a 90-console version. The 60-console version will accommodate the following number of units and elements: 3 CE's, 4 SE's, 4 DE's, 2 IOCE's, 12 DG's, 3 RKM's, 2 DAU's, and 2 TCU's. Whenever the number of any one unit or element type is increased beyond these quantities, the Configuration Console must be expanded to its 90-console version. In its 90-console version, the Configuration Console will accommodate the following number of units and elements: 4 CE's, 5 SE's, 5 DE's, 2 IOCE's, 17 DG's, 5 RKM's, 2 DAU's, and 2 TCU's. Expanding from a 60 to a 90-console version requires significant additional logic hardware and cabling to the added units and/or elements. Maintenance subsystem hours will be required for checkout and testing. Total system hours will be required to test full capability.

The 90 console version of the Configuration Console may be expanded to accommodate a third IOCE and third TCU. This expansion requires the addition of logic and cabling to the added units. Maintenance subsystem hours will be required for checkout and test.

2803-1 Tape Control Unit (TCU)

When expanding the configuration to include a third IOCE a third TCU must be added for maintenance purposes. Adding a third TCU requires installation of external cabling to the IOCE and CE. Subsystem hours are required for checkout and testing.

INTRODUCTION

The IBM 7201-02 Computing Element (CE), is the computational, logical, and control element of both the IBM 9020D, Central Computing Complex (CCC), and the IBM 9020E Display Channel Processor (DCP). As the focal element within both the 9020D and 9020E System, the 7201-02 CE provides the functional duality to establish, organize, and control either multi-element computer system to perform the particular system task.  It contains special facilities for inter-element communications and maintenance which enable it to operate effectively in the FAA environment.

As a computing element, the IBM 7201-02 has a wide range of computational, data processing, and system control capabilities.  It can operate using fixed or variable-field data.  Arithmetic operations are performed with decimal numbers, short or long floating-point numbers, or full or half-word binary numbers.  As a CE, the IBM 7201-02 issues input-output instructions to initiate IOCE data transfers to or from I/O devices and to control I/O processor operations.

GENERAL CHARACTERISTICS

Salient features of the IBM 7201-02 Computing Element (CE) are:

- Architecturally compatible with 9020A:

  1   9020A instruction set

  2   9020A configuration control

- Special instructions for display processing

- Interface with up to three IOCE's

- Interface with up to four DE's (7289-04) and four SE's (7251-09) expandable to five DE's and five SE's (9020E) or interface with up to eight SE's (7251-09) expandable to ten SE's (9020D)

- 200-ns machine cycle

- Battery back-up power

- Read Only Storage (ROS) Control

- Two major working registers:  AB and ST.

- 60-bit parallel adder

- 8-bit serial adder

- 8-byte instruction buffer:   (Q-register)

- 25-register local storage

- Interruption capability

- Houses an optional 1052 Keyboard-Printer Adapter

The CE is organized to process data in 36-bit word form, each word consisting of four bytes of information (byte = eight data bits plus parity bit).  Data are stored in or fetched from Storage Elements (0.8 usec cycle) and Display Elements (0.8 usec cycle) on a double-word basis; controls are provided to selectively update a specific byte within a word for byte oriented operations.  Although the capa-bility to ultimately address up to 16,777,216 byte locations in storage is achieved by using a 24-bit binary address, the basic CE for the 9020D and 9020E Systems is designed to address locations in 10 (65,536 doublewords) Storage Elements or 5 (65,536 double-words) Storage Elements and 5 (32,768 doubleword) Display Elements, respectively.

The CE has a basic internal cycle time of 200-ns.  It's internal logic contains data registers, interconnecting data paths, and sequence controls.  Some of the registers are contained in Local Storage (LS).  The 200-ns transistorized high-speed local storage consists of 16 general purpose (32 bits + 4 parity) and 4 double length (64 bits + 8 parity) floating-point, addressable registers.  One additional register (32 bits + 4 parity) is provided for temp-orary storage during execution of some instructions.

Sequence control is accomplished by microprogram commands (microinstructions) executed from a 200-ns capacitive Read Only Storage (ROS).  Groups of microinstructions are linked to form a microprogram.  A microprogram controls an entire sequence of cycles forming a complete operation, e.g., the execution of an instruction or the transfer of a data word to an IOCE.

The Read Only Storage is not addressable by the standard pro-gram instructions (except by the DIAGNOSE instruction).  Modification of the information contained in this unit can only be made by physically changing the hardware components.

Read Only Storage (ROS) is a 2816-word, 200 nsec. storage.  Each word contains 100 bits; 95 are used for control, 3 for parity, and 2 are used for bit plane testing.  The control bits are grouped into fields up to 10 bits long.  Each field, with the exception of the Next Address Field, is decoded into a set of control lines which control the action of the CE for one cycle.

The Interval Timer is a 32-bit register located in preferential storage location 80.  The timer word is fetched from storage and decremented by a microprogramming-generated constant and written back.

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The interconnecting internal data paths consist primarily of a serial adder, a parallel adder, and two major working registers. The serial adder can function as a binary adder or can perform logical operations such as AND, OR, and EXCLUSIVE OR. The parallel adder is a 60 bit full binary arithmetic unit which is also used for most intra-CE data transfers. The two major working registers serve as operand buffers between main storage and/or local storage and the other CE registers for arithmetic and logical operations.

A CE Control Panel is provided. The main functions of the control panel are to provide the ability to store and display information in storage, in local storage, some registers, part of the program status word (PSW), to allow the operator to reset the system and to perform the initial program load (IPL) sequence.

The controls are divided into a monitor and a maintenance section. The main functions provided in the monitor section are the control and indication of power, the indication of system status, operator to machine communication, and initial program loading.

The controls used for operator intervention are the same as those used for maintenance. These controls include resets, store and display functions, control of instruction execution rates, etc. The controls for marginal checking and special tests are normally used for maintenance in State Zero.

The environment external to 7201-02, which partially characterizes the CE in either the 9020D or 9020E environment, consists of those elements with which it must communicate. The CE, in either system environment, is capable of exercising various degrees of control and supervision over the major system elements, including other 7201-02 Computing Elements. Two-way communication (control and/or data) interfaces are provided between each 7201-02 CE and each of the following:

9020D CCC System

IBM 7201-02 Computing Element (CE)

IBM 7251-09 Storage Element (SE)

IBM 7231-02 Input/Output Control Element (IOCE)

IBM 7265-02 System Console (SC)

IBM 7289-02 Peripheral Adapter Module (PAM)

IBM 2803-01 Tape Control Unit (TCU)

IBM 2314-A1 Storage Control Unit (SCU)

9020E DCP System

IBM 7201-02 Computing Element (CE)

IBM 7251-09 Storage Element (SE)

IBM 7289-04 Display Element (DE)

IBM 7231-02 Input/Output Control Element (IOCE)

IBM 7265-03 Configuration Console (CC)

IBM 2803-01 Tape Control Unit (TCU)

IBM 2701-01 Data Adapter Unit (DAU)*

*Two-way communication via the IOCE and Configuration Console.


Unless otherwise stated, the following discussion of the IBM 7201-02 CE is applicable in either the CCC or DCP environment.

## FUNCTIONAL CHARACTERISTICS

The IBM 7201-02 Computing Element (CE) performs arithmetic, logical, and control instructions specified by a stored program. The CE (Figure 2-1) contains facilities for addressing the SE and DE, processing fixed-point, floating-point, and decimal arithmetic, operating on logical data, sequencing instructions in the desired order, control of I/O processor operations, and initiating I/O operations. Also provided are facilities for character-handling, processing of fixed-length and variable-field-length (VFL) data, indexing, and indirect addressing.
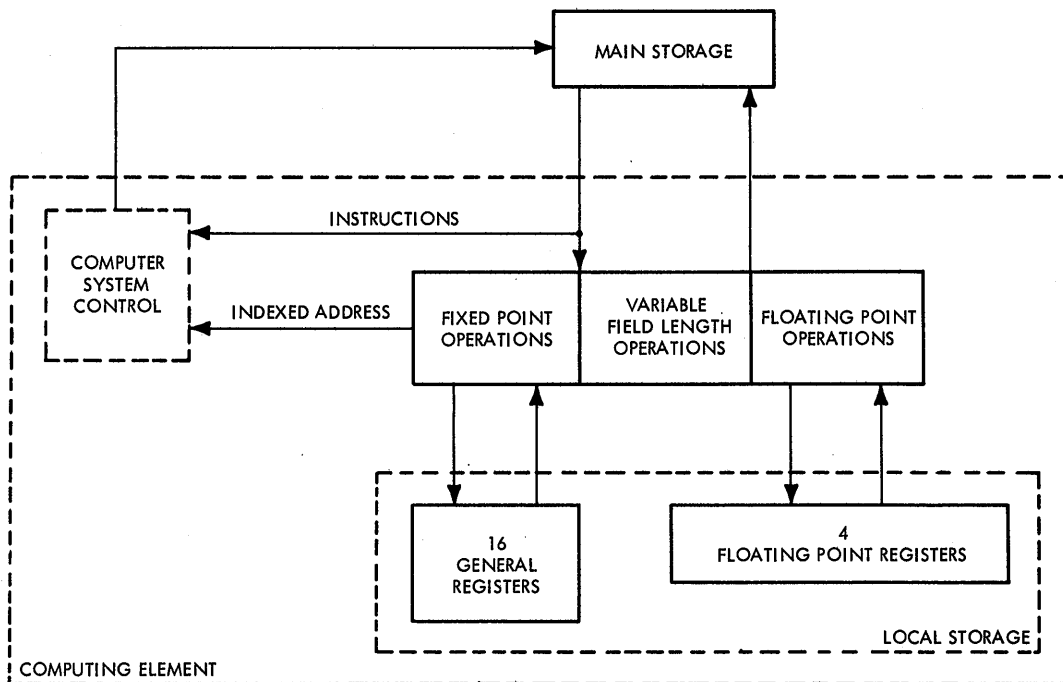


Figure 2-1. Computing Element Block Diagram

Functionally, the CE can be divided into four major sections: control; storage control interface (SCI); instruction fetching; and instruction execution.

## Control Section

The basic CE clock cycle period is 200 ns. A clock signal generator provides a 5-MHz symmetrical (100-ns clock and 100-ns not-clock portions) signal. Clock distribution logic distributes and synchronizes the clock signals to the logic gates, and stops distribution of clock signals to most of the CE processing logic upon detection of a machine check during certain operations. To provide additional time for CE logic functions, the symmetrical clock signal is modified to give a 5-MHz unsymmetrical (80-ns clock and 120-ns not clock portions) signal.

A significant feature of the CE is Read Only Storage (ROS) which is used to control operations. The ROS contains a permanently recorded microprogram holding information that remains fixed during machine operations. The information is in the form of 100-bit words, each word containing a unique, predetermined bit pattern. When decoded, the bits control gates to route data in the CE. Word access time is approximately 95-ns. The information can be read out as required, but a physical modification is necessary to change the stored information. In general, a control word is read out from ROS at the end of each machine cycle (200-ns), and controls a portion of the CE during the following machine cycle. Each ROS word contains the address of the ROS word to control the CE during the following cycle. The number of control words (and machine cycles) required to perform a particular operation may vary because both the individual functions and the address of the next ROS word are modifiable by the (1) operation in progress, (2) data or control bit configuration, and (3) detection of interruptions or exceptional conditions. Used as a control device, ROS eliminates the need for most complex instruction decoders and sequencing networks.

The Program Status Word (PSW), a doubleword, contains the information required for proper program execution. Primarily, the PSW controls instruction sequencing and holds the system status in relation to the program being executed. By storing the PSW, the program can preserve the status of the CE for subsequent analysis, By loading a new PSW or part of a PSW, the mode of operation of the CE may be changed.

## Storage Control Interface (SCI)

The SCI controls the transfer of addresses (via the storage address bus) and data (via the storage data bus in/out) between the CE and the SE's or DE's. When the CE requires access to an SE or DE a request is sent to the SCI. Upon receipt, the SCI determines the SE or DE to be accessed, develops the address, and generates the appropriate select pulse. Since the SE's and DE's can serve multiple users, a Storage Switch Unit (SSU) contained in each SE/DE receives the select pulses and grants the priorities.

After issuing the select, the SCI stops the CE and waits for an accept pulse from the SE or DE, which indicates to the SCI that it's request has been given priority. The SCI then allows the CE to resume processing. Should an accept not be received within 25 msec (nominal), the SCI will force a dummy storage cycle, restart the CE, and cause a machine check (Storage Timeout). Thus, the primary function of the SCI is to provide communication between the CE and the SE's or DE's.

## Instruction Fetching

An instruction buffer, the Q-Register, provides buffering for eight instruction bytes (four halfwords), thus reducing the number of storage requests that must be made to fetch instructions from main storage. The R-Register is associated with the Q-Register. It holds the halfword (two bytes) containing the Op Code received from the Q-Register, of the instruction to be executed next. As a result, the R-Register allows overlapping of instruction fetching while containing the Op Code of the instruction being presently executed. The instruction Op Code is used to address the ROS, which provides the required microprogram for execution of a specific instruction.

## Instruction Execution

The CE operates on a basic internal cycle time of 200-ns. The data flow (Figure 2-2) utilizes two major working registers (ST and AB) to give increased speed and simplified implementation of the instruction set. The 6- bit parallel adder is the focal point for most data transfers, and facilitates handling the full long fraction in floating-point operations. An 8-bit serial by byte adder provides simultaneous execution of the floating-point exponent as the fraction is operated on in the parallel adder, and has the capability of executing decimal arithmetic and Variable Field Length (VFL) instructions.

The CE extracts from the doubleword fetched from main storage, the bytes on which it will operate. Thus, storage accesses are not required for every byte. As a result, processing speed is increased and system performance is improved. Data may be stored, however, on a byte basis; any number and combination of bytes up to 8 (doubleword) can be stored in one storage cycle. Addresses for data are formulated in the arithmetic section of the CE and then placed in the D-Register for addressing storage.

The CE incorporates a local storage of 25, word-length, registers: 16 word-length general-purpose registers for fixed-point operations; 4 doubleword length (8 word-length) floating-point registers, and an additional word-length register called the Local Storage Working Register, for miscellaneous operations. Local storage serves two functions: (1) it is used in the generation of effective operand addresses in main storage and (2) it holds operands and intermediate results of data operations, thus eliminating the need for special-purpose registers, such as accumulators. Local storage employs nondestructive readout, eliminating the need for regeneration, and operates on a 200-ns cycle with an 80-ns access time.

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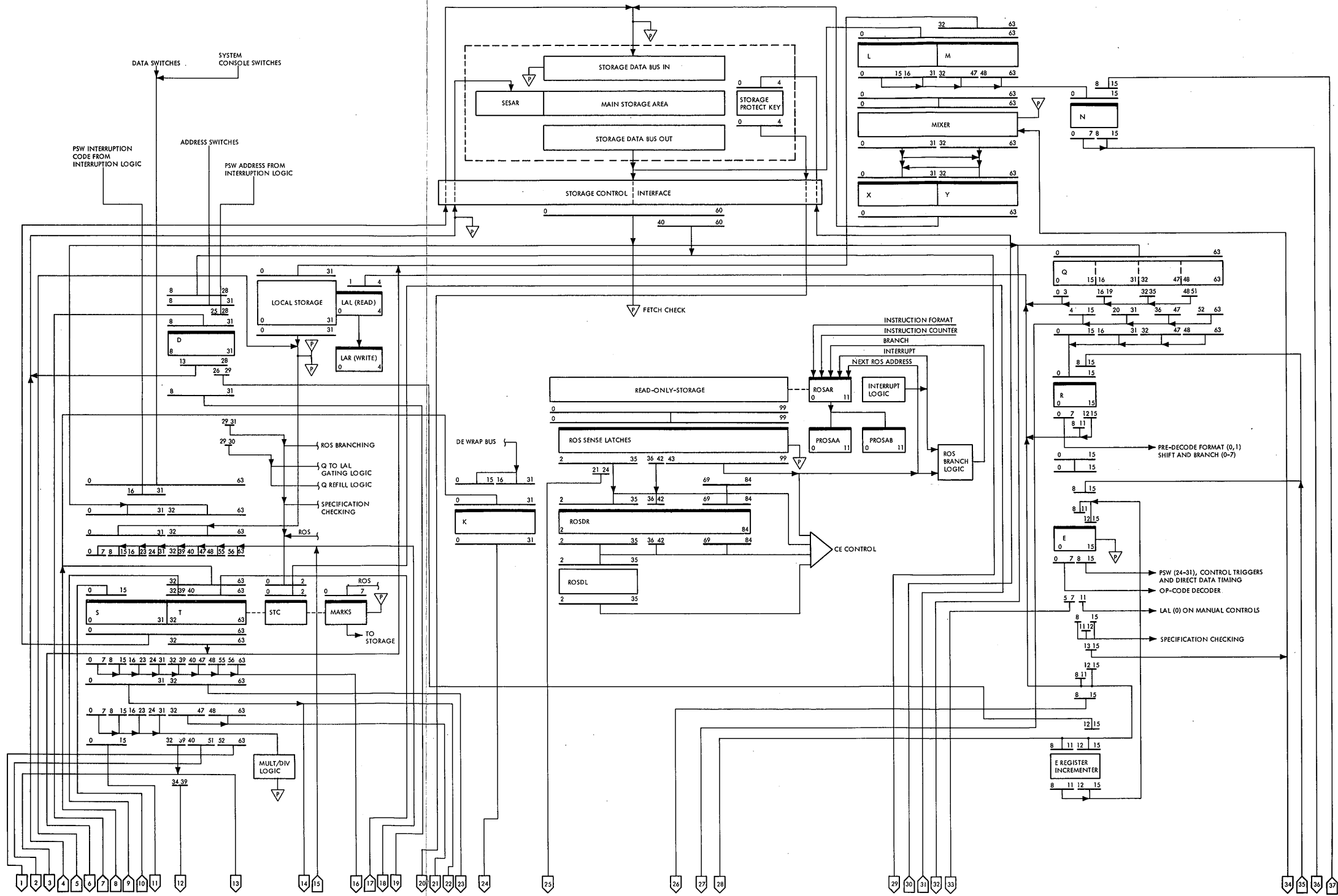
●Figure 2-2.  CE Data Flow (Sheet 1 of 2)
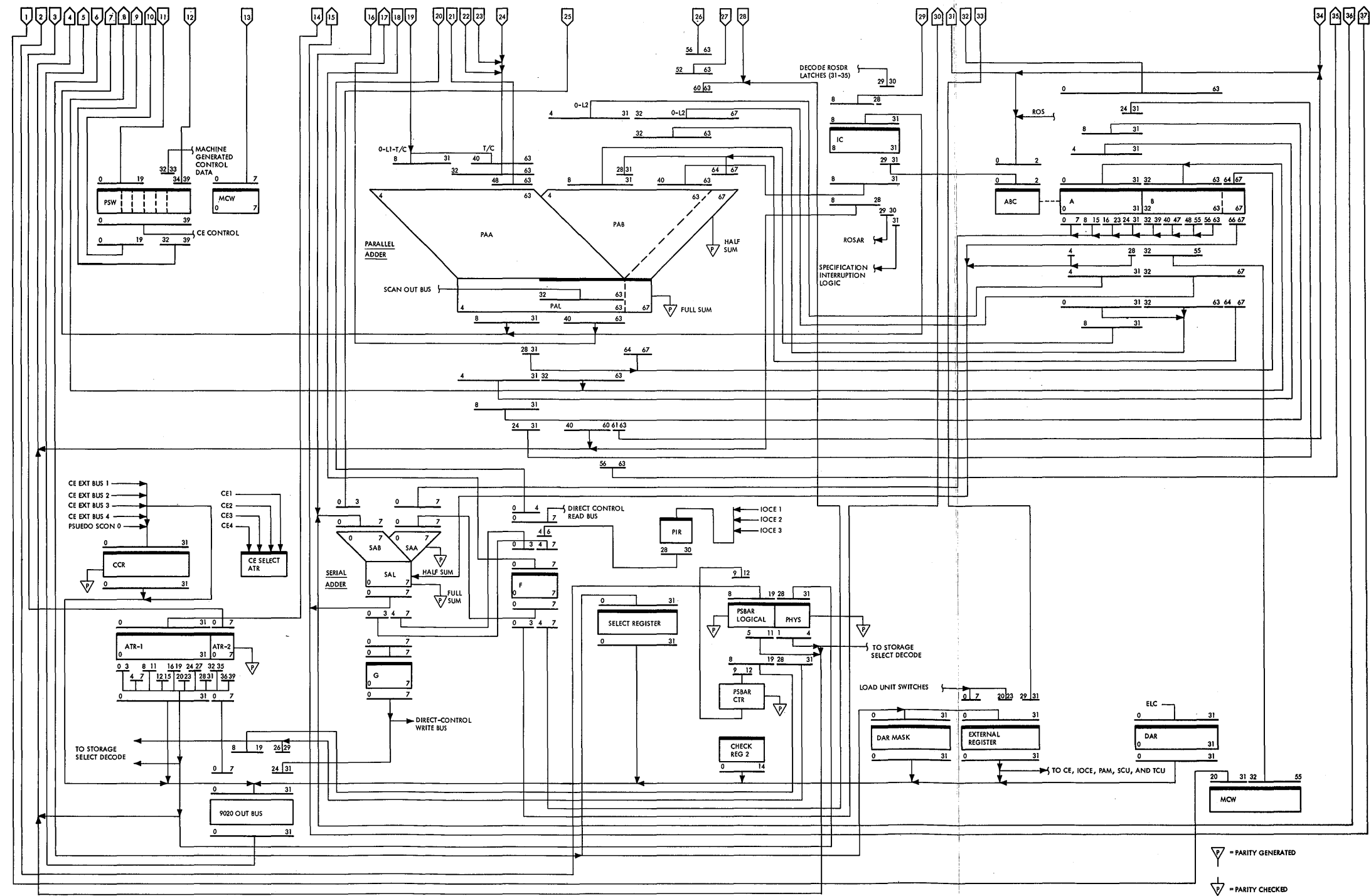
•Figure 2-2. CE Data Flow (Sheet 2 of 2)

An interruption capability permits the CE to change mode of operation automatically as a result of conditions arising outside the system, in I/O units, or in other CE's. An interruption switches the CE from one program to another by changing the instruction address (this is done by the automatic fetching of a new PSW). The interruption cause and all essential machine status information is stored for analysis in an old program status word. This information is available to the system as required. When a different program is requested, the status information about the current program is stored temporarily and is retrieved when that program is to be continued.

This facility allows interrupted programs to resume at the point of interruption without the loss of control conditions.

Direct control facilities (utilizing the F and G Registers) enable direct transferring of a single byte of information between the CE and any other CE. Also, control signals initiated from a CE can be passed to another CE or IOCE to initiate a particular action.

In the CE, checking is facilitated by providing a parity bit for each byte of data. Odd parity is maintained. A parity check is made on data transferred to and from main storage. Most data transfers within the CE are made via the parallel adder, in which the parity of each byte of the operand is checked. The parity of the sum, which is generated logically within the adder, is checked against the latched sum. A parity check is also made on data transferred from Local Storage.

As programs are executed, they are checked for correct instructions and data. This monitoring action identifies and separates program errors and machine errors. Since each type of error causes a unique interruption, program errors cannot create machine checks (errors).

The CE also incorporates an IOCE interface that is used to initiate I/O operations, respond to I/O interrupts, and to control IOCE processing.

INTERNAL OPERATIONS

Instruction Execution

The function and timing of each of the instructions executed by the IBM 7201-02 CE is described in the IBM 9020D/E System Principles of Operation manual. This section describes the procedure used by the CE to execute those instructions.

The initial phase of instruction processing provides for fetching of instructions from main storage, and for placing the operands specified by the up-coming instruction into the desired data flow registers. Instruction fetching is under ROS and hardware control. The various initializing actions are similar to many instructions and are therefore controlled by a common ROS microprogram. To increase the speed of instruction processing, conventional hardware

is also used to provide additional control of several I-Fetch routines. This I-Fetch support hardware allows the CE to:

1. Initiate requests for new instructions.

2. Increment the instruction counter (IC).

3. Ingate new instructions into the CE at the correct time.

## Instruction Fetching

When the CE establishes a need for more instructions, a request is made for the next doubleword in main storage and the Instruction Counter (IC) is gated to the storage address bus. Since instructions can vary from 1 to 3 halfwords in length, as many as 4 complete instructions (RR format) or as few as 1-1/3 instructions (SS format) can enter the CE. Instructions received are gated into the instruction buffer (Q Register) for buffering and are sequentially selected for processing by the CE.

Two additional registers are associated with the instruction process; the R-(intermediate register) and the E-(execution register). The R-Register contains the first halfword of the next instruction to be executed and allows for prefetching of the operands. The E-Register contains the first halfword of the instruction being executed.

## Interruption Processing

When the execution phase of an instruction is finished, and before the program branches to the appropriate I-Fetch routine for the next instruction, the interrupt logic examines various triggers to determine whether an interruption or exceptional condition has arisen. If it has, a branch micro-order blocks the I-Fetch and forces a branch address into the ROS address register (ROSAR). (Interruptions allow the CE to change its mode of operation as a result of conditions external to the system, in I/O units, or in the CE, while exceptional conditions are unusual conditions that require special action, e.g., Interval Timer Update, manual control wait, etc.)

## External Interruption Handling

External interruption provides a means by which the CE responds to signals from the timer, the interrupt key, external units, and in certain circumstances from itself. A request for an external interruption may occur at any time, and requests from different sources may occur at the same time. Requests are preserved until honored by the CE. All pending requests are presented simultaneously when an external interruption occurs. Each request is presented only once. When several requests from one source are made before the interruption is taken, only one interruption occurs. Details of external interruption handling are contained in the IBM 9020D/E System Principles of Operation manual.

## Classes of CE Instructions

The following paragraphs discuss general CE operational responses
to the different classes of CE instructions.  Instruction times are
discussed in the IBM 9020D/E Principles of Operation manual.

### Branch Instructions

A departure from the normal instruction sequence occurs when branch-
ing is performed.  Depending upon the format and the instruction,
branching may be conditional or unconditional.  On conditional branches,
branching is always considered to be successful unless proven other-
wise.  If the branch is found to be unsuccessful, the instruction
address from the D register (branch address) is ignored.  If
successful, the branch address is used and the storage request
issued per the IC during I-Fetch is blocked.

### Status Switching Instructions

There is a set of privileged instructions provided to switch the
status of the CE from the Supervisor to the problem state, or vice
versa, to set the various masks in the PSW and set and load the
Storage Protection Keys.

### Fixed-Point Instructions

Fixed-Point arithmetic operations are, in general, executed using the
parallel adder which obtains the operands from the ST and AB regis-
ters.  Condition codes are generally set per the result noted in the
parallel adder latch.

### Shift Instructions

Left shifting is performed by one (L1), two (L2), and four (L4) bit
shifts, while right shifting is performed with a combination of four
bit right shifts (R4) plus L1, L2, and L4.  The operand is initially
in the ST register with the shift amount in the D and E register.

### Floating-Point Instructions

All of the floating-point instructions exist in four versions:  short
and long factors, and RR and RX format.  Data Flow is divided into
two paths:  (1) the fraction path through the parallel adder and (2),
the sign and characteristic path from ST or AB through the serial
adder to the F Register.

### Variable-Field Length Instructions

Variable-field length instructions are always in the SS format and
operate on data which may range from 1 to 256 bytes in length.  In
general, the operands are held in the AB and ST registers with sub-
sequent sequential byte gating to the serial adder for the arithmetic
operation (in excess -6 arithmetic), or the logical operation.

Multiprocessing Instructions

The 9020D/E combines Computing Elements, IOCE's, Storage Elements and Display Elements into a multi-processing environment which requires multiprocessor type instructions for coordination and control. These instructions are described in detail in the IBM 9020D/E Principles of Operation manual, Chapter 8.

Display Processing Instructions

The display processing instructions utilized within the 9020E DCP environment are described in detail in the IBM 9020D/E Principles of Operation manual, Chapter 8.

I/O and I/O Processor Operations

The IBM 9020D/E System consists of up to three Input/Output Control Elements (IOCE), each of which will operate as an I/O processor while controlling one multiplexor Channel and two Selector Channels.*   (See 9020D/E Principles of Operating Appendix H).  All I/O control communications with the computing elements (CE) are through the IOCE's except for configuration control.

        The I/O or I/O processor operations to be performed, interruption requests, system mask, channel and unit addresses, condition codes and various other control functions are transmitted across the IOCE-CE interface.  Only control information is transferred across this interface.

        A CE may have several IOCE's on line at one time.  The communication between a CE and the IOCE's would be in an interleaved manner allowing an operation between one CE and only one IOCE channel or IOCE processor at a given instant.  An IOCE may be under control of only one CE at a time.

        I/O instructions are available to IBM 9020D/E Systems for execution by the Ce.  These instructions are:

        START I/O

        TEST CHANNEL

        TEST I/O

        HALT I/O

        SET PCI

        START I/O PROCESSOR

These instructions are defined in the IBM 9020D/E System Principles of Operation manual.

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*   Two IOCE's within a 9020D/E System can have, optionally, a third selector channel.

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In addition, control lines cause the IOCE to perform special functions. These lines are:

| | | |
|---|---|---|
| IPL | FLT Backspace | Write Direct Processor |
| Logout | Reconfigure Select | Start |
| Permit I/O Interruption | SATR Select | Write Direct Processor |
| Permit MC Interruption | 360 Mode (IOCE-1 | Stop |
| FLT Load | only) | Write Direct Processor |
| | | Interrupt |

## Computing Element Control Panel

The Computing Element Control Panel (Figure 2-4) contains the switches and indicators necessary to operate and control a computing subsystem. A subsystem is considered to consist of a combination of CE's, SE's, DE's (E System only), IOCE's control units, and I/O devices.

These switches and indicators may be used to control an active system as backup for the Systems Console or Configuration Console when it is not operating. These system functions are activated by turning on the System Interlock Switch on the CE control panel.

Computing Element States

Each computing element with power on is in one of four states, and these states are represented by indicators on the CE Control Panel. In addition to four indicators, a Test switch is provided which is functional only in the Zero State. The states are defined by setting the state bits (S0, S1) in the CCR. The state bits and the System Interlock switch control the effect of all manual switches on the CE.

CE controls are divided into two sections - the monitor section and the maintenance section.

Monitor Section

This section of the CE Control Panel contains those operator controls that are required by the operator when the CE is operating under program control.

The main functions which are provided at the monitor section are the control and indication of power, the indication of element status, operator to machine communication, and initial program loading. This section is located at the lower half of the panel, except for the Element Master Power Off pull switch which is at the upper right corner of the panel.

Maintenance Section

This section of the CE control panel contains those controls intended primarily for maintenance use, although in some cases an overlap exists with the monitor controls. These controls fall logically into two categories: maintenance control, and marginal check and voltage display control.

DESIGN DETAILS

The IBM 7201-02 data flow path (Figure 2-2) utilizes two major working registers (ST and AB) to give increased speed and simplified implementation of the instruction set. A 60-bit parallel adder is the focal point for most data transfers and facilitates handling the full long fraction in floating point operations. A 8-bit serial adder provides simultaneous execution of the floating point exponent as the fraction is operated on in the parallel adder and has the capability of executing decimal arithmetic and variable field length instructions.

The CE's data flow diagram (Figure 2-2) can be divided into four basic parts: arithmetic and logical units; registers and counters; storage control interface; and ROS. The arithmetic and logical units are responsible for performing all arithmetic and logical (OR, AND, and EXCLUSIVE OR) functions. Registers and counters are used for data flow and control. Storage Control Interface's (SCI) primary responsibility is to provide communication between the CE and SE/DE. Read Only Storage controls basic CE operation.

The following paragraphs discuss the functional components of the CE's data flow diagram.

Arithmetic and Logical Unit

The arithmetic and logical unit can process binary integers and floating-point fractions of fixed length, decimal integers of variable length, and logical information of either fixed or variable length.

Arithmetic and logical operations performed by the CE fall into four classes: fixed-point arithmetic, decimal arithmetic, floating-point arithmetic and logical operations. These classes differ in the data formats used, in the registers involved, in the operations which are provided, and in the way the field length is stated.

Serial Adder - The serial adder is an 8-bit (plus 1 parity) adder capable of performing both binary and decimal arithmetic operations as well as logical operations such as AND, OR, and EXCLUSIVE OR. The serial adder performs sign insertions and correction, zero and non-zero detection, and parity adjustments. Two byte sources (ST and AB or F Registers) may be selected simultaneously for logical or arithmetic operations by the serial adder.

For binary operations, the adder functions as a straight 8-bit (plus parity) full-binary adder, processing bytes from either the ST register or N-Register or bits 21-24 of ROS Word (B side input) and either AB or F Register (A side input).

For decimal operations, each byte of data from the ST, AB or F-Register is treated as two individual 4-bit groups which are processed with excess 6 arithmetic.

Output from the serial adder is through the Serial Adder Latch (SAL) to the ST, F, N, or G-Register.

Parallel Adder - The parallel adder is a 60-bit (plus parity) full-binary arithmetic unit. In addition to arithmetic functions, the parallel adder performs certain logical operations and is involved in most intra-CE data transfers.

Immediate left (L4) and right (R4) shifting capabilities are available at the adder output, with parity adjusted accordingly. A 4-position adder extension is provided to retain low order significance during certain right-shift operations.

Inputs to the adder are from the ST, AB, D, Q, K, IC or E registers and the serial adder. Output from the parallel adder is through the Parallel Adder Latch (PAL) to storage, ST, AB, D, K, IC, E or R registers.

## Registers and Counters

AB Register- The AB Register is a 64-bit (plus 8 parity) trigger register that functions as a working register and also as a buffer for doubleword operands received from storage.

The AB Register is logically divided into two 32-bit (plus 4 parity) registers, A and B. A four-position extension (bits 64-67) provides for retention of low-order significance during certain arithmetic and shifting operations.

Inputs to the AB Register are from storage (via SDBO) and the parallel adder.

Outputs from the AB register are to the serial adder (e.g., for VFL operations), the parallel adder and MCW register. An L2 shift function is provided through the outgating.

ST Register- The ST Register is a 64-bit (plus 8 parity) trigger register that functions as an operand buffer between main storage, Local Storage (LS), and other registers as well as a working register for arithmetic and logical operations.

The ST Register is logically divided into two 32-bit (plus 4 parity) registers (S and T), which serve as working registers for all operations and also as a final assembly area for resultant data to be entered in either LS (from T) or main storage (from S and T).

Inputs to the ST Register are from main storage, LS, parallel adder serial adder, PSW Register, Data Switches, and the special 9020 registers.

Outputs from the ST Register are to main and display storage, LS, PSW Register, serial adder, parallel adder, multiply/divide logic and some special purpose registers (External, DAR, etc.).

AB and ST Counter-  Both the AB and ST have 3-position byte counters (ABC and STC) to provide selective byte outgating.

PSW Register-  The Program Status Word (PSW) Register contains detailed information pertaining to the particular mode in which the CE is operating.

        Input to the PSW Register is from both the ST Register and interruption control logic.  Outgating is to the ST Register and CE control circuitry.

Q-Register-  The Q-Register is a 64 bit (plus 8 parity) trigger register that buffers all instructions entering the CE from main storage and provides for overlap of I-Fetch and instruction execution.

        The Q-Register is loaded directly from the Storage Data Bus Out (SDBO), with outgating provided to the Local Storage Address Registers (LAR Read and LAR Write), the R-Register (op codes), and the parallel adder (for "effective address" computation).

E-Register-  The E-Register is a halfword (16 bits plus 2 parity) trigger register that contains the first halfword (op code) of the instruction being executed.

        The input to the E-register is gated from the R-register and parallel adder under ROS control.

        The first byte (op code) is gated to the op code decoder and the second byte is gated to either LAR, E-register increment (e. g., reducing length fields in logical VFL operations), or is used to generate direct control operations.

E-Register Incrementer - The E-Register incrementer consists of 2 four position incrementers which can either increment or decrement 4 bit fields by 1.  The input to the E-register incrementer is from the D-register and the E-register.  The output of the incrementer is to the E-register.

Instruction Counter-  The Instruction Counter (IC) is a 24 bit register used primarily for accessing the next sequential double-word of instructions from main storage.  Source operand data are also addressed by the IC during VFL instructions.

        Inputs to the IC are from the parallel adder, or SDBO.

        Outputs from the IC are to the parallel adder, Storage Address Bus (SAB), AB counter, ROSAR, or Specification interruption logic.

D-Register-  The D-Register is a 24 bit (plus 3 parity) register that functions as a main storage address register during manual control, branching, and certain arithmetic operations, and as a channel and unit address register during I/O operations.

        Inputs to the D-register are from the parallel adder, the Address switches or SDBO.

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Outputs from the D-register are to the STC-register, E-register, parallel adder, Storage Control Interface (SCI), and E-register incrementer.

Mark Triggers- Eight mark triggers indicate to the main storage area which bytes of doubleword data placed on the Storage Data Bus In (SDBI) are to be entered into storage. This provides a means of storing CE data into main storage on a byte basis.

F-Register- The F-Register is an eight bit (plus 1 parity) register used in certain arithmetic, logical and data-transfer operations.

G-Register- The G-Register is an eight-bit register used for buffering data between the CE and a remote system unit for direct-control operations.

N-Register- The N-Register is a 16 bit (plus 2 parity) register used for the special display instructions.

LM Register- The LM register is a 64 bit (plus 8 parity) register used during the special display instructions.

Inputs to the LM-register are from storage (SDBO) or from the T-register (2nd word only).

Outputs from the LM register are to the XY register via the Mixer, and to the N register.

XY-Register- The XY-register is a 64 bit (plus 8 parity) register used during the special display instructions.

Input to the XY-register is from the LM-register via the mixer.

Output from the XY-register is to storage via the SDBI.

Mixer - The Mixer provides several special display instruction formatting sequences under control of bits 13-15 of the E-Register.

Input to the Mixer is from the LM-Register.

The output of the Mixer is to the XY-Register.

K-Register- The K-register is a 32-bit (plus 4 parity) register which is used as an A side input to the parallel adder and is also used for DE wrap test input .

Local Storage Address Registers (LAR and LAL) - Two five bit LAR's (read and write) are used in selecting the 25 individual local store registers.

Inputs to LAR are from the Q, R, or E register as well as directly from the Read Only Storage Data Register (ROSDR).

Local Storage Registers - The local storage registers are a bank of 16 general purpose registers, four double length floating-point registers, and one working register that is used within the CE and not available to the programmer. These 25 registers are 32 bits (plus four parity bits) in length.

R-Register- The R-register, a halfword (plus 2 parity bits) register, provides intermediate buffering of op-code bytes between the Q-, and E- registers.

ROS Data Register - The Read Only Storage Data Register holds fields A through H, M, N, P, and Q of the ROS word for use in the next machine cycle. Fields H (local storage control), M, N, P, and Q (adder control) are decoded directly from ROSDR. Fields A through G are further delayed via the ROSDR latches for register ingating.

ROS Data Latches- The read only storage data latches store portions of a ROS word for use early in the next machine cycle.

ROS Address Register (ROSAR) - The ROSAR is a 12 bit register which contains the address of the ROS word presently being executed.

Inputs to the ROSAR are the Next Address (NA) field of the ROS Sense Latches and several branching condition lines.

Output from the ROSAR goes to the Previous ROS Address Registers (A and B) and is used to address ROS.

Previous ROS Address Register (A and B) - The PROSAA and PROSAB are 12 bit registers which contain (alternately) the address of the previous and previous-previous ROS words executed.

Maintenance Control Word Register - The MCW Register is loaded with the specified MCW during execution of a Diagnose instruction.

Inputs to the MCW are from the T and B-registers.

The Outputs from the MCW register are used to provide the various MCW functions; e.g., count fields, control lines, ROS address, etc.

External Register- A 32-bit register that provides the unit and channel address as well as the coded I/O operation for FLT, IPL, and normal I/O instructions, and I/O processor operations. This register provides the storage for data being routed to other system components.

Configuration Control Register (CCR)- A 32-bit register used to define the intercommunication between elements in a system. It is loaded with the configuration mask bits during a SCON instruction.

Diagnose Accessible Register (DAR) - This 32-bit position register is filled by external interruption requests and is read and reset

only by the DIAGNOSE instruction. It contains a group of external interruption requests that are too numerous to be individually stored in the PSW. If any of the DAR bits are set and are not masked off by the DAR mask or bit 7 of the PSW, an interruption is taken. The interruption causes bit 31 of the PSW to be set.

Select Register (SR) - A 32 bit register that defines the elements to be configured by the SCON operation or a SATR.

DAR Mask Register - DAR Mask Register (loadable by a diagnose kernel) is used to mask off the external interruption requests stored in the DAR. In this case, a bit is required in a position of the DAR mask, corresponding to the bit in the DAR, for the interruption to be allowed.

PSBAR - Two Preferential Storage Base Address Registers allow the relocation of the CE's preferential storage area (1024 Words) to any 1024 word block in main storage. The PSBAR function is implemented in two registers: Logical PSBAR (11 bits) and Physical PSBAR (4 bits). Logical PSBAR is loaded when the Load Preferential Storage Base Address (LPSB) instruction is executed. Bits 9-12 of the new contents are translated via the Address Translation Register and placed in the physical PSBAR. The output at the combined PSBAR's (9-12 from physical PSBAR and 13-19 from logical PSBAR) supplies the high-order portion of the storage address. These bits are OR'd into the high order bits of the address whenever the PSBAR zero detect logic finds 12 high order zeros in the logical storage address. Both PSBAR registers are parity checked and logged out as shown in Figure 2-3.

Address Translation Register (ATR) - The ATR is comprised of two registers: a 32-bit (plus parity) register (ATR-1) and an eight bit (plus parity) register ATR-2. They may be logically considered as one 40 bit register. The ATR provides dynamic address translation of logical address blocks into selectable physical address blocks.

Address translation takes place for both normal and PSA storage references. ATR is parity checked and logged out as shown in Figure 2-3. A description of the Address Translation feature is presented later.

PIR Register - This is a three bit register to preserve external interrupt requests from an I/O processor.

Interval Timer

The interval timer is a 32 bit register located in preferential storage location 80. Approximately every 16.7 ms, the timer word is fetched from storage, decremented, and written back under microprogram control. If the decrementing causes a transition from a positive value to a negative value, the timer bit in the external interrupt register is turned on.

## Storage Control Interface

The Storage Control Interface (SCI) controls the flow of data between the CE and storage.

Storage interleaving is provided via the SCI by treating the even storage addresses and the odd storage addresses as separate storage elements, with each storage element having its own storage cycle.

Although CE processing is overlapped with storage requests and data transfer operations, the degree of overlap is limited. A group of CE sequences is started in the SCI to stop the CE clock in the event that the addressed storage unit is busy, in which case the requested data will not be available to the CE on the particular cycle specified by the request.

## Address Translation Feature

The address translation feature allows a span of logical main storage addresses and/or logical display storage addresses (on appropriate boundaries) to be physically located within any main storage or display element (respectively) configured to the using element. Address relocation is controlled in the CE by two internal registers, Address Translation Registers (ATR) 1 and 2. These registers, which may be considered as one 40 bit (plus parity) register, are loaded by the Set Address Translator (SATR) instruction. Each half byte (four data bits) in the ATR represents a translator position.

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A 7201-02 CE used within a CCC environment can access up to 10 main storage elements. Consequently, all ATR positions are used to effect main storage address translation.

The first position in the ATR represents a translator register for the logical range of addresses from 0 to 524K bytes, the second from 524K to 1,048K bytes, etc. Each position can contain a hexadecimal digit from 1 through A to represent a physical main storage element (1 through 10). The high order bits of a logical address (bits 9-12), which identify a logical block of 524K bytes, are decoded to select one logical position of the ATR. The contents of the selected ATR position will represent the high order bits at the physical address (or physical element) which is currently assigned to the respective logical address block which is being translated. The physical address block representation will be subsequently used in lieu of the logical address block.

For example, if the third position (bits 8-11) of ATR 1 contains the hexadecimal digit 6, then the logical addresses falling within the third block of 524K bytes will be translated to select physical SE6. Translation of an address includes issuing an access request to the selected SE and modifying bits 9-12 of the address. In the Load PSBAR instruction, translation also takes place, resulting

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**BIT POSITIONS IN MAIN STORAGE**

| PSA LOC-ATION | PSA WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 128 | 32 | F REG P 0-7 | D REG P 8-15 | P 16-23 | P 24-31 | | | | | Q REG P 0-7 | P 8-15 | P 16-23 | P 24-31 | P 32-39 | P 40-47 | P 48-55 | P 56-63 | DAR MASK P 0-7 | P 8-15 | P 16-23 | P 24-31 | | | | | | | | | | | | | PARITY FOR F, D, Q AND DAR MASK |
| 132 | 33 | SELECT REG P 0-7 | P 8-15 | P 16-23 | P 24-31 | | | | | ST REGISTER P 0-7 | P 8-15 | P 16-23 | P 24-31 | P 32-39 | P 40-47 | P 48-55 | P 56-63 | CCR P 0-7 | P 8-15 | P 16-23 | P 24-31 | | | | | | | | | | | | | PARITY FOR SR, K, ST AND CCR |
| 136 | 34 | CE SEL SATR 1 | | G REG P 0-7 | P 32-39 | ATR P 0-7 | P 8-15 | P 16-23 | P 24-31 | IC REQ | RPT INSTR ADJ | INSTR STEP TGR | DISABLE INTER-LEAVE | STAT TGR A | I FETCH 1 TGR | IL NOT AVAIL | EXT INTRPT CE4 WDD 28 | MCW RTP 0 | ADDR SEQ 0 | FLT CLOCK 0 | | MARK P 0-7 | ST REG P 32-39 | AB REG P 64-67 | PADDL P 64-67 | | | | | | | | | |
| 140 | 35 | EXTERNAL TRIGGERS PERMIT IOCE 2 | LOGOUT IOCE 1 | LOGOUT IOCE 2 | LOGOUT IOCE 3 | | | | | AB REGISTER P 0-7 | P 8-15 | P 16-23 | P 24-31 | P 32-39 | P 40-47 | P 48-55 | P 56-63 | R REG P 0-7 | P 8-15 | E REG P 0-7 | P 8-15 | | | | | | | | | | | | | |
| 144 | 36 | CE SEL SATR 2 | 3 | 4 | TIME CLOCK STEP | BCU OSC INH | SELECT IOCE 1 | 2 | 3 | IOCE MC REQ | INTRPT GATE TGR | | | EXTERNAL REG P 0-7 | P 8-15 | P 16-23 | P 24-31 | G REG (WRITE DIRECT) 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 32 | ATR-2 33 | 34 | 35 | 36 | 37 | 38 | 39 | G REG, ATR-2 |
| 148 | 37 | PAM/RCU 1/1 | 2/2 | 3/ | TCU 1 | 2 | 3 | 6 | 7 | SE/DE 1/ | 2/ | 3/ | 4/ | 5/ | 6/1 | 7/2 | 8/3 | 9/4 | 10/5 | 18 | 19 | CE 1 | 2 | 3 | 4 | SCU 1 | 2 | 3 | 27 | 28 | IOCE 1 | 2 | 3 | SELECT REG |
| 152 | 38 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | ATR-1 (ADDRESS TRANSLATION REGISTER) |
| 156 | 39 | STAT TRIGGERS B | C | D | E | F | G | H | BLOCK I FETCH | I FETCH 2 TGR | I FETCH 3 TGR | EXEC IN PROG TGR | | PROG STORE COMP | I FETCH REQ TGR | BR INV ADDR TGR | I FETCH INV ADDR TGR | CE1 WDD 20 | CE1 RDD 21 | CE2 WDD 22 | CE2 RDD 23 | TIMER 24 | PB 25 | CE3 WDD 26 | CE3 RDD 27 | CE4 RDD 29 | PIR 30 | DAR 31 | PIR 1 | 2 | 3 | | TIMING GT TGR |
| 160 | 40 | SYSTEM MASK 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | KEY 8 | 9 | 10 | 11 | A 12 | M 13 | W 14 | P 15 | IC IN LSWR 1 | COND CODE 34 | 35 | 36 | PROGRAM MASK 37 | 38 | 39 | MC INTRPT | | | PROGRAM INTERRUPT CODE 8 | 4 | 2 | 1 | INTERRUPT PRIORITY 1 | 2 | PSW (PROGRAM STATUS WORD) |
| 164 | 41 | D REQ | SCAN REQ | SET KEY | INSERT KEY | 3 CYCLE REQ | PAGE 1 LTH | | | RPT INSTR INIT | PULSE MODE ADJ | PULSE MODE INIT | STOP TGR | BLOCK TGR | PASS PULSE TGR | BLOCK INTRPT | FORCE ADDR TGR | SINGLE CYCLE TGR | CHECK SUM | CLOCK INHIBIT | RPT TEST | FLT TEST | ROS TEST TGR | SCC TGR | SYNC TGR | DISABLE INTER-LEAVE REV STOR ADDR | FLT BKSP | CONSOLE LOG OUT | SOROS | DIAG TGR | FLT REL | TIC | GAP | |
| 168 | 42 | STORAGE CHECK ADDRESS REGISTER 0 | 1 | 2 | 3 | 360 MODE | TEST MODE | SE STPD IN 360 MODE | | SAB CHK | SDBI CHK | SE/DE T/O | SE/DE ADDR CHK | SE/DE DATA CHK | SDBO FETCH CHK | LOS TO SE/DE | | IOCE BUS CHK | LOCAL STORE BUS CHK | CCR PTY CHK | ATR PTY CHK | PSBAR PTY CHK | PSBAR NOT CONF | PSBAR ALT CHK | SPLIT LOG OUT | LOG ROS CHK | LOG ADDR CHK | CE LOG REQ | RDD T/O | | | | | CR2 (CHECK REGISTER 2) |
| 172 | 43 | LACMP 1 | RSA FSP 2 | RMP 3 | MCW REGISTER RSARP 4 | LOC 5 | LOC 6 | DT 7 | DT 20 | SCAN ADDRESS SEQUENCER 1 | 2 | 3 | | SCAN CYCLE COUNTER 0 | 1 | 2 | 3 | FLT CLOCK 1 | ROS TEST SEQUENCER 0 | 1 | 2 | | | | | | FLT PASS | FLT FAIL | | FLT STG ERR | | MAINT MODE STOP CLOCK | SCAN BUFFER 1 | |
| 176 | 44 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | EXTERNAL REG |
| 180 | 45 | MARKS 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | TX TGR | AB REG 64 | 65 | 66 | 67 | | ABC 0 | 1 | 2 | PADDL 64 | 65 | 66 | 67 | | | | INSERT LOCAL STORE SIGN | STC 0 | 1 | 2 | |
| 184 | 46 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | AB REG (0-31) |
| 188 | 47 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | AB REG (32-63) |

●Figure 2-3.  CE Logword Formats (Sheet 1 of 3)

BIT POSITIONS IN MAIN STORAGE

| PSA LOC-ATION | PSA WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 192 | 48 | \ PHYSICAL PSBAR \ 9 10 11 12 | | | | P 9-12 | \ PSBAR COUNTER \ 9 10 11 | | | P 9-15 | \ LOGICAL PSBAR \ 9 10 11 12 13 14 15 16 17 18 19 | | | | | | | | | | ALT PSBAR | | | | \ PROGRAM STATUS WORD SYSTEM MASK \ 16 17 18 19 | | | | SE STPD 24 | \ PSA LOCKOUT \ 1 25 | 2 26 | 3 27 | PSBAR |
| 196 | 49 | CONFIGURATION CONTROL REGISTER (CCR) STATE S0 S1 | | \ SCON \ 1 2 3 4 | | | | \ ILOS \ 6 7 | | \ SE/DE \ 1/ 2/ 3/ 4/ 5/ 6/1 7/2 8/3 9/4 10/5 18 19 | | | | | | | | | | \ CE \ 1 2 3 4 24 25 26 27 28 | | | | | | | | | \ IOCE \ 1 2 3 | | | CCR |
| 200 | 50 | DIAGNOSE ACCESSIBLE REGISTER MASK \ IOCE \ 1 SPARE 2 SPARE 3 SPARE | | | | | | | \ SE/DE \ 1/ 2/ 3/ 4/ 5/ 6/1 7/2 8/3 9/4 10/5 | | | | | | | | | SPARE 16 | SPARE 17 | \ PAM/RCU \ 1/1 2/2 3/ | | | \ TCU \ 1 2 3 | | | \ SCU \ 1 2 3 | | | \ OTHER CE/OWN OTC \ 1 2 3 4 | | | | CE OWN OBS | DAR MASK |
| 204 | 51 | \ SERIAL ADDER LATCHES (SADDL) \ 0 1 2 3 4 5 6 7 | | | | | | | | \ INSTRUCTION COUNTER (IC) \ 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | | | | | | | | | SADDL, IC |
| 208 | 52 | \ R REGISTER \ 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 | | | | | | | | | | | | | | | | \ E REGISTER \ 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 | | | | | | | | | | | | | | | | R REG, E REG |
| 212 | 53 | \ F REGISTER (READ DIRECT) \ 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 | | | | | | | | | | | | | | | | \ D REGISTER \ 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | D REG, F REG |
| 216 | 54 | \ Q REGISTER \ 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Q REG |
| 220 | 55 | \ Q REGISTER \ 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | Q REG |
| 224 | 56 | DIAGNOSE ACCESSIBLE REGISTER (DAR) \ IOCE1 A B | | \ IOCE2 A B | | \ IOCE3 A B | | \ SE/DE ELC \ 1/ 2/ 3/ 4/ 5/ 6/1 7/2 8/3 9/4 10/5 | | | | | | | | | SPARE 16 | SPARE 17 | \ PAM/RCU ELC \ 1/1 2/2 3/ | | | \ TCU ELC \ 1 2 3 | | | \ SCU ELC \ 1 2 3 | | | \ OTHER CE ELC/CE OWN OTC \ 1 2 3 4 | | | | CE OWN OBS | DAR |
| 228 | 57 | CHECK REGISTER 1 \ PARALLEL ADDER FULL SUM-CHECK \ 4-7 8-15 16-23 24-31 32-39 40-47 48-55 56-63 | | | | | | | | | | | | | | | | \ PARALLEL ADDER HALF-SUM CHECK \ 4-7 8-15 16-23 24-31 32-39 40-47 48-55 56-67 | | | | | | | | | | | | \ ROS PARITY CHECK \ 2-42 43-68 69-99 | | | SADD HALF SUM CHK | SADD FULL SUM CHK | CR1 |
| 232 | 58 | CHECK REG 1 \ LSWR \ P 0-7 | P 8-15 | P 16-23 | P 24-31 | E REG PTY 0-7 | PADD FULL SUM 64-67 | MPR DECODE PTY CHK | PADD HALF SUM CHK | \ EXT TGRS \ PERMIT IOCE 1 | IOCE INTRPT REQ | \ N REG \ P 0-7 | P 8-15 | \ PSW REG \ P 0-7 | P 8-15 | NO RETRY | SVC INTRPT | PHYS PSBAR PTY 9-12 | PSBAR CNTR 12 | LOGICAL PSBAR PTY 16-19 | | SADDL P 0-7 | \ IC REG \ P 8-15 | P 16-23 | P 24-31 | | | | | | | | | |
| 236 | 59 | \ LOCAL STORAGE WORKING REGISTER (LSWR) \ 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSWR |
| 240 | 60 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 244 | 61 | \ T32-63 TO PADDA \ 32-63 COMP | T 31-62 L1 | T 31-62 C-L1 | \ T 32-47 TO PADDA 48-63 | T 48-63 TO PADDA 48-63 | K 0-31 TO PADDA 32-63 | 8-31 | \ D8-31 TO PADDA \ 7-30 L1 | 7-30 C-L1 | 40-63 | 40-63 COMP | FMTO | FMTN | FMTW | IC 8-31 TO PADDB 40-63 | AB 4-7 TO PADDB 4-7 | AB 8-31 TO PADDB 8-31 | AB 32-63 TO PADDB 32-63 | AB 64-67 TO PADDB 64-67 | AB 6-31 TO PADDB 4-29L2 | AB 32-67 TO PADDB 30-65L2 | AB 64-67 TO PADDB 28-31 | EX 6 TO PADDB 28-63 | HOT ONE TO PADDB 60 | E 8-11 TO PADDB 56-59 | E 12-15 TO PADDB 60-63 | E 8-11 TO PADDB 60-63 | Q 4-15 TO PADDB 52-63 | Q 20-31 TO PADDB 52-63 | Q 36-47 TO PADDB 52-63 | Q 52-63 TO PADDB 52-63 | |
| 248 | 62 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 252 | 63 | \ READ ONLY STORAGE DATA REGISTER (ROSDR) \ 70 71 72 73 74 75 76 77 79 80 81 82 83 84 | | | | | | | | | | | | | | P 43-68 | 86 88 89 90 | | | | P 69-99 | 92 93 94 95 | | | | 97 98 99 | | | RIGHT DIGIT TGR | S TGR | LEAVE TGR | STEP ABC TGR | ROSDR |

●Figure 2-3.  CE Logword Formats (Sheet 2 of 3)

| PSA LOC- ATION | PSA WORD NO. | BIT POSITIONS IN MAIN STORAGE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
| 256 | 64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 260 | 65 | READ ONLY STORAGE DATA REGISTER (ROSDR) | | | | | | | | | | | | | | | | | | | | | | | | | | | | INHIBIT LS WRITE | PROSA A LAST | FLT MODE | | ROSDR |
| | | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 64 | 65 | 66 | 67 | 68 | | | | |
| 264 | 66 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 268 | 67 | READ ONLY STORAGE DATA REGISTER (ROSDR) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ROSDR |
| | | | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 19 | P 2–42 | 21 | 22 | 23 | 24 | 25 | 26 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | |
| 272 | 68 | L REG | | | | K REG | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | P 0–7 | P 8–15 | P 16–23 | P 24–31 | P 0–7 | P 8–15 | P 16–23 | P 24–31 | | | | | | | | | | | | | | | | | | | | | | | | | |
| 276 | 69 | READ ONLY STORAGE ADDRESS REGISTER (ROSAR) | | | | | | | | | | | PREVIOUS ROS ADDRESS (A) | | | | | | | | | | | PREVIOUS ROS ADDRESS (B) | | | | | | | | | ROSAR, PROSA, PROSB |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 10 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
| 280 | 70 | M REG | | | | X REG | | | | Y REG | | | | | | | | N REGISTER | | | | | | | | | | | | | | | | N REG |
| | | P 32–39 | P 40–47 | P 48–55 | P 56–63 | P 0–7 | P 8–15 | P 16–23 | P 24–31 | P 32–39 | P 40–47 | P 48–55 | P 56–63 | | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
| 284 | 71 | ROSAR | | PROSA | | SPARE | | READ ONLY STORAGE DATA REGISTER (ROSDR) | | | | | | | | S 0–31 TO PADDA 32–63 | D 8–31 TO PADDA 8–31 C | AB 0–31 TO PADDB 32–63 | F 4–7 TO PADDB 60–63 | | | | | LOCAL STORAGE ADDRESS REG | | | | | WR LOCAL STORE | | | ROSAR, LSAR |
| | | 0 | 9 | A6 | B3 | | | 9 | 18 | 27 | 36 | 45 | 54 | 63 | 69 | 78 | 87 | 96 | | | | | | | 0 | 1 | 2 | 3 | 4 | | | | |
| 288 | 72 | K REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | K REG |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
| 292 | 73 | MAINTENANCE CONTROL WORD (MCW) | | | | | | | | | | | | | RNOP | FDGR | DSE 1 | RERP | RC | WRAP DE | | | | | | | | | | | | | | MCW |
| | | DE/SE | | SELECT | | | DG SELECT | | | CVG SELECT | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | | | | | | | | | | | | | |
| 296 | 74 | LM REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LM REG |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
| 300 | 75 | LM REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LM REG |
| | | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | |
| 304 | 76 | XY REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | XY REG |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
| 308 | 77 | XY REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | XY REG |
| | | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | |
| 312 | 78 | ST REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ST REG |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |
| 316 | 79 | ST REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | ST REG |
| | | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | |

•Figure 2-3.  CE Logword Formats (Sheet 3 of 3)

in loading of the Physical PSBAR.

### 9020E System

A 7201-02 CE used within a DCP environment can access up to five Storage Elements (SE) and five Display Elements (DE). Therefore the ATR is operationally and functionally viewed as two five position ATR's; the main storage ATR being positions 1-5 and the display storage ATR being positions 6-10.

ATR positions 1-5 represent translation registers for the logical range of addresses 0 to 2,621,439 bytes which represents five main storage elements (each 524K bytes). Each of these five positions can contain a hexadecimal digit 1 through 5 to represent a physical storage element (1-5).

ATR positions 6-10 represent translation registers for the disjunctive logical range of addresses 2,621,440 to 4,980,735 bytes which represents five display storage elements (each 262K bytes). Each of these five positions can contain a hexadecimal digit 6-A to represent a physical display element (6-10). Since display elements are 262K byte modules and their respective ATR positions represent 524K byte address boundaries, addresses associated with ATR positions 6-10 which lie in the upper half of the respective 524K byte address range (e.g., 262K to 524K of the 0 to 524K range) will be invalid.

In either the 9020D or 9020E System, hexadecimal 0 may appear in any ATR position. It is ignored and, if accessed, will produce an invalid address.

### Read Only Storage (ROS)

ROS is a 2816-word, 200 ns storage with approximately 90 ns access. Each word contains 100 bits; 95 bits are used as control bits, 3 bits are for parity, and two bits are used for bit plane testing. The control bits are grouped into 21 fields, the largest field being ten bits long. Each field, with the exception of the ROS address (NA field), is decoded into a set of control lines which control the action of the CE for one cycle. The microinstruction format that is used in ROS words is contained in table 2-1.

### 360 Mode

When running System/360 programs on a 9020D/E subsystem (comprised of a CE, one or more SE's, and IOCE 1), it is necessary to inhibit certain actions which are not compatible with System/360 operating programs.

Table 2-1. Microinstruction Format

| Field | ROS Bits | Function of Field |
|---|---|---|
| | 0-1 | Used in bit plane testing |
| | 2-5 | FAA controls |
| A | 6-9 | A,B, IC ingating |
| B | 10-11 | Local store to S and T |
| C | 12-16 | Ingating to ST, D, PSW, G, Q |
| D | 17-19 | Serial adder to F and End OPS (see note). |
| | 20 | Parity of bits 0-42 |
| E | 21-24 | E and R ingating |
| F | 25-30 | Miscellaneous control lines (see note) |
| G | 31-35 | Miscellaneous control lines (see note) |
| | 36-37 | Extended local store control |
| H | 38-42 | Local store control |
| L | 43-46 | Memory requests and mark sets |
| NA | 47-56 | Next address field |
| K | 57-61 | Y conditional branches |
| J | 62-68 | Z conditional branches/functional branches |
| M | 69-73 | Serial adder A side controls |
| N | 74-77 | Serial adder B side controls |
| P | 78-80 | Parallel adder latch controls |
| | 81 | E field extended |
| Q | 82-84 | Hot ones to adder A side |
| | 85 | Parity of bits 43-68 |
| R | 86 | Outgates to serial adder inbus A |
| T | 87-90 | Outgates to parallel adder B side |
| | 91 | Parity of bits 69-99 |
| U | 92-95 | Outgates to parallel adder A side |
| | 96 | U field extended |
| V | 97-99 | E,Q, to parallel adder B side |

NOTE: SCAN Mode Special Control Lines

A 360 mode indicating switch on the CE operators panel turns a
360 mode latch on or off.  It accomplishes the following when on:

1.  Causes the subsystem to operate as though bit 6 of the CCR
    (Inhibit Logout Stop) is set on.  The system cannot perform
    split logout, or issue logout stop to an SE.  PSBAR's are
    set to zero and cannot be stepped.

2.  Inhibits manipulation of PSW bits 16-19 (extended system
    mask) on Load PSW and Set System Mask.

3.  Causes a PSA lockout to create a machine-stop condition.

4.  Causes an SE stopped condition to create a machine-stop
    condition.

5.  Causes all unique 9020D/E System instructions to be invalid.

6.  Causes I/O Processor operations to cease.

Only IOCE 1 will operate in 360 mode and only if the CE and IOCE 1
are configured to each other.  If IOCE 1 is not configured to the
CE in 360 mode, the CE will not be able to execute I/O operations.

When in 360 Mode, depressing the 360 Mode switch returns the
subsystem to 9020 mode.  360 Mode is also released by the following:

1.  An External Start issued to the CE.

2.  A CE Power-On reset.

3.  A reconfiguration which places the CE in states 2 or 3.

4.  FLT Load

Computing Element Control Panel

The CE control panel (Figure 2-4) contains the indicators and controls
necessary to operate and control a computing subsystem.  A subsystem
is considered to consist of a combination of CE's, SE's, IOCE's,
Control Units, and I/O devices.  These switches and indicators may
be used to control an active system as backup for the System Console
or Configuration Console when it is not operating.  These system
functions are activated by turning on the SYSTEM INTERLOCK switch on
the CE control panel, or by the CE entering State One or Zero.

Functionally, the CE control panel is divided into two sections:
the monitor section and the maintenance section.  Tables 2-2 and
2-3 list the controls and indicators associated with the monitor and
maintenance sections of the CE control panel.  Table 2-4 lists the
CE switches and their operational environment.

The CE control panel is divided into seven panels (A through
G) as shown in Figure 2-4.  The following paragraphs discuss the
function of the controls and indicators located on each panel.

Table 2-2.  Monitor Controls and Indicators

| Name | Implementation |
|---|---|
| Load | Indicator |
| Manual | Indicator |
| Wait | Indicator |
| Test | Indicator |
| Element MPO Pull | Pull switch |
| Interrupt | Pushbutton switch |
| Load | Pushbutton Switch |
| Load Unit | Rotary switches (3) |
| Main Storage Select | Rotary switch |
| Power On/Off | Pushbutton |
| Power Sequence Complete | Indicator |
| System Interlock | Key switch |
| Address | Lever switches (24) |
| Data | Lever switches (64) |
| System | Indicator |
| Display | Pushbutton switch |
| Address Compare | Lever switch |
| Repeat Instruction | Lever switch |
| Rate | Rotary switch |
| Set IC | Pushbutton switch |
| Start | Pushbutton switch |
| Stop | Pushbutton switch |
| Storage Select | Lever switch |
| Store | Pushbutton switch |
| Reset | Pushbutton switch |
| PSW Restart | Pushbutton switch |
| State Three | Indicator |
| State Two | Indicator |
| State One | Indicator |
| State Zero | Indicator |
| 360 Mode | Indicating pushbutton switch |

Monitor Section

This section of the CE Control Panel contains those operator controls
that are required by the operator when the CE is operating under
program control.  The main functions which are provided at the
monitor section are the control and indication of power, the indi-
cation of element status, operator-to-machine communication, and
initial program loading.  This section is located at the lower
half of the panel, except for the Element Master Power Off pull
switch which is at the upper right corner of the panel.

Maintenance Section

This section of the CE control panel contains those controls intended
primarily for maintenance use, although in some cases an overlap

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Figure 2-4.   CE Control Panel (Sheet 1 of 2)

PANEL D    PANEL E

1052 I/O INTERFACE

ENABLE    DISABLE

DISABLE

K

DATA 0-31

| BYTE 0 | BYTE 1 | BYTE 2 | BYTE 3 |

0 1 2 3 4 5 6 7   8 9 10 11 12 13 14 15   16 17 18 19 20 21 22 23   24 25 26 27 28 29 30 31

CK REG 1 SUMMARY

DATA 32-63

| BYTE 4 | BYTE 5 | BYTE 6 | BYTE 7 |

32 33 34 35 36 37 38 39   40 41 42 43 44 45 46 47   48 49 50 51 52 53 54 55   56 57 58 59 60 61 62 63

L

PSBAR

SE

CE

STATE    SCON    ILOS    IOCE

1024 512 256   128 64 32 16 8 4 2 1
COUNT

ROS ADDRESS COMPARE

ADDRESS

| | 27 | 28 | 29-31 |
|---|---|---|---|
| LOCAL STORE | 0 | | REGISTERS 0-15 |
| FP | 1 | 0 | REGISTERS 16-23 |
| WORKING REGISTER | 1 | 1 | REGISTER 24 |

8 9 10 11 12 13 14 15   16 17 18 19 20 21 22 23   24 25 26 27 28 29 30 31

M

CK REG 2 SUMMARY

MAIN STOR ADDRESS COMPARE

10    15    20    25    30    35    40    45    50

N

| SCAN MODE | DEFEAT INTERLEAVING | | | STORAGE SELECT | ADDRESS COMPARE | CHECK CONTROL | PULSE MODE | REPEAT INSN | ROS ADDRESS | IND RLR 1 |
|---|---|---|---|---|---|---|---|---|---|---|

RQS    NO REV    MAIN BYTE    LOOP    STOP    TIME    MPLE    STOP    L REG
PROC    PROC    MAIN    PROC    PROC    PROC    PROC    PROC    M REG
FLT    REV    LOCAL    STOP    DSBL    COUNT    SINGLE    RPT

P

REPEAT    INHIBIT CE HARD STOP    DISABLE INTERVAL TIMER    INDICATE RLR 1 POSITION 6

SYSTEM RESET    LAMP TEST ALLOW IND    CHECK RESET

Q

RATE
PROCESS

INSN STEP    SINGLE CYCLE
SINGLE CYCLE STORAGE INHIBIT

PSW RESTART    REGISTER SET    R.O.S. TRANSFER

FREQUENCY ALTERATION

DISABLE    ENABLE

REGISTER SELECT

PROCESS
AIR    PSBAR
CCR

| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 0 1 1 |
| 4 | 0 1 0 0 |
| 5 | 0 1 0 1 |
| 6 | 0 1 1 0 |
| 7 | 0 1 1 1 |
| 8 | 1 0 0 0 |
| 9 | 1 0 0 1 |
| A | 1 0 1 0 |
| B | 1 0 1 1 |
| C | 1 1 1 0 |
| D | 1 1 0 1 |
| E | 1 1 1 0 |
| F | 1 1 1 1 |

SET IC    STORE    DISPLAY

R

S

START    STOP    BACKSPACE FLT    LOG OUT

SYSTEM INTERLOCK

ON POWER OFF    POWER SEQUENCE COMPLETE

MAIN STORAGE SELECT    LOAD UNIT

INTERRUPT    SYSTEM MANUAL WAIT TEST LOAD    LOAD

PANEL F    PANEL G

●Figure 2-4.  CE Control Panel (Sheet 2 of 2)

Table 2-3.   Maintenance Controls and Indicators

| Name | Implementation |
|---|---|
| Check Reg 1 Summary | Indicator |
| Check Reg 2 Summary | Indicator |
| Status | Indicators (216) |
| Indicate On Roller 1 Pos 6 | Lever Switch |
| Check Reset | Pushbutton |
| Check Control | Lever Switch |
| Scan Mode | Lever Switch (2) |
| Backspace FLT | Pushbutton |
| Test Switch | Lever Switch |
| Disable Interval Timer | Lever Switch |
| Logout | Pushbutton |
| ROS Address | Lever Switch |
| Register Set | Pushbutton |
| Register Select | Rotary Switch |
| Lamp Test/Allow Indicate | Pushbutton |
| ROS Transfer | Pushbutton |
| Inhibit CE Hard Stop | Lever Switch |
| Defeat Interleaving | Lever Switch |
| Frequency Alteration | Rotary Switch |
| Marginal Meter Select | Rotary |
| Pulse Mode | Lever Switch |
| 1052 Enable-Disable | Toggle Switch |
| Disable | Indicator |

Table 2-4.   CE Switches and Their Operational Environment

| | CE Program State | | Controls at CE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Operational | Stopped | Key Off State | | | | | Key On** State | | | | |
| | | | 3 | 2 | 1 | 0 | Ø | 3 | 2 | 1 | 0 | Ø |
| Address Compare | X | | | | X | X | X | X | X | X | X | X |
| Address * | | | | | X | X | X | X | X | X | X | X |
| Backspace FLT | X | X | | | | X | X | | | | X | X |
| Check Control | X | X | | | | X | X | | | | X | X |
| Check Reset | X | X | | | | X | X | | | | X | X |
| Data * | | | | | X | X | X | X | X | X | X | X |
| Defeat Interleaving | X | | | | | X | X | | | | X | X |
| Disable Interval Timer | X | | | | | X | X | | | | X | X |
| Display | | X | | | X | X | X | X | X | X | X | X |
| Element MPO | X | X | X | X | X | X | X | X | X | X | X | X |
| Frequency Alteration | X | X | | | | | X | | | | | X |

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Table 2-4.  CE Switches and Their Operational Environment (Cont)

| | CE Program State | | Controls at CE | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Operational | Stopped | Key Off State | | | | | Key On** State | | | | |
| | | | 3 | 2 | 1 | 0 | Ø | 3 | 2 | 1 | 0 | Ø |
| Indicate On Roller 1 Pos. 6 | X | X | X | X | X | X | X | X | X | X | X | X |
| 1052 Enable-Disable | X | X | X | X | X | X | X | X | X | X | X | X |
| Inhibit CE Hard Stop | X | X | | | | X | X | | | | X | X |
| Interrupt | X | | | | X | X | X | X | X | X | X | X |
| Key (System Interlock) | X | X | X | X | X | X | X | X | X | X | X | X |
| Lamp Test/Allow Indicate | X | X | X | X | X | X | X | X | X | X | X | X |
| Load | X | X | | | X | X | X | X | X | X | X | X |
| Load Unit * | | | | | X | X | X | X | X | X | X | X |
| Logout | X | X | | | X | X | X | X | X | X | X | X |
| Main Storage Select * | | | | | X | X | X | X | X | X | X | X |
| Marginal Check and Voltage Controls | X | X | X | X | X | X | X | X | X | X | X | X |
| Power Off | X | X | | | | X | | | | | | X |
| PSW Restart | X | X | | | X | X | X | X | X | X | X | X |
| Pulse Mode | X | X | | | | X | | | | | | X |
| Rate | | X | | | X | X | X | X | X | X | X | X |
| Register Select * | | X | | | | X | | | | | | X |
| Register Set | | X | | | | X | | | | | | X |
| Repeat Instruction | | X | | | X | X | X | | | X | X | X |
| ROS Address | X | X | | | X | X | X | | | X | X | X |
| Reset | X | X | | | X | X | X | | | X | X | X |
| ROS Transfer | | X | | | X | X | X | | | X | X | X |
| Scan Mode | X | X | | | | X | X | | | | X | X |
| Set IC | | X | | | X | X | X | X | X | X | X | X |
| Start | | X | | | X | X | X | X | X | X | X | X |
| Store | | X | | | X | X | X | X | X | X | X | X |
| Stop | X | | | | X | X | X | X | X | X | X | X |
| Storage Select * | | | | | X | X | X | X | X | X | X | X |
| Test Switch | X | X | | | | X | X | | | | X | X |
| 360 Mode | X | X | | | X | X | X | | | X | X | X |

Legend

    X - Control is functional
KEY  - System Interlock Switch
  *  - Static; requires use of other control
 **  - If both CE and SCC or CC keys are on, the SC or CC key
        takes precedent.
  Ø  - State 0 and Test Mode

exists with the monitor controls.  These controls fall logically
into two categories:  maintenance control, and marginal check and
voltage display control.

Panel A

Meter- The meter indicates the voltage levels of the marginable
supplies.  The particular supply indicated is determined by the
MARGIN/METER SEL switch.

Margin/Meter Sel- This switch has six positions to enable selection
of the power supply to be indicated by the meter and for determination
of which of the CE gates may be marginally checked:

    1.  Gate A- Indicates and selects CE logic gate A.
    2.  Gate B- Indicates and selects CE logic gate B.
    3.  Gate C- Indicates and selects CE logic gate C.
    4.  Gate E- Indicates and selects CE logic gate E.
    5.  Gate K & L- Indicates and selects CE logic gates K and L.
    6.  ROS- Indicates the 18V ROS bias power supply.

Margin

    1.  Active - Indicates that an internal power supply is being
        varied to marginally check the logic.

    2.  Locate- Indicates when the MARGIN/METER SEL switch is at
        the position of a margined power supply.

Power Status

    Main Line On-  Indicates that the CE is being powered via its
    normal power supply system (non-battery powered).

    OBS (On Battery Signal) - Indicates when the CE is being battery
    powered for five seconds (to perform housekeeping tasks) prior to
    the dropping of unit power.

    Thermal-  Indicates the presence of an excessive heat condition
    within one of the CE's logic gates.

    Power Check-  Indicates an incomplete power-up condition in the
    CE, a thermal condition, or an over-current or under-voltage
    condition at one of the DC regulators.

Panel B

The six controls on this panel, ROS, +6M A GT, +6M B GT, +6M C GT,
+6M E GT, and +6M K & L GT, raise or lower the output voltage levels
from the 18V ROS, the 6V gate A,B,C,E, and K & L regulators, res-
pectively.

Panel C

Element MPO Pull- Pulling this switch turns off all power beyond
the entry terminal of the CE.

This switch latches in the "out" position and can be restored to its "in" position only by maintenance personnel.

When the ELEMENT MPO PULL switch is in the out position, the Power On switch is ineffective. The MPO switch is effective in all element states.

Panel D

360 Mode- This back lighted switch places the CE (and IOCE 1 if configured) in System/360 mode. When in 360 mode (light on), depression of the pushbutton restores to 9020 mode.

State Indicators- There are four states of CE availability. Each state defines a condition of operational capability.

1. Three - The CE state bits in the CCR are set to 1,1. (Most of the control panel is disabled.) State Three is the highest operational state.

2. Two- The state bits in the CCR are set to 1,0. . (Most of the control panel is disabled.) When in State Two the CE is capable of being recalled to State Three.

3. One - The CE state bits in the CCR are set to 0,1. (Certain manual controls are enabled.) When in State One the CE is capable of being recalled to State Three.

4. Zero - This indicator is on when CE state bits in the CCR are set to 0,0. The Test switch is enabled. The CE control panel is operative. The Test switch being turned on allows power on-off operation, manual manipulation of the configuration register contents, and prevents interference from elements outside the subsystem.

Test Switch - Operable only in State Zero and enables all manual controls.

1052 I/O Interface Enable-Disable Switch - This switch causes the 1052 adapter to logically disconnect from the channel when placed in the Disable position. Any operation in process is completed prior to disconnecting, and the Disable indicator is then turned on. When the switch is placed in the Enable position, the 1052 adapter is connected to the channel, and the Disable indicator is turned off.

Panel E

Status- These lights are arranged in six groups of thirty six-each, to provide a display of CE status information. The data displayed in each set of lights is controlled by a selector rotary switch which can select up to six words, with the exception of roller 1 which can select up to seven words under control of the Indicate Roller 1 Pos 6 lever switch. The selector rotary switch also adjusts a roller format to identify the information displayed. Figure 2-5 details the data displayed for each of the three groups.

●Figure 2-5.  CE Roller Strip Layout (Sheet 1 of 2)

**DISPLAY NO. 4**

Row 1 — SYSTEM MASK CHANNEL / PROTECTION KEY / PSW PROGRAM MASK / PROGRAM INTRPT / INTRPT PRI

| P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | EXT 7 | P 8-15 | 0 | 1 | 2 | 3 | ASCII 12 | MACH CHK | WAIT 14 | PROB 15 | NO RETRY | IC IN LSWR | COND 2 | COND 1 | FXP OVFLW | DEC OVFLW | EXP UNFLW | LOST SIG | MACH CHK INTRPT | SUPV CALL INTRPT | | | 8 | 4 | 2 | 1 | 1 | 2 |

Row 2 — Q REGISTER

| P 32-39 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | P 40-47 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | P 48-55 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | P 56-63 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

Row 3 — B REGISTER

| P 32-39 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | P 40-47 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | P 48-55 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | P 56-63 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

Row 4 — A SIDE CTL SERIAL ADDER / B SIDE CTL SERIAL ADDER / PADDL CONTROL / EW EXTD / GATE ONES PA / AB→F / AB, IC, F→PB / ST, DA→PA / E, Q→PB / RT DIG / EDIT

| M 69 | 70 | 71 | 72 | 73 | N 74 | 75 | 76 | 77 | P 78 | 79 | 80 | 81 | 82 | 83 | 84 | R 43-68 | 86 | T 87 | 88 | 89 | 90 | U 69-99 | 92 | 93 | 94 | 95 | 96 | V 97 | 98 | 99 | RT DIG | S | LEAVE | STEP ABC |

Row 5 — STATUS TRIGGERS / INSTRUCTION FETCH CONTROLS / EXTERNAL INTERRUPTS

| A | B | C | D | E | F | G | H | BLOCK | 1 | 2 | 3 | EXEC | PS CMPR | IN STOR FETCH | BR INVLD ADDR | INVLD ADDR | IL NOT AVAIL | CE 1 WD | RD | CE 2 WD | RD | TC AT LIMIT | CONS PB | CE 3 WD | RD | CE 4 WD | RD | PIR | DAR | IOCE 1 | PIR IOCE 2 | IOCE 3 | TIME GATE TGR |

Row 6 — EXTERNAL REGISTER

| P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |

DISPLAY 4 legend:
1 PSW
2 Q REG (32-63)
3 B REG (32-63)
4 ROSDR (69-99), EDIT
5 STATUS, INSN FETCH, EXTERNAL INTERRUPTS
6 EXTERNAL REG 0-31

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**DISPLAY NO. 5**

Row 1 — PHYSICAL PSBAR / PSBAR COUNTER / LOGICAL PSBAR / SYSTEM MASK / PROGRAM INTRPT

| P 9-12 | 9 | 10 | 11 | 12 | P 9-12 | 9 | 10 | 11 | 12 | P 9-15 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-19 | 16 | 17 | 18 | 19 | ALT PSBA | | | | 16 | 17 | 18 | 19 | SE STOP | PSA LOCKOUT 1 | 2 | 3 |

Row 2 — REV SABTP / LCMPR / REV SAFSP / REV MRKP / REV SARPA / REV SARPB / LOG CNT / ADDR SEQUENCE / FLT COUNTER / FLT CHK / ROS TEST SEQ / PASS / FAIL / FLT STG ERR / MMSC / BFR 1

| ROS PLANE | | LFTHF | UNCT | CONDT | ERSLT | DSBL TMR | 0 | 1 | 2 | 3 | 4 | 0 | 1 | 2 | 3 | 0 | 1 | 0 | 1 | 2 | | | PASS | FAIL | FLT STG ERR | | MMSC | BFR 1 |

Row 3 — R REGISTER / OPERATION CODE / E REGISTER

| P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

Row 4
| S 0-31 | T32-63 | | T32-63 | | T32-47 | T48-63 | K00-31 | DB-31 | | DB-31 | | DB-31 | | IC | A0-31 | A4-7 | A8-31 | B32-63 | B32-67 | B64-67 | A6-31 | B32-67 | B64-67 | EXCS-6 | F4-7 | HOT 1 | E8-11 | E12-15 | E8-11 | Q4-15 | Q20-31 | Q36-47 | Q52-63 |
| 32-63 | 32-63 | | 31-62 | 48-63 | 48-63 | 32-63 | 8-31 | | 7-30 | | 40-63 | FMTO | FMTN | FMTW | 40-63 | 32-63 | 4-7 | 8-31 | 32-63 | 64-67 | 4-29 | 30-65 | 28-31 | 28-63 | 60-63 | 60 | 56-59 | 60-63 | 52-63 | 52-63 | 52-63 | 52-63 |
| | T | C | TL1 | CL1 | | | | T | C | TL1 | CL1 | T | C | | | | | | | | | | | | L2 | L2 | | | | | | | |

Row 5 — CONFIGURATION CONTROL REGISTER / STATE / SCON / SE / SE/DE / CE / IOCE

| P 0-7 | STATE S0 | S1 | SCON 1 | 2 | 3 | 4 | ILOS | P 8-15 | 1 | 2 | SE 3 | 4 | 5 | SE/DE 6 | 7 | P 16-23 | 8 | 9 | 10 | | | CE 1 | 2 | 3 | 4 | P 24-31 | 1 | 2 | 3 | IOCE 1 | 2 | 3 |

Row 6 — DIAGNOSE ACCESSIBLE REGISTER MASK

| P 0-7 | IOCE 1 | IOCE 2 | IOCE 3 | 1 | 2 | P 8-15 | SE 3 | 4 | 5 | 6 | 7 | SE/DE 8 | 9 | 10 | P 16-23 | PAM/RCU 1 | 2 | 3 | TCU 1 | 2 | 3 | P 24-31 | SCU 1 | 2 | 3 | OTHER CE/OWN OTC 1 | 2 | 3 | 4 | CE OWN OBS |

DISPLAY 5 legend:
1 PSBAR, SYS MASK, INTRPTS
2 MCW AND FLT CONTROL
3 R REG, E REG
4 GATE CONTROL TGRS
5 CCR
6 DAR MASK

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**DISPLAY NO. 6**

Row 1 — PARALLEL ADDER LATCHES

| P 32-39 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | P 40-47 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | P 48-55 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | P 56-63 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

Row 2 — MARKS / ST PTY / LS ADDRESS REGISTER / LS WRITE / INHIB STORE WRITE / TX TGR / B REG / ABC / PADDL / INSERT LS SIGN / STC

| P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | ST PTY 32-39 | 0 | 1 | 2 | 3 | 4 | LS WRITE | INHIB STORE WRITE | TX TGR | P 64-67 | 64 | 65 | 66 | 67 | ABC 0 | 1 | 2 | P 64-67 | 64 | 65 | 66 | 67 | INSERT LS SIGN | STC 0 | 1 | 2 |

Row 3 — SERIAL ADDER LATCHES / INSTRUCTION COUNTER

| P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |

Row 4 — DIAGNOSE ACCESSIBLE REGISTER

| P 0-7 | IOCE 1 a | b | IOCE 2 a | b | IOCE 3 a | b | 1 | 2 | P 8-15 | SE/DE ELC 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | P 16-23 | PAM/RCU ELC 1 | 2 | 3 | TCU ELC 1 | 2 | 3 | P 24-31 | SCU ELC 1 | 2 | 3 | OTHER CE ELC/CE OWN OTC 1 | 2 | 3 | CE OWN OBS |

Row 5 — STOR UNIT CHECK ID / 360 MODE / TEST MODE / SE STOP 360 / CHECK REGISTER 2

| STOR UNIT CHECK ID 0 | 1 | 2 | 3 | 360 MODE | TEST MODE | SE STOP 360 | | SAB PTY CHK | SDBI PTY CHK | STG TO | STG ADDR CHK | STG DATA CHK | SDBO FETCH CHK | LOS SENT | | IOCE CHK RESP | LS BUS CHK | CCR PTY CHK | ATR PTY CHK | PSBAR PTY CHK | PSBAR NOT CONF | PSA ALT | SPLIT LOGOUT | | LOG ROS CHK | LOG ADDR CHK | CE LOG REQ | RDD TO | |

Row 6 — LOGOUT OR WRAP SELECTED STG ID / DG SELECTED / DE WRAP / CVG SELECTED / MAINTENANCE CONTROL WORD

| P 32-39 | 0 | 1 | 2 | 3 | DG SELECTED 0 | 1 | 2 | 3 | P 40-47 | CVG SELECTED 1 | 2 | 3 | 4 | 5 | 6 | FORCE DG REQ | P 48-55 | DIAG SE 1 | INV EXT PTY | RST CHKS | WRAP DE | | | | | | | | | | | | |

DISPLAY 6 legend:
1 PADDL (32-63)
2 MARK, LAR, B REG, ABC, PADDL, STC
3 SADDL, IC
4 DAR
5 CHECK REG 2
6 MCW (32-51)

•Figure 2-5.  CE Roller Strip Layout (Sheet 2 of 2)

Data 0-31 and Data 32-63 switches-  These 64 switches, in hexadecimal groups, permit data to be entered manually.  Correct parity is automatically generated.  These switches can be changed without disrupting CE operation.

Address Switches-  These 24 switches provide a manual means of selecting an addressable location in storage.  The operation is as follows:

1.  Twenty-four switches are arranged in hexadecimal groups, to permit storage addressing.

2.  Correct parity will be automatically generated.

3.  Address switches 9-28 are used in conjunction with the Address compare switch for selection of an address for an address compare stop or address compare sync.

4.  **Address switches 8-19 are used for selection of a ROS address for a ROS address compare sync or stop.  The sync pulse will be provided whenever there is a compare between the ROS address and the switches.**

Check Reg 1 Summary - Indicates an error in the CE as defined in Check Register 1 (roller 2 pos. 2).

Check Reg 2 Summary - Indicates an error in the CE as defined in Check Register 2 (roller 6 pos 5).

Panel F

Scan Mode-  Provides two modes of testing.  The Disable Interval Timer switch must be placed in the disable position when running either test.

1.  In the FLT position, the CE is ready for FLT testing.

2.  In the ROS position, this switch allows checking each bit in ROS.  A depression of the Load pushbutton will obtain the tests from tape and compare them against data in the ROS.

Repeat-  Continuously repeats the test in storage or the new test being sought.  The operation is as follows:

1.  With the toggle in the Repeat position, depressing the Start pushbutton will cause the ROS or FLT test in storage to be executed repeatedly.

2.  With the toggle in the Repeat position, the test number in the data keys, and the FLT tape rewound, the test is begun by depressing the Store, then Load pushbutton.  A new FLT test is then sought out according to the alternate test number in the T-register and executed repeatedly.

Defeat Interleaving-  A three-position lever switch that performs the following functions:

1.  No Rev (up) position - Interleaving of main storage addressing is disabled.

2. Rev (down) position - Interleaving of main storage is disabled, and the main storage addresses are reversed (low-order half to high-order and vice versa).

3. Proc (center) position - Addressing is interleaved with no reversal of storage addresses.

Inhibit CE Hard Stop- Provides a means of inhibiting the CE from entering a hard stop state upon encountering hard stop error conditions such as a storage check during logout and PSBAR parity check.

Disable Interval Timer- Prevents the interval timer from advancing.

Storage Select- This switch (in conjunction ... th e Store and Display switches) selects the storage area that is to be addressed by the ADDRESS switches. The three positions are:

1. Main - Selects the doubleword main storage address specified by Address switches for both storing and displaying data.

2. Main Byte - For storing, selects the byte (Address switches 29, 30, and 31) within the doubleword specified by Address switches 8-28 for displaying, same as main.

3. Local- Selects Local Storage per Address switches 27-31 for both storing and displaying data. (see Figure 2-4).

Address Compare- Provides a machine stop on a CE storage compare. The operation is as follows:

1. In the center or normal position, a sync pulse is provided whenever there is a compare between the storage address bus and bits 9-28 of the Address switches.

2. Down position-Stop. The CE will stop at the end of the instruction in progress, whenever there is a compare between the storage address bus and bits 9-28 of the Address switches.

3. Up position-Loop. Will cause a looping operation between addresses specified in the data switches 40-63 (start address) and the Address switches (loop back to address in Data switches)

Check Control - Provides three modes of operation when a CE check condition is detected.

1. In the process position, the CE issues an element check. If the Machine Check Mask bit, PSW bit 13, is on, logout of the CE occurs. If the Machine Check Mask bit is off, processing continues, the check trigger is set, and the logout and machine check interruption is deferred until the PSW is loaded with bit 13 on.

2. In the Stop position, a stop occurs with no logout.

3.  In the Disable position, the appropriate check trigger is set but no stop, logout, or interruption occurs.

Pulse Mode- Provides a means of looping through a selected count of machine cycles starting at a selected address, or when the interval timer is advanced. The starting address must be stored in bits 40 to 63 of location zero before beginning pulse mode. The operation is as follows:

1.  Count (Down position) - The operations start at the address contained in location zero and proceed through the number of machine cycles entered in Data switches 53-63. A system reset then takes place as does a restart at the address specified in main storage location zero. The maximum count is 2047.

2.  Time (Up position) - The start occurs at the address specified by location zero and proceeds until the interval timer advances. The Disable Interval Timer switch is inoperative. When the interval timer advances a system reset takes place as does a restart at the address specified in main storage location zero. No action will occur if the Rate switch is not in the Process position.

3.  Process (Center position) - Normal machine cycling will prevail. The machine must be in the stopped state to enter or leave Pulse Mode. Pulse Mode is inoperative during repeat instruction.

Repeat Insn (repeat instruction) - Provides a method for repeating a single instruction or a group of up to four halfword instructions. The operation is as follows:

1.  Multiple (Up position) - The group of instructions can be placed in the Data switches and is continually executed (looping through the four halfwords).

2.  Single (Down position) - Only the first instruction in the Data switches is repeated continuously.

3.  Process (Center position) - Normal instruction sequencing prevails.

The instruction buffer is not changed, so branching instructions only change the instruction counter and an execute instruction executes the contents of the Data switches from the buffer.

ROS Address - Provides the ability to repeat or stop on any ROS address that is placed in the Address switches. The operation is as follows:

When in the Repeat ROS Address position, the CE is placed in repeat ROS address mode. Operation is started by depressing the ROS Transfer switch and is stopped by depressing the Reset

switch. A ROS parity error may occur if the Address switches
are changed during the operation. When in the Stop position,
the CE stops when the ROS address contained in the address
switches is encountered.

Indicate Roller 1 Pos 6 - This switch allows selection of either
the L register or M register to be displayed on status roller 1,
position 6.

Frequency Alteration - In the Disable position clock pulses are
distributed from the oscillator to cause a 200-ns cycle. In the
Enable position clock pulses are distributed from the oscillator
to cause a 195±½ ns cycle.

Register Select - Directs the loading of PSBAR, CCR, or ATR from the
Data switches upon depression of the Register Set pushbutton.

Rate- Indicates the manner in which instructions are to be per-
formed. The four positions are:

   1.  Process - CE runs in normal processing mode.

   2.  INSN Step - CE executes a single instruction with each
       depression of Start switch.

   3.  Single Cycle - Causes CE to execute a single machine cycle
       with each depression of Start switch.

   4.  Single Cycle Storage Inhibit - Same as Single Cycle
       operation except all storage references are blocked.

Start- Starts the operation defined by the Rate switch. If it is
pressed after a normal stop, it causes the continuation of instruction
processing as if no stop had occurred. If it is pressed after
system or sub-system reset, the instruction designated by the
Instruction Counter is the first one executed.

Reset- Initiates a subsystem reset which resets the issuing CE and
all IOCE's and SE's configured to the issuing CE but does not alter
any CCR.

Lamp Test/Allow Indicate- Allows all indicators, with the exception
of those located on Panel A and Panel E, to be tested simultaneously.
In addition, the Allow Indicate function allows machine status to
be indicated when stopped during a logout sequence.

Check Reset- Provides a means of resetting all CE check triggers
to the non error state. All logic check indicators are turned off.
In order to reset hard-stop errors, the Inhibit Hard Stop switch must
be put on. For a PSBAR parity error, correct parity should first be
set in PSBAR while the Inhibit Hard Stop switch is on.

PSW Restart- Used in conjunction with the system interlock key to
generate a system or subsystem PSW restart.

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Register Set- When the Register Set switch is depressed, it causes
the contents of the DATA switches to be loaded into PSBAR (data
switches 41-51), CCR (data switches 32-63), or ATR (data switches
0-39) depending on the REGISTER SELECT switch setting.  Note:  When
loading PSBAR, data keys 32-40 and 52-63 should be zero.  If they
are not, a PSBAR parity check may result.

R.O.S. Transfer- Provides a means to visually interrogate the
contents of a ROS location, or to begin processing from any ROS
address.  The operation is as follows:

1.  With the machine in the stopped or reset state and the
    absolute ROS address in the 12 high-order address switches,
    depressing the ROS Transfer pushbutton causes the addressed
    ROS word to be read out into the sense latches.  Operation
    beyond this point depends on the setting of the Rate switch.

    a.  If the Rate switch is in the Process position, the CE
        continues executing ROS commands from the entry point.

    b.  If the Rate switch is in the INSN Step (instruction
        step) position, the CE continues until End operation is
        reached.

    c.  If the Rate switch is in the Single Cycle or Single
        Cycle Storage Inhibit positions, the ROS and the CE
        stop with the contents of the ROS word, specified by
        the Address switches, displayed in the sense latches.
        Depressing of the Start switch will advance the ROS
        one cycle.  The ROS positions which have the data
        register indicated can be viewed.  Further depressions
        of the START pushbutton advance the ROS as in single
        cycle mode.

2.  In all cases, checks may occur because of storage data
    bus gating to registers and the registers through the
    adder.  The CE check switch in the DSBL (Disable) position
    can be used to keep the machine from stopping on these
    checks.

Set IC (Instruction Counter)- Sets the value contained in the ADDRESS
switches into the instruction address portion of the PSW and fills
the Q-and R-registers with the instructions beginning at the selected
address.

Store- Stores information in an addressed location.  The contents
of the storage Data switches are placed in the location specified
by the instruction Address switches.  Storage protection is ignored.
The switch is active only while the CE is in the stopped state.

Display - Causes the data in the storage location specified by the
Address switches to be displayed.  The switch is active only while
the CE is in the stopped state.

Stop- Causes the CE to enter the stopped state.  The stopped state
is indicated by the Manual light being on.  The transition from
operating state to stopped state occurs at the end of instruction
execution, prior to the fetching of the next instruction.  When the
CE is in the wait state, the transition takes place immediately.  All
interruptions which are pending and which are not masked off are
taken causing the old PSW to be stored and the new one fetched be-
fore entering the stopped state.

Backspace FLT - Provides a method to backspace a record on tape.
This facility is usually used during ROS or FLT test mode operation.

Logout- Causes a complete logout of CE status.  The Logout is identical
to that which occurs when a check condition is detected.  It is not
maskable by PSW bit 13.

Panel G

Power On/Off-  Initiates the power-on and power-off sequence for
the CE.  At the completion of the power-on sequence a power on
reset occurs.  The switch is active only when the Element MPO
Pull switch is in its "in" position, and may cause power to be
turned off in the zero state with the Test switch on.

System Interlock- A regular key lock type switch (similar to the
one used by IBM for equipment usage meters).  Tumbler settings
provided are unique to 9020 System.  (Affected controls are listed
in Table 2-4).  Operation of this switch enables the functions of
the controls interlocked.

Power Sequence Complete- The light is on after all DC voltages have
been turned on.

NOTE:  Power on Reset causes an Element (Unit) to be reset when all
D.C. voltages are at their normal operating levels.  All SCON bits
are set to one in the CCR; other CCR bits are set to zero.

SE Storage Select- Provides the capability to select one of up to
ten storage elements in a D System (five in an E-System) for IPL
or PSW restart.

Load Unit- These three switches provide hexadecimal numbers to
select the channel and I/O device to be used for IPL.  The left
switch has eleven positions labeled 0 to A, and selects the channel.
The other two switches have sixteen positions each, labeled with
the standard hexadecimal characters O-F, and select the device.

Interrupt- Causes an external interruption request.

SYST (System)- Indicates that the CE is in the running state.

Wait- Indicates that the CE is in the wait state.

Test- Indicates when a manual control is not in its normal position.

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Load- This light is on while the CE is executing the system or sub-system initial program loading (IPL). The light is turned on when the LOAD switch is depressed, and is turned off after the read operation and the loading of the new program status word (PSW) are completed successfully.

Load- This switch used without the System Interlock switch causes a subsystem IPL procedure. If the System Interlock switch is on, a system reset and system IPL procedure are initiated. If the scan Mode switch is in the FLT or ROS load position depressing the Load switch generates a subsystem reset and FLT load.

The steps necessary to perform a system or subsystem IPL are:

1. Select a main storage element using the SE Storage Select switch.

2. Select the address of the I/O device by using the Load Unit select switches.

3. Turn on the System Interlock switch (System IPL only).

4. Depress the Load pushbutton.

The load indicator adjacent to the Load pushbutton will turn on when the IPL sequence is being performed and will remain on until the IPL is complete. If a fault should occur during the IPL sequence the Load light will remain on.

NOTE: System reset causes all 9020 System elements and units not in State Zero (Test switch on) to terminate their current operations and perform an internal reset. System reset is initiated by de-pressing the Load switch at the System Console/Computing Element or by depressing the PSW Restart switch at the CE provided the System Interlock key is on. All ATR's are reset to zero. All CCR SCON bits are set to ones; other CCR bits are set to zero. a dual line is used for system reset so that noise on one line will not cause an element (unit) to be reset.

MAINTENANCE FEATURES

Maintenance features for the IBM 7201-02 Computing Element fall into two general categories:

1. Those used for error detection during normal operation, such as error detecting logic and interruptions.

2. Those aids used for diagnosing the cause of failures and for preventive maintenance.

This second category includes the CE control panel, the scan logic (FLT, ROS and logout), and marginal checking, diagnose instruction, and a DE wrap bus.

## CE Checking

The data flow in the CE is checked in eight-bit bytes. Control
information is checked in bytes of varying length, CE error indica-
tions are divided into two groups: Check Register 1 and Check
Register 2. Located on the two indicators (CR 1 summary and CR 2
summary) that represent each group of error conditions. Either
indicator is activated whenever an error condition occurs within
it's associated group. Further isolation to the specific type of
error condition requires use of the roller charts.

## Half-Sum Check

A half-sum check indicates either incorrect parity on data entering
an adder or a failure in the adder half-sum generation circuits.

## Full-Sum Check

Full-sum checking, which is performed on the adder latches, checks
that correct parity has been generated for the developed sum.

## Check Registers

Two check registers are provided (Check Register 1 and Check Register
2) for presentation of check indications from CE checking circuits.

Fault detection circuits set a unique bit in the check registers.
The following table shows the bit assignment for each position of the
check registers. Both check registers are displayed on the CE Control
Panel and their contents are included in the logout information.

Whenever an appropriate bit is set in Check Register 1 or 2, the
CE will issue an ELC signal to all other CE's. Then if machine
checks are not masked (PSW bit 13 is on) the CE automatically logs
out and performs a machine check interruption. The CE logout is
initiated approximately 11 ms after the ELC signal is issued. If
machine checks are masked, the logout and machine check interruptions
are deferred until machine checks are not masked. In Test state,
manual controls may modify the internal operation upon the occurrence
of a malfunction, but the ELC signal is always issued upon the
occurrence of a malfunction unless Disable or Inhibit CE Hardstop
switches are active.

## Check Stop

A Stop-on-check feature is implemented in the CE. This causes the
CE to stop upon hardware detection of a failure. This stop occurs
at the end of the cycle in which the check is detected and, effectively
freezes CE status.

## CE Control Panel

The CE Control Panel (Figure 2-4) provides the controls and in-
dicators required to diagnose and repair machine malfunctions rapidly.
Controls and indicators provide for indication and control of power,
marginal checking, storage, data flow at normal speed, instruction

Table 2-5. Check Register Bit Assignment

CHECK REGISTER 1 (Roller 2 Pos 2)

| Ind Bit | Function | Ind Bit | Function |
|---------|----------|---------|----------|
| 0 | E Reg Parity | 22 | PADD Half-Sum 24-31 |
| 1 | PADD Full-Sum 4-7 | 23 | PADD Half-Sum 32-39 |
| 2 | PADD Full-Sum 8-15 | 24 | PADD Half-Sum 40-47 |
| 3 | PADD Full-Sum 16-23 | 25 | PADD Half-Sum 48-55 |
| 4 | PADD Full-Sum 24-31 | 26 | PADD Half-Sum 56-67 |
| 5 | PADD Full-Sum 32-39 | 27 | (PADD Half-Sum) Error |
| 6 | PADD Full-Sum 40-47 | | Trigger |
| 7 | PADD Full-Sum 48-55 | 31 | ROS Parity 2-42 |
| 8 | PADD Full-Sum 56-63 | 32 | ROS Parity 43-68 |
| 9 | PADD Full-Sum 64-67 | 33 | ROS Parity 69-99 |
| 18 | MPLR Decode Parity | 34 | SADD Half-Sum |
| 19 | PADD Half-Sum 4-7 | 35 | SADD Full-Sum |
| 20 | PADD Half-Sum 8-15 | | |
| 21 | PADD Half-Sum 16-23 | | |

CHECK REGISTER 2 (Roller 6 Pos 5)

| Ind Bit | Function | Ind Bit | Function |
|---------|----------|---------|----------|
| 10 | SAB Check | 22 | ATR Parity |
| 11 | SDBI Check | 23 | PSBAR Parity |
| 12 | Storage Timeout | 24 | PSBAR Not Configured |
| 13 | Address Check | 25 | PSBAR ALT Check |
| 14 | Data Check | 26 | Split Logout |
| 15 | Fetch Data Check | 28 | Log ROS |
| 16 | SE/DE LOS | 29 | Log ADR |
| 19 | Control Bus Check | 30 | CE Logout Request |
| 20 | LS Bus Check | 31 | Read Direct Timeout |
| 21 | CCR Parity | | |

Storage Check Register (Roller 6 Pos 5)

| Bit | Function |
|-----|----------|
| 0 | These bits are |
| 1 | decoded binarily |
| 2 | to determine which |
| 3 | SE or DE caused |
| | the check on a |
| | SE Timeout, Address, |
| | Data or Fetch check |

step and single cycle, data store and display, machine checks, and
testing.

Scan Logic

Provides the control logic necessary for the operation of FLT, ROS
Test, and logout functions.  FLT's check the CPU at the logic block
level.  ROS tests check each bit position of every ROS word. Log-
out stores the status of the console indicators in fixed positions
of main storage when a trouble symptom occurs.  The data logged out
may be subsequently recalled for analysis although the status of the
indicated logic is changed from what it was when the symptom appeared.

Fault Locating Tests (FLT's)

Data paths exist between main storage and the various CE registers
and triggers.  These paths allow any internal machine status to be
set according to the contents of main storage words (Scan in), and
also allow for the logging out of the internal status back to main
storage (Logout).  The Scan in mainly makes use of the normal data
paths while the logout uses a separate bus provided specifically for
that purpose.

Logout

The logout feature of the CE records, in fixed storage locations,
the state of the CE triggers.  The recording is accomplished by
storing binary bits that represent the states of the various triggers
and registers in the CE.  Logout is automatic following a CE machine
check with machine checks enabled (PSW 13 on and CE Check switch
in PROC), or it can be initiated manually by using the LOG OUT
pushbutton.  Logout is also initiated under program control by
the use of the diagnose instruction (log on count option).

   Automatic logout is enabled when the CE Check switch is set to
the PROC position.  The occurrence of a machine check with machine
checks enabled (PSW 13 on) forces the following sequence:

   1.  The CE clock is stopped (controlled clock) for 11 ms $\pm$ 1 ms.

   2.  The logout is executed

   3.  The CE is reset, the controlled clock is started, and an
       interrupt sequence is initiated.  This causes a fetch of the
       new machine check PSW and a store of the old PSW.  Before
       the store, the old PSW is set with an interrupt code of
       all 0's which denotes a CE internal machine check.

   Manual logout, which is initiated by pressing the LOG OUT push-
button, is effective only if CE is in the stopped state.

   By executing the Diagnose instruction, setting the MCW register
to some cycle count, bit position 6 on, and position 7 off, logout
is forced after the specified number of CE cycles have occurred
following the Diagnose instruction.

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Checks on Logout Circuitry. Most machine checks are ignored during logout. However, the following checks are mad on the logout circuitry and, if any occur during logout, they cause the appropriate bit to be set in Check Register 2 and the CE to check stop.

1. Log Address check - occurs if the CE attempts to store logout data in a location outside the CE logout area.

2. Log ROS Check - occurs if an address is encountered during logout which is not in the logout microprogram.

3. PSBAR parity check - occurs if a parity check is detected on the contents of PSBAR.

4. PSBAR alternate check - occurs when PSBAR stepping is required with the alternate latch already on .

5. Storage address or data check during logout.

Figure 2-3 shows the CE Logout format and the kinds of data recorded.

Marginal Checking

The marginal checking facility permits the operation of the CE with nonstandard voltage conditions, thus providing a means of detecting critical circuits that are deteriorating to a critical voltage-sensitive operating point. In addition, the CE may have its clock decreased from 200-ns to 195-ns, providing a means of detecting circuits that have developed slower switching speeds.

Diagnose Instruction

Those Diagnose kernels which are provided for maintenance use, and available only in state zero, cause certain predetermined functions to be performed according to the bit configuration of the Maintenance Control Word. Reference maintenance publications for the IBM 9020D/E Systems for further discussions.

Those Diagnose kernels which are available in all states are discussed in Chapter 8, IBM 9020D and 9020E System Principles of Operation manual.

DE Wrap Bus

A multiplex bus and a simplex test interface is provided on each CE to allow testing of the system Display Elements (DE). Two test operations, Force Request and Wrap, are available via the DIAGNOSE instruction while the CE is in state zero.

The Forced Request operation provides a facility to simulate solid Character Vector Generator (CVG) requests on the Display Generator (DG) interfaces of a selected DE.

The Wrap operation provides a facility which allows a CE to attack to a DG interface of a selected DE and to, once attached, simulate a DG by accepting data from the DE. Reference maintenance publications for the IBM 9020D/E Systems for further discussion.

INTRODUCTION

The Storage Element (SE) is a solid state element.  The IBM 7251-09
contains one SE within each physical package.  The basic cycle time
of the Basic Storage Module (BSM) is 750-ns.  Interleaving of Storage
accesses is permissible if successive references are to odd and even
addresses.  Interleaving allows a possible effective basic storage
cycle time of 400-ns.  This time is limited by the 400-ns cycle time
of the storage protect buffer.  The SE contains 524,288 bytes, each
byte consisting of eight data bits plus one parity bit.  Bytes can
be accessed by the Storage Element circuits only in groups of eight,
called doublewords.  Individual or multiple bytes within a word can
be operated upon or selected by various machine instructions or
operations.  Each SE contains its own power supply, back-up battery
power, and maintenance panel.

     Each SE can be accessed from any of four CE's and three IOCE's
honoring of accesses is controlled by a Configuration Control Reg-
ister and priority circuitry.  There is special interface circuitry
provided to buffer address and key information during IOCE accesses.
This feature allows the 7251-09, during IOCE accesses, to appear in
timing and function the same as the 7251-03/04/08.

     Since the 7251-09 cycle is much faster than the IOCE cycle, the
request from an IOCE is honored at the point within the IOCE cycle
when a storage cycle is required.  When the IOCE is fetching data,
the request is honored immediately.  If the IOCE is performing a
store operation the IOCE request is delayed at the SE until the store
signal drops.  The IOCE drops the Store signal approximately 780-ns
after starting the Storage Ring clock.  In either case the SE cycle
time for an IOCE cycle is 800-ns, with other users capable of utiliz-
ing the storage during the remainder of the IOCE cycle.

     When a CE or IOCE is perfroming "AND, OR, or EX-OR" immediate
instructions (requiring two cycles) a double cycle request is sent
to the SE.  This line guarantees the accessing element two successive
SE cycles before any other user's access request is honored for that
BSM.

     If a CE cycle with double cycle request is honored prior to an
IOCE request to the same side (odd or even), both CE cycles are
granted.  The IOCE cycle (in core) is delayed by the amount of time
required to service the CE.

     Accompanying each SE (65,536 doublewords) is an associated core
storage used for storing keys for storage protect functions.

FUNCTIONAL CHARACTERISTICS

## Basic Storage Module

There are four Basic Storage Modules (BSM) in each SE. Each BSM
(131,072 bytes) is a coincident-current magnetic core storage unit.
Two of the BSMs are associated with odd doubleword accesses and the
other two are associated with even doubleword accesses. There are
two Storage Element Storage Address Registers (SESAR), one for the
two odd BSMs and the other for the two even BSMs. There are four
Storage Element Storage DAta Registers (SESDR), one within each BSM.
Contents of the BSM's are preserved under normal power on-off seq-
uences by proper sequencing of the DC voltages in the BSM circuitry.
Normal sequencing will not be maintained under abnormal failure
conditions.

## Storage Protect

The Storage Protect Buffer (SPB) is a 400-ns core buffer (256 bytes,
1 key per byte) used in conjunction with the storage protect feature.
Each key position consists of four key bits, one fetch protect bit
plus parity. Each block of 2,048 bytes of the Storage has a storage
protect key associated with it. Each access of a doubleword in
Storage results in accessing of the storage protect buffer for the
associated storage key. The storage key readout of the SPB is com-
pared with a protection key sent by the accessing element. The
first four bits (bits 0-3) of the storage key are used to protect
storage from being altered. If the fifth bit of the storage key
(bit 4) is set to a one, the first four bits are used to determine
whether the data in the accessed location is fetch protected. If a
store operation is attempted and no match occurs, a Storage Protect
Check is indicated to the accessing element and no data is stored.
When fetch protect is in effect, if a fetch type instruction is
attempted, and there is no match, a Storage Protect Check also occurs.
The storage protect keys can be accessed or altered by a CE under
control of the Insert Storage Key (ISK) and Set Storage Key (SSK)
instructions respectively.

During Insert Storage Key, the SPB Key specified by the internal
Storage Address Bus (SAB) bits 1 through 7 plus Hi/Lo bit of the
Address is red out to the accessing CE element.

During Set Storage Key, the SPB Key location specified is re-
placed with the contents of the key sent by the CE. See the "Check-
ing" section for details of checking for ISK, SSK and normal access-
ing.

The contents of the storage protect buffer are preserved during
nromal power on-off sequences.

DESIGN DETAILS

The 7251-09 contains the following registers:

## Storage Element Storage Data Register (SESDR)

There are four SESDRs, one associated with each BSM.  Each register contains 64 data bits and 8 parity bits.  The SESDR is set by the sense amplifier outputs (Figure 3-1), the bit switches on the maintenance panel, or any of up to seven external elements.  Contents of these registers can be indicated on the maintenance panel in test mode (one at a time-dependent on address selected).  These registers feed the inhibit circuitry of the associated BSMs and one set of drivers to each external element.  Output of these registers also feed parity checking circuitry.  Storage Check (IOCE) or Data Check (CE) is sent to the accessing element if a parity check is detected.

## Storage Element Storage Address Registers (SESAR)

There are two SESAR's one for the two even BSMs and one for the two odd BSMs.  Each SESAR contains 14 address bits and 2 parity bits.  The address bits determine which one of the 32K doublewords will be accessed in the selected pair of BSMs.

Storage Check (IOCE) or Address Check (CE) is sent to the accessing element if a parity check is detected.  The SESAR can be set by the address switches on the maintenance panel, the output of the test counter, or by any of up to seven external elements.  Inputs to the high order half are paralleled to the address register of the SPB.  This register feeds the address matrix of the BSM, and the logout circuitry.  It also feeds parity checking circuits.  The contents of the register are indicated on the maintenance panel.

## IOCE Storage Address Buffer Registers (SABR)

There are three SABRs, one associated with each IOCE.  The SABR buffers the address from the IOCE.  At the proper time the contents of the SABR are gated to the appropriate SESAR.

The SABR is set from bit positions 8 to 31 of the Storage Data Bus In (Figure 3-2).  Bits 14 to 27 of SDBI (bit 6-19 SABR) are subsequently transferred to bits 1-14 of the SESAR.  Bit 21 of SABR is used to determine which half of the data word (bytes 0-3 or 4-7) is affected by this IOCE cycle.  Bits 22 and 23 of SABR are used to determine the specified byte on a Test and Set operation.  Bits 1-4 (SABR) are sent to the Box Tag compare logic.  Bit 5 is sent to the Hi/Lo selection logic.

## Configuration Control Register

The Configuration Control Register (CCR) is a 16-bit (plus two parity bits) register which controls communication to the storage element.  Each SE contains a configuration register.

Seven configuration bits (CE 1-4 and IOCE 1-3) control all normal accesses to the Storage Element.  If the configuration bit is a one accessing is allowed from the specified element; if a zero, no access is allowed.

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Four SCON bits (SCON 1-4) control requests from CEs to alter the configuration register. Reconfiguration requests may come only from the Computing Elements (1-4). If a SCON bit is one, a reconfiguration request from that CE is honored. If the SCON bit is zero the request is ignored. If all SCON bits are zero and the State bits are other than zero, or a CCR parity error exists a request will be honored from any CE.

If more than one reconfiguration request is received at the SE at the same time, the results of the reconfiguration action cannot be guaranteed. However, through proper programming, this situation should not occur. Reconfiguration requests take priority over all access requests. The reconfiguration is delayed only by the time necessary to complete the present storage cycle.

Upon completion of a reconfiguration, contents of the storage CCR are parity checked. (Checking is continuous except during re-configuration). If the CCR has proper parity, a response is sent to the issuing CE. If improper parity is detected, ELC is sent. An invalid address condition is generated within an element whenever it is configured away from an SE before its access request is honored with an accept.

The state bits (S0, S1) are used to define the four operating states a storage element may assume.

| S0 | | S1 | | State |
|----|----|----|----|-------|
| On | (1) | On | (1) | Three |
| On | (1) | Off | (0) | Two |
| Off | (0) | On | (1) | One |
| Off | (0) | Off | (0) | Zero |

See Chapter 8 for further definition of these states.

A test switch is provided to increase the flexibility of the zero state.

If the storage element is in zero state and the Test switch is in the normal position (off):

1. All maintenance controls are inactive **except Lamp Test** (See **Table 3-1 for details**).

2. The storage element may be reconfigured as defined by its SCON bits.

3. Power On-Off is inactive.

If the storage element is in zero state and the Test switch is in the Test Position (On):

1. All maintenance controls are active (see Table 3-1 for details).

●Figure 3-1. SE Data Flow

3-5/3-6

STORAGE
DATA
BUS
IN

SDBI 00-31   00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31   $P\frac{00}{07}$ $P\frac{08}{15}$ $P\frac{16}{23}$ $P\frac{24}{31}$

SDBI 32-63   32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63   $P\frac{32}{39}$ $P\frac{40}{47}$ $P\frac{48}{55}$ $P\frac{56}{63}$

DATA
CE

SDBI 00-31   00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31   $P\frac{60}{67}$ $P\frac{08}{15}$ $P\frac{16}{23}$ $P\frac{24}{31}$

SDBI 32-63   32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63   $P\frac{32}{39}$ $P\frac{40}{47}$ $P\frac{48}{55}$ $P\frac{56}{63}$

DATA
IOCE

SDBI 00-31   00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31   $P\frac{00}{07}$ $P\frac{08}{15}$ $P\frac{16}{23}$ $P\frac{24}{31}$

KEY AND
ADR
IOCE

KEY: 0 1 2 3     ADDRESS: 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23
SDBI 00-31   $P\frac{00}{07}$ $P\frac{08}{15}$ $P\frac{16}{23}$ $P\frac{24}{31}$

CONFIGURATION
CE

SDBI 32-63   STATE: 80 S1   SCON: 1 2 3 4   SPARE SPARE   ///   CE: 1 2 3 4   SPARE   IOCE: 1 2 3   $P\frac{32}{39}$ $P\frac{40}{47}$ $P\frac{48}{55}$ $P\frac{56}{63}$

STORAGE ADDRESS BUFFER REGISTER
(IOCE CYCLE)
SDBI 08-31

NOT USED: 00   BOX TAG: 01 02 03 04   NOTE 1: 05   SESAR 1-14: 06 07 08 09 10 11 12 13 14 15 16 17 18 19   NOTE 2: 20   NOTE 3: 21   NOTE 4: 22 23
$P\frac{00}{07}$ $P\frac{08}{15}$ $P\frac{16}{23}$

STORAGE ADDRESS REG
SABR 06-19 OR SAB 06-19

SESAR 1-14: 01 02 03 04 05 06 07 08 09 10 11 12 13 14
$P\frac{01}{07}$ $P\frac{08}{14}$

STORAGE ADDRESS BUS
(CE CYCLE)

BOX TAG: 01 02 03 04   NOTE 1: 05   SESAR 1-14: 06 07 08 09 10 11 12 13 14 15 16 17 18 19
$P\frac{01}{05}$ $P\frac{06}{12}$ $P\frac{13}{19}$

NOTE 1 – BIT 05 = 0 SELECTS LO
BIT 05 = 1 SELECTS HI
NOTE 2 – BIT 20 = 0 SELECTS EVEN
BIT 20 = 1 SELECTS ODD
NOTE 3 – BIT 21 = 0 SELECTS DATA BITS 00 – 31 (IOCE CYCLE)
BIT 21 = 1 SELECTS DATA BITS 32 – 63 (IOCE CYCLE)
NOTE 4 – BITS 22 – 23 SELECT BYTE ON TEST AND SET OPERATION (IOCE CYCLE)

Figure 3-2.  Storage Communication Formats

Table 3-1. SE Switches and Their Operational Environment

| | State Zero | |
| --- | --- | --- |
| | Test Switch Off | Test Switch On |
| Element MPO Pull | X | X |
| Marginal Test | X | X |
| Test Switch | X | X |
| Lamp Test | X | X |
| Storage Test | | X |
| Power On/Off/Reset | | X |
| Start | | X |
| Stop | | X |
| Reset | | X |
| Set Configuration | | X |
| Address | | X |
| Rev. Adr Parity | | X |
| Data Entry | | X |
| In Key | | X |
| Key | | X |
| Mark Keys | | X |
| Store/Fetch | | X |
| Priority/Storage | | X |
| Reset Mode | | X |
| Stop On Check Test | | X |
| Cancel | | X |
| SCON | | X |
| Test & Set | | X |
| Logout Stop | | X |
| Double Cycle Test Time Out | | X |
| Stop on Check Test | | X |
| Worst Case/Data Keys | | X |
| Priority | | X |

2.     The storage element cannot be reconfigured from an external source.

3.     Power On-Off is active.

4.     The storage is logically isolated from all other elements.

All resets (with the exception of Test to Normal reset) coming into the configuration register turn all SCON bits on, and other positions of the register off. Proper parity is maintained. The contents of the configuration register indicate the state: Three, Two, One, Zero.

Test to Normal Reset, resets the state bits, and corrects parity for the SCON byte. The communication bits and SCON bits are not altered.

## Storage Protect Buffer (SPB)

The Storage Protect Core array consists of a 256 byte buffer. The SPB is accessed each time a request is made for a storage cycle. Each of the 256 bytes contains a storage protect key. Each key protects 256 main core addresses (2048 bytes).

The SPB receives Storage Address Bus (SAB) bits 1 through 7 plus the status of the Hi/Lo select bit. These bits are inserted into the Storage Protect Address Register (SPAR) which controls accessing the correct byte (key). The selected key is latched in the Storage Protect Out Key Register (SPOKR) for comparison on a store or fetch (fetch protect bit on) operation or transfer to a CE user on an Insert Key operation. On Set Storage Key (SSK), the key from the Storage Protect In Key Register (SPIKR) will be gated into the storage protect array.

The contents of the SPIKR and SPOKR are indicated on the maintenance panel.

## LOGOUT

The Storage Element has the ability to place its latched information on the SDBO. Following receipt of a Logout Stop Signal from the accessing element the SE will accept Logout Select and Logout Word Number signals from any computing element.

Format of these words is shown in Figure 3-3. The Computing Element controls the sequencing and gating of these words. The SE logout is placed in a storage location defined by the Diagnose instruction. The SE will send a signal (SE stopped) to all elements indicating that it has been stopped for logout.

Storage must be stopped to logout. Logout Stops will be accepted only from those elements configured to the storage. Storage will remain stopped until a Logout Complete (or a reset signal) is received from a CE during logout. The SE issues an ELC signal to all CE's upon initiation of SE Stopped condition.

3-10

BIT POSITIONS IN MAIN STORAGE

| WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | \<----------------------------------------- SESDR (EVEN) (or IOCE SBO) -----------------------------------------\> 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SESDR (EVEN) |
| 1 | \<----------------------------------------- SESDR (EVEN) -----------------------------------------\> 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SESDR (EVEN) |
| 2 | MARKS (EVEN): 0-7, 8-15, 16-23, 24-31, 32-47, 40-47, 48-53, 54-63; TAG (EVEN) 1 2 3 4; HI/LO 5; IOCE SAB (EVEN) 6 7 8 9; SESAR 1-14 (EVEN) 10 11 12 13 14 15 16 17 18 19; IOCE SAB 20 21 22 23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | MARKS, SESAR (EVEN) |
| 3 | CCR (8-15): CE 1 2 3 4, BIT 12, IOCE 1 2 3; REQUEST (EVEN): CE 1 2 3 4, IOCE 1 2 3; RESPONSE (EVEN): CE 1 2 3 4, IOCE 1 2 3; STATE S0 S1; CCR (0-7): SCON 1 2 3 4, BIT 6, BIT 7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | CCR, REQUEST AND RESPONSE LATCHES (EVEN) |
| 4 | SE ID 1 2 3 4; OPERATION ISK SSK; OPERATION (EVEN) T&S STORE FETCH, SUPP LOG CHK; BLK SEL LATCH EVEN ODD; SCON BACK UP LATCHES 1 2 3 4; MARK PARITY (EVEN); ADDR PARITY 1-5 0-7, 6-12 8-15, 13-19 16-23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | TYPE OF OP (EVEN) |
| 5 | CHECK CONDITION (EVEN): MARK PARITY CHK, ADDR PARITY CHK, DATA PARITY CHK, SP PARITY CHK, KEY, NORMAL OP CHK; CHECK CONDITIONS (COMMON): CCR, TAG PARITY CHK, TAG, SAB (IOCE), SBO (IOCE); OBS, OTC THERMAL; CCR PARITY 0-7, 8-15; SBO (IOCE) 0-7, 8-15, 16-23, 24-31; SESDR PARITY (EVEN) 32-39, 40-47, 48-55, 56-63 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | CHECKS (EVEN AND COMMON), SESDR (EVEN) |
| 6 | \<----------------------------------------- SESDR (ODD) -----------------------------------------\> 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SESDR (ODD) |
| 7 | \<----------------------------------------- SESDR (ODD) -----------------------------------------\> 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SESDR (ODD) |
| 8 | MARKS (ODD): 0-7, 8-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-63; TAG (ODD) 1 2 3 4; HI/LO 5; IOCE SAB (ODD) 6 7 8 9; SESAR 1-14 (ODD) 10 11 12 13 14 15 16 17 18 19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | MARKS, SESAR (ODD) |
| 9 | REQUEST (ODD): CE 1 2 3 4, IOCE 1 2 3; RESPONSE (ODD): CE 1 2 3 4, IOCE 1 2 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | REQUEST AND RESPONSE LATCHES (ODD) |
| 10 | SPIKR: P 0-4, 0, 1, 2, 3, 4; SPOKR: P 0-4, 0, 1, 2, 3, 4; OPERATION (ODD): T&S STORE FETCH, SUPP LOG CHK; MARK PARITY (ODD); ADDR PARITY 1-5 0-7, 6-12 8-15, 13-19 16-23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SPIKR, SPOKR, TYPE OF OP (ODD) |
| 11 | CHECK CONDITION (ODD): MARK PARITY CHK, ADDR PARITY CHK, DATA PARITY CHK, SP PARITY CHK, KEY, NORMAL OP CHK; SPAR: P X Y 2 3 4 5 6 7; SESDR PARITY (ODD) 0-7, 8-15, 16-23, 24-31, 32-39, 40-47, 48-55, 56-63 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | CHECKS (ODD), SPAR, SESDR (ODD) |

Figure 3-3. SE Logword Formats

Interface Switching Control

Input Switching

The input switch, under control of the priority controls, gates one
of seven CE/IOCE to SE busses.  The outputs of the switch feed the
SE storage data registers, the SE Storage Address Registers, the
Configuration Register, the Storage Address Buffer Registers, the
Mark Registers, the Storage Protect Address Register, and the
Storage Protect In Key Register.

Output Switching

The output switch, under control of the Logout, ISK, or normal access-
ing controls, gates the specified data onto one of three 36-bit IOCE
output busses, one of four 72-bit CE output busses, or one of four
6-bit Out Key busses.  Data is gated only to the requesting unit.

Test Counter

The Test Counter is a 14-bit binary coupled counter used to address
storage in the zero state with the Test switch on.  The counter is
stepped once for each consecutive storage access so long as the
appropriate controls are enabled.  Depression of the Reset and Start
switches will cause addressing to begin at word 1.  The counter out-
put is gated to the SE input switch at address time to simulate
system operation.  Parity generation is automatic, thus allowing
normal error checking.

Priority Controls

The 7251-09 SE's, which provide interleaved accesses, contain two
separate sets of priority circuitry; one set for granting accesses
to odd doubleword accesses, the other set for even doubleword access-
es.  Each set of priority circuitry operates, for the most part,
independently of the other with respect to granting access priority,
the major interdependence being their common usage of the Storage
Protect Buffer facility and common data paths.  Consequently, unless
stated otherwise, the following discussion represents the character-
istics of either an odd or even set of priority circuitry, the other
set having identical characteristics.

    The SE priority circuitry accepts access requests from up to
three IOCE's and four CE's, the IOCE's having access priority over
the CE's.  Priority within each element type (IOCE or CE) is primarily
given on a first in - first out basis except for simultaneous re-
quests which are serviced in ascending order, e.g., IOCE 1, 2, 3.

    Two levels of priority latches exist for both IOCE and CE access
requests (see Figure 3-4).  Requests from CEs and Fetch Requests from
IOCE's enter level 1 priority immediately, while an IOCE Store Request
is inhibited from entering level 1 until the IOCE drops the Store
signal.  The SE services both IOCE and CE requests pending at level
#2 in ascending priority sequence within element type.  Upon servic-

ing all level #2 IOCE requests or CE requests, the SE will scan in
all pending level #1 requests to level #2 for the IOCE's or CE's,
respectively.  Subsequent requests from the element(s) will then
accumulate at level #1 until all level #2 requests are serviced for
the particular element(s).  If no IOCE requests are stacked in level
#2, an IOCE request will go immediately from level #1 to level #2 and
may gain priority over a CE request pending at level #2.  A sample
odd or even priority sequence is shown in Figure 3-5 while a sample
odd and even priority sequence is shown in Figure 3-6.
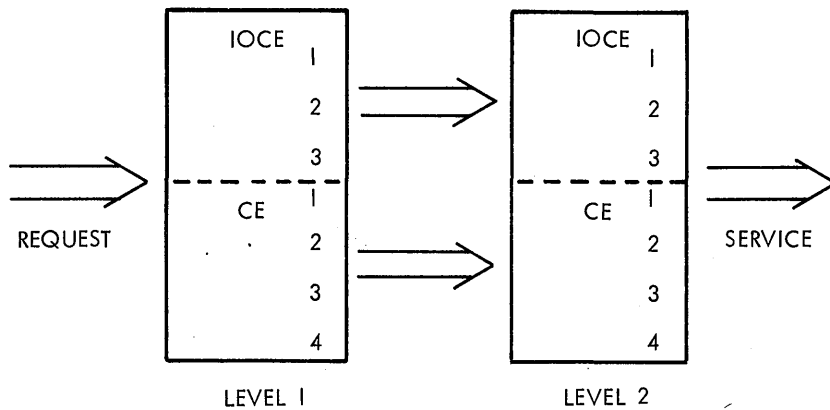
Figure 3-4.  SE Priority Levels

IOCE'S FETCHING

SE NOT BUSY | IOCE 1 | CE 1 | CE 2 | IOCE 2 | CE 3 | IOCE 1 | CE 1 | SE NOT BUSY | CE 2

SCAN 1  SCAN 2  SCAN 3  SCAN 4  SCAN 5  SCAN 6  SCAN 7  SCAN 8  SCAN 9

IOCE'S STORING

SE NOT BUSY

SE NOT BUSY | CE 1 | IOCE 1 | CE 2 | IOCE 2 | CE 1 | IOCE 1 | CE 3 | CE 2

SE NOT BUSY

SCAN 1  SCAN 2  SCAN 3  SCAN 4  SCAN 5  SCAN 6  SCAN 7  SCAN 8  SCAN 9  SCAN 10

SELECT IN SIGNALS

CE 1         CE 2         CE 3  CE 1                CE 2
IOCE 1              IOCE 2         IOCE 1
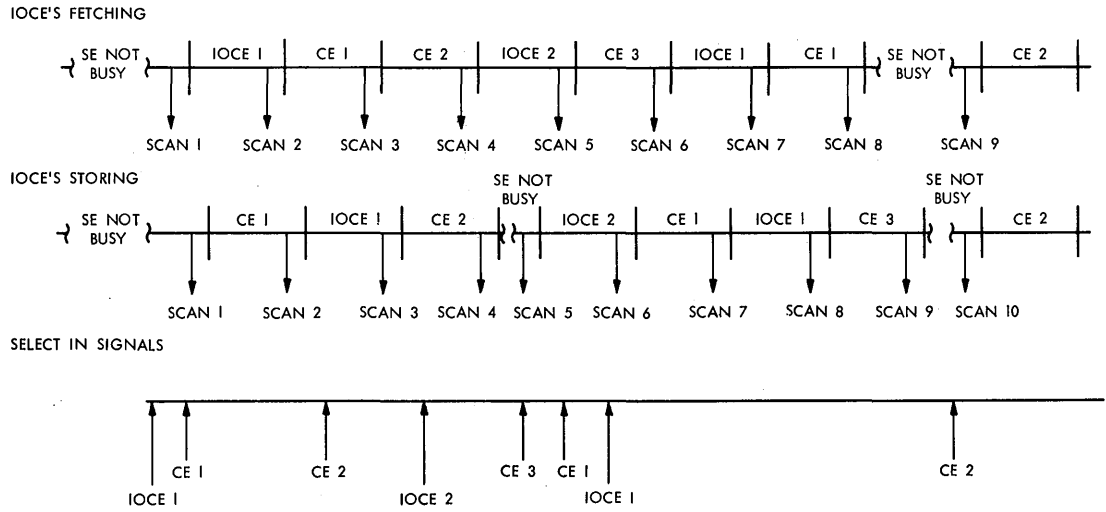
IOCE FETCHING

1. IOCE-1 Select initiates SCAN-1

2. IOCE-1 awarded storage cycle

3. SCAN-2 awards 2nd cycle to CE-1

4. SCAN-3 awards cycle to CE-2

5. SCAN-4 awards cycle to IOCE-2

6. SCAN-5 awards cycle to CE-3

7. SCAN-6 picks up IOCE-1 and CE-1 selects and awards cycle to IOCE-1

8. SCAN-7 awards cycle to CE-1

9. SCAN-8 finds no requests and SE goes not busy

10. CE-2 select initiates SCAN-9 and awards cycle to CE-2

IOCE STORING

1. CE-1 Select initiates SCAN-1

2. CE-1 awarded storage cycle (IOCE select has not entered level 1 priority)

3. SCAN-2 awards 2nd cycle to IOCE-1

4. SCAN-3 awards cycle to CE-2

5. SCAN-4 finds no user requests (IOCE select has not entered level 1 priority)

6. IOCE-2 Request delayed 780ns initiates SCAN-5 and IOCE-2 is awarded cycle.

7. SCAN-6 picks up CE-1 and CE-3 selects and awards cycle to CE-1

8. SCAN-7 finds IOCE-1 request (delayed) and grants IOCE-1 priority over CE-3.

9. SCAN-8 awards cycle to CE-3

10. SCAN-9 finds no user requests and SE goes not busy

11. CE-2 select initiates SCAN-10 and awards cycle to CE-2

Figure 3-5. SE Odd or Even Priority Sequence

IOCE FETCHING                    IOCE STORING
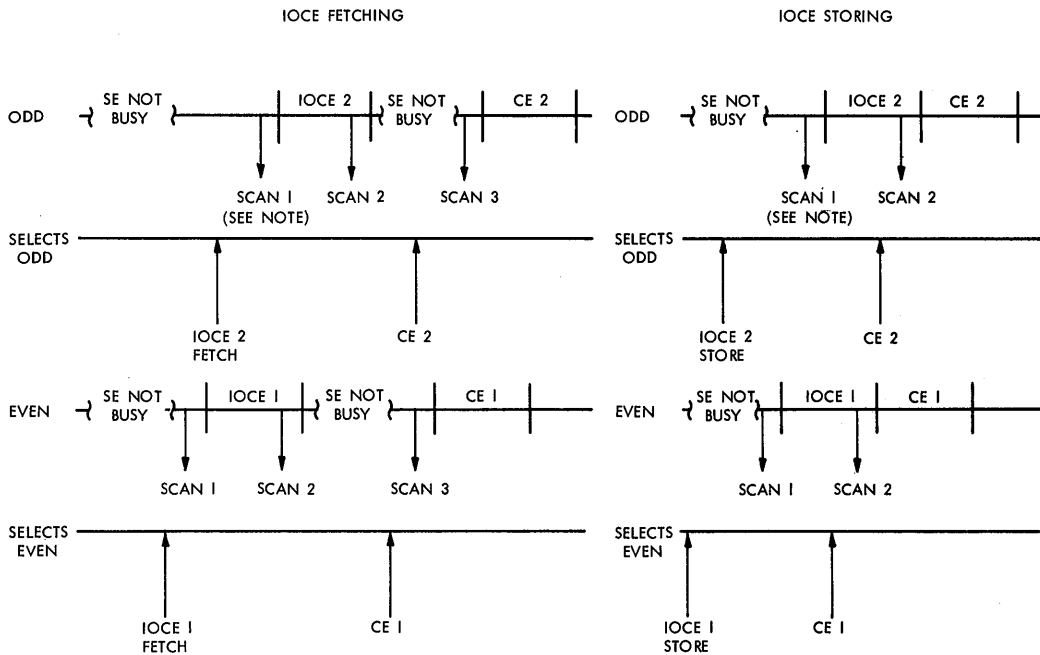


NOTE: ODD SCAN IS INITIATED BY EVEN CLOCK.

IOCE FETCHING

1. Odd and Even Storages are not busy. IOCE-1 select Even initiates SCAN and receives Even cycle.

2. IOCE-2 Select Odd arrives. 400ns after the Even SCAN an Odd SCAN is initiated which awards the Odd cycle to IOCE-2.

3. Even SCAN-2 finds no requests pending. 400ns later Odd SCAN-2 finds no requests and SE goes not busy.

4. CE-1 Even Select arrives which initiates Even SCAN-3 giving CE-1 the next even cycle.

5. 400ns later an Odd SCAN finds CE-2 request and grants CE-2 the next cycle.

IOCE STORING

1. Odd and Even Storages are not busy. IOCE-1 select Even arrives. Approximately 400 ns later IOCE-2 Odd Select arrives. The SE remains not busy.

2. 780ns after the arrival of IOCE-1 Select, Even SCAN-1 is initiated and IOCE-1 is awarded the following Even cycle.

3. 400ns after Even SCAN-1, an Odd SCAN is initiated. The Odd SCAN awards IOCE-2 the next Odd cycle.

4. Even SCAN-2 awards the next Even cycle to CE-1.

5. 400ns later Odd SCAN-2 awards the next Odd cycle to CE-2.

Figure 3-6.   SE Odd and Even Priority Sequence

Box Tag Status

A Storage Element decodes the high order bits of the address sent
from an accessing element to determine if the address associated
with the select lies in the selected element.  If the address does
not lie within the selected element the SE will generate a Storage
Check (IOCE), or Address Check (CE) signal and force a regeneration
cycle.

Fetch

During fetch cycles, data read from the BSMs is gated from the
appropriate SESDR to the accessing element's Storage Data Bus Out
(SDBO).  If SESDR has incorrect parity, it is not corrected, but is
placed back into the BSM with incorrect parity.  During CE Fetch
cycle, parity checks are made on SESAR, SESDR, SPIKR and SPOKR.
During the IOCE Fetch cycle parity checks are made on SESAR, SESDR,
SPIKR, SPOKR.

Store

Storing of information into one of the four BSMs is controlled on a
byte basis by the Byte Stats (IOCE) or Mark bits (CE).  During the
read portion of the STORE cycle, data bytes whose stats or mark bits
are not On are read into the BSM's SESDR.  The bytes from the access-
ing element whose stats or mark bits are on are gated from the Storage
Bus In (SBI) to the appropriate SESDR.  These byte positions and the
byte positions to be regenerated are then parity checked during the
write portion of the store cycle.  If bad parity is detected in the
SESDR, the bad word is placed into storage and a storage check (IOCE)
or data check (CE) is sent to the accessing element.

Test and Set

During the execution of test and set, the storage element will fetch
the BSM contents specified by the address.  These contents are gated
into SESDR at normal fetch time.

    The contents of the byte specified by Address bits 21, 22, 23
(IOCE Cycle) or the mark bits (CE Cycle) will be replaced with all
ones.  All other bytes will be regenerated.  Normal parity checking
will occur.  The original contents of the altered byte will be sent
to the accessing element on its SDBO.

Checking

Nine types of check signals may be generated and transmitted to the
system as follows:

| Check Signal | Sent To |
| --- | --- |
| Element Check | All CEs |
| Storage Check | Accessing IOCE |

3-17

| | |
|---|---|
| Storage Data Check | Accessing CE |
| Storage Address Check | Accessing CE |
| Storage Protect Check | Accessing CE or IOCE |
| Logic Check | System Console or Configuration Console |
| Power Check | System Console or Configuration Console |
| On Battery | System Console or Configuration Console |
| Emergency Power Off* | System Console or Configuration Console |

*(Consist of 3-wire EPO Interface)

Element Check

Element Check is sent to all attached computing elements without regard to storage element configuration register or to accessing controls. Checks within this area are:

1. Configuration register parity
2. Marginal temperature
3. On battery
4. Storage check
5. Data check
6. Addressing check
7. Double cycle time out
8. Box tag parity or mismatch
9. Multi accept
10. Normal Op check

    A 525-ns pulse is issued when one of the above conditions is detected.

11. Over-voltage or over current
12. Normal Power Off, Master Power Off (MPO), or loss of power.
13. SE stopped signal (Note: Element check is reset upon Logout complete).
14. Catastrophic temperature (results in power off).

A static element check will be issued upon detection of one of the conditions 11 through 14. The ELC will remain on until the condition has been cleared.

Storage Check (IOCE)

This line is generated by parity check errors (except configuration register parity check errors) to request a logout stop. This signal is gated only to the accessing IOCE at the time the error is detected. At the time of the check condition the SE will go into a 2.5usec time out condition and stop at the end of the current cycle(s) in progress. Simultaneously with the storage check signal, a pulsed ELC will be issued to all CE's.

If Logout Stop has not been signaled by the accessing element, the SE will proceed following the 2.5usec timeout and the error information latches will be reset.

Data Check and Address Check (CE)

The Data Check and Address Check signals are handled in a manner identical to the storage check except they are sent to the accessing CE.

The SESDRs, SESARs, SPIKR, and SPOKR, have parity checking on a byte basis. The associated SESAR (odd or even) and SESDR (Odd Hi, Odd Lo, Even Hi or Even Lo) are parity checked during each storage cycle. Any detected error will be signaled to the accessing element. If a parity error is detected in the SESAR the accessed location will be regenerated. If a parity error is detected in the SESDR during fetch or store the doubleword is written back into storage with incorrect parity. SESDR and IOCE SDBI parity checking is disabled during Suppress Log Check cycles.

Storage Protect Buffer Parity Checking

The SPIKR and SPOKR are parity checked on all cycles. Box Address Checking occurs on all cycles and forces a storage check (IOCE's) when the address sent to the SE does not lie within the SE accessed (mismatch). Pluggable means exist to define the address available within a storage element. These will be plugged at system installation time.

Storage Protect Check

A Storage Protect Check signal is generated when the four data bits sent by the accessing element do not match the four data bits of the key in the SPB. There is no compare initiated on ISK or SSK cycles. During all Fetch cycles, if the fetch protect bit is a one, the four bit In Key must compare to the Storage Protect Key. During all fetch and store cycles, if either key (In Key or Storage Protect Key) is all zeros no match is required. On a mismatch a Storage Protect Check is sent to the user and the accessed location will be regenerated.

Logic Check

Logic Check is a signal sent to the System Console or Configuration Console whenever the ELC is energized. The ELC is an OR of all check

conditions (except Protect Check) within the SE.  Protect Check is a
program error and is not included in Logic Check.

MAINTENANCE PANELS

These panels contain facilities to allow off-line maintenance of tne
SE and contain indications of the SE status.  (Figures 3-7, 3-8 and
3-9.)  These facilities include:  indicators, Table 3-2; pushbutton
switches, Table 3-3; and toggle switches, Table 3-4.

    All manual switches and pushbuttons on the SE maintenance panel
are under control of the CCR State bits and the Test switch.  The
Test switch is active only in state zero.

    On the power control panel the Power On/Off/Reset switch is
under control of the CCR state bits and Test switch.  Voltages may be
monitored in any state.  The Marginal Check Controls, Thermal Reset
function of the Power On/Off/Reset switch, and Element MPO switch are
always operational.

    In addition to the controls and indicators shown in Figures 3-8
and 3-9 the following momentary contact switches are located in the
SE power section and are always operational.

OTC Test - Simulates the thermal warning condition and causes ELC to
be sent to all CE's.

Table 3-2.  Indicators

| Title | Number of Indicators |
|-------|----------------------|
| Data Reg | 72 |
| Address Reg (even) | 17 |
| Address Reg (odd) | 17 |
| Address Counter | 17 |
| Storage Protect Out Key Reg | 6 |
| Storage Protect In Key Reg | 6 |
| Storage Protect (address)    (check) | 1 |
| Storage Protect (Key)    (check) | 1 |
| Storage Protect (SAP)    (check) | 1 |
| Configuration Control Reg | 18 |
| Data Byte (even)    (check) | 8 |
| Data Byte (odd)    (check) | 8 |
| Marks (even) | 9 |
| Marks (odd) | 9 |
| Fetch (even) | 1 |

Table 3-2.  Indicators (cont.)

| Title | Number of Indicators |
|---|---|
| Fetch (odd) | 1 |
| Mark (even)                         (check) | 1 |
| Mark (odd)                          (check) | 1 |
| Storage Address Reg.(even)      (check) | 1 |
| Storage Address Reg.(odd)       (check) | 1 |
| Normal Op (even)                  (check) | 1 |
| Normal Op (odd)                   (check) | 1 |
| Logout Stopped | 1 |
| Tag (parity,compare)              (check) | 2 |
| IOCE SBI                           (check) | 1 |
| Multi-accept                       (check) | 1 |
| Compare Check                    (check) | 1 |
| Double Cycle Time-Out           (check) | 1 |
| Test Stop | 1 |
| Configuration Parity              (check) | 1 |
| Priority Status Request | 7 |
| Priority Status Request | 7 |
| Test | 1 |
| Driver On                (SSU Power Panel) | 1 |
| SSU Power Check      (SSU Power Panel) | 1 |
| DC On                    (SSU Power Panel) | 1 |

Table 3-3. Pushbutton Switches

| Title | Description | Number of Switches |
|-------|-------------|--------------------|
| Set Config | Gates contents of appropriate Data switches to Configuration Register | 1 |
| Start | Initiates a storage cycle Further operation is controlled by the status of other switches. | 1 |
| Stop | Stop storage cycles at end of current cycle. | 1 |
| Reset | Resets all error indications ot zero. Stop any operation at end of write portion of cycle. | 1 |
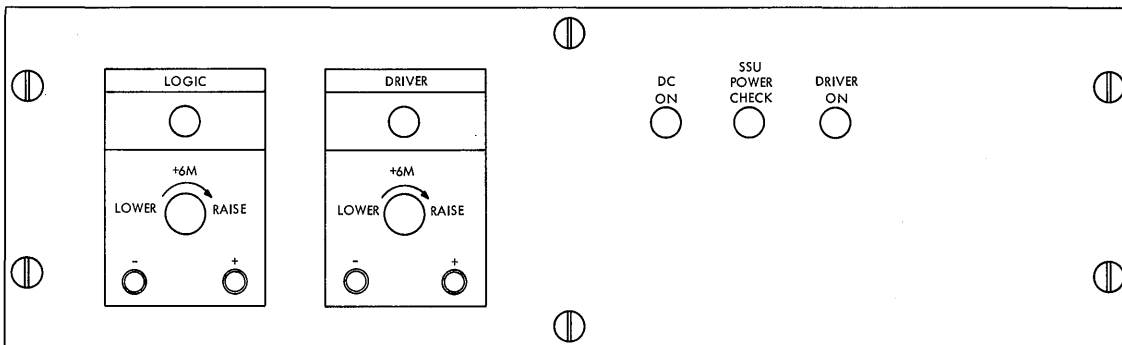


Figure 3-7. Power Control Panel

Table 3-4. Toggle Switches

| Title | Description | Number of switches |
|-------|-------------|--------------------|
| Power ON/Off/Reset | This switch provides Power ON/OFF function in State zero with the test switch ON. The Reset position provides a unit thermal reset function. | 1 |
| Indicator Test | Test all SE logic indicators on maintenance panel. | 1 |
| Test/Normal | This switch in the Test Position (with SE in State Zero will activate all manual switches and provides isolation from all other System Elements. | 1 |
| Data Entry | Eight data switches plus parity are provided to store any bit combination into a specified location These switches in conjunction with the Mark Key switches specify the data and byte (or bytes) to be stored. During a fetch operation the contents of the specified location are compared to the Data Entry Switch settings. These switches are also used to set information into the CCR and simulate the Logword number interface. | 9 |
| Storage Address | Used to facilitate all address functions for both IOCE and CE cycles. | 23 |
| Stop on Check Test | When this switch is in the On position any check condition will stop the test panel clock for operator intervention. | 1 |

Table 3-4.  Toggle Switches (cont.)

| Title | Description | Number of Switches |
|-------|-------------|--------------------|
| Store/Fetch | Determines Store or Fetch operation.  In the Fetch Position data received from storage is compared with the Data Entry Switches. | 1 |
| SCON Cont/Single | In the Single Position the CCR is loaded once per depression of the Set Configuration Pushbutton. In the Cont. Position the CCR is loaded repeatitively. | 1 |
| Reset Mode | This switch provides a reset and restart function to allow cycling on an error condition. Auto Position - A reset and restart is forced similar to depressing Check Reset and Start pushbutton. Manual Position - Normal operation occurs dependent upon other switch functions. | 1 |
| Priority/Storage | Priority Position - the seven Priority switches are enabled to test the SSU's logic.  Also the Priority scan logic is exercised. Storage Position - Priority logic is bypassed. | 1 |
| Data Keys/ Worst Case | Data Key Position - Nine (P,0-7) Data Entry switches are used. Worst Case Position - a Worst Case pattern is automatically loaded into storage. | 1 |

Table 3-4. Toggle Switches (cont.)

| Title | Description | Number of Switches |
|---|---|---|
| Cancel | A cancel pulse shall be sent to storage which will nullify a TAS, STORE, Set Key, Insert Key or Fetch operation. | 1 |
| Reverse Address Parity | Placing this switch in the PA or OB position shall invert the respective parity bits from the test panel's address counter. | 1 |
| Test and Set(TAS) | This switch causes the addressed word in storage to be read out to the test panel and the byte with corresponding Mark bit (set to 1) to be written back into storage with all ones. | 1 |
| Key | Exercises Storage Protect feature. Set Position - Set Key command is generated and In Keys are stored into the specified Storage Protect location. Insert Position - Insert Key command is generated and the information at the specified Storage Protect location is transferred to the test panel where it is compared with the In Key switches. Data Position - Not performing Storage Protect operations. | 1 |
| Mark Keys | Each switch position, except parity, controls gating of one eight bit byte (plus parity)into storage. Switches 4 and 7 also control gating of Data keys to CCR. | 9 |

Table 3-4.  Toggle Switches (cont.)

| Title | Description | Number of Switches |
|-------|-------------|--------------------|
| In Keys | The contents of these switches will be stored into the specified Storage Protect address during a SSK operation. During Storage cycles the contents of these switches provide the In Key for protection checking. | 6 |
| Priority | These switches (4 CE and 3 IOCE) are provided to test the priority scan logic.  Each switch has an odd, even and center OFF position.  These switches are active when the Priority/Storage switch is in the Priority position. | 7 |
| Double cycle | Test Timeout position - In single cycle mode this switch enables checking of the Double Cycle time-out circuits.<br><br>Off Position - Normal operation. | 1 |
| Single Cycle | Single Cycle position - Storage will take one cycle at each depression of the Start pushbutton.<br><br>Normal Position - Normal operation occurs dependent upon other switch functions. | 1 |
| Logout Stop | This switch in conjunction with the data switches (0-2), allows display of logwords in the data indicators. | 1 |
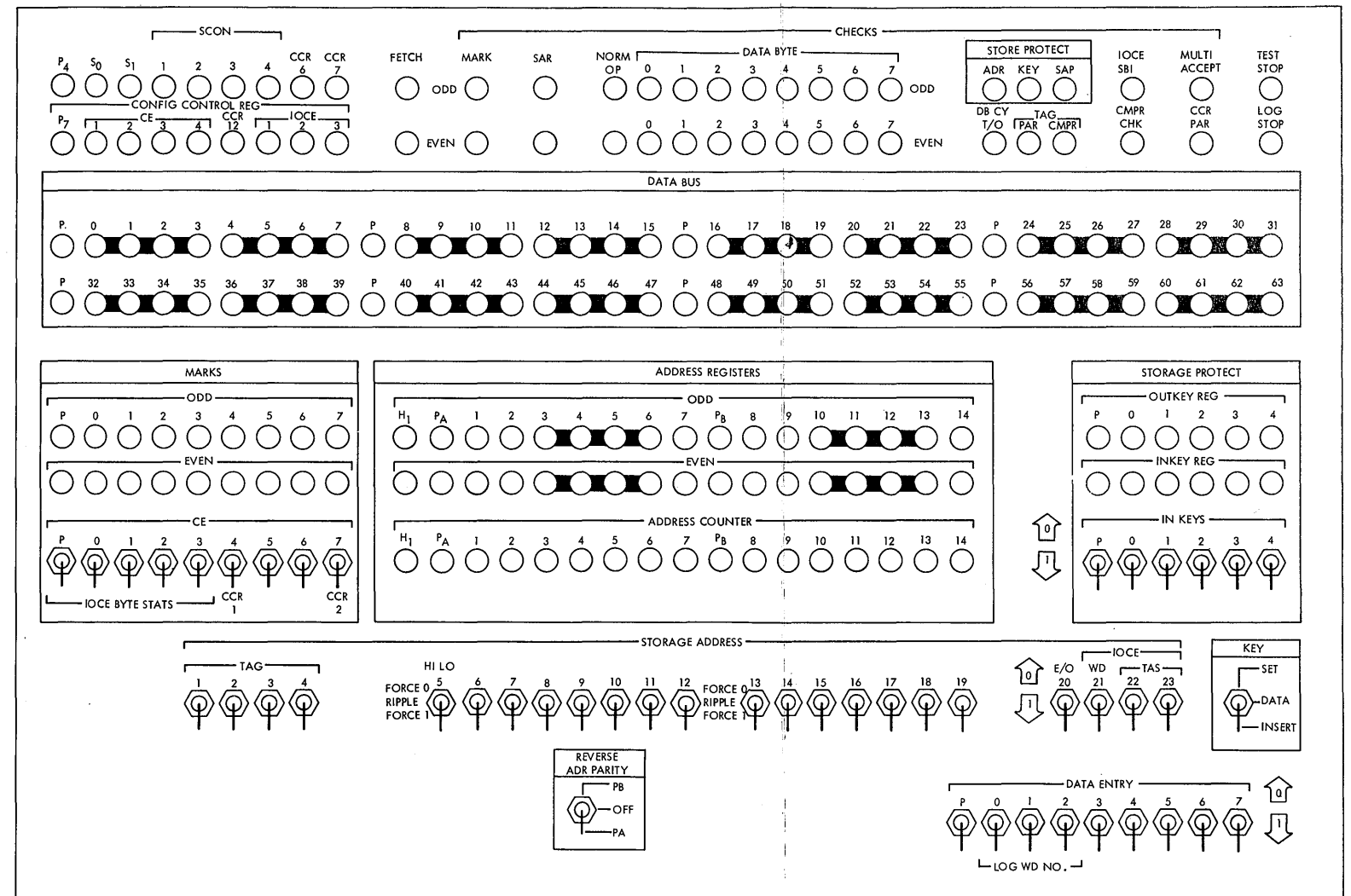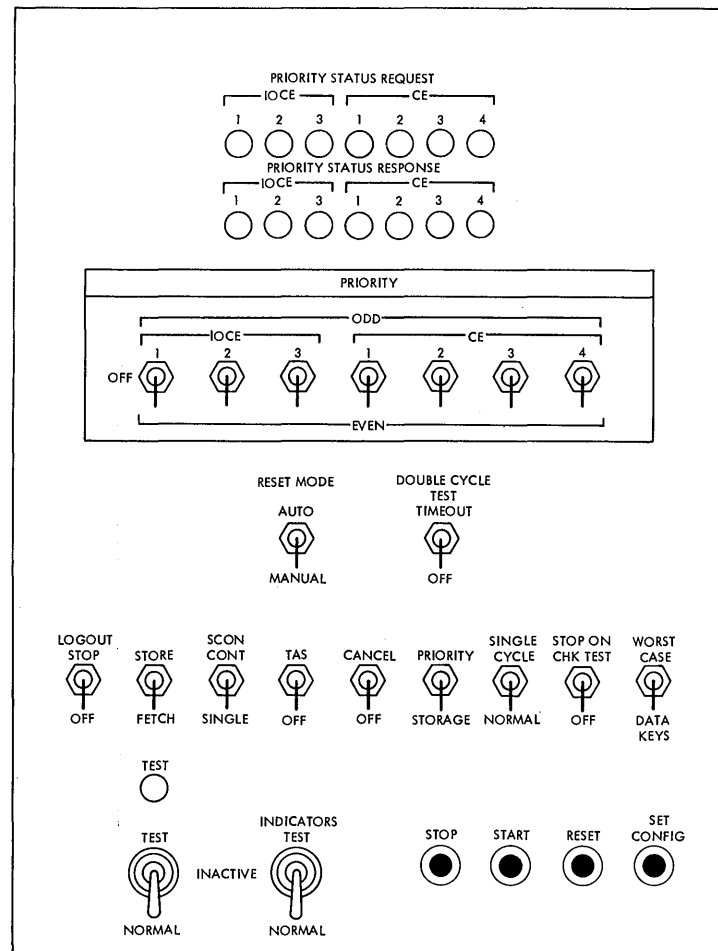
Figure 3-8.  SE Maintenance Panels
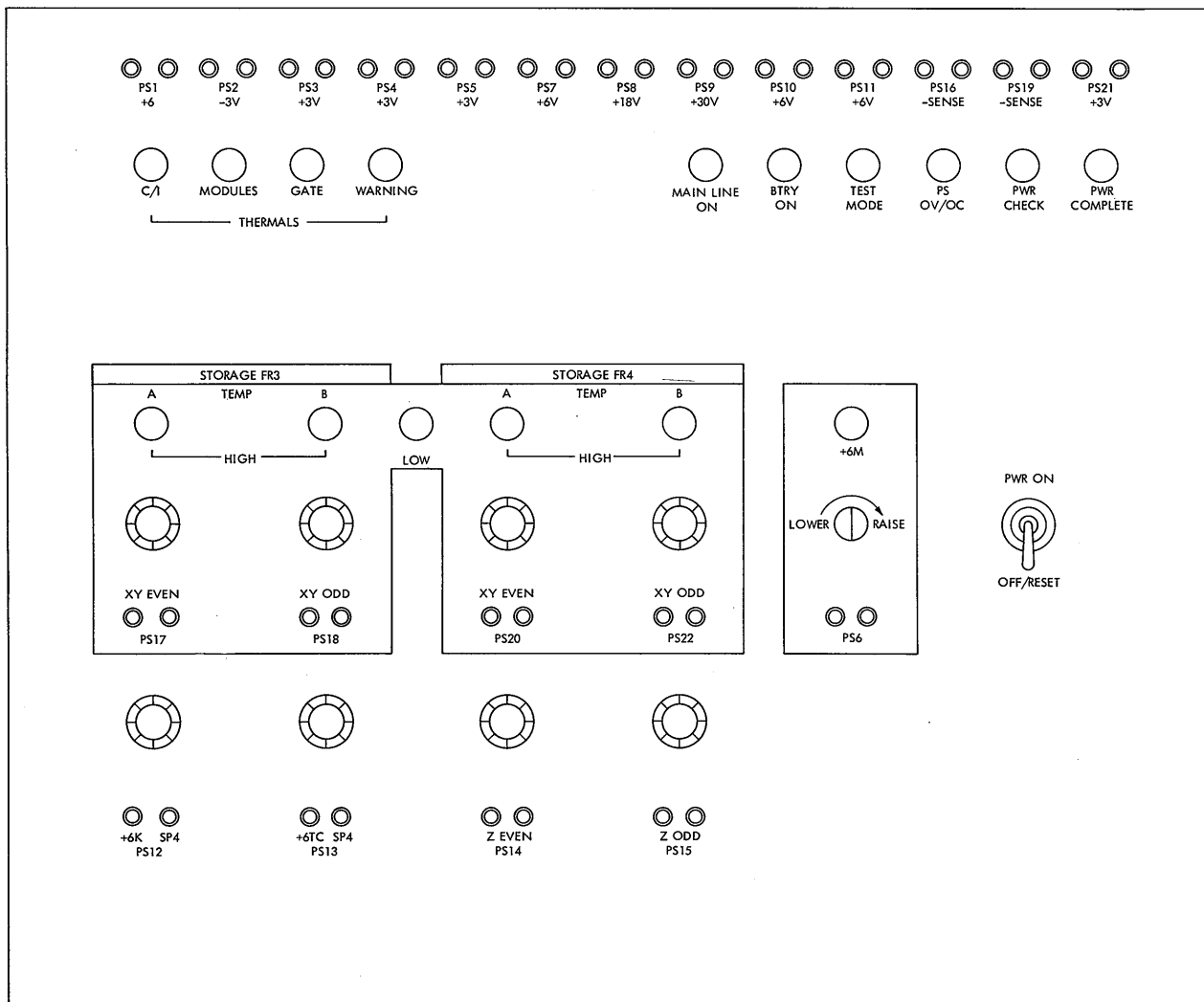
Figure 3-9.  SE Power Control Panel

INTRODUCTION

The Display Element (DE) is a self contained self powered unit.  The
DE contains core storage, request priority controls, and refresh
scanning controls capable of handling four Display Generators (DGs)
simultaneously.  Each DE also contains battery backup power and a
maintenance panel.

Each DE contains two 131,072 byte Basic Storage Modules
(designated as Even BSM and Odd BSM) for a total of 262,144 bytes.  A
byte consists of eight data bits and one parity bit.  Data is trans-
ferred to and from storage in doublewords (a doubleword is 8 bytes).
The BSM cycle time is 800 nanoseconds; however, the two BSMs can
be accessed so that, using two way interleaving, a doubleword can
be obtained every 400 nanoseconds.

Each DE can be accessed from any of four 7201-02s (CEs) and
twenty-four Character Vector Generators (CVGs).  The honoring of
requests is controlled by the priority circuitry and the Configura-
tion Control Register (CCR).  The CCR determines which CEs and
CVGs will be scanned by the priority logic.

Each DE contains a storage protect buffer which provides
a protection key for each contiguous block of 2048 bytes of storage.
These keys can be set and inspected by executing the Set Storage
Key and Insert Storage Key instructions respectively.

FUNCTIONAL CHARACTERISTICS

Basic Storage Module (BSM)

The heart of the BSM is a coincident-current magnetic core storage
unit which contains 131,072 bytes of data.  The BSM receives a
16-bit Address on the Storage Address Bus and inputs data on a
72-bit Storage Data Bus In.  Output data is sent on a 72-bit Storage
Data Bus Out.  The total storage capacity of the DE is divided into
two sections, Even BSM and Odd BSM, each containing separate address
and data registers.  Contents of Storage are preserved under normal
power on-off by the proper sequencing of DC voltages.  Normal power
on-off does not include malfunctions within the DE that cause power
to be abnormally switched off, such as an Emergency Power Off con-
dition.

Storage Protect Buffer (SPB)

The Storage Protect Buffer is a coincident-current magnetic core
unit which holds the 128 storage keys needed to protect main storage.
The keys are sent from the CE to the DE via a 6-bit In Key Bus
(5 key bits, 1 parity bit, Figure 4-1).  A storage protect cycle
is automatically initiated at the start of a main storage cycle and

PROTECTION KEY

| | MATCH BITS | | | | FETCH PROTECT BIT |
|---|---|---|---|---|---|
| P | 0 | 1 | 2 | 3 | 4 |
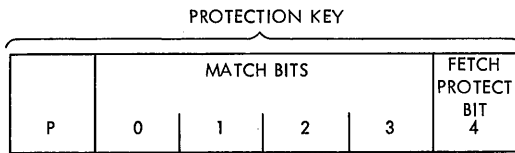
●Figure 4-1.   6 Bit Protection Key Format

is completed in sufficient time to indicate a key mismatch.   If a
mismatch occurs, and neither key is zero, the storage cycle is
canceled and a Protect Check is sent to the user.

Switch Unit (SU)

The Switch Unit serves to attach multiple users (CEs and CVG/DGs) to
the BSM.   It intercepts all data requests and presents them to the
BSMs according to a predetermined priority scheme.   If the request is
from a CVG, the Switch Unit directs the fetched data to the quadword
register designated to the CVG, as dictated by the CCR.   The SU is
capable of servicing 24 CVGs and 6 CE accesses within a 21.6-usec
period.   All DE/DG and DE/CE communication is controlled by the
Configuration Control Register located in the SU.   The CCR also
dictates which CE is allowed to reconfigure the DE.

DESIGN DETAILS

Base Storage Module (BSM)

Main Storage is divided into two BSMs called Even and Odd.   Each
BSM is random access and has a capacity of 16,384 doublewords.
There is a 72-bit Storage Data Register (DESDR - 64 data and 8
parity), a 16-bit Storage Address Register (DESAR - 14 data and 2
parity), and a 9-bit Mark Register (8 data and 1 parity) associated
with the Even BSM.   An identical set of registers are associated
with the Odd BSM (Figure 4-2).   Although the Even and Odd BSMs,
function as separate storages, they share common address and data
buses to and from the Switch Unit.   They also share a common
Storage Protect Buffer.   The address bus is 16-bits wide and the
SDBI and SDBO are both 72-bits wide.   Parity is checked on all
registers.

Storage Protect Buffer (SPB)

The SPB contains a 6 x 128 random access core array which holds the
128-storage keys necessary to protect two BSMs.   Each key protects
a contiguous 2048 byte block of main storage.   A key is composed of
six bits (5 data and 1 parity).   Four of the data bits are the actual
match bits while the fifth bit is a Fetch Protect bit (Figure 4-1).
If the Fetch Protect bit is a "1" data cannot be fetched from a BSM
unless the keys compare.

     At the beginning of each BSM storage cycle a key will be sent
on the In Key bus from the accessing user to the SPB (CEs may use
any combination of the key bits:   the DG/CVGs will always send a key

4-2

EVEN BSM                                    ODD BSM

SDBI

| 0 | 63 | | 0 | 63 |
| EVEN DESDR | | ODD DESDR |

PC — EVEN DESDR                              ODD DESDR — PC

| 0 | 63 | | 0 | 63 |
| CORE ARRAY EVEN | | CORE ARRAY ODD |

72 BIT
SDBO

14 BIT
SAB

| 1 | 14 | | 1 | 14 |
EVEN DESAR — P C                            ODD DESAR — P C
| 1 | 14 | | 1 | 14 |

TO EVEN                                     TO ODD
ARRAY DRIVERS                               ARRAY DRIVERS

MARK BUS

| 0 | 7 | | 0 | 7 |
MARK REG EVEN — P C                         MARK REG ODD — P C
| 0 | 7 | | 0 | 7 |

TO EVEN                                     TO ODD
ARRAY GATES                                 ARRAY GATES
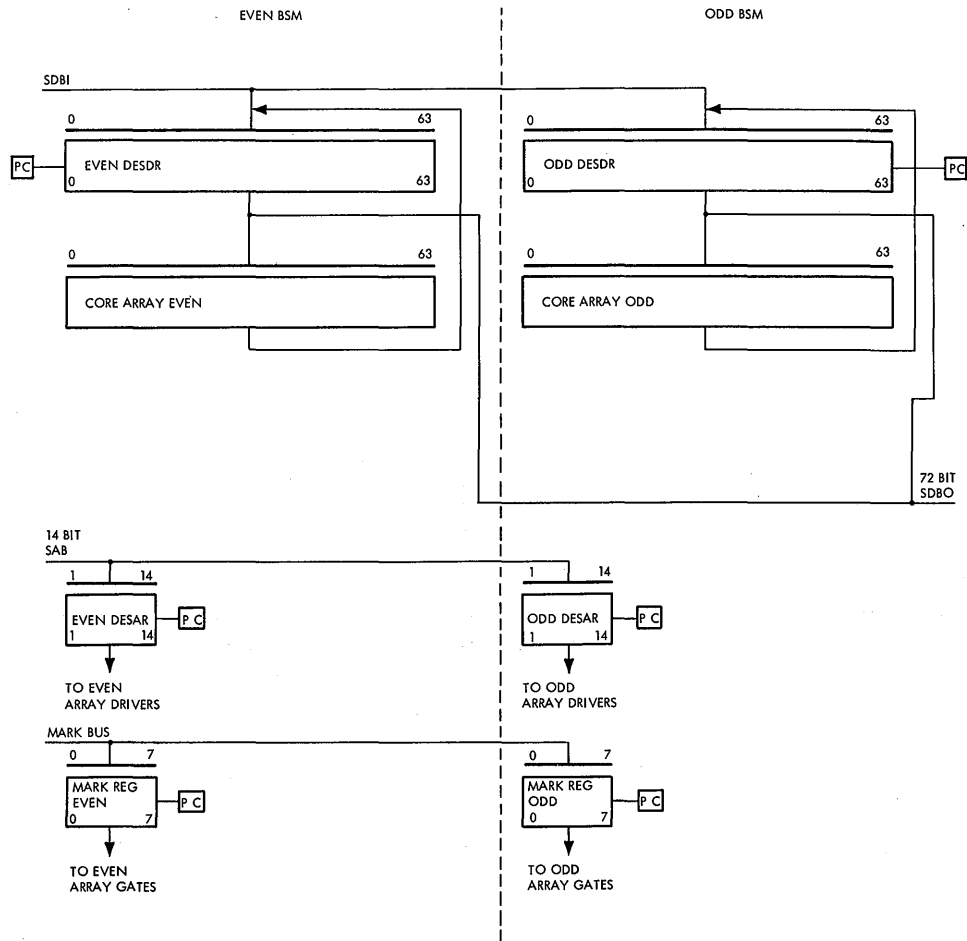
●Figure 4-2.  BSM Data Flow

of zeroes).  The key is compared with the one contained in the SPB
for the block of core designated by the Address or the Storage
Address Bus.  If the keys compare, the access is granted, otherwise
the cycle is canceled.  A key of all zeroes is considered to be
a master key.  If a user sends a key of zeroes to the SPB, access
will be granted regardless of the key pattern in the SPB for the
address block of core.  If the SPB contains a zero key for any
block of core, access will be granted to any user regardless of the
key pattern sent from the user.

Keys contained within the SPB can be set or inspected by any
configured CE.  This is accomplished by the execution of the Set
Storage Key (SSK) and the Insert Storage Key (ISK) instructions
respectively.  These operations are treated as storage access re-
quests except that the new keys are sent to the DE on the In Key
Bus for the SSK instruction and keys are sent from the SPB on the
Out Key Bus for the ISK instruction.

4-3

## Switch Unit (SU)

The Switch Unit portion of the DE is physically attached to the BSM frame and provides the BSM with Interfaces to a maximum of four CEs and four DGs. The Switch Unit contains the logic necessary to **award storage priority. The SU also contains logic necessary to** buffer DG data and transfer data to four DGs and one CE at the same time.

## DG Data Transfer

The DE is designed to maintain addresses and award priority to a maximum of 24 CVGs. Each of the four DGs attached to the DE have up to six CVGs. To facilitate this, the DE has a 16-bit Local Store Register for each CVG (24 total) and one quadword data register for each DG (4 total).

When a quadword of data has been buffered for a CVG, the DE will generate the four bit CVG address (3 bits + odd parity) which identifies to the DG which CVG is to receive the data. The DE now initiates the DE/DG data transfer sequence by sending the four bit address (MSB first, parity last) serially at a 225ns per bit rate. The quadword of buffered data is transferred next at 225ns per 16 bit transfer. The rise of the address parity bit precedes the rise of the first data transfer by 225ns (Figure 4-3).



```
CVG REQUEST

ADDRESS LINE

DATA BUS

DATA SAMPLE (4.4MH)

WORD SYNC (1.1MH)
```

```
    * 16 DATA BITS PER TRANSFER
   ** CVG REQUESTS WILL FALL DURING THIS TIME FRAME
      SEE UNIT TIMING SECTION FOR TIMING RELATIONSHIPS
   Δ ADDRESS BIT 1 OF NEXT CVG SEQUENCE
```
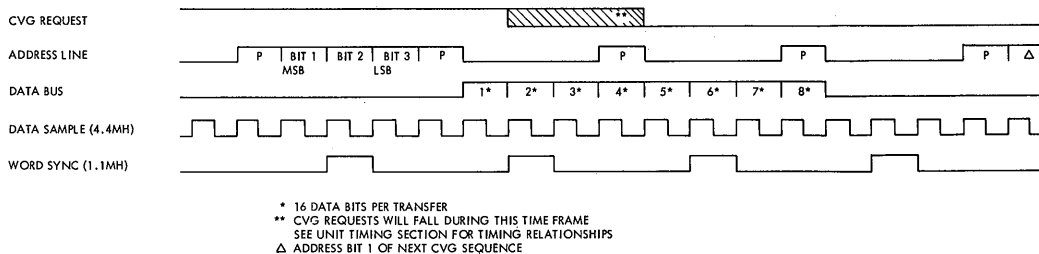
Figure 4-3.  DE/DG Interface Timing

## Local Store Registers

The Local Store Registers are 16 bits wide (14 plus 2 parity) and are used to maintain the address in core of the next quadword to be fetched for each CVG (Figure 4-4). There is a separate register for each of the 24 possible CVGs attached to the DE.

Contents of the LS Regs can be changed by any of three operations.

1.  Whenever Storage Priority is awarded to a CVG for other than a start of display quadword, the contents of its Local Store Register are used to address the BSM. The register is then incremented by one quadword so that it points to the next quadword of data in that CVGs data stream.

4-4

FROM SDBO

1                    14

CVG NO. 1  DATA ADDRESS

CVG NO. 2  DATA ADDRESS

CVG NO. 23  DATA ADDRESS

CVG NO. 24  DATA ADDRESS

1                    14

HARDWARE GENERATED ADDRESS
9                    13

TO DESAR

1                    14

INCREMENTER

1                    14
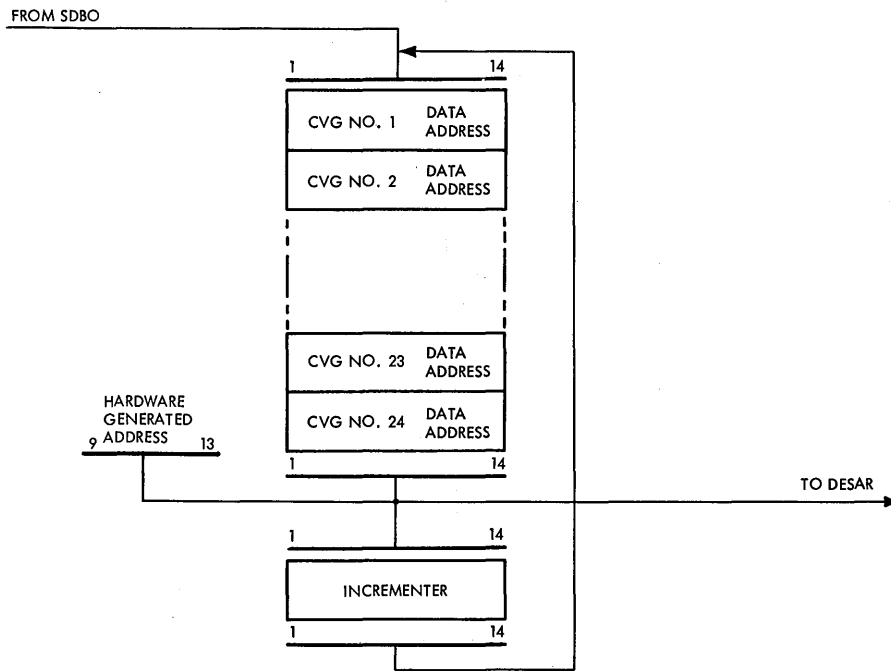
•Figure 4-4.  Local Store Address Register

    2.   When a transfer command is encountered in the data stream, the Local Store Register is loaded with the address portion of the command.  The Transfer command acts like a branch instruction which allows the system to branch around blocks of data which are not to be displayed.

    3.   When a new Refresh Scan is initiated for a CVG, the hardware-generated address of its Start-of-Display quadword is used to address the BSM.  The hardware-generated address is incremented by one quadword and stored in the Local Store Register.

## Data Buffers

The DE has four quadword registers which are used by the DGs (one register is assigned to each DG, Figure 4-5).  Each quadword register is divided into two sections.  Each section is designed to hold one doubleword of data.  Since each CVG request is for one quadword, an access request is sent to both BSMs.  As a doubleword of data is received from each BSM (data arrival time between BSMs is skewed by 400ns.) it is placed in one-half of the quadword register (Figure 4-5).  As soon as the register is full, the BSMs are free to service another user as directed by the priority logic.

Several tests are performed on the data as it comes from the BSM. All data is parity checked by the BSM as it passes through the DESDR (see Storage Check). Next a test is made for a Transfer command or and End-of-Frame command (see respective section). Upon completion of the tests the data is sent to the designated DG/CVG.

Each register is 144-bits wide (128 data and 16 parity). Within the DE parity is maintained on a per byte basis (1 parity bit per 8 data bits). These parity bits are not sent to the DG when the data is transferred. The DG, however, requires that the first bit (bit 0) of each doubleword reflects odd parity for the entire doubleword. Therefore, the DE will combine the 8 standard parity bits of each doublewcrd as it comes from the BSM so that the first bit of each doubleword (quadword bits 0 & 64) will be hardware set to a state (1 or 0) that reflects odd parity for each 64 bit doubleword.

Priority

Each DE can receive access requests asynchronously from four CE's and twenty-four CVG's. The Configuration Control Register in the DE determines which units can be entered in the priority scan regardless of pending access requests.

The DE provides interleaved accesses to its two BSM's (even and odd) via priority logic which scans all attached users in a fixed sequence. The priority scan has twenty-four CVG slots which provide two consecutive accesses per slot. These accesses can be a request to the Even BSM followed by a request to the Odd BSM or an Odd Request followed by an Even. The position of the CVG within the Scan determines whether it will request Even-Odd or Odd-Even. The priority scan also has six CE slots which provide only one access per slot. The CE slots are uniformly distributed throughout the entire scan with three slots allocated for each BSM (even or odd). See Figure 4-6 for an illustration of the priority scan.

The priority scanner is driven by a crystal oscillator and is continuously sampling the users in the sequence shown in Figure 4-6. The priority scanner is designed to award interleaved storage accesses at a 400 nsec rate. Since two interleaved cycles are available to each of the twenty-four CVG's and six cycles are available to CE's, the scanner attempts to make fifty-four DE storage accesses per scan Because the scan is oscillator controlled and scans in a fixed sequence each CVG is insured priority to access two 64-bit doublewords of data at 21.6 usec intervals.

The DE priority logic accepts requests from two classes of users; CVG's (or DG's) and CE's. The manner in which the logic establishes priority within a class of users is tailored to the characteristics of that class.

The manner in which CVG's are awarded priority is very rigid. Each CVG occupies a unique fixed position in the priority scan which cannot be occupied by another CVG. When a CVG requests data, it is
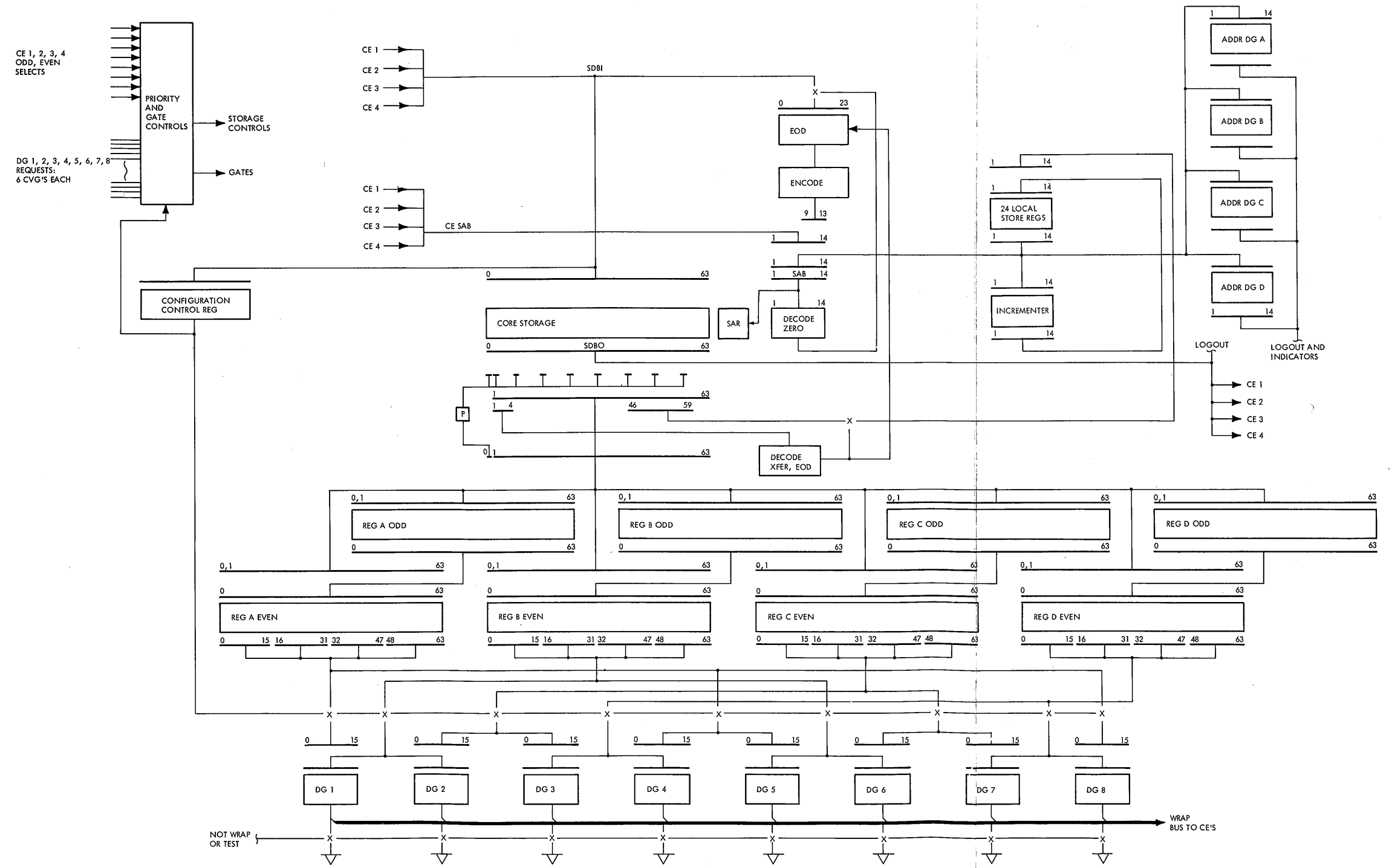
•Figure 4-5.  DE Data Flow Diagram

EVEN BSM |CVG 1|CVG 7|CVG 13|CVG 19| CE* |CVG 2|CVG 8|CVG 14|CVG 20|CVG 3|CVG 9|_____|CVG 12|CVG 18|CVG 24|

ODD BSM |CVG 1|CVG 7|CVG 13|CVG 19|CVG 2|CVG 8|CVG 14|CVG 20| CE* |CVG 3|CVG 9|_____|CVG 12|CVG 18|CVG 24| CE* |

* RESERVED FOR CES ONLY
- CYCLE TIME IS 800 NS
- EACH CYCLE YIELDS A DOUBLEWORD
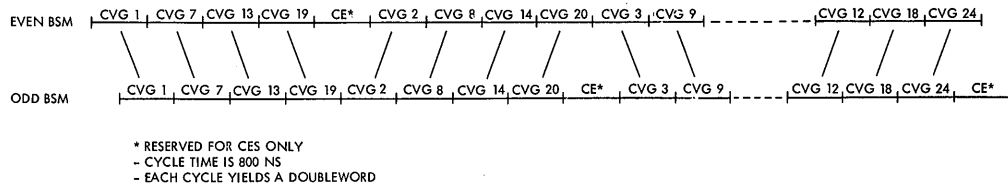
●Figure 4-6. Slotted Priority Scheme

guaranteed priority when the scanner reaches its slot. A CVG re-
quest must be active at the priority logic at least 125 nsec prior
to the start of the storage cycle for that slot to receive priority.

The establishment of CE priority is handled differently from
that of CVG's. Since any, or all, of four CE's can request DE service
for a doubleword, priority is established by scanning all requesting
CE's when a slot is available to CE's. Two levels of selects are
maintained for each BSM to award CE priority. As selects arrive at
the DE they are entered into the select 1 latches. These latches are
only used to accumulate CE selects. Approximately 125 ns prior to
the start of a storage cycle the select 1 latches are transferred
to the select 2 latches provided no select 2 latches are set.
Priority is granted to CE selects in the select 2 latches with CE 1
being highest priority and CE 4 being lowest priority. Each time a
cycle is available to a CE the highest priority select 2 request
receives the cycle until all select 2 requests have been serviced.
When select 2 is empty and a cycle is available to a CE the process
is repeated by transferring accumulated select 1 requests to select
2 and granting priority from select 2 latches.

When a CVG slot is not utilized by a request from the assigned
CVG, the slot is made available to CE requests. Priority for these
slots is awarded the same as for a CE slot. Since an unused CVG slot
represents two cycles (even and odd), the priority logic attempts to
give the slot to two CE's, one having an even request pending and
the other having an odd request pending.

## DE/DG Refresh Control Words

Refresh Control Words occupy the first 50 quadwords of each Display
Element. This area is divided by functions into two sections.
The first quadword contains a control bit for each of the 24 CVGs.
The remainder of this quadword, and the second quadword are not
used. The next 48 quadwords are designated as Start-of-Display
quadwords. There are two for each CVG. There are no hardware
checks to insure that the data within the Refresh Control area is
valid (except for normal parity checking). It is the responsibility
of the Program to set up and maintain the proper control words in
this area.

First Quadword- The first twenty four bits of location zero are
designated as CVG control bits. A "1" stored into any control
bit position(s) will initiate a control operation for the correspond-
ing CVG(s). The control operation is initiated by a store into the

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DE and address zero being decoded. When the decode is successful, the first 24 bits on the SDBI are sent to the control logic. Since all 24 bits are inspected, logical "0" has no significance except to indicate that no action by the DE is required for the corresponding CVG(s); therefore, a control bit must be set to "0" anytime a store is executed into location zero and new action is not needed for that CVG. When the DE recognizes a control bit set for a CVG it will turn on the associated EOD trigger. When the CVG is operating in the synchronous mode, setting of the control bit will cause the CVG to become idle. If the CVG is operating in the asynchronous mode, this action will start a new refresh scan as soon as the next data request is received from the CVG. Once idle a CVG will remain so until the next Refresh Clock pulse. The clock pulse will then cause the CVG to start a new Refresh Scan by loading its Start-of-Display quadword. This function can idle CVGs for a maximum period of 18.2 milliseconds.

PROGRAMMING NOTE:

The first twenty-four bits of location zero were designed to be used as a programming aid under abnormal conditions and not intended for use during normal refresh image switchover. For example, if DE storage is full it may be necessary to pre-empt the old DE image in order to re-allocate the storage area for the new image.

Start-of-Display Quadwords (SOD) - The third through the 50th quad-words are pointers to the start of the data fields for each of the twenty-four CVGs. Whenever a new refresh scan is to be started for a CVG, the address of its Start-of-Display quadword is hardware generated. Each SOD is divided into four recommended functions:

    1.   The first doubleword contains the Start-of-Display command which will be sent to the CVG.

    2.   The second doubleword contains a Test command which will be sent to the CVG. This command performs a confidence check on the CVG-PVD interface.

    3.   The third doubleword contains the Trackball symbol which is also sent to the CVG.

    4.   The fourth doubleword contains a Transfer command which points to the CVG data field located in the BSMs. The Transfer Command is also sent to the CVG.

Refresh Commands

The DE is concerned with two Refresh Commands, Transfer and End-of-Display. A third command, Start-of-Display, is sent to the DGs by the DE whenever a CVG starts a new Refresh Scan, provided the command has been stored by the program. The DE does not decode this command or take any action on it.

## Transfer

The Transfer command is used by the program as an aid to storage, or image management. It functions as a branch command which permits a CVG's refresh image to be non-contiguous in core. The DE will check each doubleword directed to the DG registers for a Transfer command. The check is performed as the data comes from the BSMs on the SDBO. Since a quadword of data is fetched for each CVG request, the Transfer can be in either the Even or Odd doubleword.

If the transfer is in the Even doubleword, the Odd doubleword is not part of the Refresh image. Therefore, to avoid erroneous data from being sent to the CVGs, the odd doubleword is not sent. However, the transfer in the Even doubleword will be sent twice to complete the quadword transfer to the CVG. The transfer command will have the effect of a No-Op command at the DG, therefore, no hardware problem is incurred by sending Transfers to the DG.

If the Transfer is in the Odd doubleword no problem exists since the Even doubleword contains valid data for the CVG. In either case the Address portion of the Transfer is loaded into the correct CVG Address Register.

## End-of-Display

When an EOD is decoded by the DE and the CVG is operating in synchronous mode, the DE will ignore data requests from that CVG until the next Refresh Clock pulse is sensed. It does not matter whether the EOD is the Even or Odd doubleword. If the EOD is in the Odd doubleword, both doublewords are sent to the DG. If the EOD is in the Even doubleword, it is sent to the DG as both the Even and Odd doubleword. This is done to prevent erroneous data transfer to the CVG.

## Refresh Clock

The Refresh Clock controls the Refresh Rate of the CVG(s) to insure that they do not Refresh faster than the predetermined safe rate, which is nominally 55 Hz. The crystal-controlled Refresh Clock is maintenance pluggable for a Refresh Rate of 20 to 60 Hz in 5 Hz increments.

## Refresh Synchronization

The Refresh Clock is used to sync all CVGs. When a clock pulse occurs all idle CVGs will start a new image. Each CVG will continue to process its image until it detects an End-of-Display command, at which time the DE will not honor any requests for that CVG until the next clock pulse. If the EOD occurs prior to the next Refresh Clock pulse (image displayed in less than 18.2 ms) the CVG is said to be operating in the synchronous mode. Two modes of operation are defined for CVGs, Synchronous and Asynchronous. See Figure 4-7.

REFRESH CLOCK        REFRESH CLOCK        REFRESH CLOCK

|← 18.2 MS →| |← 18.2 MS →|

```
*   SOD        DATA        EOD | SOD        DATA        EOD | SOD
    |----------------------------| |----------------------------| |---

*   SOD     DATA      EOD        | SOD    DATA    EOD          | SOD
    |---------------------|        |------------------|          |---

*   SOD DATA  EOD                 |SOD DATA  EOD               | SOD
    |------------|                 |----------|                | |---


▽   SOD        DATA              | EOD        DATA            | EOD
    |----------------------------|-----------------------------|
                                  SOD                           SOD
▽   SOD        DATA              |        EOD       DATA      | SOD
    |----------------------------|-----------------------------|
                                        SOD
```

   * CVG OPERATING IN SYNCHRONOUS MODE

   ▽ CVG OPERATING IN ASYNCHRONOUS MODE
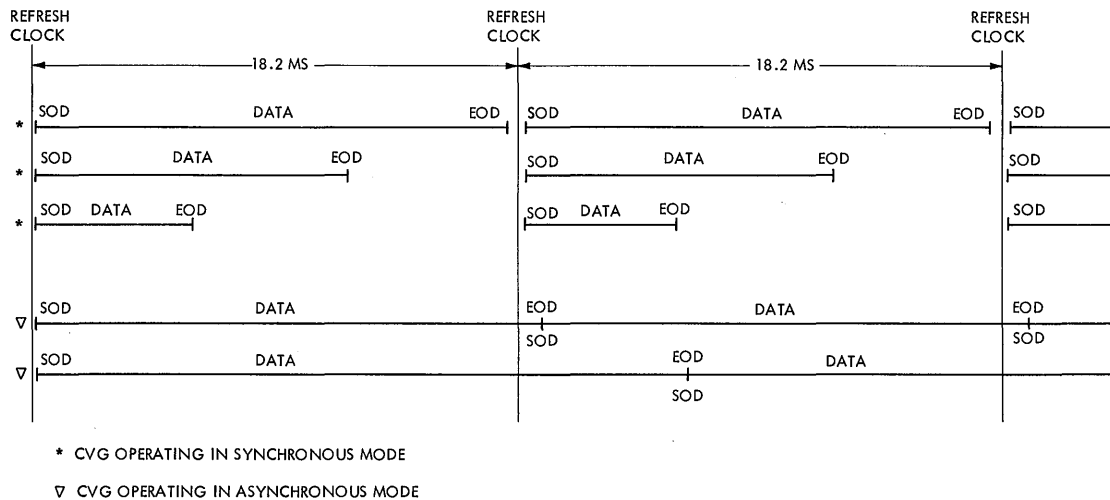
Figure 4-7.  CVG Modes

Synchronous CVGs- A synchronous CVG is one that has an image small enough to be processed and displayed within one refresh period (18.2 ms nominal).  It receives a SOD command when a clock pulse occurs and scans its image to EOD before the next clock pulse.

Asynchronous CVGs- An asynchronous CVG is one that has an image of such magnitude that it cannot be processed and displayed within one refresh period.  If a CVG is asynchronous it will start a new refresh scan as soon as an EOD is decoded.  It will not stop and wait for the next clock pulse.

Two triggers per CVG control the refreshing of CVG data; the Start of Display (SOD) and the End of Display (EOD).  The SOD is set whenever the SOD quadword is fetched and is reset by the refresh clock pulse.  The EOD is set by decoding of a EOD display word in the CVG data image or by the setting of a CVG control bit.  It is reset by the SOD being turned on.  The setting of these triggers at refresh clock time determines the mode of operation.

If both SOD and EOD are "on" the CVG is synchronous.  If the SOD is "on" and the EOD is "off" the CVG is asynchronous.

Configuration Control Register (CCR)

Each DE contains a 31 bit Configuration Control Register.  The CCR controls all communications with the DE (Figure 4-8).  The CCR is composed of 27 data positions and 4 parity positions.  It is divided functionally into four sections.  They are:  the DG communication field, the CE communications field, the SCON field, and the STATE field.

DG Communication Field - This field occupies 16 positions of the CCR and controls the connection of the eight DG interfaces to the four quadword registers within the DE.  (Refer to DE/DG Interconnection

DE/DG COMMUNICATION MASK*

| 0 | | | | | | | | | | | | | | | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | 2 | | 3 | | 4 | | 5 | | 6 | | 7 | | 8 | |
| A | B | B | C | C | D | D | A | A | B | B | C | C | D | D | A |

| 32 | | | | | | 39 |
|---|---|---|---|---|---|---|
| STATE | | SCON | | | | NOT USED | IDES |
| $S_0$ | $S_1$ | 1 | 2 | 3 | 4 | | |

| 56 | | | 59 |
|---|---|---|---|
| CE | | | |
| 1 | 2 | 3 | 4 |
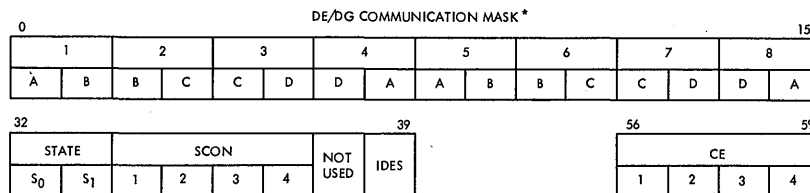
*NUMBERS REPRESENT DG TAIL REGISTERS
LETTERS REPRESENT DG BUFFER REGISTERS

SDBI BIT POSITIONS ARE INDICATED ON THE FORMATS

●Figure 4-8.   DE Configuration Mask

assignment and expansion of DE/DG interconnection assignment).  Two positions are allocated to each DG interface.  Each of these two bits represent a DG quadword register that can be connected to that interface.  If a CCR bit is a "1", accessing is allowed from the specified DG; if the bit is a "0", the request is not allowed.  The 16-bits are checked to insure that no more than one buffer is enabled to any tail at any one time and that no two DGs are enabled to the same data buffer.

CE Communication Field- This field occupies 4 positions of the CCR and determines which CEs are allowed to access the DE.  If the CCR bit is a "1" the DE will honor requests from the corresponding CE.  If the CCR bit is a "0", the corresponding CE's request will be ignored.

SCON Field - Four SCON bits control requests from CEs to alter the Configuration Control Register.  Reconfiguration requests may come only from Computing Elements 1-4.  If its SCON bit is a "1" a reconfiguration request from that CE will be honored.  If the SCON bit is a "0" the request will be ignored.  When in states 1, 2, or 3 with all SCON bits off, or when a CCR parity exists, reconfiguration requests will be accepted from any CE.

State Field- The State bits (S0, S1) are used to define the four operating states a Display Element may assume.

| S0 | S1 | State |
|---|---|---|
| On (1) | On (1) | Three |
| On (1) | Off (0) | Two |
| Off (0) | On (1) | One |
| Off (0) | Off (0) | Zero |

See Chapter 8 for further definitions of states.

The CCR contains one bit labeled Inhibit DE Stop (IDES).  This bit, when set, inhibits the DE from stopping when a DG/CVG related error occurs in the DE.  If the IDES bit is off the DE will hard

stop when a DG/CVG related error occurs  (See Logout).

Reconfiguration requests take priority over all access requests. The design of the DE is such that it is interlocked for the cycle when it is reading or writing.  Therefore, it cannot change the CCR during the middle of the cycle and will accept reconfiguration requests to change the configuration only at the end of a cycle.  No priority is assigned to individual reconfiguration requests.  If more than one reconfiguration request is received by the DE, it will attempt to honor all request simultaneously.  Through proper programming this situation is not likely to occur.

Upon completion of a Reconfiguration, the CCR contents are parity checked.  If the CCR has proper parity and a valid configuration, a response is sent to the issuing CE.  If improper parity or an invalid configuration is detected, no response is sent.  Execution of a Reconfiguration prior to logout will alter the CCR and alter indication of the unit last accessing the storage.  An invalid address condition is generated within an element whenever it is configured away from a DE before its access request is honored.  The CCR is continuously monitored for redundancy and parity errors.  If such an error occurs an ELC is issued to all CEs.  If all bits in the SCON mask are turned off while in states 1, 2, or 3 and not test, the DE will accept a reconfiguration request from any CE.

A Test switch is provided to increase the flexibility of the zero state.  If the Display Element is in zero state and the Test switch is in the "normal" position (Off):

1.  All maintenance controls are inactive.

2.  The display element may be reconfigured as defined by its SCON bits.

3.  Power On-Off is inactive.

4.  DE/DG Interfaces are degated.

If the Display Element is in zero state and the Test switch is in the "test" position:

1.  All maintenance controls are active.

2.  The Display Element cannot be reconfigured from an external source.

3.  Power On-Off is active.

4.  The storage is logically isolated from all other elements.

5.  DE/DG Interfaces are degated.

System reset coming into the CCR will turn all SCON field bit positions ON and all other bit positions OFF.  Proper parity will be maintained.

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Logout

The Display Element has the ability to place its "latched" information on the storage data bus out. Following receipt of a Logout Stop signal from the accessing element the DE will accept Logout Proceed signals from any configured Computing Element.

The Computing Element controls the sequencing and gating of these doublewords. The DE Logout is placed by the CE in a storage location defined by the Diagnose instruction. The DE will send a signal (DE stopped) indicating that it has been stopped for logout to all elements configured to it (Figure 4-9).

Storage must be "stopped" to logout. Logout Proceed signals will be accepted only from those elements configured to the DE. The DE will remain stopped until a Logout Complete or a Reset signal is received from the CE during the logout. The DE issues a level ELC signal to all CE's upon receipt of the Logout Stop signal.

The DE divides hardware checks into two classes, CE related and DG related. CE related checks are those that occur while a CE is accessing the DE. When a CE check occurs the DE will finish any cycle that is currently in progress and wait up to 2.5 usec for a Logout Stop signal. At the end of this time, the DE will either stop, if the Logout Stop has been received, or reset the error and restart the element if a Logout Stop was not received. The second class of DE checks are those that occur when a CVG is accessing the DE. The CCR contains an inhibit stop bit (IDES) which controls DE Logout when a DG related check occurs. If the inhibit bit is OFF the DE will stop at the end of any storage cycle which may be in progress and remain stopped until a Logout Complete is sent to the DE. If the inhibit is ON the DE will not stop when a DG check occurs but will signal an ELC and reset the check conditions.

Fetch

During fetch cycles, data read from storage is gated to the DESDR. If the data is for a CE it is put on the SDBO, otherwise the data is gated to the DG Register assigned to the requesting CVG. Parity is checked on the DESAR, DESDR, and in the DG registers.

Store

Storing of information in BSM is controlled on a byte basis by the marks. Data is read from BSM into DESDR. The 8 bytes from the accessing elements whose marks are "on" are gated from the SDBI onto the DESDR.

Any DESAR, MARK, or SPB parity check, or a Protect Check signal will force the regeneration of the storage data, and signal the accessing element.

## Test-and-Set

During execution of Test and Set, the storage element will fetch
the contents of the BSM specified by the address. These contents are
gated into DESDR at normal fetch time. The contents of the byte
specified by the MARK bit will be set to all ones. The other seven
bytes will be regenerated.

In addition to the Normal Test-and-Set function the DE will
provide a hardware generated Test-and-Set as a programming aid. Any-
time a CVG starts to scan a new refresh image its Start-of-Display
quadword is fetched (see DE/DG Refresh Control). Byte four (bits
32-39) of the SOD will automatically be set to ones via the hard-
ware generated Test-and-Set each time the SOD is fetched for a CVG.
(Figure 4-10)

Normal parity checking will occur.

## Checking

Seven types of check signals may be generated and transmitted to the
system as follows:

| | |
|---|---|
| Element Check | Power Check |
| Storage Check | On Battery |
| Protect Check | Emergency Power Off |
| Logic Check | |

Element Check (ELC) - Element Check is sent to all attached comput-
ing Elements without regard to the Display Element Configuration
Control Register or to accessing controls. Checks within this area
are:
1. CCR Parity
2. Marginal Temperature (OTC)
3. On Battery (OBS)
4. Storage Address Check
5. CE Storage Data Check
6. DG Storage Check
7. Normal Op Check
8. Box Tag Mismatch
9. Box Tag Parity
10. Multi-accept

With one exception, a 525-ns ELC pulse is issued when conditions 1-10
are detected. The exception is detection of a DG Storage Check when
the IDES bit is off, which results in a level ELC. Other functions
within the DE are not inhibited (except under storage check) and the
DE will continue to function as normally as possible.

11. Over/Under voltage or over current.
12. Normal Power Off. Master Power Off (MPO) or loss of power.
13. DE Stopped signal (Note: ELC is reset upon logout com-
    plete).

A level ELC will remain issued upon detection of conditions 11-13.
The ELC will remain on until the condition has been cleared.

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**BIT POSITIONS IN MAIN STORAGE**

| WORD NO | Field layout | COMMENTS |
|---|---|---|
| | Bit positions: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | |
| 0 | DESDR (EVEN): 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | DESDR (EVEN) |
| 1 | DESDR (EVEN): 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 | DESDR (EVEN) |
| 2 | MARKS (EVEN): 0-7 8-15 16-23 24-31 32-39 40-47 48-55 56-63 \| DESDR PARITY (EVEN): 0-7 8-15 16-23 24-31 32-39 40-47 48-55 56-63 \| DESAR 1-14 (EVEN): P 6-12, 6, 7, 8, 9, 10, 11, 12, P 13-19, 13, 14, 15, 16, 17, 18, 19 | MARKS, DESDR, DESAR (EVEN) |
| 3 | OPERATION (EVEN): MARK PARITY, T & S, STORE, FETCH \| CHECK CONDITIONS (EVEN): DATA CHK, ADDR CHK, MARK PARITY CHK, CANCEL LATCH \| SPIKR: P 0-4, 0, 1, 2, 3, 4 \| SPOKR: P 0-4, 0, 1, 2, 3, 4 \| OPERATION: ISK, SSK \| CHECK CONDITION (COMMON): SP ADDR CHK, SP KEY CHK, KEY MISMATCH, OBS, OTC | OPERATION, CHECKS (EVEN AND COMMON), SPIKR, SPOKR |
| 4 | DESDR (ODD): 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 | DESDR (ODD) |
| 5 | DESDR (ODD): 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 | DESDR (ODD) |
| 6 | MARKS (ODD): 0-7 8-15 16-23 24-31 32-39 40-47 48-55 56-63 \| DESDR PARITY (ODD): 0-7 8-15 16-23 24-31 32-39 40-47 48-55 56-63 \| DESAR 1-14 (ODD): P 6-12, 6, 7, 8, 9, 10, 11, 12, P 13-19, 13, 14, 15, 16, 17, 18, 19 | MARKS, DESDR, DESAR (ODD) |
| 7 | OPERATION (ODD): MARK PARITY, T & S, STORE, FETCH \| CHECK CONDITIONS (ODD): DATA CHK, ADDR CHK, MARK PARITY CHK, CANCEL LATCH | OPERATION CHECKS (ODD) |
| 8 | CCR — DG: P0, 1A, 1B, 2B, 2C, 3C, 3D, 4D, 4A, P1, 5A, 5B, 6B, 6C, 7C, 7D, 8D, 8A, P4 \| STATE: S0, S1 \| SCON: 1, 2, 3, 4 \| IDES \| P7 \| CE: 1, 2, 3, 4 \| CCR INVALID | CCR |
| 9 | CE CHECK: 1, 2, 3, 4 \| CVG OPERATION: A: 1, 2, 3, 4, 5, 6; B: 7, 8, 9, 10, 11, 12; C: 13, 14, 15, 16, 17, 18; D: 19, 20, 21, 22, 23, 24 \| ADDRESS REG: A, B, C, D | OPERATION LATCHES DG ADDR REG ID |
| 10 | DG REGISTER CHECK: 1, 2, 3, 4, 5, 6, 7, 8 \| CHECK CONDITIONS (COMMON): TAG PARITY CHK, TAG, CCR PARITY CHK, MULTI ACCEPT, LS PARITY CHK, NORMAL OP, REFRESH PARITY CHECK \| DG ADDRESS REGISTER: P 1-7, 1, 2, 3, 4, 5, 6, 7, P 8-14, 8, 9, 10, 11, 12, 13, 14 | CHECKS, DG ADDR REG |
| 11 | TAG: P 1-5, 1, 2, 3, 4, 5 \| DE ID: 1, 2, 3, 4 \| HALFWORD COUNTER: 8, 4, 2, 1 \| DG DATA REGISTER: P 0-7, 0, 1, 2, 3, 4, 5, 6, 7, P 8-15, 8, 9, 10, 11, 12, 13, 14, 15 | DG DATA REG |

●Figure 4-9.  DE Logword Format

|  | 0 | 23 24 | 63 64 | 127 |
|---|---|---|---|---|
| ADDRESS ZERO | * | NOT USED | NOT USED | |
| | NOT USED | | NOT USED | |
| CVG 1 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |
| CVG 2 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |
| CVG 3 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |
| CVG 4 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |
| CVG 5 | SOD** | | TEST | |
| CVG 23 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |
| CVG 24 | SOD** | | TEST | |
| | TRACKBALL | | XFER | |

* 24 CVG CONTROL BIT - ONE PER CVG

** FORCED TAS ON BITS 32-39 EACH TIME A CVG REFERENCES THIS DOUBLEWORD

Figure 4-10.  Refresh Control Area

Storage Check - Storage Data Check and Storage Address Check, these lines are generated by parity check errors (except configuration register parity check errors) to request a logout. These signals are gated only to the accessing unit at the time the error is detected. The DE will stop for 2.5 usec following completion of the cycle on which an error was detected. Configuration requests will not be honored during this 2.5 usec stop. Simultaneously with the Storage Check signal, a pulse ELC will be issued to all CEs.

If Logout Stop has not been signalled by an attached element, the DE will proceed following the 2.5 usec wait, and the error information latches will be reset.

Whether Logout Stop is signalled or not, reconfiguration may take place following the 2.5 usec stop.

DESDR is parity checked on all fetch and store cycles. It is disabled on all ISK cycles, SSK cycles, and any time a cycle is hardware canceled. If the DESDR has incorrect parity, it will not be corrected but is placed back in storage with incorrect parity.

Address checking occurs on all cycles and forces Box Tag Mismatch when the address sent to the DE does not lie within the DE addressing. Pluggable means exist to define the addresses available within a Display Element. These will be plugged at system installation time.

Protect Check - In general, a Protect Check is generated when the four data bits of the key sent by the accessing CE do not match the four data bits of the key in the SPB, and neither key is zero. The violation is suppressed on ISK and SSK cycles. A match will not occur if either key has incorrect parity. A protect check also occurs if the keys do not compare and the fetch protect bit is on. If the fetch protect bit is off, any location can be fetched without regard to key matching.

Logic Check - This signal is sent to the Configuration Console whenever a hardware-detected check occurs in the DE.

Power Check - Power Check is sent to the Configuration Console whenever any of the following conditions are present:

1. Marginal or catastrophic temperature
2. Over/under voltage or overcurrent
3. Normal power off or loss of power

This Power Check signal remains active as long as any of the conditions 1-3 exist.

On Battery (OBS) - The On Battery signal is generated whenever the DE transfers from main power to battery power. The signal is sent to the Configuration Console and a pulsed ELC is issued to all CEs.

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**Master Power OFF (MPO)** - Whenever the MPO switch is activated, the DE power drops and a level ELC will be sent to all CEs. The ELC signal remains active until the MPO switch is deactivated.

DE/DG Interface

The DE can interface with eight DG's. Only four interfaces can be active at any one time. The DE can service a maximum of twenty-four CVG's on the four active DG interfaces. The DE accepts data request asynchronously from the CVG's and establishes storage priority for each request. When two 64-bit doublewords of data have been accumulated by the DE for a CVG, the CVG address is generated and sent to the attached DG serially via the CVG address line. The data is then sent to the DG on the Display Data Bus.

Line Definition -

DE/DG Interconnections:

| Name | No. of Lines | Description |
|------|--------------|-------------|
| | DE to DG | |
| Display Data | 16 | Display data bits |
| CVG Address | 1 | CVG Address and parity |
| Data Sample Timing | 1 | 4.4 MHZ timing |
| Word Sync Timing | 1 | 1.1 MHZ timing |
| | DG to DE | |
| Data Request | 6 | CVG data requests |

**Data Request (6 lines)** - When a CVG is ready to accept more refresh data, its Data Request line is raised. These request signals are sent on six discrete lines to the DE, one per CVG or six per DG. CVG Request Lines are scanned individually by the Priority Logic. If the Request Line is active when the priority logic scans for that particular CVG, that CVG will be awarded DE access. Each CVG is scanned every 21.6 usec.

**CVG Address (1 line)** - Upon honoring of a CVG request for data, the DE transmits an address code to the DG to identify the CVG for which the subsequent data is intended. This is a 3-bit code (plus odd parity) transmitted serially at 4.4 MHZ rate. The rise of the fourth address bit (parity) precedes the rise of the first data transfer by 225ns. To prevent Address parity errors from occurring between successive DG services when there is not a CVG Address to be sent to the DG, a logical "1" bit will be sent in the Address parity position of each 900ns clock period. The CVG's are addressed 1 through 6, binary 001 through 110 plus odd parity.

Display Data (16 lines) - Data is transmitted in parallel 16-bit halfwords from the DE to the DG. The Data Request is considered serviced when eight halfwords have been transmitted. Odd parity for each respective 64-bit doubleword is located in the first bit position of the first halfword and the fifth halfword. Bit position 0 is the MSB (most significant bit) for each doubleword; bit position 63 contains the LSB for each doubleword.

Unit Timing (2 lines) - Two free running clock signals are sent from the DE to each DG to control the transfer of CVG data and Addresses. A 4.4 MHZ Data Sample clock is used to Strobe Out Address and data bits at a 225ns per transfer rate. A 1.1 MHZ Word sync signal is used to initialize and synchronize DG hardware (Figure 4-3). The following timing relationships exist for the DE/DG interface.

1. The period of one data sample pulse is 225 ± 15ns.
2. The "UP" level of one data sample pulse is 112 ± 15ns.
3. The rise of the word sync is coincident with the rise of every fourth Data Sample pulse ± 10ns.
4. All data and Address bits are stable prior to the rise of the data sample pulse and will remain stable for a minimum of 170ns after the rise of the data sample pulse.
5. The "UP" level of one word sync is 225 ± 15ns.

Interface Sequences

The interface sequences are shown in Figure 4-3.

Data Request - To initiate a Data Request sequence the Data Request lines for any CVG(s) requiring data will be raised. These lines are asynchronous to the DE operation. Upon receipt of the signal, the DE will enter the requesting CVG(s) into the slotted priority scan. When a CVG has top priority, (i.e., its slot is reached) requests are issued to storage to get a quadword of data (two 64-bit doublewords). This data is gated to one of the four quadword buffers where it is held until it is sent to the DG/CVG requesting it.

Data Transfer - When a quadword of data has been buffered for a DG/CVG, the data transfer is initiated. A 4-bit CVG address (three bits plus parity) is sent serially to the DG housing the requesting CVG at the rate of one bit every 225ns. Data transfer begins 225ns after the rise of the last address bit. For any CVG, a data transfer consists of a burst of eight halfwords. The halfwords are sent parallel by 16-bits at 225ns intervals. When two 64-bits doublewords of data are transferred, the sequence is terminated and the DE is free to service another CVG in that DG.

Configuration

A DE has eight DG interfaces and four quadword buffers. Each DG interface can be enabled to either of two predetermined buffers in the DE. Since the DE has only four buffers, there can be only four active DG's per DE. Interface activation and interface-to-buffer gating is under CE/DE Configuration control.

The DE shall guarantee that two doublewords will be transmitted every 21.6 microseconds to each CVG, if the CVG is requesting data. For any given display load the time between successive transmissions of a given piece of data to the CVG shall not vary due to the DE by more than plus or minus 125 microseconds. If the CVG requests data simultaneously with the priority sample time an unpredictable situation may occur which may cause the time between successive transmission of a given piece of data to exceed ± 125 microseconds. The transmission rate to any CVG shall not affect the transmission rate to any other CVG.

The refresh rate for a CVG shall be held constant at 55 CPS except when the quantity of data exceeds 1/55 second for display. When the quantity of data exceeds 1/55 second for display, the refresh period shall be determined by the quantity of data.

When the amount of data is reduced to where the refresh period can be contained within the 1/55 of a second, several refresh periods may be required to sync the CVG to the 55 CPS refresh rate.

The 55 CPS rate (1/55 second refresh period) shall be maintenance adjustable in 5 CPS steps from 20 CPS to 60 CPS.

No interruption of transmission service shall occur when the CVG switches over to updated data.

Reconfiguration for a single CVG failure shall not require reconfiguration of any other on-line CVG.

All 64 bit doublewords sent to the DG are considered to have a unique identifying command code and are not dependent on any other display word or sensitive to position in the data field.

For display management purposes the DE will, under program control, restart a CVG image readout before the entire image has been displayed. This action results in two SODs being sent to the CVG prior to the sending of an EOD. This condition does not cause any problem since display words have unique independent functions.

Electrical Characteristics

All signals between the DE and DG are carried by a 100 ohm balance transmission system. The cable is an overall shielded cable containing multiple twisted pair conductors.

Line Driver- The output signals from the DE shall have the following specifications when a 100 ohm plus or minus 5% resistive terminator is connected between the + signal lead and the - signal lead at each of the two DE output connector points.

A logical one is represented by the + signal line being - 1.6 volts (+0.3v, -0.7v) with respect to the -signal line.

A logical zero is represented by the + signal line being + 1.6 volts (-0.3v, +0.7v) with respect to the -signal line.

The + signal and - signal lines shall not exceed plus or minus 7.0 volts with respect to the DE signal ground (DC return) when measured at the DE output connector.

Rise and fall times shall not exceed 20ns (10% to 90% points) when measured from + signal or - signal line to ground. This measurement is made with no external cable attached and a 100 ohm ± 5% resistor connected between the associated + and - signal lines at each of the two output connectors.

Differential skew is defined as the time interval when the driver output is not in a definite state. The driver is in a indefinite state when the differential voltage between the + and - signal lines is less than 1.3 volts. Differential skew will be 20 ns or less at the driver output.

### Driver Output

Power Off condition all drivers: Signal Line differential voltage= 0.0v ± 1.0mv.

(Measured at DE output connector with 100 ohm terminator from + Signal to - Signal).
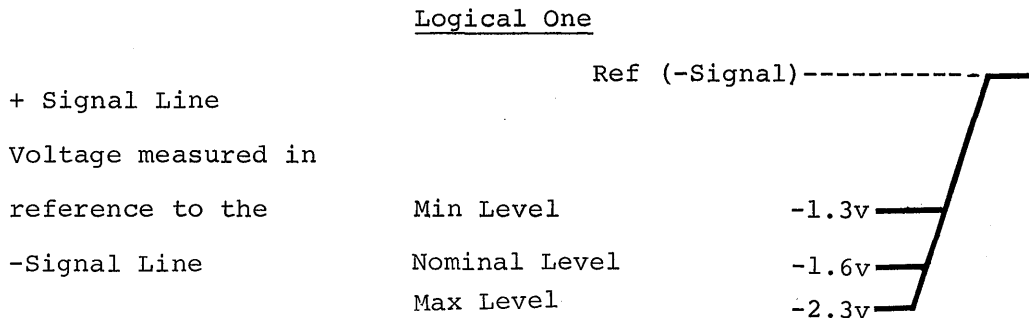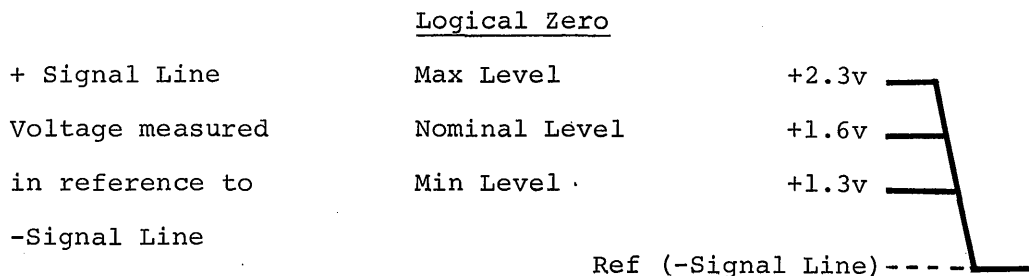
### Logical Zero

| + Signal Line | Max Level | +2.3v |
| Voltage measured | Nominal Level | +1.6v |
| in reference to | Min Level · | +1.3v |
| -Signal Line | | |
| | Ref (-Signal Line) | |

### Logical One

Ref (-Signal)

| + Signal Line | | |
| Voltage measured in | | |
| reference to the | Min Level | -1.3v |
| -Signal Line | Nominal Level | -1.6v |
| | Max Level | -2.3v |

Line Receiver - The characteristic impedance between the + signal and - signal Lines at the input connector to the DE shall be 100 ohms ± 5%. A logical "zero" is represented by the + signal line being equal to or greater than +0.6 volts in respect to the -signal line when measured at the receiver input. A logical "one" is represented by the + signal line being equal to or greater than -0.6 volts in respect to the -signal line when measured at the receiver input.

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The + signal and - signal lines shall remain between + 3 volts and unit signal ground (DC return).
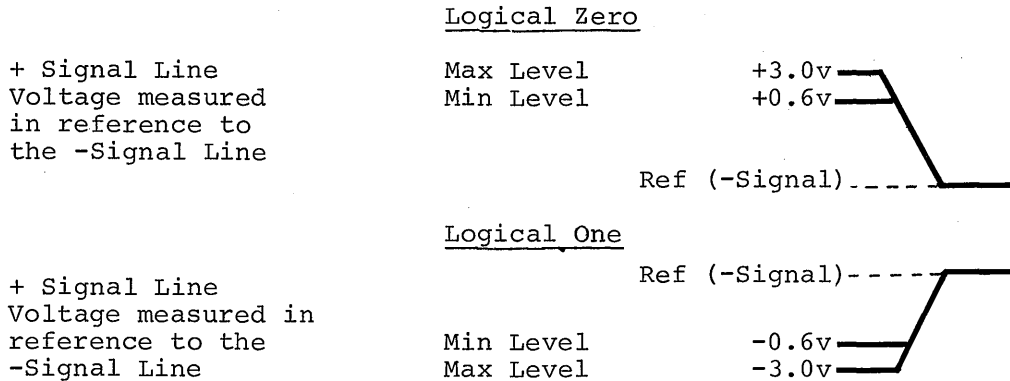
Receiver Input Requirements -

Logical Zero

| + Signal Line | Max Level | +3.0v |
| Voltage measured | Min Level | +0.6v |
| in reference to | | |
| the -Signal Line | | |

Ref (-Signal)

Logical One

Ref (-Signal)

| + Signal Line | | |
| Voltage measured in | | |
| reference to the | Min Level | -0.6v |
| -Signal Line | Max Level | -3.0v |

Fault Conditions -

1.  A grounded signal line must not damage drivers, receivers or terminators.

2.  Both lines shorted together must not damage drivers, receivers, or terminators.

3.  An open line or terminator must not damage the driver or receiver circuit.  (This condition may result in one signal line rising to 7.0 volts with respect to signal ground).

4.  Power down at the DG driver may cause a condition at the DE receiver circuit which could allow small noise signals to switch the receiver circuit.  The DE will provide facilities for degating its receiver outputs where needed to prevent erroneous system interruption.

5.  A receiver which is not connected to a driver circuit must not generate spurious signals.

Cabling- Cables must meet the defined following specifications and must utilize standard Serpent type connectors at the DE end.

Characteristic Impedance = 95 ohms

Resistance DC                    $\leq$.019 ohms/conductor/ft.

TPD Propagation Delay            =1.5 ± .05 ns./ft.

ΔTPD                             =.02 ns./ft.

Attenuation                      =2.1 db/100 ft. at 4 MHz

Cable and connector requirement at the DE end per DG are as follows:

Data/Address Out       19 Signals       1 - 48-Pin Serpent

Request In              6 Signals       1 - 48-Pin Serpent

Refer to Table 4-1 for connector pin assignments.

Table 4-1.  DE/DG Interface Pin Assignments

| Connector 1 | |
|---|---|
| Pin | Signal Name |
| B02 | +Sample pulse |
| D02 | -Sample pulse |
| B04 | +Sync pulse |
| B03 | -Sync pulse |
| D04 | +Bit 00 |
| D05 | -Bit 00 |
| B07 | +Bit 01 |
| B05 | -Bit 01 |
| D06 | +Bit 02 |
| D07 | -Bit 02 |
| D08 | Ground |
| B09 | +Bit 03 |
| B08 | -Bit 03 |
| D09 | +Bit 04 |
| D10 | -Bit 04 |
| B12 | +Bit 05 |
| B10 | -Bit 05 |
| D11 | +Bit 06 |
| D12 | -Bit 06 |
| D13 | +Bit 07 |
| B13 | -Bit 07 |
| G04 | +Bit 08 |
| G03 | -Bit 08 |
| J04 | +Bit 09 |
| J05 | -Bit 09 |
| G07 | +Bit 10 |
| G05 | -Bit 10 |
| J06 | +Bit 11 |
| J07 | -Bit 11 |
| J08 | Ground |
| G09 | +Bit 12 |
| G08 | -Bit 12 |
| J09 | +Bit 13 |
| J10 | -Bit 13 |
| G12 | +Bit 14 |
| G10 | -Bit 14 |
| J11 | +Bit 15 |
| J12 | -Bit 15 |
| G02 | +Address Bit |
| J02 | -Address Bit |

Table 4-1.  DE/DG Interface Pin Assignments (cont)

| Connector 2 | |
| --- | --- |
| Pin | Signal Name |
| B02 | -CVG #1 Request |
| D02 | +CVG #1 Request |
| B04 | -CVG #2 Request |
| B03 | +CVG #2 Request |
| D04 | -CVG #3 Request |
| D05 | +CVG #3 Request |
| B07 | -CVG #4 Request |
| B05 | +CVG #4 Request |
| D06 | -CVG #5 Request |
| D07 | +CVG #5 Request |
| D08 | Ground |
| B09 | -CVG #6 Request |
| B08 | +CVG #6 Request |

NOTE: - (Name) is - Signal Line
      + (Name) is + Signal Line

Serpent Connector Blocks - Serpent connectors used in the DE will be 48 pin "A" style connectors.  These must be mated with a "B" style connector on the external cable.  Serpent contact termination to termination resistance (includes 2 crimps and mated contacts) will not exceed:
     0.20 ohms when used with #22 wire or larger.
     0.30 ohms when used with #24 or #26 wire

External Cable Length - The maximum external cable length is 65 feet connector to connector (5 feet are used internal to the DE).

MAINTENANCE PANELS

The DE Maintenance Panel (Figure 4-11), DE Power Control Panel (Figure 4-12) and SU Power Control Panel (Figure 4-13) contain facilities to allow off-line maintenance of the DE and contain indications of the DE status.  The facilities on the DE Maintenance Panel include: Indicators, Pushbuttons, Rotary Switches, Toggle Switches, and Miscellaneous Maintenance Panel items (Tables 4-2 to 4-5).

Table 4-2.  DE Maintenance Panel Indicators

| NAME | QUANTITY |
|---|---|
| Data Register | 72 |
| Address Registers | 32 |
| Mark Register Even | 9 |
| Mark Register Odd | 9 |
| Out Key Register | 6 |
| In Key Register | 6 |
| Configuration Control Register | 31 |
| DG Data | 18 |
| CVG Address | 1 |
| EOD | 6 |
| EOD decoded for CVGs 1-6 | |
| DG selected via a rotary switch | |
| SOD | 6 |
| SOD decoded for CVGs 1-6 | |
| DG selected via a rotary switch | |
| DG/CE Sequencers | 5 |
| CVG Sequencers | 6 |
| CE Select | 4 |
| CVG Select | 24 |
| Halfword Counter | 4 |
| Fetch Even | 1 |
| Fetch Odd | 1 |
| EOD    (command decoded on SDBO) | 1 |
| Transfer | 1 |
| Even/Odd | 1 |
| CVG Fetching EVEN doubleword first | |
| TEST | 1 |
| STOP | 1 |
| Data Byte Even | 8 |
| Data Byte Odd | 8 |
| Address Register Even Check | 1 |
| Address Register Odd Check | 1 |
| Mark Register Even Check | 1 |
| Mark Register Odd Check | 1 |
| DG Register Check | 8 |
| SPB Address Check | 1 |
| SPB Key Check | 1 |
| SPB Protect Check | 1 |
| Box Tag Parity Check | 1 |
| Box Tag Mismatch | 1 |
| Multi-Accept | 1 |
| CCR Parity Check | 1 |
| CCR DG Redundancy Check | 1 |
| Normal OP | 1 |
| Refresh Counter Parity Check | 1 |
| Local Store Parity Check | 1 |
| Compare Check | 1 |
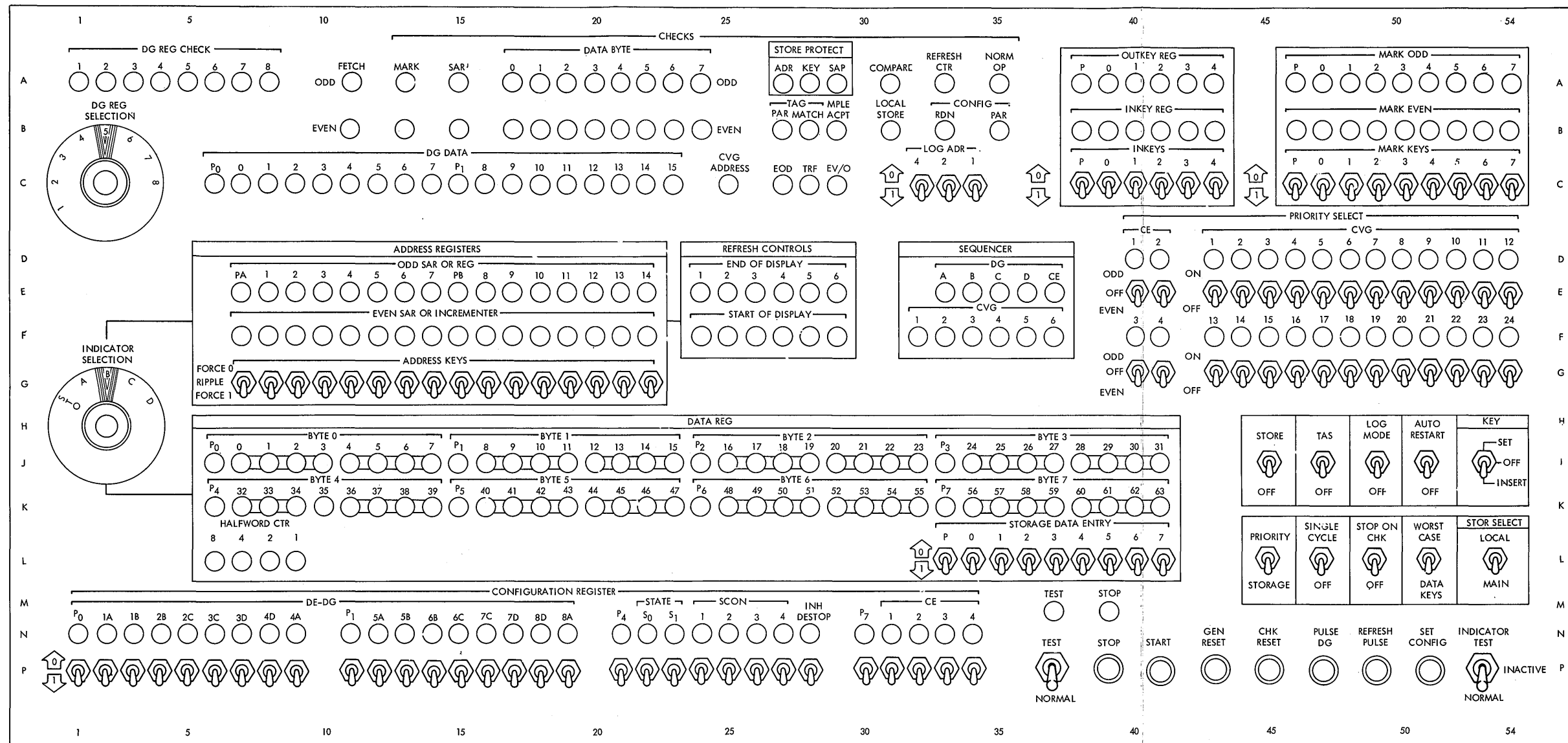
•Figure 4-11.  DE Maintenance Panel
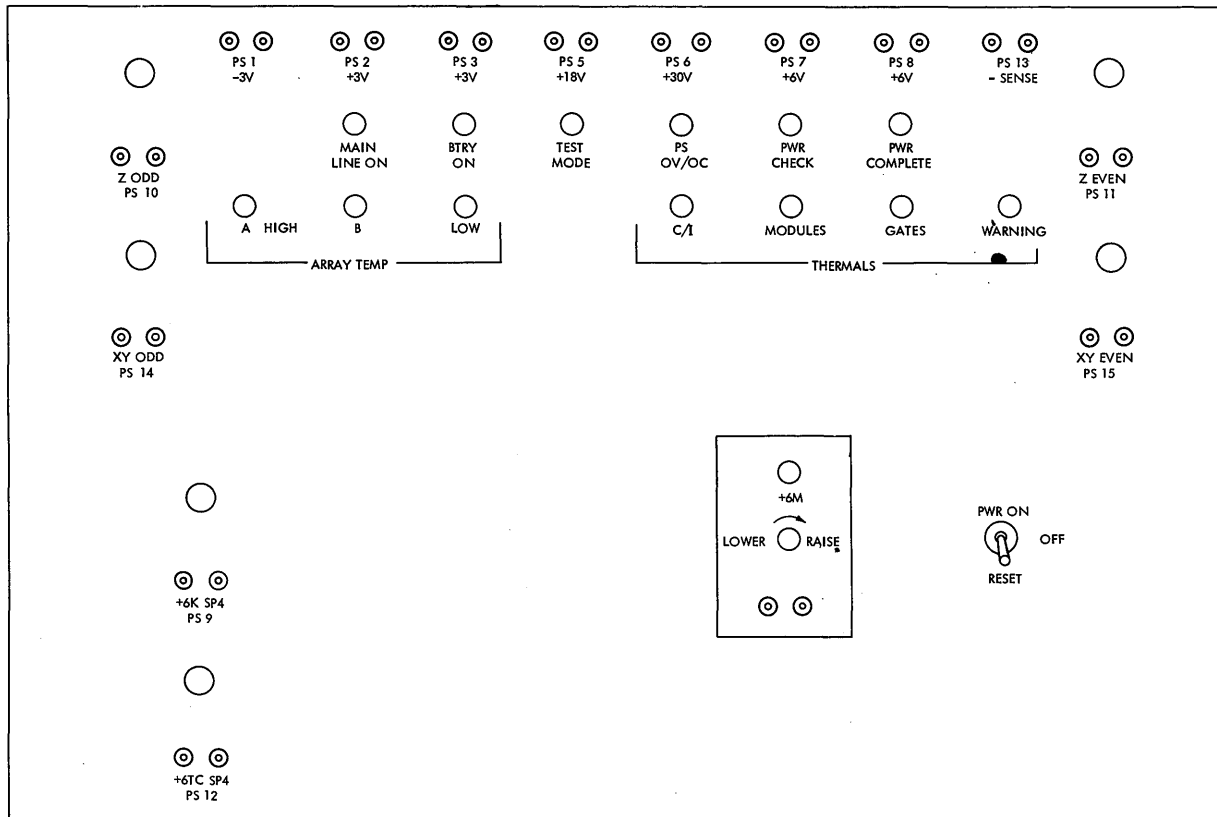
●Figure 4-12.   DE Power Control Panel

Table 4-3. DE Maintenance Panel Toggle Switches

| NAME | QUANTITY |
|---|---|
| Data Entry | 9 |
| Address Entry | 16 |
| Mark Entry | 9 |
| Inkeys | 6 |
| CCR Entry | 31 |
| CE Select | 4 |
| CVG Select | 24 |
| Storage Select (Main/Local) | 1 |
| Store | 1 |
| Test and Set | 1 |
| Set Key/Insert Key | 1 |
| Priority/Storage | 1 |
| Single Cycle | 1 |
| Worst Case/Data Keys | 1 |
| Stop on Check | 1 |
| Auto Restart | 1 |
| Log Mode | 1 |
| Log Address | 3 |
| Indicator Test/Indicator OFF/Normal | 1 |
| Test Mode/Normal | 1 |

Table 4-4. DE Maintenance Panel Pushbuttons

| NAME | QUANTITY |
|---|---|
| Stop | 1 |
| Start | 1 |
| General Reset | 1 |
| Check Reset | 1 |
| Set CCR | 1 |
| Refresh Pulse | 1 |
| Pulse DG | 1 |
|   Forces one **112** ns pulse on DG Interface | |

**Table 4-5.** DE Maintenance Panel Rotary Switches

| NAME | NUMBER OF POSITIONS |
|---|:---:|
| DG Register Select<br>  Selects one of eight Interfaces | 8 |
| Indicator Select<br>  Selects Address and Data from<br>  storage or Selects 1 of 4 DG Registers | 5 |

All manual switches and pushbuttons on the DE maintenance panel (Figure 4-11) are under control of the CCR State bits and the Test switch, including the Lamp Test switch. The Test switch is active only in State Zero.

On the DE power control panel (Figure 4-12) the Power ON/OFF switch is under control of the CCR State bits and Test switch. Voltages may be monitored in any state. The Marginal Check controls, Thermal Reset, and Element MPO Switch are always operational.

Two momentary contact switches are located in the DE power section and are always operational.

OTC Test – This switch simulates the thermal warning condition and causes ELC to be sent to all CE's.

OBS Test – This switch simulates the on-battery condition and causes ELC to be sent to all CE's.
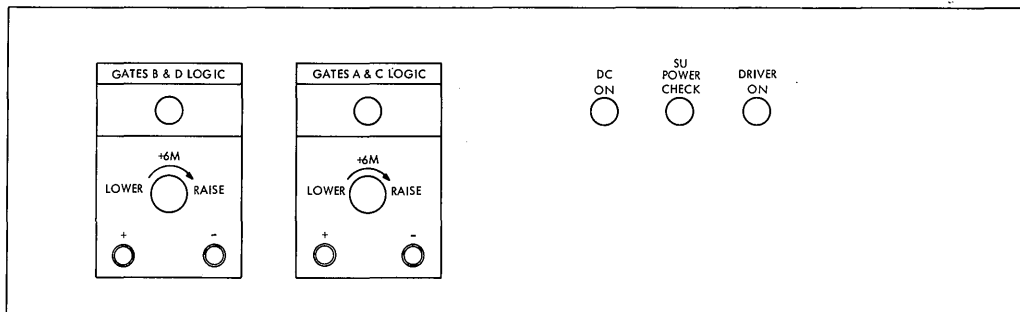


•Figure 4-13. SU Power Control Panel

## Switches

DC Register Selection - This eight position rotary switch selects the DG whose register contents and CVG address will be displayed in the DG Indicators.

Indicator Selection - This five position rotary switch controls the use of several sets of indicators.

1. Address Registers

    A.  Positions A, B, C or D - Display the content of the associated Address Register, and Local Store Incrementer.

    B.  Storage Position - Display the contents of Odd and Even SAR.

2. Data Register

    A.  Position A,B,C, or D - Display the contents of the selected Even Data Register.

    B.  Storage Position - Display the content of the SDBO.

3. Refresh Controls

    A.  Position A,B,C,D - Display the setting of the Start of Display and End of Display Latches associated with the selected Data Register.

    B.  Storage Position - Degated such that all indicators will be on.  (Same as indicator test.)

Log Address - Three switches provided to allow selection of log-words for display in the Data Register indicators.  Counts of 0 through 5 are used to display logout doublewords 0 through 5 (logwords 0 through 11).

If counts of 6 or 7 are used, the data displayed is zeros.

In Keys - Five switches are provided to store data into the specified SP4 address location.  Parity shall be manually inserted with the associated parity switch.  Parity must be odd.

Mark Keys - Eight switches are provided to control gating of the 72-bit data word into storage.  Each of the eight Mark bits controls the gating into storage of one eight-bit byte (plus parity). Parity shall be manually inserted via the parity switch associated with the Mark switches.  Parity must be odd.

Address Keys - Fourteen address switches are provided on the maintenance panel to select any specified address or group of addresses. Two parity switches are provided to facilitate automatic or forced parity generation.  Each switch has three positions (Force 0, Ripple, and Force 1).

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Switches 1-14 being in either the Force 0 or Force 1 position will cause the Address Counter to be set to the specified address value. When the switches are in the Ripple position, the Address Counter will step binarily with each cycle for those bit positions whose switches are in the Ripple position.

Switches $P_A$ and $P_B$ being in the Ripple position will allow automatic parity generation to occur. These switches may be placed in Force 0 or Force 1 positions to override the automatic parity generation. This may result in either good or bad parity to be assigned.

The sending of odd and even selects to storage is controlled by the Priority Select switch for CE #1 when in "storage" mode. All other Priority Select switches are ignored.

The Address Switches are also used as data switches when performing manual store operations into the Local Store Registers.

Priority Select Switches - Twenty-eight switches are provided to test the Priority Scan logic in the SU. The function of the switches are as follows:

CE (1-4)    These switches shall simulate even, odd or no Compute Element Selects. Any combination of these switches and other priority switches may be used to exercise the Priority Scan logic.

NOTE:   The switch for CE #1 is also used in conjunction with manual store and fetch operation selections when in storage mode.

CVG (1-24) These switches shall simulate requests from the CVGs.

NOTE:   These switches shall also be used for Local Store Register selection on manual store and fetch operations.

Storage Data Entry Switches - Eight data switches plus parity are provided to store any bit combination into a specified address location. Parity shall be manually inserted. These switches, in conjunction, with the Mark switches, specify the data and byte (or bytes) to be stored. During a Fetch operation the contents of the specified address is compared with the contents of the data switch settings on a bit-by-bit basis. Failure of a comparison shall cause the Compare (CMPR) Check indicator to be turned on.

Configuration Register Switches - Twenty-seven switches plus four parity are provided to allow manual setting of the Configuration Control Register (CCR). Parity shall be manually inserted. When the Set Configuration pushbutton is depressed, the switch content is transferred to the CCR. Redundancy checking of the DE-DG Configuration bits will be performed. Parity check will also be performed on the CCR. The appropriate check indicator will be turned on if either error is detected (CONFIG RDN or CONFIG PAR).

Store Switch - This two position switch controls the routing of data to storage or the Local Store Registers when it is in the Store position and from storage or Local Store Registers (with a comparison to the worst case patterns or the data switches) when in the Off position and no other operation is in process.

Test and Set (TAS) Switch - This two-position switch, when in the "TAS" position and in conjunction with a Fetch (i.e., no Store, Set or Insert Key operations) causes the selected byte(s) (controlled by the Mark Switches which must be set) of the addressed doubleword to be placed on the SDBO and regenerated to core as all ones. All other bytes are regenerated without change. Address, Mark, Key or Protect Checks will inhibit the forced ones and all bytes will be regenerated. All zeros with good parity will appear on the SDBO following a protected area violation.

Log Mode Switch - Placing this switch in the ON position allows exercising of the logout control logic via the Log Address switches. It also stops the DE.

To activate the operation, the Start pushbutton must be depressed. Logout data for the doubleword selected by the three Log Address switches (binary code) will appear in the Data Register indicators. A new doubleword may be selected by changing the address switches and depressing the Start pushbutton.

Auto Restart Switch - This switch forces a reset and restart operation to allow for cycling on an error condition. Operation is similar to the use of the Check Reset and Start pushbutton operations.

Key Switch - This three position switch permits exercising of the Storage Protect Feature. The function of the switch position is as follows:

Set:      In this position, a Set Key Command is generated and
          Indicates the subsequent storing of the contents of the
          In Key switches into the specified Storage Protect address
          location.

Insert:   In this position, an Insert Key Command is generated which
          shall cause the information at the specified Storage Pro-
          tect address to be transferred to the maintenance panel
          where it is compared against the content of the In Key
          switches.

OFF:      The switch is placed in this position when not performing
          Storage Protect operations.

Priority/Storage Switch - With this switch in the Storage position, the SU Priority Scan logic is bypassed. Data and control signals are gated directly from the test logic to the storage common logic.

When the switch is in the priority position, the priority logic is exercised by simulating user selects with the Priority Select switches.

Single Cycle Switch - This two-position switch controls the access
mode. When in the OFF position, all operations are performed in
their normal manner.

When the switch is in the Single Cycle position, for each depression
of the Start pushbutton, the processing of one priority slot will
take place based on the Priority Select and Sequencer values.

Stop On Check Switch - With this switch in the OFF position, the DE
will stop only on DG Checks provided that the Inhibit DE Stop bit
in the CCR is off.

When the switch is in the Stop on Check position, the DE will stop
on any check condition regardless of the setting of the Inhibit DE
Stop bit in the CCR.

Worst Case/Data Keys Switch - When this switch is in the Data Keys
position the contents of the eight Storage Data Entry switches plus
parity are used.

When the switch is in the Worst Case position, data shall be trans-
ferred to storage in the following pattern.

A first 64 locations    - all ones.
B second 64 locations   - all zeros.
C third 64 locations    - all ones.
D fourth 64 locations   - all zeros.
E fifth 64 locations    - all zeros.
F sixth 64 locations    - all ones.
G seventh 64 locations  - all zeros.
H eighth 64 locations   - all ones.

NOTE:  all "locations" are doublewords.

The cycle repeats starting at step A until all of storage is loaded.
The operation is stopped by depressing the Stop pushbutton.  Fetch
data is compared during either operation when in Storage Test mode.

Storage Select - This two position switch works in conjunction with
the Storage Data Entry, Address, Priority Select, and Store switches
to control store and fetch operations with storage and the Local
Store Registers.  The switch selects either local or main storage.

Test/Normal Switch - When this switch is placed in the Test position,
the test logic samples the CCR State Bit decoding logic for the 0
condition.  When this condition is found, all control and data paths
for test functions are enabled.  All user interfaces are disabled
and the unit is electrically disconnected from the system.  When this
switch is restored to the Normal position, all test logic is reset
and disabled, a Test/Normal reset is performed, and the State Bits
(in the CCR) are set to zero (0).  The SCON bits remain as they were
in Test, the CE Communication Bits and DE/DG bits are not altered,
and the unit is restored to the system.

Stop Pushbutton - Depression of this pushbutton shall prevent the test circuitry from initiating another cycle.

Start Pushbutton - The function performed when this pushbutton is depressed will depend upon the setting of the various sequence switches (Store, Log Mode; Single Cycle, etc.). Basically, it will cause resetting of the Stop Latch and allow the selected sequence to begin operation.

General Reset Pushbutton - Depressing this pushbutton will cause a resetting action in the following:

        CE Select Latches
        CE/DG Priority Sequencers
        Scan Latches
        SOD Triggers   (ON)
        EOD Triggers   (ON)
        Refresh Counter
        DG Even/Odd Buffers
        DG Registers
        Halfword Counters
        Configuration Control Register
                (Turns on parity and SCON bits.  Resets all others)
        Logout Controls
        Error Latches

Check Reset Pushbutton - Depressing this pushbutton will cause a resetting action of the Logout Controls and Error Latches.

**Pulse DG Pushbutton - This pushbutton simulates the DG interface sequence by stepping the halfword counters.  When the high order bit of the halfword counter is set, each depression of the pushbutton will cause the transfer of the next 16 bits from all Data Registers to their configured DG Reigsters.**

Refresh Pulse Pushbutton - When the DE is stopped or in Single-Cycle mode, the Refresh Counter is incremented at manual speed.  Once an End-of-Display (EOD) Command has been decoded for a CVG, no further requests from that CVG will be honored until a Refresh Pulse has been generated (Synchronous Mode).  In order to simulate this 18 millisecond timeout condition, this pushbutton has been provided to generate this Refresh Pulse.

Set Configuration Pushbutton - Depression of this pushbutton shall cause the contents of the Configuration Register Switches to be entered into the Configuration Control Register and applicable indicators to be turned on.

Indicators Switch - This three-position switch allows testing of all indicators on the maintenance panel.  The function of each position is as follows:

Test - All indicators are turned on.

Inactive - All indicators are disabled (turned off).

Normal - On and off state of indicators is determined by the
associated trigger or latch setting.

Indicators

DG Register Check - Eight indicators.  One indicator for each of
eight 16-bit DG Registers.  A parity error in any of these registers
would cause the associated check indicator to be lit.

Fetch (Odd/Even) - One indicator for each side of storage which is
lit when that side is performing a fetch operation.

Mark Check (Odd/Even) - Two indicators from storage common to the
test panel to indicate that a mark parity check has been detected.

SAR Check (Odd/Even) - Two indicators from storage common to the
test panel to display a SAR Check (parity) condition.

Data Byte (Odd/Even) - Sixteen indicators from storage common to
the test panel to indicate which odd or even data byte had a check
condition.

Storage Project - Three indicators from storage common to the test
panel to indicate check conditions detected by the storage protect
feature.

Address:   This indicator is turned on when the SP detects even
           parity in the address.

Key:       This indicator is turned on when the SP detects even
           parity in the Out Key or In Key.

SAP:       This indicator is turned on if there is not an equal
           compare between the In Key and the contents of the
           specified SP address location either during a store,
           or when the Fetch Protect bit is on in the stored key
           during a fetch.

Tag Check - Two indicators that are turned on by errors detected
in the tag field (SAB bits 1-5) sent from the CE to the DE.

Parity (PAR) - Bad parity on the tag field.

Match - Mismatch between the tag field sent by the CE and the
wired-in tag field in the DE.

Multiple Accept - This indicator is turned on by the SU Priority Scan logic if there is an attempt to service more than one user or odd and even from the same user simultaneously.

NOTE:    This indicator is turned on in Test mode by turning on the T & S switch and the Set Key switch.

Compare Check - When in Storage Test mode, this indicator is turned on during an even or odd cycle if the fetched data does not compare with the data keys.  When the check is received, the Stop On Check test switch shall be sensed.

Refresh Counter Check - This indicator is turned on when a parity error is detected in the 12-bit Refresh Counter.

Normal Operation Check - This indicator is turned on as a result of the DE receiving Store or Fetch (absence of other commands) commands without the Normal Operation signal.  It can also be turned on by the DE receiving a Set Key, Insert Key, or Test and Set with the Normal Operation signal.

Local Store Check - This indicator is turned on by a parity error detected at the input to the Local Store Registers.

Configuration Check - Two indicators that are turned on by errors detected in the Configuration Register.

Redundancy - This indicator is turned on when more than one DG Register is configured to a Data Register or when more than one Data Register is configured to a DG Register.

Parity - This indicator is turned on when a parity check is detected in the Configuration Register.

DG Data - Eighteen indicators are provided to display sixteen data bits and two parity bits from the DG Register selected by the DG Register Selection rotary switch.

CVG Address - This indicator is switchable to any of the eight DG interfaces by way of the DG Register Selection Switch.  It indicates the on (1) or off (0) condition of the serial Address line at the DG interface.

EOD - This indicator is turned on when an End-of-Display command is decoded in the SDBO.

TRF - This indicator is turned on when a Transfer Command is decoded in the SDBO.

EV/O - This indicator is on when the sequence or CVG requests is even followed by odd. It is off when the sequence is odd followed by even.

Outkey/Inkey Registers - Two rows of indicators consisting of five bits each plus parity from the SP to display the contents of the Out Key ·and In Key Registers.

Mark (Odd/Even) - Two rows of indicators consisting of eight bits each plus parity from storage common to display the contents of the Mark Registers. When a parity check is detected on the specified Mark Register, the appropriate Mark Check Indicator is turned on.

Address Registers - Twenty-eight indicators plus four parity. When the Indicator Selection switch is in the Storage position these indicators display the contents of the Odd and Even Storage Address Registers. When the selection switch is in any other position, the indicators display the content of the associated Address Register and the Incrementer.

NOTE:   Manual Display Local Store gates the OR of all selected CVG's (therefore only one should be selected) on a bit basis. The displayed value is placed in all 4 Address Registers.

Sequencer - Eleven indicators which are used to display the progress of the Priority Scan circuits.

The starting point for the Priority Scan is A-1 (CVG #1 of the DG that is configured to Data Register A). This will be followed by B-1. (Reference Slotted Priority Scheme, Figure 4-6).

Priority Select (CE/CVG) - Twenty-eight indicators which will turn on in normal operation for approximately 3.6 microseconds when the request for the associated CVG has been honored. CE indicator is only on when request is waiting in LO select latches. In Single-Cycle mode, the indicator will stay on from the time the request has been honored until the time of the next priority slot occurs for the same DG.

Data Register - Seventy-two indicators are provided to display sixty-four bits of data and eight parity bits. The bits are divided into eight groups of eight bits, each plus parity. Each eight bit group is graphically subdivided, into two (2) four bit groups to facilitate reading of data.

The indicators display the contents of the Even Data Registers A,B,C,D or the Storage Data Bus Out.

Halfword Counter - Four indicators used to display the contents of the Halfword Counter as selected by Indicator selection switch.

Configuration Register - Thirty-one indicators are provided to display the twenty-seven Configuration Bits and their four associated parity bits.

Test - Indicates that the DE is in State 0 with the Test/Normal switch in the Test position.

Stop - Indicates the status of the Stop Latch.  Turned on by a Single Cycle, Stop Pushbutton, error detected with Stop on Check switch on, Master Reset, Test Mode single-shot, or Log Mode.


DE/DG CONFIGURATION

DE/DG Interconnection Assignment

Table 4-6 and 4-7 show DE/DG interconnection assignments for a 60-PVD and 90-PVD system.  Each DE has four quadword registers and eight interfaces.  Each interface may be connected to one of two adapters by configuration control.  Since there are four adapters, at any one time four interfaces may actively connect four DG's to a DE.  The numbers in the matrix indicate the interface.  Since each DG has two interfaces, there are a total of 24 (60 PVD System) 34 (90 PVD System) DG interfaces including two spare DG's.

DE-1 and DE-3 are used to provide the required DE/DG interfacing to the spare DG's (DG-Spare (SP) 1 & DG-Spare (SP) 2).  Each of these DE's is capable of interfacing to either spare DG under Configuration control.  In a 60-PVD and 90-PVD system, either DE-1 for DE-3 must be in the active system along with a redundant adapter with a path configurable to the spare DG, so that upon a single CVG failure reconfiguration action will only involve the failed CVG and the spare CVG brought on line.  To provide for training or other uses of the spare consoles, either DE-1 or DE-3 must be included in the redundant system.

| Qty of DE's | Qty of DG's | Qty of Active PVD's | Qty of Spare PVD's | Total Qty of PVD's* |
|---|---|---|---|---|
| 2 | 4 | 18 | 6 | 24 |
| 3 | 8 | 42 | 6 | 48 |
| 4 | 12 | 60 | 12 | 72 |
| 4 | 13 | 66 | 6 | 72 |
| 5 | 17 | 90 | 6 | 96 |

* This number represents the maximum number of PVD's that can be working in the system.

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Table 4-6 shows typical connections for the active DE's in the System. For each of the following cases, it is shown that the system can lose one DG and one DE and retain full operational capability.

DE/DG CONFIGURATION (60 PVD SYSTEM)

The following are sample cases (Refer to Table 4-6) which are included to show that the system may lose one DE and one DG and still retain full operational capability in the 60 PVD Configuration.

Case 1 DE 1 Off Line

| Event | Reconfiguration Action |
|---|---|
| Loss of one DG (3-7) | DG SP-1 to adapter D of DE 3 |
| Loss of one DG (8-12) | DG SP-2 to adapter A of DE 3 |

Case 2 DE 2 Off Line

| Event | Reconfiguration Action |
|---|---|
| Loss of one DG(3-7) | DG SP-1 to adapter D of DE 3 |
| Loss of one DG(8-12) | DG SP-2 to adapter A of DE 3 |

Case 3 DE 3 Off Line

| Event | Reconfiguration Action |
|---|---|
| Loss of one DG (3-7) | DG SP-1 to adapter D of DE 1 |
| Loss of one DG(8-12) | DG SP-2 to adapter A of DE 1 |

Case 4 of DE 4 Off Line

| Event | Reconfiguration Action |
|---|---|
| Loss of one DG (3-7) | DG SP-1 to adapter D of DE 1 |
| Loss of one DG (8-12) | DG SP-2 to adapter D of DE 1 |

Table 4-6.  DE/DG Interconnection Assignment Matrix

|  | DE 1 | DE 2 | DE 3 | DE 4 |
|---|---|---|---|---|
| CASE 1-DGs - | NONE | 5,6,7,8 | 9,10 | 3,4,11,12 |
| CASE 2-DGs - | 4,5,6,7 | NONE | 8,9 | 3,10,11,12 |
| CASE 3-DGs - | 4,5 | 6,7,8,9 | NONE | 3,10,11,12 |
| CASE 4-DGs - | 3,4 | 5,6,7,8 | 9,10,11,12 | NONE |

| DG | DE 1 | | | | DE 2 | | | | DE 3 | | | | DE 4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | A | B | C | D | A | B | C | D | A | B | C | D | A | B | C | D |
| 3 | 1 | 1 |  |  |  |  |  |  |  |  |  |  | 4 |  |  | 4 |
| 4 |  | 2 | 2 |  |  |  |  |  |  |  |  |  | 5 | 5 |  |  |
| 5 |  |  | 3 | 3 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
| 6 | 4 |  |  | 4 |  | 2 | 2 |  |  |  |  |  |  |  |  |  |
| 7 | 5 | 5 |  |  |  |  | 3 | 3 |  |  |  |  |  |  |  |  |
| 8 |  |  |  |  | 4 |  |  | 4 | 1 | 1 |  |  |  |  |  |  |
| 9 |  |  |  |  | 5 | 5 |  |  |  | 2 | 2 |  |  |  |  |  |
| 10 |  |  |  |  |  |  |  |  |  |  | 3 | 3 | 1 | 1 |  |  |
| 11 |  |  |  |  |  |  |  |  | 4 |  |  | 4 |  | 2 | 2 |  |
| 12 |  |  |  |  |  |  |  |  | 5 | 5 |  |  |  |  | 3 | 3 |
| SP-1(3-7) |  |  | 7 | 7 |  |  |  |  |  |  | 7 | 7 |  |  |  |  |
| SP-2(8-12) | 8 |  |  | 8 |  |  |  |  | 8 |  |  | 8 |  |  |  |  |

60 PVD System

DE/DG CONFIGURATION (90 PVD SYSTEM)

❙The following are sample cases (Refer to Table 4-7) which are intended to show that the system may lose one DE and one DG and still retain full operational capability in the 90 PVD Configuration.

Case 1 DE 5 Off Line

| Event | Reconfiguration Action |
|-------|------------------------|
| Loss of one DG (3-9) | DG SP-1 to adapter D of DE 3 |
| Loss of one DG (10-17) | DG SP-2 to adapter D of DE 3 |

Case 2 DE 4 Off Line

| Event | Reconfiguration Action |
|-------|------------------------|
| Loss of one DG (3-9) | DG SP-1 to adapter D of DE 1 |
| Loss of one DG (10-17) | DG SP-2 to adapter D of DE 1 |

Case 3 DE 3 Off Line

| Event | Reconfiguration Action |
|-------|------------------------|
| Loss of one DG (3-9) | DG SP-1 to adapter D of DE 1 |
| Loss of one DG (10-17) | DG SP-2 to adapter D of DE 1 |

Case 4 DE 2 Off Line

| Event | Reconfiguration Action |
|-------|------------------------|
| Loss of one DG (3-9) | DG SP-1 to adapter D of DE 3 |
| Loss of one DG (10-17) | DG SP-2 to adapter D of DE 3 |

Case 5 DE 1 Off Line

| Event | Reconfiguration Action |
|-------|------------------------|
| Loss of one DG (3-9) | DG SP-1 to adapter D of DE 3 |
| Loss of one DG (10-17) | DG SP-2 to adapter D of DE 3 |

Table 4-7.  DE/DG Interconnection Assignment Matrix

|        | DE 1 | DE 2 | DE 3 | DE 4 | DE 5 |
|--------|------|------|------|------|------|
| CASE 1-DGs - | NONE | 6,7,8,9 | 10,11,12 | 13,14,15,16 | 3,4,5,17 |
| CASE 2-DGs - | 6,7,8 | NONE | 9,10,11,12 | 13,14,15,16 | 3,4,5,17 |
| CASE 3-DGs - | 5,6,7 | 8,9,10,11 | NONE | 12,13,14,15 | 3,4,16,17 |
| CASE 4-DGs - | 4,5,6,7 | 8,9,10,11 | 12,13,14 | NONE | 3,15,16,17 |
| CASE 5-DGs - | 3,4,5,6 | 7,8,9,10 | 11,12,13 | 14,15,16,17 | NONE |

| DG | DE 1 | | | | DE 2 | | | | DE 3 | | | | DE 4 | | | | DE 5 | | | |
|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|    | A | B | C | D | A | B | C | D | A | B | C | D | A | B | C | D | A | B | C | D |
| 3  | 1 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4 |   |   | 4 |
| 4  |   | 2 | 2 |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 5 |   |   |
| 5  |   |   | 3 | 3 |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 6 |   |
| 6  | 4 |   |   | 4 | 1 | 1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 7  | 5 | 5 |   |   |   | 2 | 2 |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 8  |   | 6 | 6 |   |   |   | 3 | 3 |   |   |   |   |   |   |   |   |   |   |   |   |
| 9  |   |   |   | 4 |   |   |   | 4 | 1 | 1 |   |   |   |   |   |   |   |   |   |   |
| 10 |   |   |   |   | 5 | 5 |   |   |   | 2 | 2 |   |   |   |   |   |   |   |   |   |
| 11 |   |   |   |   |   | 6 | 6 |   |   |   | 3 | 3 |   |   |   |   |   |   |   |   |
| 12 |   |   |   |   |   |   |   |   | 4 |   |   | 4 | 1 | 1 |   |   |   |   |   |   |
| 13 |   |   |   |   |   |   |   |   |   | 5 | 5 |   |   | 2 | 2 |   |   |   |   |   |
| 14 |   |   |   |   |   |   |   |   |   |   | 6 | 6 |   |   | 3 | 3 |   |   |   |   |
| 15 |   |   |   |   |   |   |   |   |   |   |   |   | 4 |   |   | 4 | 1 | 1 |   |   |
| 16 |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 5 |   |   | 2 | 2 |   |
| 17 |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 6 |   |   | 3 | 3 |
| SP-1 (3-9) |   |   | 7 | 7 |   |   |   |   |   |   | 7 | 7 |   |   |   |   |   |   |   |   |
| SP-2(10-17) | 8 |   |   | 8 |   |   |   |   | 8 |   |   | 8 |   |   |   |   |   |   |   |   |

90 PVD System

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INTRODUCTION

The IBM 7231-02 Input/Output Control Element (IOCE) is an advanced, solid state functional element that enables I/O units to be attached to the 9020D/E System. It does this by providing and controlling two selector channels and a multiplexor channel to which I/O control units can be attached. The IOCE operates in conjunction with 7201-02 Computing Elements (CE) and 7251-09 Storage Elements (SE) in a multiprocessing configuration. I/O control units attach to the IOCE via the channels. The IOCE can also operate as a processor under control of the 7201-02 Computing Element. The IOCE can perform I/O operations and processing concurrently.

   The 7231-02 incorporates extensive error checking, diagnostic and service aids. Major attributes of the element are:

1.   Simultaneous operation of up to 256 subchannels on the multiplexor channel and a high-speed device on each selector channel.

2.   Data paths to and from each SE.

3.   Optional channel-to-channel adapters, housed within the IOCE, to provide data paths between IOCE's of separate 9020 Systems.

4.   The 7231-02 channel operations are initialized by a 7201-02 computing element and proceed independently of the CE until an interruption occurs.

5.   A self-contained core storage that is used to store control words for the multiplexor channel and provides storage for IOCE Processor operations, I/O channel data, and for maintenance operations.

6.   The IOCE internal operation is controlled by a capacitor read-only storage.

7.   A sixty-four (64) word local storage that is used for selector channel control words, temporary storage for multiplexor channel control words, IOCE Processor operations, and maintenance operations.

8.   The 7231-02 processor operations are initiated by a 7201-02 Computing Element and proceed independently until either an interruption occurs or until the processor is stopped by the 7201-02.

9.   The 7231-02 processor can execute a subset of the 9020 instruction set independent of any channel operation. (See IBM 9020D and 9020E System Principles of Operation Appendix H.)

GENERAL CHARACTERISTICS

Each IBM 7231-02 IOCE contains:

1.  The logic necessary to execute CE initiated operations,
    control data flow between storage and I/O units, exe-
    cute instructions for data processing, and provide for
    stand-alone servicing and maintenance.

2.  MACH (Maintenance And CHannel) storage.

3.  Multiplexor and Selector Channel circuitry.

4.  A Control Panel.

This equipment is housed in three frames.  One frame contains
channel circuitry and most of the IOCE logic; the second con-
tains the MACH storage.  The third frame, located at the junc-
tion of the first two, contains the power controls and power
supplies for the IOCE, plus additional IOCE logic.  The IOCE
logic in the first and third frames is referred to as the
Common Logic Unit (CLU).

Common Logic Unit (CLU)

The CLU contains transistor registers, data transfer paths, and
controls.  The CLU also has twenty-one (21) full-word registers
used for channel data and control storage.  These registers are
located in a sixty-four (64) word, 0.5 microsec core storage
unit (Local Storage) that is also used for working registers in
various CLU and diagnostic operations.

    Data flow is controlled by a Read-Only Storage Unit.  This
is a capacitor storage unit operating on a 0.5 usec cycle.  Data
parity is checked during transfer for each eight-bit byte with-
in the full word.

MACH Storage

MACH (Maintenance and Channel) storage is a 32K word, 2.0 usec
cycle core storage contained in the IOCE.  Part of this storage
(1024 words) is used to store control words for the multiplexor
channel (four words per subchannel).  The remainder provides
storage facility for processor operations, channel data, and
maintenance operations.

Multiplexor Channel

The 7231-02 is equipped with one Multiplexor Channel.  This
channel is capable of controlling several low to medium speed
I/O units simultaneously in multiplex mode or a single higher speed
unit in burst mode.

When operating in the multiplex mode, the channel uses the CLU for the length of time it takes to service the transfer of a data byte or group of data bytes. This involves the fetching of the control words for that unit, the fetching or storing of the data byte, and the updating and storing of the control words.

When operating in the burst mode, only one device at a time may use the Multiplexor Channel. Data is .transferred one byte at a time. However, the control word is retained in Local Storage during the entire operation of the channel rather than being fetched and returned to MACH storage for each byte transfer. This reduces the number of MACH-storage references.

Selector Channel

The 7231-02 is equipped with two Selector Channels (expandable to three channels in the first two IOCE's within a 9020 System). A Selector Channel is capable of handling high speed I/O devices.

Selector Channels operate in burst mode. Only one device may be selected at a time, and no other I/O device on the Selector Channel can operate until the activity of the selected unit has been terminated. Although data is transmitted a byte at a time between the I/O device and the channel, data transfers between SE and a Selector Channel are serial by word. Channel control words retained in Local Storage of the 7231-02, reduces the usage of the CLU and is one of the factors that enables a Selector Channel to operate at a higher rate than the Multiplexor Channel. A Selector Channel is designed to the "Input/Output Interface, Channel to Device Control Unit Specifications", (Appendix D), and can control any device designed to this interface whose data rate does not exceed that of the channel.

Channel-to-Channel Adapter

An optional Channel-to-Channel Adapter feature provides data paths between IOCE's of different 9020 Systems (reference Figure 5-1 for sample channel-to-channel usage). The adapter is housed in one of the two channels between which communication paths are required. In a particular IOCE, up to two Channel-to-Channel Adapters may be installed, one in Selector Channel 1 and/or one in Selector Channel 2. The Channel-to-Channel Adapter appears to each channel as a standard control unit and is connected by means of the standard I/O interface as described in Appendix D.

IOCE Control Panel

The IOCE Control Panel contains the switches and indicators used to monitor and maintain the 7231-02. It is mounted on the end of the frame containing the CLU. The functions which can be performed from the Control Panel are:

    1.  Reset the element.

CCC

DCP

IOCE 1

SEL 1

SEL 2

CTC #1
CU : CU

TO OTHER
CONTROL UNITS

IOCE 2

SEL 1

SEL 2

CTC #5
CU : CU

TO OTHER
CONTROL
UNITS

IOCE 3

SEL 1

SEL 2

CTC #3
CU : CU

TO OTHER
CONTROL
UNITS

IOCE 1

SEL 1

SEL 2

SEL 3

CTC #2
CU : CU

TO OTHER
CONTROL UNITS

TO OTHER
CONTROL UNITS

TO OTHER
CONTROL UNITS

IOCE 2

SEL 1

SEL 2

SEL 3

CTC #4
CU : CU

CTC #6
CU : CU

TO OTHER
CONTROL UNITS

TO OTHER
CONTROL UNITS

TO OTHER
CONTROL UNITS
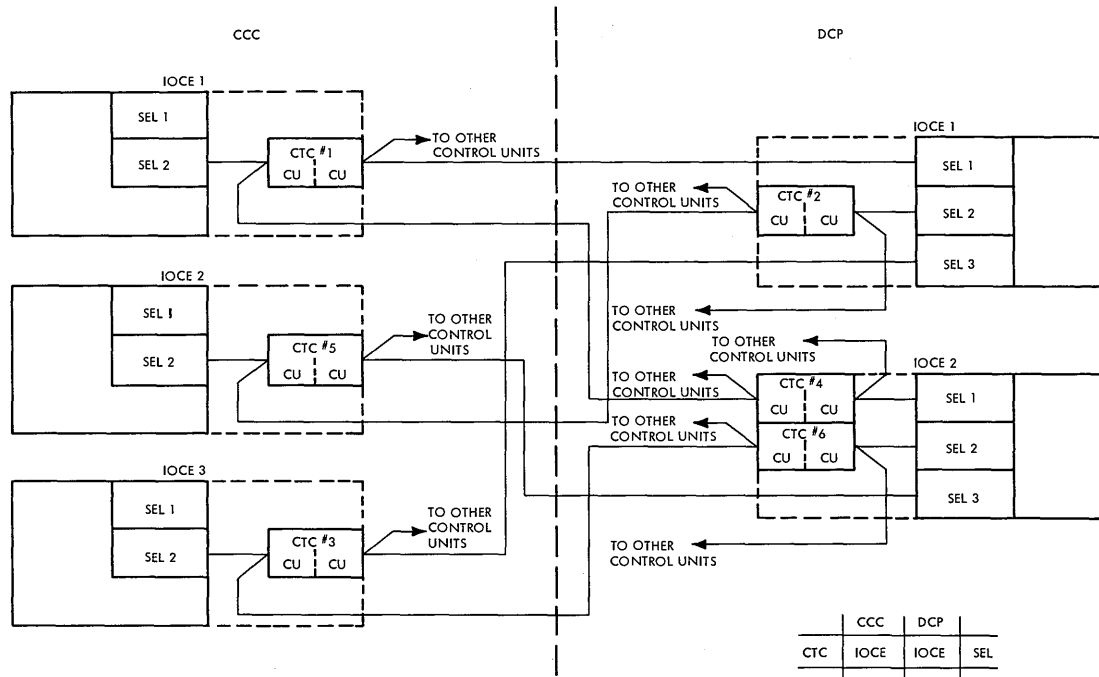
3-CCC/IOCE'S        2-DCP/IOCE'S

• 2-SIMULTANEOUS CTC PATHS

• RECONFIGURATION ON 1-SUBSYSTEM DOES NOT REQUIRE RECONFIGURATION IN
  OTHER BUT DOES REQUIRE THAT OTHER BE NOTIFIED THROUGH PROGRAMMING.

• DUAL PATH MAINTAINED

|     | CCC | DCP |     |
| --- | --- | --- | --- |
| CTC | IOCE | IOCE | SEL |
| 1 | 1 | 1 | 1 |
| 2 | 2 | 1 | 2 |
| 3 | 3 | 1 | 3 |
| 4 | 1 | 2 | 1 |
| 5 | 2 | 2 | 3 |
| 6 | 3 | 2 | 2 |

Figure 5-1.   Sample Channel-To-Channel Adapter Usage

2.  Store and display information in MACH storage, local
    storage, registers, main storage, etc.

3.  Control maintenance operations.

When the 7231-02 is operating in States Two and Three, the manual
controls are disabled.  Limited manual controls are available in
State One, and all controls are either enabled or can be enabled
in State Zero.

I/O Attachment

Input/Output devices are attached to the 9020 System via control
units which connect to either Selector or Multiplexor Channels.
The interface, defined as "Input/Output Interface Channel to
Device Control Unit", is described in Appendix D.

Device Control Units attached via this interface to the
Multiplexor Channel are:

1.  PAM

2.  System Console (9020D)

    a.  1052 I/O Printer Keyboard Adapter

    b.  2821 Control Unit for 2540 and 1403

3.  Configuration Console (9020E)

    a.  2821 Control Unit for 2540 and 1403

4.  Data Adapter Unit (DAU)

5.  1052 I/O Printer Keyboard Adapter (CE-9020E)

Control Units attached via this interface to the Selector Channel
are:

1.  Tape Control Unit (TCU)

2.  Channel-to-Channel Adapter

3.  Storage Control Unit (SCU)

FUNCTIONAL CHARACTERISTICS

The IOCE will respond to the following instructions executed by
a CE:

    Start I/O

    Test I/O

    Test Channel

    Halt I/O

Set PCI

SCON (Set Configuration)

SATR (Set Address Translator)

SIOP (Start I/O Processor)

Write Direct

The first five instructions are associated with I/O operations. The SCON instruction is associated with configuration control. The SATR instruction is associated with storage address translation. The SIOP and Write Direct instructions are associated with processor operations.

The IOCE is under configuration control as are all major elements in the IBM 9020D/E Systems. Within the CLU, there is a configuration control register (CCR) which defines:

1. the state of the element;

2. the elements from which the IOCE will accept normal data and control directives; and

3. those CE's which can reconfigure the IOCE or change its Address Translation Register.

## I/O Operations

All I/O operations are initiated and controlled by I/O instructions, commands and control words. The sequence of operations performed by the IOCE in response to a CE initiated I/O instructions is described below: (Start I/O is assumed.)

The CE recognizes an I/O instruction: it then signals the specified IOCE over the IOCE/CE interface to perform the necessary operations. The CLU under ROS control, determines the condition of the addressed channel, subchannel, and I/O device. See IBM 9020D and 9020E System Principles of Operation manual for condition code responses. The IOCE obtains the contents of the channel address word (CAW) from the PSA of the SE designated by the CE which in turn defines the location of the channel command word (CCW). The CCW defines the command to be executed, the location in storage from or to where the I/O device data is to be transferred, and various control data such as byte count, flags, etc. The control information is stored in MACH storage for Multiplexor Channel operation and in local storage for the Selector Channel; the words in MACH storage are designated UCW (Unit Control Words). The operation defined by the CCW is transmitted to the I/O device via the channel and I/O interface. If the channel and I/O equipment are available and not busy, the CE is signalled with the appropriate condition code and response; this releases the CE to continue with its program. Data transfers (for read operations) pass from the I/O control device to the interface, then to the channel in 8-bit bytes. In the case of the Selector Channel,

the bytes are assembled into words (4 bytes), and transfers within the CLU as well as to the storage are by word. The completion of an I/O operation (without CCW chaining) results in an interruption of the CE and storing of the Channel Status Word in the PSA of the CE designated SE.

I/O Processor Operations

All I/O Processor operations are initiated by the controlling CE with a SIOP (Start I/O Processor) instruction as described below.

The CE decodes the SIOP instruction, insures the data (key and address) are not illegal, and signals the specified IOCE over the IOCE/CE interface. The CLU uses the data sent (key and address) to address a location in either main or MACH storage, depending on address. The contents of the double word obtained from storage becomes the PSW for the processor with the exception that I/O masking is under CE control, and is not affected by the I/O Processor's PSW. Upon completion of loading the PSW, the CLU signals the CE and then begins processing under the new PSW control.

Processing can be stopped and restarted with the same PSW by use of the Write Direct Stop and Start respectively in the CE.

The I/O Processor can be made to take an external interrupt under control of its own PSW Bit 7 masking by use of a Write External Interrupt from the CE.

Data Flow and Diagram

The IOCE data flow (Figure 5-2) consists of hardware required to control:

    1.   Information transfers between IOCE and CE.

    2.   Information transfers between IOCE and preferential storage area (PSA) within a Storage Element (SE).

    3.   Data transfers between I/O control devices attached to the Multiplexor Channel and the Storage Elements (SE) or MACH storage.

    4.   Data transfers between I/O control devices attached to the Selector Channel and the Storage Elements (SE) or MACH storage.

    5.   Transfer of certain IOCE status conditions to the System Console or Configuration Console.

    6.   Information transfers between CLU and MACH and/or main storage.

The 7231-02 is logically divided into the CLU and the channels.

TO COMPUTING ELEMENTS

```
                    ┌──────────────────────────┐
                    │     IOCE - CE            │
                    │   INTERFACE CONTROLS     │
                    └──────────────────────────┘
```

```
┌──────────────┐   ┌──────────────┐                    ┌──────────────┐
│   IOCE-SE    │   │              │                    │              │      To PAM's and
│  INTERFACE   │   │     CLU      │                    │    MPLX      │      SYSTEM CONSOLE
│  CONTROLS    │   │    DATA      │    ┌──────────┐     │  CHAN (0)    │      or CONFIGURATION
│              │   │    FLOW      │    │          │     │              │      CONSOLE and DAU's
│              │   │     &        │    │  COMMON  │     │              │
│              │   │    ROS       │    │ CHANNEL  │     │              │
│              │   │  CONTROL     │    │          │     │              │
└──────────────┘   │              │    │          │     └──────────────┘
                   │              │    │          │
┌──────────────┐   │              │    │          │     ┌────────┬─────┐
│   IOCE-      │   │              │    │          │     │        │  1  │    To DCP, SCU's, and
│  CONSOLE     │   │   MACH       │    │          │     │        ├─────┤    TCU's if on 9020 D
│  INTERFACE   │   │  STORAGE     │    │          │     │        │  2  │    To CCC and TCU's
│  CONTROLS    │   │              │    └──────────┘     │        ├─────┤    if on 9020 E
│              │   └──────────────┘                     │        │  3  │    OPTIONAL
└──────────────┘                                        └────────┴─────┘
```

TO SE's

TO SYSTEM
CONSOLE
OR CONFIG
CONSOLE

SELECTOR CHANNELS
(1 and/or 2 may contain a channel to channel adapter)

•Figure 5-2.   IOCE Data Flow

Common Logic Unit

The CLU contains data registers, data paths and sequence controls
required to process instructions and to perform the operations it
is directed to by its controlling CE, to service the Selector and
Multiplexor Channels, and to generate and respond to IOCE/CE and
IOCE/SE interface signals.  Many of the registers are held in a small
core storage unit called the Local Storage.  Within this Local Storage,
a group of four words is assigned to each channel; they serve to re-
tain such information as key, command address, controls, data address,
channel states, count and unit addresses.  Other registers are used
for PCI interruption buffer and the general interruption buffer,
temporary R and L buffers, and diagnostic operations.

The CLU data flow includes the transistor register positions and
the data transfer paths connecting them.  A thirty-two (32) bit adder
and an eight (8) bit mover constitute the major portion of the in-
ternal data paths.  The adder is a binary adder.  The mover is used
for byte handling.  It can form the logical connectives of AND, OR,
or EXCLUSIVE OR, and is used extensively for control operations.

The CLU controls include: a microprogram stored in read-only
storage; transistor clock circuits used to cycle this storage; and
decoding circuits by which the CLU controls the data flow path.

Priority control is established in the CLU with channel data receiving the highest priority, CE initiated operations receiving the second order priority, and IOCE-Processor operations taking the lowest priority.

Channels

All channels of the IOCE execute the following commands:

1. Write

2. Read

3. Read Backward

4. Control

5. Sense

6. Transfer in Channel

Each command (except transfer in channel) contains a control order (command modifier) which specifies to the I/O device the details of how the command is to be executed. The exact meaning of the order is a function of the type of I/O device.

The CLU, when it services a channel, does so on the basis of the following priority:

1. Data transfers are serviced first on the Multiplexor Channel (Channel 0); then Selector Channel 1, Selector Channel 2, and if it is present, Selector Channel 3. It should be noted, however, that the Multiplexor Channel will probably be the first to overrun if the data rate limitations of the IOCE are exceeded.

2. The Multiplexor and Selector Channels share certain common controls, which are referred to as the "common channel". This group of controls is primarily concerned with the initiation and termination of I/O operations and with storage priority controls.

3. The channels also share many CLU facilities. They utilize the same read-only storage for microprogram control and use the same data paths for handling nearly all data and control information.

Multiplexor Channel

The Multiplexor Channel contains only the interface signal and response circuits and certain sequence recognition circuits. Therefore, as each service request is recognized by the Multiplexor Channel, it takes control of the CLU registers, data paths, and read-only storage. When it has completed its response, it frees the CLU for other operations.

An area of Local Storage is set aside for the Multiplexor
Channel use.  MACH storage contains the status and control informa-
tion for subchannels of the Multiplexor Channel.  Four words of MACH
storage are assigned to each Multiplexor Subchannel.

Selector Channel

The Selector Channel operates in the burst mode, one transmission
operation at a time.  Other I/O devices attached to the channel
can, in the meantime, be performing functions that do not involve
communication with the channel.  When not executing an operation,
the Selector Channel is in a reset state waiting for a request
signal from one of the attached I/O devices or a selection signal
from the common channel.

The Selector Channels do not require the use of the CLU for each
byte.  Instead, they buffer several bytes in registers before tak-
ing microprogram control of the CLU data paths.  When operating
with their own buffer registers, they employ conventional sequen-
tial logic control contained within the channel.

Channel-to-Channel Adapter

The functional characteristics of the Channel-to-Channel Adapter
are described in IBM 9020D and 9020E System Principles of Operation
manual.

Interfaces

The IOCE interfaces with the CE, SE, PAM, TCU, SCU, DAU and System
Console or Configuration Console and IOCE's of another 9020 System
via Channel-to-Channel Adapter via the "Input/Output Interface,
Channel to Device Control Unit".  A detailed description of this
interface is contained in Chapter 13.

Communication between IOCE and CE is accomplished via cabling
between the units.  This cabling constitutes the logical boundary
(interface) between the IOCE and CE of the IBM 9020D or 9020E
System.

One CE may control several IOCE's on-line at one time.  The
communication between a CE and the IOCE's would be in an interleaved
manner allowing an operation between one CE and only one IOCE at
a given instant.  An IOCE may be under control of only one CE at
a time and must be configured that way.

In general, I/O instructions, IOCE-Processor control signals,
interruptions, masks, addresses, condition codes and various
other inter-element control functions are transmitted across
the IOCE/CE interface.  It should be noted that only control
information is transferred between these elements.

In addition, the IOCE will accept signals over the interface to perform the special functions:

| | |
|---|---|
| IPL (Initial Program Load) | SATR Select |
| Logout | FLT Backspace |
| Permit I/O Interruption | 360 Mode |
| FLT Load | Write Direct Start |
| Permit MC Interruption | Write Direct Stop |
| Reconfigure Select | Write Direct External Interrupt |

Similarly, communication between IOCE and SE is via the IOCE/SE interface cabling.  The information passing over this interface is primarily data, protection keys, and addresses.

The communication between the IOCE, and the PAM, and DAU, another IOCE via Channel-to-Channel Adapter, System Console, or Configuration Console, and TCU is over the I/O interface.  This interface is described in the Input/Output interface, Channel to Device Control Unit (Appendix D).

Additional communication between IOCE and System Console or Configuration Console is via the IOCE/System Console or Configuration Console interface cabling.  The information passing over this interface is primarily IOCE status information.

DESIGN DETAILS

Internal Design Details

Data Flow Registers (See Figure 5-3)

Adder - The left input to the adder can be from the L register through a true-complement gate.  The L register contents may be gated directly into the adder or the low-order sixteen (16) bits may be cross-gated to the sixteen (16) high-order positions of the adder with zeros filling the adder low-order positions.  The right input to the adder can be from the R-register, the M-register, or the H-register.  In addition to 32-bit transfers, the M-register low-order sixteen (16) bits can be gated to the adder; the high-order adder sixteen (16) bits would be filled with zeros.

Shifter - This is a 32-bit shift register capable of a zero shift or of a shift either right or left by one or four bits.  Shifter input is from the adder.

F-Register - This is a four-bit register used to hold the spilled bit(s) after a shift.  The F-register bit(s) may be entered into the bit position(s) vacated by a shift operation, thus enabling any two 32-bit registers to be coupled for shifting.

5-11

L-Register - This is a 32-bit register used to buffer data fetched from local storage. The data may also be regenerated into local storage.

R-Register - This is a 32-bit register with functions identical to the L-register.

J-Register - This is a four-bit register used for addressing the local storage.

MD Register - This is a four-bit register used for addressing the local storage.

Local Storage (LS) - This is a 0.5 usec core storage unit with a 64-word capacity. LS contains Selector Channel control words, temporary storage for Multiplexor Channel control words, and general purpose register for pre-processor operations. A map of local storage is shown in Figure 5-4.

Local Storage Address Register (LSAR) - This is a six-bit register used to hold the address of the selected local storage location. The two high-order bits may be obtained from the LSFR. The four low-order bits may come from the J Register or the MD Register, or they may be forced to a specific value by the ROS emit field.

Local Storage Function Register (LSFR) - This is a two-bit register which is used to specify the sector in LS which is being addressed. For example, it will distinguish between I/O channel and working storage areas.

Q-Register - This is one-bit register. Its function is identical to that of the F Register for one-bit shifts.

I/O Register - This is a two-bit register. It is used in Selector Channel operations for data byte boundary identification.

Instruction Address Register (IAR) - This 24-bit register receives input from the adder latches, and provides output to either the H Register or the SAR.

Mover and Mover Latches - This is an eight-bit path used for exe-cution of Multiplexor Channel operations, VFL instructions, and logical instruction execution.

M-Register and H-Register - These are each 32-bit general purpose registers.

Storage Address Register (SAR) - This is a 24-bit register that contains the address of the storage location to be referenced.

Storage Data Register (SDR) - This is a 32-bit register plus parity that contains the contents of a referenced storage location.
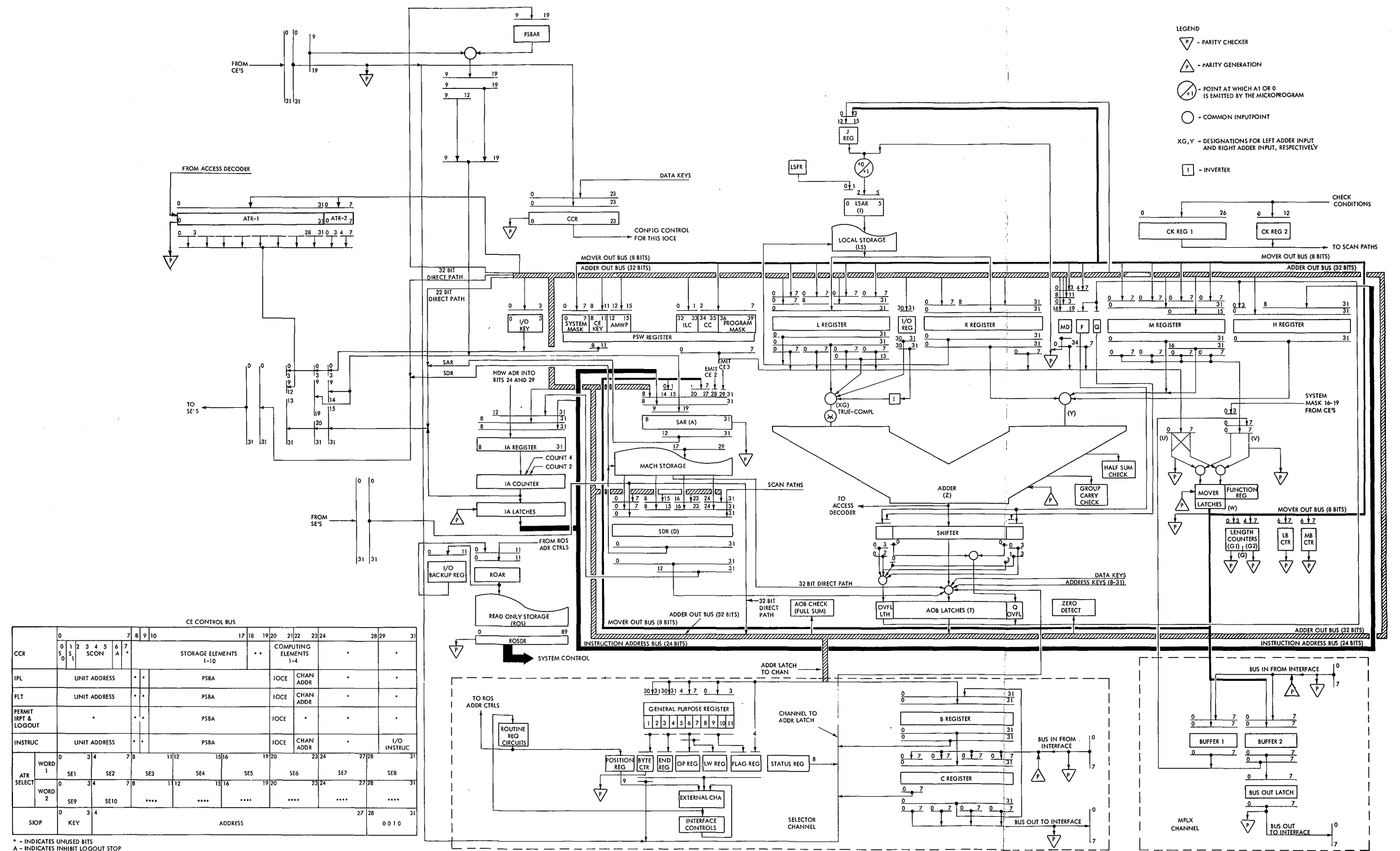
•Figure 5-3.   IOCE Data Flow Registers

| | LOCAL STORE | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SECTOR 22-23 | REGISTER 24-27 | | | | | | | | | | | | | | | |
| | SEL CHAN 1 | | | | SEL CHAN 2 | | | | SEL CHAN 3 | | | | MPX CHAN 0 | | | |
| 00 CHAN | CA 0 | DA 1 | UA CT 2 | DT 3 | CA 4 | DA 5 | UA CT 6 | DT 7 | CA 8 | DA 9 | UA CT 10 | DT 11 | CA 12 | DA 13 | CT 14 | UA 15 |
| 01 WORKING STORAGE | | | | | | | | PSW 0-15 7 | | | | | | | I BF 14 | |
| 10 BFR | SPCI INT | | | | | | | | | | | | CHAN BFR | | MPX | |
| | | 1 | | | | | | | 8 | 9 | 10 | 11 | R BU 12 | L BU 13 | INT 14 | BU 15 |
| 11 GEN REGS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |

LEGEND:
DA – DATA ADDRESS
UA – UNIT ADDRESS
CA – COMMAND ADDRESS
CT – COUNT
DT – DATA
BU – BACKUP
BFR
BF } BUFFER

Figure 5-4. Map of Local Storage, IOCE

LB Register and MB Register - These are each two-bit byte counter registers.

G1 Register and G2 Register - These are each four-bit length count registers.

IA Counter and Latches - These are used to increment the IAR.

Function Register - This is a four-bit register used in conjunction with the mover to define the logical connectors to be performed by the mover.

Read Only Storage (ROS) - ROS is a capacitor storage unit which operates on a 0.5 usec cycle and which controls IOCE data flow.

Read-Only Address Register (ROAR) - This register contains the ROS (read only storage) address of the next micro-instruction to be obtained from ROS.

I/O Backup Register - This register contains the ROS address of the next CLU routine when an I/O routine is concurrently using the ROAR.

Read-Only Storage Data Register (ROSDR) - This register contains the micro-instruction just obtained from ROS.

I/O Key - A four-bit register which is set from the Adder Out
Bus. Its contents form the I/O key which is used in place of
the CE key in the PSW for I/O operations.

Configuration Control Register (CCR) - This is a register in the
CLU that is loaded by a SCON instruction issued by a CE via the
IOCE/CE interface. The contents of this register define:

1. The state that the element is in, which in turn determines
   which manual controls are enabled on the IOCE Control
   Panel.

2. The CE with which it operates for all functions other
   than the SCON instruction.

3. Those CE's from which the IOCE will accept a reconfig-
   uration instruction (SCON).

4. The SE's with which the IOCE can communicate

5. Whether an IOCE will issue a Logout Stop signal to an
   SE in response to a storage check (Inhibit Logout Stop).

The CCR is laid out as follows:

| State | SCON | | | SE | | CE |
|---|---|---|---|---|---|---|
| SO SI | 1  2  3  4 | A | * | 1  2  3  4  5  6  7  8  9  10  *  * | | 1  2  3  4 |

Bit Pos    0  1  2       5  6  7  8                       19  20     23

A - Inhibit Logout Stop

* Not Used

Address Translation Register (ATR) - The ATR is comprised of 2
Registers; a 32-bit (plus parity) register (ATR-1) and an 8-bit
(plus parity) register (ATR-2). They may be logically considered
as one 40-bit register. The ATR in the IOCE is set when the SATR
instruction is issued by the CE to which it is configured. The
ATR provides dynamic address translation of logical address
blocks into selectable physical address blocks. Any 131K word
block of SE assigned logical addresses (on 131K multiple boundaries)
may be physically located in any configured SE. Address trans-
lation in the IOCE takes place only for non-PSA storage refer-
ences. PSA references in the IOCE are accomplished through the
IOCE PSBAR, which is set from a CE and contains the physical
(already translated) storage element addresses. The ATR is
parity checked and logged out as shown in Figure 5-5. Details
concerning the Address Translation operation are presented in
Chapter 2 of this manual and in the IBM 9020D and 9020E System
Principles of Operation Manual.

Figure 5-5. IOCE Logout Format (Sheet 1 of 3) — bit positions in main storage.

**BIT POSITIONS IN MAIN STORAGE**

| PSA LOCA-TION | PSA WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 324 | 81 | P 8-15 | | | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | | 0 | 1 | 2 | 3 | |
| 328 | 82 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | | 0 | 1 | 2 | 3 | |
| 332 | 83 | P 0-30 / 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | | ROSDR BITS 0-30 |
| 336 | 84 | P 31-55 / 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 1 | 2 | 3 | 1 | 2 | 3 | | ROSDR BITS 31-55 |
| 340 | 85 | P 56-89 / 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 | 84 | 85 | 86 | 87 | ROSDR BITS 56-87 |
| 344 | 86 | P | 0 | 1 | 2 | 3 | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | ROSDR 88 | ROSDR 89 | | | | | | | | | ROSDR BITS 88-89 |
| 348 | 87 | P | 0 | 1 | 2 | 3 | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | FLT END STAT CHECK | CE EXT INTRP REQ | ONE SYL OP STAT | RE-FETCH STAT | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | CURRENT ROS ADR AND PSW GROUP |
| 352 | 88 | SE 1 | SE 2 | SE 3 | SE 4 | SE 5 | SE 6 | SE 7 | SE 8 | SE 9 | SE 10 | SE 11 | SE 12 | S 7 | A 13 | M 14 | W 14 | P 15 | PROC MODE | P 8-15 | | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-19 | 16 | 17 | 18 | 19 | SE ACC REQ PSBAR |
| 356 | 89 | HALF SUM 0-7 | HALF SUM 8-15 | HALF SUM 16-23 | HALF SUM 24-31 | FULL SUM 0-7 | FULL SUM 8-15 | FULL SUM 16-23 | FULL SUM 24-31 | GROUP CARRY | L BYTE CNTR | M BYTE CNTR | MD CNTR | G1 CNTR ERR | G2 CNTR ERR | MOVER LEFT INPUT | MOVER RIGHT INPUT | MOVER OUTPUT | | SAR P 8-15 | SAR P 16-23 | SAR P 24-31 | ROS P 0-30 | ROS P 31-55 | ROS P 56-89 | | | LOG RQST | | | | | | CHECK REG 1 |
| 360 | 90 | | | | | | | | | | | | | | | | | | | CCR PTY CHK 0 | STOR CHK 1 | SE TIME OUT 2 | SE LOS 3 | FETCH DATA CK 4 | INV ROS ADR 5 | LOG ROS CHK 6 | LOG ADR CHK 7 | CE LOG RQST 8 | CNTRL BUS CHK 9 | ATR PTY CHK 10 | MPX INTFC PTY 11 | PSA LOCK-OUT 12 | 13 | CHECK REG 2 |
| 364 | 91 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | | | | | ATRI 0-23 |
| 368 | 92 | P 24-31 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | | | | | ATRI 24-31 / ATR2 0-15 |
| 372 | 93 | P 0-7 | S0 | S1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | P 16-23 | 9 | 10 | | | 1 | 2 | 3 | 4 | | | | | CCR |
| 376 | 94 | P | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SAME AS WORD 84 |
| 380 | 95 | P | 0 | 1 | 2 | 3 | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 34 | 35 | FLT END STAT CHECK | CE EXT INTR | ONE SYL OP STAT | RE-FETCH STAT | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | SAME AS WORD 87 |

**Field groupings (column headers per word):**

- **Word 81 (324):** STORAGE ADDRESS REGISTER (SAR); BYTE STATS
- **Word 82 (328):** INSTRUCTION ADDRESS REGISTER (IAR); BYTE STORE STATS
- **Word 83 (332):** MOVER LEFT INPUT; MOVER RIGHT INPUT; ROS ADDRESS BITS 0-5; ADR 6-9 OR FUNCTION BRANCH CONTROL; ROS ADDR BRANCH CONTROL; ADDER LATCH OUTPUT AND SCAN BUS GATE; LOGSP; LOCAL STORE ADR CONTROL; LOCAL STORE DATA CONTROL
- **Word 84 (336):** IAR TO SAR CNTROL; GATE TO ADDER LATCH CONTROL; MOVER OUTPUT DESTINATION; BYTE COUNTER FUNCT CNTL; MD CNTL; LB CNTL; MB CNTL; G1, G2 COUNTER CONTROL; MOVER BIT 0-3 CONTROL; MOVER BIT 4-7 CONTROL; MOVER FUNCTION CLU MODE; MOVER FUNCTION I/O MODE
- **Word 85 (340):** EMIT FIELD; LEFT ADDER INPUT; TRUE COMPL; RIGHT ADDER INPUT; ADDER FUNCTION CONTROL; CONDITION TEST CONTROLS FOR A BRANCH; CONDITION TEST CONTROLS FOR B BRANCH; SE STORE; STATUS SETTING FUNCTION FIELD
- **Word 86 (344):** BYTE STORE L STATS; PREVIOUS ROS ADDRESS BUFFER (ROS BASE ADDRESS BITS 0-5; FUNCTION BRANCH 6-9; A, B BRANCH); STATUS SETTING FN (ROSDR 88, ROSDR 89)
- **Word 87 (348):** STORAGE PROTECT KEY; ROS BASE ADDRESS BITS 0-5; FUNCTION BRANCH 6-9; A, B BRANCH; CE COND CODE; FLT END STAT CHECK; CE EXT INTRP REQ; ONE SYL OP STAT; RE-FETCH STAT; INSTR LENGTH PSW; CONDITN REG PSW; PSW BITS; PROGRAM MASK PSW
- **Word 88 (352):** SE ACCESS/REQUEST; PSW; PSBAR
- **Word 89 (356):** CHECK REGISTER
- **Word 90 (360):** CHECK REGISTER 2
- **Word 91 (364):** ADDRESS TRANSLATION REGISTER 1
- **Word 92 (368):** ADDRESS TRANSLATION REGISTER 1 / ADDRESS TRANSLATION REGISTER 2
- **Word 93 (372):** CONFIGURATION CONTROL STORAGE ELEMENTS (STATE BITS; SCON BITS; ILOS); COMPUTING ELEMENTS
- **Word 94 (376):** IAR TO SAR CONTROLS; GATE TO ADDER LATCH CONTROLS; MOVER OUTPUT DESTINATION; BYTE COUNTER FUNCT/CNTL; MD CNTL; LB CNTL; MB CNTL; G1, G2 COUNTER CONTROL; MOVER BIT 0-3 CONTROL; MOVER BIT 4-7 CONTROL; MOVER FUNCTION CLU MODE; MOVER FUNCTION I/O MODE
- **Word 95 (380):** STORAGE PROTECT KEY; CURRENT ROS ADDRESS BUFFER (ROS BASE ADDRESS; FUNCTION BRANCH; A, B); CE COND REG; FLT END STAT CHECK; CE EXT INTR; ONE SYL OP STAT; RE-FETCH STAT; INSTR LNGTH; CONDITN REG; PSW BITS; PROGRAM MASK

●Figure 5-5. IOCE Logout, Format (Sheet 1 of 3)

Figure table — IOCE Logout Format (Sheet 2 of 3)

BIT POSITIONS IN MAIN STORAGE

| PSA LOCA-TION | PSA WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 384 | 96 | I/O MODE | I-O REGISTER PTY | 30 | 31 | TIMER | INTR PB | L BYTE COUNTER P | 0 | 1 | M BYTE COUNTER P | 0 | 1 | F REGISTER P | 0 | 1 | 2 | 3 | Q REG | | WAIT LOOP | GENERAL PURPOSE STATS 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | L SIGN STAT | R SIGN STAT | CARRY STAT | NO RETRY LATCH | STATUS GROUP |
| 388 | 97 | | LOCAL STORE ADR REG 0 | 1 | 2 | 3 | 4 | 5 | LS FN REG 0 | 1 | J REGISTER P | 0 | 1 | 2 | 3 | MD COUNTER P | 0 | 1 | 2 | 3 | | G1 COUNTER SIGN | P | 0 | 1 | 2 | 3 | G2 COUNTER SIGN | P | 0 | 1 | 2 | 3 | LSAR GROUP |
| 392 | 98 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | H REG |
| 396 | 99 | | | | | | | | | | | | | | | | | | | | | | | | | 28 | 29 | 30 | 31 | | | | | H REG |
| 400 | 100 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | M REG |
| 404 | 101 | | | | | | | | | | | | | | | | | | | | | | | | | 28 | 29 | 30 | 31 | | | | | M REG |
| 408 | 102 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | R REG |
| 412 | 103 | | | | | | | | | | | | | | | | | | | | | | | | | 28 | 29 | 30 | 31 | | | | | R REG |
| 416 | 104 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | L REG |
| 420 | 105 | | | | | | | | | | | | | | | | | | | | | | | | | 28 | 29 | 30 | 31 | | | | | L REG |
| 424 | 106 | P 0-7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P 8-15 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | P 16-23 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | P 24-31 | 24 | 25 | 26 | 27 | SDR |
| 428 | 107 | | | | | | | | | | | | | | | | | | | | | | | | | 28 | 29 | 30 | 31 | | | | | SDR |
| 432 | 108 | START I/O | I/O INSTRUCTION TEST I/O | HALT I/O | TEST CHANL | SET PC1 | CHANNEL SELECT TGRS 2 | 1 | REPLY REGISTER 0 | 1 | 2 | 3 | REPLY READY | I/O INTR RQST | PERMT I/O INTR | TIME OUT | TIME OUT CHECK | FAULT ON START I/O | | | | | SPCIB FULL | RTNE RQST BFP POS X | | | | | | | | | | COMMON CHANNEL |
| 436 | 109 | RTNE RCVD | PCI ENABL | BREAK IN | I/O RTNE MODE | EARLY FIRST CYCLE | FIRST CYCLE FIRST CYCLE | FIRST CYCLE CHAIN | LOCAL STORE ACCESS READ | WRITE | CHAL DTC | ALCH DTC | CHAIN REG | LAST CYCLE | BREAK OUT | MEMORY BYTE CONTROL REGISTER 0 | 1 | 2 | 3 | | | TIMING SIGNALS ROS33 | ROS34 | CONTROL SIGNALS ROS46 | ROS47 | FIRST CYCLE CHECK | | | | | | | | COMMON CHANNEL |
| 440 | 110 | CHANNEL BUFFER 1 CHAN 0 | CHAN 1 | CHAN 2 | CHAN 3 | CHANNEL BUFFER 2 CHAN 0 | CHAN 1 | CHAN 2 | CHAN 3 | CHANNEL BUFFER 3 CHAN 0 | CHAN 1 | CHAN 2 | CHAN 3 | I/O STATS 0 | 1 | 2 | 3 | 4 | I/O CHECK MODE | CHANNEL LOG RQSTS CHAN1 | CHAN2 | CHAN3 | GATE STATUS | LOG RESET CHANL | | | | | | | | | | COMMON CHANNEL |

Figure 5-5.  IOCE Logout, Format (Sheet 2 of 3)

Figure 5-5. IOCE Logout, Format (Sheet 3 of 3)

BIT POSITIONS IN MAIN STORAGE

| PSA LOCA-TION | PSA WORD NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DATA BUFFER 1 | | | | | | | | | DATA BUFFER 2 | | | | | | | | | | | | | START LOG-OUT | | | | | | | | | | |
| 444 | 111 | P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | START LOG-OUT | | | | | | | | | MPX CHAN-NEL |
| | | MULTIPLEX CHANNEL INTERFACE TAGS | | | | | | | | | | | | MPX BUS OUT | | | | | | | | | | CHECKS | | | | | | | | | | |
| 448 | 112 | SELCT OUT | SELCT IN | OP IN | SUPR OUT | RQST IN | SVC OUT | ADR OUT | CMD OUT | SVC IN | ADR IN | STAT IN | | | P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | PRGM | PROTCT | | | | | | | | | MPX CHAN-NEL |
| | | CONTROLLED EMIT | | | | ROUTINE REQUEST REG | | | | | PRIORITY REG | | CONTROL TRIGGERS | | | | | | | MPX I/O STATS | | | | | | | | | | | | | | |
| 452 | 113 | 0 | 1 | 2 | 3 | A | E1 | E2 | E3 | E4 | PRIOR 2 | PRIOR 3 | PCI RQST | CMND CHAIN | DTCI | UCW STORE | INTR BFR FULL | POLL CTRL | BURST MODE | STAT REG 0 | STAT REG 1 | STAT REG 2 | STAT REG 3 | DATA XFR CTL | COMCH RST CTL | | | | | | | | | MPX CHAN-NEL |
| | | B REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 456 | 114 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | SELECT CHAN-NEL |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B REGISTER PARITY | | | | |
| 460 | 115 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | P 0-7 | P 8-15 | P 16-23 | P 24-31 | SELECT CHAN-NEL |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | C REGISTER PARITY | | | | |
| 464 | 116 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | P 0-7 | P 8-15 | P 16-23 | P 24-31 | SELECT CHAN-NEL |
| | | C REGISTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 468 | 117 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | SELECT CHAN-NEL |
| | | BYTE COUNTERS | | | | | LAST WORD AND EOR CONTROL | | | | | | | DATA BUFFER CONTROL | | | | | READ INSTRUCTIONS | | | WRITE INSTRUCTIONS | | | | | | | CHANNEL CHECKS | | | | |
| 472 | 118 | BYTE CTR A-2 | BYTE CTR A-1 | BYTE CTR B-P | BYTE CTR B-2 | BYTE CTR B-1 | END REG 2 | END REG 1 | LAST 3 WORDS | LAST WORD | EOR CNT INTLK | EOR 1 | EOR 2 | READ INTLK | B REG ALMST CHGD | LS ENABLE | LS FULL | C REG FULL | READ BKWD | READ TYPE OP | READ READY | IF READ | WRITE TYPE OP | WRITE READY | IF WRITE | SIM CHECK | IL 1 | PGM CHECK | STO PROT CHECK | CHAN DTA CHECK | CHAN CTL CHECK | IF CTL CHECK | CHAIN CHECK | SELECT CHAN-NEL |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SELECTR CHAN GRP 3 | | | | |
| 476 | 119 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | BYTE CTR A PTY | LAST 2 WDS | B REG FULL | CD-PC CK | SELECT CHAN-NEL |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SELECTR CHAN GRP 4 | | | | |
| 480 | 120 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | UA FETCH | CC STEP O PHA | PRI 1 REQ | REQ REG STO | SELECT CHAN-NEL |
| | | ROUTINE TYPE REGISTER | | | | | | | | CYCLE COUNTER | | | A CLOCK | | | PRIORITY RQST LATCHES | | | | ROUTINE REQUEST ADDRESS CONTROLS | | | | | | | | | PRIORITY DETECT LATCHES | | | | |
| 484 | 121 | CCW1 TYPE | CCW2 TYPE | UNIT SEL | READ STORE | WRITE FETCH | END UPDTE | ADR COMP | INTR RTNE | CYCTR PH A STEP 1 | CYCTR PH A STEP 2 | CYCTR PH A STEP 3 | CLOCK A0 | CLOCK A1 | CLOCK STEP CTL | LS RQST | PC1 RQST | REQ REG PRI 2 | REQ REG PRI 3 | REQ REG 0 | REQ REG 1 | REQ REG 2 | REQ REG 3 | REQ REG 4 | REQ REG 5 | REQ REG STAT 1 | REQ REG STAT 2 | REQ REG STAT 3 | LS RQST DETCT | CHAN PRI 1 DETCT | CHAN PRI 2 OR 3 | PCI DETCT | DETCT INHB RTNE | SELECT CHAN-NEL |
| | | GENERAL PURPOSE REGISTER | | | | | | | | FLAGS | | | | | | RECORD TRANSFER CTRLS | | | | | | | | STATS NEXT | MULTIPURPOSE LATCHES | | | | INTERFACE CONTROLS | | | | |
| 488 | 122 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | FLT READ | CHAIN DTA | CHAIN CMD | SILI | SKIP | PCI | FIN LATCH | FIRST WD | FIRST BYTE | TOTAL REC FETCH | WRITE CHAIN PROCD | IF STOP REL | | | | STATS NEXT | C1 | C2 | C3 | C4 | SUPR OUT COND | GATD RQST IN | SVC OUT HOLD | ENABL STAT IN | SELECT CHAN-NEL |
| | | A CLOCK LATCHES | | | | | SPL PURPOSE LATCHES | | | | | | INTERFACE CONTROLS | | | | | | | | | | | | | | | | INTERFACE TAGS | | | | |
| 492 | 123 | INH READ STORE | A CLOCK A | A CLOCK B | A CLOCK C | A CLOCK D | D1 LATCH | D2 LATCH | INSTR SCAN | POLL | POLL INTR END | INSTR INH | B CLOCK READY | UNADR TOBUS OUT | UNSEL ADDR OUT | COMPR EQUAL | COMPR NOT EQ | CH DTA 1 STBY | CHAIN DATA | BY CT MOD ENABL | WRITE CHAIN RDY | RCD END | OP IN TEST | EXT CHAN STOP | SEL OUT | SEL IN | OP IN | SERV OUT | ADR OUT | CMND OUT | SERV IN | ADR IN | STATS IN | SELECTR CHAN-NEL |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SELECTR CHAN | | | | |
| 496 | 124 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | POSN REG XFR | CHAN IN USE | IF STOP | STOP RTNE | SELECTR CHAN-NEL |
| | | MPLX CHANNEL UNIT ADDRESS | | | | | | | | | MPLX CHANNEL UNIT ADDRESS | | | | | | | | | | | | | | | | | | | | | | |
| 500 | 125 | P | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | P | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | | | | | | | | | | | | | | | SELECTR CHAN-NEL |

PSBAR - The Preferential Storage Base Address Register in the IOCE
is a twelve-bit register.  In normal operation, PSBAR is set when-
ever updated PSBAR data is sent to the IOCE from the CE for I/O
instruction, IPL, FLT Load, and Permit I/O or MC Interrupt.  PSBAR
contents are gated from IOCE to SE during an IOCE PSA access.
PSBAR always specifies the physical storage to be accessed; hence,
is not translated in the ATR.  Two types of PSA accesses are pro-
cessed in the IOCE.  The first includes all PSA operations except
IPL and FLT load and confines the accesses to the PSA in the spec-
ified SE.  High order address bits 9-19 are specified by PSBAR.  Bits
20-31 are passed through the normal AOB to SAR path.  The second
type of PSA access, found in IPL and FLT Load, allows the IOCE to
access any address within the SE specified by PSBAR.  High order
bits 9-12 are specified by PSBAR.  Bits 9-12 are passed through
the normal AOB to SAR path.  PSBAR is parity checked and logged
out as shown in Figure 5-5.

360 Mode Operation

IOCE 1 may be configured in a System/360 compatible simplex sub-
system with any CE.  This is accomplished by the CE (having been
placed in 360 Mode) activating the 360 Mode line to IOCE 1.  When
in 360 Mode, the IOCE peforms the following functions:

1. Bit 6 in the CCR (Inhibit Logout Stop) is set on, thus
   preventing the IOCE from issuing Logout Stop to an SE.

2. Bits 0-3 of the PSW from the CE are used as the mask
   bits for the channels.

3. In the Interruption Code field of the PSW stored by the
   IOCE (i.e., Bytes 2 and 3), Bits 16-19 are forced to
   zero.

4. Resets Processor mode preventing operation of the IOCE-
   Processor.

5. Reverts to 360 addressing making MACH addresses invalid.

360 Mode operation is discussed in the IBM 9020D and 9020E
System Principles of Operation manual.

Control

Microprogram Control

The CLU, the Multiplexor Channel, and some functions of the
Selector Channels of the 7231-02 are controlled by a micro-
program held in the read-only storage.  Microprogram control
is also used for maintenance and some manual-control functions.

     Each word of read-only storage contains a micro-instruction.
The word is divided into fields to control the various functions
of the CLU.  Each field, with the exception of the ROS address

and emit fields, is decoded into a set of control lines. These control lines control the action of the CLU for one cycle. Normally a new micro-instruction is fetched for each cycle of operation.

Micro-instructions are not executed from sequential read-only storage addresses under control of an instruction counter, but rather each micro-instruction may have as many as sixty-four (64) different successors; most do not have more than four successors. The choice of a successor is made on the basis of branching tests specified by the micro-instruction. This branching ability of the micro-program contributes significantly to reducing the number of words of read-only storage required.

Selector Channel Organization

Selector Channel activity is controlled by special circuitry in each channel, as well as by micro-program routines stored in the read-only storage. These routines control the flow of data, flow of control words to and from storage and local storage, and the modifications to control words resulting from channel activity. The micro-program has the ability to perform conditional branches based upon conditions in the Selector Channel. Branching allows a general micro-program routine to be used for several different purposes.

The Selector Channel has three data buffers: A, B, and C. The C Register is a four-byte register used for byte assembly and disassembly. On output operations, the C Register receives data from the B Register and transmits it to the I/O interface. For input operations, this data flow is reversed. These paths are shown in Figure 5-3.

The B Register is connected to the C Register and to the CLU adder latch. In this way, the channel has access to the various registers and local storage in the CLU.

Each Selector Channel has a unique location in Local Storage that it uses as a data buffer. This location is called Register A. For output operations, the data word fetched from storage is placed in Register A. Input data can be placed in Register A prior to storing into storage.

Each Selector Channel uses three other words of local storage to hold parts of the channel control word, the channel address word, and the unit address. One word holds the command address with the protection key; a second word holds the data address and the protection key, the third word contains the address of the device in operation and the count.

A description of the other registers in each Selector Channel follows:

Byte Counter - This two-bit counter controls the selection and gating of Bytes 0-3 between the C Register and the I/O interface.

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End Register - This two-bit register is set with the value that the byte counter should contain after the last byte of data has been transmitted to or from the I/O interface.  (It is set to the value of the count modulo 4 plus 1.)

General Purpose Register - This eleven-bit register receives the initial byte count, the end register count, last word indications, operation code and flags from the CLU facilities.  This information is sent to the proper registers from the General Purpose Register.

Operation Register - This three-bit register reflects the operational state of the channel:  Input (read or sense), Output (write or control), or Input Backward (read backward).

Flag Register - This five-bit register is used to store the five flag conditions from the channel control word.

Request Register - This register contains the priority of the routine currently being requested by the channel.  This priority is used by the common channel to determine which channel shall obtain the next storage cycle.

Position Register - A functional nine-bit register which defines to the external channel controls the logic to be used as a function of the requested micro-program routine.

Channel Status Register - This eight-bit register holds the status conditions detected in the channel that form part of the channel status word.  This information is subsequently gated to the CLU.

Last Word Latches - These three latches are set by the micro-program and indicate the termination of a data transfer; i.e., last word, last two words, and last three words.

Channel Output Operation

During an output operation, data is transmitted from storage to the I/O device using the A, B, and C data buffers.  Within the IOCE, the data is transmitted four bytes, or one full word, at a time.

Registers A, B, and C are set up initially with the first three words, and the data address and count are adjusted accordingly. The data bytes are disassembled in the C Register and transmitted a byte at a time over the I/O interface.  After the transmission of the last byte from the C Register, the word in the B Register is set into C. The channel then requests the micro-program routine which transfers the word in A (local storage) to B.  Since A is now empty, the channel requests the routine which loads A from storage.  This routine also updates the data address and count.

At the end of the operations, the Last Word Latches provide for the correct handling of the last three words.  The End Register is used to cause the transmission to terminate with the correct byte of the last word.

Channel Input Operation

During an input operation, data is transmitted from the I/O device
and is assembled a byte at a time in the C Register under control
of the Byte Counter.  After the word is assembled, it is transferred
to the B Register, freeing the C Register.  The channel then requests
a micro-program routine to transfer the contents of B to local stor-
age Register A or to storage.  If the word was placed in Register A,
it is then transferred to storage from local storage by another micro-
program routine, which also updates the data address and count.

        If the operation is READ BACKWARD, the data flow is the same,
except that the bytes are assembled in reverse order in the C
Register; the data address is decremented rather than incremented
as in a normal read operation.

Note:  Controls are provided within the IOCE to enable the in-
itiation of an I/O operation at a byte address other than word
boundaries, as well as to terminate an operation at a byte address
other than word boundaries.  Fetching data from storage does not
affect the data stored in storage.  In the case of storing the
data during Channel Input operation, there are controls provided
on the interface lines between the storage and the IOCE which
establish the bytes to be written, and,therefore, the bytes to be
regenerated within a given word.  Excess bytes transferred from
storage to the IOCE are discarded by the channel.

Multiplexor Channel Organization

Two 8-bit plus parity registers, Buffer Registers 1 and 2, are pro-
vided for Multiplexor Channel use.  Both registers can be set from
either the Interface Bus In or the Mover Output.  Both registers can
also be gated to the right input of the mover, but only Buffer Regis-
ter 2 can be gated to the Interface Bus Out Latch.  These paths are
shown in Figure 5-3.

        The path of data for an input operation is from Interface Bus
In to Buffer Register 2, to the input of the mover, through the
mover and into the proper byte of the L Register, and then to SDR
and storage. The path for an output operation is from storage to the
L Register, where the proper byte is gated through the mover to
Buffer Register 2, then to the Interface Bus Out.  Each byte of data
transmitted or received requires a storage cycle.

        Signals on the interface lines to the I/O units are usually
initiated under control of the micro-program and terminated in
response to signals from the I/O units.  All interface "in" lines
set latches under control of the clock.  The outputs of these latches
are used by the channel, rather than the input lines themselves,
thus synchronizing all interface operations with the IOCE clock.

        An 8-bit Routine Request Buffer is provided to hold the
ROS address of the next micro-program routine desired.  The output
of this register, together with outputs of a 3-bit Priority Register,
are sent to priority controls in the Common Channel to request

the next routine. The output of the Routine Request Buffer is also used to determine what routine is being executed and to prepare for the next routine. In this case, it is combined with other conditions in the Routine Generator. These other conditions include the interface-in tags, the emit field of the micro-instruction, several status latches, and operation code lines from the Common Channel.

Conditional branching is used extensively in the Multiplexor Channel micro-program.

Nine words in local storage are provided for Multiplexor Channel use. They are shown on the Map of Local Storage, Figure 5-4. Sector 00, Words 12 through 15, contain the unit control word (UCW) for the device (subchannel) currently using the interface. When the device disconnects, the UCW is transferred to the MACH storage locations assigned to that subchannel. Five words in Sector 10 are used as follows. Word 1 is the Set PCI Interruption Buffer used to perform the Set PCI instruction. Words 12 and 13 are set aside as back-up storage for the L and R Registers in the CLU, which enable a Selector Channel or Multiplexor Channel to break into CLU operation. Word 14 is the interruption buffer, used for normal Multiplexor Channel interruptions. Word 15 is a general back-up register used during various Multiplexor ROS routines.

Input/Output Operation

When the Multiplexor Channel is not servicing a device, the channel will respond to a Request In with Select Out to poll the interface. If the IOCE received an I/O instruction from the CE, a signal is sent to the Multiplexor Channel and, if no device needs service, a request for a micro-program routine is made. When this request is honored by the "Common Channel", the Multiplexor Channel assumes control of the CLU.

If burst mode is indicated by the device (Operational In does not drop) and an output operation is to be performed, the first byte of data is fetched immediately and the channel waits for a Service In signal. If an input operation is to be performed, the channel waits for the Service In signal.

If a multiplex mode is indicated (Operational In drops before the data handling routine is requested), the sequence indication in the UCW is set to busy, and the information concerning the operation on this device is stored in the MACH storage. The channel then waits for a request from the interface.

An Address In signal, generated by a device when the Interface is being polled, causes micro-program routines to be executed which fetch the UCW for the subchannel from MACH storage and put it in the local storage. At this time, the channel assumes a single byte transfer and updates the count and data address accordingly in the UCW in MACH storage. If an output operation is indicated, a fetch of the proper byte is performed. The channel then waits for an "in" tag.

If the Status In tag rises, the channel requests a routine to analyze the status to determine the next routine. This could be an interruption preparation routine, a chain address fetch routine, or a return to waiting for a request from the interface.

If the Service In tag rises, the data-handling routine is performed. On an input operation, this routine routes the data from the Interface In Bus to the proper byte of the L register and stores it in storage. On an output operation, this routine puts the byte on the Interface Out Bus and fetches the next byte of data from storage. Counts and data addresses are updated in LS. If the count is exhausted, the unit is signalled to stop. The PCI flag is checked and, if the interruption buffer is empty, a request for a PCI routine is generated. The PCI routine loads the interruption buffer with the unit address and type of interruption.

If the count goes to zero when it is updated in the data-handling routine, a request for a count zero routine is generated. The count zero routine checks the Chain Data Address Flag and, if it is on, requests the chain address for the next CCW. If this flag is off, the channel waits for the next data-handling routine to halt the device.

Interruption Preparation

When an interruption is indicated and the interruption buffer is empty, the channel requests an interruption preparation routine. This routine makes sure that the count and data address are correct in the UCW stored in the MACH area, and loads the unit .ddress and type of interruption in the interruption buffer.

When the Interruption Buffer is loaded for a Device End or Attention type interruption, the status is always queued at the device. When the interruption occurs, the device must then be selected to clear this status.

Checking

Common Logic Unit

The data flow of the 7231-02 is checked in 8-bit bytes. Control information is checked in bytes of varying length; parity checks are made in various locations on the data flow.

The adder is parity checked and provides three levels of failure detection:

1. Half-sum check,

2. Carry check, and

3. Full-sum check (adder latch check).

Half-Sum Check - A half-sum check indicates either incorrect parity on data entering the adder or a failure in the adder half-sum generation circuits.

Group Carry Check - A look ahead technique generates its own parity which is then compared with the actual parity generated by the adder.  Comparison is made for each group of four bits (digit).

Full-Sum Check - Full-sum checking, which is performed on the adder latch, checks that correct parity has been generated for the developed sum, or that data entering the adder latch from the external source (i.e., storage data, data keys, address keys, IOCE-CE Control Bus) has correct parity.

Checks Registers - Two Check Registers are provided to store indicators from IOCE checking circuits.

Fault-detection circuits set a unique bit in the CLU Check Registers.  Table 5-1 shows the bit assignment for each position of the Check Registers.  Both Check Registers are displayed on the IOCE Control Panel and are included in the logout information.

Table 5-1.  IOCE Check Registers

| Check Indicated | Bit Set In Check Register 1 |
|---|---|
| Half Sum 0-7 | 0 |
| Half Sum 8-15 | 1 |
| Half Sum 16-23 | 2 |
| Half Sum 24-31 | 3 |
| Full Sum 0-7 | 4 |
| Full Sum 8-15 | 5 |
| Full Sum 16-23 | 6 |
| Full Sum 24-31 | 7 |
| Group Carry | 8 |
| LB Counter | 9 |
| MB Counter | 10 |
| MD Counter | 11 |
| Length Counter G1 | 12 |

Table 5-1. IOCE Check Registers (Cont.)

| Check Indicated | Bit Set In Check Register 2 |
|---|---|
| Length Counter G2 | 13 |
| Mover Left Input | 14 |
| Mover Right Input | 15 |
| Mover Output | 16 |
| Storage Address Register 8-15 | 18 |
| Storage Address Register 16-23 | 19 |
| Storage Address Register 24-31 | 20 |
| ROS 1-30 | 21 |
| ROS 32-55 | 22 |
| ROS 57-89 | 23 |
| Log Request | 26 |
| CCR Parity | 0 |
| Storage Check | 1 |
| Storage Timeout | 2 |
| SE LOS | 3 |
| Fetch Data Check | 4 |
| Invalid ROS Address | 5 |
| Log ROS Check | 6 |
| Log ADR Check | 7 |
| CE Log Request | 8 |
| Control Bus Check | 9 |
| ATR Parity | 10 |
| Multiplexor Interface Parity | 11 |
| PSA Lockout | 12 |

Selector Channels

The following Check Conditions are detected in the Selector Channels:

| Control Checks | Interface Checks |
|---|---|
| Byte Counter Parity | Multiple Tags |
| Address Out Parity | Address In Parity |
| Routine Response Check | Address Compare |
| | Status Parity |
| | Timeout Check |

The conditions listed under control checks are all 'OR'd' together into Bit 45 of the channel status word to indicate a channel control check. The conditions listed under interface checks are all 'OR'd' into Bit 46 of the channel status word which is defined as an interface control check.

Data entering or leaving at the interface are parity checked, as is all data transferred between the channel and CLU. This latter checking is provided by the adder latch check.

If such a check (adder latch) occurs, an MC Interruption request is issued to the CE; when generated, a logout is performed and a selective reset will be issued on the interface of the suspect channel after completion of the logout.

Multiplexor Channel

When the CE is attempting to initiate an operation with the Multiplexor Channel and the CLU is not being used to service other channel operations, a count loop is executed in the CLU. At the end of the countdown, a Timeout signal is sent to the channel, followed by a Timeout Check signal. If the channel is handling bytes of data and does not start polling the interface before the Timeout signals occur, the channel is in burst mode, and this condition is so indicated to the CE via a condition code setting. If the channel starts performing the operation and does not release the CLU before the timeout, a channel control check is indicated and a logout occurs. For Multiplexor Channels, interface and channel control checks are grouped together as channel control checks.

Program checks are made using CLU facilities and any check conditions are indicated in the resulting CSW. CSW function is described in the IBM 9020D and 9020E System Principles of Operation.

Parity checks are performed using the CLU facilities, and a check on the interface for invalid sequences is performed in the channel. Parity checks are also performed in the channel on both the in and out bus to the interface. If a check condition is detected, the IOCE stops and an element check signal is generated.

Check Stop

A stop-on-check feature is implemented in the 7231-02.  This
causes the CLU to stop upon hardware detection of a failure.
The stop occurs at the end of the cycle in which the condition
is detected and effectively freezes CLU status.  A bit is set
in Check Register 1 and 2 which defines the cause of the
check-stop.  The IOCE then issues an ELC signal to all CE's
and a machine check interruption request to the configured CE.
The logout of the IOCE is deferred until the CE issues a Permit
MC interruption.  If the MC interruption should occur during the
execution of an I/O or processor instruction, the instruction is
terminated.  Following the Permit MC interruption and the actual
logout, the IOCE will reset process mode if on, will store its
old PSW in MACH, and will issue a response to the CE, which in
turn causes a machine check interruption with the "old" machine
check PSW set to identify the malfunctioning IOCE.  In test state,
manual controls may modify the internal operation upon the occur-
rence of a malfunction, but the ELC signal is always issued upon
the occurence of a malfunction.  For independent Selector Chan-
nel data checks, no logout will occur, only an I/O interruption
request at the end of the operation.  On "read" operations, parity
is corrected and the data stored.  The check conditions during the
operation will be indicated in the CSW when the interruption is
allowed.  The CLU, Multiplexor Channel Status, and Selector Chan-
nel information is available for logout purposes, allowing machine
status at the time of the condition to be stored in storage.
Switch control (when enabled) provides the ability to stop, bypass,
or logout and interrupt upon the detection of a CLU or channel
error.

Maintenance Techniques

Fault detection and location in the 7231-02 are provided by special
hardware features and associated diagnostic programs.  This section
describes fault-locating tests, error logout, and the instructions
which can be executed in diagnostic mode.

Diagnostic Mode Instruction Execution.  A subset of the 9020 instruc-
tion set is implemented in the IOCE to enable the IOCE to execute
some of the diagnostic and maintenance techniques without the need
of a CE.  (This mode is entered by an IOCE whenever all the CE data
bits within its own CCR are set to zero, and the IOCE is in States
1 or 0.)

Fault-Locating Tests.  The fault-locating test (FLT) technique
involves the use of pattern test diagnostic programs for the
CLU and channels.

     The 7231-02 may be required to initiate FLT testing under its
own control.  The FLT program is read into its MACH storage and
the program is used to apply the FLT techniques to the 7231-02.

Since an IPL sequence involves CLU common channel hardware and is under ROS control, an alternate method of loading FLT's into MACH storage is required. For this purpose, additional hardcore controls and an alternate data path directly into MACH storage are provided (FLT Load). If this FLT Load hardcore logic fails, manual intervention and diagnosis is required.

Scan In, Logout. Scan paths are provided for both CLU registers, counters and triggers, and common, Multiplexor, and Selector Channel control triggers and registers.

Progressive Scan

Progressive scan allows FLT's to sequence the channels through its normal operation under IOCE diagnostic program control, comparing channel states with expected states held in MACH storage. This is accomplished by providing a path from the I/O interface and its controls back to the IOCE, thereby allowing the CLU to control both ends of the channel. In this way, FLT's can be run to test and logout at predetermined points of an asynchronous operation, under control of a maintenance program.

Error Logout. CLU status and channel status are available for error logout upon request of a CE. It requests a logout from the CE via a special machine check interruption. Enabling this interruption will cause the IOCE logout to proceed. Error logout occurs directly upon detection of an error if the I/O Instruction line from the CE is active at the time this occurs. Details may be found in Appendix E. A CE may still logout an IOCE by using the appropriate Write-Direct Instruction, but this is not critical to the handling of IOCE errors. When in Diagnostic Mode, the logout occurs upon detection of an IOCE malfunction under control of the Check Control Switch and PSW Bit 13. MC interruption occurs at the end of the logout.

Proper parity is generated for each word logged out. To allow logging of register parity positions, each register requires two positions of main storage. For example, to log all 36 bits of the R Register, the 4 parity bits plus Data Bits 0-27 are stored in one word, and Data Bits 28-31 are stored in a second word. There are two types of error logouts that can occur due to malfunctions. The first type logs the CLU, the Common Channel, the Multiplexor Channel, and one Selector Channel if one requires logging. If no Selector Channel was concerned with the malfunction, all zeros are loaded into the log area for the Selector Channel. Figure 5-5 lists the status from this type logout. A logout to the PSA of an SE begins at Word 81.

The second type of logout occurs for Selector Channel malfunctions which do not affect the remainder of the system. In this case, only the Selector Channel portion of the log area is stored, starting at Word 114.

IOCE CONTROL PANEL

The IOCE Control Panel contains the switches and indicators
necessary for maintenance. It is in an integral part of the IOCE
and is attached directly to the end of the CLU frame. It normal
position will be flat against the frame, but for maintenance
purposes it may be swung out 180 degrees. Figure 5-6 is an over-
all view of the 7231-02 Control Panel. Detailed data concerning
the local storage map is located in the lower left corner of the
IOCE Control Panel (Figure 5-6).

Table 5-2 lists the controls and indicators on the IOCE Control
Panel. Table 5-3 summarizes the conditions under which the IOCE
switches may be used.

Table 5-2.  IOCE Controls and Indicators

| Name | Implementation |
|---|---|
| Manual | Indicator |
| System | Indicator |
| Wait | Indicator |
| Element MPO | Pull Switch |
| Interrupt | Pushbutton Switch |
| Load | Pushbutton Switch |
| Load | Indicator |
| Load Unit | Rotary Switches (3) |
| Power On-Off | Toggle Switch |
| Power Sequence Complete | Indicator |
| State Three | Indicator |
| State Two | Indicator |
| State One | Indicator |
| State Zero | Indicator |
| Test | Indicator |
| Main Line On | Indicator |
| Battery | Indicator |
| Address | Lever Switches (24) |
| Data | Lever Switches (32) |
| Reverse Data Parity | Lever Switch |
| Display | Pushbutton |
| Address Compare | Lever Switch |
|    (Storage Address) | |
| Rate | Rotary Switch |
| Set IC | Pushbutton Switch |
| Start | Pushbutton Switch |
| Stop | Pushbutton Switch |
| Storage Select | Rotary Switch |
| Store | Pushbutton Switch |
| Reset | Pushbutton Switch |
| PSW Restart | Pushbutton Switch |
| Register Set | Pushbutton Switch |
| Set ATR | Lever Switch |
| Set PSBAR/CCR | Lever Switch |
| IAR | Indicators (27) |

Table 5-2.   IOCE Controls and Indicators

| Name | Implementation |
|---|---|
| Master Check | Indicator |
| MC Points | Indicators (36) |
| SDR | Indicators (36) |
| Status | Indicators (144) |
| Check Control | Rotary Switch |
| Check Reset | Pushbutton Switch |
| FLT Control | Rotary Switch |
| FLT Mode | Lever Switch |
| FLT Force Condition | Lever Switch (Spring Loaded) |
| Repeat Instruction (IAR) | Lever Switch |
| Disable Interval Timer | Lever Switch |
| Logout | Pushbutton Switch |
| Address Compare (ROS) | Lever Switch |
| Repeat Instruction (ROS) | Lever Switch |
| Test | Lever Switch |
| Selector Channel Display | Rotary Switch |
| Invert SAR Bit 17 | Lever Switch |
| Stop on Check | Lever Switch |
| Storage Test | Rotary Switch |
| Write | Lever Switch |
| Bump Test | Lever Switch |
| Frame Thermal | Indicators (3) |
| Lamp Test | Lever Switch (Spring Loaded) |
| Marginal Voltage | Indicators (8) |
| Marg. Volt. Ctl. | Potentiometers (8) |
| Marg. Volt. Sel. | Rotary Switch |
| Open CB | Indicator |
| Power Check | Indicator |
| OTC Test | Pushbutton Switch (In Power Section) |
| OBS Test | Pushbutton Switch (In Power Section) |
| On-Line/Off-Line | Toggle Switch |
| Disabled | Indicator |
| On-Line/Off-Line | Toggle Switch |
| Disabled | Indicator |
| Monitor Voltage | Voltmeter |
| Mon. Volt. Sel | Rotary Switch |

Manual - This indicator is on when the IOCE is in the stopped state.

System - This indicator is on when the IOCE is operating.

Wait - This indicator is on when the IOCE is in the wait state.

Element MPO - Pulling this switch turns off all power beyond the entry terminal.  The switch latches in this position and can be restored to its "In" position only by maintenance personnel.

Interrupt - This switch causes an external interruption request to the IOCE. The interruption is taken when not masked off and when the CLU is not stopped. Otherwise, the interruption request remains pending. Bit 25 of the PSW is set to one when the interruption occurs to indicate that the interrupt switch is the source of the external interruption.

Load - This switch causes an element reset, places the IOCE in diagnostic mode (the CE communication bits in the IOCE's CCR are set to zeros) and starts the element IPL procedure.

Load Indicator - This indicates an initial program loading sequence is being performed.

Load Unit - These switches (3) provide an 11-bit number to select the channel and I/O device to be used for IPL. The left switch has 4 positions labeled 0 to 3 and selects the channel. The other two switches have 16 positions each, labeled with the standard hexadecimal characters 0-9 and A-F, and select the device.

Power On/Off - This switch initiates the power-on sequence for the IOCE. At the completion of the power-on sequence, an IOCE reset occurs. The switch is active only when the Element MPO is in its "in" position, the IOCE is in state zero and the test switch is in the "on" position.

Power Sequence Complete - This indicator is on when the power sequence to the IOCE is complete.

State Three - The IOCE state bits in the CCR are set to 1,1. (The IOCE control panel is disabled.)

State Two - The state bits in the CCR are set to 1,0. (The control panel is disabled.)

State One - The element may be performing maintenance operations. The IOCE state bits in the CCR are set to 0, 1 and limited manual controls are enabled if in Diagnostic Mode to perform preventive maintenance.

State Zero - This indicator is on when IOCE state bits in the CCR are set to 0, 0. The test switch is enabled. The IOCE control panel is operative. The test switch being turned on allows power on-off operation and manual manipulation of the configuration register contents.

Test - This indicator is on when a manual control is not in its normal position.

Main Line On - This indicator is on when main line power is on.

Battery - This indicator is on when the element is on battery power.

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Figure 5-6. IOCE Control Panel

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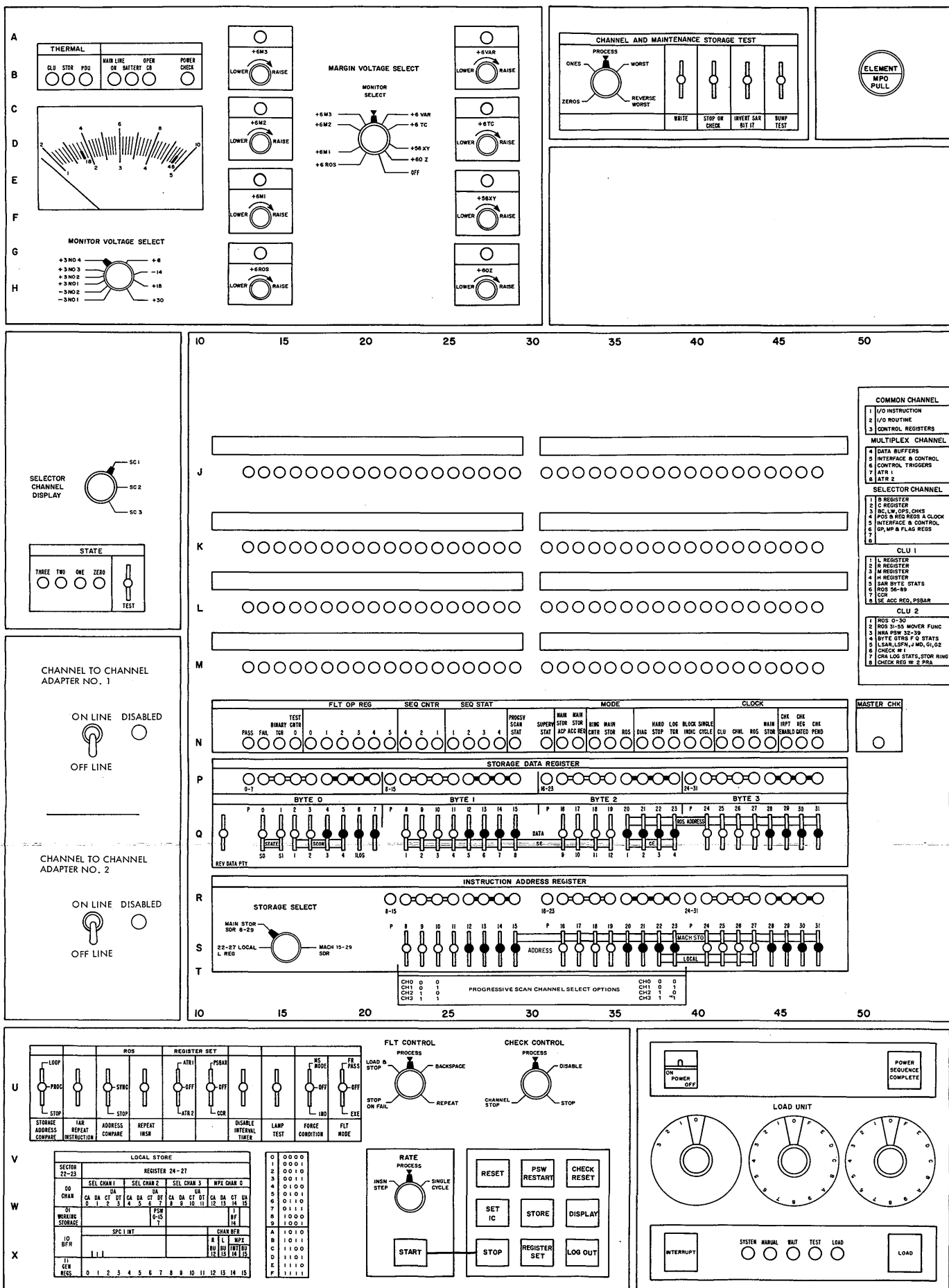
Address - These keys address a location in storage. The keys, in conjunction with the Storage Select Switch, permit access to any addressable location. Correct address parity is generated. The keys can be changed without disrupting IOCE operation. The Address Keys are also used to simulate various conditions when manually testing channel operation.

Data - These keys specify the data to be stored in an addressed location. Correct parity is normally generated. Incorrect parity may be generated under control of the Reverse Data Parity Switch. The keys can be changed without disrupting the IOCE operation.

Reverse Data Parity - This switch causes incorrect parity to be generated for data specified in the Data Keys. The test light is on when this switch is on.

Display - This switch causes information in an addressed location to be displayed. The data in the storage location specified by the Address Keys and Storage Select Switch is displayed in the indicators normally associated with the item selected. The switch is active only while the IOCE is in the stopped state.

Address Compare (Storage Address) - This switch provides a means of performing the following functions on an instruction address comparison.

   1.  In the STOP position, an equal comparison between the
       Address Keys and Instruction Address Register causes
       the IOCE to enter the stopped state. The stop occurs
       at completion of execution of the addressed instruction.

   2.  In the LOOP position, an equal comparison between the
       Address Keys and the Instruction Address Register
       causes a looping operation between the addresses
       specified in the Data Address and IAR keys.

   3.  In the PROCESS position, no comparison is performed.
       This is the normal position.

The test light is on when this switch is not in the Process position.

Rate - This switch indicates the manner in which instructions are to be performed when in diagnostic mode.

   1.  In the PROCESS position, the system operates at normal
       clock speed.

   2.  In the INSTRUCTION-STEP position, one complete machine
       instruction is executed for each depression of the Start
       Switch, after which the IOCE returns to the stopped state.
       Any machine instruction can be executed in this mode.
       Input/Output instructions are executed in this mode.
       Input/Output instructions are completed to the inter-

ruption point. The interval timer is not incremented
while the Rate Switch is in this position. Moving the
Rate Switch from PROCESS to INSTRUCTION STEP while IOCE
is running, stops the IOCE after completion of the current
instruction.

3. In the SINGLE-CYCLE position, the CLU advances by its
   minimum clock amount for each depression of the Start
   Switch, returning to the stopped state each time. Input/
   Output instructions can be single cycled to the point
   where asynchronous operation begins on the next de-
   pression of the Start Switch and runs to completion.
   If an interruption request results, the interruption
   sequence must be single cycled. Moving the Rate Switch
   from PROCESS to SINGLE-CYCLE while the IOCE is running
   causes the IOCE to enter the stopped state.

The test light is on when the Rate Switch is off the PROCESS
position.

Set IC - This switch enters an address into the Instruction Address
Register; the address is specified in the Address Keys. The switch
is active only while the IOCE is in the stopped state.

Start - This switch starts the operation defined by the Rate Switch.
If it is pressed after a normal stop, it causes the continuation of
instruction processing as if no stop has occurred. If it is pressed
after system reset, the instruction designated by the Instruction
Address Register is the first one executed.

Stop - This switch causes IOCE to enter the stopped state. The
stopped state is indicated by the manual indicator being on. The
transition from operating state to stopped state occurs at the
end of instruction execution, prior to the fetching of the next
instruction. When the IOCE is in the wait state, the transition
takes place immediately. All interruptions which are pending
and which are not masked off are taken, causing the old PSW
to be stored and the new one fetched before entering the stopped
state.

Storage Select - This switch selects the storage area that is to
be addressed by the Address Keys. The three positions are:

1. MACH Storage

2. Local Storage

3. Main Storage

The switch can be changed without disrupting IOCE operations.

NOTE: The Local Store Map on the console is to be used as
an aid in setting up the address switches for displaying
or storing information in local storage. The sector column
indicates the setting of the IAR Switches 22 and 23 which

identifies the appropriate quadrant in local storage. The
word within the quadrant, from 0 to 15, is addressed through
the IAR Switches 24 through 27 by the Binary Settings 0000
through 1111, respectively. The appropriate pushbutton is
then used to produce the intended result (see Figure 5-4).

Store - This switch stores information in an addressed location. The
contents of the Data Keys are placed in the location specified by
the Address Keys and the Storage Select Switch. The switch is
active only while the IOCE is in the stopped state.

Reset - This switch resets the IOCE. The IOCE is placed in the
stopped state and all pending interruptions are eliminated. All
error status indicators are reset.

PSW Restart - This switch causes a subsystem reset followed by a load
PSW operation from MACH storage location zero. At the completion of
the PSW load, the IOCE is changed from stopped to operating state.
The switch is active only while the IOCE is in the stopped state.

Register Set - This pushbutton transfers the contents of the Data
Keys to the configuration register PSBAR, or ATR, under control of
the Set PSBAR/CCR or Set ATR switch. It is active only while the
IOCE is in the stopped state.

Set PSBAR/CCR - This switch directs the loading of PSBAR or CCR from
the Data Keys.

Set ATR - This switch directs the loading of ATR Registers from the
Data Keys.

Check Reset - This pushbutton resets the Check Registers.

IAR - This group of indicators displays the contents of the Instruc-
tion Address Register.

Master Check - This indicator is on when any trigger in one of the
Check Registers is on.

MC Points - This group of indicators displays the following hard-
core maintenance control points:

| | |
|---|---|
| Pass | Supervisory STAT |
| Fail | Main Storage Accept |
| Binary Trigger | Main Storage Access Request |
| Test Counter = 0 | Ring Counter Mode |
| FLT Operation Register 0 | Main Storage Mode |
| FLT Operation Register 1 | ROS Mode |
| FLT Operation Register 2 | Diagnostic Mode |
| FLT Operation Register 3 | Hard Stop |
| FLT Operation Register 4 | Log Trigger |
| FLT Operation Register 5 | Block Indicators |
| Sequence Counter 4 | Single Cycle |
| Sequence Counter 2 | CLU Clock |

```
Sequence Counter 1          Channel Clock
Sequence Stat 1             ROS Clock
Sequence Stat 2             Main Storage Clock
Sequence Stat 3             Check Interruption Enable
Sequence Stat 4             Check Register Gated
Progressive Scan Stat       Check Pending
```

<u>SDR</u> - This group of indicators displays the Storage Data Register.

<u>Status</u> - These indicators are arranged in four groups of 36 each to provide a display of CLU and channel status information. The data displayed in each set of indicators are controlled by a rotary switch which can select up to 8 words. The Selector Switch also adjusts a roller format to identify the information displayed. Figure 5-7 details the data displayed for each of the 4 groups.

<u>Check Control</u> - This switch provides 4 modes of operation.

1.  In the DISABLE position, any CLU error that occurred is set into the Check Register but no further action will occur.

2.  In the STOP position, the first CLU error causes the element to stop with the error displayed in the Check Register.

3.  In the PROCESS position, each error detected in the CLU causes an error logout and machine check interruption if Bit 13 of the PSW is not masked. If Bit 13 of the PSW is masked, the Check Register is set, and a check pending trigger is set.

4.  In the CHANNEL STOP position, a Selector Channel or CLU error will cause the channel and CLU to stop with the error displayed on the Check Register.

<u>Check Reset</u> - This switch resets all triggers in the Check Register and turns off the master check light.

<u>FLT Controls</u> - This switch provides 5 methods of operation when running FLT programs.

1.  In the PROCESS position, each FLT test is executed 16 times.

2.  In the STOP ON FAIL position, the CLU stops after repeating a test 16 times if the fail trigger has been set.

3.  In the REPEAT position, the FLT test being executed is repeated continuously.

4.  Backspace

5.  Load and Stop

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Figure 5-7.  IOCE Roller Strip Layout

The test light is on when this switch is not in its normal position.

FLT Mode -

1.  Execute Position - This position of the switch redefines
    the load switch to provide for initial loading of FLT
    programs.

2.  Force-Pass Position - The switch in this position causes
    a failing pass/fail test to be by-passed.

The test light is on when this switch is not in its normal position.

Force Condition -

1.  Indicators Position - A special FLT Op Register is used to
    control scan-out during execution of FLT's. At such times
    the information displayed in the switchable indicators is
    under control of this Op Register rather than the normal
    selector rotary switches. Force Indicators provide a par-
    tial override of the FLT Op Register. It allows certain
    registers and status information to be displayed regardless
    of the contents of the Op Register, and is intended for
    use primarily during single cycling of FLT's.

2.  MS Mode Position - Forces MACH storage mode

Repeat Instruction (IAR) - This switch causes the instruction at the
location specified by the Address Keys to be repeated under control
of the Rate and Start Switches. The test light is on when this
switch is not in its normal position.

Disable Interval Timer - This switch prevents the interval timer
from advancing. The test light is on when this switch is not in
its normal position.

Logout - This switch causes a complete logout of CLU and channel
status into MACH Storage. The logout is identical to that which
occurs when a check condition is detected.

Address Compare (ROS) - This switch causes a comparison of the
twelve low-order Data Keys and the ROS address.

1.  In the STOP position, the CLU stops on an equal com-
    parison. The stop occurs at completion of the ad-
    dressed micro-instruction.

2.  In the SYNC position, an oscilloscope sync pulse is
    generated on an equal comparison.

The test light is on when this switch is not in the SYNC position.

Repeat Instruction (ROS) - This switch causes the mirco-instruction
at the location specified by the twelve low-order Data Keys to be re-
peated continuously. The test light is on when this switch is not
in its normal position.

Test - This switch is operative when the state bits are both zero
(i.e., the element is in State Zero). When set "on", the power-on/
off switch is enabled and the CCR contents may be changed by manual
controls.

Selector Channel Display - This switch selects a Selector Channel
for display purposes. The particular status word displayed is
selected by the rotary switch and format roller arrangement des-
cribed under the status indicators.

Invert SAR Bit 17 - This switch inverts SAR Bit 17, thereby inter-
changing the two 16k halves of the 32k (byte) MACH storage. The
test light is on when this switch is not in its normal position.

Stop On Check - This switch provides for termination of the stor-
age test when a storage check is detected.

Storage Test - This switch selects one of four test patterns to be
applied to MACH storage. The four patterns are:

    1.   All-Zeros Test

    2.   All-Ones Test

    3.   Worst-Pattern Test

    4.   Inverse Worst-Pattern Test

The test light is on when this switch is not in its normal position.

Write - This switch causes the pattern defined by the storage test
switch to be written into all MACH storage locations when start is
depressed. Testing is terminated by a stop on check condition or
by an element reset.

Bump Test - This switch causes the pattern defined by the storage
test switch to be written into all bump storage locations when
start is depressed. Testing is terminated by a stop on check
condition or by an element reset. Bump cores, not used by the
IOCE, require periodic testing to insure they are not inducing
noise in the array.

Frame Thermal - This group of indicators monitors frame temper-
atures within the element. Whenever a temperature upper limit
is exceeded in the IOCE storage, or power distribution unit, the
corresponding indicator is lit.

Lamp Test - This switch allows all indicators, with the exception of
the marginal-voltage indicators, frame thermals, open CB, and power
check, to be tested simultaneously.

Marginal Voltage - This set of indicators, one for each of the mar-
ginal voltage control potentiometers, indicates when a marginal
voltage has been varied from its nominal value.

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Marginal Voltage Control - This set of potentiometers, one for each
of the marginal voltages, allows a marginal voltage to be varied
around its nominal value.  More than one voltage can be varied at
a time.

Marginal Voltage Select - This switch selects the marginal voltage
to be monitored on the meter.  The following voltages may be se-
lected:

| | |
|---|---|
| 1. +6 TC | (Temperature Compensation -- Local Storage) |
| 2. +6 VAR | (Variable -- Local Storage) |
| 3. +6 M1 | (Variable -- CLU) |
| 4. +6 M2 | (Variable -- CLU) |
| 5. +6 M3 | (Variable -- CLU) |
| 6. +6 ROS | |
| 7. +60 XY | (MACH Storage XY Drivers) |
| 8. +60 Z | (MACH Storage Z Drivers) |

In addition, a MONITOR VOLTAGE position enables the Monitor Volt-
age Select Switch.

Monitor Voltage Select - This switch selects a non-marginal volt-
age to be monitored by the meter.  The switch is active only when
the Marginal Voltage Select Switch is in the Monitor Voltage po-
sition.

Open CB - This indicator is turned on if any circuit breaker in
the power distribution unit opens.

Power Check - This indicator is turned on if one or more DC power
regulators is overloaded.

OTC Test and OBS Test - These switches, in the IOCE power section,
simulate the thermal warning and on-battery conditions respectively.

On-Line/Off-Line (Channel-to-Channel Adapter 1) - This toggle switch
is installed on the control panel when one or more Channel-to-Channel
Adapters are installed in the IOCE.  It enables or disables the
interfaces on the inboard and outboard side of Channel-to-Channel
Adapter 1.  It is active only when the host IOCE is in State Zero.

Disabled (Channel-to-Channel Adapter 1) - This indicator is in-
stalled on the control panel when one or more Channel-to-Channel
Adapters are installed in the IOCE.  It lights green when Channel-
to-Channel Adapter 1 interfaces are disabled.

On-Line/Off-Line (Channel-to-Channel Adapter 2) - This toggle
switch is installed on the control panel when one or more
Channel-to-Channel Adapters are installed in the IOCE. It
enables or disables the interfaces on the inboard and out-
board side of Channel-to-Channel Adapter 2. It is active
only when the host IOCE is in State Zero and Channel-to-
Channel Adapter 2 is installed into the IOCE.

Disabled (Channel-to-Channel Adapter 2) - This indicator is in-
stalled on the control panel when one or more Channel-to-Channel
Adapters are installed in the IOCE. It lights green when Channel-
to-Channel Adapter 2 interfaces are disabled. If Channel-to-
Channel Adapter 2 is not in the IOCE, it will light green when
the On-Line/Off-Line Switch for Channel-to-Channel Adapter 2 is
in the OFF LINE position.

Table 5-3. IOCE Switches and Their Operational Enviroment

| | State Zero | | State One |
|---|---|---|---|
| | Test Switch Off | Test Switch On | Diagnostic Mode |
| Element MPO (Always Enabled) | x | x | x |
| Interrupt | x | x | x |
| Load | x | x | x |
| Load Unit | x | x | x |
| Power On-Off | | x | |
| Address Keys | x | x | x |
| Data Keys | x | x | x |
| Reverse Data Parity | x | x | x |
| Display | x | x | x |
| Address Compare (Storage Addr.) | x | x | x |
| Rate | x | x | x |
| Set IC | x | x | x |
| Start | x | x | x |
| Stop | x | x | |
| Storage Select | x | x | x |
| Store | x | x | x |
| Reset | x | x | |
| PSW Restart | x | x | x |
| Register Set | | x | |
| Check Control | x | x | |
| Check Reset | x | x | |
| FLT Control | x | x | x |
| FLT Mode | x | x | x |
| FLT Force Condition | x | x | x |
| Repeat Instruction (IAR) | x | x | |
| Disable Interval Timer | x | x | x |
| Logout | x | x | x |
| Address Compare (ROS) | x | x | |
| Repeat Instruction (ROS) | x | x | |
| Test | x | x | |

Table 5-3.  IOCE Switches and Their Operational Enviroment (Cont.)

| | State Zero | | State One |
| --- | --- | --- | --- |
| | Test Switch Off | Test Switch On | Diagnostic Mode |
| Selector Channel Display | x | x | |
| Invert SAR Bit 17 | x | x | |
| Stop on Check | x | x | |
| Set PSBAR/CCR | | x | |
| Set ATR | | x | |
| Bump Test | x | x | x |
| Storage Test | x | x | |
| Write | x | x | |
| Lamp Test 1 | x | x | x |
| Marginal Voltage Select 1 | x | x | x |
| Monitor Voltage Select 1 | x | x | x |
| Marginal Voltage Controls 1 | x | x | x |
| OBS Test 2 | x | x | x |
| OTC Test 2 | x | x | x |
| On Line/Off Line Chan. to Chan. Adapter | x | x | |

1  Always enabled.
2  Always enabled.  Located in IOCE power section.

INTRODUCTION

The Peripheral Adapter Module (PAM), IBM 7289-02, provides for the
on-line attachment of remote and local peripheral devices to the
9020D System.  PAM controls the communications of data between the
IOCE and such typical peripheral devices as Teletypewriters, Lenkurt
26B Modems and the 1052 Printer Keyboard.

PAM is functionally divided into PAM Common and PAM Adapters.
PAM Common provides addressing, priority, configuration and general
controls to service all adapters.  The adapters provide all necessary
bit/byte conversion, data control, message initiation, message ter-
mination, and matching of device electrical interface characteristics.

GENERAL CHARACTERISTICS:

The PAM, IBM model 7289-02, is comprised of PAM Common and adapters*
as follows:

PAM Common

PAM Common includes seven functional sections (see Figure 6-1).

1.  Interface Control - Provides control for transfer of data
    between the adapters and one of two IOCE - PAM interfaces.

2.  Address Control - Provides a check for a valid 8-bit address
    code from IOCE during an initial selection sequence.

3.  Priority Control - Establishes priority for servicing adapt-
    ers, previously selected.

4.  Configuration Control - Enables communication paths into the
    PAM and controls the configuration state of the PAM.

5.  Test and Monitor Adapter - Monitors malfunctions in PAM
    Common and permits all other adapters to be tested using
    test commands.  The adapter includes special addressing con-
    trols.

6.  Maintenance Test Panel - Provides manual switches and indi-
    cators to manually test PAM.  The panel also includes power
    status and indications of malfunctions.

7.  Common Control - Provides sequencing and interconnection to
    other six control functions in PAM Common.

*The 7289-02 has the capability to provide other adapters for future
systems.
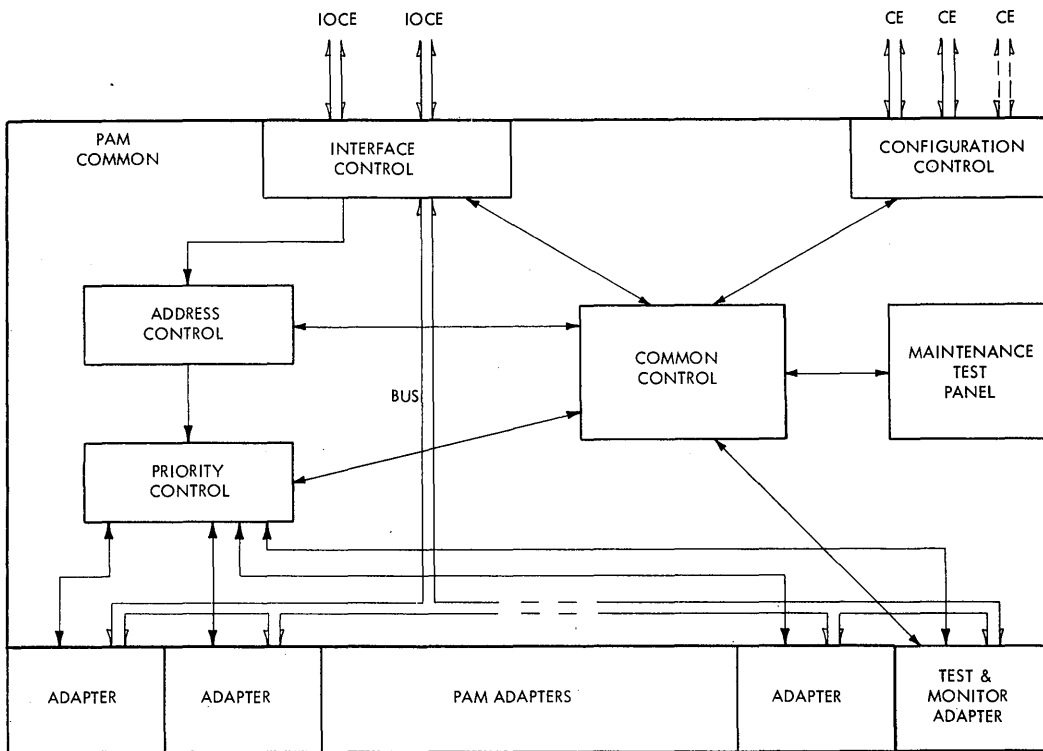
Figure 6-1. PAM Block Diagram

Adapters

Adapters provide the electrical interface suitable for the device or
class of devices to be attached to the 9020D System. These adapters
are classified as either simplex or duplex; with a simplex adapter a
device may attach to only one adapter while, with duplex adapters, a
single device may attach to one adapter in each of two PAM's. Duplex
adapters may also be used in a simplex adapter configuration. A flow
diagram of a typical PAM adapter is shown in Figure 6-2.

1. General Purpose Input - Receives data bytes in bit parallel/
byte serial fashion of up to 8 bits plus parity and operates
on a demand/response basis from a device with matching elec-
trical interface.

2. General Puspose Output - Transmits data bytes of up to 8 bits
plus parity bit parallel/byte serial fashion and operates on
a demand/response basis to a device with matching electrical
interface.

3. Interfacility Input - Receives data bytes of 8 bits plus
parity, serially, and operates at 600, 1200 or 2400 bits
per second from a standard Lenkurt 26B Modem or optionally,
from a Digital Modem which has a Type III NAS DACOM inter-
face.

6-2

PAM COMMON/ADAPTER INTERFACE
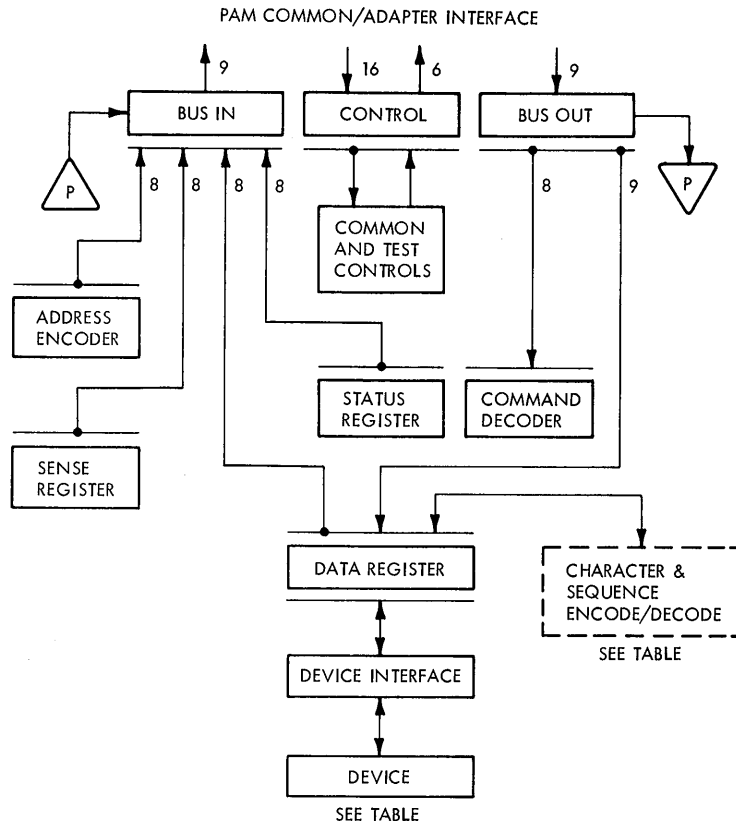
| | ADAPTER | DATA FROM/TO DEVICE | | CONTROL LINES | | CHARACTER & SEQUENCE |
|---|---|---|---|---|---|---|
| | | SERIAL | PARALLEL | IN | OUT | ENCODE/DECODE |
| | GPI | | 8+P | 2 | 4 | |
| | GPO | | 8+P | 6 | 3 | |
| | INTI | 8+P | | 1 | | SYNC SDC LRC EOM |
| | INTO | 8+P | | 1 | | SYNC LRC EOM |
| | RVDP | | 6+P | 3 | 1 | |
| | CD | 12+P | | 3 | | TAG BITS |
| | TTYLL | 5 | | | | START STOP SDC SYNC LRC EOM FIGS LTRS |
| 1052 | PRINTER | | 6+P | 4 | 7 | EBCDI TO T/R |
| | KEYBOARD | | 6+P | 5 | 1 | PT & T TO EBCDI |
| | FDEP | 6+P | | | | START STOP LRC UC LC CANCEL |
| | BP | 6+P | | 12 | 19 | |

Figure 6-2.  PAM Adapter Flow Diagram

4.  Interfacility Output - Transmits data bytes of 8 bits plus
    parity, serially, and operates at 600, 1200 or 2400 bits per
    second into a standard Lenkurt 26B Modem, or optionally, into
    a Digital Modem which has a Type III NAS DACOM interface.

5.  Teletypewriter, Half Duplex, Long Lines - Transmits and re-
    ceives data bytes of 7.42 Baudot start/stop code serially at
    100 words per minute.

6.  Radar Video Data Processor (RVDP) - Receives data bytes of 6
    bits plus parity in parallel and operates at 2400 or 7200
    bits per second from a Burroughs RVDP.

7.  1052 - Transmits data bytes of 6 bits plus parity in parallel
    and operates at 14.8 characters per second to a 1052 Printer.
    Receives data bytes of 6 bits plus parity in parallel and
    operates up to 14.8 characters per second from a 1052 Key-
    board.

8.  Common Digitizer (CD) - Receives data fields of 12 bits plus
    odd parity serially at 2400 bits per second from one channel
    of a CD Data Receiving group.

9.  Flight Data Entry and Printout (FDEP) - Transmits and re-
    ceives characters serially in 6 bits plus parity PT and T
    start/stop code at up to 8.33 characters (75 bits) per
    second to/from a modified IBM 1051 Control Unit over leased
    telegraph lines.

10. Buffer Processor (BP) - Half Duplex, transmits and receives
    data serially in any 6 bit plus odd parity code at 81,600
    bits per second.

Connection and Termination of Parallel Adapters

The signal lines from each device are routed to one adapter in each
of two PAM's to provide a duplexed adapter configuration.*  The
method of parallel attachment is via a jumper cable between the two
PAM's (shown in Figure 6-3) is as follows:

    The signal cable from the device terminates in a Type A serpent
connector which plugs into the associated I/O connector in PAM 1, then
runs to the adapter via flat transmission cable.  It enters the adap-
ter via flat transmission cable.  It enters the adapter circuit th-
rough a board connector.  The parallel line then leaves the board via
an adjacent connector and flat cable running back to the I/O connector.
At this point, a coax cable with Type B serpent connector is plugged
in and runs to the equivalent I/O connector in PAM 2 where it plugs
in via a Type A serpent connector.  The signal travels to the adapter
via flat cable, plugging into the board connector as was done in PAM
1.  The adjacent board connector is used to plug in a terminator card.
This terminates the transmission line.

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*Not applicable to simplex adapters.

6-4
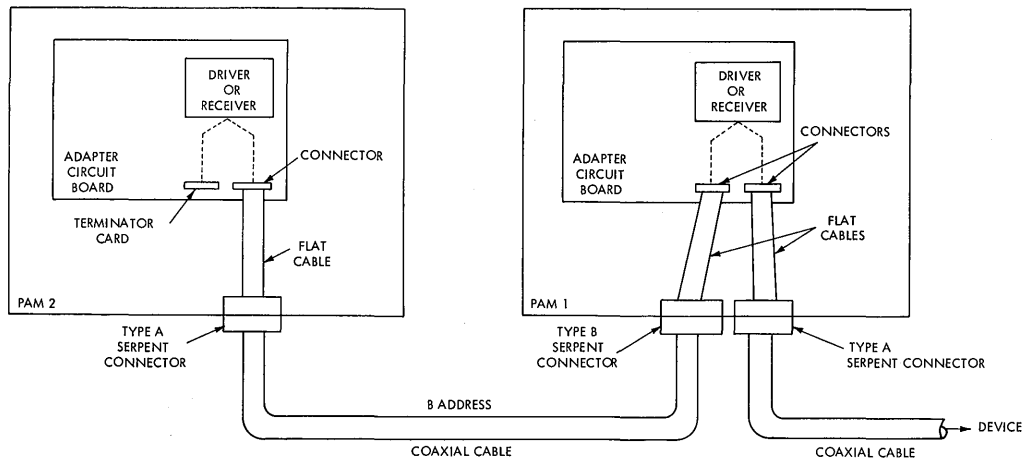
Figure 6-3.  Connection and Termination of Parallel Adapters

When removing a PAM 1 adapter from the line, it is necessary to insure continuity of signal to the PAM 2 adapter.  This is done by removing the Type A and B serpent connectors for that adapter from their I/O connectors in PAM 1, and plugging them together.

When removing a PAM 2 adapter from the line, it is necessary to re-terminate the line at PAM 1.  This is done by unplugging the flat cable in PAM 1 which runs from the circuit board to the I/O connector for PAM 2.  In its place on the board, a terminator card is inserted.

When removing a PAM 1 or PAM 2 adapter from the line, power need not be removed in the PAM nor will any disruption to other adapter take place.

NOTE:  The foregoing does not apply to the TTYLL, BP, FDEP or 1052 adapters.  References to terminator cards applies only to those lines requiring termination.

FUNCTIONAL CHARACTERISTICS

PAM adapters are selected by one of two IOCE's through the associated IOCE - PAM interface in PAM.  This IOCE multiplexor channel interface is assigned in PAM Common by Configuration Control, previously set from a CE in the 9020D System.  The adapters are then selected and serviced by that IOCE via PAM Common Control on a demand/response basis.

Initial Selection

An initial selection sequence is initiated by the multiplexor channel as a result of the execution of the Start I/O instruction or as a result of command chaining within the channel.

The PAM will not respond to initial selection when any of the following conditions occur:

1. Parity error on Address Out to PAM.

2. PAM is not operational (i.e., power off or PAM is being reset).

3. PAM is isolated for test purposes.

4. PAM is not configured for selection by the particular IOCE.

5. The address is not used in PAM.

6. The address is not available in PAM (i.e., not all addresses are available to the secondary interface).

A command with an invalid code or incorrect parity will be rejected during initial selection by presenting Unit Check Status.

After initial selection of a PAM adapter by the IOCE, further I/O instructions to that address will be handled in accordance with the description of this type of operation in the IBM 9020D and 9020E System Principles of Operation manual.

Data Servicing

Once initial selection has been completed and the addressed adapter has accepted a command, data servicing occurs to transfer bytes to and from the multiplexor channel. Data servicing is initiated by the PAM. When the current command is Write, a request for byte service is set when the data buffer becomes empty within the adapter. When the adapter is scanned, the address of the adapter becomes available. The Interface Control establishes contact with the multiplexor channel and the data byte is loaded into the adapter data register.

An input data servicing cycle is similar, except the direction of flow of the data byte is reversed. The Interface Control establishes contact with the channel as before and presents the adapter address. After receiving an indication from the channel, the contents of the adapter data register are transferred to the IOCE.

During either input or output data servicing, the channel could respond with a Stop sequence terminating the current command. Data is not transferred during this cycle in either case; on input, the data is lost. The data byte is also lost on input should an attempt be made to store in a protected area of main storage. The addressed adapter presents interrupt conditions to the multiplexor channel through status.

Status Servicing

Status servicing is similar to input data servicing and occurs via the interface such that valid status information of the adapter is set into the CSW Status byte.

6-6

If the status is accepted by the channel, the channel will acknowledge receipt of the status byte. The interface Control can then begin priority scanning for data and/or status to be serviced from the next adapter.

If the status cannot be accepted by the channel, then it will be queued. Status will be presented later when it can be accepted by the channel.

The status byte indicates if the I/O operation for the command was executed successfully. Detection of a malfunction is indicated by a Unit Check bit. A sense command may be issued by the program to the same adapter to obtain a sense byte containing further information about the condition in the adapter.

Test and Monitor Adapter

Malfunctions occurring in PAM Common during PAM operation are stored in a sense register of the Test and Monitor Adapter. This adapter requests service when malfunctions are detected in PAM Common.

The Test and Monitor Adapter is also used to test adapters through program control or manual control. This Test and Monitor Adapter accepts test commands that cause signals on test lines to all other adapters. These adapters, if issued a test mode command, will respond to the test lines so that correct operation can be monitored.

Maintenance Test Panel

A Maintenance Test Panel contains switches and indicators to manually test adapters through use of the Test and Monitor Adapter. Both the Maintenance Test Panel and Operator's Panel are used to indicate power failures, PAM state, and provide a Power ON-OFF switch. Marginal Checking of voltages is possible at the Maintenance Test Panel.

DESIGN DETAILS

PAM COMMON

PAM Common contains the controls which are common to all adapters. A diagram showing PAM Common data flow is presented in Figure 6-4.

PAM Addressing

Data or control bytes transmitted between PAM and IOCE are preceded by an 8 bit unit address byte which uniquely specifies the adapter (and associated I/O device) for the multiplexed operation. During initial selection the PAM adapter that is addressed responds with an address that is checked by the IOCE to verify the selection. A total of 240 binary address codes, 16 to 255, are available in PAM.
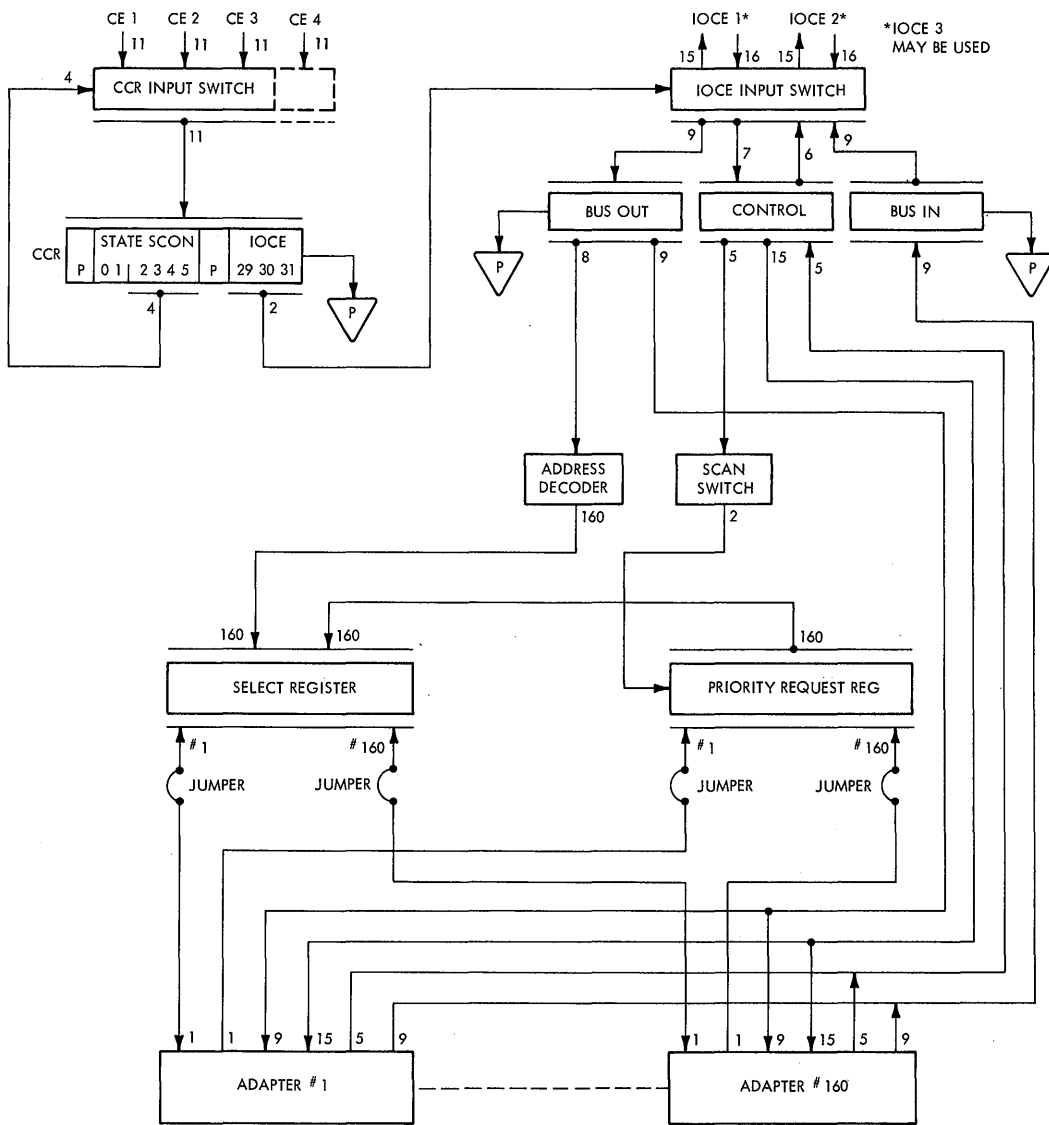
Figure 6-4. PAM Common Data Flow

Interface Addresses

Addresses are available to each PAM interface as given in Figures 6-5 and 6-6. The secondary interface can be assigned to one group of 80 addresses or to two groups of 80 addresses through program control (by issuing the half secondary or full secondary commands to the Test and Monitor adapter) while the primary interface always provides for two groups of 80 addresses. Only one interface if any, is assigned at a time, as described under Configuration Control. The addresses avail-
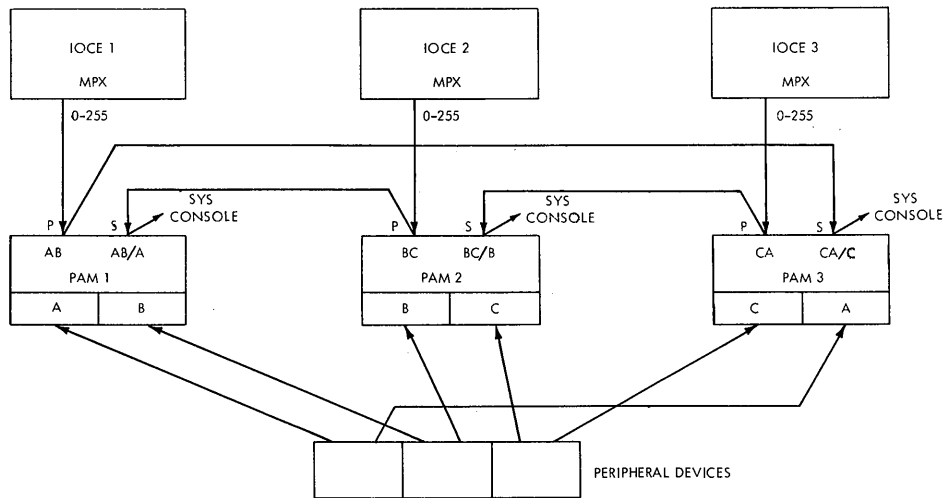
P – PRIMARY INTERFACE – ACCEPTS UP TO 160 ADDRESSES.

S – SECONDARY INTERFACE – ACCEPTS UP TO 80 ADDRESSES OR 160 ADDRESSES.

ADAPTERS A – ADDRESSES 16 TO 95 ⎫
ADAPTERS B – ADDRESSES 96 TO 175 ⎬ EACH IOCE CAN ADDRESS 0 TO 255.
ADAPTERS C – ADDRESSES 176 TO 255 ⎭

Figure 6-5.   PAM Addressing Capability – 3 PAM's



P – PRIMARY INTERFACE – ACCEPTS UP TO 160 ADDRESSES

S – SECONDARY INTERFACE – ACCEPTS UP TO 80 ADDRESSES OR 160 ADDRESSES.

ADAPTERS A – ADDRESSES 16 TO 95 ⎫ EACH IOCE CAN ADDRESS
ADAPTERS B – ADDRESSES 96 TO 175 ⎭    0 TO 255.

Figure 6-6.   PAM Addressing Capability – 2 PAM's

able at an interface are determined by the address selection jumpers and secondary commands as follows:

Address Codes

| PAM Designation | Primary | Half Secondary 80 addresses | Full Secondary 160 addresses |
|---|---|---|---|
| 1 | 16-175 | 16-95 | 16-175 |
| 2 | 96-255 | 96-175 | 96-255 |
| 3 | { 16-95 } { 176-255 } | 176-255 | { 16-95 } { 176-255 } |

Configuration Control

Configuration control determines which PAM interface is active for selection by the attached IOCE. The Configuration Control Register (CCR) specifies through the SCON bit assignments those Computing Elements which can reconfigure a PAM. Two state bits specify one of four system states for PAM. The Configuration Control register in PAM contains a total of 9 bits plus 2 parity bits as shown below.

| P | S0 | S1 | 1 | 2 | 3 | 4 | | P | 1 | 2 | 3 |
|---|---|---|---|---|---|---|---|---|---|---|---|

Parity  State          SCON          Parity    IOCE
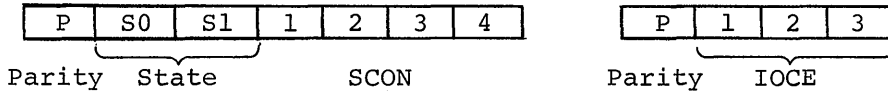
IOCE assignment is determined through the use of three bits. Only one IOCE can be assigned by these bits.

PAM System IOCE Bit Assignments

IOCE BITS

| PAM | 1 | 2* | 3 |
|---|---|---|---|
| 1 | X | X | - |
| 2 | - | X | X |
| 3 | X | - | X |

*IOCE bits 1 and 2 are used in a two PAM system.

X - Either/or condition for a PAM's IOCE bits. If both X's are one's, the assignment is forced to the PAM's like numbered IOCE.

SCON Assignment

SCON bits assign up to four computing Elements by a "one" in the corresponding bit position of the SCON assignment.

State Assignment

System state of PAM is specified by state assignment in the CCR as follows:

SO  Sl

1   1   State Three
1   0   State Two
0   1   State One
0   0   State Zero (The Maintenance panel is available for main-
                   tenance purposes only in this state.)

Parity

The CCR is parity checked continuously and incorrect parity conditions are indicated through the Element Check line.  The Configuration parity bit in the sense register of the Test and Monitor adapter is also set by incorrect parity.

Priority Controls

PAM Priority

The PAM's should be cabled to have highest priority of the control units in the Multiplexor channel.  The PAM with the primary interface should have higher priority than the PAM with the secondary interface on the channel.

Adapter Priority Controls

Priority is address dependent, with the lowest address code of each address in the group (16 to 95), (96 to 175), and (176 to 255) having highest priority.  Similarily, priority decreases until the highest address code of each group has lowest priority.

Priority is assigned to the two address groups within each PAM as follows:

|  | PAM 1 Addresses (16 to 95) and (97 to 175) | PAM 2 Addresses (96 to 175) and (177 to 255) | PAM 3 Addresses (176 to 255) and (17 to 95) |
|---|---|---|---|
| 1st Priority | 16* | 96* | 176* |
| 2nd Priority | 17 | 97 | 177 |
| 3rd Priority | 97 | 177 | 17 |
| : | : | : | : |
| : | : | : | : |
| 158th Priority | 95 | 175 | 255 |
| 159th Priority | 175 | 255 | 95 |

*Not Available on secondary interface (TAM Adapters)

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Address Assignment

First priority addresses (16, 96, and 176) are assigned to the test and monitor adapter in PAM 1, PAM 2 and PAM 3 respectively.*  Priority of an adapter and the attached peripheral device can be changed by a maintenance man after initial assignment through a different address assignment.

Priority Scan and Service

The priority request lines from the adapters are scanned approximately every 5 microseconds.  Priority controls recognize the adapter request and raise the Request In line to the IOCE.  Scanning continues until the IOCE is available, then stops and services the adapter with highest priority at that time.  Scanning is resumed prior to the end of the "Command Out" signal from the IOCE.

An adapter with high priority could be serviced several times, if required, before an adapter with lower priority is serviced. Priority controls will service an adapter upon request when the following conditions are met:

1.  The adapter requesting service has highest priority at the time of the previous scan.

2.  IOCE multiplexor channel is available.

3.  PAM common is available.

If the secondary interface is assigned in PAM, and an adapter which can be addressed only from the primary interface attempts to request service, it will be ignored.

I/O Operation

PAM common operates in data interleave mode with the multiplexor channel attached to the active interface.  When operating with the CD adapter, PAM common operates in a 2-byte burst mode.  The PAM is designed to operate with the "Input/Output Interface, Channel to Device Control Unit specifications, Appendix D."

PAM Common to Adapter Interface

There are 41 lines between PAM Common and the PAM adapters (Figure 6-7).  Operation of these lines for an initial selection sequence, data servicing and status servicing is shown in timing diagrams in Figures 6-8, 6-9 and 6-10.  The lines are as follows:

Bus Out (9 lines) - There are 8 Bus Out lines from PAM Common to the adapter for the address, data or command byte and one Bus Out line for odd parity.

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*Use of these addresses, since they are used as Test and Monitor adapter addresses, is reduced to a simplex function.
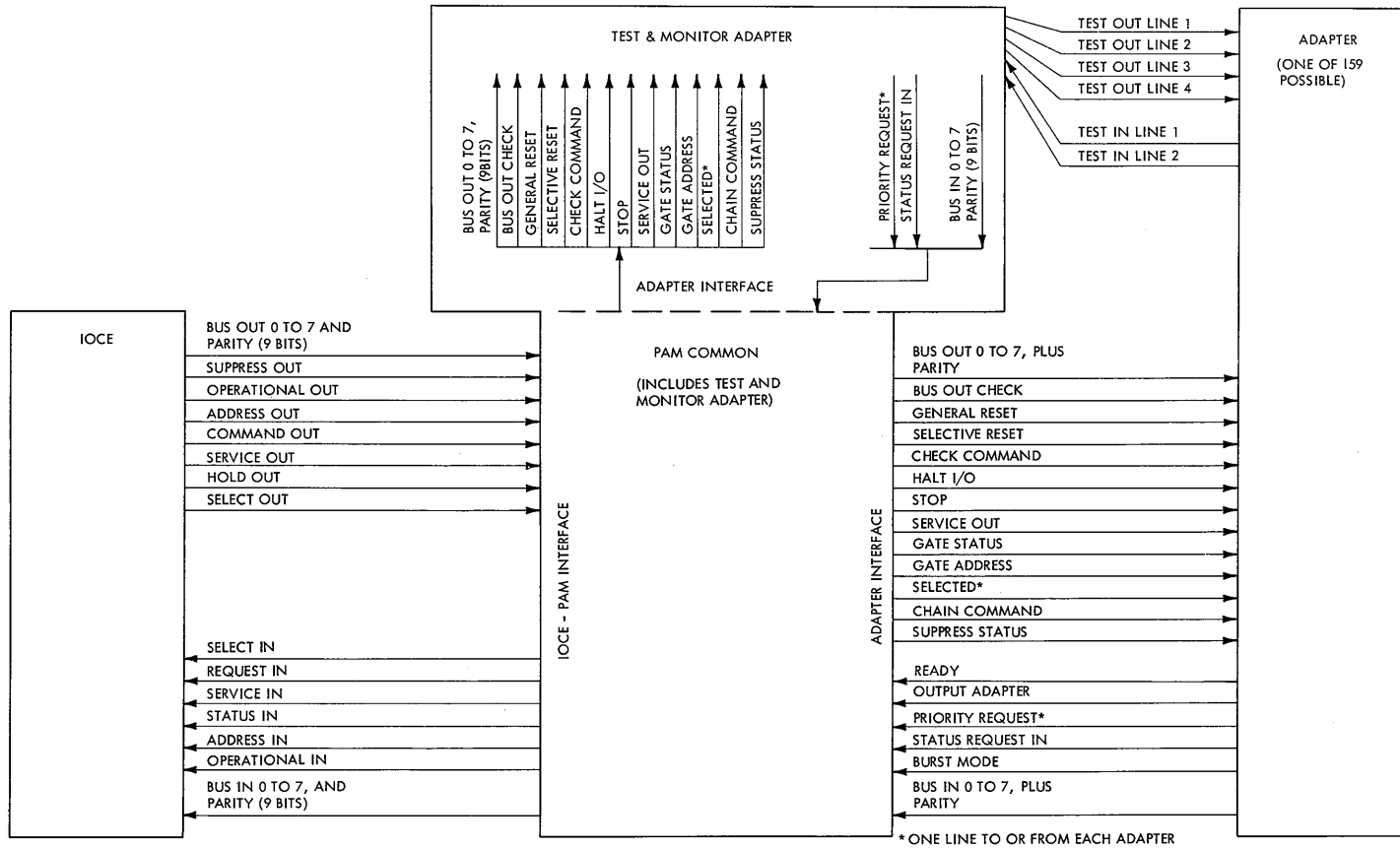
Figure 6-7.  PAM Interfaces
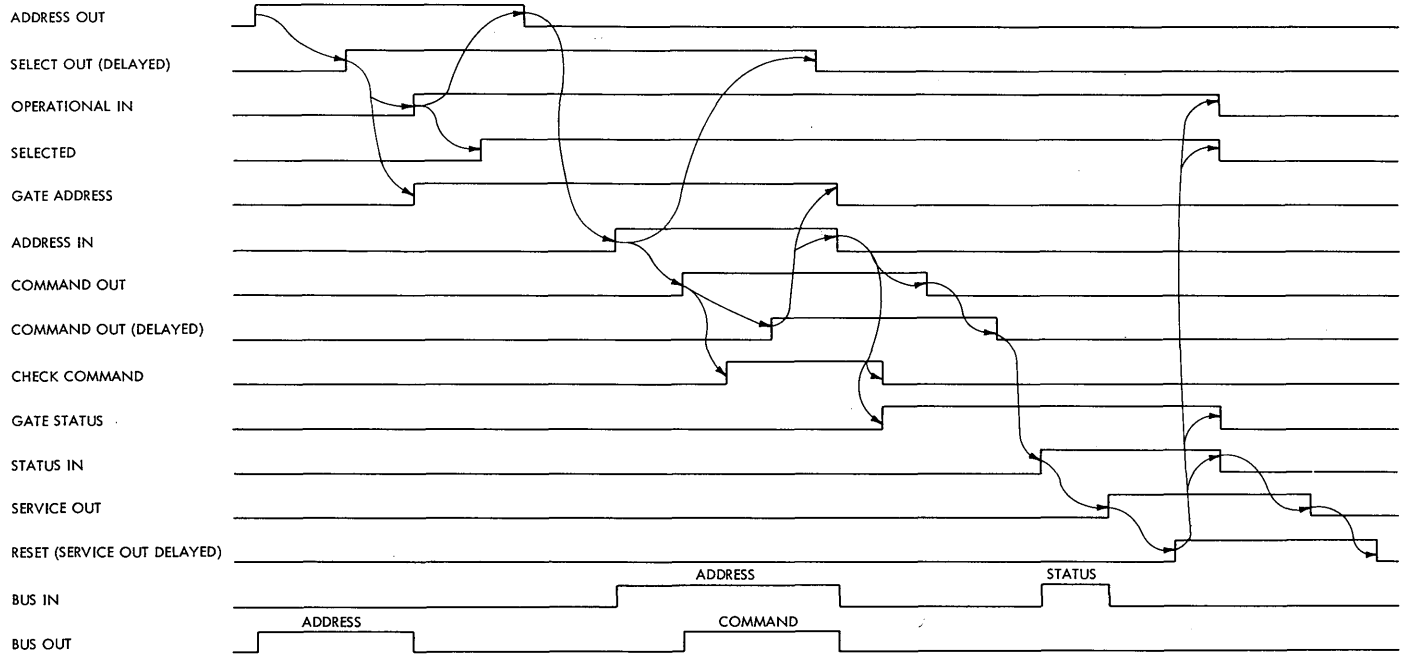
Figure 6-8.  Initial Selection Sequence
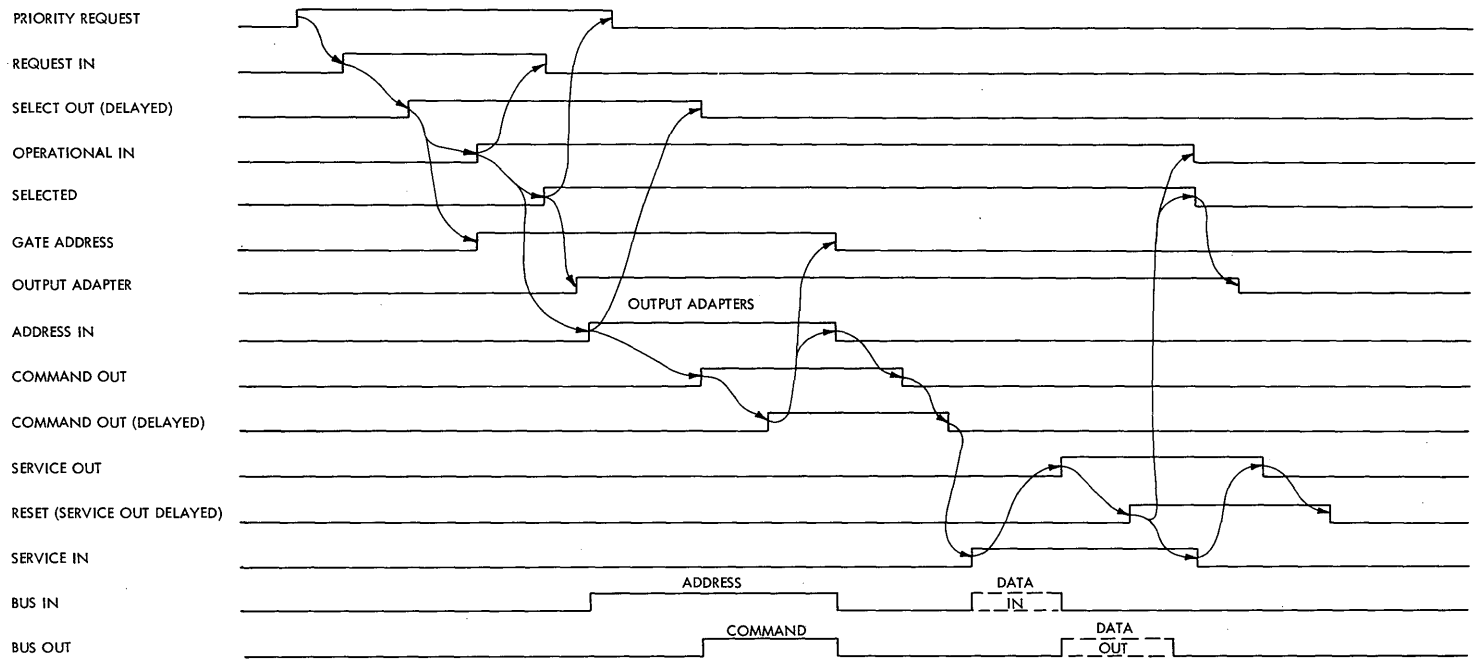
Figure 6-9.  Data Servicing Sequence

PRIORITY REQUEST

REQUEST IN

SELECT OUT (DELAYED)

OPERATIONAL IN

SELECTED

GATE ADDRESS

ADDRESS IN

COMMAND OUT

COMMAND OUT (DELAYED)

GATE STATUS

STATUS IN

SERVICE OUT

RESET (SERVICE OUT DELAYED)

STATUS REQUEST

BUS IN

ADDRESS       STATUS

BUS OUT

COMMAND
PROCEED
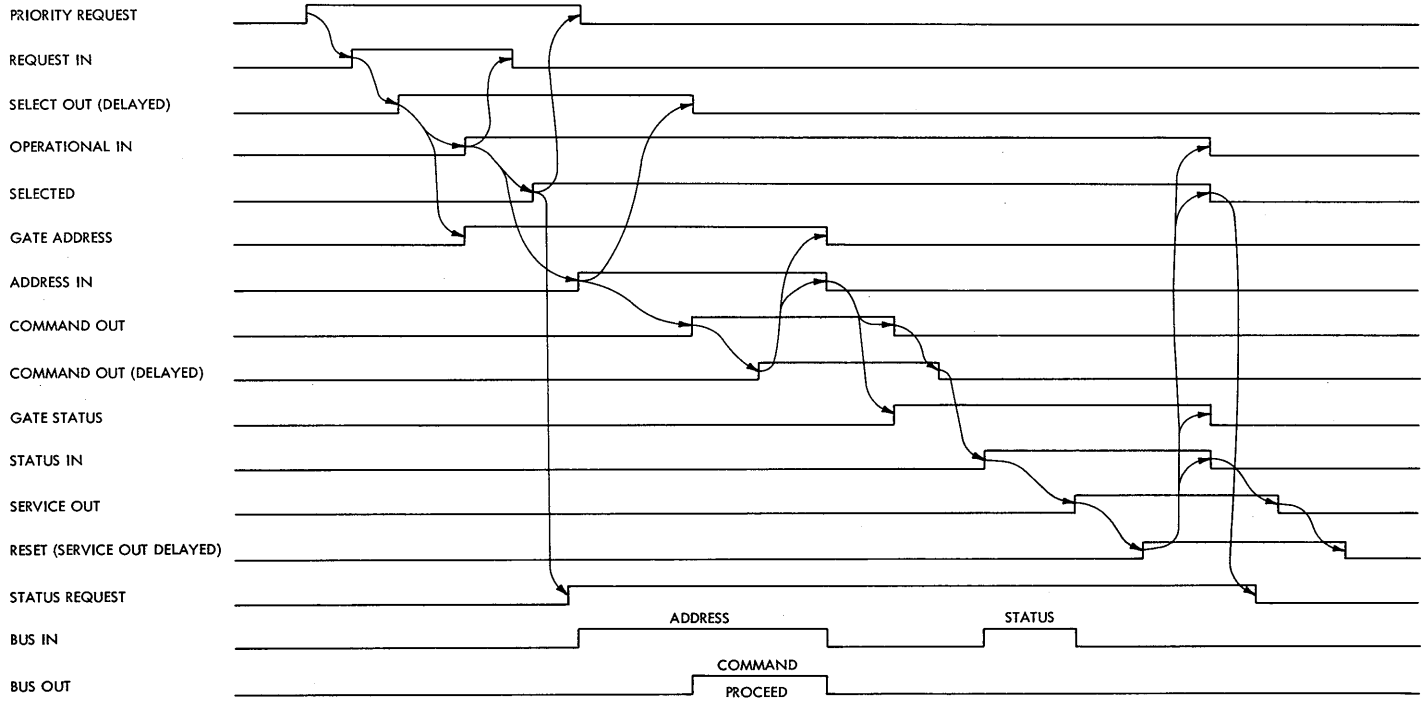
Figure 6-10.   Status Servicing Sequence

Bus In (9 lines) - There are 8 Bus In lines from the adapter to PAM Common for the address, data or status byte, and one Bus In line for odd parity.

Control Out (11 lines) - There are 11 lines from PAM Common which are bussed to all adapters and are set as indicated below.

1.  Bus Out Check - This line is raised by PAM Common when incorrect parity is detected in PAM Common on the IOCE-PAM interface.

2.  General Reset - This line is raised by PAM Common when PAM common detects this condition.

3.  Selective Reset - same as item 2 above.

4.  Halt I/O - same as item 2 above.

5.  Stop - same as item 2 above.

6.  Service Out - same as item 2 above.

7.  Chain Command - same as item 2 above.

8.  Suppress Status - same as item 2 above.

9.  Check Command - This line is raised by PAM Common to indicate the adapter should sample the command byte on Bus Out.

10. Gate Status - This line is raised by PAM Common to indicate the adapter should place its status byte on Bus In.

11. Gate Address - This line is raised by PAM Common to indicate the adapter should place its address byte on Bus In.

Control In lines (4 lines) - There are 4 lines which are bussed from all adapters to PAM Common and set as indicated below.

1.  Output Adapter - This line is raised by the selected adapter to indicate that a write command is being executed.

2.  Status Request In - This line is raised by the selected adapter to indicate that the adapter has status to present within the selection cycle.

3.  Burst Mode - This line is raised by the CD Adapter when it has a two-byte field to present to the channel.

4.  Ready - This line is raised by an adapter having burst mode capability, after receiving service for the first byte in the burst, to indicate that a succeeding byte is available.

Unique lines (2 lines)- There are two lines between PAM Common and each adapter.  These lines are duplicated for all adapters.

1. Selected - This line is raised by PAM Common to select one and only one adapter. Only one Selected line can be set at a time.

2. Priority Request - This line is raised by the adapter to request service for the transmission of a status or data byte.

Test lines (6 lines)- There are four Test Out lines and two Test In lines between the Test and Monitor Adapter in PAM Common and each adapter. These six lines are available for the purpose of testing each adapter and are used according to the adapter requirements.

PAM Resets- Five PAM resets cause PAM Common, except the CCR, and all adapters to be reset. The adapters are reset from the General Reset line in the adapter interface.

1. Power On Reset - This reset occurs when a DC power on condition occurs in PAM at any time; the CCR is reset to zero, except the SCON bits are set to ones.

2. General Reset Pushbutton - This reset occurs when the General Reset Pushbutton is operated at the Maintenence Test Panel. The CCR is not reset.

3. System Reset - This reset occurs when PAM Common receives a System-Reset signal on the CE-PAM interface. The CCR is reset to zero except for the SCON bits which are set to ones.

4. General Reset - PAM is reset when PAM Common receives a General Reset sequence (Suppress Out is down and Operational Out is down) on the IOCE - PAM interface assigned by the CCR. The CCR is not reset.

5. Configuration Reset - PAM is reset after PAM Common receives a new configuration in its CCR which changes the assignment from one interface to another or to no interface. The CCR is not reset. This reset also occurs in Test Mode using manual switches to change the IOCE assignment bits.

Test and Monitor Adapter

The Test and Monitor (TAM) Adapter serves three basic purposes.

1. The TAM adapter, as an addressable control unit, permits diagnostic checking of PAM common by being assigned a unique address on the multiplexor channel. The TAM adapter is able to provide check indications to the program through the Attention Status and the Sense Command.

2. The TAM adapter provides a programmable and manual means of testing all other adapters in the PAM without utilizing their attached devices. To accomplish the testing by programmable means, the program issues Test Mode commands to the adapter under test and issues Test Out and/or check forcing commands to the TAM adapter. Also, it allows test-

ing of other adapters by manual means through use of the
maintenance and test panel.

3. The TAM adapter provides through program control a means of
   selecting either the half or full secondary IOCE/PAM inter-
   face assignments within the limitations of configuration
   control.

The TAM adapter transmits or receives address, command, status, and
sense information to or from the multiplexor channel in the same
manner as other adapters.

General Description

Interface.  The Test and Monitor (TAM) adapter interfaces with PAM
Common over the adapter interface.  There are six test lines to each
adapter; four lines originate in the TAM adapter and terminate at
each adapter, and two lines provide a response from the adapter to
the TAM adapter as shown in Figure 6-7.

Commands.  The TAM adapter will decode commands from the channel
during a select cycle and indicate the acceptance or rejection of the
command to the channel.  The valid commands for the TAM adapter are
as follows:

|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Full Secondary | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Half Secondary | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| Test Out Line 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Test Out Line 1 Pulsed | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| Test Out Line 2 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Test Out Line 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| Test Out Line 4 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| Test Out Line Reset | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Reset Test Out Line 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| Reset Test Out Line 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| Reset Test Out Line 3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

|                               | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|-------------------------------|---|---|---|---|---|---|---|---|
| Reset Test Out Line 4         | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| Force Check Stop              | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| Force TAG Check               | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| Force Configuration Check     | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| Force Address Out Check       | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| Force Command Out Check       | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| Force Service Out Check       | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| Force Address In Check        | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| Force Status In Check         | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| Force Service In Check        | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Pass Address                  | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| Bypass Check Stop             | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Any other codes with correct parity will set a sense bit and present the unit check bit in the unit status byte in response to the command.

Test I/O (0000 0000) - If the Test I/O command reaches the TAM adapter and no outstanding status bits are present, a zero status byte is returned to the channel. If status information is pending, all status bits present are transmitted to the channel.

Control No-Op (0000 0011) - The control no-op command is treated as an immediate type command. It performs no operation, and channel end and device end are transmitted together during the initial selection.

Sense (0000 0100) - When the TAM adapter has accepted a sense command, it will initiate a service request to the channel through PAM common. When the adapter is serviced, it will gate the contents of its first sense byte with correct parity to the channel. Two more service requests will follow and three sense bytes will be transferred. After the third sense byte is accepted, the TAM adapter will initiate a termination sequence.

Full Secondary (1000 1011) - The Full Secondary command is an immediate type command that sets the secondary interface so as to accept 160 addresses. The acceptable addresses within a PAM depend on the position of the Address Selection jumpers (see PAM Addresses). This mode assignment remains until changed from 160 addresses to 80 addresses by a Half-Secondary command or a PAM reset.

Half Secondary (1001 0011) - The Half Secondary command is an immed-
iate type command that sets the secondary interface so as to accept
80 addresses.  The acceptable addresses within a PAM depend on the
position of the Address Selection jumpers (see PAM Addresses).  This
mode assignment remains until changed by a Full Secondary command.

   Test Out Line 1 (0000 1011)

   Test Out Line 2 (0001 1011)

   Test Out Line 3 (0010 0011)

   Test Out Line 4 (0010 1011)

Test Out Lines 1, 2, 3, and 4 commands are four immediate type com-
mands that initiate continuous signals on Test Out Lines 1, 2, 3
and 4 respectively.  Each line is used to cause an action at one or
more adapters, if it is in test mode, so as to test adapter logic.
It is possible to issue the four commands in sequence and activate
all four lines.  The assignment of Test Out Lines for each adapter
is shown in Table 6-1.

Test Out Line Reset (0011 0011) - Test Out Line Reset is an immediate
type of command that resets Test Out Lines 1, 2, 3, and 4.

   Reset Test Out Line 1 (1100 1011)

   Reset Test Out Line 2 (1101 1011)

   Reset Test Out Line 3 (1110 0011)

   Reset Test Out Line 4 (1110 1011)

Reset Test Out Lines 1, 2, 3 and 4 commands are four immediate type
commands that reset the individual Test Out Lines 1, 2, 3 and 4
respectively.  It is possible to issue any or all of these commands
in sequence and de-activate the Test Out Lines.

Test Out Line 1 Pulsed (0001 0011) - Test Out Line 1 Pulsed is an
immediate type of command that transmits a pulse of 15 usec duration
on Test Out Line 1.

Check Forcing Commands

There are 9 immediate types of commands that force a check in PAM
Common controls during the next cycle after the command is accepted.
Three commands force Check Stop, Tag, or Configuration check.  Six
other commands force incorrect parity during Bus Out for an address,
command or data byte, and Bus In for an address, status or data byte
respectively.

Pass Address (0011 1011) - The Pass Address command causes the PAM
to pass (ignore) the next valid address it receives during an initial
selection sequence.  This allows an IOCE to have access to an adapter
on a secondary PAM interface when an adapter on a primary PAM inter-
face is not functioning and both have the same address.

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•Table 6-1.   Test Line Usage

|  | TOL 1 | TOL 2 | TOL 3 | TOL 4 | TIL 1 | TIL 2 |
|---|---|---|---|---|---|---|
| General Purpose Input | I/O Request | Data pattern | Data pattern | Data pattern | Device gate monitor | Adapter response monitor |
| General Purpose Output | I/O Request | Test parity | Set device status bits 1,3,5,6 in sense byte | Set device status bit 7 in Sense byte | Output parity monitor | Adapter response monitor |
| Interfacility In | Clock | Not used | Simulated input data line | 17 zeros | Sync completed | Our message (SDC detected) |
| Interfacility Out | Clock | Test parity | Not used | Sync completed | Start latch set | Serial output data monitor or idle pattern |
| TTY Long Line Read | Simulated input data line | Inhibit Echo Check | Step one cycle | Simulate SDC | Sync Trigger (SOM decoded) | Start Detected |
| TTY Long Line Write | Not used | Test parity | Step one cycle | Not used | Not used | Serial output data monitor |
| RVDP | Char. Available | Data pattern | Data Pattern | Data pattern | Device Gate monitor | Character received monitor |
| IBM 1052 Read | Keyboard Strobe | Data pattern | Data pattern | Data pattern | Parity compare | Function Monitor |
| IBM 1052 Write | Service request | Not used | Not used | Not used | Output (AUX) parity monitor | Function Monitor |
| Common Digitizer | Clock | Data | EOM | SOM | Not used | Not used |
| FDEP | Step one cycle | Data | Inhibit Timeout | Not used | Receive Mode monitor | Serial output data monitor |
| BP | Oscillator | "W" Status Transfer Demand Station In | Input data, "X" Status | "Y"-"Z" Status Demand In Ready Memory Request (TOL 3&4) Not Ready, Special In | Test Out Demand Clear, Transmit Command, Serial Output Data | Demand Out Transmit RMA6 |

After one valid address is passed, the condition is cleared automatically.  An address is invalid if it is not wired for use in the PAM, not assigned to that IOCE-PAM interface, or has incorrect parity.

The Pass Address command is effective for the next valid address due to a START I/O, TEST I/O or HALT I/O instruction, but not when command chaining is indicated within a START I/O.  If chaining is indicated between receipt of the Pass Address command and the next initial selection sequence containing a valid address, the pass function will be stored in PAM until chaining is no longer indicated. At that time, the pass function will be re-activated and effective for the next valid address received.

The Pass Address command is an immediate type operation.  Channel End and Device End are set during the initial selection cycle.

Bypass Check Stop (1001 1011) - The Bypass Check Stop command results in the clearing of the Check Stop latch (and ELC if caused by Check Stop.)  It does not remove the condition which may have caused the Check Stop.  This command allows the priority and scan operation to continue if Check Stop was caused by an intermittent check condition or by the Force Check Stop command.  If Check Stop was caused by a solid check condition, it will allow the scan to continue for one cycle at which time Check Stop will again be set by the check condition.

Bypass Check Stop is an immediate type command which sets Channel End, Device End during the initial selection cycle.

Status Information

The status byte is transmitted to the channel in the following situations:

1. During initial selection.

2. At termination of any adapter command.

3. When permitted to present queued status.

4. To present the Attention Signal.

Status Byte Format

| Bit | Designation |
|-----|-------------|
| 0 | Parity |
| 1 | Attention |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bit 0 (Attention)- The Attention Status bit will be set by PAM Common malfunctions which set a bit in one of the last two sense bytes except the Address Out check sense bit. It is set when the following conditions are met:

1. Initial selection is not in progress.

2. A status byte is not being transmitted.

3. The adapter is not busy executing the sense command. (Other commands are immediate type.)

4. Command chaining is not indicated.

5. Status is not suppressed.

Status Bit 3 (Busy)- The Busy status is set when attention status is set. The Busy status is reset when the status byte is accepted by the multiplexor channel during status servicing or a Test I/O command. The adapter will not accept a command, except Test I/O and sense, when the Busy status is set.

Status Bit 4 and 5 (Channel End and Device End)- Channel End and Device End are always presented together by the Test and Monitor Adapter. They are set when the I/O operation is terminated and the adapter will present status to the channel when allowed to do so.

These bits are set on the following conditions:

1. Under the initial selection phase of all immediate type commands.

2. At the termination of a sense command.

They are reset by the acceptance of the status byte by the channel.

Status Bit 6 (Unit Check)- A Unit Check is sent during the initial selection. Cause of the Unit Check condition can be determined by executing a sense command. The unit check condition is set by:

1. Command Reject

2. Bus Out Check

Unit Check is reset by acceptance of a status byte by the channel.

Sense Information

A sense command may be executed after detection of Unit Check or Attention status. The sense register is reset at the termination of the sense command.

| Byte | Bit | Designation |
|------|-----|-------------|
| 1 | P | Parity |
|   | 0 | Command Reject |
|   | 1 | Not Used |
|   | 2 | Bus Out Check |
|   | 3 | Not Used |
|   | 4 | Not Used |
|   | 5 | Test Out Lines |
|   | 6 | Test In Line 1 |
|   | 7 | Test In Line 2 |
| 2 | P | Parity |
|   | 0 | Check Stop |
|   | 1 | Multiple Priority Response Check |
|   | 2 | Single Priority Response Check |
|   | 3 | Priority Transfer Check |
|   | 4 | Scan Check |
|   | 5 | Configuration Check |
|   | 6 | TAG Check |
|   | 7 | Not Used |
| 3 | P | Parity |
|   | 0 | Address Out Check |
|   | 1 | Command Out Check |
|   | 2 | Service Out Check |
|   | 3 | Address In Check |
|   | 4 | Status In Check |
|   | 5 | Service In Check |
|   | 6 | Out of Tolerance Check (OTC) |
|   | 7 | Not Used |

Sense Byte 1, Sense Bit 0 (Command Reject)- Command reject will be set during initial selection if command code with correct parity is other than those listed under commands.

Sense Bit 2 (Bus Out Check)- Bus out check will be set during the initial selection if incorrect parity was detected in the command byte.

Sense Bit 5 (Test Out Lines)- Test Out Lines is set when all four test out lines are active due to the issuance of the four Test Out Line commands.

Sense Bit 6 (Test In Line 1)- Test In Line 1 sets sense bit 6 to indicate adapter response to the Test Out Line commands when in test mode.

Sense Bit 7 (Test In Line 2)- Test In Line 2 sets sense bit 7 to indicate adapter response to the Test Out Line commands when in test mode.

Sense Byte 2, Sense Bit 0 (Check Stop)- Check Stop is set if a malfunction is detected in the Priority control circuitry. The four causes of a Check Stop also set unique sense bits 1, 2, 3, and 4.

Sense Bit 1 (Multiple Priority Response Check)- Multiple Priority Response Check is set if a malfunction is detected when the priority response lines are scanned such that more than one line is activated while servicing a priority request.

Sense Bit 2 (Single Priority Response Check)- Single Priority Response Check is set if a malfunction is detected such that no adapter is selected when a priority request is accepted for servicing.

Sense Bit 3 (Priority Transfer Check)- Priority Transfer Check is set if a malfunction is detected such that no adapter is selected when a priority request is accepted for servicing.

Sense Bit 4 (Scan Check)- Scan check is set if a malfunction is detected such that two successive scan pulses occur without receiving a transfer to hold pulse or vice versa.

Sense Bit 5 (Configuration Check)- Configuration Check is set if incorrect parity is detected in the Configuration Control Register.

Sense Bit 6 (TAG Check)- TAG Check is set if a malfunction is detected due to two or more tags from the multiplexor channel being active at one time.

Sense Byte 3, Sense Bit 0 (Address Out Check)- Address Out Check is set if incorrect parity is detected on Bus Out while transferring an address byte to PAM Common. It is detected when both Select Out and Address Out tags are active. The address is not accepted by PAM. This check does not set the Attention bit.

Sense Bit 1 (Command Out Check)-Command Out Check is set if in-
correct parity is detected on Bus Out while transferring a command
byte to PAM Common.  It is detected during an initial selection se-
quence between the rise of Command Out and the fall of Address In.
It causes Bus Out check to be set in sense bit 2 at the adapter.

Sense Bit 2 (Service Out Check)- Service Out Check is set if in-
correct parity is detected on Bus Out while transferring a data byte
to PAM Common.  It is detected after the rise of Service Out.  The
data byte is transmitted to the adapter with incorrect parity.

Sense Bit 3 (Address In Check)- Address In Check is set if incorrect
parity is detected on Bus In (from the adapter) while transferring an
address byte to the IOCE.  It is detected when the Address In tag is
active.  The address is transmitted to IOCE with incorrect parity.

Sense Bit 4 (Status In Check)- Status In Check is set if incorrect
parity is detected on Bus In (from the adapter) while transferring a
status byte to the IOCE.  It is detected when the Status In tag is
active.  The status byte is transmitted to the IOCE with incorrect
parity.

Sense Bit 5 (Service In Check)- Service In Check is set if incorrect
parity is detected on Bus In (from the adapter) while transferring a
data byte to the IOCE.  It is detected when the Service In tag is
active.  The data byte is transmitted to the IOCE with incorrect
parity.

Sense Bit 6 (OTC)-  Out of tolerance condition of internal PAM
temperature.

Address and Priority Assignment. Address 16, 96 or 176 will be assigned
to the Test and Monitor Adapter for the three possible settings of the
address selection jumpers.  Address changes are possible in the field.

Maintenance Panel (See Figure 6-11)

The purpose of the Maintenance Panel is to single - sequence, execute,
and repeat select and transfer cycle to manually test PAM without the
use of the IOCE and attached devices.

Switches and Indicators

Address Switches-  Eight switches set the address of the PAM Adapter
under test.

Command Switches-  Eight switches set the command code for the PAM
Adapter.

Data/SCON - IOCE Switches-  Eight switches set data bytes for the PAM
adapter or SCON and IOCE assignments with parity for the CCR.

Parity Insert Switch-  A switch which sets correct or incorrect
parity for addresses, commands or data.
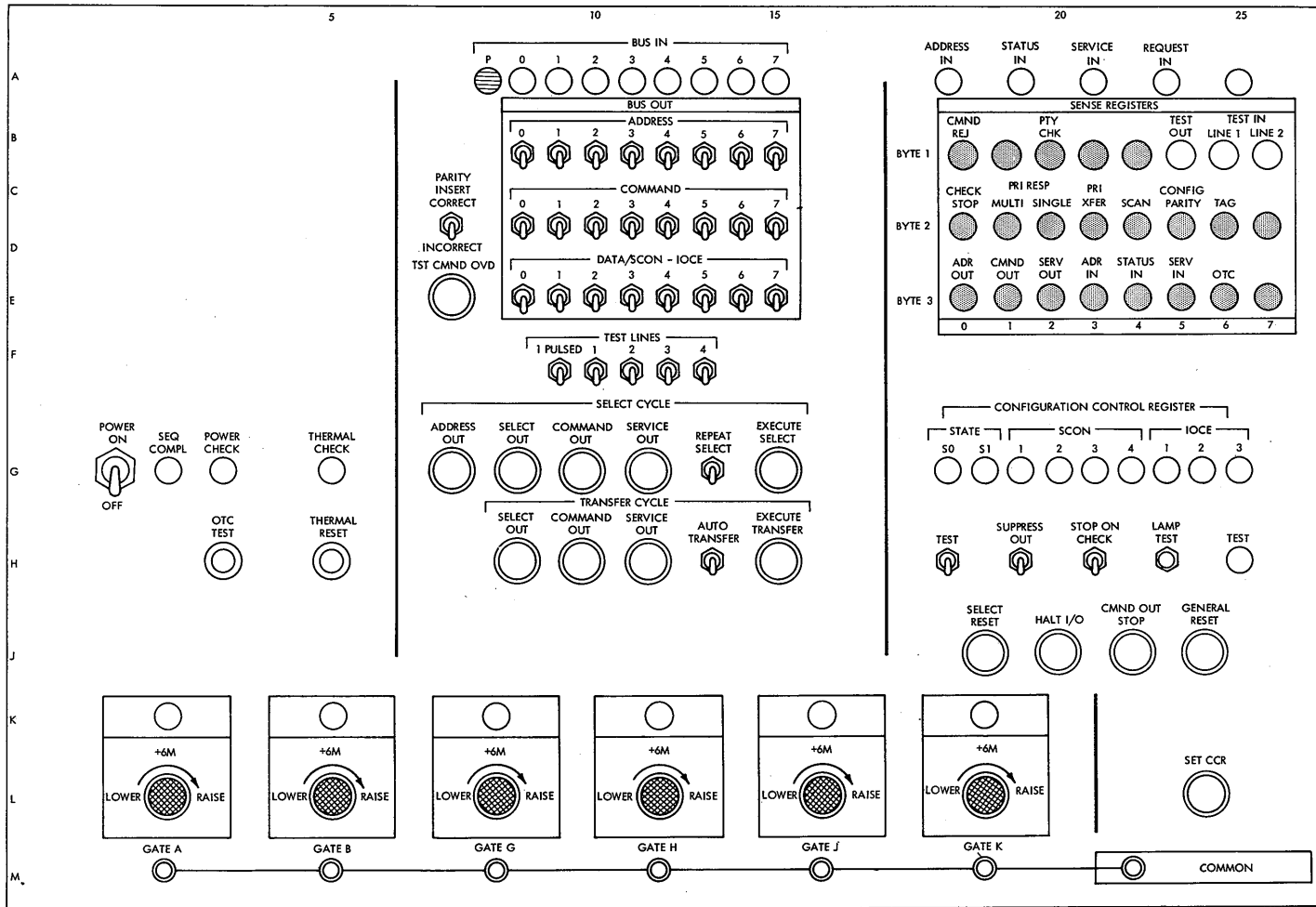
Figure 6-11.  Maintenance Test Panel

Bus In Indicators- Nine indicators present address, status or data byte with parity on Bus In as specified by three indicators below.

Address In Indicator- Indicates an Address on Bus In.

Status In Indicator- Indicates Status on Bus In.

Service In Indicator- Indicates Data on Bus In.

Sense Byte 1 Indicators (8)- Indicates Command Reject, parity check on Bus Out, Test Out (lines 1 through 4), Test In Line 1, Test In Line 2, and three spares.

Sense Byte 2 Indicators (8)- Indicates Check Stop, Multiple Priority Response Check, Single Priority Response Check, Priority Transfer Check, Scan Check, Configuration Check and Tag Check.

Sense Byte 3 Indicators (8)- Indicates Address Out Check, Command Out Check, Service Out Check, Address In Check, Status In Check, Service In Check and OTC.

Test Switch- This switch is operative (logically) only in the test state. All manual test switches are operative only when the Test Switch is in the on position or the Enable/Disable switch on the operator's panel is in the Disable position, and PAM is in State 0.

Stop On Check Switch- This switch causes PAM to stop on a malfunction.

Suppress-Out Switch- This switch if on, will suppress status from being presented by the adapter.

Selective Reset Pushbutton- This pushbutton resets selected adapter.

General Reset Pushbutton- This pushbutton resets PAM.

Configuration Control Indicators- Nine indicators which present contents of 4 SCON bits, 3 IOCE bits and 2 state bits.

Set CCR Pushbutton- This pushbutton sets the SCON and IOCE assignments from the Data/SCON-IOCE switches into the CCR.

Test Command Override PB- This pushbutton disables logic that forces Read and Write Co-mands at this test panel to occur only in Test Mode. This pushbutton is pushed in combination with Command Out, Execute, Select or Repeat Select of the Select Cycle Group.

Select Cycle/Address Out PB- This pushbutton gates the Address Switches to Bus Out.

Select Cycle/Select Out PB- This pushbutton sets scan control line for the addressed adapter.

Select Cycle/Command Out PB- This pushbutton gates the Command Switches to Bus Out.

Select Cycle/Service Out PB-  Pushbutton gates the Data Switches to Bus Out.

Select Cycle/Execute Select PB-  This pushbutton initiates a select cycle simulating action of four previous pushbuttons.

Select Cycle/Repeat Select Switch-  This switch causes a select cycle to be repeated every 15 usec from completion to start.

Transfer Cycle/Select Out PB-  This pushbutton sets scan control line for the addressed adapter.

Transfer Cycle/Command Out PB-  This pushbutton gates the Command Switches to Bus Out.

Transfer Cycle/Service Out PB-  This pushbutton gates the Data Switches to Bus Out.

Transfer Cycle/Execute Transfer PB-  This pushbutton initiates a Transfer cycle and simulates action of three previous pushbuttons.

Transfer Cycle/Auto Transfer Switch-  This switch causes a transfer cycle to occur automatically at time of Request In.

Command Out Stop PB-  This pushbutton causes the selected adapter to stop when PAM Common receives Command Out in response to Service In to the channel.

Halt I/O PB-  This pushbutton causes a halt condition at the selected adapter when PAM Common detects Address Out and Operational In are active while Select Out is down from the channel.  PAM Common is reset, except for CCR.

Power Switches and Indicators

Power On/Off Switch-  There are two Power On/Off switches in the PAM Element, one on the Operators Panel and one on the Maintenance Test Panel.  Both switches must be in the On position to turn power on. Either switch may be used to turn power off.  The Off position of this switch is interlocked such that power may not be removed from the element unless the element is in State Zero with the Test switch in Test position.

Thermal Reset Switch-  When the PAM Temperature reaches or exceeds approximately 10% below the nominal thermal protection temperature the Thermal check indicator will light.  Regardless of any change in temperature the indicator will remain on until the Thermal Reset switch is operated.  Only if the temperature is below marginal level will the indicator extinguish when the switch is operated.

When the temperature reaches the Thermal protection level the Thermal Check indicator will already be lit; at this temperature level DC power is removed from the element.  Operating the Thermal Reset switch will cause DC power to cycle up, provided the temperature

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is below the thermal protection level.  The indicator will remain lit
until such time that the temperature is approximately 10 percent below
the protection level when the Thermal Reset switch is operated.

Power Check Indicator- This indicator is lit to indicate a catastrophic
power failure has occurred, or that a normal power off situation
prevails.

Thermal Check Indicator-  The thermal check indicator will light when
the temperature is approximately 10 percent below the normal thermal
protect temperature and will remain lit until the Thermal Reset
switch is operated at a time when the marginal temperature is not
detected.

Marginal Check Controls +6M- Each of the +6M power supplies has an
external control on the panel so that the power supply voltage may be
varied.  There is a control (and power supply) associated with each
gate of PAM.

Voltmeter Selector Switch-  A single meter is provided for monitoring
the output voltage of each of the marginal checking +6M power supplies.
The Voltmeter Selector Switch is provided so that the meter will
monitor the +6M power supply desired.  The voltmeter, and Voltmeter
Selector Switch, are located in a separate panel to the left of the

Maintenance Test Panel (Figure 6-12).



MARGIN VOLTAGE SELECT

GATE H

GATE G — GATE J
GATE B — GATE K
GATE A — OFF
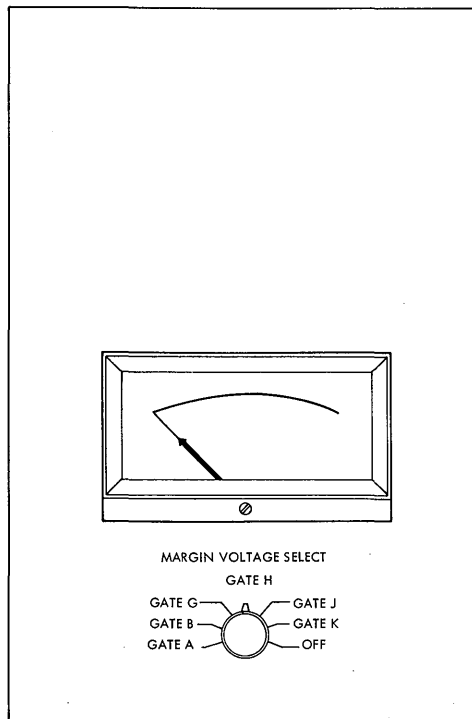
Figure 6-12.  Marginal Checking Controls

Marginal Check Indicators- Each Marginal check control (+6M) has an indicator associated with it which will light when the control is moved from its normal operating position (nominal +6 voltage). The indicator will extinguish when the associated control is returned to the normal position.

Lamp Test- Operation of this switch turns on all indicators on the Maintenance Test Panel.

Sequence Complete- This indicator will be turned on when the last DC power supply has sequenced on.

Test Indicator- This indicator will be on when the test switch is on.

Request In- This indicator will be on when an adapter receives service.

Test Lines- These switches provide a manual means to simulate the test line commands.

OTC Test- This pushbutton switch simulates a thermal warning condition, setting the OTC sense bit and Attention status bit in the TAM adapter.

"B" Gate Lamp Test- Operation of this switch (located facing the "B" Gate) turns on all indicators on all of the priority boards present in the "B" Gate.

Relay Test Panel Adapters (See Figure 6-13)
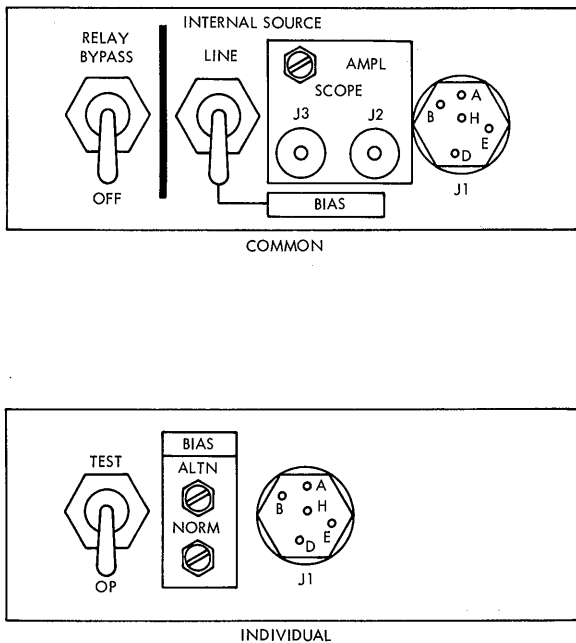




Figure 6-13. Relay Test Adapters

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The Relay Test Panel, located below the Maintenance and Test Panel provides controls which allow adapters interfacing with 62.5 ma. neutral signalling telegraph lines to be isolated from the lines for maintenance and test purposes.

There are two types of test adapters on the Relay Test Panel. The topmost panel in figure 6-13 is common to all telegraph line adapters. Its functions are as follows:

Relay Bypass Switch-  In the Bypass position, this switch removes all relays in the PAM from the lines and inserts a 91 ohm resistor in the lines.

Internal Source Switch-  In the Line position, this switch provides a fixed 62.5 ma. DC current to Output Jack J1 and to any selected (plug inserted in J1) adapter to furnish the necessary line current so that adapter relay operation may be echo checked using diagnostic programs.  In the Bias position, the switch provides a variable AC current to Jack J1 and to any selected adapter which is used to adjust read relay sensitivity (bias voltage).

Bias Amplitude Control-  This potentiometer varies the AC test current amplitude and may be observed with an oscilloscope at Jacks J2 and J3.

Test Jack J1-  This jack may be used to provide the Line or Bias current to an external point such as the PAM input connector.  In this manner, operation of the adapter through the Bypass relay may be checked.

The lower panel in Figure 6-13 shows the individual test controls provided for each adapter.  Each panel performs the following functions for its adapter.

Test/Operate Switch-  In the Test position, the adapter's relays are isolated from the line and replaced with 91 ohm resistor.

Bias Controls-  Two potentiometers, labeled Alternate and Normal, are used to adjust the bias voltage on the respective reed relays while observing their operation on an oscilloscope.

Test Jack J1 -  A special plug must be inserted into J1 for the selected adapter to enable the Line or Bias current to be applied to that adapter's relay.  The Test/Operate switch must be in the Test position before this plug is inserted.

Operators Panel (See Figure 6-14)

Element Master Power Off (Element MPO) - When this mechanically inter-locked pull switch is activated, the PAM emergency power off contactor drops.  This action removes all power in the element outside of the prime power compartment except for the 24 VDC used in the EPO circuits.
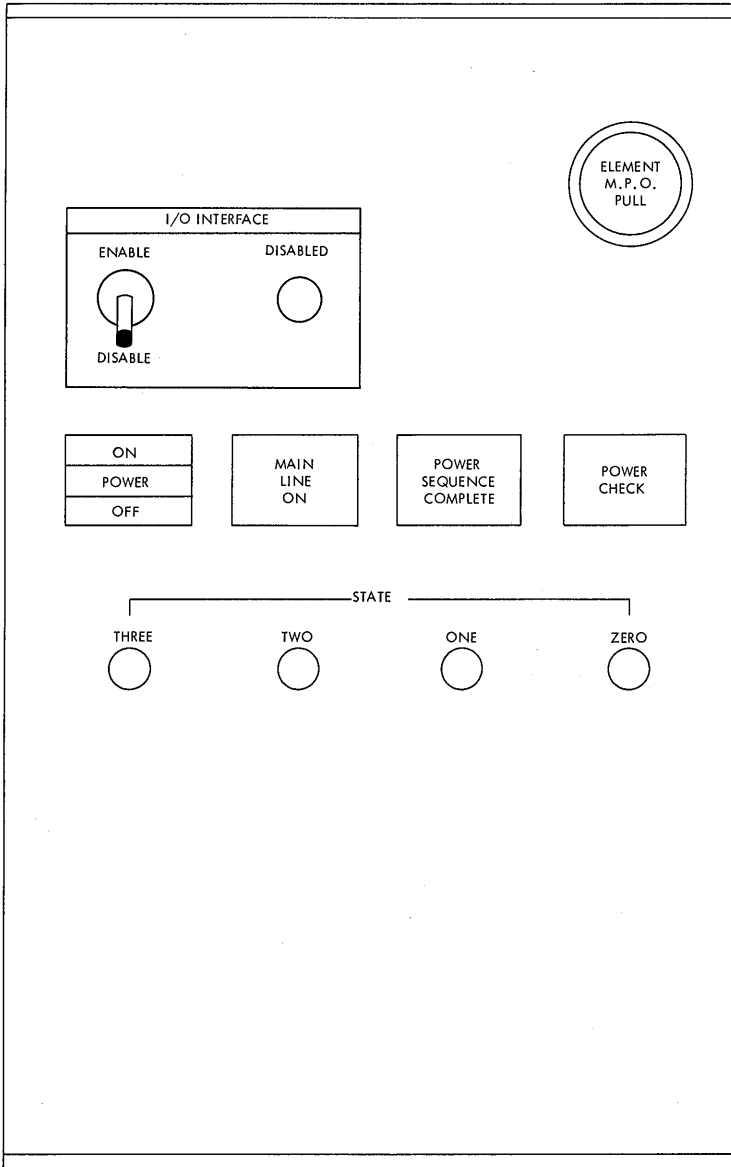
Figure 6-14.  Operators Panel

   Operation of this switch does not affect the power circuits in
any other element.  This switch, used only in an emergency, is
restored to its normal operating position, through access to the switch
mechanism behind the panel.

I/O Interface Enable - Disable Switch- This switch is used to Enable Disable the IOCE to PAM Interface without affecting other units which may be attached and operating on this same IOCE Interface. The interface can only be disabled when the switch is in the Disabled position or the Test Switch is on and the PAM is configured to State zero. (Same logical function as the test Switch on the Maintenance Test Panel).

I/O Interface Disabled Indicator- This indicator is lighted when the IOCE to PAM interface is disabled within the PAM. (Same logical function as the test light in the Maintenance Test Panel)

Power On-Off Switch- Operates as described for Maintenance Test Panel.

Main Line On Indicator- The indicator indicates the presence of prime power into the PAM element.

Sequence Complete Indicator- Operates as described for the Maintenance Test Panel.

Power Check Indicator- Operates as described for the Maintenance Test Panel.

State Indicator- One of four indicators is set to indicate PAM state, and is determined by decoding the two state bits in the CCR. States One, Two or Three are equivalent states in PAM. State Zero permits the Test switch to be placed in Test and thus unlock all manual switches at the Maintenance Test Panel.

ADAPTERS

There are nine types of adapters which interface with government furnished peripheral devices and one type of adapter for the IBM 1052 Printer Keyboard. Those I/O devices that transmit to and/or receive data from the IBM 9020D System through PAM adapters are as follows:

| | Adapter | Peripheral Device |
|---|---|---|
| 1. | General Purpose Input | Keyboard, Clock, Etc. |
| 2. | General Purpose Output | Printer, Digital Filter, Etc. |
| 3. | Interfacility Input | Lenkurt 26B Data Set/Digital Modem |
| 4. | Interfacility Output | Lenkurt 26B Data Set/Digital Modem |
| 5. | Teletypewriter - Long Line | Model 28 ASR |
| 6. | RVDP | Radar Video Data Processor |
| 7. | 1052 Printer Keyboard | 1052 Printer Keyboard |
| 8. | Common Digitizer | CD Data Receiving Group |
| 9. | FDEP | Flight Data Entry and Printout Equipment |
| 10. | BP | UNIVAC ® 1900 Buffer Processor |

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GENERAL PURPOSE INPUT ADAPTER

General Characteristics

This adapter will present a device interface to enable various devices
to send and control data transferred to the processor.  Normally the
GPI adapter will accept data in a format of 8 bits plus parity in
parallel.  The maximum data rate is determined by the 9020D system.
However, any number of bits may be used, to a maximum of 8, either
with or without parity.  The parity may be either odd or even.  In all
cases, the device will initiate the data transfer signal and will work
with the GPI adapter on a demand/response basis.  Unused data positions
will be presented to the processor as zeros.

General Description

Interfaces

The GPI adapter provides for communication between the input device
and PAM common.  The GPI communicates with PAM common over the adapter
interface and with the input device over a device interface.

Device Interface.  The device interface lines between the GPI adapter
and the device are listed below and described later.  There are 15
lines:

    8 Data In Lines
    1 Parity In Line
    1 I/O Request In Line
    1 Adapter Response Out Line
    1 EOM In Line
    3 Device Control Out Lines

Commands

The GPI adapter will decode commands from the channel and indicate the
acceptance or rejection of the command to the channel during a select
cycle.  The valid commands for the GPI adapter are as follows:

| Command | Code | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Read | 1 | M | 0 | M | M | 0 | 1 | 0 |
| Test Read Mode | M | M | 1 | M | M | 0 | 1 | 0 |

    M= Modifier bit may be 0 or 1, but bits 1, 3 and 4 cannot all be
    zero.

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Any other codes with correct parity will set sense bit 0, Command
Reject and present the Unit Check bit in the status byte in response
to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the GPI
adapter and no outstanding status conditions exist, a zero status byte
is returned to the channel. If status information is pending, all
status bits present are transmitted to the channel.

Control No-Op (0000 0011)- The control no-op command is treated as
an immediate type command. It performs no operation, and Channel End
and Device End are transmitted together during the initial selection
cycle.

Sense (0000 0100)- When the GPI adapter has accepted a sense command,
it will initiate a service request to the channel through PAM common.
When the adapter is serviced, it will gate the content of its sense
register with correct parity to the channel. When the sense byte is
accepted, the GPI will initiate a termination sequence

Read (1MOM M010)- Internally to the GPI adapter these commands work
the same; the only difference being in the output signal presented by
the three Device Control Lines to the device due to the setting of the
three modifier bits. Device Control Lines 1, 3 and 4 are set by
modifier bits 1, 3 and 4 respectively.

The modifier bit zero of this command code is set to a "one" to
condition a second gate for each output signal from the adapter to
the device. The purpose is to prevent erroneous signal from being
transmitted to the device in the event of a component failure.

When the GPI has accepted a read command, it will allow the device
to initiate a data transfer signal (I/O Request In). When the GPI has
received this signal, it will sample the input data lines and send a
response signal back to the device (Adapter Response Out). The GPI
adapter will also ask for service in via the PAM common. When the GPI
is granted service, it will place the contents of its data register
with proper parity on data Bus In. After this data has been accepted
by the channel, the GPI adapter will again allow the device to initiate
a new I/O request in. This sequence is repeated until termination is
indicated. Termination can be indicated in one of two ways:

1.  Device determines End

    After the last byte of a message has been sent to the channel,
    the device will present a termination signal (EOM In). At
    I/O Request in time, the GPI adapter will initiate a termina-
    tion sequence.

2.  Channel determines End

    When the byte count equals zero and the channel receives a
    request in from GPI adapter, the channel stops data transfer
    and signals the adapter. The adapter will then initiate a
    termination sequence.

Test Read Mode (MM1M M010)- Once the GPI adapter has accepted any of the test mode read commands, it will degate the device interface and allow the adapter to monitor and initiate a signal on the test lines to and from the Test and Monitor adapter.

Status Information

The status byte is transmitted to the channel in the following situation:

1. During initial selection.

2. At termination of any adapter command.

3. When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bit 4 and 5 (Channel End and Device End)- Channel End and Device End status are always presented together by the GPI adapter. Once set, the I/O operation will be terminated and the adapter will present status to the channel when allowed to do so.

These bits are set on the following conditions:

1. During the initial selection phase of a Control No-Op.

2. At the termination of a sense command.

3. At the termination of a read or test read mode command.

4. Upon detection of a Halt I/O condition.

The Channel End and Device End conditions are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)- Unit Check status is indicated only during an initial selection or at Channel End and Device End time of a read command. To enable the processor to obtain a more detailed picture of the cause of the Unit Check condition, a sense command should be

initiated. Unit Check is set when the following conditions are detected:

1. During an initial selection - cycle

   a. Command Reject
   b. Bus Out Check

2. At Channel End and Device End time of a read command.

   a. Data Check

The Unit Check condition is reset by acceptance of a status byte by the channel.

Sense Information- A sense command should be initiated upon detection of a Unit Check condition in the status byte. The sense register positions are reset by the acceptance of the next valid Read or Test Read Mode command. With the exception of bit 2, Bus Out Check, the sense register is also reset when Bus Out Check occurs during Command Out. When the exception of the Command Reject bit, the sense register is also reset when a Command Reject occurs.

Sense Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Not Used |
| 4 | Data Check |
| 5 | Not Used |
| 6 | Not Used |
| 7 | Not Used |

Sense Bit 0 (Command Reject)- Command reject will be set during the initial selection cycle of a command if the code with correct parity is other than those listed in the "Commands" selection of the GPI description (above). All other sense register positions are reset.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set at anytime a Bus Out Check signal is received over the adapter interface. A Bus Out Check signal will occur if PAM common detects a parity error on the Data Bus Out (from the IOCE to PAM common) and the Command Out tag is active.

A Bus Out Check detected during a select sequence will set a Unit Check bit in the status byte, the command will be ignored, and the operation is not initiated. The sense register, with the exception of Bus Out Checks, will be reset at this time.

Sense Bit 4 (Data Check)- Data Check will be set only during a read
operation when the GPI adapter detects a data byte with incorrect
parity will be corrected by the GPI adapter as the byte is transmitted
to the channel. Data Check itself will not terminate the read opera-
tion but will set a Unit Check condition during the read termination
sequence.

Priority- The priority position is address dependent, i.e., the
lower the address assigned the higher the priority. To upgrade or
downgrade the priority of a particular adapter, the address of the
adapter must be changed accordingly. The reassignment of the priority
(and address) is changeable in the field.

General Purpose Device Input Interface Description

The General Purpose Input interface provides a uniform method of
attaching input devices to a general - purpose input adapter. It
consists of a set of lines which are used to transmit information
from the input device. Each interface can accomodate one input
device.

The signal lines for the General Purpose Input interface are as
follows:

| Data Lines | Initiated By |
|---|---|
| Data In Bit Pos. P | Device |
| Data In Bit Pos. 0 | Device |
| Data In Bit Pos. 1 | Device |
| Data In Bit Pos. 2 | Device |
| Data In Bit Pos. 3 | Device |
| Data In Bit Pos. 4 | Device |
| Data In Bit Pos. 5 | Device |
| Data In Bit Pos. 6 | Device |
| Data In Bit Pos. 7 | Device |

| Control Lines | Initiated By |
|---|---|
| I/O Request In | Device |
| Adapter Response Out | Adapter |
| Device Control Line 1 Out | Adapter |
| Device Control Line 3 Out | Adapter |
| Device Control Line 4 Out | Adapter |
| EOM In | Device |

Signal Lines Description

Data In Lines (Bits 0-7)- The signal levels on these eight parallel
lines will be presented to the adapter by the device and be static
when the I/O request is detected by the adapter. The adapter is
capable of monitoring up to 8 data lines; however, the device need only
present the number of data signals applicable to the device. If less
than 8 data lines are used, then the high order positions starting
with bit 0 are not used.

Parity Line- The signal level on this line is originated by the device to establish even or odd parity for the associated data lines. System parity is odd and is preferable at the device. The signal will be Presented to the adapter and will be static when the I/O request is detected by the adapter. The device need only present this line if applicable. Odd or even assignment is jumper wired and is changeable in the field.

I/O Request In- The signal level on this line is initiated by the input device. When an active I/O request signal is detected by the adapter at a time that the adapter is selected and the adapter data register is empty, the adapter will sample the status of the data and parity lines into the adapter data register. The I/O request signal will also be used to sample the EOM line.

By controlling the frequency of the I/O request line, the device sets the data transfer rate within system limitation. The device will only make the I/O request signal inactive when the adapter response signal is detected by the device. The I/O request signal must be made inactive and then active again before the transmission of either another data character or the EOM signal is possible.

Adapter Response Out- An active signal on this line is initiated by the adapter and indicates to the device that the adapter has sampled the data, parity, and EOM lines. The adapter response signal will go inactive when the device causes the I/O request signal to go inactive. The active to inactive transition of the Adapter Response Signal could occur before the associated I/O Request signal went inactive if the channel recognized the termination sequence before the device dropped the I/O Request Signal.

Device Control Line 1 Out, Device Control Line 3 Out, Device Control Line 4 Out- The signals of these three lines will be initiated by the adapter when selected to perform a read operation. These signals will remain active until termination of the read operation. The processor will control the setting of these signals by placing a bit in modifier position 1, 3 and 4 to activate Device Control Line 1, 3 and 4 respectively.

Device Control Line 1 Out- This signal will be up when modifier bit 1 of a read command is set to a "one".

Device Control Line 3 Out- This signal will be up when modifier bit 3 of a read command is set to a "one".

Device Control Line 4 Out- This signal will be up when modifier bit 4 of a read command is set to a "one".

EOM In- A signal level on this line is initiated by the device and presented to the adapter after the transfer of the last byte of the message has been effected, I.E., the I/O request and adapter response signals transferring the last byte of the message has been brought inactive.

The signal on this line should be presented and static when the I/O request signal is detected by the adapter.

Electrical Characteristics

The signal line voltage of +3.7 volts will be used for the active state (one bit) and ground for the inactive (zero bit) state.

Timing

The timing chart for the general purpose input adapter is shown in Figure 6-15.

NOTES

GENERAL PURPOSE INPUT ADAPTER INTERFACE TIMING CHART

NOTE 1: Devices that read and respond to Device Control Out Lines should raise I/O Request In only after the detection of an active Device Control Out Line. Devices that do not use Device Control Out Lines may raise I/O Request In prior to the detection of an active Device Control Out Line.

NOTE 2: Minimum time between the fall of one I/O Request and the rise of another I/O Request is $\geq$ 2 microsecond.

NOTE 3: Minimum time between successive input bytes is 25 microseconds. This minimum time may be exceeded and is a function of the number of cycles taken by adapters with a higher priority and other 9020D System activity.

NOTE 4: The rise time measured from the 10 to 90% points of the input of the receiver at the end of 300 feet of IBM Part No. 5353912 (see Appendix B) coaxial transmission line is $\leq$ 200 nanoseconds. This time applies to circuit receivers at both the adapter end and device end of the transmission line.

NOTE 5: The fall time measured from the 10 to 90% points at the input of the receiver at the end of 300 feet of IBM Part No. 5353912 (see Appendix B) coax transmission line is $\leq$ 400 nanoseconds. This time applies to circuit receivers at both the adapter end and device end of the transmission line.

NOTE 6: Minimum time between end of one read operation and the initiation of another read operation at the device level as evidence by the fall and rise of Device Control Out lines 1, 3, or 4 is a function of the program and other 9020D System activity.

NOTE 7: The active to inactive transition of the adapter response signal could occur before the associated I/O Request signal went inactive if the channel recognized the termination sequence before the device brought the I/O Request signal inactive.

ADAPTER SELECTED
FOR DATA TRANSFER

I/O REQUEST SIGNAL GOES INACTIVE
WHEN DEVICE RECOGNIZES ACTIVE
ADAPTER RESPONSE SIGNAL.

* DEVICE CONTROL OUT LINES 1, 3, OR 4     +3.7V / 0V

NOTE 1

* I/O REQUEST IN     +3.7V / 0V

* ADAPTER RESPONSE OUT     +3.7V / 0V

DATA REGISTER LOADED

* DEVICE DATA AND PARITY LINES IN     +3.7V / 0V

LAST BYTE

* EOM IN     +3.7V / 0V

TERMINATION SEQUENCE

I/O REQUEST SIGNAL GOES ACTIVE
INDICATING ADAPTER CAN SAMPLE.
ADAPTER WILL SAMPLE AND INITIATE
MEMORY ACCESS CYCLE.

ADAPTER RESPONSE SIGNAL WILL
GO INACTIVE WHEN I/O REQUEST
SIGNAL IS DETECTED INACTIVE.

ADAPTER RESPONSE SIGNAL GOES ACTIVE
INDICATING ADAPTER HAS SAMPLED DATA
AND PARITY OR EOM LINE.

* DEVICE INTERFACE LINES

GENERAL

   a.  Transmission line is [IBM Part No. 5353912 or equivalent]
      terminated @ both ends into 100 Ω to ground.

   b.  On the line, +3.7V is a logic ONE, ground is a logic ZERO.

DRIVER

   a.  +3.7 volts @ 77 ma is required to generate a logic ONE.

   b.  200 μa or less into line is required to generate a logic
      ZERO.

RECEIVER

   a.  Receiver output provides a logic ONE for logic ONE input.

   b.  ±0.9 volt input is a logic ZERO.

   c.  +2.0 volts input is a logic ONE.

Figure 6-15. General Purpose Input Adapter Interface Timing Chart

NOTE 8:   If output signals appear on more than one Device Control Out
line, then a maximum skew in the output signals of 0.1 microseconds
can occur at the PAM connector.  Differences in cable and receiver
characteristics will increase signal skew between lines.  This note
is not applicable under present contemplated use which is to activate
only one device control line at a time.

Device to Adapter Interface Circuit Specification

The Transmission line must be terminated at each end in 100 ohms
±5 ohms to ground.  The connection between the end of the trans-
mission line and the 100 ohm line terminator shall not exceed 6
inches.  The device circuits and adapter circuits may be placed
anywhere along the transmission line; however, the connection
between the device circuit of adapter circuit signal to the
transmission line shall not exceed 6 inches.  The length of the
transmission line between the device circuit output and the device
input-output connector (external cable connector) point is limited
by the DC resistance of the transmission line and shall not exceed
two ohms.  The receiver and driver design requirements take into
account the extraneous voltages on the transmission line due to
coupled noise (±0.5 volt maximum) and attenuated ground shift
between device and adapter circuit ground.  The unattenuated
ground shift between device and adapter circuit ground shall not
exceed ±0.5 volt.

    Unattenuated ground shift is defined as that voltage which
exists between the device termination ground and the adapter termina-
tion ground.

    Attenuated ground shift is that portion of the unattenuated
ground shift which appears across the termination resistor.  It is
the ratio of the adapter resistance (100 ohms) to the total circuit
resistance (100 ohms at the adapter plus 100 ohms at the device plus
the cable resistance), times the unattenuated ground shift.

Driver Requirements

With respect to the transmission line, the driver provides a logic
zero by supplying less than 200 ua of current into or out of the line
it provides a logic one by supplying a minimum of +3.7 volts to the
line.  In order to drive the line load, 77 ma is required at +3.7
volts.  The maximum voltage the driver may present to the line is
established by the receiver's maximum allowable positive input vol-
tage of +6.24 volts.

Receiver Requirements

The receiver output shall be interpreted as presenting:  a logic one
when the receiver input is a logic one and a logic zero when the
receiver input is a logic zero, ground, or open.  The open input is
defined as retaining the 100 ohm line termination to ground at the
input to the receiver.

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The equivalent circuit of the receiver presented to the transmission line shall be 1000 ohms or greater referenced to an internal bias voltage anywhere between ±1.0 volt. The receiver must accept any voltage between ±0.9 volt as a logic zero input from the transmission line. For the logic one input, the receiver must not require an input level from the transmission line more positive than +2.0 volts, nor be damaged by an input level of +6.24 volts.

Fault Conditions

1. The signal lines may be grounded with no damage to either drivers or receivers.

2. Loss of power at either end does not cause any damage.

3. Line operation is unaffected where power is switched off in any receiver or driver.

GPI Adapter Device Interface Pin Assignments

| I/O Connector Pin | Cable-Line Name |
|---|---|
| B02 | Date Bit Pos P |
| D07 | Data Bit Pos 0 |
| B03 | Data Bit Pos 1 |
| B04 | Data Bit Pos 2 |
| D04 | Data Bit Pos 3 |
| D05 | Data Bit Pos 4 |
| B05 | Data Bit Pos 5 |
| D06 | Data Bit Pos 6 |
| B10 | Data Bit Pos 7 |
| B09 | I/O Request |
| D09 | Adapter Response |
| B08 | EOM |
| D10 | Device Control Line 4 |
| D13 | Device Control Line 3 |
| B12 | Device Control Line 1 |
| B07, B13) D02, D08) | Shields |

For signal and shield terminations, refer to Appendix B.

GENERAL PURPOSE OUTPUT ADAPTER

General Characteristics

This adapter will present a device interface to enable various
government furnished devices to receive and control data transferred
from the processor.

The GPO adapter will present data in an 8-bit plus parity (even or
odd) format on a demand/response basis where the device will initiate
the byte transfer signal.  Unused data positions are zero and appear
in the high order bits of the data byte starting with bit 0.  Maximum
data rate is determined by the 9020 system.

General Description

Interfaces

The GPO adapter provides for communication between PAM common and the
output device.  The GPO communicates with the PAM common over the
adapter interface, and with the output device over the device inter-
face.

Device Interface.  The device interface lines between the GPO adapter
and the device are listed below and described later.  There are 18
lines:

|   |   |
|---|---|
| 8 | Data Out Lines |
| 1 | Parity Out Line |
| 5 | Device Status In Lines |
| 1 | I/O Request In Line |
| 1 | Adapter Response Out Line |
| 1 | Adapter Selected Out Line |
| 1 | Adapter EOM Out Line |

Commands

The GPO adapter will decode commands from the channel and indicate
the acceptance or rejection of the command to the channel during a
select cycle.

The valid commands for the GPO adapter are as follows:

| Command | Code | | | | | | | |
|---|---|---|---|---|---|---|---|---|
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Write | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Test Write Mode | M | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

M   Modifier bit may be 0 or 1

Any other codes with correct parity will set sense bit 0, Command Reject, and present the unit check bit in the status byte in response to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the GPO adapter and no outstanding status conditions exist, a zero status byte is returned to the channel during the select cycle. If status information is pending, all status bits present are transmitted to the channel during the select cycle.

Control No-Op (0000 0011)- The control no-op command is treated as an immediate type command. It performs no operation, and channel end and device end are transmitted together during the initial selection cycle.

Sense (0000 0100)- Once the GPO adapter has accepted a sense command, it will initiate a service request to the channel through PAM Common. When the adapter is serviced, it will gate the contents of its sense register, with correct parity, to the channel. When the sense byte is accepted by the channel, the adapter will initiate a termination sequence.

Write (1000 0001)- Once the GPO adapter has accepted a write command, it will initiate a service request to the channel via PAM Common to transfer the first data byte into the adapter data register for transmission to the device. When the device has requested and accepted this data byte, another service request is initiated and the sequence is repeated until termination is indicated.

After the last byte of the message has been set into the adapter data register (in other words, the byte count equals zero at the channel) and the device has accepted the last byte, the ensuing service request from the adapter will result in a termination indication from the channel. The adapter will then initiate a termination sequence and present Channel End and Device End status.

The modifier bit zero in this command code is set to a "one" to condition a second gate for each output signal from the adapter to the device. The purpose is to prevent erroneous signals from being transmitted to the device in the event of component failures.

Test Write Mode (0010 0001) (1010 0001)- Once the GPO adapter has accepted a test write mode command, it will degate the device interface and allow the adapter to monitor and initiate signals on the test lines from/to the Test and Monitor adapter.

Status Information

The status byte is transmitted to the channel in the following situations:

    1.  During initial selection.

    2.  At the termination of any adapter command.

    3.  When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Not used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bit 4 and 5 (Channel End and Device End)- These bits are always presented together by the GPO adapter. Once set, they will block any further transmission of data or sense information and will present status to the channel when allowed to do so. They are set under the following conditions.

    1. During the initial selection phase of a Control No-Op.

    2. At the termination of a sense command.

    3. At the termination of a write or test write mode command.

    4. Upon detection of a Halt I/O condition.

The Channel End and Device End condition is reset by the acceptance of the status byte by the channel.

Status Bit 6 (Unit Check)- Unit Check status is indicated during the initial selection cycle or at Channel End Device End time. To enable the processor to obtain a more detailed picture of the cause of the Unit Check condition, a sense command should be initiated.

    Unit Check status is set when the following conditions are detected:

    1. During an initial selection cycle --

        Command Reject
        Bus Out Check

    2. At Channel End and Device End time (write termination sequence)

        Bus Out Check
        Data Check
        Device Inoperative Indication
        Device Status Line 3 Indication
        Device Status Line 5 Indication
        Device Status Line 6 Indication
        Device Status Line 7 Indication

Sense Information

General- A sense command should be initiated upon detecting a unit
check condition in the status byte. The sense register position are
reset by the acceptance of the next valid Write or Test Write Mode
Command. With the exception of bit 2, Bus Out Check, the sense
register is also reset when Bus Out Check occurs during Command Out.
With the exception of the Command Reject bit, the sense register is
also reset when a Command Reject occurs.

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Device Inoperative |
| 2 | Bus Out Check |
| 3 | Device Status Line 3 |
| 4 | Data Check |
| 5 | Device Status Line 5 |
| 6 | Device Status Line 6 |
| 7 | Device Status Line 7 |

Sense Bit 0 (Command Reject)- Command Reject will be set during the
initial selection cycle of a command if the bit configuration with
correct parity is other than those listed in the "Commands" selection
of the GPO description (above). All other sense register positions
are reset.

Sense Bit 1 (Device Inoperative)- Device sense bit 1, will be set on
two occasions:

    1.  During a Test I/O select sequence if the Device Inoperative
        Line is at a ground level.

    2.  At any time after the adapter has accepted a valid write
        command has raised the adapter Selected Out line and is not
        in the act of presenting status information to or obtaining
        data from the processor, and the Device Inoperative Line is
        at ground level.

In the event the Device Inoperative Line between the device and the
adapter is broken, a bit is set into Sense Register position 1 on the
two occasions listed above. Whenever this line is sensed and found
to be active (open or ground level) the adapter will also sense Device
Status Lines 3, 5, 6, and 7. Upon detection of a "Device Inoperative"
condition, the operation will be terminated and Unit Check presented
with Channel End and Device End status.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set at any time a
Bus Out Check signal is received over the adapter interface. A Bus
Out Check signal will occur if PAM common detects a parity error on
the data Bus Out (from the IOCE to PAM common) and the Command Out or
Service tags are active.

A Bus Out Check detected during a select sequence will set a unit check bit in the status byte and the command will be ignored. The sense register, with the exception of Bus Out Check, will be reset at this time.

A Bus Out Check detected during a Write operation (data transfer) will cause the Write operation to be terminated and the Unit Check bit set along with Channel and Device end in the ensuing status byte. The data byte in error will not be transmitted, and no further data bytes will not be transmitted, and no further data bytes will be transferred from the channel during that particular write operation.

Sense Bit 3 (Device Status Line 3)- Device Sense Bit 3 will be set if the Device Status Line 3 is active during a Write operation in the interval between the I/O request signal going inactive and the adapter response signal going inactive, or at any time that the Device Status Line 3 is active when Device Inoperative is active. The Unit Check indication is presented along with Channel End and Device End in the ensuing status byte. An active Device Status Line 3 signal detected by the GPO adapter will cause the Write operation to be terminated.

PROGRAMMING NOTE: The meaning assigned to Device Status Line 3 is a function of the device attached to the GPO adapter. This assignment could indicate parity errors detected at the device.

Sense Bit 4 (Data Check)- Data Check will be set at any time a data byte with incorrect parity is set into the GPO adapter data register. A Data Check will cause the Write operation to be terminated and the Unit Check indication will occur along with Channel End and Device End in the ensuing status byte. The data byte in error will be transmitted, and no further data bytes will be transferred from the channel during that particular write operation.

Sense Bit 5 (Device Status Line 5)- Device Sense Bit 5 will be set if the Device Status Line 5 is active during a Write operation in the interval between the I/O request signal going inactive and the adapter response signal going inactive or, at any time that the Device Status Line 5 is active when Device Inoperative is active. The Unit Check indication is presented along with Channel End and Device End in the ensuing status byte.

An active Device Status Line 5 detected by the GPO adapter will cause the write operation to be terminated.

PROGRAMMING NOTE: The meaning assigned to Device Status Line 5 is a function of the device attached to the GPO adapter.

Sense Bit 6 (Device Status Line 6)- Device Sense Bit 6 will be set if the Device Status Line 6 is active during a write operation in the interval between the I/O request signal going inactive and the adapter response signal going inactive, or at any time that the Device Status Line 6 is active when Device Inoperative is active. The Unit Check indication is presented along with Channel End and Device End in the ensuing status byte.

An active Device Status Line 6 detected by the GPO adapter will cause the write operation to be terminated.

PROGRAMMING NOTE: The meaning assigned to Device Status Line 6 is a function of the device attached to the GPO adapter.

Sense Bit 7 (Device Status Line 7)- Device Sense Bit 7 will be set if the Device Status Line 7 is active during a write operation in the interval between the I/O request signal going inactive and the adapter response signal going inactive, or at any time that the Device Status Line 7 is active when Device Inoperative is active. The Unit Check indication is present along with Channel End and Device End in the ensuing status byte.

An optional termination of the write operation is provided if an active device status line 7 is detected by the GPO adapter. This option is manually selectable in the field

If the GPO adapter is "jumper wired" not to terminate the write operation upon detection of an active Device Status Line 7, sense register position 7 is set. However, Unit Check status is not presented to the channel until status is initiated from another source (Channel End and Device End or the detection of active device status lines 1, 3, 5 or 6.

If the GPO adapter is "jumper wired" to terminate the write operation, detection of an active Device Status Line 7 will cause write operation to be terminated and Sense Bit 7 to be set.

PROGRAMMING NOTE: The meaning assigned to Device Status Line 7 is a function of the device attached to the GPO adapter.

Priority

The priority position is address dependent; i.e., the lower the address assigned the higher the priority. To upgrade or downgrade the priority of a particular adapter, the address of the adapter must be changed accordingly.

General Purpose Device Output Interface Description

The General Purpose Output interface provides a uniform method of attaching output devices to the General Purpose Output adapter. It consists of a set of lines which are used to transmit information to the output device. Each interface can accommodate one output device.

Signal Lines

The signal lines for the General Purpose Output interface are as follows:

| Data Lines | Initiated By |
|---|---|
| Data Out Bit Pos P | Adapter |
| Data Out Bit Pos 0 | Adapter |

```
Data Out Bit Pos 1                          Adapter
Data Out Bit Pos 2                          Adapter
Data Out Bit Pos 3                          Adapter
Data Out Bit Pos 4                          Adapter
Data Out Bit Pos 5                          Adapter
Data Out Bit Pos 6                          Adapter
Data Out Bit Pos 7                          Adapter

        Control Lines                       Initiated By

I/O Request In                              Device
Adapter Response Out                        Adapter
Device Inoperative In                       Device
Device Status Line 3 In                     Device
Device Status Line 5 In                     Device
Device Status Line 6 In                     Device
Device Status Line 7 In                     Device
Adapter Selected Out                        Adapter
Adapter End of Message Out                  Adapter
```

Signal Line Description

Data Out Line (Bits 0-7)- The signals on these parallel lines will be
presented by the adapter to the device and will be static when the
adapter response signal is detected by the device.

   The adapter is capable of presenting 8 data out lines to the de-
vice; however, the device need only monitor the number of lines appli-
cable to the device.

Parity Line-  The adapter originates a signal on this line to establish
odd (or even) parity to the associated data lines.  This signal level
will be presented to the output device and will be static when the
adapter response signal is detected by the device.  The device need not
monitor this line if not applicable to the device.  The odd (or even)
assignment is "jumper wired" and is easily changeable in the field.

I/O Request In-  The signal level on this line is initiated by the out-
put device.  When the I/O request signal is detected by the adapter,
and the adapter has a data byte or EOM Out signal to transfer to the
device, the adapter will initiate an adapter response signal to the
device.  When the I/O request signal goes inactive,  the adapter will
initiate the transfer of the next data byte from the processor to the
adapter data register.  By controlling the frequency of the signals on
the I/O Request Line, the device sets the data transfer rate within a
system limitation.  The device must assure that signals on device
status lines 3, 5, 6, or 7 are static for sampling when the fall of
I/O request is detected by the adapter.

Adapter Response Out-  An active signal on this line is initiated by
the adapter when the adapter has a data byte or EOM Out to transfer
to the device and the I/O request signal is active.  The adapter
response signal will go inactive after the device auses the I/O Request
signal to go inactive and the adapter has read the device status lines.

Device Inoperative- See Sense Bit 1, Device Inoperative.

Device Status Lines 3, 5, 6, and 7- These lines are monitored by the
adapter whenever the Device Inoperative Line is active (ground level
or open) or, in the absence of an active Device Inoperative signal,
between the fall of I/O Request In and the fall of Adapter Response
Out, during a Write operation. Upon detection of a signal(s) on line
3, 5, and 6, the operation is terminated. A signal on Device Status
Line 7 will not terminate the operation, but can be optionally changed
so as to terminate the operation. Device shall reset Device Status
Lines after adapter signals termination by dropping Adapter Selected
Out. This will not reset sense register bits that have been set by
Device Status Lines.

Adapter Selected Out- A signal on this line is initiated by the adap-
ter and is active whenever the adapter is selected for message transfer
(write mode). This signal, detected by the device, indicates that
the processor has a message to transmit. Under normal conditions this
signal is brought inactive during the termination sequence. If the
adapter selected signal is brought inactive without the EOM signal
having been presented to the device, the device is able to determine
that the adapter has been deselected (write Operation terminated) by
some abnormal condition. There are several abnormal conditions caus-
ing the write operation to be terminated: Bus Out Check, Data Check,
Device Inoperative, or an active Device Status In Line 3, 5, 6, or 7
(optional) detected by the adapter, a Halt I/O condition initiated by
the program, a selective reset issued by the channel, or a system reset.
This abnormal condition detected by the device could be used to enable
the device to reset and set up for a retransmission. If the EOM option
is exercised; i.e., not used by the device, the device would only be
able to recognize that the write operation was terminated; the device
may not be able to associate the fall of adapter selected with a normal
or abnormal termination.

Adapter End of Message Out- The use of the adapter EOM out signal by
the device is optional. This option is made possible by a "jumper
wire" and is easily changeable in the field.

    If this signal is used by the device, the adapter response signal,
resulting from any active I/O request from the device, is used by the
device to sample the adapter EOM signal (the data lines are not valid
when the active adapter EOM signal is sampled). The fall of the I/O
Request in that transferred the EOM signal to the device will cause
the adapter to initiate the termination of the write operation.

    If this signal is not used by the device, the fall of the I/O
Request in signal that transferred the last byte of the message will
cause the adapter to initiate the termination of the write operation.

Timing- The timing chart for the General Purpose Output Adapter is
shown in Figure 6-16.

WRITE SELECT SEQUENCE

* ADAPTER SELECTED OUT    +3.7V    0V

* DEVICE STATUS IN LINE
  (DEVICE INOPERATIVE)

TERMINATION
SEQUENCE

* ADAPTER SELECTED OUT    +3.7V    0V

* I/O REQUEST IN    +3.7V    0V

DATA REGISTER LOADED

* ADAPTER RESPONSE OUT    +3.7V    0V

SAMPLE DEVICE STATUS IN
LINES 3, 5, 6 & 7 (SEE TEXT)

SAMPLE DEVICE INOPERA-
TIVE

* DEVICE INTERFACE LINE

NOTE 5

LAST BYTE

* ADAPTOR EOM OUT    +3.7V    0V

TERMINATION SEQUENCE

TERMINATION SEQUENCE
NOTE 6

ADAPTOR SELECTED FOR
DATA TRANSFER

ADAPTOR SELECTED OUT

I/O REQUEST IN

ADAPTOR RESPONSE OUT

I/O REQUEST SIGNAL IS BROUGHT
INACTIVE BY DEVICE WHEN SAMPLE
IS COMPLETE. ADAPTOR WILL GET
THE NEXT DATA BYTE FROM THE PRO-
CESSOR. DEVICE MUST ASSURE THAT
SIGNALS ON DEVICE STATUS IN
LINES 3, 5, 6, 7 ARE STATIC SAMPL-
ING WHEN THE FALL OF I/O IS
SELECTED BY THE ADAPTER.

WHEN I/O REQUEST GOES
ACTIVE AND ADAPTOR HAS
BYTE TO TRANSFER, THE
ADAPTOR RESPONSE SIGNAL
WILL GO ACTIVE.

ACTIVE ADAPTOR RESPONSE
SIGNAL DETECTED BY OUTPUT
DEVICE INDICATES DATA AND
PARITY LINES ARE STATIC FOR
SAMPLING. DATA LINES MAY
BE CHANGING IF ADAPTOR
RESPONSE SIGNAL IS
INACTIVE.

ACTIVE RESPONSE SIGNAL
BROUGHT INACTIVE WHEN
DEVICE MAKES I/O REQUEST
INACTIVE. WHEN THE DEVICE
DETECTS THIS INACTIVE CON-
DITION, THE SIGNALS ON THE
DEVICE STATUS IN LINES 3,
5, 6, 7 MAY BE REMOVED.

* DEVICE INTERFACE LINE

GENERAL

a. Transmission line is [IBM Part No. 5353912 or equivalent]
   terminated @ both ends into 100Ω to ground.

b. On the line, +3.7V is a logic ONE, ground is a logic ZERO.

DRIVER

a. +3.7 volts @ 77 ma is required to generate a logic ONE.

b. 200 μa or less into line is required to generate a logic
   ZERO.

RECEIVER

a. Receiver output provides a logic ONE for logic ONE input.

b. ±0.9 volt input is a logic ZERO.

c. +2.0 volts input is a logic ONE.

Figure 6-16.   General Purpose Output Adapter Interface Timing Chart

NOTES

GENERAL PURPOSE OUTPUT ADAPTER INTERFACE TIMING CHART


NOTE 1. Minimum inactive time of I/O request between two sucessive data transfers is $\geq$ 2 usec.

NOTE 2. Time between rise of Adapter Selected Out (or Fall of I/O Request) until adapter data register is loaded (reloaded) is a function of the number of cycles taken by adapters with a higher priority and of other CCC activity.

NOTE 3. The rise time measured from the 10 to 90% points at the input of the receiver at the end of 300 feet of IBM Part No. 5353912 coax transmission line is < 200 nano sec. This time applies to circuit receivers at both the adapter end and device end of the transmission line.

NOTE 4. The fall time measured from the 10 to 90% points at the input of the receiver at the end of 300 feet of IBM Part No. 5353912 coax transmission line is < 400 nano sec. This time applies to circuit receivers at both the adapter end and device end of the transmission line.

NOTE 5. It is not necessary for the device to look at the Adapter Selected Out Line before raising the I/O Request Line, depending upon the type of device.

NOTE 6. If the adapter is jumper wired to operate without the device using Adapter EOM out, the termination sequence will take place as shown. Adapter Selected Out will fall at the end of the termination sequence.

NOTE 7. Minimum time between the end of one write operation and the initiation of another write operation at the level is evidenced by the fall of Adapter Selected Out and rise of another Adapter Selected Out. This interval is a function of the program and other CCC activity.

NOTE 8. Minimum time between fall of I/O Request In (when EOM out is active) and Adapter Selected Out falling is a function of the program and other CCC activity.

NOTE 9. Time between fall of I/O Request and fall of Adapter Response Out (measured at the adapter end of a 300 foot transmission line) is < 300 nano seconds.

NOTE 10. A device should make the Device Status Lines active at least 200 nanoseconds before dropping the I/O Request signal. This will assure that the signals on the Device Status lines are static for sampling when the adapter detects the fall of I/O request.

Device - Adapter Interface Circuit Specifications, General

The transmission line must be terminated at each end in 100 ohms +5 ohms to ground. The connection between the end of the transmission line and the 100 ohm line terminator shall not exceed 6 inches. The device circuits and adapter circuits may be placed anywhere along the transmission line, however, the connection between the device circuit or adapter circuit signal to the transmission line shall not exceed 6 inches. The length of the transmission line between the device circuit output and the device input-output connector (external cable connector) point is limited by the DC resistance of the transmission line and shall not exceed two ohms. The receiver and driver design requirements take into account the extraneous voltages on the transmission line due to coupled noise (+0.5 volt maximum) and attenuated ground shift between device and adapter circuit ground. The unattenuated ground shift between device and adapter circuit ground shall not exceed +0.5 volt.

Unattenuated ground shift is defined as that voltage which exists between the device termination ground and the adapter termination ground.

Attenuated ground shift is that portion of the unattenuated ground shift which appears across the termination resistor. It is the ratio of the adapter resistance (100 ohms) to the total circuit resistance (100 ohms at the adapter plus 100 ohms at the device plus the cable resistance), times the unattenuated ground shift.

Driver Requirements

With respect to the transmission line, the driver provides a logic zero by supplying less than 200 ua of current into or out of the line; it provides a logic one by supplying a minimum of +3.7 volts to the line. In order to drive the line load, 77 ma is required at +3.7 volts. The maximum voltage the driver may present to the line is established by the receiver's maximum allowable positive input voltage of +6.24 volts.

Receiver Requirements

The receiver output shall be interpreted as presenting: a logic one when the receiver input is a logic one and a logic zero when the receiver input is a logic zero, ground, or open. The open input is defined as retaining the 100 ohm line termination to ground at the input to the receiver.

The equivalent circuit of the receiver presented to the transmission line shall be 1000 ohms or greater referenced to an internal bias voltage anywhere between + 1.0 volts. The receiver must accept any voltage between +0.9 volt as a logic zero input from the transmission line. For the logic one input, the receiver must not require an input level from the transmission line more positive than +2.0 volts, nor be damaged by an input level of +6.24 volts.

Fault Conditions

1. The signal lines may be grounded with no damage to either drivers or receivers.

2. Loss of power at either end does not cause any damage.

3. Line operation is unaffected where power is switched off in any receiver or driver.

GPO Adapter Device Interface Pin Assignments

| I/O Connector Pin | Cable-Line Name |
|---|---|
| D11 | Device Inoperative |
| B12 | Device Status Line 3 |
| D12 | Device Status Line 5 |
| B11 | Device Status Line 6 |
| D13 | Device Status Line 7 |
| D10 | I/O Request |
| D07 | Adapter Selected |
| B08 | Adapter Response |
| B09 | End of Message |
| D09 | Data Bit Pos 0 |
| B03 | Data Bit Pos 1 |
| B04 | Data Bit Pos 2 |
| D04 | Data Bit Pos 3 |
| B05 | Data Bit Pos 4 |
| D05 | Data Bit Pos 5 |
| D06 | Data Bit Pos 6 |
| B10 | Data Bit Pos 7 |
| B02 | Data Bit Pos P |
| B07, B13) | |
| D02, D08) | Shields |

For signal and shield terminations refer to Appendix B

INTERFACILITY INPUT ADAPTER

General Characteristics

This adapter will meet the interface requirements of a Lenkurt 26B
data set or optionally, the Type III NAS DACOM interface requirements
of a Digital Modem.  The data set or digital modem is government
furnished.  The INTI adapter will receive data 8 bits plus odd parity
serially from a device operating at 600, 1200 or 2400 bits per second
and assemble it into an 8 bits plus odd parity byte for parallel
transfer to the processor.

General Description

Interface

The INTI adapter provides for a communications between PAM Common and
the input device.  The INTI communicates with the PAM Common over the
adapter interface, and with the input device via the device interface.

Commands

The INTI adapter will decode commands from the channel and indicate
the acceptance or rejection of the command to the channel during the
selection cycle.  The valid commands for the INTI adapter are as
follows:

| Command | Code | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Test Read Mode | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

Any other codes with correct parity are invalid and will set sense
bit 0, Command Reject, and present the Unit Check bit in the status
byte in response to the command.

Test I/O (0000 0000)-  If the test I/O command is accepted by the INTI
adapter and no outstanding status bits are present, a zero status byte
is returned to the channel.

     If status information is pending, all status bits present are
transmitted to the channel.

Control No-Op (0000 0011)-  The control no-op command is treated as an
immediate operation that performs no operation.  Channel End and Device

End are transmitted together in the status byte during initial selection cycle.

Sense (0000 0100)- Once the INTI adapter has accepted the sense command it will initiate a service request to the channel through PAM common. When the adapter is serviced, it will gate the contents of the sense register, with correct parity to the channel. When the sense byte is accepted by the channel, the adapter will initiate a termination sequence.

Read (0000 0010)-

Sync Pattern. The sync pattern recognized by the INTI adapter is seventeen zero bits (eighteen if preceded by an idle message zero) followed by a one bit. The INTI adapter will monitor the Data In line constantly for this sync pattern. When the sync pattern is detected, the next nine bits received constitute the first byte of the message. If the INTI adapter is not selected to Read by the time the byte is assembled, the sync condition is reset and the line monitoring resumes. In addition, if a nineteenth consecutive zero is sensed, the sync pattern count will be reset and will not start again until a one bit is received.

Read Mode. If the INTI adapter is selected in a read mode when the sync pattern is detected, the next assembled byte is assumed to be the station direction code (SDC). The SDC character, which need not be unique is changeable and also can be removed in the field in which case the first byte is assumed to be part of the message. Once the SDC character has been decoded properly and transmitted to the channel each byte of the message will be assembled serially (P through 7) into an 8 bit plus odd parity format. The INTI will then request service via PAM common and when service is granted the adapter will gate the contents of its data register onto data bus in. When this byte has been received by the channel the INTI adapter will allow the assembling of the next character.

Every byte assembled excluding the SDC will be checked for odd parity. If a parity error occurs, it will generate a data check and will be presented as a unit check at termination time. A parity error on the SDC character will not permit this character to be decoded as a valid SDC and the message will be ignored.

Every byte assembled including the SDC updates an 8 bit LRC register. The parity bit is not updated; only the data bits.

Every byte assembled is checked for an LRC prepare character. Once this character is detected it is sent to the channel and the next character assembled is assumbed to the LRC character. This LRC is compared with the accumulated INTI adapter LRC and the results of the compare, which appear as an exclusive OR, is sent to the channel. If the two LRC characters are identical, the results will be on all zero (except parity) LRC byte. If any bit position in the two characters differ, a "one" will appear in that bit position of the LRC byte set to the channel. An LRC error will set sense bit 7 and will be presented as a unit check at termination time. The LRC prepare character is

changeable in the field.  It must be a unique character not used else-
where in the interfacility message.

Every byte assembled is checked for an EOM character.  Once this
character is detected and sent to the channel the INTI adapter will
inititate a termination sequence.  The EOM character is changeable in
the field.  It must be a unique character not used elsewhere in the
message.  In order to prevent the receiving INTI adapter from detecting
19 consecutive zeros while monitoring for the sync pattern, the EOM
character used must have a "one" in its last bit position (bit7).

Termination occurs if the channel byte count goes to zero.  On the
next request from the adapter the channel will halt the operation and
the INTI will initiate a termination sequence

Termination occurs if a byte in the message is assembled that
contains all zeros (including the parity bit).  This is considered as
a "dead line" and the  INTI will force a termination sequence.

Test Read Mode (0010 0010)-  The test read mode command will select the
INTI adapter in test read mode.  Test mode will degate the device inter-
face and allow the adapter to monitor and initiate signals on the test
lines from/to the test and monitor adapter.

Status Information

The status byte is transmitted to the channel in the following situa-
tions:

1.  During initial selection

2.  At termination of any adapter command

3.  When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
| --- | --- |
| P | Parity |
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bits 4 and 5 (Channel End and Device End)- The Channel end and device end status bits are always presented together by the INTI adapter. Once set the adapter will terminate the I/O operation and will present status to the channel when allowed to do so. These bits are set on the following conditions:

1. During the initial selection sequence of a control no-op.

2. After the sense byte has been accepted during a sense operation.

3. At the termination of a read command.

4. Upon detection of a halt I/O condition.

Channel End and Device End status are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)- A unit check status bit is set during the initial selection or at channel end and device end time of a read command. To enable the processor to obtain a more detailed picture of the cause of the unit check condition, a sense operation should be performed.

The unit check condition is set by:

1. At initial selection

   a. Command reject
   b. Bus out check

2. At device end and channel end time of a read command

   a. Data check
   b. Overrun
   c. Longitudinal redundancy check
   d. Equipment check

Unit check condition is reset by the acceptance of the status byte by the channel.

Sense Information

A sense command should be executed when the unit check bit is set in the status byte to determine the type of equipment or programming error in the previous command. The sense register positions are reset by the acceptance of the next valid Read or Test Read Command. With the exception of bit 2 Bus Out Check, the Sense Register is also reset when Bus Out Check occurs during Command Out. With the exception of the Command Reject bit, the sense register is also reset when a Command Reject occurs.

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Equipment Check |
| 4 | Data Check |
| 5 | Overrun , |
| 6 | Not Used |
| 7 | Longitudinal Redundancy Check |

Sense Bit 0 (Command Reject)- Command reject will be set during the initial selection phase of a command if the bit configuration with correct parity is other than those listed in the "Commands" section of the INTI description. All other sense register positions are reset.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set any time a Bus Out check signal is received over the adapter interface. A Bus Out check signal will occur if PAM common detects a parity error on the Data Bus Out (from IOCE to PAM common) and the Command Out tag is active.

A Bus Out Check detected during a select sequence will set a unit check bit in the status byte and the command will be ignored. The sense register, with the exception of Bus Out Check, will be reset at this time.

Sense Bit 3 (Equipment Check)- Equipment check will be set during the read operation when during the read in a message a byte of 9 zeros is detected. Equipment check will terminate the read operation.

Sense Bit 4 (Data Check) - Data check at Device End signifies a byte parity error from the data set or digital modem. Data check does not terminate the Read operation, but sets unit check at Channel and Device End time.

Sense Bit 5 (Overrun)- Overrun indicates the adapter has begun to assemble another character before the previous character has been accepted by the channel. Overrun will terminate the read operation.

Sense Bit 7 (Longitudinal Redundancy Check) - Longitudinal Redundancy Check will be set when the Longitudinal Redundancy Count (LRC) from the data set or digital modem does not agree with the LRC generated in the adapter. LRC check does not terminate the read operation but sets Unit Check at Channel and Device End time.

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Priority

The priority position is address dependent; i.e., the lower the address code assigned, the higher the priority.  To upgrade or downgrade the priority of a particular adapter, the address of the adapter must be changed accordingly.  The reassignment of the priority (and address) is changeable in the field.

## Interfacility Input Device Interface Description

Lenkurt 26B Data Set

Signals between device and adapters shall be driven on 300 feet maximum length transmission line that has the equivalent electrical properties of IBM Part No. 5353912.  The receivers for the Data In Line and the Clock In Line will be able to operate from the device driver signal levels provided by a standard Lenkurt 26B data set which is +10 volts at the data set.  The INTI adapter receivers for the Data In Line and Clock In Line will operate from an input at PAM of +3 to +25 volts for a one bit and -3 to -25 volts for a zero bit.  The receivers present an input impedance of 1560 ohms* or greater.  No termination is added.  The rise and fall times of the Data and Clock signals will not exceed 3% of the data or clock bit interval, measured at the device driver.

Signal Line Description (Clock In Line)-  The signal on this line is initiated by the device, and is used to gate the data in line into the adapter.  This signal is presented by the device at all times at a selected frequency of 600, 1200 or 2400 cps rate without regards to data being present.

Data In Line - The signal on this line is initiated by the device, and is used to present a "one" or "zero" indication to the adapter. If no data is being transferred, the adapter will interpret an alternate one-zero bit pattern as the idle state.

Digital Modem (Type III NAS DACOM Interface)

General.  Signals between device and adapters shall operate over interchange circuit cable lengths up to 300 feet of RG-62B/U coaxial cable, IBM 5353912, or equivalent.  (Cables required will be supplied by the Government.)

The equipment shall be designed to operate with potential differences, noise impulse levels, or both, between interchange circuit network grounds, up to 0.5 volt peak of either polarity.

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*Lenkurt 26B brochure specifies 3000 ohms, however.  Lenkurt Engineers state that 1560 ohms is satisfactory.

Interface protection. The following fault conditions shall not sub-
ject interface circuitry to conditions which exceed the manufacturer's
published ratings:

(a) Interchange circuit termination: open circuited or
    short circuited.

(b) Loss of signal or power at either end of the interface
    circuit.

(c) Transient signals, noise, etc.: ±25 volts peak; steady-
    state or keyed signals.

Receivers. The INTI adapter receivers for the Data In Line and
Clock In Line will have the following characteristics:

(a) Impedance -- 5000 ohms minimum (input resistance)

(b) Binary logic amplitudes -- +0.5 volt (binary 1), -0.5 volt
    (binary 0); or -0.5 volt (binary 1), +0.5 volt (binary 0).
    Operation using either positive or negative data logic
    shall be provided by a simple wiring change.

(c) Input capacity -- 2500 picofarads maximum

(d) Sensitivity -- Minimum input circuit sensitivity shall be
    such that a positive (negative) voltage not in excess of
    0.5 volt shall cause the input circuitry to assume a
    binary "1" state, and a negative (positive) voltage not
    in excess of 0.5 volt shall cause the input circuitry to
    assume a binary "0" state. (Parenthetical references
    apply to operation with negative data logic.) The voltage
    amplitude within these limits is not specified; however,
    the positive and negative operating amplitudes shall be
    balanced to within 10 percent of each other. Maximum
    operating current required on the input interface circuit
    to assume a binary logic state shall be 100 microamperes.

(e) Rise and fall times -- Between 5% and 15% of the duration
    of the unit interval at 4800 BPS (measured between 10%
    and 90% amplitude levels).

Signal Line Description - Clock in Line. The signal on this line is
intiated by the device, and is used to gate the Data In line into the
adapter. This signal is presented by the device at all times at a
selected frequency of 600, 1200 or 2400 cps rate without regards to
data being present.

Data In Line. The signal on this line is initiated by the device,
and is used to present a "one" or "zero" indication to the adapter.
If no data is being transferred, the adapter will interpret an alter-
nate one-zero bit pattern as the idle state.

<u>Timing Diagram.</u>  The timing Diagram follows (6-17).


INTI Adapter Device Interface Pin Assignments


<u>I/O Connector Pin</u>                              <u>Cable-Line Name</u>

        B02                                      Clock Line
        B3                                       Data Line
        B07, B13⎫
        D02, D08⎭                                Shields

        For signal and shield termination refer to Appendix B.
All four shield pins must be utilized (each shield to 2 pins).

INTERFACILITY OUTPUT ADAPTER

<u>General Characteristics</u>

    1.    This adapter will meet the interface requirements of a
          Lenkurt 26B set or optionally, the Type III NAS DACOM inter-
          face requirements of a Digital Modem operating at 600, 1200
          or 2400 bits per second.  The data set or digital modem, is
          government furnished.

    2.    The INTO adapter will be used to transfer an 8-bit byte
          plus odd parity from the processor in bit serial fashion
          (P through 7) to the data set or digital modem and hence
          to a receiving facility.

<u>General Description</u>

Interfaces

The INTO adapter provides for communication between PAM Common and the
output device.  The INTO communicates with the PAM Common over the
adapter interface, and with the output device via the device interface.

Commands

The INTO adapter will decode commands from the channel and indicate the
acceptance or rejection of the command to the channel during a selec-
tion cycle.  The valid commands for the INTO adapter are as follows:


| <u>Command</u> | | <u>Code</u> | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

NOTES
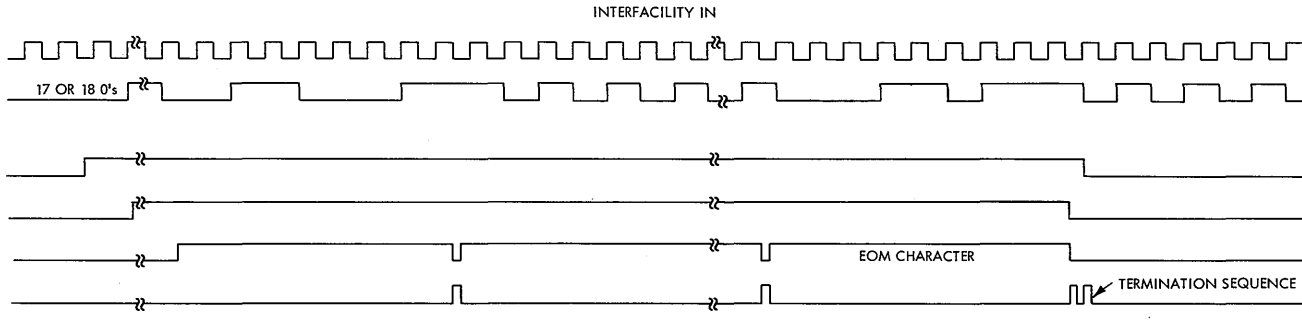
INTERFACILITY IN

*1. CLOCK

*2. DATA IN    17 OR 18 0's

ADAPTER
SELECTED

3. SYNC CODE
   DETECTED

4. ASSEMBLE
   BYTE                                    EOM CHARACTER

5. DATA BYTE                                                    TERMINATION SEQUENCE
   STORED

* DEVICE INTERFACE LINE

NOTES:

1. THE CLOCK SIGNAL, INITIATED FROM THE DEVICE RUNS
   CONTINUOUSLY AT 600, 1200, OR 2400 CPS.

2. THE LEVEL OF THE DATA LINE MUST BE STATIC FOR
   SAMPLING AT THE FALL OF THE CLOCK PULSE.

3. NO DATA WILL BE TRANSFERRED TO THE CHANNEL UNTIL
   THE SYNC CODE HAS BEEN DETECTED.

4. THE SERIAL DATA IS ASSEMBLED INTO AN 8 BIT PLUS
   PARITY BYTE

5. AFTER THE ADAPTER IS IN SYNC, DATA IS TRANSMITTED
   TO THE PROCESSOR EVERY 9 BITS.

|← 1 CYCLE →|

CLOCK

DATA        "ONE" BIT      "ZERO" BIT

DATA SAMPLE

.12 μ sec
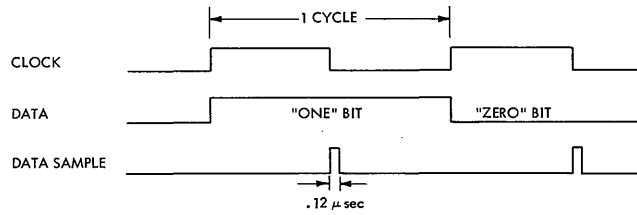
Figure 6-17.   Interfacility Input Adapter Timing Chart

|              Command              |     | Code |   |   |   |   |   |   |
|-----------------------------------|-----|-----|---|---|---|---|---|---|
|                                   | 0   | 1   | 2 | 3 | 4 | 5 | 6 | 7 |
| Sense                             | 0   | 0   | 0 | 0 | 0 | 1 | 0 | 0 |
| Write                             | 1   | 0   | 0 | 0 | 0 | 0 | 0 | 1 |
| Test Write Mode                   | M   | 0   | 1 | 0 | 0 | 0 | 0 | 1 |

M = Modifier bit may be a 0 or 1.

Any other codes with correct parity are invalid and will set sense bit 0, command reject, and present the Unit Check bit in the status byte in response to the command.

Test I/O (0000 0000)-  If the Test I/O command is accepted by the INTO Adapter and no outstanding status bits are present, a zero status byte is returned to the channel.

If status information is pending, all status bits present are transmitted to the channel.

Control No-Op (000 0011)-  The control no-op command is treated as an immediate operation.  Channel End and Device End are transmitted together in the initial selection cycle.

Sense (0000 0100)-  Once the INTO adapter has accepted a sense command, it will initiate a service request to the channel through PAM Common. When the adapter is serviced, it will gate the contents  of its sense register, with correct parity, onto the channel.  When the sense byte is accepted by the channel, the adapter will initiate a termination sequence.

Write (1000 0001)-  The sync pattern generated by the INTO adapter is seventeen zero bits followed by a one bit.  When the INTO adapter is not selected to Write, the Data Out line appears as alternate zero and one bits.  After the INTO adapter has accepted the Write command, the sync pattern is transmitted by the adapter and a request is made for the first message byte.

1.  After seventeen consecutive zeros and a one bit are transmitted, the adapter will request service via PAM Common. When service is granted it will gate the data on Bus out into its data register.  This byte will be gated out serially until all bits (8 plus odd parity) have been transmitted. When the last bit has been set, the INTO adapter will request service again for the next byte of the message.  This sequence will continue until the entire message is transmitted.

2. Every byte gated into the data register will be checked for odd parity. If a parity error occurs and is detected by the adapter or PAM Common, it will set a sense bit and present unit check status in the status byte at termination time. Correct parity will be assigned and transferred with the data byte to the device.

3. Every byte gated into the Data Register will update an 8-bit LRC register. The parity bit is not updated, only the data bits.

4. Every byte gated into the data register will be checked for a LRC Prepare character. After the LRC Prepare character has been transmitted the adapter will reques the next byte as before. This byte will be an all zero (with correct parity) byte inserted by the program. The contents of the LRC register will be transmitted to the device in lieu of the all zero character.

   If in the previous part of the message a parity error had occurred, the contents of the LRC register will be complemented before being sent. In this way, the device will be signaled of the error. The LRC Prepare character is changeable in the field. It must be a unique character not used elsewhere in the Interfacility message.

5. Every byte gated to the data register will be checked for EOM character. Once this character is detected and transmitted, the INTO adapter will initiate a termination sequence. The EOM character is changeable in the field. It must be a unique character not used elsewhere in the message. In order to prevent the receiving INTI adapter from detecting 19 consecutive zeros while monitoring for the sync pattern, the EOM character used must have a "one" in its last bit position.

6. Termination occurs if the channel byte count equals zero. Upon the next request from the adapter, the channel will halt the operation and the adapter will initiate a termination sequence.

   The modifier bit zero is set to a "one" in the command code to condition a second gate for each output signal from the adapter to the device. The purpose is to prevent erroneous signals from being transmitted to the device in the event of component failures.

Test Write Mode (M010 0001)- Either test mode command will select the INTO adapter in write-test mode. These modes will degate the device interface and allow the adapter to monitor and initiate signals on the test lines from/to the Test and Monitor Adapter.

Status Information

The status byte is transmitted to the channel in the following situations:

    1.  During initial selection.

    2.  At termination of any adapter command.

    3.  When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
| --- | --- |
| P | Parity |
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bits 4 and 5 (Channel End and Device End)- Both of these status bits are always presented together by the INTO adapter. Once set, the adapter will terminate the I/O operation and will present status to the channel when allowed to do so. They are sent under the following conditions:

    1.  During the initial selection sequence of a Control No-Op.

    2.  After the sense register has been accepted during a sense command.

    3.  At the termination of a write or a test write mode command.

    4.  Upon detection of a halt I/O condition.

The Channel End and Device End condition are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)- A Unit Check condition is set only during
the initial selection or when Channel End and Device End status is
presented to the channel.  To enable the processor to obtain a more
detailed picture of the cause of the Unit Check Condition, a Sense
operation should be performed.

    The Unit Check condition is set by:

        1.  At Initial Selection

            a.  Command reject
            b.  Bus out check

        2.  At Device End

            a.  Bus Out Check
            b.  Data Check
            c.  Overrun

The Unit Check condition is reset by the acceptance of the status byte
by the channel.

Sense Information

A sense command should be executed when the Unit Check bit is set in
the status byte to determine the type of equipment or programming
error in the previous command.  The sense register positions are reset
by the acceptance of the next valid Write or Test Write Mode command.
With the exception of bit 2, Bus Out Check, the Sense Register is also
reset when Bus Out Check occurs during Command Out.  With the exception
of the Command Reject bit, the Sense register is also reset whenever a
Command Reject occurs.

    Sense Byte Format:

| Bit | Designation |
| --- | --- |
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Not Used |
| 4 | Data Check |
| 5 | Overrun |
| 6 | Not Used |
| 7 | Not Used |

Sense Bit 0 (Command Reject)- Command Reject will be set during the initial selection phase of a command if the bit configuration with correct parity is other than those listed in the "Commands" section of the INTO description. All other Sense register positions are reset.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set at anytime a Bus Out Check signal is received over the adapter interface. A Bus Out Check signal will occur if there is a parity error on Bus Out from the channel and the Command Out or Service Out tag is active. A Bus Out Check condition detected during data transfer will not cause the Write Operation to be terminated. A Bus Out Check condition detected during a select sequence will set the Unit Check bit in the status byte and the command will be ignored. The Sense Register with the exception, of Bus Out Check will be reset at this time.

Sense Bit 4 (Data Check)- Data Check will be set during the execution phase of a write operation if the adapter detects a parity error when the data byte is set into the INTO adapter data register. The data check condition will not cause the write operation to be terminated. Correct parity will be sent to the device.

Sense Bit 5 (Overrun)- Overrun will be set upon the detection of an overrun condition. The overrun condition occurs if the adapter has not received the next data byte from the channel at the time of the next Clock in signal from the device. The overrun condition will cause the transmission of a byte consisting of nine zeros and will then terminate the Write operation.

Priority. The priority position is address dependent, i.e., the lower the address assigned within a group the higher the priority. To upgrade or downgrade the priority of a particular adapter, the address of the adapter must be changed accordingly. The reassignment of the priority (and address) is changeable in the field.

Interfacility Output Device Adapter Interface Description

Lenkurt 26B Data Set

Signals between device and adapters shall be driven on 300 feet maximum length transmission line that has the equivalent electrical properties of IBM Part No. 5353912. The receiver for the Clock In Line will be able to operate from the device driver signal levels provided by a standard Lenkurt 26B data set which is +10 volts at the data set. The input at PAM must be +3 to +25 volts for a one bit and -3 to -25 volts for zero bit. The two duplexed adapters present an input impedance of 1560 ohms* or greater. The line cannot accommodate a line termination at either end of the transmission line. The INTO adapter driver for the Data Out Line will provide +0.5volts (or more negative)to represent a zero bit and +3.0 volts (or more positive) to represent a one bit at

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*Lenkurt 26B brochure specifies 3000 ohms, however Lenkurt Engineers state that 1560 ohms is satisfactory.

300 feet into a minimum of 4600 ohms input.  The driver output into a 4600 ohms load at the adapter is -1.24 volts for a zero bit and +3.3 volts for a one bit in the worst case where power has failed at the unselected adapter and all components are at worst purchase tolerance. The rise and fall times of the Clock In signal will not exceed 3% of the clock bit interval at the driver.  The driver for the Data Out Line will provide a signal whose rise and fall times will not exceed 25 microseconds at the device receiver.

Data Out Line-  The signal on this line is initiated by the adapter and will present a "one" bit or a "zero" bit indication to the device. The INTO adapter will use the active Clock in signal from the device to gate the data to the device.  If no data is being transferred, the adapter will transmit to the device an alternate one and zero pattern. Each pair of duplexed INTO adapters (one in each of two PAM's) is interconnected by a pair of Adapter Interlock Lines.  These lines perform the following functions:

    1.  If neither adapter is selected for service, both adapters will transmit the alternate one-zero pattern in sync.

    2.  If one adapter becomes selected, the non-selected adapter will stop transmitting the one-zero pattern.

Clock in Line-  The signal on this line is initiated by the device and occurs at a 600, 1200 or 2400 cps rate; it is used to gate the data signal onto the Data Out Line.

    This signal is presented to the adapter without regard to the adapter being ready to transfer data.

Digital Modem (Type III NAS DACOM Interface)

General.  Signals between device and adapters shall operate over inter-change circuit cable lengths up to 300 feet of RG-62B/U coaxial cable, IBM 5353912, or equivalent.  (Cables required will be supplied by the Government)

    The equipment shall be designed to operate with potential dif-ferences, noise impulse levels, or both, between interchange circuit network grounds of the terminal equipment and external equipment grounds, up to .5 volt peak of either polarity.

Interface protection.  The following fault conditions shall not sub-ject interface circuitry to conditions which exceed the manufacturer's published ratings:

    (a)  Interchange circuit termination - open circuited or short circuited.

    (b)  Loss of signal or power at either end of the interface circuit.

(c)   Transient signals, noise, etc. - ±25 volts peak;
      steady-state or keyed signals.

Clock Input Characteristics.

(a)   Impedance - 5000 ohms minimum (input resistance)

(b)   Binary logic amplitudes - +0.5 volt (binary 1),
      -0.5 volt (binary 0); or -0.5 volt (binary 1),
      +0.5 volt (binary 0).  Operation using either positive
      or negative data logic shall be provided by a simple
      wiring change.

(c)   Input capacity - 2500 picofarads maximum

(d)   Sensitivity - Minimum input circuit sensitivity shall
      be such that a positive (negative) voltage not in excess
      of 0.5 volt shall cause the input circuitry to assume a
      binary "1" state, and a negative (positive) voltage not
      in excess of 0.5 volt shall cause the input circuitry to
      assume a binary "0" state.  (Parenthetical references
      apply to operation with negative data logic.)  The voltage
      amplitude within these limits is not specified; however,
      the positive and negative operating amplitudes shall be
      balanced to within 10 percent of each other.  Maximum
      operating current required on the input interface circuit
      to assume a binary logic state shall be 100 microampers.

(e)   Rise and fall times - Between 5% and 15% of the duration of
      the unit interval at 4800 BPS (measured between 10% and
      90% amplitude levels).

Data Output Characteristics.

(a)   Source Impedance - 100 ohms maximum; short circuit current
      delivered to interface shall not exceed 100 MA.

(b)   Binary logic amplitudes - Open circuit voltage shall be
      positive and negative 6 ± 1 volts, balanced within 10%
      of each other; +6 volts (binary 1), -6 volts (binary 0);
      or -6 volts (binary 1), +6 volts (binary 0).  Operation
      using either positive or negative data logic shall be
      provided by a simple wiring change.

(c)   Rise and fall times - Between 5% and 15% of the duration of
      the unit interval at 4800 BPS (measured between 10% and
      90% amplitude levels).

(d)   Data jitter - 3% maximum of the duration of the unit
      interval (measured from the 50% level of the negative-
      going clock transition to average zero voltage level of
      the data unit interval)

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Data Out Line. The signal on this line is initiated by the adapter and will present a "one" bit or a "zero" bit indication to the device. The INTO adapter will use the active Clock In signal from the device to gate the data to the device. If no data is being transferred, the adapter will transmit to the device an alternate one and zero pattern. Each pair of duplexed INTO adapters (one in each of two PAM's) is interconnected by a pair of Adapter Interlock lines. These lines perform the following functions:

1. If neither adapter is selected for service, the adapter farthest from the device will transmit the alternate one-zero pattern.

2. If one adapter becomes selected, the selected adapter will assume control of the data line.

Clock In Line. The signal on this line is initiated by the device and occurs at a 600, 1200 or 2400 cps rate; it is used to gate the signal onto the Data Out Line.

This signal is presented to the adapter without regard to the adapter being ready to transfer data.

Timing. The Timing diagram follows Figure 6-18.

INTO Adapter Device Interface Pin Assignments

| I/O Connector Pin | Cable-Line Name |
|---|---|
| B02 | Clock Line |
| B03 | Data Line |
| B07, B13 D02, D08 | Shields |
| *B04 | Adapter Interlock In |
| *B05 | Adapter Interlock Out |

*PAM to PAM cables only

For signal and shield terminations refer to Appendix B. All four shield pins must be utilized (each shield to 2 pins).

TELETYPEWRITER, HALF-DUPLEX, LONG LINE ADAPTER

General Characteristics

This adapter will present, under processor control, serial information to a Teletype Corporation Model 28 ASR device (or equivalent) or receive serial information from similar devices for transfer to the processor. Each charter is transmitted using 7.42 Baudot start/stop transmission code.

INTERFACILITY OUT

*1. CLOCK

*2. DATA OUT

17 ZEROS

NOTE 5 |←— SYNC —→|

NOTE 5

ADAPTER
SELECTED

3. DATA BYTE
FETCH

EOM CHARACTER

4. TERMINATION
SEQUENCE

*DEVICE INTERFACE LINE

NOTES:

1. THE CLOCK SIGNAL, INITIATED FROM THE DEVICE RUNS CONTINUOUSLY
AT 600, 1200, OR 2400 CPS.

2. THE LEVEL OF THE DATA LINE IS STATIC FOR SAMPLING AT THE FALL OF
THE CLOCK PULSE.

3. AN 8-BIT PLUS PARITY BYTE IS FETCHED FROM THE PROCESSOR AND IS
DISASSEMBLED FOR SERIAL TRANSMISSION TO THE DEVICE

4. AFTER TRANSMITTING AN EOM CHARACTER THE ADAPTER INITIATES A
TERMINATION SEQUENCE.

5. ALTERNATE ONE-ZERO PATTERN MAY TERMINATE WITH A ONE OR
ZERO (SEE TEXT)

|←— 1 CYCLE —→|

CLOCK

DATA            "ONE" BIT    "ZERO" BIT
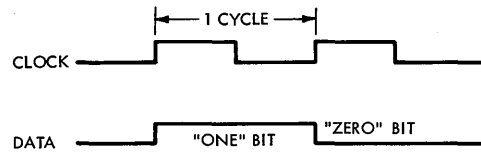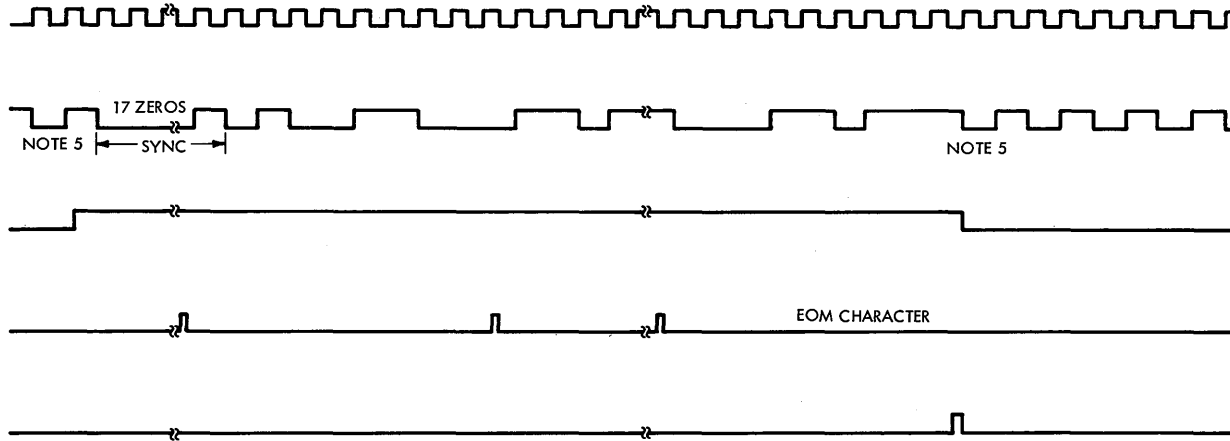
Figure 6-18.   Interfacility Output Adapter Timing Chart

Data Byte Format

The data byte format is as follows:

| Bit | Function |
|-----|----------|
| P | Parity |
| 0 | End of Message |
| 1 | LRC Insert |
| 2 | Figures or Letters Indication |
| 3 | Character data bit 1* |
| 4 | Character data bit 2* |
| 5 | Character data bit 3* |
| 6 | Character data bit 4* |
| 7 | Character data bit 5* |

* Order of transmission/receipt


Message Format

The message format may include a 13-character SOM sequence at the
beginning of each message preceding the information fields.  The
13-character SOM sequence will consist of the following groups in the
order listed:

    EOM (3 characters)-  Line Feed, Carriage Return and Letters
    Filler (1 character) - Letters
    Conditioning Code (3 characters)- Carriage Return, Carriage
    Return, Letters
    Station Directing Code (3 characters)- Selectable
    Sync Code (3 characters)- Letters, Carriage Return, and Line
    Feed

    On an input message, the adapter will recognize the 3 character
Station Directing Code for the assigned site.  The recognition of the
three characters will permit all characters received thereafter to be
transferred to the computer.

    A predetermined "LRC Insert" indication consisting of 2 characters
(Carriage Return, Letters) will be used to enable the receiving facil-
ity to detect the LRC character.

    The complete LRC sequence is as follows:

|  |  |
|--|--|
| Carriage Return | NOTE:  This document describes the |
| Letters | 5 character sequence.  A sixth |
| Inserted LRC character | character (Letters) may be option- |
| Carriage Return | ally used after LRC or Line Feed. |
| Line Feed | Adapter Operation is unaffected. |

LRC generation will begin with the character following Line Feed.  The
two character sequence, Carriage Return, Line Feed, following the in-
serted LRC character (also used in the sync code) resets the LRC
register.

A predetermined 3-character EOM sequence will be inserted by the program to enable the receiving facility to recognize the End of Message. The EOM sequence will consist of Line Feed, Carriage Return, and letters.

General Description

Commands

The TTYLL adapter will decode commands from the channel and indicate the acceptance or rejection of the command to the channel during a select cycle. Valid commands for the TTYLL adapter are as follows:

| Command | Code | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Write Normal | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Write Alternate | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Read Normal | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Read Alternate | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Test Write Mode, Normal | M | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Test Write Mode, Alternate | M | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Test Read Mode, Normal | M | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| Test Read Mode, Alternate | M | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

M=Modifier may be 0 or 1

Any other codes with correct parity will set sense bit zero, command reject, and present the unit check bit in the status byte in response to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the TTYLL adapter and no outstanding status conditions exist, a zero status byte is returned to the channel during the select cycle. If status information is pending, all status bits present are transmitted to the channel during the select cycle.

Control No-Op (0000 0011)-  The Control No-Op command is treated as
an immediate type command.  It performs no operation and Channel End
and Device End status are transmitted together during the initial
selection cycle.

Sense (0000 0100)-  Once the TTYLL adapter has accepted a sense command
it will initiate a service request to the channel through PAM common.
When the adapter is serviced, it will gate the contents of its sense
register, with correct parity, to the channel.  When the sense byte is
accepted by the channel, the adapter will initiate a termination
sequence.

Write Normal (1000 0001), Write Alternate (1001 0001)-  There are two
sets of relays associated with each TTYLL adapter; a "normal" and an
alternate" set.  The selection of either set is under control of the
command.  Following the selection of the "normal" set of relays, the
alternate transmit relay will be continuously energized (contacts open)
thereby allowing line currect to flow through the "normal" set of
relays only.  Similarly, after selection of the "alternate" set, the
"normal" transmit relay is continuously energized (contacts open) and
not used for data transmission.  The relays remain in the last selected
mode, except when power is brought up, in which case the relay may come
up in either mode.

    The modifier bit zero in this command code is set to one to con-
dition a second gate for the output signal from the adapter to the
write relay.  The purpose is to prevent an erroneous signal from pick-
ing the write relay in the event of component failures.

    Once the TTYLL adapter has accepted a write command, it will
initiate a service request, to the channel via PAM common, for the
first data byte.  The write operation as performed by the TTYLL adapter
is as follows:

        1.  Each data byte is set into the data register and checked
            for correct parity.  A data byte with a parity error will
            be transmitted to the device and the adapter upon detec-
            tion of at least one parity  error in the information
            field (between successive LRC character transmissions)
            will invert the ensuing LRC character before transmission.

        2.  Each byte transferred to the adapter, except the
            13-character SOM sequence and the last 3 characters of
            the LRC sequence, will update a 5-bit LRC register.

        3.  The 5-bit data byte is clocked out to the device under
            control of a crystal oscillator set at 100 words per
            minute.

PROGRAMMING NOTE:  The 13-character SOM code preceding a teletype
message will be inserted by the program.

        4.  The adapter will monitor bit position 2 in each byte for
            a change from the preceding byte.  If a change from a

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zero to one is detected, the adapter will automatically transmit a figures character to the device, followed by the data character (in position 3-7 on the same byte). A change detected from one to zero will cause a letter character to be transmitted followed by the data character.

5. The adapter will monitor bit position 1 in each byte received from the processor for an "LRC Insert" indication. The presence of this bit will cause the adapter to insert the contents of the LRC register as a character onto the line and reset the LRC register. The LRC feature may be bypassed by insertion of jumper wires in the TTYLL adapter. If the feature is bypassed, the adapter will not recognize the LRC insert indication and will not generate an LRC character.

PROGRAMMING NOTE: The program must insert an all zero byte in the character position to be replaced by the adapter generator LRC character. This character should be the third character of the LRC sequence.

6. There is no limit to the number of LRC sequence used in a single message.

7. When the channel byte counter goes to zero or the End of the Message indication is received, the adapter will initiate a termination sequence. The adapter will monitor bit position 0 in each byte received form the processor for an End of Message indication. This occurs on the third character of an EOM sequence. In the event the 0 bit is not set then the TTYLL adapter will request the next byte. When the channel byte counter goes to zero, the channel will respond with a stop indication setting up the termination sequence of the write operation.

Read Normal (1000 0010), Read Alternate (1001 0010)- There are two sets of relays associated with each TTYLL adapter; "normal" and an "alternate" set. The selection of either set is under control of the command. Following the selection of the "normal" set of relays, the alternate transmit relay will be continuously energized (contacts open) thereby allowing line current to flow through the "normal" set of relays only. Similarly, after selection of the "alternate" set; the normal transmit relay is continuously energized (contacts open) and not used for data transmission. The relays remain in the last selected mode, except when power is brought up, in which case the relays may come up in either mode.

Upon acceptance of a Read command, the TTYLL adapter will monitor the device line for data. The Read operation is performed by the TTYLL adapter as follows:

1. The TTYLL adapter will not transfer any data to the channel until the 3 character SDC code has been recognized in proper sequence.

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2. After the above has been recognized, the adapter will transfer the following message bytes to the channel. Each byte assembled after recognition of the last two Sync Code characters will update a 5-bit LRC register. The adapter will assign correct parity to data bytes before transmission to the channel.

3. After the SDC sequence is detected, the TTYLL adapter will monitor for the first two characters of a 5-character "LRC Sequence" indication. These two characters, detected in sequence, will be transferred to the channel, and will force an LRC compare between the accumulated LRC character and the transmitted LRC character. The Letters Character following Carriage Return does not affect the setting of bit 2.

   The result of the comparison which appears as an "exclusive or" of the two LRC characters, will be inserted in the 3rd character of the LRC sequence for later anlysis by the program.

   A one bit will be placed in position 1 of the byte containing the results of the compare as a flag to the program.

   An LRC compare error will cause a Unit Check in the status byte of the termination sequence, and will set a bit in sense position 7. If the LRC feature is bypassed in the adapter, the adapter will not recognize the Carriage Return, Letters sequence as LRC insert and will not perform an LRC count of incoming data.

4. The LRC count starts again with the first character after the Carriage Return, Line Feed sequence.

5. The adapter will monitor each byte assembled for a "Figures" or Letters" character. A "Figures" detection will cause bit position 2 to be set with a "one" bit. The adapter will insert a bit inposition 2 in each character transferred to the channel thereafter until a Letters indication is received. The ensuing bytes after this indication will have bit position 2 equal to a "zero" bit until detection of a Figures character reverses the indication. Whenever Letters or Figures encountered in the text, they do not get transferred to the channel. The Letters character in the LRC and EOM sequence will not affect the setting of bit position 2. Instead the Letters character itself will be sent to the channel.

6. The adapter will monitor bytes received for a predetermined 3 character EOM sequence.

After the last character of the EOM sequence is detected and transmitted to the channel the TTYLL adapter will terminate the Read Operation.

Test Write Mode (M01M0001)- The Test Write Mode command will degate the interface and allow the adapter to monitor and initiate signals on the test lines to/from the test and monitor adapter.

Test Read Mode (M01M0010)- The Test Read Mode command will degate the device interface and allow the adapter to monitor and initiate signals on the test lines to/from the test and monitor adapter.

Status Information

The status byte is transmitted to the channel in the following situations:

1. During initial selection

2. At the termination of any adapter command.

3. When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
|---|---|
| P | Parity |
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bit 4 and 5 (Channel End and Device End)- These bits are always presented together by the TTYLL adapter. Once set, they will terminate the I/O operation and will present status to the channel when when allowed to do so. These bits are set on the following conditions:

1. Initial selection cycle of a Control No-Op

2. After the sense byte has been stored during a sense operation

3. At the termination of a read, write, or test mode command

4. Upon detection of a Halt I/O condition

Channel End and Device End status are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)- Unit Check status is indicated during the initial selection cycle or at Channel End and Device End time. To enable the processor to obtain a more detailed picture of the cause of the unit check condition, a sense operation should be performed. Unit Check status is set by:

    1.  During an initial selection cycle:

        a.  Command Reject
        b.  Bus Out Check

    2.  At Channel End and Device End time (termination of an adapter command)

        a.  Data Check
        b.  Overrun
        c.  Longitudinal Redundancy Check
        d.  Bus Out Check
        e.  Echo Check Normal
        f.  Echo Check Alternate

Unit Check status is reset by the acceptance of a status byte by the channel.

Sense Information

A sense command should be initiated upon detecting a unit check condition in the status byte. The sense register positions are reset by the acceptance of the next valid Read, Write, or Test Mode Command. With the exctption of Bit 2, Bus Out Check, the Sense Register is also reset when Bus Out Check occurs during Command Out. With the exception of the Command Reject bit, the sense register is also reset when a Command Reject occurs.

    Sense Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Echo Check Normal |
| 4 | Data Check |
| 5 | Overrun |
| 6 | Echo Check Alternate |
| 7 | Longitudinal Redundancy Check |

Sense Bit 0 (Command Reject)- Command Reject will be set during the
initial selection cycle of a command if the bit configuration with
correct parity is other than those listed in the "Commands" section
of the TTYLL description.  All other sense register position are reset.

Sense Bit 2 ( Bus Out Check)-  Bus Out check will be set at any time
a Bus Out check signal is received over the adapter interface.  A
Bus Out check signal will occur if PAM common detects a parity error
on the data bus out (from IOCE to PAM common) and the command out
(write or read mode) or service out (write mode) tags are active.

   A Bus Out Check detected during a select sequence will set a
unit check bit in the status byte and the command will be ignored.
The Sense Register, with the exception of Bus Out Check, will be
reset at this time.

   A Bus Out Check detected during a write operation (data transfer)
will not cause the write operation to be terminated.  The byte in
error will be transmitted, and a Unit Check bit will occur in the
status byte presented to the channel in the EOM termination cycle.
The ensuing LRC character will be inverted prior to transmission.

Sense Bit 3 (Echo Check Normal)-  Echo Check Normal will be set during
a write operation when the normal write relay is being used to key the
line and the write echo is not correct.  The Echo Check Normal condi-
tion will occur during a read or write operation when using the normal
path and the following conditions arise on a bit by bit check:

   1.  Marking or open line while writing

   2.  Failure of the read relay detected while writing

   3.  Open line while reading

   4.  Marking line while reading (must occur after Start bit is
       detected)

   5.  Conflict (line is being used to receive and write simultan-
       eously).

Echo Check Normal will cause the read or write operation to be termin-
ated.

Sense Bit 4 (Data Check)-  Sense register position 4, Data Check, will
be set at any time a data byte with incorrect parity is set into the
TTYLL adapter data register (write mode).  A data check detected during
a write operation (data transfer) will not cause the write operation
to be terminated.  The byte in error will be transmitted, and a Unit
Check will occur in the status byte presented to the channel in the
EOM termination cycle.  The ensuing LRC character will be inverted
prior to transmission.

Sense Bit 5 (Overrun)-  Overrun will be set during the execution of a
write operation if the adapter does not receive data from the channel

by the time the start bit must be transmitted. No character is trans-
mitted. Overrun will be set on a Read operation if the first data bit
of the next data byte is received before the preceding data byte is
transferred. Overrun will cause the read or write command to be ter-
minated.

Sense Bit 6 (Echo Check Alternate)- Echo Check Alternate will be set
during a write operation when the alternate write relay is being used
to key the line and the write echo is not correct. The Echo Check
Alternate condition will occur during a read or write operation when
using the alternate path and the following conditions arise on a bit
by bit check:

 1. Marking or open line while writing.

 2. Failure of the read relay detected while writing.

 3. Open line while reading.

 4. Marking line while reading must occur after Start Bit is
    detected.

 5. Conflict (line is being used to receive and write simultan-
    eously).

Echo Check Alternate will cause the read or write operation to be
terminated.

Sense Bit 7 (Longitudinal Redundancy Check)- LRC Check will be set
during the execution of a read operation if the adapter detects a
Longitudinal Redundancy Check (LRC) check on an input message. LRC
check will not terminate the read operation.

Priority

The priority position is address dependent, i.e., the lower the address
the higher the priority. To upgrade or downgrade the priority of a
particular adapter, the address of the adapter must be changed accord-
ingly. The reassignment of the priority (and address) is changeable
in the field.

Interface

The receive and transmit relays are housed in the PAM unit. These
relays are mercury wetted relays manufactured by C. P. Clare Co.,
assembly number HGS 4Y 1042. The resistance seen by the line, is
91 ohms ±10%; these coils operate with a nominal current of 62.5 ma,
and have a 2 msec. pick and drop time. A constant current is applied
to the receive relay bias winding. A potentiometer in series with the
bias winding is preadjusted for proper output response of the receive
relay.

TTYLL Adapter Device Interface Pin Assignment are:

| I/O Connector Pin | Cable-Line Name |
|---|---|
| A | Device Line |
| B | Device Line Return |
| H | Cable Shield |

Distortion Definitions:

Normal Bit Period (NBP) - non-distorted bit length as determined by a specified bit rate of 100 wpm.

Normal Character Start - The start of a normal character is referenced to the transition from a stop bit or idle status to a start bit.

Receive Distortion Tolerance - Using the transition from the stop bit or idle status to the start bit, the start bit must be no shorten than 60% of the normal bit period. Any succeeding bit of the character may be shortened by 40% from the leading edge and 40% from the trailing edge of a normal bit location in a normal character. A normal character with a zero time reference at the start bit transition is shown below (Fig. 6-19) where shaded areas show the amount of distortion that can be tolerated.

Transmit Distortion - The transmit distortion will not exceed ±5%.
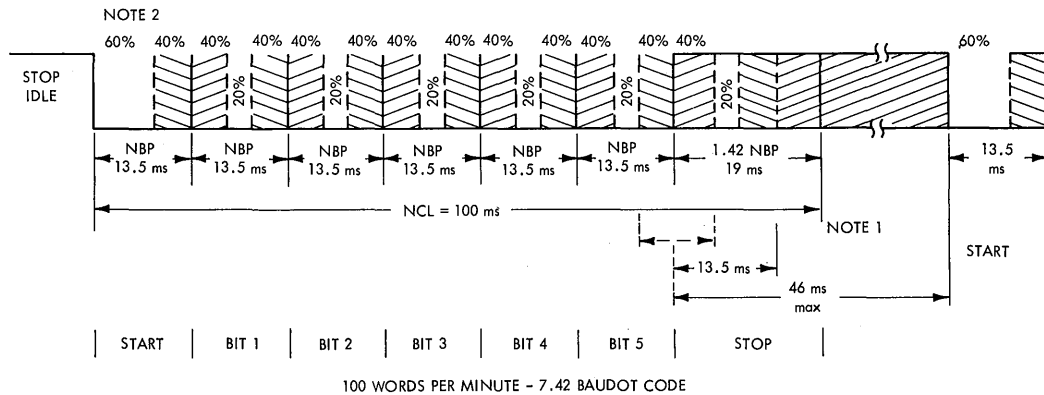


NOTE 1   START TRANSITION MAY OCCUR BETWEEN 13.5 ms AND 46 ms AFTER STOP TRANSITION. OCCURRENCE BEFORE 13.5 ms WILL RESULT IN LOSS OF SYNC. OCCURRENCE AFTER 46 ms WILL RESULT IN "MARKING LINE WHILE READING" CHECK.

NOTE 2   ALL % FIGURES RELATE TO NORMAL BIT PERIOD (13.5 ms).

Figure 6-19.   Normal Character with Zero Time Reference

Timing

The timing charts for the teletypewriter adapter are shown in Figures 6-20 and 6-21.

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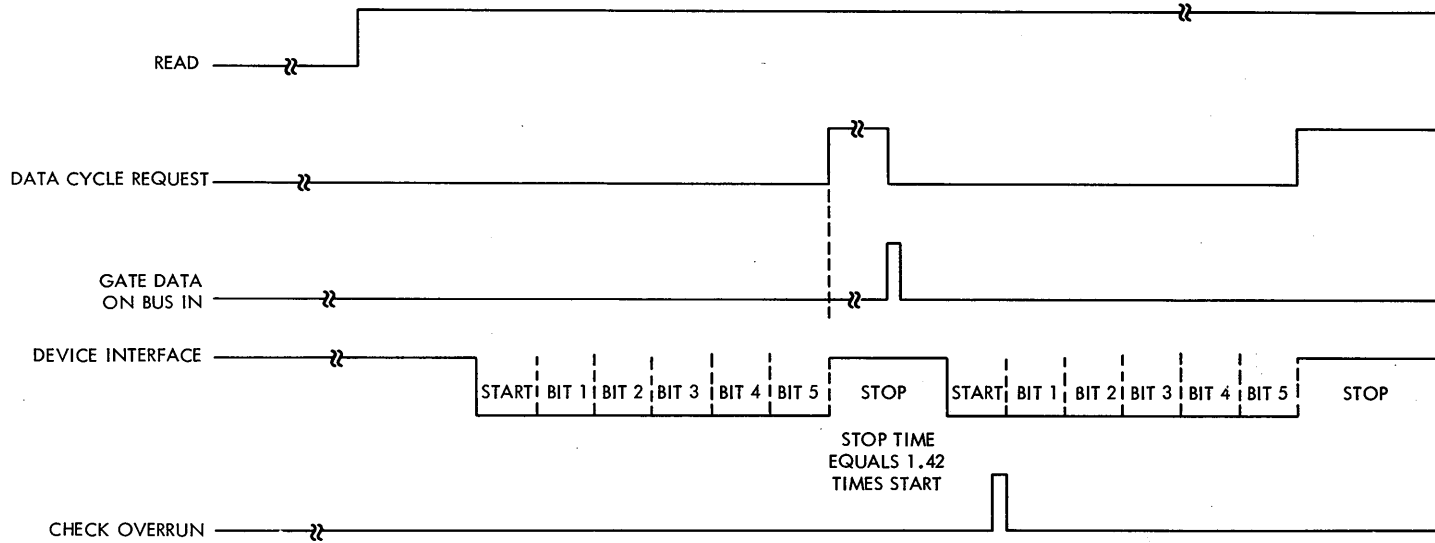
Figure 6-20.  TTYLL Timing Diagram for Read Operation
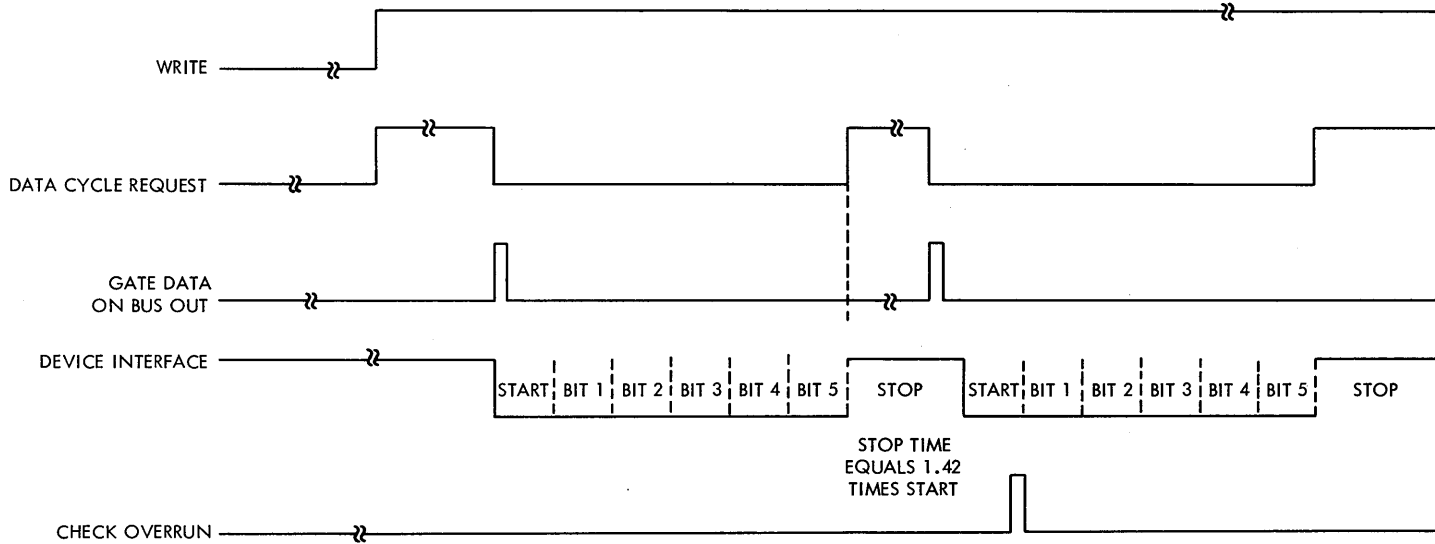


Figure 6-21.  TTYLL Timing Diagram for Write Operation

Interface Circuit Schematic

See Figure 6-22

RADAR VIDEO DATA PROCESSOR ADAPTER (RVDP)

General Characteristics

This adapter will meet the interface requirements of a Burroughs
RVDP.

The RVDP adapter will accept data in a format of 6 bits plus
odd parity in parallel at an equivalent serial rate of 2400 or 7200
bits per second within system limitations. The device will initiate
the data transfer signal and will work with RVDP adapter on a demand/
response basis.

General Description

The RVDP adapter provides for communication between the input device
and PAM common. The RVDP communicates with PAM common over the adapter
interface, and with the input device over the device interface.

Device Interface

The device interface lines between the RVDP adapter and the device
are listed below and described later. There are 11 lines.

                6   Data In Lines
                1   Parity in Line
                1   Character Available Line
                1   Character Received Line
                1   EOM In Line
                1   SOM In Line

NOTE: The "Map Message" line from the device is not monitored by the
RVDP adapter.

Commands

The RVDP adapter will decode commands from the channel and indicate
the acceptance or rejection of the command to the channel during a
select cycle. The valid commands for the RVDP are as follows:

| Command | | Code | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Read | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Test Read Mode | | M | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
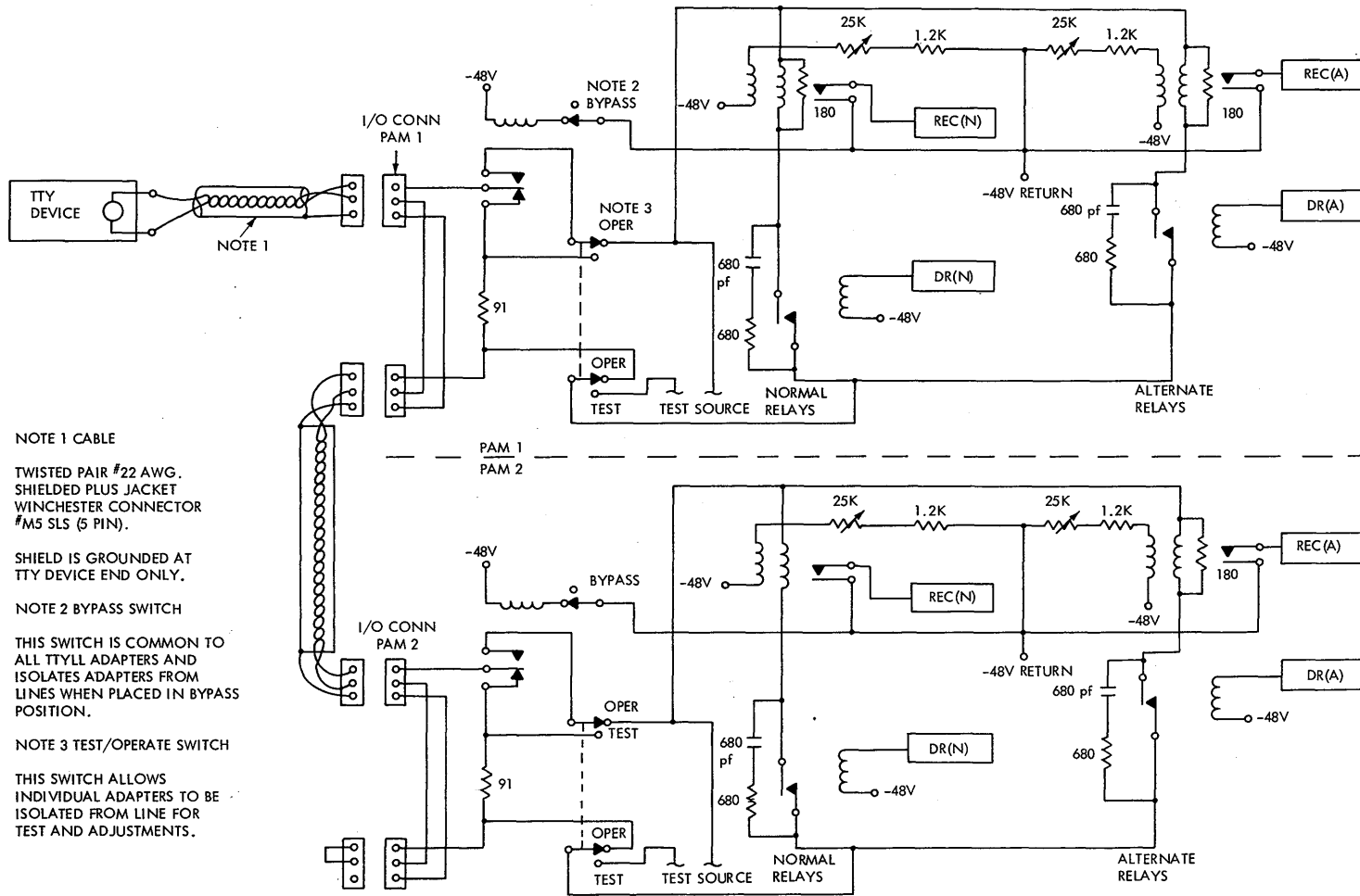
M=Modifier bit may be 0 or 1.

NOTE 1 CABLE

TWISTED PAIR #22 AWG.
SHIELDED PLUS JACKET
WINCHESTER CONNECTOR
#M5 SLS (5 PIN).

SHIELD IS GROUNDED AT
TTY DEVICE END ONLY.

NOTE 2 BYPASS SWITCH

THIS SWITCH IS COMMON TO
ALL TTYLL ADAPTERS AND
ISOLATES ADAPTERS FROM
LINES WHEN PLACED IN BYPASS
POSITION.

NOTE 3 TEST/OPERATE SWITCH

THIS SWITCH ALLOWS
INDIVIDUAL ADAPTERS TO BE
ISOLATED FROM LINE FOR
TEST AND ADJUSTMENTS.

Figure 6-22.   TTYLL Interface Circuit Schematic

Any other codes with correct parity are invalid and will set sense bit 0, command reject and present the Unit Check bit in the status byte in response to the command.

Test I/O (0000 0000)- If the test I/O command is accepted by the RVDP adapter and no outstanding status condition exists, a zero status byte is returned to the channel. If status information is pending all status bits present are transmitted to the channel.

Control No-Op (0000 0011)- The control no-op command is treated as an immediate type command. It performs no operation and channel end and device end are transmitted together during the initial selection cycle.

Sense (0000 0100)- Once the RVDP adapter has accepted a Sense command, it will initiate a service request to the channel through PAM common. When the adapter is serviced, it will gate the contents of its semse register with correct parity to the channel. When the sense byte is accepted, the RVDP adapter will initiate a termination sequence.

Read (1000 0010)- Once the RVDP adapter has accepted a Read command it will sample the Character Available line and the Start of Message (SOM) line. When the SOM is detected, the RVDP adapter will sample and input data lines and send Character Received back to the device. The RVDP adapter will also ask for "service in" via the PAM common. When the RVDP is granted service, it will place the contents of its data register onto Data In Bus Position 2-7. (if incorrect parity was detected from the device, a bit is placed in position 1 of the byte in error.) When this data has been accepted by the channel the RVDP adapter will look for a new "Character Available" signal.

This sequence is repeated until termination or EOM from the device is indicated. When an EOM signal is detected by the RVDP adapter it will sample the data lines as above and when the byte is sent to the channel a bit will be placed in position 0. A new SOM signal must be presented to the adapter before any more data will be accepted. Termination of the Read operation will occur if the RVDP adapter detects an indication that the byte count equals zero after requesting "service in" from the channel.

PROGRAMMING NOTE: Termination is indicated as a result of the next service request (generated from the RVDP adapter to the channel) after channel byte count has gone to zero. However, due to the free-running characteristics of the input and the nature of the data being transmitted, a Channel End condition initiated by the adapter when byte count equals zero should not normally occur. The program should use data chaining and the information obtained through use of the SET PCI instruction to allocate memory buffer areas and to monitor the progress of data transfers.

The modifier bit zero is set to a "one" in the command code to condition a second gate for each output signal from the adapter to the device. The purpose is to prevent erroneous signals from being transmitted to the device in the event of component failures.

Test Read Mode (0010 0010) (1010 0010)- Once the RVDP adapter has accepted either of the test read mode commands, it will degate the device interface and allow the adapter to monitor and initiate signals on the test lines to and from the Test and Monitor adapter.

Status Information

The status byte is transmitted to the channel in the following situations:

1. During initial selection

2. At termination of any adapter command

3. When permitted to present queued status.

Status Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Not Used |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

Status Bit 4 and 5 (Channel End and Device End)- These bits are always presented together by the RVDP adapter. Once set the adapter will terminate the I/O operation and will present status to the channel when allowed to do so. Those bits are set on the following conditions:

1. During the initial selection sequence of a control no-op

2. After the sense byte has been accepted during a sense operation.

3. At the termination of a read or test read mode command.

4. Upon detection of a halt I/O condition.

Channel End and Device status are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)- A Unit Check status can be indicated only during an initial selection. To enable the processor to obtain a more detailed picture of the cause of the unit check condition, a sense command should be initiated. Unit Check is set when the following condition is detected.

1. Command Reject

2. Bus Out Check

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Unit Check is reset by the acceptance of a status byte by the channel.

Sense Information

A sense command should be initiated upon detecting the Unit Check bit in the status byte. The sense register positions are reset by the acceptance of the next valid Read or Test Read Mode command. With the exception of bit 2, Bus Out Check, the Sense Register is also reset when Bus Out Check occurs during Command Out. With the exception of the Command Reject bit, the Sense register is also reset when a Command Reject occurs.

Sense Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Not Used |
| 4 | Not Used |
| 5 | Not Used |
| 6 | Not Used |
| 7 | Not Used |

Sense Bit 0 (Command Reject)- Command Reject will be set during the initial selection phase of a command if the code with correct parity is other than those listed in the "Commands" section of the RVDP description. All other Sense register positions are reset.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set at anytime a bus out check signal is received over the adapter interface. A Bus Out Check signal will occur if PAM Common detects a parity error on the Data Bus out (from the IOCE to PAM Common) and the Command Out tag is active.

A Bus Out Check detected during a select sequence will set a unit check bit in the status byte and the command will be ignored. The sense register, with the exception of Bus Out Check, will be reset at this time.

Priority

The priority position is address dependent, i.e., the lower the address assigned the higher the priority. To upgrade or downgrade the priority of a particular adapter, the address of the adapter must be changed accordingly. The re-assignment of the priority and address is changeable in the field.

RVDP Device Interface Description

the RVDP interface provides a uniform method of attaching Radar Video Data Processor inputs to a RVDP adapter. It consists of a set of lines which are used to transmit information from the input device. The interface can accommodate one input device.

Signal Lines

The signal lines for the RVDP interface are as follows:

| Data Lines | Initiated By |
| --- | --- |
| Data in Bit Position P | Device |
| Data in Bit Position 2 | Device |
| Data in Bit Position 3 | Device |
| Data in Bit Position 4 | Device |
| Data in Bit Position 5 | Device |
| Data in Bit Position 6 | Device |
| Data in Bit Position 7 | Device |

| Control Lines | Initiated By |
| --- | --- |
| Character Available | Device |
| Character Received | Adapter |
| SOM In | Device |
| EOM In | Device |

Signal Lines Description

Data In Bit Position 2 to 7- The signal on these parallel lines will be presented to the adapter by the device, and will be static when the Character Available signal is detected by the adapter.

The adapter is capable of monitoring up to 6 data lines. The 6 data lines will be placed in positions 2 - 7 of Data in Bus during data transfer.

NOTE: Data In positions 2-7 are considered to be the device data lines position 2 being the most significant and position 7 being the least significant.

Data in Bit Position P- The signal on this line is originated by the device to establish odd parity to the associated data lines. The signal will be presented to the adapter and will be static when the Character Available signal is detected by the adapter.

SOM In- The signal on this line is initiated by the device. When the SOM signal is detected by the adapter, and the adapter has been previously selected by a read command, it will allow the RVDP adapter to accept the message. Data will be accepted until the adapter detects an EOM In signal from the device

Character Available- The signal on this line is intiated by the input device. When an active Character Available signal is detected by the adapter, and the adapter has received SOM either with this byte or a previous one, and the adapter data register is empty, the adapter will sample the status of the data and parity lines into the adapter data register. The Character Available will also be used to cause the sample of the EOM line.

By controlling the frequency of the signals of the Character
Available line, the device sets the data transfer rate within system
limitation.  The Character Available signal must be made inactive
and then active again before the transmission of another data byte.

Character Received- An active signal on this line is initiated by the
adapter and indicates to the device that the adapter has sampled the
data, parity, SOM and EOM lines.  The character Received signal will
go inactive when the device causes the Character Available signal to
to inactive.  The RVDP adapter will not initiate a signal on the
Character Received line unless the adapter is selected and a signal
has been received on the SOM In line, with the first byte.

EOM In-  A signal on this line is initiated by the device and presented
to the adapter at the same time as the last byte of the message.  The
signal on this line should be presented and static when the Character
Available signal is detected by the adapter.  A bit will be placed in
Position 0 of Bus In when the data byte is transferred to the channel.

Electrical Characteristics

There are two basic interface conditions which must be met by the
RVDP adapter.  The first is where information from the device driver
is transmitted over a transmission line to the adapter receiver.  The
second condition is where the adapter driver transmits information to
the device receiver over  a transmission line.  The positive signal
voltage on the transmission line will be used for the logic one and
ground for the logic zero state.

Timing.  The timing chart for the RVDP adapter is shown in Figure 6-23.

Transmission Line and Termination. The transmission lines used between
device and adapters will be DS100485 and will be terminated as started
below.  The maximum total length of transmission line shall be 300
feet.  The stub lingth between the transmission line and any receiver
or driver shall not exceed 6 inches.

Adapter Driver Output Characteristics.  Characteristics of the Adapter
Driver's Output Logic One and Logic Zero signals are described below:

    Logic One Signal.  The voltage output signal at the RVDP is +2.44
    volts (minimum) to +5.0 volts (maximum) when terminated into 2,100
    ohms (maximum load) in parallel with 50 ohms +5% terminating re-
    sistance at the receiver (RVDP) end of 300 feet of line, and 50
    ohms +5% at the most remote driver end of the line.

    Logic Zero Signal. The voltage output signal at the RVDP is +0.5
    volts (minimum) to -0.5 volts (maximum) when terminated as des-
    cribed for a logic one signal.

Adapter Receiver Input Characteristics.  Characteristics of the Adapter
Receiver Input Logic One and Logic Zero signals are described below:

    Logic One Signal.  The voltage input signal at the adapter is
    +1.48 volts (minimun) to +6.5 volts (maximum).  The receiver

RVDP ADAPTER SELECTED BY PROCESSOR

CHARACTER AVAILABLE +3V 0V

DATA LINES STATIC FOR SAMPLING +3V 0V — 1ST BYTE OF MSG 139 OR 417 μ SEC — ANY BYTE EXCEPT 1ST BYTE OF MSG

CHARACTER RECEIVED +3V 0V

SOM +3V 0V

RVDP ADAPTER SELECTED BY PROCESSOR +3V 0V

CHARACTER AVAILABLE +3V 0V

DATA LINES STATIC FOR SAMPLING +3V 0V — 1ST BYTE OF MSG — 2ND BYTE OF MSG — LAST BYTE OF MSG — 1ST BYTE OF MSG

CHARACTER RECEIVED +3V 0V

SOM +3V 0V

EOM +3V 0V

NOTE 1: IF THE RVDP ADAPTER IS NOT SELECTED FOR DATA TRANSFER BY THE PROCESSOR, A CHARACTER RECEIVED SIGNAL IS NOT INITIATED BY THE ADAPTER. NO DATA IS TRANSFERRED TO THE PROCESSOR

NOTE 2: IF THE RVDP ADAPTER IS SELECTED FOR DATA TRANSFER, AND A START OF MESSAGE INDICATION HAS NOT BEEN DETECTED BY THE ADAPTER, THEN A CHARACTER RECEIVED SIGNAL IS NOT INITIATED BY THE ADAPTER. NO DATA IS TRANSFERRED TO THE PROCESSOR.

NOTE 3: IF THE SYSTEM LIMITATIONS ARE APPROACHED WITH RESPECT TO COMBINED DATA TRANSFER RATE OR A CONDITION DEVELOPS WITHIN THE SYSTEM THAT PREVENTS DATA TRANSFER, THE CHARACTER RECEIVED SIGNAL IS DELAYED OR NOT SENT AT ALL. THIS CONDITION ENABLES THE DEVICE TO DETECT AN ALARM CONDITION

NOTE 4: WHEN OPERATING AT 7200 BITS PER SECOND, THE DATA LINES ARE STATIC FOR SAMPLING FOR 1/7200 SECONDS; AT 2400 BITS PER SECOND, THE DATA LINES ARE STATIC FOR 1/2400 SECONDS. THE TIME INTERVAL BETWEEN 2 SUCCESSIVE DATA SAMPLE TIMES IS 6/7200 OR 6/2400 SECONDS

Figure 6-23. RVDP Adapter Interface Timing Chart

presents an impedance to the transmission line of greater than
100K ohms. The Character Available line is terminated at the most
remote receiver end into 50 ohms +5% (to ground). The Data, SOM
and EOM lines are terminated at the most remote receiver end into
100 ohms +5% to ground.

Logic Zero Signal. The voltage input signal at the adapter is
+0.72 volts (minimum) to -2.37 volts (maximum). The receiver
presents an impedance to the transmission line of greater than
3.7K ohms, and is terminated as described for a logic one signal.

The rise and fall times fo the signals at the device will not exceed
25 nanoseconds as measured across the terminals of a 50 ohm resistive
load.

### RVDP Adapter Device Interface Pin Assignments

| I/O Connector Pin | Cable-Line Name |
| --- | --- |
| *B02 | Data Bit Pos P |
| B03 | Data Bit Pos 3 |
| B04 | Data Bit Pos 4 |
| B05 | Data Bit Pos 7 |
| *B08 and D07 | Character Available |
| B09 | SOM |
| B10 | Data Bit Pos 2 |
| D04 | Data Bit Pos 5 |
| D05 | Data Bit Pos 6 |
| D06 | EOM |
| *D09 and D10 | Character Received |
| B07,B13,D02,D08 | Shields |

*In order to provide proper impendance matching, the Character Avail-
able line must be connected to pins B08 and D07, and the Character
Received line must be connected to pins D09 and D10 at the PAM input
end of the device cable.

For signal and shield terminations refer to Appendix B.

1052 PRINTER KEYBOARD ADAPTER

The 1052 Adapter provides the Interfacing and control functions for
attachment of a 1052 Printer Keyboard to System 9020D. The Adapter,
via the PAM Common, communicates with an IOCE. The 1052 Adapter
recognizes the 8 bit plus parity Extended Binary Coded Decimal Inter-
change (EBCDI) shown in Figure 6-24 when communicating with the PAM.

The 1052 Model 7 Printer Keyboard basically provides the follow-
ing functions:

1. Facilities through which the operator can enter data. The
keyboard generates an internal 6 bit plus parity code
(PT&T) to communicate with the 1052 adapter. The keyboard

| BITS 4567 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 | BITS 0123 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 |  |  |  |  | SPACE | & x | - x |  |  |  |  |  |  |  |  | 0 x | |
| 0001 |  |  |  |  |  | / |  |  | a x | j |  |  | A | J x |  | 1 | |
| 0010 |  |  |  |  |  |  |  |  | b x | k | s |  | B | K x | S x | 2 | |
| 0011 |  |  |  |  |  |  |  |  | c | l x | t x |  | C x | L | T | 3 x | |
| 0100 |  |  |  |  |  |  |  |  | d x | m | u |  | D | M x | U x | 4 | |
| 0101 | HT x | NL | LF |  |  |  |  |  | e | n x | v x |  | E x | N | V | 5 x | |
| 0110 |  | BS |  |  |  |  |  |  | f | o x | w x |  | F x | O | W | 6 x | |
| 0111 |  |  |  |  |  |  |  |  | g x | p | x |  | G | P x | X x | 7 | |
| 1000 |  |  |  |  |  |  |  |  | h x | q | y |  | H | Q x | Y x | 8 | |
| 1001 |  |  |  |  |  |  |  |  | i | r x | z x |  | I x | R | Z | 9 x | |
| 1010 |  |  |  |  | ¢ | ! x |  | : |  |  |  |  |  |  |  |  | |
| 1011 |  |  |  |  | . x | $ | , | # x |  |  |  |  |  |  |  |  | |
| 1100 |  |  |  |  | < | * x | % x | @ |  |  |  |  |  |  |  |  | |
| 1101 |  |  |  |  | ( x | ) | — | ' x |  |  |  |  |  |  |  |  | |
| 1110 |  |  |  |  | + x | ; | > | = x |  |  |  |  |  |  |  |  | |
| 1111 |  |  |  |  | | | ¬ x | ? x | " |  |  |  |  |  |  |  |  | |

HT = HORIZONTAL TAB
NL = NEW LINE (CAR.RET, LINE FEED)

LF = LINE FEED
BS = BACKSPACE

Figure 6-24. Extended Binary Coded Decimal Interchange

is capable of generating 88 distinct graphic and alphanumeric characters plus 7 control functions to the adapter, as shown in Figure 6-25.

2. Facilities for printing data. The printer is a modified Selectric print mechanism which recognizes a 6 bit plus parity Tilt-Rotate (T/R) code and seven individual control lines. The printer is capable of recognizing 88 printable graphic and alphanumeric characters, as shown in Figure 6-26.

3. There is no mechanical or direct electrical connection between printer and keyboard. All communication is via the 1052 adapter.

BIT POSITIONS ⟶ S

| 8421 | \| 0 \| BA = 00 | 01 | 10 | 11 | \| 1 \| 00 | 01 | 10 | 11 |
|------|------|------|------|------|------|------|------|------|
| 0000 | SP x | @ | - | & x | SP x | ¢ | — | + x |
| 0001 | 1 | / x | j x | a | = | ? x | J x | A |
| 0010 | 2 | s x | k x | b | < | S x | K x | B |
| 0011 | 3 x | t | l | c x | ; x | T | L | C x |
| 0100 | 4 | u x | m x | d | : | U x | M x | D |
| 0101 | 5 x | v | n | e x | % x | V | N | E x |
| 0110 | 6 x | w | o | f x | ' x | W | O | F x |
| 0111 | 7 | x x | p x | g | > x | X x | P x | G |
| 1000 | 8 | y x | q x | h | * | Y x | Q x | H |
| 1001 | 9 x | z | r | i x | ( x | Z | R | I x |
| 1010 | 0 x | NA | NA | NA x | ) x | NA | NA | NA x |
| 1011 | # | , x | $ x | . | " | \| x | ! x | ¬ |
| 1100 | NSNP x | NSNP | NSNP | NSNP x | NSNP x | NSNP | NSNP | NSNP x |
| 1101 | NSNP | LF x | CR x | HT | NSNP | LF x | CR x | HT |
| 1110 | NSNP | NSNP x | BS x | NSNP | NSNP | NSNP x | BS x | NSNP |
| 1111 | NSNP x | NSNP | NSNP | NSNP x | NSNP x | NSNP | NSNP | NSNP x |

S = CASE  (0 = LOWER CASE, 1 = UPPER CASE)
LF = LINE FEED
CR = CARRIER RETURN
HT = HORIZONTAL TAB
BS = BACKSPACE
SP = SPACE
NA = NOT AVAILABLE FROM KEYBOARD
NSNP = NEITHER SPACE NOR PRINT

x = PARITY BIT IS 1

Figure 6-25.  PT and T Code

TILT MAGNETS

UPPER CASE

| ( | < | ) | * | ' | \| | + | ¬ | ; | " | = |
|---|---|---|---|---|---|---|---|---|---|---|
| x |   |   | x | x |   | x | x |   |   | x |
| — | T | V | X | Y | ? | S | U | W | Z | : |
|   | x | x |   |   | x |   |   | x | x |   |
| J | L | N | P | Q | > | K | M | O | R | ! |
|   | x | x |   |   | x |   |   | x | x |   |
| A | C | E | G | H | % | B | D | F | I | ¢ |
| x |   |   | x | x |   | x | x |   |   | x |

| $T_1$ | $T_2$ |
|---|---|
| 1 | 1 |
| 0 | 1 |
| 1 | 0 |
| 0 | 0 |

LOWER CASE

| 1 | 3 | 5 | 7 | 8 | 0 | 2 | 4 | 6 | 9 | # |
|---|---|---|---|---|---|---|---|---|---|---|
| x |   |   | x | x |   | x | x |   |   | x |
| / | t | v | x | y | - | s | u | w | z | , |
|   | x | x |   |   | x |   |   | x | x |   |
| ¡ | l | n | p | q | & | k | m | o | r | $ |
|   | x | x |   |   | x |   |   | x | x |   |
| a | c | e | g | h | @ | b | d | f | i | . |
| x |   |   | x | x |   | x | x |   |   | x |

| $T_1$ | $T_2$ |
|---|---|
| 1 | 1 |
| 0 | 1 |
| 1 | 0 |
| 0 | 0 |

| -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 |
|----|----|----|----|----|---|----|----|----|----|----|
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

ROTATE MAGNETS

| R2A |
|-----|
| R2 |
| R1 |
| R5 |
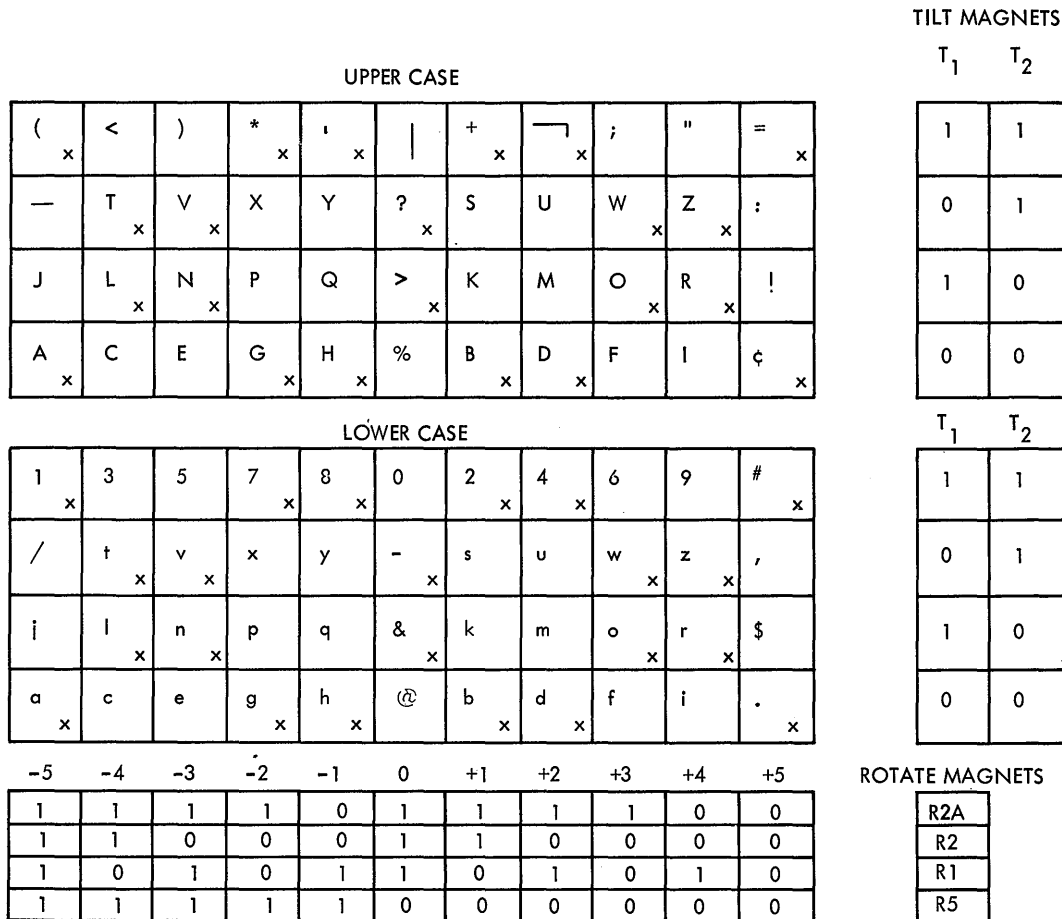
x = AUX MAGNET PICKED

Figure 6-26.   Tilt-Rotate Code

General Description

Translation

The 1052 adapter transmits to and receives from PAM common an 8 bit byte plus parity on a demand/response basis where the adapter initiates the byte transfer.  Hardware translation is provided by the adapter to convert to the various code formats (EBCDI, PT&T, T/R) utilized between the device and adapter.  The nominal printer character rate is 14.8 characters per second.

Data Handling

If a write command is accepted by the Adapter and requires a printer output the Adapter requests data (8 bits plus parity) from the channel.  This data is translated into a Tilt-Rotate code to pick

the proper magnets in the printer for a printable character, or
into a distinct line to pick the proper printer function magnet,
Figure 6-27.  If a Read command is accepted by the Adapter, and re-
quires the operator to enter data, the operator will key in the
desired character or printer function.  The Adapter receives data
from the keyboard as a 6 bit byte plus parity.  This data is trans-
lated into a 8 bit byte plus parity for subsequent transfer to the
channel.  The Adapter requests service from the channel and places
the character on Bus In.  When the channel accepts the data byte, the
adapter translates the data to a Tilt-Rotate code for printing or
converts the data to a function line.  All other commands accepted
by the Adapter do not require direct participation of the I/O device.

Commands

The 1052 adapter will decode commands from the channel during the
selection cycle and indicate the acceptance or rejection of the
command to the channel.  The valid commands for the 1052 adapter
are as follows:

| Command | Code | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Inhibit Priority Request | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Read | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| Test Read Mode | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Write Inhibit Carrier Return | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Write Auto Carrier Return | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| Test Write Mode Inhibit | M | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Test Write Mode Auto | M | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

M  =  Modifier bit may be 0 or 1

Any other codes with correct parity will set sense bit 0, Command
Reject, and present the Unit Check bit in the status byte in response
to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the
1052 Adapter and no outstanding status bits are present, a zero
status byte is returned to the channel.  If status information is
pending, all status bits present are transmitted to the channel.

Note:  the busy condition is defined differently with respect to
Test I/O.

Control No-Op (0000 0011)- The control No-Op command is an immediate
command.  No operation is initiated.  Channel End and Device End
are transmitted together in the initial selection sequence.

Sense (0000 0100)- The sense command will transmit one bit byte
plus parity to the channel.  This byte consists of data contained
in the sense register.  When the sense byte is accepted by the
channel, the adapter will initiate a termination sequence.

| PT+T CHARACTER | C B A 8 4 2 1 | EBCDI CHARACTER | P 0 1 2 3 4 5 6 7 | CHARACTER | FUNCTION | A | T1 | T2 | R2A | R2 | R1 | R5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SP | 1 0 0 0 0 0 0 | SP | 0 0 1 0 0 0 0 0 0 | | SPACE | - | - | - | - | - | - | - |
| = | 0 0 0 0 0 0 1 | = | 1 0 1 1 1 1 1 1 0 | = | | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| < | 0 0 0 0 0 1 0 | < | 0 0 1 0 0 1 1 0 0 | < | | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| ; | 1 0 0 0 0 1 1 | ; | 0 0 1 0 1 1 1 1 0 | ; | | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| : | 0 0 0 0 1 0 0 | : | 0 0 1 1 1 1 0 1 0 | : | | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| % | 1 0 0 0 1 0 1 | % | 1 0 1 1 0 1 1 0 0 | % | | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| ' | 1 0 0 0 1 1 0 | ' | 1 0 1 1 1 1 1 0 1 | ' | | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| > | 0 0 0 0 1 1 1 | > | 0 0 1 1 0 1 1 1 0 | > | | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| * | 0 0 0 1 0 0 0 | * | 1 0 1 0 1 1 1 0 0 | * | | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| ( | 1 0 0 1 0 0 1 | ( | 1 0 1 0 0 1 1 0 1 | ( | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ) | 1 0 0 1 0 1 0 | ) | 0 0 1 0 1 1 1 0 1 | ) | | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| + | 1 1 1 0 0 0 0 | + | 1 0 1 0 0 1 1 1 0 | + | | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| UC | 0 0 0 1 1 1 0 | UC | ———— | | SHIFT | - | - | - | - | - | - | - |
| ¢ | 0 0 1 0 0 0 0 | ¢ | 0 0 1 0 0 1 0 1 0 | ¢ | | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| ? | 1 0 1 0 0 0 1 | ? | 1 0 1 1 0 1 1 1 1 | ? | | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| S | 1 0 1 0 0 1 0 | S | 1 1 1 1 0 0 0 1 0 | S | | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| T | 0 0 1 0 0 1 1 | T | 0 1 1 1 0 0 0 1 1 | T | | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| U | 1 0 1 0 1 0 0 | U | 1 1 1 1 0 0 1 0 0 | U | | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| V | 0 0 1 0 1 0 1 | V | 0 1 1 1 0 0 1 0 1 | V | | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| W | 0 0 1 0 1 1 0 | W | 0 1 1 1 0 0 1 1 0 | W | | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| X | 1 0 1 0 1 1 1 | X | 1 1 1 1 0 0 1 1 1 | X | | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Y | 1 0 1 1 0 0 0 | Y | 1 1 1 1 0 1 0 0 0 | Y | | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| Z | 0 0 1 1 0 0 1 | Z | 0 1 1 1 0 1 0 0 1 | Z | | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| \| | 1 0 1 1 0 1 1 | \| | 0 0 1 0 0 1 1 1 1 | \| | | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| LF | 1 0 1 1 1 0 1 | LF | 0 0 0 1 0 0 1 0 1 | | LINE FEED | - | - | - | - | - | - | - |
| EOB | 1 0 1 1 1 1 0 | EOB | ———— | | END OF BLOCK | - | - | - | - | - | - | - |

| PT+T CHARACTER | C B A 8 4 2 1 | EBCDI CHARACTER | P 0 1 2 3 4 5 6 7 | CHARACTER | FUNCTION | A | T-1 | T-2 | R2A | R-2 | R-1 | R-5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | 0 1 0 0 0 0 0 | - | 0 0 1 1 0 1 1 0 1 | - | | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| J | 1 1 0 0 0 0 1 | J | 1 1 1 0 1 0 0 0 1 | J | | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| K | 1 1 0 0 0 1 0 | K | 1 1 1 0 1 0 0 1 0 | K | | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| L | 0 1 0 0 0 1 1 | L | 0 1 1 0 1 0 0 1 1 | L | | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| M | 1 1 0 0 1 0 0 | M | 1 1 1 0 1 0 1 0 0 | M | | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| N | 0 1 0 0 1 0 1 | N | 0 1 1 0 1 0 1 0 1 | N | | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| O | 0 1 0 0 1 1 0 | O | 0 1 1 0 1 0 1 1 0 | O | | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| P | 1 1 0 0 1 1 1 | P | 1 1 1 0 1 0 1 1 1 | P | | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| Q | 1 1 0 1 0 0 0 | Q | 1 1 1 0 1 1 0 0 0 | Q | | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| R | 0 1 0 1 0 0 1 | R | 0 1 1 0 1 1 0 0 1 | R | | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| " | 0 0 0 1 0 1 1 | " | 0 0 1 1 1 1 1 1 1 | " | | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| CR | 1 1 0 1 1 0 1 | CR | 0 0 0 0 1 0 1 0 1 | | CARRIER RETURN | - | - | - | - | - | - | - |
| BS | 1 1 0 1 1 1 0 | BS | 0 0 0 0 1 0 1 1 0 | | BACKSPACE | - | - | - | - | - | - | - |
| CAN. | 1 1 0 0 0 0 0 | CAN. | ———— | | CANCEL | - | - | - | - | - | - | - |
| ! | 1 1 0 1 0 1 1 | ! | 1 0 1 0 1 1 0 1 0 | ! | | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| A | 0 1 1 0 0 0 1 | A | 0 1 1 0 0 0 0 0 1 | A | | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| B | 0 1 1 0 0 1 0 | B | 0 1 1 0 0 0 0 1 0 | B | | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| C | 1 1 1 0 0 1 1 | C | 1 1 1 0 0 0 0 1 1 | C | | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| D | 0 1 1 0 1 0 0 | D | 0 1 1 0 0 0 1 0 0 | D | | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| E | 1 1 1 0 1 0 1 | E | 1 1 1 0 0 0 1 0 1 | E | | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| F | 1 1 1 0 1 1 0 | F | 1 1 1 0 0 0 1 1 0 | F | | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| G | 0 1 1 0 1 1 1 | G | 0 1 1 0 0 0 1 1 1 | G | | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| H | 0 1 1 1 0 0 0 | H | 0 1 1 0 0 1 0 0 0 | H | | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| I | 1 1 1 1 0 0 1 | I | 1 1 1 0 0 1 0 0 1 | I | | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| ⌐ | 0 1 1 1 0 1 1 | ⌐ | 1 0 1 0 1 1 1 1 1 | ⌐ | | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| HT | 0 1 1 1 1 0 1 | HT | 1 0 0 0 0 0 1 0 1 | | HORIZONTAL TAB | - | - | - | - | - | - | - |
| LC | 0 1 1 1 1 1 0 | LC | ———— | | SHIFT | - | - | - | - | - | - | - |

Figure 6-27.  Upper-Case Character Formats

PT+T / EBCDI / TILT ROTATE

| CHARACTER | C B A 8 4 2 1 | CHARACTER | P 0 1 2 3 4 5 6 7 | CHARACTER | FUNCTION | A | T-1 | T-2 | R2A | R-2 | R-1 | R-5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SP | 1000000 | SP | 001000000 | | SPACE | - | - | - | - | - | - | - |
| 1 | 0000001 | 1 | 011110001 | 1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 2 | 0000010 | 2 | 011110010 | 2 | | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 3 | 1000011 | 3 | 111110011 | 3 | | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 4 | 0000100 | 4 | 011110100 | 4 | | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 5 | 1000101 | 5 | 111110101 | 5 | | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 6 | 1000110 | 6 | 111110110 | 6 | | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 7 | 0000111 | 7 | 011110111 | 7 | | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 8 | 0001000 | 8 | 011111000 | 8 | | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 9 | 1001001 | 9 | 111111001 | 9 | | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1001010 | 0 | 111110000 | 0 | | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| & | 1110000 | & | 101010000 | & | | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| UC | 0001110 | UC | ——— | | SHIFT | - | - | - | - | - | - | - |
| @ | 0010000 | @ | 001111100 | @ | | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| / | 1010001 | / | 001100001 | / | | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| s | 1010010 | s | 010100010 | s | | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| t | 0010011 | t | 110100011 | t | | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| u | 1010100 | u | 010100100 | u | | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| v | 0010101 | v | 110100101 | v | | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| w | 0010110 | w | 110100110 | w | | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| x | 1010111 | x | 010100111 | x | | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| y | 1011000 | y | 010101000 | y | | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| z | 0011001 | z | 110101001 | z | | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| , | 1011011 | , | 001101011 | , | | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| LF | 1011101 | LF | 000100101 | | LINE FEED | - | - | - | - | - | - | - |
| EOB | 1011110 | EOB | ——— | | END OF BLOCK | - | - | - | - | - | - | - |

PT+T / EBCDI / TILT ROTATE

| CHARACTER | C B A 8 4 2 1 | CHARACTER | P 0 1 2 3 4 5 6 7 | CHARACTER | FUNCTION | A | T-1 | T-2 | R2A | R2 | R1 | R5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | 0100000 | - | 101100000 | - | | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| ¡ | 1100001 | ¡ | 010010001 | ¡ | | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| k | 1100010 | k | 010010010 | k | | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| l | 0100011 | l | 110010011 | l | | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| m | 1100100 | m | 010010100 | m | | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| n | 0100101 | n | 110010101 | n | | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| o | 0100110 | o | 110010110 | o | | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| p | 1100111 | p | 010010111 | p | | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| q | 1101000 | q | 010011000 | q | | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| r | 0101001 | r | 110011001 | r | | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| # | 0001011 | # | 101111011 | # | | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| CR | 1101101 | CR | 000010101 | | CARRIER RETURN | - | - | - | - | - | - | - |
| BS | 1101110 | BS | 000010110 | | BACKSPACE | - | - | - | - | - | - | - |
| CAN | 1100000 | CAN | ——— | | CANCEL | - | - | - | - | - | - | - |
| $ | 1101011 | $ | 001011011 | $ | | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| a | 0110001 | a | 110000001 | a | | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| b | 0110010 | b | 110000010 | b | | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| c | 1110011 | c | 010000011 | c | | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| d | 0110100 | d | 110000100 | d | | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| e | 1110101 | e | 010000101 | e | | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| f | 1110110 | f | 010000110 | f | | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| g | 0110111 | g | 110000111 | g | | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| h | 0111000 | h | 110001000 | h | | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| i | 1111001 | i | 010001001 | i | | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| . | 0111011 | . | 101001011 | . | | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| HT | 0111101 | HT | 100000101 | | HORIZONTAL TAB | - | - | - | - | - | - | - |
| LC | 0111110 | LC | ——— | | SHIFT | - | - | - | - | - | - | - |

Figure 6-28. Lower Case Character Formats

Inhibit Priority Request (0000 0111)- Inhibit Priority Request is an immediate type command. Channel End and Device End are set in the status byte during initial selection. It will cause the 1052 adapter to disable its Priority Request line so it cannot present attention or Device End to the channel, thus preventing double interruptions when the Printer Keyborad is attached to two adapters and both adapters are configured to an IOCE (or 2 IOCE's).

After this command is accepted, the adapter presents Busy status to all commands except Test I/O, which is used to restore the adapter to normal. A General or Selective Reset will also restore the adapter to normal.

PROGRAMMING NOTE: The 1052 Control Unit in the System Console does not utilize this command. It interprets this bit configuration as a Control No-Op.

Read (1000 1010)- Upon acceptance of the read command, the keyboard is unlocked and the proceed light is lit. The proceed light indicates that the operator may key in a character. When the operator keys in a character, a keyboard strobe is generated in addition to the keyed character. The keyboard is automatically locked at this time. The character is then parity checked (6 bits plus parity), translated to an eight bit plus parity byte and set into the data register. The adapter will then request service from the channel. When the channel accepts the data byte, the proceed light is extinguished, the keyboard stays locked, the character is translated to a T-R code or function line and printed, or the printer function performed. The keyboard is then unlocked and the proceed light is lit, allowing the next character to be keyed in. The above procedure is continued until termination is indicated. The read command may be terminated by one of three following methods:

1. Byte count 0 at the channel.

2. Enter signal by the keyboard operator. The Enter signal is issued by depressing the Enter Pushbutton.

3. Cancel signal by the keyboard operator. The cancel signal is used to indicate an operator error in the message and that the entire message must be retransmitted. The cancel signal is issued by depressing the Cancel Pushbutton.

When the adapter detects any of the above mentioned terminating signals it will lock the keyboard (which will remain locked until a read command is issued), turn off the proceed light, initiate a carrier return operation, and send a Channel End status to the channel. The Unit Exception status bit will be sent with Channel End if termination was accomplished by teh cancel signal.

When the carrier is returned to the left hand margin, the adapter will request service from the channel to present a status byte consisting of Device End.

<u>Write Auto Carrier Return (1000 1001)</u>- The write command will
select the 1052 adapter in write mode. After the write seelction
cycle is completed and the adapter has accepted the command, the
adapter will initiate a request to the channel via PAM common
to get the first data byte into the adapter data register for
transmission to the device. When the device has printed the
character or performed the function, another service request is
initiated; and the sequence is repeated until termination is
indicated. Write Auto Carrier Return will automatically return
the carrier at the end of the message.

After the last byte of the message has been sent to the adapter,
and the byte count equals zero at the channel, the ensuing service
request from the adapter will result in a termination indication
from the channel. The adapter will execute a Channel End status
cycle and initiate the carrier return sequence to the device. When
the carrier is returned to the left-hand margin, the adapter will
initiate a Device End status cycle to the channel.

<u>Write Inhibit Carrier Return (1000 0001)</u>- This command proceeds
the same as Write Auto Carrier Return, except that upon receipt
of the stop signal, the adapter transmits both Channel End and
Device End in the status byte. Write Inhibit Carrier Return will
not cause an end of message carrier return.

For either Write command, the byte in the adapter data register
is examined to see if type head shifting is required; if required,
shifting is done. The character is then translated to a tilt-ro-
tate code or function line and is printed or performs the function.
Another priority request is made only after the printer completes
its operation.

NOTE: The adapter reverts to lower case at the termination of a
Read command, while the operator could leave the shift key in the
locked (upper case) position. The adapter terminates a Write Inhibit
Carrier Return command in the shift case of the last character of
the message, thus will begin the next operation in that case. In
order to prevent errors from occurring, the operator should observe
several operating practices.

1. Prior to entering data during a Read operation, depress
   and release the shift key to ensure that the adapter and
   keyboard are in the same (lower) case.

2. Return the keyboard to lower case prior to ending a message
   with Enter or Cancel.

3. Leave the keyboard in lower case during all Write operations.

<u>Test Modes (M010, M001, 0010 1010)</u>- The test mode command will
select the adapter in write/read test mode. Test mode will degate
the device interface and allows the adapter to monitor and
initiate signals on the test lines from/to the Test and Monitor
adapter.

The test lines are used as follows during Test Write mode.

1.  Test Out line 1 - I/O Request line.

2.  Test Out line 2, 3 and 4 - not used.

3.  Test In line 1 - tilt rotate translator parity assignment.

4.  Test In line 2 - function in progress.

The test lines are used as follows during Test Read mode:

1.  Test Out line 1 - I/O request line used to simulate keyboard stroke.*

2.  Test Out lines:

        2 3 4   C B A 8 4 2 1

        0 0 0   1 0 0 0 0 0 0   Space

        0 0 1   0 0 0 1 1 1 0   Shift U.C.

        0 1 0   0 0 1 0 1 1 0   Character "w"
        0 1 1                   Attention

        1 0 0   0 1 0 1 0 0 1   Character "r"

        1 0 1                   Cancel

        1 1 0   1 1 1 1 1 1 1   NSNP (No space, no print)

        1 1 1                   Enter

3.  Test In line 1 - comparison of the PT&T and tilt rotate parity bits.

4.  Test In line 2 - function in progress.

Codes

The codes used by the Adapter are as shown in Figure 6-24 through 6-26.

Code Translators

The translation of the 256 possible combinations of the EBCDI code into printable characters, printer functions, and dummy cycles are as shown in Figure 6-29.

---

*Note:  I/O request line rate cannot exceed 14.8 Hz.

6-104

Figure table:

| BITS: 4567 → | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 | BITS: 0123 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | SP (x) | & | - | - (x) | SPACE | & (x) | - (x) | - | @ | & (x) | - (x) | 0 | % (x) | > | ? | 0 (x) | |
| 0001 | a | n (x) | / (x) | 8 | a (x) | n | / | 8 (x) | a (x) | i | / | 1 (x) | A | J (x) | — | 1 | |
| 0010 | b | o (x) | b (x) | , | b (x) | o | b | , (x) | b (x) | k | s | 2 (x) | B | K (x) | S (x) | 2 | |
| 0011 | b (x) | o | s | # (x) | b | o (x) | s (x) | # | c | l (x) | t (x) | 3 | C (x) | L | T | 3 (x) | |
| 0100 | NSNP | NSNP (x) | NSNP (x) | NSNP | 2 (x) | 2 | @ | @ (x) | d (x) | m | u | 4 (x) | D | M (x) | U (x) | 4 | |
| 0101 | HT (x) | NL | LF | NSNP (x) | 1 | 5 (x) | / (x) | 8 | e | n (x) | v (x) | 5 | E (x) | N | V | 5 (x) | |
| 0110 | NSNP (x) | BS | NSNP (x) | NSNP | 2 (x) | 6 | k (x) | # | f | o (x) | w (x) | 6 | F (x) | O | W | 6 (x) | |
| 0111 | NSNP | NSNP (x) | NSNP (x) | NSNP | 2 (x) | 6 | s | # (x) | g (x) | p | x | 7 (x) | G | P (x) | X (x) | 7 | |
| 1000 | h | q (x) | y (x) | y | H (x) | Q | Y | y (x) | h (x) | q | y | 8 (x) | H | Q (x) | Y (x) | 8 | |
| 1001 | i (x) | r | z | 9 (x) | i | r (x) | z (x) | 9 | i | r (x) | z (x) | 9 | I (x) | R | Z | 9 (x) | |
| 1010 | . (x) | $ | . | , (x) | ¢ | ! (x) | ¢ (x) | : | @ | & (x) | - (x) | 0 | % (x) | > | ? | 0 (x) | |
| 1011 | . | $ (x) | , (x) | # | . (x) | $ | , | # (x) | . (x) | $ | ; | # (x) | ¢ | ! (x) | : (x) | # | |
| 1100 | 3 (x) | 7 | @ | @ (x) | < | * (x) | % (x) | @ | e | n (x) | u (x) | 4 | E (x) | N | U | 4 (x) | |
| 1101 | 1 | 5 (x) | / (x) | 8 | ( (x) | ) | — | ' (x) | e (x) | n | v | 5 (x) | E | N (x) | V (x) | 5 | |
| 1110 | 2 | 6 (x) | & (x) | # | + (x) | ; | > | = (x) | e (x) | p | u | 6 (x) | E | N (x) | U (x) | 6 | |
| 1111 | 0 (x) | 4 | - | 9 (x) | \| | ¬ (x) | ? (x) | " | e | n (x) | v (x) | 5 | E (x) | N | V | 5 (x) | |

HT = HORIZONTAL TAB
NL = NEW LINE (CAR.RET, LINE FEED)
LF = LINE FEED
BS = BACKSPACE
SP = SPACE
NSNP = NEITHER SPACE NOR PRINT

x = PARITY BIT = 1
* CHARACTERS AND FUNCTIONS WITHIN
HEAVY LINES ARE DEFINED FOR 1052
ADAPTER

Figure 6-29.   Translation of Combinations Into Printable Characters

Status Information

The status byte is transmitted to the channel in four different situations:

1.   During initial selection.

2.   At the termination of any adapter command.

3.   When permitted to present queued status.

4.   To present the Attention or Device End signal to the channel.

Status Byte Format

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Attention |
| 1 | Not Used |
| 2 | Not Used |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Unit Exception |

Status Bit 0 (Attention)- The attention status bit will be set after the Request pushbutton is depressed and the following conditions are met:

1.  No initial selection is in progress.

2.  No command chaining is indicated.

3.  Status is not queued.

4.  A status byte is not being transmitted to the channel.

5.  The adapter and device are in a Not Busy Condition.

After the attention status bit has been set, the adapter and device become busy. Any new commands (except Test I/O) issued at this time will not be initiated by the adapter and will receive an attention status bit and a busy status bit. The adapter will remain busy with the attention status until the attention status is accepted by the channel. In the case of a Test I/O command, the attention status bit will be sent alone.

The adapter will request service from the channel and place the attention status bit on Bus In. The channel will then respond with either Service Out, indicating acceptance of status, or Command Out, indicating queue status. The I/O operation immediately following the acceptance of the attention status is under program control. Two interrupts may occur for attention status if the 1052 Printer Keyboard is attached to two adapters and each PAM is configured to present status to the IOCE. The Inhibit Priority Request command may be used to prevent this from occurring.

Status Bit 3 (Busy)- A busy condition for the adapter is set up under the following conditions:

1.  After the Initial Selection phase of a Read, Write, Sense, or Inhibit Priority Request.

2.  At the time the attention status bit is set on.

3.  When going from a Not Ready to Ready state.

4.  Any time status is stacked.

5.  When the 1052 Printer Keyboard is in CE Mode (the Status bit does not provide the indication).

The busy condition is reset by the acceptance of the attention status bit or Device End status bit, or by Test I/O if Inhibit Priority Request had been issued.

The busy status is sent to the channel during initial selection under the following conditions.

1.  New commands other than Test I/O:

    a.  After Channel End has been rejected by the channel.

    b.  After Device End has been generated but either has not been sent to the channel or has been rejected by the channel.

    c.  After Attention has been generated but has been rejected by the Channel.

2.  Any New Command:

    a.  After Channel End has been accepted by the channel but Device End has not occurred.

    b.  During CE Mode, Busy is presented to all commands even with invalid code or incorrect parity.

Status Bit 4 (Channel End)-  The Channel End status bit will inform the channel that the I/O device may be disconnected from the I/O interface.

1.  Control No-Op and Inhibit Priority Request are control immediate operations which send Channel End status during the Initial Selection phase.

2.  A sense operation will send Channel End after transferring one data byte consisting of the contents of the sense register.

3.  A write operation will send Channel End after receipt of the stop command from the channel indicating end of data transfer (Byte Count 0).

4.  A read operation will send Channel End after one of the following conditions have occurred.

    a.  After receipt of the stop command from the channel indicating end of data transfer (Byte Count 0).

    b.  After an Enter indication from the keyboard operator.

    c.  After a Cancel indication from the keyboard operator.

Status Bit 5 (Device End)- The Device End status bit indicates the adapter or device has completed an operation, or the device has noted a Not Ready to Ready transition.

1. Control No-Op and Inhibit Priority Request are control immediate operations which send Device End status during the initial selection phase, with Channel End.

2. A sense operation will send Device End with Channel End after transferring one data byte consisting of the contents of the sense register.

3. A read or write operation will send Device End at the completion of the last mechanical cycle of the printer for that operation.

4. When going from a Not Ready to Ready state, a Device End status will be sent to the channel. Two interruptions could occur (see Attention).

Status Bit 6 (Unit Check)- The Unit Check status bit is sent during initial selection or with Device End or Channel End status.

1. At Initial Selection:

   a. Command Reject

   b. Bus Out Check

   c. Intervention Required

2. At Device End and/or Channel End:

   a. Bus Out Check

   b. Equipment Check

Status Bit 7 (Unit Exception)- The Unit Exception status bit is sent during Channel End status time in Read operation if Channel End has been initiated by a cancel indication from the keyboard operator.

Sense Information

Snese Byte Format is as follows:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Intervention Required |
| 2 | Bus Out Check |
| 3 | Equipment Check |
| 4 | Not Used |
| 5 | Not Used |
| 6 | Not Used |
| 7 | Not Used |

Sense Bit 0 (Command Reject)- Command Reject will be set during initial selection if a command byte contains any code with correct parity other than those commands listed previously. All other sense register positions are reset except Intervention Required.

Sense Bit 1 (Intervention Required)- Intervention Required is the not ready condition of the I/O device and will occur IF:

1. The Not Ready pushbutton is depressed.

2. The printer runs out of forms.

3. After power is brought up and before the Ready pushbutton is depressed.

NOTE: The Intervention Required condition will not terminate a Read or Write operation that is in progress.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set if there is a parity error on Bus Out from the channel and the Command Out or Service Out tags are active. A Bus Out Check condition detected during data transfer will not cause the Read or Write operation to be terminated.

A Bus Out Check condition detected during a select sequence will set the Unit Check bit in the status byte and the command will be ignored. The Sense Register, with the exception of Bus Out Check and Intervention Required, will be reset at this time.

Sense Bit 3 (Equipment Check)- Equipment Check is set if:

1. Incorrect parity is detected from the Keyboard during a Read operation.

2. The printer fails to take a mechanical cycle as determined by the absence of a Printer Cycle signal.

3. There is a comparison check between keyboard input parity and the generated aux magnet parity.

Equipment Check will not terminate the Read or Write operations.

Reset- Sense bits 0, 2 and 3 will be cleared by the next acceptable Read or Write. Sense bits 0 and 3 are cleared when Bus Out Check occurs during Command Out. Sense bits 2 and 3 are cleared when Command Reject occurs. Sense bit 1 will be cleared when both causes are relieved. The Ready Pushbutton clears the Not Ready indication.

Priority

The 1052 adapter is assigned a certain position, with respect to other adapters, in the overall PAM priority scheme. The priority position in address dependnet, i.e., the lower the address assigned the high the priority. To upgrade or downgrade the priority of a

particular adapter, the address of the adapter must be changed accordingly. The re-assignment of the priority (and address) is easily changeable in the field.

Priority Request

Providing it has not been issued the Inhibit Priority Request command, the adapter will raise Priority Request line if it is disconnected from the channel, and no Initial Selection is in progress and one of the following conditions are met:

1.   Attention Interruption required.

2.   Device End Interruption required.

3.   Data Transfer required.

4.   Status is stacked and Suppress Out is down.

5.   Channel End Interruption required.

The Adapter will drop Priority Request whenever one of the following conditions are met.

1.   The Selected line is raised.

2.   Suppress status rises while conditions 1, 2, 4, or 5 of above are active.

Adapter-Device Interface Lines

The following are the Adapter/Device Lines used in communication.

Keyboard

| To Device | From Device |
|---|---|
| Lock Keyboard | (7) Data Bit In Lines<br>Keyboard Strobe<br>Alternate Code Key (Not Used)<br>Request Pushbutton<br>Ready Pushbutton<br>Not Ready Pushbutton<br>Enter Pushbutton<br>Cancel Pushbutton |

Printer

| To Device | From Device |
|---|---|
| (7) Tilt Rotate Magnets<br>(7) Function Magnets | Carrier in motion<br>End of Line Contact<br>End of Forms Contact<br>Printer Cycle |

Test Panel at Device

      C. E. Mode (customer engineer)
      On Line
      Continuous Write
      Read
(8)  Data Register Indicators
      Read Indicator
      Write Indicator
      Inhibit C. R. Indicator
      Upper Case Indicator
      Printer Busy Indicator
      Printer Cycle Indicator
      Command Reject Indicator
      Intervention Required Indicator
      Bus Out Check Indicator
      Equipment Check Indicator
      Proceed Indicator
      Attention Indicator

A description of the 57 lines listed above for the Adapter/Device interface follows:

Keyboard (15 lines)

There are 15 lines between the keyboard and the 1052 adapter as follows:

| | | |
|---|---|---|
| 1. | Keyboard PT&T 1 | Data bit from Keyboard |
| 2. | Keyboard PT&T 2 | Data bit from Keyboard |
| 3. | Keyboard PT&T 4 | Data bit from Keyboard |
| 4. | Keyboard PT&T 8 | Data bit from Keyboard |
| 5. | Keyboard PT&T A | Data bit from Keyboard |
| 6. | Keyboard PT&T B | Data bit from Keyboard |
| 7. | Keyboard PT&T C | Data bit from Keyboard |

    8.  <u>Lock Keyboard</u>-  This line is pulsed by the adapter to unlock the keyboard (which is automatically locked after each character is entered). A D.C. level on this lines has a dual meaning and locks the keyboard to prevent character entry.

    9.  <u>Keyboard Strobe</u>-  This line is raised by the Keyboard to indicate to the adapter that a character is available.

   10.  <u>Alternate Coding Key</u>-  This line is not used.

   11.  <u>Request Pushbutton</u>-  This line is set by the Request Pushbutton and causes the Attention status to be set.

12. <u>Ready Pushbutton</u>- This line is set by the Ready Pushbutton and causes Device End status to be set.

13. <u>Not Ready Pushbutton</u>- This line is set by the Not Ready Pushbutton and causes sense bit 1, Intervention Required, to be set.

14. <u>Enter Pushbutton</u>- This line causes the adapter to terminate the Read operation.

15. <u>Cancel Pushbutton</u>- This line causes the adapter to terminate the Read operation and set Unit Exception in the status byte.

Printer (18 lines)

There are 18 lines between the Printer and the 1052 adapter as follows:

| | | |
|---|---|---|
| 1. | Tilt Magnet 1 | Data bit to Printer |
| 2. | Tilt Magnet 2 | Data bit to Printer |
| 3. | Rotate Magnet 1 | Data bit to Printer |
| 4. | Rotate Magnet 2 | Data bit to Printer |
| 5. | Rotate Magnet 2A | Data bit to Printer |
| 6. | Rotate Magnet 5 | Data bit to Printer |
| 7. | Auxiliary (aux) Magnet | Data bit to Printer |

Seven lines (8-14 below) are raised by the 1052 adapter to cause the appropriate function magnet in the Printer to be operated as follows:

8. <u>Horizontal tab</u>- advance to next horizontal tabulation STOP position.

9. <u>Backspace</u>- backspace one character position.

10. <u>Carrier Return and Line Feed</u>- causes carrier to return and advances paper one line.

11. <u>Line Feed</u>- advances paper one line.

12. <u>Shift to Upper Case</u>- shifts typing head to upper case.

13. <u>Shift to Lower Case</u>- shifts typing head to lower case.

14. <u>Space</u>- advance carrier one character position.

15. <u>Carrier In Motion</u>- This line is raised by the printer until the completion of the printer function initiated by lines 8, 10, or 11 above.

16. <u>End of Line Contact</u>- This line is set when the end of print line is detected by the printer and initiates carrier return and line feed.

17. <u>End of Forms Contact</u>- This line is set by the Printer when end of paper forms is detected and causes sense bit 1, Intervention Required, to be set.

18. <u>Printer Cycle</u>- This line is raised by the Printer and indicates mechanical cycle has been performed.

Test Panel (24 lines)

There are two switches on the Test panel of the 1052 Printer Keyboard (see figure 11-5) that are connected to the 1052 adapter through 4 lines as follows:

<u>CE Mode Switch</u>- One of two lines in raised to indicate to the 1052 adapter that the 1052 Printer Keyboard is in Customer Engineer (CE) test mode or On Line mode. The CE Mode position is disabled unless a jumper card is inserted in the 1052 adapter by maintenance personnel. The jumper card places both adapters (one in each of two PAM's if duplexed) in CE Mode regardless of the CE Mode switch position. However, the switch must be thrown to CE Mode to perform a CE Mode Read or Write operation, with the adapter in which the jumper card was inserted. If an I/O channel attempts selection of the 1052 Adapter when in CE Mode, the adapter will return Busy status to the channel. No CE Mode jumper card is required for the System Console connected Printer Keyboard.

<u>Continuous Write/Read Switch</u>- One of two lines is raised to indicate to the adapter that the 1052 Printer Keyboard is to be tested in a Write operation or a Read operation.

The following 20 indicators light when the specified condition occurs in the 1052 adapter and sets the corresponding line as follows:

1. <u>READ Indicator</u>- This indicator is set when the Adapter is executing a read command.

2. <u>WRITE Indicator</u>- This indicator is set when the Adapter is executing a write command.

3. <u>INHIB CR Indicator</u>- This indicator is set when the adapter is executing a Write Inhibit Carrier Return command.

4. <u>UPPER CASE Indicator</u>- This indicator is set when the Printer is in upper case.

5. <u>PRTR BUSY Indicator</u>- This indicator is set when the Printer is executing a print or function cycle.

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6.  PRTR CYCLE Indicator- This indicator is set when the Printer executes a mechanical cycle upon receipt of a character.

7.  CMND REJ Indicator- This sense indicator is set when an invalid command code is detected by 1052 adapter.

8.  INTVTN REQD Indicator- This sense indicator is set when the Not Ready condition (Out of paper forms, Not Ready pushbutton or power turned on but Ready pushbutton not yet depressed) is detected by 1052 adapter.

9.  BUS OUT Indicator- This sense indicator is set when the adapter detects incorrect parity on Bus Out.

10. EQUIP Indicator- This sense indicator is set if:

    a.  Incorrect parity is detected from the keyboard during a Read operation.

    b.  The printer fails to take a mechanical cycle as determined by the absence of a Printer Cycle signal.

    c.  There is a comparison check between keyboard input parity and the generated aux magnet parity.

11. PROCD Indicator- This indicator is set when the 1052 adapter can accept a character from the keyboard (keyboard is unlocked).

12. ATTN Indicator- This indicator is set by the Request Pushbutton.

The following eight indicators are set when the corresponding bit in the adapter data register is set to a one.

13. Data Bit 0                17. Data Bit 4

14. Data Bit 1                18. Data Bit 5

15. Data Bit 2                19. Data Bit 6

16. Data Bit 3                20. Data Bit 7

A lever is provided at the left end of the test panel to set or clear tab stops on the printing mechanism.

Timing

Timing diagrams for a read and write command are shown in Figure 6-30 and 6-31. Timing is obtained through use of single shots and requires approximately 68 milliseconds between characters.
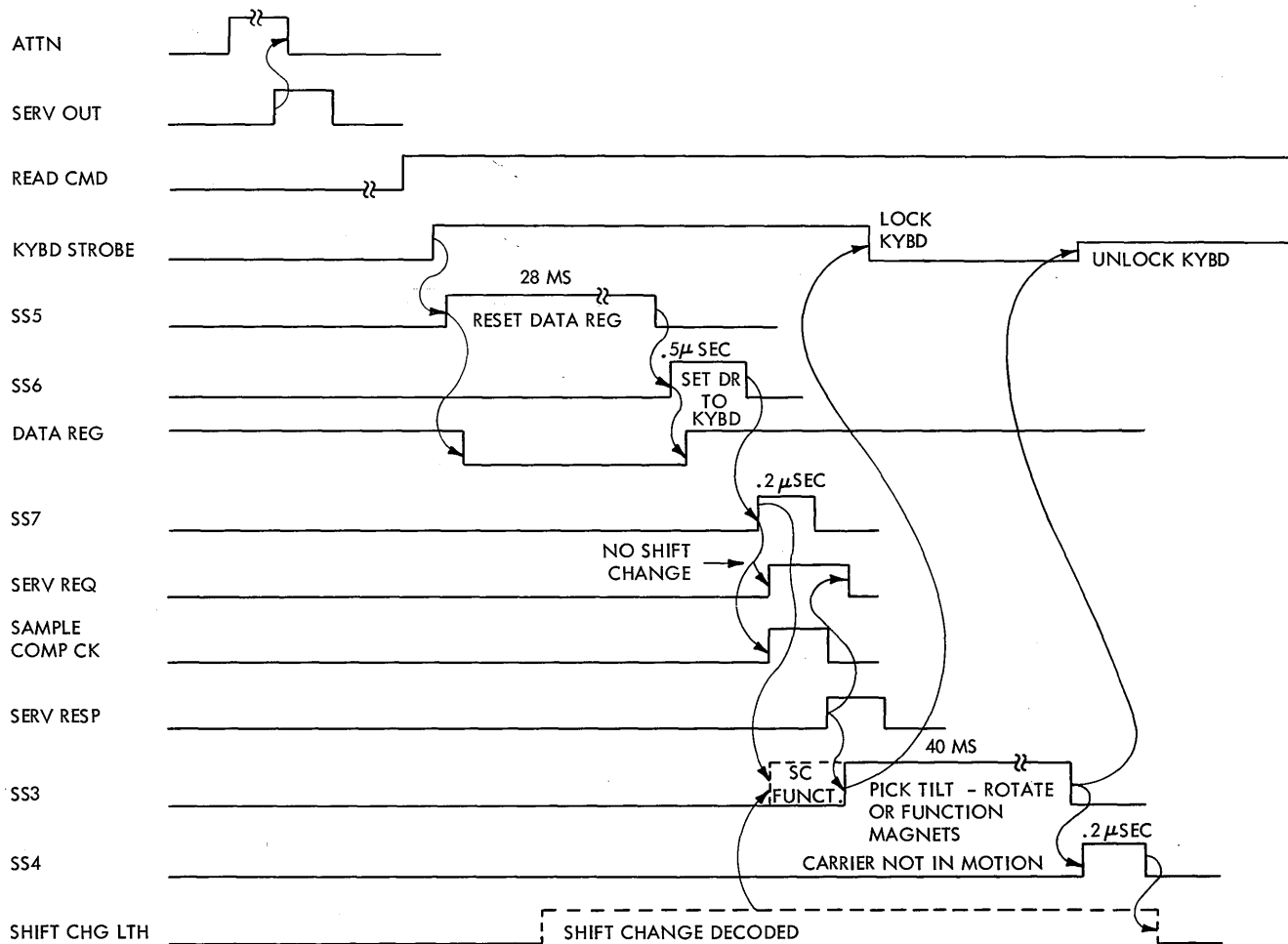
Figure 6-30.  1052 Adapter Read Command Timing Diagram

WRT CMD

SERV REQ

NO SC

SERV RESPONSE

.5 μ SEC

SS1
SET DR TO
BUS OUT

SHIFT CHANGE
INH SET OF
DR TO BO

IF SHIFT CHANGE

DATA REG

.2 μSEC
ENABLE TURN
OFF SC LTH
SS2
SERV IN

40 MS

SS3
PICK TILT – ROTATE
OR FUNCTIONAL
MAGNETS

.2 μSEC
RESET DR IF NO SC
SS4

28 MS

SS5

CARRIER NOT
IN MOTION

.5 μSEC
TURN ON SS1
IF SHIFT CHG

SS6
TURN ON
SVC REQ
(NO SC)

.2 μSEC
RST
SC LTH
SS7

PTR BUSY
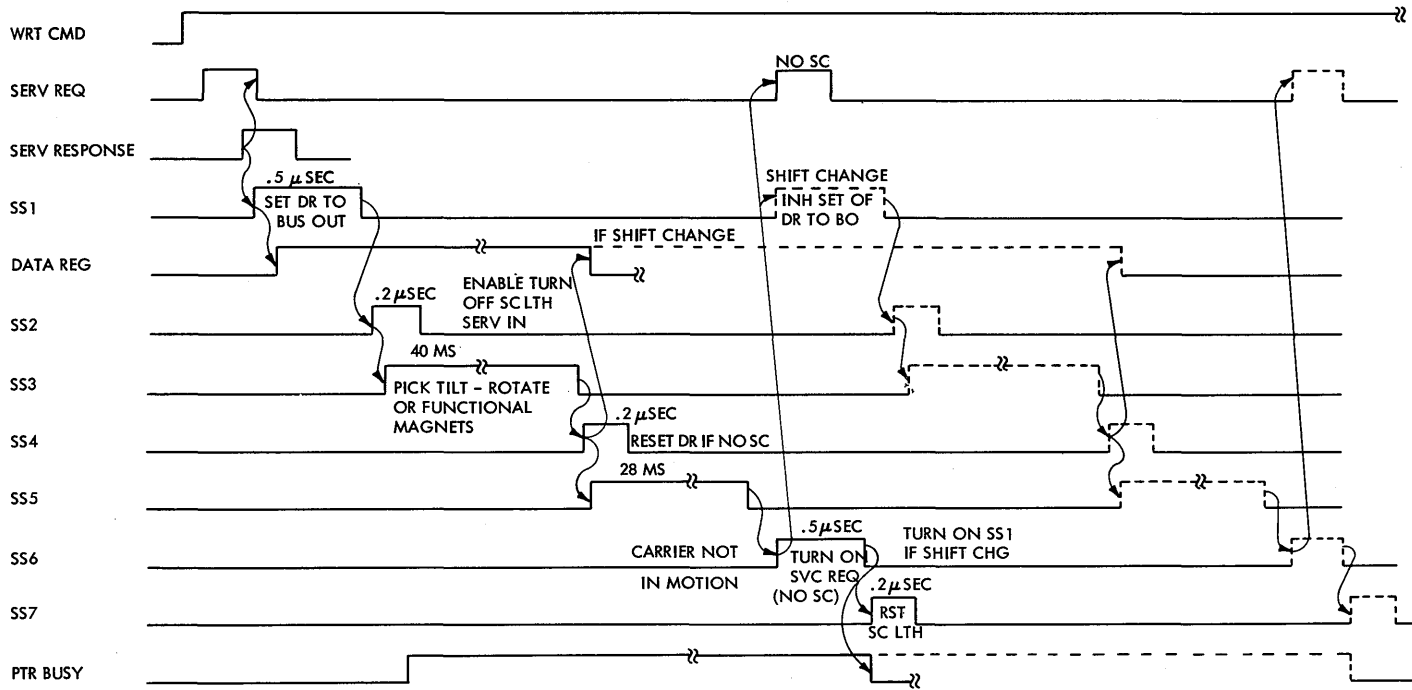
Figure 6-31.  1052 Adapter Write Command Timing Diagram

1052 Adapter Device Interface Pin Assignments

| I/O Connector Pin (Cable 1) | Cable-Line Name |
|---|---|
| B02 | Spare |
| D02 | Ground |
| B03 | +Keyboard = 1 bit |
| *D03 | +Lock Keyboard |
| B04 | Cancel |
| D04 | +Keyboard = 2 bit |
| B05 | +Keyboard = 4 bit |
| *B06 | +Lock Keyboard |
| D05 | Enter |
| D06 | +Keyboard = 8 bit |
| B07 | Ground |
| D07 | Spare |
| B08 | +Keyboard = A bit |
| D08 | Ground |
| B09 | Spare |
| D09 | +Keyboard = B bit |
| B10 | +Keyboard = C bit |
| D10 | Spare |
| B11 | Spare |
| D11 | +48 Keyboard Strobe |
| B12 | Minus Lock Keyboard |
| D12 | Spare |
| B13 | Ground |
| D13 | +48v Alternate Coding (Not Used) |
| G02 | Not Used |
| J02 | Ground |
| G03 | -Pick T2 Mag |
| J03 | -Pick CR-LF Mag |
| G04 | -Pick line Feed Mag |
| J04 | -Pick Aux Mag |
| G05 | -Pick $T_1$ Mag |
| G06 | Not Used |
| J05 | -Pick LC Shift Mag |
| J06 | -Pick R2A Mag |
| G07 | Ground |
| J07 | +48 Not CAM Cycle |
| G08 | -Pick R1 Mag |
| J08 | Ground |
| G09 | -Pick UC Shift Mag |
| J09 | -Pick R2 Mag |
| G10 | -Pick R5 Mag |
| J10 | GND End of Line |
| G11 | +Open End of Forms |
| J11 | -Pick Tab Mag |
| G12 | -Pick Space Mag |
| J12 | +48 Carrier in Motion |
| G13 | Ground |
| J13 | -Pick Backspace |

*Used in PAM to PAM cables only

1052 Adapter Device Interface Pin Assignments (continued)

| I/O Connector Pin (Cable 2) | Cable-Line Name |
|---|---|
| B02 | -Ind Attention |
| D02 | Ground |
| B03 | -Ind DR 5 |
| D03 | Not Used |
| B04 | -Ind DR 6 |
| D04 | Spare |
| B05 | -Ind DR 7 |
| B06 | Not Used |
| D05 | Spare |
| D06 | Spare |
| B07 | Ground |
| D07 | -Ind CMD Reject |
| B08 | -Ind Intervention REQD |
| D08 | Ground |
| B09 | -Ind Bus Out Check |
| D09 | -Ind DR 4 |
| B10 | -Ind Equip Chk |
| D10 | -Ind DR 0 |
| B11 | Not Used |
| D11 | -Ind DR 1 |
| B12 | -Proceed Lamp |
| D12 | -Ind DR 2 |
| B13 | Ground |
| D13 | -Ind DR 3 |
| G02 | +3 volts |
| J02 | Ground |
| G03 | -CE Mode |
| *J03 | CE Mode |
| G04 | +Ready PB |
| J04 | Lamp Write |
| G05 | -CE Cont WRT |
| G06 | +3 volts |
| J05 | -Ind Inh. C. R. |
| J06 | -Upper Case Lamp |
| G07 | Ground |
| J07 | -CE Read |
| G08 | +Not Ready PB |
| J08 | Ground |
| G09 | -Request PB NC |
| J09 | -PRT Busy Lamp |
| G10 | -Request PB NO |
| J10 | -Printer Cycle Lamp |
| G11 | +3 volts |
| J11 | Lamp Read |
| G12 | +CE Reset |
| J12 | +3 volts |
| G13 | Ground |
| J13 | +3 volts |

For Signal and Shield terminations refer to Appendix B.
*Used in PAM to PAM cables only.

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## Customer Engineer (CE) Mode Operations

### Write

The ability is provided to perform a continuous write operation, alternating between two previously selected coded characters. This operation is accomplished by the adapter and the printer and does not utilize the Test and Monitor Adapter.

### Read

The ability is provided to operate all keyboard keys and to confirm proper operation by observation of the printer and the indicators on the panel. This operation is accomplished by the adapter and the printer-keyboard and does not utilize the Test and Monitor Adapter.

## COMMON DIGITIZER ADAPTER

### General Characteristics

The Common Digitizer (CD) adapter matches the interface requirements of the Common Digitizer input. The CD adapter receives data serially from one of 3 channels of the CD Data Receiving Group (DRG) at a rate of 2400 bits per second. The data is received as messages consisting of two or more fields. Each field is composed of 12 data bits plus an odd parity bit. A field will be assembled into two bytes (8 bits plus odd parity), and transferred to the multiplexor channel in two successive data cycles under burst mode.

### General Description

#### Interfaces

The CD adapter provides for communication between a Data Receiving Group (DRG) channel and PAM Common. The CD Adapter communicates with PAM Common over the adapter interface, and with the DRG over the device interface.

#### Device Interface

The four device interface lines between the CD adapter and a DRG channel are as follows:

    1 SOM in line
    1 EOM in line
    1 Data in line
    1 Clock in line

#### Commands

The CD adapter will decode commands from the IOCE channel and indicate the acceptance or rejection of the command to the channel

during a Select cycle.  The valid commands for the CD adapter are
as follows:

| Command | Code |
|---------|------|
|         | 0 1 2 3 4 5 6 7 |
| Test I/O | 0 0 0 0 0 0 0 0 |
| Control No-Op | 0 0 0 0 0 0 1 1 |
| Sense | 0 0 0 0 0 1 0 0 |
| Read | *M 0 0 0 0 0 1 0 |
| Test Read Mode | *M 0 1 0 0 0 1 0 |

        M  =  Modifier bit may be 0 or 1

Any other codes with correct parity are invalid and will set sense
bit 0, Commond Reject, and present Unit Check in the status byte
in response to the command during initial selection.  No operation
is performed.

Test I/O (0000 0000)-  If the Test I/O command is accepted by the
CD adapter, and no outstanding status condition exists, a zero status
byte is returned to the channel.  If status information is pending,
all status bits present are transmitted to the channel.

Control No-Op (0000 0011)-  The Control No-Op command is treated as
an immediate type command.  It performs no operation, and Channel
End and Device End are transmitted together during the initial
selection cycle.

Sense (00000100)-  When the CD adapter has accepted a Sense command,
it will initiate a service request to the channel through PAM Command.
When the adapter is serviced, it will gate the contents of its sense
register with correct parity to the channel.  When the sense byte
is accepted, the CD adapter will initiate a termination sequence.

Read (0000 0010) (1000 0010)-  After accepting a Read command, the
CD adapter will sample the Start of Message (SOM) Line and the Data
In Line.  A SOM signal indicates that the first bit of the field is
present on the Data In Line.

Data Pattern-  The data is received in fields consisting of 12 data
bits followed by an odd parity bit.  Within a field, the most
significant bit (MSB) is received first, and the least significant
bit (LSB) is received last.  The number of fields per message is
variable, but there will always be more than one field.  SOM is sent
concurrent with the first data bit of the first field of a message.
EOM is sent concurrent with the last data bit of the last field of a
message.

Data Formatting-  The CD adapter will treat each field of the incom-
ing message as follows.  Refer to figure 6-32.

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SERIAL OUTPUT FROM DRG

| MSB 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | LSB 12 | P |
|-------|---|---|---|---|---|---|---|---|----|----|--------|---|

TAG BITS

| P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

S E F M
O O I A
M M E L
L F
D U
N
P C
A T
R I
I O
T N
Y

BYTE #1

| P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

BYTE #2
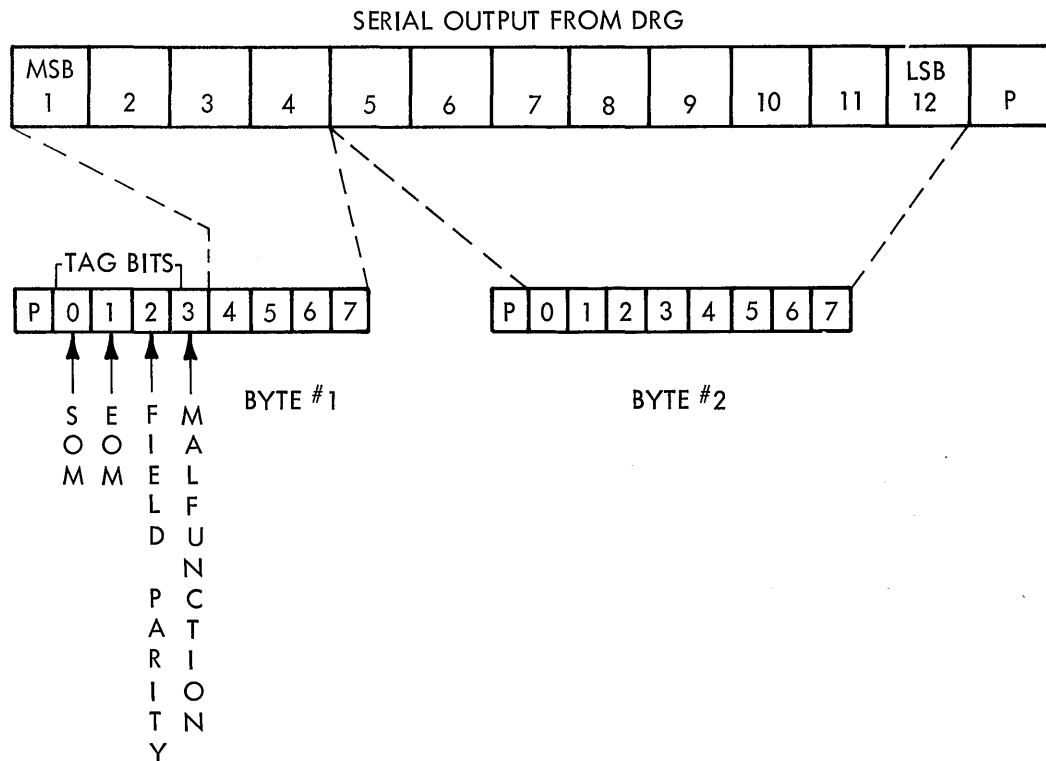
Figure 6-32.  DRG Serial Output Conversion to Storage Bytes

     Upon detection of the first bit of the field, the adapter
will reset the tag bits and the bit counter will be set to one.
In addition, if this is the first field of a message, the SOM line
will be active concurrently with the first data bit.  Upon detection
of the SOM, the adapter will place a one bit in position 0 of Byte 1.
The first 4 incoming data bits will be assembled in the 4 least
significant bits of an 8 bit register (Byte 1).  Bit positions 0-3
of Byte 1 (Tag Bits) will be used for SOM, EOM, field parity error,
and malfunction indicator, respectively.  The remaining 8 incoming
data bits will be assembled in a second 8 bit register (Byte 2).
Each byte will be sent to the channel with an odd parity bit
assigned by the adapter.  The non-data bits are set as follows:

     SOM.  Upon detection of a SOM signal, the adapter will place a
     "one" in bit position 0 of Byte 1.

     Field Parity Check.  The adapter will generate a field parity
     bit for each field of 12 data bits received and will compare
     it with the field parity bit received (bit 13 of field).  If
     a field parity error is detected, a one will be placed in bit
     position 2 of Byte 1.

     Malfunction Indicator.  When any field of an incoming message
     contains a field parity error, this indication will be retained
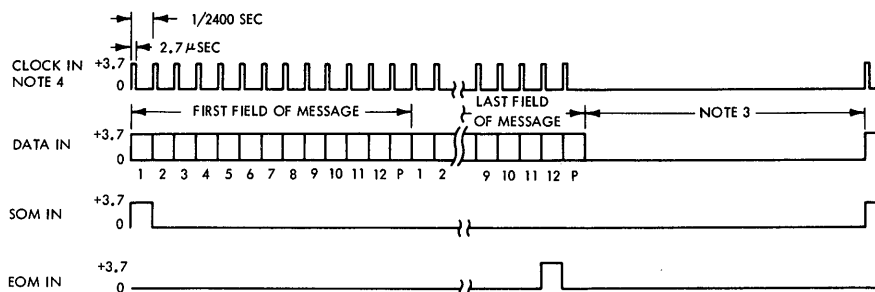
NOTES

1. SOM OCCURS DURING ENTIRE TIME INTERVAL OF BIT ONE OF FIELD ONE.

2. EOM OCCURS DURING ENTIRE TIME INTERVAL OF BIT 12 OF LAST FIELD.

3. SUCCESSIVE MESSAGES ARE SEPARATED BY A MINIMUM OF ONE FIELD INTERVAL (13/2400 SEC).

4. CLOCK PULSES ARE DELAYED (MIN 300 NANOSEC, MAX 3 MICROSEC) SO THAT DATA, SOM, AND EOM ARE STATIC AT CLOCK TIME.

5. RISE TIME (10 TO 90% POINTS) AT INPUT OF ADAPTER RECEIVER IS ≤ 200 NANOSEC.

6. FALL TIME AS MEASURED ABOVE IS ≤ 450 NANOSEC.

7. MAXIMUM CABLE LENGTH:
   IBM P/N 5353912 - - 300 FT
   RG62 A/U - - - - - - 300 FT
   RG62 B/U - - - - - - 238 FT

Figure 6-33.  Common Digitizer Adapter Timing Chart

until the time of storing the two bytes for the last field of the message.  At that time, the adapter will place a one in bit position 3 of Byte 1.  This will signify that the adapter has detected a field parity error in one or more fields of the message.  The malfunction indicator is also used to signal certain abnormal SOM-EOM timing relationships.  These are described under Abnormal Sequences or Conditions.

EOM.  An EOM signal will appear on the EOM line concurrent with the 12th bit (last data bit) of the last field of an incoming message.  Upon receipt of the EOM signal, the adapter will place a one in bit position 1 of Byte 1.  Bit position 0 of Byte 1 will be forced to zero.  The parity bit is then received as the 13th and last bit of the field.  Bit position 2 of Byte 1 will be set to one if a field parity error is detected and bit position 3 will be set to a one if a field parity bit was set to a one in any field of the message.

*Bit zero of both Read and Test Read Mode commands is not utilized by the CD adapter.  In order to provide RVDP program compatibility, the adapter will accept either a "one" or a "zero" in this position.

After each field is assembled into two bytes, the CD adapter will ask for service in via the PAM Common.  When service in is granted, the adapter will gate the contents of Byte 1 followed by Byte 2 to

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the Bus In, in two consecutive data cycles under burst mode operation, such that Byte 1 will be stored in byte storage address n and Byte 2 will be stored in byte storage address n + 1.

This sequence of assembling two bytes and gating them to the Bus In is repeated for successive fields. Following detection of an EOM signal, the Data In line will accept the next bit as parity for the field. A new SOM signal must be detected by the adapter before any more data will be accepted. Termination of the Read operation will occur if the CD adapter detects an indication that the channel byte count has gone to zero after requesting service in from the channel. Termination takes place when the channel accepts the Channel End, Device End conditions in the status byte. EOM from the device does not terminate the Read operation.

PROGRAMMING NOTE: Termination will occur as a result of the next service request (generated from the CD adapter to the channel) after the channel byte count has gone to zero and chaining is not indicated. However, due to the free-running characteristics of the input and the nature of the data being transmitted, a Channel End condition initiated by the adapter when the byte count equals zero should not normally occur. The program should use data chaining and the information obtained through the use of the SET PCI instruction to allocate storage buffer areas and to monitor the progress of data transfers.

Abnormal Sequences or Conditions. The CD adapter design uses the philosophy that in the event of detection of certain abnormal sequences or conditions the adapter will send either two bytes of data or no data to the channel for the last field received.

The CD adapter uses the SOM signal for purposes of message synchronization. When an SOM signal is received, the CD adapter will perform appropriate resetting functions. Based on this design philosophy, the following apply:

1.  Data and EOM signals preceding the first SOM signal after the Read command is accepted will be ignored.

2.  If more than one SOM signal is detected within the time period of one field (13/2400 second), the second SOM will take precedence and the partial field preceding it (stored in the adapter) is lost.

3.  In the event that an EOM signal is lost, successive messages will be resynchronized by SOM signals.

4.  If the EOM signal occurs at the wrong time, it will either be treated as a spurious signal or will set the malfunction bit.

Detection of an overrun condition terminates the Read operation after setting the Unit Check bit and Overrun bit. See Sense information paragraph following.

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Detection of various equipment malfunctions as a result of information transfers to the CD adapter and the DRG will cause the following:

1.  If SOM and EOM signals are detected within the same field time interval (13/2400 second), one of the following will occur:

    a.  If SOM and EOM signals are detected in the same bit interval (1/2400 sec.), the SOM functions will take precedence and data in the adapter preceding the EOM/SOM will not be stored.  The EOM is assumed to be a spurious signal, and is therefore ignored.

    b.  If the SOM signal is detected before the EOM signal, the SOM functions will have taken place when EOM is received, and when the EOM signal is detected, it will cause the malfunction indicator (bit 3 of Byte 1) to be set to a one.  The other tag bits (bits 0 through 2 of the Byte) will be set to zeros.  The data in the last four bits of Byte 1 and the eight bits of Byte 2 will be transferred to the channel in the manner of a normal field.

    c.  If the EOM signal is detected before the SOM signal, the SOM signal resets the adapter.  The EOM signal is ignored.  Data stored in the adapter prior to SOM is lost.

2.  If the EOM signal is detected during a field time interval other than that of SOM, but not concurrent with data bit 12, the tag bits are set to 0001 and the two data bytes are transferred to the channel as in preceding paragraph 1b.

Summary of Tag Bits for CD Messages

Byte 1

| Bits 0-3 | Meaning |
|---|---|
| 1000 | SOM signal was detected.  No field parity error was detected in the first field of the message. |
| 0100 | EOM signal was detected.  No field parity error was detected in the last field or any other field of the message, nor was the malfunction indicator bit set. |
| 0000 | No SOM or EOM signals were detected.  No field parity error was detected.  This is neither the first nor last field of the message. |
| 1010 | SOM signal was detected.  A field parity error was detected in the first field of the message. |
| 0101 | EOM signal was detected.  A field parity error was detected in one or more fields of the message but not in the last field. |

Byte 1

Bits 0-3     Meaning     (cont.)

0111         EOM signal was detected.  A field parity error was de-
             tected in the last field of the message.  Other fields
             of this message may have had a field parity error.

0010         A field parity error was detected.  This field is
             neither the first nor the last field of the message.

0001         The malfunction indicator is set.  EOM signal was de-
             tected within the same field as SOM, or at other than
             bit 12 time.

Test Read Mode (0010 0010) (1010 0010).  The Test Read Mode command
will select the CD adapter in Test Read Mode.  this will degate the
device interface and allow the adapter to monitor and initiate
signals on the test lines from/to the Test and Monitor adapter.

Status Information

The status byte is transmitted to the channel in the following
situations:

    1.   During initial selection.

    2.   At termination of any adapter command.

    3.   When permitted to present stacked status.

Status Byte Format

| Bit | Designation |
|-----|-------------|
| P   | Parity      |
| 0   | Not Used    |
| 1   | Not Used    |
| 2   | Not Used    |
| 3   | Not Used    |
| 4   | Channel End |
| 5   | Device End  |
| 6   | Unit Check  |
| 7   | Not Used    |

Status Bits 4 and 5 (Channel End and Device End)-  The Channel End
and Device End status bits are always presented together by the CD
adapter.  When set, the adapter will terminate the I/O operation
and will present status to the channel when allowed to do so.  These
bits are set on the following conditions:

    1.   During the initial selection sequence of a Control No-Op.

    2.   After the sense byte has been accepted during a Sense Oper-
         ation.

3.  At the termination of a Read or Test Read Mode Command.

4.  Upon detection of a Halt I/O condition.

Channel End and Device End status are reset by the acceptance of a status byte by the channel.

Status Bit 6 (Unit Check)-  A Unit Check status bit is set during the initial selection or at Channel End and Device End time of a Read command.  To enable the processor to obtain a more detailed picture of the cause of the Unit Check condition, a Sense operation should be performed.  The Unit Check condition is set.

1.  At initial selection by

    a.  Command Reject

    b.  Bus Out Check

2.  At Channel End and Device End time of a Read command by overrun.

Unit Check condition is reset by the acceptance of the status byte by the channel.

Sense Information

When the Unit Check bit is found to be set in the status byte, a Sense command should be executed to determine the type of equipment or programming check associated with the previous command.  The sense register positions are reset by the acceptance of the next valid Read or Test Read Mode command.  With the exception of bit 2, Bus Out Check, the sense register is also reset whenever Bus Out Check occurs during Command Out.  With the exception of Bit 0, Command Reject, it is also reset whenever a Command Reject occurs.

Sense Byte Format

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Not Used |
| 4 | Not Used |
| 5 | Overrun |
| 6 | Not Used |
| 7 | Not Used |

Sense Bit 0 (Command Reject)-  Command Reject is set during the initial selection phase of a command if the bit configuration is other than one of those listed previously.  All other sense register positions are reset.

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Sense Bit 2 (Bus Out Check)- Bus Out Check will be set any time
a Bus Out Check signal is received over the adapter interface. A
Bus Out Check signal will occur if PAM Common detects a parity
error on the Bus Out (from IOCE to PAM Common) and the Command Out
tag is active.

A Bus Out Check detected during a Select sequence will set the
Unit Check bit in the status byte and the command will be ignored.
The sense byte, with the exception of Bus Out Check, is reset at this
time.

Sense Bit 5 (Overrun)- The CD adapter provides buffering of the
incoming data such that overrun will not occur unless the twelfth
bit of an incoming field arrives at the adapter data register before
the two bytes of the previous field have been serviced by the
channel. This allows the adapter approximately 5.0 milliseconds
(12 bit time) to obtain channel service before overrun could occur.
Overrun will terminate the Read operation after both bytes of the
previous field are accepted by the channel. The incoming field is
lost.

Priority

The priority position is address dependent, i. e., the lower
the address assigned within a group, the higher the priority.
To upgrade or downgrade the priority of a particular adapter, the
address of the adapter must be changed accordingly. The re-assign-
ment of the priority and address is changeable in the field.

CD Adapter - Device Interface Description

The CD adapter interface provides a uniform method of attaching one
CD DRG channel device to a CD adapter. It consists of a set of lines
which are used to transmit information from the device.

Signal Lines. The signal lines for the CD interface are as follows:

| Data Line | Initiated By |
|---|---|
| Data In | Device |

| Control Lines | Initiated By |
|---|---|
| SOM In | Device |
| EOM In | Device |
| Clock In | Device |

Signal Lines Description. Description of the above signal lines
follows.

Data In- A signal on this line is initiated by the device and
monitored by the CD adapter if the SOM signal has been detected. The
Data In Line presents a one or zero to the adapter. The signal must
be static when Clock In is detected by the adapter.

SOM In- A signal on this line is initiated by the device and monitored by the CD adapter. The signal must be static when Clock In is detected by the adapter. When the SOM signal is detected and the CD adapter has been previously selected by a Read command, it will cause the CD adapter to perform appropriate resetting functions and to monitor the Data In Line.

EOM In- A signal on this line is initiated by the device and monitored by the CD adapter. The signal must be static when the adapter detects Clock In for the last data bit of a field of a message. Occurrence during any other clock time is abnormal and results in either setting of the malfunction indicator, or the EOM signal being ignored as described under the Read command description.

Clock In- The signal on this line is initiated by the device and monitored by the CD adapter. It is used to establish a sample of the Data In, SOM In, and EOM In lines. This signal is presented to the CD adapter at a 2400 bit per second rate during the time a message is being transmitted from the device, i. e., from SOM until the parity bit following EOM.

Electrical Characteristics

A nominal signal line voltage of +3.7 volts will be used for a 1 bit, and ground will be used for a 0 bit.

Timing. The timing diagram for the CD adapter is shown in Figure 6-33.

Device Interface Pin Assignments

| I/O Connection Pin | Cable-Line Name |
| --- | --- |
| B02 | Clock Line |
| B03 | Data Line |
| B04 | SOM |
| B05 | EOM |
| B07, B13 | |
| D02, D08 | Shields |

For signal and shield terminations refer to Appendix B.
All 4 shield pins must be utilized (one shield per pin).

Device - Adapter Interface Circuit Specification

Signals between the device and the CD adapter must be driven on a transmission line that is electrically equivalent to RG62B/U, RG62A/U, or IBM Part No. 5353912. The transmission line must be terminated at each end in 100 ohms ± 5 ohms to ground. The connection between the end of the transmission line and the 100 ohm line terminator shall not exceed 6 inches. The length of transmission line from this point to the device exit connector (external cable connector point) shall not exceed 15 feet. The receiver design requirements take into account the extraneous voltages on the

transmission line due to coupled noise (+ 0.5 volt maximum) and attenuated ground shift between device and adapter circuit ground. The unattenuated ground shift between device and adapter circuit ground as governed by interframe bonding and installation environment shall not exceed + 0.5 volt.  See figure 6-33 for Notes.

Driver Requirements

There are no drivers in the CD adapter.

Receiver Requirements

The receiver output shall be interpreted as presenting a logic one when the receiver input is a logic one, and a logic zero when the receiver input is a logic zero, ground, or open.  The open input is defined as retaining the 100 ohm line termination to ground at the input to the receiver.  The equivalent circuit of the receiver presented to the transmission line shall be 1000 ohms or greater, referenced to an internal bias voltage anywhere between + 1.0 volt. The receiver must accept any voltage between + 0.9 volt as a logic zero input from the transmission line.  For the logic one input, the receiver must not require an input level from the transmission line more positive than +2.0 volts, nor be damaged by an input level of up to +6.24 volts.  the maximum length of the connector between the receiver input and transmission line is 6 inches.

Fault Condition Requirements

    1.  The signal lines may be grounded with no damage to either
        drivers or receivers.

    2.  Loss of power at either end does not cause any damage to
        either drivers or receivers.

    3.  Line operation is unaffected where power is switched off in
        any receiver or driver.

FLIGHT DATA ENTRY AND PRINTOUT ADAPTER

General Characteristics

The Flight Data Entry and Printout (FDEP) Adapter matches the interface requirements of a modified IBM 1051 Data Communications Control Unit (DCCU) operating in a half duplex mode 75 baud (bps) over non code sensitive leased telegraph facilities such as Western Union Class C channel or other common carrier schedule 3 channels.  The DCCU (hereafter referred to as the device) attached to this system will have the Telegraph Line Attachment feature installed and operate at the rate of 8.33 characters per second over this 75 baud line.

Character and Byte Formats

The transmission code is Perforated Tape and Transmission (PT & T) code (see Figure 6-34) which is 6 bit plus odd parity (C bit).

Bit Positions      S

| BA | 00 | 01 | 10 | 11 | 8421 | 00 | 01 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|
| | SP | @ | ‾ Ⓝ | ¤ | 0000 | SP | ⌽ | ⊕ | + |
| | 1 | / | i | a | 0001 | 1 | ≡ | J | A |
| | 2 | s | k | b | 0010 | 2 | S | K | B |
| | 3 | t | l | c | 0011 | 3 | T | L | C |
| | 4 | u | m | d | 0100 | 4 | U | M | D |
| | 5 | v | n | e | 0101 | 5 | V | N | E |
| | 6 | w | o | f | 0110 | 6 | W | O | F |
| | 7 | x | p | g | 0111 | 7 | X | P | G |
| | 8 | y | q | h | 1000 | 8 | Y | Q | H |
| | 9 | z | r | i | 1001 | 9 | Z | R | I |
| | 0 | FS | BR | RR | 1010 | 0 | FS | BR | RR |
| | ↕ Ⓓ | ☆ | ↓ | • Ⓨ | 1011 | → | ○ | ← | ⌽ |
| | | | | | 1100 | | | | |
| | | LF | CR | HT | 1101 | | LF | CR | HT |
| | UC | EOB Ⓑ | BS | LC | 1110 | UC | EOB Ⓑ | BS | LC |
| | EOT Ⓒ | | IL | CAN | 1111 | EOT Ⓒ | | IL | CAN |

CS = Case Shift (0-Lower, 1-Upper)
SP = Space
LF = Line Feed
CR = Carrier Return and Line Feed
HT = Horizontal Tabulation
UCS = Upper Case Shift
LCS = Lower Case Shift
EOB = Ⓑ LRC follows
BS = Backspace
EOT = Ⓒ Set Control Mode at Device
BR = Black Ribbon (Write only)
RR = Red Ribbon (Write only)
CAN = Cancel Character (Read only)
IL = Idle Character (Used after HT, CR or LF)
FS = Unused control or function code (Read only)
UCS ≣ LCS = Printer Cancel Sequence
UCS, CAN, LCS = Adapter Cancel Sequence

Figure 6-34.  PT & T Code

Each 7 bit character is preceded by a Start bit and followed by a Stop bit as shown below. The Start and Stop bits are not transferred between channel and adapter. The high order B bit is the first bit transmitted to the line following the Start bit. The Stop bit is transmitted following the C bit.

| Start | Data B | Data A | Data 8 | Data 4 | Data 2 | Data 1 | Odd Parity C | Stop |
|-------|--------|--------|--------|--------|--------|--------|--------------|------|
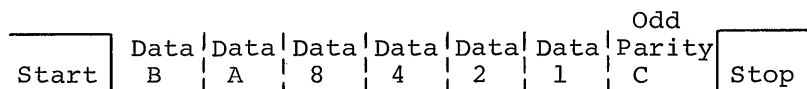
In receive mode, the adapter checks character parity on the PT & T code received, removes the character parity bit (C) and indicates correct or incorrect character parity to the channel by setting bit position "0" in the 9 bit byte transmitted to the 9020D ("1" if correct, "0" if incorrect). The adapter will monitor each data byte received (PT & T) for Upper Case Shift and Lower Case Shift characters. When the Upper Case Shift character is detected, a "1" will be set in bit position "1" of each succeeding 9 bit byte transferred to the 9020D. When the Lower Case Shift character is detected, a "0" will be set in bit position "1" of each succeeding 9 bit byte transferred to the channel. The shift characters as well as all other control function codes will be transferred to the computer storage.

In transmit mode, the adapter checks parity of the 9 bit 9020D byte, removes byte bits "P", "0" (always "1"), and "1" and adds PT&T code character parity bit "C". The adapter monitors each 9 bit 9020D byte received from the channel for a change in bit position "1" from the preceding byte. Upon sensing a change from "0" to "1" in this bit, the adapter automatically transmits an Upper Case Shift (UCS) character. Upon sensing a change from "1" to "0" in this bit, the adapter will automatically transmit a lower case shift (LCS) character. The six data bits of the byte will be transmitted immediately following the shift character. The six bits containing data are not converted nor changed in any way by the adapter.

The processor communicates with the adapter in a 9-bit byte version of the PT&T code. The data format relationship between the PT&T code (device) and the 9-bit byte version of the PT&T code (IBM 9020) is as follows:

| | Bit | Function |
|---|-----|----------|
| | P | Computer Byte Parity (odd) |
| | 0 | Character Parity Indication |
| | | Write (1) |
| | | Read: |
| | |    Correct Data Parity (1) |
| | |     Incorrect Data Parity (0) |
| 9 bit byte to/from 9020 | 1 | Case Shift: Upper (1), Lower (0) |
| | 2 | B ⎫ |
| | 3 | A ⎪ |
| | 4 | 8 ⎪ |
| | 5 | 4 ⎬ PT & T to/from Device |
| | 6 | 2 ⎪ |
| | 7 | 1 ⎪ |
| | | C ⎭ |

Modes and Message Formats

A message is transmitted or received by the adapter after a Poll to the device. Each Write or Read command is preceded by a Poll Command from the channel.

Specific character codes, which at other times may be print characters, are used between the adapter and remote DCCU, when appropriate, as mode control characters. Control character explanation is as follows:

| Control Character | Data Character or Function Code Used | |
|---|---|---|
| Ⓒ | EOT | Used only from processor as first character of a Poll command to set control mode. |
| *  Ⓓ | ↑ | 1. Ready reply from Keyboard device addressed by Poll. |
| | | 2. Control character from processor at start of a Write operation. |
| | | 3. Affirmative LRC answer from adapter to device at completion of a Read operation. |
| *  Ⓨ | . | 1. Ready reply from Printer device addressed by Poll. |
| | | 2. Affirmative LRC answer (from device) at completion of Write. |
| *  Ⓝ | − | 1. Not Ready reply from the device to a Poll. |
| | | 2. Negative LRC answer (LRC and/or VRC not correct, or Device on Write operation, or from adapter on Read operation. |
| *  Ⓑ | EOB | End of Block (EOB) at end of text from processor or Keyboard. LRC character follows. |
| *  CAN | CAN | Cancel Character (1111111). Sent to adapter when cancel key of keyboard is operated. Sent as a sequence of USC, 1111111, and LCS. All three are transferred to the processor. |
| | | 1. As a text cancellation character when the keyboard key was operated during message composition. |
| | | 2. After Ⓝ LRC answer from adapter (before timeout) for Read operation when Keyboard Cancel key was operated. |

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*When waiting for one of these responses or answers, the adapter
starts a 3 or 18 second time-out. The terminating sequence is set
if no character is received from the device within the appropriate
time limit.

Polling is accomplished by using a Poll command that functions
similar to a Write command. For each Poll command, three bytes
are sent from the processor. Sequentially, these contain the ©
control character, an alpha character to designate a station, and a
numeric character to designate the device (s) at that station. Bytes
are requested from the channel until the adapter is advised that
the byte count (which was initially 3) in the channel control word
(ccw) has gone to zero. The adapter then starts a 3 second time-
out and monitors the communication line for a response to the Poll.

Write Operation

| Function | Processor to Adapter | Adapter to Device | Adapter to Processor | Device to Adapter | Remarks |
|---|---|---|---|---|---|
| Poll Command and message | ©——→ Alpha——→ Numeric——→ <br><br>Channel Stop (Byte count = 0) | <br><br><br><br>Adapter start 3 sec timeout | | | Set control mode <br>Poll a station <br>Select a component |
| Device Response | | | | Ⓨ <br>Ⓝ | Device Ready <br>Device Not Ready <br>Reset LRC |
| Write Command and message | Ⓓ——→ <br><br><br><br>first char.——→ <br>last char.——→ <br>Ⓑ——→ <br>100000000 | <br><br><br><br><br><br><br>LRC <br>Adapter start 3 sec timeout | | | Set write text mode <br>Hold LRC reset through first character Ⓓ . <br>Set lower case <br>Text begins <br>Text ends <br>End of block, LRC follows <br>LRC character transmitted |
| Device LRC Answer | | | | Ⓨ <br><br>Ⓝ | LRC and VRC correct and message printed correctly. <br>LRC and/or VRC incorrect or message printed incorrectly. <br>Rest LRC |

Each keyboard device should be polled periodically to see if it wants access. Write as well as Read access to each device is always preceded by a Poll command to both select the device and to determine its condition.

Typical sequences of control and text characters for messages between adapter and device are presented below.

Read Operation

| Function | Processor to Adapter | Adapter to Device | Adapter to Processor | Device to Adapter | Remarks |
|---|---|---|---|---|---|
| Poll Command and message | ©———————▶ Alpha———————▶ Numeric———————▶ Channel Stop (Byte count = 0) | Adapter start 3 sec timeout | | | Set control mode Poll a station Select a component |
| Device Response | | | | Ⓓ Ⓝ | Device Ready Device Not Ready Reset LRC |
| Read Command and message | | Adapter start 3 sec timeout | ◀———first char. ◀———last char. | | Set Lower Case Text begins Text ends |
| | | | ◀———UCS ◀———1111111 ◀———LCS | | Cancel Sequence |
| | | | ◀——— LRC compare character | Ⓑ LRC | OR Enter ———┘ |
| Adapter Answer to Enter | | Ⓓ or Ⓝ Adapter start 18 sec timeout | | | LRC/VRC correct Reset LRC LRC/VRC no correct |
| Device Response to Ⓝ | | | ◀———UCS ◀———1111111 ◀———LCS | | Cancel Sequence Reset LRC |

General Description

Interfaces

The FDEP adapter provides for communication between the device and PAM Common. the adapter communicates with PAM Common over the adapter interface and with the device over the device interface.

Device Interface. The device interface is a telegraph line adapter which provides for the attachment of leased telegraph lines utilizing 62.5 ma neutral signalling non-code sensitive media. The interface is described later.

Commands

The FDEP adapter will decode commands from the channel and indicate the acceptance or rejection of the command to the channel during an initial selection cycle. Valid commands for the FDEP adapter are as follows:

Bit Positions

| Command | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Test I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control No-Op | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Sense | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Poll Normal | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| Poll Alternate | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| Write Normal | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Write Alternate | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Read Normal | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Read Alternate | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Test Poll Normal | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| Test Poll Alternate | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Test Write Normal | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Test Write Alternate | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Test Read Normal | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| Test Read Alternate | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

Any other codes with correct parity will set sense bit "0", Command Reject, and present the Unit Check bit in the status byte in response to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the FDEP adapter and no outstanding status conditions exist, a zero status byte is returned to the channel during the initial selection cycle. If status information is pending, all status bits present are transmitted to the channel.

Control No-Op (0000 0011)- The Control No-Op command is treated as an immediate type command. It performs no operation and Channel End and Device End status are transmitted to the channel during the initial selection cycle.

Sense (0000 0100)- Once the FDEP adapter has accepted a Sense command, it will initiate a service request to the channel through PAM Common. When the adapter is serviced, it will gate the contents of its sense register, with correct parity, to the channel. When the sense byte is accepted by the channel, the adapter will initiate a termination sequence.

Poll Normal (1000 1001), Poll Alternate (1001 1001)- There are two sets of relays associated with each FDEP adapter; a "normal" and an

"alternate" set. The selection of either set is under control of the command. Following the selection of the "normal" set of relays, the "alternate" transmit relay will be continuously energized (contacts open) thereby allowing line current to flow through the "normal" set of relays only. Similarly, after selection of the "alternate" set, the "normal" transmit relay is continuously energized (contacts open) and not used for data transmission. The relays remain in the last selection mode except when power is brought up, in which case the relays may come up in either mode.

The Poll Command is used to either (1) determine if the keyboard has requested service or (2) select a Printer and obtain the response indicating whether the addressed Printer is Ready or Not Ready. The numeric (component address) portion of the three character address sequence ( Ⓒ , Alpha, Numeric) supplied from the processor specifies the input or output device (s) requested. The Poll command operation, as performed by the FDEP adapter, is as follows:

1. Upon receipt of a Poll Command, the adapter will request data bytes from the channel and transmit them to the device until a channel stop is received (byte count must be set to three for a Poll Command).

    a. An LRC character is not used during a Poll.

    b. The adapter will not monitor for shift changes during a Poll.

    c. A parity error detected in any data byte will cause termination of the Poll command. Channel End, Device End and Unit Check will be set in the status byte. Sense bit 4, Data Check, will be set in the sense byte if bad parity is detected by the adapter. Sense bit 2, Bus Out Check, will be set if PAM Common detects a bad parity.

    d. The occurrence of an echo check during the poll operation will also cause termination of the command. Channel End, Device End, and Unit Check will be set in the status byte. Sense Bit 3, Echo Check, will be set in the sense byte. Refer to Sense Information, Sense Bit 3, Echo Check, for a description of this condition.

2. On detection of a channel stop, the adpater will enter a receive mode, begin a three second time-out, and monitor the communication line for a response.

    a. If the response is Ⓓ or Ⓨ , Status Modifier, Channel End and Device End are set in the status byte and the Poll operation terminated.

    b. If the response is Ⓝ , Channel End and Device End are set in the status byte and the Poll operation terminated.

    c. If the time-out ends and no response has been detected, Channel End, Device End and Unit Check are set in the status byte, and byte, and the Poll operation terminated.

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d.  If the response character received has a parity error, Status Modifier, Channel End, Device End, and Unit Check are set in the status byte, sense bit 4, Data Check, is set in the sense byte, and the Poll operation terminated.

e.  If any correct parity response character other than (D) (Y) or (N) is detected by the adapter, Status Modifier, Channel End, Device End, and Unit Check are set in the status byte, sense bit 1, Intervention Required, is set in the sense byte, and the Poll operation terminated.

3.  During any Poll termination sequence, the adapter will reset the LRC register.

Write Normal (1000 0001), Write Alternate (1001 0001)-  There are two sets of relays associated with each FDEP adapter; a "normal" and an "alternate" set.  The selection of either set is under control of the command.  Following the selection of the "normal" set of relays, the "alternate" transmit relay will be continuously energized (contacts open) thereby allowing line current to flow through the "normal" set of relays only.  Similarly, after selection of the "alternate" set, the "normal" transmit relay is continuously energized (contacts open) and not used for data transmission.  The relays remain in the last selected mode except when power is brought up, in which case the relays may come up in either mode.

A Write command must be preceded by a Poll command that selected the addressee, and obtained a (Y) (ready) response.  After the FDEP adapter has accepted a Write command, it will initiate a service request to the channel, via PAM common, for the first data byte, and set lower case mode in the adapter.

The Write operation, as performed by the FDEP adapter, is as follows:

1.  The adapter will perform a parity check on each byte.

a.  If the first byte is not a correct parity character, Channel End, Device End and Unit Check are set in the status byte, sense bit 4, Data Check, is set in the sense byte and the operation terminated.  Sense bit 2, Bus Out Check, will be set if PAM Common detected a bad parity.

b.  When the adapter is in Write text mode (after first character) a byte with bad parity will be transmitted to the device. The Write Operation will continue and Unit Check will be set in the Status byte for presentation to the channel during the next termination cycle.  Sense bit 4, Data Check, (and if PAM Common detects a bad parity also, sense bit 2, Bus Out Check) will be set in the sense byte.  The LRC register will be complemented prior to transmission of the LRC character to notify the device of an error in the message.

2.  The occurrence of an echo check during a write operation
    will cause immediate termination of the command.  Channel
    End, Device End, and Unit Check will be set in the status
    byte.  Sense Bit 3, Echo Check, will be set in the sense
    byte.  Refer to Sense Information, Sense Bit 3, Echo Check,
    for a description of this condition.

3.  Invalid characters (correct parity) will not be detected at
    the adapter nor at the device.  Program Note:  The translate
    converting EBCDIC code structure to the 9 bit byte version
    of PT & T is to convert to valid code structures only.

4.  Characters are clocked out serially to the device, in 7 bit
    PT&T code, under control of a crystal oscillator at 75 bits
    per second.

5.  The first data byte from the processor program will be a
    (D).  It will be accepted from PAM Common and transmitted
    to the device.  After transmission of the first data byte,
    the adapter will reset the LRC and enter Write text mode.

6.  When in Write text mode (after first character), the adapter
    will monitor bit position 1 in each byte for a change from
    the preceding byte.  If a change from "0" to "1" is de-
    tected, the adapter will automatically transmit an Upper
    Case Shift character to the device followed by the data
    character from bit position 2-7 of the same byte (both
    characters will update the LRC register).  A change detected
    from "1" to "0" will cause a Lower Case Shift character to
    be transmitted followed by the data character (both
    characters update the LRC register).

7.  Each character transmitted to the device in Write text mode
    (after first character up to and including  (B)  ) will
    update a 7 bit LRC register.

8.  The adapter monitors the ensuing data bytes for a  (B)
    character (case shift bit not analyzed) indicating End of
    Block, LRC to follow.  An all zero byte (with odd parity
    bit) must follow  (B)  from the processor.  The  (B)  is
    transmitted to the device followed by the contents of the
    adapter's LRC register which is inserted in the all-zero
    byte.

9.  After transmitting the LRC character, the adapter will start
    a 3 second time-out.  During this time, the adapter will be
    in a receive mode and will monitor the communication line for
    a response.

    a.  If the response is  (Y)  , Channel End and Device End
        are set in the status byte, and the operation terminated.

    b.  If the response is  (N)  , Channel End, Device End and
        Unit Check are set in the status byte, sense bit 7,
        LRC, is set in the sense byte, and the operation termi-
        nated.

c.  If the time-out ends and no response has been detected,
    Channel End, Device End, and Unit Check are set in the
    status byte, sense bit 6, Time-out, is set in the sense
    byte, and the operation terminated.

d.  If the response character received has a parity error,
    Channel End, Device End and Unit Check are set in the
    status byte, sense bit 4, Data Check, is set in the sense
    byte, and operation terminated.

e.  If any correct parity character other than  (Y)  or
    (N)  is received, Channel End, Device End, and Unit
    Check are set in the status byte, sense bit 1, Inter-
    vention Required, is set in the sense byte, and operation
    terminated.

10. If the channel byte count has gone to "0" (stop), or a Halt
    I/O instruction is issued, before termination of the Write
    operation (  (B)  received), the adapter will respond with
    Channel End, Device End and Unit Exception in the status
    byte, terminating the Write operation.

11. During any Write termination sequence, the adapter will
    reset the LRC register.

Read Normal (1000 0010), Read Alternate (1001 0010)-  There are two
sets of relays associated with each FDEP adapter; a "normal" and an
"alternate" set.  The selection of either set is under control of the
command.  Following the selection of the "normal" set of relays,
the "alternate" transmit relay will be continuously energized (contacts
open) thereby allowing line current to flow through the "normal"
set of relays only.  Similarly, after selection of the "alternate" set,
the "normal" receive relay is not used.  The relays remain in the last
selected mode except when power is brought up, in which case the relays
may come up in either mode.

    A Read command must be preceded by a Poll command that selected
the addressee, and obtained a  (D)  (ready) response.  Upon accep-
tance of a Read command, the adapter will set lower case mode and
monitor the communication line for data.  The Read operation as
performed by the FDEP adapter is as follows:

1.  The adapter will monitor the communication line for a Start
    bit.  Receipt of the Start bit will enable the adapter to
    recognize the next 7 bits as a character to be assembled
    for presentation to the channel.  Each character received
    will update a 7 bit LRC register.

2.  The adapter will monitor each assembled character for
    Upper Case Shift and Lower Case Shift characters.  When
    either the Upper Case Shift or Lower Case Shift character
    is detected, the adapter will transfer that shift character
    to the channel and cause bit position "1" (Case Shift) of
    each succeeding byte transferred to the channel to be set
    to "1" (upper case) or "0" (lower case) respectively.

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3. Bit positions 2 through 7 and the C bit of each character assembled, excluding the LRC character, will be checked for odd parity and then the C bit will be dropped. If the 7 bit character parity was good, bit position "0" (Character Parity Indicator) in the 9 bit byte transmitted to the channel will be a "1". If the 7 bit character parity was in error, bit position "0" in the 9 bit byte transmitted to the channel will be a "0". The 9 bit byte will be transmitted to the channel with correct byte parity. If a 7 bit character parity error was detected, sense bit 4 (Data Check) will be set in the sense byte and at the termination of the Read operation, Unit Check will be set in the status byte. The adapter continues to receive from the device until normal end.

4. If, during a Read, the adapter detects the first data bit (B) of a character before the preceding data byte has been accepted by the channel, the operation is terminated with Channel End, Device End and Unit Check set in the status byte, bit 5 (Overrun) set in the sense byte.

5. If, during the Read operation, a time period greater than 18 seconds elapses between consecutive characters, the acceptance of a Read command and the receipt of the first character of the message, or the transmission of the (N) response (error indication) to the device and the receipt of the reply character (normally a cancel sequence) from the device, Channel End, Device End and Unit Check are set in the status byte, sense bit 6 (Timeout) is set in the sense byte and the operation terminated.

6. The adapter will monitor the incoming message for the Cancel character (1111111). If this character is detected in the text of the incoming message, it and the next character are sent to the channel, Status Modifier, Channel End, Device End and Unit Exception are set in the status byte and the operation terminated. (The total Cancel sequence consists of UCS 1111111 LCS).

7. The adapter will monitor each assembled character for (B) (EOB character). Detection of (B) will indicate that the next character is the LRC character. The (B) is transferred to the channel and is the last character to update the LRC register. When the LRC character is received, a bit by bit "exclusive OR" compare is made between it and the accumulated character in the adapter LRC register, resulting in an "LRC compare" character. A "1" bit in any position "excluding the shift position) of the LRC compare character indicates an LRC error has occurred in that data bit position. The LRC compare character, rather than the LRC character is sent to the channel to permit later analysis by the program. An LRC compare error will cause Unit Check to be set in the status byte and sense bit 7 (LRC) to be set in the sense byte.

8.  After the LRC compare character is read by the channel, the adapter goes to transmit mode and sends an LRC answer to the device.

    a.  If the Unit Check status bit has not been set due to a parity error in any 7 bit character of the message, or a bad LRC compare, the adapter will transmit (D) to the device. Channel End and Device End are set in the status byte and the operation terminated.

    b.  If an error condition exists due to either an LRC compare error or an error in any 7 bit character of the message, the adapter will transmit (N) to the device and start an 18 second time-out. One of the following will then take place:

        (1)  If no response is detected within 18 seconds, Channel End, Device End, and Unit Check are set in the status byte, sense bit 6, Time-out, is set in the sense byte, and the operation terminated.

        (2)  If a bad parity character is detected in the device answer to the (N), Channel End, Device End, and Unit Check are set in the status byte, sense bit 4, Data Check, is set in the sense byte, and the operation terminated. The bad parity character will be the last character transferred to the channel.

        (3)  If the device response to the (N) contains the cancel character (1111111), the adapter will transfer it, plus the next character received, to the channel and terminate the operation. (Total sequence would normally be UCS 1111111 LCS). Status Modifier, Channel End, Device End, and Unit Exception are set in the status byte.

9.  If the Read operation should be prematurely terminated by the channel because of a zero byte count or a Halt I/O instruction, Channel End, Device End and Unit Exception will be set in the status byte, and the operation terminated.

10.  During any Read termination sequence, the adapter will reset the LRC register.

11.  The occurrence of an echo check during a read command will cause immediate termination of the command. Channel End, Device End and Unit Check will be set in the status byte. Sense Bit 3, Echo Check, will be set in the sense byte. Refer to Sense Information, Sense Bit 3, Echo Check, for a description of this condition.

Test Modes (001M 1001) (001M 0001) (001M 0010)- A test mode command will select the adapter in Poll/Write/Read test mode. This will degate the device interface and allow the adapter to monitor and initiate signals on the test lines from/to the Test and Monitor adapter.

Code. The code transmitted and received by the adapter is Perforated
Tape and Transmission (PT & T) as shown in Figure 6-34.

Status Information

The status byte is transmitted to the channel in the following
situations:

    1.  During initial selection.

    2.  At the termination of any adapter command.

    3.  When permitted to present stacked status.

All status bits are reset by the acceptance of the status byte by
the channel.

    Status Byte Format

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Not Used |
| 1 | Status Modifier |
| 2 | Not Used |
| 3 | Not Used |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Unit Exception |

Status Bit 1 (Status Modifier)- This bit, when set at the termina-
tion of a Poll, indicates that either (1) a Read or (2) a Write
command should be issued, depending on whether the Poll contained
(1) an input or (2) an output component address. If set with Unit
Check, the device response character to the Poll was invalid or
contained incorrect parity.

This bit when set during a Read operation (Unit Exception bit also
set) indicates that a cancel was received, (Program should re-issue
a Poll command).

Status Bits 4 and 5 (Channel End and Device End)- These bits are
always presented together by the adpater. Once set, they will
terminate the operation and will present status to the channel when
allowed to do so. These bits are set on the following conditions:

    1.  During the initial selection sequence of a Control No-Op.

    2.  After the sense byte has been accepted during a Sense
       command.

    3.  At the termination of a Poll, Write, Read or Test Mode
       command.

    4.  Upon detection of a Halt I/O condition.

Status Bit 6 (Unit Check)- Unit Check may be set during an initial selection cycle or at Channel End and Device End time of a Poll, Write, Read or Test Mode command. To enable the processor to obtain a more detailed picture of the cause of the Unit Check condition, a Sense operation should be performed. Unit Check is set at initial selection time by the following conditions:

    1.  Command Reject

    2.  Bus Out Check

It is set at Channel End, Device End time by the following conditions:

    1.  Intervention Required

    2.  Bus Out Check

    3.  Echo Check

    4.  Data Check

    5.  Overrun

    6.  Time-out

    7.  Longitudinal Redundancy Check

Status Bit 7 (Unit Exception)- Unit Exception will be set and the operation terminated under the following conditions:

    1.  Byte Count equals zero before normal end of operation (Write, Read).

    2.  Halt I/O instruction is issued (Poll, Write, Read).

In addition, during a Read operation, Unit Exception will be set with Status Modifier if a cancel character was received and transferred to the channel.

Sense Information

A sense command should be executed when the Unit Check bit is set in the status byte to determine the type of equipment or programming check associated with the previous command. The sense register positions are reset by the acceptance of the next valid Poll, Write, Read, or Test Mode command. If Bus Out Check, or Command Reject occurs during an initial selection sequence, Unit Check is set in the Status byte and all sense bits are reset with the exception of Bus Out Check or Command Reject, respectively.

Sense Byte Format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Intervention Required |
| 2 | Bus Out Check |
| 3 | Echo Check |
| 4 | Data Check |
| 5 | Overrun |
| 6 | Timeout |
| 7 | Longitudinal Redundancy Check |

Sense Bit 0 (Command Reject)- Command Reject will be set during the
initial selection sequence of a command if the bit configuration with
correct parity is other than those listed previously (Unit Check set
in status byte). All other sense bits are reset.

Sense Bit 1 (Intervention Required)- Intervention Required will be
set if any device response or answer character (correct parity) is
undefined for that control sequence. When set, this bit will term-
inate operation (Channel End, Device End, and Unit Check set in
status byte).

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set any time
a Bus Out Check signal is received over the PAM Common/adapter
interface. A Bus Out Check signal will occur any time PAM Common
detects a parity error on the Bus Out (from IOCE to PAM Common)
and the Command Out or Service Out tags are active.

A Bus Out Check detected during an initial selection sequence
will set the Unit Check bit in the status byte and reset the sense
byte with the exception of Bus Out Check. The command will be ig-
nored.

A Bus Out Check during a Poll command, or first character of a
Write, will cause the operation to be terminated (Channel End,
Device End and Unit Check will be set in the status byte). Data
Check may also be set in the sense byte if the parity error was
detected by the adapter.

A Bus Out Check during Write command in text mode will not cause
the operation to be terminated. The byte in error will be trans-
mitted and the Unit Check bit will be set in the status byte for
presentation to the channel during the next End sequence. (Data
check may also be set in the sense byte). The accumulated LRC
character will be inverted prior to its transmission to the device.

Sense Bit 3 (Echo Check)- Echo Check will be set during a Poll, Write,
or Read operation when either the normal or alternate write relay
is being used to key the line and the echo is not correct. The
Echo Check will also occur during either a Poll, Write, or Read

operation if the adapter detects an open line (continuous spacing
signal) for more than a character time or if any of the following
conditions arise on a bit by bit check:

1.  Failure of the read relay detected while writing.

2.  Conflict (Line is being used to receive and write simul-
    taneously).

Echo Check will cause the operation to be terminated (Channel End,
Device End, and Unit Check set in status byte).

Sense Bit 4 (Data Check)- Data Check will be set any time a data
byte (including a device address character) with incorret parity
is set into the adapter data register during a Poll or Write command,
or if a bad parity character is received during a Read command.  If
the Data Check condition is detected during a Write Text mode
(after first character) or a Read command, the byte in error will be
transmitted (Write) or accepted (Read; bit "0" set to zero) and the
operation will continue.  Unit Check will be set in the status byte.
If the Data Check occurred during a Write operation, the accumulated
LRC character will be inverted prior to transmission to the device.

   If Data Check is detected during a Poll command, the command
is terminated with Channel End, Device End, and Unit Check set in
the status byte.

Sense Bit 5 (Overrun)- Overrun will be set on a Read operation if
the first data bit of a data byte is received before the preceding
data byte is accepted by the channel.  Overrun will terminate the
operation (Channel End, Device End, and Unit Check set in status
byte).

Sense Bit 6 (Timeout)- Timeout is set whenever a Line timeout occurs.
There are two timecuts possible.

1.  Three (3) second timeout; when the adapter is waiting for a
    response to a poll or an answer to an LRC character (Write
    operation).

2.  Eighteen (18) second timeout; when the adapter detects a
    mark of 18 seconds between successive characters of text
    during a Read Operation, when the first character of a can-
    cel sequence is not received within 18 seconds after the
    adapter has sent a negative response  (N)  to a Read LRC, or,
    if the first character of a message is not received within
    18 seconds after the acceptance of a Read command.

Timeout will set Channel End, Device End and Unit Check in the status
byte and terminate the operation.

Sense Bit 7 (Longitudinal Redundancy Check)- LRC will be set at the
completion of a Write operation if a  (N)  is detected as the LRC
response from the device.  It will also be set if a bad LRC compare
is detected during a Read operation.  Channel End, Device End and
Unit Check will be set in the status byte.

Priority

The priority position is address dependent, i. e., the lower the
address within a group the higher the priority.  To upgrade or
downgrade the priority of a particular adapter, the address of the
adapter must be changed accordingly.  The reassignment of the
priority (and address) is changeable in the field.

Interface

The receive and transmit relays are housed in the PAM unit.  These
relays are mercury wetted relays manufactured by C. P. Clare Co.,
assembly number HGS 4Y 1042.  The resistance seen by the line is 91
ohms $\pm$ 10%.  The coils operate with a nominal current of 62.5 ma.
and have a 2 msec pick and drop time.  A constant current is applied
to the receive relay bias winding.  A potentiometer in series with
the bias winding is pre-adjusted for proper output response of the
receive relay.

<div align="center">

FDEP Adapter Device Interface Pin
Assignments

</div>

| I/O Connector Pin | Cable-Line Name |
|---|---|
| A | Device Line |
| B | Device Line Return |
| H | Cable Shield |

Distortion Definitions:

Normal Bit Period (NBP)-  non-distorted bit length as determined by
a specified bit rate of 75 bits per second.

Normal Character Start-  the start of a normal character is referenced
to the transition from a stop bit or idle status to a start bit.

Receive Distortion Tolerance-  Using the transition from the stop bit
or idle status to the start bit, the start bit must be no shorter
than 60% of the normal bit period.  Any succeeding bit of the
character may be shortened by 40% from the leading edge and 40% from
the trailing edge of a normal bit location in a normal character.  A
normal character with a zero time reference at the start bit transi-
tion is shown below (Figure 6-35) where shaded areas show the amount
of distortion that can be tolerated.

Transmit Distortion-  the transmit distortion will not exceed $\pm$ 5%.

Timing Diagrams.

See Figures 6-36 and 6-37.

Circuit Schematic.

See Figure 6-38.

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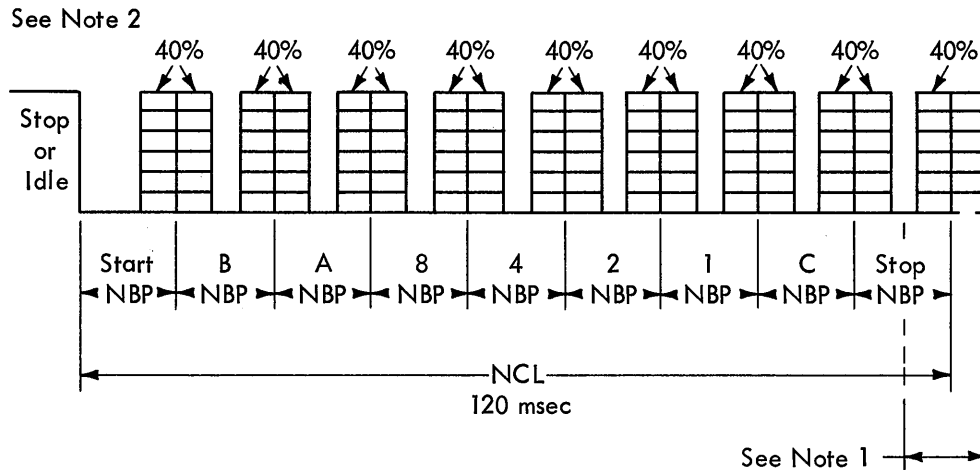
NOTE 1:   During Read, maximum time between Stop bit and
          next Start bit is 18 seconds (Timeout).

NOTE 2:   All percentages refer to the Normal Bit Period
          (NBP).

Figure 6-35.   Normal Character with Zero Time Reference (75 bits per
               second)

BUFFER PROCESSOR ADAPTER

General Characteristics

The Buffer Processor adapter provides the capability of operationally
attaching a Univac type 1900 Buffer Processor (BP) to a 7289-2
Peripheral Adapter Module (PAM).  Data transfer on the adapter-BP
interface is bit serial-character serial; each character composed
of 6 data bits plus odd parity.  On both input and output data trans-
fers, the adapter will initiate the operation and control it in a
synchronous manner at an 81.6 kilocycle bit rate over half duplexed
lines.

Character and Byte Formats

Any 6 bit plus odd parity transmission code may be used on the adapter-
BP interface.  Data is both received and transmitted in a high order
bit of high order character to low order bit of low order character
sequence.  The adapter does no data character decoding nor code
modification in the process of data transfer, nor is any unique
character or bit detection performed.

        During a Read operation, the BP adapter inserts the 6 bit
plus odd parity BP character into the low order seven bits of a 9020D
byte; the high order bit within the byte will contains "zero".

Read

Data Cycle

Gate Data on Bus In

Device Interface

Start | B | A | 8 | 4 | 2 | 1 | C | Stop    Start | B | A | 8 | 4 | 2 | 1 | C | Stop

Sample Time
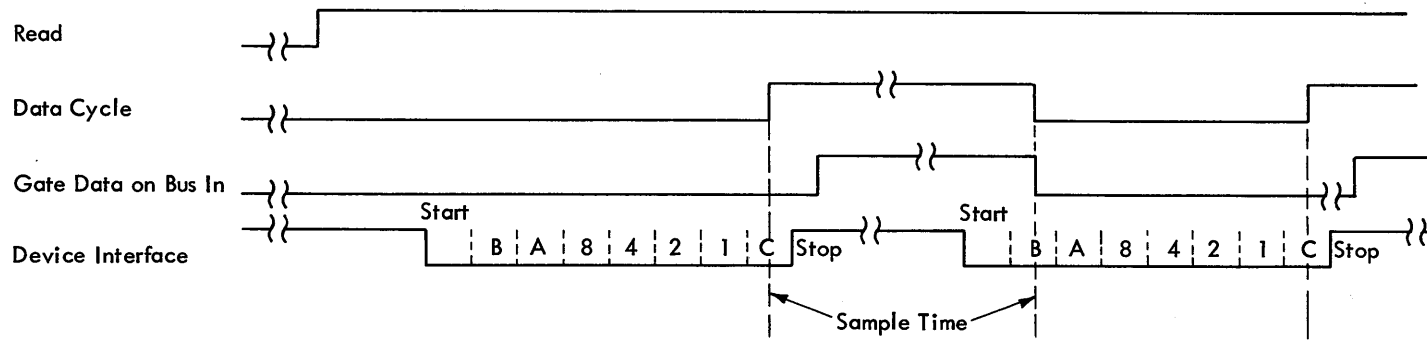
Figure 6-36. FDEP Timing Diagram for Read Operation

Poll or Write

Data Cycle

Gate Data to Adapter

Device Interface

Start | B | A | 8 | 4 | 2 | 1 | C | Stop    Start | B | A | 8 | 4 | 2 | 1 | C | Stop
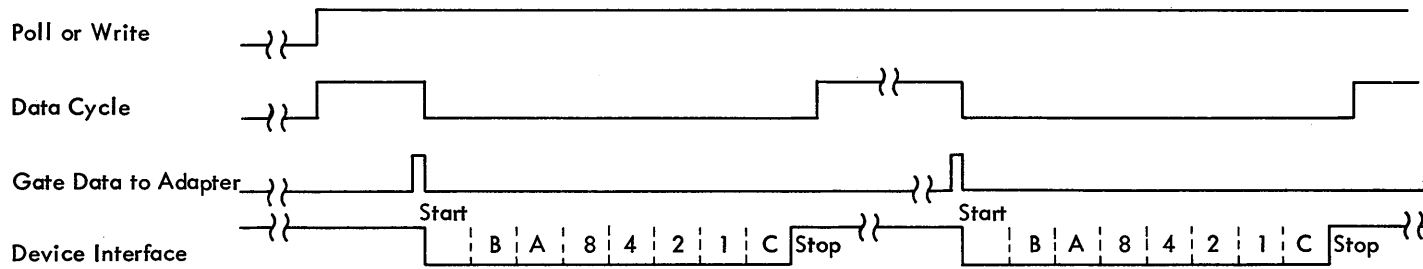
Figure 6-37. FDEP Timing Diagram for Poll or Write Operation
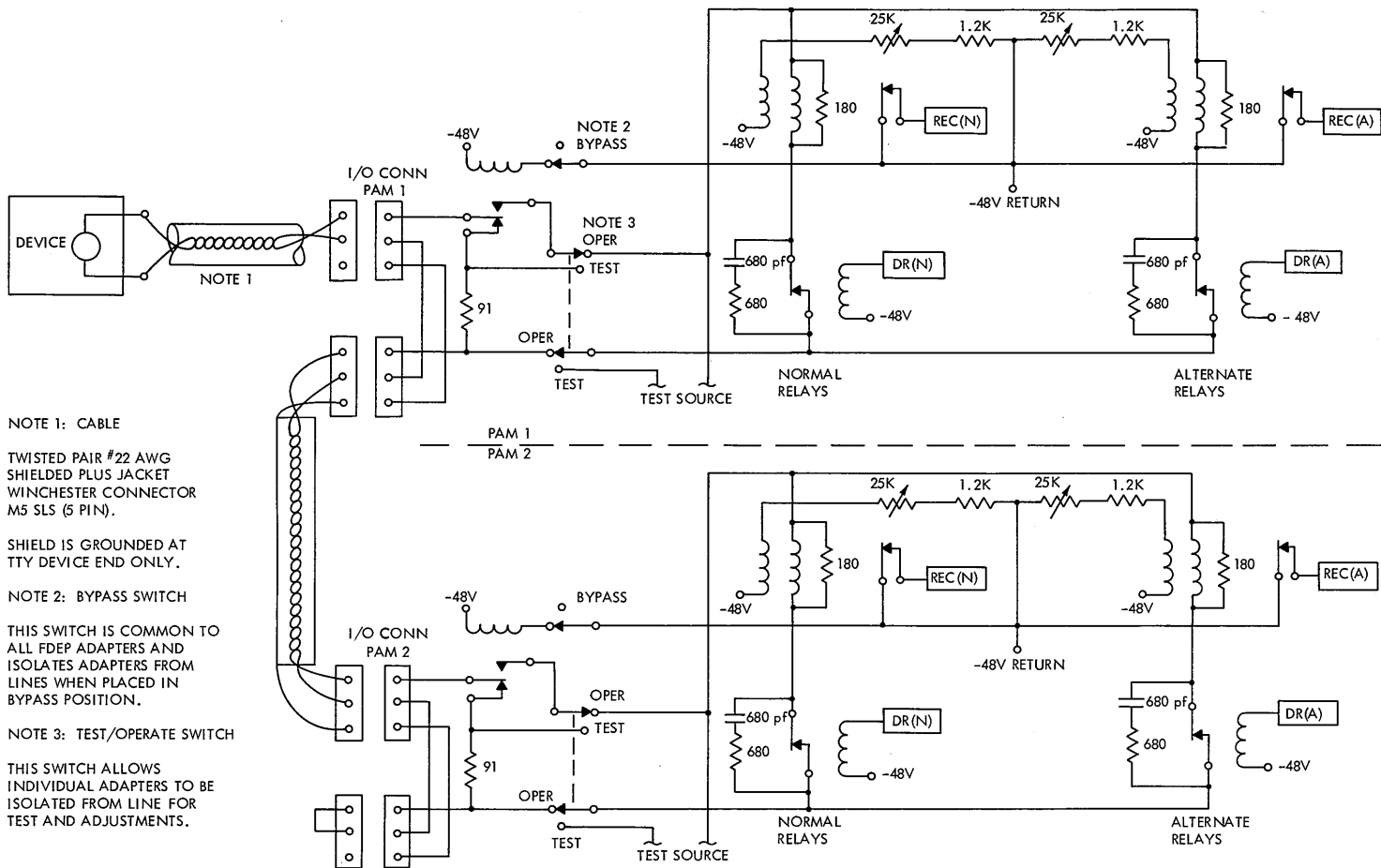
Figure 6-38. FDEP Interface Circuit Schematic

NOTE 1: CABLE

TWISTED PAIR #22 AWG
SHIELDED PLUS JACKET
WINCHESTER CONNECTOR
M5 SLS (5 PIN).

SHIELD IS GROUNDED AT
TTY DEVICE END ONLY.

NOTE 2: BYPASS SWITCH

THIS SWITCH IS COMMON TO
ALL FDEP ADAPTERS AND
ISOLATES ADAPTERS FROM
LINES WHEN PLACED IN
BYPASS POSITION.

NOTE 3: TEST/OPERATE SWITCH

THIS SWITCH ALLOWS
INDIVIDUAL ADAPTERS TO BE
ISOLATED FROM LINE FOR
TEST AND ADJUSTMENTS.

On output operations, the adapter serializes the low order
seven bits of the 9020D byte onto the BP device data lines.

These seven bits must contain odd parity when received from
the channel as the adapter does not generate a character parity bit.
(While the adapter will check for correct byte parity, the 7 bit
character parity will not be checked before transmission during a
Write operation).

Data Output

Data format in 9020 core storage;



Byte address
in core       X                                    X+3

Order of bit
transfer to BP      1 2 3 4 5 6 7        8 9 10 11 12 13 14      15 etc.
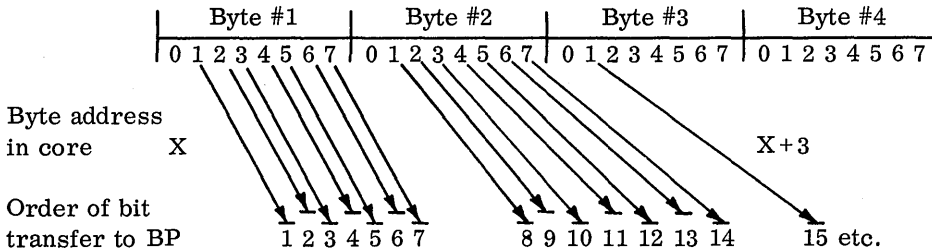
NOTE* Zero bit is stripped from 9020 byte.

The significance of the character bits are reversed between the
adapter and the device, i.e., bit 1 of the adapter byte is the MSB
of the character, where as this bit is placed in the LSB position
of the device character.

Data Input

Order of bit
transfer from BP   1 2 3 4 5 6 7  8 9 10 11 12 13 14     15 etc.

Data format in
9020 core storage



          0 1 2 3 4 5 6 7   0 1 2 3 4 5 6 7   0 1 2 3 4 5 6 7   0 1 2 3 4 5 6 7
             Byte #1            Byte #2            Byte #3            Byte #4
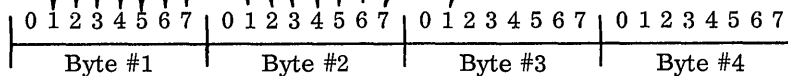
Byte address
in 9020 core    X                                    X+3

NOTE* Zero bit is padded into 9020 byte (zero insert).

The significance of character bits are reversed between the adapter
and the device, i.e., bit 1 of the adapter byte is the MSB of the
character, where as this bit is placed in the LSB position of the
device character.

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## Message Formats

Output messages to the Buffer Processor may contain a maximum of 256 characters. Within this maximum, a message must contain either k, l, m, or n bytes, where k, l, m and n are each a multiple of four bytes. Input messages from the Buffer Processor are a fixed length of p bytes, where p is equal to a multiple of four, minus one.

## Operational Description

Data transfer to and from the Buffer Processor is performed via Poll, Read and Write commands.

The Poll command is so constructed as to require a minimum of channel time; that is, upon acceptance of a Poll, the adapter will independently continue to cycle through a polling sequence until terminated by either the channel (Halt I/O) the adapter (error condition) or the device (request for service). The occurrence of anyone of these conditions will cause the adapter to terminate to poll operation with appropriate status and sense (if applicable) bits set.

Read and Write commands are each composed of three functional operations; (1) an adapter-BP communication initiation sequence, (2) a data transfer, and (3) an adapter-BP communication termination sequence.

The initiation sequence within each of these commands allows the adapter to interrogate both the device condition(Ready or Not Ready) and its status. Upon receipt of positive responses, the adapter will present the related command to the BP. Error conditions noted during this sequence (e.g., device not ready, no device response, incorrect device response, or, during a Write, Device Status Line X) will cause the operation to terminate with Channel End set in the status byte. Other status and sense bits, which may be set as a result of an error condition, will be presented at Device End time.

NOTE: Device End status will be available to the channel as soon as the adapter clears the BP (i.e., BP in the Demand Clear state); the channel may or may not receive Device End and Channel End together, depending on channel service time.

Upon successful execution of an initiation sequence, the adapter enters a data transfer mode to either transmit (Write) or receive (Read) data. During this data transfer mode, any termination of operation caused by either the channel (Halt I/O or byte count equals zero) or an adapter error condition (parity error or overrun) will set Channel End.

Upon completion of the data transfer sequence (either completed or terminated by an error condition), the adapter enters a communications termination sequence. During this last sequence, the

adapter continues to interrogate the device until BP status is available on the previous data transfer, if any. The adapter will appear busy to all commands from channel acceptance of Channel End until the adapter has received final device status and has set Device End in the status byte. Commands other than Test I/O will continue to receive a Busy indication until the channel has accepted Device End status. Device status and data transfer error indicators (if applicable) will be available at Device End time. However, adapter detected error conditions occurring during this termination sequence will cause the adapter to terminate (present Device End) the operation without final device status.

A maximum flexibility is incorporated into the adapter in view of the fact that the adapter interfaces two programmed devices. For example, the command modifier bits (see description of commands) are not interrogated by the adapter but merely passed onto the BP. The device status lines are also adaptable to any 9020D-BP mutual agreement within the following restrictions:

Device Status Line W - will stop a Poll and set Status Modifier. It will also set Status Modifier, if active, on completion of a Read or Write.

Device Status Line X - will prevent the initiation of a Write Command.

General Description

Interfaces

The BP adapter provides for communication between the device and PAM common. The BP adapter communicates with PAM common over the adapter interface and with the BP over the device interface.

Device Interface

The thirty-one device interface lines between the BP adapter and the BP are listed below and described later. For the purposes of clarity, the references to "In" and "Out" are related to the adapter ("Out"-adapter to BP; "In" BP to adapter).

    2 Data In Lines (one for 1 bits; one for 0 bits)
    2 Data Out Lines (one for 1 bits; one for 0 bits)
    5 clock Out Lines (TA, TB, TA1, TA7, TB7)
    4 Device Status In Lines (W, X, Y, Z)
    7 Device Control Out Lines (a, b, c, d, e, f, g)
    1 Test Out Line
    1 Ready In Line
    1 Not Ready In Line
    1 Demand Out Line
    1 Special In Line
    1 Memory Request In Line
    1 Transfer Demand Station In Line

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1 Demand Clear Out Line
1 Initiate and Terminate Buffer Transfer Out Line (RMA6)
1 Demand In Line
1 Selective or General Reset Out Line

Commands

The BP adapter will decode commands from the channel and indicate the acceptance or rejection of the command to the channel during a select cycle. The valid commands for the BP adapter are as follows:

Command                                        Code

| | a b c d e f g |
|---|---|
| BP Interface Line | a b c d e f g |
| 9020D Bit Position | 0 1 2 3 4 5 6 7 |

| Command | Code |
|---|---|
| Test I/O | 0 0 0 0 0 0 0 0 |
| Control No-Op | 0 0 0 0 0 0 1 1 |
| Sense | 0 0 0 0 0 1 0 0 |
| Poll | 1 0 0 0 1 0 0 1 |
| Test Poll Mode | 0 0 1 0 1 0 0 1 |
| Read | 1 M 0 M 0 M 1 0 |
| Test Read Mode | 0 M 1 M 0 M 1 0 |
| Write | 1 M 0 M 0 M 0 1 |
| Test Write Mode | 0 M 1 M 0 M 0 1 |

M = Modifier (may be either a 0 or 1)

Any other codes with correct parity will set sense bit zero, Command Reject, and present the Unit Check bit in the status byte in response to the command.

Test I/O (0000 0000)- If the Test I/O command is accepted by the BP adapter and no outstanding status conditions exist, a zero status byte is returned to the channel during the initial selection cycle (See description of Busy Status). If status information is pending, all status bits present are transmitted to the channel.

Control No-Op (0000 0011)- The Control No-Op command is treated as an immediate type command. It performs no operation and Channel End and Device End status are transmitted to the channel during the initial selection cycle.

Sense (0000 0100)- Once the BP adapter has accepted a Sense command, it will initiate a service request to the channel through PAM Common. When the adapter is serviced, it will gate the contents of its sense register, with correct parity, to the channel. When the sense byte is accepted by the channel, the adapter will initiate a termination sequence.

Poll (1000 1001)- The BP adapter Poll command provides a method of determining the device condition and status. Should the adapter detect a device Not Ready condition during the Polling sequence,

Channel End is set in the status byte and the operation terminated. Upon subsequent clearing of the device, the adapter will present Unit Exception (status bit 7) and Device End to the channel. If, however, the device is ready, the adapter will then interrogate device status. Should the device signal that traffic is available (via Device Status Line W), Channel End is immediately set in the status byte. The adapter will present Status Modifier (Status bit 1) and Device End after issuing a Demand Clear to the device. If the device status reflects a no traffic available condition, the adapter will continue interrogating both device condition (Ready-Not Ready) and device status (Traffic-No Traffic). This interrogation sequence will continue until either (1) one of the above terminating conditions is detected, (2) a channel Halt I/O is received, or (3) an error condition is noted. The error conditions possible during this command are as follows:

    1.   Timeout. The device failed to respond to an adapter inquiry within the predefined time limits. The Poll is terminated immediately with Channel End set in the status byte. After clearing the device, Timeout (Sense bit 6) is set and Unit Check (Status bit 6) and Device End (Status Bit 5) are presented to the channel.

    2.   Invalid Response Line. The device brought up an invalid signal line sequence; Channel End is set and the operation terminated. The adapter will then proceed to send a Demand Clear to the device and subsequently present Unit Exception (Status bit 7) and Device End (Status bit 5) to the channel.

Read (1M0M0M10)- Upon receipt of a Read command, the adapter will initiate communications with the device via a request for the device condition (i.e., Ready or Not Ready). Should the device return a Not Ready indication, the adapter will terminate the operation with Channel End set in the status byte. After clearing the BP, the adapter will present Unit Exception (Status bit 7) and Device End (Status bit 5) to the channel. A Ready condition will cause the adapter to demand device status and subsequently transfer the command to the device. (No action is taken on the device status). The Read command transferred to the device is composed of the low order seven bits of the command from the channel (M0M0M10). Acknowledgement of the command by the device will result in the initiation of a data transfer from device to channel. Any error condition noted by the adapter before the start of a data transfer will cause an immediate termination of the command with Channel End presented in the status byte. Follow-on sense and status indications set are dependent on the type of error condition and will be presented with Device End (status bit 5) as soon as the adapter clears the BP. Possible error conditions during this sequence are as follows:

    1.   Timeout (Sense bit 6) set in the sense byte and Unit Check (Status bit 6) set in the status byte indicates that the device did not respond to an adapter inquiry control line within the predefined time limits.

2. Unit Exception (Status bit 7) set in the status byte will indicate that an invalid device control line sequence was noted by the adapter.

Once the adapter has begun a synchronous data transfer, the data will be transferred to the channel via a four byte buffer in four byte bursts. Each byte will be parity checked at the adapter. As the shift register becomes full, the four bytes will be transferred to the buffer and a subsequent request made for channel service. Should, at any time during this data transfer, the adapter note that both the shift register and the buffer are full, an overrun condition will exist. The data transfer will cease and Channel End will be presented to the channel. Parity errors noted by the adapter during the data transfer will also cause immediate termination of the data transfer with Channel End being presented to the channel. After either of these error conditions, the adapter will continue to interrogate the device condition until a Ready response is received.

At this time, the device status will be requested and presented to the channel with Device End (Status bit 5). Those sense and status indications (i.e., Unit Check (Status bit 6) and Overrun (Sense bit 5) or Data Check (Sense bit 4) for the overrun and parity error condition, respectively) resulting from error conditions detected in the data transfer will also be presented at this time.

On an error free data transfer, the adapter will present Channel End upon detection of a channel stop (byte count equal to zero). The adapter will subsequently demand device status and present such status, if any, to the channel with Device End (Status bit 5). (See description of device status line indicators in both the sense and status byte).

Any error conditions detected by the adapter during the device ending sequence (i.e., obtaining device condition and status), such as timeouts or invalid signal line sequences, will cause immediate termination without device detected status. However, Device End (Status bit 5) will be presented along with status reflecting the terminating error condition as well as any pending adapter status from data transfer error conditions which were detected by the adapter Appropriate sense bits will then be available.

Write (1M0M0M01)- Upon receipt of a write command, the adapter will initiate communications with the device via a request for device condition. A Not Ready response from the device will cause the adapter to terminate the command with Channel End being presented to the channel. After issuing a Demand Clear to the device, the BP adapter will present Unit Exception (Status bit 7) and Device End (Status bit 5), reflecting the terminating condition. A ready response from the device allows the adapter to request device status. If Device Status Line (DSL) X is active, the operation is immediately terminated (Channel End presented to the channel). Upon clearing the device, the adapter will set DSL X (Sense bit 1), Unit Check (Status bit 6), and Device End (Status bit 5). Should no device status be present, or only status other then DSL X, the adapter pre-

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sents the Write command to the BP (low order seven bits of the channel command, M0M0M01). A correct command acknowledgement from the device causes the adapter to initiate a data transfer from the channel to the device.

Any error condition noted by the adapter before the start of a data transfer will cause an immediate termination of the command with Channel End being presented to the channel. The adapter will subsequently issue a Demand Clear to the device and set the appropriate status and sense bits with Device End (Status bit 5). Possible error conditions during this pre-data transfer sequence are as follows:

1. Timeout (Sense bit 6). Set with Unit Check (Status bit 6) if the device did not respond to an adapter inquiry control line within the predefined time limits.

2. Unit Exception (Status bit 7). Set if an invalid device control line sequence was detected by the adapter.

The data transfer from the channel to the adapter buffer will be performed in four byte bursts. If each byte within the burst contains correct parity, the bytes are transferred (four byte parallel) to the shift register for bit serial synchronous transfer to the device. The channel to adapter data transfer will be terminated and Channel End presented to the channel if either a parity error or overrun condition is detected. Either of these conditions will cause the adapter to transmit a seven zero-bit character (bad parity) to the device. The adapter will then continually interrogate the device until a Ready response is received, at which time the device status is requested. Device status as well as the following defined indications for overrun and parity error conditions encountered during the data transfer, will be presented with Device End (Status bit 5).

1. Overrun. If the adapter buffer is not full when the shift register requests the next four bytes, an overrun condition exists. Overrun (Sense bit 5) and Unit Check (Status bit 6) are set.

2. Parity Error. If either or both the adapter and PAM Common detect a parity error, the transfer is terminated. Unit Check (Status bit 6) and either or both Data Check (Sense bit 4), and Bus Out Check (Sense bit 2) are set, for adapter or PAM Common detected parity errors, respectively.

An error free data transfer will continue until channel stop is received from the channel (byte count equals zero). Channel End is presented at this time. The adapter will then interrogate the device and upon receipt of a Ready response, request device status. Device status, if any, will be presented to the channel along with Device End (Status bit 5).

As in a Read command, any error conditions detected by the adapter during the device ending sequence (i.e., obtaining device condition and status), such as timeouts or invalid signal line sequences, will cause immediate termination without device detected

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status.  However, Device End (Status bit 5) will be presented along
with status and sense reflecting the terminating error condition as
well as any pending adapter status or sense from data transfer error
conditions which were detected by the adapter.


Test Modes (0010 1001) (0M1M 0M10) (0M1M 0M01)- A test mode command
will select the adapter in Poll/Read/Write Test Mode.  This will de-
gate the device interface and allow the adapter to monitor and ini-
tiate signals on the test lines from/to the Test and Monitor adapter.

Operational Termination- In the process of terminating the operation
during a Poll, Read or Write command for any of the conditions indi-
cated in the description of these commands, the adapter takes the
action necessary to reset the device interface logic (put the device
"off" demand).

        The action necessary depends upon the sequence in which
termination is initiated.  These are summarized below:

| Command | | Sequence | Adapter Action |
|---|---|---|---|
| Poll | | Any Termination | Demand Clear |
| Read or Write | a. | Before Memory Request | Demand Clear |
| | b. | After Memory Request but before first RMA6 | RMA6, RMA6, Demand Clear |
| | c. | After first RMA6 | RMA6, Demand Clear |
| | d. | After second RMA6 | Demand Clear |

It should be noted that the adapter will not attempt to clear the
device if a channel reset is received at the adapter.

Status Information

The status byte is transmitted to the channel in the following
situations:

    1.  During initial selection.

    2.  At the Termination of any adapter command.

    3.  When permitted to present stacked status.

    4.  To present Device End signal to the channel.

Status Byte Format:

| Bit | Designation |
|---|---|
| P | Parity |
| 0 | Not Used |

| Bit | Designation |
|-----|-------------|
| 1 | Status Modifier (Device Status In Line W) |
| 2 | Not Used |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Unit Exception |

Status Bit 1 (Status Modifier)- This bit, when set at the termination of a Poll, a Read or a Write indicates that the device has traffic for the adapter (Device Status Line W active).

Status Bit 3 (Busy)- A busy condition for the adapter is set up under the following conditions:

1.  After the Initial Selection phase of a Poll, Read, Write or Sense.

2.  Any time status is stacked.

The busy condition is reset by the acceptance of the Device End status bit. The busy status is sent to the channel during initial selection under the following conditions:

1.  New commands other than Test I/O.

    a.  After Channel End has been presented to the channel until Device End has been accepted by the channel.

2.  Test I/O.

    a.  After Channel End has been presented to the channel but Device End has not occurred.

Status Bit 4 (Channel End)- The Channel End status bit is set by the adapter on completion of the portion of an I/O operation involving transfer, if any, of data or control information between the device and channel.

1.  Control No-Op is an immediate type command which will set Channel End status during Initial Selection.

2.  A sense operation will set Channel End after transferring one data byte consisting of the contents of the sense register.

3.  A Poll operation will set Channel End upon receiving a Channel halt (Halt I/O), encountering an error condition, or detecting an active Device Status Line W.

4. A Read or Write operation will send Channel End to indicate end of data transfer after any of the following conditions:

   a. Channel Stop (byte count = 0).

   b. Error condition detected by the adapter.

   c. Halt I/O

Status Bit 5 (Device End)- This bit, when set, indicates that the adapter has terminated communications with the device.

   1. Control No-Op, an immediate type command, will send Device End and Channel End together during initial selection.

   2. Sense commands will send Device End with Channel End after transferring one byte of sense information.

   3. During a Poll Device End is set with appropriate status and sense bits describing the termination condition.

   4. Device End will be set on Read and Write operations when the device enters a Ready condition and presents its status or an error condition occurs before initiation of a data transfer.

Status Bit 6 (Unit Check)- The Unit Check bit may be set during initial selection or at Device End time. During initial selection, this bit is set if either Command Reject or Bus Out Check is set in the sense byte. At device end time, Unit Check is set if any sense bit is set.

Status Bit 7 (Unit Exception)- Unit Exception will be set with Device End if the adapter detects a device Not Ready condition or an improper device control line response. (See description of BP control lines).

Sense Information

A Sense command should be executed when the Unit Check bit is set in the status byte to determine the type of equipment or programming check associated with the previous command. The sense register positions are reset by the acceptance of the next valid Write, Poll, Read or Test Mode command. If Bus Out Check or Command Reject occurs during an initial selection sequence, Unit Check is set in the Status byte and all sense bits are reset with the exception of Bus Out Check or Command Reject, respectively.

Sense Byte Format

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |

| Bit | Designation |
|-----|-------------|
| 1 | Device Status Line X |
| 2 | Bus Out Check |
| 3 | Device Status Line Y |
| 4 | Data Check |
| 5 | Overrun |
| 6 | Timeout |
| 7 | Device Status Line Z |

Sense Bit 0 (Command Reject)- Command Reject will be set during the initial selection sequence of a command if the bit configuration, with correct parity, is other than those listed previously.  (Unit Check set in status byte).  All other sense bits are reset.

Sense Bit 1 (Device Status Line X)- This bit will be set whenever the adapter detects an active Device Status Line (DSL) X.  This DSL is interrogated on completion of a Read or Write operation (will be presented, if active, with Unit Check and Device End), and on initiation of a Write.  If DSL X is active on the initiation of a Write, the operation is terminated with Channel End.  Unit Check and Device End are set in the status byte after the device is put "off" demand.

Sense Bit 2 (Bus Out Check)- Bus Out Check will be set at any time a Bus Out Check Signal is received over the PAM Common/adapter interface.  A Bus Out Check signal will occur any time PAM Common detects a parity error on the Bus Out (from IOCE to PAM Common) and the Command Out or Service Out Tags are active.

A Bus Out Check detected during an initial selection sequence will set the Unit Check bit in the status byte and reset the sense byte with the exception of Bus Out Check.  The command will be ignored.

A Bus Out check during a Write operation will cause termination of the operation.  The byte in error will not be transferred to the device; the adapter will transfer the contents (if any) of the shift register plus a bad parity character (seven zeroes) to the device to notify the device of an error condition.  The data transfer will cease (Channel End presented to the channel) and the device placed "off" demand.

Bus Out Check will be set with Unit Check at Device End time.

NOTE:  The last correct parity character received at the device is not necessarily the last correct parity character received by the adapter from the channel.

Bus Out Check may only occur during initial selection for the remaining commands.

Sense Bit 3 (Device Status Line Y)- The Device Status Line (DSL) Y bit will be set upon completion of a Read or Write operation (at Device End time) if DSL Y is active.  This line represents device status on the last message transferred.

Sense Bit 4 (Data Check)- Data Check will be set any time a data
byte with in correct parity is received at the adapter from either
the channel or the device. (Byte parity on Write-character parity
on Read). Upon detection of a data check condition, the adapter
will cease data transfer. If detected during a Read operation, the
adapter will signal the device to go "off" demand and present
Channel End to the channel. During a Write command, a data check
condition will cause the adapter to transmit a bad parity character
(seven zeroes) to the device before signalling it to go "off" demand.
Unit Check will be presented to the channel, at Device End time.

Sense Bit 5 (Overrun)- The Overrun bit will be set whenever a Read or
Write overrun condition is detected by the adapter. During a Read,
an overrun condition exists if, at any time, both the buffer and the
shift register are full. Overrun during a Write occurs if the buffer
is not full when the shift register requests the next four bytes.

Overrun on either a Write or Read will cause immediate data
transfer termination. (If occurring during a Write, seven zeroes are
transferred to the device). The device is put "off" demand and
Channel End is presented to the channel. Unit Check is presented at
Device End time.

Sense Bit 6 (Timeout)- The Timeout bit is set if the device fails to
respond to a control line inquiry from the adapter within the prede-
fined time limits. These limits are as follows:

| Response to | Time Limit |
| --- | --- |
| Test Out | 12.25 usec. |
| Demand Out | 98 usec. |
| C → I/O (Command) | 1 msec.(± 25%) |

These conditions result in an immediate termination with Channel
End or Unit Check and Device End (depending on when it occurs) being
presented to the channel.

Sense Bit 7 (Device Status Line Z)- The Device Status Line (DSL) Z
bit will be set at the completion of a Read or Write operation (at
Device End time) if DSL Z is active. This line represents device
status on the last message transferred.

Priority

The priority position is address dependent; i.e., the lower the
address assigned the high ther priority. To upgrade or downgrade the
priority of a particular adapter, the address of the adapter must be
changed accordingly. The reassignment of the priority (and address)
is changeable in the field.

Interface Description

The Buffer Processor interface provides a method of attaching a
UNIVAC Buffer Processor, used in the existing Computer Updating

Equipment and Remote Strip Printing subsystems, to the 7289-2 Peripheral Adapter Module (PAM). The Buffer Processors were designed to interface with a UNIVAC File II processor and the BP adapter essentailly simulates the File II interface characteristics for the BP. Data and control communication are accomplished in a synchronous manner as related to the adapter clock pulses. Each interface can accommodate half duplex (one direction at a time) communication with one BP. The Buffer Processor adapter is not designed to function in a duplexed adapter configuration.

The signal lines for the BP adapter interfaces are as follows: (For the purposes of clarity references to "In" and "Out" are associated with the Adapter, i.e., Out-Adapter to BP; In-BP to Adapter.

| Clock Lines | Initiated By |
|---|---|
| TA Out | Adapter |
| TB Out | Adapter |
| TA1 Out | Adapter |
| TA7 Out | Adapter |
| TB7 Out | Adapter |

| Data Lines | Initiated By |
|---|---|
| Data Out logic "1" level | Adapter |
| Data Out logic "0" level | Adapter |
| Data In logic "1" level | BP |
| Data In logic "0" level | BP |

| Control Lines | Initiated By |
|---|---|
| Test Out | Adapter |
| Ready In | BP |
| Not-ready In | BP |
| Demand Out | Adapter |
| Demand In | BP |
| Special In | BP |
| Device Status In Line 4 (W) | BP |
| Device Status In Line 1 (X) | BP |
| Device Status In Line 2 (Y) | BP |
| Device Status In Line 3 (Z) | BP |
| Device Control Out a | Adapter |
| Device Control Out b | Adapter |
| Device Control Out c | Adapter |
| Device Control Out d | Adapter |
| Device Control Out e | Adapter |
| Device Control Out f | Adapter |
| Device Control Out g | Adapter |
| Memory Request In | BP |
| Transfer Demand Station In | BP |
| RMA6 Initiate and terminate Buffer | Adapter |
| Demand Clear Out | Adapter |
| Selective or General Reset Out | Adapter |

Line Description

Clock Out Lines (TA, TB, TA1, TA7, TB7)- The clock lines are presented
by the adapter to the BP to synchronize transmission of data bits and
control pulses between the adapter and the BP.  The adapter clock
generates TA and TB pulses at an 81.6 KC rate (12.25 microseconds
between consecutive TA or TB pulses) with TA pulses leading TB by
6.125 microseconds.  The TA1 pulse designates which of the TA
pulses is considered number 1 and reoccurs every seven TA pulses.
The TA7 pulse designates which of the TA pulses is considered number
7 (six pulses after TA1) and reoccurs every seven TA pulses.  The
TB7 pulse designates which of the TB pulses is number 7 (actually the
TB pulse following the TA7 pulse) and reoccurs every seven TB pulses.
The timing diagrams designate the relationship of the data bits and
control pulses to the various clock pulses.  These clock pulses will
be transmitted from the BP adapter as long as power is applied to
the BP adapter within the PAM.  When the BP adapter has power applied
and is not in Test mode, i.e., Test Poll mode, Test Read mode or
Test Write mode Command, clock pulses will be transmitted consistent
with the 81.6 Kilo Hertz rate.  When the BP adapter is in Test mode,
the clock pulses transmitted will be under control of the test vehi-
cle, (Test Out line 1 commands to the TAM adapter or the Test Out
line 1 switch on the PAM Maintenance and Test Panel) at a variable
rate and may not necessarily consist of a complete sequence of clock
pulses, i.e., TA1, TB1, TA2, Reset, TA1).  During the time that the
adapter is entering or leaving a test mode, the clock pulses may not
always occur in sequence.  The adapter when entering a test mode will
cause the clock to be reset.  Therefore, the first clock pulse to be
distributed to the Buffer Processor after the adapter is put in a
test mode will be a TA1.  When leaving the Test mode, the first com-
plete clock pulse sequence (TA1 through TB7) is unpredictable.

Data Lines (Data In "1", Data In "0", Data Out "1", and Data Out "0")-
There are two sets of data lines associated with this interface.  One
set transmits bits, serially, from the Adapter to the BP; the other
transmits bits, serially, in the opposite direction.  Each set has
two lines; one to indicate the data bit is a logic "1", the other
to indicate it is a logic "0".  The pulses over each line of the set
exhibit identical characteristics; the line transmitting the pulses
thereby indicating the logic of the bit.  As can be seen from the
timing diagrams, the transmission of Data In (BP to adapter) bit
pulses are related to the TA clock pulses, with TA1 defining the
first bit of the character and TA7 the last (seventh) bit; whereas
the Data Out (adapter to BP) bit pulses are similarly related to the
TB clock pulses.

Test Out, Ready In or Not Ready In Control Lines- The pulse on the
Test Out line is presented by the adapter to the BP to determine
the condition of the BP (Ready or Not Ready).  This pulse enables
gates in the BO which immediately respond with a pulse to the adapter
on either the Ready In or the Not Ready In Line.  The Not Ready res-
ponse indicates that the BP is not in a condition to communicate with
the adapter.  If it occurs during a Poll sequence or at the start of
a Read or Write sequence, the adapter will terminate with Channel

End; followed by Device End and Unit Exception status bits. If it occurs at the end of a Read or Write sequence, the adapter will re-cycle until a Ready response is received.

During a poll sequence or at the start of a Read or Write sequence, Ready response indicates the BP is available for further communication thereby allowing the adapter to proceed with the control sequence. A Ready response at the end of a Read or Write sequence indicates that the BP has completed all interface functions on the last message and is prepared to present device status relevant to the last data transfer.

Demand Out, Demand In or Special In Control Lines- Upon receipt of a Ready response, the adapter will continue with the control sequence by presenting a pulse to the BP on the Demand Out Line. This pulse enables gates in the BO which respond with a pulse to the adapter (at appropriate clock pulse times) on either the Demand In or the Special In lines. During a Poll or at the start of a Read or Write sequence, a Demand In response indicates that the BP is available to perform any function directed by the processor and has no special information for the processor; at the end of a Read or Write sequence, it indicates the BP had no problems with the preceding data transfer as well as no other special information. A Special In response in-dicates that the BP has information (presented by the four Device Status In Lines) which may have a bearing on any command the pro-cessor may transfer next. The Special In response should only be received by the adapter when one of the Device Status In lines are enabled. Accordingly, if the adapter receives this response with no status lines or, Demand In with status lines, it will terminate with Channel End; followed by Device End and Unit Exception set in the status byte.

Device Status In (W, X, Y, Z) Control Lines- The meaning of these lines is primarily up to software in both the BP and the processor. Pulses on these lines are presented by the BP to the adapter in response to the Demand Out pulse and in conjunction with the Special In pulse, and will set respective bits in the adapter status and sense bytes for subsequent analysis by the processor software. Device Status In Line W indicates the BP has a message to send and, if occurring during a Poll or at the end of a Read or Write sequence, will cause the adapter to terminate with Channel End or Device End and Status Modifier set in the status byte, respectively.

Device Status in Line X, if occurring at the start of a Write sequence, will cause adapter termination with Channel End. Device End and Unit Check will then be set in the status byte and DSL X set in the sense byte. Any of the status lines which are active at the end of a Read or Write sequence will set their appropriate status or sense bits.

Device Control Out a,b,c,e,f,g Control Lines- These lines are set by the Read or Write commands and sent to the BP (at the proper s) to advise it of the function it is to perform. The meaning of these lines is dependent on program philosphy.

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The 9020D bit position - BP control line relationships are as follows:

```
9020D bit position        0 1 2 3 4 5 6 7
Device Control Outlines    a b c d e f g
```

Memory Request In and Transfer Demand Station In Control Lines.  After the BP has analyzed the Device Control Out lines and is oriented to perform the work directed by the processor, the BP advises the adapter to proceed by presenting pulses to the adapter on the Memory Request In line and Transfer Demand Station In line (if set to send data to the adapter) and on the Memory Request In line only (if set to receive data from the adapter).  These pulses continue every TA clock pulse until the adapter responds with RMA6.

If an invalid control line sequence is detected by the adapter (e.g., TRSI line active in response to a Write command, or inactive in response to a Read command), the operation will be terminated with Channel End.  Following a BP restore procedure, Unit Exception (Status Bit 7) and Device End (Status Bit 5) will be set.

RMA6 Initiate and Terminate Buffer Out Control Line- This line both initiates transfer of data and terminates the transfer.  The pulse is accordingly presented by the adapter to the BP twice during each message transfer; the first in response to Memory Request In from the BP, the second in response to a channel byte count reaching zero or an adapter detected error condition occurring during data transfer. Once the first RMA6 pulse is sent, the second must be sent to reset logic in the BP.

Demand Clear Out Control Line- A pulse on the Demand Clear Out Line is presented by the adapter to the BP as part of the adapter Poll, Read or Write terminjtion sequence to reset demand logic in the BP. Also, if any of the adapter sequen ces proceed through the generation of a pulse on the Demand Out line and, for some reason, the sequence is terminated (by some means other than a reset), the adapter will present a Demand Clear pulse prior to starting the next control sequence.

General and Selective Reset Line- The adapter may receive either a general or selective reset and will in turn active the General and Selective Reset Line.  A General Reset occurs in five forms:

1.  Power On Reset In PAM.

2.  General Reset Pushbutton on PAM Maintenance Test Panel.

3.  System Reset received for the CE. (e.g., IPL reset).

4.  General Reset received from the IOCE, (e.g., IOCE CCR reset).

5.  PAM CCR Reset.

Reference:   9020D and 9020E System Design Data, Peripheral Adapter
             Module, Chapter 6, PAM Reset, for discussion.

A Selective Reset occurs either through activation of the Selective
Reset Pushbutton on the PAM Maintenance Test Panel or upon receipt of
a Selective Reset from the IOCE.  Selective resets from the IOCE
occur upon detection of any of the following conditions;

    1.  Channel Control Check caused by any machine malfunction
        affecting channel controls, including parity errors on
        CCW and data addresses, and parity errors on the contents
        of the CCW.

    2.  Interface Control Check caused by an invalid signal on the
        I/O interface.  Usually indicates malfunctioning of the
        adapter which is detected by the channel.  Included in
        these malfunctions are an address or status byte received
        from a device has invalid parity, a device responded with
        an address other than the address specified by the channel
        during initiation of an operation, or a signal from the
        device occurred at an invalid time or had invalid duration.
        During command chaining, this condition would also arise
        if the adapter appeared not operational or indicated the
        busy condition without providing any other status bits.

Reference:   9020D and 9020E System Principles of Operation, Chapter
             10, Channel Control Check, and Interface Control Check.

Interface Electrical Characteristics

Driver.  The output of the driver card, with a 95 ± 5 ohm load will be
as shown in Figure 6-39 (measured at the driver card).
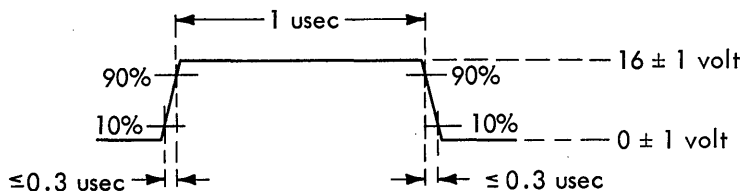


Figure 6-39.   BP Adapter Output Pulse

        The driver will deliver a positive output for a positive in-
put and will not be damaged by a short circuit on the output.
Maximum output current under a short, condition will be 85 milli-
amps.  Under no conditions will the output be up for more than 2.5
usec.

        This driver will drive only one receiver and is designed for
use over a maximum cable length of 150 feet (characteristic impedance
of 95 ± 5 ohms).

Under an ON condition (i.e., 16 ± 1 volt), the driver impedance will range from 19 to 180 ohms.

Under an OFF condition, the driver impedance will be 1.51K ± 5% if the driver signal is less than or equal to + 0.8 volts. Driver signals greater than + 0.8 volts but less than +15 volts will present an impedance range of 10 to 1.51K ± 5% ohms.

Receiver. The input of the receiver card will be as shown in Figure 6-40 (measured at the receiver card).
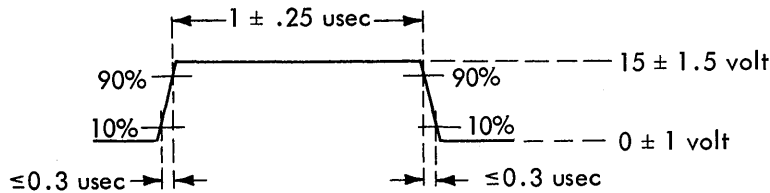


Figure 6-40. BP Adapter Input Pulse

The receiver card will deliver a positive output for a positive input and shall terminate the driving line with 95 ± 5 ohms. Neither the output nor the input shall be damaged if shorted to ground.

The receiver is designed for a logic one signal (at the receiver), of 13.5 volts (minimum) to 16.5 volts (maximum) and a logic zero signal at the receiver of -1.0 volts (minimum) to +1.0 volts (maximum).

The receiver is designed for use over a maximum cable length of 150 feet (characteristic impedance of 95 ± 5 ohms).

The receiver impedance will range from 86.6 to 96.7 ohms under both an ON and OFF condition.

The maximum input duty cycle is 10%, where duty cycle is defined as in Figure 6-41.

$$\text{Duty Cycle} = \frac{t_{up}}{T} \times 100$$



where, $t_{up}$ = time input is at up level (defined as 50% voltage level)
   $T$ = total time
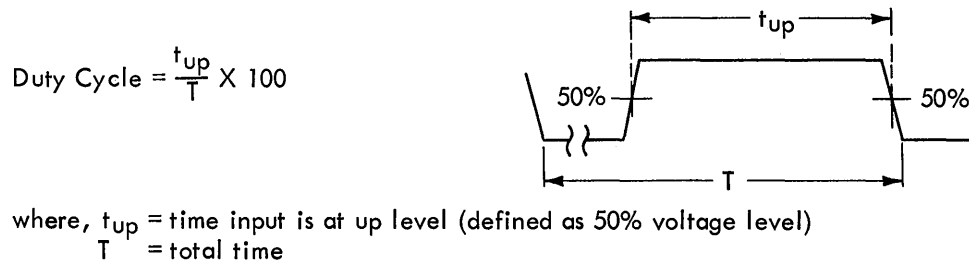
Figure 6-41. BP Adapter Duty Cycle

Interface Cable Pin Assignments

Buffer Processor Cable "A" with IBM "B" (dark gray) serpent connector
attached.  This cable will attach to an IBM "A" serpent connector
which is resident on the adapter.

| Signal Name | Signal Pin | Return Pin |
|---|---|---|
| Clock Lines TA | D03 | D04 |
| TA1 | B06 | B08 |
| TA7 | D07 | D09 |
| TB | B04 | B05 |
| TB7 | B09 | B10 |
| RMA6 | D10 | D11 |
| TRSI* | D12 | D13 |
| Memory Request* | B11 | B12 |
| Unused | B02 | B03 |
| Unused | D05 | D06 |
| Unused | G02 | G03 |
| Unused | G04 | G05 |
| SEL or GEN Reset | J05 | J06 |
| Command Lines a | J03 | J04 |
| b | G06 | G08 |
| c | J07 | J09 |
| d | G09 | G10 |
| e | J10 | J11 |
| f | G11 | G12 |
| g | J12 | J13 |

* Inputs to IBM adapter from Buffer Processor.

NOTE:  B07, B13, D02, D08⎫ These pins are tied to ground within the
       G07, G13, J02, J08⎭            adapter.

Buffer Processor Cable "B" with IBM "A" (light gray) serpent
connector attached.  This cable will attach to an IBM "B" serpent
connector which is resident on the adapter.

| Signal Name | Signal Pin | Return Pin |
|---|---|---|
| Status Lines W* | D03 | D04 |
| X* | B06 | B08 |
| Y* | D07 | D09 |
| Z* | B09 | B10 |
| Ready * | D12 | D13 |
| Not Ready * | B11 | B12 |
| Special In * | D10 | D11 |
| Unused | B02 | B03 |
| Unused | B04 | B05 |
| Unused | D05 | D06 |
| Unused | G02 | G03 |
| Unused | J05 | J06 |
| Data Zero Bit | G04 | G05 |
| Demand Clear | G06 | G08 |
| Demand Out | G09 | G10 |
| Data One Bit | J03 | J04 |
| Test Out | J07 | J09 |

| Signal Name | Signal Pin | Return Pin |
|-------------|------------|------------|
| Data Zero Bit * | J12 | J13 |
| Data One Bit * | G11 | G12 |
| Demand In * | J10 | J11 |

* Inputs to IBM adapter from Buffer Processor.

NOTE: B07, B13, D02, D08  These pins are tied to ground within the
G07, G13, J02, J08       adapter.

Event Sequence Diagrams

The following diagrams (figures 6-42 and 6-43) present a functional
vs time representation of the Buffer Processor adapter operation.
All actual interface lines (except General and Selective Reset) are
represented either explicity or implicitly; conversely however, all
functions shown on these diagrams do not necessarily represent
actual interface lines (see notes at bottom of Poll Command diagram).

Cross hatches, as shown on these diagrams, represent the
particular functions would occur and does not necessarily imply an
actual occurrence. Function lines (horizontal) such as No Device
Status represents the absence of a function and are included for
clarity only. Sequences shown as dotted lines represent optional
(exclusive OR) paths; the actual path being dependent on device
response.

An adapter General or Selective Reset will activate the
General and Selective Reset interface line (not shown) and may occur
at any time. This condition will cause an immediate adapter termin-
ation (no ending status presented).

The Poll command, as shown, represents a complete cycle of
device interrogation. Unless terminated by either an error, device
status, or channel, the Poll command will continue to cycle through
this basic sequence. Unlike the Poll command, a Read or Write
command proceeds through the outline sequence once per command
issuance.

Note A – Incorrect line sequence, set Channel End
Note B – X, Y, or Z device status received
Note C – W device status received, set Channel End
Note D – Incorrect line sequence, set Channel End
Note E – Halt I/O received during poll cycle , set Channel End
Note F – Set Channel End
 * Not an actual unterface line
** Represents multiple interface lines

= Indicates final status and sense bits set upon termination

Figure 6-42.   Poll Command Event Sequence Diagram

Figure 6-43. Read or Write Command Event Sequence Diagram (Sheet 1 of 2)

TA

TB

Data Lines**

Note T

RMA6

Note N

Note O

Demand Clear

Note M

Device End (Note R)

Timeout, Unit Check, Device End (Note R)

Timeout, Unit Check, Device End (Note R)

Test Out

Note P

Not Ready

Ready

Timeout*

Demand Out

Device Status**

No Device Status**

Note H

Demand In

Special In

Unit Exception, Device End (Note R)

Demand Clear

"Device Status", Device End (Note R)

|← Data Transfer Sequence →|← Communications Termination Sequence →|

Note G – Set Channel End
Note H – Incorrect line sequence
Note I – Write command-status line X active, set Channel End
Note J – Write command-status line X not active;
    Read command- any status active
Note K – Halt I/O received or invalid line sequence, i.e., TRSI received during
    Write command or TRSI not received during Read command
Note L – Invalid line sequence, see Note K; set Channel End

Note M – Halt I/O received
Note N – Stop received, set Channel End
Note O – Parity or overrun noted during Write command, transmit seven zeros, set Channel End
Note P – No Halt I/O
Note Q – Halt I/O (Channel End set upon receipt)
Note R – Plus data transfer error indications, if present
Note S – o (Send)  I (Receive)
Note T – Parity or overrun noted during Read command, set Channel End

Figure 6-43.  Read or Write Command Event Sequence Diagram (Sheet 2 of 2)

INTRODUCTION

The 2701 Data Adapter Unit (DAU) is a self contained self powered
unit which interfaces Radar Keyboard Multiplexors (RKM) to the IBM
DCP subsystem (RKMs are non-IBM equipment).  All necessary bit-
byte conversion, data control, and interfaces matching is accomplish-
ed by the three functional sections of the DAU:  the Two Processor
Switch (TPS); the Transmission Interface Converter (XIC; and the
Modified Parallel Data Adapter (MPDA).  The TPS, XIC, and MPDA
operate together to provide a single complete path for the IOCE/RKM
operation.  (Figure 7-1)

FUNCTIONAL DESCRIPTION

Each 2701 can interface with up to five RKM's.  This interface,
consists of a Data Bus Out (DBO) to the RKM, a Data Bus In (DBI) to
the 2701, an Address Bus Out (ABO) to the RKM, and the control lines
necessary for proper interface sequencing.  The interface operates
in a demand/response mode and contains both multiplex and simplex
lines.  Although the 2701 can have five devices attached to it,
it cannot operate these devices in a multiplexed environment.  It
must complete an operation with one RKM before initiating an oper-
ation with another.

     The data paths provided to and from the 2701/RKM (DBO, DBI) are
one byte each (8 data bits, 1 parity bit).  The ability to buffer
two bytes of data is provided in the MPDA to make the RKM dis-
connect sequence compatible with the IOCE disconnect sequence.

     The RKM does not share the same repertoire of commands as the
DAU.  Since the commands are different in both format and function,
it is necessary for the DAU to generate acceptable RKM commands.
The DAU reformats the 8-bit IOCE/DAU command to form the RKM command.

     Each DAU has a Two Processor Switch (TPS) which is used to
connect it to two IOCEs.  The TPS is under configuration control and
receives its enable/disable signals from the Configuration Console
(CC).

     The DAU functions as a control unit for the RKMs.  To the
system the DAU functions and responds the same as any 9020 control
unit, (see "9020D and 9020E System Principles of Operation" for
additional I/O architecture).  Commands and addresses are passed
from IOCE through the TPS, XIC, MPDA, and out to the RKM.  The DAU
once selected, controls the data flow between IOCE and RKM as two
independent functions.  The DAU accumulates check and sense inform-
ation transfers it to the system upon request or during status
time.
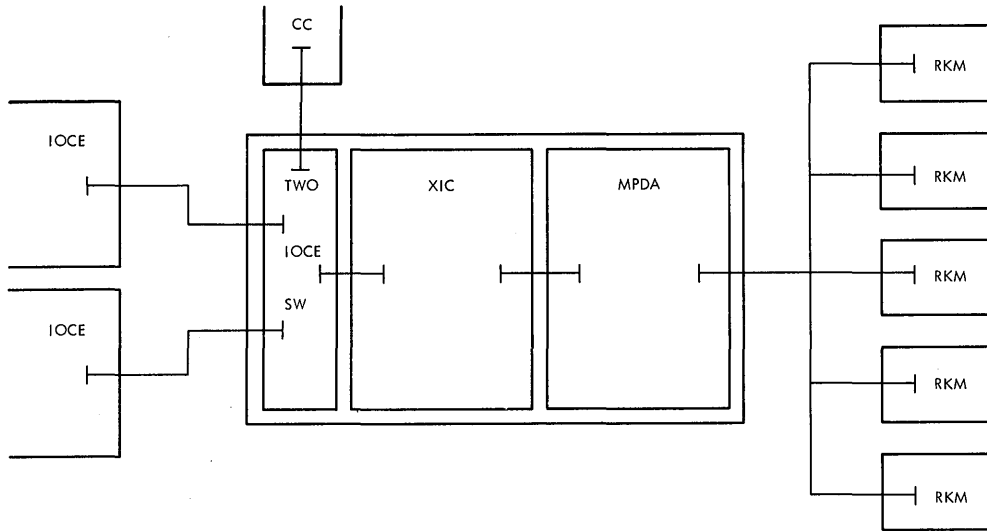
Figure 7-1. 2701 Block Diagram

DESIGN DETAILS

Two Processor Switch (TPS)

Each DAU is provided with a TPS which allows it to be connected to two IOCEs. A complete description of the interface lines, functions, and sequences is described in Appendix D. The design of the DAU is such that even though two IOCEs are attached, only one can be logically connected and operating

The enabling and disabling of these interfaces is under configuration control via the configuration console over a separate DAU/CC interface. This is to allow only those IOCE's in the same subsystem as the DAU to communicate with it. Once enabled to an interface, by the CC, the DAU is dedicated to that IOCE until such a time as it receives a CC signal to change its configuration. The DAU will ignore activity on any interface it is not enabled to by the CC. There are manual switches located on the DAU to override the configuration set by the CC. These switches are three position toggle switches (enable, neutral, disable) which are only activated when the DAU is in State $\emptyset$. When the DAU is in State $\emptyset$ and either switch is in a position other than neutral, the Ready Line to the CC will be deactivated until both switches are returned to their neutral positions. The Ready Line being inactive indicates to the CC that the DAU is not program configurable. The DAU will not allow the CC to enable both interfaces at the same time, if this occurs the DAU will not accept the reconfiguration command. Both interfaces disabled is a valid configuration.

Transmission Interface Converter (XIC)

The XIC is that functional portion of the DAU which controls
operation of the IOCE/DAU interface. The primary functions of the
XIC are:

1. Accumulates and stores status bytes.

2. Accumulates and stores sense bytes.

3. Receives and passes command codes to the MPDA.

4. Recognizes five RKM addresses.

5. Generates and checks IOCE/DAU data.

6. Responds to specific control unit commands.

7. Provides an interface to the MPDA.

A Start I/O instruction executed in the IOCE causes the channel
to access a CCW from which a command is extracted. During the
initial selection sequence the command is placed in a one byte
command register within the XIC (Figure 7-2). At RKM selection time
this command is transferred to and reformatted by the MPDA for
transmission to the RKM.

When the MPDA accepts data from an RKM, it signals the XIC to
take the data and pass it to the IOCE. Similarly when an RKM re-
quests data from the MPDA it signals the XIC to fetch data from the
IOCE. As status conditions occur (ending sequence, attention, check,
etc) they are sent from the MPDA to the XIC where they are put in
the proper position of the Status Register for transfer to the IOCE
during status time. (See Appendix D, "Input/Output Interface,
Channel to Device Control Unit", for a description of the IOCE/2701
interface operation.) The XIC will place in a Sense Register any
sense information sent from the MPDA which can be retrieved by the
program by execution of a sense command.

The XIC is designed to recognize and store five different RKM
addresses. Only the Low order 3-bits are used to decode an RKM.
All other bits are used to identify the DAU. The DAU address is
pluggable and will be set at system installation time. The address
structure is shown in Table 7-1.

The DAU is designed and addressed as a single adapter which
can communicate with five attached devices. Therefore, any of the
five RKM addresses can be used for DAU commands such as, Sense,
Test I/O, or No-Op. For example, if RKM-1 caused unit check to be
set, a sense to any RKM will retrieve, the Sense data for RKM-1.

During initial selection, the IOCE sends a DAU/RKM address to
the DAU, the most significant five bits of the 8-bit code will be
compared with the preassigned DAU address to confirm that the
IOCE is attempting to connect to it. If the address does not com-
pare the DAU ignores all interface activity until the next time the
IOCE presents an address. If the address compares, the DAU will
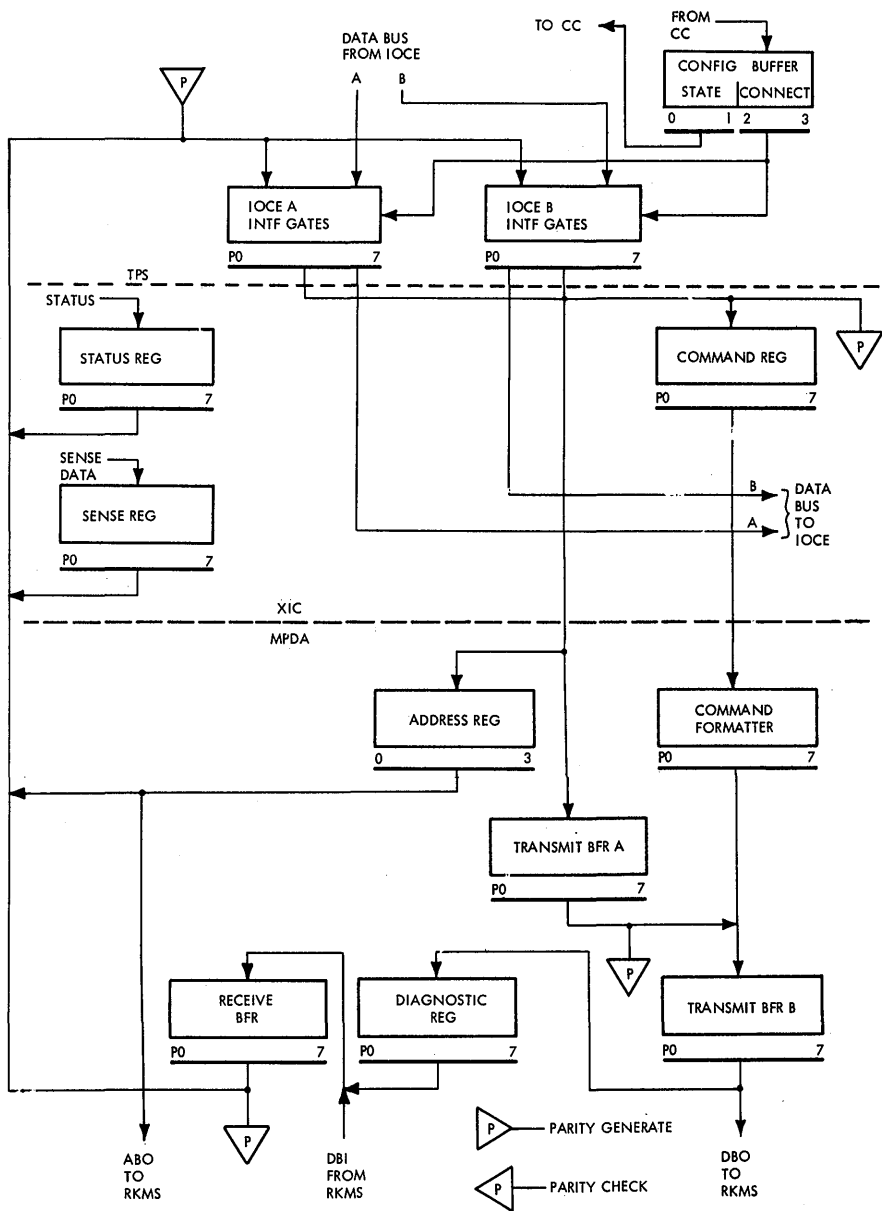
Figure 7-2. DAU Data Flow

load the low order 3 bits of the address into the RKM Address Register (if these bits are within the range of a binary-encoded number of 1-5) and complete the initialization sequence with the IOCE. If the DAU is addressed and the low order three address bits specify an address other than binary 1-5, no selection occurs.

7-4

Table 7-1.  IOCE/DAU/RKM Addressing

| IOCE/DAU Bus | | | | | | | | DAU/RKM Bus | | | | RKM |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | ID |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | x | x | x | x | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| x | x | x | x | x | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 2 |
| x | x | x | x | x | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 3 |
| x | x | x | x | x | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| x | x | x | x | x | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 5 |

NOTE:   XXXXX - is reserved for DAU addressing.

The DAU will not complete the RKM selection sequence prior to releasing the IOCE.  When the IOCE sends an address and command to a DAU, it will pass them to the MPDA and complete the selection sequence.  If the DAU is unsuccessful in its attempt to select an RKM, it will notify the IOCE by interrupting it.  If the selection attempt is successful, no notification is necessary.  This scheme allows the earliest possible disconnect with the IOCE and avoids holding up IOCE operations excessively since the RKM will frequently be selected during normal operations.

Each time the DAU selects the IOCE for data the contents of the RKM address register are transferred, along with the DAU address, to the IOCE.  This identifies the RKM that is requesting data.

Commands

Figure 7-3 shows the commands for the DAU/RKM subsystem.  The sixteen DAU/RKM commands are those commands which are sent to the RKM in RKM format by the DAU.  The twenty-one IOCE/DAU commands are those command formats received by the DAU from the IOCE channel.  Sixteen of these commands are reformatted and passed on to the RKM as shown in Figure 7-3.  The remaining five commands are for DAU use only and have no effect on the RKM.

Disconnect- This is a control type command.  The command as received by the DAU is reformatted as shown in Figure 7-3 and passed to the RKM.  The I/O operation is completed and status returned at the end of the initial selection sequence (see "Interface Sequences" section of this chapter).

Write RKM - This is a write type command.  The command as received by the DAU is reformatted as shown in Figure 7-3 and passed to the RKM.  At the end of initial selection, the data path to the RKM is established and data transfer takes place in the Write data to

RKM mode (see "Interface Sequences section of this chapter). All
Write type commands, except for the unique reformatting for each
command, operate, with respect to the DAU, the same as the Write
RKM command.

DAU/RKM BUS | | | | | | | | RKM DATA BUS / SYSTEM 360 BUS | IOCE/DAU BUS | | | | | | | | HEX

| $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | RKM DATA BUS — SYSTEM 360 BUS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | HEX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | DISCONNECT | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 |
| 1 | 0 | 0 | 1 | 1 | b | 0 | 0 | WRITE RKM | 1 | 1 | b | 0 | 0 | 0 | 0 | 1 | V1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | CLEAR RKM MEMORY | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 |
| 1 | 0 | 0 | 1 | 0 | B | 1 | 0 | BLINK DISPLAY SET/RESET | 1 | 0 | B | 1 | 0 | 0 | 0 | 1 | W1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | FETCH DISPLAY CONSTANT | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOAD QUEUE ADDRESS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | MOVE DATA | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | SPECIAL MOVE | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 |
| 1 | 1 | 0 | 1 | 1 | b | 0 | 0 | READ RKM | 1 | 1 | b | 0 | 0 | 0 | 1 | 0 | X2 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | READ QUEUE ADDRESS | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | LOAD I/O ADDRESS | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | KEYBOARD WRITE | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 |
| 1 | 0 | 1 | B | 1 | $L_0$ | $L_1$ | $L_2$ | BIT MODIFY | B | 1 | $L_0$ | $L_1$ | $L_2$ | 1 | 0 | 1 | YZ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | READ RKM STATUS | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | READ RKM ERROR STATUS 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | READ RKM ERROR STATUS 2 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16 |

V = C or E
W = 9 or B
X = C or E
Y = 4, 5, 6, 7
       C, D, E or F
Z = 5 or D
U = 0 or 2

B  Bit to be stored (1 or 0)
L  Binary Encoded position of bit B
b  When b=1 Codes -- 11 1111
   and -- 11 1110 are interchanged
   at RKM interface during
   function execution
y  1 = Set   0 = Reset
M  Modifier Bit (1 or 0)

COMMANDS FOR DAU ONLY

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | HEX |
|---|---|---|---|---|---|---|---|---|---|
| DIAGNOSTIC WRITE | 0 | 0 | M | 0 | 1 | 0 | 0 | 1 | U9 |
| DIAGNOSTIC READ | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| TEST I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| SENSE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| NO-OP | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| RESERVE | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4 |
| RELEASE | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D4 |

Figure 7-3.   RKM-DAU Command Formats

Clear RKM Memory- This is a Write type command (see Write RKM
command).

Blink Display Set/Reset- This is a Write type command (see Write
RKM command).

Fetch Display Constants- This is a Write type command (see Write
RKM command).

Load Queue Address- This is a Write type command (see Write RKM
command).

Move Data- This is a Write type command (see Write RKM command).

Special Move- This is a Write type command (see Write RKM command).

Load I/O Address- This is a Write type command (see Write RKM
command).

Keyboard Write- This is a Write type command (see Write RKM command).

Bit Modify- This is a Write type command (see Write RKM command).

Read RKM- This is a Read type command. The command, as received by the DAU is reformatted as shown in Figure 7-3 and passed on to the RKM. At the end of initial selection the data path from the RKM is established and data transfer takes place in the Read data from RKM mode (see "Interface Sequences" section of this chapter).

Read Queue Address- This is a Read type command (see Read RKM command).

Read RKM Status- This is a Read type command. The command is reformatted as shown in Figure 7-3 and sent to the RKM. The operation then proceeds as for a Read RKM command, except that the RKM will return a fixed length data message of one byte.

Read RKM Error Status 1 and 2 - These are Read type commands. The command is, with respect to the DAU, identical as the Read RKM command, except for the reformatting, see Figure 7-3, and the message length. The RKM for these commands will return a fixed length data message of one byte.

Diagnostic Write - This command is used to exercise internal control and data paths in the DAU. Data is transferred from the IOCE through the DAU into the Diagnostic Register. Any number of bytes may be transferred to the DAU; however, only the last byte will be retained in the Diagnostic Register.

Diagnostic Write Modified - This command is handled the same as the Diagnostic Write command in that it transfers an unrestricted number of bytes from the IOCE to the DAU. In addition the command sets all five of the RKM attention interrupt latches. Upon completion of the command, five attention interrupts will be presented to the system. This function allows the interrupt handling and associated address generation circuitry to be tested.

Diagnostic Read - This command transfers the data previously set into the Diagnostic Register by the Diagnostic Write through the DAU to the IOCE. The Diagnostic Register is not reset by the Diagnostic Read Command, allowing any number of bytes to be transferred.

Test I/O- This is an I/O Instruction which is passed by the channel to the DAU as an I/O command (see 9020D and 9020E System Principles of Operation). It is for the DAU only. The DAU will return status, of the DAU, in response to Test I/O. If the DAU has no status it will return a status byte of all zeroes.

Sense- This command is for the DAU only. The DAU will return one Sense byte to the channel in response to the Sense command. For the meanings of the Sense bits, see Sense Byte section of this chapter.

No-Op - This command is for the DAU only.  It is a control type command.  The DAU in response to this command will perform the initial selsction sequence (see Appendix D), and return Device End and Channel End status.  No further operation takes place.

Reserve - When the DAU accepts a Reserve command from either of its two IOCE channel interfaces, the two channel switch will be dedicated to that interface until a Release command is received (over that interface) or the interface is switched via configuration control. Once reserved, or dedicated to an interface, the DAU will be unavailable to the other interface.

Release - After a Release command, the DAU is free to accept selections from either interface.  This is contingent upon the setting of the Configuration Register, (must be in states 1, 2, or 3), or the setting of the Enable switches when in State 0.

Status Byte

The status bits inform the IOCE that an operation has ended or that an abnormal condition has occurred.  These bits are placed in the Status Register, in the XIC, as they occur.  The contents of the Status Register are sent to the IOCE during the initial selection sequence and the ending sequence.  The five bits used in the Status Byte are:  Attention, Busy, Channel End, and Device End, and Unit Check.

| Bit | Name |
|-----|------|
| 0 | Attention |
| 1 | Status Modifier |
| 2 | Control Unit End |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | ------ |

The following combinations of the status bits are reported by the DAU:

Unit Check - Indicates that during initial selection a Bus Out Check or Command Reject condition has occurred.

Device End, Channel End - Indicates the operation has been brought to a normal ending.

Device End, Channel End, Control Unit End - Indicates that Control
Unit Busy has been transmitted to the channel due to a selection
attempt for one device while another device is busy, and the busy
device is terminating the operation normally.

Device End, Channel End, Attention - Indicates the operation has been
brought to a normal ending and an attention interrupt has been
received from the RKM. The attention bit can be set, in this
instance, only by the RKM that has caused the Channel End, Device End.

Device End, Channel End, Unit Check - Indicates that an unusual end-
ing condition has occurred and the sense byte should be inspected
for more detailed information.

Device End, Channel End, Control Unit End, Attention - This bit Con-
figuration is generated when Control Unit Busy has been indicated to
the channel due to a selection attempt for one device while another
device is busy, and the busy device is terminating the operation
normally. Attention being set indicates an Interrupt signal has been
received from the busy RKM.

Device End, Channel End, Control Unit End, Unit Check - This bit Con-
figuration is generated when Control Unit Busy has been indicated to
the channel due to a selection attempt for one device while another
device is busy, and the busy device is terminating the operation with
an error condition.

Device End, Channel End, Unit Check, Attention - Indicates an unusual
ending condition has occurred and an Attention has been received from
the RKM. The sense byte should be inspected for detailed error in-
formation.

Device End, Channel End, Control Unit End, Unit Check, Attention -
This bit configuration is generated when Control Unit Busy has been
indicated to the channel due to a selection attempt for one device
while another device is busy and the busy device is terminating the
operation ABNORMALLY. Attention has also been received from the RKM.
The sense byte should be inspected for detailed error information.

Attention - Indicates an Interrupt signal has been received from one
of the RKM's.

Attention, Control Unit End - Indicates while the DAU was busy attempt-
ing to present a stand-alone Attention, it presented Control Unit Busy
to the channel in response to a selection attempt.

Busy - Indicates that the DAU was working with one of the RKM when an
attempt was made to select it.

Status Modifier, Busy - These two status bits, indicating Control
Unit Busy are presented to the channel when the DAU is busy with one
device and the channel attmepts an initial selection for another
device. Control Unit End is also stored in the DAU for later pre-
sentation.

Sense Byte

The Sense Byte is stored in the Sense Register which is located in
the XIC.  The Sense Byte is set as abnormal, or unusual, conditions
occur in the DAU.  The sense byte is sent to the IOCE upon receipt
of a Sense command and is used to further define the information in
the Status Byte.  Seven bit positions are used in the Sense Register.

They are:

| Bit | Name |
|-----|------|
| 0 | Command Reject |
| 1 | Intervention Required |
| 2 | Bus Out Check |
| 3 | ------- |
| 4 | Data Check |
| 5 | RKM Error |
| 6 | ------- |
| 7 | Timeout |

Command Reject - Is set any time the XIC decodes an invalid command
being sent from the IOCE.

Intervention Required - Is set when the time between subsequent data
transfers signaled by the Request In Line is 50 usec or more.  Inter-
vention Required is also set if the RKM fails to raise Request In
within 50 usec after the completion of the RKM selection sequence.
It indicates an abnormal DAU/RKM interface operation.

Bus Out Check - Is set when a parity check occurs on the IOCE Bus
Out.

Data Check - Is set when a parity check occurs on the RKM Bus In
during a Read Operation.  When writing, Data Check is set when a
parity check occurs at the output of Transmit Buffer A.

RKM Error - Is set when the RKM raises its Error In signal to the
DAU during a data transfer operation.

Timeout - Is set when Response In is not raised within 1.9 usec after
the MPDA raises either Order Out or Acknowledge Out.  It indicates
an abnormal DAU/RKM interface operation.  If a command is sent to
the DAU for an RKM which is not attached to the DAU, Unit Check
status will be sent to the IOCE and the Timeout bit will be set.  If
the DAU is in State Zero and a command to any RKM is issued a Unit
Check will occur and the Timeout sense bit will be set.

## Modified Parallel Data Adapter (MPDA)

The MPDA is that functional section of the DAU that controls all communications between the DAU and the RKM. The MPDA allows for the connection and operation of a maximum of five RKM's. Through the MPDA the RKM's can transfer data parallel by bit serial by byte in a non-multiplexed environment with the IOCE via the XIC. The MPDA presents a demand/response interface to the RKM's that control the transfer of data between RKM and XIC. The MPDA develops and checks parity on the DAU/RKM interface and provides the address and data buffering necessary for both read and write operations. RKM command reformatting is also performed by the MPDA.

A description of the registers located in the MPDA appears in Figure 7-2.

Transmit Buffer A - Receives the data from the XIC to be passed to the RKM, via Transmit Buffer B.

Transmit Buffer B - Receives data from Transmit Buffer A and reformated commands from the Command Register. Transmit Buffer B outputs data to the RKM data bus out and to the Diagnostic Buffer, depending on the command being executed.

Read Buffer - Receives data from RKM data bus in or the Diagnostic Buffer, depending on the command being executed. Data is outputed to the XIC for transfer to the IOCE.

Diagnostic Register - Receives data from Transmit Buffer B and outputs data to Read Buffer. This is used in conjunction with the diagnostic Read and Write commands as maintenance aids.

The Diagnostic Register also receives the output of the command formatter whenever an RKM is selected. This facility provides a means of checking the output of the formatter.

## Interrupts

There are two Interrupt signals that can be sent by the RKM to the DAU; Interrupt A, and Interrupt B. These can be sent asynchronous to each other and to any RKM or DAU operation. The interrupts signify the completion of RKM operations that were requested by the program. When either of the two interrupt lines ary pulsed, an interrupt latch is set in the MPDA (one latch per RKM). The interrupts are presented to the IOCE in the form of Attention Interrupts when the DAU does not have an operation in progress or in the course of a normal channel ending. Only one stand-alone Attention Interrupt can be presented to the channel between consecutive program initiated operations.

NOTES:      1. The program should respond to an Attention Interrupt with a Read RKM Status command. This is the only way to identify which interrupt occurred. It also resets the interrupt bit in the RKM.

2. A single Attention Interrupt can be presented any time
   the DAU is idle with one exception. When an abnormal
   ending occurs and Unit Check is set in the ending
   status, no Attention Interrupts will be issued until
   another command has been given to the DAU. This is
   done to allow a sense command to be issued immediately
   following the check condition without interference.

Speed of Operation

Determining the maximum overall data rate possible between the RKM
and IOCE is a complex function. It is dependent on such parameters
as: is the DAU on a Selector or Multiplexor channel, how many other
devices are working with the IOCE at a time, their data rates, and
the transfer rate of the RKM. The MPDA is capable of transferring
data to and from the IOCE at the maximum channel rate (Selector or
Multiplexor) whenever conditions exist that allow that rate. The
maximum transfer rate of the DAU to RKM interface is fixed at 66.6 Kb.

Checks

The DAU checks parity on data transferred from both the IOCE and the
RKM.

A. IOCE DBO parity is checked on every data, address and
   command byte sent to the XIC.

B. RKM DBI parity is checked as each byte enters the Read
   Buffer.

C. Timeouts on the RKM/DAU interface are used to prevent a hang-
   up condition from tying up the DAU.

   If a check condition is detected, Unit check is set in the
status register and the proper bit or bits are set in the sense
register. The XIC parity circuitry also generates odd parity for
the data that is sent to the IOCE.

   All hardware checks are reported two ways. When the check
occurs, it is recorded in the sense and status bytes to be inspected
by the program. Checks are also signaled to the CC via a Logic
Check Line which is an OR of any logic check condition. This results
in lighting of a check indicator on the CC.

Configuration

The TPS is under configuration control from the CC.  A separate
interface exists between CC and DAU to control the TPS.  The
channel interface logic contains a four position register which is
loaded via the CC interface and controls the enabling of the TPS/IOCE
interfaces.  The four positions are; Interface A, Interface B, SØ,
and S1.  The Interface positions determine the TPS configuration
and the SØ and S1 bits set the state of the 2701.

   The SØ and S1 bits are decoded and provide two functions:

   1.  One of four possible states can be decoded Ø-3 from these
       bits.  The 2701 will drive the appropriate line over the
       2701/CC interface to indicate at the CC which of the four
       states it is in.

   2.  The internal 2701 hardware will recognize only State Ø
       and not State Ø.  When in State Ø an indicator will be
       "turned on" on the operators panel, all switches will be
       enabled, and all activity on the 2701/RKM interface will
       be ignored.

     When the system wants to change the DAU configuration the CC
sends a Configuration Strobe Line to the channel interface with the
desired configuration.  If the configuration is valid and both manual
switches are in the neutral position, an Accept will be returned
to the CC.  If the configuration is not valid (DAU cannot be enabled
to both IOCE's) no Accept is sent to the CC and the current configura-
tion is retained.  Once accepted, the new configuration will be set
as soon as the DAU becomes idle.  This is to prevent reconfiguration
in the middle of an operation.

DAU/DCP Interfaces

IOCE/DAU.  There are two IOCE/DAU interfaces per DAU.  These are
standard System/360 channel I/O interfaces and are described in
Appendix D.

DAU/CC.  The description of this interface is in Chapter 13.

DAU/RKM Interface Lines

The DAU/RKM interface consists of the following lines:

| 2701 to RKM | Quantity | Type |
|---|---|---|
| Address Bus Out | 4 lines | Multiplex |
| Data Bus Out | 9 lines | Multiplex |
| Order Out | 1 line | Multiplex |
| Acknowledge Out | 1 line | Multiplex |
| Data Strobe Out | 1 line | Multiplex |
| Disconnect Out | 1 line | Multiplex |

| RKM to 2701 | Quantity | Type |
|---|---|---|
| Data Bus In | 9 lines | Multiplex |
| Request In | 1 line | Simplex |
| Response In | 1 line | Multiplex |
| Interrupt In A | 1 line | Simplex |
| Terminate In | 1 line | Multiplex |
| Error In | 1 line | Multiplex |
| Interrupt In B | 1 line | Simplex |

## Multiplex Lines

Address Bus Out - The Address Bus Out (ABO) consists of four lines. The Address on the ABO is binary encoded and is taken from the three least significant bits of the eight bit address sent from IOCE to 2701. ABO timing is dependent on the sequence being executed.

1.  Initial Selection. The 2701 will put the address of the desired RKM on the ABO 100ns prior to raising Order Out (Figure 7-4). This address will remain stable for 700ns after the fall of Order Out.

2.  Read Sequence. When the 2701 is ready to read a byte of data it will raise ABO 100ns prior to raising Acknowledge Out. The ABO will drop 100ns after tha fall of Acknowledge Out (Figure 7-5). On the last byte to be transferred, (Figure 7-6) when Terminate In is sensed, the address will remain on the ABO for 100ns after the fall of Disconnect Out.

3.  Write Sequence. When the 2701 is ready to write a byte, it will put the RKM address on the ABO 100ns before it raises Acknowledge Out (Figure 7-7). The address will drop 700ns after the fall of Data Strobe Out. When the 2701 sends the last byte of data to the RKM, the ABO will drop 100ns following the fall of Disconnect Out (Figure 7-8).

INITIAL SELECTION

AT THE START OF THE INITIAL SELECTION SEQUENCE, THE 2701 WILL RECEIVE FROM THE IOCE A DEVICE (RKM) ADDRESS WHICH IT WILL PUT INTO A UNIT
ADDRESS REGISTER. NEXT, THE 2701 WILL RECEIVE A COMMAND WHICH IT WILL TRANSLATE INTO RKM FORMAT AND HOLD IN THE COMMAND REGISTER. THE
2701 NOW GATES THE RKM ADDRESS TO THE ABO, GATES THE COMMAND TO THE DBO, WAITS 100 NS BEFORE RAISING ORDER OUT, AND WAITS FOR THE RKM
TO REPLY WITH RESPONSE IN. WHEN THE RKM REPLIES, THE 2701 SAMPLES THE STATUS ON THE DBI (IF A STATUS COMMAND IS BEING EXECUTED), DROPS
ORDER OUT, HOLDS THE ADDRESS ON ABO AND THE COMMAND ON THE DBO FOR 700NS, AND THEN SETS INTERNAL CONTROLS FOR THE
FOLLOWING READ OR WRITE OPERATION.
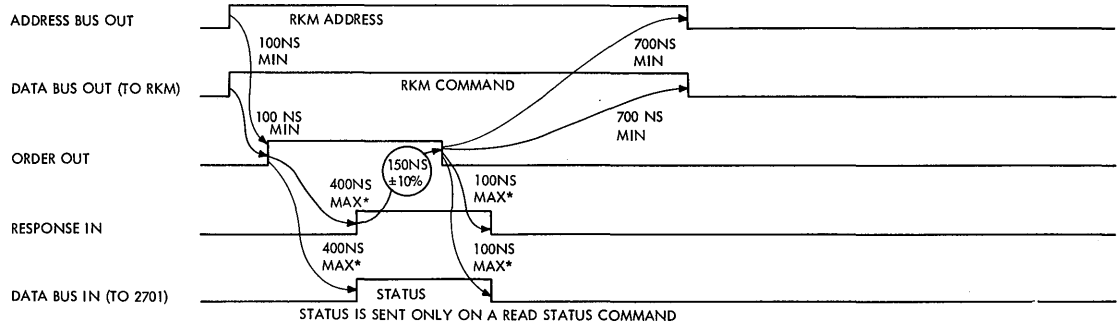


NOTES: TIMING SHOWN AT 2701 CONNECTOR. TOLERANCES SHOWN AS MAXIMUM ASSUME A
MINIMUM OF ZERO. TOLERANCES SHOWN AS MINIMUM ASSUME A MAXIMUM OF THE
STATED VALUE PLUS 25%.

* RKM LOGIC DELAY. ASSUMING AN AVERAGE PROPAGATION DELAY OF 1.5NS PER FOOT,
ADD 3.0NS TO THIS VALUE FOR EACH FOOT OF EXTERNAL CABLE USED BETWEEN THE 2701
AND THE RKM.

●Figure 7-4. 2701 to RKM Selection Sequence

READ SEQUENCE

THE RKM STARTS THIS SEQUENCE BY RAISING REQUEST IN WHEN IT IS READY TO TRANSFER A BYTE OF DATA. WHEN THE 2701 IS READY TO
RECEIVE THAT BYTE, IT PUTS THE RKM ADDRESS ON THE ABO, WAITS 100NS, THEN RAISES ACKNOWLEDGE OUT. UPON RECEIPT OF
ACKNOWLEDGE OUT, THE RKM HAS 400NS TO PUT THE BYTE ON THE DBI AND TO RAISE RESPONSE IN. WHEN THE 2701 HAS SAMPLED THE
DBI, IT DROPS ACKNOWLEDGE OUT AND WAITS 100NS BEFORE DROPPING THE ABO. THE RKM MUST DROP THE DBI, REQUEST IN, AND
RESPONSE IN WITHIN 100NS AFTER THE RECEIPT OF THE FALL OF ACKNOWLEDGE OUT. THE SEQUENCE IS REPEATED FOR EACH BYTE THAT
IS TRANSFERRED.
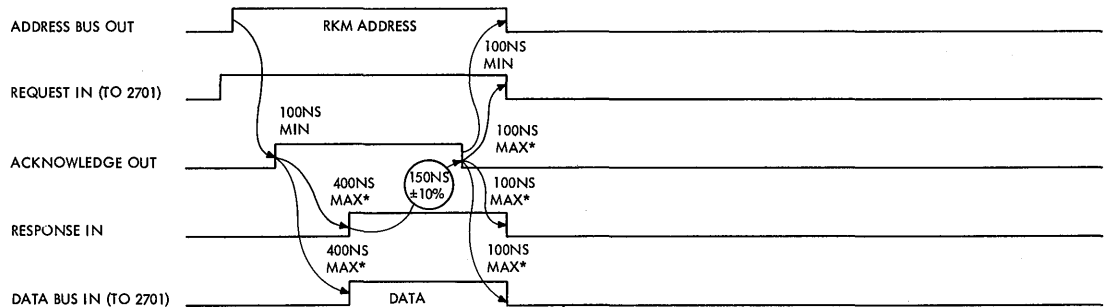


NOTES: TIMING SHOWN AT 2701 CONNECTOR. TOLERANCES SHOWN AS MAXIMUM ASSUME A
MINIMUM OF ZERO. TOLERANCES SHOWN AS MINIMUM ASSUME A MAXIMUM OF THE
STATED VALUE PLUS 25%.

* RKM LOGIC DELAY. ASSUMING AN AVERAGE PROPAGATION DELAY OF 1.5NS PER FOOT,
ADD 3.0NS TO THIS VALUE FOR EACH FOOT OF EXTERNAL CABLE USED BETWEEN THE 2701
AND THE RKM.

●Figure 7-5. RKM to 2701 Data Transfer

DISCONNECT SEQUENCE

IF A READ OPERATION IS IN PROGRESS, AND THE RKM WISHES TO HALT THE OPERATION, IT WILL RAISE TERMINATE IN AT THE SAME TIME IT RAISES RESPONSE
IN FOR THE LAST BYTE TO BE TRANSFERRED. THE 2701, WHEN IT DROPS ACKNOWLEDGE OUT, WILL HOLD THE ABO STABLE AND WAIT A MINIMUM OF
1.0 μSEC BEFORE RAISING DISCONNECT OUT FOR 500 NS. THE ABO WILL REMAIN STABLE FOR 100 NS AFTER DISSCONNECT OUT DROPS. THE INTERFACE
NOW RESUMES AN IDLE CONDITION. IF A WRITE OPERATION IS IN PROGRESS (FIGURE 7-8), THE 2701 WILL HALT THE OPERATION BY RAISING DISCONNECT
OUT FOR 500 NS NO SOONER THAN 500 NS FOLLOWING THE FALL OF DATA STROBE OUT. THE ABO WILL REMAIN STABLE FOR 100 NS FOLLOWING THE FALL
OF DISCONNECT OUT. WHEN THE RKM DETECTS THE DISCONNECT SIGNAL, IT WILL NOT REQUEST ANY ADDITIONAL DATA, AND THE INTERFACE WILL
BECOME IDLE.
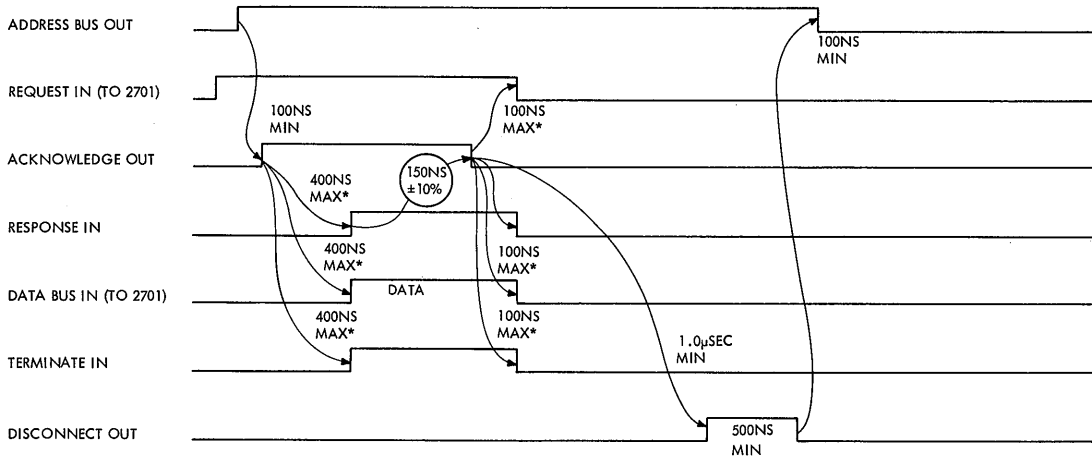


NOTES: TIMING SHOWN AT 2701 CONNECTOR. TOLERANCES SHOWN AS MAXIMUM ASSUME A
MINIMUM OF ZERO. TOLERANCES SHOWN AS MINIMUM ASSUME A MAXIMUM OF THE
STATED VALUE PLUS 25%.

* RKM LOGIC DELAY. ASSUMING AN AVERAGE PROPAGATION DELAY OF 1.5NS PER FOOT,
ADD 3.0NS TO THIS VALUE FOR EACH FOOT OF EXTERNAL CABLE USED BETWEEN THE 2701
AND THE RKM.

●Figure 7-6.   RKM to 2701 Transfer Last Data Byte and Ending Sequence


Data Bus Out - The Data Bus Out (DBO) is the data path from the
2701 to the RKM's.  The bus consists of eight data lines and one
parity line.  Odd parity is always maintained on the DBO.  During
initial selection time, the 2701 will place a command for the RKM
on the DBO 100ns prior to raising Order Out (Figure 7-4) and holds
it there for 700ns following the fall of Order Out.  During a write
operation the data will be on the DBO 100ns prior to raising Data
Strobe and will remain on the DBO for 700ns after the Data Strobe
Line falls (Figure 7-7).

Data Bus In - The Data Bus In (DBI) is the data path from the RKM
to the 2701.  The bus consists of eight data lines and one parity
line.  The DBI is checked for odd parity by the 2701.  During the
initial selection sequence (Figure 7-4), the RKM will put a byte of
status on the DBI (RKM status commands only).  This status must be
stable at the RKM connector within 400ns after the RKM receives the
rise of Order Out and must fall within 100ns from the fall of Order

WRITE SEQUENCE

WHEN THE RKM IS READY TO RECEIVE A BYTE OF DATA, IT WILL RAISE REQUEST IN. WHEN THE 2701 IS READY TO SERVICE THE REQUEST, IT PUTS THE RKM ADDRESS ON THE ABO AND RAISES ACKNOWLEDGE OUT 100NS LATER. THE RKM HAS 400NS TO RAISE RESPONSE IN AFTER RECEIPT OF ACKNOWLEDGE OUT. THE 2701 WILL DROP ACKNOWLEDGE OUT IN RESPONSE TO THE RISE OF RESPONSE IN. THE RKM HAS 100NS TO DROP REQUEST IN AND RESPONSE IN AFTER THE RECEIPT OF THE FALL OF ACKNOWLEDGE OUT. THE RKM IS NOW READY TO INGATE THE DATA. THE 2701 PUTS THE DATA ON THE DBO AND RAISES DATA STROBE OUT 100NS LATER. DATA STROBE REMAINS ACTIVE FOR 600NS. THE ABO AND THE DBO WILL REMAIN STABLE FOR 700NS AFTER THE FALL OF DATA STROBE OUT. IF THE RKM DETECTED A PARITY ERROR ON THE DBO, IT MUST RAISE ERROR IN WITHIN 400NS AFTER RECEIPT OF THE RISE OF DATA STROBE OUT AND DROP THE ERROR SIGNAL WITHIN 100NS AFTER THE FALL OF THE STROBE. THIS SEQUENCE IS REPEATED FOR EVERY BYTE TRANSFERRED.
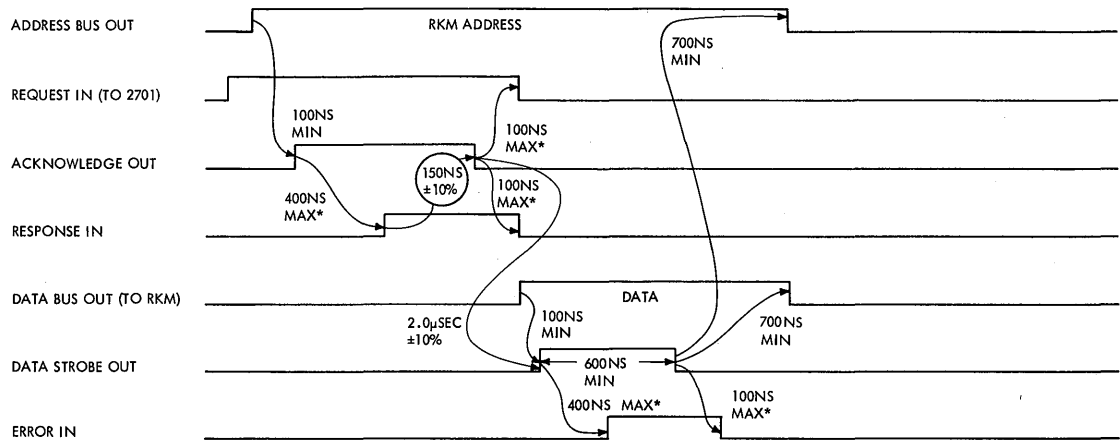
ADDRESS BUS OUT — RKM ADDRESS — 700NS MIN

REQUEST IN (TO 2701) — 100NS MIN — 100NS MAX*

ACKNOWLEDGE OUT — 150NS ±10% — 100NS MAX* — 400NS MAX*

RESPONSE IN — 100NS MAX*

DATA BUS OUT (TO RKM) — DATA — 2.0μSEC ±10% — 100NS MIN — 700NS MIN

DATA STROBE OUT — 600NS MIN — 400NS MAX* — 100NS MAX*

ERROR IN

NOTES: TIMING SHOWN AT 2701 CONNECTOR. TOLERANCES SHOWN AS MAXIMUM ASSUME A MINIMUM OF ZERO. TOLERANCES SHOWN AS MINIMUM ASSUME A MAXIMUM OF THE STATED VALUE PLUS 25%.

* RKM LOGIC DELAY. ASSUMING AN AVERAGE PROPAGATION DELAY OF 1.5NS PER FOOT, ADD 3.0NS TO THIS VALUE FOR EACH FOOT OF EXTERNAL CABLE USED BETWEEN THE 2701 AND THE RKM.

•Figure 7-7.   2701 to RKM Data Transfer

Out.  During a read sequence when the RKM is transferring data to the 2701 (Figure 7-5), the data must be stable on the DBI within 400ns after the rise of Acknowledge Out and the data must fall within 100ns after the fall of Acknowledge Out.  The DBI will be sampled when Response In is sensed at the 2701.

Order Out - During an initial selection sequence, the 2701 puts an RKM unit address on the ABO, a command on the DBO, and raises Order Out to tell the RKM to start the sequence specified by the command on the DBO.  Order Out will rise 100ns after the RKM address is put on the ABO and will remain up until Response In is received from the RKM (Figure 7-4).

Acknowledge Out - Acknowledge Out is the 2701 reply to Request In from any RKM.  During a read (Figure 7-5) sequence when the 2701 is ready to accept a byte of data, it raises Acknowledge Out.  This signal will remain active until Response In is received from the RKM. During a write operation (Figure 7-7) when the RKM raises its Request In line to ask for a byte of data, the 2701 replies with Acknowledge Out the same as for a read operation.
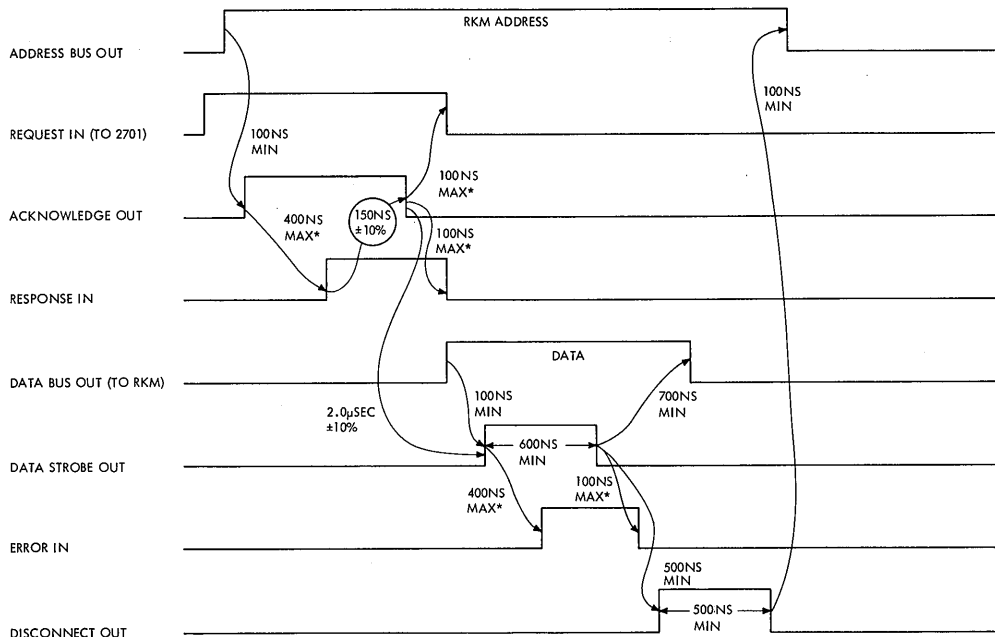
NOTES: TIMING SHOWN AT 2701 CONNECTOR. TOLERANCES SHOWN AS MAXIMUM ASSUME A
MINIMUM OF ZERO. TOLERANCES SHOWN AS MINIMUM ASSUME A MAXIMUM OF THE
STATED VALUE PLUS 25%.

* RKM LOGIC DELAY. ASSUMING AN AVERAGE PROPAGATION DELAY OF 1.5NS PER FOOT,
ADD 3.0NS TO THIS VALUE FOR EACH FOOT OF EXTERNAL CABLE USED BETWEEN THE 2701
AND THE RKM.

●Figure 7-8.  2701 to RKM Data Transfer with Ending Sequence

Data Strobe Out - The Data Strobe Out signal is only used during a
Write operation.  This line indicates to the RKM that data is stable
on the DBO.  The Data Strobe Line is brought up 100ns after the data
is put on the DBO and remains active for 600ns (Figure 7-7).

Disconnect Out - When the 2701 wishes to terminate a write operation
with any RKM, it raises Disconnect Out no earlier than 500ns after
Data Strobe drops (Figure 7-8) for the last byte to be transferred.
Disconnect Out will remain active for 500ns after which time the RKM
will not request any more data.  The RKM will not reply to the dis-
connect signal.  When the 2701 senses the terminate signal (Figure
7-6), it will raise Disconnect Out no sooner than 1.0us after the
fall of Acknowledge Out and hold it active for 500ns.  In either
case, the interface enters an idle state and the 2701 generates
ending status to the system.  When the 2701 wishes to terminate a
variable length message, it will send a 500nsec Disconnect Out Signal
to the RKM 1 usec after the fall of Acknowledge Out.

Response In - Response In indicates to the 2701 that the RKM has
sampled the data on the DBO during initial selection (Figure 7-4),
the RKM is ready to accept data during a Write sequence, or the RKM
has put data on the DBI during a Read sequence (Figure 7-5).  The RKM
must raise the Response In line within 400ns after the receipt of the

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rise of Order Out on an initial selection, or the receipt of the rise of Acknowledge Out on a read or write operation. The RKM must drop Response In within 100ns after the receipt of the fall of either Order Out or Acknowledge Out.

**Terminate In** - During a Read sequence, the RKM will raise Terminate In to stop a data transfer for fixed length messages only. The RKM must raise Terminate In within 400ns after the receipt of the rise of Acknowledge Out on the last byte of data to be read, and must drop within 100ns after the receipt of the fall of Acknowledge Out. The 2701 will respond with a 500ns Disconnect Out signal no sooner than 1 microsecond following the fall of Acknowledge Out.

**Error In** - Error In signals the 2701 that the RKM has detected a parity error on the DBO. The RKM must raise Error In within 400ns after the receipt of the rise of Data Strobe Out and drop within 100ns after the receipt of the fall of Data Strobe Out (Figure 7-7).

Simplex Lines

**Request In** - The Request In line from any RKM to the 2701 is a request by that RKM for the 2701 to read a byte of data, or it is a request for the 2701 to send a byte of data to it. This signal remains active until the RKM is serviced. The RKM must drop Request In within 100ns after the receipt of the fall of Acknowledge Out. The 2701 need not service the Request as soon as it is received.

**Interrupt A** - This signal is a 2.0usec pulse sent from the RKM to the 2701 as a result of a Read Display Constants command issued by the System. It signifies that the RKM has fetched the constants from the desired display and they can be read at this time. The 2701 will signal an Attention Interrupt to the IOCE upon receipt of Interrupt A.

**Interrupt B** - This line is pulsed by the RKM (2.0usec duration) whenever the RKM has completed a pass of all 32 consoles attached to it and has put data from one or more of these consoles into the Queue. The 2701 will signal an Attention Interrupt to the IOCE upon receipt of Interrupt B.

DAU/RKM Interface Sequences

There are four interface sequences to be considered: initial selection; read data from RKM; write data to RKM; and ending or disconnect sequence.

Initial Selection. Figure 7-4 summarizes the initial selection sequence and it's timing considerations.

Read Data from RKM. Figure 7-5 summarizes the read data from RKM sequence and it's timing considerations.

Write Data to RKM. Figure 7-7 summarizes the write data to RKM sequence and its timing considerations.

End or Disconnect. Figures 7-6 and 7-8 summarizes the end or disconnect sequences and their timing considerations.

## Electrical Characteristics - Multiplex Signals

All signals except Interrupt A, Interrupt B, and Request In between the 2701 and RKM will be over 28 conductor flat Mylar* insulated cables or equivalent. The transmission system is a balanced transmission system with states defined as follows:

Driver Output. (Measured at 2701 output connector with 145 ohm terminator from + signal to -signal with no cable attached.)

Power off condition all drivers: Signal Line differential voltage = 0.0v ± 1.0 mv.

| "1" State | 0 State |
|---|---|
| $V_a$ = +1 ± 0.2 volts | $V_a$ = -1 ± 0.2 volts |
| $V_b$ = -1 ± 0.2 volts | $V_b$ = +1 ± 0.2 volts |

Receiver Input

| "1" State | 0 State |
|---|---|
| $V_a$ = +0.8 ± 0.2 volts | $V_a$ = -0.8 ± 0.2 volts |
| $V_b$ = -0.8 ± 0.2 volts | $V_b$ = +0.8 ± 0.2 volts |

$V_a$ represents the dc level on the minus (-) signal line and $V_b$ represents the dc level on the plus (+) signal line. Refer to Table 7-2 for 2701 pin assignments.

All levels measured with respect to ground.

Line Characteristics - The impedance of the external cable is 145 ± 9 ohms with a capacitance of 20pf per foot or less. The resistance per foot, per conductor, is 0.043 ohms ± 10% at 20°C. The maximum skew between signal lines is 0.1 ns per foot. The attenuation is ≤ 4.0 db/100 ft at 10 MHz.

Receiver Input Characteristics

Power On/Off differential Z = 7.2K ± 3%.
Power On/Off each input to Ground Z = 3.6K ± 3%.

The above values are valid only with the line termination resistor disconnected.

Minimum input voltage required to switch states (differential).
$\Delta Vin_1$ = 0.6 Vdc

Maximum allowable differential input voltage.
$\Delta Vin_2$ = 15.0 Vdc

Maximum absolute input voltage for either input leg of the receiver.
$Vin_3$ = -13.2 Vdc to +15 Vdc.

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* Trademark of E. I. Dupont de Nemours & Co. (Inc.)

AC Characteristics. Differential Driver skew between signal lines 1 and 2 measured at the 2701 tailgate will be 50ns or less measured from the +1.0v level to the -1.0v level on the differential waveform.

Rise and fall times for Driver Output is 30ns +50% -90% when measured between ground and the +1.0v or -1.0v points on the differential waveform.

Fault Conditions - for both Simplex and Multiplex lines

1. A grounded signal line must not damage drivers, receivers or terminators.

2. Both lines shorted together must not damage drivers, receivers, or terminators.

3. An open line or terminator must not damage the driver or receiver circuit. (In the case of point to point simplex lines this condition may result in one signal line rising to 7.0 volts with respect to signal ground).

4. Power down at the RKM driver may cause a condition at the 2701 receiver circuit which could allow small noise signals to switch the receiver circuit. The 2701 will provide facilities for degating its receiver outputs where needed to prevent erroneous system interruption.

5. A receiver which is not connected to a driver circuit must not generate spurious signals.

Electrical Characteristics - Simplex Signals

The Interrupt A, Interrupt B, and Request In signals between the 2701 and RKM are carried by a 100-ohm balanced transmission system. The cable is an overall shielded cable containing multiple twisted pair conductors.

Line Driver. The driver output shall have the following specifications when a 100-ohm plus or minus 5% resistive terminator is connected between the + signal lead and the - signal lead at the output connector pins.

A logical one is represented by the + signal line being - 1.6 volts (+0.3v, -0.7v) with respect to the -signal line.

A logical zero is represented by the + signal line being +1.6 volts (-0.3v, +0.7v) with respect to the -signal line.
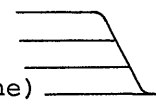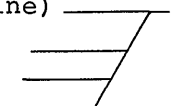
The + signal and -signal lines shall not exceed plus or minus 7.0 volts with respect to the DAU signal ground (DC return) when measured at the DAU output connector.

Rise and fall times shall not exceed 20ns (10% to 90% points) when measured from + signal or -signal line to ground. This measurement is made with no external cable attached and a 100 ohm ± 5% resistor connected between the associated + and -signal lines.

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Differential skew is defined as the time interval when the driver
output is not in a definite state.  The driver is in a indefinite
state when the differential voltage between the + and -signal
lines is less than 1.3 volts.  Differential skew will be 20ns or
less at the driver output.
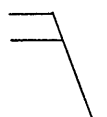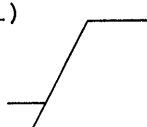
Driver Output

(Measured at output connector with 100-ohm terminator from + signal
to - signal)

                              Logical Zero

+ Signal Line              Max Level              +2.3v
Voltage measured           Nominal Level          +1.6v
in reference to            Min Level              +1.3v
-Signal Line                           Ref (-Signal Line)

                              Logical One

                                       Ref (-Signal Line)

+Signal Line               Min Level              -1.3v
Voltage measured           Nominal Level          -1.6v
in reference to the        Max Level              -2.3v
-Signal Line

Line Receiver - The characteristic impedance between + signal and
- signal lines at the input connector to the 2701 shall be 100 ohms
± 5%.  A logical "zero" is represented by the + signal line being
equal to or greater than +0.6 volts in respect to the - signal
line when measured at the receiver input.  A logical "one" is
represented by the + signal line being equal to or greater than
-0.6 volts in respect to the - signal line when measured at the
receiver input.  The + signal and - signal lines shall each remain
between + 3 volts and unit signal ground (DC return).

Receiver Input Requirements.

                              Logical Zero

+ Signal Line              Max Level              +3.0v
Voltage measured           Min Level              +0.6v
in reference to
the -Signal Line

                                       Ref (-Signal)

                              Logical One

                                       Ref (-Signal)

+ Signal Line
Voltage measured in
reference to the           Min Level              -0.6v
-Signal Line               Max Level              -3.0v

2701 - RKM Cabling

There are twenty-nine multiplex and three simplex signals between a
2701 and any RKM.  There can be two RKMs in one cabinet; therefore,
in a system configuration with five RKMs there will be three cabinets.

The 2701 provides four tailgate connectors for the RKM interface
(Figure 7-9).  Two connectors provide simplex and multiplex signals
for RKMs one, two, and three, while the other two cables provide
simplex and multiplex signals for RKMs four and five.  The cables
must meet the defined electrical specifications and must utilize
standard serpent-type connectors at the 2701 end.
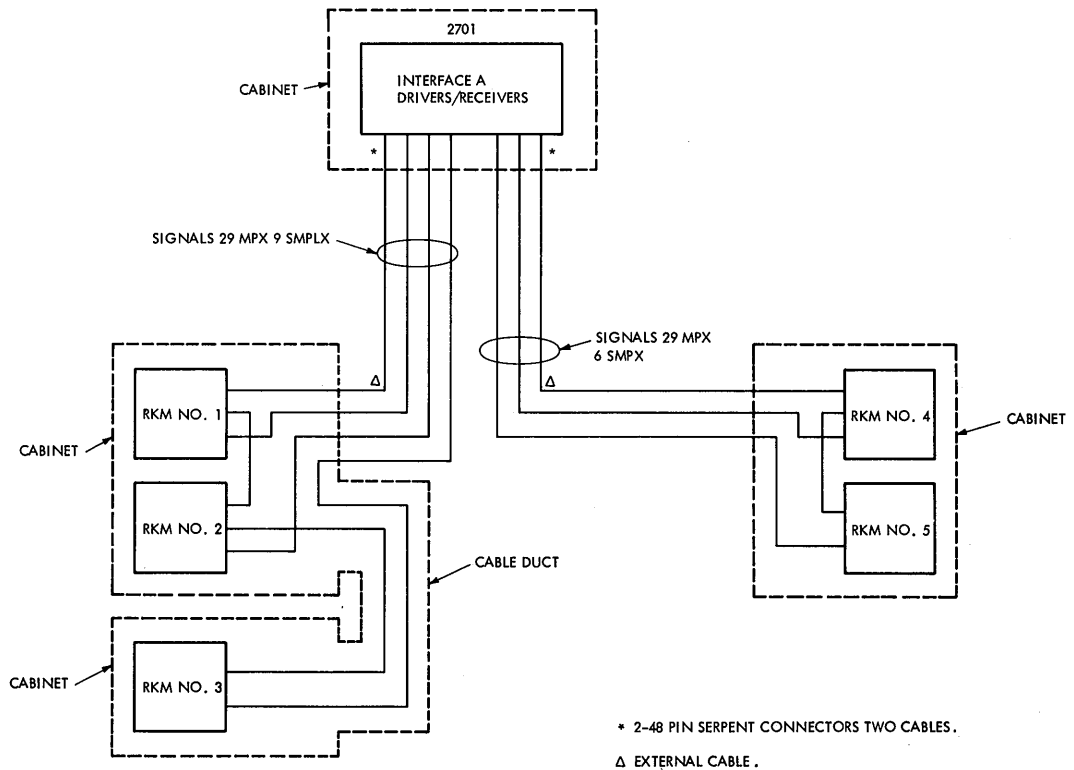


•Figure 7-9.  2701 - RKM Cabling Diagram

Cable and connector requirements at the 2701 are as follows:

|  |  |
|---|---|
| Multiplex In | 12 Line Pairs |
| Multiplex Out | 17 Line Pairs |
| Simplex (per 5 RKMs) | 15 Line Pairs |
|  | 44 Line Pairs Total |

    RKMs 1-3  Two 48-pin serpent connectors
    RKMs 4-5  Two 48-pin serpent connectors

Serpent Connector Blocks - All serpent connectors used in the 2701
will be 48-pin "B" style connector on the external cable to properly
mate with the "A" style mounted in the 2701.  Serpent contact term-
ination to termination contact resistance (includes 2 crimps and
mated contacts) will not exceed:

.020 ohms when used with #22 wire or larger
.030 ohms when used with #24 or #26 wire

External Cable Length - The maximum external cable length is 100 feet connector to connector (3 feet is used within the 2701).

MAINTENANCE PANELS

Each DAU is equipped with an Operators Panel, CE Panels, and connectors used to attach a Test Box. These panels and the test box allow maintenance personnel to exercise the DAU and its interfaces in an off line environment.

Operators Panel

The Operators Panel provides DAU power on/off capabilities and control over DAU/IOCE interfaces. The following indicators and switches are provided on the panel.

Power On- This is an indicator/pushbutton type switch. Depressing it turns power on. Upon completion of the power on sequence the indicator is lit.

Power Off- This is an indicator/pushbutton type switch. Depressing it turns DAU power off. When power is off, the indicator is lit, providing A.C. power is being supplied to the box.

Enable/Disable- Two of these toggle switches are provided per DAU. One switch is used for each of the IOCE interfaces. When disabled, the DAU will ignore any activity on that interface.

OFFLINE Indicator- This indicator is lit whenever the DAU is operating in the Offline mode.

State Ø Indicator - This indicator is lit whenever the DAU is in State Ø (SØ & S1 positions of the CR are ØØ).

CE Panel

This panel is not accessible without opening the DAU covers. The switches provided and their functions are as follows:

The I/O Test box contains indicator and switches which allow data and tag control signals to be manipulated in such a way as to let the maintenance man simulate both the IOCE and RKM interface. The indicator show data and control signals throughout the entire DAU.

ON/OFF Line - This switch removes the DAU from the On-Line mode and makes it unavailable to the IOCE's.

Driver Degate - This switch is used to degate all the drivers and receivers in the IOCE/DAU interfaces.

Record Lock - This switch is used to force burst mode on the IOCE Interface.

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Table 7-2.   2701 Pin Assignments

| Pin | Connector 01S-A1A3 Line Name | Pin | Connector 01S-A1A4 Line Name |
|-----|------------------------------|-----|------------------------------|
| B02 | + Interrupt In A1 | B02 | - Data Bus In 4 1-3 |
| D02 | - Interrupt In A1 | D02 | + Data Bus In 4 1-3 |
| D03 | + Interrupt In B1 | D03 | - Data Bus In 5 1-3 |
| B03 | - Interrupt In B1 | B03 | + Data Bus In 5 1-3 |
| B04 | + Interrupt In A2 | B04 | - Data Bus In 6 1-3 |
| D04 | - Interrupt In A2 | D04 | + Data Bus In 6 1-3 |
| D05 | + Interrupt In B2 | D05 | - Data Bus In 7 1-3 |
| B05 | - Interrupt In B2 | B05 | + Data Bus In 7 1-3 |
| B06 | + Interrupt In A3 | B06 | - Data Bus In P 1-3 |
| D06 | - Interrupt In A3 | D06 | + Data Bus In P 1-3 |
| D07 | + Interrupt In B3 | B09 | + Address Bus Out 0 1-3 |
| B07 | - Interrupt In B3 | D09 | - Address Bus Out 0 1-3 |
| D08 | GND | B08 | GND |
| B08 | - Response In 1-3 | D08 | GND |
| D09 | + Response In 1-3 | D10 | - Address Bus Out 1 1-3 |
| D10 | - Error In 1-3 | B10 | + Address Bus Out 1 1-3 |
| B09 | + Error In 1-3 | B11 | - Address Bus Out 2 1-3 |
| B10 | - Order Out 1-3 | D11 | + Address Bus Out 2 1-3 |
| D11 | + Order Out 1-3 | D12 | - Address Bus Out 3 1-3 |
| D12 | - Acknowledge Out 1-3 | B12 | + Address Bus Out 3 1-3 |
| B11 | + Acknowledge Out 1-3 | G02 | - Data Bus Out 0 1-3 |
| B13 | GND | J02 | + Data Bus Out 0 1-3 |
| B12 | - Disconnect Out 1-3 | J03 | - Data Bus Out 1 1-3 |
| D13 | + Disconnect Out 1-3 | G03 | + Data Bus Out 1 1-3 |
| G02 | - Terminate In 1-3 | G04 | - Data Bus Out 2 1-3 |
| J02 | + Terminate In 1-3 | J04 | + Data Bus Out 2 1-3 |
| J03 | + Request In 1 | J05 | - Data Bus Out 3 1-3 |
| G03 | - Request In 1 | G05 | + Data Bus Out 3 1-3 |
| G04 | + Request In 2 | G06 | - Data Bus Out 4 1-3 |
| J04 | - Request In 2 | J06 | + Data Bus Out 4 1-3 |
| J05 | + Request In 3 | J07 | - Data Bus Out 5 1-3 |
| G05 | - Request In 3 | G07 | + Data Bus Out 5 1-3 |
| G06 | - Data Bus In 0 1-3 | J08 | GND |
| J06 | + Data Bus In 0 1-3 | G08 | - Data Bus Out 6 1-3 |
| J07 | - Data Bus In 1 1-3 | J09 | + Data Bus Out 6 1-3 |
| G07 | + Data Bus In 1 1-3 | J10 | - Data Bus Out 7 1-3 |
| G08 | - Data Bus In 2 1-3 | G09 | + Data Bus Out 7 1-3 |
| J09 | + Data Bus In 2 1-3 | G10 | - Data Bus Out P 1-3 |
| J08 | GND | J11 | + Data Bus Out P 1-3 |
| J10 | - Data Bus In 3 1-3 | G11 | GND |
| G09 | + Data Bus In 3 1-3 | G12 | GND |
| G10 | GND | J12 | GND |
| J12 | - Data Strobe Out 1-3 | G13 | GND |
| G12 | + Data Strobe Out 1-3 | J13 | GND |
| G11 | GND | | |
| J11 | GND | | |
| G13 | GND | | |
| J13 | GND | | |

Table 7-2. 2701 Pin Assignments (cont)

| Pin | Connector 01S-A1A5 Line Name | Pin | Connector 01S-A1A6 Line Name |
|---|---|---|---|
| B02 | + Interrupt In A4 | B02 | - Data Bus In 4 4-5 |
| D02 | - Interrupt In A4 | D02 | + Data Bus In 4 4-5 |
| D04 | + Interrupt In B4 | D04 | - Data Bus In 5 4-5 |
| B03 | - Interrupt In B4 | B03 | + Data Bus In 5 4-5 |
| B04 | + Interrupt In A5 | B04 | - Data Bus In 6 4-5 |
| D05 | - Interrupt In A5 | D05 | + Data Bus In 6 4-5 |
| D06 | + Interrupt In B5 | D06 | - Data Bus In 7 4-5 |
| B05 | - Interrupt In B5 | B05 | + Data Bus In 7 4-5 |
| B07 | - Response In 4-5 | B07 | - Data Bus In P 4-5 |
| D09 | + Response In 4-5 | D07 | + Data Bus In P 4-5 |
| D10 | - Error In 4-5 | B08 | GND |
| B08 | + Error In 4-5 | D08 | GND |
| D08 | GND | B09 | + Address Bus Out 0 4-5 |
| B09 | - Order Out 4-5 | D09 | - Address Bus Out 0 4-5 |
| D11 | + Order Out 4-5 | D10 | - Address Bus Out 1 4-5 |
| D12 | - Acknowledge Out 4-5 | B10 | + Address Bus Out 1 4-5 |
| B10 | + Acknowledge Out 4-5 | B11 | GND |
| B12 | - Disconnect Out 4-5 | D11 | GND |
| D13 | + Disconnect Out 4-5 | B12 | - Address Bus Out 2 4-5 |
| B13 | GND | D12 | + Address Bus Out 2 4-5 |
| G02 | - Terminate In 4-5 | D13 | - Address Bus Out 3 4-5 |
| J02 | + Terminate In 4-5 | B13 | + Address Bus Out 3 4-5 |
| J04 | + Request In 4 | G02 | - Data Bus Out 0 4-5 |
| G03 | - Request In 4 | J02 | + Data Bus Out 0 4-5 |
| G04 | + Request In 5 | J04 | - Data Bus Out 1 4-5 |
| J05 | - Request In 5 | G03 | + Data Bus Out 1 4-5 |
| J06 | - Data Bus In 0 4-5 | G04 | - Data Bus Out 2 4-5 |
| G05 | + Data Bus In 0 4-5 | J05 | + Data Bus Out 2 4-5 |
| J07 | - Data Bus In 1 4-5 | J06 | - Data Bus Out 3 4-5 |
| G07 | + Data Bus In 1 4-5 | G05 | + Data Bus Out 3 4-5 |
| J08 | GND | G07 | - Data Bus Out 4 4-5 |
| G08 | - Data Bus In 2 4-5 | J07 | + Data Bus Out 4 4-5 |
| J09 | + Data Bus In 2 4-5 | J08 | GND |
| J10 | - Data Bus In 3 4-5 | J09 | - Data Bus Out 5 4-5 |
| G09 | + Data Bus In 3 4-5 | G08 | + Data Bus Out 5 4-5 |
| G10 | GND | G09 | - Data Bus Out 6 4-5 |
| G11 | GND | J10 | + Data Bus Out 6 4-5 |
| J11 | GND | G11 | GND |
| J12 | - Data Strobe Out 4-5 | J11 | - Data Bus Out 7 4-5 |
| G12 | + Data Strobe Out 4-5 | G10 | + Data Bus Out 7 4-5 |
| G13 | GND | G12 | - Data Bus Out P 4-5 |
| J13 | GND | J12 | + Data Bus Out P 4-5 |
|  |  | G13 | GND |
|  |  | J13 | GND |

INTRODUCTION

The 9020D and the 9020E, with their various system elements, may
be structured into many different configurations, with varying
degrees of autonomy or interdependency.   The equipment and tech-
niques used to achieve the various configurations have been class-
ified under the aggregate heading of Configuration Control.

The controlling mechanism for the 9020D and 9020E will be the
Executive Control (EXC) program.*   Neither system has a preferred
system structure;   i.e., no inherent master-slave relationships
which require that a specific computing element exercise primary
control.   Configuration Control does contain certain features
which could, however, restrict the critical control functions to
designated computing elements in order to obtain an orderly pro-
cessing of the ATC task.

The use of both the 9020D and 9020E in the National Airspace
System imposes certain fundamental requirements upon the systems
with respect to their ability to assume various sub-system con-
figurations.   These requirements stem from the total nature of the
ATC task, including both the critical operational work and the
important, but necessarily subservient, support functions.

   a.   When units of the 9020D or 9020E Systems are actively
        engaged in performing the ATC operational task, other
        units not so engaged, or malfunctioning units, must not
        be permitted to interfere.

   b.   If units of the 9020D or 9020E are not required for the
        operational task, they should be available for subsidiary
        tasks or maintenance.

   c.   Those units of 9020D or 9020E which are not actually
        malfunctioning or undergoing maintenance should be
        immediately available to EXC to perform the operational
        task, regardless of their current subsidiary tasks.

   d.   Units requiring maintenance must be provided with adequate
        maintenance facilities and effective isolation from the
        remainder of the operating system.

GENERAL CHARACTERISTICS

Configuration control establishes the instantaneous system struc-
tures of both the 9020D and 9020E by specifying to each major
system element which other major system elements it may commun-
icate with at any given time.   This communication between major

*EXC is a non-deliverable item under Contract No. FA64WA-5223.

system elements consists of data and/or control information. To achieve the requisite flexibility, separate controllable paths for both types of information flow between elements are provided.

The elements which are included in the configuration control structure of the 9020D and 9020E systems and consequently, for discussion within this chapter, considered to be major system elements, are as follows:

| 9020D | 9020E |
|---|---|
| ● Computing Elements | ● Computing Elements |
| ● Input/Output Control Elements | ● Input/Output Control Elements |
| ● Storage Elements | ● Storage Elements |
| ● Peripheral Adapter Modules | ● Display Elements |
| ● Tape Control Units | ● Configuration Console |
| ● Storage Control Units | ● Tape Control Units |

NOTE: The 2701 DAU, while containing a Configuration Control Register, does not directly receive configuration information from a CE nor does the 2701 have a direct input path to any CE Diagnose Accessible Register as do those elements listed above. For these reasons, the discussions of 2701 configuration control are included in Chapters 7 (Data Adapter Unit) and 10 (Configuration Console).

GENERAL DESCRIPTION OF ELEMENT STATES

Each major system element of both the 9020D and 9020E can be in one of four states. These states are established by EXC via configuration control. Element states are closely related to the immediate role of the element in the overall ATC task. The following four sub-sections describe generally each state. For a more detailed analysis of each state, see Figure 8-1.

State Three

If a major system element is designated as being in State Three by EXC, the element is presumed to be at its highest operational capability level. Normally, it is presumed that the ATC operational task would be run in this state. A CE in State Three has the ability to initiate reconfiguration of the existing system structure subject to the information and control paths established by EXC.

State Two

A major system element designated by EXC as being in State Two is considered free of malfunctions and completely capable of performing the ATC operational task, except that a CE in this state cannot effect a system reconfiguration. While in State Two, a major system element might be employed in performing subsidiary processing tasks, but it is capable of being immediately recalled by EXC to

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| | STATE BITS | | ISSUE SCON$_1$ | ACCEPT SCON | CE ELC MASKABLE$_6$ | ELEMENT CONTROLS | MAINTENANCE CONTROLS | SYSTEM CONSOLE- CONFIGURATION CONSOLE CONTROLS | POWER AND CCR CONTROLS |
|---|---|---|---|---|---|---|---|---|---|
| | $S_0$ | $S_1$ | | | | | | | |
| THREE | 1 | 1 | YES | YES$_3$ | YES | NO | NO | YES$_9$ | NO |
| TWO | 1 | 0 | NO$_2$ | YES$_3$ | NO | NO | NO | YES$_9$ | NO |
| ONE | 0 | 1 | NO$_2$ | YES$_3$ | NO | YES | NO | YES$_9$ | NO |
| ZERO TEST SWITCH "OFF" | 0 | 0 | YES | YES$_3$ | NO | YES | NO$_8$ | YES$_9$ | NO |
| ZERO TEST SWITCH "ON" | 0 | 0 | YES$_4$ | NO$_5$ | YES | YES | YES | NO | YES |

NOTES: 1. WHERE "YES" IS ENTERED, IT IMPLIES A LEGAL OR PERMISSIVE ABILITY TO ISSUE SCON. THE ISSUING CE MUST HAVE ITS OWN SCON BIT SET AND MEET ALL OTHER SCON RESTRICTIONS.

2. IF A CE ATTEMPTS SCON, A SPECIFICATION CHECK INTERRUPTION WILL RESULT. NO SIGNALS WILL ISSUE TO OTHER ELEMENTS.

3. RECEIVING ELEMENT MUST HAVE PROPER SCON BIT SET.

4. WHEN SWITCH IS "ON", SCON WILL NOT AFFECT ANY EXTERNAL ELEMENT. THE ISSUING CE MAY ACCEPT SCON FROM ITSELF. WHEN THE TEST SWITCH IS "ON", IT WILL BE POSSIBLE FOR A CE TO HAVE ITS STATE BITS CHANGED MANUALLY. IF THE STATE BITS ARE CHANGED FROM 00 TO 11, SCON MAY BE EXERCISED BY THE CE, BUT NO ELEMENT EXCEPT THE ISSUING CE WILL RESPOND. IF THE STATE BITS ARE CHANGED TO 10 OR 01, NOTE 2 APPLIES.

5. SCON'S WILL BE REJECTED REGARDLESS OF CCR, EXCEPT THAT A CE MAY ACCEPT SCON FROM ITSELF IF IT HAS ITS OWN SCON BIT SET.

6. THIS COLUMN APPLIES TO RECEIVING CE'S. INCOMING CE ELC'S ARE MASKED BY SCON BITS IN RECEIVING CE'S, AS EXPLAINED IN FIGURE 8-8. WHERE "YES" IS ENTERED, THE ELC MAY ALSO BE MASKED BY NORMAL INTERRUPTION MASK CONTROLS. WHERE "NO" IS ENTERED, NO FURTHER MASKING IS POSSIBLE.

7. THESE INCLUDE: IPL, INTERRUPT, STORE, DISPLAY, RATE SWITCH, ADDRESS COMPARE, PSW RESTART, SET IC, START, STOP, S/360 MODE SWITCH.

8. MAINTENANCE CONTROLS ARE GENERALLY DISABLED EXCEPT WHERE OTHER TRUTH TABLES INDICATE EXCEPTIONS.

9. SYSTEM CONSOLE OR CONFIGURATION CONSOLE SYSTEM INTERLOCK SWITCH "ON".

Figure 8-1.   Summary of State Definitions

assist other units in an operational task or to replace a malfunc-
tioning unit. It is assumed that any subsidiary programs run while
in State Two will be debugged and under tight monitor control.
Preventive maintenance programs of the "confidence routine" variety
may also be effectively run in this state. If a computing element
has been designated by EXC to be recallable, it will automatically
interrupt its current tasks and go to State Three when certain
check signals are received from other computing elements.

State One

State One may be considered to be a quasi-redundant state. When in
State One, an element may be designated as recallable by EXC. How-
ever, certain operator manual controls will be enabled. These
controls will provide the necessary manual intervention to debug
programs and run diagnostic programs. Thus, this state permits a
non-malfunctioning unit to be used for various tasks which are not
sufficiently predictable to be run in State Two with its tight
monitor control, yet remain available to EXC for operational use.
As in State Two, a CE in State One, when designated as recallable,
will automatically terminate its current task and go to State Three
upon receipt of certain check signals from other CE's.

State Zero

To accommodate the maintenance needs of the 9020D and 9020E, State
Zero has been provided. The zero state is actually composed of two
sub-states. The desired sub-state is selected by a switch which is
enabled in only zero state, i.e., state field = 00.

    With the Test switch Off, the zero state is considered primarily
useful for subsystem testing. All manual controls, except those
governing the manual setting of CCR's, ATR's, PSBAR's and those
which turn off element power, are enabled. An element may, however,
be recalled by EXC if it has been designated as recallable. If so
designated, a CE will go to State Three upon receipt of certain
check signals from other computing elements. Effective subsystem
isolation can be retained in this mode if desired. Care must be
exercised when in the zero state with the Test switch off, due to
the availability of most manual intervention capabilities of the
system. It is assumed that a system performing the ATC task will
protect itself, via configuration control, from spurious signals
generated by a subsystem under test.

    When an element's Test switch is On it is isolated from the
remainder of the system to the extent required for its stand-alone
or unit test operations to be used. In the case of PAM, TCU, SCU,
DE, SE, and RCU, this is a blanket isolation, i.e., all system inter-
faces are closed. For the CE and IOCE, this isolation is primarily
achieved by refusing to accept the SCON instruction. (In the case
of CE's from other CE's.) Complete isolation is not desirable for
these elements. In this sub-state, all manual controls including
power and manual CCR controls are active. To preclude loss of switch
control, the state bits of each element will be reset to State Zero
(00) whenever the Test switch is turned off after having been in the
On state.

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SCON INSTRUCTION

The Set Configuration (SCON) instruction is the program means by which the 9020D or 9020E may be configured into the desired system configuration.  SCON establishes the system configuration by specifying to the system elements:  (a) the state they are to assume, (b) the CE's which can issue future SCON instructions to them, and (c) the system elements they may communicate with via their data paths,  (d) ILOS, IDES.

Two conditions imposed on the use of SCON are not given by Figure 8-1.  They are:

1.  The SCON instruction can be issued by a CE only when it is in the supervisor state.  If SCON is attempted in the problem state, a program interruption (privileged exception) will result.

2.  The SCON instruction must configure a system element so that it will accept future SCON instructions from at least one CE.  An automatic check is made to insure this and if the condition is violated a program check (specification exception) will occur.

CONFIGURATION CONTROL REGISTER

Configuration control, in conjunction with the interface circuitry design, provides a protection facility for active system components from a malfunctioning system component.  When one system component is not configured to communicate with another, circuit failures and/or spurious signal emissions from one component will not disrupt the operation of the other.

The configuration control register (CCR) is a physical register in each major system element.  The CCR is set by SCON, and contains the information necessary to establish the state of the element to which it is attached, the CE's from whom it will accept future SCON's, and the other system elements with which it may communicate. The CCR of each CE and IOCE will also indicate if a "Logout Stop" of the SE or DE should take place for an SE or DE logout, respectively.  The CCR of each DE will, additionally, indicate if a Logout Stop state should be immediately entered upon encountering a DE malfunction related to a Display Generator access.  Because of the various functions of the system elements, there are differences in the format of their respective CCR's.  The CCR format for each 9020D System Element is shown on Figure 8-2, while the format for each 9020E System Element is shown in Figure 8-3.  A position is assumed to be set when it contains a "1".

The CCR in each major system element consists of a state field, SCON field, and a communications field.  Additionally, an Inhibit Logout-Stop (ILOS) field is contained in each CE and IOCE and an Inhibit Display Element Stop (IDES) in each DE.

**CE**

| P0 | | | | | | P1 | | | | | | | | | | | | P2 | | | | | P3 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STATE | | SCON | | | | | | SE | | | | | | | | | | | | CE | | | | | | | | | IOCE | | |
| S0 | S1 | 1 | 2 | 3 | 4 | A | * | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | * | * | 1 | 2 | 3 | 4 | * | * | * | * | * | * | 1 | 2 | 3 |
| 0 | 1 | 2 | | | 5 | 6 | 7 | 8 | | | | | | | | 17 | 18 | 19 | 20 | | 23 | 24 | | | | 28 | 29 | | 31 | | |

**IOCE**

| P0 | | | | | | P1 | | | | | | | | | | | | P2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STATE | | SCON | | | | | | SE | | | | | | | | | | | | CE | | |
| S0 | S1 | 1 | 2 | 3 | 4 | A | * | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | * | * | 1 | 2 | 3 | 4 |
| 0 | 1 | 2 | | | 5 | 6 | 7 | 8 | | | | | | | | 17 | 18 | 19 | 20 | | | 23 |

**SE**

| P4 | | | | | | | P7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STATE | | SCON | | | | | | CE | | | | | IOCE | |
| S0 | S1 | 1 | 2 | 3 | 4 | * | * | 1 | 2 | 3 | 4 | * | 1 | 2 | 3 |
| 0 | 1 | 2 | | | 5 | 6 | 7 | 8 | | | 11 | 12 | 13 | 15 |

**PAM, SCU, AND TCU**

| P0 | | | | | | P3 | | |
|---|---|---|---|---|---|---|---|---|
| STATE | | SCON | | | | IOCE | | |
| S0 | S1 | 1 | 2 | 3 | 4 | 1 | 2 | 3 |
| 0 | 1 | 2 | | 5 | 6 | 8 | |

NOTES: 1. * DENOTES UNUSED BITS WHICH MAY BE ONE OR ZERO.

2. MAXIMUM CONFIGURATION IS ASSUMED. FOR LESSER SYSTEMS, THOSE BITS NOT REQUIRED BECOME SPARES.

3. COMPLETE MASK IS TRANSMITTED TO SE'S VIA THE STORAGE DATA BUS AND SE'S GATE IN REQUIRED FIELDS. SDBI TRANSMISSION IS AS FOLLOWS:

| P0 | P1 | P2 | P3 | P4 | | | | | | | | P5 | P6 | P7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | STATE | | SCON | | | | | | | | CE | | | | | IOCE | | |
| * | * | * | * | S0 | S1 | 1 | 2 | 3 | 4 | A | * | * | * | 1 | 2 | 3 | 4 | * | 1 | 2 | 3 |
| 0 | 7 8 | 15 16 | 23 24 | 31 32 | | | | | | 39 40 | | 47 48 | | 55 56 | | | | | | | 63 |

* DENOTES UNUSED BITS WHICH MAY BE ZERO OR ONE.

4. PAM'S AND TCU'S RECEIVE ONLY THE INDICATED BITS.

5. "A" IN BIT 6 DENOTES INHIBIT LOGOUT STOP.

●Figure 8-2. 9020D Configuration Control Register Format

State Field

The <u>State</u> field contained in each major system element's CCR indicates which of four states has been established for each element.

NOTES: 1. * DENOTES UNUSED BITS WHICH MAY BE ONE OR ZERO.

2. MAXIMUM CONFIGURATION IS ASSUMED. FOR LESSER SYSTEMS, THOSE BITS NOT REQUIRED BECOME SPARES.

3. COMPLETE MASK IS TRANSMITTED TO SE'S AND DE'S VIA THE STORAGE DATA BUS; SE'S AND DE'S GATE IN THE REQUIRED FIELDS. SDBI TRANSMISSION IS AS FOLLOWS.



* DENOTES UNUSED BITS WHICH MAY BE ZERO OR ONE.

4. TCU'S AND RCU'S RECEIVE ONLY THE INDICATED BITS.

5. "A" IN BIT 6 INDICATES INHIBIT LOGOUT STOP.

6. "B" IN BIT 23 INDICATES INHIBIT DISPLAY ELEMENT STOP.

●Figure 8-3.  9020E Configuration Control Register Format

SCON Field

The SCON field contained in each major system element's CCR indicates which CE, when in State 0 or 3, may issue the SCON instruction to other major system elements.

Communications Field

The Communications field contained in each major system element's
CCR indicates to each individual element those other major system
elements with which it may communicate.  Two-way communication
between most major system elements requires that the appropriate
communication bits be set on at both ends of the communication path
(i.e., in the CCR of both major system elements).  Exceptions to this
rule are the IOCE/TCU, IOCE/PAM, IOCE/SCU, IOCE/RCU, and DE/DG inter-
faces.


ILOS Field

The ILOS bit, which is contained in the CCR of each IOCE and CE
determines if a Logout Stop signal is returned by these elements
upon receipt of a Storage Check (IOCE) from an SE or, an Address
Check or Data Check (CE) from either an SE or DE.

IDES Field

The IDES bit, which is contained in the CCR of each DE, determines
if this element ignores detection of a storage malfunction during a
storage access by a display generator.

        A communication or SCON bit, when set, enables the inter-
face from the associated unit,  In some cases this may involve only
the control lines, and in other cases may also involve data lines.
In the use of all interfaces, some control action is required before
any data bus is examined.  If this control function is inhibited,
it is unnecessary to further degate the data bus since it will not
be examined.  Signals to the DAR are not gated by the CCR because
it may be desirable to monitor the status of an element without
being required to communicate with it.  Also, response signals to
reconfigurations are not gated by the issuing CE's CCR since it is
desirable to reconfigure elements without being required to accept
other communications from them.

        The error detection circuitry of the system provides the
protection from propagation of logic errors.  The program may then
use configuration control to isolate the malfunctioning unit for main-
tenance purposes.  Each power supply contains an over-voltage and
over-current sensor which, when activated, will turn the power off
in that unit before damage occurs.  Configuration control provides
degating from units with normal power status.

    The circuitry which directly connects to a distributed simplex
interface has been designed so that the interface will not be dis-
abled by commonly encountered component failures, unless, of course,
the failure occurs in the primary element.  The latter case is
exemplified by a component failure in the drivers on the CE to 10
SE/DE interfaces, while the former is exemplified by a component
failure in an SE or DE receiver in the same interface.

    The circuitry which is directly connected to the I/O Interface,
Channel to Device Control Unit, in the PAM, SCU, TCU, System Console,
DAU and Configuration Console has been designed so that power may be
turned on and off in these units without disrupting any activity

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not concerning that unit in the interface. Also, in the interfaces
in the 9020D or 9020E Systems of the type exemplified by the one
from a CE to 10 SE's and/or DE's, turning power on and off in an
SE connected to that interface will not disrupt the functioning of
that interface. However, in order to prevent turning power on and
off in the CE from disrupting the activities of the SE's connected
to that interface, the SE's must be configured not to accept com-
munications from that CE.

## Configuration Mask

The Configuration Mask (CM) is made available to SCON from either
(9020D) or (9020E) General Purpose Registers. The contents are
loaded by SCON into the CCR of major system elements. The CM
contains the necessary configuration control information appropriate
to each element. The CM format for a 9020D System is shown in
Figure 8-4, and the CM format for a 9020E System is shown in Figure
8-5. The CM format is sufficient to contain necessary configuration
data for any type of element. For those elements which do not need
all its contents, the necessary data is selectively sent.

## Selection Mask

The Selection Mask (SM), shown in Figure 8-4 (9020D) and Figure 8-5
(9020E) is made available to SCON from a general purpose register.
The SM designates the elements to receive the data contained in the
CM when SCON is issued. In effect, the SM is an address word for
the CM. Multiple CCR's may be set with one SCON instruction, pro-
vided that identical configuration masks are to be used in each
receiving element.

## SYSTEM MONITORING

The 9020D System and the 9020E System each consist of multiple
elements which may be configured to accomplish various tasks. These
tasks may be divided into two major categories: ATC related and non-
ATC related. The non-ATC related category includes "good" elements
running diagnostics (or other programs) and elements which are not
"good" due to malfunctions, maintenance, or engineering change act-
ivity.

The previous section described the CCR and its control of data
communication between elements, the four element states, and SCON
ability of elements. This section describes the method for monitor-
ing system malfunctions. This monitoring system must be separated
from the CCR since on many occasions subsystems will be separate
from the standpoint of data communication, but not from the stand-
point of malfunction monitoring or system control. More explicitly,
the system performing the ATC task should monitor certain classes of
element malfunctions, which may be generated by other elements in
State Two or State One performing other tasks, since these other
elements may be called on at any time to do the ATC task.

Monitoring takes on two general forms, namely, program com-
munication and hardware communication between subsystems.

8-9

**CONFIGURATION MASK**

| STATE | SCON | | | SE | | | CE | | IOCE | |
|---|---|---|---|---|---|---|---|---|---|---|

S0 S1 | 1 2 3 4 A * | 1 2 3 4 5 6 7 8 9 10 * * | 1 2 3 4 * * * * * * | 1 2 3 | *

0 1 2  5 6 7 8  17 18 19 20  23 24  28 29  31 32  63

**SELECTION MASK**

| PAM | TCU | | | SE | | | CE | | SCU | | IOCE | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

1 2 3 | 1 2 3 * * | 1 2 3 4 5 6 7 8 9 10 * * | 1 2 3 4 | 1 2 3 * * | 1 2 3

0  2 3  5 6 7 8  17 18 19 20  23 24  26  28 29  31

NOTES: 1. * DENOTES UNUSED BITS WHICH MAY BE ZERO OR ONE.
2. MAXIMUM CONFIGURATION IS ASSUMED. FOR LESSER SYSTEMS, THOSE BITS NOT REQUIRED BECOME SPARES.
3. THE "A" ON BIT POSITION 6 DENOTES INHIBIT LOGOUT STOP.

●Figure 8-4.  9020D Configuration Mask and Selection Mask Formats

**CONFIGURATION MASK**

| STATE | SCON | | | SE | DE | CE | | IOCE | DG | | |
|---|---|---|---|---|---|---|---|---|---|---|---|

S0 S1 | 1 2 3 4 A B | 1 2 3 4 5 | 1 2 3 4 5 * * | 1 2 3 4 * * * * * * | 1 2 3 | 1A 1B 2B 2C 3C 3D 4D 4A 5A 5B 6B 6C 7C 7D 8D 8A | *

0 1 2  5 6 7 8  12 13  17 18 19 20  23 24  28 29  31 32  47 48  63

**SELECTION MASK**

| RCU | TCU | | | SE | DE | CE | | IOCE | |
|---|---|---|---|---|---|---|---|---|---|---|

1 2 * | 1 2 3 * * | 1 2 3 4 5 | 1 2 3 4 5 * * | 1 2 3 4 * * * * * * | 1 2 3

0 1 2 3  5 6 7 8  12 13  17 18 19 20  23 24  28 29  31

NOTES: 1. * DENOTES UNUSED BITS WHICH MAY BE ZERO OR ONE.
2. MAXIMUM CONFIGURATION IS ASSUMED.  FOR LESSER SYSTEMS, THOSE BITS NOT REQUIRED BECOME SPARE.
3. THE "A" IN BIT POSITION 6 DENOTES INHIBIT LOGOUT STEP.
4. THE "B" IN BIT POSITION 7 DENOTES INHIBIT DISPLAY ELEMENT STEP.

Figure 8-5.  9020E Configuration Mask and Selection Mask Formats

Program Communication

Certain normal element malfunctions (e.g., Tape Drive logic failure, PAM channel logic failure, etc.) must be handled by the subsystem monitor program and communicated to the ATC EXC in an orderly fashion.

Hardware Communication

Certain element malfunctions are of specific interest to the EXC program directly and therefore hardware facilities are provided to communicate the conditions. Included are those items which cannot be handled by the subsystem (e.g., CCR failure in PAM, power fail- ure in TCU) since normal lines of communication may not exist. Also these elements might be idle, i.e., not part of a subsystem, when these conditions occur. Certain malfunctions in SE's or CE's might place the subsystem in such a position that program communication is no longer possible.

The hardware communication lines utilize the external interrup- tion facility to all CE's in order to notify the EXC of a particular condition.

Overall Operation

Figure 8-6 shows the general method of monitoring one element mal- functions by another. The case presented is the interruption of a CE to control the analysis procedure and determine a course of action after a malfunction is detected in another CE. Simplifying assumptions have been made (e.g., intermittent parity check) to present the philosophy. The two CE's are labeled malfunctioning and "attentive" since the attentive element need only be configured to listen to the malfunctioning CE and is not necessarily performing the ATC task (as may have been inferred previously). No indication is given of the masking which could be performed.

The general course of action taken in this situation may be divided into four phases, labeled A, B, C, and D on Figure 8-6.

A. The malfunctioning CE detects an error. It stops its current processing and generates an element check to all CE's. After a delay period, it then proceeds to perform its own logout in three parts, as shown.

B. An "attentive" CE responds to the element check by accepting an external interruption. It will indicate to the malfunc- tioning CE (by alteration of a program in storage) that there is a listening element. The attentive CE will then perform the necessary "first line" analysis of the situation, in order to determine the immediate course of action neces- sary. This could also be extended to include a reasonably detailed analysis of logout data from the malfunctioning CE.

C. The malfunctioning CE now waits until action is taken by the attentive CE. If the malfunctioning CE had not been informed

MALFUNCTIONING CE                                    ATTENTIVE CE

SOFTWARE                    HARDWARE

```
                        ┌──────────────────┐
                        │   MALFUNCTION    │
            STOP        │   DETECTED       │
    ◄───────────────────┤                  │
                        └──────────────────┘

                            ELEMENT CHECK          ┌──────────────────┐
                        ●──────────────────────────►   EXTERNAL       │
                                                   │   INTERRUPTION    │
                                                   │   PROCESSING      │
                        ┌──────────────────┐       └──────────────────┘
        A               │   11MS DELAY     │
                        └──────────────────┘

                        ┌──────────────────┐       ┌──────────────────┐
                        │   LOGOUT         │       │  INDICATE      *  │   B
                        │   1. HARDCORE    │       │  ATTENTIVE        │
                        │   2. MICRO PRGM  │       │  CE AVAILABLE     │
                        └──────────────────┘       │                   │
    MACHINE CHECK INTERRUPT                         │  DELAY UNTIL      │
                                                    │  LOGOUT           │
                                                    │  COMPLETE         │
    ┌──────────────────┐                            └──────────────────┘
    │  LOGOUT VIA       │
    │  PROGRAM          │                           ┌──────────────────┐
    └──────────────────┘                            │  ANALYSIS OF   *  │
                                                    │  LOGOUT RECORD    │
                                                    │  MALFUNCTION      │
                                                    │  DETERMINE ACTION │
    ┌──────────────────┐                            └──────────────────┘
    │  WAIT UPON     *  │
    │  DETERMINING      │
    │  ATTENTIVE CE     │
    │  AVAILABLE        │
    └──────────────────┘

                    C

D
                                ACTION
    ┌──────────────────┐
    │  RESPONSE         │◄──────────────────────────
    └──────────────────┘
```

*PROGRAM FUNCTIONS

●Figure 8-6.  Monitoring of Element Malfunction

8-12

that someone had been listening to its element check, it could elect to start an analysis of its own logout data. The success of this would depend upon the nature of the condition.

D.  The malfunctioning CE will now respond to the course of action taken by the attentive CE.

## System Facilities

Certain system facilities are provided to enable system monitoring.

a.  Inter-Element Signal Lines
b.  Logout
c.  External Interrupt
d.  Diagnose Accessible Register (DAR)
e.  Diagnose Accessible Register Mask (DARM)

## Inter-Element Signal Lines

These lines exist between system elements and the CE's. They are used to indicate to CE's that an exception condition (i.e., temperature, tolerance check, power shutdown, CCR parity check, logic check etc.) has occurred in an element. These external signals will cause a single external interruption in each of the receiving CE's that is not masked against the condition. If the originating element is a CE, the signal will bring all receiving CE's not in the zero state with Test switch ON into State Three, provided these CE's are configured to accept a SCON instruction from the originating CE.

Upon receipt of such a signal, the receiving CE will take appropriate actions to determine the operational status of the originating element and  (1) attempt to alleviate the condition which generated the external signal, or  (2) remove the element from the operational system.

The external signals that can be expected are divided into three general categories.

1.  Element Check (ELC); caused by an element failure (power or logic)

2.  Out of Tolerance Check (OTC); caused by element temperature approaching marginal condition.

3.  On Battery Signal (OBS); caused by an element switching from Main Line Power to batteries.

Figure 8-7 summarizes the conditions which result in an external interruption.

## Logout

A logout signal to a CE or an IOCE will cause an orderly storing of that element's control conditions and critical registers into a Preferential Storage Area (PSA). The address of the specific

| Element | Generating Condition | External Signal | Originating Element Status After Signal |
|---------|---------------------|-----------------|----------------------------------------|
| CE | CCR Parity<br>Logic Check<br>OTC<br>OBS<br><br>Power Check<br>Storage Check | ELC<br>ELC<br>OTC<br>OBS<br><br>ELC<br>ELC | Operational<br>Operational<br>Operational<br>Operational<br>(6.5 sec)<br>Down<br>Check Stop* |
| SE | Logout Stop<br>CCR Parity<br>OTC<br>OBS<br><br>Power Check<br>Storage Check<br>Address Check<br>Data Check | ELC<br>ELC<br>ELC<br>ELC<br><br>ELC<br>ELC<br>ELC<br>ELC | Stopped<br>Operational<br>Operational<br>Operational<br>(5.5 sec)<br>Down<br>Operational<br>Operational<br>Operational |
| DE | Logout Stop<br>CCR Parity<br>OTC<br>OBS<br><br>Power Check<br>Address Check (CE access)<br>Data Check (CE access)<br>Address Check (DG access)<br><br>Data Check (DG access)<br><br>DGDR Check<br><br>DGAR Check | ELC<br>ELC<br>ELC<br>ELC<br><br>ELC<br>ELC<br>ELC<br>ELC<br><br>ELC<br><br>ELC<br><br>ELC | Stopped<br>Operational<br>Operational<br>Operational<br>(5.5 sec)<br>Down<br>Operational<br>Operational<br>Operational/<br>Stopped ***<br>Operational/<br>Stopped ***<br>Operational/<br>Stopped ***<br>Operational/<br>Stopped *** |
| IOCE | CCR Parity<br>Common Logic Check<br>Storage Check<br>OTC<br>OBS<br><br>Power Check | OBS/Pulse<br>ELC<br>ELC<br>OTC<br>OBS/level<br><br>ELC | Operational<br>Check Stop**<br>Check Stop**<br>Operational<br>Operational<br>(6.5 sec)<br>Down |
| PAM,TCU,RCU SCU | CCR Parity<br>Power Check<br>Check Stop (PAM)<br>OTC (RCU, SCU) | ELC<br>ELC<br>ELC<br>ELC | Operational<br>Down<br>Down<br>Operational |

OTC - Out of Tolerance (Temperature)
OBS - On Battery Signal

\*   - This is the status of the element if the generating condition occurred during logout. If it occurred during processing, the CE initiates its own logout.

\*\*  - This is the status of the element if the generating condition occurred during logout. If it occurred during processing, the IOCE issues a machine check interruption request to its associated CE and waits for a response.

\*\*\* - Depends on Status of Inhibit Display Element Stop bit.

●Figure 8-7.  External Interruption (Non-Programmed) Status Table
8-14

PSA is pointed to by the PSBAR (Preferential Storage Base Address Register). Successful completion of the hardware logout will automatically activate a "machine check" interruption in the CE or an I/O interruption by the IOCE. The processing of the interruption may include the "stored program" saving of additional registers (for the CE) to be placed in the PSA for later analysis, or it may result in a wait.

Logout of SEs and DEs is under program control of a CE, and the data is automatically placed in an SE as specified by the CE performing the logout.

Detailed malfunction information is available for TCU's, PAM's, SCU's, DAU's, and RCU's via the normal I/O SENSE commands.

External Interruption

This facility allows the CE's to continually monitor system conditions of selected elements while simultaneously performing the normal processing functions.

The external interruption scheme of the 9020D and 9020E systems is provided to allow programmed signalling between various CE's and hardware signalling between the system elements and the CE's. Whenever an external interruption is accepted by a CE, a unique bit is set in that CE. The external interruptions are completely maskable by bit 7 of the current PSW, except as described in Figure 8-8. The interruptions are divided into two classes: normal and abnormal.

Normal Interruptions

Normal interruptions are illustrated by Figure 8-9 (a). These are program controlled and not related to System Check conditions. The CE Read and Write (Direct) or I/O Processor Write Direct indications are under control of the CCR described previously. The Interrupt and Timer bit positions in the PSW will be set regardless of the CCR. This type of interruption is described in detail in 9020D/E System Principles of Operation Manual. Normal interruptions do not require use of the DAR and, therefore, bit 31 of the PSW will not be set for normal interruptions.

Abnormal Interruptions

Abnormal interruptions are illustrated by Figure 8-9 (b). These are the hardware generated signals of current or impending failures. Each signal of this class, will cause the appropriate DAR bit to be set. This, in turn, will cause an external interruption if the CE is not set to mask external interruptions. The DAR bit (31) in the old PSW will be set at the time the interruption is taken.

The components of the external interruption system of each CE, with usage and control, are defined below.
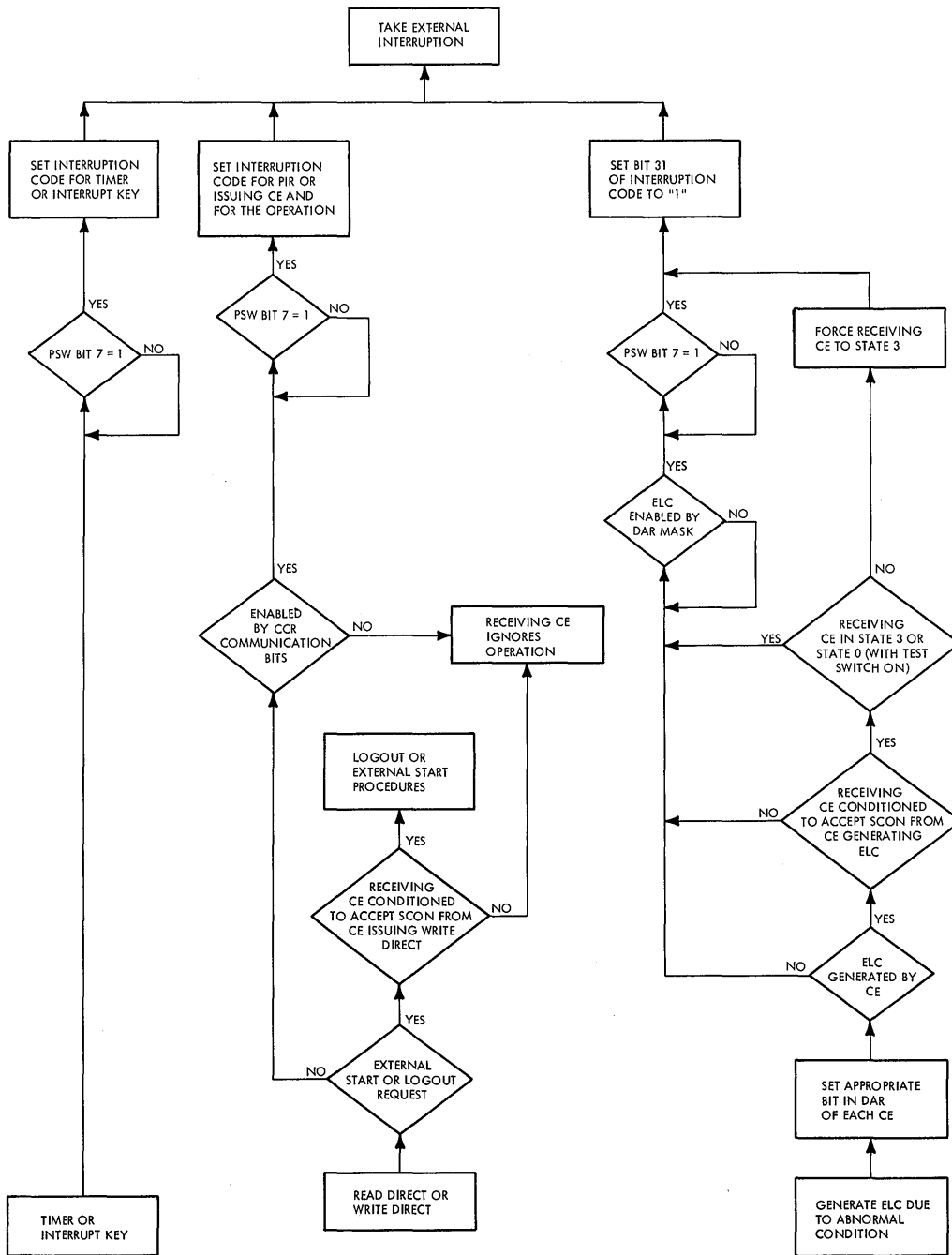
Figure 8-8. External Interrupt Handling

**9020D**

| IOCE 1 | | IOCE 2 | | IOCE 3 | | SE ELC | | | | | | | | | | SPARE | SPARE | PAM ELC | | | TCU ELC | | | SCU ELC | | | OTHER CE ELC/ CE OWN OTC | | | | CE OWN OBS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| a | b | a | b | a | b | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | | | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 4 | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | | | | | | | | | 15 | 16 | 17 | 18 | | 20 | 21 | | 23 | 24 | 25 | 26 | 27 | | | 30 | 31 |

**9020E**

| IOCE 1 | | IOCE 2 | | IOCE 3 | | SE ELC | | | | | DE ELC | | | | | SPARE | SPARE | RCU ELC | | SPARE | TCU ELC | | | SPARE | SPARE | SPARE | OTHER CE ELC/ CE OWN OTC | | | | CE OWN OBS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| a | b | a | b | a | b | 1 | 2 | 3 | 4 | 5 | 1 | 2 | 3 | 4 | 5 | | | 1 | 2 | | 1 | 2 | 3 | | | | 1 | 2 | 3 | 4 | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | | | | 10 | 11 | | | | 15 | 16 | 17 | 18 | 19 | 20 | 21 | | 23 | 24 | 25 | 26 | 27 | | | 30 | 31 |

(b) DIAGNOSE ACCESSIBLE (DAR)

| CE1 | | CE2 | | TIMER | INTPT | CE3 | | CE4 | | PIR | DAR |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RD DIR | WRT DIR | RD DIR | WRT DIR | | | RD DIR | WRT DIR | RD DIR | WRT DIR | | |
| 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |

(a) EXTERNAL INTERRUPTIONS (PSW 20-31)

| a | b | |
|---|---|---|
| 0 | 0 | NO CHECKS SIGNALS |
| 0 | 1 | OBS (NOTE: PULSE = CCR PARITY; LEVEL = OBS) |
| 1 | 0 | OTC |
| 1 | 1 | ELC |

•Figure 8-9. External Interruption Controls and Indicators

Masking

Bit 7 of the current PSW is used to mask external interruptions with one exception. If the CE is in State Two, One or Zero (with Test Switch Off) a CE ELC with the corresponding SCON bit on is sufficient to force an external interrupt and ignore Mask Bit 7. If this bit is a one, normal interruptions can proceed as usual. Abnormal interruptions may be subject to further masking by the DARM. If Zero, all interruptions are held pending until the bit is one or the CE is reset. There are multiple unique reasons for external interruptions. If, while masked, more than one request for a single reason is received, all but the last request will be lost (i.e., although multiple external interruption requests may be stacked, only one of a particular type will be saved).

PSW Interruption Code

Bits 20 through 31 of the PSW contain the identification of the external interruption source. The appropriate PSW bit is set at the time the external interruption is taken. Figure 8-9 (a) illustrates the source identification.

The eight bits associated with CE Read and Write Directs speci-
fying data communication are gated by the CCR.  That is, if the CE
is not configured to listen to the requesting CE, the request will
be ignored, and the bit in the Interruption Code will not be set.
If the CE is configured, the appropriate bit will be set in the
PSW and an external interruption will be taken if not masked by
PSW bit 7.

The interrupt and Timer bits are set any time the source signals
are received and interruption is not masked by bit 7.

The PIR bit (30) refers to a special three-position register
used to identify external interrupts from an IOCE Processor.  The
bits are gated with the IOCE bits in CCR, and the interrupt is taken
if not masked by PSW bit 7.

The DAR bit refers to the special register, shown in Figure
8-9(b), that contains a group of interruption identification con-
ditions too numerous to be included in the PSW.  The DAR bit is set
at the time the external interruption is requested.

Diagnose Accessible Register (DAR)

The DAR is so named because it is not normally an addressable reg-
ister; a Diagnose instruction is required for access.  This register
is used to store and identify hardware generated external interrup-
tion requests.  At the time of an external interruption, this reg-
ister will be read to supplement the PSW.  The conditions that set
this register are illustrated by Figure 8-7.  The register layout
is shown in Figure 8-9 (b).

When any element generates one of the specified interruption
requests, its identification bit is set in DAR.  This bit will cause
an external interruption if the mask conditions are met.  These con-
ditions are:

   a. Each position of the DAR has a corresponding mask position
      in the DAR Mask (DARM, to be described later).  If the DARM
      bit is 1, and bit 7 in the current PSW is set to 1, an ex-
      ternal interruption will occur at the completion of the
      current instruction with the DAR bit in the old PSW set to 1.
      (The following section will describe the special masking
      technique for IOCE bits in the DAR.)

   b. When a CE is in State Two, One, or Zero (with the Test
      Switch Off), CE ELC's cannot be masked off - that is, mask
      bits are ignored if the CE is configured to receive a SCON
      instruction from the originating CE.

The bits in the DAR will remain set until a read instruction (Diag-
nose) is issued to the register; then the entire register will be
reset.

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The character of each signal (pulse or level) which sets DAR is specified in Appendix E. If the signal which sets DAR is specified as a pulse, then reading of DAR will clear the affected bit and it will not be set again unless, of course, the condition occurs again. If the signal which sets DAR is a level, then reading of DAR will clear the bit momentarily, but it will be immediately set again. This forced setting of DAR will continue until the condition causing the signal is cleared. An examination of these level signals, however, will show that there should be no ambiguity in interpretation, since a level will indicate either a non-determinable time for the condition; e.g., OTC, power off, etc., or will indicate the condition causing the signal has also forced the affected unit to cease operation and require assistance. This method of signaling, in fact, will prove valuable in determining whether an element can perform some degree of self-diagnosis or must be assisted. As an example, assume that a CE has detected some error and generates a check signal. This is sent to all other CE's as an ELC and will set the appropriate DAR bit. This signal is a pulse; when read by the receiving CE, the receiving DAR bit will be cleared. The CE shich generated the ELC will proceed to logout to its PSA. Suppose however, that the CE is unable to perform this logout. This could occur for several reasons, but usually because of double errors (See Appendix E.) The CE would generate a second ELC and stop. This signal, however, is a level. A receiving CE, if it read its DAR twice in succession, would find the DAR bit still set. This static ELC would remain until the CE which generated it was restarted by some external means.

When DAR is read via Diagnose, the entire register is obtained without regard for any mask which may be used to control interruptions. No interruptions will set DAR during the read operation.

Diagnose Accessible Register Mask (DARM)

The DARM is program addressable (write) by a special Diagnose instruction. It permits program control over the conditions from the other elements that will be allowed to cause an external interruption in this particular CE. The CCR limits normal data flow between the various system elements while the DARM independently limits exception data flow between the system elements.

DARM contains a position for each position of DAR, except as noted in the next paragraph. If the DARM position is set to one, a corresponding interruption request through DAR will, if not further masked by PSW bit 7, set the DAR bit in the PSW and request an external interruption. If the DARM is zero, corresponding positions of DAR will not be allowed to propagate to the DAR bit in the PSW. Note previous exceptions on CE ELC's.

There are only two bits allotted for each IOCE, and they are not sufficient to indicate the necessary conditions. Consequently, these bits are encoded (Figure 8-9), and cannot be considered to be

distinct indications. DARM will mask both bits for each IOCE with a single mask bit. Specifically, the masking arrangement is as follows:

| DAR Bits | DARM Mask Bit |
|----------|---------------|
| 0,1 | 0 |
| 2,3 | 2 |
| 4,5 | 4 |

DARM bits 1, 3, and 5 will be considered spare bits.

## Special Element and System Condition Signals

The conditions which generated external interruptions were itemized in the previous section. This section discusses all the signals of this nature from the elements and the method of handling them independent of whether an external interruption is generated. Figure 8-10 summarizes the handling procedure.

## Power Supply

The power supply output malfunction of any major element will cause an ELC condition to be generated for that element at the Computing Elements.

## Out of Tolerance (OTC)

Sensing is provided for out of tolerance temperature conditions by all major system elements. The following indications have been defined for each element of the system for OTC checks.

CE- An OTC condition in a CE will cause that CE to take an external interruption. This condition will cause a unique identification bit to be set in the DAR of the CE to allow identification of the cause.

It is expected that each CE can handle its own OTC checks since they do not indicate an error environment but instead warn of an environment that could soon become erroneous. If the CE cannot finish its expected actions before a power shutdown, the latter condition (Power Supply above) will cause an ELC signal to the remaining CE's indicating trouble.

SE- An OTC condition in an SE will cause that element to generate an ELC. This ELC will be sent to all CE's. Those that are not masked for that condition will take an external interruption. This condition will set a unique identification bit in DAR. The functional capability of the SE will not be impaired by the generation of this ELC. An SE logout will be necessary to further isolate the ELC originating conditions.

DE- An OTC condition in a DE will cause that element to generate an ELC. This ELC will be sent to all CE's. Those that are not masked for that condition will take an external interruption. This

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| Element Condition | OTC | Power OFF | CCR Parity | Logic Check | OBS |
|---|---|---|---|---|---|
| CE | EXT to itself only | EXT | EXT | EXT | EXT to itself only |
| IOCE | EXT | EXT | EXT Pulse on OBS line | EXT Common Equip PRGRM Sel. Chnl | EXT |
| SE | EXT | EXT | EXT | EXT (also Sto Chk, Addr Chk or Data Chk to using element) | EXT |
| DE | EXT | EXT | EXT | EXT (also Addr chk or Data Chk to using element if a CE) | EXT |
| TCU | PRGRM | EXT | EXT | PRGRM | NONE |
| PAM | PRGRM | EXT | EXT | PRGRM EXT (check stop) | NONE |
| RCU | EXT | EXT | EXT | PRGRM | NONE |
| SCU | EXT | EXT | EXT | PRGRM | NONE |

NOTE:  EXT = External interruption to all listening CE's
       PRGRM = Program interruption handled by the subsystem
              monitor in normal  programming fashion.

•Figure 8-10.  Summary of Procedure for Handling External Interruption
              Signals.

condition will set a unique identification bit in DAR.  The function-
al capability of the DE will not be impaired by the generation of
this ELC.  A DE logout will be necessary to further isolate the ELC
originating conditions.

IOCE-  An OTC condition in an IOCE will cause that element to gen-
erate an OTC.  This OTC will be sent to all CE's.  Those that are
not masked for that condition will take an external interruption.
This condition will set a unique identification code in DAR.  The
functional capability of the IOCE will not be impaired by the gen-
eration of this OTC.

TCU- An OTC condition in a TCU will cause that element to generate an "Attention" on its IOCE-TCU interface as part of the status byte either at the end of an operation or when an attempt is made to select the TCU. The Attention signal is only used for OTC indications by this unit. This interruption condition is handled in the same manner as any other interruption condition.

The generation of the OTC condition will not affect the operational capabilities of the TCU.

PAM- An OTC condition in a PAM will cause that element to generate "Attention" status from the Test and Monitor Adapter. This interruption condition is handled in the same manner as any other interruption condition.

The generation of the OTC condition will not affect any of the operational capabilities of the PAM. A sense command through the IOCE will be necessary to detect that an OTC condition does exist. The sense data will include among other things an OTC bit and CCR parity indication.

RCU- An OTC condition in an RCU will cause generation of a pulsed ELC. The ELC will be sent to all CE's. Those that are not masked for that condition will take an external interruption.

This condition will set a unique identification bit in DAR. The functional capability of the RCU will not be impaired by the generation of this ELC.

A sense command through the IOCE will be necessary to detect that an OTC condition does exist. The sense data will include among other things an OTC bit and CCR parity bit.

SCU- An OTC condition in an SCU will cause generation of a pulsed ELC. The ELC will be sent to all CE's. Those that are not masked for that condition will take an external interruption.

This condition will set a unique identification bit in DAR. The functional capability of the SCU will not be impaired by the generation of this ELC.

A sense command through the IOCE may be used to determine that an OTC condition does exist. The sense data includes an OTC bit position.

CCR Parity

Every major element has a CCR register. Parity is continually monitored on this register by the element; whenever incorrect parity is detected, ELC is generated. However, if the CCR is in the process of being loaded, generation of ELC is suppressed since other means are used to inform EXC* of the condition. This ELC will be

*Executive Control Program

transmitted to all CE's.  Those that are not masked for that con-
dition will take an external interruption.  The ELC condition will
cause an ELC identification bit or code to be set in DAR.

Should an element's CCR become set to allow no CE to issue a
SCON to the element, this element would be lost to automatic system
control.  This condition can occur only through a malfunction or
through manual action.  Equipment is provided to detect this con-
dition.

When this condition is detected, the CCR SCON field gating is
bypassed, and the element will accept a SCON from any CE, provided
that the element is not in State Zero.  If an element is in State
Zero, and its SCON field is set all zero's, it is presumed to be a
desired condition, and all SCON's are rejected.

A special indicator is used for CCR parity from the IOCE.  This
is a pulse on the OBS indication to provide easy identification.
The normal OBS indication is a level.

The generation of the ELC will not affect the operational
capability of the element.  To further analyze the condition it
is necessary to logout or sense the element.

Logic Check

Every system element has built-in internal checking procedures,
described in the following section.  This section does not include
the CCR which has been described previously.

CE-  An internal logic check will cause the CE to signal an ELC to
all other CE's.  The CE which has the logic check may proceed with
a logout, depending upon whether its machine check interruption is
masked or not.

IOCE - An internal common logic check (or multiplex channel check)
will cause the IOCE to Check Stop and signal ELC to all CE's, the
reception of which was described previously.  The IOCE will request
a special machine check interruption from the configured controlling
CE which will allow it to logout. The IOCE will suspend IOCE Pro-
cessor operations until the controlling CE re-initiates them.

A malfunction in a selector channel hardware will cause that
channel to Stop.  The IOCE will request an I/O interruption of its
configured CE.  When the interruption is permitted, the selector
channel will be logged out and the interruption performed.

SE-  An internal logic check of an SE will only be signalled when
another element is using it.  The signal will appear as a pulsed ELC
to all CE's, as either an Address Check or Data Check to a CE user,
or as a Storage Check to the IOCE user.

DE - An internal logic check of a DE may be signalled when either a
CE or display generator is using it.  If signalled while a CE
is using it, the signal will appear as a pulse ELC to all CE's, and

as either an Address or Data Check to the using element. If signal-
led because of a logic malfunction related to a display generator
access, the signal will appear as a level ELC to all CE's.

TCU- The TCU will attempt to signal the IOCE of any logic failures
and will expect remedial action through the IOCE using normal I/O
checking hardware (and software). Malfunctions affecting only an
individual Tape Drive or associated path will not affect the oper-
ation of the remainder of the TCU. Malfunctions originating from
the common logic of the TCU will affect the entire TCU system.

PAM- PAM will attempt to signal the IOCE of any malfunction and
remedial action is expected through the IOCE interface in much the
same fashion as the TCU. Some malfunctions in PAM common will stop
all PAM data service cycles, while malfunctions originating in the
PAM adapters will only affect the malfunctioning adapter.

RCU- The RCU will attempt to signal the IOCE of any logic failures
and will expect remedial action through the IOCE using normal check-
ing hardware (and software). Malfunctions affecting individual
Configuration Interfaces will not affect the remainder of the RCU.
Common Channel logic malfunctions will affect the entire RCU.

DAU- The DAU will attempt to signal the IOCE whenever a logic
failure occurs and expect remedial action through the IOCE using
normal I/O checking hardware (and software). Malfunctions orig-
inating within the DAU will affect operation of the entire DAU.
Those checks emanating from RKM equipment will not affect DAU
operation with other RKM units.

SCU - The SCU will attempt to signal the IOCE of any logic failures
and will expect remedial action through the IOCE using normal
checking hardware (and software). Malfunctions affecting only an
individual Disk Storage Unit will not affect the operation of the
SCU. Malfunctions within the SCU will affect the entire Direct Access
Storage Facility.

On Battery Signal (OBS)

Four of the major elements of the system (CE, IOCE, SE, and DE) have
battery backup in case of power failure. A means is provided to
signal when the batteries are being used. Switching from normal
operation to batteries will cause an On Battery Signal (OBS) to be
generated. A pushbutton is provided at each of these elements to
simulate the OBS condition for testing.

    This OBS will be treated in the following manner for the affect-
ed elements.

CE- Only the generating CE will receive its own OBS signal. This
signal will cause an external interruption. This condition will set
a unique identification bit in DAR. The operational status of the
CE will not be affected by the generation of the signal.

IOCE- The IOCE will transmit its OBS to the CE's as a level. The
CE's, if not masked for the condition, will take an external inter-
ruption. A unique OBS identification code will be set in DAR in

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the CE. The operational status of the IOCE will not be affected by the generation of this signal.

To enable rapid identification, the CCR parity indication is signalled as a pulse in the OBS line.

SE — The SE will transmit its OBS signal under the common heading of $\overline{ELC}$ to all CE's. These CE's, if not masked for the condition, will take an external interruption. This condition will set that SE's unique ELC bit in DAR in the CE. An SE logout is necessary to determine the cause of the ELC. The generation of the signal will not affect the operational capability of the SE.

DE — The DE will transmit its OBS signal under the common heading of $\overline{ELC}$ to all CE's. These CE's, if not masked for the condition, will take an external interruption. This condition will set that DE's unique ELC bit in DAR in the CE. A DE logout is necessary to determine the cause of the ELC. The generation of the signal will not affect the operational capability of the DE.

The OBS signal for all units is sent to the System/Configuration Console for display.

GENERAL

The System Console, IBM 7265-02 (Figure 9-1), is the central mon-
itoring and control position in the IBM 9020D System.  The console
is divided functionally into four parts:  Maintenance Controls,
Monitor Displays, Operator's Controls and Emergency Power Off.

     The console is addressable as an I/O device to display the
system mode of operation, generate audible alarms, and display
updated system element configurations.  The System Console contains
logic to electronically switch, a Printer Keyboard, and a Card
Read/Punch and Printer to the selected Multiplexor Channel.
Switching is under manual control of switches located on the
Operators Panel.  Operator controls which could disrupt the System
program or elements are interlocked on the control panel.

     All critical console functions are duplicated elsewhere in the
system.  Table 9-1 indicates where each of the critical console
indicators and controls are duplicated by other elements in the
system in the event that the System Console is not operable.

FUNCTIONAL OPERATION

This section describes the functional operation of the System Con-
sole's mode of communication with the IBM 9020D System.  Basically,
the communication may be divided as operations and controls requiring
operator intervention, program generated control and status, and
displays to enable the operator to monitor the system.  A console
data flow diagram is provided in Figure 9-2.

Operator Intervention

There are several important functional operations associated with
control of the active system that may be controlled from the System
Console.  These functions include Initial Program Loading, manual
entry of information to the active system, and assistance to the
Executive Control Program in accomplishing reconfiguration by manual
switching of I/O equipment at the console.

Initial Program Loading

All of the controls for Initial Program Load (IPL) are located on
Panel H*, Figure 9-3.  These controls include the CE Select Switch,
Main Storage Select Switch, Load Unit Select Switches, Load
Pushbutton and System Interlock.


* Panel letters for purpose of description only, will not appear as
  actual hardware.

Table 9-1. Duplication of Critical Console Indicators and Controls

| Indication or Control | CE | Indicator or Control Backup | |
| --- | --- | --- | --- |
| | | PAM 1052 | All Major Elements |
| Mode of Operation | | X Hard Copy | |
| System EPO** | | | |
| Status | | | X |
| Alarms (Faults) | | | X |
| Alarms (Audible) | | X Hard Copy | |
| Configuration | | X Hard Copy | |
| SD | X | | |
| IA | X | | |
| Set IC | X | | |
| Store | X | | |
| Display | X | | |
| Start | X | | |
| Stop | X | | |
| Control CE | X | | |
| Address Compare | X | | |
| Rate | X | | |
| IPL Controls | X | | |
| Interrupt | X | | |
| IBM 2821 Control Unit Printer-Card Read/Punch | | X | |
| IBM 1052-7 Printer Keyboard | | X | |
| Sense Switches | | X | |

**Always operable from System Console

The procedure for IPL from the System Console is as follows:

1. Select a CE using the CE Select Switch.

2. Select a Main Storage Element using the Main Storage Select Switch.

3. Select the address of the I/O device by using the Load Unit Select Switches.

4. Turn on the System Interlock.

5. Depress the Load Pushbutton.

An indicator contained in the Load Pushbutton will turn on when the IPL sequence is being performed and will remain on until the IPL is complete. If a fault should occur during the IPL sequence, the load light will remain on.
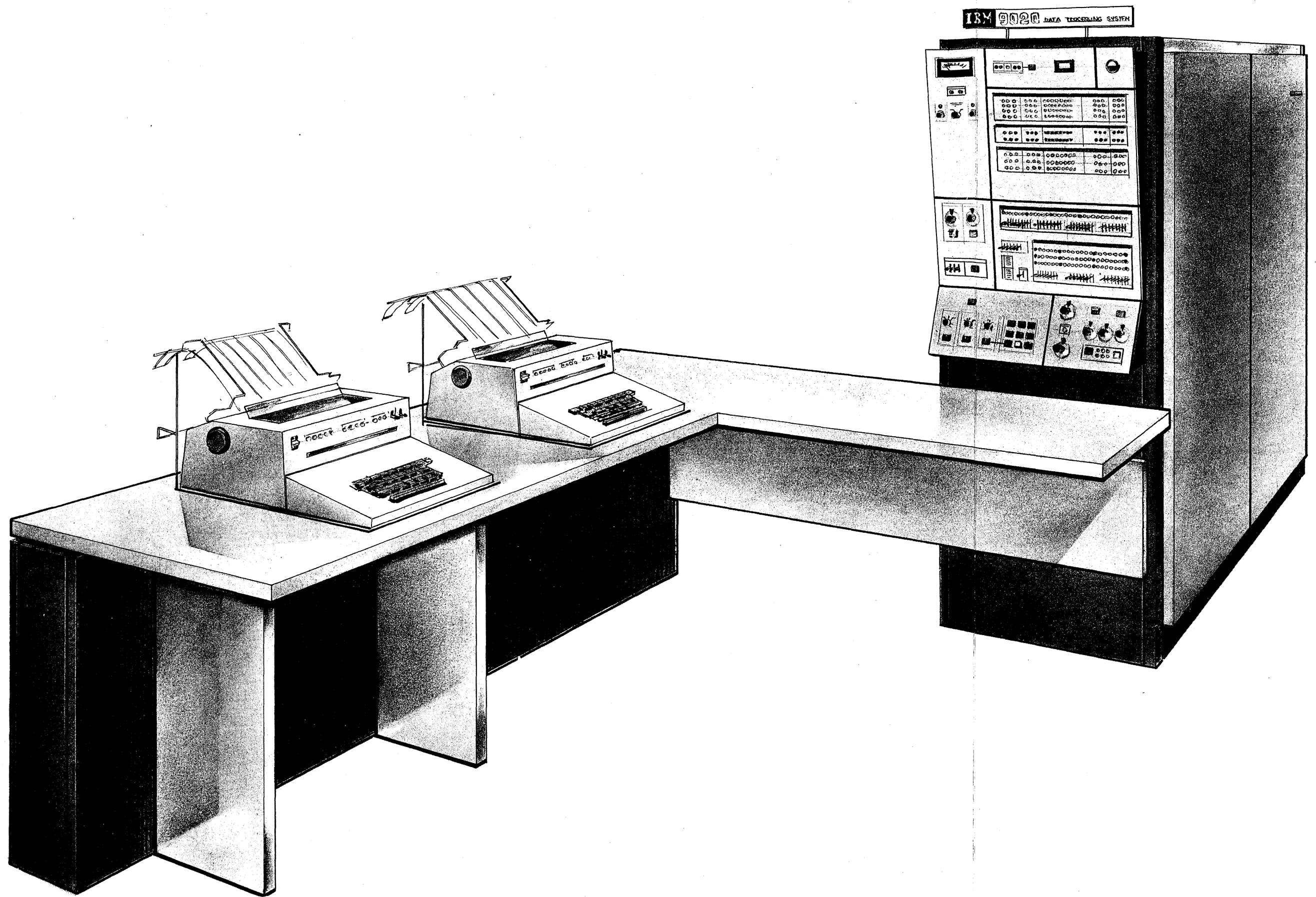
Figure 9-1.  System Console
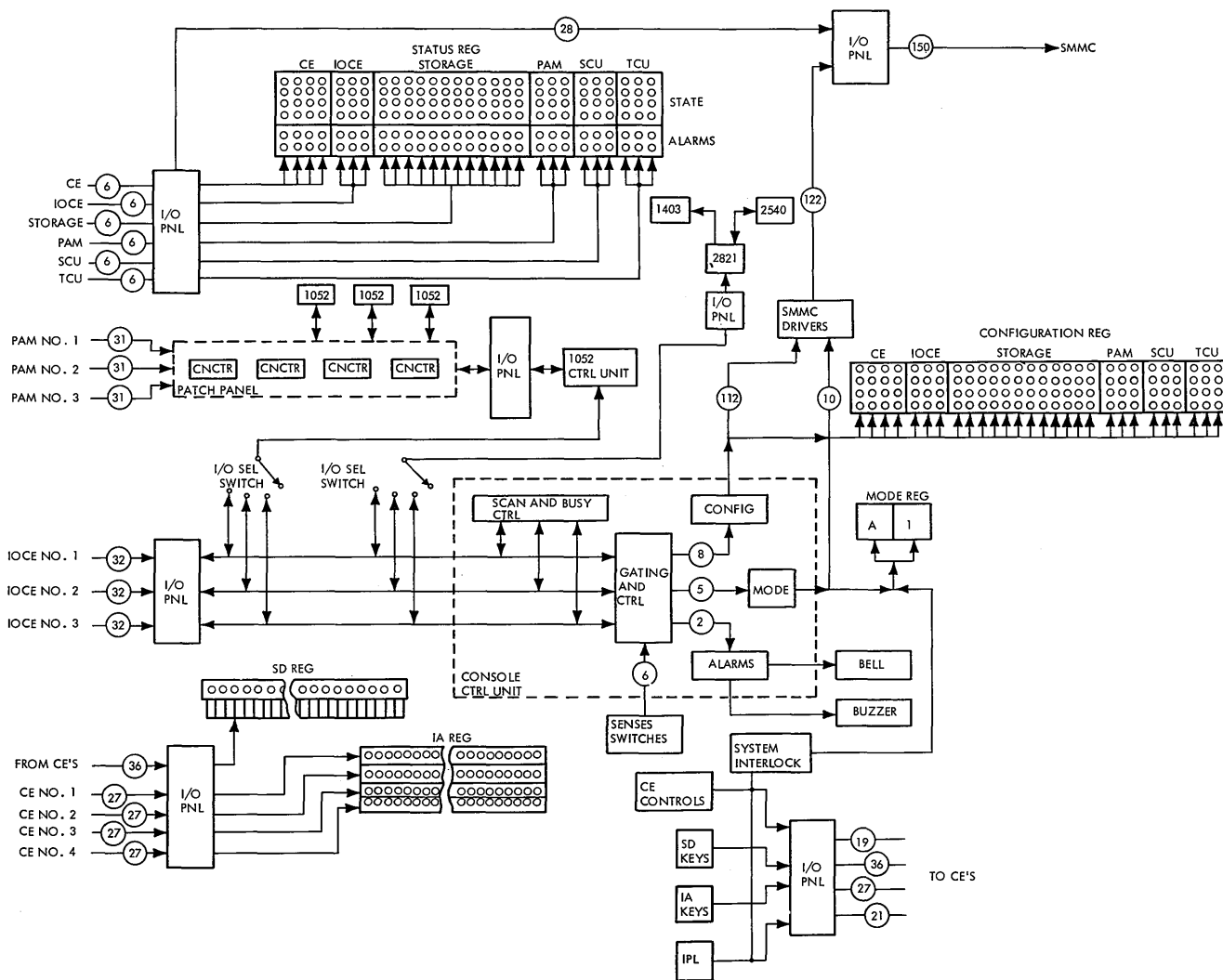
●Figure 9-2.  System Console Data Flow
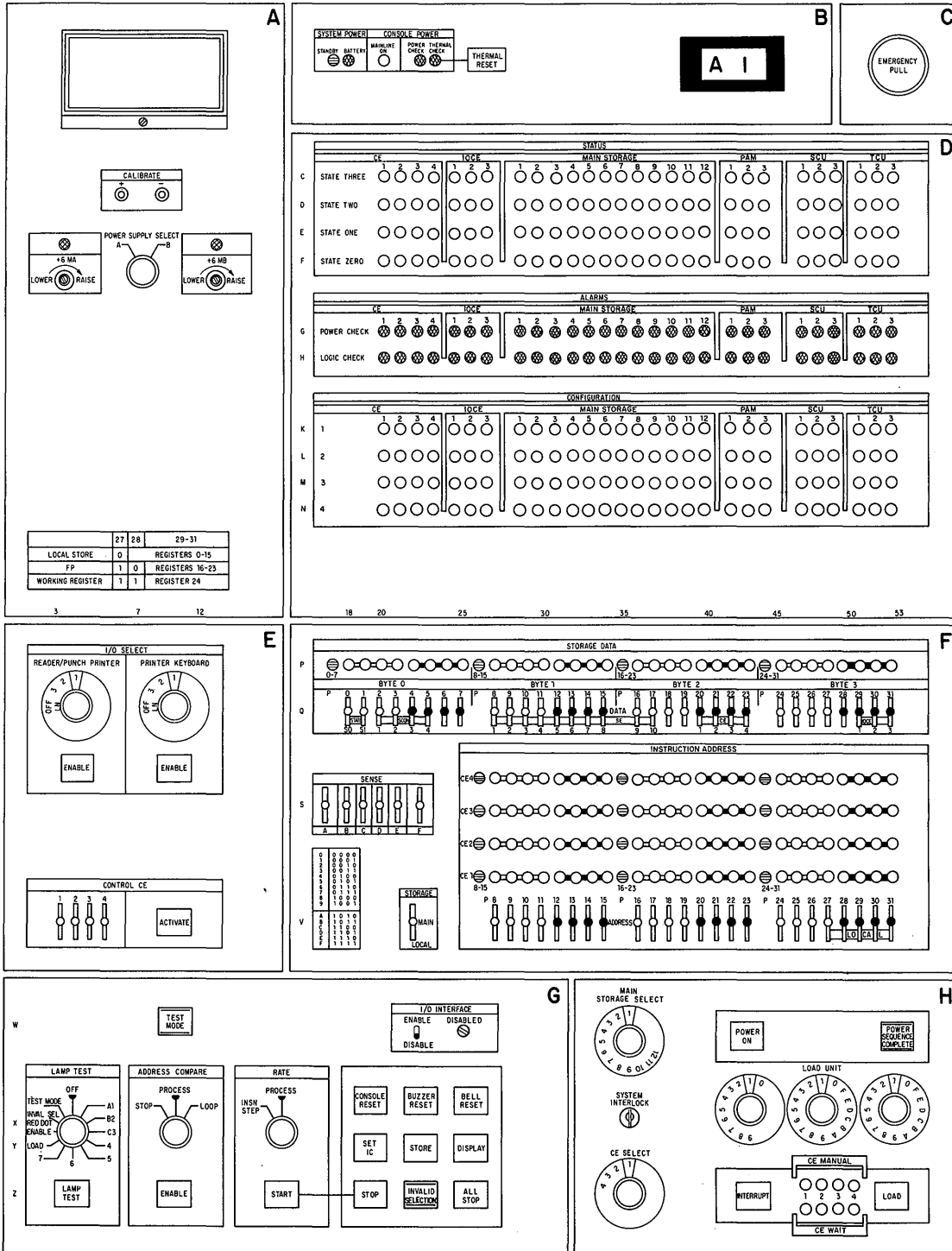
●Figure 9-3.  9020D System Console Operator's Panel

Manual Entry of Information or Display

There are several methods for entry of manual information to the
Active System; these include data entry using the IBM 1052-7
Printer Keyboard, Sense Switch Entry, Storage Modification of the
CE Configuration Registers, and modification of CE Instruction
Counters (IA).

Printer Keyboard.  Printer Keyboards (IBM 1052-7) are located at the
System Console for data entry.  One 1052 enters data through a con-
trol unit in the System Console.  The other 1052's enter data
through adapters in the Peripheral Adapter Module (PAM) IBM 7289-2.
For maximum flexibility, the System Console interconnected 1052 can
be manually switched to any of the three IOCE Interfaces.
(Reference I/O Switching Section)  In addition, through use of a
patch panel at the System Console, the 1052's may be manually
interchanged with each other.

Sense Switch Entry.  The console has six sense switches shown in
Panel F, Figure 9-3, which can be read by program means into storage
through one of three interconnected IOCE's.  Upon acceptance of
address (01) and a Read Sense Switch Command, the contents of all
the sense switches are sent back to the requesting IOCE.  If two or
more IOCE's address the console simultaneously, the tie will be
broken by appropriate circuits and the lowest (logically) numbered
IOCE will be given priority.  All others will receive Control Unit
Busy status.

The command byte has the following format:

Byte Bit Positions                        0   1   2   3   4   5   6   7

                                      P   0   0   0   0   0   0   1   0

                                          Sense switch tag ⌐

                                          Read operation ──────────┘

     The contents of the sense switches are sent back to the
requesting IOCE in the following format.

                                         Bit Positions

                           P   0   1   2   3   4   5   6   7

Data Byte                  P   0   0   1*  1   1   1   1   1
Sense Sw. Assignment          Not used   A   B   C   D   E   F
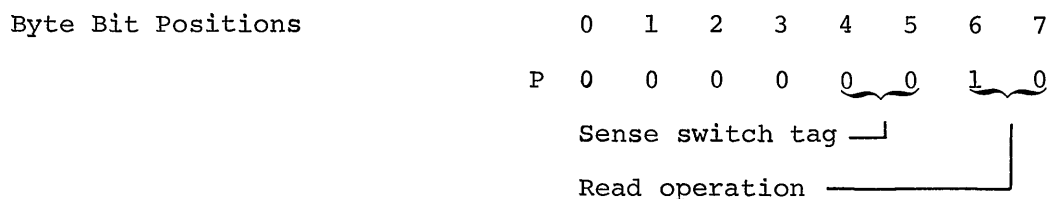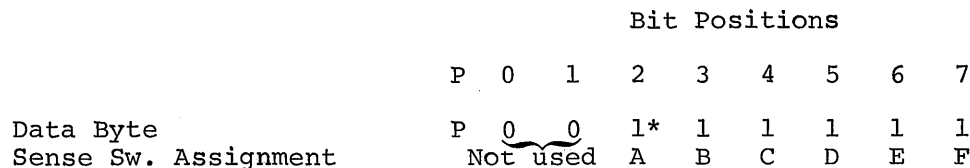
*A sense switch in the On position will cause a 1 to be inserted in
its assigned bit position.

Storage Modification or Display.  The contents of a selected storage
location may be modified through the use of the Storage Data Keys,

Address Keys, Storage Select Switch, and Store Pushbutton. The procedure for storage modification from the System Console is as follows (refer to Figure 9-3):

1. Select a CE using the CE Select switch (Panel H).

2. Enter data in Storage Data Keys (Panel F). Correct byte parity (odd) is automatically assigned.

3. Enter Storage Address in Address Keys (Panel F). Correct byte parity (odd) is automatically assigned.

4. Designate Main or Local Storage using Storage Select Switch (Panel F).

5. Turn on System Interlock Switch (Panel H).

6. Depress Stop Pushbutton (Panel G).

7. Depress Store Pushbutton (Panel G).

The contents of a selected location may be displayed in a similar manner. The procedure for display of storage from the System Console is as follows (refer to Figure 9-3).

1. Select a CE using the CE Select switch (Panel H).

2. Enter Storage Address in Address Keys (Panel F). Correct byte parity (odd) is automatically assigned.

3. Designate Main or Local Storage using Storage Select Switch (Panel F).

4. Turn on System Interlock Switch (Panel H).

5. Depress Stop Pushbutton (Panel G).

6. Depress Display Pushbutton (Panel G).

If an invalid storage address for the selected CE is placed in the address keys, the store or display attempted will not be performed. The invalid selection light will be turned on. The invalid selection condition will be reset on the next valid store or display attempt. An invalid selection can be caused by entering a storage address which refers to an SE which is either not operational (power off, malfunction, etc.) or not configured to the selected CE.

Modification of CE Configuration Register. The controls for the modification of the selected CE configuration register are shown in Figure 9-3. The procedure for modification of the CE configuration register from the System Console is as follows:

1. Set the desired configuration for the SCON bits in the Control CE Switches. An odd parity bit will automatically be assigned at the console (Panel E). The state bits of the selected CE are reset to 00.

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2.  Select the desired CE using the CE Select Switch
       (Panel H).

   3.  Turn on the System Interlock Switch (Panel H).

   4.  Depress Stop Pushbutton (Panel G).

   5.  Depress the Activate Pushbutton (Panel E). The State
       Bits of the selected CE are reset to 00.

Modification of a CE Instruction Counter (IC). The controls for
modification of a CE's Instruction Counter are shown on Panels F, G
and H, Figure 9-3. The controls required are the Instruction
Address Keys, the Set IC (Instruction Counter) Pushbutton, and the
CE Select rotary switch. The procedure is as follows:

   1.  Select a CE with the CE Select switch (Panel H).

   2.  Set the desired contents of the IC in the Instruction
       Address Keys (Panel F).

   3.  Turn on System Interlock Switch (Panel H).

   4.  Depress Stop Pushbutton (Panel G).

   5.  Depress the Set IC Pushbutton (Panel G). The address
       will appear in the selected CE's Instruction Address
       display indicators.

Display of Information from Local Storage

To assist the operator in setting up the address switches for
displaying information from Local Storage, a map of the LS is
provided on the System Console. The map, shown in Figure 9-4,
indicates that LS is divided into three sectors. The sector is
selected by the setting of the IA keys, position 27 and 28, which
identifies the appropriate section in Local Storage.

|  | 27 | 28 | 29-31 |
|---|---|---|---|
| Local Store | 0 | | Registers 0-15 |
| FP | 1 | 0 | Registers 16-23 |
| Working Register | 1 | 1 | Register 24 |

Figure 9-4. Map of Local Storage, System Console

   When bit 27 is set to zero, General Registers from 0 to 15, are
addressed through IA keys 28 through 31 by the binary settings 0000
through 1111 respectively. The Floating Point Registers are address-
ed through IA Keys 29-31 when the bits 27 and 28 equal 10. The
appropriate pushbutton is then used to produce the intended result.

The working register may be addressed any time the bits 27 and 28 =
11.  The entire LS block of registers may be displayed.  Only FP
and General Registers may be addressed and used by the programmer.


I/O Switching

Two rotary selection switches and two selection Enable pushbuttons
are positioned on Panel E, Figure 9-3.  They provide the operator
with the ability to interconnect the selected I/O devices to any one
of the three available IOCE interfaces logically designated 1, 2,
and 3.  The switching is accomplished by the System Console logic.
The interconnected I/O devices are independently program addressable.
The unit addresses are as follows:

        Printer Keyboard (IBM 1052-7)    02

        Card Reader (IBM 2540)           03

        Card Punch (IBM 2540)            04

        Printer (IBM 1403-2)             05

     If the I/O devices are addressed by an IOCE not connected
through the I/O Select switch, a Select In signal (Condition Code 3,
device not operational) is returned.


Program Generated Control and Status

The operational characteristics of the System Console, which
primarily involve monitoring of the program generated control and
status, are described in the following sections.  Program generated
information includes Mode of Operation, System Configuration
Registers, and Audible Alarms.  The console has a control unit which
recognized address 01 and which allows the appropriate programmed
activity to occur.  Operator intervention as a result of the data
interpretation is accomplished as described in the 'Operator
Intervention' Section.


Mode of Operation Indicators

The Mode of Operation Indicators are an output device for the
Executive Control Program and display an alphanumeric code to define
system operating capability as defined by the program.  The
indicators are updated by program means after the console has
accepted its address (01), which should be followed by a command
byte and data byte transfer.  When changing the Mode of Operation
Indicator display, it is not necessary to reset the display.  If two
or more IOCE's address the console simultaneously, the tie will be
broken by appropriate circuits and the lowest (logically) numbered
IOCE will be given priority.  The others shall set Condition Code 2.

Data is transmitted in multiplexed mode.  The command byte has the following format:

Byte Bit Positions                     0   1   2   3   4   5   6   7

                              P    0   0   0   0   0   1   0   1

Mode of Operation
Indicator Tag ──────────────────────────────────────────┘         │
Write ──────────────────────────────────────────────────────────────┘
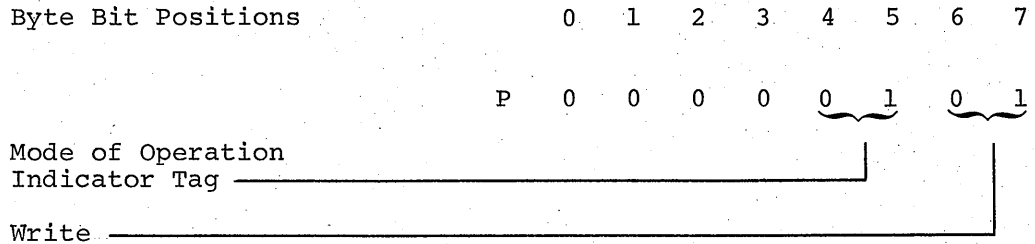
    The data byte for the alpha and numeric characters is as follows:

Byte Bit Positions

P     0    1    2    3              4       5    6    7

Not  ──┘        0    0 - Reset     Not     0    0    0 - Reset
Used            0    1 - A         Used    0    0    1 - 1
                1    0 - B                 0    1    0 - 2
                1    1 - C                 0    1    1 - 3
                                          1    0    0 - 4
                                          1    0    1 - 5
                                          1    1    0 - 6
                                          1    1    1 - 7
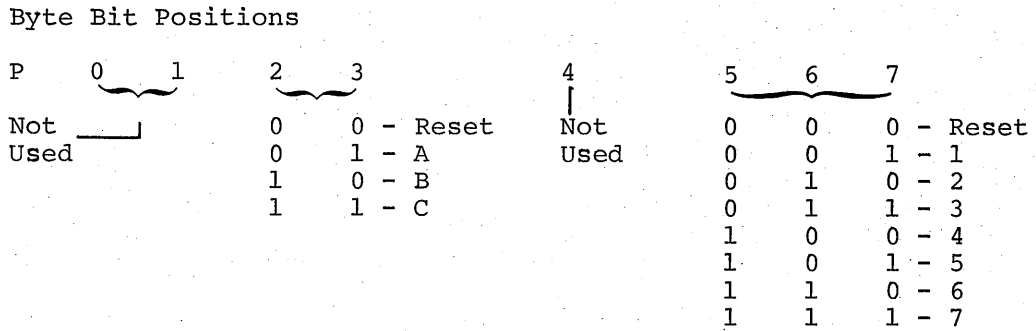
The Reset code results in no display.  Mode of Operation Information is also sent to the SMMC via the SC/SMMC Interface.

Configuration Indicator Registers

Four registers of indicators shown on the console in Panel D, Figure 9-3, are program addressable and can be used to display the combination of elements that are configured into the system or sub-system.  The Configuration Register indicators may be updated after the console has accepted address (01) followed by a command byte (specifying the register(s)) and four data bytes per register.

    The command byte has the following format:

                                        Bit Positions

                            P   0   1   2   3   4   5   6   7

        Command Byte        P   0   1   1   1   1   0   0   1
        Config. Reg.            4   3   2   1
        Assignment
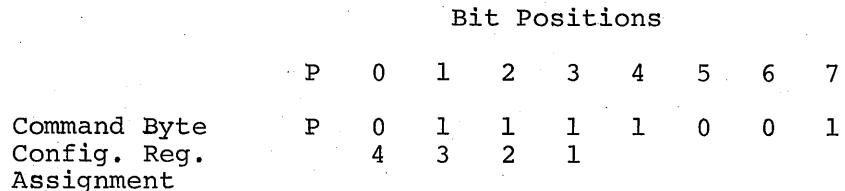
The order of writing the Configuration Registers is 1, 2, 3, and
4. Any register not selected by a 1 in its bit position will cause
that register to be skipped. Four bytes of data are transferred by
the channel for each register selected. The order of byte transfer
is 1, 2, 3, and 4. The structure of the four data bytes, related to
the Configuration Register bit positions, is as follows:

| PAM | | TCU | | | | | SE | | | | | | | | | | | | CE | | | | SCU | | | | | IOCE | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 1 | 2 | 3 | * | * | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 | 4 | 1 | 2 | 3 | * | * | 1 | 2 | 3 |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

|      Byte 1      |      Byte 2      |      Byte 3      |      Byte 4      |

*Indicates unused bits.

NOTE: The format shown is for a maximum system but must be followed
for all systems. Bit positions for elements or units not contained
in a particular system will be transferred and displayed by the
System Console circuitry.

    If two or more IOCE's address the console simultaneously, the
tie will be broken by appropriate circuits and the lowest (logically)
numbered IOCE will be given priority. All other IOCE's shall set
Condition Code 2. Configuration Register Information is also sent
to the SMMC via the SC/SMMC Interface.

Audible Alarms

Two audible alarms, a bell and buzzer, are provided in the System
Console for operator attention. Operation of both alarms is
initiated by program control. The audible alarms are turned on after
the console accepts address (01) and a command byte transfer. If
two or more IOCE's address the console simultaneously, the tie will
be broken by appropriate circuits and the IOCE with the lowest
(logical) number will be given priority. All others will set
Condition Code 2. The command byte has the following binary
configuration.

Bit Position        P    0    1    2    3    4    5    6    7

                    P    0    0    0    0    0    1    1    1

Bell Tag _____|

Control _____|

Bit Position        P    0    1    2    3    4    5    6    7

                    P    0    0    0    0    1    0    1    1

Buzzer Tag _____|

Control _____|

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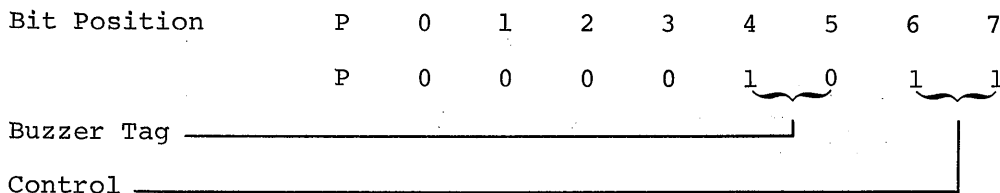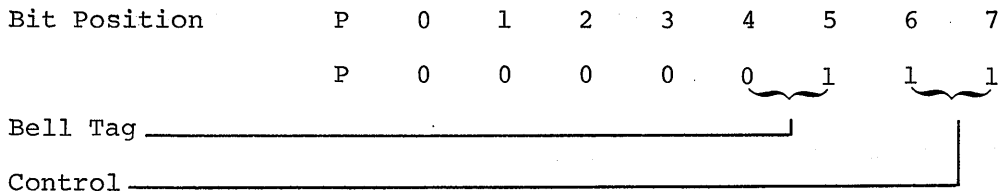
If the buzzer or bell is sounding, and an IOCE addresses the console, no busy indication shall be returned to the IOCE.

The audible alarms may be reset by depression of the applicable pushbutton on Panel G, Figure 9-3.

CONSOLE INDICATORS, KEYS, AND SWITCHES

This section describes the indicators, keys and switches provided on the Operator's Panel of the System Console to monitor and control the IBM 9020D System. In addition to the functional components, the controls and switches for two console test operations are positioned on the panel. The first, Lamp Test controls, may be used by the operator to check the panel for indicator faults. Components should be replaced by qualified maintenance personnel. The second, Marginal Check controls, are to be used only by maintenance personnel during periods of scheduled maintenance. Power control, Marginal Check, and Power indicators will be described in the 'Power Control, Marginal Checking, and Indicators' Section. Table 9-2 lists these controls and indicators and their implementation.

Console Indicators

Mode of Operation Indicators

The System's Mode of Operation is displayed on the console by two visual inline readouts. One readout indicates alpha characters (A or B or C). The other indicates numeric values (1 through 7). The indicators are set by the program when the control unit recognizes the specified Write Mode command. Mode of operation indicators are also sent to the SMMC.

The Mode of Operation display will be backlighted with a red light when the System Interlock Switch is in the 'On' position.

Unit Status Indicators

Four indicators for each Computing Element, Storage Element, Peripheral Adapter Module, Input/Output Control Element, Storage Control Unit, and Tape Control Unit are provided on the System Console (Panel D, Figure 9-3) to indicate Unit Status.

Each element or unit decodes its own Status and turns on one of four indicators designated State Three, State Two, State One and State Zero. When an element or unit has power off, no indicator for it is turned on.

State Three - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Three.

Table 9-2. Controls and Indicators

| Name | Implementation |
|---|---|
| Mode of Operation | Alpha-Numeric Indicator |
| Unit Status | Indicators (112) |
| Unit Alarms | Indicators (56) |
| Configuration Registers | Indicators (112) |
| Storage Data (SD) | Indicators (36) |
| Instruction Address (IA) | Indicators (108) |
| Manual Status (CE) | Indicators (4) |
| Wait Status (CE) | Indicators (4) |
| Invalid Selection | Indicator |
| Test Mode | Indicator |
| Reader/Punch-Printer Select | Rotary Switch |
| Reader/Punch-Printer Enable | Pushbutton Switch-Indicator |
| Printer Keyboard Select | Rotary Switch |
| Printer Keyboard Enable | Pushbutton Switch-Indicator |
| Control CE | Lever Switches (4) |
| Control CE Activate | Pushbutton Switch |
| Storage Data | Lever Switches (32) |
| Sense | Lever Switches (6) |
| Instruction Address | Lever Switches (24) |
| Storage Select | Lever Switch |
| Address Compare | Rotary Switch |
| Address Compare Enable | Pushbutton Switch |
| Rate | Rotary Switch |
| Start | Pushbutton Switch |
| Console Reset | Pushbutton Switch |
| Bell Reset | Pushbutton Switch |
| Buzzer Reset | Pushbutton Switch |
| Set IC | Pushbutton Switch |
| Store | Pushbutton Switch |
| Display | Pushbutton Switch |
| Stop | Pushbutton Switch |
| All Stop | Pushbutton Switch |
| Main Storage Select | Rotary Switch |
| Computing Element Select | Rotary Switch |
| Load Unit | Rotary Switches (3) |
| Load | Pushbutton Switch Indicator |
| Interrupt | Pushbutton Switch |
| System Interlock | Key Operated Switch |
| Lamp Test Select | Rotary Switch |
| Lamp Test | Pushbutton Switch |
| Interface Enable/Disable | Toggle Switch |
| I/O Interface Disabled | Indicator |

State Two - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Two.

State One - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State One.

State Zero - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Zero.

Unit Alarms

There are two alarm indicators on the System Console for each CE, IOCE, SE, PAM, SCU, and Tape Control Unit.

Power Check - This indication is turned on by the respective element or unit whenever one or more of the following conditions exist in the element:

1.  Catastrophic Power Supply Failure

2.  Over Temperature

3.  Normal Power Off

The indicator shall be turned on by +24 v DC from the failing element. The Power Check light shall function regardless of the System Console power status except during Emergency Power Off. The Power check lines are also sent to the SMMC via the SC/SMMC Interface.

NOTE: Definition of the above conditions is found in the IBM 9020 System Power Chapter.

Logic Check - This indicator is turned on by the respective component when the element or unit detects its own logic check condition (defined in individual element specification). In addition, each CE will turn on its console logic check indicator when even parity is transferred from the System Console to the selected computing element.

Registers

Configuration Indicator Registers - Four indicator registers, designated 1, 2, 3, and 4, are provided to display system configuration for each CE, IOCE, SE, PAM, SCU, and TCU. The indicators are turned on under program control (Configuration Indicator Registers Section) and shall remain on until updated by the program or reset by depressing the Console Reset Pushbutton. The configuration indicators are also sent to the SMMC via the SC/SMMC Interface.

Storage Data (SD) - One SD word composed of 36 indicators shall be provided to display the contents of the selected storage location as specified in the Storage Modification or Display Section. Parity of the indicators shall not be checked at the console.

Instruction Address (IA) - The IA for each Computing Element shall be provided on the console to continually display the contents of the respective CE Instruction Counter. Each register contains 27 indicators to indicate IA contents. Parity of the indicators shall not be checked at the console.

Manual Status

The Manual Status Indicator, which exists on each of the Computing Elements, shall be duplicated on the console. This light shall be turned on when the element is in the Stopped state.

Wait Status

The Wait Status indicator, which exists on each of the Computing Elements, shall be duplicated on the console. This light shall be turned on when the Computing Element's Wait bit in the PSW is set to one.

Invalid Selection Indicator

This indicator shall be turned on by the selected CE whenever an invalid or illegal storage address is specified by the operator during a manual intervention.

Test Mode Indicator

This indicator shall be turned on by the Test-Operate switch located on the console maintenance and test panel to inform the operator that the test panel controls are operable. The indicator is turned off when the Test-Operate switch is positioned to Operate.

Disabled Indicator - The Disabled indicator (green) is turned on when all interfaces from the SC to the IOCEs are logically disconnected (initiated by placing the I/O Interface Enable/Disable switch in the Disable position). The indicator is turned off when the SC is logically connected to the IOCE multiplex channels.

Console Keys and Switches

The Address Compare, Storage Data Keys, Address Keys, Storage Select, Control CE and IPL controls are protected against accidental operator use by interlocking the activating control pushbutton as defined in this specification with the System Interlock Switch. Table 9-3 defines the console switch interlocking.

Reader/Punch-Printer Select Switch - This switch permits selection of IOCE interfaces designated 1, 2, 3 for interconnection of the Reader/Punch-Printer to the selected interface via the IBM 2821 Control Unit.

Reader/Punch-Printer Enable Switch-Indicator - Depression of the enable pushbutton will condition the I/O selection designated by the select switch. The indicator will be turned on at the completion of the switching operation and remain on as long as the select switch remains in this position. The indicator will turn off if the select switch is repositioned to select another interface. The indicator will be turned on if either the enable pushbutton is depressed or the select switch is returned to the initial selected position.

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Printer Keyboard Select Switch - This switch permits selection of
the IOCE interface designated 1, 2, 3 for interconnection of the
Printer Keyboard to the selected interface via the adapter control
unit in the console. The 1052 adapter is described in Chapter 6.

Printer Keyboard Enable Switch/Indicator - Depression of the enable
pushbutton will condition the I/O selection designated by the select
switch. The indicator will be turned on at the completion of the
switching operation and remains on as long as the select switch
remains in this position. The indicator will turn off if the select
switch is repositioned to select another interface. The indicator
will be turned on if either the enable pushbutton is depressed or
the select switch is returned to the initial selected position.

Table 9-3. System Console Switch Interlocking

| Always Enabled | Under System Interlock Switch Control |
|---|---|
| Emergency Pull | Control CE Activate |
| Power On/Off | CE Select |
| Thermal Reset | |
| Power A & B | Addr. Comp. Enable |
| Reader/Punch-Printer Select | Start |
| Reader/Punch-Printer Enable | |
| | Set IC |
| Printer Keyboard Select | |
| Printer Keyboard Enable | Store |
| Bell Reset | Display |
| Console Reset | |
| Buzzer Reset | Stop |
| Lamp Test | All Stop |
| Marginal Checking | Interrupt |
| Sense Switches | Load |
| I/O Interface Enable/Disable | Rate |

I/O Interface Enable/Disable Switch - The I/O Interface Enable/
Disable switch allows the operator to logically disconnect all
control units associated with the SC from the IOCE multiplexor
channels. The switch must be placed in the Disable position prior
to dropping power on the SC to prevent interruption of other chan-
nel operations. The operator must wait until the Disabled indicator
is turned on (indicating all interfaces are logically disconnected)
before dropping power. When power is turned on, the Interface

Enable/Disable switch should be in the Disable position. After
power sequence complete, the switch may be placed in the Enable
position, which allows the logical connections to be made to the
IOCE's.

Control CE Switches - Four switches are provided to modify the
four SCON bits in the CCR of the selected CE. Each switch modifies
the corresponding SCON bit when the Activate button is depressed and
the state bits of the selected CE are reset to 00. (Refer to
Modification of CE Configuration Registers).

Control CE Activate Pushbutton - Depression of this pushbutton
transfers the contents of the Control CE Switches to the SCON bits
in the configuration register of the selected CE and resets the
State bits to 0,0. The System Interlock switch must be turned on to
enable this pushbutton.

Storage Data Keys - Thirty-two Storage Data Keys are provided on the
System Console to allow manual data generation for transfer into any
program addressable Local Storage or Main Storage location. The
console shall automatically assign odd byte parity to the data,
which will be checked at the selected Computing Element.

Sense Switches - Six switches on the console are provided for pro-
gram sense switch operations. The contents of the switches are
transferred with odd parity when the Console's Control Unit
recognizes the specified Read Sense Switch command byte (Sense
Switch Entry Section).

Instruction Address Keys - Twenty-four Instruction Address Keys
(referred to as Address Keys) are provided on the System Console
to enable addressing of any addressable Local Storage or Main
Storage location. The console automatically assigns odd byte parity
to the address which will be checked at the selected Computing
Element.

Storage Select Switch - The Storage Select Switch is a two position
switch which will select the storage area to be addressed by the
address keys:

       1.   Center Position - Main Storage.

       2.   Down Position - Local Storage (in the selected CE).

Address Compare - The Address Compare switch is a three position
switch which operates in conjunction with the Computing Element

Select Switch, Address Keys, Storage Data Keys, System Interlock
switch, and Address Compare Enable pushbutton.  The positions of the
switch are:

      1.  STOP

      2.  PROCESS

      3.  LOOP

In the STOP position, any memory access by the selected
Computing Element to the address specified in the Address Keys
causes that Computing Element to enter the Stopped State at the end
of the instruction that made the storage reference.

In the PROCESS position, normal processing functions of the
Computing Elements are performed.  This is the normal position for
the Address Compare Switch.  In all other positions, the System
Interlock switch must be turned on and the enable pushbutton
depressed.

The LOOP position of the Address Compare Switch, coupled with
the use of the Storage Data, IA  Keys and the ENABLE pushbutton,
allows an instruction or set of instructions to be repeated
continuously by the selected CE until there is manual intervention.
The instruction(s) can be executed at normal speeds or single
stepped.  The bounds of the loop are defined by the addresses set in
the Storage Data and IA  keys.  The first address of the loop is
specified by the Storage Data Keys.  Some care must be exercised,
since a branch instruction in the set of instructions within the
loop can make the loop much larger than contemplated.

Address Compare Enable - Depression of the Enable pushbutton with
the System Interlock switch turned on enables the Address Compare
switch in the STOP and LOOP positions.  Release of the ENABLE push-
button has the effect of placing the Address Compare switch in the
PROCESS position.

Rate - The Rate is a two position switch which operates in
conjunction with the Computing Element Select Switch, Start and Stop
Pushbuttons, and System Interlock Switch.  The Stop pushbutton must
be depressed before putting the Rate switch in the Instruction Step
position.  The positions of the switch are:

      1.  Process

      2.  Instruction Step

In the PROCESS position, the selected Computing Element will
operate at normal clock speed when the Start pushbutton is
depressed.

In the INSTRUCTION STEP position, each depression of the Start
pushbutton results in one complete instruction being executed.

Any machine instruction can be executed in this mode.

When the Rate Switch is set to the Instruction Step position and an interruption occurs, no action will take place until the Start button is depressed. Then the interruption will be serviced; that is, the PSW's will be exchanged and the first instruction in the interruption handling routine will be executed. If the CE happens to be in the process of executing an instruction when an interruption occurs, the instruction will be completed and the CE will wait for the next depression of the Start pushbutton to service the interruption.

The stop at the end of each instruction execution will be identical to that achieved by the Stop button.

Start - Depression of the Start pushbutton with the System Interlock Switch turned on will start the selected Computing Element. If Start is activated after normal stop, it will cause the continuation of instruction processing as if no stop had occurred.

Console Reset - Depression of the Console Reset pushbutton resets all console logical functions. The unit status and alarm indicators are not affected.

Bell Reset - Depression of the Bell Reset pushbutton resets the audible bell alarm.

Buzzer Reset - Depression of the Buzzer Reset pushbutton resets the audible buzzer alarm.

Set IC - Depression of the Set IC pushbutton in the stopped state transfers the contents of the 24 address keys (plus odd byte parity) into the selected Computing Element's Instruction Address Counter. The System Interlock Switch must be turned on for this switch to be enabled.

Store - Depression of the Store pushbutton when the selected CE is in the stopped state causes the contents of the 32 Storage Data Keys (plus odd byte parity) to be placed into the storage location as specified by the 24 Address Keys and the Storage Select Switch. The System Interlock Switch must be turned on for this switch to be enabled.

Display - Depression of the Display pushbutton when the selected CE is in the stopped state causes the selected Computing Element to place the contents of the storage location specified by the Address Keys and the Storage Select Switch into the Console's Storage Data (SD). The System Interlock Switch must be turned on for this switch to be enabled.

Stop - Depression of the Stop pushbutton will cause the selected CE to be placed in the stopped state without destroying the Computing Element's environmental status. The selected Computing Element will proceed to the end of the current instruction being executed at the time the stop is initiated.

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If the current instruction causes a program interruption, the change of program status words (PSW) will be accomplished before stopping. An I/O device will be allowed to complete its operation, although I/O or external interruptions will not be recognized. The System Interlock Switch must be turned on for this switch to be enabled.

All Stop - Depression of this pushbutton with the System Interlock switch turned on causes all Computing Elements to enter the stopped state at the completion of their current instructions as defined above for Stop.

Main Storage Select - A rotary switch is provided to select the Main Storage Element for IPL. The output signal levels from this switch are binary, with odd parity assigned at the console. This switch has the capability to select up to ten storage elements when expansion so requires.

Computing Element Select - A four-position rotary switch is provided which will transmit a "select" line to the selected Computing Element. The System Interlock switch must be turned on for this switch to be enabled.

Load Unit - Three hexadecimal rotary type switches are provided to select the channel address and I/O unit addresses.

Channel Address - This rotary switch designates the data path input to each IOCE during Initial Program Load. The switch is numbered (0) through (A). The output signal levels from this switch are binary with parity assigned at the System Console.

Unit Address - Two rotary switches are provided to select a total of 256 unique I/O unit addresses during initial program load. Each switch is numbered (0) through (F). The output signal levels from each switch are binary and common odd parity (i.e., for both switches), is assigned at the System Console.

Load - Depression of the Load pushbutton will generate a signal to enable the IPL switch settings (Load Unit switches and Main Storage Select) to the selected Computing Element. When the load operation starts, the Computing Element will turn the Load pushbutton indicator on. When the IPL operation is complete, the selected Computing Element will turn the Load indicator off. The System Interlock switch must be on for this button to be enabled.

Interrupt - Depression of the Interrupt pushbutton causes a Console Interrupt signal which sets bit 25 of the PSW in the selected Computing Element. The System Interlock switch must be on for this switch to be enabled.

System Interlock - The System Interlock is a two position On-Off switch. A key is inserted to turn the switch On and may not be extracted until the switch is turned Off. In the On position, a red

indicator is turned on in the Mode of Operation display to warn the operator that manual controls on the console are enabled.

The System Interlock will enable the console manual controls as defined in Table 9-3.

Lamp Test - Two lamp test switches are provided on the console to permit the operator to test the operator's panel for faulty indicators.

1. Lamp Test Pushbutton - Depression of the Lamp Test Push-button turns on all status, register, and control indicators on the operator's panel.

2. Lamp Test Rotary Select - Rotation of this selection switch will test the alphanumeric displays for the Mode of Operation and the following indicators: Load, Invalid Selection, Test Mode, Enable and Red Dot (System Interlock Indicator).

POWER CONTROL, MARGINAL CHECKING, AND INDICATORS

The power controls and indicators provided on the console are used to monitor the system power source, control and monitor the power of the console, and provide a central position for removal of power to all elements of the IBM 9020D System by manually tripping the Emergency Pull Switch located on the console. Manually switch-able duplexed power supplies are provided for the console logic, and are sequenced upward and downward to protect against erroneous signal levels on the interconnected element data paths. Thermal, over-under voltage, and over current sensing, is provided in the power fault detection circuitry.

Marginal checking, facilities are provided on the operator's panel to manually provide voltage excursions on the +6 voltage supply for each set of power supplies to detect marginal circuitry in the logic. The marginal check controls are to be used only by trained personnel.

Control of power for the IBM 2821 Control Unit is supplied from the System Console. When the console power sequence is complete, power will automatically be turned on in the IBM 2821 Control Unit providing its Remote/Local switch is in the Remote position. When the console Power On/Off switch is turned off, power will automatically be turned off in the IBM 2821 Control Unit.

In the event of prime power failure, the console will cycle its own power up without manual intervention when prime power is restored, provided the console Power On/Off switch is on.

The operator controls and indicators are described in the following sections.

Table 9-4 lists the controls and indicators described in this section.

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Table 9-4.  Power Controls and Indicators

| Name | Implementation |
|------|----------------|
| Power On/Off | Illuminated Pushbutton Switch |
| Power Supply Select | Rotary Switch |
| Emergency Pull | Pull Switch |
| Thermal Reset | Pushbutton Switch |
| Marginal Voltage | Voltmeter |
| Marginal Excursion | Potentiometers (2) |
| Marginal Voltage | Indicators (2) |
| Calibrate | Voltage Jacks (2) |
| System Standby | Indicator |
| Battery | Indicator |
| Console Main Line On | Indicator |
| Console Power Check | Indicator |
| Thermal Check | Indicator |
| Power Sequence Complete | Indicator |

Power Switches

Power On/Off Switch - The Power On/Off switch is an illuminated pushbutton located in Panel H, Figure 9-3.  Depressing this switch will cause it to illuminate, cooling blowers to be turned on, and the DC power supplies to be sequenced on.  After the last DC supply is sequenced on, the Power Check light will be turned off, and the Power Sequence Complete light will be turned on.

When power is on, depressing this switch turns off the light, the DC power supplies will be sequenced off and the cooling blowers will turn off.  When the first DC supply is sequenced off, the Power Sequence Complete light will go out and the console Power Check light will come on.

Power Supply Select Switch - The Power Supply Select Switch is located in Panel A, Figure 9-3.  This switch is used to select one set (A or B) of the duplexed DC power supplies within the console when the Power On/Off switch is turned on.

Emergency Pull - This switch is a red, mechanically latched, pull-type switch, located in Panel C of Figure 9-3. When the switch is pulled, power to all IBM 9020D System Elements will be removed within a two second period. Power will still be present in the power compartments of each system element. This switch must be manually reset at the console to restore system power. Power will automatically sequence up on all units if their power switch is on.

Thermal Reset Pushbutton - The Thermal Reset Pushbutton is located on Panel B, Figure 9-3. Depression of this pushbutton turns out the Thermal Check Light and allows DC power to be restored by turning Power Off then On after loss of power due to a thermal condition, provided the temperature has been reduced to the normal operating range.

Marginal Check Controls - The marginal check controls are located in Panel A, Figure 9-3. The marginal check controls consist of a voltmeter to monitor the output of the selected +6 V DC power supply, two excursion controls to vary the selected +6 V DC power supply, an indicator for each excursion control (which is turned off only when the output of the selected DC power supply is a nominal value). Two voltage jacks are provided for calibration of the console voltmeter.

Power Indicators

System Standby Indicator - This indicator will light when the diesel generator is supplying the prime AC power to the system. The indicator circuit will function regardless of the System Console power status. The power for this indicator (if used) will be GFE.

Battery Indicator - This indicator will light when one or more of the System Elements indicates that it has switched to battery power. The indicator circuit will function regardless of the System Console power status. The element changing to battery power will supply +24 V DC to light the indicator. The +24 V DC will be removed when the element is switched to standby power, or main line power, or power is sequenced down.

Console Main Line On Indicator - This indicator is located in Panel B, Figure 9-3. The indicator will be on when prime AC is supplied from either the main or standby source, and the main console circuit breaker is on, provided the EPO switch has not been activated.

Console Power Check Indicator - This indicator is located in Panel B, Figure 9-3. The indicator will be turned on if any or all of the following conditions occur:

1. Catastrophic Power Failure

2. Temperature in excess of critical level

3. Normal Power Off

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Thermal Check Indicator - This indicator is located in Panel B, Figure 9-3. The indicator will be turned on when the console operating temperature is within approximately 10 degrees of the thermal shutdown temperature.

Power Sequence Complete Indicator - This indicator is located in Panel H, Figure 9-3. The indicator will be turned on when the last DC power supply has sequenced on, to indicate that all DC voltages are available to the console logic circuits. The indicator will be turned off when the first power supply in the power down sequence is turned off.

MAINTENANCE AND TEST PANEL

This panel of the System Console (Figure 9-5) contains the controls and indicators necessary for maintenance and test of the unit, and is intended for use by trained maintenance personnel only. As previously mentioned, the Marginal Checking facility is a part of the maintenance feature of the console, although these controls are located on the operator's panel.

The panel has been designed to permit manual test of the Console Control Unit, 2821 Printer-Reader/Punch Control Unit, and Printer-Keyboard Control Unit. Console checkout and maintenance will be performed during scheduled maintenance periods with console diagnostic programs.

The panel is located internally on the "B" logic gate and is accessible by opening the left side covers and swinging the "A" logic gate 90 degrees. The controls, switches and indicators are described in the following sections.

Controls and Switches

Control Unit Select Switch - The Control Unit Select is a seven position rotary select switch which will select one of the programmable eddresses for the attached I/O devices. In the case of the device attached to the 2821 Control Unit, selection of either the Printer, Reader, or Punch shall make the other two devices unavailable to IBM 9020D System. The setting of the I/O select switch on the operator's panel cannot make available any of the 2821 equipment when under control of the Control Unit Select Switch.

Selection of the console control unit interface, designated 1, 2, and 3, shall make the console unavailable to the IBM 9020D System.

Selection of any one control unit (2821, Printer Keyboard, or Console) for test allows the other two control units and their attached devices to remain available for use by the active system.

Three Test Selection indicators are provided on the maintenance and test panel to indicate the control unit in test.

CONTROL UNIT
TEST SELECTION

PRTR
2821    KEYBD    CNSL

CONTROL UNIT SELECT
PRTR KEYBD

TEST

2821
PRTR
PCH
RDR

1
2
3

CONSOLE

OPERATE

BUS IN

P    0    1    2    3    4    5    6    7

PARITY
INSERT
CORRECT    0    1    2    3    4    5    6    7

BUS OUT

INCORRECT

CONTROL IN

REQ    SEL    OP    ADR    STATUS    SERV

CONTROL OUT

ADR    SEL    CMND    SERV    SUP

MODE

SINGLE
BYTE

CONTINUOUS
TRANSFER

SINGLE
COMMAND

RESET                                   START

TEST CONTROLS
BUS        ADR
INITIAL    WRITE    OUT    OUT
SEL        MODE    GATE    GATE

PRINTER KEYBOARD CONTROL UNIT

INITIAL    WRITE              INTRVN                CMND      EQUIP    BUT OUT
SEL        MODE    ATTN    REQD    BUSY    REJECT    CHECK    CHECK

DATA REGISTER

0    1    2    3    4    5    6    7

STATUS              INHIBIT    UPPER    PRTR    PRTR
STOP    STACKED    PRD    CAR RET    CASE    BUSY    CYCLE

CONSOLE CONTROL UNIT

REQ    ADR    STATUS    SERV    OPL              INITIAL            END
IN     IN     IN        IN      IN    CHAIN    SEL     DISC    OP

BUS OUT

P    0    1    2    3    4    5    6    7

CONTROL LATCHES
MODE                    SENSE    CONFIG    TEST
INDR    BELL    BUZZER    SW    REG    I,O    SENSE    NOP

SELECTED            SCAN CTRL        CONFIG REG CTRL
CTR            RESET
1    2    3    1    2    BIT 2    BIT 1    CTRL 2    CTRL 1

LAMP TEST

Figure 9-5.    System Console Maintenance and Test Panel

Test/Operate Key - The Test/Operate Key is a two position toggle switch.  In the Test position, the switch enables all controls on the maintenance panel and turns on the Test Mode indicator on the Operator's panel.  In the Operate position, the switch permits normal console operation and turns off the Test Mode indicator.

BUS Out Keys - Eight toggle switches (0 1 2 3 4 5 6 7) are provided on the panel to manually enter data or commands to the interface designated by the Control Unit Select Switch.

Parity Insert Key - The Parity Insert Key is a two position toggle switch.  In the Correct position, it causes odd parity to be assigned to the contents of the BUS Out Keys.  In the Incorrect position, it causes even parity to be assigned to the contents of the BUS Out Keys.

Control Out Keys - Five toggle switches, ADDRESS, SELECT, COMMAND, SERVICE, and SUPPRESS, are provided on the panel to manually sequence control functions to the interface designated by the Control Unit Select Switch.  All control lines normally transmitted with five controls are automatically generated and transmitted by the test circuitry.

Reset - Depression of the Reset pushbutton resets the logic associated with the maintenance and test panel, resets the selected Control Unit, and connects the test panel to the designated control unit.

Mode Select Switch - The Mode Select is a three position select switch which will select the test panel mode of operation to facilitate the generation of commands and/or data from the panel.

In the Single Command position, the five Control Out Keys are activated by depression of the Start pushbutton; this allows single commands to be sequenced to the interface selected.

In the Single Byte mode, the logic is conditioned to automatically sequence the interface commands.  This mode of operation allows the operator to transmit or receive a single byte of data for each depression of the Start pushbutton.

In the Continuous Transfer Mode of operation, data is transmitted or received continuously after depression of the Start Pushbutton, providing a convenient method of scoping internal circuitry. The operation is terminated by the control unit sending status or by the operator switching to Single Byte or Single Command mode.

Start - Depression of the Start pushbutton in Test Mode initiates a command or data transfer in the test mode specified by the Mode Selection Switch.

Lamp Test - Depression of the Lamp Test pushbutton turns on all indicators displayed on the Maintenance and Test panel.

## Indicators

Control Unit Select Indicators - Three Test Selection indicators are provided to display which control unit is connected to the test circuitry.

1. Printer Keyboard Control Unit. This indicator will be turned on when the Control Unit Select switch is positioned to Printer Keyboard, the Test/Operate switch is in Test, and the reset pushbutton is depressed.

2. 2821 Control Unit. This indicator will be turned on when the Control Unit Select switch is positioned to select either the Printer, Reader, or Punch for test operation, the Test/Operate switch is in Test, and the reset pushbutton is depressed.

3. Console Control Unit. This indicator shall be turned on when the Control Unit Select switch is positioned to select one of the console control interfaces designated 1, 2, and 3, the Test/Operate switch is in Test, and the Reset pushbutton is depressed.

BUS In - Nine indicators (P, 0 1 2 3 4 5 6 7) are provided to display the contents of either data or commands on BUS In from the interface designated by the Console Control Unit Select Switch.

Control In - Six indicators, REQUEST, SELECT, OPERATIONAL, ADDRESS, STATUS, and SERVICE are provided to display the control lines from the interface designated by the Console Control Unit Select Switch.

Test Controls - Four indicators are provided to indicate the status of internal latches in the test panel logic. Indicators are turned on when the associated latch is set.

1. INITIAL SEL. This indicator is on when the Maintenance and Test Panel is in an initial select cycle.

2. WRITE MODE. This indicator is on when the Maintenance and Test Panel is performing a Write command.

3. BUS OUT GATE. This indicator is on when the Bus Out Switches are gated to the test bus out.

4. ADR OUT GATE. This indicator is on when the address encoded from the Control Unit Select switch is on the test bus out.

Printer-Keyboard Control Unit Indicators - Twenty-three indicators are provided (plus 4 spares) to display the condition of internal latches in the 1052 (Printer Keyboard) Control Unit whether in test or operational functions.

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1.  INITIAL SEL.  This indicator is on when the 1052 CU is in
    an initial select cycle.

2.  WRITE MODE.  This indicator is on when the 1052 CU has
    decoded a Write command.

3.  ATTN.  This indicator is on when the Attention Status bit
    has been set by the Request pushbutton.

4.  INTRVN REQD.  This indicator is on when the Not Ready
    condition (Out of forms, Not Ready pushbutton) is
    detected by the 1052 CU.

5.  BUSY.  This indicator indicates that a Busy Status has
    been set due to the 1052 CU being busy with a command or
    when Attention or Device End is set.

6.  CMND REJECT.  This indicator is on when an invalid
    command code is detected by the 1052 CU.

7.  EQUIP CHECK.  This indicator is on if:

    a.  Incorrect parity is detected from the Keyboard during
        a Read operation.

    b.  The Printer fails to take a mechanical cycle as
        determined by the absence of a Printer Cycle signal.

    c.  There is a bad comparison check between the Keyboard
        input parity and the generated aux magnet parity.

8.  BUS OUT CHECK.  This indicator is on when the 1052 CU
    detects incorrect parity on the Bus Out.

9.  thru

16. DATA REGISTER bit positions 0 through 7.  These
    indicators are on when the corresponding bit in the
    1052 CU data register is set to a one.

17. **STOP.  This indicator is on when the 1052 CU detects a
    stop from the IOCE during Write or Read, or when the Enter
    or Cancel pushbuttons are depressed during Read.**

18. STATUS STACKED.  This indicator is on when this condition
    is recognized by the 1052 CU.

19. PRD.  This indicator is on when the Proceed light is on
    at the Keyboard and the 1052 CU can accept a character
    from the Keyboard.

20. INHIBIT CAR RET.  This indicator is on when the 1052 CU
    is executing the Write, Inhibit Carrier Return command.

21. UPPER CASE. This indicator is on when the Printer is in upper case.

22. PRTR BUSY. This indicator is on when the Printer is executing a print or function cycle.

23. PRTR CYCLE. This indicator is on when the Printer executes a mechanical cycle upon receipt of a character.

Console Control Unit Indicators - Thirty-five indicators (plus one spare) are provided to display the condition of internal latches in the Console Control Unit (CCU) whether in test or operational functions.

1. REQ IN.

2. ADR IN.

3. STATUS IN.

4. SERV IN.

5. OPL IN.

These indicators are on when the corresponding latch is set by the CCU trying to raise the corresponding inter-face line to the IOCE. That line is not necessarily up.

6. CHAIN. This indicator is on when command chaining is indicated from the IOCE.

7. INITIAL SET. This indicator is on when the CCU is an initial selection cycle.

8. DISC. This indicator is on when the CCU detects a Stop command, HALT I/O or Stack status from the IOCE.

9. END OP. This indicator is on when the CCU is in the process of ending an operation. It normally causes Channel End and Device End to be sent to the IOCE.

10. thru

18. BUS OUT bit positions P, 0 through 7. These indicators are on when the corresponding bit on Bus Out from the selected IOCE is set to one.

19. MODE INDR.

20. BELL

21. BUZZER

22. SENSE SW

23. CONFIG REG

24. TEST I/O

25. SENSE

26. NOP

These indicators are on when the corresponding control
latch is set due to decoding the associated command
by the CCU.

27. thru

29. SELECTED 1, 2, 3. These indicators are on when the
associated IOCE is presently working with the CCU; only
one IOCE can be selected at a given time.

30, 31. SCAN CTRL 1, 2. These indicators are on when their
associated latches, concerned with interface selection, are
set.

SCAN CTRL 1 is set when operating with an IOCE;
SCAN CTRL 2 when not operating with an IOCE.

32, 33. CONFIG REG CTRL CTR Bit 1, Bit 2. These two indicators
indicate by their binary count (0-3) which of the four
bytes in the selected Configuration Register is being
written.

34, 35. CONFIG REG CTRL RESET CTRL 1, CTRL 2. These two
indicators indicate by their binary count (0-3) which
of the four Configuration Registers is being updated.

SYSTEM MAINTENANCE MONITOR CONSOLE INTERFACE

Interface Signals

The 9020D SC to SMMC Interface consists of the following signals:

112 Configuration Lamp signals

10 Mode Indicator signals

28 Power Check signals

The signals present the same information to the SMMC as is displayed
by the System Console.

Configuration Lamp Signals - The 112 signals are broken down into
four rows of 28 lamps each. All 28 lines for the four rows may be
programmed by the 9020D even though CE-4 and SE-9 through 12 are not
installed in the system. It will be the responsibility of the CCC
program and/or the SMMC to recognize the lack of CE#4 and/or main
storages 9 through 12.

Mode Indicator Signals - The 10 signals are broken into three alpha and seven numeric lines.  These correspond to the two positions of the Mode Indicator on the SC.  No more than one alpha and one numeric line will be active at one time.

Power Check Signals - Twenty eight signals are provided, one for each of four CEs, three IOCEs, 12 SEs, three PAMs, three SCUs, and three TCUs.  The signal will be activated by the respective unit when any one of the following conditions exist:

     1.   Normal Power Off

     2.   Over Temperature Condition

     3.   Catastrophic Power Supply Failure

ELECTRICAL CHARACTERISTICS

Configuration and Mode Indicator Signals

The interface drivers for the configuration lamp and mode indicator signals will provide the following levels:

     Signigicant level positive (Lamp ON)

        Max. up level     +5.75 v

        Min. up level     +4.50 v

     Non Significant level (Lamp OFF)

        Max. down level  +.3 v

        Min. down level     OV

Each signal line at the SMMC should be terminated with 510 ohms to ground.

   During the period of preventive maintenance on the System Console, the significant level may be as high as +6.75 and as low as +3.0V.  The down level will be unaffected.

   The rise and fall times associated with the configuration lamp and mode indicator signals are specified at the System Console output connector pins.  The 510 ohm terminator resistor to ground is connected at the SC output pin with no external cable attached. With this configuration, the worst case rise and fall time at the output pin will not exceed the following values:

     Rise Time         10 ns.
     Fall Time         10 ns.

When the external cable is attached to the SC and the termination resistor moved to the SMMC, the rise and fall times at the receiving end must be determined by measurement.

Power Check Signals

This signal is full-wave rectified 60 cps. AC which results in a
non-filtered +27v ± 3v DC. Termination of the signal at the SMMC
must be 750 ohms or greater to limit the load current to 40 ma or
less. The significant signal (Power Check indicated) is +27v ± 3v
DC. The absence of the voltage (ground or open) indicates no power
check.

Cable Configuration

Four 48-pin Serpent connectors are provided in the System Console
I/O area for the 112 configuration lamp signals, 10 mode indicator
signals, and 28 Power Check signals. Pin assignments for these four
connectors are shown in Tables 9-5 through 9-8. The external cables
must have Type B-connectors to properly mate with the Type A
connectors mounted in the System Console. Ground return lines should
be carried as individual conductors through the external cables and
connectors to minimize ground shift.

Table 9-5. 9020D SC to SMMC Pin Assignment Connector 01S-S3C2

| Pin | Line Name | Pin | Line Name |
|-----|-----------|-----|-----------|
| B02 | Config. Reg-1 CE-1 | G02 | **Config. Reg-1 Storage 12** |
| D02 | Gnd Return | J02 | Gnd Return |
| B03 | Config. Reg-1 CE-2 | G03 | Config. Reg-1 PAM-1 |
| D03 | Config. Reg-1 CE-3 | J03 | Config. Reg-1 PAM-2 |
| B04 | Config. Reg-1 CE-4 | G04 | Config. Reg-1 PAM-3 |
| D04 | Config. Reg-1 IOCE-1 | J04 | Config. Reg-1 TCU-1 |
| B05 | Config. Reg-1 IOCE-2 | G05 | Config. Reg-1 TCU-2 |
| D05 | Config. Reg-1 IOCE-3 | J05 | Config. Reg-1 TCU-3 |
| B06 | Config. Reg-1 Storage-1 | G06 | Config. Reg-2 CE-1 |
| D06 | Config. Reg-1 Storage-2 | J06 | Config. Reg-2 CE-2 |
| B07 | Gnd Return | G07 | Gnd Return |
| D07 | Config. Reg-1 Storage-3 | J07 | Config. Reg-2 CE-3 |
| B08 | Config. Reg-1 Storage-4 | G08 | Config. Reg-2 CE-4 |
| D08 | Gnd Return | J08 | Gnd Return |
| B09 | Config. Reg-1 Storage-5 | G09 | Config. Reg-2 IOCE-1 |
| D09 | Config. Reg-1 Storage-6 | J09 | Config. Reg-2 IOCE-2 |
| B10 | Config. Reg-1 Storage-7 | G10 | Config. Reg-2 IOCE-3 |
| D10 | Config. Reg-1 Storage-8 | J10 | Config. Reg-2 Storage-1 |
| B11 | Config. Reg-1 Storage-9 | G11 | Config. Reg-2 Storage-2 |
| D11 | Config. Reg-1 Storage-10 | J11 | Config. Reg-2 Storage-3 |
| B12 | **Config. Reg-1 Storage-11** | G12 | Config. Reg-2 Storage-4 |
| D12 | **Config. Reg-1 SCU-1** | J12 | **Config. Reg-1 SCU-3** |
| B13 | **Gnd Return** | G13 | **Gnd Return** |
| D13 | **Config. Reg-1 SCU-2** | J13 | **Config. Reg-2 SCU-1** |

Table 9-6. 9020D SC to SMMC Pin Assignment Connector 01S-S3D2

| Pin | Line Name | Pin | Line Name |
|-----|-----------|-----|-----------|
| B02 | Config. Reg-2 Storage 5 | G02 | Config. Reg-3 IOCE-1 |
| D02 | Gnd Return | J02 | Gnd Return |
| B03 | Config. Reg-2 Storage 6 | G03 | Config. Reg-3 IOCE-2 |
| D03 | Config. Reg-2 Storage-7 | J03 | **Config. Reg-3 IOCE-3** |
| B04 | Config. Reg-2 Storage-8 | G04 | **Config. Reg-3 Storage 1** |
| D04 | Config. Reg-2 Storage-9 | J04 | Config. Reg-3 Storage-2 |
| B05 | Config. Reg-2 Storage-10 | G05 | Config. Reg-3 Storage-3 |
| D05 | **Config. Reg-2 Storage-11** | J05 | Config. Reg-3 Storage-4 |
| B06 | **Config. Reg-2 Storage-12** | G06 | Config. Reg-3 Storage-5 |
| D06 | Config. Reg-2 PAM-1 | J06 | Config. Reg-3 Storage-6 |
| B07 | Gnd Return | G07 | Gnd Return |
| D07 | Config. Reg-2 PAM-2 | J07 | Config. Reg-3 Storage-7 |
| B08 | Config. Reg-2 PAM-3 | G08 | Config. Reg-3 Storage-8 |
| D08 | Gnd Return | J08 | Gnd Return |
| B09 | Config. Reg-2 TCU-1 | G09 | Config. Reg-3 Storage-9 |
| D09 | Config. Reg-2 TCU-2 | J09 | Config. Reg-3 Storage-10 |
| B10 | Config. Reg-2 TCU-3 | G10 | Config. Reg-3 Storage-11 |
| D10 | Config. Reg-3 CE-1 | J10 | Config. Reg-3 Storage-12 |
| B11 | Config. Reg-3 CE-2 | G11 | Config. Reg-3 PAM-1 |
| D11 | Config. Reg-3 CE-3 | J11 | Config. Reg-3 PAM-2 |
| B12 | Config. Reg-3 CE-4 | G12 | Config. Reg-3 PAM-3 |
| D12 | **Config. Reg-2 SCU-2** | J12 | **Config. Reg-3 SCU-1** |
| B13 | Gnd Return | G13 | Gnd Return |
| D13 | **Config. Reg-2 SCU-3** | J13 | **Config. Reg-3 SCU-2** |

Table 9-7.   9020D SC to SMMC Pin Assignment Connector 01S-S3E2

| Pin | Line Name | Pin | Line Name |
|-----|-----------|-----|-----------|
| B02 | Config. Reg-3 TCU-1 | G02 | Config. Reg-4 Storage-9 |
| D02 | Gnd Return | J02 | Gnd Return |
| B03 | Config. Reg-3 TCU-2 | G03 | Config. Reg-4 Storage-10 |
| D03 | Config. Reg-3 TCU-3 | J03 | **Config. Reg-4 Storage-11** |
| B04 | Config. Reg-4 CE-1 | G04 | **Config. Reg-4 Storage-12** |
| D04 | Config. Reg-4 CE-2 | J04 | Config. Reg-4 PAM-1 |
| B05 | Config. Reg-4 CE-3 | G05 | Config. Reg-4 PAM-2 |
| D05 | Config. Reg-4 CE-4 | J05 | Config. Reg-4 PAM-**3** |
| B06 | Config. Reg-4 IOCE-1 | G06 | Config. Reg-4 TCU-1 |
| D06 | Config. Reg-4 IOCE-2 | J06 | Config. Reg-4 TCU-2 |
| B07 | Gnd Return | G07 | Gnd Return |
| D07 | Config. Reg-4 IOCE-3 | J07 | Config. Reg-4 TCU-3 |
| B08 | Config. Reg-4 Storage-1 | G08 | Mode Ind. Alpha-A |
| D08 | Gnd Return | J08 | Gnd Return |
| B09 | Config. Reg-4 Storage-2 | G09 | Mode Ind. Alpha-B |
| D09 | Config. Reg-4 Storage-3 | J09 | Mode Ind. Alpha-C |
| B10 | Config. Reg-4 Storage-4 | G10 | Mode Ind. Numeric-1 |
| D10 | Config. Reg-4 Storage-5 | J10 | Mode Ind. Numeric-2 |
| B11 | Config. Reg-4 Storage-6 | G11 | Mode Ind. Numeric-3 |
| D11 | Config. Reg-4 Storage-7 | J11 | Mode Ind. Numeric-4 |
| B12 | Config. Reg-4 Storage-8 | G12 | Mode Ind. Numeric-5 |
| D12 | **Config. Reg-3 SCU-3** | J12 | Mode Ind. Numeric-6 |
| B13 | **Gnd Return** | G13 | Gnd Return |
| D13 | **Config. Reg-4 SCU-1** | J13 | Mode Ind. Numeric-7 |

Table 9-8.  9020D SC to SMMC Pin Assignment Connector 01S-S3B2

| Pin | Line Name | Pin | Line Name |
|-----|-----------|-----|-----------|
| B02 | Power Check CE-1 | G02 | Power Check PAM-1 |
| D02 | Gnd Return | J02 | Gnd Return |
| B03 | Power Check CE-2 | G03 | Power Check PAM-2 |
| D03 | Power Check CE-3 | J03 | Power Check PAM-3 |
| B04 | Power Check CE-4 | G04 | Power Check TCU-1 |
| D04 | Power Check IOCE-1 | J04 | Power Check TCU-2 |
| B05 | Power Check IOCE-2 | G05 | Power Check TCU-3 |
| D05 | Power Check IOCE-3 | J05 | **Power Check SCU-1** |
| B06 | Power Check Storage-1 | G06 | **Power Check SCU-2** |
| D06 | Power Check Storage-2 | J06 | **Power Check SCU-3** |
| B07 | Gnd Return | G07 | Gnd Return |
| D07 | Power Check Storage-3 | J07 | Spare |
| B08 | Power Check Storage-4 | G08 | Spare |
| D08 | Gnd Return | J08 | Gnd Return |
| B09 | Power Check Storage-5 | G09 | Spare |
| D09 | Power Check Storage-6 | J09 | Spare |
| B10 | Power Check Storage-7 | G10 | Spare |
| D10 | Power Check Storage-8 | J10 | Spare |
| B11 | Power Check Storage-9 | G11 | Spare |
| D11 | Power Check Storage-10 | J11 | Spare |
| B12 | **Power Check Storage-11** | G12 | Spare |
| D12 | **Power Check Storage-12** | J12 | **Config. Reg-4 SCU-2** |
| B13 | Gnd Return | G13 | **Gnd Return** |
| D13 | Spare | J13 | **Config. Reg-4 SCU-3** |

Chapter 10. IBM 7265-03 CONFIGURATION CONSOLE

INTRODUCTION

The IBM 7265-03 Configuration Console (CC) is the central monitoring
and control position for the 9020E System and also provides configur-
ation and fault reporting paths for Display Generators (DG), Radar
Keyboard Multiplexors (RKM) attached to the 9020E System. Configur-
ation data paths for the IBM 2701 Data Adapter Units (DAU) and a
programmable data path to the attached System Maintenance Monitor
Console (SMMC) are also provided.

The CC (Figure 10-1) is divided into two major functional areas:

System Console Function
Error Reporting and Reconfiguration Function

A block diagram of the Configuration Console is provided in Figure
10-2.

The System Console function is similar to the function provided
by the IBM 7265-02 System Console for the 9020D System. The function
is provided by direct connection to various elements and units and by
an internal System Console Control Unit (SCCU) which supports program-
med I/O operations for updating indicators, reading switches and
transferring data to the SMMC.

The Error Reporting and Reconfiguration Function is provided by
duplexed Reconfiguration Control Units (RCU). Each RCU is function-
ally identical and each can perform the total reconfiguration task.
The RCU's are separately powered and capable of being independently
maintained. Each RCU is attached to two (expandable to three) IOCE
multiplex channels and connections are established by configuration
control from the controlling CE.

SYSTEM CONSOLE FUNCTIONAL OPERATION

Functional operation of the System Console portion of the Configur-
ation Console is described in the following paragraphs. Basically,
the communication may be divided as operations and controls requiring
operator intervention, program generated control and status, program
generated unit status messages, and indicators to enable the operator
to monitor the 9020E System and the display subsystem equipment.
Refer to Figure 10-3.

All critical console functions are duplicated elsewhere in the
system. Table 10-1 indicates where each indicator or control is
duplicated in the event the console is not operable.

Table 10-1.    Duplication of Critical Console Indicators and Controls

| Indicator or Control | Indicator or Control Back Up | | | |
| --- | --- | --- | --- | --- |
| | CE | CE 1052 | All 9020E Major Elements | Display Units |
| 9020E System EPO * | | | | |
| 9020E Status | | | X | |
| 9020E Alarms (Faults) | | | X | |
| Display Unit Status | | X Hard Copy | | X |
| Display Unit Alarms (Faults) | | X Hard Copy | | X |
| Audible Alarms | | X Hard Copy | | |
| Subsystem Configuration | | X Hard Copy | | |
| Storage Data | X | | | |
| Instruction Address | X | | | |
| Set IC | X | | | |
| Store | X | | | |
| Display | X | | | |
| Start | X | | | |
| Stop | X | | | |
| Control CE | X | | | |
| Address Compare | X | | | |
| Rate | X | | | |
| IPL Controls | X | | | |
| Interrupt | X | | | |
| IBM 2821 Control Unit | | X | | |
| Printer-Card Read/Punch | | X | | |
| Sense Switches | | X | | |

*   Always operable from the Configuration Console
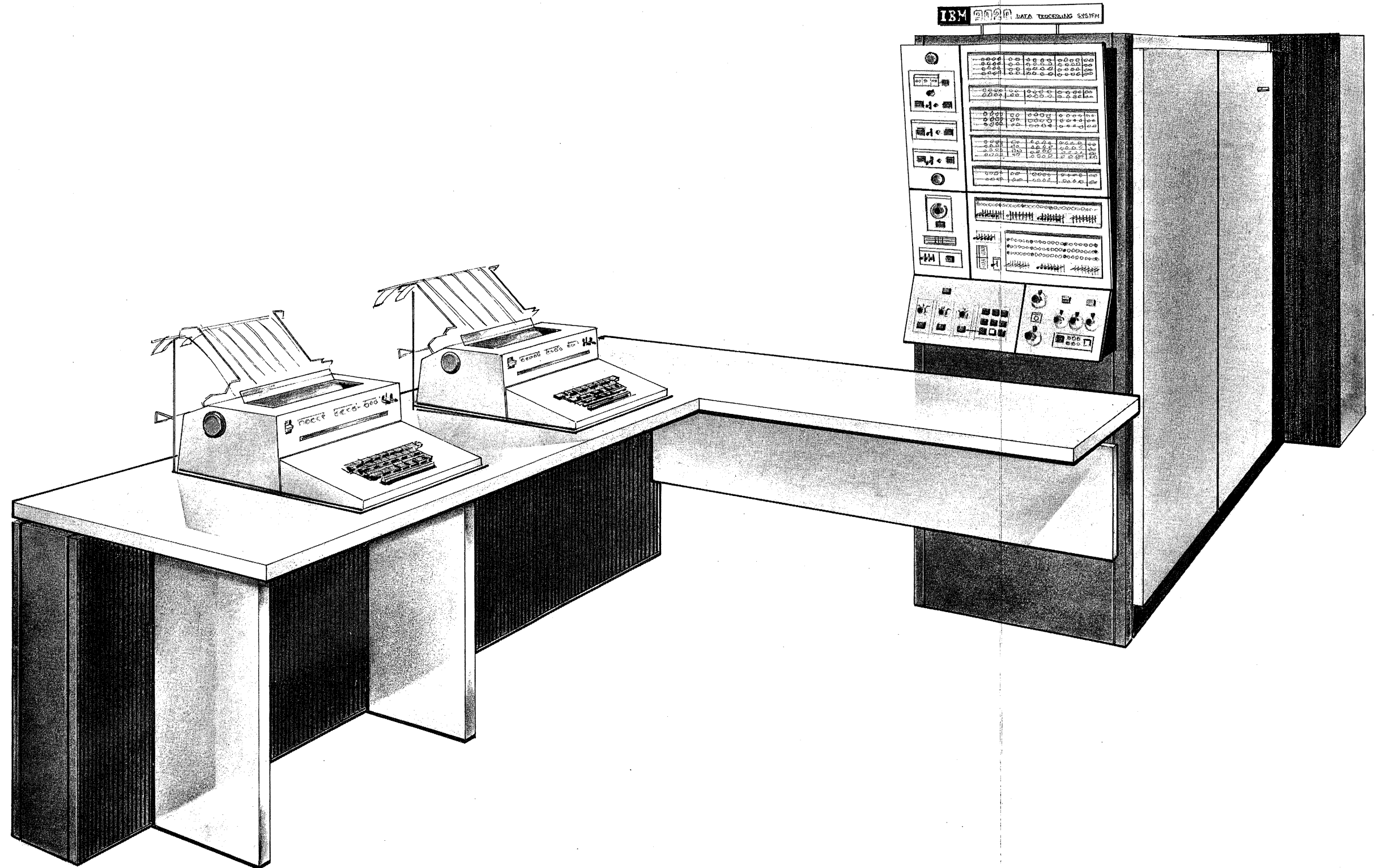
Figure 10-1.  Configuration Console
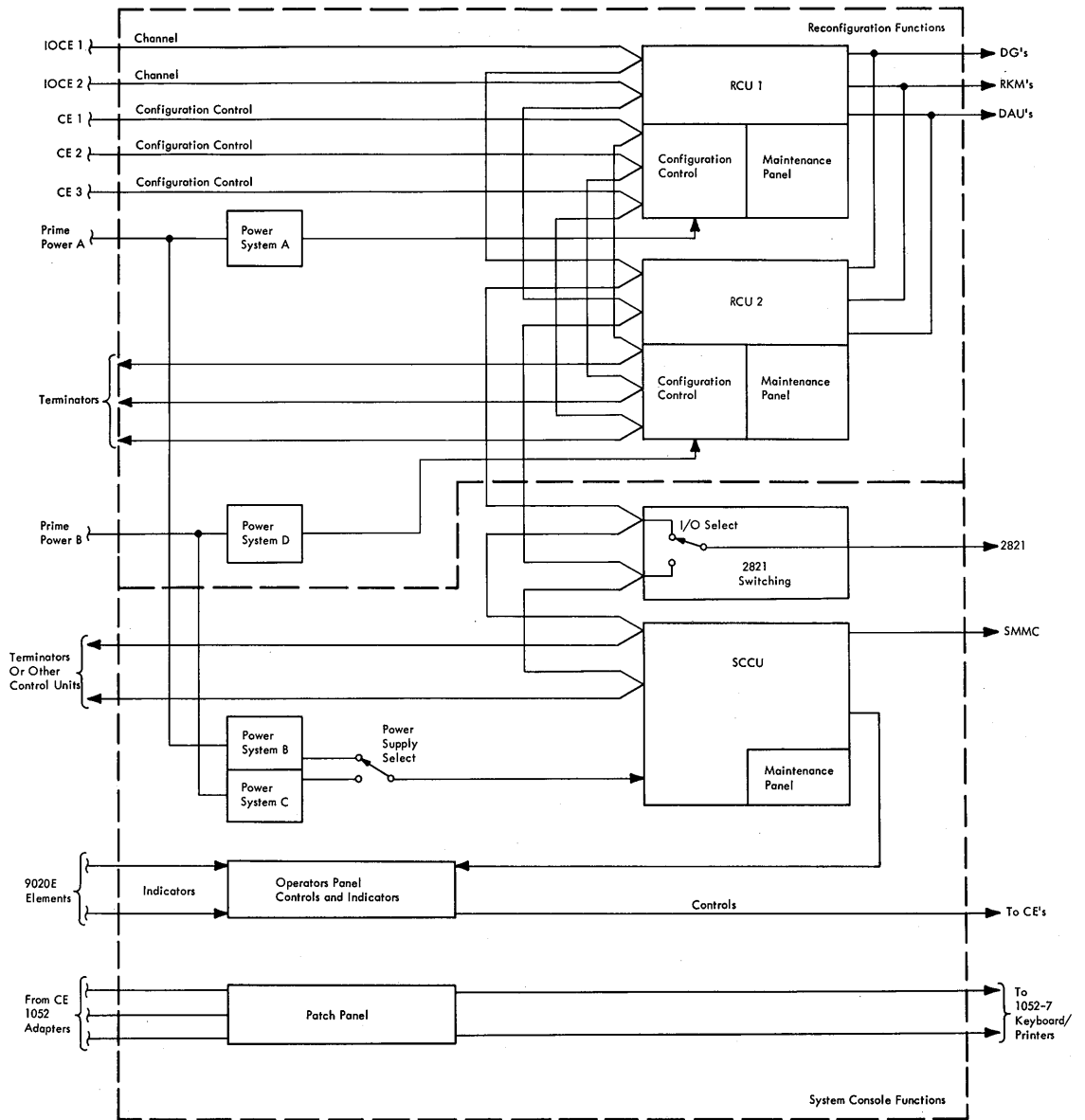
Figure 10-2. Configuration Console Block Diagram
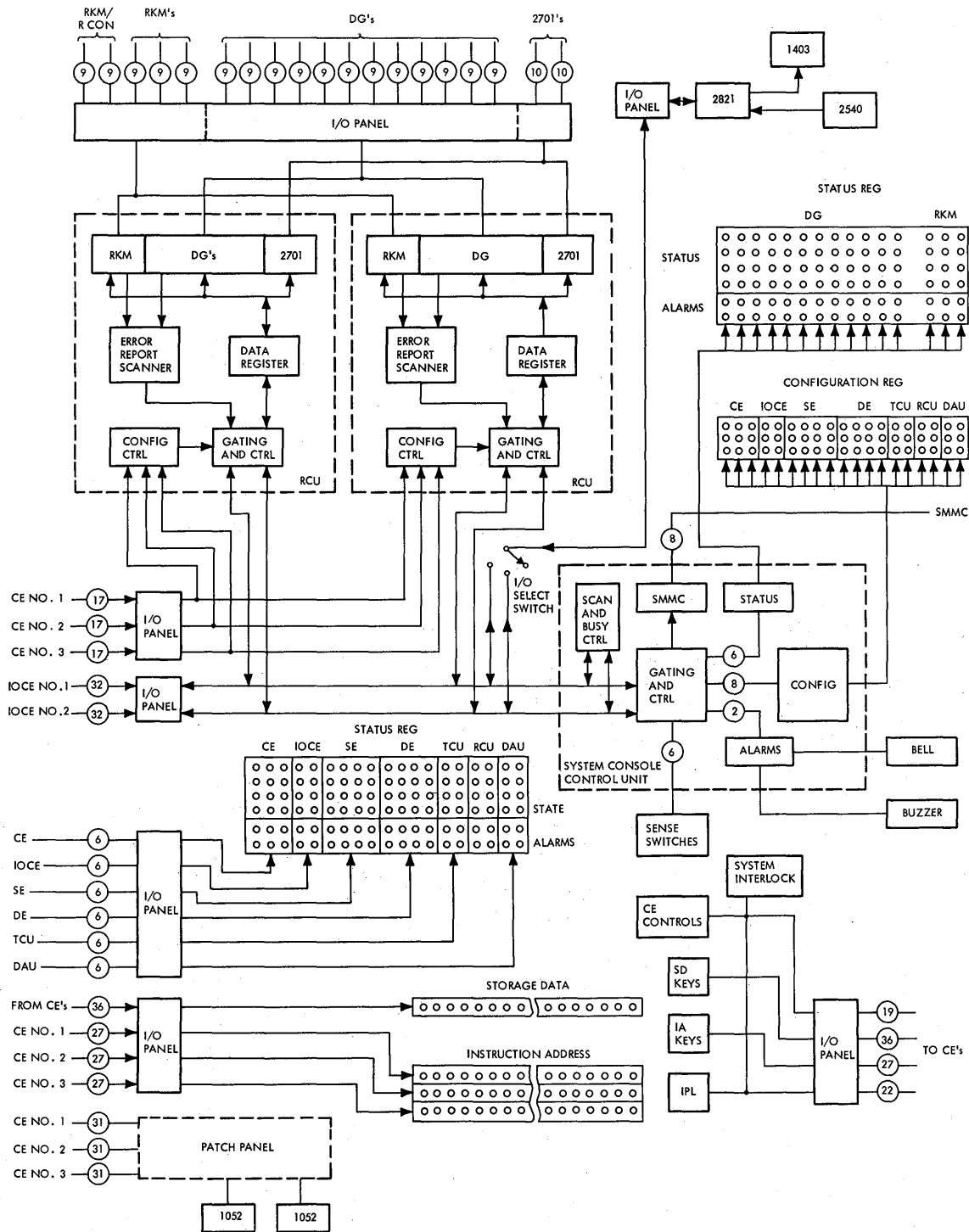
Figure 10-3. Configuration Console Data Flow Diagram

## Operator Intervention

Several important functional operations associated with control of
the active system can be controlled from the Configuration Console.
These functions include Initial Program Loading (IPL), manual entry
of information to the active system, and manual switching of I/O
equipment.

Initial Program Loading

The IPL Controls are located on Panel F, Figure 10-4. These controls
include the CE Select Switch, Main Storage Select Switch, Load Unit
Select Switch, Enable System IPL Pushbutton, Load Pushbutton and
System Interlock.

Subsystem IPL or System IPL may be performed from the CC panel.

The procedure for subsystem IPL from the Configuration Console
is as follows:

1.    Select a CE using the CE Select switch.
2.    Select a Main Storage Element using the Main Storage
      Select switch.
3.    Select the address of the I/O device containing the
      program to be loaded by using the Load Unit Select switches.
4.    Turn on the System Interlock.
5.    Depress the Load Pushbutton.

An indicator contained in the Load Pushbutton will turn on when the
IPL sequence is being performed and will remain on until the IPL is
complete. If a fault should occur during the IPL sequence, the Load
light will remain on. A Subsystem IPL is effective only when the
selected CE is in State 1 or State zero with the test switch off.

The procedure for a System IPL is the same as that described
for Subsystem IPL except that the following additional action is
required.

After turning on the System Interlock Switch, depress and hold
the Enable System Interlock Pushbutton. Depressing the Load Push-
button will then cause a system IPL.

Manual Entry of Information or Display

There are several methods of entering manual information into the
Active System; these include data entry via the IBM 1052-7 Printer
Keyboard, Sense Switch Entry, Storage Modification, Modification of
the CE Configuration Registers and modification of the CE Instruction
Counter.

Printer Keyboards. Printer Keyboards (IBM 1052-7) are located at the
Configuration Console for data entry. All 1052's enter data through
adapters located in the CE (IBM 7201-2). For flexibility a patch
panel at the Configuration Console allows the two 1052's to be elect-
rically interchanged with each other. Expansion capabilities are

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provided to allow three 1052's to be interconnected with up to four
1052 adapters.

Sense Switch Entry. The console has six sense switches shown in
Figure 10-4 which can be read by program means into storage through
one of the interconnected IOCE's. Upon acceptance of the SCCU address
and a Read Sense Switch command, the contents of all the sense
switches are transmitted to the requesting IOCE. If two or more
IOCE's address the console simultaneously, the tie will be broken by
appropriate circuits and the lowest (logically) numbered IOCE will
be given priority. All others will receive Control Unit Busy status.
The command byte has the following format:

```
        Byte Bit Positions        P 0 1 2 3 4 5 6 7
        Command                   P 0 0 0 0 0 0 1 0
```

The contents of the sense switches are returned to the requesting
IOCE in the following format:

```
        Bit Positions             P 0 1 2 3 4 5 6 7
        Data Byte                   0 0 1 1 1 1 1 1
                                    Not
                                    Used
        Sense Switch Assignment       A B C D E F
```

        A sense switch in the ON position will cause a one (1)
        to be inserted in its assigned bit position.

Storage Modification or Display. The contents of a selected storage
word in the SE or DE may be modified through the use of the Storage
Data Keys, Address Keys, Storage Select Switch, Store Pushbutton, and
CE Select Switch. The procedure for storage modification from the
Configuration Console is as follows (see Figure 10-4):

    1.   Select a CE using the CE select switch.
    2.   Enter data in Storage Data Keys. Correct byte parity (odd)
         is automatically assigned.
    3.   Enter Storage Address in the Address Keys. Correct byte
         parity (odd) is automatically assigned.
    4.   Designate Main or Local storage using Storage Select Switch.
    5.   Turn on the System Interlock.
    6.   Depress the Stop Pushbutton.
    7.   Depress the Store Pushbutton.

The contents of a selected storage word may be displayed in a similar
manner. The procedure for display of storage from the Configuration
Console is as follows (refer to Figure 10-4):

    1.   Select a CE using the CE Select Switch.
    2.   Enter storage word address in the Address Keys. Correct
         byte parity (odd) is automatically assigned.
    3.   Designate Main or Local Storage using the Storage Select
         Switch.
    4.   Turn on the System Interlock Switch.
    5.   Depress Stop Pushbutton
    6.   Depress Display Pushbutton.

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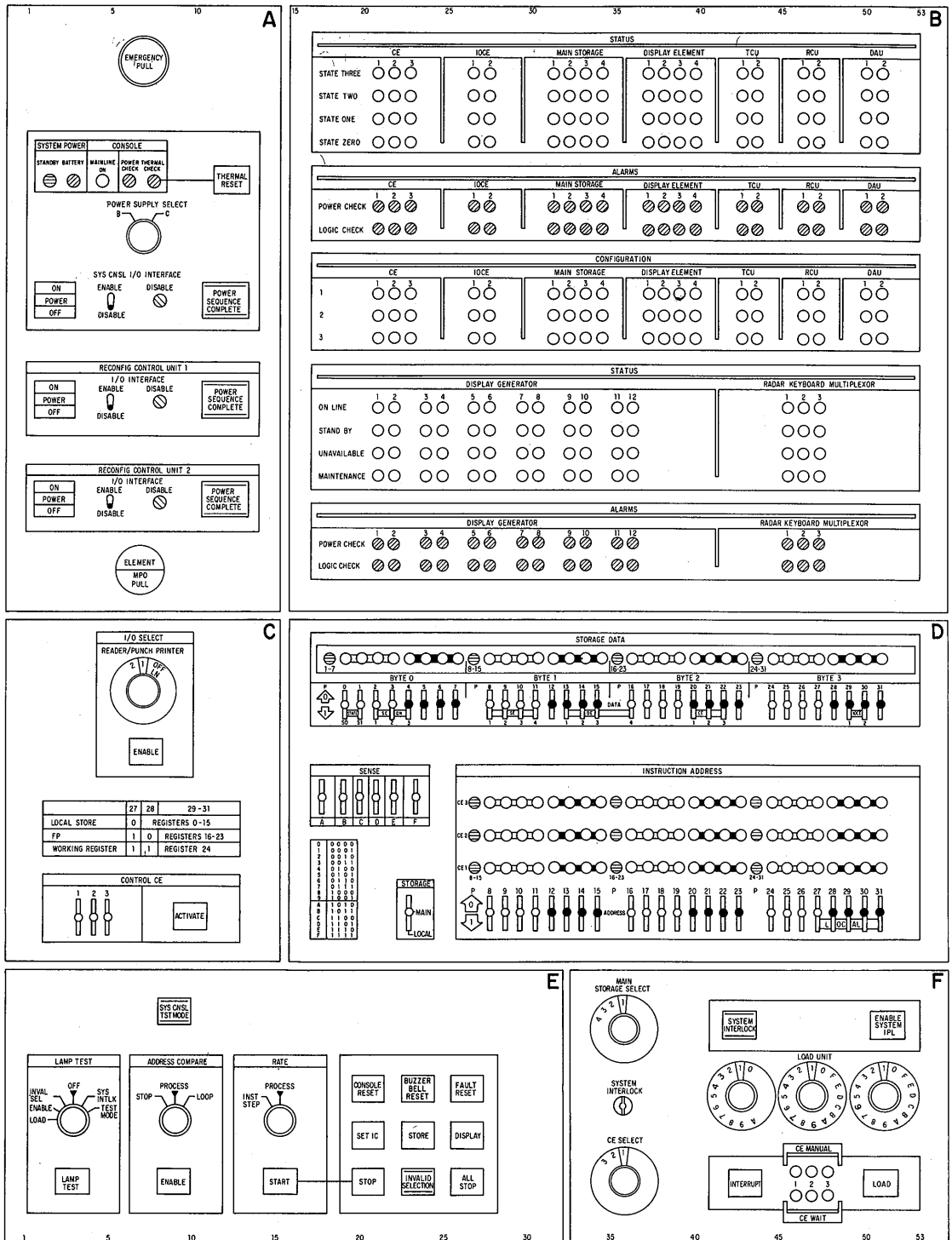
●Figure 10-4.   Configuration Console Operators Panel

If an invalid storage address for the selected CE is placed in the
Address Keys, the store or display operation will not be performed.
The invalid selection indicator will be turned on and remain on
until a valid selection is made.  An invalid selection can be caused
by attempting to reference an SE or DE which is either not operation-
al (power off) or not configured to the selected CE.  An invalid
selection can also result from the selection of a logical address
range not assigned to a range of physical addresses by the CE's
Address Translation Register (ATR).

Modification of CE Configuration Register.  The controls for modifi-
cation of the CE configuration register are located at the left
center of the operators panel (refer to Figure 10-4).  The procedure
for modification of the CE configuration register is as follows:

    1.   Set the desired configuration for the SCON bits in the
        Control CE Switches.  An odd parity bit will automatically
        be assigned.
    2.   Select the desired CE using the CE Select Switch.
    3.   Turn on the System Interlock Switch.
    4.   Depress Stop Pushbutton.
    5.   Depress the Control CE Activate Pushbutton.  The SCON bits
        will be set with the contents of the Control CE switches
        and the State bits will be reset to 00.

Modification of CE Instruction Counter.  The controls for modifica-
tion of the CE Instruction Counter (Instruction Address) are shown
in Figure 10-4.  The controls required are Address Keys, Set IC
Pushbutton, and the CE Select Switch.  The procedure is as follows:

    1.   Select a CE with the CE Select Switch.
    2.   Set the desired contents of the IC in the Address Keys.
    3.   Turn on the System Interlock.
    4.   Depress Stop Pushbutton.
    5.   Depress the Set IC Pushbutton.  The address will appear
        in the selected CE's Instruction Address indicators.


Display of Information from Local Storage

To assist the operator in setting up the address switches for dis-
playing information from Local Storage, a map of LS is provided on
the Configuration Console.  The map, indicates Address Key settings
required to display General Registers, Floating Point Registers or
the Working Register.

    When bit 27 is set to zero, bits 28-31 are used to select one
of the sixteen General Registers in Local Storage.  The registers
(0-15) are addressed by binary setting of 0000 through 1111 respect-
ively.

    Setting the Address Keys bits 27 to 1 and bit 28 to 0, selects
Floating Point Registers.  The eight (16-23) FP registers are
addressed by bits 29-31 with binary settings 000 through 111 respect-
ively.

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When bits 27 and 28 of the Address Keys are set to 11, the
Working Register (24) is addressed. The contents of the remaining
bits positions in the Address Keys are not used for this operation.

| | 27 | 28 | 29    31 |
|---|---|---|---|
| LOCAL STORE | 0 | | REGISTERS 0 - 15 |
| FP | 1 | 0 | REGISTERS 16 - 23 |
| WORKING REGISTER | 1 | 1 | REGISTER 24 |

Map of Local Storage

I/O Switching

A rotary switch and associated Enable Pushbutton are positioned on
Panel C of the operators panel. These switches provide the operator
with the ability to connect the IBM 2821 Printer-Card Read Punch/
Punch control unit to any one of the available IOCE's. The switching
is accomplished by console logic when the Enable Pushbutton is de-
pressed. When the connection is established an indicator behind the
Enable Pushbutton is turned on.

The interconnected I/O devices are independently program address-
able. The unit addresses are as follows:

       Card Reader  (IBM 2540)     03
       Card Punch   (IBM 2540)     04
       Printer      (IBM 1403-2)   05

If a selection of one of these I/O devices is attempted by an IOCE
not connected by the I/O Select Switch, a Select In signal (Condition
Code 3, device not operational) is returned.

Program Generated Control and Status

The operational characteristics of the SCCU portion of the Configur-
ation Console, which primarily involve monitoring of the program
generated control and status, are described in the following sections.
Program generated information includes Subsystem Configuration Reg-
isters, Display Status and Check Register, and Audible Alarms. The
SCCU recognizes a single address hexadecimal (01) and allows appro-
priate programmed activity to occur. A Data Flow diagram for the SCCU
is shown in Figure 10-5.

Subsystem Configuration Registers

Three registers of indicators are provided on the operators panel
(refer to Figure 10-4) which may be program set to indicate those
elements which are interconnected into a system or subsystem. Space
has been provided to include additional system elements in each Con-
figuration Register, such as a 4th CE, 3rd IOCE, 5th SE, 5th DE and
3rd TCU.
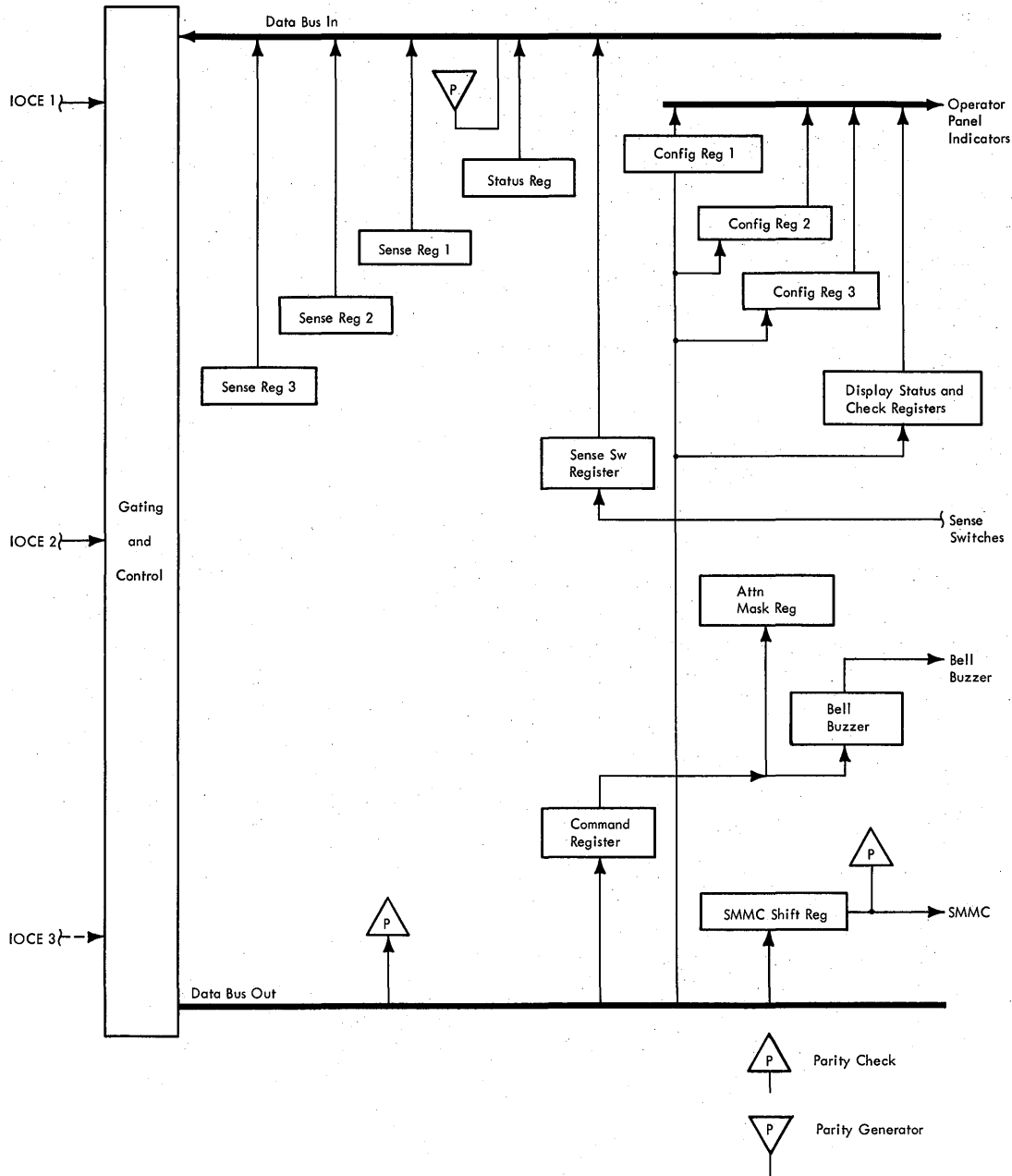
•Figure 10-5. SCCU Data Flow

The Configuration Registers are updated after the console has accepted its assigned address followed by a command byte and three data bytes per register. The command byte has the following format:

Bit Position          P 0 1 2 3 4 5 6 7
Command               P 0 0 0 0 0 0 0 1

The order of writing the Configuration Registers is 1, 2, 3; requiring three bytes of data from the IOCE for each register. The structure of the three data bytes in relation to the configuration register bit positions is as follows:

| DAU | RCU | TCU | DE | SE | CE | IOCE |
|-----|-----|-----|-----|-----|-----|------|
| 1 2 | 1 2 | 1 2 3 | 1 2 3 4 5 | 1 2 3 4 5 | 1 2 3 4 | 1 2 3 |
| 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 | | | | |
| BYTE 1 | BYTE 2 | BYTE 3 | | | | |

This format is for a maximum system and must be followed for all system configurations. Bit positions not installed, by an expansion feature are transferred but not indicated.

If more than one IOCE addresses the console simultaneously, the tie will be broken by appropriate circuits and the lowest (logically) numbered IOCE will be given priority. All other IOCE's receive Control Unit Busy (Condition Code 2).

Display Status and Check Indicator Registers

Six registers are provided on the Configuration console operators panel (refer to Figure 10-4) which may be program set to indicate Status and Check conditions for each of the Display Generators (DG) and Radar Keyboard Multiplexor (RKM) units. Space has been provided on the panel to expand from 12 DG's to 17 DG's and from 3 RKM's to 5 RKM's.

The Status and Check indicator registers are updated after the console has accepted its assigned address followed by a command byte and one data byte for each unit. In the event that more than one IOCE addresses the console simultaneously, the tie will be broken by appropriate circuits and the lowest (logically) numbered IOCE given priority. Other IOCE's will receive Control Unit Busy Status (Condition Code 2).

The Write Display Status command has the following format:

Bit Position          P 0 1 2 3 4 5 6 7
Command Code            0 0 0 0 0 1 0 1

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Once accepted the command will initiate data transfer from the IOCE
to the console. Each data byte contains the status and check inform-
ation for one unit as follows:

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ON LINE | STAND-BY | UN-AVAILABLE | MAINTEN-ANCE | POWER CHECK | LOGIC CHECK | NOT USED | NOT USED |

The order of writing the status and check registers is sequential by
unit with one byte per unit. The order is as follows:

         Bytes  1-12 - DG 1 through DG 12
         Bytes 13-15 - RKM 1 through RKM 3
        *Bytes 16-20 - DG 13 through DG 17
        *Bytes 21-22 - RKM 4 and RKM 5

          *Assigned for expanded version of the Configuration Console

Audible Alarms

Two audible alarms, a bell and buzzer, are provided in the Configur-
ation Console for operator attention. Operation of both alarms is
initiated by program control. The audible alarms are turned on after
the SCCU accepts its assigned address and a command byte transfer.
If two or more IOCE's address the SCCU simultaneously, the tie will
be broken by appropriate circuits and the IOCE with the lowest
(logical) number will be given priority. All others will receive
Control Unit Busy Status. The command byte has the following
binary configuration.

         Bit Position   P 0 1 2 3 4 5 6 7
         Bell Command   P 0 0 0 0 0 1 1 1

         Bit Position   P 0 1 2 3 4 5 6 7
         Buzzer Command P 0 0 0 0 1 0 1 1

If the buzzer or bell is sounding, and an IOCE addresses the console,
a busy indication will not be returned to the IOCE. The audible
alarms may be reset by depression of the applicable pushbutton on
Panel E, Figure 10-4.


Program Generated SMMC Messages and Controls

The SCCU provides a path from the IOCE multiplex channels to the
System Maintenance Monitor Console (SMMC). Data in the form of Unit
Status messages and various control lines may be transmitted to the
SMMC under program control. Operator requests from the SMMC are
accepted by the SCCU and sent to the appropriate IOCE.

Unit Status Messages

The transmission of Unit Status messages from the Configuration

Console to the SMMC is initiated by the acceptance of the SCCU address followed by a Write SMMC command from an IOCE. In the event more than one IOCE addresses the console simultaneously, the lowest (logically) numbered IOCE is given priority. Other IOCE's receive Control Unit Busy status (Condition Code 2).

The Write SMMC command has the following format:

```
Bit Position    P 0 1 2 3 4 5 6 7
Command Code      0 0 0 0 1 0 0 1
```

Each Unit Status message consists of two data bytes received from the IOCE in multi byte mode. One parity bit (odd parity) is generated by the console circuits based on the byte parity bits received from the IOCE. When a Unit Status Message has been assembled by the console, the CC to SMMC interface is activated and the message is transferred serially by bit to the SMMC. Upon completion of the transfer, another Unit Status message is requested from the IOCE.

The relationship between the Unit Status message format and the IOCE data bytes is as follows:

| UNIT STATUS MESSAGE | | |
|---|---|---|
| UNIT NUMBER | UNIT STATUS | P |
| 0 1 2 3 4 5 6 7 | 8 9 10 11 12 13 14 15 | 16 |
| 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 | |
| BYTE 1 | BYTE 2 | |

*NOTE: Reference applicable Interface Control Document for description of Unit Number and Unit Status bit assignments.

SMMC Control Commands

Two commands which are interpreted by the Configuration Console allow the 9020E System to inform the SMMC when conditions exist which may prevent proper operation of the CC or CC to SMMC interface. These commands, accepted by the Configuration Console after being addressed from an IOCE, cause a unique signal to be transmitted to the SMMC. In the event more than one IOCE addresses the console simultaneously, the tie will be broken by appropriate circuits and the lowest (logically) numbered IOCE given priority. Other IOCE's will receive Control Unit Busy (Condition Code 2).

The Control Help command has the following format:

```
Bit Position    P 0 1 2 3 4 5 6 7
Command Code      0 0 1 0 0 1 1 1
```

The Control Help command will cause the Help signal to be transmitted
to the SMMC.  The Help signal informs the operator at the SMMC that
a condition exists which requires manual intervention in order to
properly reconfigure the 9020E System or display subsystem.

The Control Fault command has the following format:

```
            Bit Position      P 0 1 2 3 4 5 6 7
            Command Code        0 1 1 0 1 1 1
```

The Control Fault command will cause a Fault signal to be transmitted
to the SMMC.  This signal will also be transmitted if SMMC Data Check
condition is detected by the Configuration Console.  The Fault Signal
persists until reset by depressing the Fault Reset pushbutton.

SMMC Operator Requests

The Configuration Console receives from the SMMC an Operator Request
signal via the CC to SMMC interface.  When this signal is activated
the console will generate Attention Status to an IOCE if enabled by
the system.  A command, Enable SMMC Request, is provided which
allows the 9020E System to control and route the SMMC requests to the
desired IOCE.

The enable SMMC Request command has the following format:

```
            Bit Position          P 0 1 2 3 4 5 6 7
                                    1 X X X 1 1 1 1

        Enable IOCE Number 1 ─────────┘ │ │
        Enable IOCE Number 2 ───────────┘ │
       *Enable IOCE Number 3 ─────────────┘
```

*Assigned for the expanded version of the CC.

When an IOCE enable bit position equals one, the IOCE bit in the
request mask register is set.  Only one IOCE mask bit may be set at
any time, or all bits may be turned off (Control Disable Request).
When set, an IOCE mask bit allows a SMMC request signal to be sent to
the associated IOCE as Attention Status.  When all bits are turned
off, Operator request signals are lost.

The Enable SMMC Request command is accepted by the SCCU after
acceptance of the assigned address.  In the event more than one IOCE
addresses the console simultaneously, the tie will be broken by
appropriate circuits and the lowest (logically) numbered IOCE given
priority.  Other IOCE's will receive Control Unit Busy (Condition
Code 2).

PROGRAMMERS NOTE:  Initial power on will set all bits in the IOCE
mask register to zero.

SMMC Interface General Characteristics

The SMMC Interface provides a data path from the 9020E System to the
System Maintenance Monitor Console for transmitting unit status in-
formation.  Data is transmitted serially by bit over one data line.

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Two eight bit bytes plus one parity bit makes up a unit status
message.  Parity of the 17 bits is odd.

Interface Lines.  The SMMC Interface consists of the following lines:

```
                           |————————————————— DATA ——————————————————►|
                           |                                           |
                           |————————————————— CLOCK —————————————————►|
                           |                                           |
                           |——————————————— TRANSFER ————————————————►|
CONFIGURATION              |                                           |  SMMC
                           |——————————————— DISABLED ————————————————►|
CONSOLE                    |                                           |
                           |————————————————— FAULT ——————————————————►|
                           |                                           |
                           |————————————————— HELP ———————————————————►|
                           |                                           |
                           |◄———————————————— REQUEST —————————————————|
                           |                                           |
                           |————————————————— INTERLOCK ———————————————|
                           |                                           |
                           |———————————— POWER MONITOR TRIPPED —————————|
                           |                                           |
                           |———————————— POWER MONITOR OVERRIDE ————————|
```
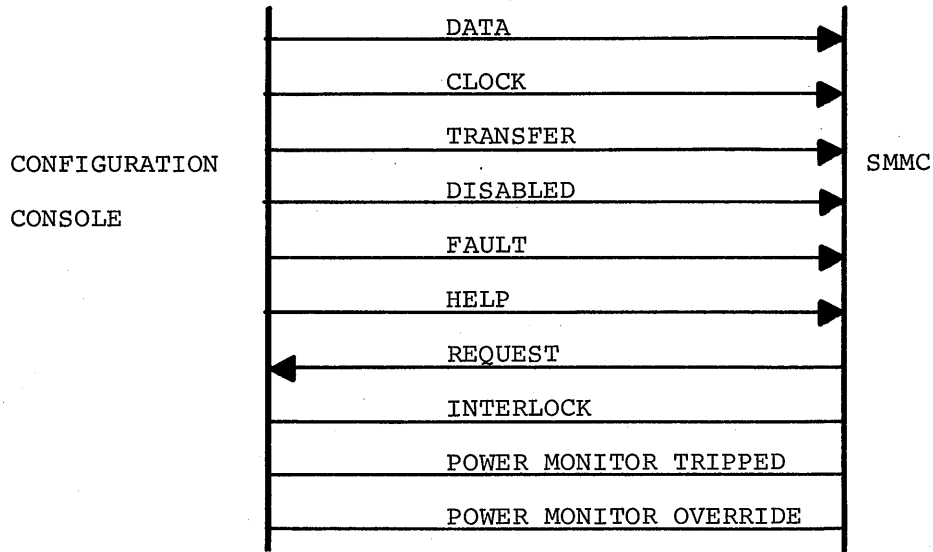
Data - This line transmits data serial by bit from the CC to the
SMMC.

Clock - This line is used to transmit 17 clock pulses at a 10KHz ± 10%
rate for each unit message.  The 10KHz signal is symmetrical i.e., up
for 50 usec ± 5.0 usec and down for 50 usec ± 5.0 usec.  The first
clock pulse starts one and one half clock cycles after the Transfer
Line is activated.

Transfer - This signal is raised when the CC has a message to trans-
mit to the SMMC, and dropped at the end of each message.

Disabled - This signal is a level which is activated when the SCCU is
in maintenance mode.

Fault - This line will be activated when a SMMC Data Check is detect-
ed within the CC or may be activated by a Control Immediate command
from the IOCE.  The Signal persists until manually reset at the CC
operators panel.

Help - This line will transmit a 1 usec ± 10% duration pulse to the
SMMC when a Control Immediate - Help - command is decoded by the SCCU.

Request - This signal originating from the SMMC is a pulse of 2 milli-
seconds minimum duration.  Upon receipt of this signal the SCCU will
generate Attention Status to the selected IOCE providing the Enable
Request Mask bit for that IOCE is set.

Interlock - This line informs the SMMC that the CC is attached. The CC will provide a jumper wire between the + signal line and - signal line.

Power Monitor Tripped - This line is not used by the 9020E System. The CC will insure the line is open circuited.

Power Monitor Override - This line is not used by the 9020E System. The CC will insure the line is open circuited.

Interface Operation, Data Transfer. Transfer of data takes place as shown in Figure 10-6. When the CC has 2 bytes of data to transmit, the first bit is placed on the Data Line coincident ± 1.0 usec with the rise of the Transfer Line. One and one-half clock cycles later the Clock line is enabled with a series of 17 clock pulses. The Data line is changed to the next bit at the fall of the Clock line ± 1.0 usec. One clock cycle after the fall of the Clock line for the 17th bit the transfer line will be dropped. The transfer line will remain down for a minimum of three clock cycles.

Electrical Characteristics. All signals between the CC and SMMC are carried by a 100 ohm balanced transmission system. The cable is an overall shielded cable containing multiple twisted pair conductors.

Line Driver - The output signals from the CC shall have the following specifications when a 100 ohm plus or minus 5% resistive terminator is connected between the + signal lead and the - signal lead at the CC output connector pins.

A logical one is represented by the + signal line being -1.6 volts (+0.3v, -0.7v) with respect to the -signal line. A logical zero is represented by the +signal line being +1.6 volts (-0.3v, +0.7v) with respect to the signal line. The + signal and -signal lines shall not exceed plus or minus 7.0 volts with respect to the CC signal ground (DC return) when measured at the CC output connector.

Rise and Fall times at the CC output connector shall not exceed 40ns (20% to 80% points) when measured from +signal or -signal line to ground. This measurement is made with no external cable attached and a termination resistor of 100 ohms ± 5% connected from the +signal line to -signal line.

Differential skew between + and - signal lines is defined as the time interval when the driver output is not in a definite state. The driver is in an indefinite state when the differential voltage between the + and - signal line is less than 1.3 volts. Differential skew will be 20ns or less at the driver output.

Driver Output - Driver output signals are measured at CC output connector with 100 ohm terminator from + signal to -signal with no cable attached.

Power off condition all drivers:

signal line differential voltage = 0.V ± 1.0 mv.

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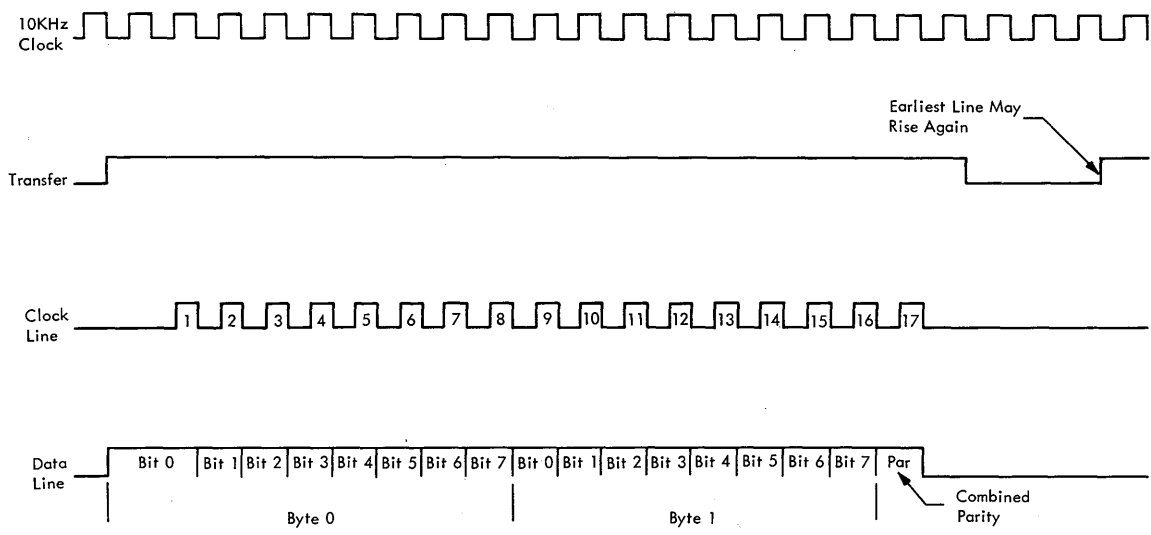
Figure 10-6.  SMMC Interface Timing

<pre>
                         LOGICAL ZERO

+ Signal line           Max Level                    +2.3v ───┐
                                                              │
Voltage measured        Nominal Level                +1.6v ──┤
                                                              │
in reference to         Min Level                    +1.3v ──┤
                                                              │
- Signal line                                                 │
                                                              │
                                     Ref. (-Signal Line)───└──

                         LOGICAL ONE

                                     Ref. (-Signal Line)───┌──
                                                           │
+ Signal Line           Min Level                    -1.3v ──┤
                                                           │
voltage measured        Nominal Level                -1.6v ──┤
                                                           │
in reference to the     Max Level                    -2.3v ──┘

- Signal line
</pre>
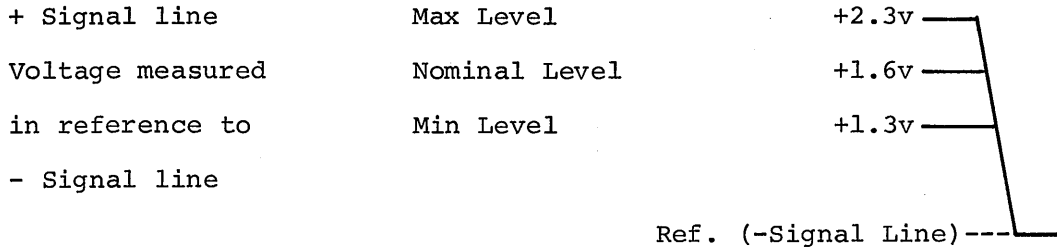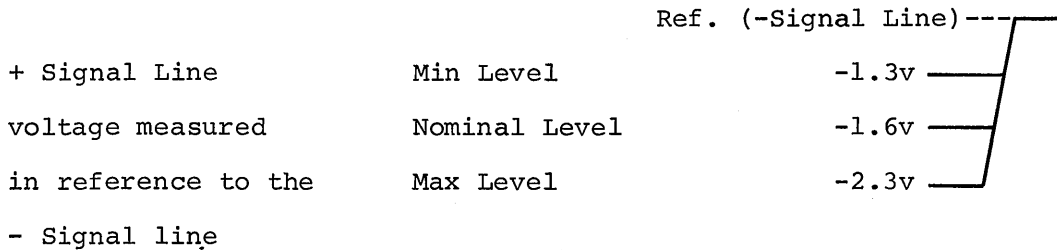
Line Receiver - The characteristic impedance between the + signal
and -signal lines at the input connector to the CC shall be 100 ohms
± 5%.  A logical zero is represented by the + signal line being equal
to or greater than +0.6v volts in respect to the - signal line when
measured at the receiver input.  A logical one is represented by the
+ signal line being equal to or greater than -0.6v volts in respect
to the - signal line when measured at the receiver input.  The +
signal and - signal line shall each remain between +3 volts and
Unit Signal ground (DC return).

Receiver Input Requirements -

<pre>
                         LOGICAL ZERO

+ Signal Line           Max Level                    +3.0v ──┐
                                                             │
Voltage measured        Min Level                    +0.6v ──┤
                                                             │
in reference to                                              │
-Signal Line                        Ref. (-Signal)──────────└──

                         LOGICAL ONE

+Signal Line                        Ref. (-Signal)──────────┌──
                                                            │
Voltage measured in                                         │
                                                            │
reference to the        Min Level                    -0.6v ──┤
                                                            │
-Signal Line            Max Level                    -3.0v ──┘
</pre>

## Fault Conditions

1. A grounded signal line must not damage drivers, receivers, or terminators.

2. Both lines shorted together must not damage drivers, receivers, or terminators.

3. An open line or terminator must not damage the driver or receiver circuit. (This condition may result in one signal line rising to 7.0 volts with respect to signal ground).

4. Power down at the driver may cause a condition at the receiver which could allow small noise signals to switch the receiver circuit. The CC will provide facilities for degating receiver outputs where needed to prevent erroneous system interruption.

5. A receiver which is not connected to a driver circuit must not generate spurious signals.

6. Changing power status (normal power on or off) shall not propagate signals over the interface.

Cabling. Cables must meet the defined following specifications and must utilize standard Serpent type connectors at the CC end.

Characteristic Impedance = 95 ohms
Resistance DC           = .019 ohms/conductor/ft.
TPD Propagation Delay   = 1.5 ± .05 ns/ft.
△ Tpd                   = .02 ns/ft.
**Attenuation**         = 2.1 db/100 ft. at 4 MHz

Cable and connector requirement at the CC are as follows:

10 signals              1 - 24 Pin Serpent

**Refer to Table 10-2 for connector pin assignments.**

Serpent Connector Blocks - All serpent connectors used in the CC will be type A connectors. These must be mated with a type B connector on the external cable. Serpent contact termination to termination contact resistance (includes 2 crimps and mated contacts) will not exceed:

.020 ohms when used with #22 wire or larger
.030 ohms when used with #24 or #26 wire

External Cable Length - The maximum external cable length is 300 feet connector to connector (5 feet is used within the CC).

## SCCU Status Information

The status byte used for the SCCU is transferred to the channel in the following situations:

1. During initial selection.
2. At the termination of a command.
3. When permitted to present stacked status.
4. To present Attention signal to the channel.
5. To present Control Unit End to the channel.

The status byte has the following format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Attention |
| 1 | Status Modifier |
| 2 | Control Unit End |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Not Used |

The following status bit combinations are used by the SCCU:

| Bit Position 0 1 2 3 4 5 6 7 | Use |
|-----|-----|
| 0 0 0 0 1 1 0 0 | Channel End, Device End |
| 0 0 0 0 1 1 1 0 | Channel End, Device End, Unit Check |
| 1 0 0 0 0 0 0 0 | Attention |
| 0 1 0 1 0 0 0 0 | Status Modifier, Busy |
| 0 0 1 0 0 0 0 0 | Control Unit End |
| 0 0 0 0 0 0 1 0 | Unit Check |

Channel End, Device End - This bit configuration is generated as a
normal ending status or as a result of a Halt I/O when busy and no
check conditions exist.

Channel End, Device End, Unit Check - This bit configuration is gen-
erated under the following conditions.

1. When a Bus Out Check condition is detected on a data byte
   transfer.
2. When a Data Check condition is detected on transfer to
   the SMMC.
3. When an odd number of bytes is specified by the programmer
   for a Write SMMC command.

Attention - This status condition is generated when a Request signal
is received from the SMMC and the following conditions are met:

1. The Enable Request command has been issued.
2. An initial selection sequence is not in process.
3. Command chaining is not indicated.
4. Status is not stacked.
5. The SCCU is not busy.

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Table 10-2.   CC to SMMC Pin Assignments

01S-A5A

| B02 | – SMMC Data | D02 | + SMMC Data |
|-----|-------------|-----|-------------|
| B03 | + SMMC Clock | D03 | Not used |
| B04 | – SMMC Clock | D04 | – Transfer |
| B05 | + Disabled | D05 | + Transfer |
| B06 | Not used | D06 | – Fault |
| B07 | – Disabled | D07 | + Fault |
| B08 | + Help | D08 | Ground Return |
| B09 | – Help | D09 | – SMMC Request |
| B10 | + Interlock | D10 | + SMMC Request |
| B11 | Not used | D11 | – Power Monitor Tripped (Not used) |
| B12 | – Interlock | D12 | + Power Monitor Tripped (Not used) |
| B13 | + Power Monitor Override (Not used) | D13 | – Power Monitor Override (Not used) |

Status Modifier, Busy - This configuration is generated in response to initial selection from an IOCE when the SCCU is busy with another IOCE.

Control Unit End - This status condition is generated when the SCCU has previously returned a Busy status to an IOCE and is now indicating that it is no longer busy.

Unit Check - This configuration is generated during the initial selection cycle when a Bus Out Check or Command Reject condition occurs.

The status bits are reset when the status byte has been accepted by the channel.

SCCU Sense Information

A Sense command should be executed when the Unit Check bit in the status byte is set in order to determine the type of equipment or programming check associated with the previous command. The sense register is reset by the acceptance of the next Valid Read, Write or Control (except Control NOP) command from the associated IOCE. The sense bits except for bit 2, Bus Out Check, are also reset when a Bus Out Check occurs during an initial selection cycle. The sense bits except for bit 0 (Command Reject) are also reset whenever Command Reject occurs.

The sense byte for the SCCU has the following format:

| Bit | Designation |
|-----|-------------|
| P | Parity |
| 0 | Command Reject |
| 1 | Not Used |
| 2 | Bus Out Check |
| 3 | Not Used |
| 4 | Data Check |
| 5 | Not Used |
| 6 | Not Used |
| 7 | Wrong Length Message |

Sense Bit 0 - Command Reject - Command Reject is set during the initial selection phase of a command if the bit configuration with correct parity is other than those listed as valid commands for the SCCU. Unit Check is set in the status byte and the command is ignored. All other sense bits are reset.

Sense Bit 2 - Bus Out Check - Bus Out Check will be set if a parity error is detected by the SCCU during the initial selection or during a data transfer operation. If the condition occurs during initial selection, the sense register is cleared (except for Bus Out Check). During data transfer, a Bus Out Check terminates the operation and sets Unit Check in the status byte.

Sense Bit 4 - Data Check - Data Check is set when the SCCU determines that the data received from the IOCE had correct parity and the resulting data transmitted to the SMMC had incorrect parity. A Data Check condition terminates the operation and sets Unit Check in the status byte for presentation during the termination cycle.

Sense Bit 7 - Wrong Length Message - A Wrong Length Message (WLM) condition results when the programmer specifies an odd number of bytes for transmission to the SMMC. When the SCCU requests a unit status message (two bytes) from the IOCE and only one byte is received, the WLM Sense bit is set. The operation is immediately terminated with Channel End, Device End and Unit Check Status. The last byte is not transmitted to the SMMC.

CONSOLE INDICATORS, KEYS AND SWITCHES

This section describes the indicators, keys, and switches located on the Operator's Panel of the Configuration Console to monitor and control the IBM 9020E System. In addition to the functional components, the controls and switches for console test operations are positioned on the panel. The Lamp Test controls, may be used by the operator to check the panel for indicator faults. Components should be replaced by qualified maintenance personnel. Power control, and Power indicators will be described in the 'Power Control and Indicator' Section.

| Name | Implementation |
|------|----------------|
| DCP Unit Status | Indicators |
| DCP Unit Alarms | Indicators |
| Configuration Registers | Indicators |
| Display Unit Status | Indicators |
| Display Unit Alarms | Indicators |
| **Storage Data (SD)** | Indicators |
| Instruction Address (IA) | Indicators |
| Manual Status (CE) | Indicators |
| Wait Status (CE) | Indicators |
| Invalid Selection | Indicator |
| System Console Test Mode | Indicator |
| I/O Interface Disabled | Indicator |
| System Interlock | Indicator |
| Reader/Punch-Printer Select | Rotary Switch |
| Reader/Punch-Printer Enable | Pushbutton Switch-Indicator |
| Control CE | Lever Switches |
| Control CE Activate | Pushbutton Switch |
| Storage Data | Lever Switches |
| Sense | Lever Switches |
| Instruction Address | Lever Switches |
| Storage Select | Lever Switch |
| Address Compare | Rotary Switch |
| Address Compare Enable | Pushbutton Switch |
| Rate | Rotary Switch |
| Start | Pushbutton Switch |
| Console Reset | Pushbutton Switch |
| Fault Reset | Pushbutton Switch |

| Name | Implementation |
|------|----------------|
| Buzzer Bell Reset | Pushbutton Switch |
| Set IC | Pushbutton Switch |
| Store | Pushbutton Switch |
| Display | Pushbutton Switch |
| Stop | Pushbutton Switch |
| All Stop | Pushbutton Switch |
| Main Storage Select | Rotary Switch |
| Computing Element Select | Rotary Switch |
| Load Unit | Rotary Switches |
| Load | Pushbutton Switch-Indicator |
| Enable System IPL | Pushbutton Switch |
| Interrupt | Pushbutton Switch |
| System Interlock | Key Operated Switch |
| Lamp Test Select | Rotary Switch |
| Lamp Test | Pushbutton Switch |
| I/O Interface Enable-Disable | Toggle Switch |

## Console Indicators

Indicators are provided on the Configuration Console operator's panel for display of 9020E System and display subsystem status and Fault information, Subsystem Configurations, and other registers for control of a selected Computing Element.

### 9020E State Indicators

Four indicators for each CE, SE, DE, IOCE, TCU, RCU, and DAU are provided on the Configuration Console operators panel (Figure 10-4) to indicate Unit Status. Space is provided to also display Unit Status for additional system elements such as a 4th CE, 3rd IOCE, 5th SE, 5th DE, or 3rd TCU.

Each element or unit decodes its own Status and turns on one (and only one) of four indicators designated State Three, State Two, State One and State Zero. When an element or unit has power off, no indicator for it is turned on.

State Three - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Three.

State Two - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Two.

State One - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State One.

State Zero - This indicator shall be turned on when the "state bits" of the respective system element are decoded to be in State Zero.

### 9020E Unit Alarm Indicators

There are two alarm indicators on the System Console for each CE, IOCE, SE, DE, TCU, RCU, and DAU.

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Power Check - This indicator is turned on by the respective element or unit whenever one or more of the following conditions exist in the element:

1. Catastrophic Power Supply Failure
2. Over Temperature
3. Normal Power Off

The indicator shall be turned on by +24v dc from the failing element. The Power Check light shall function regardless of the SCCU power status except during Emergency Power Off.

Logic Check - This indicator is turned on by the respective element or unit when a logic check condition is detected. In addition, each CE will turn on its console logic check indicator when even parity is transferred from the Configuration Console to the selected Computing Element.

Display Subsystem Status Indicators.

Four indicators for each Display Generator and Radar Keyboard Multiplexor are provided on the Configuration Console operator's panel. Space is provided for expansion from 12 DG's to 17 DG's and from 3 RKM's to 5 RKM's.

These indicator registers may be program set; for example when a change in unit status is made. A DG or RKM may be placed in one or more of the following status conditions.

ON - Line
Stand-by
Unavailable
Maintenance

Display Subsystem Unit Alarm Indicators.

Two indicators for each Display Generator and Radar Keyboard Multiplexor are provided on the Configuration Console for indication of Check conditions. Space is provided for expansion from 12 DG's to 17 DG's and from 3 RKM's to 5 RKM's.

These indicator registers are program set when desired to indicate a check condition.

Logic Check - This indicator is turned on by program means when a logic check condition is indicated to the program. These conditions are reported to the 9020E System through the Reconfiguration Control Unit.

Power Check - This indicator is turned on by program means when a power fault is detected and reported to the 9020E System via the Reconfiguration Control Unit.

Configuration Indicator Registers - Three indicator registers, designated 1, 2, and 3, are provided to display system configuration for

each CE, IOCE, SE, DE, TCU, RCU and DAU.  The indicators are turned
on under program control (Configuration Indicator Registers Section)
and remain on until updated by the program or turned off by depress-
ing the Console Reset pushbutton.

Storage Data (SD) - Is a register consisting of 36 indicators to
display the contents of the selected storage word as specified in
the Storage Modification or Display Section.  Parity of the indi-
cators is not checked at the console.

Instruction Address (IA) - The IA for each Computing Element is pro-
vided on the console to continually display the contents of the
respective Instruction Counter.  Each register contains 27 indicators
to indicate IC contents.  Parity of the indicators is not checked at
the console.  Additional space has been provided on the console
to add a fourth row of IA indicators for a fourth CE.

Manual Status Indicators

The Manual Status indicator, which exists on each of the Computing
Elements, is duplicated on the console.  This indicator is turned on
when the element is in the Stopped state.  Additional space has been
provided to add a fourth CE Manual Status indicator.

Wait Status Indicators

The Wait Status Indicator, which exists on each of the Computing
Elements is duplicated on the console.  This indicator is turned on
when the Computing Element's Wait bit in the PSW is set to one.
Additional space has been provided to add a fourth CE Wait Status
indicator.

Invalid Selection Indicator

This indicator is turned on by the selected CE whenever an invalid
storage address is specified by the operator during a manual inter-
vention.

SCCU Test Mode Indicator

This indicator is turned on by the Test-Operate switch located on
the SCCU maintenance and test panel to inform the operator that the
test panel controls are operable.  The indicator is turned off when
the Test-Operate switch is positioned to Operate.

I/O Interface Disabled Indicators

SCCU Interface Disabled Indicator - This green indicator is turned on
when the SCCU I/O Interface Enable-Disable switch is placed in the
Disable position and the SCCU and 2821 control units have been logic-
ally disconnected from all interconnected IOCE.  When this indicator
is on the Power On-Off switch and/or Power Supply switch may be
operated without causing interference on the IOCE interfaces.

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RCU Interface Disabled Indicators - This green indicator is turned on when the associated RCU I/O Interface Enable-Disable switch is placed in the Disable position and the RCU has been logically disconnected from the IOCE.

Systems Interlock Indicator - This indicator is turned on any time the System Interlock key switch is turned on.

Console Keys and Switches

The Address Compare, Storage Data Keys, Address Keys, Storage Select, Control CE, and IPL controls are protected against accidental operator use by interlocking the activating control pushbutton with the System Interlock Switch.  Certain RCU switch funcitons are enabled only when the RCU is in State Zero with the Test switch on.  Table 10-3 defines the console switch interlocking.

Table 10-3.  Configuration Console Switch Interlocking.

| Always Enabled | Under System Interlock Switch Control | Enabled Only In RCU State Zero (Test) |
|---|---|---|
| Emergency Pull (9020 System) | Control CE Activate | Power On/Off (RCU) |
| Element Master Power Off Pull | CE Select | I/O Interface Enable-Disable (RCU) |
| Power On/Off (SCCU) | Address Compare Enable | |
| Thermal Reset | Start | |
| Power B & C | Set IC | |
| Reader/Punch-Printer Select | Store | |
| Reader/Punch-Printer Enable | Display | |
| Buzzer Bell Reset | Stop | |
| Fault Reset | All Stop | |
| Console Reset | Interrupt | |
| Lamp Test | Load | |
| Sense Switches | Rate | |
| I/O Interface Enable-Disable (SCCU) | | |

Initial Program Load Switches

The switches described in this section are primarily used when performing a system or subsystem IPL.

Computing Element Select - This three position rotary switch will
send a Select signal to a selected Computing Element.  The System
Interlock switch must be turned on for this switch to be enabled.
The switch has the capability of being expanded to select a fourth
CE when required.

Main Storage Select - This rotary switch is used to select the Main
Storage Element for IPL.  The output signal levels from this switch
are binary, with odd parity assigned at the console.  This switch has
the capability to select up to five storage elements when future ex-
pansion requires it.

Load Unit - Three hexadecimal rotary type switches are used to select
the channel address and I/O unit addresses.

    Channel Address - This rotary switch designates the data path
input to each IOCE during Initial Program Load.  The switch is
numbered (0) through (A).  The output signal levels from this switch
are binary, and odd parity assigned at the Configuration Console.

    Unit Address - Two rotary switches are provided to select a
total of 256 unique I/O unit addresses during Initial Program Load.
Each switch is numbered (0) through (F).  The output signal levels
from each switch are binary and common odd parity (i.e., for both
switches), is assigned at the Configuration Console.

Enable System IPL - This pushbutton switch allows the operator to
designate a System IPL by holding this switch depressed while press-
ing the Load pushbutton.  When this switch is not depressed, a sub-
system IPL will be performed when the Load pushbutton is depressed,
provided the selected CE is in State One or State Zero with the Test
switch off.

Load - Depression of the Load pushbutton will generate a signal to
enable the IPL switch settings (Load Unit switches and Main Storage
Select) to the selected Computing Element.  When the load operation
starts, the Computing Element will turn the Load pushbutton indicator
on.  When the IPL operation is complete, the selected Computing
Element will turn the Load indicator off.  The System Interlock
switch must be on for this button to be enabled.

System Interlock - The System Interlock is a two position On/Off
switch.  A key is inserted to turn the switch On and may not be
extracted until the switch is turned off.

    The System Interlock will enable the console manual controls as
defined in **Table 10-3**.

Data and Address Keys

Storage Data Keys - Thirty-two Storage Data Keys are provided on the
Configuration Console to allow manual data generation for transfer
into any program addressable word of Local  Storage, Main Storage or
Display Storage.  The console automatically assigns odd byte parity
to the data, which will be checked at the selected Computing Element.

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Instruction Address Keys - Twenty-four Instruction Address Keys (referred to as Address Keys) are provided on the Configuration Console to enable addressing of any addressable Local Storage, Main Storage, or Display Storage location. The console automatically assigns odd byte parity to the address which will be checked at the selected Computing Element.

Sense Switches - Six switches on the console are provided for program sense switch operations. The contents of the switches are transferred with odd parity when the SCCU recognizes the specified Read Sense Switch command byte (Sense Switch Entry Section).

Computing Element Control Switches

The switches described in this section are used by the operator to perform various operations with a selected CE. In general, these switches perform the associated function in the CE selected by the CE Select Switch.

Interrupt - Depression of the Interrupt pushbutton causes a Console Interrupt signal which sets bit 25 of the PSW in the selected Computing Element. The System Interlock switch must be on for this switch to be enabled.

Set IC - Depression of the Set IC pushbutton in the stopped state transfers the contents of the 24 Address Keys (plus odd byte parity) into the selected Computing Element's Instruction Counter. The System Interlock Switch must be turned on for this switch to be enabled.

Store - Depression of the Store pushbutton when the selected CE is in the stopped state causes the contents of the 32 Storage Data Keys (plus odd byte parity) to be placed into the storage word as specified by the 24 Address Keys and the Storage Select switch. The System Interlock switch must be turned on for this switch to be enabled.

Display - Depression of the Display pushbutton when the selected CE is in the Stopped state causes the selected Computing Element to place the contents of the storage word specified by the Address Keys and the Storage Select switch into the Console's Storage Data Indicators. The System Interlock switch must be turned on for this switch to be enabled.

Stop - Depression of the Stop pushbutton will cause the selected CE to be placed in the Stopped state without destroying the Computing Element's environmental status. The selected Computing Element will proceed to the end of the current instruction being executed at the time the stop is initiated.

If the current instruction causes a program interruption, the change of program status words (PSW) will be accomplished before stopping. An I/O device will be allowed to complete its operation, although I/O or external interruptions will not be recognized. The System Interlock switch must be turned on for this switch to be

enabled.

All Stop - Depression of this pushbutton with the System Interlock switch turned on causes all Computing Elements to enter the stopped state at the completion of their current instructions as defined above for stop.

Rate - The Rate switch is a two position switch which operates in conjunction with the Computing Element Select switch, Start and Stop pushbuttons, and System Interlock switch. The Stop pushbutton must be depressed before putting the Rate switch in the Instruction Step position. The positions of the switch are:

1. PROCESS
2. INSTRUCTION STEP

In the PROCESS position, the selected Computing Element will operate at normal clock speed when the Start pushbutton is depressed. In the INSTRUCTION STEP position, each depression of the Start push- button results in one complete instruction being executed. Any machine instruction can be executed in this mode.

When the Rate switch is set to the Instruction Step position and an interruption occurs, no action will take place until the Start button is depressed. Then the interruption will be serviced; that is, the PSW's will be exchanged and the first instruction in the interruption handling routine will be executed. If the CE happens to be in the process of executing an instruction when an interruption occurs, the instruction will be completed and the CE will wait for the next depression of the Start pushbutton to service the interruption. The stop at the end of each instruction execution will be identical to that achieved by the Stop button.

Start - Depression of the Start pushbutton with the System Interlock switch turned on will start the selected Computing Element. If Start is activated after normal stop, it will cause the continuation of instruction processing as if no stop had occurred.

Address Compare - The Address Compare switch is a three position switch which operates in conjunction with the Computing Element Select switch, Address Keys, Storage Data Keys, System Interlock switch, and Address Compare Enable pushbutton. The positions of the switch are:

1. STOP
2. PROCESS
3. LOOP

In the STOP position, any memory access by the selected Computing Element to the address specified in the Address Keys causes that Computing Element to enter the Stopped State at the end of the instruction that made the storage reference.

In the PROCESS position, normal processing functions of the Computing Elements are performed. This is the normal position for the Address Compare switch. In all other positions, the System Interlock switch must be turned on and the enable pushbutton depressed.

The LOOP position of the Address Compare switch, coupled with the use of the Storage Data, IA Keys and the Enable pushbutton, allows an instruction or set of instructions to be repeated continuously by the selected CE until there is manual intervention. The instruction(s) can be executed at normal speeds or single stepped. The bounds of the loop are defined by the addresses set in the Storage Data and IA Keys. Some care must be exercised, since a branch instruction in the set of instructions within the loop can make the loop much larger than contemplated.

Address Compare Enable - Depression of the Enable pushbutton with the System Interlock switch turned on enables the Address Compare switch in the STOP and LOOP positions. Release of the Enable pushbutton has the effect of placing the Address Compare switch in the PROCESS position.

Control CE Switches - Three switches are provided to modify the three SCON bits in the CCR of the selected CE. Each switch modifies the corresponding SCON bit when the Activate pushbutton is depressed (Refer to Modification of CE Configuration Registers). Additional space has been provided to expand to a 4th Control CE switch. The State Bits of the Selected CE are reset to 00.

Control CE Activate Pushbutton - Depression of this pushbutton transfers the contents of the Control CE switches to the SCON bits in the configuration register of the selected CE and resets the State bits to 0,0. The System Interlock switch must be turned on to enable this pushbutton.

Storage Select Switch - The Storage Select switch is a two position switch which will select the storage area to be addressed by the Address keys:

1. Center Position - Main Storage or Display Storage
2. Down Position - Local Storage (in the selected CE).

Configuration Console Control Switches

This section describes those switches associated with the system console portion of the Configuration Console.

Console Reset - Depression of the Console Reset pushbutton resets all System Console logical functions. The 9020E unit status and alarm indicators are not affected.

Fault Reset - Depression of the Fault Reset pushbutton will turn off the SMMC Fault signal.

Buzzer Bell Reset - Depression of the Buzzer Bell Reset pushbutton resets both the buzzer and bell audible alarms.

Lamp Test - Two lamp test controls are provided on the console to permit the operator to test the operator's panel indicators.

Lamp Test Pushbutton- Depression of the Lamp Test pushbutton turns on all status, register, and control indicators on the opeator's panel.

Lamp Test Rotary Select - Rotation of this selection switch will test the following indicators: Load, Invalid Selection, Test Mode Enable and System Interlock.

Reader/Punch-Printer Select Switch - This switch permits selection of IOCE interfaces designated 1 or 2 for interconnection of the Reader/Punch-Printer to the selected interface via the IBM 2821 Control Unit. Expansion capability for a third IOCE interface is provided.

Reader/Punch-Printer Enable Switch-Indicator - Depression of the Enable pushbutton will condition the I/O selection designated by the Select switch. The indicator will be turned on at the completion of the switching operation and remain on as long as the Select switch remains in this position. The indicator will turn off if the select switch is repositioned to select another interface. The indicator will be turned on if either the Enable pushbutton is depressed or the Select switch is returned to the initial selected position.

SCCU I/O Interface Enable-Disable Switch - This switch provides the capability of logically disconnecting the SCCU and 2821 control unit from the IOCE's. This function is used when it is necessary to change power status, either on, off or switching to the other set of duplexed power supplies.

When placed in the Disable position this toggle switch causes the System Console Control unit and 2821 Control unit to logically disconnect from the IOCE's. The control unit(s) complete any operation in process prior to disconnecting. When the disconnect has been completed for all IOCE's, the Disabled indicator is turned on. If an IOCE attempts to select the Console Control unit or the Reader/Punch-Printer while the disabled indicator is on, the Select In signal (Condition Code 3 device not operational) is returned to the IOCE. When disabled, the indicator behind the I/O Select Enable pushbutton is turned off.

RCU I/O Interface Enable-Disable Switch - These switches provide the capability of logically disconnecting the associated RCU from the IOCE multiplexor channels. The switch which is enabled only when the RCU is in State Zero, causes the RCU to logically disconnect from the channel when placed in the Disable position. Any operation in process is completed prior to disconnecting and the Disabled indicator is then turned on. When Disabled, a selection attempt by an IOCE results in Condition Code 3 (device not operational). The

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RCU power may be turned off when Disabled.

When the switch is placed in the Enable position, the RCU is logically connected to the configured IOCE channel and the Disabled indicator is turned off.

RECONFIGURATION FUNCTION

The second major function of the Configuration Console is to provide configuration paths to the Display Generators, Radar Keyboard Multiplexors and the IBM 2701 Display Adapter Units. In addition, status and fault information is received from the DG and RKM units and returned to the 9020E System.

General Characteristics

The reconfiguration function is provided by two (duplexed) Reconfiguration Control Units (RCU). Each RCU is physically located on an individual logic gate, has its own independent power system and maintenance panel. Each RCU is functionally identical and either may perform the entire active system reconfiguration and Fault reporting task.

In general, one RCU is assigned the active system task while the other RCU is redundant, and may be utilized in another subsystem to perform test on non-active units. The redundant RCU may also be tested by a maintenance subsystem utilizing built-in program test capabilities.

The RCU assigned to the active system may control the communication paths from the display units to both RCU's; thus establishing which units communicate with the redundant RCU as well as the active RCU. A display unit may communicate with one RCU at a time.

Functional Characteristics

Since each RCU is functionally identical, the characteristics will be discussed as a singular unit and only where necessary for clarity will the relationship between the duplex units be noted.

The RCU is a multi-device Control Unit which interprets IOCE commands and sequences and controls appropriate signals to the display units and the IBM 2701 DAUs. In addition, fault reporting signals from the display units are scanned and reported to the 9020E System through the RCU to the IOCE.

The RCU attaches to two IOCE multiplexor channels (expandable to three IOCE's). IOCE connections are established by the controlling CE through the use of the SCON instruction which loads the Configuration Control Register (CCR) in the RCU. State bits, IOCE communication bits, and CE SCON mask bits are received from the CE when a SCON instruction is performed which selects a RCU. The IOCE communication bits establish which IOCE may communicate with the RCU. Only one IOCE may be enabled to a RCU at a time. The state bits establish The operational state of the RCU and exercise some control of the

RCU hardware.

Information transfer from and to the DGs and RKMs is via a standard Configuration Interface (CI). The RCU provides 17 CIs (expandable to 25) for connection of the following units.

|                             | Base | Expansion |
|-----------------------------|------|-----------|
| Display Generators          | 12   | 17        |
| Radar Keyboard Multiplexors | 3    | 5         |
| RKM/R Console               | 2    | 3         |

Addressing

The 17 Configuration Interfaces and the two IBM (2701) DAUs are each individually addressed as a device. The RCU has fixed device addresses within two sequential sets of control unit addresses.

| Address Bit Position | 0 1 2 3 | 4 5 6 7 |
|---|---|---|
| Set 1 | X X X 0 | |
| Set 2 | X X X 1 | |
| | Control Unit Address | Device Address |

The bit positions 0, 1, and 2 are assigned in the RCU by address jumper cards. The cards provide a simple means of changing the control unit address assignments within system limitations.

Control Unit addresses for each RCU may be assigned the same binary configuration. The RCU is then transparent to the program i.e., DG-1 is always addressed with the same address regardless of the RCU path assigned. This method of addressing assumes that the two RCUs are not both configured to the same IOCE multiplexor channel.

The addresses assigned to each RCU for the 9020E System are shown in Figure 10-7. Hexadecimal addresses 34 through 3B are provided only when the 90 Console Expansion Feature is installed.

Configuration Control

Configuration Control of the RCU is accomplished by two levels of control.

1. RCU to IOCE configuration.
2. RCU to DG and RKM configuration.

The RCU to IOCE configuration is established by the use of the SCON instruction in the controlling CE and utilizes the direct configuration control connection of the RCU to each of the three CEs (expandable to four).

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| DEVICE | HEX ADDRESS | BINARY ADDRESS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| DG-1 | 21 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| DG-2 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| DG-3 | 23 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| DG-4 | 24 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| DG-5 | 25 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| DG-6 | 26 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| DG-7 | 27 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| DG-8 | 28 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| DG-9 | 29 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| DG-10 | 2A | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| DG-11 | 2B | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| DG-12 | 2C | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| RKM-1 | 2D | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| RKM-2 | 2E | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| RKM-3 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| RKM/R CONSOLE-1 | 30 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| RKM/R CONSOLE-2 | 31 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| DAU-1 | 32 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| DAU-2 | 33 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| DG-13 | 34 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| DG-14       RESERVED | 35 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| DG-15          FOR | 36 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| DG-16       EXPANSION | 37 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| DG-17 | 38 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| RKM-4 | 39 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| RKM-5 | 3A | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| RKM/R CONSOLE-3 | 3B | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |

NOTE:   The term RKM/R Console represents a configuration
        interface to the active RKM.   The RKM/R Console
        interface is used to transfer data which configures
        up to 32 radar consoles to either the active or
        spare RKM.

Figure 10-7.   RCU Addressing

The outboard configuration (RCU to DG and RKM) is set by I/O commands via the IOCE multiplexor channel and is designed to be controlled by the active system for both RCU's. This second level of configuration control is dependent on the first level, i.e., the degree of control allowed by the second level is dependent upon the RCU state and IOCE communication paths established by the RCU to IOCE configuration. The outboard configuration (RCU to DAU) is controlled exclusively by the state of the RCU. The DAUs are configured to the RCU which is in State 3, insuring "Active" system control of DAU configuration.

RCU to IOCE Configuration - Each RCU has been provided with a Configuration Control Register (CCR) whose contents designate from which CE the RCU may accept configuration mask bits, with which IOCE the RCU may exchange data and control information, and which of the four unit states the RCU is to assume. The bit assignments for the CCR are defined in Figure 10-8.

The CCR is loaded by means of the Set Configuration (SCON) instruction. Refer to IBM 9020D and 9020E Systems Principles of Operation, Chapter 8.

The design of the RCU's allow the Executive Control Program to control dual data paths through the duplex RCUs. One RCU is normally assigned to active-system task by setting the state bits to 11 (State 3) and the appropriate IOCE communication bits to allow communication with the active IOCE. The second RCU is assigned either State 2, 1, or 0 and communicates with the redundant IOCE. When in State 2 or 1 the redundant RCU provides a path to those DG and RKM units not assigned to the active system (this assignment is determined by the active RCU to DG and RKM configuration). When in State 0 (not test) the redundant RCU may be program checked using diagnostic facilities and is recallable by the active system if required.

RCU to DG and RKM Configuration. The connections between the RCU and DG and RKMs is established by the Enable Communications I/O command addressed to the device to be configured. Communication may be enabled or disabled as desired and no action is taken at the device as a result of this command.

The Enable Communication command is accepted by an RCU only if the RCU is in State Three, or State Zero (Refer to Table 10-4). In other states, Unit Exception status is returned during the initial selection sequence and no action is taken as a result of this command. When accepted, the command either sets or resets a communication bit in the RCU for the addressed device (Bit is set to enable and reset to disable).

The communications bits in the RCU control the connections between each DG and RKM and the duplex RCU's. The "State" of the RCU is used to determine the degree of control allowed by the communications bits in each RCU. Table 10-4 shows the various combinations of states and resulting control by the communication bits.

| | STATE | | SCON | | | | | IOCE | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $P_0$ | $S_0$ | $S_1$ | 1 | 2 | 3 | 4 | $P_3$ | 1 | 2 | 3 |

$P_0$- Establishes "Odd" parity for the com-
bined State and Scon bits.

$S_0,S_1$- Specify the "State" the RCU is to
assume.

| $S_0$ | $S_1$ | STATE |
|---|---|---|
| 1 | 1 | THREE |
| 1 | 0 | TWO |
| 0 | 1 | ONE |
| 0 | 0 | ZERO |

SCON- A "1"in any of these bits indicates
that the RCU may accept configuration
control information from the CE with
the corresponding number. If this
field contains no "1s", the RCU will
accept SCON from any CE when in state
1, 2, or 3 and not test.

$P_3$- Establishes "Odd" parity for the IOCE
bits.

IOCE- A "1" in any one of these bit posi-
tions indicates from which IOCE the
RCU may accept commands. Only one
Bit should be set. If an attempt is
made to set more than one bit the CCR
will be set and the RCU will connect
to the lowest (logically) numbered
IOCE specified. In this case the
SCON instruction will not be accepted,
resulting in condition code 2.

•Figure 10-8.  RCU Configuration Control Register

Table 10-4. RCU State Control

| RCU #1 / RCU #2 | STATE 3 | STATE 2 OR STATE 1 | STATE 0 NOT TEST |
|---|---|---|---|
| STATE 3 | EACH RCU'S COMMUNICATION BITS CONTROL ITS OWN CONNECTIONS.<br><br>IF EQUAL "1" UNIT IS CONNECTED.<br><br>IF EQUAL "0" UNIT IS NOT CONNECTED.<br><br>NOTE: PROGRAMMER MUST EXERCISE CAUTION TO INSURE SAME DG AND RKM IS NOT CONNECTED TO BOTH RCU'S. | RCU #2 COMMUNICATION BITS CONTROL CONNECTIONS TO BOTH RCU'S.<br><br>IF EQUAL "1" CONNECTED TO RCU #2.<br><br>IF EQUAL "0" CONNECTED TO RCU #1. | RCU #2 COMMUNICATION BITS CONTROL CONNECTIONS TO RCU #2.<br><br>IF EQUAL "1" UNIT IS CONNECTED.<br><br>IF EQUAL "0" UNIT IS NOT CONNECTED.<br><br>RCU #1 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED. |
| STATE 2 OR STATE 1 | RCU #1 COMMUNICATION BITS CONTROL CONNECTIONS TO BOTH RCU'S.<br><br>IF EQUAL "1" CONNECTED TO RCU #1.<br><br>IF EQUAL "0" CONNECTED TO RCU #2. | THIS STATE IS NOT NORMALLY USED.<br><br>INTERFACE CONNECTIONS TO BOTH RCU'S ARE DISABLED. | RCU #2 COMMUNICATION BITS HAVE NO CONTROL.<br><br>ALL INTERFACE CONNECTIONS TO RCU #2 ARE DISABLED.<br><br>RCU #1 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED. |
| STATE 0 NOT TEST | RCU #1 COMMUNICATION BITS CONTROL CONNECTIONS TO RCU #1.<br><br>IF EQUAL "1" UNIT IS CONNECTED.<br><br>IF EQUAL "0" UNIT IS NOT CONNECTED.<br><br>RCU #2 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED. | RCU #1 COMMUNICATION BITS HAVE NO CONTROL.<br><br>ALL INTERFACE CONNECTIONS TO RCU #1 ARE DISABLED.<br><br>RCU #2 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED. | RCU #1 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED.<br><br>RCU #2 CANNOT COMMUNICATE WITH DG'S AND RKM'S.<br><br>DIAGNOSTIC MODE IS ENABLED. |

PROGRAMMING NOTES:

1.  An RCU Power On Reset sets all outboard communication bits equal to Zero (Interfaces disabled).

2.  When a RCU is in State Zero (not test), Enable Communication commands may be used to set the communication bits for diagnostic purposes.

3.  A system IPL sets both RCU's to State Three with all outboard communication bits equal zero.

System Monitoring of the RCU. The RCU signals each CE in the system, by means of the Element Check signal (ELC), upon occurrence of conditions significant to the system. The condition indicated by this signal are:

| Condition | Type of ELC |
|---|---|
| RCU Power Check | Level |
| RCU Power Off | Level |
| CCR Parity Check | Level |
| Out of Tolerance Check | Pulse |

The ELC signal is sent to each CE to request an external interruption A unique bit indicating the source of the ELC is set in the Diagnose Accessable Register (DAR).

Commands

Each RCU responds to the following valid commands:

| COMMAND | COMMAND BIT POSITIONS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| TEST I/O | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CONTROL NOP | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| SENSE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| WRITE CONFIGURATION | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| READ CONFIGURATION | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| READ STATUS * | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| CONTROL RESET * | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| CONTROL STOP * | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| CONTROL RESUME * | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| CONTROL DISABLE INTERFACES * | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| CONTROL TEST * | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| CONTROL ENABLE ATTENTION * | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

| COMMAND | COMMAND BIT POSITIONS |
| | 0   1   2   3   4   5   6   7 |
| --- | --- |
| CONTROL DISABLE ATTENTION * | 0   0   0   1   1   1   1   1 |
| CONTROL ENABLE COMMUNICATION * | 1   0   1   0   1   1   1   1 |
| CONTROL DISABLE COMMUNICATION * | 0   0   1   0   1   1   1   1 |

    *  These Commands are valid for addresses associated
       with DGs, RKMs, and RKM/R Consoles only.

Any other command code with correct parity is invalid and will set
sense bit 0, Command Reject, and present Unit Check in the status
byte.  The command will be ignored.

Test I/O (0000 0000) - When the Test I/O command is accepted by the
RCU, and no outstanding status conditions exist, a zero status byte
is transferred to the associated IOCE multiplexor channel.  If
status information is pending, status bits present are transferred
to the channel.

Control NOP (0000 0011) - Control NOP is an immediate type command.
It performs no operation.  Channel End and Device End status bits
are transferred to the channel during the initial selection sequence.

Sense (0000 0100) - When the RCU has accepted a Sense command, the
contents of the sense register are transferred to the IOCE.  Two
sense bytes contain the sense data (detailed in Sense Data section)
pertaining to the previous operation.  When the second sense byte is
accepted by the channel, the operation is terminated by Channel End
and Device End in the Status byte.

Write Configuration (0011 0001) - When accepted by the RCU, the Write
Configuration command will request from the IOCE the proper number
of bytes required for the addressed device.

    The number of bytes required for each device is as follows:

          DG                  2 bytes
          RKM               2 bytes
          DAU               1 byte
          RKM/R Console    4 bytes

PROGRAMMING NOTE:  The programmer should specify a byte count equal
to or greater than the required count for the device, otherwise the
Wrong Length Message sense bit will be set and no data transferred
to the device (Refer to Sense Information).  The RCU will accept only
the number of bytes required for the addressed device.

    When the data has been assembled in the RCU, the interface
associated with the addressed device is activated and the data
transmitted to the device.  Upon completion of data transfer to the

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device, Channel End and Device End are returned to the IOCE in the status byte, terminating the operation.

The configuration data formats for each device are shown in Tables 10-5, 10-6, 10-7 and 10-8 for the DG, RKM, DAU, and RKM/R Console, respectively.

Read Configuration (0010 0010) - This command, when accepted by the RCU, initiates a transfer of configuration data from the addressed device to the RCU. When the data has been assembled in the RCU, the data bytes for the device are transferred to the IOCE in burst mode. The number of bytes is device dependent and is defined as follows:

| | |
|---|---|
| DG | 2 bytes |
| RKM | 2 bytes |
| DAU | 1 byte |
| RKM/R Console | 4 bytes |

The data formats for each device are shown in Tables 10-5, 10-6, 10-7 and 10-8 for the DG, RKM, DAU, and RKM/R Console respectively.

When the IOCE has accepted the last data byte, Channel End and Device End is set in the status byte to terminate the operation. If the IOCE terminates the operation prior to transfer of all required data bytes, the remaining bytes are lost.

Read Status (0001 0010) - This command provides the ability to obtain a detailed report of error conditions from the addressed device. The command is not valid for the DAU addresses and if issued to a RKM/R Console, will result in 4 bytes of zeros. When accepted by the RCU, this command initiates a transfer of the addressed DG or RKM status register to the RCU. Once assembled in the RCU the status information is transferred to the IOCE in burst mode. Two bytes are transferred for the DG and four bytes are transferred for the RKM as shown in Tables 10-9 and 10-10. When the last byte has been accepted by the IOCE, Channel End and Device End status is set in the status byte to terminate the operation. If the IOCE terminates the operation prior to transfer of all required data bytes, the remaining bytes are lost.

Control - Reset (0000 0111) - This control immediate command is valid for DG, RKM, and RKM/R Console addresses only. When accepted by the RCU, a Reset order is transmitted to the addressed device providing the device is configured to the RCU.

The command is terminated by setting Channel End and Device End in the initial selection status byte.

Control - Stop (0100 0111) - This control immediate command is valid for DG, RKM, and RKM/R Console addresses only. When accepted by the RCU, a Stop order is transmitted to the addressed device providing the device is configured to the RCU.

The command is terminated by setting Channel End and Device End in the initial selection status byte.

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Table 10-5.  DG Configuration Data

| BYTE | BIT POSITION | FUNCTION |
|---|---|---|
| 1 | 0 | UNIT STATUS - ON LINE |
| | 1 | UNIT STATUS - STANDBY |
| | 2 | UNIT STATUS - UNAVAILABLE |
| | 3 | UNIT STATUS - MAINTENANCE |
| | 4 | CONNECT TO CVG NUMBER 1 * |
| | 5 | CONNECT TO CVG NUMBER 2 * |
| | 6 | CONNECT TO CVG NUMBER 3 * |
| | 7 | CONNECT TO CVG NUMBER 4 * |
| 2 | 0 | CONNECT TO CVG NUMBER 5 * |
| | 1 | CONNECT TO CVG NUMBER 6 * |
| | 2 | 0 ⎫ DE WORD SIZE |
| | 3 | 1 ⎭ HARDWARE SET BY RCU |
| | 4,5,6,7 | NOT USED |

* If the bit is set to "1", the PVD is connected to the Active CVG. If the bit is set to "0", the PVD is connected to the Spare CVG.

Table 10-6.  RKM Configuration Data

| BYTE | BIT POSITION | FUNCTION |
|---|---|---|
| 1 | 0 | UNIT STATUS - ON LINE |
| | 1 | UNIT STATUS - STANDBY |
| | 2 | UNIT STATUS - UNAVAILABLE |
| | 3 | UNIT STATUS - MAINTENANCE |
| | 4 | CONNECT TO DAU NUMBER 1 |
| | 5 | CONNECT TO DAU NUMBER 2 |
| | 6,7 | NOT USED |
| 2 | 0 - 7 | NOT USED |

Table 10-7.  DAU Configuration Data

| BYTE | BIT POSITION | FUNCTION |
|---|---|---|
| 1 | 0 | CONNECT TO INTERFACE A |
| | 1 | CONNECT TO INTERFACE B |
| | 2 | $S_0$ * |
| | 3 | $S_1$ * |
| | 4,5,6 | NOT USED |
| | 7 | RESET DAU * |

* Not used for Read Configuration

Table 10-8.  RKM/R Console Configuration Data

| BYTE | BIT POSITION | FUNCTION |
|------|------------|----------|
| 1 | 0 | CONNECT TO RADAR CONSOLE 1 |
|   | 1 | CONNECT TO RADAR CONSOLE 2 |
|   | 2 | CONNECT TO RADAR CONSOLE 3 |
|   | 3 | CONNECT TO RADAR CONSOLE 4 |
|   | 4 | CONNECT TO RADAR CONSOLE 5 |
|   | 5 | CONNECT TO RADAR CONSOLE 6 |
|   | 6 | CONNECT TO RADAR CONSOLE 7 |
|   | 7 | CONNECT TO RADAR CONSOLE 8 |
| 2 | 0 | CONNECT TO RADAR CONSOLE 9 |
|   | 1 | CONNECT TO RADAR CONSOLE 10 |
|   | 2 | CONNECT TO RADAR CONSOLE 11 |
|   | 3 | CONNECT TO RADAR CONSOLE 12 |
|   | 4 | CONNECT TO RADAR CONSOLE 13 |
|   | 5 | CONNECT TO RADAR CONSOLE 14 |
|   | 6 | CONNECT TO RADAR CONSOLE 15 |
|   | 7 | CONNECT TO RADAR CONSOLE 16 |
| 3 | 0 | CONNECT TO RADAR CONSOLE 17 |
|   | 1 | CONNECT TO RADAR CONSOLE 18 |
|   | 2 | CONNECT TO RADAR CONSOLE 19 |
|   | 3 | CONNECT TO RADAR CONSOLE 20 |
|   | 4 | CONNECT TO RADAR CONSOLE 21 |
|   | 5 | CONNECT TO RADAR CONSOLE 22 |
|   | 6 | CONNECT TO RADAR CONSOLE 23 |
|   | 7 | CONNECT TO RADAR CONSOLE 24 |
| 4 | 0 | CONNECT TO RADAR CONSOLE 25 |
|   | 1 | CONNECT TO RADAR CONSOLE 26 |
|   | 2 | CONNECT TO RADAR CONSOLE 27 |
|   | 3 | CONNECT TO RADAR CONSOLE 28 |
|   | 4 | CONNECT TO RADAR CONSOLE 29 |
|   | 5 | CONNECT TO RADAR CONSOLE 30 |
|   | 6 | CONNECT TO RADAR CONSOLE 31 |
|   | 7 | CONNECT TO RADAR CONSOLE 32 |

NOTE:  If the bit is set to "1", the console is
       connected to an Active RKM.  If the bit is "0",
       the console is connected to the Spare RKM.

Table 10-9.   DG Status

| BYTE | BIT | NAME | DESCRIPTION |
|------|-----|------|-------------|
| 1 | 0 | OVER TEMPERATURE | DG OVER TEMPERATURE. ATTENTION IS NOT GEN-ERATED ON THIS CONDITION. |
| | 1 | RELAY P. S. FAILURE | GENERATED BY SPARE DG ONLY. ATTENTION IS NOT GENERATED ON THIS CONDITION. |
| | 2 | DE DATA PARITY ERROR | PARITY ERROR DETECTED ON DATA FROM DE. |
| | 3 | DE ADDRESS PARITY ERROR | PARITY ERROR DETECTED ON ADDRESS FROM DE. |
| | 4 | INVALID CVG ADDRESS | CVG ADDRESS IS INVALID OR INCORRECT. |
| | 5 | CVG NUMBER 1 ERROR | INTERNAL ERROR DETECTED IN CVG 1. |
| | 6 | CVG NUMBER 2 ERROR | INTERNAL ERROR DETECTED IN CVG 2. |
| | 7 | CVG NUMBER 3 ERROR | INTERNAL ERROR DETECTED IN CVG 3. |
| 2 | 0 | CVG NUMBER 4 ERROR | INTERNAL ERROR DETECTED IN CVG 4. |
| | 1 | CVG NUMBER 5 ERROR | INTERNAL ERROR DETECTED IN CVG 5. |
| | 2 | CVG NUMBER 6 ERROR | INTERNAL ERROR DETECTED IN CVG 6. |
| | 3 | TEST | BIT IS SET BY TEST COMMAND FROM THE RCU OR AN ACTION REQUEST FROM THE MAINTENANCE PANEL ON THE DG. |
| | 4 | NOT USED | |
| | 5 | NOT USED | |
| | 6 | NOT USED | |
| | 7 | NOT USED | |

NOTE:   Byte 1, bit 0 (Over Temperature) and byte 1,
        Bit 1 (Relay P.S. Failure) conditions do not
        raise the Error Out line from the DG to the
        RCU.   These two conditions therefore, do not
        generate attention and require periodic
        polling by the program to be detected.

Table 10-10. RKM Status

| BYTE | BIT | NAME | DESCRIPTION |
|------|-----|------|-------------|
| 1 | 0 | OVER TEMPERATURE | OVER TEMPERATURE IN RKM. ATTENTION IS NOT GENERATED. |
| | 1 | I/O P.S. FAILURE | I/O POWER SUPPLY HAS FAILED ATTENTION IS NOT GENERATED. |
| | 2 | DAU PARITY ERROR | PARITY ERROR ON DATA OR ORDERS FROM DAU. |
| | 3 | DISPLAY CON- STANT PARITY | PARITY ERROR ON AT LEAST ONE OF THE EIGHT BYTES. |
| | 4 | NO RESPONSE TO INTERRUPT | NO READ QUEUE MESSAGE RE- CEIVED FOLLOWING THE INTERRUPT. |
| | 5 | DAU PROCEDURAL ERROR | PROCEDURAL ERROR ON THE DAU-RKM INTERFACE. |
| | 6 | DISPLAY CONSTANTS FAULT | NO RESPONSE FROM THE ADDRESSED CONSOLE. ATTEN- TION IS NOT GENERATED. |
| | 7 | QUEUE OVERFLOW | QUEUE ADDRESS COUNTER HAS REACHED ITS MAXIMUM. |
| 2 | 0 | DAU INVALID ORDER | INVALID ORDER CODE OR PAR- ITY ERROR IN ORDER CODE. |
| | 1 | CONSOLE PARITY ERROR | PARITY ERROR DETECTED FROM A CONSOLE DURING POLLING. |
| | 2 | MEMORY PARITY ERROR | PARITY ERROR WHEN READING THE RKM MEMORY. |
| | 3 | DATA OPERATOR ADDRESS REGIS- TER OVERFLOW | OVERFLOW DETECTED IN THE DATA OPERATOR ADDRESS REGISTER. |
| | 4 | DATA OPERATOR HANGUP | OPERATIONAL ERROR ASSOCIA- TED WITH THE DATA OPERATOR. |
| | 5 | DAU INTERFACE HANGUP | SEQUENCING FAULT DETECTED AT THE DAU-RKM INTERFACE. |
| | 6 | DATA CONTROL HANGUP | FUNCTIONAL OR SEQUENCE ERROR IN THE DATA CONTROL. |
| | 7 | TEST | BIT IS SET FROM THE RCU BY TEST COMMAND OR AN ACTION REQUEST FROM THE MAINTE- NANCE PANEL ON THE RKM. |
| 3 | 0-7 | NOT USED | |
| 4 | 0-7 | NOT USED | |

NOTE: Byte 1, bits 0,1 and 6 do not generate attention and require periodic polling by the program to be detected.

Control - Resume (0101 0111) - This control immediate command is
valid for DG, RKM, and RKM/R Console addresses only.  When accepted
by the RCU, a Resume order is transmitted to the addressed device
providing the device is configured to the RCU.

The command is terminated by setting Channel End and Device
End in the initial selection status byte.

Control - Disable Interface (0111 0111) - This control immediate
command is valid for DG, RKM and RKM/R Console addresses only.  When
accepted by the RCU, the command causes a Disable Interfaces order
to be transmitted to the addressed device providing the device is
configured to the RCU.

The command is terminated by setting Channel End and Device End
in the initial selection status byte.

Control Test (0110 0111) - This control immediate command is valid
for DG, RKM, and RKM/R Console addresses only.  When accepted by
the RCU, a Test order is transmitted to the addressed device provid-
ing the device is configured to the RCU.  If the RCU is in State
Zero the Test command will generate an Attention Interrupt (Refer to
Diagnostic Facilities).

The Test command is terminated by setting Channel End and Device
End in the initial selection status byte.

Control Enable Attention (1001 1111), Control Disable Attention
(0001 1111) - These two control immediate commands allow the program
to control attention interrupts on a device basis.  The commands are
valid for DG, RKM, and RKM/R Console addresses only.  When accepted
by the RCU the command either sets the Enable Attention bit for the
addressed device (Enable Attention Command), or resets the bit
(Disable Command), in the RCU.  The commands have no affect at the
device.

Both commands terminate their operation by returning Channel
End and Device End in the initial selection status byte.

PROGRAMMING NOTES:

1.   An Enable Attention command issued when an error report is pend-
     ing results in Attention status being generated after termin-
     ation of the Enable command.  Attention is not presented with
     Channel End and Device End.

2.   Power On Reset or System Reset turns all Enable Attention bits
     off.  The Program must Enable Attentions after initial power
     on and following a System IPL.

Control Enable Communication (1010 1111), Control Disable
Communication (0010 1111) - These two control immediate commands
allow the program to establish the desired outboard configuration
of RCU with DG, RKM, or RKM/R Console.  The commands are valid for
DG, RKM and RKM/R Console addresses only.

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These commands are accepted by the RCU only when the RCU is in
State Three or State Zero.  The acceptance of the commands while the
RCU is in State Zero is provided for maintenance purposes and has no
effect on outboard configurations (Reference Diagnostic facilities).
If either of the commands are issued to an RCU in State 1 or State 2,
Unit Exception status is returned to the channel during initial
selection and no action is taken as a result of the command.

When the RCU is in State Three and one of these commands is
accepted, the communication bit for the addressed device is set
(Enable command) or reset (Disable command).  The command is then
terminated by Channel End and Device End status in the initial
selection status byte.  These commands have no affect on the address-
ed device other than allowing or switching the RCU with which the
device may communicate.

Status Information

The status byte for the RCU is transferred to the channel in the
following situations:

    1.    During initial selection
    2.    At the termination of a command.
    3.    When permitted to present stacked status.
    4.    To present Attention signal to the channel.

The status byte has the following format:

| Bit | Designation |
| --- | --- |
| P | Parity |
| 0 | Attention |
| 1 | Status Modifier |
| 2 | Control Unit End |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Unit Exception |

The following status bit combinations are used by the RCU.

Bit Position

| 0 1 2 3 4 5 6 7 | Use |
| --- | --- |
| 0 0 0 0 1 1 0 0 | Channel End, Device End |
| 0 0 0 0 1 1 1 0 | Channel End, Device End, Unit Check |
| 0 0 0 0 0 0 0 1 | Unit Exception |
| 1 0 0 0 0 0 0 0 | Attention |
| 0 1 0 1 0 0 0 0 | Status Modifier, Busy |
| 0 0 1 0 1 1 0 0 | Control Unit End, Channel End, Device End |

Bit Position

```
0 1 2 3 4 5 6 7                    Use

0 0 1 0 1 1 1 0                    Control Unit End, Channel End
                                   Device End, Unit Check
0 0 0 0 0 0 1 0                    Unit Check
```

Channel End, Device End - This bit configuration is generated as a normal ending status or as a result of a Halt I/O when busy and no check conditions exist.

Channel End, Device End, Unit Check - This bit configuration is generated under the following conditions:

1.  A Bus Out Check is encountered on data during a Write Configuration command.  The operation is terminated immediately with no data being transmitted to the device.

2.  A Data Check condition is detected at the completion of the shift of data to the device during a Write Configuration command.  Improper data may have been recorded at the device.

3.  **A short message is specified by the program.  The Wrong Length Message sense bit is set and data is not transmitted to the device.**

4.  During a Write Configuration to the DAU when the DAU detects invalid configuration data.  Data Check is also set in the sense register.

Unit Exception - This bit is returned in the status byte when the command cannot perform its function because of the RCU state or configuration.  Unit Exception is set by the two following conditions and indicates no action has been taken as a result of the command.

1.  An Enable Communications or Disable Communications command is directed to an RCU which is in State 1 or 2.

2.  A command is addressed to a device which is not configured to that RCU.

Attention - Attention status is presented by itself when the RCU is not busy or in response to a Test I/O addressing a device with attention pending.  Attention is presented when a device reports an error condition and the Enable Attention bit is on in the RCU.  An error report is a result of either (1) the device raising the Error Out line or (2) the Power On line from the device indicating power has dropped.

Status Modifier, Busy - These two status bits, indicating Control Unit Busy, are presented to the channel when the RCU is busy with one device and the channel attempts an initial selection for another device.  Control Unit End is also stored in the RCU for presentation later.

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when the process terminated.

Control Unit End, Channel End, Device End - This bit configuration is generated when Control Unit Busy has been indicated to the channel due to a selection attempt for one device while another device is busy, and the busy device is terminating the operation normally.

Control Unit End, Channel End, Device End, Unit Check - This bit configuration is generated when the Control Unit Busy has been indicated to the channel due to a selection attempt for one device while another device is busy, and the busy device is terminating the operation with an error condition (Refer to Channel End, Device End, Unit Check).

Unit Check - This bit is returned to the channel during initial selection when one of the following conditions occurs:

1.    The command has proper parity but is not valid for the addressed device.  Command Reject is set in the sense register.

2.    The command byte has improper parity.  Bus Out Check is set in the sense register.

3.    The addressed device is not ready.  Intervention Required is set in the sense register.

The status bits are reset when the status byte is accepted by the channel.

Sense Information

When the Unit Check bit in the status byte is set, a Sense command should be executed to determine the type of equipment or programming check associated with the previous command.  The sense bits associated with the previous command are reset by the acceptance of the next valid Read, Write or Control (except Control NOP) command.  The sense bits in byte 1 except for bit 2 (Bus Out Check), are also reset when a Bus Out Check occurs during the initial selection cycle.  A Command Reject condition during initial selection also resets all bits in sense byte 1 except bit 0 (Command Reject).  A Control NOP or Test I/O which generates Intervention Required Sense bit due to a not ready device, will also reset all sense bits in byte 1 except bit 1 (Intervention Required).

The bits contained in sense byte 2 are generated by the RCU as a result of an Out of Tolerance check or CCR parity error or when multiple IOCE communication bits are set in the RCU CCR by the SCON instruction.  These three conditions remain set in the sense register until the condition causing the bit to be set is cleared.

The sense bytes for the RCU have the following format:

| Byte | Bit | Designation |
|------|-----|-------------|
| 1 | 0 | Command Reject |
|   | 1 | Intervention Required |
|   | 2 | Bus Out Check |
|   | 3 | Not Used |
|   | 4 | Data Check |
|   | 5 | Not Used |
|   | 6 | Not Used |
|   | 7 | Wrong Length Message |
| 2 | 0 | Not Used |
|   | 1 | Not Used |
|   | 2 | Not Used |
|   | 3 | CCR Program Check (Multiple IOCE Bits) |
|   | 4 | Not Used |
|   | 5 | Not Used |
|   | 6 | CCR Parity Check |
|   | 7 | Out of Tolerance Check |

Sense Byte 1, Bit 0 - Command Reject - Command Reject is set during
the initial selection phase of a command if the bit configuration
with correct parity is not a valid command for the addressed device.
Unit Check is set in the status byte and the command is ignored.
Other sense bits in byte 1 are reset.

Sense Byte 1, Bit 1 - Intervention Required - Intervention Required
is set when a valid command is issued to a device which is not ready
(Power Off or not available to the system).  Unit Check is set in
the initial selection status byte and the command is ignored.

NOTE:  The RKM/R Console does not indicate a power off or not avail-
able condition.  This indication is obtained from the associated RKM.

Sense Byte 1, Bit 2 - Bus Out Check - Bus Out Check will be set if
a parity error is detected by the RCU during initial selection or
during a data transfer operation.  If the condition occurs during
initial selection, the bits in sense byte 1 (except Bus Out Check)
are reset.  Unit Check is set in the status byte and the command is
ignored.

     If the condition occurs during data transfer, the operation is
terminated immediately with Channel End, Device End and Unit Check
bits in the status byte and Bus Out check set in sense byte 1.

Sense Byte 1, Bit 4 - Data Check - Data Check is set when the RCU
determines that correct parity was received on data from the channel,
and the parity of the bits shifted to the device did not compare
with the precomputed parity generated by the RCU from the channel
byte parity bits.  A Data Check condition indicates that improper
data may have been recorded at the device.  The operation is term-
inated with Channel End, Device End and Unit Check in the status
byte and Data Check set in sense byte 1.

Sense Byte 1, Bit 7 - Wrong Length Message - The WLM bit is set by
the RCU when the programmer specifies a message length shorter than

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required for the addressed device. The operation is terminated by
Channel End, Device End and Unit Check status, the data is not
transmitted to the device and the WLM bit is set in sense byte 1.

Sense Byte 2, Bit 3 - CCR Program Check - This bit is set when more
than one IOCE communication bit is set in the RCU CCR during a
SCON instruction. When this condition occurs, the RCU logically
connects to lowest (logically) numbered IOCE specified and rejects
the SCON select. The bit is reset when the condition is corrected
by another SCON instruction.

Sense Byte 2, Bit 6 - CCR Parity Check - This bit is set when the RCU
detects a parity error in the CCR, either on the State and SCON bits
or the IOCE communication bits. Parity is continuously monitored at
the CCR and if a parity check condition occurs, a level ELC is also
sent to all CE's. The bit is reset when the condition is corrected
by setting new information into the CCR.

Sense Byte 2, Bit 7 - Out of Tolerance Check - When the temperature
of the logic gate or power supplies associated with the RCU approach-
es within approximately 10 degrees of the shut down level, the Out
of Tolerance bit is set. A pulsed ELC is also generated to all CE's.
The sense bit is reset when the temperature decreases to a normal
level.

DESIGN DETAILS

Registers

A RCU data flow diagram showing the registers and transfer paths is
shown in Figure 10-9.

Address Register - A five bit register which contains the device
address portion of the address received from the IOCE during initial
selection.

Command Register - This eight bit register retains the command dur-
ing its execution. The register is loaded during the initial selec-
tion cycle and the output is decoded to provide necessary controls
for execution.

CI Shift Register - During a read operation this thirty-two bit
shift register receives configuration data or status information
serially by bit from the addressed device and transfers the
assembled data to Bus In one byte at a time. Conversely, during
a write operation the register is loaded one byte at a time from
the IOCE until the specified number of bytes have been assembled
and then the data is shifted serially by bit to the addressed
device.

Status Register - This five position register is set when status
information is generated by an operation in process or when
generated by an asynchronous condition such as an error report.
The contents of the register are transmitted to the IOCE as one
byte when the Status In signal is on. The register is reset
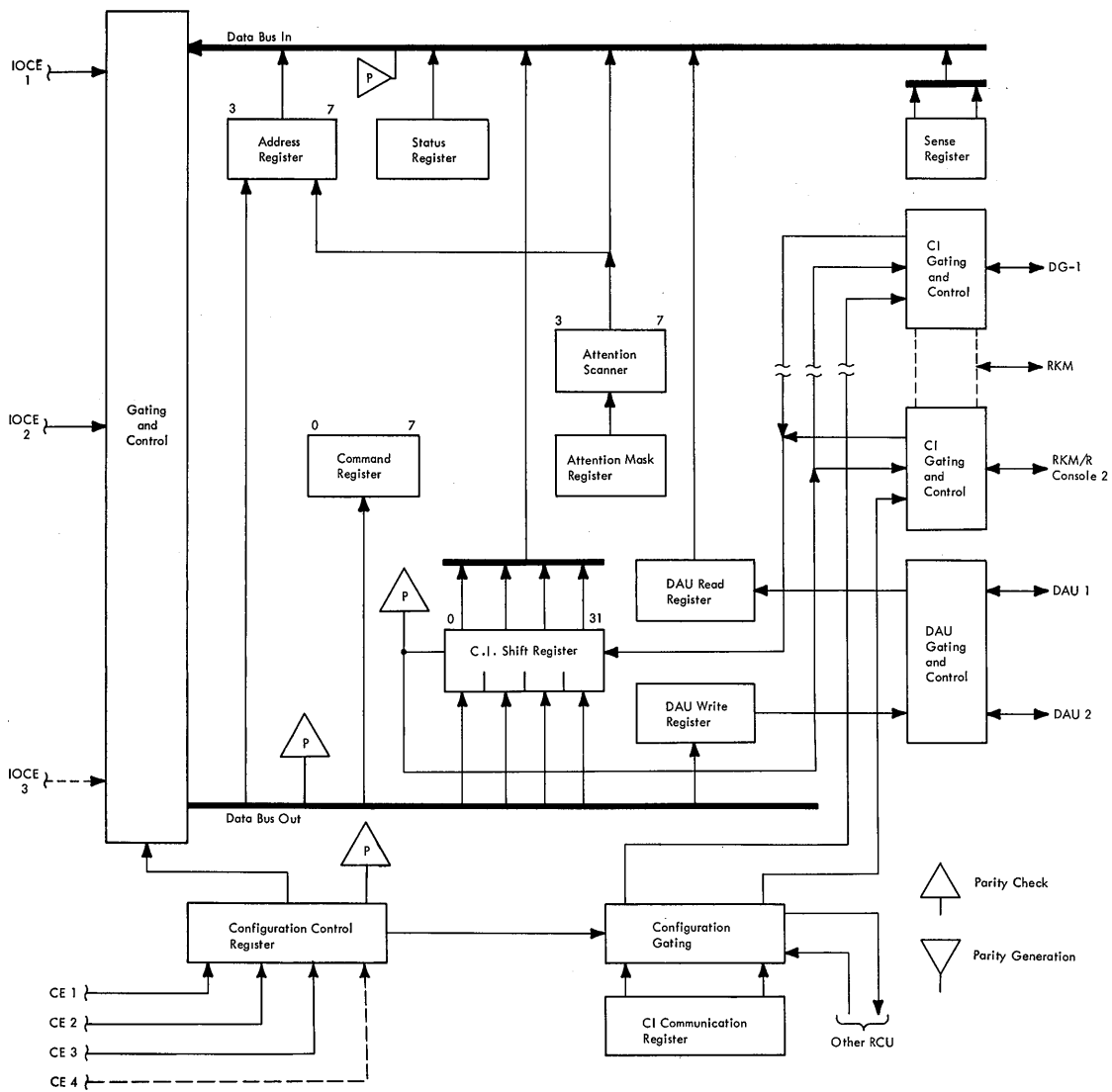
•Figure 10-9. RCU Data Flow

when the status information is accepted by the IOCE.

Sense Register - This eight bit register is set by various check
conditions detected by the RCU. The contents of the register are
transferred to the IOCE in response to a Sense Command as two data
bytes. The first data byte contains check condition pertinent to
the previous operation while the second byte contains check condi-
tions related to the RCU CCR and OTC bit.

Attention Scanner - The Attention Scanner is a 5 bit binary counter
with a decoder on the output which sequentially scans the CI inter-
faces for error reports. When an error report is encountered, and
the associated attention control register bit is set, stepping of
the counter is inhibited. When allowed to present the pending
attention to the IOCE, the contents of the attention scan counter
are transferred to the IOCE as the device address. After the IOCE
accepts the attention, the counter is then allowed to step to the
next sequential device. Stepping occurs every 2.0 usec until the
next error report is encountered.

Attention Mask Register - This seventeen bit (twenty five in the
expanded version) register contains a position for each CI interface
and its contents provide a mask for error reports. Each bit position
of the register is set or cleared by an Enable or Disable Attention
command addressed to the associated device. When a position is set
(equal one) an error report for the associated device will generate
an attention when the attention scanner allows. If the bit equals
zero, an attention is not generated as a result of an error report.

DAU Write Register - This five position register is used during a
Write Configuration operation to buffer the configuration data during
transfer to the DAU.

DAU Read Register - The DAU Read Register is a two position register
used to buffer configuration data received from the DAU, during a
Read configuration operation.

Configuration Control Register - The CCR is a nine bit plus two
parity bit register which contains the State bits, SCON bits, and
IOCE communication bits for the RCU. The register is loaded directly
from the control CE via the configuration control interface connec-
tion between the RCU and the CE. The parity of this register is
constantly monitored and any error is reported to all CE's via the
Element Check signal.

CI Communication Register - This register contains a bit position
for each CI, each of which controls the interface driver and
receivers for the Configuration Interfaces. The register's contents
are also gated to the second RCU if the contents of the CCR state
bits designate State Three. The RCU uses the contents of its own
CI communications register for control of its own drivers and re-
ceivers when in State Three. When in State Two or One the contents
of the other RCU CI communication register is used for control of
the CI drivers and receivers provided the other RCU is in State
Three.

The CI Communication Register is program loaded by the Enable Communication or Disable Communication command. Each bit position of the register is addressable by the associated CI address. The register may be loaded only when the RCU is in State Three or State Zero, not Test.

Diagnostic Facilities

Diagnostic Facilities provided by the RCU are designed for use by the maintenance programs and are enabled when the RCU is in State Zero, not Test. In this State the outbound drivers and receivers for the CI's and DAU interfaces are deconditioned, which inhibits communication between the RCU and the DGs, RKMs, and DAUs. Internal communication and control paths are established which allow program testing of the RCU addressing, commands, outboard configuration, error reporting and data paths.

CI Diagnostic Facilities. The following diagnostic facilities are provided for the CI portion of the RCU.

1.  An Enable Communication or Disable Communication command may be used to set or clear the addressed bit position in the CI communication register. The output of the register is tested by the CI Read, Write and Control commands, thus providing normal responses to these commands.

2.  When command chaining is indicated to the RCU during a Read Configuration, Write Configuration or Read Status command, the CI shift register is not reset at the end of the operation. In addition a Write Configuration command enables a data path connection between the output of the shift register via the addressed CI interface logic and back to the input of the shift register. These two hardware facilities allow check-out of the CI shift register, serial data paths and the parity detection circuitry associated with the output of the shift register.

3.  To assist in checkout of addressing decoding, attention scan circuitry and the commands associated with attention control, a decoder located in each CI logic area is provided which decodes a Control Test Command (0110 0111). The decoder output simulates an error report which subsequently generates an attention (if enabled) via the attention scanner. In response, the program may issue a Read Status command, which will set the bit position in the shift register corresponding to the device "Test" bit position and then transfer the contents of the register to the IOCE.

DAU Diagnostic Facilities. The following diagnostic facilities are provided for the DAU portion of the RCU.

1.  A Write Configuration command followed by a Read Configuration command results in reading back the data previously written. If the Write data byte contains a zero in the

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Reset bit position, the Read operation results in transfer
of the Interface A and Interface B bit positions from the
DAU Write register to the DAU Read register.  When the Write
data byte contains a one in the Reset bit position, the
Read operation results in transfer of the S0 and S1 bit
positions from the DAU Write register to the DAU Read
register.

2.   When a Write Configuration command with a data byte consist-
ing of bits 0, 1, 2, 3, and 7 equal one, is specified a
data check condition is simulated.

RCU External Interfaces

The RCU provides external configuration interfaces to attach the DGs
and RKMs, to the 9020E System.  Two interfaces are also provided for
configuration of the IBM 2701 DAUs.  The DAU interfaces are discussed
in Chapter 13.  The DG and RKM interfaces are defined as follows:

|                         | Base           | Expansion     |
|-------------------------|----------------|---------------|
| DG Configuration Interface | 12 DG's     | 17 DG's       |
| RKM Configuration Interface | 3 RKM's    | 5 RKM's       |
| RKM Configuration Interface | 2 RKM/R Console | 3 RKM/R Console |

DG and RKM Configuration Interface, General Characteristics.  The DG
and RKM Configuration Interface is used to transmit configuration
data and status information between the RCU and the DGs, RKMs, and
RKM/R Consoles.  Each interface is addressable as an I/O device by
the 9020E System.

Interface Lines.  Each interface consists of the following control
and data lines.

```
                          ┌─────── ERROR OUT ───────────┐
                        ◄─┤                             ├─
                          │─────── DATA   OUT ──────────│
                        ◄─┤                             ├─
                          │───── CONFIGURATION IN ──────│──►
                          │                             │
                          │──────── CLOCK ──────────────│──►
    CONFIGURATION         │                             │  DISPLAY SUBSYSTEM
                          │──────── CONTROL 1 ──────────│──►
    CONSOLE               │                             │  UNIT   (DG OR RKM)
                          │──────── CONTROL 2 ──────────│──►
                          │──────── CONTROL 3 ──────────│──►
                          │──────── CONTROL 4 ──────────│──►
                        ◄─┤──────── POWER   ON ─────────│
                          │── MEMORY ENABLE (RKM ONLY) ─│──►
                          └─────────────────────────────┘
```
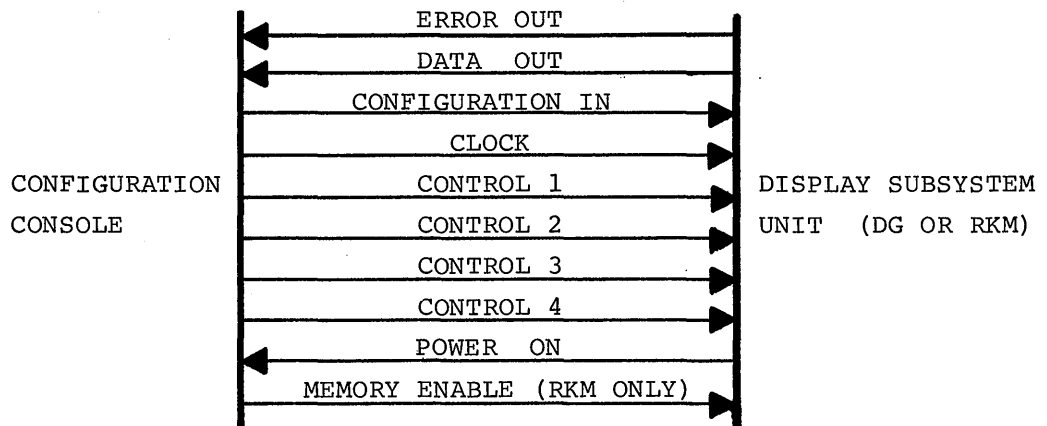
Control Lines - Control lines 1, 2, 3, and 4 are used to transmit the following commands to the DG or RKM. Control line C4 is always transmitted as a logical zero.

| Command | C1 | C2 | C3 | C4 |
|---------|----|----|----|----|
| Reset | 0 | 0 | 0 | 0 |
| Read Status | 0 | 0 | 1 | 0 |
| Read Configuration | 0 | 1 | 0 | 0 |
| Set Configuration | 0 | 1 | 1 | 0 |
| Stop | 1 | 0 | 0 | 0 |
| Resume | 1 | 0 | 1 | 0 |
| Test | 1 | 1 | 0 | 0 |
| Disable Interfaces | 1 | 1 | 1 | 0 |

Each of these operations is described below.

Reset - This code in conjunction with a single clock pulse on the Clock Line resets the DG or RKM to a null state in which it is prepared to receive commands and data via normal system paths. For the RKM/R Console, this command in conjunction with a clock pulse on the Clock line places the data in the 32 bit shift register into the 32 bit configuration register.

Read Status - This code and a series of clock pulses on the Clock Line cause the contents of the status register in the DG or RKM to be shifted serially by bit to the RCU on the Data Out Line. Order of transfer is MSB to LSB. Setting of the status register is inhibited when this code is recognized by the selected unit. For the DG a series of 12 clock pulses are issued. For the RKM and RKM/R Console a series of 32 clock pulses are provided.

Read Configuration - This code and a series of clock pulses on the Clock line will cause the DG or RKM to shift the contents of its configuration register to the RCU on the Data Out Line. For the RKM/ R Console, this code in conjunction with 32 clock pulses causes the data in the 32 bit shift register to be transferred serially by bit to the RCU on the Data Out line. Order of transfer is MSB to LSB. The number of bits for each unit is as follows:

```
DG              - 12 bits
RKM             - 14 bits
RKM/R console   - 32 bits
```

Set Configuration - This code and a series of clock pulses on the Clock line will cause configuration data to be transmitted bit serially to the DG, RKM or RKM/R Console from the RCU on the Configuration In line. Order of transfer is MSB to LSB. The number of bits for each unit is as follows:

```
DG              - 12 bits
RKM             - 14 bits
RKM/R Console   - 32 bits
```

Stop - This code in conjunction with a single clock pulse on
the Clock line causes the RKM to stop all normal operation at the end
of the next internal clock cycle.  The RKM/R Console uses this com-
mand in conjunction with a clock pulse to transfer data from a para-
llel shift register to a serial shift register in preparation to read
RCRD configuration upon receipt of the Read configuration command.

Resume - This code in conjunction with a single clock pulse on
the Clock line will cause the RKM to continue operation from the
point it was stopped by a Stop command.

Test - This code in conjunction with a single clock pulse on
the Clock line will cause the DG or RKM to set the test bit in its
status register.

Disable Interfaces - This code in conjunction with a single
clock pulse on the Clock line will cause the RKM to disconnect
all unit interfaces to other units except the Configuration Inter-
face with the RCU.

> NOTE:  The commands Stop, Resume, and Disable Interfaces are not
> used by the DG.  The commands Read Status, Resume, Test and
> Disable Interfaces are not used by the RKM/R Console.  In each
> case the unused commands perform no operation and result in no
> error conditions at the respective DG or RKM/R Console.

Clock Line - The clock line is used to transmit a 1.0 MHz clock train
starting 1.5 usec after the control line code is raised.  The clock
train serves as a sync for data being transmitted over the Configur-
ation In or Data Out lines and is variable in length depending upon
number of bits being transmitted.

Data Out - This line is used to transmit configuration data or
status information from the DG or RKM to the RCU.

Configuration In - This line is used to transmit the configuration
data from the RCU to the DG or RKM.

Error Out - This line is raised by the DG or RKM whenever an error
condition has been loaded into the status register.  It persists
as long as the error condition remains in the unit.

Power On - This signal is a level which is in the Zero State when
all logic power supplies in the DG or RKM are operating.  The RCU
will assume a power supply has failed in the unit if a logical
one is received on this line or zero differential voltage exists
between the + signal and - signal lines.  This line is not used
for the RKM/R Console interfaces.  The RCU does not provide a
power off indication to the 9020E System for the RKM/R Console.

Memory Enable (RKM Only) - This line is not used by the 9020E System.
The CC will insure the line is open circuited.

Data Formats.  The data formats for Set Configuration and Read Con-
figuration are shown in Tables 10-5, 10-6, and 10-8 for the DG, RKM,
and RKM/R Console respectively.  The data formats for Read Status are
shown in Tables 10-9 and 10-10 for the DG and RKM.

Data Transfer RCU to RKM, RKM/R Console or DG - The operation is
started by raising a control code on the four control lines.  Refer
to Figure 10-10.  The first bit of data is placed on the Configur-
ation In line at the same time the control lines are activated.
One and one-half clock cycles later (1.5 usec) the Clock line is
activated with a series of clock pulses at 1.0 MHz rate.  This clock
signal is up for 110ns ± 10% and down for 890ns ± 10%.  The RCU will
change the Configuration In Line 500ns ± 50ns after the rise of the
clock signal.  The number of bits transmitted is controlled by the
number of clock pulses sent by the RCU on the Clock Line.

Data Transfer RKM, RKM/R Console, or DG to RCU - Status information
and configuration data is read from the DG and RKM upon demand from
the RCU.  The operation is initiated by raising a control command
either Read Status or Read Configuration.  The DG or RKM must place
the first data bit on the Data Out line no later than 200 ns after
receipt of the command.  One and one-half clock pulses (1.5 usec)
after raising the command the clock line is activated with a series
of 1.0 MHz pulses.  Upon receipt of the rise of each clock pulse
the DG or RKM must change the Data Out line for the next bit within
200 ns.  (The signal must be static at the DG's and RKM's output
connector within 200 ns).

Electrical Characteristics.  All signals between the RCU and DG's
and RKM's are carried by a 100 ohm balanced transmission system.
The cable is an overall shielded cable containing multiple twisted
pair conductors.

Line Driver - The output signals from the CC shall have the following
specifications when a 100 ohm plus or minus 5% resistive terminator
is connected between the + signal lead and the - signal lead at the
CC output connector pins.

     A logical one is represented by the + signal line being
-1.6 volts (+0.3v, -0.7v) with respect to the - signal line.  A
logical zero is represented by the + signal line being +1.6 volts
(-0.3v, +0.7v) with respect to the - signal line.

     The + signal and - signal lines shall not exceed plus or minus
7.0 volts with respect to the CC signal ground (DC return) when
measured at the CC output connector.

     Rise and Fall times at the CC output connector shall not exceed
40 ns (20% to 80%) when measured from + signal or - signal line to
ground.  This measurement is made with no external cable attached
and a termination resistor of 100 ohms ± 5% connected from the +
signal line to the -signal line.

     Differential skew will be 20 ns or less at the driver output.
Differential skew between + and - signal lines is defined as the

10-60

Read

1000ns ±100ns

110ns
±10%

Clock
Out

890ns
±10%

1500
ns
±150

1500
ns
±150

Control
Read

150ns
min
650ns
max

150ns
min
650ns
max

150ns
min
650ns
max

Data Out
Line

1st Bit          2nd Bit        3rd Bit        Nth Bit

Write

110ns
±10%

Clock
Out

890ns
±10%

1500
ns
±150

1500
ns
±150

Control
Write

500
ns
±150

500
ns
±150

500
ns
±150

Configuration
In Line

1st Bit          2nd Bit        3rd Bit        nth Bit

Control

110ns
±10%

Clock
Out

1500
ns
±150

1500
ns
±150

Control
Reset

Note:
All signal times
shown at CC connector.

●Figure 10-10.  CI Interface Timing

time interval when the driver output is not in a definite state.
The driver is in an indefinite state when the differential voltage
between the + and - signal lines is less than 1.3 volts.

Line Receiver - The characteristic impedance between + signal and
- signal lines at the input connector to the CC shall be 100 ohms
± 5%.  A logical "zero" is represented by the + signal line being
equal to or greater than +0.6 volts in respect to the -signal line
when measured at the receiver input.  A logical "one" is -0.6 volts
in respect to the - signal line when measured at the receiver in-
put.  The + signal and - signal lines shall each remain between +3
volts and unit signal ground (DC return).

Driver Output - The driver output is measured at CC output connector
with 100 ohm terminator from + signal to - signal with no cable
attached.

Power Off condition all drivers:

     Signal line differential voltage = 0.v ± 1.0mv.

                         LOGICAL ZERO

+ signal line            Max Level                 +2.3v ─┐

Voltage measured         Nominal Level             +1.6v ─┤

In reference to          Min Level                 +1.3v ─┤

- signal line                         Ref. (-Signal Line)─┴─

                         LOGICAL ONE

                              Ref. (-Signal Line)─┬─

+ signal line            Min Level                 -1.3v ─┤

Voltage measured         Nominal Level             -1.6v ─┤

In reference to          Max Level                 -2.3v ─┘

- signal line

Receiver Input Requirements - The receiver input is defined as
follows:

                         LOGICAL ZERO

+ signal line            Max Level                 +3.0v ─┐

Voltage measured         Min Level                 +0.6v ─┤

In reference to

- signal line                         Ref. (-Signal Line)─┴─

LOGICAL ONE

Ref. (-Signal Line) --

+ signal line

voltage measured

in reference to          Min Level          -0.6v

- signal line            Max Level          -3.0v
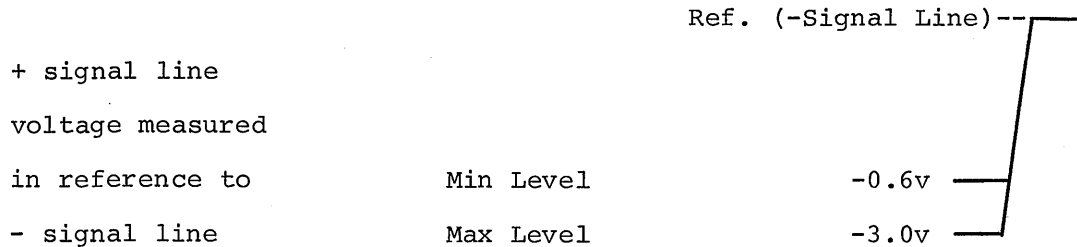
Fault Conditions - The following Fault conditions may occur during maintenance periods or due to circuit malfunction.

1.  A grounded signal must not damage drivers, receivers, or terminators.

2.  Both lines shorted together must not damage drivers, receivers, or terminators.

3.  An open line or terminator must not damage the driver or receiver circuit. (This condition may result in one signal line rising to 7.0 volts with respect to signal ground).

4.  Power down at the driver may cause a condition at the receiver which could allow small noise signals to switch the receiver circuit. The CC will provide facilities for degating receiver outputs where needed to prevent erroneous system interruption.

5.  A receiver which is not connected to a driver circuit must not generate spurious signals.

6.  Changing power status (Normal Power On or Off) shall not propagate signals which might affect configuration of a DG or RKM or cause an abnormal system interruption.

Cabling - Cables must meet the defined following specifications and must utilize standard Serpent type connectors at the CC end.

    Characteristic Impedance   = 95 ohms
    Resistance DC              = .019 ohms/conductor/ft.
    TPD, (Propagation Delay)   = 1.5 ± .05 ns/ft.
    $\triangle$ TPD            = .02 ns/ft.
    **Attenuation**            = 2.1 db/100 ft at 4 MHz.

Cable and connector requirement at the CC end per DG and RKM Configuration Interface are as follows:

    Configuration Interface    10 Signals    1-24 Pin Serpent

Refer to Table 10-11 for connector pin assignments.

A minimum of 17 connectors are provided in the basic version of the CC. The expanded CC provides 25 connectors.

Table 10-11.  Configuration Interface Pin Assignments

| B02 | - Control 1 | D02 | + Control 1 |
|-----|-------------|-----|-------------|
| B03 | + Control 2 | D03 | Not used |
| B04 | - Control 2 | D04 | - Control 3 |
| B05 | + Control 4 | D05 | + Control 3 |
| B06 | Not used | D06 | - Clock |
| B07 | - Control 4 | D07 | + Clock |
| B08 | + Config In | D08 | Ground |
| B09 | - Config In | D09 | - Error Out |
| B10 | - Power On | D10 | + Error Out |
| B11 | Not used | D11 | - Data Out |
| B12 | + Power On | D12 | + Data Out |
| B13 | + Memory Enable (Not used) | D13 | - Memory Enable (Not used) |

Serpent Connector Blocks - All serpent connectors used in the CC will be type A connectors.  These must be mated with a type B connector on the external cable.  Serpent contact termination to termination contact resistance (includes 2 crimps and mated contacts) will not exceed:

    .020 ohms when used with #22 wire or larger
    .030 ohms when used with #24 or #26 wire

External Cable Length - The maximum external cable length for each DG or RKM Configuration Interface is 150 feet connector to connector (5 feet is used within the CC).

POWER CONTROL AND INDICATIONS

General

The power controls and indicators provided on the console are used
to monitor the system power source, control and monitor the unit
power of the console, and provide a central position for Emergency
removal of power to all elements of the IBM 9020E System.  Four power
systems are contained in the Configuration Console providing in-
dependent power and control for the three control units.  The two
power systems for the RCU's designated A and D, each receive prime
power from individual power cords which feed prime power to the bulk
Transformer/Rectifier power pack (T/R pack).  The T/R packs in turn
feed the individual power supply modules which supply the regulated
DC voltages required by the RCU logic.

Two additional power systems designated B and C are provided
for the System Console functions.  These two power systems also
each consist of bulk T/R packs feeding individual power  supply
modules.  Each receive prime power from one of the two prime power
cords.  The two systems are duplexed, one of the two being manually
selectable from the operators panel.

Note:  There is no interlocking between the two prime power cords.
       If a wall breaker feeding one power cord is opened, power
       will remain up on the two power systems connected to the
       second power cord.

Thermal, over-under voltage, and over current sensing is pro-
vided in the power fault detection circuitry for each power system.

Marginal checking facilities are provided on each maintenance
and test panel to manually provide voltage excursions on the +6 volt-
age supply for each set of power supplies to detect marginal circuitry
in the logic.  The marginal check controls are to be used only by
trained maintenance personnel.

Power for the IBM 2821 Control Unit is controlled from the Con-
figuration Console.  When the console power switch is turned on,
power will automatically be turned on in the IBM 2821 Control Unit
providing its Remote/Local switch is in the Remote position.  When
the System Console Power On/Off switch is turned off, power will
automatically be turned off in the IBM 2821 Control Unit.

Power for the 1052-7's is supplied from the associated adapter
located in the CE.

In the event of prime power failure, the console will cycle its own power up without manual intervention when prime power is restored, provided the console Power On/Off switches are on.

Operator controls and indicators are described in the following sections. The following table lists the controls and indicators described in this section.

| Name | Implementation |
|------|----------------|
| Power On/Off | Toggle Switch |
| Power Supply Select | Rotary Switch |
| Emergency Pull | Pull Switch |
| Thermal Reset | Pushbutton Switch |
| Element MPO | Pull Switch |
| System Standby | Indicator |
| Battery | Indicator |
| Console Main Line On | Indicator |
| Console Power Check | Indicator |
| Thermal Check | Indicator |
| Power Sequence Complete | Indicator (3) |

Power Switches

Power On-Off Switches - Three Power On-Off toggle switches located on panel A of Figure 10-4 provide power on/off control for the System Console, and the two RCUs. Placing a switch in the On position causes the associated power system to sequence on, the associated power check indicator is turned off and the Power Sequence Complete indicator is turned on.

When power is on, and the Power On/Off switch is placed in the Off position, the power supplies are sequenced off, the Power Check indicator is turned on, and the Power Sequence Complete indicator is turned off. In the case of the RCUs the power off function is operative only if the RCU is in State Zero with the Test switch on or in State Zero with the I/O Interface Disabled.

System Console Power Supply Select Switch - The Power Supply switch is located in panel A, Figure 10-4. This switch is used to select one set (B or C) of the duplexed DC power supplies within the console when the Power On/Off switch is turned on.

Emergency Pull - This switch is a red, mechanically latched, pull-type switch, located on Panel A or Figure 10-4. When the switch is pulled, power to all IBM 9020E System elements will be removed within a two second period. Power will still be present in the power compartments of each system element. This switch must be manually reset at the console to restore system power. Power will automatically sequence up on all units if their power switch is on.

System Console Thermal Reset Pushbutton - The Thermal Reset push-button is located on Panel A, Figure 10-4. Depression of this push-button turns out the Thermal Check Indicator for the System Console

provided the temperature has been reduced to the normal operating range.

Element MPO - This switch is a red and white, mechanically latched, pull type switch, located on Panel A of Figure 10-4. When the switch is pulled, power to all Configuration Console circuits and cabling outside the prime power compartments is removed. This switch must be manually reset to restore CC power. Power will auto- matically sequence up if the power switches are on.

System Power Indicators

System Standby Indicator - This indicator will light when the diesel generator is supplying the prime AC power to the system. The in- dicator circuit will function regardless of Configuration Console power status. The Indicator is turned on by an externally located contact closure.

Battery Indicator - This indicator will light when one or more of the 9020E System elements indicates that it has switched to battery power. The indicator circuit will function regardless of the System Console power status. The element changing to battery power will supply +24 V DC to light the indicator. The +24 V DC will be removed when the element is switched to standby power, or main line power, or power is sequenced down.

Console Power Indicators

Console Main Line On Indicator - This indicator is located in Panel A, Figure 10-4. The indicator will be on when prime AC is supplied from either the main or standby source to either or both of the prime power cords. At least one of the main console circuit breakers must be on and the EPO switch must be inactive.

System Console Power Check Indicator - This indicator is located on Panel A, Figure 10-4. The indicator will be turned on if any or all of the following conditions occur for the SCCU.

    1. Catastrophic Power Failure
    2. Temperature in excess of critical level
    3. Normal Power Off.

Thermal Check Indicator - This indicator is located on Panel A Figure 10-4. The indicator will be turned on when the SCCU operating temperature is within approximately 10 degrees of the thermal shut- down temperature.

Power Sequence Complete Indicators - These indicators are located on Panel A, Figure 10-4. The indicator will be turned on when the last DC power supply has sequenced on, to indicate that all DC voltages are available to the associated logic circuits. The in- dicator will be turned off when the first power supply in the power down sequence is turned off. Three indicators are provided, one for each logically controlled unit.

MAINTENANCE PANELS

The CC contains three maintenance panels, one for each of the
internal control units.  Each panel provides the controls and
indicators necessary for maintenance and test of the associated
unit, and are intended for use by maintenance personnel only.
The panel for the SCCU is located on the internal logic gate D,
while each of the RCU maintenance panels are located on gate A
and B for RCU number 1 and RCU number 2 respectively.

SCCU Maintenance Panel

The SCCU Maintenance Panel (Figure 10-11) contains the controls and
indicators necessary for maintenance and test of the SCCU.  The
panel also has been designed to permit manual test of the attached
2821 control unit.

Controls

Lamp Test - Depressing this switch turns on all indicators on the
maintenance panel.

Test-Operate - When this two position toggle switch is placed in
the Test position all controls on the Maintenance panel are enabled
and the System Console Test Mode on the operators panel and the
Test indicator on the maintenance panel are turned on.  In the
Operate position, normal operation of the SCCU is enabled and the
two test mode indicators are turned off.

Marginal Check Adjust - Two controls are provided on the maintenance
panel to allow manual +6 power supply voltage excursion to be applied
to the SCCU logic to assist in the detection of marginal circuitry.
The controls, designated B MC Adjust and C MC Adjust, are used to
adjust the B or C power supply system.  An indicator is provided
above each control and is turned on when the control is moved from
its nominal setting.

Control Unit Select - The Control Unit Select is a four position
rotary switch which will select either the 2821 or one of the three
SCCU IOCE interfaces to be connected to the Maintenance panel
circuitry.  When this switch is in the 2821 position the functions of
theI/O Select switch on the operators panel are disabled provided
the unit is in Test.

Address Switches - Nine toggle switches (Parity Insert, 0, 1, 2, 3,
4, 5, 6, 7,) are provided on the panel to manually enter the address
of a device to be tested.

Bus Out Switches - Nine toggle switches (Parity Insert, 0, 1, 2, 3,
4, 5, 6, 7) are provided on the panel to manually enter data or
commands for the selected control unit.

Control Out Switches - Five toggle switches designated Address,
Select, Command, Service, and Suppress are provided on the panel to
select control functions for the addressed device.  The test cir-

10-68
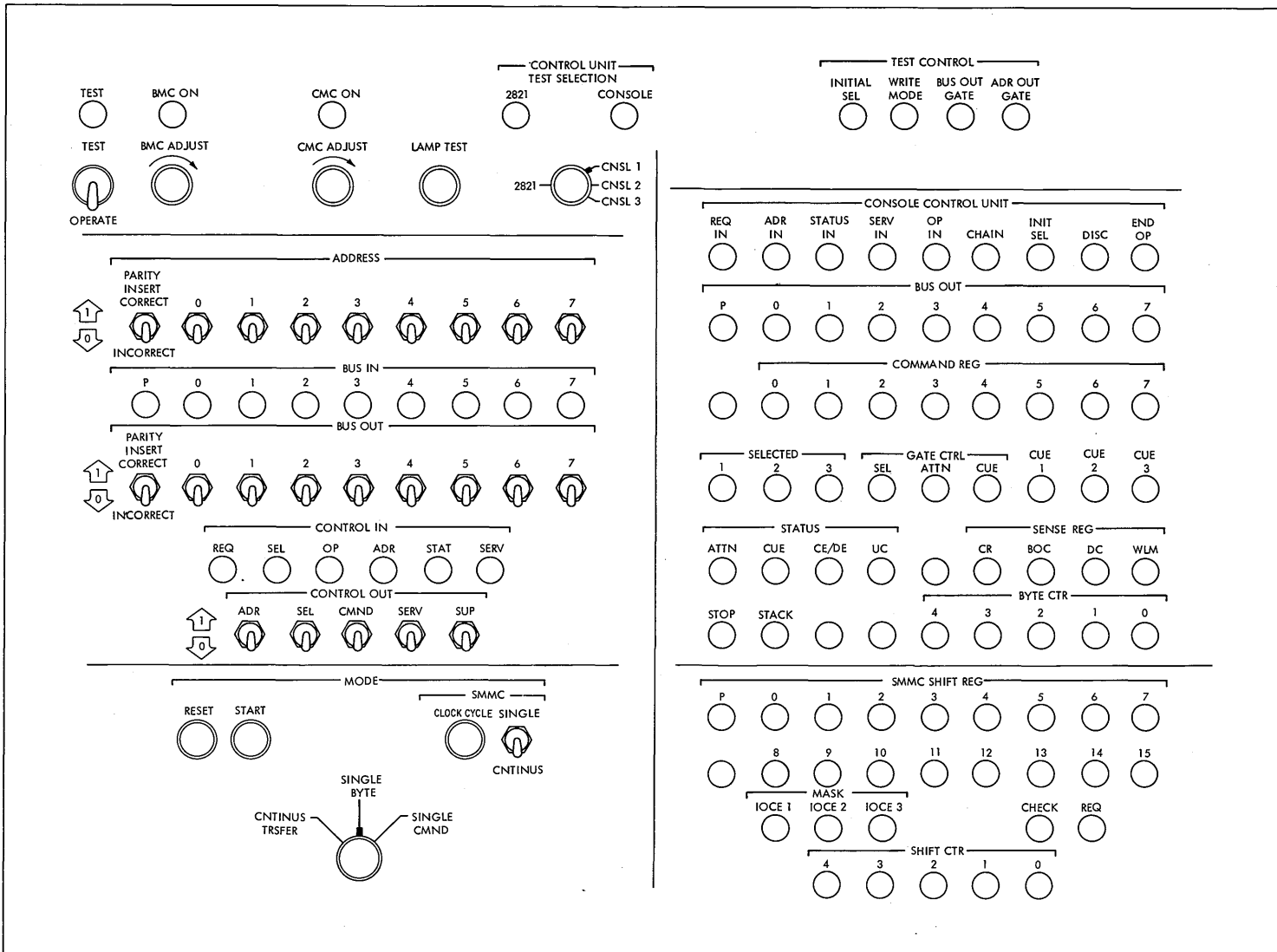
•Figure 10-11. SCCU Maintenance & Test Panel

cuitry automatically encodes the control lines to correspond to
the control function selected.  These switches are used when in
Single Command mode.

Reset - Depression of the Reset pushbutton resets the logic associat-
ed with the maintenance and test panel and resets the selected control
unit.

Start - Depression of the Start pushbutton when in test mode in-
itiates an address, command and/or data transfer as specified by the
Mode Selection switch.

Clock Cycle - This pushbutton, enabled when the Single-Continuous
switch is in the Single position, permits one step of the SMMC
shift clock for each depression of the pushbutton.

Single-Continuous - This two position toggle switch is provided to
allow single-cycle operation of the SMMC shift clock.  When in the
Single position the SMMC shift clock is stepped once for each
depression of the Clock Cycle pushbutton.  When in the Continuous
position the clock steps at its normal rate.

Mode Select Switch - The Mode Select switch is a three position
Rotary switch which will select the test panel mode of operation
for the generation of commands and/or data from the panel.

     In the Single Command Mode, the Control Out switches are
activated by depression of the Start pushbutton, allowing the trans-
fer of one control line sequence to the selected control unit.

     In the Single Byte mode, the test logic is conditioned to auto-
matically sequence the interface control lines.  This mode  of oper-
ations allows the operator to transmit or receive a single byte of
data for each depression of the Start pushbutton.

     In the Continuous Transfer mode of operation, data is trans-
mitted or received continuously after depression of the Start
pushbutton.  The operation is terminated when the selected control
unit returns status or by the operator switching to Single Byte
or Single Command Mode.

Test Panel Indicators

Test - This indicator is on when the Test-Operate switch is in the
Test position.

MC On Indicators - Two indicators designated B MC On and C MC On are
provided on the maintenance panel.  Each indicator, when on, indicates
that the associated MC Adjust control is adjusted to a position which
will cause the associated +6 volt power supply to have an output
value either above or below its nominal value.

Control Unit Select Indicators - Two indicators designated 2821 and
Console indicate which control unit is selected for connection to
the maintenance test panel.

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Bus In Indicators - Nine indicators designated P, 0, 1, 2, 3, 4, 5, 6, 7, display the Address, Data, Status, or Sense byte being received from the control unit connected to the test circuitry.

Control In Indicators - Six indicators designated Request, Select, Operational, Address, Status and Service display the Control In signals being received from the selected control unit.

Test Control Indicators - Four indicators designated Initial Select, Write Mode, Bus Out Gate, and Address Out Gate are turned on when the associated internal control latches of the test circuitry are set.

System Console Control Unit Indicators

A group of indicators are provided to indicate the set condition of internal control latches for the SCCU. The indicators are operational in both test and operational modes.

Interface In Tag Indicators - Five indicators designated Request In, Address In, Status In, Service In and Operational In display the status of the associated In Tag signal. Each indicator is on when the corresponding latch is set by the SCCU attempting to raise the corresponding interface line to the IOCE.

Chain - This indicator is on when command chaining is indicated by the IOCE.

Initial Select - This indicator is on during the SCCU initial selection sequence.

Disconnect - This indicator is on when the SCCU detects a Halt I/O command from the IOCE.

End Operation - This indicator is on when the SCCU is in the process of ending an operation.

Bus Out Indicators - Nine indicators designated P, 0, 1, 2, 3, 4, 5, 6, 7, display the data or command byte being received by the SCCU from the IOCE.

Command Register Indicators - Eight indicators designated 0, 1, 2, 3, 4, 5, 6, 7, display the contents of the SCCU command register.

Selected 1, 2, 3 - Indicators are on when the associated IOCE is actively working with the SCCU.

Gate Control Indicators - Three indicators designated Sel. (Select), Attn (Attention) and CUE (Control Unit End) indicate the type of cycle in process with the IOCE.

Control Unit End Indicators - Three indicators designated CUE 1, CUE 2, and CUE 3 indicate pending control unit end status for each IOCE.

Status - Four indicators designated Attention (ATTN), Control Unit
End (CUE), Channel End/Device End (CE/DE) and Unit Check (UC) dis-
play the status of the SCCU.

Sense Register - Four indicators designated Command Reject (CR),
Bus Out Check (BOC), Data Check (DC) and Wrong Length Message (WLM)
display the contents of the Sense Register in the SCCU.

Stop - This indicator is on when the SCCU has received a "Stop" (byte
count equals zero) from the IOCE.  It is turned off when Channel End
and Device End status is returned and accepted by the IOCE.

Stack - This indicator is turned on when status has been stacked at
the SCCU.  It is turned off when the stacked status is accepted by
the IOCE.

Byte Counter - These 5 indicators display the contents of the SCCU
Byte Counter.

SMMC Interface, Register and Latch Indicators

Twenty-seven indicators are provided for indication of the internal
registers and control latches associated with the SMMC interface
portion of the SCCU.

SMMC Shift Register - Seventeen indicators display the contents of
bits P, 0-15 of the SMMC shift register.

IOCE Mask Indicators - These indicators display which IOCE is en-
abled to receive an SMMC request (Attention).

Check - This indicator is on when a parity error has been detected on
shift out to the SMMC.

Request - This indicator is on when a request signal is pending from
the SMMC.

Shift Counter - These indicators display the contents of the SMMC
Shift Counter contained in the SCCU logic.

RCU Maintenance Panel

The RCU maintenance panel (Figure 10-12) contains the controls and
indicators required to exercise and test the RCU internal logic
functions and also provides controls for marginal check, power con-
trol and lamp test.

Controls

Test-Operate - This toggle switch is used to enable the power and
test controls of the maintenance panel.  When placed in the Test
position with the RCU in State Zero the RCU is logically isolated
from the system and the maintenance controls are functional.  If
placed in the Test position while the RCU is in State 1, 2, or 3,
the RCU remains operational with the system and the maintenance

10-72
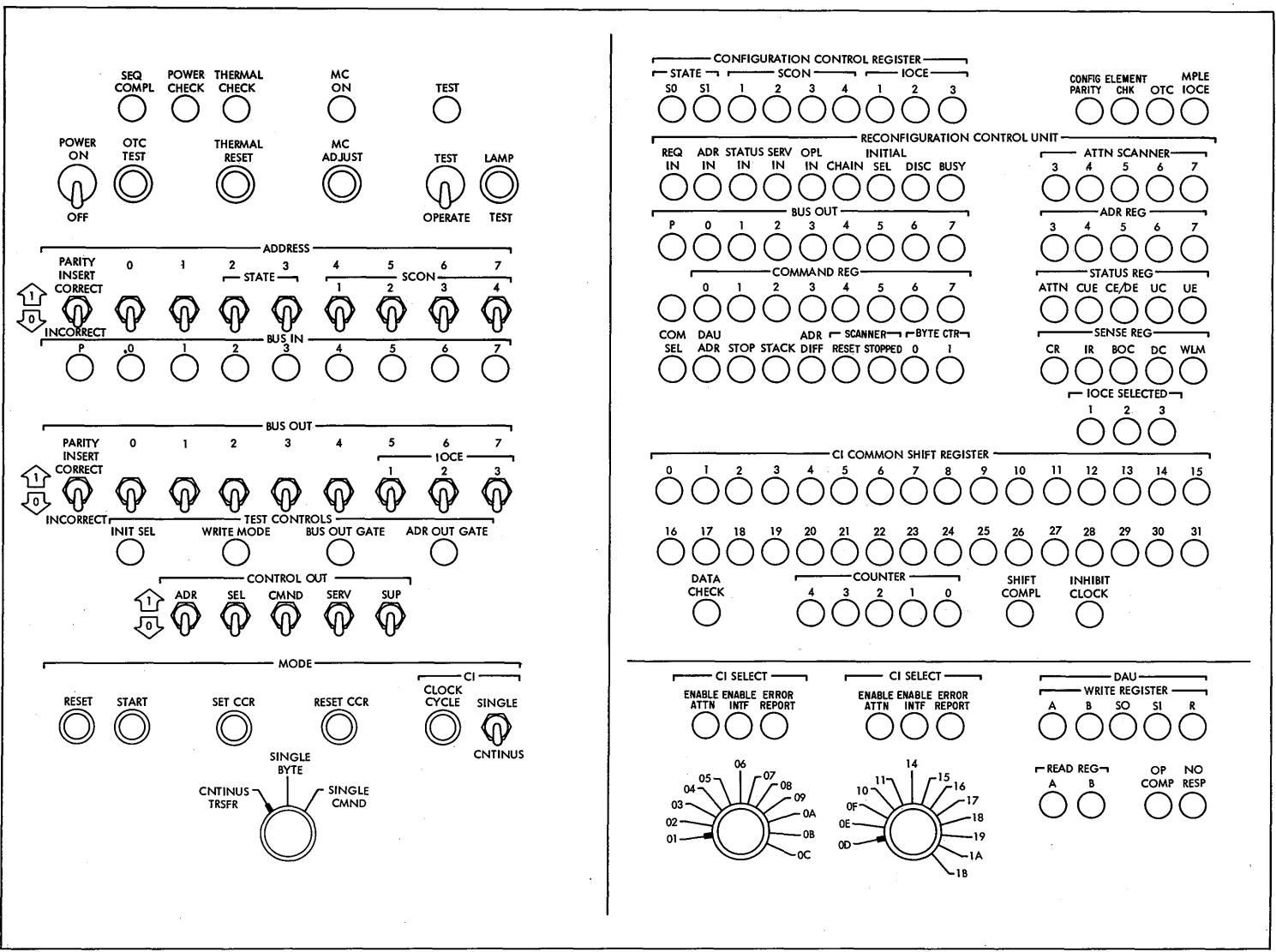
•Figure 10-12.    RCU Maintenance & Test Panel

controls remain disabled.

The following controls located on the RCU maintenance panel are active for all states of the RCU regardless of the Test-Operate switch position.

Lamp Test - When this pushbutton is depressed all indicators on the maintenance and test panel are turned on.

Thermal Reset - When depressed this pushbutton will reset the thermal check condition if the internal temperature has dropped to a normal operating level.

Marginal Check Adjust - This control is used to manually provide voltage excursions on the +6 volt power supply to assist in the detection of marginal circuitry in the RCU logic.

OTC Test - This pushbutton, when depressed, simulates an Out of Tolerance check condition. A pulsed ELC is generated by the RCU and sense byte 2, bit 7 is set and remains until the pushbutton is released.

CI Select - These two rotary switches allow selection of two Configuration Interfaces for indication of the associated Enable Attention, Enable Interface and Error Report latches. One switch provides selection of interfaces 1 through 0C while the second switch provides selection for the remainder of the configuration interfaces.

The following controls are enabled when the RCU is in State Zero, has the Test-Operate switch in the Test position.

Reset - Depression of the Reset pushbutton resets the logic associated with the maintenance and test panel and prepares the RCU logic for initial Selection.

Start - Depression of the Start pushbutton initiates an address, command and/or data transfer as specified by the Mode Selection.

Clock Cycle - This pushbutton, enabled when the Single-Continuous switch is in the Single position, permits one step of the RCU clock for each depression of the pushbutton.

Single-Continuous - This two position toggle switch controls the RCU clock stepping. When in the Continuous position, clock stepping is at a normal rate; when in the Single position, the clock steps once for each depression of the clock cycle pushbutton.

Address Switches - The nine address switches designated Parity Insert, 0-7 permit address selection of the device to be tested.

Bus Out Switches - The Nine Bus Out switches designated Parity Insert, 0-7 are provided to manually enter data or commands to the

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device selected by the address switches.

Control Out Switches - The five toggle switches designated Address, Select, Command, Service, and Suppress are provided on the panel to select control functions for the addressed device. The Test circuitry automatically encodes the control lines to correspond to the control function selected.

Mode Select - The Mode Select is a three position rotary switch which will select the test panel mode of operation for the generation of commands and/or data from the panel.

In the Single Command Mode, the Control Out switches are activated by depression of the Start pushbutton, allowing the transfer of one control sequence to the RCU.

In the Single Byte mode, the test logic is conditioned to automatically sequence the interface commands. This mode of operation allows the operator to transmit or receive a single byte of data for each depression of the Start pushbutton.

In the Continuous Transfer mode of operation, data is transmitted or received continuously after depression of the Start pushbutton. The operation is terminated by depressing the Reset pushbutton or by the operator switching to Single Byte or Single Command mode.

Set CCR - Depression of this pushbutton causes the CCR in the RCU to be set with the value contained in bits 2-7 of the address switches and bits 5, 6, and 7 of the bus out switches. The State bits are set from bits 2 and 3 of the address switches, SCON bits from bits 4-7 of the address switches and the IOCE bits from bits 6-7 of the Bus Out switches.

Reset CCR - Depression of this pushbutton resets the entire RCU including the State bits, SCON bits, and IOCE bits in the RCU CCR. The $P_0$ and $P_3$ positions in the CCR are set to ones.

Indicators

The following indicators display the status of the RCU power, marginal check, and test mode are located in the upper left section of the panel.

Sequence Complete - This indicator is turned on when the last DC power supply has sequenced on, and indicates that all DC voltages are available to the RCU logic circuits. The indicator is turned off when the first DC power supply is turned off and is a duplicate of the Power Sequence complete indicator located on Panel A of the CC operators panel.

Power Check - This indicator duplicates the RCU Power Check indicator on Panel B of the CC operator panel. It is turned on when any or all of the following conditions occur:

1. Catastrophic power failure
2. Temperature in excess of critical level
3. Normal power off

Thermal Check - This indicator is turned on when the RCU operating temperature is within approximately 10 degrees of the thermal shutdown temperature.

MC On - This indicator is turned on when the MC Adjust control is positioned to cause the associated +6 volt power supply to have a output value either above or below its nominal value.

Test - This indicator is turned on when the Test-Operate switch is placed in the Test position, the RCU is in State Zero, and the RCU has been logically connected to the test panel circuitry. When on, operation of the maintenance and test panel is enabled.

The following group of indicators on the maintenance and test panel display the status of the test bus and various control latches associated with operation of the test controls.

Bus In Indicators - Nine indicators designated P, 0-7 display the Address, Data, Status, or Sense byte being received from the RCU by the test circuitry. These indicators are always active.

Test Controls Indicators - Four indicators designated Initial Select, Write Mode, Bus Out Gate, and Address Out Gate indicate the status of internal control latches in the test panel logic.

Initial Select - Indicates that the test panel is in an initial selection cycle.

Write Mode - Indicates that a write command has been issued and the test logic is conditioned to transmit data.

Bus Out - Indicates that data from the Bus Out switches is being gated to the RCU interface.

Address Out - Indicates that the contents of the Address Switches is being gated to the RCU interface.

The following group of indicators display the status of pertinent internal RCU registers and control latches. The indicators are active regardless of the position of the Test-Operate switch.

Configuration Control Register (CCR) - Nine indicators are provided to display the contents of the CCR. The indicators are designated S0 and S1 for the state bits; 1, 2, 3, 4 for the SCON bits; and 1, 2, 3, for the IOCE communication bits.

Configuration Parity - This indicator is turned on when the CCR contains incorrect parity.

Element Check - This indicator is turned on when the RCU has detected a condition which generates an Element Check (ELC).

OTC - This indicator is on when the internal temperature of the RCU is above the warning level. (Approximately 10 degrees less than shutdown.) The indicator is also turned on when the OTC pushbutton is depressed.

Multiple IOCE - Any time the contents of the CCR has more than one IOCE bit set, this indicator is turned on.

Interface In Tag Indicators - Five indicators designated Request In, Address In, Status In, Service In, and Operational In display the status of the In Tag control latches in the RCU.

Chain Indicator - This indicator displays the contents of the chain latch in the RCU, which is set when command chaining is indicated by the IOCE.

Initial Select - This indicator is turned on when the RCU is in an initial selection sequence.

Disconnect - This indicator is turned on upon receipt of an interface disconnect sequence at the RCU.

Busy - This indicator is turned on when the RCU is busy.

Attention Scanner - Five indicators designated 3, 4, 5, 6, and 7 display the address of the device being tested by the attention scanner for an error report.

Bus Out Indicators - These nine indicators designated P, 0-7 display the contents of bus out from the IOCE or test panel switches being received at the RCU.

Address Register - Five indicators designated 3-7 display the device address contained in the RCU address register.

Command Register - Eight indicators designated 0-7 display the contents of the RCU command register.

Status Register - Five indicators designated attention (Attn), Control Unit End (CUE), Channel End-Device End (CE/DE), Unit Check (UC), and Unit Exception (UE) display the contents of the internal RCU status register.

Common Select - This indicator displays the contents of the common select control latch. When on, a selection of either a CI or DAU is indicated.

DAU Address - This indicator when on, indicates the common select is for a DAU address. When off the common select is for a CI address.

Stop - This indicator displays the contents of the stop latch, which is set when a stop command (byte count equals zero) is received by the RCU.

Stack - This indicator is turned on when the RCU status has been stacked in the control unit.

Address Different - This indicator is turned on when the RCU received an address during initial selection that is not equal to the address contained in the address register.

Scanner - Two indicators designated Reset and Stopped indicate the status of the attention scanner.

Byte Counter - Two indicators designated 0-1 are provided to display the binary contents of the RCU byte counter.

Sense Register - Five indicators designated Command Reject (CR), Intervention Required (IR), Bus Out Check (BOC), Data Check (DC), and Wrong Length Message (WLM) display the contents of the RCU sense register.

IOCE Selected - Three indicators designated 1, 2, and 3 display the contents of the IOCE selected latches which are used to determine the actual IOCE configuration connection.

CI Common Shift Register - Thirty two indicators designated 0-31 display the contents of the CI common shift register.

Data Check - This indicator is turned on when a data check is detected at the output of the CI common shift register.

Counter - Five indicators display the contents of the shift control counter. This counter controls the shifting of data into or out of the CI common shift register.

Shift Complete - This indicator is turned on at the completion of shifting data.

Inhibit Clock - This indicator is turned on when the clock has stepped the appropriate number of times for the particular device addressed, and indicates that the interface is no longer transmitting clock pulses.

CI Select Indicators - Two groups of three indicators designated Enable Attention, Enable Interface, and Error Report are provided to monitor the respective control latches in the CI logic. The indicators are turned on when the respective latches are set in the logic selected by the CI Select Switch.

DAU Write Register - Five indicators designated A, B, S0, S1, and Reset display the contents of the DAU output register.

DAU Read Register - Two indicators display the contents of the input DAU Read Register. These indicators are designated A and B.

DAU Operation Complete - This indicator is turned on when an operation directed to a DAU is completed.

DAU No Response - This indicator is turned on when an attempted DAU operation results in no response from the DAU.
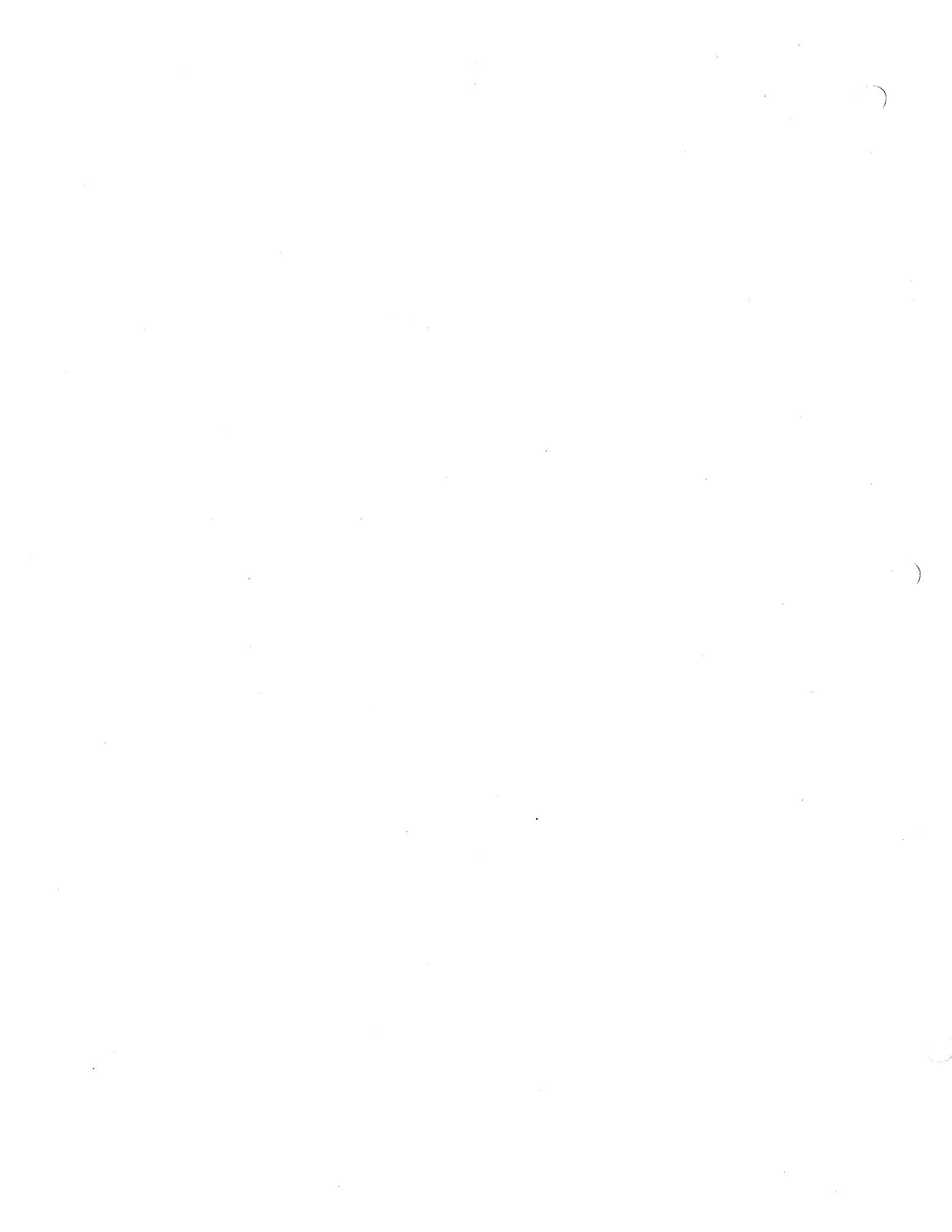
The IBM input/output (I/O) devices used with the 9020 D/E Systems
provide each system with external storage facilities and means of
communications with the external environment.  The 9020 D/E I/O
configurations are shown in Figure 11-1.

APPLICABLE IBM SYSTEM REFERENCE LIBRARY DOCUMENTS

The following IBM System Reference Library documents are provided to
describe the operation and features of the indicated IBM units and
devices used with the IBM 9020 system.

> IBM 2400 and 2816 Model 1 Principles of Operation -
>    Form No. A22-6866
>
> 2803  Model 1 Tape Control Unit
>
> 2401  Model 2 Magnetic Tape Unit
>       Nine Track Read-Write Head Option
>
> 2401  Model 3 Magnetic Tape Unit
>       Nine Track Read-Write Head Option
>
> IBM 2821 Control Unit - Form No. A24-3312
>
> 2821  Model 1 Control Unit
>       1403-2 Attachment Feature
>       Universal Character Set Adapter Feature
>
> 2821  Model 2 Control Unit
>       1403-2 Attachment Feature
>
> IBM 1403 Printer - Form No. A24-3073
>
> 1403  Model 2 Printer
>       Interchangeable Chain Cartridge Adapter Feature
>       Universal Character Set Feature
>
> IBM 2450 Card Read Punch - Component Description and Operating
>    Procedures - Form No. A21-9033
>
> IBM Direct Access Storage Facility - Form No. GA26-1610
> 2314 Model A1 Storage Control Unit
> 2312 Model A1 Disk Storage Unit
> 2318 Model A1 Disk Storage Unit

Only those portions of these documents relating to the units,
devices and features specified in Contract FA64WA-5223, and its
amendments, are applicable.  Features and modifications made to this
equipment specifically for 9020 System applications are described
in the following sections of this chapter.

GENERAL CHARACTERISTICS

The I/O devices supplied and used with the IBM 9020 System are:

> Magnetic Tape Units
> Disk Storage Units
> Card Read/Punch Unit
> Line Printer Unit
> Printer Keyboard Units

These I/O devices connect to the system through necessary Control Units, Adapters, and switches. Where required, special system control connections are made directly to the Computing Elements. The connection of I/O devices in the 9020 D/E systems are shown in Figure 11-1.

Magnetic Tape Equipment

The IBM 9020 System uses the IBM 2803-1 Tape Control Unit (TCU) which can control as many as eight IBM 2401-2/3 Magnetic Tape Units (TU). Only one TU at a time may transmit data to or receive data from the TCU.

A program controlled I/O Interface Switch feature and a Configuration Control and Monitoring Feature have been incorporated in the TCU for use with the IBM 9020 System to allow the TCU to be functionally connected to one Selector Channel in each of two IOCE's.

The characteristics of the IBM 2401-2/3 Magnetic Tape Units are listed below in Table 11-1.

Table 11-1. Characteristics of IBM 2401-2/3 TU's

| Characteristics | Model 2 (9-Track) | Model 3 (9-Track) |
|---|---|---|
| Density (Bytes/inch) | 800 | 800 |
| Data Rate (Bytes/Second) | 60,000 | 90,000 |
| Tape Speed (in./sec.) | 75.0 | 112.5 |
| Interrecord Gap (in.) | 0.6 | 0.6 |
| Rewind Time - Full Reel (minutes) | 1.5 | 1.0 |
| Rewind Unload (minutes) | 1.6 | 1.0 |
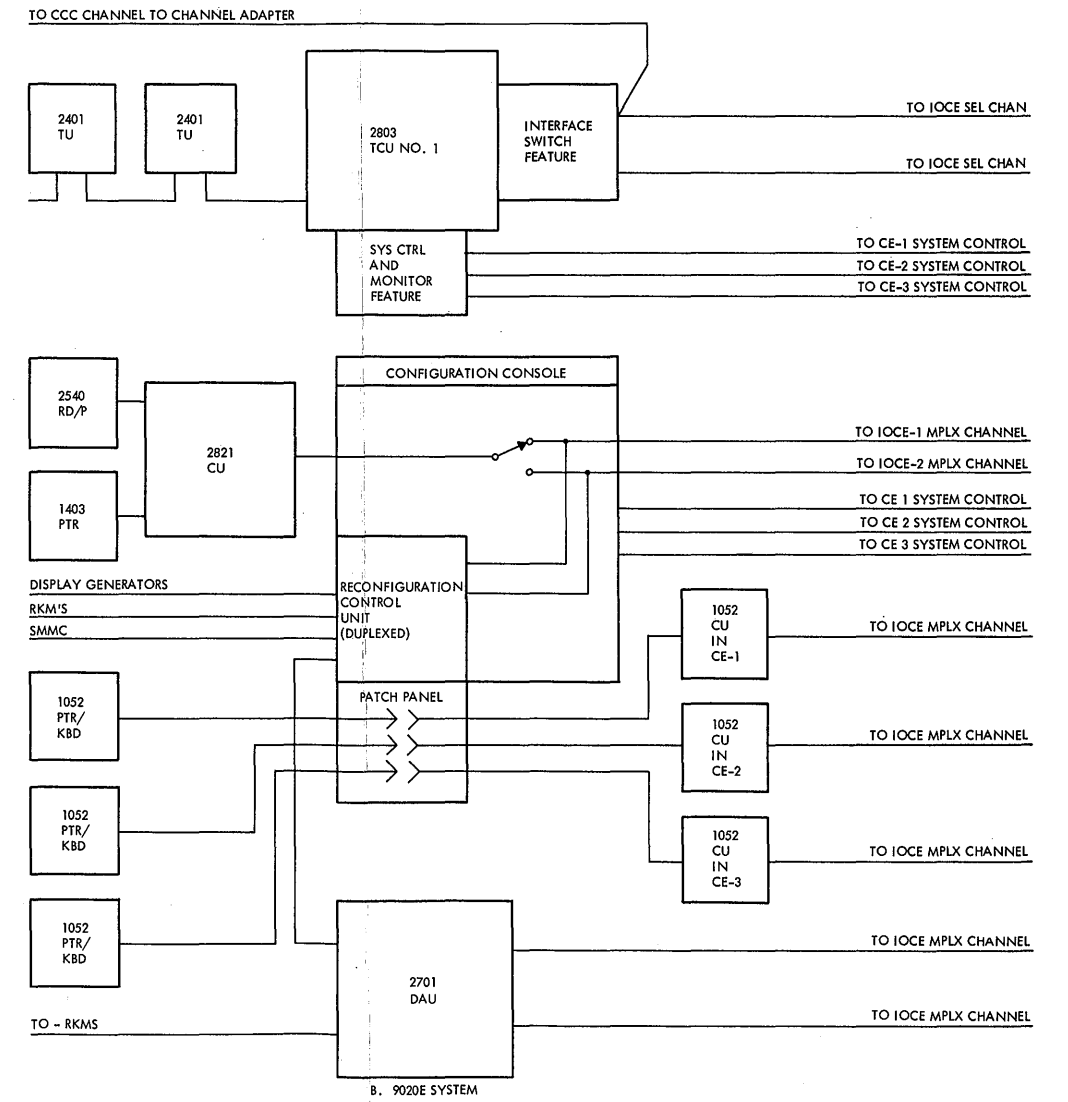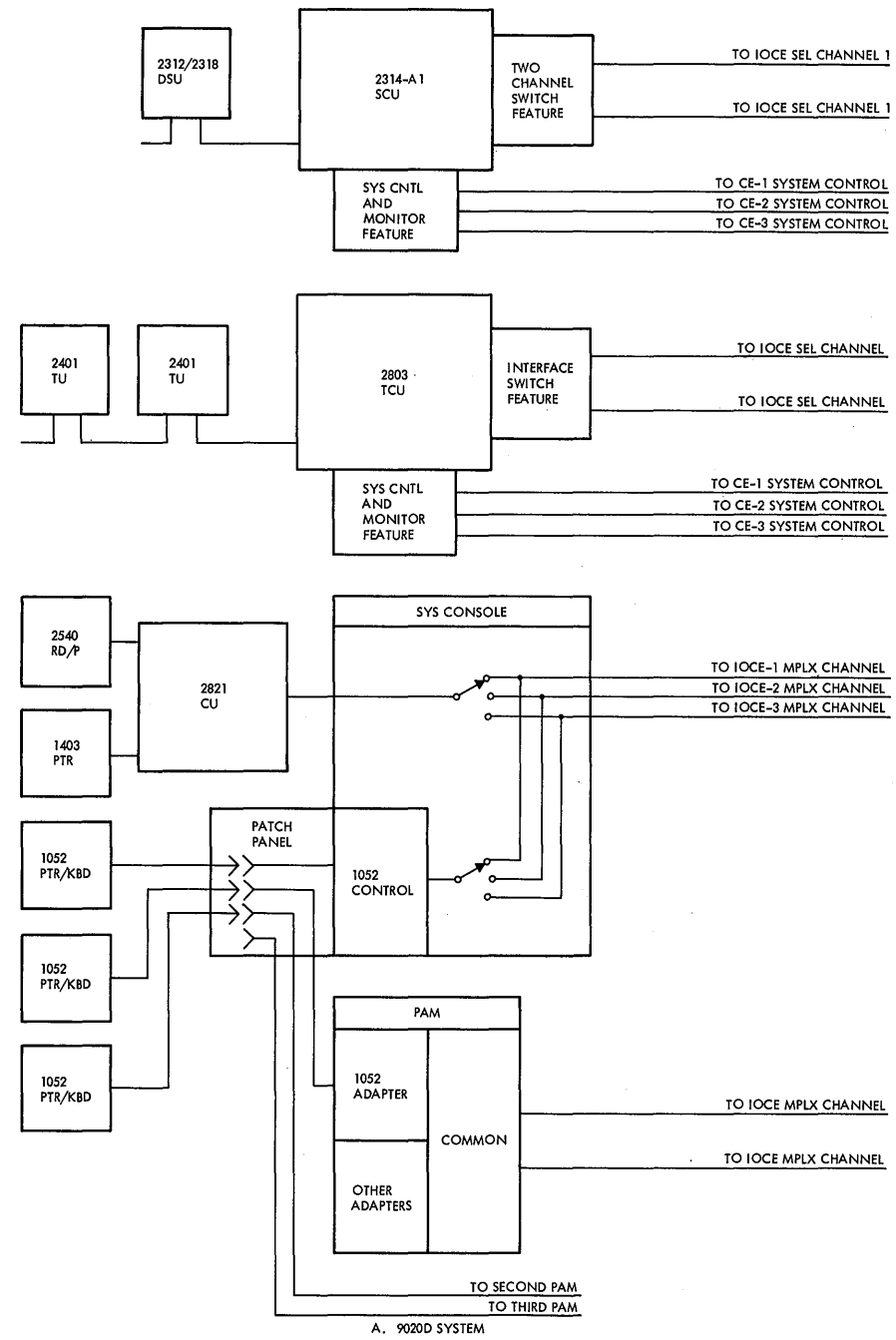
•Figure 11-1.   I/O Device Connections

## Disk Storage Equipment

The IBM 9020 System uses the IBM 2314-A1 Storage Control Unit (SCU) which can control IBM 2312-A1 and/or 2318-A1 Disk Storage Units (DSU). The combination of SCU and one or more DSUs is referred to as the IBM Direct Access Storage Facility (DASF).

The 2312-A1 DSU contains one disk drive; the 2318-A1 contains two disk drives. A maximum of five DSUs may be attached to a single 2314-A1. 2312-A1 and 2318-A1 DSU may be intermixed. However, no more than nine disk drives may be attached to a 2314-A1.

A program-controlled I/O Interface switch feature and a Configuration Control and Monitoring Feature have been incorporated in the SCU for the IBM 9020 system. These features allow the SCU to be functionally connected to one Selector Channel in each of two IOCEs.

The 2316-01 Disk Pack used with the DSUs is a removable unit with a storage capacity of 29,176,000 bytes of data. The average access time is 60 ms.

## Card Read Punch-Line Printer Equipment

The IBM 9020 System uses the IBM 2540 Card Read-Punch and the IBM 1403-2 Printer connected to the IBM 2821-1 or 2 Control Unit (CU). The CU is attached to the system through the Console to an IOCE multiplexor channel. The Console provides facilities and manual controls to switch the CU to any one of the IOCE's. In the event that the Console should be inoperable for any reason, the 2821 CU may be connected (by manual cable reconnection following appropriate safety and system operating procedures) in the Multiplexor Cable Loop of any one of the IOCE's for operation by only the one IOCE.

The 2821 CU controls the 2540 and 1403-2, and permits these devices to operate logically as separate units, selected by unique addresses and controlled by individual commands. It contains code translation facilities to convert 8 bit EBCDI code to Extended Hollerith Code and vice versa.

The 2540 Card Read-Punch can read up to 1000 cards per minute and punch up to 300 cards per minute.

The 1403-2 Printer has 132 print positions per line and prints up to 600 lines per minute.

## Printer Keyboard

The IBM 9020 System uses IBM 1052-7 Console Printer Keyboards. These units are physically located in the Operator area of the System Console.

System Console Printer Keyboard, 9020D System

The control unit function for this device is contained in the System Console, and provides facilities and manual controls to connect the device to the Multiplexor Channel of any one of the IOCE's.

Auxiliary Printer Keyboards, 9020D System

The control unit function for these devices is contained in each of the PAM units. Provision is made to connect the devices to any of the PAM's.

Printer Keyboards, 9020E System

The control unit functions for these devices are contained in the CE's. One keyboard is connected via its control unit to one IOCE; the other keyboard is connected via its control unit to the second IOCE.

The nominal printer character rate on writing operations (output) is 14.8 characters/second. The printer will print 10 characters/inch horizontally and 6 lines per inch vertically. It is equipped with a pin feed platen which provides a 12 5/8 inch maximum writing line on 13 5/8 inch overall paper width. The pin feed perforations are spaced 13 1/8 inch horizontally from hole center to hole center.

FUNCTIONAL CHARACTERISTICS

IBM 2803 TCU with 2401 TU's

The IBM 2400 series magnetic tape equipment consists of the 2401,
2402, 2403, 2404, 2803, and 2804 units.  The IBM 9020 System is
provided magnetic tape capability by use of the 2803 Tape Control
Unit, which houses read-write, and control functions to operate up
to eight 2401 Magnetic Tape Units.  The standard functional charac-
teristics of this equipment, as well as any 2400 series combination
of tape control and tape unit are presented in the IBM System
Reference Library Document, IBM-2400 and 2816 Model 1 (Form A22-
6866) submitted with this specification.  The data conversion
feature and the 2816 Switching Unit described in this document are
not applicable to this specification.  Additions to the 2803 TCU
for use with the 9020 System are described in the sections that
follow.

     The IBM 2400 Series tape equipment used in the 9020 System has
been designed to provide protection for tape recorded data, includ-
ing safeguards against inadvertent magnetic erasure as well as
against physical damage to the recording medium.  A file protection
feature is provided in each tape unit that allows the operator to
guard against unwanted tape over-writing or erasure.  Equipment
interlocks terminate or prevent tape motion when abnormal conditions
occur.

     To preclude damage to the tape when power is restored following
a prime power loss, each tape unit, if not already in an unloaded
status, will perform an unloading operation and will become NOT
READY.  Operator intervention is then required to initiated a local
load-rewind operation so that the tape unit may be made READY.  A
program routine is required to re-position the tape to the desired
data record.

I/O Interface Switch Feature

This feature allows the TCU to be physically connected to two IOCE
selector channels, and controls the functional connection of the
I/O Interface so that it may operate with only one of these channels
at any one time.

Interface Selection.  The first channel to issue a standard TCU
command (Read, Write, Control, Sense, Test I/O) will activate the
switch to functionally connect the I/O Interface to the channel
which issued the command.  This functional connection will be main-
tained until the channel commands the switch to release the Inter-
face, or until broken by a System Reset or a SCON operation.

Interface Release.  A channel which is functionally connected to the
I/O Interface may break the connection by issuing the following
command:

                    Release          0000          1011

Status Byte response to this command will be the same as for all
standard TCU commands. Execution of this command if the TCU is
configured to both channels will return the Interface Switch to the
neutral position (interface functionally connected to neither chan-
nel).

Interface Busy Condition. A channel which issues a command to the
TCU at a time when the Interface is functionally connected to the
other channel (interface selected and not yet released) will receive
a Control Unit Busy status indication in response to the command. A
subsequent Release operation by the functionally connected channel
will cause a Control Unit End status interruption to be signalled to
the channel that previously received the CU Busy indication and the
TCU will be functionally connected to that channel.

Configuration Control and Monitoring Feature

This feature provides a communication path and necessary circuitry
for the TCU to be controlled by and to respond to the 9020 System
Configuration Control and Monitoring circuitry. By means of this
feature, the CE establishes the system configuration with respect
to the TCU and the TCU reports conditions of system significance to
the CE.

Configuration Control Register (CCR). The TCU is provided with a
register to exercise control over its interfaces and manual controls.
Figure 11-2 defines the bit assignments in the CCR.

Set Configuration Control(SCON). The CCR will be set with informa-
tion transferred bit parallel from the CE over the TCU-CE Interface.
The TCU will indicate that the information was received with proper
parity by sending a response to the CE.

CCR Parity Check. The CCR is continuously monitored for incorrect
parity indication. If a parity check is detected, an ELC interrup-
tion will be generated and Bit 5 of Sense Byte 4 will be set.

SCON Field Zero Check. The SCON field is continuously monitored to
detect an "all zero" condition. Detection of this condition, when
the TCU is in States One, Two, or Three, will cause the SCON bit
gating of the TCU-CE Interface to be bypassed and will allow the
acceptance of SCON information from any CE.

CCR Reset. The reset condition of the CCR is as follows:

|  |  |
|---|---|
| State Bits | "0      0" |
| SCON Bits | All "1's" |
| IOCE Bits | All "0's" |

The CCR is reset only by the Power On Reset function or by a System
Reset signal.

State Control of TCU. Table 11-2 shows the status of interfaces and
controls for the various TCU "States."

| STATE | | | SCON | | | | | IOCE | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PO | SO | S1 | 1 | 2 | 3 | 4 | P3 | 1 | 2 | 3 |

A "1" IN ANY OF THESE BITS INDICATES TCU I/O INTERFACE MAY ACCEPT COMMANDS FROM THE IOCE WITH THE CORRESPONDING NUMBER. (NOTE: EACH TCU WILL BE PHYSICALLY CONNECTED TO ONLY TWO IOCE'S.)

ESTABLISHES ODD PARITY FOR THE CONTENTS OF THE IOCE BITS.

A "1" IN ANY OF THESE BITS INDICATES THAT THE TCU MAY ACCEPT CONFIGURATION CONTROL INFORMATION FROM THE CE WITH THE CORRESPONDING NUMBER. (IF THIS FIELD CONTAINS NO "1'S", TCU WILL ACCEPT SCON FROM ANY CE.)

SPECIFY THE STATE THE TCU IS TO ASSUME:

| SO | S1 | STATE |
|---|---|---|
| 1 | 1 | THREE |
| 1 | 0 | TWO |
| 0 | 1 | ONE |
| 0 | 0 | ZERO |

ESTABLISHES ODD PARITY FOR THE COMBINED STATE AND SCON BITS.

Figure 11-2. TCU Configuration Control Register

Table 11-2. "State" Control of TCU

| State | Interfaces | | Diag. Aids | Off Line (Test) Sw. | Manual Controls | Power On/Off Switch |
|---|---|---|---|---|---|---|
| | I/O | CE | | | | |
| Three, Two, One | E | E | D | D | D | D |
| Zero-Online | E | E | E | E-Off | D | D |
| Zero-Offline | D | D | E | E-On | E | E |

Legend:  D - Disabled
         E - Enabled

In State Zero, with the Off Line (Test) switch in the off-line position, the TCU is isolated from external control and is completely under manual control.

Element Check Interruption (ELC). The TCU indicates the following conditions to the CE's by means of this interruption.

1. TCU over current condition

2. TCU power off condition

3. CCR parity check

Attention Status.  The TCU indicates that its internal temperature
has reached the thermal check level by setting the Attention bit in
the Status Byte.  Attention Status will be presented to the channel
on the next ending sequence or the next selection sequence, which-
ever occurs first.  The Attention bit will be cleared after it has
been presented to a channel.

Power Control Facilities

The power controls and indicators added to the TCU for operation
with the 9020 system are listed below.  A detailed explanation of
their function with respect to the system may be found in Chapter
12, System Power Controls.

> Element MPO Pull switch
>
> Power On/Off switch
>
> Power Sequence Complete indicator
>
> Thermal Check indicator
>
> Power Check indicator

The TCU is connected to the System Emergency Power Off
facility so that actuating the Emergency Pull switch at the System
Console will cause all output power from the TCU power control
compartment to be removed.

A DC Power switch has been provided to remove logic power from
the TCU logic gates.  This switch will be enabled only in State Zero
with Off Line (Test) switch On.

System Console Indicators

The following TCU indicators are displayed on the System Console:

| | |
|---|---|
| State Three | On when CCR State Bits are "11" |
| State Two | On when CCR State Bits are "10" |
| State One | On when CCR State Bits are "01" |
| State Zero | On when CCR State Bits are "00" |
| Logic Check | On whenever the TCU detects an equipment check condition |
| Power Check | On whenever the TCU detects a Power Check condition, a thermal warning condition, or has power off |

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Maintenance

Additions and modifications to the standard maintenance capabilities
have been made so that the circuitry added by the above features may
be exercised.

Command Simulation.  The manual command simulation circuitry is
modified to recognize and execute the Release command.

Data Entry.  The manual data entry switch outputs may be gated to
allow manual setting of the SCON, IOCE, and parity bits of the CCR.

Indicators.  Indicators have been added to display the contents of
the CCR and pertinent control functions.

OTC Test.  A pushbutton switch is provided to simulate a thermal
warning condition.

Interfaces

The TCU in the 9020 System communicates over three unique interfaces,
as described in Chapter 13.

        I/O Channel to Device Interface

        CE to TCU Interface

        TCU to System Console Interface

IBM 2314-A1 SCU with 2312-A1/2318-A1 DSUs

The IBM Direct Access Storage Facility consisting of an IBM 2314-A1
SCU and one or more IBM 2312-A1/2318-A1 DSUs provides high-volume,
on-line storage media capable of being directly addressed.  The
2316-01 Disk Pack consists of 11 flat, rotating disks which can store
up to 29,176,000 bytes of data.

The functional characteristics of the Direct Access Storage
Facility are presented in the IBM System Reference Library Document,
IBM 2314 Direct Access Storage Facility (Form GA26-1610).  The
special features for use with the 9020 System are described in the
following sections.

Two-Channel Switch Feature

This feature allows the SCU to be physically connected to two IOCE
selector channels, and controls the functional connection of the I/O
Interface so it may operate with only one of the channels at any one
time.  The SCU must have both IOCE communication bits on in the
Configuration Control Register to operate in the two-channel switch
mode.

Interface Selection.  The first channel to issue a standard SCU command will activate the switch to functionally connect the SCU to that channel.  This functional connection will be maintained until Channel End Status is presented to the channel for the operation or chain of operations which established the connection.  The switch then returns to a neutral position, capable of being selected from either channel.  An established connection may also be broken by a System Reset or by a SCON operation.

Interface Busy Condition.  A channel which issues a command to the SCU at a time when the interface is functionally connected to the other channel will receive a Control Unit Busy status indication. When the functional connection to the opposite channel is broken, Control Unit End Status will be signalled to the channel which previously received the Control Unit Busy status.

Configuration Control and Monitoring Feature

This feature provides a communication path and necessary circuitry for the SCU to be controlled by and to respond to the 9020 System Configuration Control and Monitoring circuitry.  By means of this feature, the CE establishes the system configuration with respect to the SCU, and the SCU reports conditions of system significance to the CE.

Configuration Control Register (CCR).  The SCU is provided with a register to exercise control over its interfaces and manual controls. Figure 11-3 defines the bit assignments in the CCR.

Set Configuration Control (SCON).  The CCR will be set with information transferred bit parallel from the CE over the SCU-CE Interface. The SCU will indicate that the information was received with proper parity by sending a response to the CE.

CCR Parity Check.  The CCR is continuously monitored for incorrect parity indication.  If a parity check is detected, an ELC interruption will be generated, and Bit 2 of Sense Byte 4 will be set.

SCON Field Zero Check.  The SCON field is continuously monitored to detect an "all zero" condition.  Detection of this condition, when the SCU is in States One, Two, or Three, will cause the SCON bit gating of the SCU-CE Interface to be bypassed and will allow the acceptance of SCON information from any CE.

CCR Reset.  The reset condition of the CCR is as follows:

    State Bits          "0     0"
    SCON Bits           All "1's"
    IOCE Bits           All "0's"

The CCR is reset only by the Power On Reset function or by a System Reset signal.
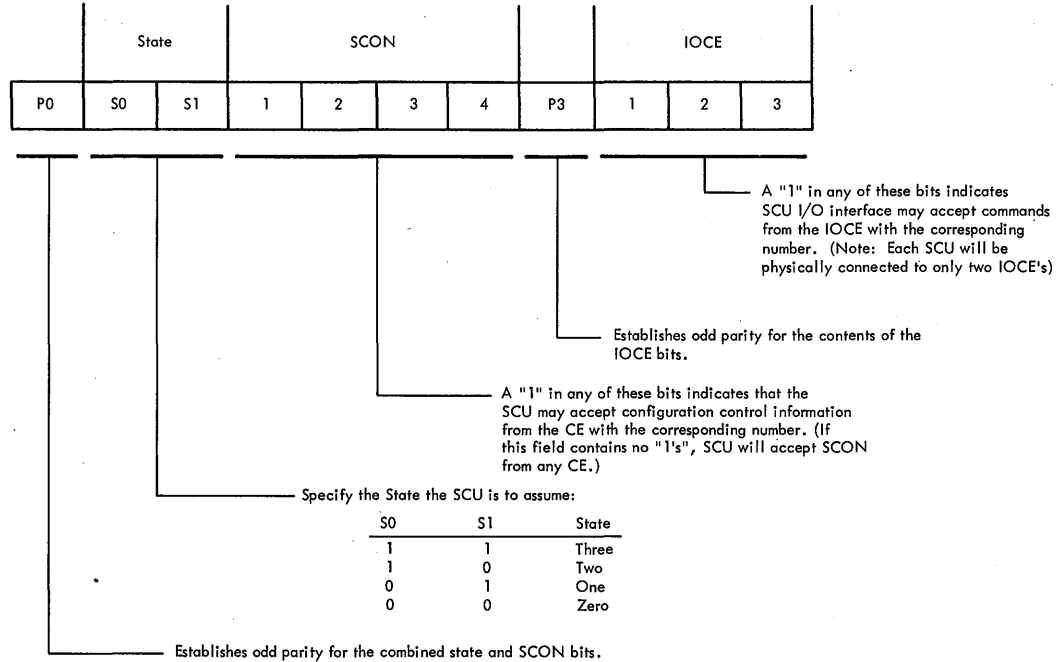
Figure 11-3.  SCU Configuration Control Register


State Control of SCU.  Table 11-3 shows the status of interfaces and controls for the various SCU "States."


Table 11-3.  "State" Control of SCU

| State | Interfaces I/O | Interfaces CE | Diag Aids | Off Line (Test) Sw | Manual Controls | Power On/Off Switch |
|---|---|---|---|---|---|---|
| Three, Two, One | E | E | D | D | D | D |
| Zero-Normal Mode | E | E | E | E | D | D |
| Zero-In Line Mode | E | E | E | E | E* | D |
| Zero-CE Mode | D | D | E | E | E | E |

Legend:   D - Disabled
          E - Enabled
          * - Micro-Diagnostic controls enabled.

    In State Zero, with the CE/Normal/In Line switch in the CE (Test) position, the SCU is isolated from external control and is completely under manual control.

Element Check Interruption (ELC).  The SCU indicates the following
conditions to the CEs by means of this interruption.

    1.  SCU over-current condition

    2.  SCU Normal power-off condition

    3.  CCR parity check

    4.  Out of Tolerance condition (OTC).

Thermal Check

The SCU indicates that its internal temperature has reached the
Thermal Check level (approximately 10° below the shutdown level) by
generating a pulsed Element Check to all CEs.  Bit 3 of sense byte 4
is also set.

Power Control Facilities

The power controls and indicators added to the SCU for operation with
the 9020 system are listed below.  A detailed explanation of their
function with respect to the system may be found in Chapter 12,
System Power Controls.

    Element MPQ Pull switch

    Main-Line On indicator

    Thermal Check indicator

    Power Check indicator

The SCU is connected to the System Emergency Power Off facility
so that actuating the Emergency Pull switch at the System Console
will cause output power from the SCU power control compartment to be
removed.

    A DC Power switch is available to remove logic power from the
SCU logic gates.  This switch will be enabled only in State Zero
with the CE/Normal/In line switch in the CE (Test) position.

System Console Indicators

The following SCU indicators are displayed on the System Console:

    State Three        On when CCR State Bits are "11".

    State Two          On when CCR State Bits are "10".

    State Onr          On when CCR State Bits are "01".

    State Zero         On when CCR State Bits are "00".

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|                |                                                          |
|----------------|----------------------------------------------------------|
| Logic Check    | On whenever the SCU detects a unit check condition related to the internal hardware of the SCU. |
| Power Check    | On whenever the SCU detects a Power Check condition, a thermal warning condition, or has normal power off. |

Maintenance

Additions and modifications to the standard maintenance capabilities have been made so that the circuitry added by the above features may be exercised.

Data Entry. Switches have been added to allow manual setting of the SCON, IOCE, and parity bits of the CCR.

Indicators. Indicators have been added to display the contents of the CCR and pertinent control functions.

OTC Test. A pushbutton switch is provided to simulate a thermal warning condition.

Interfaces

The SCU in the 9020 System communicates over the following three unique interfaces, as described in Chapter 13:

I/O Channel to SCU Interface

CE to SCU Interface

SCU to System Console Interface

IBM 2821 CU with 2540 and 1403

The standard functional characteristics of the punched card and line printer equipment used with the 9020 System are presented in the enclosed IBM System Reference Library documents.* Only those portions pertaining to the basic 2821-1 Control Unit (CU) with Universal Character Set optional feature operating one 2540 Card Read-Punch and one 1403-2 Printer are applicable to this specification.

The system requirement for a character set including 50 to 64 different printable characters on the 1403 is met (and exceeded) by the Universal Character Set optional feature. This feature provides a means for program loading a 240 character coded print chain image in the 2821 CU to match the physical print chain installed in the 1403 printer at any time. Print chains in any configuration up to 240 different printable characters may be ordered for various applications. The exact character set or sets to be used by the 9020 System will be established by mutual agreement in the future.

---

*IBM 2821 Control Unit; IBM 2540 Card Read-Punch: IBM 1403 Printer.

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Additional details of Universal Character Set feature may be found in the 2821 SRL

Prime power for the System or Configuration Console switchable 2821 CU and its attached devices is supplied under control of the Console power control circuitry (See Chapter 9 and 10).

## IBM 1052 Printer-Keyboard

The IBM 1052-7 Printer-Keyboard is composed of three independent functional subsections enclosed in a cover assembly to provide an integrated printer-keyboard device for operator communication with the 9020 System.  These subsections are:

Printer

Data Entry Keyboard

Test Panel

### Printer Operations

The printer section is a modified IBM Selectric print mechanism which incorporates the use of a single print element which traverses across a stationery form feed mechanism (pin feed platen).  All data to be printed or functions to be performed are presented to the printer by the 1052 adapter.

Data Printing - Data to be printed is transmitted to the printer in Tilt-Rotate (T/R) code.  This code is such that it is directly converted through electromagnets to select the proper character by tilting and rotating the print element.

Data Checking - The printer requires that at least one of the 7 data lines (T/R code) contains a signal to initiate a mechanical print cycle.  All data parity checking is performed by the 1052 Adapter.

Print Cycle Checking - The printer signals the 1052 adapter that the printer did perform a print cycle.

Character Set.  The printer is equipped with a printing element of 88 unique character positions (44 each, upper and lower case).  The character set provided by this printing element is shown in Figure 11-4.  The character which will be printed to represent the various unique EBCDI codes used in the 9020 System is shown in Chapter 6, Figure 6-23.

Functions.  The following functions are performed by the printer as a result of signals on the 7 discrete control lines from the 1052 Adapter.

Horizontal Tabulation - The print element will move to the right to the next horizontal tabulation stop from a single signal.  During this operation the printer will signal "Carrier in Motion" to the adapter.

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| SYMBOL | DESCRIPTION | SYMBOL | DESCRIPTION |
|--------|-------------|--------|-------------|
| A-Z | 26 ALPHABETIC CHARACTERS | - | MINUS (HYPHEN) |
| a-z | 26 ALPHABETIC CHARACTERS | + | PLUS |
| 0-9 | 10 NUMERIC CHARACTERS | = | EQUAL |
| . | PERIOD | < | LESS THAN |
| , | COMMA | > | GREATER THAN |
| ; | SEMICOLON | % | PERCENT |
| : | COLON | | |
| ? | QUESTION MARK | $ | DOLLAR |
| ! | EXCLAMATION POINT | ¢ | CENT |
| ' | APOSTROPHE | @ | AT |
| " | QUOTATION MARKS | & | AMPERSAND |
| ( | LEFT PARENTHESIS | # | NUMBER |
| ) | RIGHT PARENTHESIS | * | ASTERISK |
| / | SLASH | \| | LOGICAL OR (VERTICAL BAR) |
| _ | UNDERSCORE | ¬ | LOGICAL NOT |

Figure 11-4.   1052 Printer-Keyboard Characters 9020 System

Line Feed - The paper form will be advanced one line space vertically for each signal received.  During this operation the printer will signal 'carrier in motion' to the adapter.

Carrier Return - The print element will move to the left margin stop and the paper form will be advanced one line space vertically for each signal received.  During this operation the printer will signal 'carrier in motion' to the adapter.

Shift to Upper Case - The print element will be shifted to upper case upon receipt of this signal and remains in this case until a shift to lower case signal is received.

Shift to Lower Case - The print element will be shifted to lower case upon receipt of this signal and remains in this case until receipt of shift to upper case signal is received.

Space - The print element will move one print position to the right for each signal received.

Backspace - The print element will move one print position to the left for each signal received.

End of Line Sensing - The printer will sense the last print position on a line, signal this to the adapter, and internally initiate a line feed and carrier return function.

End of Forms Sensing - The printer will sense the end of paper approximately three inches before the print line position. It will signal this condition to the adapter.

Cycle Timing - The printer will accomplish the following cycles within the times indicated. The actual times for the various operations will not be less than the indicated cycle times but are a function of the 1052 adapter controls.

| | |
|---|---|
| Print Cycle | 68 ms |
| Space or Backspace Cycle | Same as print cycle |
| Tab or Carrier Return | $(1.5 + T)$ x 68 ms where T = the number of inches to be traversed by the carrier |
| Line Feed | 2 x 68 ms = 136 ms |

Keyboard Operations

The keyboard section of the 1052 provides manual data entry keys and **control function keys for operator use. The keyboard layout is shown in Figure 11-5.**

Data Entry - Depression of a data key will cause the encoding of the seven data lines to the adapter and will generate a signal to the adapter that a coded character is available on the data lines.

Data Checking - All data checking is performed by the adapter. A visual data check may be made by the operator since the adapter routes the data received to the printer.

Character Set - The keyboard generates a seven bit coded character for all keys except Alternate Coding, Request, Ready, Not Ready, Lock, Enter, and Cancel, as shown in Figure 6-24.

The EBCDI code, which will result from keyboard operations, is a function of the adapter and is shown in Chapter 5, Figure 6-27.

Alternate Coding - This key is not functional.

Request - Depression of this key signals the adapter to indicate operator will enter a message on the keyboard.

Ready - Depression of this key signals the adapter to indicate operator requires 1052 be put in Ready status.

Not Ready - Depression of this key signals the adapter to indicate operator requires 1052 to be put in Not Ready status.

Enter - Depression of this key signals the adapter to terminate the Read operation normally.

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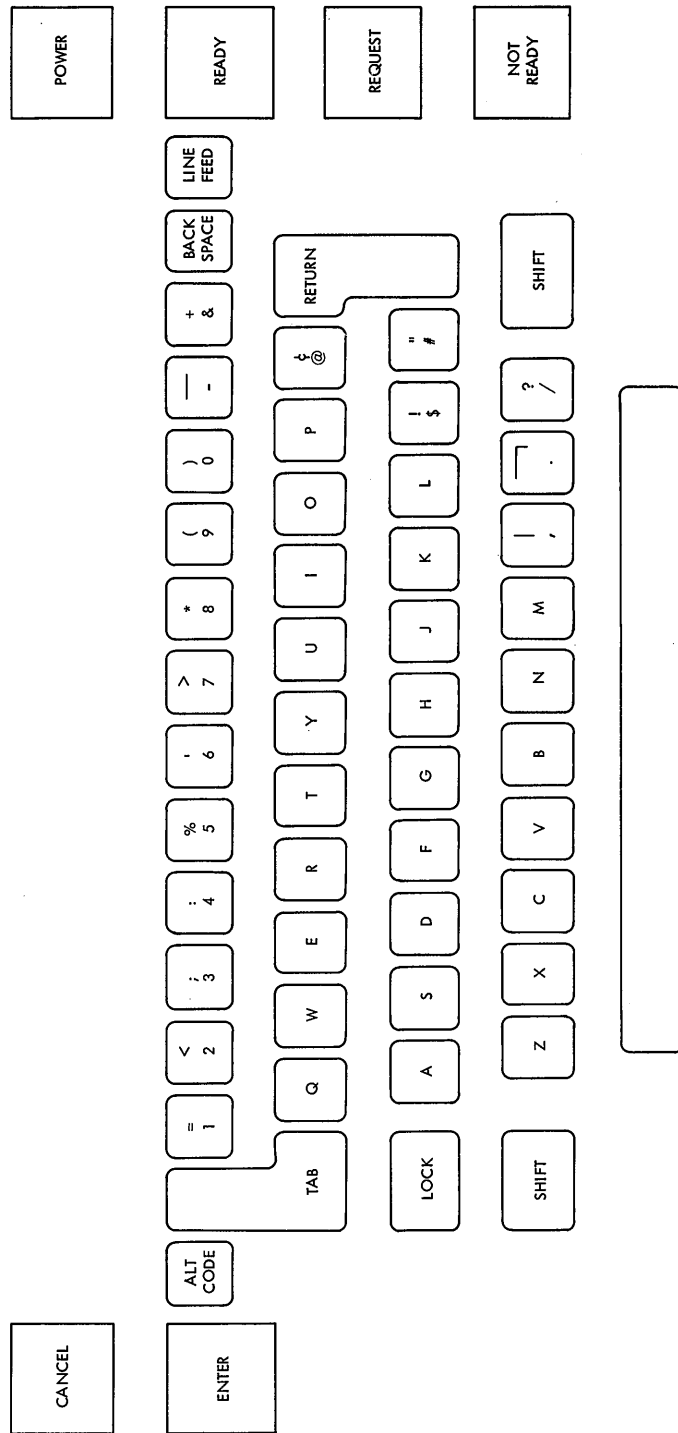
Figure 11-5. 1052 Keyboard Layout

Cancel - Depression of this key signals the adapter that the message
is in error and the Read operation is terminated abnormally.

Lock Key - This key will lock the shift key in the upper case
position.

Keyboard Restore and Keyboard Lock Functions - One line is provided
for the adapter to exercise control over all keying operations
except Request, Ready, and Not Ready.

> Restore Function - A pulse applied to this line (Keyboard Lock)
> will electromechanically restore the keyboard mechanism to
> operating state following the depression of a key.

> Lock Function - A voltage level maintained on this line
> (keyboard lock) will electromechanically lock the keyboard
> mechanism.  Removal of the signal will leave the keyboard
> mechanism restored for subsequent operation.

Timing - The timing for successive keyboard operations is a function
of the operator and the 1052 adapter.

Test Panel

This panel for the 1052 adapter is mounted on the 1052, and is shown
in Figure 11-6.  The functions provided by this panel are described
in Chapter 6, 1052 Printer-Keyboard adapter.
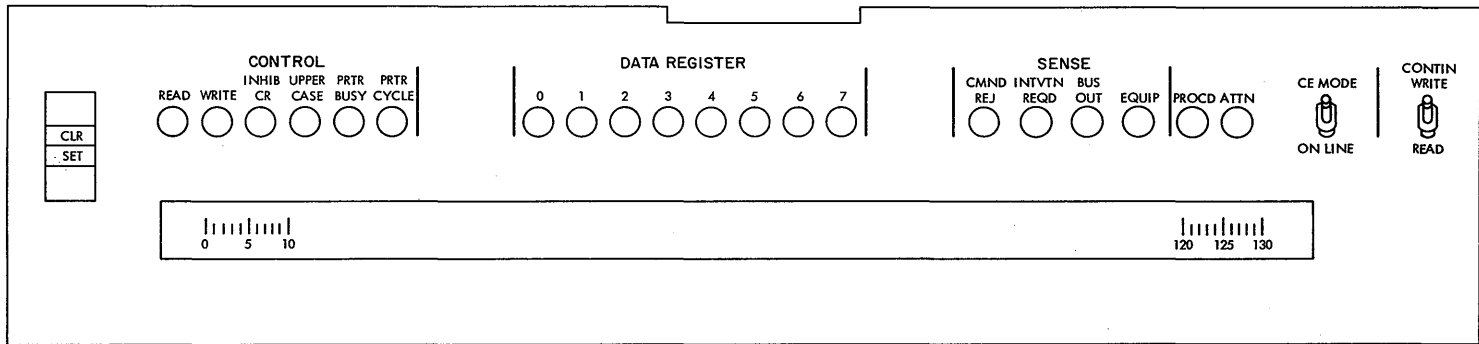
Figure 11-6.  Test Panel for 1052 Adapter

INTRODUCTION

Each of the 9020D and 9020E System components receives 208 volt
primary power individually from the installation power distribution
system, and contains equipment to convert this primary power to
voltages required for its own operation, and for the operation of
attached IBM devices initially supplied with the system. Manual
controls, protective circuits, and appropriate indicators are
provided at each system component for the proper operation of its
power equipment.

The combining of these individual components into a system
configuration imposes the need for system coordination of these
individual power facilities. To achieve this coordination, certain
system power control functions are provided.

1.  The Executive Control Program is provided the capability
    to restrict the manual removal of power from all elements
    and some units.

2.  Loss of power at all elements, Peripheral Adapter Module
    (PAM), Tape Control Unit (TCU), RCU portion of Configuration
    Console (CC), Storage Control Unit (SCU), and 2701 is
    indicated to the Executive Control Program. However, the
    2701 indication will occur only if an I/O Selection is
    attempted.

3.  Element and some unit power indicators are displayed at the
    System Console or Configuration Console.

4.  Provision is made for the removal of all system power except
    that of the prime power compartments should an emergency
    situation occur.

5.  All elements are equipped to detect the loss of input
    power and to automatically operate from a temporary
    sustaining power source.

6.  The ability is provided for all system components to be
    returned automatically to a power on status following the
    return of prime power.

The tables that follow indicate element and unit power control
facilities for the primary elements and units within the system. The
power control for the secondary units and devices is supplied by the
primary unit to which they are attached, as indicated below:

    1052  Auxiliary and Console Printer Keyboards

'1.  9020D SYSTEM

    a.  The Auxiliary Printer Keyboards receive
    power under control of the PAMs.

    b.  The Console Printer Keyboard receives all
    power under control of the System Console
    (SC).

2.  9020E SYSTEM

    All Printer Keyboards receive power from its
    associated Computing Element.

    Each 1052 has a Power-On indicator to show the
    presence of power in the device.

2401    Tape Units - These devices receive power under
control of the 2803 TCU.  They do not have power-
on indicators displayed.

2821    CONTROL UNIT

1.  Console switched Control Unit - 9020D and
9020E
This control unit receives primary power from
its own receptacle, but under control of the
System Console (SC), or Configuration Console
(CC) and supplies power to the 2540 Card Read-
Punch and the 1403 Printer.

2.  Independent two-channel Control Unit - 9020D
This control unit has its own power source and
supplies power to its associated 2540 and 1403.
The 1403 does not have a power on indicator.

SYSTEM POWER CONTROL FACILITIES

The System Power Control facilities provided in the 9020D and 9020E
Systems are of four general categories:

1.  Power control functions

2.  Elements Indicators-Local

3.  System Control Indicators

4.  Power System Interruptions

Power Control Functions

Table 12-1 lists the power control functions of system significance.
The descriptions that follow are applicable to the components
indicated in the table.

Table 12-1.  Power Control Functions - 9020D and 9020E Systems

| Function | System Component | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | IOCE 7321 -2 | DAU 2701 | PAM 7289 -2 | TCU 2803 -1 | SC 7265 -2 | SE 7251 -9 | CE 7201 -2 | CC 7265 -3 | DE 7289 -4 | SCU 2314 -A1 |
| Power Interlocks | | | | | | | | | | |
| Power On/Off Interlock | X | NO | X | X | NO | X | X | X | X | X |
| M. C. Interlock | X | NO | X | * | X | X | X | X | X | X |
| Power On-Off Facilities | | | | | | | | | | |
| Emergency Pull Switch | NO | NO | NO | NO | X | NO | NO | X | NO | NO |
| Emergency Power Off | X | X | X | X | X | X | X | X | X | X |
| Element Master Power Off | X | NO | X | X | NO | X | X | X | X | X |
| Power On/Off | X | X | X | X | X | X | X | X | X | X |
| Power On Delay | X | NO | X | NO | X | X | X | NO | X | NO |
| Warning & Protection Facilities | | | | | | | | | | |
| Thermal Warning | X | NO | X | X | * | X | X | X | X | X |
| Thermal Protection | X | * | X | X | * | X | X | X | X | X |
| Over Voltage/ Over Current Protection | X | * | X | * | * | X | X | X | X | * |
| Temporary Sustaining Power Source | | | | | | | | | | |
| Prime Power Sensing | X | NO | NO | NO | NO | X | X | NO | X | NO |
| Battery Back-up Power Source | X | NO | NO | NO | NO | X | X | NO | X | NO |
| Duplex Power | | | | | | | | | | |
| Duplex Power Supplies | NO | NO | NO | NO | X | NO | NO | X | NO | NO |

Legend to Table 12-1:

        X - Function provided as defined

        * - Function provided - See note under standard definition

        NO - Function not provided

        CE - Computing Element

        IOCE - Input/Output Control Element

        SE - Storage Element

        PAM - Peripheral Adapter Module

        TCU - Tape Control Unit

        SC - Systems Console

        CC - Configuration Console

        DAU - Data Adapter Unit

        DE - Display Element

        SCU - Storage Control Unit

Power Interlocks

Power On/Off Interlock.  "Power On/Off" switch will be rendered incapable of performing a power off function whenever the element or unit state, as specified by its CCR, is other than State Zero with the Test Switch on.

M. C. Interlock.  "Marginal Check Excursion Controls" will be slotted and recessed behind their control panels to prevent inadvertent operation of these potentiometers if they are located on an exposed operator's panel.

NOTE:  The M. C. Excursion capability for the TCU is provided by means of portable test equipment (Power Supply - MC-SMS) which will be connected only during maintenance activities.

Power On/Power Off Facilities

Emergency Pull Switch.  This switch will be round, red in color, and bear the label "Emergency Pull".  Activation of this switch will cause the removal of all output power from circuits and cabling outside the power control compartment of each System Component with the exception of essential control voltages.  This switch is so constructed that once activated, the services of maintenance personnel are required to restore power to the system.

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Emergency Power Off Function.  This function allows removal of output power (except for essential control voltages) from circuits and cabling outside the power control compartment of each system component.  The facility is activated by use of the "Emergency Pull" switch at the SC or CC.  It will be operable at all times that any element within the system has primary power present.  Removal of power by this means may result in data loss.  Use of this switch must be restricted to Emergency situations.

Element Master Power Off Function.  This facility will be activated by use of the "Element MPO Pull" switch at the element.  Activation of this switch will cause the removal of all output power (except for essential control voltages) from circuits and cabling outside the power control compartment of that element, PAM, CC, SCU, or TCU.  This switch is not interlocked by any other function.  Removal of power by this means may result in data loss.  Use of this switch must be restricted to emergency situations.

Power On/Off.  This facility provides the normal means for the controlled application and/or removal of operating power.  All power except control voltage and convenience outlets are under control of this facility.

     The manual "power off" function is inoperable when the element or unit except SC or SCCU portion of the CC is in other than State Zero with the Test Switch enabled.

     The "power on" function, if active at the time of a prime loss, will automatically be restored upon the return of prime power.

Power On Delay.  A delay function, adjustable by maintenance personnel over a range of 5 to 30 seconds, is provided.  This facility allows the setting of the individual element delays within the system to effect staggered element power on sequence.

Warning and Protection Facilities

Thermal Warning.  A thermal sensing circuit will be provided which will determine when an element or unit's internal temperature has reached a point approximately 10 degrees below the nominal thermal protection temperature.  Actuation of this circuit will (1) light a Thermal Check indicator on the element or unit, (2) light the Power Check indicator on the SC or CC, and (3) provide a Marginal Condition interruption to the Program (See Table 12-2).

NOTE:  The SC will light a thermal check indicator upon sensing the thermal warning temperature.  It does not generate an Interruption condition.

Thermal Protection.  A thermal sensing circuit will be provided to determine that the element or unit internal temperature has reached the Thermal Protection temperature.  Actuation of this circuit will (1) cause a Power Off function, (2) will light the element or unit Thermal Check Indicator and (3) will light the corresponding Power Check indicator on the System Console or Configuration Console.  The Power Off function will cause an Element Check Interruption.

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NOTE: The SC will light a thermal check indicator and sequence power down upon sensing a thermal protection temperature. It does not generate an Element Check Interruption. The DAU will perform items 1, 2, and 3 above. It will not generate an Element Check Interruption.

Table 12-2. Local Element Indicators, 9020D/E System Power Control

| Local Indicators | System Component | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | IOCE 7231 -2 | PAM 7289 -2 | TCU 2803 -1 | SC 7265 -2 | SE 7251 -9 | CE 7201 -2 | CC 7265 -3 | DE 7289 -4 | DAU 2701 | SCU 2314 -A1 |
| Power Indicators | | | | | | | | | | |
|   Main Line On | X | X | X | X | X | X | X | X | X | X |
|   Sequence Complete | X | X | X | X | X | X | X | X | NO | NO |
| Environmental Check Indicators | | | | | | | | | | |
|   Thermal Check | X | X | X | X | X | X | X | X | X | X |
|   Power Check | X | X | X | X | X | X | X | X | NO | X |
| Battery | | | | | | | | | | |
|   On Battery | X | NO | NO | NO | X | X | NO | X | NO | NO |

Legend: X - Function provided as defined

NO - Function not provided

Over Voltage/Over Current Protection. A sensing circuit will be provided on the output of each D. C. power supply which will determine when the supply output has reached a point predetermined for each element or unit, above which further variation could cause circuit damage. When actuated, these sensing circuits will:

    1. Immediately suppress the output of the power supply whose sensing circuit has been actuated.

    2. Sequence power off in the element or unit.

    3. Light the element or unit Power Check Indicator.

    4. Light a Power Check indicator on the SC or CC.

    5. Generate an Element Check Interruption.

NOTE: The SC will perform items 1 through 4 above when it senses an Over Voltage/Over Current Condition. It will not generate an interruption. The TCU, SCU, and DAU provide only Over Current Protection by means of circuit breakers on the input of each D.C. power supply.

Temporary Sustaining Power Source

Prime Power Sensing. A sensing circuit will be provided on all elements to determine the loss of the prime power source. When the loss of prime power is detected, this circuit will enable control circuitry to activate the Battery Backup Power Source. The return of prime power will deactivate the Battery Backup Power Source upon completion of the timeout, if the interruption is less than the preset battery timeout period. Emergency power off will not activate this circuit.

Battery Backup Power Source. Batteries are provided as a backup source to sustain the CE and IOCE power for 6.5± .5 seconds and the SE and DE power for 5.5± .5 seconds. Recharging circuits are pro- vided to maintain the battery charge at specified level. The required recharge time to restore the battery after use is 300 times the period the batteries were in use. Repeated use of the batteries without sufficient recharge time may deplete the cells.

On Battery Timer. A timing device is energized when the Battery Backup Power Source is activated. If the Battery Backup source is still activated after a period of 6.5 ± .5 seconds*, this device will cause a normal power off function and will deactivate the backup power source. This power off function is not program interlocked and is operable in all element states.

Duplex Power Supplies

The SC and System Console portion of the CC are each provided with two totally independent power supply facilities which are selectable by a single manual control. The switching controls are so designed that changing from one power facility to the other may be accom- plished only by effecting a power off function. The power controls and indicators are simplex, serving only the selected power supply facility. The CC has two additional simplex power supply facilities; one for each RCU in the CC.

Element Indicators - Local

Table 12-2 lists the indicators of system significance located on the various system components. The descriptions that follow are applicable to each component as indicated in the table.

Power On Indicators

Main Line On Indicator - This indicator will be on when prime power is available from the power control compartment. Prime power is not available when Emergency Pull or Element MPO Pull have operated.

_____

*SE and DE timers are set to 5.5 ± .5 seconds.

Sequence Complete Indication - This indicator will be on when all operating voltages are present in an element or unit.

Environmental Check Indicators

Thermal Check Indicator(s) - One or more indicators will be provided to indicate when the internal temperature has reached the thermal warning level. The indicator(s) may be turned off by activating the Thermal Check Reset if the temperature has fallen below the warning level.

Power Check Indicator - This indicator will be lighted when a power off condition exists whether from a functional or a protective cause. The TCU turns on Power Check only for a protective cause.

Battery

On Battery Indicator - This indicator will be on when the element is operating from the Battery Backup Power Source.

System Control Indicators

Tables 12-3 and 12-4 list the System Control Indicators displayed at the System Console and Configuration Console.

Power Check Indicators

These indicators are turned on by the respective unit or element when one or more of the following conditions exist:
  1.  Catastrophic power supply failure.
  2.  Overtemperature.
  3.  Normal power off.

NOTE:  The SC and CC provide their own Power Check Indicator and have a separate Thermal Check Indicator.  The DAU does not have a local power check indicator.

Table 12-3.  System Control Indicators, 9020D System Power Control

| System Console Indicators | Source | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | CE 7201-2 | IOCE 7231-1 | SE 7251-9 | PAM 7289-2 | TCU 2803-1 | SCU 2314-A1 | SC 7265-2 | External |
| Power Check | X | X | X | X | X | X | * | NO |
| Battery | X | X | X | NO | NO | NO | NO | NO |
| Standby | NO | NO | NO | NO | NO | NO | NO | X |

Legend:  X - Function provided as defined
         NO - Function not provided
         * - Function provided - see special definition

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Table 12-4. System Control Indicators, 9020E System Power Control

| Configuration | Source | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Console | CE 7201 -2 | IOCE 7231 -2 | SE 7251 -9 | DE 7289 -4 | TCU 2803 -1 | CC 7265 -3 | DAU 2701 | DG | RKM | External |
| Indicators | | | | | | | | | | |
| Power Check | X | X | X | X | X | * | X | X | X | NO |
| Battery | X | X | X | X | NO | NO | NO | NO | NO | NO |
| Standby | NO | NO | NO | NO | NO | NO | NO | NO | NO | X |

Legend: X - Function provided as defined
* - Function provided - see special definition
NO - Function not provided
DG - Display Generator (GFE)
RKM - Radar Keyboard Multiplexor (GFE)

Battery Indicator - This is a single indicator shared by elements having Battery Backup Power Source. It will be lighted when one or more of the Battery Indicators on the individual elements are lighted.

Standby Indicator - This indicator will be on when the prime power for the system is being provided by a standby power supply, i.e., Motor Generator. The source of this indication will be a contact closure external to the 9020 System.

Power System Interruptions

Table 12-5 lists the power system interruptions and indicates the system components which provide the interruptions. (For uses of these interruptions for other than power conditions, see Chapter 8 Configuration Control).

Catastrophic Condition Indications

Element Check - A power off condition whether from a normal functional cause or the result of protective circuit action will cause an ELC Interruption.

Marginal Condition Indication

Out of Tolerance Check (OTC) - An element sensing a thermal warning condition will cause an OTC Interruption.

NOTE: A thermal warning in the SE or DE causes an ELC interruption and sets a bit in the logout word which indicates checks. No OTC Interruption is generated.

A thermal warning in the CC or SCU causes an ELC Interruption and sets a sense bit which indicates OTC checks. No OTC Interruption is generated.

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Table 12-5.  Power System Interruptions - 9020D/E System Power Control

| Power System Interruptions | Source | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | IOCE 7231 -2 | PAM 7289 -2 | TCU 2803 -1 | SC 7265 -2 | SE 7251 -9 | CE 7201 -2 | DE 7289 -4 | CC 7265 -3 | DAU 2701 | SCU 2314 -A1 |
| Catastrophic Condition | | | | | | | | | | |
| Element Check (ELC) | X | X | X | NO | X | X | X | X | NO | X |
| Marginal Condition. | | | | | | | | | | |
| Out of Tolerance Check (OTC) | X | NO | NO | NO | X | X | X | X | NO | X |
| Attention Status | NO | * | X | NO | NO | NO | NO | NO | NO | NO |
| On Battery | | | | | | | | | | |
| On Battery Signal (OBS) | X | NO | NO | NO | X | X | X | NO | NO | NO |

Legend:   X - Function provided as defined
          * - Function provided - see special definition
          NO - Function not provided

Attention Status - A Unit sensing a thermal warning condition will indicate the marginal condition through the I/O interface by setting the Attention bit in the Status Byte.  No OTC interruption is generated.

NOTE:  The PAM also sets a unique bit in a Sense Byte to distinguish this Attention condition from others that might occur from normal operations.  A pushbutton is provided to simulate the condition for testing.

On Battery Indication

On Battery Signal (OBS) - The element will cause an interruption to indicate that it is operating from its Battery Backup Power Source.

NOTE:  An On Battery Condition in SE or DE causes an ELC interruption and sets a bit in the logout word which indicates checks.  No OBS signal is generated.  A pushbutton is provided at the CE, DE, IOCE, and SE to simulate the condition for testing.

Element and Unit Power Control Facilities

Descriptions of the power control switches and indicators for each element and unit are presented in the chapter which describes the element or unit.

POWER CONTROL OPERATION

## System Power On/Off

The IBM 9020D/E is designed for 24 hour operation, requiring that a minimum configuration of elements and units be operating at all times.  Therefore, no System Power On/Off facility (other than Emergency Power Off) is provided.  Instead, individual element and unit Power On/Off facilities are provided for selective control of the power for the elements and units required for operation in specific situations.

     The Power On/Off circuits for the elements and units have been designed as "latching" controls which will remain in the power on position even though prime system power is lost.  Therefore, when prime power is restored following a power interruption, all elements and units which have their power on switch in the "ON" position will automatically initiate an internal power on sequence.  In addition, all System Components (except for TCU, SCU, CC, and DAU) have each been provided with an adjustable time delay which will delay the start of its own internal power on sequence following restoration of prime power.  By adjusting this time delay in each element or unit to a value different from every other element or unit, a "system power on sequence" can be established with the TCU's, SCU's, CC, and DAU's on immediately, followed by the other elements or units spaced over a delay range of 5 seconds minimum to 30 seconds maximum.

     In the event that a power loss were less than the present on-battery value, the battery backup system in the CE's, IOCE's, SE's, and DE's would sustain these elements in an uninterrupted power on status, leaving only the TCU's, SCU's, SC, or CC and DAU's or PAM's to be cycled back up.

## Element Power Equipment

The high frequency power equipment in a 9020D/E element contains four major sections:

1.  Power Control and Sequencing, which provides input power control protection and distribution and also satisfies Power Sequencing required within the element.

2.  Converter - Inverter, which converts 60 Hz, 3-phase 208 VAC input power to single phase, square wave, 2500 cycle power.

3.  AC/DC Regulators, which convert the 2500 cycle power to regulated DC power as required in the element or unit.

4.  Battery Backup System, which keeps the Converter - Inverter running for a period of time if an input line failure occurs.

## Power Control and Sequencing

The Control and Sequencing section is unique in detail to each element. Its function is to control the distribution of prime power, to protect circuits using this power, and to sequence the application of power as required by the individual circuits.

Application of prime power to an element (Figure 12-1) will bring up that element's Prime DC Control Voltage supply. The output of this supply is connected to the EPO (Emergency Power Off) circuit in the SC or CC. If the EPO switch is closed, a contactor in the console will pick, providing a return for the EPO circuit within each element.

At the element, the MPO (Master Power Off) switch, when closed, will pick the element EPO contactor which will apply 208 VAC to the convenience outlet transformer and the Prime AC Control Voltage supply. It also applies DC control voltage to the sequence and control relays.

Closing the power on-off switch will start a time delay. This delay is adjustable from 5 to 30 seconds and will be set to a value to obtain a staggered Power On sequence of the various system elements. At the end of this time delay, the AC On contactor will apply 208 VAC to the blowers, Converter-Inverter, and the battery charger.

The output of the Converter-Inverter is distributed to the Standard Voltage Regulators and to the Bootstrap supplies. When these supplies come up, the control voltage loads will be switched from the Prime Control Voltage supplies to the Bootstrap Supplies. The AC On Contactor will still be fed from the Prime DC Control Voltage supply.

When all the standard DC voltages are up, contacts will apply the Converter-Inverter output to the Special Voltage Regulators. When the special DC voltages are up, contacts will turn on the "Sequence Complete" indicator and generate a power on reset to the logic.

A prime power loss will be detected by the line sense circuitry, which will switch-in the battery source. It will also start a timer which will time out for the pre-adjusted time interval.

If prime power is restored before the preset time interval has elapsed, the battery source will be switched out at the end of the timeout period. If prime power does not return, the timer will sequence Power Down.

A catastrophic thermal or over-voltage/over-current condition will also cause a Power Down Sequence.

## Converter-Inverter

A block diagram of the Converter-Inverter (C/I) is shown in Figure 12-2. The 3-phase, 208 line voltage is fed through RFI (Radio

12-12
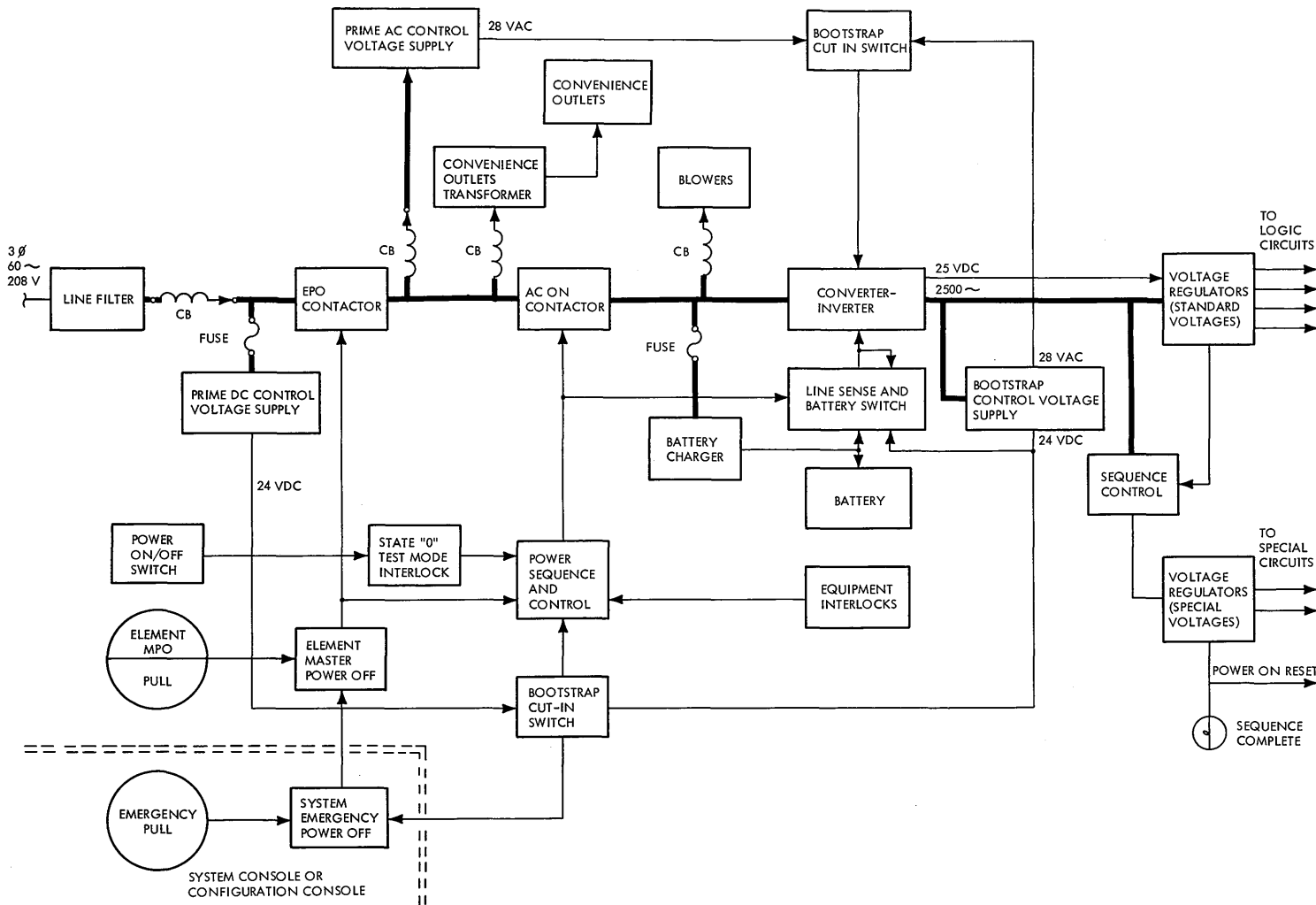
Figure 12-1.  Typical Element Power Control, 9020D/E System

Frequency Interference) filters which filter conducted line noise. The voltage is then rectified and peak filtered by means of a capacitor input filter to produce the DC voltage which is used as an input to the inverter circuit. In the case of a prime power failure, this DC voltage is supplied from a backup battery source.
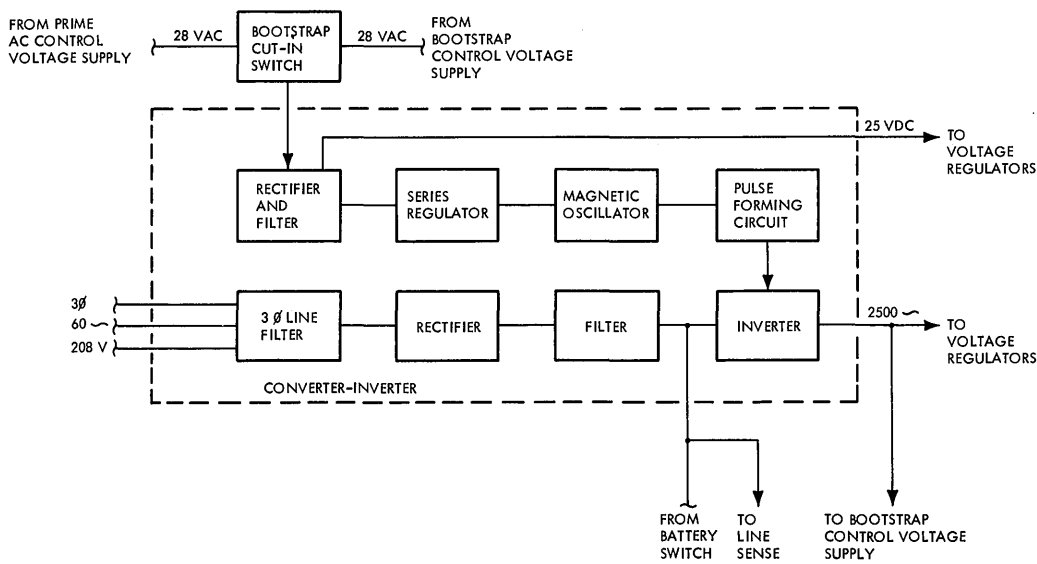


•Figure 12-2. Converter-Inverter

The inverter circuit is a parallel SCR (Silicon Controlled Rectifier) circuit which produces a 2500 Hz square wave output having an RMS value of approximately one-half the DC input to the circuit. The frequency of this output is established by a 2500 Hz clock signal fed to the inverter circuit. This clock signal is provided by an oscillator circuit which takes one phase of the line voltage, transforms it to a lower voltage (28 VAC) and feeds it into C/I where it is then rectified, filtered and regulated. The regulated DC is then used in a magnetic oscillator whose multiple outputs are formed and sent to the inverter circuit SCR's.

To maintain the output of the Converter-Inverter in the case of a prime power failure (DC input to the inverter being supplied by the battery back source), a bootstrap supply is connected to the output. This supply steps the output down and applies it to the oscillator circuit as an alternate 28 VAC source, thus maintaining its operation.

The rectifiers and filter in the oscillator circuit in the C/I also provide a 25 VDC unregulated output for use as a bias voltage in the AC/DC regulators.

The 25 amp Converter-Inverter is used in the SC while the 75 amp CI is used in the CE, SE, DE, IOCE and PAM units.

## AC/DC Regulators

The AC/DC regulators (Figure 12-3) are time-ratio controlled circuits. The regulators receive 2500 Hz C/I output with an input transformer to provide isolation as well as voltage transformation. The square wave output of this transformer is then rectified and fed to a blocking circuit. The square wave is also fed to an amplifier circuit to establish the switching cycle frequency (5000 Hz) of the blocking circuit. This amplifier also monitors the DC output of the regulator, compares it to a reference, and establishes the duration of the blocking action in each switching cycle of the blocking circuit. Thus, the blocking circuit output is 5000 Hz pulse train with feedback regulated pulse duration which, when averaged by the filter, provides the desired DC output voltage.

To protect the AC/DC regulators and the loads which they feed, a circuit is provided which monitors the output current and voltage. Should either exceed an upper limit, a short circuit is placed on the output, the regulator shut off, and the sequence and control circuitry signalled to sequence Power Down.

## Battery Back-Up System

The battery back-up system is composed of a battery pack, a charger circuit, and a line sense and battery switch circuit. When the voltage drops below a predetermined limit, the Voltage Sense circuit (Figure 12-4) applies gate current to the Battery Switch SCR. The SCR activates, performing a high speed switching function to connect the battery to the input of the Inverter circuit, thus allowing the Converter-Inverter to continue uninterrupted.
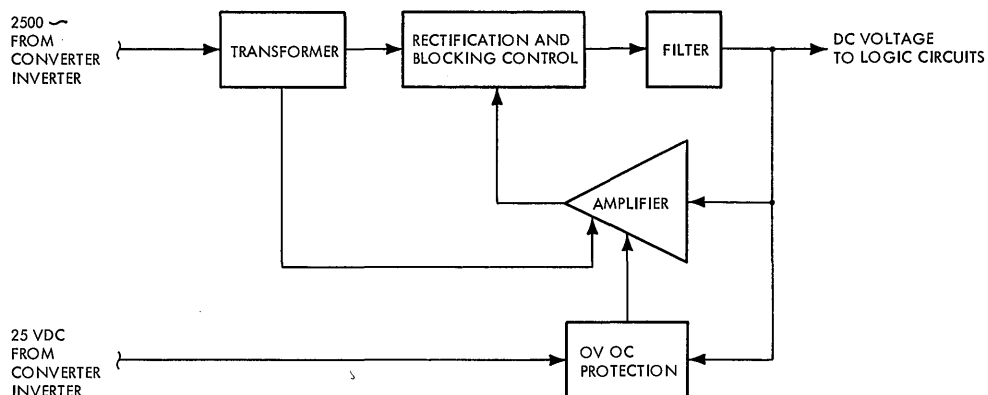


Figure 12-3.   AC/DC Regulator
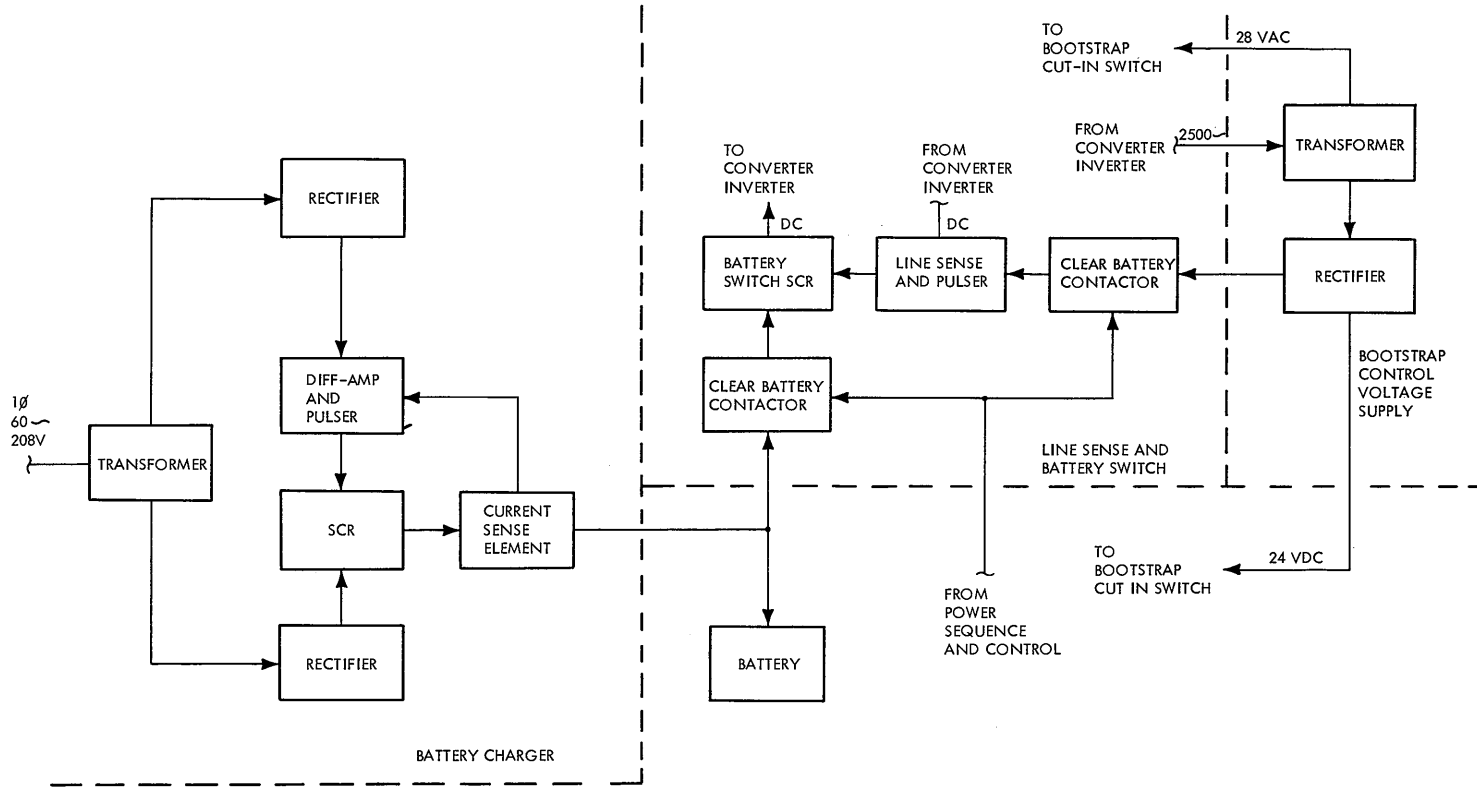
Figure 12-4. Battery Back-Up System

If prime power is restored before a preset time interval not to exceed 6.5 ± .5 seconds, the Inverter continues to be powered from the Battery for the duration of the timer. At the end of the time interval, the Sequence and Control circuitry will open a contactor to disconnect the Battery. The Inverter will again be powered by the normal means and the battery charger will restore the charge on the battery. The charger is a time-ratio controlled circuit which provides an average DC trickle charge current of 150 milliamps.

Should power not be restored before the preset time interval, the Sequence and Control circuitry will cause a power down sequence and then disconnect the Battery.

Appropriate interlocks are included in the control circuitry to prevent the Battery Back-Up System from being activated during normal power sequencing operations or when the Emergency Power Off circuit has been operated.

The battery packs used in the 9020 System equipment are made up of a number of individual nickel cadmium cells (1.2 volts/cell) of the sealed, safety vent type. These cells are connected in a series parallel arrangement to provide the required voltage and current rating to operate the Converter-Inverter to which they are attached. Cells are packaged in groups of ten called ten-packs.

The batteries employed in the 9020 System never require the addition of electrolyte or water. Because they are sealed, no gassing occurs and no maintenance is required. The seal mechanism is intended to automatically relieve cell pressure at a point well below cell rupture and then will reseal with no noticeable effect on performance. The battery pack is housed in each element in a way that authorized maintenance personnel will not, unless actually working with them, come into contact with the cells. Only the external connection points are exposed.

The battery back-up system as implemented in each element meet the following criteria:

Line Sense - Battery Cut In Point

The battery cut in point is adjustable and will be set so that the battery switch will not be activated before the prime power input voltage falls to 187 VAC RMS, but will always be activated before the input voltage falls to 175 VAC RMS.

Battery Pack Capacity

The fully charged battery pack will be capable of sustaining uninterrupted operation of the fully loaded Converter-Inverter for a period of at least 5.5 seconds.

Battery Pack Recharge Time

The battery pack will be restored to full charge condition after an uninterrupted charge time of 300 times the number of seconds in use.

Chapter 13's discussion of interface lines is divided into two parts.
Part I discusses the interface lines for the 9020D System.   Part II
discusses the 9020E System interface lines.   However, because of the
similarity between the two systems, only the differences between
them will be discussed in Part II.   To avoid duplication, references
will be made to the 9020D System discussion for similar interface
functions.

PART I.   9020D SYSTEM

INTRODUCTION

This section describes the following interfaces between elements of
the IBM 9020D System.   Tables 13-1 through 13-11 list lines between
the pair of components as defined in the individual interfaces.

| | | | | |
|---|---|---|---|---|
| CE | - CE | | TCU | - System Console |
| CE | - SE | | SCU | - System Console |
| IOCE | - SE | | CE | - SCU |
| SE | - System Console | | CE | - TCU |
| CE | - IOCE | | CE | - PAM |
| IOCE | - System Console | | TCU | - TU |
| CE | - System Console | | 2821 ICU | - Printer |
| PAM | - System Console | | 2821 ICU | - Card Reader/Punch |

All interface lines from the IOCE  to control units are described in
Appendix D, Input/Output Interface, Channel to Device Control Unit;
interface lines from the 1052 adapter to the 1052 Printer Keyboard
are described in Chapter 5.

System diagram Figure 13-1 shows the interface lines.

CE - CE INTERFACE

The CE - CE Interface (Table 13-1) has four purposes:   transmission
of configuration (SCON) or address translation (SATR) information
from an issuing CE to a receiving CE during execution of a SCON or
SATR instruction; the Direct Control feature which allows CE-to-CE
communications, CE External Start, CE External Stop, and CE Logout;
transmission of element check signals; and system reset during IPL.

Control Bus - A bus consisting of 32 data positions plus four parity
positions for transmitting CCR or SATR data to receiving CE.

Reconfigure Select - A line sent by the issuing CE to select a
particular CE to receive the configuration mask on the control bus.

SATR Select - A line sent by the issuing CE to select a particular
CE to receive the ATR mask.

SCON/SATR Response - A line returned to the issuing CE to indicate the selected CE has accepted the CCR or SATR data with correct parity.

Element Check - Used to transmit logic and power check signals.

Table 13-1.  CE to CE Interface

| Line Name | Number of Lines |
|-----------|-----------------|
| For SCON and SATR | |
|     Control Bus | 36 |
|     Reconfigure Select | 1 |
|     SATR Select | 1 |
|     SCON/SATR Response | 1 |
| Element Check | |
| Direct Control | |
|     Direct Out | 9 |
|     Signal Out | 5 |
|     System Reset | 2 |

Direct Out - Consists of 9 lines (8 data plus parity) for Write Direct.

Signal Out - Consists of 5 lines to each CE as follows:

    1.   Write Direct

    2.   Read Direct

    3.   External Start

    4.   External Stop

    5.   CE Logout

System Reset - This signal causes a CE to reset its DAR, DAR Mask, Check Registers, PSBAR, Interrupt Requests, ATR, and CCR.  The CCR SCON bits are then set to all ones.

The signals on the two reset lines must go (-) on line 1 and (+) on line 2 simultaneously to generate the system reset.  These lines are not gated by the CCR.

•Figure 13-1. 9020D System Diagrams, Interface Lines
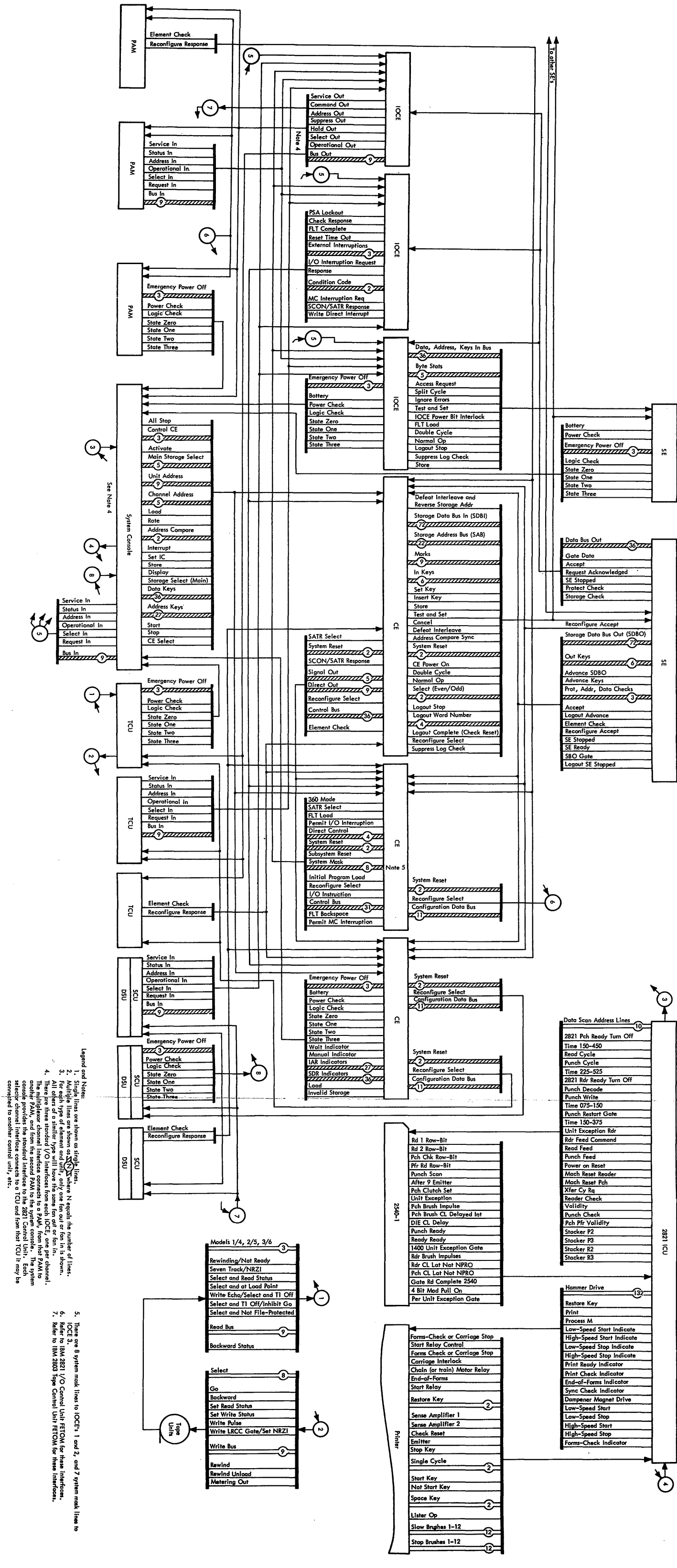
Table 13-2.  CE to SE Interface

| Line Name | Number of Lines |
|---|---|
| To SE | |
|    Storage Data Bus In (SDBI) | 72 |
|    Storage Address Bus (SAB) | 22 |
|    Marks | 9 |
|    In Keys | 6 |
|    Set Key | 1 |
|    Insert Key | 1 |
|    Store | 1 |
|    Test and Set | 1 |
|    Cancel | 1 |
|    Defeat Interleave | 1 |
|    Address Compare Sync | 1 |
|    System Reset | 2 |
|    CE Power On | 1 |
|    Double Cycle | 1 |
|    Normal Op | 1 |
|    Select (even/odd) | 2 |
|    Logout Stop | 1 |
|    Logout Word Number | 3 |
|    Logout Complete (Check Reset) | 1 |
|    Reconfigure Select | 1 |
|    Suppress Log Check | 1 |
|    Defeat Interleave Reverse | 1 |
|    Logout Select | 1 |

Table 13-2.  CE to SE Interface (con't)

| Line Name | Number of Lines |
|-----------|-----------------|
| From SE | |
| Storage Data Bus Out (SDBO) | 72 |
| Out Keys | 6 |
| Advance SDBO | 1 |
| Advance Keys | 1 |
| Prot, Addr, Data Checks | 3 |
| Accept | 1 |
| Logout Advance | 1 |
| Element Check | 1 |
| Reconfigure Accept | 1 |
| SE Stopped | 1 |
| Logout SE Stopped | 1 |
| SE Ready | 1 |
| SDBO Gate - Ident Tag | 1 |

CE/IOCE-SE INTERFACE

The CE/IOCE-SE Interface lines are listed in Tables 13-2 and 13-3.
A description of each line follows the tables.

Interface to SE

IOCE to SE Bus

A group of 36 lines carry Data or Address information from one IOCE
to one of up to four SEs.  The accessed SE gates the signals off the
bus.  During the first part of a storage cycle, 24 lines carry in
the Address and four lines carry the Storage Protect Key.  During
the remainder of the cycle, if a Store is called for, 36 lines
carry data.  (Bytes read-out and not to be replaced by data are
regenerated.)

Table 13-3. IOCE to SE Interface

| Line Name | Number of Lines |
|---|---|
| To SE | |
| Data, Address, Keys In Bus | 36 |
| Byte Stats | 5 |
| Access Request | 1 |
| Split Cycle | 1 |
| Ignore Errors | 1 |
| IOCE Power Bit Interlock | 1 |
| FLT Load | 1 |
| Double Cycle | 1 |
| Normal Op | 1 |
| Logout Stop | 1 |
| Suppress Log Check | 1 |
| Test and Set | 1 |
| Store | 1 |
| From SE | |
| Data Bus Out | 36 |
| Gate Data | 1 |
| Storage Check | 1 |
| Accept | 1 |
| Protect Check | 1 |
| Request Acknowledged | 1 |
| SE Stopped | 1 |

CE to SE Bus

A group of 72 lines for Data (SDBI); 22 lines for address (SAB),
9 lines for marks; 6 lines for In Key carry information from the
CE to the SE. The accessed SE gates the signals off the bus.
The SDBI carries the configuration mask during execution of the
SCON instruction.

Interface Signals

Storage Data Bus In (SDBI) - Supplies data from the CE to SE on
Store operations.  During execution of Set Configuration (SCON)
instruction, 16 data bits plus 2 parity bits are transferred to
the SE via this bus.

IOCE Data, Address, Keys In Bus - Provides Address to be accessed and
Key bits for comparison to the protect key stored in the
Storage Protect area of the SE during the initial portion of the
cycle; Data to be stored following ACCEPT for a STORE operation.

Refer to Figure 13-2 for data, address and keys formats for this
bus.  Address and key are put on the buss simultaneously.

Storage Address Bus (SAB) - Consist of Box Tag and Address lines
from the CE to SE.

Marks - Store or regeneration control line for each byte of the
72 bit storage word accessed by the CE.

In Keys - Five key bits from the CE, 4 of which are compared to the
key bits stored in the storage protection area of the SE.  The fifth
bit, if on, indicates fetch protection is active.  The sixth bit is
an odd parity.

Byte Stats (IOCE only) - Four bits plus parity which control storage
of data from DATA BUS IN.  One bit is set for each byte of data to be
stored.  All bytes not having the corresponding STATS bit set are
regenerated to core from the SESDR.

Set Key - Signal from the CE that will inform the storage device to
perform a Set Keys cycle.

Access Request - Signal from IOCE to SE to request priority for a
storage cycle.

Insert Key - Signal from the CE that will inform the storage device
to perform an Insert Keys cycle.

Split Cycle - This signal from the IOCE is not used by the SE but is
terminated by the SE.

Store - Control line from CE or IOCE to SE to permit a data store.

Ignore Errors - This signal from the IOCE is used for normal oper-
ation checking in the SE.  It shall have a terminator associated with
it but will not be used in controlling the 7251-09.  (This signal was
used for diagnostic test purposes in the 9020A System but is not re-
quired in the 9020D/E Systems.)

Test and Set - Signal CE generated:  Control line to perform a Test
and Set cycle in storage.  The byte specified is fetched and forced
to all ones during regeneration.  All other bytes are not affected.

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| BYTE | 0 | | | | | | | | 1 | | | | | | | | 2 | | | | | | | | 3 | | | | | | | | PARITIES | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BUS BIT POS | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 |
| KEYS | 0 | 1 | 2 | 3 | NOTE 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | P | | | |
| ADDRESS | | | | | NOTE 1 | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | P 0-7 | P 8-15 | P 16-23 |
| DATA | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | P 0-7 | P 8-15 | P 16-23 | P 24-31 |

NOTES:
1. WHEN BUS IS USED FOR KEYS AND ADDRESS, BIT POS 4-7 ARE ALWAYS 0.

2. DURING PSBAR ACCESS, KEY BITS ARE FORCED TO 0 AND KEY PARITY TO 1.

3. DURING TEST AND SET OPERATION, ADDRESS BITS 22 AND 23 CONSTITUTE A 2-BIT
   BINARY CODE INDICATING WHICH ONE OF THE 4 BYTES IS TO BE FETCHED AND SET TO ONES.

4. ADDRESS BITS 1, 2, 3, AND 4 ARE BOX TAG BITS USED FOR COMPARISON
   WITH A JUMPER CARD IN THE SE.

Figure 13-2.   IOCE Data Address, Keys in Bus Formats

Signal IOCE generated:  Instruction to SE to Fetch the data byte specified by Address bits 22 and 23 (Bits 30 and 31 of Data, Address Keys in Bus constitute a 2 bit code during Address time of a Test and Set), transmit it to the IOCE and force it to all 1's on the Regeneration cycle.  All other Bytes are regenerated as is.

IOCE Power Bit Interlock - This signal shall inhibit the IOCE interface when inactive.  It is provided from the IOCE on a Last On, First Off basis to assure that power cycling in the IOCE does not generate a false storage operation caused by unstable interface signals.

Cancel - A signal from the CE user to SE that will cause a storage regenerate and no data or error signal transfer.

FLT Load - A signal from the IOCE used for Normal Operation checking only.  (FLTs for the 7201-02 load differently than the 7201-01 and do not require the FLT Load.)

Defeat Interleave - Indicates the Storage Element shall operate in a Defeat Interleave mode.  The SE will substitute Address bit 20 for bit 6 when gating the IOCE Storage Address Buffer Register to the SESAR.  The SE will also sample IOCE Address bit 6 (Bus bit 14) to determine whether the access request is for odd or even.

Address Compare Sync  - Negative significant - provides a scope point for syncing purposes when the setting of the ADDRESS switches on the CE control panel match the SAB and the ADR Compare switch is in the normal position.  Hard wired from CE with no logic involved.

System Reset (1,2) - These signals cause a storage reset at System Reset time.  The signals must go (-) on Line 1 and (+) on Line 2 simultaneously to generate a reset.  They are not gated by CCR bits. They will normally exist as line 1(+) and line 2(-) when not in use.

The CCR is reset to all zeros except parity and SCON bits which are all set ON.

Defeat Interleave Reverse - Identical to Defeat Interleave except that the significance of bit 6 is looked at in reverse when sampling for odd or even.

CE Power On - A ground significant level when power is down in the CE.  This line shall fall prior to CE power going off and remain there until after CE power on reset.  It shall inhibit the output of the associated communication bit in the CCR of the SE.

Double Cycle - Signal CE generated:  Control line to guarantee 2 sequential even or odd storage cycles to the CE.  Inhibits priority scan until second select from issuing CE.  Gated by first cycle Accept.  CE must issue second select within the SE timeout period or a pulsed ELC will be issued, and the unit will become available for new requests immediately.  No wait period (for logout stop) will be initiated.  Outstanding selects will not be reset.

Signal IOCE generated:  Request to SE to grant IOCE two sequential storage cycles (both even or odd).  This request, once granted, inhibits all other users from access to that section of storage until the second cycle has been taken.  The IOCE must generate the second select within the SE timeout period or a Pulsed ELC will be generated.  The SE will not wait for Logout Stop but will become available for access immediately.  Outstanding selects will not be reset.

Normal Op - Signal CE generated:  To assure that control bus driver or receiver failures do not cause multiple instruction execution resulting in data loss.  This signal is valid with Fetch and Store operations only.  If sensed with Test and Set, Set key, Insert key, Suppress Log Check or Double cycle, Address Check will be issued to using CE and entire SE will stop; ELC will be sent to CEs with wait time out set.  If not sensed with Fetch or Store, Address Check, ELC and wait timeout will also be initiated.

Signal IOCE generated:  Raised by IOCE whenever Store or Fetch cycle is requested.  Presense of this signal when Test and Set, Suppress Log Check, Double Cycle, FLT Load, or Ignore Errors operation is requested constitutes an error.  The entire SE will be stopped, storage check will be sent to IOCE and ELC to CEs.  The wait timeout will be set.  Absence of this signal when a store or fetch is requested also constitutes an error.

Select (Even/Odd) - Signal from the CE to SE to request an even or odd storage cycle.

Logout Stop - Signal from CE which sets the SE Stop Latch.  Causes SE to halt all activity at end of cycle in progress (if not already stopped).

Signal from IOCE which sets the SE Stop Latch, causes SE to halt all activity at the end of cycle in progress (if not already stopped).

Logout Select - Signal from CE requesting doubleword of logout data.

Logout Word Number - These three signals gate the logout words to SDBO and are under CE control.  They shall exist in all zero's state when not in use.

Logout Complete - Resets storage following a Logout or when issued as a subsystem reset.  This signal is sensed as a Check Reset.  SE Stopped and outstanding SELECTS are reset at completion of Reset Sequence.

Reconfigure Select - This signal causes SE to gate contents of SDBI to the Configuration Control Register (CCR).  This signal is gated by SCON bit unless CCR Parity error exists or SCON field is zero and SE is not in state zero, in which case SCON bits are ignored.

Suppress Log Check - Suppression of Data Check signal and ELC when this line is active.

Interface From SE.

Storage Data Bus Out (SDBO) - Data from the SE to the CE during either
a Fetch or a Logout operation.

Data Bus Out - Data to IOCE on a Fetch cycle.

Out Keys - Five key bits plus an odd parity bit from SE to the CE on
an Insert Storage Key cycle.

Gate Data - Signal to IOCE indicating that Data Bus Out is being
activated during a Fetch cycle.

Advance SDBO - Signal sent from SE to the CE, in advance of data out.
It will be activated in advance of data on a Fetch cycle and at the
same time on all other cycles.

Advance Keys - Signal from the SE on Insert Key cycle to alert CE
that out Keys are on the bus.

Protection, Address, and Data Checks -

To CE:

Protect Check  - Signal from the SE to the CE that a key mismatch has
                 been detected on a Store or Fetch to a protected
                 location.

Address Check  - Indicates mark parity, address parity, tag parity,
                 tag mismatch, multi-accept condition, storage protect
                 parity, address parity, in key or out key parity and
                 invalid Op errors.  Causes a pulsed ELC to be sent
                 to all CEs.

Data Check     - Indicates a Storage data parity error to the CE, also
                 causes a pulsed ELC.  This signal is inhibited by
                 Suppress Log Check when a data error occurs.

To IOCE:

Protect Check  - Signal to IOCE to indicate that a Key mismatch has
                 been detected on a Store or Fetch operation to a
                 protected address.

Storage Check  - Signal to IOCE to indicate that one of the following
                 errors has occurred in the SE.

                 1.  A parity error on Byte stats, Key, Address, or
                     Data (Check signal upon Data parity error is
                     inhibited by Suppress Log Check).

                 2.  Box Tag mismatch

                 3.  Invalid Op

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4.  Multi-accept

This signal also causes a Pulsed ELC to attached CEs
and starts the wait timeout.

Accept - Indicates to CE that SE has been started in response to its
request (select).

Signal to IOCE requesting data to be placed on the Data bus for
a store operation.

Request Acknowledged - Signal to IOCE to indicate that:

1.  The select has been received

2.  The IOCE is configured to the SE

Logout Advance - Signal to CE that logout data is being placed on
SDBO.

Element Check - To alert all CEs (regardless of configuration) that
the SE has an error condition as follows:

Pulsed ELC's are coincident with:

1.  Configuration Control Register (CCR) parity
2.  Temperature marginal
3.  On Battery Signal
4.  Storage Check, Address Check, Double Cycle Timeout, or
    Data Check Condition.

Static ELCs are coincident with:

1.  Over voltage/over current
2.  Power Off (Normal, Element Master or Loss)
3.  SE Stopped on.

Reconfigure Accept - This signal indicates to the CE that the Con-
figuration Control Register has loaded the data from SDBI and cor-
rect parity exists.

SE Stopped - Indicates to system that SE has received a Logout Stop
signal from an IOCE or CE.  Inhibits all operations except logout,
reconfiguration, or reset.  (CE functions only.)  This signal is de-
gated (CEs only) when the SE is in Defeat Interleave or Defeat Inter-
leave Reverse mode.

Logout SE Stopped - This signal has the same timing as SE Stopped
except that it is not degated in Defeat Interleave or Defeat Inter-
leave Reverse.  The signal enables the CE to properly store the final
word of the SE logout.

SE Ready - Informs CE user that storage is available for use, that
is, power is on, not in test, not configured away from the particular
CE, and the System Reset lines are in their normal states.

SBO Gate - Identify tag used by the CE to identify the SE during a Fetch data cycle.

SYSTEM CONSOLE - SE INTERFACE

The lines which define the interface between the System Console and the SE are listed in Table 13-4.

Table 13-4.  System Console to SE Interface

| Line Name | Number of Lines |
|-----------|-----------------|
| System Status | 1 |
|     State Three | 1 |
|     State Two | 1 |
|     State One | 1 |
|     State Zero | 1 |
| Logic Check | 1 |
| Power Lines | |
|     Emergency Power Off | 3 |
|     Power Check | 1 |
|     Battery | 1 |

State Three - A line indicating that the state bits of the SE Configuration Register are both ones.

State Two - A line indicating that the state bits are:  $S_0=1$, $S_1=0$ in the SE Configuration Register.

State One - A line indicating that the state bits are:  $S_0=0$, $S_1=1$ in the SE Configuration Register.

State Zero - A line indicating that both state bits are zero in the SE Configuration Register.

Logic Check - A line indicating that a Storage Check, Address Check, Data Check or CCR Parity Check has occurred in the SE.

Power Interface Lines

Emergency Power Off- Three lines between the SE and the System Console activate the EPO circuits.

1.  A +24 vdc line from the SE power supply to the console.

2.  0 Volts (24v return from console).

3.  The EPO control line from the console to the SE EPO contactor.

Power Check - A line to the console indicating that the temperature in the SE has drifted to within approximately 10 degrees of the shut down tolerance.  The line also indicates the loss of voltage or a normal power off.

Battery - A line indicating that the SE has switched to battery power.

CE - IOCE INTERFACE

The interface lines between the CE and IOCE are listed in Table 13-5.

Control Bus - The Control Bus contains 36 multiplexed lines:  32 bit positions plus 4 parity bits.  It services the Configuration Control Register, Address Translation Register, I/O instructions, IPL, Logout, I/O Processor, Interrupt signals, and FLT's.

1.  Reconfigure Select and SATR Select use the bus to set the Configuration Control Register or the Address Translation Register.

2.  I/O instructions use the Bus to transmit the channel and unit address, Preferential Storage Base Address (PSBA), and the I/O instruction identification.

3.  IPL uses the bus for the channel and unit address, and PSBA.

4.  Logout uses the bus for PSBA only.

5.  Permit interruption uses the bus for PSBA only.

6.  FLT load uses the bus for PSBA, channel and unit address.

7.  Start I/O Processor uses bus to transmit a Storage Key and an address.

I/O Instruction - A line from the CE to a specific IOCE.  A signal on this line indicates to that IOCE that an instruction, PSBA, and the channel and unit address are on the bus.

Reconfigure Select - A line to the IOCE by which it is indicated that configuration bits are on the bus.

Table 13-5.  CE to IOCE Interface

| Line Name | Number of Lines |
|---|---|
| CE to IOCE | |
|   Control Bus | 36 |
|   I/O Instruction | 1 |
|   Reconfigure Select | 1 |
|   SATR Select | 1 |
|   Initial Program Load | 1 |
|   System Mask | 8 |
|   Subsystem Reset | 1 |
|   System Reset | 2 |
|   Write Direct Stop | 1 |
|   Write Direct Start | 1 |
|   Write Direct Interrupt | 1 |
|   Logout | 1 |
|   Permit I/O Interruption | 1 |
|   Permit MC Interruption | 1 |
|   FLT Load | 1 |
|   FLT Backspace | 1 |
|   360 Mode | 1 |
| IOCE to CE | |
|   Condition Code | 2 |
|   Write Direct Interrupt | 1 |
|   Response | 1 |
|   I/O Interruption Request | 1 |
|   MC Interruption Request | 1 |

Table 13-5.  CE to IOCE Interface con't.

| Name of Line | Number of Lines |
|---|---|
| External Interruption | 2 |
| Reset Timeout | 1 |
| FLT Complete | 1 |
| PSA Lockout | 1 |
| Check Response | 1 |
| SCON/SATR Response | 1 |
| Tic | 1 |
| Gap | 1 |

Table 13-6.  IOCE to System Console Interface

| Name of Line | Number of Lines |
|---|---|
| IOCE to System Console | |
| State Three | 1 |
| State Two | 1 |
| State One | 1 |
| State Zero | 1 |
| Logic Check | 1 |
| Power Check | 1 |
| Battery | 1 |
| Emergency Power Off | 3 |

SATR Select - A line to the IOCE which indicates that the IOCE is selected to receive a new ATR mask.

Initial Program Load - A line by which an IPL is initiated in the IOCE - PSBA, channel address, and unit address are coincidently on the bus.

System Mask - The PSW System Mask bits (0-6 and 16-19) are trans-
mitted to the IOCE's as follows:  Bits 0-3 to IOCE 1, bits 4-6 and
16 to IOCE 2 and bits 17-19 to IOCE 3 for interruption masking.  In
addition, bits 16-19 are sent on separate lines to each IOCE to be
used in forming the first portion of the byte (bits 16-23) of the
PSW on permitted interruptions.  This is done so that correct parity
can be assigned to that byte before storing.  (The IOCE forms
position 16-31 of the I/O Old PSW.)

Subsystem Reset - A line by which the IOCE is signaled to do an
element reset provided the IOCE is configured to the sending CE
(CCR is not affected).

System Reset - A 1 msec. signal, double rail (two lines) which
precedes a system IPL.  It will perform hardware and microprogram
reset in the IOCE provided the Test Switch is not on, and prepare
the IOCE to take a SCON instruction.  CCR is set to zeros except
for the SCON bits which are set to ones.

Write Direct Stop - A line by which the I/O Processor is signalled
to stop processing at the end of the current instruction.

Write Direct Start - A line by which the I/O Processor is signalled
to start processing using its current PSW.

Write Direct Interrupt - A line by which the I/O Processor is
signalled to take an external interrupt.

Logout - A signal from the CE to the IOCE which sets the CE logout
request bit in the Check Register 2.  This forces the IOCE to
simulate a check condition stop and issue an Element Check and an
MC (Machine Check) Interruption Request to the CE.

Permit I/O Interruption - A reply to the IOCE in answer to an I/O
interruption request allowing the IOCE to store its CSW and the
interruption code field of the PSW.

Permit MC Interruption - A reply to the IOCE in answer to an MC
Interruption Request allowing the IOCE to logout.  The logout
consists of basic data flow, one selector channel, common channel,
multiplexor channel, check registers and configuration register.
PSBA is coincidentally on the bus.

FLT Load - This line is not used by the CE.

FLT Backspace - A line which causes the IOCE to branch from its
Wait loop and causes one record from the FLT Tape to be backspaced.
When the operation is completed, an FLT Complete signal is sent to
the CE.

360 Mode - A line which causes the IOCE to operate in the System/360
Mode.

Interface from IOCE

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Condition Code - Two lines which indicate to the CE what value to set in the Condition Code Register to complete the I/O or Write Direct instruction.

Write Direct Interrupt - A line by which the CE is signalled by the I/O Processor to take an external interrupt.

Response - A line sent to the CE to indicate that the condition code for an I/O or Write Direct instruction is present, IPL is complete, I/O or MC interruption is complete (CSW and portion of PSW stored in SE), or IOCE logout is complete.

I/O Interruption Request - A line sent to the CE indicating an unmasked interruption condition is present in a channel. The line is gated in the IOCE with the system mask bits.

MC Interruption Request - A line to the CE by which the IOCE signals that it has a condition requiring a machine check interruption.

External Interruptions - Two lines to the CE encoded to indicate Element Check (ELC), on battery signal (OBS), and/or out of tolerance (OTC)

ELC indicates:

1. CCR parity

2. Common logic check

3. Power Failure

Reset Time Out - A line sent to the CE indicating the IOCE will process the I/O instruction but is presently processing data. It prevents the CE from timing out of its "count-down" loop.

FLT Complete - Indicates to the CE that the operation started by the FLT Backspace is completed.

PSA Lockout - A line to the CE indicating a failure in attempting to access a preferential storage area. This line causes a program interruption in the CE.

Check response - A line to the CE which is used to signal that a tape error was detected during an FLT Load operation. When the CE is not in the FLT mode, this line indicates that a parity check has been detected in the IOCE on data from the CE via the Control Bus, except for the SCON configuration mask.

SCON/SATR Response - A line sent to the CE to indicate that configuration data or address translation data have been properly recieved.

TIC - A line sent to the CE to indicate a Transfer in Channel.

GAP - A line sent to the CE to indicate end of record.

IOCE - SYSTEM CONSOLE INTERFACE

IOCE - System Console Interface lines are listed in Table 13-6.
Lines are listed between the System Console and only one IOCE. This
interface also includes the Input/Output Interface. Channel to
Device Control Unit, described in Appendix D.

State Three - A line indicating that the state bits of the IOCE
Configuration Register are both ones.

State Two - A line indicating that the state bits are: $S_0=1$, $S_1=0$
in the IOCE Configuration Register.

State One - A line indicating that the state bits are: $S_0=0$, $S_1=1$
in the IOCE Configuration Register.

State Zero - A line indicating that both bits are zero in the IOCE
Configuration Register.

Logic Check - A line indicating that a logic check has occurred in
the IOCE.

Power Check - A line to the console indicating that the temperature
in the IOCE has drifted to within approximately 10 degrees of the
shut down tolerance. The line also indicates the loss of a voltage
or a normal power off.

Battery - A line indicating that the IOCE has switched to battery
power.

Emergency Power Off - Three lines between the IOCE and the system
console activate the EPO circuits.

    1.  A +24v. DC line from the IOCE power supply to the console.

    2.  0 Volts (24v return from console).

    3.  The EPO control line from the console to the IOCE EPO
       contactor.

CE - SYSTEM CONSOLE INTERFACE

The CE- System Console Interface Lines are listed in Table 13-7.
These lines are listed between one CE and the System Console.

CE Interface to System Console

Load Line - Carries signal to the console to indicate that load
sequence is in process; turns Load Indicator on.

Data Indicator Lines - Provide data from T register for data dis-
play indicators.

IC Indicator Lines - Provide data for IC display indicators.

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Table 13-7.  CE to System Console Interface

| Name of Line | Number of Lines |
|---|---|
| CE to System Console | |
| Load | 1 |
| Data Indicators (T Register) | 36 |
| IC Indicators | 27 |
| Manual Indicator | 1 |
| Wait Indicator | 1 |
| State Three | 1 |
| State Two | 1 |
| State One | 1 |
| State Zero | 1 |
| Logic Check | 1 |
| Power Check | 1 |
| Battery | 1 |
| Emergency Power Off | 3 |
| Invalid Storage | 1 |
| System Console to CE | |
| Computing Element Select | 1 |
| Stop | 1 |
| Start | 1 |
| Address Keys | 27 |
| Data Keys | 36 |
| Storage Select (Main Position) | 1 |
| Display | 1 |
| Store | 1 |

Table 13-7.  CE to System Console Interface (Cont'd)

| Name of Line | Number of Lines |
|---|---|
| Set IC | 1 |
| Interrupt | 1 |
| Address Compare | 2 |
| Rate | 1 |
| Load | 1 |
| Channel Address | 5 |
| Unit Address | 9 |
| Main Storage Select | 5 |
| Activate | 1 |
| Control CE | 3 |
| All Stop | 1 |

Manual Indicator Line - Provides indication signal that the CE is in the Stopped State.

Wait Indicator Line - Provides indication that the CE is in the Wait State.

State Three - A line indicating that the state bits of the CE Configuration Register are both ones.

State Two - A line indicating that the state bits are: $S_0 = 1$, $S_1 = 0$ in the CE Configuration Register.

State One - A line indicating that the state bits are: $S_0 = 0$, $S_1 = 1$ in the CE Configuration Register.

State Zero - A line indicating that both state bits are zero in the CE Configuration Register.

Logic Check - A line indicating that a logic check has occurred in the CE.

Power Check - A line to the console indicating that the temperature in the CE has drifted to within approximately 10 degrees of the shut down tolerance.  The line also indicates the loss of voltage or a normal power off.

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Battery - A line indicating that the CE has switched to battery power.

Emergency Power Off - Three lines between the CE and the system console activate the EPO circuits.

     1.  A +24v DC line from the CE power supply to the console.

     2.  0 Volts (24v return from console).

     3.  The EPO control line from the console to the CE EPO contactor.

Invalid Storage - A line to turn on the indicators to indicate that an invalid address has been specified with the address keys.

System Console Interface to - CE

Computing Element Select Line - Indicates to CE that it is being addressed by console.

Stop Line - Provides Stop signal to selected CE.

Start Line - Provides Start signal to selected CE.

Address Switches Lines - Provide an address to the selected CE for one of several purposes.

Data Switches Lines - Provide data to the selected CE.

Storage Select Line - Provides indication to CE that an SE address is being selected.

Display Line - Provides a display indication to selected CE.

Store Line - Provides a store indication to selected CE.

Set IC Line - Provides a Set Instruction Counter indication to selected CE.

Interrupt Line - Causes a bit in the External Interruption Register in the selected CE to be set.

Address Compare Lines - Cause one of two signals, depending on the switch setting, to initiate the address compare sequence.  In the process position, no further action required by the CE.

Rate Line - Used to indicate to the selected CE the processing rate for instructions; normal or instruction step.

Load Line - Used to initiate in the selected CE the initial program loading sequence.

Channel Address Lines - Used to transmit to the selected CE the I/O channel to be used as part of the IPL sequence.

Unit Address Lines - Provides the selected CE with the device address for the IPL sequence.

Main Storage Select Lines - Provides the SE Element number to the selected CE for the IPL sequence.

Activate Line - Provides the selected CE with Control CE initiate signal.

Control CE Lines - Provides the selected CE with the data to insert into the SCON bits of the CE's CCR.

All Stop Line - Provides a Stop signal to the CE (all CEs receive this signal regardless of CE Select switch setting.

PAM - SYSTEM CONSOLE INTERFACE

The PAM - System Console Interface lines are listed in Table 13-8 for the lines between one PAM and the System Console.

State Three - A line indicating that the state bits of the PAM Configuration Register are both ones.

Table 13-8.  PAM to System Console Interface

| Name of Line | Number of Lines |
|---|---|
| PAM to System Console | |
|     State Three | 1 |
|     State Two | 1 |
|     State One | 1 |
|     State Zero | 1 |
|     Logic Check | 1 |
|     Power Check | 1 |
|     Emergency Power Off | 3 |

State Two - A line indicating that the state bits are: $S_0=1$, $S_1=0$ in the PAM Configuration Register.

State One - A line indicating that the state bits are: $S_0=0$, $S_1=1$ in the PAM Configuration Register.

State Zero - A line indicating that both state bits are zero in the PAM Configuration Register.

Logic Check - A line indicating that a logic check has occurred in the PAM.

Power Check - A line to the console indicating that the temperature in the PAM has drifted to approximately 10 degrees below the nominal thermal protection temperature. The line also indicates the loss of a voltage or a normal power off.

Emergency Power Off - Three lines between the PAM and the system console activate the EPO circuits.

    1.  A +24v DC line from the PAM power supply to the console.

    2.  0 Volts (24v return from console)

    3.  The EPO control line from the console to the PAM EPO contactor.

TCU - SYSTEM CONSOLE INTERFACE

The Tape Control Unit - System Console Interface lines are listed in Table 13-9. Lines are listed between only one TCU and the System Console.

Table 13-9. TCU to System Console Interface

| Name of Line | Number of Lines |
|---|---|
| TCU to System Console | |
|   State Three | 1 |
|   State Two | 1 |
|   State One | 1 |
|   State Zero | 1 |
|   Logic Check | 1 |
|   Power Check | 1 |
|   Emergency Power Off | 3 |

State Three - A line indicating that the state bits of the TCU Configuration Register are both ones.

State Two - A line indicating that the state bits are: $S_0=1$, $S_1=0$ in the TCU Configuration Register.

State One - A line indicating that the state bits are: $S_0=0$, $S_1=1$ in the TCU Configuration Register.

State Zero - A line indicating that both state bits are zero in the TCU Configuration Register.

Logic Check - A line indicating that a logic check has occurred in the TCU.

Power Check - A line to the console indicating that the temperature in the TCU has drifted to within approximately 10 degrees of the shut down tolerance. The line also indicates the loss of a voltage or a normal power off.

Emergency Power Off - Three lines between the TCU and the system console activate the EPO circuits.

1. A +24v DC line from the TCU power supply to the console.

2. 0 Volts (24v return from console)

3. The EPO control line from the console to the TCU EPO contactor.

SCU - SYSTEM CONSOLE INTERFACE

The Storage Control Unit - System Console Interface lines are listed in Table 13-10. Lines are listed between only one SCU and the System Console.

Table 13-10. SCU to System Console Interface

| Name of Line | Number of Lines |
|---|---|
| SCU to System Console | |
| State Three | 1 |
| State Two | 1 |
| State One | 1 |
| State Zero | 1 |
| Logic Check | 1 |
| Power Check | 1 |
| Emergency Power Off | 3 |

State Three - A line indicating that the state bits of the SCU Configuration Register are both ones.

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State Two - A line indicating that the state bits are: $S_0=1$, $S_1=0$ in the SCU Configuration Register.

State One - A line indicating that the state bits are: $S_0=0$, $S_1=1$ in the SCU Configuration Register.

State Zero - A line indicating that both state bits are zero in the SCU Configuration Register.

Logic Check - A line indicating that a logic check has occurred in the SCU.

Power Check - A line to the console indicating that the temperature in the SCU has drifted to within approximately $10^o$ of the shut down tolerance. The line also indicates the loss of a voltage or a normal power off.

Emergency Power Off - Three lines between the SCU and the system console activate the EPO circuits.

1. A +24v dc line from the SCU power supply to the console.

2. 0 Volts (24v return from console).

3. The EPO control line from the console to the SCU EPO contactor.

CE - SCU INTERFACE

The CE - SCU communications interface performs two functions: (1) it allows the SCU to receive configuration information from the CE; and (2) allows the SCU to present an interruption signal to the CE upon the detection of certain malfunctions. The interface lines are listed in Table 13-11.

The interface consists of sixteen lines; fourteen carry signals from the CE to the SCU, and two carry signals from SCU to the CE. These lines are described below.

Table 13-11. CE to SCU Interface

| Name of Line | Number of Lines |
|---|---|
| CE to SCU | |
| Configuration Data Bus | 11 |
| Reconfigure Select - Response | 1 |
| System Reset | 2 |
| SCU to CE | |
| Element Check | 1 |

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Configuration Data Bus - An eleven-bit bus carries the configuration mask of the Configuration Control Register (CCR) to the SCU during the execution of a SCON instruction by the CE.

Reconfigure Select - Response - A line provided to signal the SCU to accept the information on the Configuration Data bus. It is effective at the SCU if the CE issuing the Reconfigure Select has its SCON bit set in the CCR of the SCU and if the SCU is not in State Zero with the Test Switch on. This line is also activated by the SCU when the configuration data is accepted by the SCU with correct parity.

System Reset - The SCU will reset provided a signal is simultaneously received on the two reset lines.

SCU-CE INTERFACE

Element Check (ELC) - This line is used to set a bit in the Diagnose Accessible Register (DAR) in the CE when one or more of the following conditions are detected in the SCU:

1. Power Failure.

2. Parity Check in the CCR.

An interruption is taken by the CE provided the SCU bit is not masked off.

CE - TCU INTERFACE

The CE - TCU communications interface performs two functions: (1) it allows the TCU to receive configuration information from the CE; and (2) allows the TCU to present an interruption signal to the CE upon the detection of certain malfunctions. The interface lines are listed in Table 13-12.

The interface consists of sixteen lines; fourteen carry signals from the CE to the TCU, and two carry signals from TCU to the CE. These lines are described below.

Table 13-12. CE to TCU Interface

| Name of Line | Number of Lines |
|---|---|
| CE to TCU | |
|   Configuration Data Bus | 11 |
|   Reconfigure Select - Response | 1 |
|   System Reset | 2 |
| TCU to CE | |
|   Element Check | 1 |

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Configuration Data Bus - An eleven-bit bus carries the configuration mask of the Configuration Control Register (CCR) to the TCU during the execution of a SCON instruction by the CE.

Reconfigure Select - Response - A line provided to signal the TCU to accept the information on the Configuration Data bus.  It is effective at the TCU if the CE issuing the Reconfigure Select has its SCON bit set in the CCR of the TCU and if the TCU is not in State Zero with the Test Switch on.  This line is also activated by the TCU when the configuration data is accepted by the TCU with correct parity.

System Reset - The TCU will reset provided a signal is simultaneously received on the two reset lines.

TCU-CE INTERFACE

Element Check (ELC) - This line is used to set a bit in the Diagnose Accessable Register (DAR) in the CE when one or more of the following conditions are detected in the TCU:

    1.  Power Failure.

    2.  Parity Check in the CCR.

An interruption is taken by the CE provided the TCU bit is not masked off.

CE-PAM INTERFACE

The CE-PAM communications interface performs two functions: (1) it allows the PAM to receive configuration from the CE; and (2) allows the PAM to present an interruption signal to the CE upon the detecting of certain malfunctions.  Interface lines are listed in Table 13-13.

Table 13-13.  CE to PAM Interface

| Name of Line | Number of Lines |
|---|---|
| CE to PAM | |
|     Configuration Data Bus | 11 |
|     Reconfigure Select-Response | 1 |
|     System Reset | 2 |
| PAM to CE | |
|     Element Check | 1 |

The interface consists of sixteen lines. Fourteen carry signals from the CE to the PAM and two carry signals from the PAM to the CE.

Configuration Data Bus - An eleven-bit bus carries the configuration mask to the Configuration Control Register (CCR) during the execution of a SCON instruction by the CE.

Reconfigure Select-Response - This line is provided to signal the PAM to accept information on the Configuration Data Bus. It is effective at the PAM if the CE issuing the Reconfigure Select has its SCON bit set in the CCR of the PAM and if the PAM is not in State Zero with the Test Switch on. The line is also activated by PAM when the configuration data was accepted by the PAM with correct parity.

System Reset - The PAM will reset provided a signal is simultaneously received on the two reset lines.

PAM-CE INTERFACE

Element Check (ELC) - This line is used to set a bit in the Diagnose Accessible Register (DAR) in the CE when one or more of the following conditions are detected in the PAM:

1.  Check-Stop error in priority controls

2.  Power failure

3.  Parity check in the CCR.

Provided that the PAM bit is not masked off in the DAR Mask and bit 7 of the PSW is not also masked off, an interruption is taken in the CE.

TCU - TAPE UNIT INTERFACE

The TCU-tape unit interface lines are listed in Table 13-14. Interface lines listed are those connecting one TCU and tape unit.

The interface consists of forty-seven lines; twenty-six carry signals from the TCU to tape unit, and twenty-one carry signals from the tape unit to the TCU. These lines are described below.

Interface to Tape Unit

Select - This input line (one of eight select lines) selects a particular tape unit from the group connected in-line to the common control unit. This signal gates the tape unit selected, allowing it to receive and transmit all subsequent signals from and to the control unit.

Table 13-14. TCU - Tape Unit Interface

| Line Name | Number of Lines |
|---|---|
| To Tape Unit | |
|   Select | 8 |
|   Go | 1 |
|   Backward | 1 |
|   Set Read Status | 1 |
|   Set Write Status | 1 |
|   Write Pulse | 1 |
|   Write LRCC Gate/Set NRZI | 1 |
|   Write Bus | 9 |
|   Rewind | 1 |
|   Rewind/Unload | 1 |
|   Metering Out | 1 |
| From Tape Unit | |
|   Models 1/4, 2/5, 3/6 | 3 |
|   Rewinding/Not Ready | 1 |
|   Seven Track/NRZI | 1 |
|   Select and Read Status | 1 |
|   Write Echo/Select and TI Off | 1 |
|   Select and TI Off/Inhibit Go | 1 |
|   Select and Not File-Protected | 1 |
|   Read Bus | 9 |
|   Backward Status | 1 |

Go - This line controls tape motion; it is conditioned after the status lines have been set to establish the operation to be performed. The Go line must be active for all operations that move tape forward or backward, except for rewind and rewind/unload. For these operations, tape motion is controlled internally.

Backward - This line sets the tape unit in backward status. If the Go line is active with 'backward status' set, tape moves backward; if backward status is not set, tape moves forward. The tape unit remains in backward status, unless reset by Set Read Status or Set Write Status. Since tape can only be written forward, 'backward' sets Read Status in the tape unit and may turn off T1.

Set Read Status - This input line sets the tape unit in read status and deconditions the write circuits. The tape unit remains in read status until Set Write Status becomes active. Set Read Status presumes a forward read and therefore resets 'backward status.'

Set Write Status - This input line sets the tape unit in write status and conditions the write circuits. The tape unit remains in write status until Set Read Status or Backward becomes active. Set Write Status also resets backward status.

NOTE: Because write checking is accomplished by reading, read circuits are conditioned during both read and write operations.

Write Pulse - These input pulses are sent into the tape unit on a line common to the write circuits of all nine tracks. This line is a sync pulse for the recording of data bytes and check characters. When active, this line signals the tape unit to write a bit in each track whose corresponding write bus position is active. It is also used with the write longitudinal redundancy check character (LRCC) gate line to write the LRC character.

Write LRCC Gate/Set NRZI - When this line is inactive, Write Pulse writes data. When this line is active, Write Pulse writes the LRC character.

Write Bus - These nine input signal lines (0-7 and P) gate the Write Pulse to the write circuits of each track. When a write bus is active (down), a 1-bit is recorded; otherwise, a 0-bit is recorded in the associated track. The up or down level of these lines is determined by the coded data sent to the tape control unit.

Rewind - This input line causes the tape unit to perform a rewind operation (tape is rewound to the load point). Rewind also turns off T1. Rewind is at high speed if there is more than approximately 1/2 inch of tape on the take-up reel; otherwise, it is a low speed rewind.

Rewind/Unload - Like Rewind, this line causes a rewind of tape to load point but continues to unload tape (and lower the power window, if present) preparatory to changing reels. Rewind/Unload also turns off T1.

Metering Out - This input line is active when the systems conditions are met for running usage meters and the control unit is not off-line. The tape unit meter stops only if the metering-out line becomes inactive, if the tape unit is unloaded and not rewinding, or if the tape unit is at load point. Metering out is terminated in each individual tape unit.

Interface to TCU

Models 1/4, 2/5, 3/6 - These output lines indicate the tape unit model and that the tape unit is selected and ready. Each tape unit activates only one of the three lines.

Rewinding/Not Ready - This output line carries a unique tape unit
address (0-7); it indicates that the tape unit is physically connect-
ed but not ready.  A tape unit is not ready if it is unloaded, in re-
set status, or performing a rewind operation.

On a Rewind/Unload command, the tape unit drops the Model line
before activating the Rewinding/Not Ready line.

Seven Track/NRZl - This output line indicates that the seven-track
feature is installed in the selected tape unit; suitable timing
circuits in the control unit are conditioned.  Seven track/NRZl may
only be active concurrently with the 'Model 1/4, 2/5, 3/6' line.

Select and Read Status - The read/write status of a selected tape
unit is indicated to the control unit through the Select and Read
Status line.  When active, this line indicates read status; when in-
active, this line indicates write status.  The Select and Read Status
line is effective, however, only while a 'Model 1/4, 2/5, 3/6' line
is active.

Select and at Load Point - This line indicates that the tape on the
selected tape unit is positioned at load point.  This line is reset
if the tape is unloaded and not rewinding or if tape is moved for-
ward.

Write Echo/Select and T1 Off - This line is activated or pulsed by
the tape unit each time a bit is written on tape.

Select and T1  Off/Inhibit Go - This line is active when the tape
indicator of the selected tape unit is off; this indicates that the
selected tape unit has not reached the useful end of tape.  T1 is
set by sensing the end-of-tape reflective marker during a forward
tape operation; it is reset by a backward, rewind, or unload opera-
tion.

Select and Not File-Protected - This line indicates that a selected
and ready tape unit may perform a write operation because it is not
file-protected.  A tape unit is file-protected (writing or erasing
of tape is prevented) when the file reel does not contain a write-
enable ring.

Read Bus - These nine lines (0-7 and P) carry the read signals from
the tape unit to the tape control unit for a read operation.

Backward Status - This line is active when the tape unit is in back-
ward status.  Conditioning the go line causes backward motion of
tape; as  for example, in backspacing.

PRINTER - CONTROL UNIT (ICU) INTERFACE

Printer- control unit interface lines are listed in Table 13-15.
These lines are described below.

Interface to Printer

Hammer Drive - The 132 drive lines are individually controlled and driven from -60V to ground for a period of 1.05 to 1.38 ms to fire the hammers.  Internal connections to the magnets are made through hammer unit connector cards.

Restore Key - This line ties down the restore key n/c point when the key is operated.

Print - For each line printed, this line receives a +U(+Y) impulse (minimum of 2 ms) from the processing unit to start the printer usage (time-recording) meter.

Process M - This line is at -U(-Y) when the processing unit is active.  It AND's with the print line to control the usage meter in the printer.

Low-Speed Start Indicate - This line is shifted to -2V to light an indicator light when the carriage low-speed start magnet is energized.  Light is returned to -12V in the printer.

High-Speed Start Indicate - This line is shifted to -2V to light an indicator light when the carriage high-speed start magnet is energized.  The light is returned to -12V in the printer.

Low-Speed Stop Indicate - This line is shifted to -2V to light an indicator light when the carriage low-speed stop magnet is energized. The light is returned to -12V in the printer.

High-Speed Stop Indicate - This line is shifted to -2V to light an indicator light when the carriage high-speed stop magnet is energized.  The light is returned to -12V in the printer.

Print Ready Indicator - This line is shifted to -2V to light an indicator if an error occurs in any of the print-control circuitry. The light is returned to -12V in the printer.

End-of-Forms Indicator - This line is shifted to -2V to light an indicator light when the end-of-forms switch is actuated.  The light is returned to -12V in the printer.

Sync Check Indicator - This line is shifted to -2V to light an indicator light when the print-control circuitry in the processing unit is not in time with the sense amplifier pulses.  The light is returned to -12V in the printer.

STL 1-8 - These eight separate input lines from the system drive the individual tape feed magnets when the printer is using the selective tape lister feature.

Dampener Magnet Drive - This single line from the system energizes the acoustical paper-dampener magnets on the Model 3.

Table 13-15.  Printer-Control Unit Interface

| Line Name | Number of Lines |
|---|---|
| To Printer | |
|   Hammer Drive | 132 |
|   Restore Key | 1 |
|   Print | 1 |
|   Process M | 1 |
|   Low-Speed Start Indicate | 1 |
|   High-Speed Start Indicate | 1 |
|   Low-Speed Stop Indicate | 1 |
|   High-Speed Stop Indicate | 1 |
|   Print Ready Indicator | 1 |
|   Print Check Indicator | 1 |
|   End-of-Forms Indicator | 1 |
|   Sync Check Indicator | 1 |
|   Dampener Magnet Drive | 1 |
|   Low-Speed Start | 1 |
|   Low-Speed Stop | 1 |
|   High-Speed Start | 1 |
|   High-Speed Stop | 1 |
|   Forms-Check Indicator | 1 |
| From Printer | |
|   Forms-Check or Carriage Stop | 1 |
|   Start Relay Control | 1 |
|   Forms Check or Carriage Stop | 1 |
|   Carriage Interlock | 1 |
|   Chain (or Train) Motor Relay | 1 |
|   End-of-Forms | 1 |
|   Start Relay | 1 |
|   Restore Key | 2 |
|   Sense Amplifier 1 | 1 |
|   Sense Amplifier 2 | 1 |
|   Check Reset | 1 |
|   Emitter | 1 |
|   Stop Key | 1 |

Table 13-15. Printer-Control Unit Interface (cont'd)

| Line Name | Number of Lines |
|---|---|
| From Printer | |
| Single Cycle | 2 |
| Start Key | 1 |
| Not Start Key | 1 |
| Space Key | 2 |
| Lister Op | 1 |
| Slow Brushes 1-12 | 12 |
| Stop Brushes 1-12 | 12 |

Low-Speed Start/Low Speed Stop - These lines are to the low-speed carriage control magents.  OFF is -60V (+60V on some Model 2s).  ON is ground level.  One line must be on, and one line off at all times when the carriage is operating.

High-Speed Start/High-Speed Stop - These lines are to be high-speed carriage control magnets.  OFF is -60V (+60V on some Model 2s).  ON is ground level.  One line must be on, and one line off at all times when the carriage is operating.

Forms-Check Indicator - This line is shifted to -2V to light an indicator light when a forms-check switch is actuated at any one of the four tractor doors.  The light is returned to -12V in the printer.


Interface to Control Unit

Forms-Check or Carriage Stop - This line shifts from -12V to floating if a paper jam operates any one of the four forms-check switches or if the carriage-stop key is pressed.

Start Relay Control - This line is commoned to the -T Start Relay line when either the start key or remote-start key is pressed.  This can be used as a start-control line.

Forms Check or Carriage Stop - This line is used in the Models 4, 5, and 6 only.  It shifts from -12V to floating if a paper jam operates any one of the four forms-check switches, or if the carriage-stop key is pressed.

Carriage Interlock - This line shifts from -12V to floating when either the carriage-control tape brushes are raised, or the 6-8 line-shift lever is operated.  The carriage stop magnets should be held on, and the carriage-start magnets held off when the -12V is removed from this line.

Chain (or Train) Motor Relay - This line goes from -60V dc to float-
ing if the T-frame is unlatched, or if either thermal switch in the
chain (or train) motor or hammer unit opens from overheating.  This
line is +60V dc on some Model 2s.

End-of-Forms - This line goes from floating to -12V if either form-
actuated switch is operated.  This indicates that no form is over the
switch.


-T Start Relay - See -T Start Relay Control.

+U(+Y) Restore Key/-T(-Y) Restore Key - A +6V through a 560-ohm re-
sistor is shifted from the +U(+Y) Restore Key line to the -T(-Y)
Restore Key line when the Carriage Restore key is pressed.  This re-
stores the carriage to home position as determined by the carriage-
control tape.

Sense Amplifier 1/Sense Amplifier 2 - These lines supply one pulse
for each slot in the chain (train) timing drum.  Amplitude is from
.5V to 1.0V peak to peak.  Output is push-pull.

Check Reset - This line shifts from -12V to +6V when the Check Reset
key is pressed.  This resets error latches in the printer error-
detection circuitry in the processing unit.

E1 Emitter - This line goes from ground to -12V when a tooth on the
E1 emitter wheel passes its magnetic head.  The emitter provides a
pulse for each carriage line space.  These pulses are normally used
for double and triple-spacing, and also skipping.

Stop Key - This line goes from floating to -6V when either the stop
key or remote-stop key is pressed.  This provides a signal that stops
operation of the process unit.

-T(-Y) Single Cycle/+U9+Y) Single Cycle - Through a 560-ohm resistor,
+6V is shifted from the -T(-Y) Single Cycle line to the +U(+Y) Single
Cycle line when the single-cycle key is pressed.  It causes the print-
er to print one line of information.

Start Key - This line goes from floating to ground when either the
Start key or Remote-Start key is pressed.

+U(-Y)Not Start Key - This line goes from ground to -12V when either
the Start key or Remote-Start key is pressed.

+U(+Y) Space Key/-T(-Y) Space Key - A +6V through a 560-ohm resistor
is shifted from the -T(-Y) line to the +U(+Y) line SC-1/157 to SC-
1/156 when the carriage space key is pressed.  It advances the car-
riage one space.

Lister Op - This is a single output line activated by a switch to
indicate when the selective tape lister device is in position to be
operated.

Slow Brushes 1 to 12 - These lines go from floating to -20V when the brush makes to the contact roll through a hole in the paper carriage-control tape.

Stop Brushes 1 to 12 - These lines go from floating to -20V when the brush makes to the contact roll through a hole in the paper carriage-control tape.


2821-2540 INTERFACE

The 2821-2540 interface lines are listed in Table 13-16. Interface lines listed are those connecting one 2821 and 2540.

The interface consists of fifty-eight lines; thirty-eight carry signals to the 2540, and twenty lines carry from the 2540 to the 2821. These lines are described below.


Interface to 2540

Data Scan Address Lines - Two out of five code which is decoded into bit addresses 00 through 80. Each address transition must occur at 000 time. (Ten lines).

2821 PCH Ready Turn Off - Optional means of externally forcing not ready condition. Ready will not drop, however, until PCH Write is down.

Time 150-450 - 1.5 to 4.5 usec of 6usec scan cycle.

Read Cycle - Indicates address being decoded is for reader. Must rise and fall at 000 time.

Punch Cycle - Indicates address being decoded is for punch. Must rise and fall at 000 time.

Time 225-525 - 2.25 to 5.25 usec of 6 usec scan cycle.

2821 RDR Ready Turn Off - Optional means of externally forcing not ready condition. Ready will not drop, however, until RDR Feed Command is down.

Punch Decode - Serial string of bits synchronous with addresses to be punched in row of card. To punch a bit, this line must be true before 225 and must not fall until after 525.

Punch Write - Indicates that a punch feed command is pending or in progress. Prevents dropping punch ready.

Time 075-150 - .75 to 1.50 usec of 6 usec scan cycle.

Punch Restart Gate - Indicates a PFR write command.

Time 150-375 - 1.50 to 3.75 usec of 6 usec scan cycle.

Unit Exception RDR - Indicates a Read Feed command was issued to the reader after the last card was read and stacked.

RDR Feed Command - Indicates that a Read Feed command is pending or is in progress. Prevents dropping of Reader Ready.

Read Feed - Command 2540 to pick reader clutch and feed a card.

Punch Feed - Command 2540 to pick punch clutch and feed a card.

Power On Reset - Active from start of power on sequence until power on is complete. Also conditions MACH Resets.

Mach Reset Reader - Reinitialize 2540 circuits to logical starting point.

Mach Reset PCH - On standard machines, this line is not used and Reader and PCH Machine Resets are tied together.

Xfer CY RQ - Allows scan cycles to be interrupted for the duration Xfer CY RQ. This line must not be active concurrently with Read Cycle or Punch Cycle. Rise and fall must occur at 000 time.

Reader Check - Lights Read Check light if reader error detected.

Validity - Lights Reader validity light if invalid card code detected.

Punch Check - Lights punch check light if punch error detected.

PCH PFR Validity - Lights validity light on punch if invalid card code detected.

Stacker P2 - Comes up with Punch Clutch Set and Punch Feed. Goes down with next Punch Clutch Set (292° to 22°). Is also active with Stacker P3.

Stacker P3 - Comes up with Punch Clutch Set and Punch Feed. Goes down with next Punch Clutch Set (292° to 22°). Also activates Stacker P2.

Stacker R2 - Timing coincides with RDR CL LAT Not NPRO. This line must also be active with Stacker R3.

Stacker R3 - Timing coincides with RDR CL LAT Not NPRO. This line must also activate Stacker R2.

2540 Meter Run - Causes the 2540 meter to run when this line is up, there are cards in either feed, and Xfer CY RQ is activated. Meter will continue to run until both feeds are empty of cards.

Table 13-16.  2821 to 2540 Interface

| Line Name | Number of Lines |
|---|---|
| Interface to 2540 | |
| Data Scan Address Lines | 10 |
| 2821 PCH Ready Turn Off | 1 |
| Time 150-450 | 1 |
| Read Cycle | 1 |
| Punch Cycle | 1 |
| Time 225-525 | 1 |
| 2821 RDR Ready Turn Off | 1 |
| Punch Decode | 1 |
| Punch Write | 1 |
| Time 075-150 | 1 |
| Punch Restart Gate | 1 |
| Time 150-375 | 1 |
| Unit Exception RDR | 1 |
| RDR Feed Command | 1 |
| Read Feed | 1 |
| Punch Feed | 1 |
| Power On Reset | 1 |
| Mach Reset Reader | 1 |
| Mach Reset PCH | 1 |
| Xfer CY RQ | 1 |
| Reader Check | 1 |
| Validity | 1 |
| Punch Check | 1 |
| PCH PFR Validity | 1 |
| Stacker P2 | 1 |
| Stacker P3 | 1 |
| Stacker R2 | 1 |
| Stacker R3 | 1 |
| 2540 Meter Run | 1 |

| Table 13-16.   2821 to 2540 Interface (cont'd)

| Line Name | Number of Lines |
|---|---|
| Interface From 2540 | |
|   RD1 Row-Bit | 1 |
|   RD2 Row-Bit | 1 |
|   PCH CHK Row-Bit | 1 |
|   PFR RD Row-Bit | 1 |
|   Punch Scan | 1 |
|   After 9 Emitter | 1 |
|   PCH Clutch Set | 1 |
|   Unit Exception | 1 |
|   PCH Brush Impulse | 1 |
|   PCH Brush CL Delayed INT | 1 |
|   Die CL Delay | 1 |
|   Punch Ready | 1 |
|   Reader Ready | 1 |
|   1400 Unit Exception Gate | 1 |
|   RDR Brush Impulses | 1 |
|   RDR CL LAT Not NPRO | 1 |
|   PCH CL LAT Not NPRO | 1 |
|   Gate RD Complete 2540 | 1 |
|   4 Bit MOD Pull On | 1 |
|   PFR Unit Exception Gate | 1 |

Interface From 2540

RD1 Row-Bit - Row-bit data from the first read station.  The particu-
lar bit on this line corresponds to the address currently being de-
coded with Read Cycle up.  Each bit comes up and is dropped at 000
time.

RD2 Row-Bit - Row-bit data from the second read station.  The partic-
ular bit on this line corresponds to the address currently being de-
coded with Read Cycle up.  Each bit comes up and is dropped at 000.
time.  Data transfer from first and second read stations occurs sim-
ultaneously.

PCH CHK Row-Bit - Row-bit data from the punch check reading brushes. The particular bit on this line corresponds to the address currently being decoded with Punch Cycle up. Bit timing is from 000 to 000.

PFR RD Row-Bit - Row-bit data from the Punch Feed Read station. The particular bit on this line corresponds to the address currently being decoded with Punch Cycle up. Bit timing is from 000 to 000. This line only used if PFR feature installed.

Punch Scan - This line transmits a series of twelve pulses with each pulse corresponding to a row in the card. Pulse duration is from .4 to 1 ms. The first Punch Scan pulse requests a punch service cycle and data to be punched in the first row of the card should be returned. No data from the PFR or punch check station is transferred during the first scan cycle. During the second through the twelfth scan cycles, data to be punched is received simultaneously with the transfer of data from the PFR and Punch Check row-bit storage.

After 9 Emitter - Indicates that an additional punch service cycle must be taken to transfer the last row of data from the PFR and Punch Check row-bit storage. No data should be sent for punch output.

PCH Clutch Set - This line transmits a continuous series of pulses when the punch motor is running. Each pulse occurs at 50 ms time intervals and has a duration of approximately 1 ms. The coincidence of this pulse and Punch Feed causes the punch clutch to pick and a card to be fed.

Unit Exception - Indicates that the reader has read and stacked the last card and End of File is on. This line is active at $12^{O}$ of the last card cycle and remains up until Unit Exception is received on an incoming line or until Reader Ready drops which will occur when RDR Feed Command is dropped.

PCH Brush Impulse - Series of twelve pulses per card with each pulse corresponding to a row of the card. Duration of each pulse is .4 to 1 ms. Each PCH Brush Impulse occurs approximately 6 ms after the rise of the corresponding Punch Scan pulse.

PCH Brush CL Delayed Int - Comes up at $285^{O}$ as the last card is passing under the punch check brushes.

DIE CL Delay - Comes up at $285^{O}$ of the second run in cycle and goes down at $285^{O}$ as the last card passes under the punch unit.

Punch Ready - Indicates that the punch is ready to accept a command. Comes on when run in is complete and turns off if PCH Write is down and an intervention required condition is detected.

Reader Ready - Indicates that the reader is ready to accept a command. Comes on when run in is complete and turns off is RDR Feed Command is down and an intervention required condition is detected.

1400 Unit Exception Gate - Indicates that the last card has been read under 1400 Mode. Comes up with End of File on at $12^{o}$ as the last card is passing under the first read brushes.

RDR Brush Impulses - Series of twelve pulses which corresponds to rows of the card being read. A reader service cycle should be taken not earlier than 150 usecs from the fall of RDR Brush Impulse. Duration of this pulse is .4 to 1 ms.

RDR CL LAT Not NPRO - Comes up between $248^{o}$ and $255^{o}$ if Read Feed is up. Goes down at $342^{o}$. Not active during NPRO.

PCH CL LAT Not NPRO - Comes up at PCH Clutch Set time ($292^{o}$) if Punch Feed is up and goes down at $347^{o}$. Not active during NPRO.

Gate RD Complete 2540 - Indicates that the read was completed successfully or that a Feed Stop was not detected during the read operation. If this line drops before the last read service cycle is completed for the card being read, the 2540 has detected a feeding error.

4 Bit MOD Pull On - Indicates that a two card run in cycle is to be taken by the punch feed and that if appropriate, service cycles must be taken to transfer data from the PFR station during run in.

Per Unit Exception Gate - Indicates that the last card has been read from the PFR station if punch End of File is on. Comes up at $347^{o}$ as the last card begins to pass under the Punch Unit. Goes down when the next clutch cycle is taken.


9020D SYSTEM, EXTERNAL INTERFACE LINES

Refer to Chapter 6, Peripheral Adapter Module for information about the 9020D System's external interface lines. Chapter 9 contains information about the 9020D Systems Console to the SMMC interface.

PART 2.  9020E SYSTEM

Part 2 describes the following interfaces between elements of the IBM 9020E System:

| | |
|---|---|
| CE - CE | TCU - Configuration Console |
| CE/IOCE - SE | CE - TCU |
| Configuration Console-SE | CE - DE |
| CE - IOCE | DE - Configuration Console |
| IOCE - Configuration Console | 2701 - IOCE |
| CE - Configuration Console | CC - 2701 |
| TCU - TU | 2821 ICU - Printer |

2821 ICU - Card Reader/Punch

In the accompanying tables the signal lines are shown between the pair of components as defined as the individual interfaces.

All interface lines from the IOCE to control units are described in Appendix D. Appendix D also contains information applicable to the Input/Output Interface and the Channel to Device Control Unit.

The system diagram Figure 13-3 shows the interface lines in diagram form.

CE to CE INTERFACE

Refer to 9020D System discussion.

CE/IOCE to SE INTERFACE

Refer to 9020D System discussion.

CONFIGURATION CONSOLE to SE INTERFACE

Similar to 9020D System discussion of System Console - SE Interface.

CE to IOCE INTERFACE

Refer to 9020D System discussion.

IOCE to CONFIGURATION CONSOLE INTERFACE

Simliar to 9020D System discussion of IOCE - System Console Interface.

CE to CONFIGURATION CONSOLE INTERFACE

This interface is divided into two sections.

1. Switch and indicator lines for control of the CE from the CC. This interface contains the same lines as the 9020D CE to SC interface except for the addition of the following line.

   Subsystem Load - This line allows a subsystem IPL to be initiated from the CC.

   Refer to CE to System Console Interface description for other lines.

2. Configuration control interface for the reconfiguration control units in the Configuration Console. This interface performs two functions: (1) it allows the RCU to

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Figure 13-3. 9020E System Diagram, Interface Lines

receive configuration information from the CE; and (2)
allows the RCU to present an interruption signal to the
CE upon detection of certain malfunctions.  Interface
lines are listed in Table 13-17.

Table 13-17.  CE to Configuration Console Interface

| Name of Line | Number of Lines |
|---|---|
| CE to CC | |
|     Configuration Data Bus | 11 |
|     Reconfiguration Select-Response | 2 |
|     System Reset | 2 |
| CC to CE | |
|     Element Check | 2 |

Configuration Data Bus - An eleven bit bus carries the configuration
mask of the Configuration Control Register (CCR) to the CC during
execution of the SCON instruction by the CE.

Reconfiguration Select-Response - A line provided to signal the CC to
accept the information on the Configuration Data bus.  It is effective
at the RCU (CC) if the CE issuing the Reconfigure Select has its SCON
bit set in the CCR of the RCU and the RCU is not in State 0 with the
test switch on.

System Reset - The RCU will reset provided a signal is simultaneously
received on the two reset lines.

Element Check - This line is used to set a bit in the Diagnose
Accessible Register (DAR) in the CE when one or more of the following
conditions exist at the RCU.

    1.    Power Check

    2.    Power Off

    3.    Parity Check in the CCR

    4.    Out of Tolerance Check (OTC)

An interruption is taken by the CE provided the associated RCU bit is
not masked off in the DAR Mask and bit 7 of the PSW is not masked off.

TCU TO CONFIGURATION CONSOLE INTERFACE

Similar to 9020D System discussion of TCU - System Console Inter-
face.

CE TO TCU INTERFACE

Refer to 9020D System discussion.

CE TO DE INTERFACE

The CE-DE Interface has several purposes:

    1.  Allows the DE to act as a storage device.

    2.  Simulates the request capability of 24CVG's to check priority circuits of the DE.

    3.  Allows wrapping back of display data to the CE to validity check the data transferred between the CE and displays.

The CE-DE Interface consists of 250 lines. 140 lines carry signals from the CE to DE and 110 lines carry signals from the DE to CE. The interface lines between the CE-DE are listed in Table 13-18.

Interface to DE

Storage Data Bus In (SDBI)-  These lines supply data from the CE to DE on Store operations.  During execution of Set Configuration (SCON) instruction, 27 data bits plus 4 parity bits are transferred to the DE via this bus.

Storage Address Bus (SAB)-  Consists of Box, Tag, and Address lines from the CE to DE.

NOTE:  Bits 00, 21, 22, 23 not used by CE.

Marks-  Store or regeneration control line for each byte of the 72-bit storage doubleword accessing by the CE.

In Keys-  Five key bits from the CE that are compared to the key bits stored in the storage protection buffer.  The sixth bit is an odd parity.

CVG Request-  The CE has the capability of forcing the request lines to remain active via the Diagnose instruction.  Once forced active by a CE, the lines remain active until the CE resets them.

DG Selected-  These lines select one of eight DG/DE interfaces. The signal is used in conjunction with the Wrap and Set Force Request.  These signals are under Diagnose control.

Logout Word Number-  These signals gate the logout words to SDBO and are under CE Control.  They shall exist in the all-zero's state when not in use.

System Reset (1, 2)-  These signals cause a storage reset at System Reset time.  The signals must go (-) on Line 1 and (+) on Line 2 simultaneously to generate a reset.  They are not gated by CCR bits.

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The CCR is reset to all zeros except parity and SCON bits which are all set ON.

NOTE: All static (DC) levels except Line 1 (+) and Line 2 (-) are considered erroneous and no action is taken.

Store- Control line from CE to DE to permit a data store.

Normal Op- Signal CE generated to assure that control bus driver or receiver failures do not cause multiple instruction execution resulting in data loss. This signal is valid with Fetch and Store Ops only. If sensed with Test and Set, Set key, or Insert key, Storage Address Check will be set and entire DE will stop; ELC will be sent to CE's with wait timeout set. If not sensed with Fetch or Store, Storage Check, ELC, and wait timeout will also be initiated.

Set Key- Signal from the CE that will inform the DE device to perform a Set Key cycle.

Insert Key- Signal from the CE that will inform the DE device to perform an Insert Key cycle.

Test and Set- Control line to perform a Test and Set cycle in the DE.

Address Compare Sync - Negative significant - provides a scope point for syncing purposes when the setting of the Address switches control panel matches the SAB, and the Address Compare switch is in the normal position. Hard wired from CE with no logic involved.

CE Power On- A ground significant level when power is down in the CE. This line will fall prior to CE power going off and remain there until after CE power-on reset. It will inhibit the output of the communication bit in the CCR of the SE.

Logout Select- Signal from CE requesting doubleword of logout.

Select (Even/Odd)- Signal from the CE to DE to request a storage cycle.

Logout Stop- Signal from CE which sets the DE logout stop latch, causes DE to halt all activity at the end of cycle in progress (if not already stopped).

Logout Complete- Resets DE following a logout. This signal is sensed as a check reset. DE Stopped is reset at completion of Reset Sequence.

Reconfigure Select- This signal causes the DE to gate contents of SDBI to the Configuration Control Register (CCR). This signal is gated by SCON bit unless CCR Parity error exists or SCON is all zeroes in states 1,2 or 3, in which case SCON bits are ignored.

Table 13-18.  CE to DE Interface

| Line Name | Number of Lines |
|---|---|
| To DE | |
|     Storage Data Bus In (SDBI) | 72 |
|     Storage Address Bus (SAB) | 22 |
|     Marks | 9 |
|     In Keys | 6 |
|     CVG Request | 6* |
|     DG Selected | 4* |
|     Logout Word Number | 4 |
|     System Reset (1, 2) | 2 |
|     Store | 1 |
|     Normal Op | 1 |
|     Set Key | 1 |
|     Insert Key | 1 |
|     Test and Set | 1 |
|     Address Compare Sync | 1 |
|     CE Power On | 1 |
|     Logout Select | 1* |
|     Select (Even/Odd) | 2* |
|     Logout Stop | 1* |
|     Logout Complete | 1* |
|     Reconfigure Select | 1* |
|     Wrap | 1* |

Table 13-18.  CE to DE Interface (cont.)

| Line Name | Number of Lines |
|---|---|
| Set Force Request | 1* |
| From DE | |
| Storage Data Bus Out (SDBO) | 72 |
| Wrap Bus | 19 |
| Out Keys | 6 |
| SBO Gate | 1* |
| Storage Data Check | 1 |
| Storage Address Check | 1 |
| Advance SDBO | 1 |
| Protect Address Check | 1 |
| Advance Keys | 1 |
| Accept | 1* |
| Logout Advance | 1* |
| Element Check | 1* |
| Reconfigure Accept | 1* |
| DE Stopped | 1* |
| DE Ready | 1* |
| Wrap Bus Busy | 1* |

*    Simplex Lines

Wrap- Signal used with the DG Select signals to gate one of the eight DG/DE interfaces to the wrap bus.  This signal is under Diagnose control.

Set Force Request - Establishes priority and data flow conditions to make subsequent wrap tests more meaningful.

Interface from DE

Storage Data Bus Out (SDBO) - Data from the DE to the CE during either a fetch or a Logout operation.

Wrap Bus - Used to send data fetched from the DE to the CE via the DG buffers within the DE. This path is also used to check the DG/DE interfaces and DE control logic without the use of a DG.

Out Keys - Five key bits plus parity from DE to the CE on an Insert Storage Key cycle.

SBO Gate - Identification tag used by the CE to identify the DE during a fetch data cycle.

Storage Data Check - Indicates a storage data parity error to the CE; also causes a pulsed ELC.

Storage Address Check - Indicates mark parity, address parity, box tag parity, box tag mismatch, multi-accept and invalid Op errors. Causes a pulsed ELC to be sent to all CE's.

Advanced SDBO - Sent from DE to the user in advance of data out. It will be sent for all storage cycles.

Protect Address Check - Signal from the DE to the CE that occurs when there is a key mismatch when attempting to store or fetch a protected location, and neither tag is zero.

Advance Keys - Signal from the DE on Insert Key cycle to alert CE that out keys are on the bus.

Accept - Indicates to CE that DE has been started in response to its request (select).

Logout Advance - Signal to CE that logout data is being placed on SDBO.

Element Check - To alert all CE's (regardless of configuration) that the DE has an error condition as follows:

Pulsed ELC's are coincident with:

    1.  Configuration Control Register (CCR) parity.

    2.  Temperature marginal or catastrophic.

    3.  On Battery signal.

    4.  Address check or data check condition related to a CE access.

    5.  DE Check condition related to a DG access.

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Static ELC's are coincident with:

1. Power off (normal, element master, or loss).

Reconfigure Accept - Indicates to the CE that the Configuration Control Register has loaded the data from SDBI and correct parity exists. The signal is sent to the CE that generated the configuration data.

DE Stopped - Indicates to the system that DE is logout stopped. Inhibits all operations except logout and reconfiguration (CE functions only).

DE Ready - Informs user that DE is available for use; that is, power is on, not in test, and not configured away from the particular user.

Wrap Bus Busy - Brought up by the DE when a diagnose wrap is accepted. This signal is sent to other CE's to prohibit the sending of Wrap requests to that DE. This signal remains active for the duration of the diagnose.

DE TO CC INTERFACE

Primary function of the DE-CC interface is to transmit DE state (status) and logic check indications to the CC. The interface lines between the DE and CC are listed in Table 13-19.

Table 13-19.  DE to CC Interface

| Line Name | Number of Lines |
|-----------|-----------------|
| DE to CC | |
|   State 3 | 1 |
|   State 2 | 1 |
|   State 1 | 1 |
|   State 0 | 1 |
|   Logic Check | 1 |
|   Power Check | 1 |
|   Emergency Power Off | 3 |

State Three - A line indicating that the state bits of the DE Configuration Register are both ones.

State Two - A line indicating that the state bits are:  $S_0=1$, $S_1=0$ in the DE configuration register.

State One - A line indicating that the state bits are:  $S_0=0$, $S_1=1$ in the DE configuration register.

State Zero - A line indicating that both state bits are zero in the DE configuration register.

Logic Check - A line indicating that a data check, address check key check, or DG related check, has occurred in the DE.

Power Check - A line to the console indicating that the temperature in the DE has drifted to within 10 degrees of the shutdown tolerance. The line also indicates the loss of a voltage or normal power off.

Emergency Power Off (EPO) - Three lines between the DE and the CC activate EPO circuits:

1. A +24vdc line from the DE power supply to the CC.

2. 0 volts (24v return from the CC).

3. The EPO control line from the CC to the DE EPO contactor.

2701 TO IOCE INTERFACE

The 2701-IOCE Interface is a standard IBM System/360 channel-control unit interface. Refer to Appendix D for information describing IOCE to control unit interface lines.

CC TO 2701 INTERFACE

The CC to 2701 Interface performs two functions: (1) Provides a Configuration Control Interface for the 2701 and; (2) Indicates Fault information and controls EPO. Interface lines are shown in Table 13-20.

Enable Interface A or B - These two lines are used to transmit configuration information to the 2701.

Reset - This line is used to reset the 2701.

S0, S1 - Two lines which determine which state the DAU will enter.

Configuration Strobe - This line transmits a pulse to the 2701 when data is valid on the Enable Interface and the S0 and S1 lines.

Indicate State 0, 1, 2, 3 - Four lines which light four state indicators on the CC (only one line will be active at any time).

Logic Check - This line indicates a logic check occurred in the 2701.

Power Check - This line is active whenever a power check occurs in the 2701.

Ready - This line is active when the DAU is program configurable via the CC.

Interfaces A or B Enabled - These lines return the 2701 configuration connections to the CC.

Table 13-20.  CC to 2701 Interface

| Name of Line | Number of Lines |
|---|---|
| CC - 2701 | |
|     Enable Interface A | 1 |
|     Enable Interface B | 1 |
|     Reset | 1 |
|     S0 | 1 |
|     S1 | 1 |
|     Configuration Strobe | 1 |
| 2701 - CC | |
|     Indicate State 0 | 1 |
|     Indicate State 1 | 1 |
|     Indicate State 2 | 1 |
|     Indicate State 3 | 1 |
|     Indicate Logic Check | 1 |
|     Indicate Power Check | 1 |
|     Ready | 1 |
|     Interface A Enabled | 1 |
|     Interface B Enabled | 1 |
|     Configuration Accept | 1 |
|     Emergency Power Off | 3 |

Configuration Accepted - This line transmits a signal from the 2701 to the CC indicating configuration data was received.

Emergency Power Off - Three lines between the 2701 and CC actuate the EPO circuits.

1. A +24v DC line from the 2701 power supply to the CC.

2. 0 Volts (24 v return from the console).

3. The EPO control line from the console to the 2701 EPO connector.

TCU - TAPE UNIT INTERFACE

Refer to 9020D System discussion.


PRINTER - CONTROL UNIT (ICU) INTERFACE

Refer to 9020D System discussion.


CARD READER/PUNCH - CONTROL UNIT (ICU) INTERFACE

Refer to 9020D System discussion.

9020E SYSTEM EXTERNAL INTERFACE LINES

Refer to Chapter 7, Data Adapter Unit, for information about the
DAU/RKM interface lines.  Refer to Chapter 4, Display Element for
information about the DE/DG interface lines.  Refer to Chapter 10
for information about the CC/RKM, CC/RKM/R Console and CC/DG inter-
face lines.

CCC to 9020E Interface

Channel-to-Channel (CTC) adapters are installed on selector channels.
The interface from the 9020E System to the CTC adapter is the same
as any control unit.  Description of this interface is discussed in
Appendix D of this document.

TECHNOLOGIES

Standard Modular System Packaging

The Standard Modular System (SMS) provides a moderate number of
standard building blocks to facilitate the manufacturing of solid-
state data processing equipment.  The units in the 9020 System
which use this type of logic are the 2401, Magnetic Tape Unit, the
2821 Control Unit, the 2540 Card Read Punch, and the 1403 Printer.

    Modular type units and pluggable printed circuit cards provide
for flexible packaging of all electronic components required in a
system.  Some of the more important advantages offered by the use
of SMS packaging are:

    1.  Standardization of circuits and packaging methods, reduce
        parts stockage in the field and parts handling in the
        manufacturing process.

    2.  Increased serviceability by allowing rapid access to cards
        and test points and elimination of the cover removal and
        storage problem.

    3.  Use of latest production techniques such as wire-wrapping
        and automated production lines.

    4.  Data processing equipment that requires a reduced amount
        of space, power, and air conditioning.

SMS Printed Wiring Cards

SMS cards facilitate the manufacturing process and permit standardi-
zation of circuits.  The pluggable printed circuit cards contain
all the components and printed wiring necessary for a particular
electronic function or functions.  A special program cap on some
SMS printed circuit cards gives additional flexibility to this
form of packaging and reduces the number of components cards
required for field servicing.  Other printed wiring cards are
used as cable connectors and back panel voltage distribution buses.

    The SMS single card (Figure 14-1) is made of an epoxy paper
laminate material and is 0.056 inch thick, 4-1/2 inches long, and
2-1/2 inches wide.  All of the electronic components and the program
cap, if used, are mounted on the front side of the standard SMS
card form.  Connections to the components and program cap are made
on the back of the SMS card form by printed wiring patterns that
terminate at contacts at the bottom of the card.  These contacts,
labeled A through R, couple the signal and standard service voltages
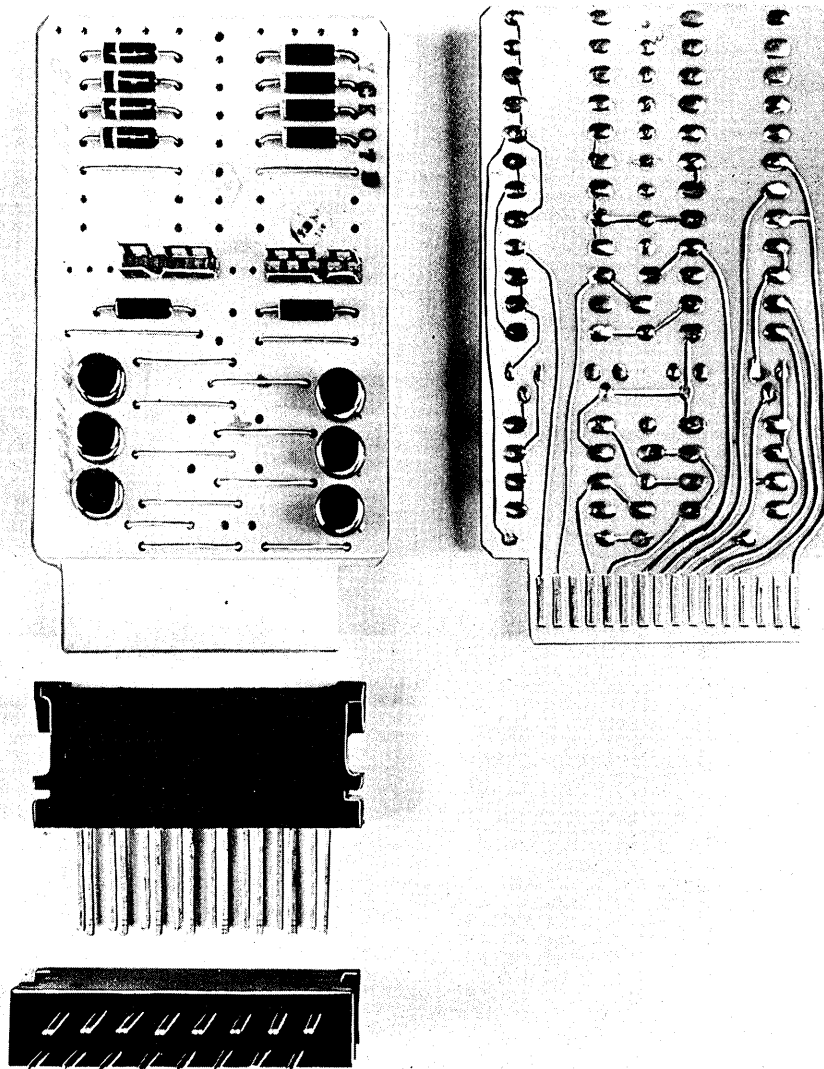
Figure 14-1.   SMS Printed Wiring Cards

to the circuit components when the card is inserted in the SMS soc-
ket.   The printed circuit wiring (land pattern) depends on the cir-
cuit configuration of the card.

The pluggable printed circuit cards are inserted into SMS re-
ceptacles as shown in Figure 14-1.   Although the contacts are all
in line on the card insertion side of the SMS receptacle, they pass

through the receptacle in a staggered arrangement as noted in the figure. This staggering allows additional room for wire-wrapping or soldering of signal and voltage wires to the terminal pins. Figure 14-2 shows an 8-position socket is also used in the SMS packages.

Solid-Logic Technology

Solid-Logic Technology (SLT) consists of a wide scope of coordinated technological developments to provide miniaturized basic building blocks and complete packaging techniques capable of reliable operation in extreme environment conditions. The 9020 Systems will contain one or more of the following elements or units using the Solid-Logic Technology: Computing Element, Storage Element, Display Element, I/O Control Element, Peripheral Adapter Module, Data Adapter Unit, Tape Control Unit, Storage Control Unit, System Console, and the Configuration Console.

Basic Building Blocks

The three basic SLT building blocks are modules, cards, and boards. Modules, which are the fundamental functional elements, are mounted on printed circuit cards in groups of 6, 12, 24, or 36. These cards, in turn, are plugged onto a printed circuit board.

Modules

Basically, SLT utilizes screened film linear components and silicon semiconductors integrated on a ceramic substrate. These assemblies, called modules, are the functional building blocks of an SLT system. A module (Figure 14-3), which is generally a complete logic circuit, is an integrated-component-package device developed through combined material, electrical, and thermal design knowledge.

Components

Semiconductors. Both diodes and transistors are silicon planar expitaxial devices fabricated on a silicon wafer with a diameter of approximately 1-1/4 inches. Silicon oxide protection is used between all diffusion steps and at the final step. Aluminum conductors are vacuum-deposited on the wafer to provide contact areas remote from the diffusion areas. The wafer is then hermetically sealed with two-high temperature borosilicate glass coatings. To provide contacts on the device, small metal balls are soldered to areas of the aluminum conductors previously exposed by etching of the glass coatings. The wafer is then cut into individual chips that are approximately 0.025 inch square.

Resistors. Resistors are fabricated by screening resistive pastes on the ceramic substrate (module), firing at temperatures of approximately 800 degrees C, and mechanically trimming to the desired value. The resulting resistors have good power-dissipation capability because of their bonding to the substrate and excellent stability because of the glazed structure.

14-3
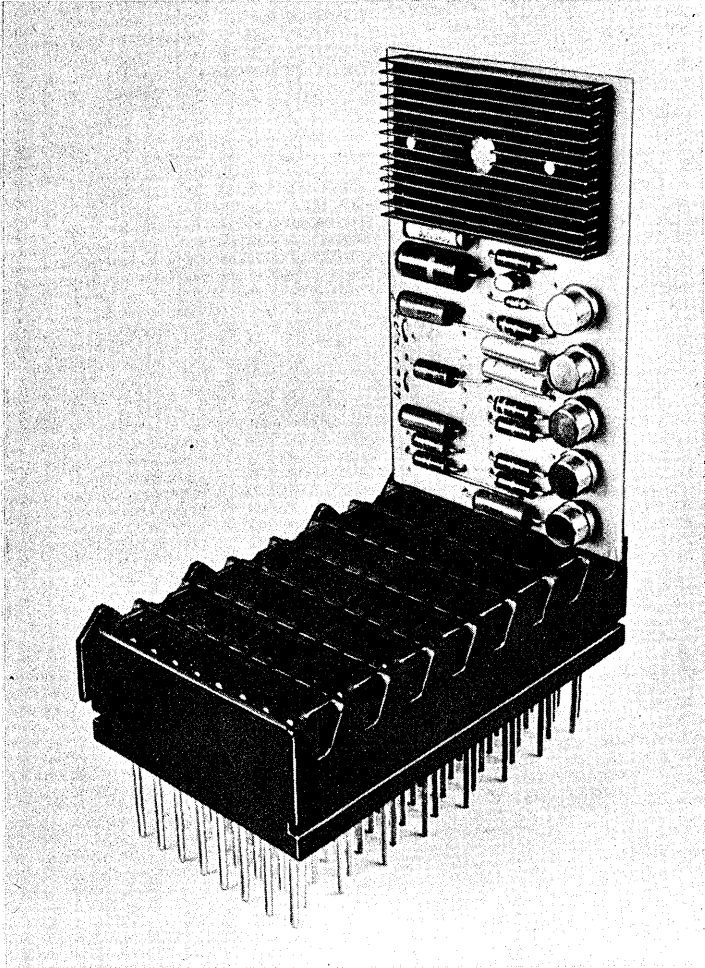
Figure 14-2.   SMS Single Card and Eight-Position Socket

Circuits

The basic circuits which will be used for the 9020 application are
diode-transistor (NAND) logic with an average operating times of
30 nanoseconds (medium speed) or 5-10 nanoseconds (high speed) per
decision.

    1.   The basic circuits require only three basic components:
        diodes, transistors, and resistors.   (Capacitors and
        inductors are used to meet special requirements.)

    2.   The circuits are designed to operate properly with all
        components at their end-of-life value in the direction
        most detrimental to operation.
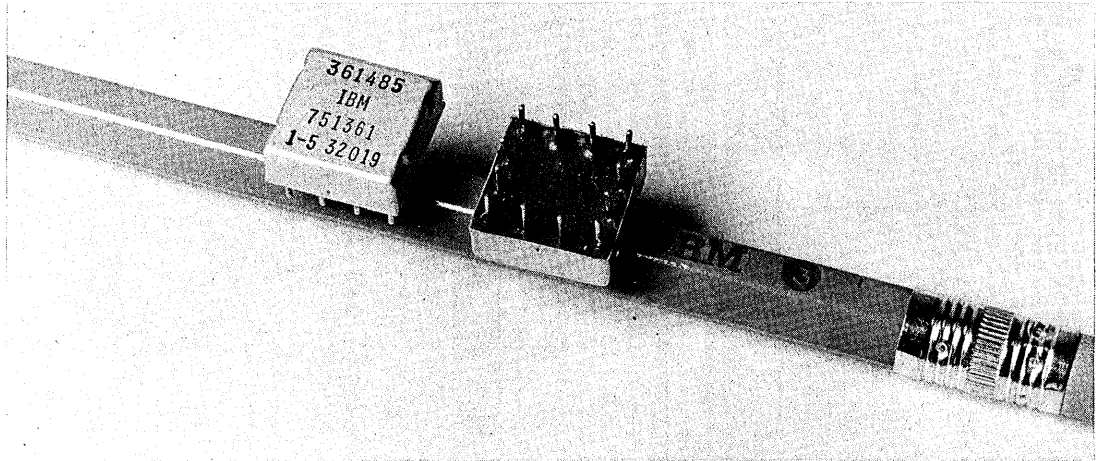
Figure 14-3. SLT Module

    3.   Three supply voltages (+6v, +3v, and -3v) are used to
        reduce the dependence of circuit speed on simiconductor
        characteristics and provide a very narrow range of delay
        variation from circuit to circuit.

    4.   Marginal checking is provided by varying the +6v supply.
        This causes the delay time of the circuit to vary, result-
        ing in logic failure in areas where timing has become
        critical.  It is IBM's experience that this approach to
        marginal checking provides the most meaningful method of
        detecting degraded circuit performance and, therefore,
        imminent system malfunctions.

A typical basic circuit, the AOI, is shown in Figure 14-4.

Cards

Modules are normally mounted on a glass epoxy printed circuit card
with conductors on both sides.  Five types of SLT cards are used
the 6-module card (6-Pac), the 12-module card (12-Pac), the 12-
module card (2-Hi 6-Pac), the 24-module card (2-Hi 12-Pac) and the
36-module card (2-Hi 36-Pac) (see Figure 14-5).  The card is pro-
vided with a connector having beryllium copper contacts and welded
gold contact points.  These contacts are spaced on 0.125 centers
giving 24 contacts on the 6-Pac and 48 on the 12-Pac.  The connector
is keyed to prevent insertion in the wrong orientation.  Additional
card sizes are planned to accommodate specific system requirements.

Boards

Printed circuit cards are, in turn, plugged onto a multilayer glass
epoxy printed circuit board.  This board has four conductor layers:
the outside two are used for signals; the inside two, for power
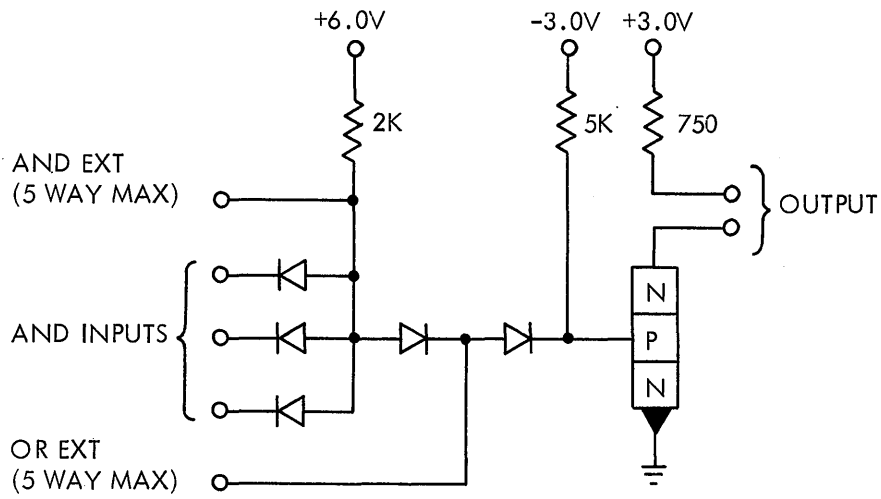
Figure 14-4. Typical SLT Circuit (And-Or Invert Block)
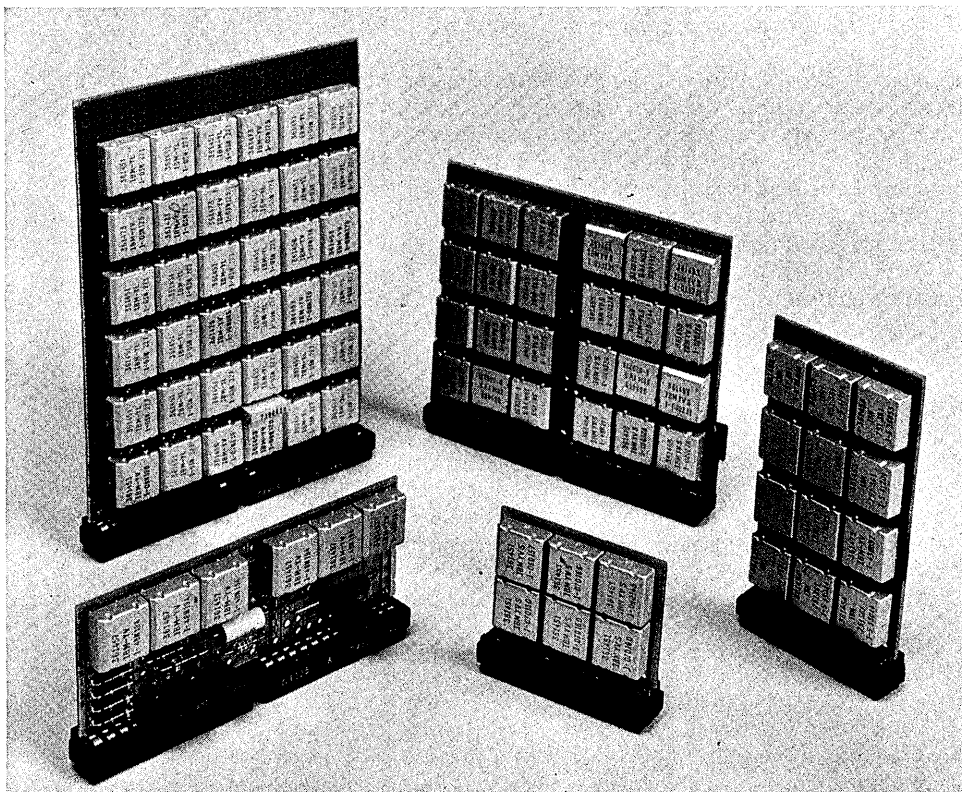


Figure 14-5. Five Types of SLT Cards

14-6

distribution and signal returns. Pins are soldered into plated-through holes on the board to provide contacts to mate to the card connector. Eighty-two 6-Pac positions are provided on the board which can be used to mount circuit cards or interboard cable connectors. Additional plated-through holes are provided for inter-connection between the conductor layers.

High wiring densities are achieved on the signal layers by using 0.010-inch-wide conductors with 0.010-inch space between them. Electrical noise, long line reflections, and excessive line-to-line coupling are avoided by utilizing the controlled-characteristic impedance of these conductors. This controlled impedance is obtained by spacing the signal lines over a virtual ground plane formed by ground and voltage distribution layers.

Gates

One or more boards may be mounted into one assembly referred to as a swinging gate. A maximum of 20 boards can be mounted on a large gate, with a maximum vertical buildup of four boards.

Frames

The outside dimensions of the main frames without covers are as follows: 70 inches high (including casters) 29.5 inches wide and do not exceed 60 inches in length. There are two sizes of power walls: 72 inches high (including casters), 24 inches wide and 60 inches long, the other type power wall is 72 inches high (including casters), 24 inches wide and 43 inches long. There are four casters and leveling pads for each main frame section. The power wall uses either the above or a dual type caster leveling pad assembly.

WEIGHTS

The average floor loading for each individual element and unit or the expected grouping of these units will not exceed 75 pounds per square foot.

To determine the floor loading per element or unit the weight is divided by the square feet of floor area occupied. This includes one half of the service clearance area in each direction, but not exceeding 30 inches from a machines surface.

Factors to be considered in determining the total floor loading are:

1. If more than three machines are placed side by side, no allowance can be taken for side clearance on the ends of the machine.

2. Twenty pounds for each square foot of service area used in calculation must be applied as live-load (personnel traffic) in floor loading computations.

3.  Ten pounds for each square foot of total area used in
    calculation must be applied as false floor load.

Floor loading is distributed by the use of 3.25 inch diameter level-
ing pads located on corners of each shipping section.  The center of
gravity is located as close to the geometric center of each frame
as possible to provide for even distribution of floor loading.

OUTLINE DRAWINGS

Plan view drawings of each of the 9020D or 9020E system components
are contained in Figures 14-6 through 14-21.  Swinging gates, panels
and doors are located and dimensioned along with the required service
clearances.  These clearances are minimum; thus, it is desirable to
increase these dimensions where convenient.  All dimensions are with
covers installed.

ELEMENT NUMBERING AND ORDER OF EXPANSION

The Computing, Storage and Display Elements are assigned numbers
which define the physical location and the (sequential) order of
expansion for each element.  The elements are numbered differently
in each system.  Figures 14-22 and 14-23 depict the numbering and
the order of expansion for 9020D and 9020E Systems, respectively.
Display Elements can expand independent of Storage Elements on a
9020E System.

     Because of cable limitations it is essential to physically
locate Storage Element #1 and #2 of a 9020D System as close as
practical.  In no case is the distance to exceed 24 feet.  The same
physical planning rule applies for Storage Element #1 and Display
Element #1 of a 9020E System.

     The I/O Control Element is a stand-alone unit and does not
require a special numbering scheme.

     The following describes symbols used on these drawings:

| | | | |
|---|---|---|---|
| ⊠ | Cable Entry and Exit | ─⊙─ | Service Area Boundary |
| ⊕ | Power Cord Exit (Power cord length is measured from this symbol) | + | Casters |
| ⊓ | Gate Swings | O | Leveling Pads or Glides |
| ─ ─ ─ | Optional Equipment | □ | Legs |
| ▬ᴛ CE | Customer Engineer Service Panel | ↕ | Non-Raised Floor Cable Exit |

14-8

7265-02 SYSTEM CONSOLE

PLAN VIEW
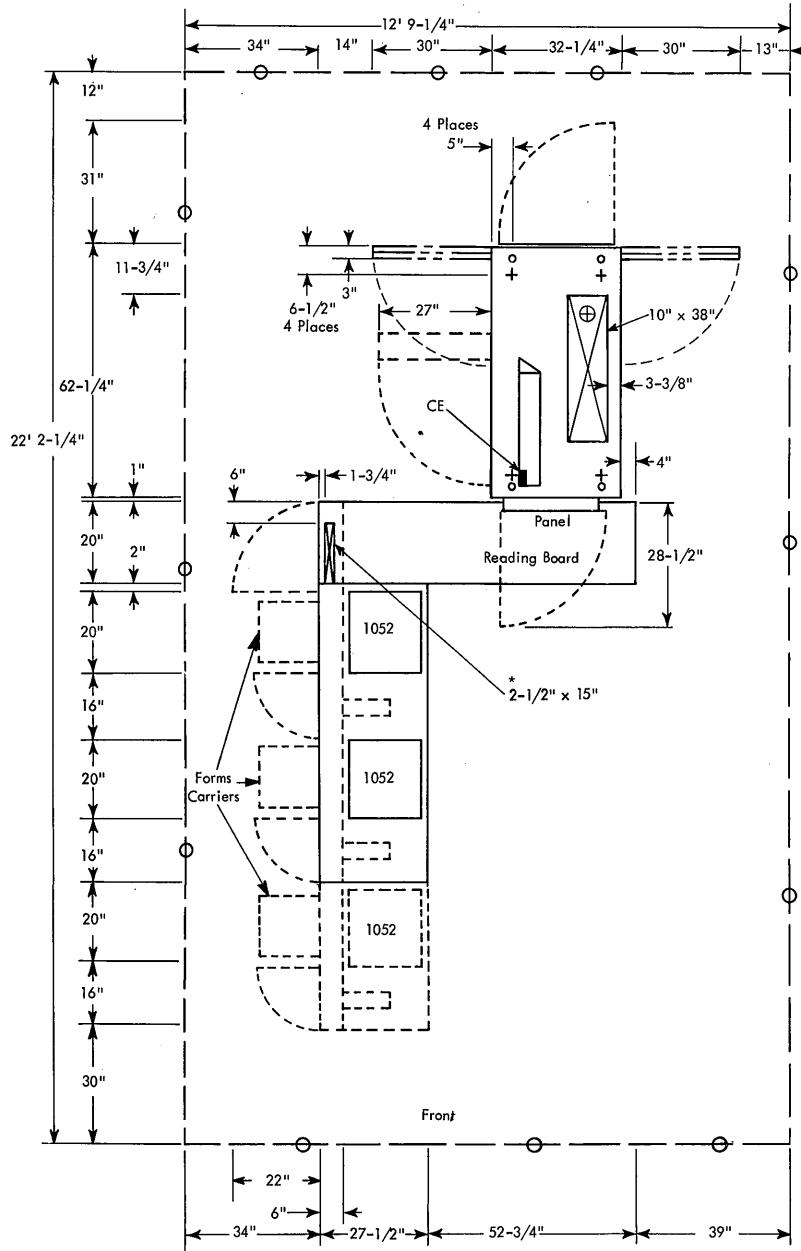


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| SEE PLAN VIEW. | | 70-3/4 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|---|---|
| 30 | 43 | 39 | 34 |

WEIGHT:  1,850 POUNDS

BTU/HR:  3,450

CFM:  350

POWER:  1.4 KVA

PHASES  3
PLUG  R AND S FS3760
CONNECTOR  R AND S FS3934
RECEPTACLE  R AND S FS3754

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|---|---|
| REL HUMIDITY | 20–80% |
| WET BULB | 78°F |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|---|---|
| REL HUMIDITY | 8–80% |
| WET BULB | 80°F |

CABLE LIMITATIONS

SEE SECTION ON CABLING.

NOTES:
*1052 CABLES

●Figure 14-6.  Plan View 7265-02 System Console

7265-03 CONFIGURATION CONSOLE

PLAN VIEW

61-1/2"

11-3/4"

28"    36"    11-1/2"

30"    4-1/2"    12" x 16"    6-1/2"    36"
(4 places)    (4 places)

12"    3"
(4 places)

25-1/2"

2"    CE

CE    CE

63-3/4"

****
6" x 12"    4-3/4"    3-1/4"
1-3/4"    (4 places)    (4 places)

21'-4"

6"

2"

Panel
21"    ***
2-1/2" x 15"    6-3/4"
Reading Board    (4 places)

22"    1052    8"

16"    Forms
Carriers

20"    1052

16"

30"    22"    6"    32-1/4"    4"

27-1/2"    Front

34"    80-1/4"

14' 5"
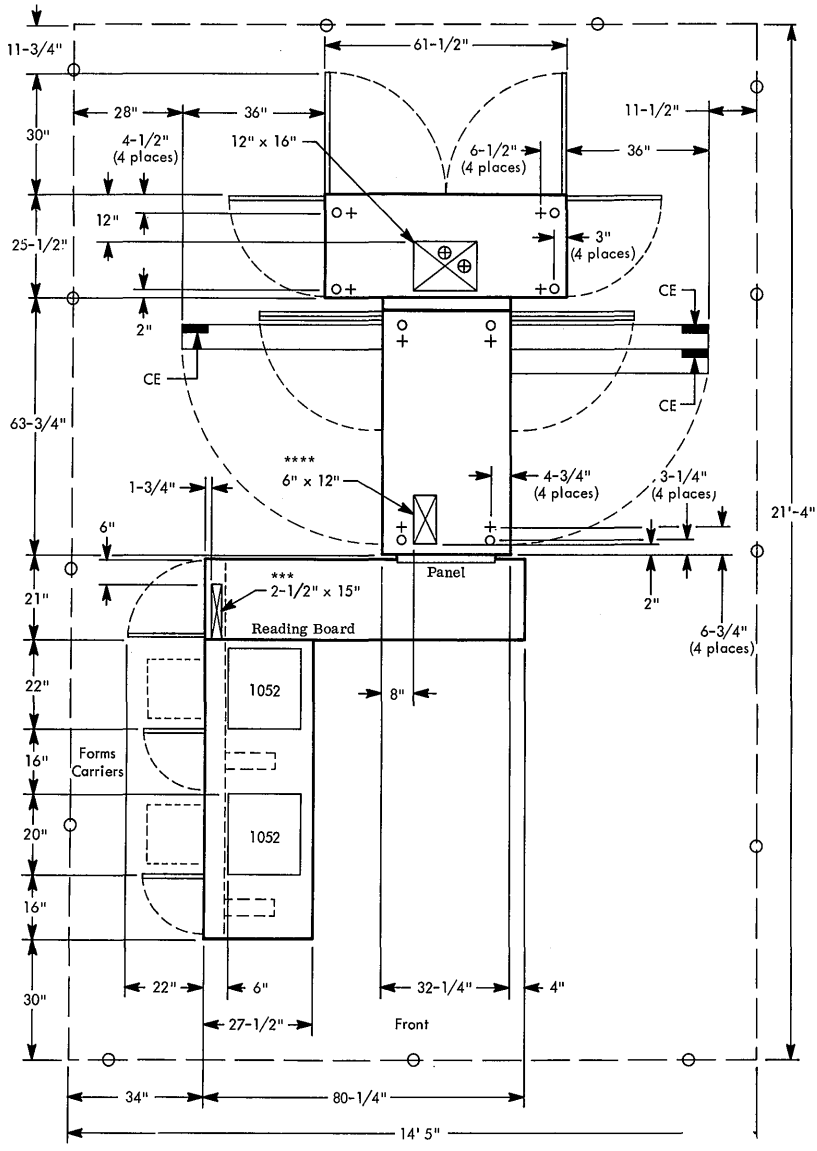
SPECIFICATIONS

DIMENSIONS (INCHES)

F    S    H
*    *    72-1/2

SERVICE CLEARANCE (INCHES)

F    R    RT    L
30    41-3/4    47-1/2    34

WEIGHT:  3,300 LBS

BTU/HR:  11,300

CFM:    1,750

**POWER    LINE 1    LINE 2
KVA    2.05 (AVE)    2.05 (AVE)

PHASES    1
PLUG    R AND S FS3750
(TWO)
CONNECTOR    R AND S FS3933
(TWO)
RECEPTACLE    R AND S FS3753
(TWO)

ENVIRONMENT OPERATING:

TEMPERATURE    60–90°F
REL HUMIDITY    20–80%
WET BULB    78°F

ENVIRONMENT NONOPERATING:

TEMPERATURE    50–110°F
REL HUMIDITY    8–80%
WET BULB    80°F

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTES:
*SEE PLAN VIEW.
**TWO SEPARATE POWER
SOURCES ARE REQUIRED
FOR THIS UNIT.  POWER
REQUIREMENTS WILL BE
EITHER 1.6 OR 2.5 KVA PER
LINE, DEPENDING UPON
POWER SOURCE SELECTED
FOR SC CONTROL PORTION
OF CC.
***1052 CABLES
****EPO CABLES

•Figure 14-7.   Plan View 7265-03 Configuration Console

7201-02 COMPUTING ELEMENT

PLAN VIEW
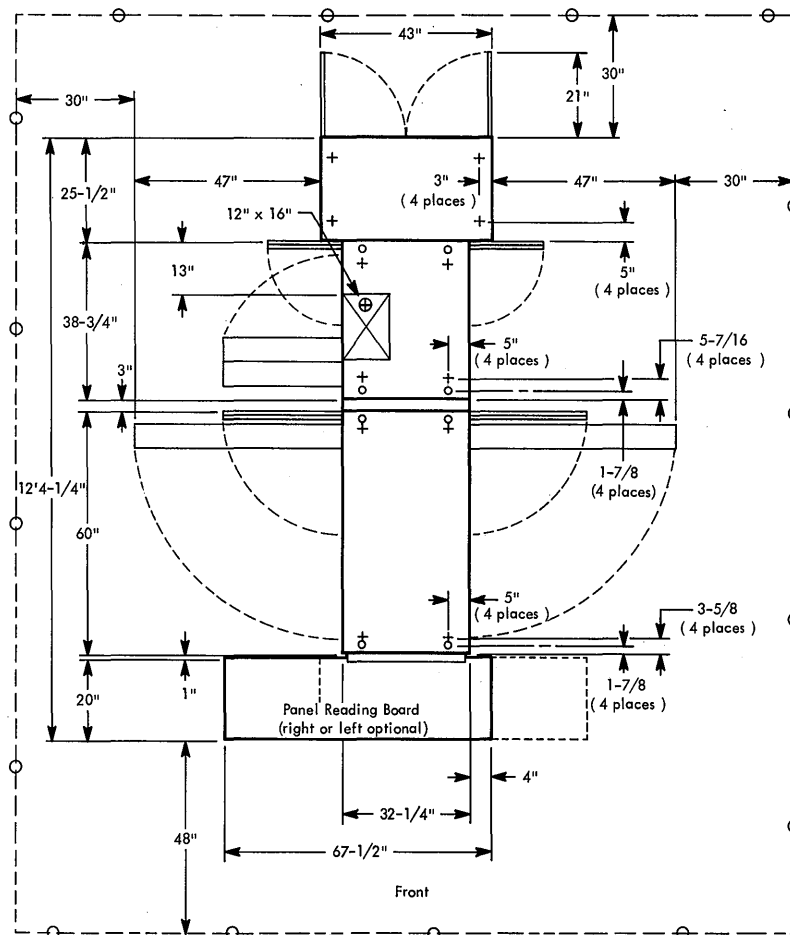


SPECIFICATIONS

DIMENSIONS

| F | S | H |
|---|---|---|
| * | * | 72-1/2 |

SERVICE CLEARANCES

| F | R | RT | L |
|---|---|----|---|
| 48 | 30 | * | * |

WEIGHT:  3,674 LBS.

BTU/HR: 19,600

CFM:     4,620

POWER:  6.0 KVA

PHASES        3
PLUG          R AND S, SC7328
CONNECTOR  R AND S, SC7428
RECEPTACLE  R AND S, SC7324

ENVIRONMENT OPERATING:

TEMPERATURE        $60^{\circ}-90^{\circ}F$
REL HUMIDITY        20–80%
MAX WET BULB       $78^{\circ}F$

ENVIRONMENT NONOPERATING:

TEMPERATURE        $50^{\circ}-110^{\circ}F$
REL HUMIDITY        8–80%
MAX WET BULB       $80^{\circ}F$

NOTES:
*SEE PLAN VIEW FOR DATA

•Figure 14-8.  Plan View 7201-02 Computing Element

CE BATTERY FRAME/MAIN WALL SPACER FRAME

PLAN VIEW
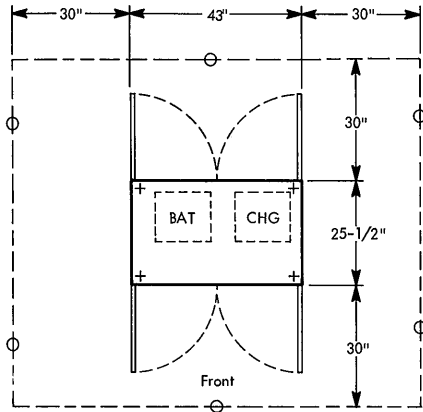


CE BATTERY FRAME

BATTERY BACK-UP FOR ONE OR TWO
CE'S CONTAINED IN THIS FRAME.

BATTERIES SERVICED FROM FRONT
SIDE OF FRAME.

REAR ACCESS REQUIRED FOR
INTER-FRAME CABLING.

PLAN VIEW
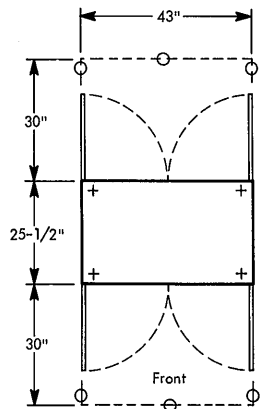


MAIN WALL SPACER FRAME

REQUIRED BETWEEN TWO SE'S OR DE'S
ON MAIN WALL WHEN NOT SEPARATED
BY A CE OR CE BATTERY FRAME.

FRONT AND REAR ACCESS REQUIRED
FOR INTER-FRAME CABLING.

●Figure 14-9. Plan View CE Battery Frame/Main Wall Spacer Frame

7251-09 STORAGE ELEMENT

PLAN VIEW
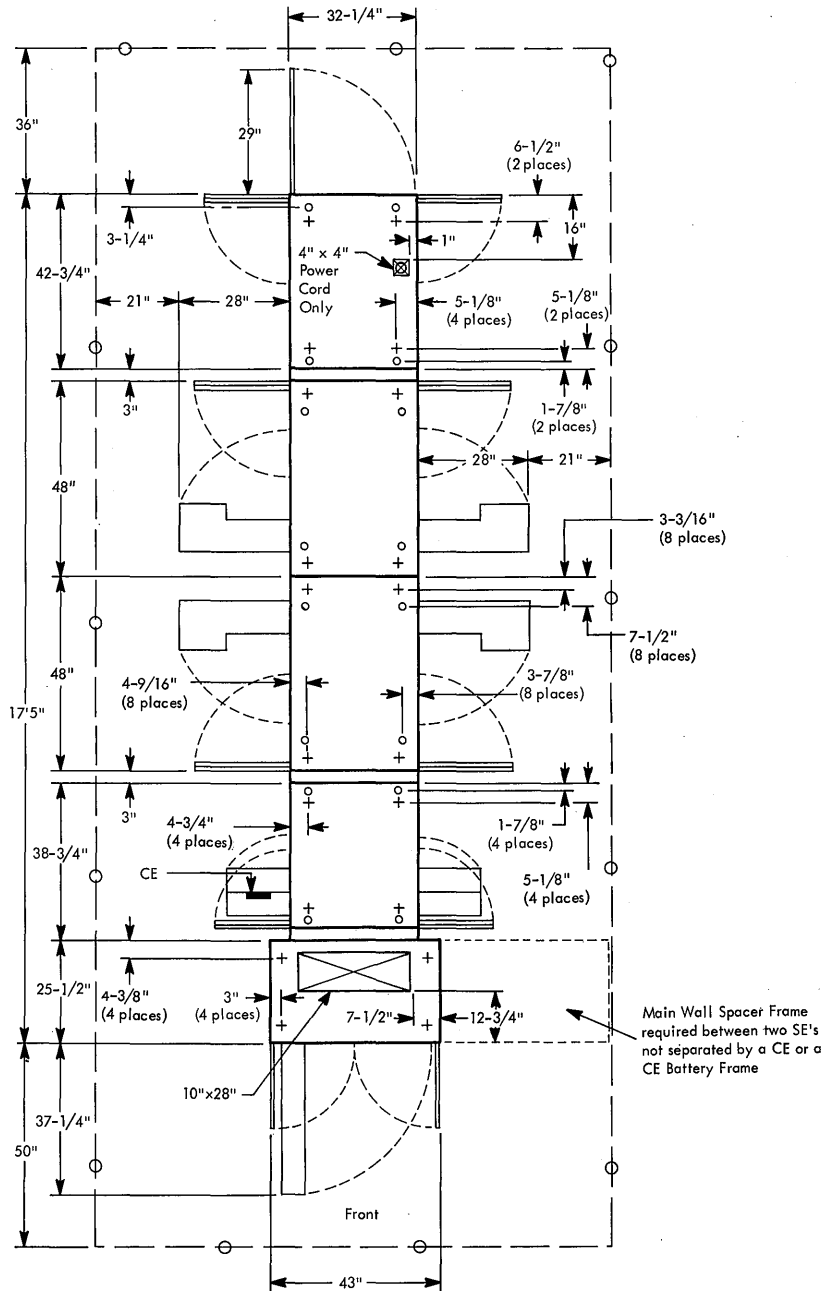
SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 43 | 209 | 72-1/2 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 50 | 36 | 49 | 49 |

WEIGHT: 4,620 LBS

BTU/HR: 21,170

CFM: 4,000

POWER: 6.7 KVA

PHASES 3
PLUG R AND S, SC7328
CONNECTOR R AND S, SC7428
RECEPTACLE R AND S, SC7324

ENVIRONMENT OPERATING:

TEMPERATURE 60–90°F
REL HUMIDITY 20–80%
WET BULB 78°F

ENVIRONMENT NONOPERATING:

TEMPERATURE 50–110°F
REL HUMIDITY 8–80%
WET BULB 80°F

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

32-1/4"
36"
29"
6-1/2" (2 places)
3-1/4"
42-3/4"
4" x 4" Power Cord Only
1"
16"
21"
28"
5-1/8" (4 places)
5-1/8" (2 places)
3"
1-7/8" (2 places)
48"
28"
21"
3-3/16" (8 places)
48"
4-9/16" (8 places)
3-7/8" (8 places)
7-1/2" (8 places)
17'5"
3"
4-3/4" (4 places)
1-7/8" (4 places)
CE
5-1/8" (4 places)
25-1/2"
4-3/8" (4 places)
3" (4 places)
7-1/2"
12-3/4"
Main Wall Spacer Frame required between two SE's not separated by a CE or a CE Battery Frame
10"x28"
37-1/4"
50"
Front
43"

●Figure 14-10.   Plan View 7251-09 Storage Element

7289-04 DISPLAY ELEMENT

PLAN VIEW
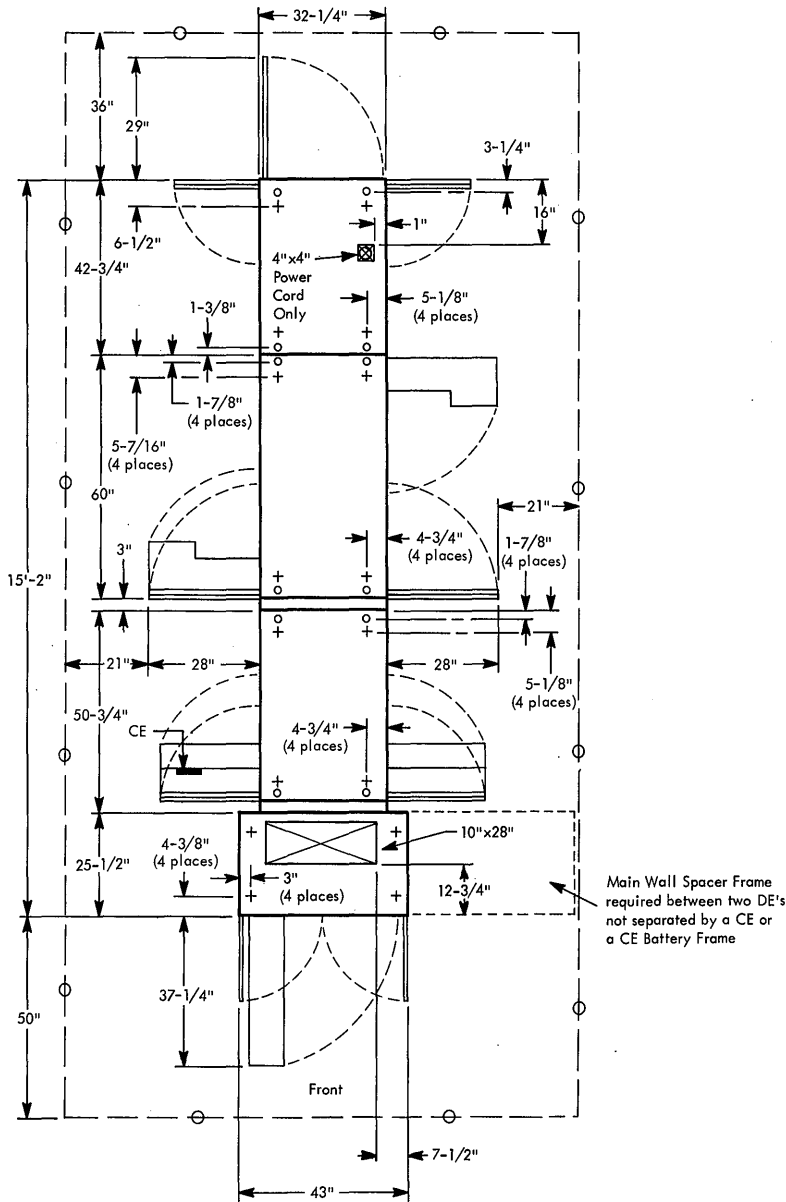


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 43 | 182 | 72-1/2 |

SERVICE CLEARANCE (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 50 | 36 | 49 | 49 |

WEIGHT: 3,500 LBS.

BTU/HR: 18,150

CFM: 3,300

POWER: 5.9 KVA

PHASES 3
PLUG R AND S, SC7328
CONNECTOR R AND S, SC7428
RECEPTACLE R AND S, SC7324

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|---|---|
| REL HUMIDITY | 20–80% |
| WET BULB | 78°F |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|---|---|
| REL HUMIDITY | 8–80% |
| WET BULB | 80°F |

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

•Figure 14-11.   Plan View 7289-04 Display Element

7231-02 I/O CONTROL ELEMENT

PLAN VIEW
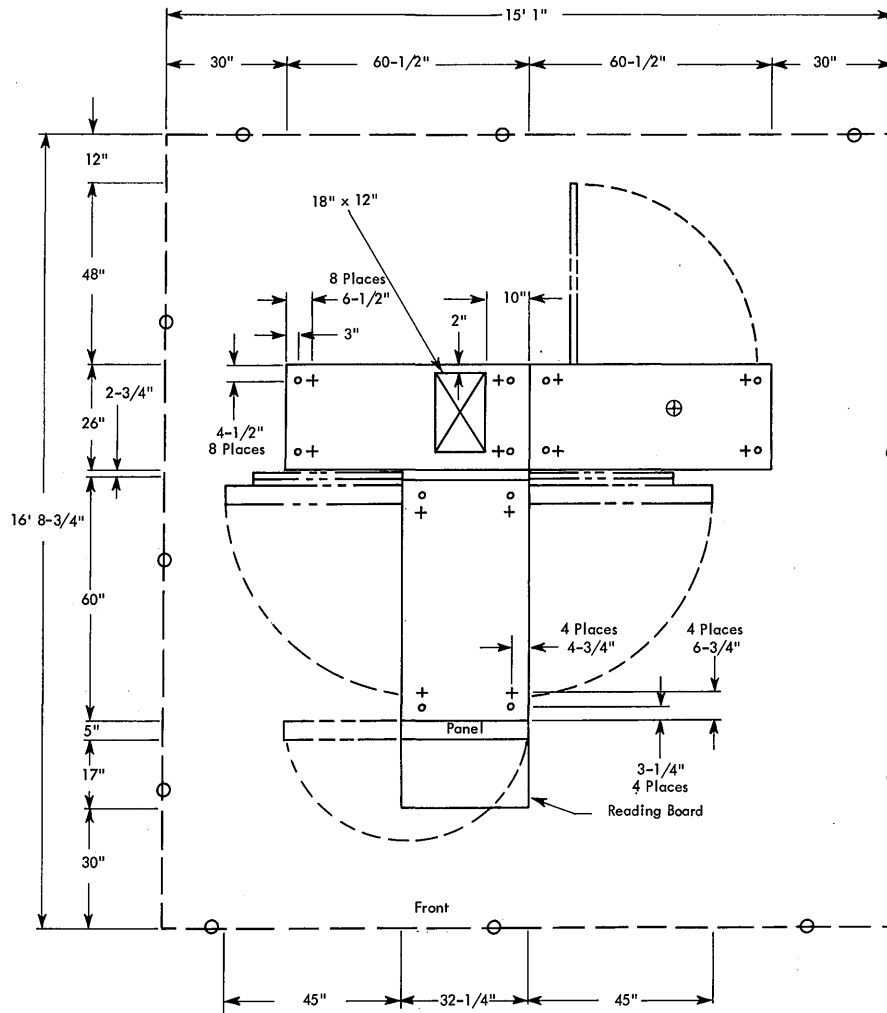


## SPECIFICATIONS

DIMENSIONS (INCHES)

|  | F | S | H |
|---|---|---|---|
| (1)* | 32-1/4 | 84-3/4 | 70 |
| (2)* | 121 | 26 | 72 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|---|---|
| 30 | 57 | 30** | 30** |

WEIGHT: 5,200 LBS

BTU/HR: 13,200

CFM: 2,550

POWER: 4.75 KVA

PHASES 3
PLUG R AND S, FS3760
CONNECTOR R AND S, FS3934
RECEPTACLE R AND S, FS3754

ENVIRONMENT OPERATING:

TEMPERATURE 60–90°F
REL HUMIDITY 20–80%
WET BULB 78°F

ENVIRONMENT NONOPERATING:

TEMPERATURE 50–110°F
REL HUMIDITY 8–80%
WET BULB 80°F

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTES:
*LINE 1 IS FOR MAIN FRAME
AND LINE 2 FOR POWER WALL.
**POWER WALLS CAN BE BUTTED
TO REDUCE FLOOR SPACE AND
CABLE LENGTH.

•Figure 14-12. Plan View 7231-02 I/O Control Element

7289-02 PERIPHERAL ADAPTER MODULE

PLAN VIEW
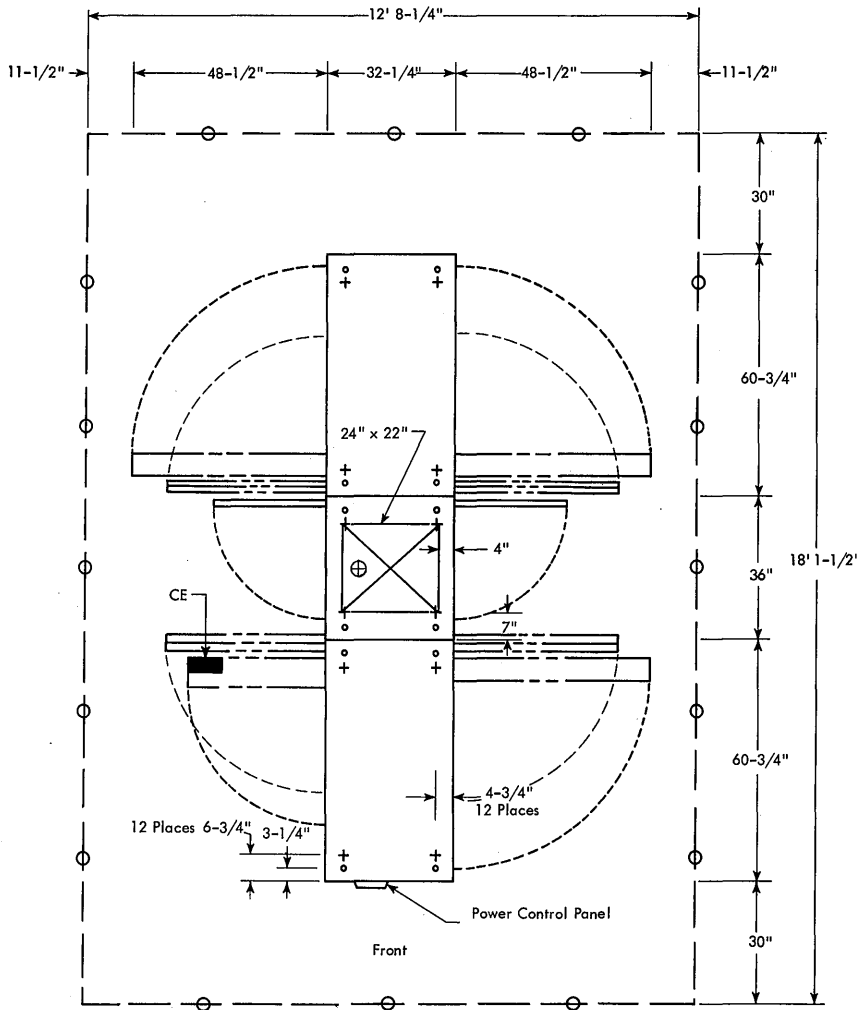


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 32-1/4 | 157-1/2 | 70 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 30 | 30 | 60 | 60 |

WEIGHT: 3,850 LBS

BTU/HR: 14,300*

CFM:     2,760*

POWER:   6 KVA*

PHASES       3
PLUG         R AND S, SC7328
CONNECTOR    R AND S, SC7428
RECEPTACLE   R AND S, SC7324

ENVIRONMENT OPERATING:

TEMPERATURE     60–90°F
REL HUMIDITY    20–80%
WET BULB        78°F

ENVIRONMENT NONOPERATING:

TEMPERATURE     50–110°F
REL HUMIDITY     8–80%
WET BULB        80°F

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTE:
*MAXIMUM VALUES GIVEN.
REQUIREMENTS VARY
ACCORDING TO THE QUANTITY
OF ADAPTERS CONTAINED IN
THE UNIT.

•Figure 14-13.  Plan View 7289-02 Peripheral Adapter Module

14–16

2830A-01 TAPE CONTROL*

PLAN VIEW
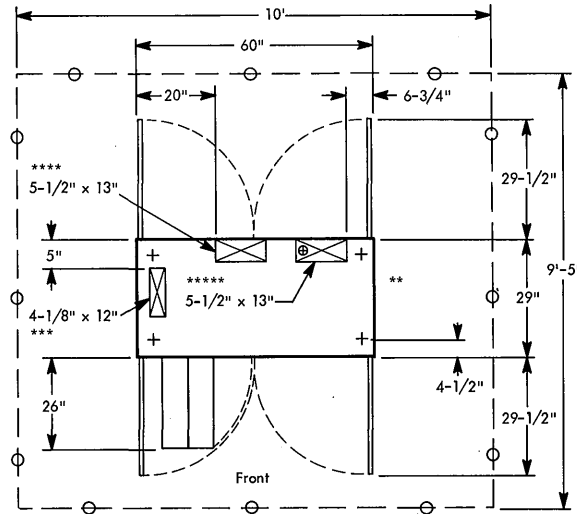


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 60 | 29 | 60 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 42 | 42 | 30** | 30 |

WEIGHT: 1,130 LBS

BTU/HR: 3,000

CFM: 500

POWER 1.2 KVA

PHASES 3
PLUG R AND S SC7328
CONNECTOR R AND S SC7428
RECEPTACLE R AND S SC7324

ENVIRONMENT OPERATING:

TEMPERATURE 60–90°F
REL HUMIDITY 20–80%
WET BULB 78°F

ENVIRONMENT NONOPERATING:

TEMPERATURE 50–110°F
REL HUMIDITY 8–80%
WET BULB 80°F

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTES:
*"A" IS A DESIGNATION TO
IDENTIFY SLT VERSION
(SERIAL NUMBERS FROM
11001 TO 13,999).
**CAN ABUT TAPE DRIVE THIS
SIDE ONLY.
***PRIMARY AND SECONDARY
INTERFACES; TAPE DRIVE
SIGNAL CABLES.
****INDICATOR AND SCON
CABLES.
*****EPO AND POWER CABLES.

●Figure 14-14.  Plan View 2803-01 Tape Control Unit

2401 MAGNETIC TAPE UNIT MODELS 2 AND 3

PLAN VIEW
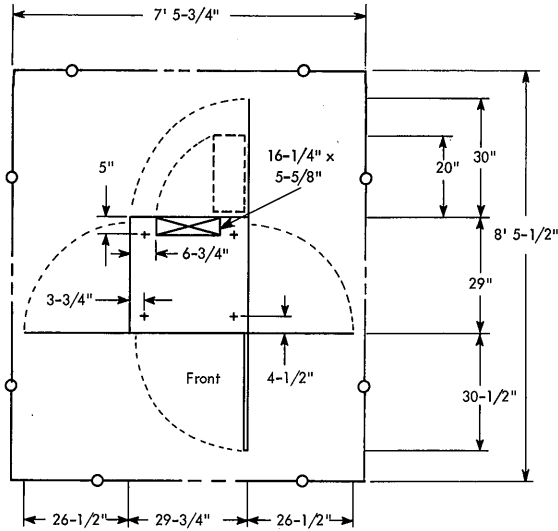


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 29-3/4 | 29 | 67 |

SERVICE CLEARANCE (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 36 | 36 | 30* | 30* |

WEIGHT: 800 POUNDS

BTU/HR: 3,500

CFM: 500

POWER 1.6 KVA**

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|---|---|
| REL HUMIDITY | 20–80% |
| WET BULB | 78°F |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|---|---|
| REL HUMIDITY | 8–80% |
| WET BULB | 80°F |

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTES:
*WHEN NOT ABUTTED TO
ANOTHER TAPE UNIT OR TAPE
CONTROL UNIT.
**POWERED FROM CONTROL
UNIT.

•Figure 14-15. Plan View of 2401 Magnetic Tape Units, Models 2 or 3

14-18

2821 CONTROL UNIT MODEL 1 AND 2

PLAN VIEW
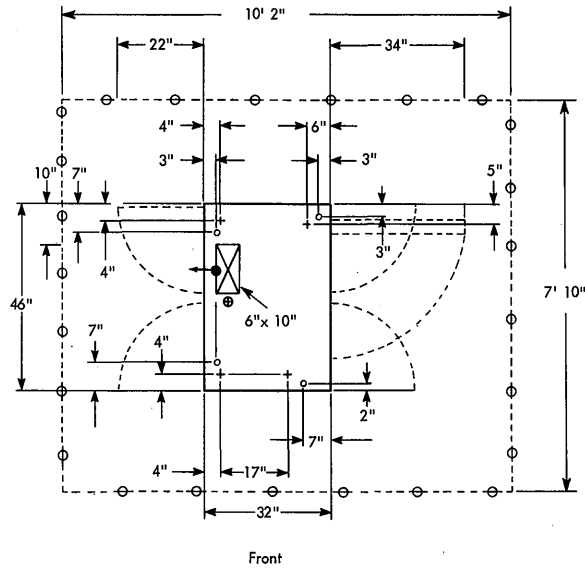


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 32 | 46 | 60 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 30 | 18 | 48 | 42 |

| | MODEL 1 | MODEL 2 |
|---|---------|---------|
| WEIGHT: | 1,000 LBS | 1,000 LBS |
| BTU/HR: | 7,500 | 6,000 |
| CFM: | 500 | 400 |
| POWER: | 3.2 KVA | 2.4 KVA |

| PHASES | 3 |
|--------|---|
| PLUG | R AND S FS3760 |
| CONNECTOR | R AND S FS3934 |
| RECEPTACLE | R AND S FS3754 |

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|-------------|---------|
| REL HUMIDITY | 8–80% |
| WET BULB | 78°F |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|-------------|----------|
| REL HUMIDITY | 8–80% |
| WET BULB | 80°F |

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

•Figure 14-16.   Plan View of 2821 Control Unit Model 1 and 2

14-19

2540 CARD READ PUNCH

PLAN VIEW
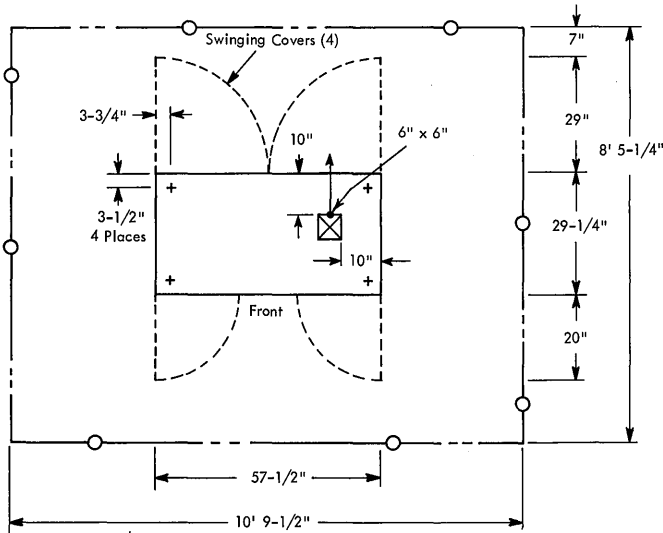


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 57-1/2 | 29-1/4 | 45-1/4* |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 36 | 36 | 36 | 36 |

WEIGHT:  1,050 POUNDS

BTU/HR:  3,000

CFM:      50

POWER:   1.2 KVA**

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|---|---|
| REL HUMIDITY | 20–80% |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|---|---|
| REL HUMIDITY | 8–80% |

CABLE LIMITATIONS:

  SEE SECTION ON CABLING.

NOTES:
 *ADD 20-1/4 INCHES FOR READ
   FILE FEED.
**POWERED FROM 2821.

•Figure 14-17.  Plan View of 2540 Card Read Punch

1403 PRINTER MODEL 2

PLAN VIEW
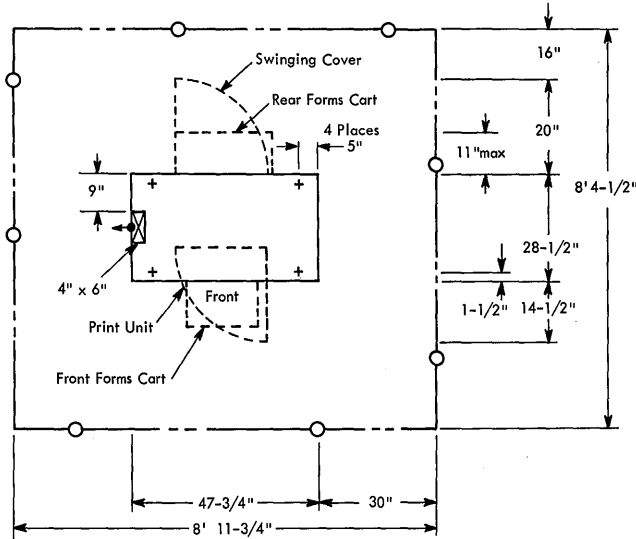


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 47-3/4 | 28-1/4 | 53-1/4 |

SERVICE CLEARANCE (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 36 | 36 | 30 | 30 |

WEIGHT: 750 POUNDS

BTU/HR: 3,000

CFM: 310

POWER: 1.0 KVA*

ENVIRONMENT OPERATING:

TEMPERATURE       60–90°F
REL HUMIDITY      20–80%

ENVIRONMENT NONOPERATING:

TEMPERATURE       50–110°F
REL HUMIDITY      8–80%

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTE:
*POWERED FROM 2821

●Figure 14-18.   Plan View of 1403 Printer Model 2

## 2701 DATA ADAPTER UNIT

### PLAN VIEW
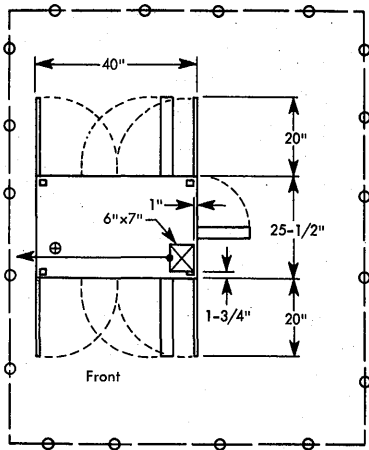


SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 40 | 25-1/2 | 40 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 42 | 42 | 42 | 6* |

WEIGHT: 600 POUNDS

BTU/HR: 3,000

CFM: 120

POWER: 1.0 KVA

| PHASES | 1 |
|--------|---|
| PLUG | R AND S, FS3720 |
| CONNECTOR | R AND S, FS3913 |
| RECEPTACLE | R AND S, FS3743 |

ENVIRONMENT OPERATING:

| TEMPERATURE | 60–90°F |
|-------------|---------|
| REL HUMIDITY | 20–80% |
| WET BULB | 78°F |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | 50–110°F |
|-------------|----------|
| REL HUMIDITY | 8–80% |
| WET BULB | 80°F |

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTES:
*FOR AIR CIRCULATION.

●Figure 14-19. Plan View of 2701 Data Adapter Unit

2314 DIRECT ACCESS STORAGE FACILITY-A SERIES

PLAN VIEW
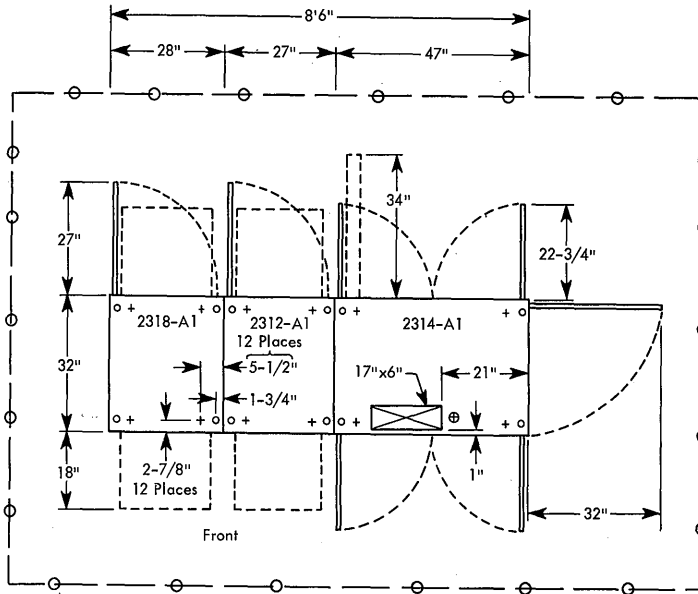


SPECIFICATIONS

DIMENSIONS (INCHES)

        F           S      H
  SEE PLAN VIEW.        60

SERVICE CLEARANCES (INCHES)

       F     R    RT   L
       36    48   42   24

WEIGHT:
BTU/HR:        } SEE TABLE
CFM:
POWER:

PHASES        3
PLUG          R AND S FS3760
CONNECTOR     R AND S FS3934
RECEPTACLE    R AND S FS3754

ENVIRONMENT OPERATING:

TEMPERATURE     60–90°F
REL HUMIDITY    20–80%
WET BULB        78°F MAX.

ENVIRONMENT NONOPERATING:

TEMPERATURE     50–110°F
REL HUMIDITY     8–80%
WET BULB        80°F MAX.

CABLE LIMITATIONS:

SEE SECTION ON CABLING.

NOTE:
*2312 AND 2318 POWERED FROM
 THE 2314 CONTROL UNIT.

INDIVIDUAL UNIT SPECIFICATIONS

| UNIT | BTU/HR | KVA | CFM | LENGTH | WIDTH | WEIGHT |
|------|--------|-----|-----|--------|-------|--------|
| 2314-A1 | 3,100 | 1.1 | 1,000 | 47 | 32 | 950 LBS |
| 2312-A1 | 1,900 | 0.7 | 200 | 28 | 32 | 500 LBS |
| 2318-A1 | 3,800 | 1.4 | 200 | 28 | 32 | 690 LBS |

•Figure 14-20.   Plan View of 2314 Direct Access Storage Facility

PLAN VIEW



SPECIFICATIONS

DIMENSIONS (INCHES)

| F | S | H |
|---|---|---|
| 23* | 19-3/4 | 9 |

SERVICE CLEARANCES (INCHES)

| F | R | RT | L |
|---|---|----|---|
| 0 | 0 | 0 | 0 |

WEIGHT: 65 POUNDS

BTU/HR: 570

CFM: 0

POWER: 0.17 KVA

ENVIRONMENT OPERATING:

| TEMPERATURE | $50-110^{\circ}F$ |
|-------------|-------------------|
| REL HUMIDITY | 10–80% |
| WET BULB | $80^{\circ}F$ |

ENVIRONMENT NONOPERATING:

| TEMPERATURE | $50-110^{\circ}F$ |
|-------------|-------------------|
| REL HUMIDITY | 10–80% |
| WET BULB | $80^{\circ}F$ |

NOTES:
*INCLUDES 1-1/2 INCHES FOR
 KNOBS ON ENDS OF PLATEN.

•Figure 14-21.  Plan View of 1052 Printer-Keyboard, Model 7

LEGEND:

——— SOLID OUTLINE DEFINES MINIMUM
CONFIGURATION. LESSER CONFIGURATION ARE
POSSIBLE SUBJECT TO DESIGN REVIEW.
– – – DOTTED OUTLINE DEFINES MAXIMUM EXPANSION.

 * CE BATTERY FRAME. BATTERY BACK-UP FOR CE(S)
CONTAINED IN THIS FRAME.

 ** MAIN WALL SPACER FRAME. REQUIRED BETWEEN
TWO SE'S WHEN NOT SEPARATED BY A CE OR A
CE BATTERY FRAME.

 *** RIGHT OR LEFT HAND READING BOARD OPTIONAL.
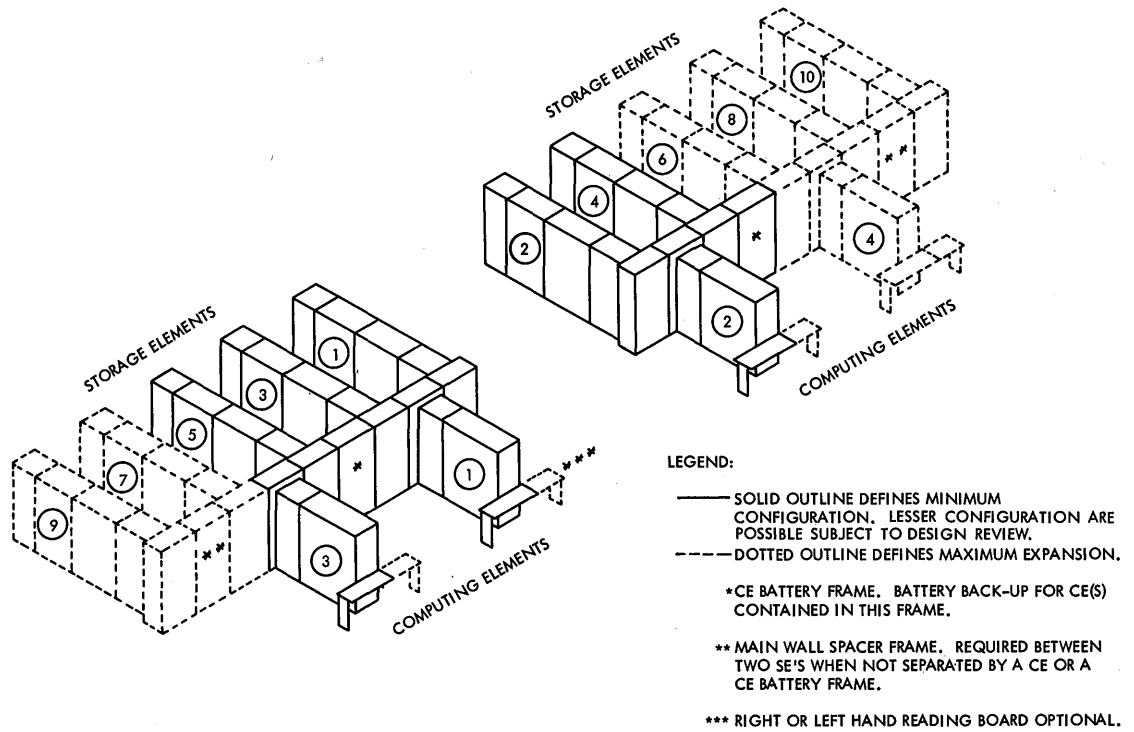
●Figure 14-22. 9020D CE and SE Element Numbering and Order of Expansion



DE'S CAN BE EXPANDED
INDEPENDENT OF SE'S

LEGEND:

——— SOLID OUTLINE DEFINES MINIMUM CONFIGURATION
LESSER CONFIGURATION ARE POSSIBLE SUBJECT TO
DESIGN REVIEW

– – – DOTTED OUTLINE DEFINES MAXIMUM EXPANSION

 * CE BATTERY FRAME. BATTERY BACK-UP FOR CE(S)
CONTAINED IN THIS FRAME.

 ** MAIN WALL SPACER FRAME. REQUIRED BETWEEN TWO
SE'S OR DE'S WHEN NOT SEPARATED BY A CE OR A CE
BATTERY FRAME.

 *** RIGHT OR LEFT HAND READING BOARD OPTIONAL.

Figure 14-23. 9020E CE, SE and DE Element Numbering and Order of
Expansion

14-25

EXTERNAL CABLING

Cabling within the 9020D/E System is accomplished, almost exclusively, through the use of 20 conductor coax cables.


Cable lengths within the system will be determined after the final equipment configuration has been selected. In the interests of best electrical design all cable lengths should be kept as short as possible. Figures 14-24 through 14-29 schematically portray the cabling length limitations for the Systems. See Appendix D for detailed information concerning cable length restrictions applicable to the selector channels of the IOCE. The dimensions listed are center to center between cabling access holes at the floor line; allowances will be necessary for false floor height and cases of indirect cable routing. Size and location of cabling access holes are included on the element Plan View Drawings, Figures 14-6 through 14-20. These openings should be smooth so as not to damage the cable insulation.

All external 9020 System cabling will be within the plenum area between the false floor and building floor. For a standard Triplex or Quad configuration, a false floor height of 12 inches appears to be adequate. It may be necessary to increase this height, based on future planning. Factors to be considered are:

1. Actual equipment configuration.
2. Planned expansion.
3. 9020 plus peripheral device cabling size and count.
4. Other conduits, cables, etc., also located under the floor.

Area of cable concentration can be determined only after the final equipment layout has been selected. Cable counts per element or unit for a typical 9020D Triplex system installation and for a Quad configuration are included in Tables 14-1 and 14-2. Cable counts for a typical 9020E Triplex and Quad configuration are contained in Tables 14-3 and 14-4. GFE cables are not included in these tables. Channel-Channel adapter cables appear only in the per-box tables (14-1 and 14-3). I/O Channel cables for the third (9020E) IOCE are not defined, all other cabling is listed. Space allowances for cabling can be estimated from these tables.

Table 14-1  Cable Count Per Box (9020D Triplex)

| ELEMENT OR UNIT | 20 CONDUCTOR COAX CABLE BODIES | TWISTED PAIR CABLE BODIES | OTHERS |
|---|---|---|---|
| CE 1 | 57 | – | 1 |
| CE 2 | 56 | – | 1 |
| CE 3 | 57 | – | 1 |
| | | | |
| SE 1 | 63 | 1 | 1 |
| SE 2 | 57 | 1 | 1 |
| SE 3 | 21 | 1 | 1 |
| SE 4 | 21 | 1 | 1 |
| SE 5 | 15 | 1 | 1 |
| SE 6 | 15 | 1 | 1 |
| SE 7 | 15 | 1 | 1 |
| SE 8 | 15 | 1 | 1 |
| | | | |
| IOCE 1 | 71 | – | 1 |
| IOCE 2 | 71 | – | 1 |
| IOCE 3 | 62 | – | 1 |
| | | | |
| SYS CONS | 64 | 11 | 25 |
| | | | |
| PAM 1* | 18 | 1 | 2 |
| PAM 2 | 18 | 1 | 2 |
| PAM 3 | 15 | 1 | 2 |
| | | | |
| TCU 1 | 16 | – | 1 |
| TCU 2 | 16 | – | 1 |
| TCU 3 | 13 | – | 1 |
| | | | |
| 2821-01 | 2 | – | 6 |
| 2821-02 | 4 | – | 6 |
| | | | |
| SCU 1 | 16 | – | 1 |
| SCU 2 | 16 | – | 1 |
| SCU 3 | 13 | – | 1 |

* PAM CABLING WILL VARY CONSIDERABLY DEPENDING ON I/O DEVICES.

Table 14-2. Maximum Cable Count by Element Or Unit
Typical 9020D Expanded Quad System

| | SE 1 | SE 2 | SE 3 | SE 4 | SE 5 | SE 6 | SE 7 | SE 8 | SE 9 | SE 10 | CE 1 | CE 2 | CE 3 | CE 4 | IOCE 1 | IOCE 2 | IOCE 3 | PAM 1 | PAM 2 | PAM 3 | SC** | TCU 1 | TCU 2 | TCU 3 | SCU 1 | SCU 2 | SCU 3 | 1052 | 2821-01 | 2821-02 | 2540 | 1403 | OTHER I/O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SE 1 | | 54 | | | | | | | | | 1 | 1 | 1 | 1 | 4 | 4 | 4 | | | | 2 | | | | | | | | | | | | |
| SE 2 | 54 | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 3 | | | | | | | | | | | 1 | 1 | 1 | 1 | 4 | 4 | 4 | | | | 2 | | | | | | | | | | | | |
| SE 4 | | | | | | | | | | | 1 | 1 | 1 | 1 | 4 | 4 | 4 | | | | 2 | | | | | | | | | | | | |
| SE 5 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 6 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 7 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 8 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 9 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| SE 10 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | | 2 | | | | | | | | | | | | |
| CE 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 17 | 17 | 1 | 4 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | | | 1 | | | | | | | | |
| CE 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 17 | | 1 | 17 | 4 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | | | 1 | | | | | | | | |
| CE 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 17 | 1 | | 10 | 5 | 2 | 2 | 1 | 1 | 1 | 6 | 1 | | | 1 | | | | | | | | |
| CE 4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 17 | 10 | | 4 | 1 | 1 | 1 | 1 | 1 | 6 | 1 | | | 1 | | | | | | | | |
| IOCE 1 | 4 | 2 | 4 | 4 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 5 | 4 | 12 | | | 2 | | | 2 | 2 | | | 2 | | | | | | | | |
| IOCE 2 | 4 | 2 | 4 | 4 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 2 | 1 | | 12 | | | 2 | | 2 | | 2 | | | 2 | | | | | | | |
| IOCE 3 | 4 | 2 | 4 | 4 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 2 | 1 | | | 12 | | | 2 | 2 | | | 2 | | | 2 | | | | | | |
| PAM 1 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | | | | 2 | 2 | 2 | | | | | | | 3 | | | | | * |
| PAM 2 | | | | | | | | | | | 1 | 1 | 1 | 1 | | 2 | | 2 | | 2 | 2 | | | | | | | 3 | | | | | * |
| PAM 3 | | | | | | | | | | | 1 | 1 | 1 | 1 | | | 2 | 2 | 2 | | 2 | | | | | | | 3 | | | | | * |
| SC** | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 6 | 6 | 2 | 2 | 2 | 2 | 2 | 2 | | 2 | 2 | 2 | 2 | 2 | 2 | 5 | 3 | 5 | | | |
| TCU 1 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | | | | | | 2 | | 4 | | | | | | | | | | |
| TCU 2 | | | | | | | | | | | | | | | | 2 | | | | | 2 | 4 | | 4 | | | | | | | | | |
| TCU 3 | | | | | | | | | | | | | | | | | 2 | | | | 2 | | 4 | | | | | | | | | | |
| SCU 1 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | | | | | | 2 | | | | | 6 | 2 | | | | | | |
| SCU 2 | | | | | | | | | | | | | | | | 2 | | | | | 2 | | | | 6 | | 6 | | | | | | |
| SCU 3 | | | | | | | | | | | | | | | | | 2 | | | | 2 | | | | 2 | 6 | | | | | | | |
| 1052 | | | | | | | | | | | | | | | | | | 3 | 3 | 3 | 5 | | | | | | | | | | | | |
| 2821-01 | | | | | | | | | | | | | | | | | | | | | 3 | | | | | | | | | | | | |
| 2821-02 | | | | | | | | | | | | | | | | | | | | | 5 | | | | | | | | | | 2 | 3 | |
| 2540 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 2 | | | |
| 1403 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 3 | | | |
| OTHER I/O | | | | | | | | | | | | | | | | | | * | * | * | | | | | | | | | | | | | |

* DEPENDS ON SELECTION OF GFE DEVICES
** EPO CABLE INCLUDED

Table 14-3. Cable Count Per Box (9020E Triplex)

| ELEMENT OR UNIT | 20 CONDUCTOR COAX CABLE BODIES | TWISTED PAIR CABLE BODIES | OTHERS |
|---|---|---|---|
| CE 1 | 63 | 1 | 2 |
| CE 2 | 61 | 1 | 2 |
| CE 3 | 62 | 1 | 2 |
| | | | |
| SE 1 | 54 | 1 | 1 |
| SE 2 | 14 | 1 | 1 |
| SE 3 | 18 | 1 | 1 |
| SE 4 | 14 | 1 | 1 |
| | | | |
| DE 1 * | 44 | 1 | 1 |
| DE 2 | 8 | 1 | 1 |
| DE 3 | 7 | 1 | 1 |
| DE 4 | 7 | 1 | 1 |
| | | | |
| IOCE 1 | 57 | - | 1 |
| IOCE 2 | 53 | - | 1 |
| | | | |
| CONF. CONS. | 53 | 11 | 21 |
| | | | |
| DAU 1 | 10 | - | 1 |
| DAU 2 | 6 | - | 1 |
| | | | |
| TCU 1 | 14 | - | 1 |
| TCU 2 | 9 | - | 1 |
| | | - | |
| 2821-01 | 2 | - | 6 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

* DG CABLING NOT INCLUDED.

Table 14-4. Maximum Cable Count by Element Or Unit
Typical 9020E Expanded Quad System

| | SE 1 | SE 2 | SE 3 | SE 4 | SE 5 | DE 1 | DE 2 | DE 3 | DE 4 | DE 5 | CE 1 | CE 2 | CE 3 | CE 4 | IOCE 1 | IOCE 2 | IOCE 3 | DAU 1 | DAU 2 | CC** | TCU 1 | TCU 2 | 1052(CE 1) | 1052(CE 2) | 1052(CE 3) | 2821-01 | 2540 | 1403 | OTHER I/O |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SE 1 | | 48 | | | | | | | | | 1 | 1 | 1 | 1 | 4 | 4 | 4 | | | 2 | | | | | | | | | |
| SE 2 | 48 | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | 2 | | | | | | | | | |
| SE 3 | | | | | | | | | | | 1 | 1 | 1 | 1 | 4 | 4 | 4 | | | 2 | | | | | | | | | |
| SE 4 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | 2 | | | | | | | | | |
| SE 5 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | | | 2 | | | | | | | | | |
| DE 1 | | | | | | | | | | | 3 | 3 | 2 | 2 | | | | | | 2 | | | | | | | | | * |
| DE 2 | | | | | | | | | | | 2 | 3 | 2 | 2 | | | | | | 2 | | | | | | | | | * |
| DE 3 | | | | | | | | | | | 2 | 2 | 2 | 3 | | | | | | 2 | | | | | | | | | * |
| DE 4 | | | | | | | | | | | 2 | 2 | 2 | 3 | | | | | | 2 | | | | | | | | | * |
| DE 5 | | | | | | | | | | | 2 | 2 | 2 | 2 | | | | | | 2 | | | | | | | | | * |
| CE 1 | 1 | 1 | 1 | 1 | 1 | 3 | 2 | 2 | 2 | 2 | | 17 | 18 | 1 | 4 | 1 | 1 | | | 3 | 1 | | | | | | | | |
| CE 2 | 1 | 1 | 1 | 1 | 1 | 3 | 3 | 2 | 2 | 2 | 17 | | 1 | 17 | 4 | 1 | 1 | | | 3 | 1 | | | | | | | | |
| CE 3 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 18 | 1 | | 10 | 5 | 2 | 2 | | | 7 | 1 | | | | | | | | |
| CE 4 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 3 | 3 | 2 | 1 | 17 | 10 | | 4 | 1 | 1 | | | 7 | 1 | | | | | | | | |
| IOCE 1 | 4 | 2 | 4 | 2 | 2 | | | | | | 4 | 4 | 5 | 4 | | 12 | | | | 2 | 2 | 2 | 2 | | | | | | |
| IOCE 2 | 4 | 2 | 4 | 2 | 2 | | | | | | 1 | 1 | 2 | 1 | 12 | | | | | 2 | 2 | 2 | | 2 | | | | | |
| IOCE 3 | 4 | 2 | 4 | 2 | 2 | | | | | | 1 | 1 | 2 | 1 | | 12 | | | | 2 | | | | | | | | | |
| DAU 1 | | | | | | | | | | | | | | | | | | | 4 | 6 | | | | | | | | | * |
| DAU 2 | | | | | | | | | | | | | | | | | | 4 | | 2 | | | | | | | | | * |
| CC** | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 7 | 7 | 2 | 2 | 2 | 6 | 2 | | 2 | 2 | 3 | 3 | 3 | 3 | | | |
| TCU 1 | | | | | | | | | | | 1 | 1 | 1 | 1 | 2 | 2 | | | | 2 | | 4 | | | | | | | |
| TCU 2 | | | | | | | | | | | | | | | 2 | 2 | | | | 2 | 4 | | | | | | | | |
| 1052(CE 1) | | | | | | | | | | | | 2 | | | | | | | | 3 | | | | 2 | | | | | |
| 1052(CE 2) | | | | | | | | | | | | | | | | | | | | 3 | | | | | | | | | |
| 1052(CE 3) | | | | | | | | | | | | 2 | | | | | | | | 3 | | | | 2 | | | | | |
| 2821-01 | | | | | | | | | | | | | | | | | | | | 3 | | | | | | | 2 | 3 | |
| 2540 | | | | | | | | | | | | | | | | | | | | | | | | | | 2 | | | |
| 1403 | | | | | | | | | | | | | | | | | | | | | | | | | | 3 | | | |
| OTHER I/O | | | | | | * | * | * | * | * | | | | | | | | * | * | | | | | | | | | | |

\* DEPENDS ON SELECTION OF GFE DEVICES
\*\* EPO CABLE INCLUDED

●Figure 14-24.  Cable Length Diagram—IOCE Channel Cabling

Within the figure:

**Top section (9020 A/D):**

Boxes: 2821-02, SYSTEM CONSOLE, PAM, PAM, SCU*, TCU

Connections labeled: D, C, B, A, E, F

NOTE: THE CHAN-CHAN ADAPTER IS CONSIDERED AS THOUGH IT WERE A CONTROL UNIT ON EACH OF THE CHANNELS INVOLVED. THE ADAPTER REQUIRES EXTERNAL CABLES TO A CONTROL UNIT OR CHANNEL OF THE SECOND SYSTEM.
* Last SCU.

INTERNAL CABLING

MULTIPLEXOR | SELECTOR / SELECTOR
IOCE

CHAN-CHAN ADAPTER
G
TCU

9020 A/D

MAXIMUM CABLE LENGTHS FOR PLANNING PURPOSES FOR SPECIFIC DETAILS REFERENCE APPENDIX D
E = 100'
E+F = 200'
G+H = 200'
THESE LENGTHS SHOULD BE MINIMIZED TO MAXIMIZE DATA RATES

H          L

9020 A/D
CHAN-CHAN ADAPTER

**Bottom section (9020E):**

Boxes: DAU, DAU, CONFIG CONSOLE, PTR/KYBD ADAPTER, PTR/KYBD ADAPTER

Connections labeled: E, D, C, B, A, K

TCU

9020E

MAXIMUM CABLE LENGTHS FOR PLANNING PURPOSES FOR SPECIFIC DETAILS REFERENCE APPENDIX D
A+B+C+D+E = 200'
J = 200'
K+L = 200'
M = 200'
THESE LENGTHS SHOULD BE MINIMIZED TO MAXIMIZE DATA RATES.

INTERNAL CABLING

MULTIPLEXOR | SELECTOR / SELECTOR / SELECTOR
IOCE

CHAN-CHAN ADAPTER
J
TCU
M

Boxes (top row): CE, CE, CE, CE, 2540, 1403

Connections labeled: X, Y, Z, W, V, V, V, V, AA, AK, AK

2821-01

AJ

SYSTEM CONSOLE

U, U, U, U, U

Boxes (bottom row): SE, IOCE, PAM, TCU, SCU

AL

2401, 2401

AM, AN

MAXIMUM CABLE LENGTHS
U = 100', V = 75'
W + X + Y + Z + AA = 150'
AJ = 50', AK = 25'
AL + AM ..... = 100'

TOTAL LENGTH MAY NOT
EXCEED 100' FOR UP TO
EIGHT 2401'S

●Figure 14-25.  Cable Length Diagram–System Console to
IBM 9020D Units and Elements

14-32

The diagram shows a configuration console connected to various IBM 9020E units and elements:

- Four CE boxes at top, connected to each other by cables X, Y, Z
- Cables V, V, V, V and W, AA connect the CE units to the CONFIGURATION CONSOLE
- The CONFIGURATION CONSOLE connects via cables U, U, U, U, U and AJ to: DE, SE, IOCE, DAU, TCU, and 2821-01
- 2540 and 140 boxes connect via AK and AK to 2821-01
- TCU connects via AL to 2401, and 2401 connects via AM to another 2401

MAXIMUM CABLE LENGTHS
U = 100' V = 75'
W+X+Y+Z+AA = 150'
AJ = 50', AK = 25'
AL+AM...₊ = 100'

TOTAL LENGTH
MAY NOT
EXCEED 100'
FOR UP TO
EIGHT 2401'S.

Figure 14-26.   Cable Length Diagram–Configuration Console to
IBM 9020E Units and Elements

9020D
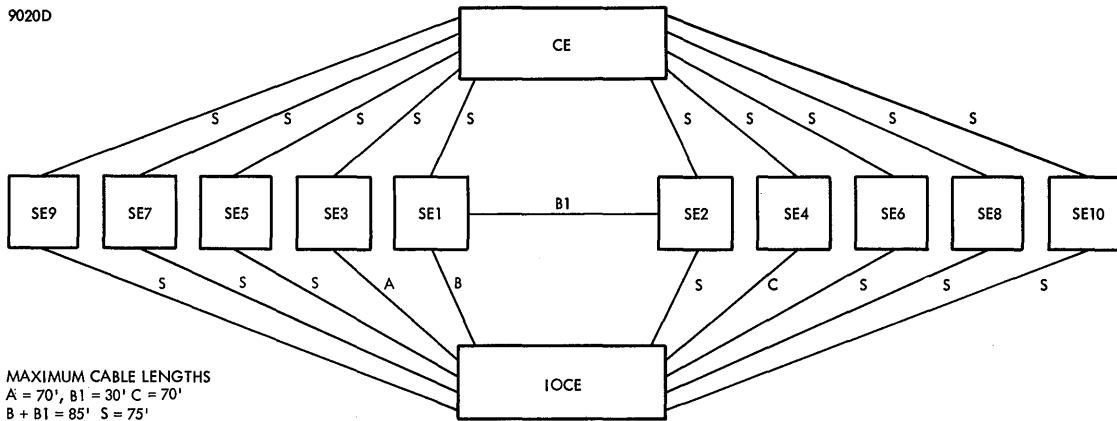
MAXIMUM CABLE LENGTHS
A = 70', B1 = 30' C = 70'
B + B1 = 85'  S = 75'

9020E
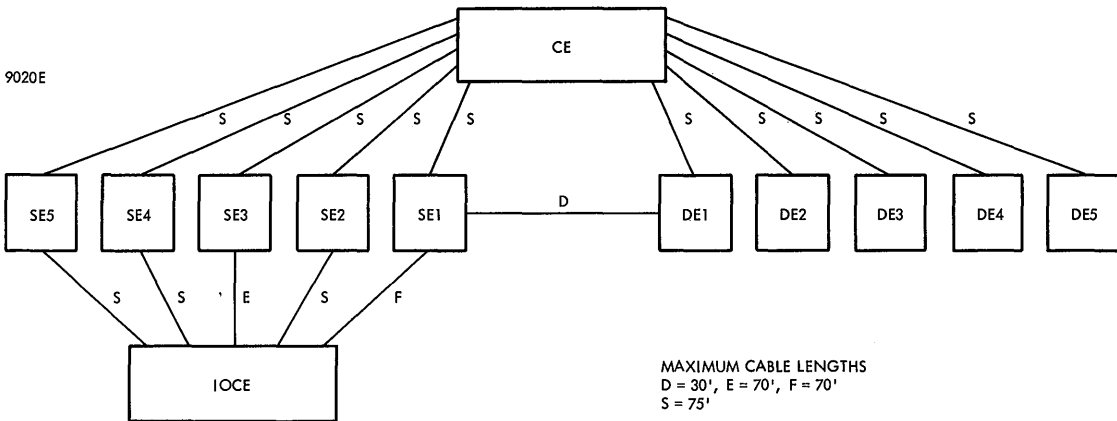
MAXIMUM CABLE LENGTHS
D = 30', E = 70', F = 70'
S = 75'

Figure 14-27.   Cable Length Diagram-SE/DE to CE and IOCE
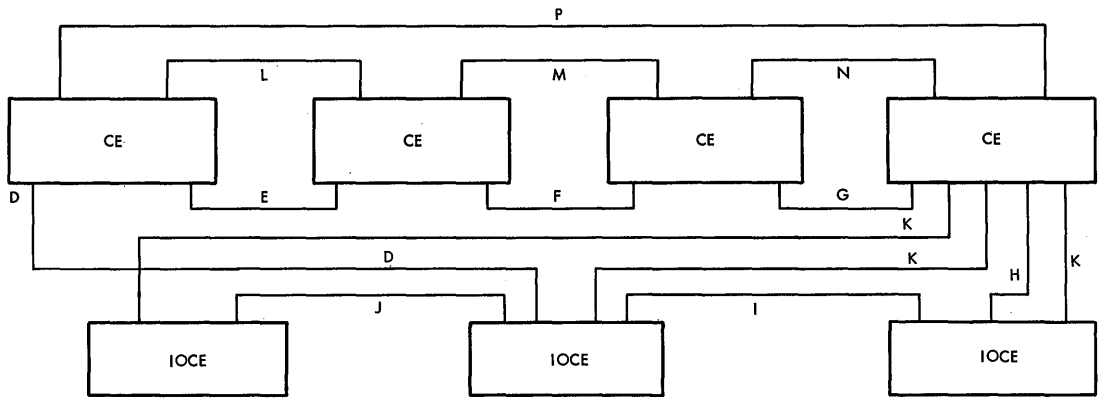
MAXIMUM CABLE LENGTHS
D + E + F + G = 150'
H + I + J = 150'
K = 100', P = 100'
L + M + N = 100'
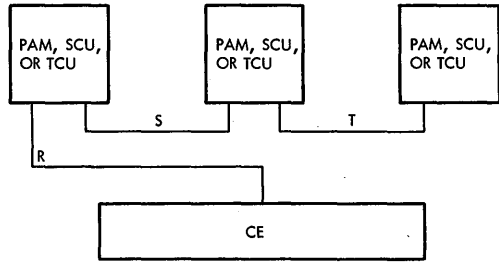
MAXIMUM CABLE LENGTH
R + S + T = 150'

Figure 14-28.  Cable Length Diagram–CE to IBM 9020D/E
Units and Elements
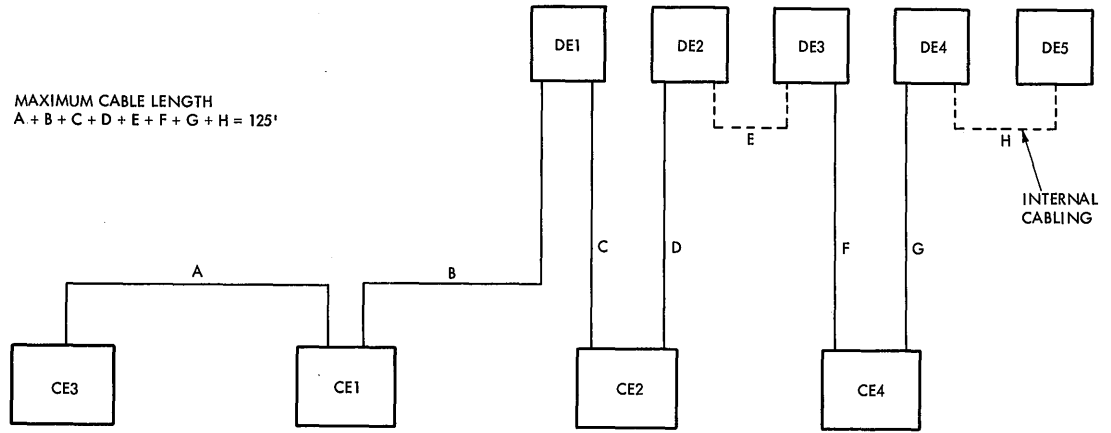


MAXIMUM CABLE LENGTH
A + B + C + D + E + F + G + H = 125'

INTERNAL
CABLING

Figure 14-29.  Cable Length Diagram–DE Test Bus

POWER

Figure 14-30 is a schematic representation of power distribution from the prime power source to the computer logic. KVA and power connector receptacle information for each of the units is listed on Figures 14-6 through 14-21. The following chart indicates the current ratings of the various power plugs and associated connectors and receptacles used. The number of wires shown include one insulated grounding conductor (green or green with yellow tracer).

|     | Plug   | Connector | Receptacle | Rating |
| --- | ------ | --------- | ---------- | ------ |
| R&S | FS3720 | FS3913 | FS3743 | 15 amp, 1 Phase, 3 wire |
| R&S | FS3750 | FS3933 | FS3753 | 30 amp, 1 Phase, 3 wire |
| R&S | FS3760 | FS3934 | FS3754 | 30 amp, 3 Phase, 4 wire |
| R&S | SC7328 | SC7428 | SC7324 | 60 amp, 3 Phase, 4 wire |

The power feeder for the computer system should be protected by a main line circuit breaker. The individual branch circuits on the distribution panel should be protected by suitable circuit breakers properly rated according to manufacturer's specifications. Branch circuits should terminate under the raised floor as close as possible to the machine they supply; however, they should not be terminated directly beneath the Signal Cable access holes because of interference with installation of the signal cabling. The receptacle or connector should in all cases be within ten feet of the power cable
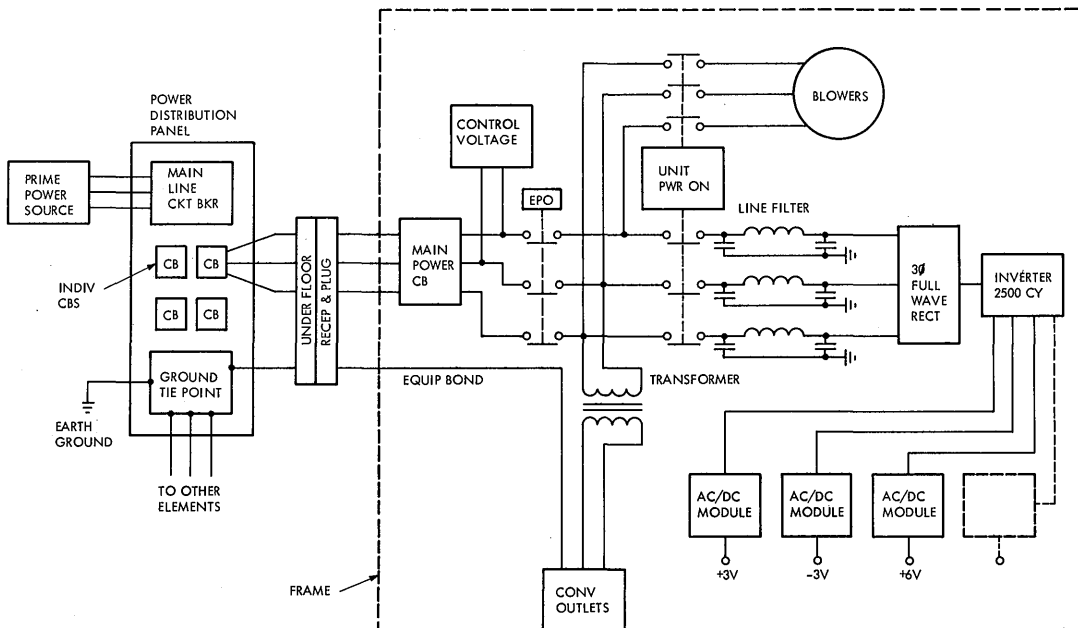


Figure 14-30. Simplified Schematic Diagram of Typical Power Distribution

exit and be under a freely removable cover. The Plan View Drawings depict the location of the power cord. The cord can be routed through the signal cable access hole when practical.

The 3-phase power receptacles for use with the system must be wired for correct phase rotation. Looking at the face of the receptacle and running counterclockwise from the ground pin, the sequencing will be: Phase 1, Phase 2, and Phase 3. Correct phasing is absolutely essential to the proper operation of the system.

A suitable number of convenience outlets should be installed in the computer room and maintenance room for use by building maintenance personnel, porter service, customer engineers, etc. IBM will supply recommendations for locating the receptacles within the maintenance room. 115V outlets are not to be supplied from the computer power panel.

Thermo-magnetic circuit breakers are used in all of the 9020D/E elements and units. Ratings are as follows:

| | | | |
|---|---|---|---|
| 7265-02 | System Console | 20 amps | |
| 7265-03 | Configuration Console | 25 amps | (two) |
| 7201-02 | Computing Element | 50 amps | |
| 7251-09 | Storage Element | 40 amps | |
| 7289-04 | Display Element | 40 amps | |
| 7231-02 | I/O Control Element | 30 amps | |
| 7289-02 | Peripheral Adapter Module | 50 amps | |
| 2803-01 | Tape Control Unit | 50 amps | |
| 2821-01/02 | Control Unit | 30 amps | |
| 2701 | Data Adapter Unit | 15 amps | |
| 2314-A1 | Storage Control Unit | 40 amps | |

Standard System/360 110 VAC convenience outlets are provided on each of the 9020 stand-alone units. All convenience outlets which are part of the 9020D/E units are protected by separate fuses or circuit breakers. Details are shown on the power logic drawing, Figure 12-1

The element and unit power factors will average approximately .8 or better.

The maximum harmonic content of the phase voltage wave forms shall not be in excess of 5% with the equipment not operating.

The input power specification for the 9020D/E elements or units is 208 VAC ±10%, 60 cycle, ±2% (except 2701, plus or minus 1 cycle).

The ambient barometric pressure limits of the system are sea level to 7,000 feet. The 7,000 foot level is an operating limit. There is no altitude limit when not operating.

## Surge Currents

Figures 14-31 through 14-44 are reproductions of oscilloscope wave-forms showing input phase currents for the 9020 D/E elements and units. Measured values shown are equal to the maximum in-rush current observed during ten or more attempts.

Figures 14-31 through 14-35 represent in-rush values observed due to the convenience outlet transformers. Also included in these figures is the surge created by the control transformer. In all cases, the control transformers contribute an insignificant in-rush current value compared to the convenience outlet transformer.

Table 14-5 is a summary of convenience outlet transformer surges by unit type. The second column defines the phase connections. All convenience outlet transformers are single-phase. The fourth column defines the recommended value to be used for planning purposes.

Table 14-5. Summary of Convenience Outlet Transformer In-Rush

| Unit Type | Phase Connection | Measured Peak In-Rush | Recommended Peak In-Rush | Reference Figure |
|---|---|---|---|---|
| 7201-02 | 02, 03 | 380 | 400 | 14-31 |
| 7231-02 | 02, 03 | 380 | 400 | 14-31 |
| 7289-02 | 02, 03 | 380 | 400 | 14-31 |
| 2803-01 | 02, 03 | 380 | 400 | 14-31 |
| 7265-02 | 02, 03 | 380 | 400 | 14-31 |
| 7265-03 | Prime Power Cord 1 | 380 | 400 | 14-31 |
| 7251-09 | 02, 03 | 170 | 200 | 14-32 |
| 7289-04 | 02, 03 | 170 | 200 | 14-32 |
| 2821-01 | 02, 03 | 120 | 180 | 14-33 |
| 2701-01 | Single Phase | 120 | 200 | 14-34 |
| 2314-A1 | 01-03 | 160 | 250 | 14-35 |

Figures 14-36 through 14-44 represent the in-rush values observed for the power supply system for each unit type. These figures include the in-rush for blower motors. Due to time delays introduced by relay circuitry, the surges produced by the power supply system are not additive with the Convenience Outlet trans-formers. An increase of 15% above values shown in Figures 14-36 through 14-44 should be used for planning purposes.

Figure 14-36 shows the in-rush produced by the 75-amp converter/ inverter (C/I) measured on phase 2 of the 7251-09 Storage Element. The other two phases have similar waveforms. Other units (7231-02, 7201-02, 7289-02, and 7289-04) also have similar values of in-rush.

As shown, the in-rush to the 75-amp C/I occurs in two steps. The 75-amp C/I has in-rush limiting circuits which limit the initial surge (beginning of waveforms). The second surge occurs where the in-rush limiting circuitry is disabled.

The maximum Converter Inverter surge current could be as high as 400 amperes due mainly to the difference between interchangeable contactor driver cards, part number 374786 and 375316 (low surge).

The in-rush produced by the 25 amp C/I is shown in Figure 14-37. The 25-amp C/I is used in the 7265-02.

Figures 14-38 and 14-39 show the surge currents produced by the 7265-03 Configuration Console. This unit has two single-phase prime power cords. Figure 14-38 shows the surge produced on prime power cord 1 when RCU-1 and the SCCU are being powered from prime power cord 1. Figure 14-39 indicates the surge produced on prime power cord 2 with only RCU-2 as a load. When the SCCU is being powered from prime power cord 2, the larger surge shown in Figure 14-38 would then appear on prime power cord 2, with the smaller surge on prime power cord 1.

Figure 14-40 shows the surge current produced when power is turned on at the 2701 DAU. The DAU is a single-phase unit.

The in-rush for the 2803-01 TCU and associated 2401 Tape Units is shown in Figure 14-41. The TCU sequences on Tape Units and the TCU in the following order:

1.  Tape Bank 1 (4 drives)

2.  TCU

3.  Tape Bank 2 (4 drives)

Figure 14-41 shows the in-rush for the 2803 (beginning of wave-form) and Bank 2 with three Tape Drives attached. When a fourth drive is attached, an increase of 25% may be expected. The in-rush for Tape Bank 1 is not shown; however, the in-rush is equal to Bank 2. The in-rush for Bank 1 starts approximately 16 ms prior to the 2803 in-rush.

Figure 14-42 shows the in-rush for the 2314-A1 Storage Control Unit (SCU) power system and associated 2312-A1 Disk Storage Unit (DSU). The initial in-rush is due to the 2314-A1 power supplies. Similar values occur on all three phases. The second in-rush (center of waveform) is the surge produced by the 2312-A1 DSU motor. The motor surge occurs on phases 1 and 3.

The in-rush for the 2821-01 and 1403 printer are shown in Figures 14-43 and 14-44 respectively. The associated 2540 starting surge is not shown because this unit will not turn on until the operator starts the machine.

Vertical Scale: 200 Amps/division

Horizontal Scale: 20 ms/division
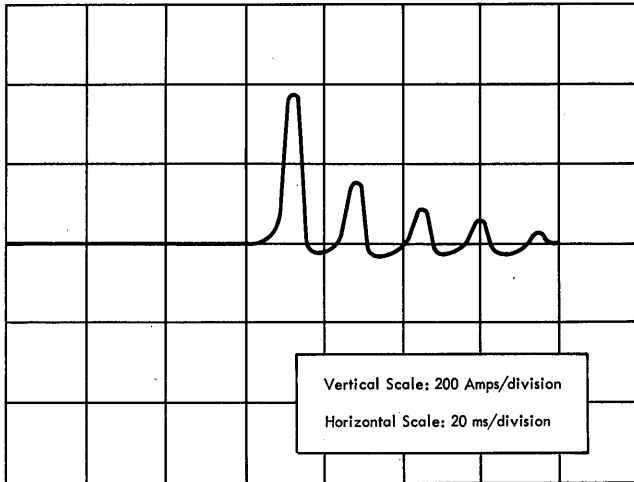
●Figure 14-31.   CE Convenience Outlet Transformer



Vertical Scale: 80 Amps/division

Horizontal Scale: 10 ms/division
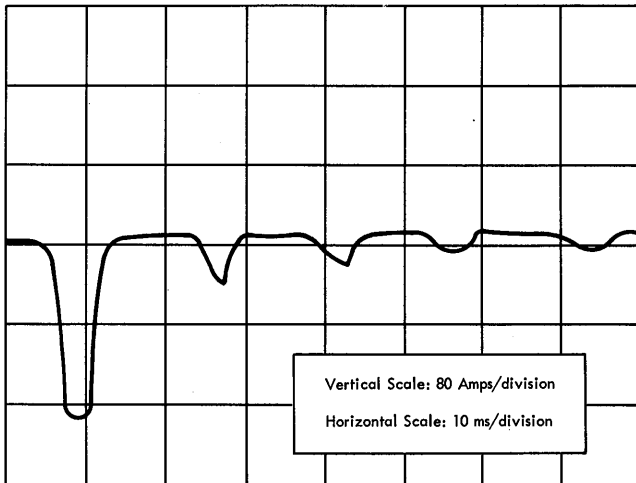
●Figure 14-32.   SE/DE Convenience Outlet Transformer

Vertical Scale: 40 Amps/division

Horizontal Scale: 10 ms/division
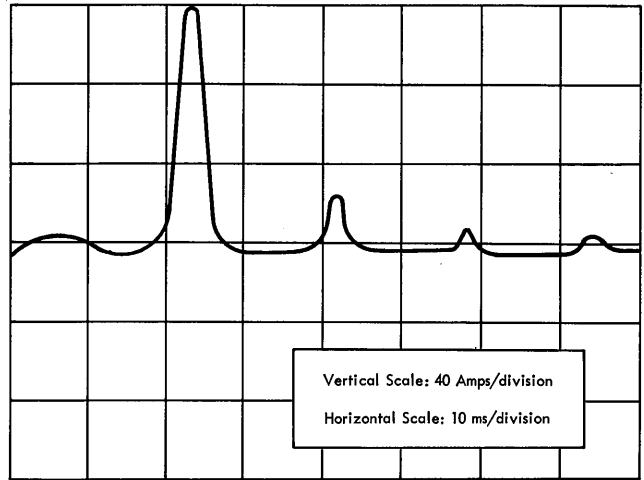
● Figure 14-33.   2821 Convenience Outlet Transformer



Vertical Scale: 40 Amps/division

Horizontal Scale: 10 ms/division
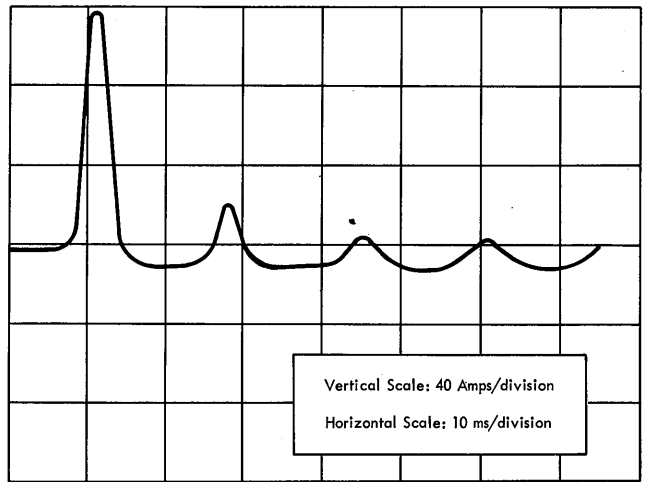
● Figure 14-34.   2701 Convenience Outlet Transformer

> Vertical Scale: 40 Amps/division
>
> Horizontal Scale: 5 ms/division
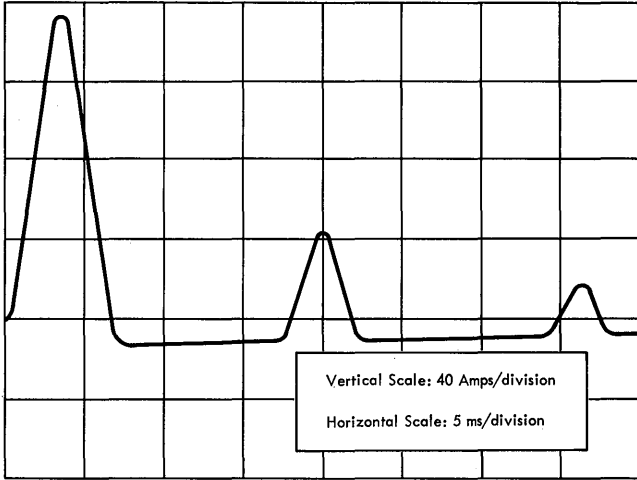
● Figure 14-35. 2314 Convenience Outlet Transformer



> Vertical Scale: 40 Amps/division
>
> Horizontal Scale: 50 ms/division
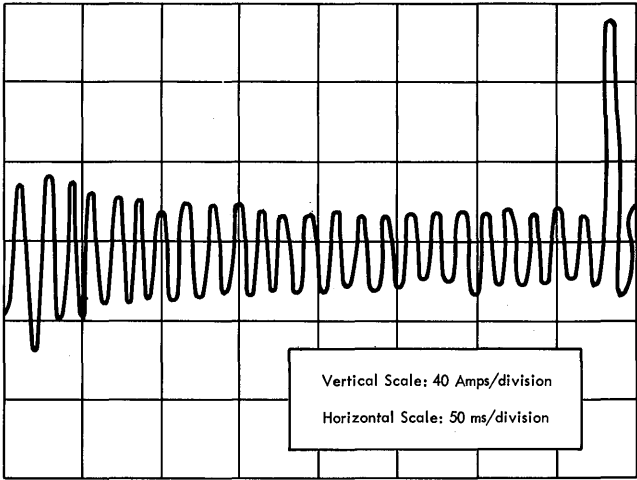
● Figure 14-36. 75-Amp Converter/Inverter

Vertical Scale: 45 Amps/division

Horizontal Scale: 10 ms/division
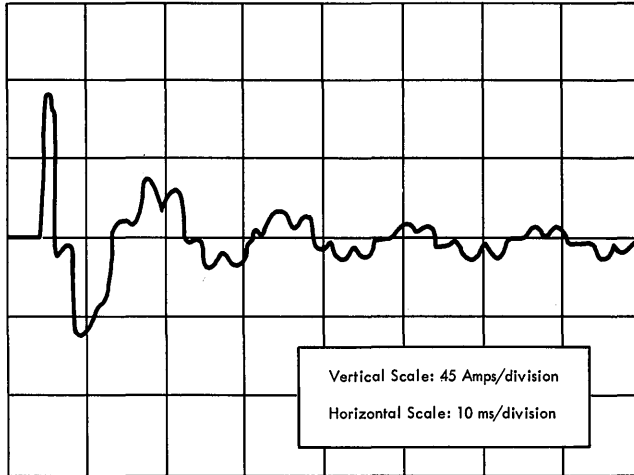
• Figure 14-37.   25-Amp Converter/Inverter, 25-Amp Load



Vertical Scale: 100 Amps/division

Horizontal Scale: 20 ms/division
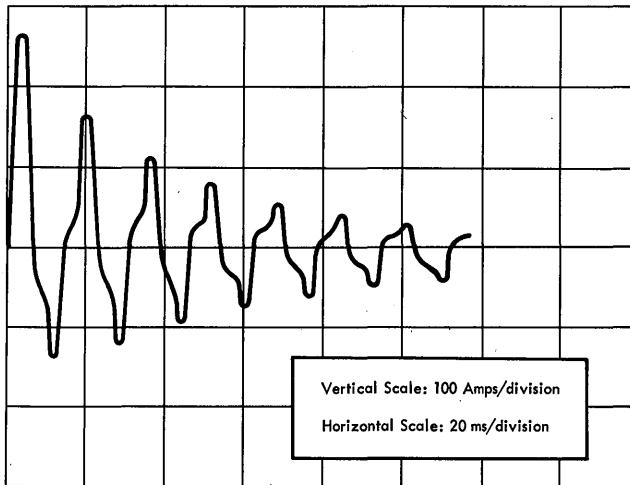
•Figure 14-38.   7265-03 Configuration Console, Prime Power Cord 1

> Vertical Scale: 100 Amps/division
>
> Horizontal Scale: 20 ms/division
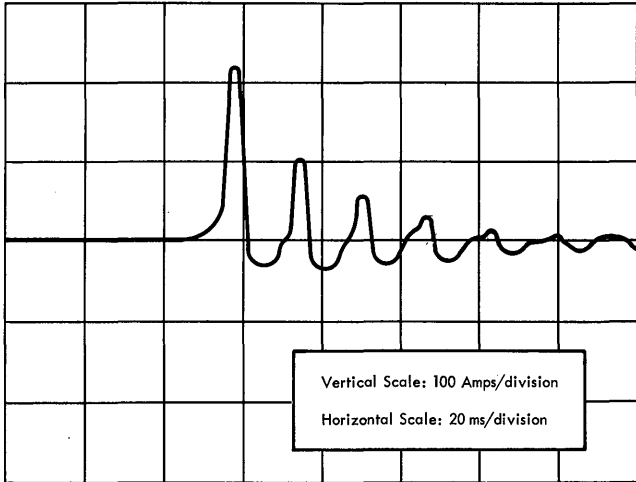
● Figure 14-39. 7265-03 Configuration Console, Prime Power Cord 2



> Vertical Scale: 20 Amps/division
>
> Horizontal Scale: 10 ms/division
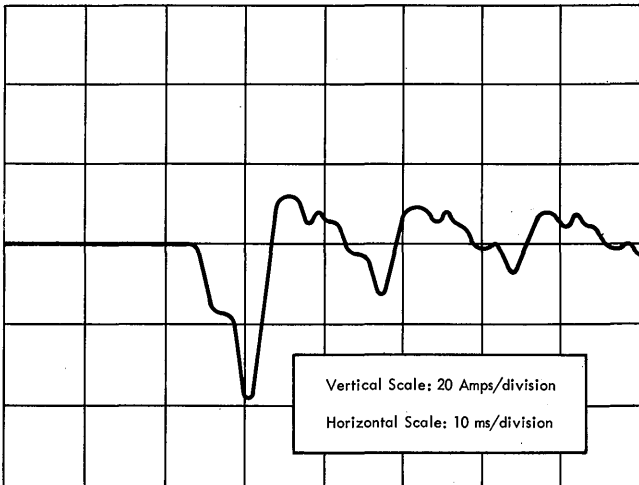
● Figure 14-40. 2701 Data Adapter Unit

14-44

> Vertical Scale: 80 Amps/division
>
> Horizontal Scale: 20 ms/division
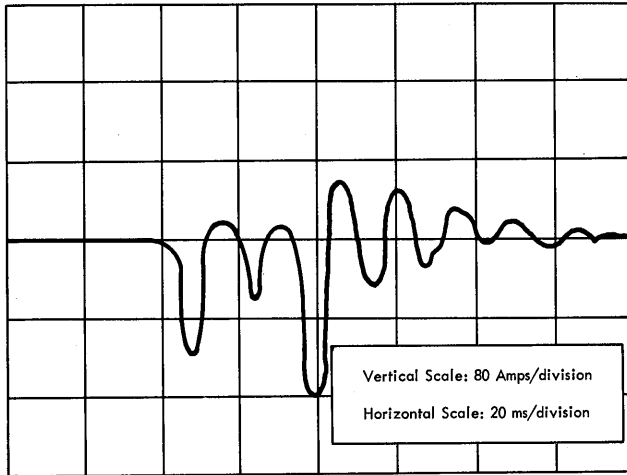
●Figure 14-41. 2803 Tape Control Unit and Tape Bank 2



> Vertical Scale: 40 Amps/division
>
> Horizontal Scale: 50 ms/division
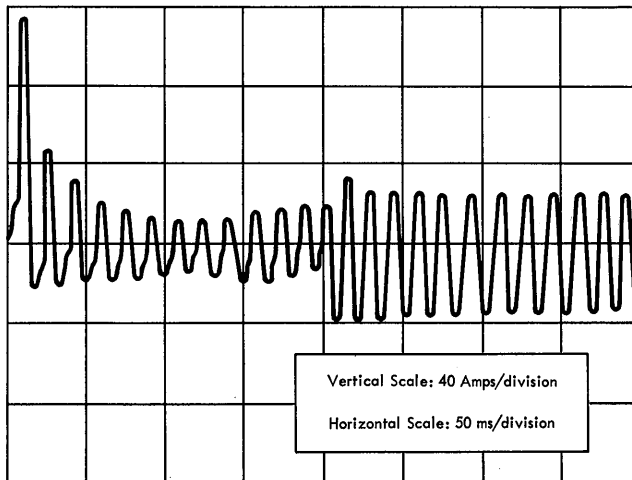
● Figure 14-42. 2314 Storage Control Unit and 2312 Disk Storage Unit

Vertical Scale: 40 Amps/division

Horizontal Scale: 20 ms/division
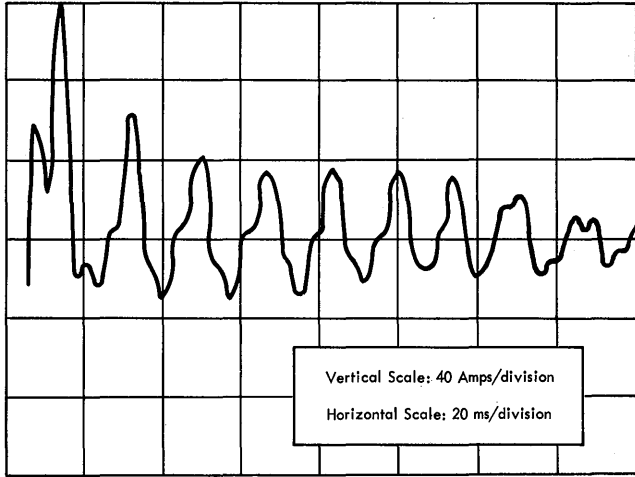
●Figure 14-43.   2821 Control Unit



Vertical Scale: 40 Amps/division

Horizontal Scale: 50 ms/division
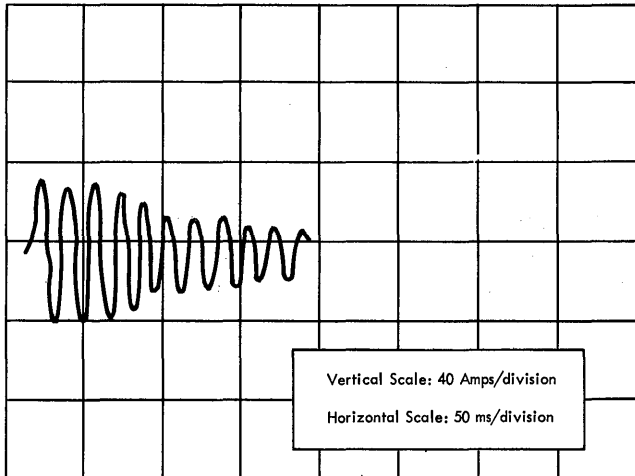
●Figure 14-44.   1403 Printer

To minimize the effects of surge currents, each of the following
elements contains a time-delay:

                 7289-02                PAM
                 7201-02                CE
                 7231-02                IOCE
                 7251-09                SE
                 7289-04                DE
                 7265-02                System Console

        The purpose of the time-delay is to provide a sequencing of
main line power to the Elements.  The relay used will conform to
the following specifications:

                 Adjustability                5 - 30 seconds
                 Reset Time                   200 milliseconds Max.
                 Timing Repeat Accuracy       ±10%

        This information will be included in the prime power requirement
specification.
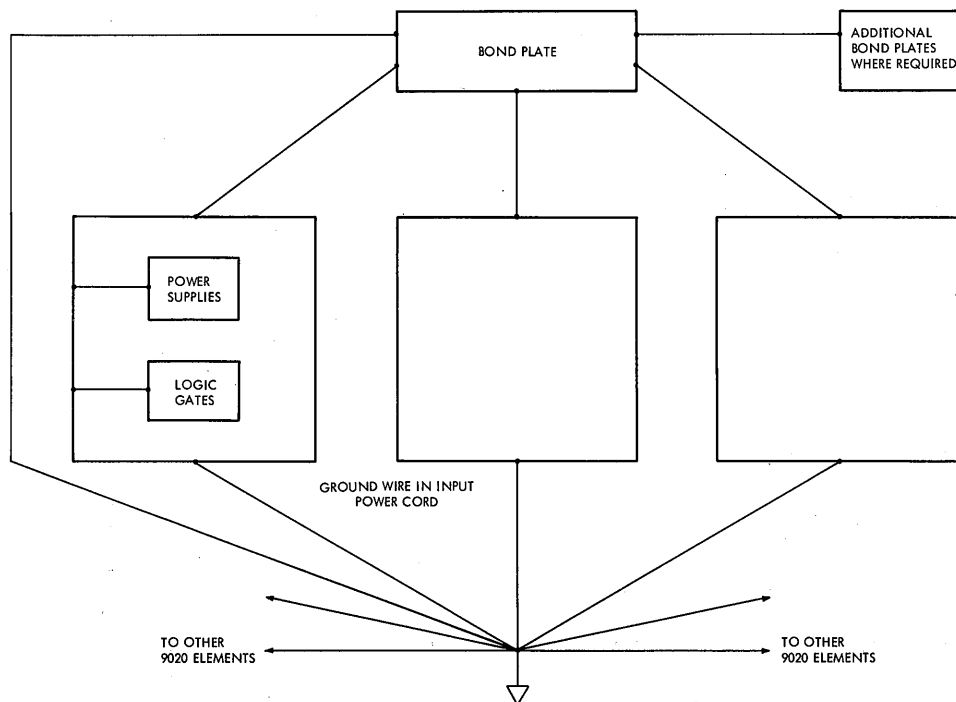


EACH ELEMENT RECEIVES AN ADDITIONAL WIRE IN THE POWER CORD TERMED GROUND WIRE. THE GROUND WIRES FOR ALL ELEMENTS SHOULD
ORIGINATE AT THE SAME POINT IN THE BUILDING GROUND SYSTEM.  THE PURPOSE OF THIS GROUND IS TO MAINTAIN ALL FRAME MEMBERS,COVERS
AND METALLIC (NON LOGIC) COMPONENTS WITHIN A SINGLE ELEMENT AND BETWEEN ALL ELEMENTS AT A COMMON POTENTIAL.  THIS GROUND
IS A PERSONNEL SAFETY MEASURE ONLY.

Figure 14-45.  9020 Element Metal (Non-Logic) Component

9020 ELEMENT A          9020 ELEMENT B

9020 ELEMENT C
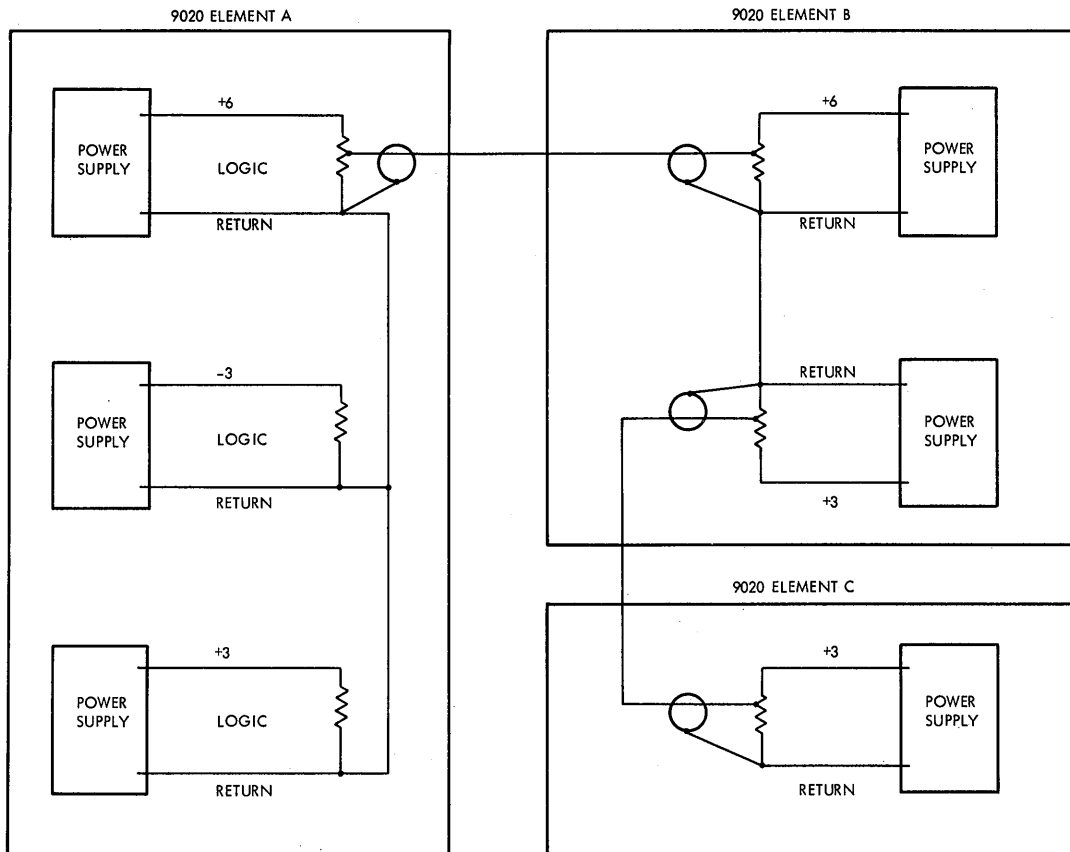
THE SIGNAL SYSTEM CONSISTS OF COAX SIGNAL WIRES, COAX SHIELDS AND POWER SUPPLY RETURNS.
THE FOLLOWING CONDITIONS APPLY.

1. ALL POWER SUPPLY RETURNS WITHIN AN ELEMENT ARE TIED TOGETHER.
2. COAX SHIELD IS USED TO TIE THE RETURNS OF ALL ELEMENTS TOGETHER.

Figure 14-46.   Signal System

SYSTEM GROUNDING AND BONDING

An earth ground is required at the computer distribution panel.
This wire shall be carried directly back to the service ground or
suitable building ground.  Conduit must not be used as the only
grounding means.  No neutral wire is to be used.  From this central
point, individual ground wires accompany the three-phase wires
through the under-floor receptacle to each element of the 9020
System (Figure 14-45).  This is actually a safety ground wire and is
tied directly to the frame of the element.  In order to reduce the
ground circuit impedance caused by the length of ground wires, a
bonding system is also used.  The bonding system is connected to the
ground system at a central point.

14-48
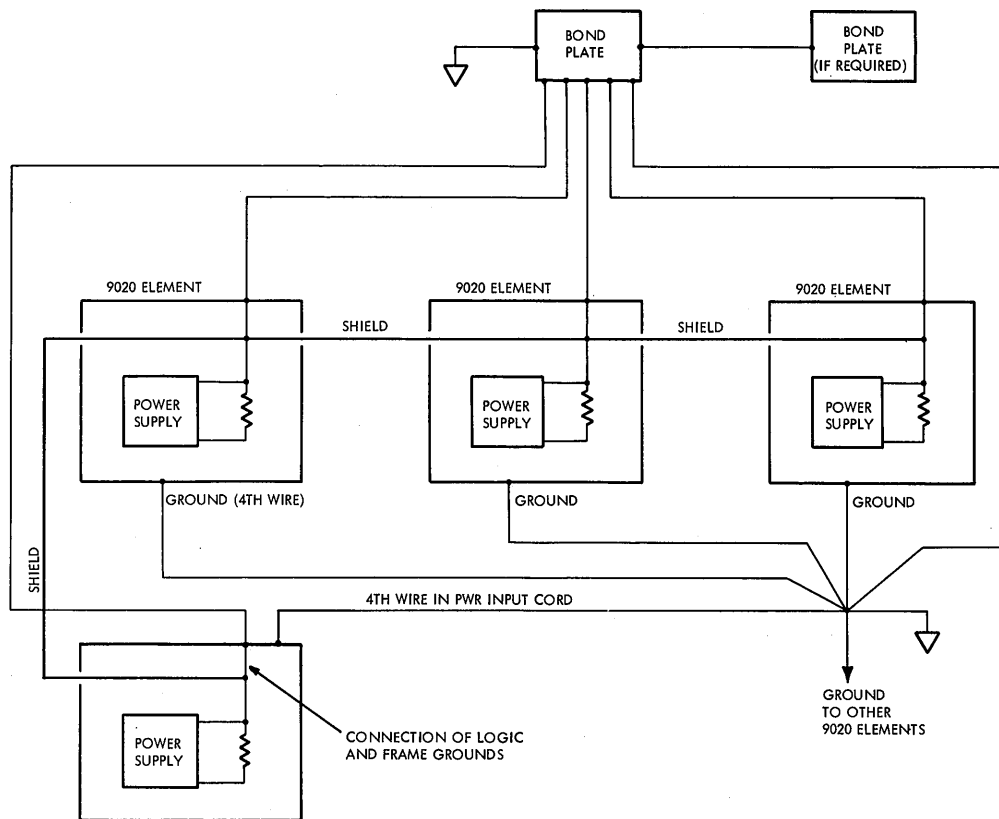
Figure 14-47. Simplified 9020 Internal Ground and Bond System

Signal reference between elements is accomplished through coax shielding (Figure 14-46).

The signal ground is connected to frame ground in the following 9020D/E system elements:  CE, SE, DE, IOCE, PAM, SCU, CC, SC, DAU, and 2821 models 1 and 2.  In addition the TCU connection is established through each interconnected tape unit.

Figure 14-48 shows two types of external device connections to/ from the 9020D/E system.

Because of the many variables to be considered, it is not possible to determine the final ground configuration at this time. This must be developed on site when the system is all tied together and operating.

SINGLE LINE

9020 UNIT

POWER SUPPLY

DRIVER OR RECEIVER

COAX

TO EXTERNAL DEVICE

LOGIC GND

FRAME GROUND

BALANCED LINE

9020 UNIT

POWER SUPPLY

DRIVER OR RECEIVER

SHIELD OR DISCRETE WIRE

TO EXTERNAL DEVICE

LOGIC GND

FRAME GROUND

SINGLE OR MULTIPLE TWISTED PAIR
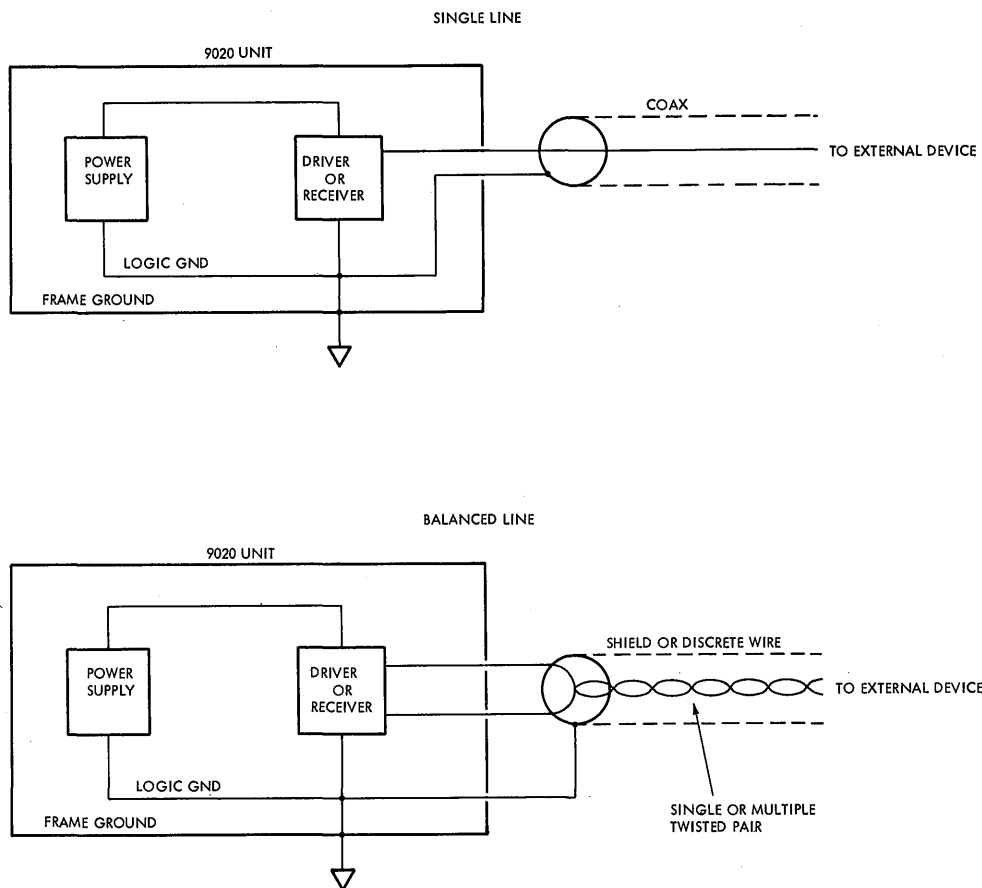
Figure 14-48.  9020 Device Grounding

VENTILATION

The cooling units used in the 9020 System are of two types; Muffin style propeller fans and duplex centrifugal blowers.  The fans and blowers are mounted in a detachable header assembly.  This assembly can be quickly removed from the gates by operating a latch and dis- connecting the power cable.  Air filters are installed on the bottom and the outside of the header assembly.  Power supply cooling is self-contained.  Each inverter/converter contains a muffin style fan.

    The air intake varies slightly from one unit to another, but in general, it is through louvers along the bottom edge.  One inch dust filters are included at each air input.  Warm air exhausts

14-50

from the top of each unit.  Ambient floor level air is drawn in to
the blowers to provide equipment cooling; however, there may be
some leakage of air from within the false floor compartment.

The ventilation requirements of each of the elements is listed
in the specification sheets, Figures 14-6 through 14-20.

The nominal internal operating temperature of the elements is
maintained sufficiently below the thermal warning threshold under
normal operating conditions so that the internal temperature with-
out blowers operating during the maximum "on battery" period
(6.5 seconds) will not reach the thermal warning threshold.

Air conditioning requirements and environment, operating and
non-operating are also listed on each of the element specification
sheets.

## APPENDIX A.  APPLICABLE PORTIONS OF "IBM 9020D and 9020E PRINCIPLES OF OPERATION"

The following portions of the "IBM 9020 Principles of Operation" manual as delineated by chapter and section are included as part of Design Data.  Where a section is delineated, all subsections contained therein are also included.  Programming Notes are not included as part of Design Data.

| Chapter | Section | |
|---------|---------|---|
| 2 | 2.1 | Main Storage |
| | 2.2 | Display Element |
| | 2.4 | Arithmetic and Logical Unit |
| | 2.5 | Program Execution |
| | 2.6 | Protection |
| | 2.11.5 | Input/Output Initiation |
| | 2.11.7 | Input/Output Termination |
| 3 | 3.3 | Condition Code |
| | 3.5 | Fixed-Point Arithmetic Instructions |
| | 3.6 | Fixed-Point Arithmetic Exceptions |
| 4 | 4.3 | Condition Code |
| | 4.5 | Decimal Arithmetic Instructions |
| | 4.6 | Decimal Arithmetic Exceptions |
| 5 | 5.4 | Condition Code |
| | 5.6 | Floating-Point Arithmetic Instruction |
| | 5.7 | Floating-Point Exceptions |
| 6 | 6.2 | Condition Code |
| | 6.4 | Logical Operation Instructions |
| | 6.5 | Logical Operation Exceptions |
| 7 | 7.2 | Decision-Making |
| | 7.4 | Branching Instructions |
| | 7.5 | Branching Exceptions |
| 8 | 8.1 | Program States |
| | 8.2 | Storage Protection |
| | 8.3 | Program Status Word |
| | 8.4.5 | Multiple Computing Element Instruction |

FAA EXTERNAL CABLE CONNECTIONS

This section describes the IBM serpent connector and its assembly to
coaxial or twisted pair cables.  Any changes to the connector assem-
blies will be brought immediately to the attention of the FAA.  All
dimensions shown in the accompanying figures are nominal values for
reference purposes only.

General Description

External cables will consist of coaxial or twisted pair cables,
terminated at the ends engaging IBM equipment with "serpent con-
nectors."  (The serpent connector is an IBM design which serves to
interface IBM equipment.)  The cable ends engaging the attached
devices will be terminated by connectors specified by the using
agency.

Manufacturing Facilities for Cable Assemblies

Listed below are cable manufacturers presently known to have equip-
ment an experience in assembling the serpent connector.  These manu-
facturers also are experienced in working with the other general
types of connectors.

> Robinson Technical Products
> 3421 Old Vestal Road
> Vestal, New York
>
> Amphenol Cadre Division
> 20 Valley Street
> Endwell, New York
>
> Ren Electronics
> 755 New Ludlow Road
> South Hadley Falls, Mass.

Serpent Connector

There are variations of the serpent connector.  The connector to be
used in a specific application is governed by the mating connector
on the IBM equipment.  Connector kits may be furnished to the device
contractors as GFE.

Serpent connectors are available in two types:  Type A; and
type B.  The A and B types are complements to each other -- some-
what analogous to plugs and sockets in commonly used connector
assemblies.  In the case of the serpent connector system, it would
be physically possible to couple two connectors of the same type;

however, in this event, corresponding contact positions would not engage. (For example, position B2 would engage position D-2 etc.) The Type B block, therefore, has contact identifications which are a mirror image of identifications on the Type A block. To facilitate identification, the Type A block is light grey in color, and the Type B block is dark grey.

Twenty-four or forty-eight individual pin positions (serpent contact) are provided for in the connector blocks. Application of the connector is limited only by the number of coaxial or twisted pair (discrete wires) wires used and the method required to terminate the grounds (shields).

When coax cable is terminated in either the 24- or 48-position type A or B serpent connector, the grounds can be either commoned in groups, or separate.

Figure B-1 is an example of where grounds are commoned in a 24-position connector; Figure B-2, where the grounds are separately terminated in a 48-position connector.

Figure B-3 describes the termination of coax cable where the grounds are commoned in groups of five; Figure B-4 depicts the orientation of the wires within the connector.

Figure B-5 describes the termination for coax cable where the grounds are separate; Figure B-6 depicts the orientation of these wires within the connector.

When twisted pair (discrete wires) are terminated into serpent connectors, the method for terminating the grounds must be determined and the proper contacts selected. Table B-1 lists the IBM serpent contact available for the range of wire size applicable.

Figure B-7 describes how individual and multiple wires are terminated.

Serpent Connector Assembly

The following items provide information regarding assembly and handling of the serpent connector system.

Crimped terminations are used on the contacts. Crimping tools compatible with the contact design must be used to insure a reliable termination, and to avoid damage to functional portions of the contact. (Soldered terminations are not recommended for this contact.) Proper crimping facilities for the IBM serpent contact system are available from the IBM Corporation.

Contacts for the wire ranges can be distinguished by examining the "U" shaped section which accepts the conductor. This section on the #24-#26 contact has a height of .070"; on the #26-#29 contact, the height is .042".

If requirements for spare contacts arise, they are available from IBM under Part Nos. 5362301, 5362302, and 5404480. These con-
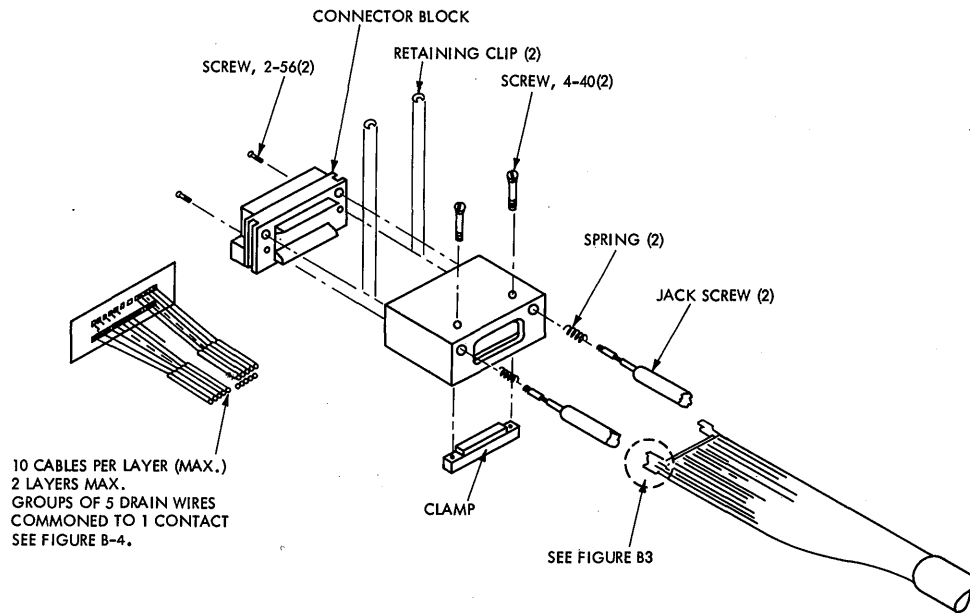
B-2

CONNECTOR BLOCK

SCREW, 2-56(2)   RETAINING CLIP (2)

SCREW, 4-40(2)

SPRING (2)

JACK SCREW (2)

10 CABLES PER LAYER (MAX.)
2 LAYERS MAX.
GROUPS OF 5 DRAIN WIRES
COMMONED TO 1 CONTACT
SEE FIGURE B-4.

CLAMP

SEE FIGURE B3

| BLOCK POSITION | | |
|---|---|---|
| NO. | LETTER | |
| | B | D |
| 2 | ⊙ | - |
| 3 | ⊙ | ⊙ |
| 4 | ⊙ | ⊙ |
| 5 | ⊙ | ⊙ |
| 6 | ⊙ | ⊙ |
| 7 | - | ⊙ |
| 8 | ⊙ | - |
| 9 | ⊙ | ⊙ |
| 10 | ⊙ | ⊙ |
| 11 | ⊙ | ⊙ |
| 12 | ⊙ | ⊙ |
| 13 | - | ⊙ |

SYMBOL IDENTIFICATION
- SHIELD LEAD
⊙ CENTER CONDUCTOR

•Figure B-1.   24 Position (Type A or B) Connector Assembly

tacts cover the range of solid or stranded wire sizes listed in
Table B-1.  Wire combinations can be terminated as indicated.

Contacts may be removed from the connector block by use of a
smooth instrument, suitable for depressing the retaining lug.
(Scratches on functional surfaces of the contact must be avoided.)
A readily available instrument, suitable for occasional usage, is
the #12 "Boye" crocheting needle.

Contact removal, or mishandling of the contact, can cause de-
formation of the retaining lug.  The .025" plus .015" minus .000"
reference dimension shown in Figure B-8 must be maintained to insure
contact retention.  The lug may be reformed to comply with this
dimension.  It is especially important that the position of the
retaining lug be checked in cases where a contact is removed and
then reinstalled in the connector block.

Screw 4-40 x 1 (2)    Retaining Clip    Screw 4-40 x 1 (4)

Cover

Spring

Screw

10 Sig
10 Gnds    Connector
Block

Clamp (2)

See Fig. B-5

See Fig. B-6
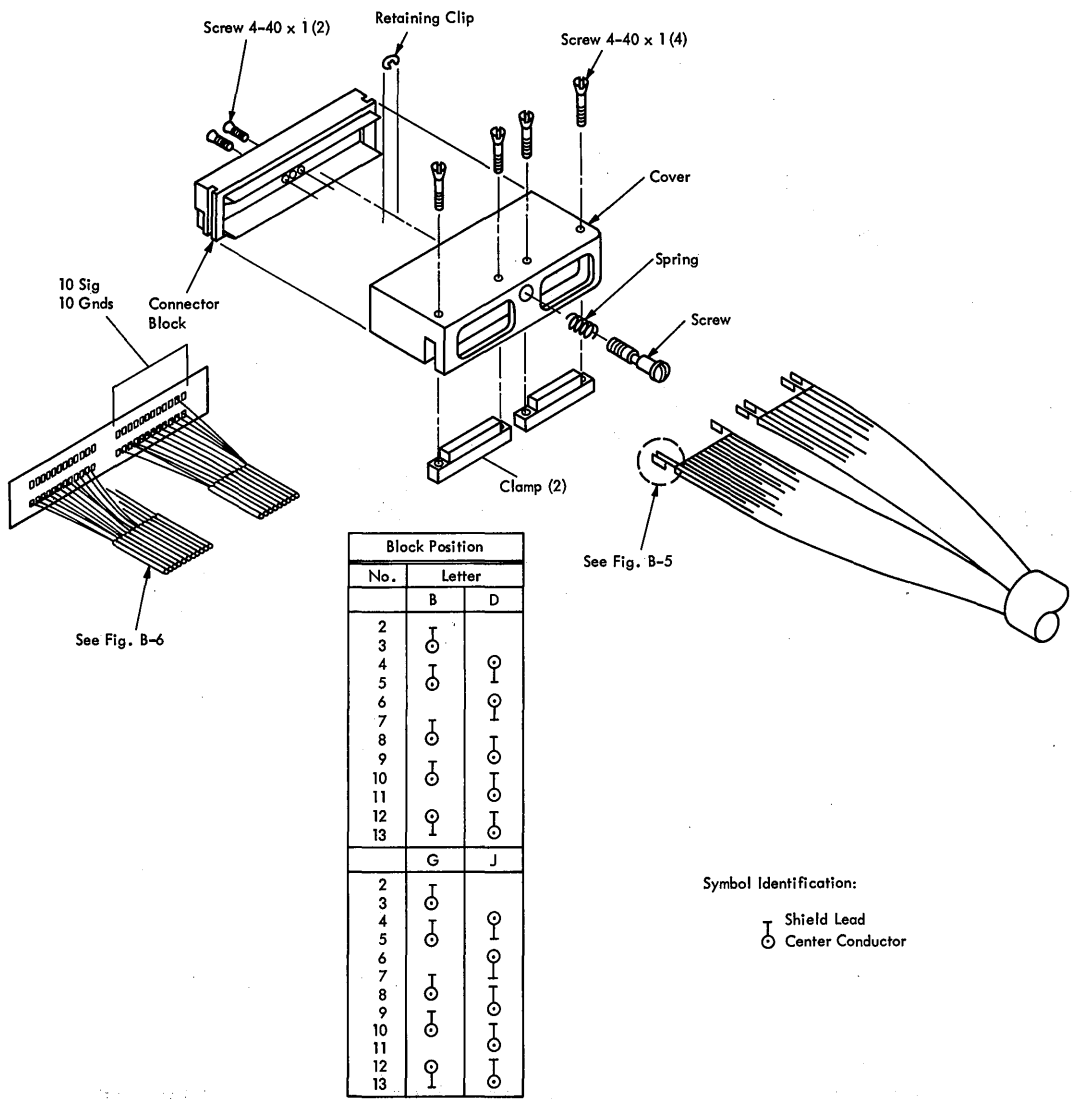
| Block Position | | |
|---|---|---|
| No. | Letter | |
| | B | D |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | | |
| 12 | | |
| 13 | | |
| | G | J |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |
| 11 | | |
| 12 | | |
| 13 | | |

Symbol Identification:

Shield Lead
Center Conductor

●Figure B-2.   48-Position (Type A or B) Connection Assembly

2.25 — #29 DRAIN WIRE
CENTER CONDUCTOR
COAX–CENTER CONDUCTOR
AND DRAIN WIRE
1.54
.14
TUBING
.38
.015
CONTACT 5362301
TUBING
NOTE
.875
CONTACT 5362301
TUBING SPAGHETTI
.88
.25
.50

NOTE: GROUPS OF 5 DRAIN WIRES ARE TO BE
COMMONED INTO 1 CONTACT, E. G.,
B2, B3, B4, B5, B6 TO POSITION B7; B8,
B9, B10, B11, B12 TO POSITION B13; D3,
D4, D5, D6, D7 TO POSITION D2; D9,
D10, D11, D12, D13 TO POSITION D8.
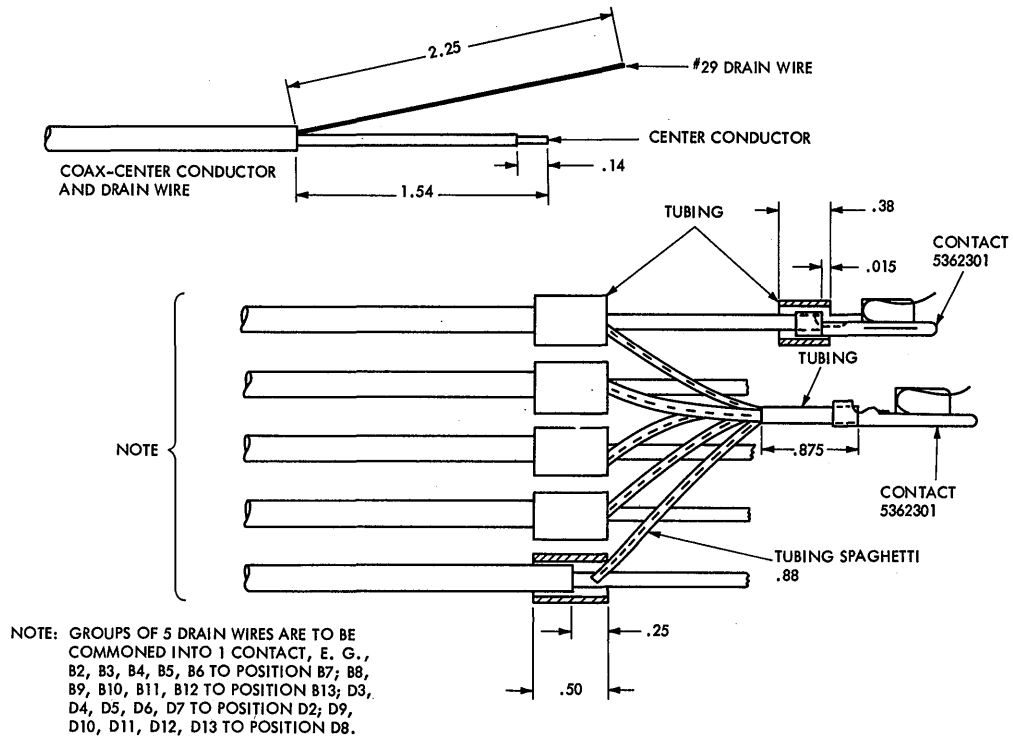
● Figure B-3.   24-Position Connector (Coax Cable) Terminations, Grounds
Commoned in Groups of Five

WIRES SHOULD BE ORIENTED PARALLEL AS SHOWN
(WIRES SHOULD NOT CROSS INSIDE COVER)
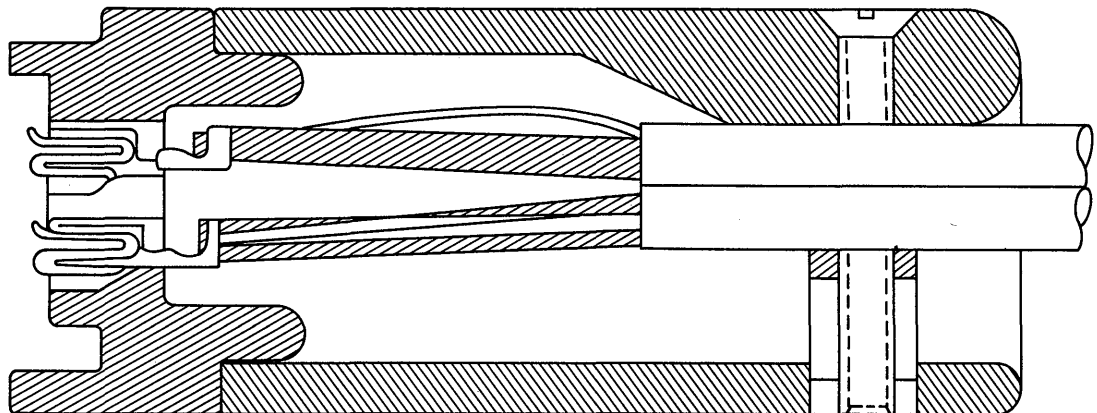


│Figure B-4.   24-Position Connector Wire Orientation

1.75

.15

1.55

Coax Line
No. 26 Center Conductor
No. 29 Drain Wire

.015

1.65

Insulating Tubing

.015

.15

Tubing (Large)

.25

.25

Tubing (Small)
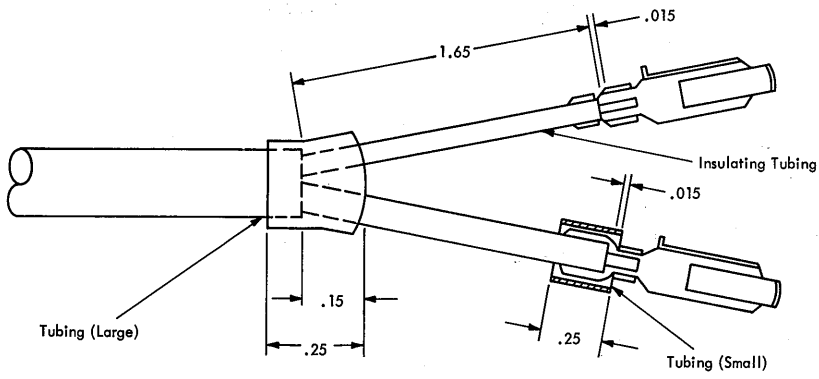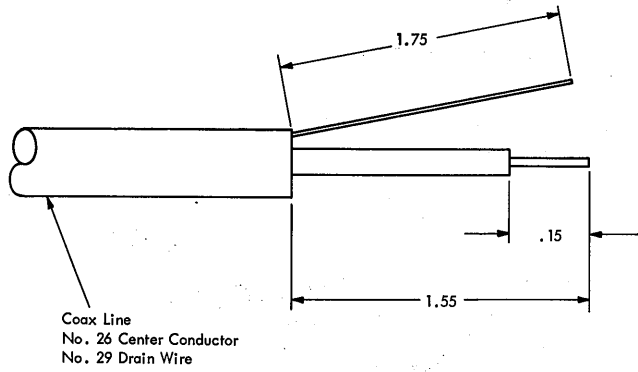
•Figure B-5.   48-Position Connector (Coax Cable) Terminations,
Separate Grounds

Wires Should be Oriented Parallel as Shown
(Wires Should not Cross Inside Cover)
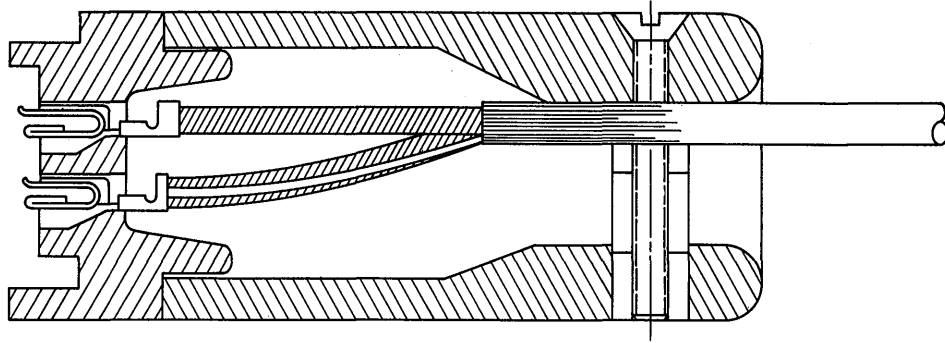


•Figure B-6.   48-Position Connector Wire Orientation

Table B-1.. Wire Terminations

| Terminating Individual Wires | Contact | Terminating Multiple Wires | Contact |
|---|---|---|---|
| #22 Solid & Stranded | 5362301 | Two #24 Solid | 5404480 |
| #24 Solid & Stranded | 5362301 | Two #24 Stranded | 5404480 |
| #26 Solid & Stranded | 5362301 | Two #26 Solid | 5362301 |
| #29 Solid | 5362302 | Two #29 Solid | 5362302 |
| #30 Solid | 5362302 | Two #30 Solid | 5362302 |
| #18 Solid & Stranded | 5404480 | Five #29 Solid | 5362301 |
| #20 Solid & Stranded | 5404480 | Ten #29 Solid | 5404480 |
| #32 Solid | 5362302 | Two #22 Solid | 5404480 |
| | | Two #22 Stranded | 5404480 |
| | | 20 & 24 Solid | 5404480 |
| | | 20 & 24 Stranded | 5404480 |

.015

Tubing

.38

TERMINATING INDIVIDUAL WIRES

.015

Tubing

.38

TERMINATING MULTIPLE WIRES

.19
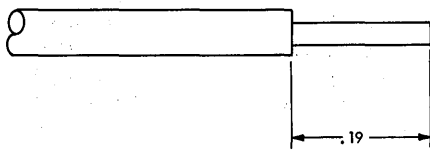
CONTACT END

●Figure B-7.  Serpent Terminations, Discrete Wiring

Mishandling of the contact can also cause a change in the contact gap. The .028" plus or minus .004" reference dimension in Figure B-8 represents the correct spacing.

The tubing, noted in Figure B-3 is dilated by soaking in toluene before installation.

To guard against damage to contacts during shipment and installation of cables, connectors should be provided with suitable protection.

Improper handling during assembly of the coax cable connectors can result in breakage of drain wire leads. A satisfactory repair for such breakage can be effected by terminating the shield with an insulated shield terminator (example: AMP Part No. 328839) and a lead of #26 insulated wire. The serpent contact would in turn be terminated to this lead.

.028 ±.004
(REF)

.025 + .015
      - .000
(REF)
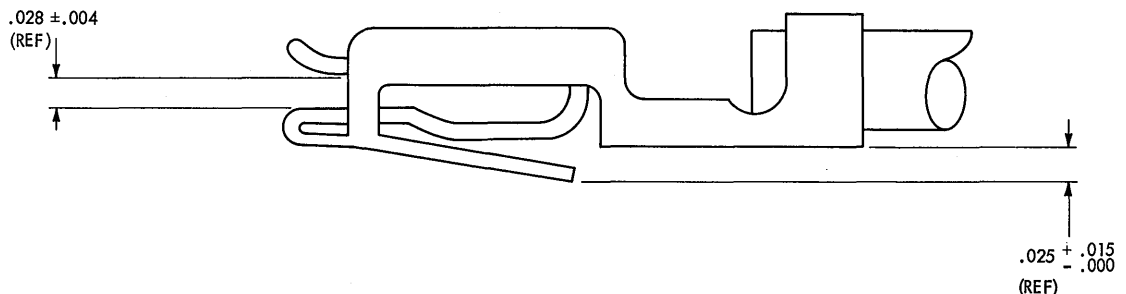
Figure B-8. Serpent Contact Tolerances


Serpent Connector Applications (External Interfaces)

The following are applications where IBM serpent connectors are used to engage external (GFE) cable interfaces.

PAM Connectors

The connectors used for the cables plugging into the PAM are 24-position connectors: Type A and Type B. Type A is used on the input to the PAM's. Type B is used on the output of one PAM which connects to the input of another PAM.

Configuration Console Connectors

The connectors used for cables plugging into the Configuration Console are 24-position connectors. The Type B connector is used on the Configuration Console end of the cable.

## Data Adapter Unit Connectors

The connectors used for cables plugging into the Data Adapter Unit are 48-position connectors. The Type B connector is used on the Data Adapter end of the cable.

## Display Element Connectors

The connectors used for cables plugging into the Display Element are 48-position connectors. The Type B connector is used on the Display Element end of the cable.

## 24 Position Type A/B Coax Cable Connector Kits

A kit for the 24-position connector, Type A or B, containing the items required to terminate one end of a 20-coax cable is available under the following identification:

5393058    NSN 9235-00-398-1065          *New Numbers*
PN 5393087    Connector Kit, 24-Position, Type A    *8-29-83*
PN 5402250    Connector Kit, 24-Position, Type B
5402059    NSN 9259-00-357-5889

The contents of the 24-position Type A connector kit (Part #5393087) are as follows:

| Quantity | Description |
|----------|-------------|
| 24 | Contact, IBM P/N 5362301 |
| 1 | Cover, Connector |
| 1 | Block, Connector Housing Type A (Light Grey) |
| 2 | Screw, Jack |
| 1 | Clamp, Cable |
| 2 | Spring, Compressing |
| 2 | Screw, Flat Head, 4-40 x 1 inch |
| 2 | Clip, Retaining |
| 2 | Screw, Flat Head, 2-56 x .5" |
| 9 Inches | Tubing |
| 11 Inches | Tubing |
| 19 Inches | Tubing, Insulating |
| 4 Inches | Tubing |

A kit for the 24 position connector Type B is available under the following identification:

Part #5402250 - Connector Kit, 24-position, Type B

The contents of the kit are identical to those for the 24-position Type A connector, except the connector block is dark grey in color and the pin identification is reversed as previously described.

The same 24 position connector kits can be used to terminate twisted pair cables provided that the wire size is compatible to the serpent contacts supplied. Refer to Table B-1 for determining the contact size required.

48 Position Type B Coax Cable Connector Kit

A kit for the 48 position connector, type B, containing the items required to terminate one end of a 20-coax cable is available under the following identification:

   P/N 5393223 Connector Kit, 48-Position, Type B

   The contents of the 48 position Type "B-" connector kit are as follows:

| Quantity | Description |
|---|---|
| 40 | Contact, IBM P/N 5362301 |
| 1 | Cover, connector block |
| 1 | Block, connector housing "B" style less insert (dark grey) |
| 2 | Clamp, cable |
| 6 | Screw, flat head, 4-40 x 1 inch |
| 11 inches | Tubing, (large) |
| 9 inches | Tubing, (small) |
| 36 inches | Tubing, insulating |
| 1 | Screw, special binding head |
| 1 | Clip, retaining |
| 1 | Spring, compression |

   The same 48 position, Type B, connector kit can be used to terminate twisted pair cables provided that the wire size is compatible to the serpent contacts supplied. Refer to Table B-1 for determining the contact size required.

CHARACTERISTICS OF COAX CABLE

The characteristics of bulk coax cable (IBM #5353913) and the coax wire used therein (IBM #5353912) are described in Figures B-9 and B-10. IBM has determined that the coax cable may be purchased from the following vendors:

   1. Brand-Rex, Willimantic, Connecticut

   2. Montrose Products, Worcester, Massachusetts

   3. Essec Wire, Chicago, Illinois

   The flat cable impedance matches that of the coax cable. Connectors represent insignificant DC resistance. Impedance mismatch resulting from connectors is compensated for when establishing circuit noise parameters.

## Bulk Cable, 20 Line, Coaxial

The bulk cable (IBM Part Number 5353913) contains 20 coaxial lines encased in a plastic jacket. Each coaxial line incorporates a "drain wire" in contact with the shield to facilitate termination to the serpent connector system. Detail characteristics of the cable and sources of supply are listed in this Appendix.
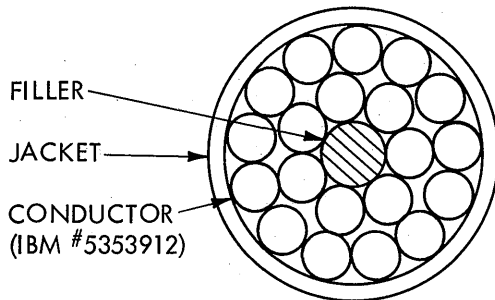


CONDUCTOR – 20 EACH WIRE-COAX (IBM #5353912)

FILLER          – PVC

WRAPPER         – MYLAR (.001 INCH)

JACKET          – PVC (.085 INCH MINIMUM WALL THICKNESS)

      TENSILE STRENGTH – 1800 PSI MINIMUM

      ELONGATION      – 200% MINIMUM

      HARDNESS        – SHORE A 85 ±5

      FINISH          – SMOOTH

CABLE O.D.    – .978 ±.04 INCH

Figure B-9.   Cable, Coax-20 Conductor (5353913)
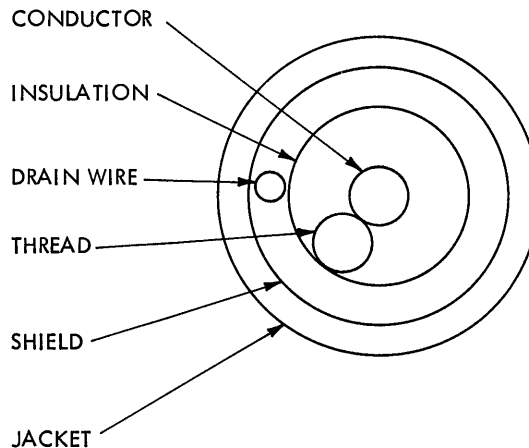
| CONDUCTOR | - #26 AWG SOLID COPPER, SILVER PLATED |
|---|---|
| THREAD | - RULAN (.025 INCH) 0.50-INCH LAY |
| INSULATION | - RULAN (.018 INCH MINIMUM) |
| DRAIN WIRE | - #29 AWG SOLID COPPER, SILVER PLATED, SPIRAL WRAP, 0.50-INCH LAY |
| SHIELD | - 7 ENDS #38 AWG TINNED COPPER, 16 CARRIERS, 14 PICKS PER INCH |
| JACKET | - PVC (.015 MINIMUM WALL THICKNESS) |
| OUTSIDE DIAMETER | - .155 +.005 INCH MEASURED OVER DRAIN WIRE |

| ELECTRICAL CHARACTERISTICS | - CAPACITANCE | - 13.5 PF PER FOOT |
|---|---|---|
| | CHARACTERISTIC IMPEDANCE | - 95 ±3 OHMS |
| | ATTENUATION | - 10 DB PER 100 FEET @ 400 MC |
| | VELOCITY OF PROPAGATION | - 83% |
| | DC RESISTANCE | - 52 OHMS (MAX.) PER 1000 FT (CONDUCTOR) |
| | | 100 OHMS (MAX.) PER 1000 FT (DRAIN WIRE) |

NOTE: FINISHED WIRE MUST WITHSTAND 10 TURNS AROUND A 1.00-INCH MANDREL, THEN REWRAPPED 10 TURNS IN THE OPPOSITE DIRECTION. WRAPPING MUST NOT DAMAGE DRAIN WIRE OR CAUSE VISUAL PROTRUSION THRU OUTER JACKET.

Figure B-10.  Wire, Coax (IBM No. 5353912)

The following is an example of the microprogram control required to perform a machine instruction.  The instruction chosen is an Add which will add a 32-bit binary word from storage to a 32-bit word in a General Register and place the sum in that General Register. Indexing is used in computing the storage address.  The instruction will take the form:

$$(RX) \qquad 5A \qquad R_1 \qquad X_2 \qquad B_2 \qquad D_2$$

Where:   5A is the Op Code

$R_1$ specifies the General Register whose contents will be added to the word from storage and which will receive the sum.

$X_2$ defines the Index Register to be used.

$B_2$ defines the Base Register to be used.

$D_2$ is the Displacement Address.

Each micro-instruction represents a 0.2-usec machine cycle.  Figure C-1 shows machine actions.  Only major actions are shown.

The first micro-instruction related to this instruction occurs as part of the previous instruction executed.  Since instructions are fetched by doublewords, the Q register may contain up to four instructions at a time.  Consequently, the address calculation for the second operand of the 5A instruction may be initiated early by accessing the $B_2$ field of the next instruction in the Q register.

Micro-instructions 1 and 2 provide a common RX format I-fetch when $X_2 \neq 0$ and $B_2 \neq 0$.  These instructions compute the address of the second operand and make a storage request.  Additionally, the next instruction is accommodated by updating the instruction counter and placing the first halfword of the next instruction in the R register for prefetching of operands.

The next three micro-instructions provide a common fixed point operand fetch operation.

The sixth micro-instruction is the execute cycle for a fixed point Add instruction.  The results are placed in local store and exceptional conditions are tested.

The final micro-instruction for Op Code 5A is a common End Operation which sets applicable condition codes and provides operand prefetch for the following instruction.

The micropropramming shown in Figure C-1 has been simplified for clarity in presentation. It is representative of the microroutine required to execute a typical machine instruction.

RX FORMAT I FETCH
$X_2 \neq 0$, $B_2 \neq 0$

FIXED POINT OPERAND FETCH

**X**
- NORMAL END OP
  - SET CONDITION CODES
  - IF NEXT INSTRUCTION IS RX, FETCH $B_2$ FROM LOCAL STORE (PER Q-REG)* AND PLACE IN T REGISTER.

BRANCH PER
FORMAT TYPE OF NEXT
INSTRUCTION
(E.G. RX)

**1**
- ADD $D_2$ (FROM Q-REG)* AND $B_2$ (FROM T-REG) THROUGH PAL AND PLACE RESULT ($D_2 + B_2$) IN B-REG.
- FETCH $X_2$ FROM LOCAL STORE (PER E ** AND PLACE IN T-REG.
- UPDATE IC PER CURRENT INSTRUCTION FORMAT AND VALUE OF IC 21, 22.
- MOVE FIRST HALFWORD OF NEXT INSTRUCTION FROM Q-REG TO R-REG.
- CHECK FOR EXCEPTIONAL CONDITIONS

**2**
- ADD $X_2$ (FROM T-REG) AND $B_2 + D_2$ (FROM B-REG) THROUGH PAL AND PLACE IN D-REG.
- MAKE STORAGE REQUEST PER D-REG.
- FETCH FIRST OPERAND $R_1$ FROM LOCAL STORE (PER E-REG)** AND PLACE IN T-REG.
- PLACE CURRENT OP CODE (BITS 2-7) IN ROA FOR BRANCH TO FIXED POINT OPERAND FETCH.

BRANCH PER
TYPE OF OPERATION
(E.G., FIXED POINT)

**3**
- MOVE FIRST OPERAND FROM T-REG TO B-REG.

**4**
- WAIT CYCLE FOR RECEIPT OF SECOND OPERAND FROM STORAGE

**5**
- RECEIVE DOUBLEWORD FROM STORAGE. SELECT 2ND OPERAND WORD PER D AND PLACE IN T-REG.
- PLACE CURRENT OP CODE (BITS 4-7) IN ROA FOR BRANCH TO. ADD EXECUTE.

(6)

OP CODE
5A EXECUTE

END OP

**6**
- ADD FIRST OPERAND (FROM B-REG) TO SECOND OPERAND (FROM T-REG) THROUGH PAL AND PLACE RESULT IN T-REG.
- PLACE RESULT IN LOCAL STORE (PER E-REG.) **
- CHECK FOR OVERFLOW OR ZERO RESULT AND SET STATS.

**7**
- NORMAL END OP
  - SET CONDITION CODES.
  - PREFETCH OPERANDS OR $B_2$ FOR NEXT INSTRUCTION IF REQUIRED.

(6)

Figure C-1. Microprogram Control of Add Instruction

INITIAL CONDITIONS (EXAMPLE)

*Q-REGISTER

| 5 A | $R_1$ | $X_2$ | $B_2$ | $D_2$ | NEXT INSTR |
|-----|-------|-------|-------|-------|------------|

0                                                              63

**E-REGISTER

| 5 A | $R_1$ | $X_2$ |
|-----|-------|-------|

0              15

## APPENDIX D. INPUT/OUTPUT INTERFACE, CHANNEL TO DEVICE CONTROL UNIT

PREFACE

The I/O Interface - Channel to Device Control unit is a communication link between Input Output Control Element (IOCE) Channels and the device control units in the IBM 9020 System. It provides a common information format and sets of signal sequences as well as a uniform means of attachment for the operation of the various types of control units and the use of their attached devices.

Information, in the form of data, status and sense information, control signals and I/O device addresses, is transmitted in both directions over the 31 time and function-shared lines of the interface. The rise and fall of signals transmitted over the interface are interlocked with their corresponding response, making the interface applicable to a wide variety of circuits and data rates and permitting the connection of control units of different circuit speeds.

The functional interface description that follows is a generalized description which applies equally to the operation of Control Units attached to either the Selector Channels or the Multiplexor Channel of the IOCE. Selector channel operations are conducted in "burst" mode, with data transfer to or from one device being continuous until the operation is terminated either by the device or by the channel. Multiplexor channel operations are normally conducted in "multiplex" mode with addresses, commands, status and sense information and data transfer to and from more than one device being interleaved to initiate, maintain and terminate simultaneous multi-device operations. In either case, the information formats are the same. The signal interlocking requirements are unchanged; the signal sequences differ only as necessary to establish interleaved communication as opposed to continuous operation. The multiplexor channel will operate in "Burst" mode only when the attached control unit forces this operation.

This document also provides electrical, mechanical, and cabling considerations and specifications for the interface. It does not define the interfaces between control units and I/O devices.

Those portions of this appendix that make reference to the number of Control Units that may be attached to an I/O Channel or to lengths of interconnecting cables that may be attached thereto are presented in the context of 'technical capability' of the I/O channel. It is not intended nor should it be inferred that this information shall constitute a commitment for IBM to provide a specific quantity of Control Units and/or Cables for operation on the I/O Channels of the 9020 System.

INTRODUCTION

Scope

This document defines the functional and electrical requirements
for the input/output interface connecting the selector and multi-
plexor channels of the IOCE and I/O device control units.

Objectives

The objective of this document is to establish a uniform means of
communicating control information and data between I/O equipment
and the selector and multiplexor channels of the IOCE.

FUNCTIONAL DESCRIPTION

Input/output devices provide external storage, and a means of com-
munication between data processing systems or between a system and
the external world.

     Input/output (I/O) devices are attached to the Input/Output
Control Element (IOCE) by means of the channels and control units
(Figure D-1 shows several typical connections to the 9020 System).

     The control unit provides the logical capability necessary to
operate and control an I/O device, and adapts the characteristics
of each device to the standard form of control provided by the
channel.  A control unit may be housed separately or it may be
physically and logically integral with the I/O device.

     The I/O device attached to the control unit may be designed
to perform only certain limited operations.  A typical operation
is moving the recording medium and recording data.  To accomplish
these functions, the device needs detailed signal sequences pe-
culiar to that particular type of device.  The control unit de-
codes the commands received from the channel, interprets them
for the particular type of device, and provides the signal
sequence required for executing the operation.

     The channel directs the flow of information between I/O
devices and main storage.

     The connection between the channel and the control unit is
called the I/O interface.  The I/O interface provides an inform-
ation format and a signal sequence that is common to all control
units.  The interface consists of a set of lines that connect a
number of control units to a channel.  Except for the signals
used to establish selection control, all communications to and
from the channel occur over a common bus, i.e., any signal pro-
vided by the channel is available to all control units (see
Figure D-2).  At any one instant, however, only one control unit
can be logically connected to the channel.  Selection of a control
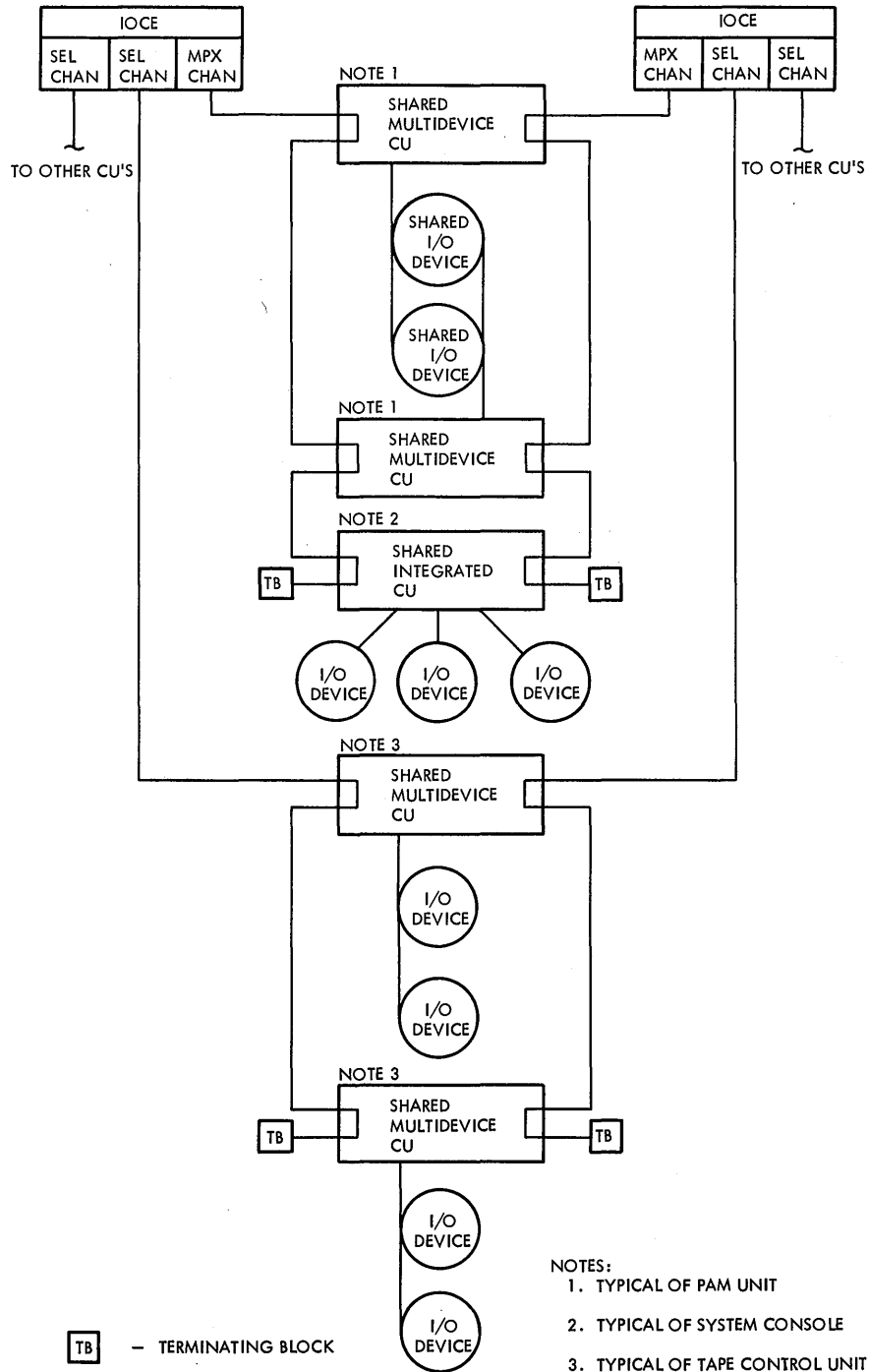
Figure D-1.   Input/Output Interfaces

CHANNEL  HIGHEST-PRIORITY CONTROL UNIT  LOWEST-PRIORITY CONTROL UNIT  SECOND-HIGHEST-PRIORITY CONTROL UNIT  TERMINATOR BLOCK

D DRIVER
R RECEIVER
T TERMINATOR
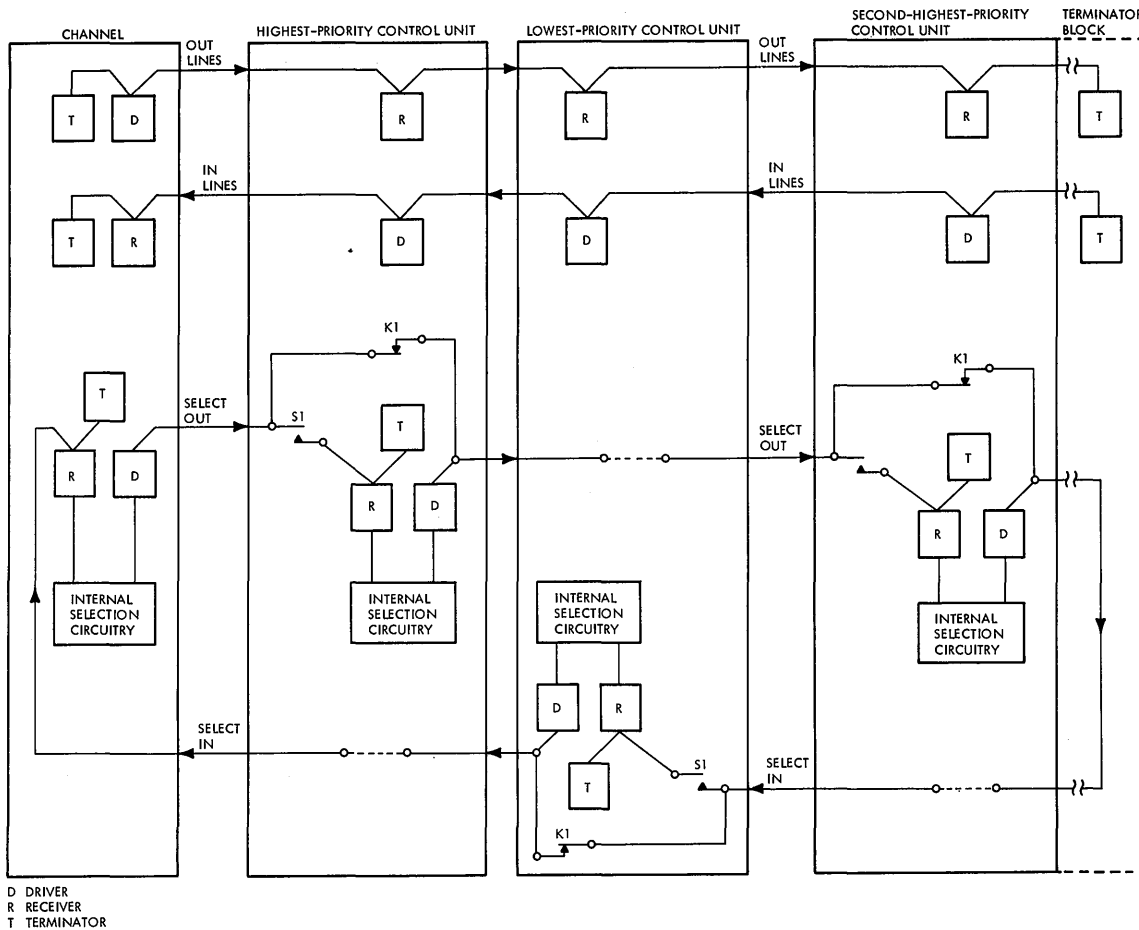
Figure D-2.   Interconnections on the Input/Output Interface

for communication with the channel is controlled by a signal
provided by the channel.  A control unit remains logically con-
nected on the interface until it transfers the information it
needs or has, or until the channel signals it to disconnect.

    The interface can accommodate up to 256 directly addressable
I/O devices (limit set by addressing facilities).  The number of
control units that can be accommodated is limited only by combined
timing and electrical considerations within the given addressing
limitations.

    The multiplexing facilities of the interface permit the
possibility of operating any number of the 256 devices concurrently
on a single interface, i.e., portions of various messages can be
transmitted over the interface in an interleaved fashion to or
from different I/O devices, or the complete message can be trans-
mitted in a single interface operation.  The operation is determined
by the particular channel and the I/O control unit.

D-4

The rise and fall of all signals transmitted over the interface are controlled by interlocked responses.  Interlocking removes the dependence of the interface on circuit speed, and makes it applicable to a wide variety of circuits and data rates.  Furthermore, interlocking permits the connection of control units with different circuit speeds to a single channel.

LINE DEFINITION

The I/O interface connects to a channel with control units.  External cables physically connect all control units in a chain, with the first control unit being connected to the channel.  See Figure D-2.

INPUT/OUTPUT INTERFACE LINES

| NAME OF LINE | ABBREVIATIONS | |
|---|---|---|
| Bus Out Position P | BUS OUT P | |
| Bus Out Position 0 | BUS OUT 0 | |
| Bus Out Position 1 | BUS OUT 1 | |
| Bus Out Position 2 | BUS OUT 2 | |
| Bus Out Position 3 | BUS OUT 3 | BUS OUT |
| Bus Out Position 4 | BUS OUT 4 | |
| Bus Out Position 5 | BUS OUT 5 | |
| Bus Out Position 6 | BUS OUT 6 | |
| Bus Out Position 7 | BUS OUT 7 | |
| | | |
| Bus In Position P | BUS IN P | |
| Bus In Position 0 | BUS IN 0 | |
| Bus In Position 1 | BUS IN 1 | |
| Bus In Position 2 | BUS IN 2 | |
| Bus In Position 3 | BUS IN 3 | |
| Bus In Position 4 | BUS IN 4 | BUS IN |
| Bus In Position 5 | BUS IN 5 | |
| Bus In Position 6 | BUS IN 6 | |
| Bus In Position 7 | BUS IN 7 | |
| | | |
| Address Out | ADR-OUT | |
| Address In | ADR-IN | |
| Command Out | CMD-OUT | |
| Status In | STA-IN | TAGS |
| Service Out | SRV-OUT | |
| Service In | SRV-IN | |
| Operational Out | OPL-OUT | |
| Operational In | OPL-IN | |
| Hold Out | HLD-OUT | |
| Select Out | SEL-OUT | SELECTION CONTROLS |
| Select In | SEL-IN | |
| Suppress Out | SUP-OUT | |
| Request In | REQ-IN | |

The signal lines of the I/O interface consist of an output and an input bus for passing information between the channel and control

units, tag lines for interlocking and for controlling the inform-
ation on the buses, and selection control lines for scanning or
selecting the I/O device.

The signal lines are listed in the table entitled Input/Output
Interface Lines. Note that the names of the lines include the
words OUT or IN. In every case: OUT describes a line which trans-
mits signals to the control units. IN describes a line which
transmits signals to the channel.

The validity of information on the buses and the timing of the
signals on the tag lines is measured at the channel cable connectors.

Buses

Each bus is a set of nine lines consisting of eight information
lines and one parity line. Information on the buses is arranged
so that bit position 7 of a bus always carries the lowest order bit
within an eight-bit byte. The highest order bit is in position 0
and intervening bits are in descending order from position 1 to
position 6.

When a byte transmitted over the interface consists of less
than eight information bits, the bits must be placed in the highest-
numbered contiguous bit positions of the bus. Any unused lines of
the bus must include the low-numbered positions, i.e., position 0
and positions adjacent to it. Unused lines present logical zeros
to the receiving end. The parity bit of any byte must appear in
the parity position (P). The byte must always have odd parity.

Bus Out

Bus Out is used to transmit addresses, commands, control orders, and
data to the control units. The type of information transmitted over
Bus Out is indicated by the outbound tag lines.

1.  When Address Out is up during the channel initiated
    selection sequence, Bus Out specifies the address of the
    device with which the channel wants to communicate.

2.  When Command Out is up during the channel initiated
    selection sequence, Bus Out specifies a command.

3.  When Service Out is up in response to Service In during
    the execution of a write or control operation, the nature
    of the information on Bus Out is dependent upon the type
    of operation. For example, during a write operation it
    will contain data to be recorded by the device. During a
    control operation it can specify an order code or a second-
    level address within the control unit or device.

The period during which information on Bus Out is valid is
controlled by the tag lines. During transmission of the device
address, information on the bus need be valid from the rise of

Address Out until the rise of Operational In, Select In, or in the case of the control-unit-busy selection sequence, until Status In drops. When the channel is transmitting any other type of information, the information on Bus Out is valid from the rise of the signal on the associated outbound tag line until the fall of the signal on the corresponding inbound tag line.

Some skew on Bus Out must be accommodated by the channel. Except as noted in the Address Out discussion, the channel must delay **raising** of the signal on the outbound tag lines by an amount which insures that the information on Bus Out will precede the signal on the outbound tag lines by not less than 100 nanoseconds (nsec) when measured at the cable connectors at the channel under the worst-case skew conditions. The channel thus must provide a delay that accommodates skew caused by its own circuitry and, in addition, must provide a delay of at least 100 nsec. This delay compensates for skew caused by the cable and for most control units, will also be sufficient to accommodate the skew caused by the interface receivers. When a control unit can cause more skew, the control unit must provide the additional delay to eliminate it.

Bus In

Bus In is used to transmit addresses, status, sense information, and data to the channel. A control unit can place and maintain information on Bus In only when its operational-in line is up, except in the case of the control-unit-busy sequence.

The type of information transmitted over Bus In is indicated by the inbound tag lines.

> 1. When Address In is up, Bus In specifies the address of the currently selected device.
>
> 2. When Status In is up, Bus In contains a byte of information describing the status of the device or control unit.
>
> 3. When Service In is up during execution of a read or sense operation, the nature of the information contained on Bus In is dependent upon the type of operation. During a read operation it may contain a byte of data from the record medium. During a sense operation, the bus contains a set of bits describing the detailed status of the device and the conditions under which the last operation was terminated.

The period during which information on Bus In is valid is controlled by the tag lines. Information on the bus must be valid within 100 nsec after the rise of the associated inbound tag and must stay valid until the rise of the responding outbound tag or in a control-unit-busy selection sequence, until Select Out drops. The 100-nsec delay between the rise of the inbound tag and the time the signal becomes valid on Bus In places the responsibility of deskewing Bus In on the channel. The channel must provide a delay in the

inbound tag lines which accommodates skew caused by the channel
circuitry including its receivers and, in addition, must provide a
delay of at least 100 nsec. This delay will compensate for skew
caused by the cable, and for most control units, the skew caused by
their drivers. This delay will provide sufficient time to deskew
the information so that the inbound tag can be raised by the control
unit at the same time information is placed on the bus. When a
control unit and cable can cause more skew than can be accommodated
by a 100 ns delay, the control unit must provide the additional
delay to eliminate it.

Operational Out

Operational Out is a line from the channel to all attached control
units and is used for interlocking purposes. Except for the suppress-
out line, all lines from the channel are significant only when
Operational Out is up. Whenever Operational Out is down, all in-
bound lines from the control unit must drop and any operation
currently working over the interface must be reset. Under these
conditions, all control-unit generated interface signals must be
down within 1.5 micro-seconds ( sec) after the fall of 'operational
out' at the control unit. (See Selective Reset and System Reset
discussions)

Request In

Request In is a line from all attached I/O control units to the
channel and is used to signal the channel when any control unit has
data or status to be serviced. Request In can be signaled by more
than one control unit at a time.

    Request In must not be signaled before the control unit is
ready to present status information or data. The request-in signal
is removed by the control unit after it gains selection and has no
further data or service requirements. Request In must fall not
later than 250 usec after the fall of Operational In if the sequence
satisfies its service requirements.

    Request In may not be up while Suppress Out is up if the
request is due to a suppressable-type status (see suppress status
discussion). Under these conditions, Request In must fall at the
control unit within1.5 microseconds after the rise of Suppress Out.

Address Out

Address Out is a line from the channel to all attached control units.
It provides two functions:

    1.  Device selection. The address-out line signals the control
        unit to decode the address on Bus Out. The control unit
        recognizing the address must respond by raising its
        operational-in line when its incoming Select Out rises
        (except in the case of Control Unit Busy). The rise of

Address Out precedes the rise of Select Out by a minimum of 400 nsec and follows the placing of the device address on Bus Out by 250 nsec.

Address Out can rise only when Select Out, Select In, and Operational In are down at the channel. Ultimate use of the address on Bus Out at the control unit is timed by the next rise of Select Out at the addressed control unit. The rise of Address Out must be delayed at least 250 nsec after the address is placed on Bus Out. Once Address Out and Select Out are up, Address Out must stay up until either Select In or Operational In rises or until Status In falls in the case of the control unit busy sequence. During device selection, Address Out cannot be concurrently up with any other outbound tag line.

2. Disconnect operations. If either Select Out or Hold Out is down and Address Out is up, the presently connected control unit must drop its operational-in line, thus disconnecting from the interface. Address Out remains up until Operational In drops. Operational In must drop within 6 usec after receiving the disconnect indication. Mechanical motion in process continues to a normal stopping point. Status will be generated and presented to the channel when appropriate (see Interface Disconnect discussion). Address Out, in this case, may be up concurrently with another outbound tag line.

## Control Unit Selection, General

Selection is controlled by the select-out, select-in, and hold-out lines. The select-out and select-in lines form a loop from the channel through each control unit to the cable terminator block (Select Out), again through each control unit back to the channel (Select In). Control unit selection logic may be attached to either the select-out or the select-in line. Since the rise of Select Out is effective only to the first control unit on the line and, if selection is not required, is in turn propagated by each control unit to the next control unit on the line, a selection priority is established. This priority is in a descending sequence from the channel through each control unit with selection logic attached to Select Out followed, in descending order back to the channel, by the remaining control units with selection logic attached to Select In (see Figure D-2).

This document assumes that the selection logic of all control units is attached to the select-out line.

Each control unit must ensure that the process of electrically by-passing 'select out' before power changes does not interfere with the propagation of 'select out'. Each control unit must therefore ensure that 'select out' discontinuities, which may occur when another control unit on the interface is powered up or down, do not affect the propagation of 'select out.' This should be

accomplished by the use of a special latch circuit.  The latch is
turned on by the AND of 'select out', and 'hold out', and is reset
by the fall of 'hold out'.  The circuit is in series with the
remaining selection circuitry in the control unit and provides a
constant 'select out' within the control unit, and therefore to
the following control unit, regardless of variations in the input
'select out' signal.

      The hold-out and select-out lines are AND'ed at the control
unit.  Throughout the following description, the select-out
signal assumes the proper operation of the hold-out signal, i.e.,
the rise of Select Out at the control unit presumes that Hold Out
is up and the fall of Select Out may be the result of the fall of
Hold Out, depending upon the particular channel implementation.

Select Out

Select Out is a line from the channel to the control unit having
highest priority and from any control unit to the control unit next
lower in priority.  This line, together with the select-in, provides
a loop for scanning the attached control units.  A control unit can
raise its operational-in line only at the rise of its incoming
select-out signal.  If a control unit does not require selection, it
must immediately propagate the signal to the next control unit.
Once a control unit propagates Select Out, it cannot raise its
operational-in line or respond with a control-unit busy sequence
until the next rise of the incoming select-out line.

      When an operation is being initiated by the channel, rise of
Address Out must precede the rise of Select Out by a minimum of 400
nsec.

      When the channel is scanning the attached control units, the
select-out line emanating from the channel is normally up.  The
channel must keep the select-out line up until either Select In or
Address In and Operational In or Status In rises.  When Select In
rises, Select Out must drop and may not again rise until after
Select In falls.  A control unit becomes selected only when it
raises its operational-in line (except for the control unit busy
sequence).  Select Out must drop in order that Operational In may
drop.  However, after the drop of Select Out the control unit must
keep Operational In up until the current signal sequence is com-
pleted.  Channels that force burst mode will normally keep the
select-out line up until the end of the operation.  Except for the
interface disconnect sequence, channels that force burst mode keep
'select out' up until the end of the operation.  A rise of the
incoming Select Out in a control unit signals that the control unit
can become selected to the channel by raising the operational-in
line.  If a control unit raises its operational-in line, it must
suppress the propagation of Select Out to the next control unit.
If the control unit does not require selection, it must propagate
Select Out to the next control unit within 1.8  s (See Time-Out
Considerations discussion.)

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Hold Out

Hold Out is a line from the channel to all attached I/O control units
and is used to enable the select-out signal. Only when Hold Out is
up can Select Out be considered active. Hold Out must gate the
select-out signal in the control units. Hold Out can only be up if
Operational Out is up and once Hold Out drops it must not rise for at
least 4.0 microseconds. Hold Out when used, minimizes the propa-
gation of the fall of Select Out.

Select In

Select In is a line which extends the select-out signal from the
cable terminator block (see Figure D-2) to the channel. It provides
a return path (to the channel) for the select-out signal. The
definition of the select-in line is the same as that for a select-
out line emanating from any control unit.

Operational In

Operational In is a line from all attached control units to the
channel, and is used to signal to the channel that a device has been
selected (except for the control-unit-busy sequence). It must stay
up for the duration of the selection. The selected device is
identified by the address byte transmitted over Bus In.

Rise of Operational In indicates that a control unit is selected
and is communicating with the channel. This communication can con-
sist of one or a combination of the following signal sequences:

1. response to address on Bus Out,

2. request for data on Bus Out,

3. offer of data on Bus In, or

4. offer of status on Bus In.

Operational In can rise only when the incoming Select Out to the
control unit is up and the outgoing Select Out is down; i.e., the
control unit must raise Operational In in response to the rise of
Select Out and must block Select Out from emanating to the next
control unit. Operational In can drop only after Select Out drops.

When Operational In is raised for a particular signal sequence,
it must stay up until all required information is transmitted
between the channel and the devices. If Select Out is down,
Operational In must drop after the rise of outbound tag associated
with the transfer of the last byte of information.

With the exception of 'request in', all inbound signals must
be down within 1.5 sec of the fall of 'operational in' at the
control unit.

## Address In

Address In is a line from all attached control units to the channel
and is used to signal to the channel when the address of the
currently selected device has been placed on Bus In.  The channel
responds to Address In by means of Command Out.

The rise of Address In indicates that the address of the
currently selected device is available on Bus In.  See Bus In for
discussion of skew.  Address In must stay up until the rise of
Command Out.  Address In must fall in order that Command Out may
fall.  Address In cannot be up concurrently with any other inbound
tag line.

## Command Out

Command Out is a line from the channel to all attached control units
and is used to signal to the selected device in response to a
signal on the address-in, status-in, or service-in lines.  A signal
on the command-out line as a response to the address-in signal during
the initial selection sequence, indicates to the selected device
that the channel has placed a command byte on Bus Out.  The command
byte has a fixed format (see Commands discussion).

The rise of Command Out indicates that the information on Bus
In is no longer required to be valid and indicates that a command
byte is available on Bus Out.  See Bus Out for discussion of skew.
Command Out must stay up until the fall of the associated address-
in, status-in, or service-in signal.  It cannot be up concurrently
with any other outbound tag line, except during an interface-
disconnect sequence (when Address Out may be up).

A command-out response to Address In means proceed, except
during a channel-initiated selection sequence.  In the case of a
channel-initiated selection sequence, Command Out indicates that
Bus Out defines the operational command to be performed.  A
command-out response to Service In always means stop (see Stop
discussion).  A command-out response to Status In means stack
(refer to Stack discussion).

When Command Out is raised to indicate Proceed, Stack, or Stop,
Bus Out must have a command byte of zero, but need not necessarily
have correct parity.

Bus Out is not checked for parity or decoded by the control
unit during these times.

## Status In

Status In is a line from all attached control units to the channel
and is used to signal the channel when the selected device has
placed status information on Bus In.  The status byte has a fixed
format and contains bits describing the current status at the

control unit. (see Status Byte discussion)  The channel responds
with either Service Out or Command Out, depending upon whether or
not it accepted the status.

The rise of Status In indicates that a byte of status informa-
tion is available on Bus In.  See Bus In for discussion of skew.
Status In cannot be up concurrently with any other inbound tag line.
Status In must stay up until the rise of an out-tag, or in the
control-unit busy selection sequence until Select Out falls.  It
must fall in order that the responding out-tag may fall.  During
the control-unit-busy selection sequence, status on Bus In must be
valid until Select Out falls.

Service Out

Service Out is a line from the channel to all attached control units
and is used to signal the selected device in recognition of a sig-
nal on the service-in or status-in line.  A signal on the service-
out line indicates to the selected device that the channel has
accepted the information on Bus In or has provided on Bus Out the
data requested by Service In.

When Service Out is sent in response to Service In during read,
read backward or sense operations, or to Status In, the service-
out signal must rise after the channel accepts the information on
Bus In.  In these cases the rise of Service Out indicates that the
information is no longer required to be valid on Bus In, and is
not associated with any information on Bus Out.  When Service Out
is sent in response to Service In during a write or control
operation, the rise of Service Out indicates that the channel has
provided the requested information on Bus Out.  In this case, the
signal must rise after the information is placed on the bus.  Ser-
vice Out must stay up until the fall of the associated service-in
or status-in signal.  Service Out cannot be up concurrently with
any other out-tag, except Address Out during an interface-disconnect
sequence (when Address Out may be up).

A service-out response to Status In while Suppress Out is up
indicates to the control unit that the operation is being chained
and that this status is accepted by the channel (see Command
Chaining discussion).

Service In

Service In is a line from all attached control units to the channel
and is used to signal to the channel when the selected device wants
to transmit or receive a byte of information.  The nature of the
information associated with Service In depends upon the operation
and the device.  The channel must respond to Service In by Service
Out, Command Out, or during an interface disconnect, by Address
Out.

During read, read backward, and sense operations, Service In
rises when information is available on Bus In.  During write and

control operations, Service In rises when information is required
on Bus Out.  Service In cannot be up concurrently with any other
inbound tag line.  Service In must stay up until the rise of either
Service Out, Command Out, or Address Out.

When, in the case of cyclic devices, the channel does not res-
pond in time to the preceding Service In, an overrun condition
occurs.  The condition must be recognized by the (cyclic) device.
In any case, Service In must not drop if an out-tag has not risen,
nor may it rise if Service Out has not dropped.

An overrun condition causes the unit-check indicator and the
overrun indicator to be set.  Data transfer will stop after an
overrun condition.  For I/O devices that may overrun, the critical
signal timings involved must be part of the device specifications.

## Suppress Out

Suppress Out is a line from the channel to all attached control units
and is used both alone and in conjunction with the out-tag lines to
provide the following special functions:  Suppress Data, Suppress
Status, Command Chaining, and Selective Reset (refer to applicable
subject discussions for additional information.)

## UNUSED LINES

All line positions shown in the mechanical connector section
including those not defined herein must be carried through the I/O
cables.  All undefined lines must be jumpered directly through the
control units.

Some of the 40 signal lines in the I/O interface are reserved.
(See "Interface Connector Pin Assignments" Figure D3.)

All 40 signal transmission lines, with the exception of 'select
out' ('select in' if low priority), must be carried through the
control units from the IN cable connector to the OUT cable
connector.

## SIGNAL INTERLOCK SUMMARY

The following rules for direct-current interlocking of signals must
be used in the design of channels and control units using the I/O
interface.

1.  Except for Address Out, during the interface disconnect
    sequence, no more than one out-tag may be up at any
    given time.

2.  No more than one in-tag may be up at any given time.

3.  An in-tag may rise only when all out-tags are down,
    except for the control-unit-busy sequence.

4.  An in-tag may fall only after the rise of a responding
    out-tag, except for Status In in the control-unit-busy
    sequence.

5.  The service-out and command-out tags may rise only in
    response to the up-level of an in-tag.

6.  The address-out tag for a channel-initiated selection
    sequence may rise only when the select-in and select-out
    signals are down at the channel.

7.  Once Address Out and Select Out have risen for a channel
    initiated selection sequence, Address Out must stay up
    until after the rise of Select In or Operational In or the
    fall of Status In.

8.  Once the address-out tag has risen for the interface-
    disconnect control sequence it must not drop until
    Operational In drops.

9.  None of the out-lines, except Suppress Out, have meaning
    when Operational Out is down.

10. Select Out can rise only if Operational In and Select In
    are down.

11. Operational In cannot fall until either:

    a.  Select Out falls and an out-tag response is sent for
        the last in-tag of any given signal sequence, or

    b.  Operational Out falls, or

    c.  An interface-disconnect sequence is given.

12. Operational In cannot rise unless Operational Out is up and
    must drop if Operational Out drops.

NOTE:  Logical designers should carefully consider the effects of
interface signal transition times.  Although transition time should
not generally be a problem, some cases may exist, due to wide
variation in circuit tolerance or physically integrated channel
control units, where transition time must be considered.

    The general design rule is that the originating unit (channel
or control unit) must fully recognize the transition of a signal
from one state to the other before any result of the transition is
fed back from the receiving unit.

OPERATIONAL DESCRIPTION

This section contains the description of the detailed signal sequences
for complete I/O operation.  These sequences include initial selec-
tion, data transfers, and ending procedures (Refer to timing charts).

## Initial Selection Sequence

To initiate an I/O operation, the channel places the address of the desired device on Bus Out and then raises the address-out line. Each control unit connected to the channel attempts to decode the address on the bus. To be acceptable, the address must have parity.

The channel then issues the select-out signal, and when the incoming select-out signal appears at the addressed control unit, the control unit blocks its propagation and raises the operational-in line. When Operational In rises, the channel responds by dropping Address Out. After Address Out falls and the unit address is on Bus In, Address In may rise. For a multiplex operation, 'hold out' with 'select out' may drop any time after this point. After the channel checks the address, it responds by placing the command on Bus Out and signaling on the command-out line. The selected control unit processes the command and then drops Address In. After Command Out drops, the control unit places the status information on Bus In and raises Status-In. If the I/O device is available, the status contains a zero status byte. If the channel accepts this status condition, it responds with a Service Out. This signal completes the initial selection phase.

If during this channel-initiated selection sequence the device is found to be operating, the control unit responds with busy status. If the control unit has status outstanding from a previous operation or externally initiated status, it responds with a busy bit,(except to the TEST IO) along with the other status conditions in the status byte.

If the command is rejected by the control unit, for instance, as a result of the detection of an invalid command, the control unit responds with the unit-check status condition. No operation is initiated at the control unit and no ending status will be generated.

An immediate-type command or command-immediate is a command whose execution meets the following requirements:

1. Execution requires no more information than than in the command byte; that is, no data or information bytes are transferred.

2. Channel-end time coincides with initial-status time; and on a normal operation, at least 'channel end' instead of zero status will be in the initial-status byte.

NOTE: A channel response of 'command out' to 'status in' cannot prevent the execution of an immediate command.

## Control-Unit-Busy Sequence

If an I/O device is addressed and the control unit to which it is attached is in a busy state or has status pending for another

device shared on the control unit other than the one addressed, the control unit responds to the channel with a status byte indicating this busy condition (refer to Busy discussion). The control unit can present this status byte in either of two ways: it can respond with status as in the initial selection sequence or it can respond with the control unit busy selection sequence.

NOTE: The control-unit-busy sequence must not be used in response to an initial selection sequence addressed to a device for which chaining has just been indicated.

The control-unit-busy selection sequence begins when the channel places the unit address on Bus Out and then raises the address-out tag. Select Out is then raised. Each control unit attempts to decode the address on Bus Out. When Select Out rises at the addressed control unit, the control unit blocks the propagation of Select Out, places the control-unit-busy status byte on Bus In, and raises the status-in tag. Operational In is not raised. After accepting the status byte, the channel drops Select Out. The control unit responds to the dropping of Select Out by dropping the status-in tag and disconnecting from the interface.

The channel must keep Address Out up until Status In drops, thus completing the control-unit selection sequence.

## Control-Unit-Initiated Sequence

When any control unit requires service, it raises its request-in line to the channel. The next time Select Out rises at any control unit requiring service and no I/O selection is being attempted by the channel (Address Out down), the control unit places the address of the device on Bus In, then signals on both the address-in and the operational-in lines. When the channel recognized the address, a command-out signal is sent to the control unit, indicating Proceed. After Address In drops, the channel responds by dropping the command-out signal.

If the service request is for data, the sequence proceeds as described for data transfer. Control unit initiated selection for data transfer occurs in multiplex mode.

If the service request is for status, the sequence proceeds as defined for the status cycle in the ending procedure.

DATA TRANSFER

Data transfer may be requested by a control unit after a selection sequence (refer to Initial Selection Sequence and Control-Unit-Initiated Sequence discussions). To transmit to the channel, the control unit places a data byte on Bus In and raises Service In; the tag and the validity of Bus In must be maintained until an outbound tag is raised in response. To request data from the channel, Service In is raised, and the channel places the data on Bus Out and signals with Service Out. The channel maintains the validity of Bus Out until Service In falls. After Service In falls the channel responds by dropping Service Out.

## Modes of Operations

After selection, the control unit remains connected to the channel for the duration of the transfer of information. The information can be a single byte of data, a status report, an initiation of a new command, a string of data bytes, or a complete operation from initiation to reception of the final status report.

The duration of the connection is under control of both the channel and the control unit. To provide a channel with a method of controlling the duration of the connection, a control unit cannot disconnect from the interface before Select Out or Hold Out falls. On the other hand, the control unit may preserve the logical connection after the channel permits the control unit to disconnect (Select Out or Hold Out down) by holding up Operational In. In this manner the control unit can force burst mode.

Depending on the duration of the connection, two modes of operation are established: multiplex and burst. If Operational In remains up for longer than the multiplexing time-out limit (see time-out consideration), selection is considered to be in burst mode. If the selection time is less than this time-out, the selection is considered to be in multiplex mode. These modes of operation are established so that the program can schedule concurrent execution of multiple I/O operations.

The multiplex mode is the normal mode for low-speed I/O devices. However, all devices are designed to work in burst mode when required by the channel. Channels which are not capable of operating in multiplex mode force burst mode by holding up the hold-out and select-out signals until the presentation of channel-end status.

The burst mode is the normal mode of operation for high-speed I/O devices. These devices force burst mode (by holding up the operational-in line) when attached to a channel capable of multiplex operation. Medium-speed or buffered devices which may normally work in either mode as determined by channel data-rate capabilities, are equipped with a manual or program switch to select the mode of operation. The switch setting is overridden when burst mode is forced by the channel. An interface-disconnect executed by the channel (see Interface Disconnect discussion) overrides the force-burst-mode condition of a control unit.

## ENDING PROCEDURE

The ending procedure may be initiated by either the I/O device or the channel. If the procedure is initiated by the device, the end of operation is completed in one signal sequence assuming that channel-end and device-end status occur together. If the procedure is initiated by the channel, the device may still require time to reach the point where the proper status information is available, in which case a second signal sequence is necessary to complete the

ending procedure. One of three situations may exist at the
initiation of the ending procedure (assume selection is already
obtained.)

1.  The channel recognizes the end of an operation before the
    device reaches its ending point.

    In this situation, whenever the control unit next requires
    service, the control unit raises the service-in line. The
    channel responds with Command Out, indicating stop. The
    control unit drops Service In and proceeds to its normal
    ending point without requesting further service. When
    the device reaches the point where it normally would send
    Channel End, the control unit places the ending status on
    Bus In and raises the status-in line. The channel responds
    with Service Out, unless it is necessary to stack the
    status.

2.  The channel and the device recognize the end of an opera-
    tion simultaneously.

3.  The device recognizes the end of an operation before the
    channel reaches the end.

For situations 2 and 3 status information is available at the control
unit. The control unit places the ending status on Bus In and
raises the status-in line.

If Device End does not occur with Channel End, it will be
presented when available and an additional status sequence is
required.

Externally Initiated Status

Externally initiated status conditions exist which are unrelated to
any previous program-initiated command. One of these is Attention,
which is normally found on console or communication devices. Another
is Device End which is generated whenever the corresponding device
goes from the not-ready to the ready state.

Externally initiated status conditions are handled in the
same way as any other status information, and are subject to the
same rules as far as presentation to the channel and stacking are
concerned. Externally initiated status must be returned to all
paths as defined by the particular device specifications.

ADDRESSING

An eight-bit address byte (plus parity) is used over the interface
for direct addressing of attached devices. A unique eight-bit
device address is assigned to each device "access path" from any
one channel at the time of installation of a control unit. The
term access path is used since a particular device may be reached
by means of more than one path in some systems or more than one

device may be reached by means of the same path with indirect addressing. Devices may be excepted from this requirement as determined on an individual basis.

At the time of installation, control units may be assigned any required number of device addresses, starting at an address boundary defined as follows:

An address boundary is established by any device address containing zeros in a number of low-order bit positions equal to the number of bits required to decode the maximum number of device access paths needed for the particular control unit.

Input/output control units must be capable of recognizing device addresses under the following rules:

1. Device address must have correct parity.

2. Device addresses will be assigned in sequence to multi-device control units unless the control unit is designed to recognize only the addresses of the devices attached.

3. Any device address from 0 to 255 may be assigned to single device-address control units.

4. Device addresses for multidevice control units always start at an address boundary as previously defined.

   Example -- A control unit with two device-access paths can be assigned any starting device address that has zero in the low-order bit position.

5. Control units must not recognize more device addresses than they are designed to handle.

   Example -- A control unit designed to handle ten device-access paths must recognize addresses 0000-1001 in the four low-order bit positions, but must reject addresses 1010-1111 in these four bit positions.

   If no control unit responds to an address ('select out' is propagated through all control units, and back to the channel on 'select in'), the device appears as not operational. Not operational may include (in addition to addresses outside an assigned set):

   a. An I/O device address not installed.

   b. An I/O device address partitioned out of the system by the program, operator, or customer engineer (off-line, disabled, etc.).

The control unit must respond to those addresses in the set which is:

a. Ready

b. Not ready but which can be made ready by means of an ordinary manual intervention. A not-ready device is indicated by the unit-check status and intervention-required sense indicator.

The control unit may respond to all addresses in the assigned set, regardless of whether the device associated with the address is installed. If a control unit responds to an address of which no device is installed, the unit-check status indicator must be turned on (as well as the appropriate sense indicator(s).

The portion of the address decoder which identifies the control unit can be set at the time of installation for any bit combination.

Single-device-address control units must decode all eight bits of the address byte and the decoder can be set to any bit combination at the time of installation.

6. Control units can never require more addresses than the maximum number of attachable devices. If more than 16 devices, but less than the maximum, are attached to a control unit, the addressing facilities may be added in increments of 16. The number of addresses can never be greater than 15 more than the number of devices attached.

Example -- if a communication type control unit has a designed capacity of fifty six direct-access paths, then:

If only forty devices are to be installed, then at the time of installation, forty eight device addresses can be assigned; but if full capacity of fifty six devices is to be installed, then exactly fifty six addresses will be assigned.

Implementation of address decoding in multidevice control units requires a fixed section and a variable section of the address decoder. Starting at an address boundary, the fixed section of the address decoder is designed to decode the required number of low-order bits for addressing the maximum number of direct access paths. In addition, this section is designed to reject addresses represented by the low-order bit combinations beyond the maximum.

The variable section of the address decoder can be set at the time of installation for any bit combination in the higher order bit positions. The higher order bit positions include all positions of the eight-bit address byte not included in the fixed section of the address decoder.

Single-device address control units have only a variable address decoder and decode all eight bits of the address byte.

COMMANDS

When the command-out line is up, the information on Bus Out is called the command byte. A channel issues the command-out signal to initiate, continue, or terminate an operation in an I/O device.

Command Bytes

Only during a channel-initiated selection sequence (when the channel addresses the device) does the command byte require decoding by the control unit. At all other times the byte is zero (parity immaterial). The low-order bit positions indicate the type of operation, while the high-order bit positions indicate a modification code which expands the basic operation at the control unit or device level.

The actual modifier codes and the particular modes set or the controls performed for them are defined in the specifications for each control unit and/or device.

The command byte on the interface is defined as follows:

BIT POSITION

| P | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TEST I/O |
| P | M | M | M | M | 0 | 1 | 0 | 0 | Sense |
| P | M | M | M | M | 1 | 1 | 0 | 0 | Read Backward |
| P | M | M | M | M | M | M | 0 | 1 | Write |
| P | M | M | M | M | M | M | 1 | 0 | Read |
| P | M | M | M | M | M | M | 1 | 1 | Control |

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M = Modifer bit
P = Parity bit

Sense, read, and control commands with all-zero modifier bits are decoded on all devices as follows:

BIT POSITION

| P | 0 | 1 | 3 | 4 | 5 | 6 | 7 | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Basic Sense |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Basic Read* |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | No Operation Control |

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*Used for Initial Program Loading in addition to Basic Read.

## BASIC OPERATIONS

The I/O operation to be executed over the interface is determined by the eight bit coded command issued to the device during a channel-initiated selection sequence.

The low-order bit positions of this command byte specify the type of operation (see command byte format). The high-order bit positions (modifier code) expand the interpretation of the basic operation at the control unit or device level.

The basic operations are expressed by the commands Read, Read Backward, Write, Control, Sense, and Test I/O. This document treats Test I/O as a command on the I/O interface, although it may originate as either a Test I/O instruction or a channel-initiated sequence for the purpose of clearing or stacking interruption conditions.

A command with invalid parity is not recognized and hence not executed.

### Read

The read command initiated execution of data transfer from the control unit to the I/O channel, and the data are obtained, for example, from the record source of the particular I/O device in operation.

A read command with all modifiers set to zero is a basic read command that is also used as an initial program loading Read. This command, if executed on a device after a system reset, performs the initial-program-loading Read as specified for that particular device.

### Read Backward

The read-backward command initiates an operation in the same manner as the read command, except that the data bytes are transferred to main storage by the channel in the reverse order to that of Read. The control unit may be designed to cause mechanical motion in the device in the opposite direction to that of a Read or may be designed to operate in the device precisely as with a Read.

Unless otherwise noted in this document, any description referring to Read also applies to Read Backward.

### Write

The sequence of signals over the I/O interface to perform a write operation is the same as for Read. In the case of Write, however, the data are sent from the channel to the control unit for such operations as recording or comparing by the selected device.

## Control

The control operation proceeds similarly as Write, except that the command modifier bits received by the control unit are decoded to determine which of several possible functions is to be performed. The function may be second-level addressing which may require several bytes of data to complete the control operation. In cases where the particular control function can be completed without involving the transfer of data, the channel-end status may be presented during the initial selection sequence.

The timing in the control unit for the bytes transferred during a control operation is normally such that the byte for this operation is no faster than the normal Read or Write for the same device. Devices may be excepted from this restriction as determined on an individual basis.

A control command with all-zero modifiers performs no operation at the I/O device, except to satisfy any previously indicated chain operations and allow certain devices to wait for conditions of checking (or any synchronizing indications) before releasing the channel. This variation of the control command is called a no-operation control.

## Sense

Sense proceeds exactly as Read, except that the data are obtained from status indicators rather than from a record source.

The basic sense command has the modifier bits set to zero. This command initiates a sense operation on all devices. The basic sense command must not change the mode or status, or initiate any operation other than to sense the sense indicators. An operable control unit should accept basic sense commands even if a device is in a not-ready condition, mechanically unable to execute certain other operations. If the control unit detects an error during the sense operation, Unit Check is sent with the channel-end status.

The timing in the control unit for the bytes transferred during a sense operation is normally such that the byte rate for this operation is no faster than the rate for the normal Read or Write for the same device. Devices may be excepted from this restriction as determined on an individual basis.

Devices that can provide special diagnostic sense information or can be instructed to perform other special functions by means of Sense may define modifier bits for the control of the function. The special sense operation may be initiated by unique combinations of modifier bits, or a group of codes may specify the sense function. Any remaining sense command codes may be considered invalid or may cause the same action as the basic sense command, depending upon the particular device.

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## Test I/O

The Test I/O is a command that relieves the addressed device path
of pending status information.  If no pending status is encountered
along with I/O path being tested, a zero status byte for the
selected device is sent to the channel for processing.  If status
is available, all pending status bits for the selected device are
transmitted to the channel.

Note that the busy condition is defined differently with res-
pect to Test I/O than for other commands.  (See Busy discussion).

The signal sequence to accomplish Test I/O is the same as any
other channel-initiated selection process except that no operation
is initiated.

## SEQUENCE CONTROLS

The sequence controls described in this section are determined by
the sequence of the signals over the interface.

## Proceed

Whenever Command Out responds to Address In at any time other than
during a channel-initiated selection sequence, it means proceed.

Proceed indicates to the device to continue the normal servicing
sequences on the interface.

## Stop

Stop is indicated by a command-out response to a service-in signal
or as a result of an interface disconnect (see Interface Disconnect),
which occurs before the normal Channel End for the operation in
process.

Stop is used to signal the device that the channel is ending
the current operation.  Upon receipt of the stop signal, the I/O
device must proceed to its normal ending point without sending any
further service-in signals to the I/O channel.  The device remains
busy until the ending status is available, and is presented and
accepted by the channel.

During data operations, Command Out is transmitted in response
to Service In on the cycle after the last byte of data.  If Select
Out is down or goes down after this sequence, Operational In must
drop on force-burst-type operations on devices that cannot meet the
time-out requirements as discussed in the Interface Time-Out
Considerations discussion.  Also, burst devices that have relatively
long times between stop and ending status and have no time-
dependent chaining requirements must drop Operational In at this
time.

## Stack Status

Stack Status is indicated by a command-out response to Status In.
The stack-status signal causes the retention of status information
at the control unit or device until that status is accepted on a
subsequent status cycle with a service-out signal.  When Stack-
Status occurs, the control unit disconnects from the interface
after Select Out is down.  Command Out remains up until Operational
In falls.  An attempt by the control unit to initiate a selection
sequence to present the status again is under control of the
suppress-out signal (See Suppress Status discussion).  Command
Out is not signaled to a zero status byte that has been provided
in response to a command other than Test I/O.

NOTE:  Rather than delay completion of an interface sequence, the
channel will either stack or accept status.

## Suppress Data

Operations whose rate of data transfer can be adjusted without
overruning are subject to suppression of data by Suppress Out.
Completely buffered devices and start/stop devices fall in this
category.  When Suppress Out is up at the control unit and the
operation is in burst mode (whether because Select Out is up or
because the control unit is forcing burst mode) the control unit
must no raise Service In.

Suppress Out must be up at least 250 nsec before Service Out
falls to insure suppression of subsequent data.

## Accept Data

Raising Service Out in response to Service In during a read, read
backward, or sense operation indicates that the information placed
on Bus In has been accepted by the channel.

## Data Ready

Raising Service Out in response to Service In during a write or
control operation indicates that the requested information has been
placed on Bus Out and is ready for acceptance by the control unit.

## Suppress Status

Whenever the channel is unable to immediately handle interruption-
causing status, Suppress Out is raised.  With this line up, the
control unit must not attempt to initiate a selection sequence to
present suppressable-type status.  Suppressable Status includes
stacked status and, at the option of the particular control units,
Device End, or Attention where either of these occurs without
Channel End and with no chaining in process, or Control Unit End.

Suppress Out must be up at least 250 nsec before Select Out
rises at the control unit if suppression of status is to be insured.

Suppress Out suppresses only the initiation of the selection of
the interface by the control unit and if Suppress Out rises after
a status sequence has started, the status sequence will proceed
normally.

The relationship between Request In and Suppress Out is
discussed in the Request In discussion.

### Accept Status

Raising Service Out in response to Status In indicates that the
status placed on Bus In has been accepted by the channel.

### Command Chaining

If Suppress Out is up when Service Out is raised in response to
Status In, Command Chaining is indicated. Command Chaining means
that another command for the device in operation will immediately
follow the presentation of Device End, provided no unusual
conditions were encountered during execution of the current
operation. The exact time at which the next command is presented
is dependent upon the channel.

When command chaining is indicated at the time device end is
presented, this indication will be valid until reselection is made
or until Suppress Out falls. Minimum down-level to insure break -
250 nanoseconds. Reselection of any device attached to the control
unit will reset the chained-command condition in the control unit.
Status conditions such as Unit Check, Unit Exception, Control Unit
End or Attention will terminate command chaining in the channel.

A multidevice control unit which is to operate on more than
one subchannel must not:

1. Reset the chained-command condition on the address other
than the one being selected.

2. Present 'control unit end' with a chaining device address.

Depending upon the particular device, the operation, and
configuration, the command-chaining indication requires certain
functional control which depends upon the individual control unit.

If chaining is indicated when Channel End is presented (Device
End not yet generated) from a control unit shared by two or more
devices, the device presenting Channel End must be the next one to
present device-end status, unless the control unit is addressed in
the meantime on the same interface.

If chaining is indicated when 'device end' is presented, the
control unit must ensure that the path to the device remains
available until the chaining operation is initiated or until
chaining is no longer indicated.

If chaining is indicated on a device shared between more than one control unit or channel, the device must remain available until the chaining operation is initiated or until chaining is no longer indicated.

To assure recognition of Command Chaining by the control unit, Suppress Out must be up at least 250 nsec before Service Out rises in response to Status In. On the other hand, if command chaining is not to be indicated, Suppress Out must be down at least 250 nsec before the rise of Service Out.

Interface Disconnect

The control unit will recognize Interface Disconnect if:

1.  Address Out is up and Select Out is down at least 250 nsec before the completion of any signal sequence, or

2.  If Address Out is up at least 250 nsec while Select Out is up and subsequently Select Out drops while Address Out remains up.

In either case, Address Out may be up concurrently with another out-tag.

When Operational In drops, the channel may drop Address Out to complete the interface-disconnect sequence. Address Out must be down for at least 250 nanoseconds before a new channel-initiated-selection sequence may be attempted.

The control unit responds to the Interface Disconnect by removing all signals, with the possible exception of Request In, from the interface. On an input operation, data on 'bus in' need not be valid after the rise of 'address out'. On an output operation, data on 'bus out' must be valid until the fall of either 'service in' or 'operational in'. When it reaches the normal ending point, the control unit attempts to obtain selection on the interface to present any generated status to the channel. Any abnormal device operation should be indicated by Unit Check (refer Unit Check discussion for additional information) in the status, and the sense information should provide additional details concerning the operation. If the interface-disconnect sequence is performed before initial status is accepted or after device-end status for an operation has been accepted by the channel, the control unit will not generate any status as a result of the Interface Disconnect.

The device path will remain busy after receiving an Interface Disconnect, while performing an operation, until the device-end status is accepted by the channel. If Interface Disconnect is received when the device is not busy no status is generated nor is the device made busy.

NOTE: If 'address out' is up concurrently with another out-tag, the information on 'bus out' must remain valid until the associated in tag drops or until 'operational in' drops.

Selective Reset

Selective Reset is indicated whenever Suppress Out is up and Operational Out drops. This condition causes Operational In to fall, and the particular device in operation and its status to be reset. The operation in process will proceed to a normal stopping point, is applicable, with no further data transfer. The device operating over the interface is the only device reset, even on multidevice control units. The particular device path will be in a busy-state throughout this procedure. Device end may be returned after the reset. To be effective, Suppress Out must rise at least 250 nsec before Operational Out drops and must remain up at least 250 nsec after Operational Out rises. Operational Out must stay down until Operational In falls or for at least 6 usec, whichever is greater, for the selective reset to be effective. The ready or not-ready state of the control unit is not changed by a selective reset.

Selective Reset is issued only as a result of a malfunction detected at the channel or a time-out by the channel. The interpretation of the reset is part of the specifications for the device.

System Reset

System Reset is indicated whenever the operational out and the suppress-out lines are down concurrently and the control unit is in the "on-line" mode. This condition causes Operational In to fall, and all control units and their attached devices, along with their status, to be reset. The control units will be in a busy state throughout this procedure. (See Operational Out for timing considerations). System Reset prepares a device for an initial program loading sequence and is performed as a part of the initial program loading procedure. The ready or not-ready state of the control unit is not changed by a system reset.

To insure a proper reset, the operational-out and suppress-out lines must be down concurrently for at least 6 usec.

The interpretation of the reset is part of the specifications for the device.

STATUS

When the status-in line is up, the information appearing on Bus In is called the status byte. The conditions reported in the status byte are called the status conditions.

The status pertains to the device or implied control unit whose address appeared on 'bus in' (with 'address in') during the

polling or selection portion of the sequence.  In the case of the
control-unit-busy sequence when no 'address in' occurs, it is
assumed that the status pertains to the addressed device or implied
control unit.

## Status Byte

The status byte has the following format:

| Bus Position | |
|---|---|
| P | Parity |
| 0 | Attention |
| 1 | Status Modifier |
| 2 | Control Unit End |
| 3 | Busy |
| 4 | Channel End |
| 5 | Device End |
| 6 | Unit Check |
| 7 | Unit Exception |

The status byte is transmitted to the channel in six different
situations:

1. During the initial selection process.

2. To present the channel-end status at the termination of
   data transfer.

3. To present the device-end signal and any associated
   conditions to the channel.  The device remains busy until
   the channel accepts the device-end status.

4. To present any externally initiated status to the channel.

5. To present any previously stacked status when allowed to
   do so.

6. To present control-unit-end or device-end status which
   signals that the control unit or device that was previously
   busy and then interrogated, is now free.

Once accepted by the channel the status byte is not presented again.

## Status Conditions

The following status conditions are detected by the I/O device or
control unit and are indicated to the channel over the I/O
interface.  The timing and causes of these conditions for each
type of devices are defined in the specifications for the device.

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When the device is accessible from more than one channel, status is signaled to the channel initiating the associated I/O operation. Handling of conditions not associated with I/O operations depends upon the type of device and conditions, and is defined in the specifications for the device.

NOTE: Control units must provide interlocks in their design so that status is not lost, hidden, or included with other status when the result would cause the program to misinterpret the original meaning and intent of the status.

Attention

Attention is generated when some asynchronous condition occurs in the I/O device. Attention is not associated with the initiation, execution, or termination of any I/O operation.

The attention condition cannot be indicated to the channel while an operation is in progress at the device or control unit. Otherwise, the handling and presentation of the condition to the channel depends upon the type of device. A device shared between more than one channel path must present the attention status to all channel paths as defined in the individual device specification. Indication of Attention causes command chaining to be suppressed. Attention can occur with Device End. Depending upon the device application, Attention may or may not be presented until command chaining is no longer indicated.

Status Modifier

The Status Modifier is used by I/O control units in three different situations:

1.  Control units that cannot provide current status in response to Test I/O present the status-modifier bit alone during the initial selection procedure.

2.  Control units that are busy present the status-modifier bit with the busy bit during the initial selection procedure to differentiate Control Unit Busy from Device Busy.

3.  Control units designed to recognize special ending conditions (e.g., Search Equal on a disk) present the status-modifier bit with Device End when the special condition occurs.

In the first case, provision is made for certain types of control units that are not capable of providing current status on a demand basis as required by Test I/O. The presentation of the status modifier bit in response to Test I/O indicates that the control unit cannot execute the command, and any existing status remains unchanged and unavailable to a Test I/O. This type of control unit provides status only on a control-unit initiated selection sequence.

In the second case, provision is made for indicating that a busy condition pertains to a control unit and not necessarily to the addressed I/O device. This condition occurs when the control unit is required to perform a function that does not involve the I/O interface (e.g., backspace file on magnetic tape). The condition may also occur when the control unit has status pending for an I/O device other than the one addressed.

In the third case, provision is made for control units designed to recognize special ending or synchronizing conditions. If the special condition occurs, the status-modifier bit with the device-end bit is presented during the device-end status cycle. The channel may use the special status indication to modify the command chain sequence if no unusual conditions occur.

Control Unit End

The control-unit-end condition is provided only by channel-shared control units or control units shared by I/O devices, and only when one or both of the following conditions occurs:

1.  The control unit was interrogated while executing an operation. The control unit is considered to have been interrogated when during a previous channel-initiated selection sequence the control unit responded with Busy and Status Modifier in the status byte.

2.  The control unit detected an unusual condition while busy, but after Channel End was accepted by the channel.

If the control unit remains busy executing an operation after signaling Channel End, but is not interrogated by the program and does not detect an unusual condition, Control Unit End is not generated.

When the busy state of the control unit is temporary, Control Unit End is included with Busy and Status Modifier in response to interrogation, even though the control unit is not yet free. The busy condition is considered temporary if its duration is less than 2 milliseconds.

The device address associated with Control Unit End is determined as follows:

1.  If Control Unit End is to be presented with Channel End and/or Device End, the address of the selected device is used.

2.  If Control Unit End is generated without Channel End or Device End and the status is presented during a control-unit initiated selection sequence, the device address to be used when presenting this status is allowed to be any legitimate address associated with the control unit

(a legitimate address is any address the control unit is capable of recognizing regardless of whether or not the device is actually attached).

3. If Control Unit End is to be presented during a channel-initiated selection sequence, the device address will be the same as the address issued with Address Out. This channel-initiated selection sequence may be either a normal full-length selection sequence or the short, control-unit-busy sequence.

A pending Control Unit End causes the control unit to appear busy for initiation of new operations. Control Unit End causes command chaining to be suppressed.

Busy

Busy can occur only during a channel initiated selection sequence and indicates that the I/O device or control unit cannot execute the command because a previously initiated operation is being executed or because status conditions exist. An operation is being executed from the time initial status is accepted until Device End is accepted. Status conditions for the addressed device, if any, accompany the busy indication.

If the busy condition applies to the control unit, Busy is accompanied by Status Modifier. The busy condition causes command chaining to be suppressed. Busy is indicated to Test I/O only if a previously initiated operation is still being executed and no end status is available.

Channel End

Channel End is caused by the completion of the portion of an I/O operation involving transfer, if any, of data or control information between the I/O device and the channel.

Each I/O operation causes only one channel-end signal to be generated. The channel-end condition is not generated unless the command is accepted. The exact time during an I/O operation when Channel End is generated depends upon the operation and the type of device. For operations such as writing, some devices generate the channel-end condition when the block has been written. On other devices that later verify the writing, Channel End may or may not be delayed until verification is performed, depending upon the device. On devices such as those equipped with buffers, the channel-end condition occurs upon completion of data transfer between the channel and the buffer. During control operations, Channel End is usually generated after the control information is transferred to the control unit, although for short operations the Channel End may be delayed until completion of the operation. Operations that do not cause data to be transferred can provide the channel-end condition during the initial selection sequence.

Device End

Device End is caused by the completion of an I/O operation at the
device or, on some devices, by manually changing the device from
the not-ready to the ready state. The device-end condition normally
indicates that the I/O device has completed the current operation.

Each I/O operation causes only one device-end condition. The
device-end condition is not generated unless the operation is
accepted.

The device-end condition associated with an I/O operation is
generated either simultaneously with the channel-end condition or
later. In the case of data-transfer operations on some devices,
the device terminates the operation at the time Channel End is
generated, and both Device End and Channel End occur together.
On buffered devices, the device-end condition may occur upon
completion of the mechanical operation. For control operations,
Device End is generated at the completion of the operation at the
device. The operation may be completed at the time Channel End is
generated or later.

When command chaining is specified, receipt of the device-end
signal, in the absence of any unusual conditions, causes the
channel to initiate a new I/O operation. If an unusual condition is
detected during the initiation of a chained command, the chain is ter-
minated without device end.

A device shared between more than one channel path and which
has a Device End generated due to the device going from not-ready to
ready state must present a Device End to all channels as defined in
the individual device specifications.

If a device is addressed while in a busy state, a Device End
must be signaled to the path initiating the command when the device
becomes not busy.

NOTE: "Not ready" means that a device requires operator intervention
to become operational. 'The not-ready condition can occur, for
example, because of any of the following actions:

   1.  An unloaded condition on magnetic tape,

   2.  Card equipment out of cards or stacker full,

   3.  Printer out of paper, or

   4.  Error conditions which need operator intervention.

Unit Check

Unit Check indicates that the I/O device or control unit requires
programming or manual intervention. Unit Check does not necessarily
indicate an error condition. The conditions causing Unit Check are

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detailed by the information available to a sense command which should normally follow the acceptance of unit-check status. The unit-check bit provides a summary indication of the conditions identified by sense data.

The unit-check condition is generated only when an error is detected during execution of a command, or during some activity associated with an I/O operation. Unless the error condition pertains to the activity initiated by a command and is of immediate significance to the program, the condition does not cause the program to be alerted after Device End is cleared. When the device is not executing an operation and does not have a pending interruption condition, equipment malfunctioning may cause the device to become not ready; Unit Check in this event is signaled to the program the next time the device is selected.

Unit Check may be signaled to indicate a condition in the control unit that needs to be handled and that additional information is available in the sense data.

If, during the initial selection sequence, the device detects that the command cannot be executed, Unit Check is presented to the channel and appears without Channel End, Control Unit End, or Device End. Such unit status indicates that no action has been taken at the device in response to the command. If the condition precluding proper execution of the operation occurs after execution has started, Unit Check is accompanied by Channel End, Control Unit End, or Device End, depending upon when the condition is detected. On special devices, errors associated with an operation may be detected after Device End is cleared. These errors are signaled by sending Unit Check with Attention.

Errors in command-code parity or otherwise invalid command codes do not cause a Unit Check if the control unit busy working or holding status at the time of selection. Under these circumstances the device responds by providing the busy bit and indicating the pending status, if any. The command-code invalidity is ignored.

When 'unit check' appears with 'channel end' and without 'device end', a shared control unit must preserve the sense data and an available device path until after the 'device end' is accepted.

When no interruption condition is pending for the addressed device at the control unit, the control unit signals 'unit check' when 'test I/O' or the 'no-operation control' command is issued to a not-ready device. In the case of no operation, the command is rejected and 'channel end' and 'device end' do not accompany 'unit check.'

Unless the command is designed to cause 'unit check', such as rewind and unload on magnetic tape, 'unit check' is not indicated if the command is properly executed even though the device has become not ready during, or as a result of, the operation. Similarly, 'unit check' is not indicated if the command can be

executed with the device not ready.  Selection of a device in the
not-ready state does not cause a unit-check indication when the
sense command is issued, and whenever an interruption condition is
pending for the addressed device at the control unit.

PROGRAMMING NOTE:  If a device becomes not ready on completion of a
command, the ending interruption condition can be cleared by 'test
I/O without generation of 'unit check' because of the not-ready
state.  Any subsequent 'test I/O' issued to the device causes a
unit-check indication.

   Unit Check causes command chaining to be suppressed.

Unit Exception

Unit Exception is caused when the I/O device detects a condition
which usually does not occur.  Conditions such as recognition of a
tape mark are included.  Unit Exception has only one meaning for any
particular command and type of device.  A sense operation is not
required as a response to the acceptance of a unit-exception
condition.

   A unit-exception condition can be generated only when the
device is executing an I/O operation, or when the device is involved
with some activity associated with an I/O operation and the condition
is of immediate significance.  If a device detects a unit-exception
condition during the initial selection sequence, Unit Exception is
presented to the channel and appears without Channel End, Control
Unit End or Device End.  Such unit status indicates that no action
has been taken at the device in response to the command.  If the
condition precluding normal execution of the operation occurs after
the execution is started, Unit Exception is accompanied by Channel
End, Control Unit End, or Device End, depending upon when the
Condition is detected.  Any unusual condition associated with an
operation, but detected after Device End is cleared, is indicated by
signaling Unit Exception with Attention.

   The Unit Exception causes command chaining to be suppressed.

SENSE INFORMATION

Data transfer during a sense operation provides information concerning
unusual conditions detected in the last operation and concerning the
status of the device.  Status information provided by the basic sense
command is more detailed than that supplied by the unit-status byte,
and may describe reasons for the unit-check indication.  It may also
indicate, for example, that the device is in the not-ready state, that
a tape drive is in the file-protected state, or that magnetic tape is
positioned beyond the end-of tape mark.

   Sense information that results from more than one action at the
unit must not be ORed when this condition would cause the program to
misinterpret the original meaning and intent of the sense information.

Note that when a group of sense indicators is shared with different devices the residual control-unit sense data that pertains to the last command addressed to the control unit may be reset if the device addressed is different from the device which generated the sense data.

For most devices the first six bits of the first sense data byte (Sense Byte 0) are common to all devices having this type of information. The six bits are independent of each other and are designated as follows:

| BIT | DESIGNATION |
|-----|-------------|
| 0 | Command reject |
| 1 | Intervention required |
| 2 | Bus-out check |
| 3 | Equipment check |
| 4 | Data check |
| 5 | Overrun |

Command Reject - The device detected a programming error. A command was received that either the device is not designed to execute, the device cannot execute because of its present state, requires use of an uninstalled optional feature, or contains invalid control data.

Command reject is also indicated when an invalid sequence of commands is recognized ('write' to a direct-access storage device without previously designating the data block).

Intervention Required - The last operation could not be executed because of a condition requiring intervention at the device. This bit indicates conditions such as an empty hopper in a card punch, or the printer being out of paper.

Intervention required is also turned on when the addressed device is in the not-ready state, is in test mode, or is not provided on the control unit.

Bus-Out Check - The device or the control unit received a data byte or a command code with an invalid parity over the I/O interface.

During writing, Bus-Out Check indicates that a parity error was detected and incorrect data may have been recorded at the device, but the condition does not cause the operation to be terminated prematurely, unless the operation is such that an error precludes meaningful continuation of the operation. No operation is initiated if the command code has a parity error. Parity errors on control information cause the operation to be terminated.

Equipment Check - The device or the control unit detected equipment malfunction during the last operation, such as an invalid card hole count or printer buffer parity error. Normally, data transmission stops and the operation terminates.

Data Check - The device or the control unit detected a data error other than those included in Bus Out Check. Data Check identifies errors associated with the recording medium and includes conditions such as reading an invalid card code or detecting invalid parity on data recorded on magnetic tape.

On an input operation, Data Check indicates that incorrect data may have been placed in main storage. The control unit forces correct parity on data sent to the channel. On writing, the data-check condition indicates that incorrect data may have been recorded at the device. Data errors on reading and writing do not cause the operation to be terminated prematurely.

Overrun - The channel failed to respond on time to a request for service from the device. Overrun can occur when data are transferred to or from a non-buffered control unit operating with a synchronous medium, and the total activity initiated by the program exceeds the capability of the channel. On an output operation, Overrun indicates that data recorded at the device may be invalid. In these cases, data overrun normally stops data transfer and the operation terminates as in Stop discussion. The overrun is also turned on when the device receives the new command too late during command chaining.

All sense information significant to the use of the device normally is provided in the first two bytes. Any bit position following those used for programming information contain diagnostic information, which may extend to as many bytes as needed. The amount and the meaning of the status information are peculiar to the type of device, and are defined in the specifications for the device.

The sense information pertaining to the last I/O operation is reset by the next command addressed to the control unit, other than Test I/O, Sense (basic), or Control (no-operation), provided that the busy bit is not included in the initial selection status byte.

A command code with invalid parity will cause the sense information to be reset only if Unit Check is turned on as a result of the invalid parity (See Unit Check discussion).

METERING

Does not apply.

POWER OFF AND OFFLINE

When the power is off on a control unit, the associated logic and circuitry of the I/O interface is designed to allow other control units on the same interface to operate with the channel. The control unit power off provides the following:

1.  Electrical bypass for the select-out line.

2.  Protection against its line drivers from interfering with the I/O interface.

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The effect of power-on/power-off transitions must not interfere with the I/O Interface. This requirement does not apply if the power off transition is due to a failure in the CU power system or a main line power failure.

A control unit in an offline condition or going to or from an offline condition does not interfere in the operation between the channel and other control units on the same interface. The control unit in the offline mode provides the following:

1. Logical bypass for the select signal.

2. Gates off all other line drivers from interfering with activity on the interface.

INTERFACE TIME-OUT CONSIDERATIONS

Signaling over the I/O interface is specified to be direct-current interlocked and thus is not time-dependent, a certain category of machine malfunctions may cause "hangup" of the system. The timing considerations involved in determining malfunction cases are dis-· cussed in the following paragraphs.

All references to particular time considerations, in this section, represent the maximum permissible time in worst-case situations. All control units are designed for minimum signal sequence response times within the limitation of the circuit family used and the sequencing method required for particular devices. A maximum worst-case interface signal sequence of 32 usec, due to the control unit, is specified. This means that from the time Select Out rises at a particular control unit for any signal sequence until the sequence is completed (Operational In drops), no more than 32 usec, dut to the control unit circuitry or the sequencing method used, will be required by the control unit. This applies to all selection sequences. However, a particular interface signal sequence may take longer due to other factors:

1. Delays introduced by the channel

2. Delay due to the need for a burst-mode device to capture the interface prior to reaching record area of media (not greater than 500 msec).

In addition to delays which may occur within a particular signal sequence, abnormal delays may exist between data cycles during burst-mode operation. The maximum delay between data cycles in burst mode shall not exceed 500 msec. Control units may be excepted from this restriction as determined on an individual basis.

If a control unit exceeds the specified delays, the channel is permitted to force an interface disconnect (see Interface Disconnect discussion) or a selective reset (see Selective Reset discussion) based on a channel time-out of the signal sequences.

Control units and channels must specify minimum and maximum response times for all interface signal sequences in their individual design specification.

## Propagation of Select Out

Whenever selection of the interface is not to be made during an initial selection or scan sequence the control unit must propagate the select-out signal within 600 nsec.

This time is measured from the rise of the incoming select-out signal to the rise of the out going select-out signal.

## ELECTRICAL SPECIFICATION, PHYSICAL REQUIREMENTS

### Multiple Drivers and Receivers

Up to ten receivers must be able to be driven by one driver. The driver must be located at one of the extreme ends.

Up to ten drivers must be able to be dot ORed to drive one receiver. The receiver must be located at one of the extreme ends.

NOTE: An end-of-line driver or receiver may be placed beyond the terminator. In this case, the distance between the end-of line driver or receiver and the terminator must be less than six inches.

Receivers must be spaced at least three feet apart. No minimum requirement is set as regards the spacing between drivers. No minimum requirement is set as regards the spacing between a terminator and driver or receiver if the terminator is placed on the outermost end of the line.

The maximum stub length from the line to a driver or receiver on the circuit card is six inches.

## GENERAL ELECTRICAL REQUIREMENTS

### Voltage Levels

There are two logical levels. A dc line voltage of +2.25 volts or more denotes a logical one state, and a dc voltage of +0.15 volt or less denotes a logical zero state. These voltages are relative to the driver ground.

### Cable

All lines must have a characteristic impedance of 92 ±10 ohms and, with the exception of 'select out', must be terminated at each extreme end in their characteristic impedance by a terminating network (For select out/select in, refer to Select-Out Circuitry discussion).

Cable length may be limited by special conditions but is never to exceed a maximum line resistance of 33 ohms. The 33 ohm resistance includes all contact resistance, internal cable resistance, and inter-unit cable resistance.

Terminating Networks

The terminating network must present an impedance of 95 ohms ±2.5 percent between the signal line and ground, and must be capable of dissipating 390 milli-watts.

Ground Shift and Noise

The maximum noise (measured at the receiver input) coupled onto any signal line must not exceed 400 milli-volts.

The maximum allowed ground shift, between any active driver and any receiver of the same interface line, is 150 millivolts. Therefore, the maximum shift, (coupled noise plus ground shift) allowed on any line is 550 millivolts.

The logical levels defined in the voltage levels discussion and the receiver threshold levels specified in receivers discussion allow for this 550 millivolt shift. That is, a negative noise pulse of 400 millivolts coupled with a positive receiver ground shift of 150 millivolts occurring during a one state (2.25 volts minimum) guarantees a receiver input of 1.7 volts or more. See Figure D-3A.

Also, a positive noise pulse of 400 millivolts coupled with a negative receiver ground shift of 150 millivolts occurring during a zero state (0.15 volt maximum) guarantees a receiver input of 0.7 volt or less. See Figure D-3B.

NOTE: The noise measurements are made at the input to the receiver. A combination of the dc level and ac noise must not exceed 0.7 volt for the down level and must not be less than 1.7 volts for the up level.

NOTE: Noise may be generated by circulating currents in the grounding network if the proper grounding rules are adhered to. In the 9020 System, the ground lead (green with yellow tracer) in the power source cable to all elements is connected to the machine (frame) ground. All signal lead shields are connected to circuit (electronic) ground. The circuit ground is connected to the frame ground at one or more points in each unit.

INTERFACE CIRCUIT REQUIRMENTS

Receivers

An input voltage (relative to receiver circuit ground) of 1.7 volts
or more is interpreted as a logical one; an input of 0.70 volt or
less is interpreted as a logical zero.  An open circuited input is
interpreted as a logical zero.

The receiver should not be damaged by:

1.  A dc input of 7.0 volts with power on in the receiver.

2.  A dc input of 6.0 volts with power off in the receiver.

3.  A dc input of -0.15 volt with power on or off.

The receiver input must not require a positve current (Figure
D-3C) larger than +0.42 milliampere at an input voltage of +3.11
volts.

Negative receiver input current at +0.15 volt must not exceed
-0.24 milliampere.  In addition, receiver input impedance must be
larger than 4.0 kilohms and less than 20 kilohms.

Receivers must be designed to ensure that no spurious noise is
generated on the line during a normal power-up or power-down
sequence.

Drivers

In the logical zero state:

1.  The output voltage must not exceed 0.15 volt at a load of +240
    microamperes. (See Figure D-3D for current polarity definition).

In the logical one state:

1.  The output voltage must be 3.11 volts or more at a load of
    +59.3 milliamperes (two terminators, ten receivers).

2.  The output voltage must not exceed 5.85 volts at a load of
    +30 microamperes (one receiver, no terminator).

3.  The output voltage must not exceed 7.0 volts at a load of
    +123.0 milliamperes during an over-voltage internal to the
    drivers.

Drivers must be designed to ensure that no spurious noise is
generated on the line during a normal power-up or power-down sequence.
For the driver, this may be accomplished by one of the following
methods:

1.  Sequencing the power supplies.

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2. Building noise suppression into the circuit.

3. Providing an externally controlled gate.  (see Figure D-3E)

For a normal power-down sequence:

1. Logically ensure that the driver is in the zero state.

2. Close contact S2.  (See Figure D-3E.)

3. Turn power off.

For a normal power-up sequence:

1. Ensure that contact S2 is closed.

2. Turn on power.

3. Logically ensure that the input level will cause the driver output to be in the zero state.

4. Open contact S2.

## Fault Conditions

A grounded signal line must not damage drivers, receivers, or terminators.

With one driver transmitting a logical one, loss of power in any single circuit driver, receiver, or terminator on the line must not cause damage to other components.

With both terminators connected, line operation must not be affected by power off in any drivers or receivers on the line.

ELECTRICAL SPECIFICATIONS FOR SELECT-OUT CIRCUITRY

## General

The 'select out' line has a single-driver to single-receiver configuration, with only the receiver end of the line terminated in the characteristic impedance.

A dc line voltage of 1.85 volts or more denotes a logical one state, and a dc line voltage of 0.15 volt or less denotes a logical zero state.  These voltages are relative to the driver ground.

NOTE:  Because of the nature of the 'select out/select in' line, negative noise tolerance has been neglected.

All electrical requirements specified in General Electrical Requirements discussion that are not redefined in this section are also applicable to 'select out'.

## Receiver

The 'select out' receiver must satisfy all requirements given in the Interface Circuit Receiver Requirements discussion.

## Driver

The select out driver must be capable of withstanding a short-circuit-to ground output condition, while in either the logical one or zero state, without damage to the driver circuit.

For the logical zero state:

1. The output voltage of a select out driver must not exceed 0.15 volt at a load of 1 milliampere.

For the logical one state:

1. Output voltage of a channel driver or the driver of a control unit contained within a channel frame must exceed 3.9 volts at a load of 41 milliamperes.

2. The output voltage of a control unit driver not contained within a channel frame must exceed 3.7 volts at a load of 41 milliamperes.

The output voltage of a select out driver should not exceed:

1. 5.8 volts at a load of 0.3 milliampere.

2. 7.0 volts at a load of 72 milliamperes during an over-voltage internal to the driver.

## Terminator

A 95 ohm ±2.5 percent, 390 milliwatt terminator to ground must be placed at each receiver for each line segment along the 'select out/select in' path, including the receiver end of 'select in' located in the channel.

The driver end of each segment of 'select out/select in' must not be terminated, including the driver end of 'select out' located in the channel. Also, the jumpered 'select out' or 'select in' and the bypassed 'select out' or 'select in' path is not terminated.

## Circuits

Figures D-3F, D-3G, D-3H show representative circuits used to drive, receive, and terminate the lines between the channel and attached control units.
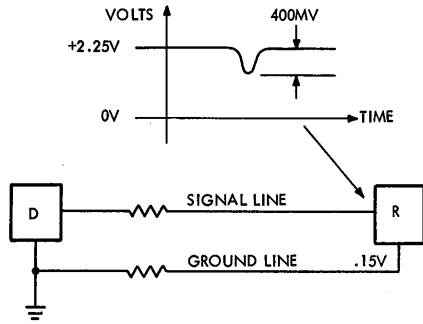
FIGURE D-3A. NEGATIVE NOISE
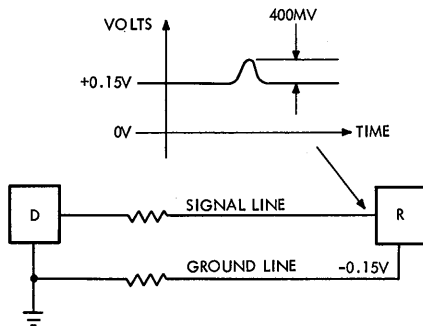


FIGURE D-3B. POSITIVE NOISE
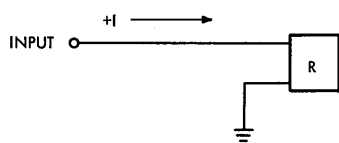


FIGURE D-3C. RECEIVER
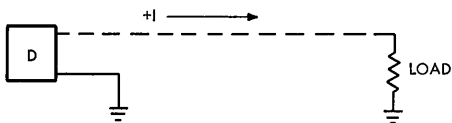


FIGURE D-3D. CURRENT POLARITY
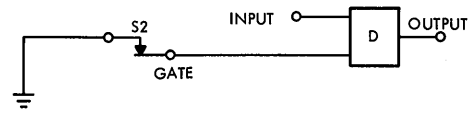


FIGURE D-3E. DRIVER GATE
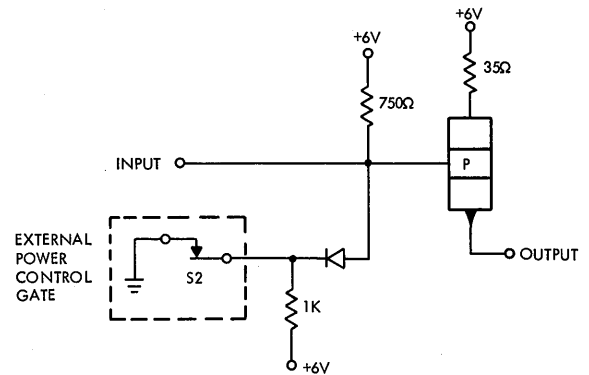


FIGURE D-3F. LINE DRIVER
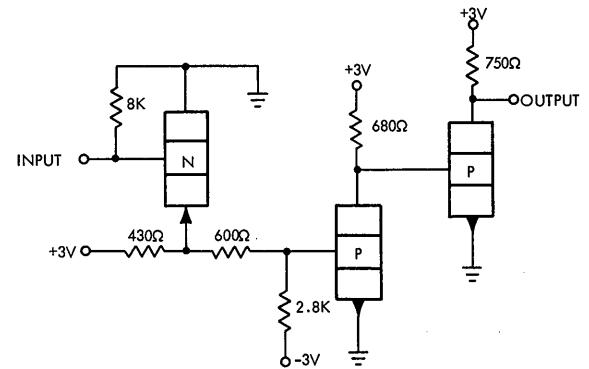


FIGURE D-3G. LINE RECEIVER
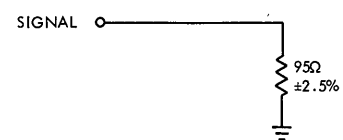


FIGURE D-3H. LINE TERMINATOR

MECHANICAL REQUIREMENTS

Interface cables will use IBM connectors defined for this purpose
or equivalent.  See Appendix B of Design Data for further
characteristics of these connectors.

PIN ASSIGNMENTS

Pin assignments for the I/O interface are shown in Figure D-4.  They
are shown as viewed from the connector side of the channel and con-
trol unit tailgates.  Two interface cables connect the channel to
the first group of control units.  Signals are assigned corresponding
pin numbers on the channel and control unit connectors.

SYSTEM CONSIDERATIONS

ATTACHMENT OF CONTROL UNITS TO THE MULTIPLEXOR CHANNEL

The system considerations in connecting Control Units to the
Multiplexor Channel are complex and inter-related.  Among these
considerations are the relative data rates of the various devices
operated by a control unit and the service priority assignment of
these devices, the relative data rates of the various devices
operated by the different control units, the service priority
assignment of the Control Units on the interface, the ability or
inability of the devices to accept service at a varying rate, and
the proportion of data cycles to non-data cycles for interleaved
multi-device operations.  A thorough analysis of each system case
should be conducted to determine the proper configuration of control
units and devices to avoid overruns and subsequent data loss caused
by interference conditions.

     Within the constraints imposed by system considerations, 256
I/O devices distributed over a maximum of 8 Control Units may be
attached to the Multiplexor Channel.  The maximum possible cable
length (from terminator to terminator), is limited by line resistance
as defined in the General Electrical Requirements, Cable discussion.

     A limitation of 200 feet of external interconnecting cable
attached to the 9020 System Multiplexor Channel is imposed to provide
allowance for proper operation of presently undefined device
combinations and system configurations.

ATTACHMENT OF CONTROL UNITS TO THE SELECTOR CHANNEL

A maximum of 8 Control Units may be attached to a Selector Channel.
Only one CU operates with the channel at any one time, therefore
attachment considerations are primarily concerned with the operation
of a specific CU without regard to the operation characteristics of
the other attached CU's.  However, the effects of the attachment of
other Control Units to the transmission line connecting the operating
CU with the Channel must be taken into consideration.

Figure D-4. I/O Interface Connector Pin Assignments

*UNUSED CONNECTOR POSITIONS.
**RESERVED FOR FUTURE USE.
***RESERVED FOR SPECIAL USE.

**CHANNEL/CONTROL UNIT OUT SERPENT CONNECTOR 2 ("A" STYLE) — LIGHT GRAY**

| | | | |
|---|---|---|---|
| * | 02 | 02 | SHIELD |
| * | 03 | 03 | OPERATIONAL IN |
| STATUS IN | 04 | 04 | SHIELD |
| SHIELD | 05 | 05 | ADDRESS IN |
| SERVICE IN | 06 | 06 | * |
| SHIELD | 07 | 07 | SHIELD |
| SHIELD | 08 | 08 | SELECT IN |
| SELECT OUT | 09 | 09 | SHIELD |
| SHIELD | 10 | 10 | ADDRESS OUT |
| COMMAND OUT | 11 | 11 | * |
| SHIELD | 12 | 12 | SUPPRESS OUT |
| SERVICE OUT | 13 | 13 | SHIELD |
| * | 02 | 02 | SHIELD |
| * | 03 | 03 | CLOCK OUT |
| METERING OUT | 04 | 04 | SHIELD |
| SHIELD | 05 | 05 | METERING IN |
| REQUEST IN | 06 | 06 | * |
| SHIELD | 07 | 07 | GROUND |
| SHIELD | 08 | 08 | ** |
| *** | 09 | 09 | GROUND |
| SHIELD | 10 | 10 | ** |
| *** | 11 | 11 | * |
| SHIELD | 12 | 12 | HOLD OUT |
| OPERATIONAL OUT | 13 | 13 | SHIELD |

**CHANNEL/CONTROL UNIT OUT SERPENT CONNECTOR 1 ("A" STYLE) — LIGHT GRAY**

| | | | |
|---|---|---|---|
| * | 02 | 02 | SHIELD |
| * | 03 | 03 | BUS OUT P |
| BUS OUT 0 | 04 | 04 | SHIELD |
| SHIELD | 05 | 05 | BUS OUT 1 |
| BUS OUT 2 | 06 | 06 | * |
| SHIELD | 07 | 07 | SHIELD |
| SHIELD | 08 | 08 | BUS OUT 3 |
| BUS OUT 4 | 09 | 09 | SHIELD |
| SHIELD | 10 | 10 | BUS OUT 5 |
| BUS OUT 6 | 11 | 11 | * |
| SHIELD | 12 | 12 | BUS OUT 7 |
| ** | 13 | 13 | SHIELD |
| * | 02 | 02 | SHIELD |
| * | 03 | 03 | BUS IN P |
| BUS IN 0 | 04 | 04 | SHIELD |
| SHIELD | 05 | 05 | BUS IN 1 |
| BUS IN 2 | 06 | 06 | * |
| SHIELD | 07 | 07 | SHIELD |
| SHIELD | 08 | 08 | BUS IN 3 |
| BUS IN 4 | 09 | 09 | SHIELD |
| SHIELD | 10 | 10 | BUS IN 5 |
| BUS IN 6 | 11 | 11 | * |
| SHIELD | 12 | 12 | BUS IN 7 |
| ** | 13 | 13 | SHIELD |

**CONTROL UNIT IN SERPENT CONNECTOR 2 ("B" STYLE) — DARK GRAY**

| | | | |
|---|---|---|---|
| SHIELD | 02 | 02 | * |
| OPERATIONAL IN | 03 | 03 | * |
| SHIELD | 04 | 04 | STATUS IN |
| ADDRESS IN | 05 | 05 | SHIELD |
| * | 06 | 06 | SERVICE IN |
| SHIELD | 07 | 07 | SHIELD |
| SELECT IN | 08 | 08 | SHIELD |
| SHIELD | 09 | 09 | SELECT OUT |
| ADDRESS OUT | 10 | 10 | SHIELD |
| * | 11 | 11 | COMMAND OUT |
| SUPPRESS OUT | 12 | 12 | SHIELD |
| SHIELD | 13 | 13 | SERVICE OUT |
| SHIELD | 02 | 02 | * |
| CLOCK OUT | 03 | 03 | * |
| SHIELD | 04 | 04 | METERING OUT |
| METERING IN | 05 | 05 | SHIELD |
| * | 06 | 06 | REQUEST IN |
| SHIELD | 07 | 07 | SHIELD |
| ** | 08 | 08 | SHIELD |
| SHIELD | 09 | 09 | *** |
| ** | 10 | 10 | SHIELD |
| * | 11 | 11 | *** |
| HOLD OUT | 12 | 12 | SHIELD |
| SHIELD | 13 | 13 | OPERATIONAL OUT |

**CONTROL UNIT IN SERPENT CONNECTOR 1 ("B" STYLE) — DARK GRAY**

| | | | |
|---|---|---|---|
| SHIELD | 02 | 02 | * |
| BUS OUT P | 03 | 03 | * |
| SHIELD | 04 | 04 | BUS OUT 0 |
| BUS OUT 1 | 05 | 05 | SHIELD |
| * | 06 | 06 | BUS OUT 2 |
| SHIELD | 07 | 07 | SHIELD |
| BUS OUT 3 | 08 | 08 | SHIELD |
| SHIELD | 09 | 09 | BUS OUT 4 |
| BUS OUT 5 | 10 | 10 | SHIELD |
| * | 11 | 11 | BUS OUT 6 |
| BUS OUT 7 | 12 | 12 | SHIELD |
| SHIELD | 13 | 13 | ** |
| SHIELD | 02 | 02 | * |
| BUS IN P | 03 | 03 | * |
| SHIELD | 04 | 04 | BUS IN 0 |
| BUS IN 1 | 05 | 05 | SHIELD |
| * | 06 | 06 | BUS IN 2 |
| SHIELD | 07 | 07 | SHIELD |
| BUS IN 3 | 08 | 08 | SHIELD |
| SHIELD | 09 | 09 | BUS IN 4 |
| BUS IN 5 | 10 | 10 | SHIELD |
| * | 11 | 11 | BUS IN 6 |
| BUS IN 7 | 12 | 12 | SHIELD |
| SHIELD | 13 | 13 | ** |

## Maximum Recommended Data Rate

The maximum recommended synchronous data rate which the 9020 System
Selector Channel is designed to sustain without a possible overrun is
400 kilo-bytes per second (KC).  Control Units should be designed to
require service at a rate not greater than 400 KC.  For further details
of channel data rate refer to Chapter 5 of the IBM 9020 System Design
Data.

## CABLE CONSIDERATIONS

### Internal Cabling

The maximum allowable internal resistance, including all contact
resistance contributed by a channel or control unit is specified as
2.0 ohms for every signal line, except 'select out'and 'select in'.
(Extended or high-performance configurations require that internal
resistance be reduced to a minimum.)  A total of 3.0 ohm maximum
resistance is specified for the control unit for the combined
'select out' and 'select in'.  The maximum resistance case for
'select out/select in' in a control unit usually occurs when the
control unit power is off and electrical bypassing is effective.

For control units, the internal resistance is measured between
the incoming and the outgoing pins on the external connectors.  For
channels, the measurement is made between the external connector pin
and the corresponding channel driver or receiver.

With the exception of the 'select out/select in' line, the
maximum signal delay measured between the external pins is specified
at 15 nanoseconds.  The maximum skew between any two signal lines is
specified at 1 nanosecond.

### External Cabling

The cable length available for the interconnection of channel and
control units is primarily limited by the resistance to the interface
lines which is contributed by the channel and the control units.
For specific control units, the signal delays due to cable length
will require that the control unit be relatively close to the channel.
However, the maximum allowable cable length is limited by total series
resistance between drivers and receivers, if signal cable delay
requirements are met for each attached control unit.

The maximum external connector-to-connector cable length for
unrestricted general systems configurations is determined by the
combined internal resistance specification for 'select out/select in'.
The maximum line resistance for the total 'select out/select in' loop
must not be greater than 52.5 ohms for worst-case conditions.

In certain customized installations where'select out' is
redriven at the end of the cable, the maximum cable length will be
determined by the 2.0 ohm internal control unit and channel resistance
specifications for the signal lines other than 'select out' and

'select in'. In this case, the maximum cable length can be calculated by using the 33 ohm driver-to-receiver maximum line resistance specification for worst-case conditions.

IBM Part No. 5353913 cable, or equivalent, containing 20 coax lines, shall be used for external interconnections. This cable shall present a resistance of 0.052 ohms per foot. See Appendix B for further detail characteristics of this cable.

Line Length

The maximum line length from terminator to terminator is limited by line resistance, defined in the General Electrical Requirements, Cable discussion.

External Cable Measurement

External cables are measured as the distance between floor access holes for cables interconnecting IBM designed Channels and Control Units. For Control Units not designed by IBM, the external cable measurement must include the distance to the connector on the Control Unit

Cable Length

The sum of the external cable lengths from the channel to the 1st CU, thence to each successive CU is defined as the Cable Length. The maximum allowable Cable Length as a function of the number of Control Units is shown below:

| No. of CU's | Max. Cable Length |
|---|---|
| 1 | 438 |
| 2 | 408 |
| 3 | 380 |
| 4 | 351 |
| 5 | 322 |
| 6 | 293 |
| 7 | 264 |
| 8 | 235 |

The above values assume that each CU presents the maximum allowable resistance to the line. The resistance presented by the channel plus the terminator is assumed to equal 4 ohms. External cable resistance of 0.052 ohms/foot is assumed.

Signal Cable Length

The sum of the external cable lengths from the channel driver and receiver circuits to the specific CU under consideration is defined as the Signal Cable Length. The maximum Signal Cable Length to connect a specific CU to the channel is a function of; 1) the data rate to be maintained, 2) the CU delay/byte cycle, 3) the Signal Cable delay/byte cycle, 4) the channel delay/byte cycle, and

5) the number of CU's the Signal Cable must pass through to reach the specific CU.  Since the byte cycle period is equal to the sum of all byte cycle delays, the formula below represents the maximum allowable Signal Cable Length for operation of a CU at a particular data rate.

$$L = \frac{P - D_{CU} - D_{CH} - nD_F}{d_{CA}}$$

Where:  L = Signal Cable Length

P = Byte Cycle Period in nanoseconds $\left(\dfrac{1}{\text{Data Rate}}\right)$

n = Number of CU's signal lines pass through to reach the CU under consideration.

$D_F$ = CU feed through delay per byte cycle in nanoseconds (a parameter of the design of each CU)

$D_{CU}$ = Delay per byte cycle of the operating CU in nanoseconds (a parameter of the CU design)

$D_{CH}$ = Delay per byte cycle of the channel in nanoseconds (a combination of channel design parameters and system operating complexity and resultant priorities)

$d_{CA}$ = Delay per byte cycle per foot of external Signal Cable

When planning connection of Cu's to the 9020 System, both physical placement and System operational characteristics must be considered.  Figure D-5 is provided as a convenient means of determining the maximum Signal Cable length allowable for the attachment of IBM design CU's to a 9020 Selector Channel.  The values used to create the plots shown are for operation of a CU with a single Selector Channel under the specific assumption that this Selector encounters no interference from any other channel or system element.  This information is applicable to the continuous data transfer portion of the operation and excludes chaining operations, transfers in channel, or other programming or control cycle variables.

Two ordinate scales are provided in Figure D-5.  The one at the extreme right is in terms of Control Unit delay ($D_{CU}$) in microseconds for a 400 KC data rate over a range of values (0.5 sec) that can reasonably be expected in the design of CU's to operate at that rate. The lefthand ordinate scale is in terms of Adjusted Byte Cycle Period (P') in nanoseconds where:

$$P' = P - D_{CU}$$
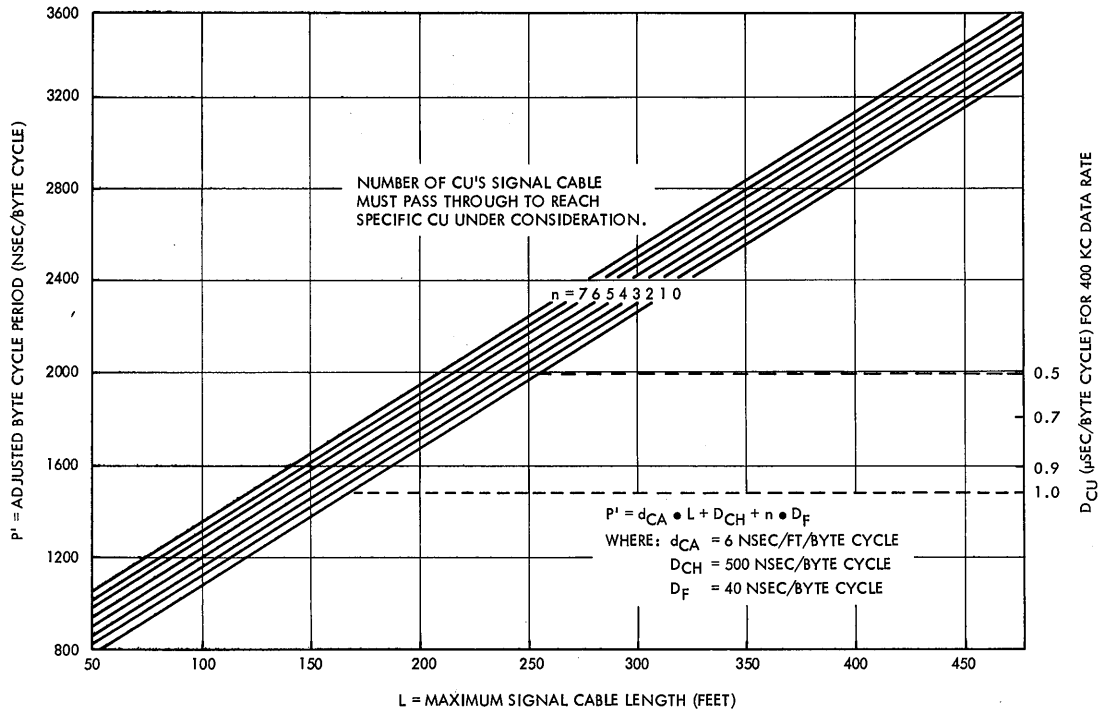
Figure D-5.   Maximum Signal Cable Lengths for Single Selector
              Channel Operation

The following constant values were assumed to create the plots:

$$D_{CH} = 500 \text{ nsec/byte cycle}$$

(This value does not include delays caused by
system or programming activities)

$$D_F = 40 \text{ nsec/byte cycle}$$

(This value is typical of the feed-through
delay inherent in IBM designed CU's).

$$d_{CA} = 6 \text{ nsec/foot/byte cycle}$$

(This value is the sum of four signal transfers
per byte cycle, each transfer delayed 1.5 nsec/
ft.)

Using the values stated above, P' as a function of L has been plotted
for each value of n from 0 to 7.  It should be noted that any point
which falls to the right and below the applicable line as established

by a known physical arrangement and known operating parameters
indicates that the basic channel operating capability has been
exceeded and that the expected data rate cannot be met.  Points falling
on the line or to the left and above the line indicate that the
expected data rate is within the basic channel capability and that
further analysis may be made taking system and programming considera-
tions into account.

OFF-LINE/ON-LINE AND POWER ON/OFF TRANSITIONS

OFF-LINE/ON-LINE

A control unit in an off-line mode must not interfere in the opera-
tion between the channel and other control units on the same inter-
face.  The control unit in the off-line mode must provide the follow-
ing:

    1. Logical bypass for 'select out'.

    2. Gate off all other line drivers from interfering with
       activity on the interface.

    The control unit transition to or from an off-line/on-line
condition must not cause machine malfunction.  The minimum following
conditions must exist concurrently before the on-line-to-off-line
transition can occur:

    1. The on-line/off-line switch is set to OFF LINE.

    2. No active communication on the interface because of this
       control unit, such as 'operational in', or 'status in', etc.

    3. No stacked or pending status is on this unit.  (Stacked
       status is that which has been presented to the channel but
       which has not been accepted.  Pending status is that which
       is forthcoming or which has been generated but not presented.)

    4. No command chaining is indicated for this unit.

The preceding conditions ensure that no machine malfunctions can
occur because of an operator throwing the switch from ON LINE to
OFF LINE.

POWER EFFECTS

Power Off State

The power-off state of any control unit must not affect any opera-
tions of other control units on the interface.  The control unit
whose power is off must provide an electrical bypass for 'select out'
and all of its interface driver and receiver circuits must be pre-
vented from interfering with the interface signals.  The incoming
'select out' signal terminator at the receiver must be disconnected
when the signal is electrically bypassed.  When power is down on all
units, 'select out' must be propagated back to the channel.

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Power Transitions

Each control unit must be designed so that, if proper procedures are followed, the process of individually powering up or down does not cause its interface driver or receiver circuits to generate noise on the interface signal lines.

Each control unit must ensure that the process of electrically bypassing 'select out' prior to power changes does not interfere with 'select out' propagation, except for possible short discontinuities (less than 1.8 microseconds) because of contact bounce coincident with signal delay through parallel logic circuits. Also, each control unit must ensure that 'select out' discontinuities, which may occur when another control unit on the interface is powering up or down, do not affect the propagation of 'select out'. This should be accomplished by the use of a special latch circuit. The latch is turned on by the AND of 'select out' and 'hold out' and is reset by the fall of 'hold out'. The circuit is in series with the remaining selection logic in the control unit and causes a constant 'select out' signal within the control unit and, therefore, to all following control units, regardless of variations in the input 'select out' signal (Figure D-6).

Power Off/On Sequence Requirements

The combination of proper procedures and circuitry must provide the following sequence of events for power off:

1. Logically disconnect the unit from the interface (a panel indicator comes on). (The control unit can become logically disconnected when it and all connected devices have completed all operations, no status is pending, or stacked, and chaining is not indicated.) This ensures that no unfinished operations exist that can cause indication of machine malfunction when power is turned off. Note that when a control unit is logically disconnected from the interface, all its drivers except 'select out' are logically gated off. A logical disconnect may be accomplished as a result of going off-line by use of the on-line/off-line.

2. Close 'select out' bypass circuit (mechanical contact K1, Figure D-6). The normal logical electronic bypass of 'select out' is still active when the control unit is logically disconnected.

3. Open the connection from the line to the 'select out' receiver terminator (mechanical contact, S1, Figure D-6).

4. Clamp interface driver gates to ground by means of a mechanical contact, S2, Figure D-6, if gated drivers are used to avoid transient signals on the interface lines.

5. Turn off power (remote/local power-control switch must be set to LOCAL if the unit has this switch.

```
SELECT OUT       K1
(INCOMING)

          S1
```

D  DRIVER          A   AND FUNCTION
R  RECEIVER        OR  OR FUNCTION
T  TERMINATOR
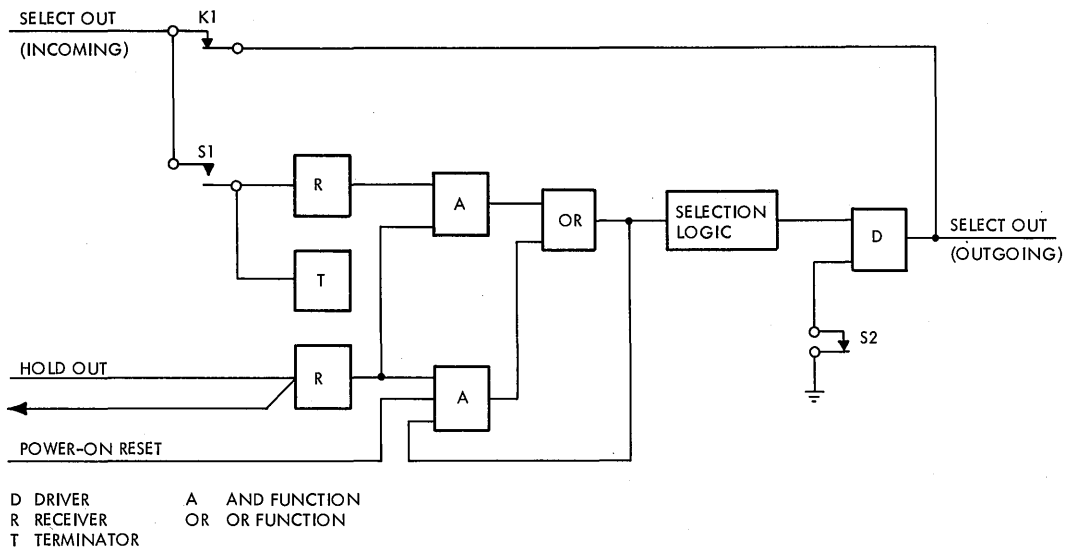
Figure D-6. Representative Select-Out/ Hold-Out Special Latch

For power on, the sequence is reversed:

1.  Turn power on (remote/local power-control switch set to
    LOCAL).  During the power-on sequence, a power-on reset
    pulse must automatically reset the control-unit circuitry,
    including reset of the special 'select out' latch,
    regardless of 'hold out'.

2.  Unclamp driver gates.  (Open mechanical contact, S2.)

3.  Connect 'select out' receiver terminator (S1).

4.  Open 'select out' bypass circuit (K1).

5.  Logically connect the unit to the interface (panel indicator
    turns off).

If some method, such as automatic power sequencing rather than gated
interface driver circuits, is used to eliminate transients on the
signal lines, the steps in the sequence that refer to driver gates
may be eliminated.

NOTE:  The 'select out' bypass function (relay transfer) of a
power-off or power-on sequence must be completed in any one control
unit attached to a channel before the 'select out' bypass function
(relay transfer) is started in another control unit.  Therefore,
the 'select out' bypass function should be completely automatic.
In any case, the 'select out' bypass function must not be interrupted,
but must be completed once it is started.

I/O INTERFACE OPERATION

Timing Chart

Timing considerations for three I/O interface operations are
summarized in Figure D-7, D-8, and D-9 (selector channel operation,
control unit in forced burst mode on multiplexor channel, and
multiplexing operation on the multiplexor channel).

Flow Charts

I/O interface operations is summarized in a series of flow charts
shown in Figures D-10 through D-16.

Figure D-7.  Timing Chart - Selector Channel

Figure D-8.  Timing Chart – Control Unit Forced Burst Mode on Multiplexor Channel

Figure D-9. Timing Chart - Multiplexing Operation on the Multiplexor Channel

AT DECISION BLOCKS INVOLVING SIGNAL LINES,
THE QUESTION TO BE RESOLVED IS --

    IS THE LINE UP.

THE PRESENCE OR ABSENCE OF (CH) AND *CU*
IN A BLOCK IMPLIES RESPONSIBILITY FOR
ACTION TAKEN OR THE DECISION MADE.

    (CH) MEANS CHANNEL
    *CU* MEANS CONTROL UNIT
    NEITHER MEANS BOTH

```
                                         *****
                                         *01 *
                                         * B3*
                                         *  *
                                          *
                                          |
                 |--------------------->|
                 |          NOTE =5   .V.
                 |                    B3  *.
                 |                  .*      *.
                 |                .*  (CH)    *.  YES
                 |               *. START POLL .*----
                 |                *.          .*     |
                 |                  *.      .*       |
                 |                    *. .*          |
                 |                     * NO          |
                 |                     |             |
                 |                     |             |
                 |                     |             |
                 |                    .V.            |
                 |                    C3  *.         |
                 |                  .* (CH) *.       |
                 |           NO   .*   START  *.     |
                 |           ----*.   INITIAL   .*   |
                 |                *. SELECTION .*     |
                 |                  *.      .*        |
                 |                    *. .*           |
                 |                     * YES          |
                 |                     |              |
                 |                     |              |
                 |                     |              |
                 |                     V              |
                 |          ****D3*********          |
                 |          *   (CH)      *          |
                 |          *   DEVICE    *          |
                 |          *   ADDRESS   *          |
                 |          *   TO BUS OUT *         |
                 |          *              *         |
                 |          *****************        |
                 |                     |             |
                 |                     |             |
                 |                     |             |
                 |                     V             |
                 |          ****E3*********          |
                 |          *              *         |
                 |          *   (CH)      *          |
                 |          *   250-NSEC  *          |
                 |          *   DELAY     *          |
                 |          *              *         |
                 |          *****************        |
                 |                     |             |
                 |                     |             |
                 |                     |             |
                 |                     V             |
                 |          ****F3*********          |
                 |          *              *         |
                 |          *   (CH)      *          |
                 |          *   RAISE     *          |
                 |          *   ADDRESS OUT *        |
                 |          *              *         |
                 |          *****************        |
                 |                     |             |
                 |                     |             |
                 |                     |             |
                 |                     V             |
                 |          ****G3*********          |
     *****        |          *              *        |
     * 01 *       |          *   (CH)      *         |
     * H2 *       |          *   400-NSEC  *         |
     *  *         |          *   DELAY     *         |
      *           |          *              *        |
      |           |          *****************       |
      |           |                     |            |
      |           |                     |            |
      V           |                     |<-----------
  ****H2*********  NOTE =1   V
  *              *  ****H3*********
  * FROM CHART 02 *  *              *
  * IF NOT LOWEST *  *   (CH)      *
  *   PRIORITY    *  *   RAISE     *
  *              *  *   SELECT OUT *
  *              *  *              *
  *****************  *****************
         |                  |
         |                  |
         |                  |
         |--------------->|<-----------
                    NOTE =1   V
                          J3  *.
                        .*      *.
                      .*  *CU*    *.  NO
                     *.  SELECT OUT .*----
                      *.          .*
                        *.      .*
                          *. .*
                           * YES
                           |
                           V
                          *****
                          *02 *
                          * B4*
                          *  *
                           *
```

NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

NOTE =5
REQUEST IN MAY BE USED TO INDICATE A NEED
FOR SERVICE BY A CONTROL UNIT. IT WOULD
RISE WHEN THE NEED FOR SERVICE ARRIVED AND
DROP WHEN THE NEED HAD BEEN SERVICED. THE
CHANNEL WOULD NORMALLY SERVICE ALL REQUESTS
ON THE CHANNEL PRIOR TO INITIATING A START I/O.
IF THE REQUEST IS TO SEND IN SUPPRESSABLE-TYPE
STATUS AND THE SUPPRESS-OUT LINE IS UP,
REQUEST IN WILL BE DROPPED WITHIN 1.5 USEC.

Figure D-10.  Flow Diagram - Start Interface Sequence (Sheet 1 of 3)

```
                                                          *****
                                                          *02 *
                                                          * B4*
                                                          * *
                                                           *
                                                           |
                                                           |
                                                          .V.
     NOTE =3  .*.                NOTE =2  .*.             B4  *.
           B2  *.                    B3  *.              .*    *.
         .* *CU* *.               .* *CU* *.      YES  .*  *CU*  *.
      NO .* CONTROL *.     YES  .* RECOGNIZE *.  .*------*. ADDRESS  *.
      *--*.   UNIT   .*<----*--*.   THIS    .*<-----    *.   OUT   .*
      |    *.  BUSY  .*          *. ADDRESS .*              *.     .*
      |      *.    .*              *.      .*                 *.  .*
      |        *.*.*                 *.*.*                      *.*
      |         * YES                 * NO                      * NO
      |         |                     |                         |
      |         |                     |                         |
      |        .V.                    |                        .V.
      |        C2  *.                 |                        C4  *.
      |       .*    *.                |                  NO  .*    *.
      |     .* *CU*   *. NO           |                  .*--*. *CU*  *.
      |    *.  STATUS  .*--*          |                  |  *. REQUIRE.*
      |     *. WAITING .*  |          |                  |   *. SERVICE.*
      |       *.     .*    |          |                  |     *.     .*
      |         *.  .*     |          |                  |       *.  .*
      |          * YES     |          V                  |        * YES
      |          |         |                             |        |
      |          |         |                             |        |
      |         .V.        |                             |       .V.
      |         D2  *.     |                             |       D4  *.
      |      .* *CU* *.    |                             |    .* *CU*  *. YES
      | YES .* STATUS  *.  |                             |    .*  DATA   *.--------
      *--*. FOR DEVICE .*  |                             |   *. TRANSFER .*       |
      |    *.ADDRESSED.*    |                            |    *.        .*         |
      |      *.     .*      |                            |      *.    .*           |
      |        *. .*        |                            |        * NO             |
      |         * NO        |                            |        |                |
      |         |           |                            |        |                |
      |        .V.          |                            |       .V.               |
      |        E2  *.       |                            |       E4  *.            |
      |      .* *CU* *.     |                            |     .* *CU*  *. NO      |
      | YES .* CONTROL *.   |                            | .SUPPRESSABLE .*--      |
      *--*. UNIT STATUS .*  |                            |  *.  TYPE   .*   |      |
      |    *.   ONLY   .*   |                            |    *. STATUS.*   |      |
      V      *.      .*     |                            |      *.    .*    |      |
             *.    .*       |                            |        * YES    |      |
              * NO          |                            |        |        |      |
      V        |            |                            |        |        |      |
      .        |            |                            |       .V.       |      |
      X        |            |                            |       F4  *.    |      V
    *****      |            |                            |     .* *CU* *.   |
    *04 *      |            |                            |    .* SUPPRESS .*--      |
    * A3*      |            |                            |   *.   OUT   .*   |      |
    * *        |            |                            |    *.      .*     V      |
     *         |            |                            |      *.  .*       .      |
               |            |                            |        * YES      X      |
               |            |                            |        |        *****    |
               |            |                            |        |        *04 *    |
               |            |                            |        |        * B3*    |
               |            |                            |        |        * *      |
               |            |                            |        |         *       |
               |            |                            |        |                 |
               |<-----------|                            |        |                 |
               V                                         |        |                 |
             *****                                       |------->|                 |
             *11 *                          NOTE =1      V        |                 |
             * B3*                     *****G4**********  *        |                 |
             * *                       *     *CU*      *           |                 |
              *                        *  PROPAGATE    *           |                 |
                                       *  SELECT OUT   *           |                 |
                                       *               *           |                 |
                                       ******************          |                 |
                                              |                    |                 |
                                              |                    |                 |
                                              |                    |                 |
                                             .V.                   |                 |
                                             H4  *.                |                 |
                          NOT-LOWEST       .*      *.     LOWEST   |                 |
                       *------------------*. PRIORITY .*------     |                 |
                       V                   *.  AS PER  .*    V     |                 |
                     *****                  *.CONFIGUR.*   *****   |                 |
                     *01 *                    *.     .*    *03 *   |                 |
                     * H2*                      *.  .*     * B3*   |                 |
                     * *                          *        * *     |                 |
                      *                                     *      |                 |
```

NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.


NOTE =2
ADDRESS-RECOGNITION REQUIRES DECODING OF
ALL ADDRESS BITS (EIGHT BITS PLUS PARITY).


NOTE =3
A CONTROL UNIT IS CONSIDERED BUSY IF IT IS
EITHER BUSY OPERATING A DEVICE OR IF IT IS
HOLDING STATUS.

Figure D-10.   Flow Diagram - Start Interface Sequence (Sheet 2 of 3)

```
                                    *****
                                    *03 *
                                    * B3*
                                    * *
                                     *
                                     |
                          ----------->|
                          |           |
                          |          .V.
                          |        B3 *.
                          |       .*    *.
                  | NO  .*  (CH)   *.
                  ----*.  SELECT IN  .*
                          *.        .*
                           *.      .*
                             *.  .*
                               * YES
                                |
                                |
ADDRESS OUT UP AT THIS TIME WILL    |
NORMALLY INDICATE UNAVAILABILITY.   |
                                |
                               .V.
                             C3 *.
                            .*    *.
                 NO  .*  (CH)   *.
                ----*.  ADDRESS  .*
              |      *.   OUT   .*
              |       *.      .*
              |         *.  .*
              |           * YES
              |            |
              |            |
              |            |
              |            V
              |   *****D3**********
              |   *              *
              |   *     (CH)      *
              |   *     DROP      *
              |   * ADDRESS OUT   *
              |   *              *
              |   ****************
              |            |
              |            |
              |            |
              ----------->|
                           |
            NOTE =1        V
            *****E3**********
            *              *
            *     (CH)      *
            *     DROP      *
            *  SELECT OUT   *
            *              *
            ****************
                  |
                  |
                  |<------------
                  |           |
                 .V.          |
               F3 *.          |
              .*    *.        |
             .*  (CH)   *. YES|
            *.  SELECT IN  .*---
              *.        .*
                *.    .*
                  *.  .*
                   * NO
                    |
                    V
                  *****
                  *01 *
                  * B3*
                  * *
                   *
```

NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

Figure D-10.   Flow Diagram - Start Interface Sequence (Sheet 3 of 3)

```
                                        *****
                                        *04 *
                                        * B3*
                                        *  *
                                        *
                                        |
                                        |
                                        V
                  *****B3*********                            .V.
                  *      *CU*     *                        B4  *.
                  *     RAISE     *                      .*      *.   NO
                  *OPERATIONAL IN *                ->*.  OPERATIONAL .*----
                  *               *                |  *.    IN     .*    |
                  *****************                |    *.      .*       |
                          |                        |      *.  .*         |
                          |                        |        *             |
                          |                        |        * YES         |
                          V                        |        |             |
                  *****C3*********                 |        V             |
                  *      *CU*     *                |  *****C4*********     |
                  *    DEVICE     *                |  *     (CH)      *    |
                  *   ADDRESS     *                |  *     DROP      *    |
                  *   TO BUS IN   *                |  *  ADDRESS OUT  *    |
                  *               *                |  *               *    |
                  *****************                |  *****************    |
                          |                        |        |             |
                          |                        |        |             |
                          |              NOTE =4   |        V             |
                         .V.                       |  *****D4*********     |
                       D3  *.                      |  *               *    |
                     .* (CH)  *.                   |  *     (CH)      *    |
                   .*  INITIAL  *.   YES           |  *  COMMAND BYTE *    |
                  *.  SELECTION  .*----            |  *   TO BUS OUT  *    |
                   *. SEQUENCE .*    |             |  *               *    |
                     *.      .*      |             |  *****************    |
                       *.  .*        |             |        |             |
                         *           |             |        |             |
                         * NO        |             |        V             |
                         |           |             |       .V.            |
                         |           |             |     E4  *.           |
                         |           |             |   .*      *.         |
                         |           |          NO .*   (CH)     *.       |
                         |           |          --*.  SUPPRESS  .*        |
                         |           |          |   *.   OUT  .*          |
                         |           |          |     *.    .*            |
                         |           |          |       *.  *             |
                         |           |          |        *                |
                         |           |          |        * YES            |
                         |           |          |        |                |
                         V           |          |        V                |
                  *****F3*********    |          |  *****F4*********       |
                  *      *CU*     *    |         |  *               *      |
                  *     DROP      *    |         |  *     (CH)      *      |
                  * REQUEST IN AT *    |         |  *     DROP      *      |
                  *  SELECTED CU  *    |         |  *  SUPPRESS OUT *      |
                  *               *    |         |  *               *      |
                  *****************    |          |  *****************      |
                          |           |          |        |                |
                          |           |          |-->|<----                |
                          |           |              |                     |
                          |           |              V                     |
                          |           |            .V.                     |
                          |           |          G4  *.                    |
                          |           |        .*  *CU* *.    YES|         |
                          |           |      .*   ADDRESS  *.----          |
                          |           |      *.     OUT    .*    |         |
                          |           |        *.       .*              |
                          |           |          *.   .*                |
                          |           |            *                    |
                          |           |            * NO                 |
                          |           |            |                    |
                          |           |<-----------                     |
                          |-->|<-------                                  |
                          V
                  *****H3*********
                  *      *CU*     *
                  *     RAISE     *
                  *  ADDRESS IN   *
                  *               *
                  *****************
                          |
                  ----->|
                  |      V
                  |    .V.
                  |  J3  *.
                  |.*      *.
               NO .*  (CH)   *.
                  *. OPERATIONAL.*
                   *.   IN    .*
                     *.      .*
                       *.  .*
                         *
                         * YES
                         |
                  ----->|
                  |      V
                  |    .V.
                  |  K3  *.
                  |.*      *.
               NO .*  (CH)   *.
                  *. ADDRESS IN.*
                   *.        .*
                     *.      .*
                       *.  .*
                         *
                         * YES
                         |
                         V
                       *****
                       *05 *
                       * A3*
                       *  *
                        *
```

NOTE =4
THE COMMAND BYTE MUST BE PLACED ON BUS OUT
AT LEAST 100 NSEC PRIOR TO RAISING
COMMAND OUT.

Figure D-11. Flow Diagram - Capture Interface Sequence

```
                              *****
                              *05 *
                              * A3*
                              * *
                               *
                               |
                             .V.
                          A3 *. *.
                        .*      *.  YES
                      .* (CH)     *._____
                      *. MULTIPLEXOR .*                |
                        *. CHANNEL .*                   |
                          *.    .*                      |
                            *. .*                        |
                            * NO                          |
                             |                            |
                             |                            |
                           .V.                          V
                        B3 *. *.              *****B4**********
                      .*      *.  YES         *              *
                    .* (CH)     *._____>*   (CH)        *
                    *. TEST I/O   .*          *   DROP        *
                      *.       .*             *   SELECT OUT  *
                        *. .*                 *              *
                        * NO                  ****************
                         |                            |
                         |                            |
            NOTE =4      |<_____|
                       V
                *****C3**********
                *              *
                *   (CH)        *
                *   RAISE       *
                *   COMMAND OUT *
                *              *
                ****************
                        |                CONTROL UNIT PROCESSES COMMAND
                        |
            _____>|
           |          .V.
           |       D3 *. *.
           |     .*      *.
      NO .*  .* *CU*       *.
        |____*. COMMAND OUT .*
                *.       .*
                  *. .*
                  * YES
                   |
                   |
                   V
           *****E3**********
           *              *
           *   *CU*        *
           *   DROP        *
           *   ADDRESS IN  *
           *              *
           ****************
                   |
                   |<_____
                 .V.           |
              F3 *. *.          |
            .*      *.  YES     |
          .* (CH)     *._____|
          *. ADDRESS IN .*
            *.       .*
              *. .*
              * NO
               |
               |
               V
        *****G3**********
        *              *
        *   (CH)        *
        *   DROP        *
        *   COMMAND OUT *
        *              *
        ****************
               |
               |
             .V.
          H3 *. *.
        .*      *.  YES
      .* INITIAL  *._____
      *. SELECTION .*                    |
        *. SEQUENCE .*                    |
          *.     .*                        |
            *. .*                           |
            * NO                             |
             |                               |
             |                               |
           .V.                              |
        J3 *. *.                            |
      .*      *.  NO                         |
    .* DATA     *._____|
    *. TRANSFER .*                            |
      *.     .*                               |
        *. .*                                 |
        * YES                                 |
         |                                    |
         |                                    |
         V                                    V
       *****                               *****
       *06 *                               *08 *
       * A4*                               * A4*
       * *                                 * *
        *                                   *
```

NOTE =4
THE COMMAND BYTE MUST BE PLACED ON BUS OUT
AT LEAST 100 NSEC PRIOR TO RAISING
COMMAND OUT.

Figure D-12.  Flow Diagram - Command Response

```
                                              *****
                                              *06 *
                                              * A4*
                                              *   *
                                               *
                                               |
        A1              A2               A3          .V.
      .* *.           .* *.            .* *.        A4
   NO .* *CU* *.   YES .* *CU* *.   YES .* *CU* *.  YES .* *CU* *.
    *.FIRST DATA.*<---*.SUPPRESSABLE.*<---*.SELECT OUT.*<---*.SUPPRESS.*
    *.  BYTE  .*      *.  DATA  .*        *.      .*        *.  OUT  .*
      *. .*             *. .*               *. .*             *. .*
       * YES             * NO                * NO              * NO
        |                 |                   |                 |
       .V.                |                   |                 |
       B1                 |                   |                 |
     .* *.                |                   |                 |
   .* *CU* *. NO          |                   |                 |
   *. SUPPRESS .*         |                   |                 |         *****
   *. OPTION .*           V                   V                 |         *06 *
     *. .*                                                      |         *C4*
      * SUP                                                     |         *  *
       |                                                        |          |
       |                                                        |          |
       |              .*.                 .V.                    |          |
       |             C3 *.               C4 *.                   |          |
       |          .* *CU* *.          .* *CU* *.                 |          |
       |        NO .* CHANNEL *.    NO .* DATA *.                |          |
       |---------->*. END STATUS.*<---*. TRANSFER.*<------------|----------|
                   *.  READY  .*      *.  READY .*
                     *. .*              *. .*
                      * *                 * YES
                       |                   |
                       V                   |
                     *****                 |
                     *08 *                 |
                     *A4 *                .V.
                     *  *                 D4
                                        .* *.
                                     .* *CU* *. YES    *****D5**********
     NOTE =1  .V.                    *.IN-BOUND.*----->* *CU*          *
             D2                      *.  DATA .*        * DATA BYTE     *
           .* *.                       *. .*            * TO BUS IN     *
        NO .* *CU* *.                   * NO            *               *
        *.SELECT OUT.*                   |              *****************
          *.      .*                     |                     |
            *. .*                        |              <------|------<--
             * YES                       |              |              |
              |                          |             .V.             |
       .V.                              .V.            E5             |
      E1                 .V.         *****E4*********  .* *.           |
    .* *.               E2           * *CU*        *  .* *CU* *. YES  |
 .* *CU* *.          .* (CH) *.      * RAISE       * *.COMMAND OUT.*--|
 *. FORCE .* YES  .*SUPPRESSING.* YES* SERVICE IN  *   *.      .*
 *. BURST .*--->.* DATA .*           *****************   * NO
 *.OPERATION*      *. .*                  |              |
   *. .*            * NO                  |          <---|-----<---
    * NO            |                    .V.         |            |
     |             |                     |          .V.          |
     V             V                     |          F5           |
 *****F1*******  *****F2*******          |        .* *.          |
 * *CU*      *   * (CH)      *           |        .* *CU* *. YES |
 * DROP      *   * DROP      *          .V.       *.SERVICE OUT.*-|
 *OPERATIONAL*   *SUPPRESS OUT*         F4         *.      .*
 *  IN      *    *            *       .* *.          *. .*
 *************    *************      .* (CH) *.        * NO
       |               |          NO .*SERVICE IN.*
    <--|---            |          |---*.      .*
    |     |            |              *. .*
   .V.    |            |               * YES
   G1     |            |                |
 .* *.    |            |                |
.* (CH) *.| YES        |               .V.
*.OPERATIONAL.*--|     |               G4
*.  IN  .*       |     |             .* *.
  *. .*          |     |          .* (CH) *. YES
   * NO          |     |          *.CHANNEL.*---
    |            |     |          *. STOP .*    |
    V            V     |            *. .*       |
  *****        *****   |             * NO       |
  *01 *        *06 *   |              |         |
  *B3 *        *C4 *   |              |         |
  *  *         *  *    |              V         |
                       |             .V.        |
                       |             H4         |
CHANNEL PROCESSES     .V.          .* *.      *****H5**********
INBOUND BYTE, IF ANY--- *****H3*********  .* (CH) *.      * (CH)          *
                        * (CH)      * YES .*OUT-BOUND.*    * RAISE         *
                        * DATA BYTE *<----*. DATA .*       * COMMAND OUT   *
                        * TO BUS OUT*       *. .*          *               *
                        *            *       * NO          *****************
                        *************        |                   |
                              |              |                   V
                              |              |                 *****
                             .V.             |                 *07 *
                        *****J3*********     |                 *B4 *
                        * (CH)      *        |                 *  *
                        * 100-NSEC  *--------|
                        * DELAY     *        |
                        *            *       V
                        *************
```

NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

```
                        *****K4**********
                        * (CH)          *
                        * RAISE         *
                        * SERVICE OUT   *
                        *               *
                        *****************
                              |
                              V
                            *****
                            *07 *
                            *B4 *
                            *  *
```

Figure D-13.   Flow Diagram - Data Transfer (Sheet 1 of 2)

```
                                                            *****
                                                            *07 *
                                                            * B4*
                                                            *  *
                                                            *
                                                            *
          | NO                                     >|
          .*.                                       .V.
        B2  *.                                    B4  *.
      .*      *.                            NO  .*      *.
    .*   *CU*   *.                            .*   *CU*   *.
   *.  COMMAND OUT *<---------------------------------*.  SERVICE OUT .*
    *.          .*                            *.          .*
      *.      .*                                *.      .*
        *.  .*                                    *.  .*
          *                                         *
          * YES                                     * YES
          |                                         |
CONTROL UNIT SETS UP                          CONTROL UNIT PROCESSES
CONTROLS TO STOP                              OUTBOUND BYTE, IF ANY
DATA TRANSFER                                     |
          |                                       |
          V                                       V
   *****C2**********                       *****C4**********
   *    *CU*       *                       *    *CU*       *
   *    DROP       *                       *    DROP       *
   *  SERVICE IN   *                       *  SERVICE IN   *
   *              *                        *              *
   ****************                        ****************
          |                                       |
          |                                       |
          |<----          <----                   |<----
          .V.     |            |                   .V.      |
        D2  *.    |            |                  D4  *.     |
      .*      *.  |            |                .*      *. YES|
    .*   *CU*   *. YES         |              .*   *CU*   *.--
   *.  SELECT OUT .*--         |             *.  SERVICE IN .*
    *.          .*   |         |              *.          .*
      *.      .*     |         |                *.      .*
        *.  .*       |         |                  *.  .*
          *          |         |                    *
          * NO       |         |                    * NO
          |          |         |                    |
          |          |         |                    |   A CHANNEL MAY NEED TO
          |          |         |                    |   TEMPORARILY HOLD UP DATA TRANSFER.
          |          |         |                    |   IT WILL ACCOMPLISH THIS BY RAISING
          |          |     | YES                    |   SUPPRESS OUT. SUPPRESSION OF THE
          .V.        |    .*.                       |   NEXT DATA BYTE CAN BE ASSURRED
        E2  *.       |  E3  *.                       |   ONLY IF SUPPRESS OUT IS UP
      .* *CU*  *.     |.*      *.                    |   AT LEAST 250 NSEC PRIOR TO THE
    .*   FORCE    *. YES V                           |   FALL OF PRECEEDING SERVICE OUT.
   *.   BURST      .*--->*.  SERVICE IN .*            |
    *.OPERATION..*        *.          .*             |
      *.      .*            *.      .*               |
        *.  .*                *.  .*                 |
          * NO                  * NO                 |
          |                       |                  |
          V                       V                  V
   *****F2**********       *****F3**********   *****F4**********
   *    *CU*       *       *    (CH)       *   *    (CH)       *
   *    DROP       *       *    DROP       *   *    DROP       *
   *OPERATIONAL IN *       *  COMMAND OUT  *   *  SERVICE OUT  *
   *              *        *              *    *              *
   ****************        ****************    ****************
          |                       |                  |
          |<----                  |                  |
          .V.    |                 |                 V
        G2  *.   |              .V.               *****
     NO .* (CH) *.              G3  *.            *06 *
   ----*.  SERVICE IN .*       .* *CU*  *.        * A4*
    *.          .*           .*  CHANNEL   *. NO   *  *
      *.      .*            *.  END STATUS  .*----  *
        *.  .*               *.AVAILABLE..*
          * YES                *.      .*
          |                       *.  .*
          |                         * YES
          .V.    |                  |
        H2  *.   |                  V
      .* (CH) *. YES|            *****
    .* OPERATIONAL .*----        *08 *
   *.    IN      .*              * A4*
    *.          .*                *  *
      *.      .*                  *
        *. .*
          * NO
          |
    |----...-->|  -
          |    |
          V
   *****J2**********
   *    (CH)       *
   *    DROP       *
   *  COMMAND OUT  *
   *              *
   ****************
          |
          |
          |<----
          .V.    |
        K2  *.   |
      .* (CH) *. YES|
    .* OPERATIONAL .*----
   *.    IN      .*
    *.          .*
      *.      .*
        *. .*
          * NO
          |
          V
        *****
        *01 *
        * B3*
        *  *
        *
```

Figure D-13.   Flow Diagram - Data Transfer (Sheet 2 of 2)

```
                                                              *****
                                                              *08 *
                                                              * A4*
                                                              *  *
                                                              *
          .*.                                                 V
        A2   *.                                     *****A4**********
      .* (CH) *.                                    *              *
     .*  INITIAL  *.     NO                         *    *CU*       *
  .*  SELECTION   *.--------                        *  STATUS BYTE  *
   *.  SEQUENCE  .*       |                         *   TO BUS IN    *
     *.        .*         |                         *              *
       *.    .*           |                         ****************
         *. .*            |                                 |
          * YES           |                                 |
                          |                                 |
          .*.             |                             .*.  |<--------
        B2   *.           |                           B4   *.        |
      .* (CH)  *.  NO      |                        .* (CH) *.  YES  |
   V .*  ZERO STATUS *.----                        *. COMMAND OUT .*----
     *.    BYTE    .*                                 *.        .*
       *.        .*                                     *.    .*
         *.    .*                                         *. .*
          * YES                                            * NO
           |                                                |
          .*.                                               |
        C2   *.                                             |
      .* (CH)  *.   YES                                 .*.  |
     *.  TEST I/O  .*------                           C5   *.
       *.        .*     |                           .* (CH) *.  YES
         *.    .*       |                          *. SERVICE OUT .*----
          * NO          |                            *.        .*
           |            |                              *.    .*
           V            |                                *. .*
     *****D2**********   |                                 * NO
     *              *    |                                  |
     *   (CH)       *    |                                  |
     *   DROP       *    |                            *****D5**********
     *  SELECT OUT  *    |                            *              *
     *              *    |                            *    *CU*       *
     ****************    |                            *   RAISE       *
           |             |                            *  STATUS IN    *
           |-----------> |<                           *              *
                                                      ****************
                                                            |
                                                            |
      .*.          .*.          .*.          .*.          .*.
    E1   *.      E2   *.      E3   *.      E4   *.      E5   *.
  .* (CH) *.   .* (CH) *.   .* (CH) *.   .* (CH) *.   .* (CH) *.   NO
 *. SUPPRESS .*<-*. COMMAND .*<-*. MULTIPLEXOR .*<-*.  CAN   .*<-*. STATUS IN .*-----
   *.  OUT  .*     *.CHAINING.*    *.CHANNEL.*     *. STATUS BE .*     *.      .*
     *.   .*         *.    .*        *.   .*       *. ACCEPTED .*        *.  .*
      * YES           * NO            NO            *.     .*              *
       |               |                            * NO
       |               |
 *****F1**********    .*.                      *****F4**********
 *              *   F2   *.   NO               *              *
 *   (CH)       *  .* (CH) *.                  *   (CH)       *
 * RAISE        *  *. SUPPRESS .*---           * RAISE        *
 * SUPPRESS OUT *    *.  OUT  .*   |           * COMMAND OUT  *
 *              *      *.   .*     |           *              *
 ****************       * YES      |           ****************
       |                 |         |                 |
 *****G1**********  *****G2**********  *****G3**********   .*.
 *              *  *              *   *              *   G4   *.
 *   (CH)       *  *   (CH)       *   *   (CH)       *  .* (CH) *.
 *  250-NSEC    *<-*  DROP        *   *  DROP        *<-*. MULTIPLEXOR .*
 *  DELAY       *  * SUPPRESS OUT *   *  SELECT OUT  *  *. CHANNEL .*
 *              *  *              *   *              *    *.   .*
 ****************  ****************   ****************      * YES
       |                 |                 |
       |-------->|<-------|                 |
       V                                    |
 *****H1**********                          |
 *              *                           |
 *   (CH)       *                           |
 * RAISE        *                           |
 * SERVICE OUT  *                           |
 ****************                           |
       |                                    |
       |----------------------->  V  <------|
                               >|<
                          NO
                         .*.
                       J2   *.
                     .* *CU* *.         NO  .*.
                    *. COMMAND OUT .*<------*. *CU* *.
                      *.        .*          *. SERVICE OUT .*
                        *.    .*              *.        .*
                          * YES                 * YES
                           |
                           V
                         *****
                         *10 *
                         * B3*
                         *  *
```

COMMAND CHAINING IS INDICATED
IF SUPPRESS OUT IS UP AT THE
CONTROL UNIT AT THIS TIME.

```
                         *****K3**********
                         *              *
                         *    *CU*       *
                         *   DROP        *
                         *  STATUS IN    *
                         *              *
                         ****************
                                |
                                V
                              *****
                              *09 *
                              * A4*
                              *  *
```

Figure D-14.  Flow Diagram - Status Transfer (Sheet 1 of 2)

```
                                              *****
                                              *09 *
                                              * A4*
                                              *  *
                                               *
                                               |
                                               |<---------+
                                               v          |
                                             .V.          |
                                        A4 .*   *.        |
                                         .*       *.      |
                                       .*  (CH)     *. YES|
                                       *.  STATUS IN  .*--+
                                        *.         .*
                                          *.     .*
                                            *. .*
                                             * NO
                                             |
                                             |
                                             v
                                     *****B4**********
                                     *              *
                                     *    (CH)      *
                                     *    DROP      *
                                     *  SERVICE OUT *
                                     *              *
                                     ****************
                                             |
                                             |
                                             v
                                           .V.
                                      C4 .*   *.
                                       .*       *.  YES
                                     .*  (CH)     *.-----+
                                     *. MULTIPLEXOR .*    |
                                      *. CHANNEL  .*      |
                                       *.       .*        |
                                         *.   .*          |
                                           * NO           |
                                           |              |
                                           |              |
                                           v              |
         .*.                             .V.              |
      D3 .*  *.                     D4 .*   *.            |
    NO .*  (CH) *.              NO .*  (CH)   *.          |
    *.   CHAINING .*--<---------*.  ZERO STATUS .*        |
      *.       .*                 *.          .*          |
        *.   .*                     *.      .*            |
          * YES                       * YES              |
          |                             |                 |
          |                             |                 |
          v                             |                 |
        .V.                             |                 |
     E3 .*   *.                         |                 |
      .*  (CH)  *.                      |                 |
    NO .* CHANNEL *.                    |                 |
    *. END STATUS .*                    |                 |
      *. ONLY  .*                       |                 |
        *.   .*                         |                 |
          * YES                         |                 |
          |                             |                 |
          |         +------>|           |                 |
          |         |       |           |                 |
          |         |     .V.           |                 |
          |         |  F3 .*  *.         |                 |
          |         |  .* *CU* *.        |                 |
       NO .*  DEVICE   *.                |                 |
          +---------*. END STATUS .*     |                 |
                     *.AVAILABLE.*       |                 |
                       *.   .*           |                 |
                         * .*            |                 |
                          *              |                 |
                          |              |                 |
                          v              |                 |
                        *****            |                 |
                        *08 *            |                 |
                        *A4*             |                 |
                         *               .V.               |
                                      G4 .*  *.            |
                                       .* (CH) *.          |
                                     NO .* IS THERE *.     |
                                     *. COMMAND TO  .*     |
                                       *. EXECUTE .*       |
                                         *.    .*          |
                                           * YES           |
                                           |               |
                                           v               |
                                         *****             |
                                         *06 *             |
                                         *A4*              |
                                          *                |
      NOTE =1                                              |
****H2**********                                           |
*              *                                           |
*    (CH)      *                                           |
*    DROP      *                                           |
*  SELECT OUT  *                                           |
*              *                                           |
****************
          |
          |
-------->|<-----------------------------------------------+
|  NOTE =1    .V.
|        J2 .*   *.
|         .* *CU* *.
|YES .* SELECT OUT .*
+---*.           .*
       *.      .*
         *.  .*
           * NO
           |
           |
           v
****K2**********
*              *
*    *CU*      *
*    DROP      *
*OPERATIONAL IN*
*              *
****************
           |
           v
         *****
         *01 *
         * B3*
          *
```
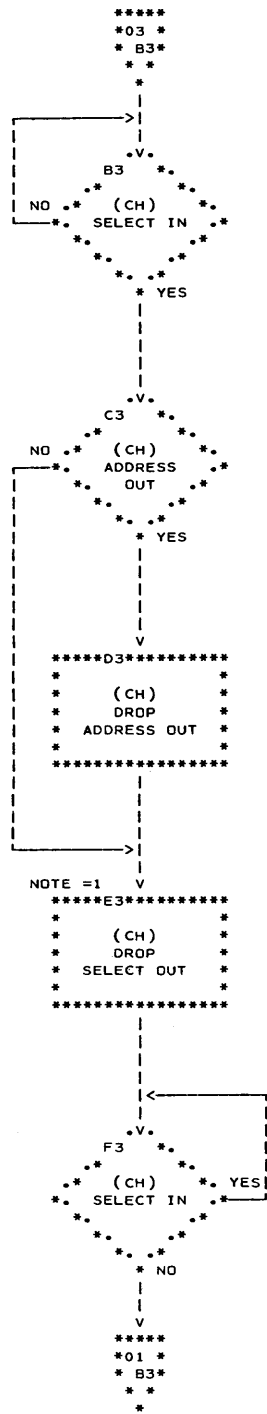
NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS.
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
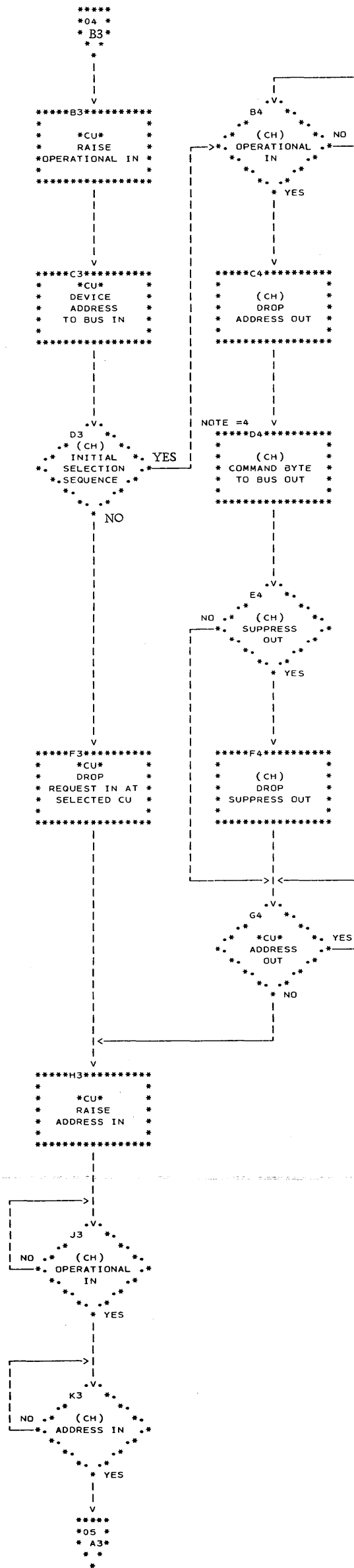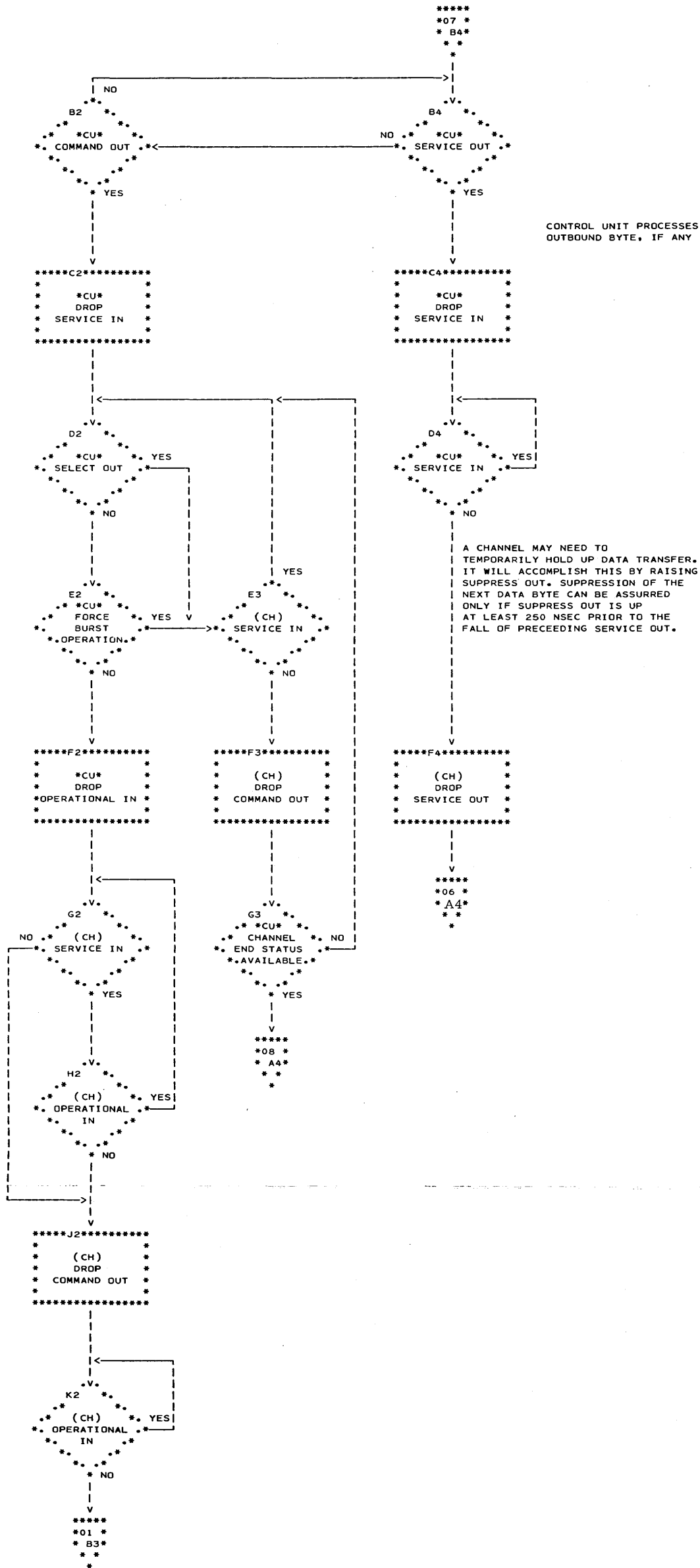SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

Figure D-14. Flow Diagram - Status Transfer (Sheet 2 of 2)

```
                              *****
                              *10 *
                              * B3*
                              * *
                               *                CONTROL UNIT WILL CAUSE STATUS
                               |                TO BE STACKED AT THIS TIME.
                               |
                               |
                               V
                     *****B3**********
                     *               *
                     *     *CU*      *
                     *     DROP      *
                     *   STATUS IN   *
                     *               *
                     *****************
                               |
                               |
                               |
                               |<----------
                               |          |
            NOTE =1       .V.            |
                          C3  *.           |
                        .*      *.         |
                      .*   *CU*   *.  YES|
                      *. SELECT OUT .*----
                        *.        .*
                          *.    .*
                            *. .*
                             * NO
                             |
                             |
                             |
                             |
                             V
                     *****D3**********
                     *               *
                     `     *CU*      *
                     *     DROP      *
                     *OPERATIONAL IN *
                     *               *
                     *****************
                               |
                               |
                               |
                               |<----------
                               |          |
                             .V.           |
                             E3  *.          |
                           .*      *.        |
                         .*   (CH)   *.  YES|
                         *. OPERATIONAL .*----
                         *.    IN     .*
                           *.        .*
                             *.    .*
                               *. .*
                                * NO
                                |
                                |
                                |
                                |
                                V
                        *****F3**********
                        *               *
                        *     (CH)      *
                        *     DROP      *
                        *  COMMAND OUT  *
                        *               *
                        *****************
                                |
                                |
                                V
                              *****
                              *01 *
                              * B3*
                              * *
                               *
```
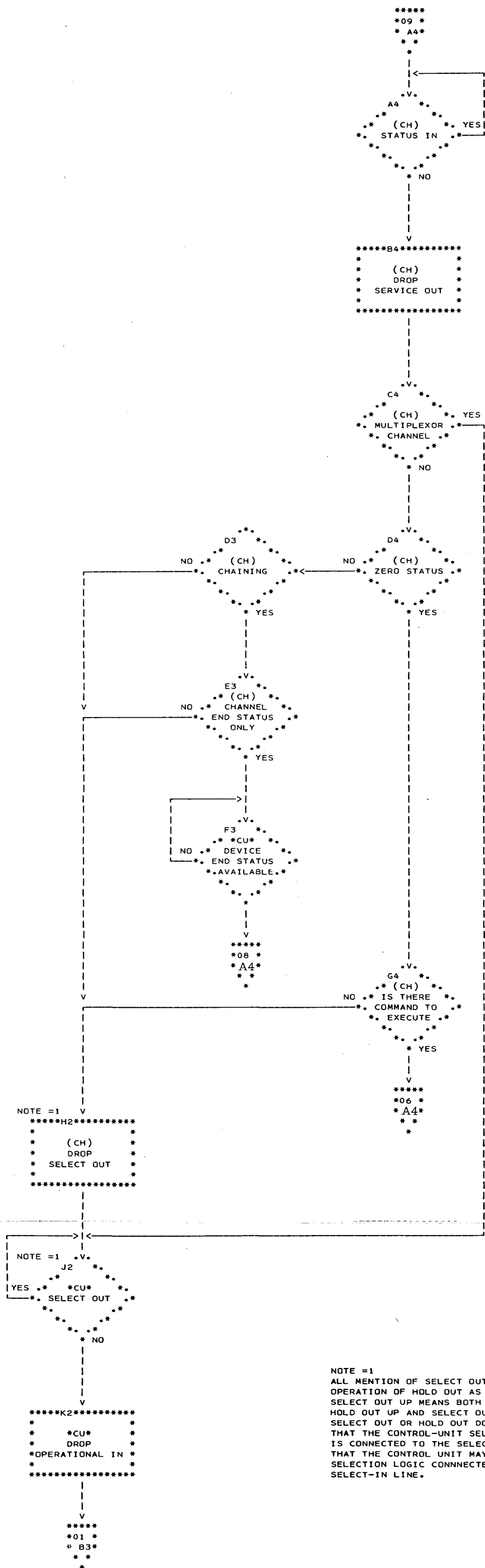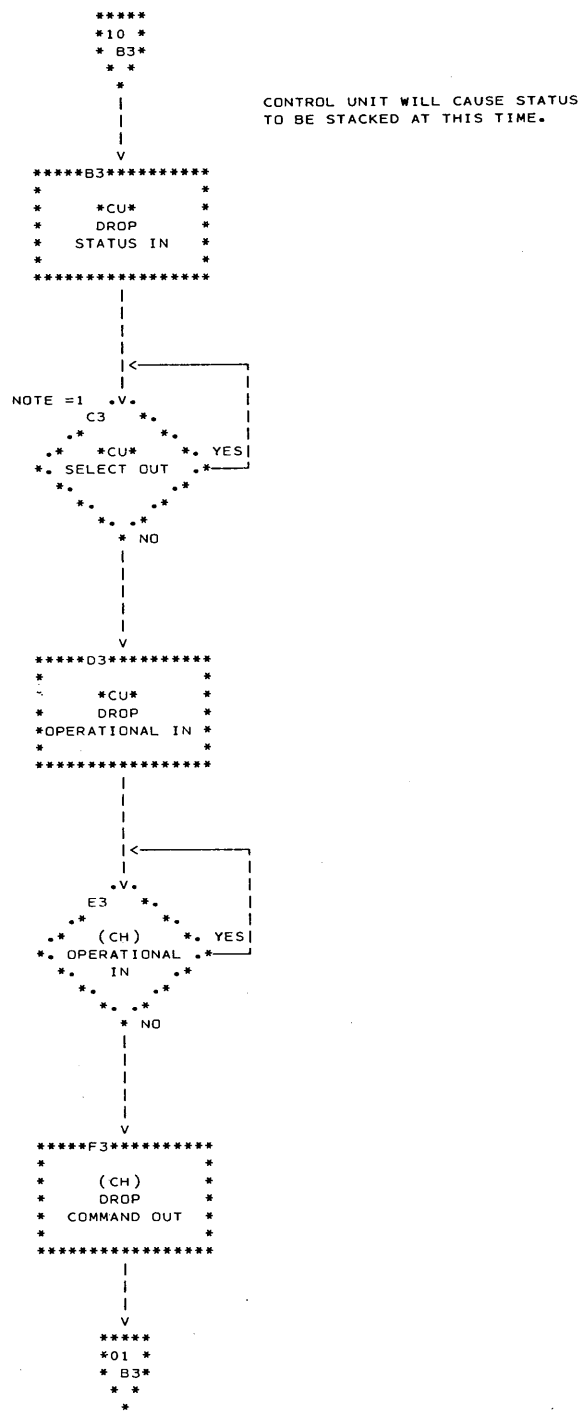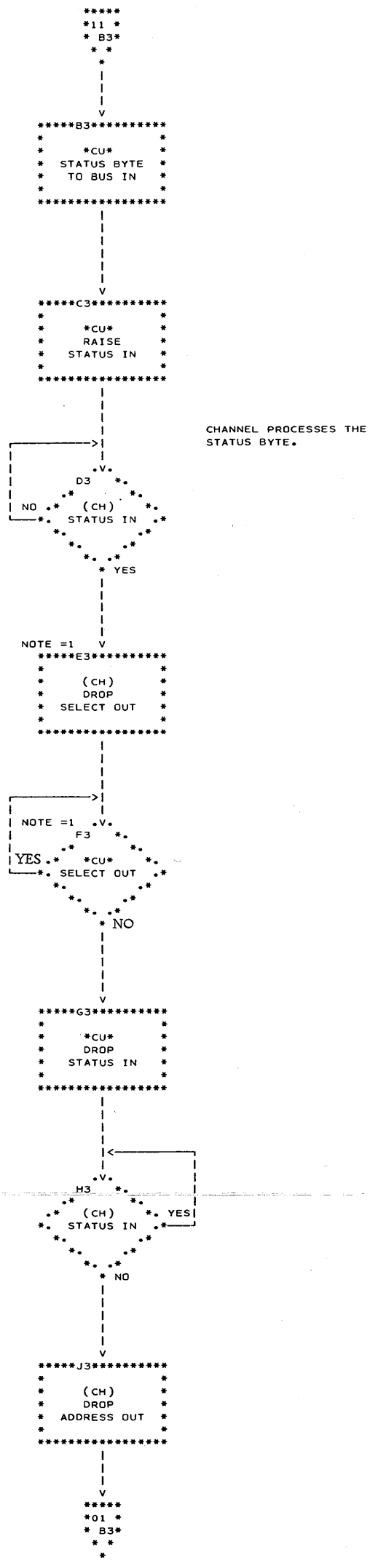
NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

Figure D-15.   Flow Diagram - Stack Status

```
                              *****
                              *11 *
                              * B3*
                              * *
                               |
                               |
                               V
                         ****B3*********
                         *             *
                         *  *CU*       *
                         * STATUS BYTE *
                         *  TO BUS IN  *
                         *             *
                         ***************
                               |
                               |
                               |
                               V
                         *****C3*********
                         *             *
                         *  *CU*       *
                         *  RAISE      *
                         * STATUS IN   *
                         *             *
                         ***************
                               |                CHANNEL PROCESSES THE
              -------->|                        STATUS BYTE.
              |        |
              |       .V.
              |      D3  *.
              |     .*     *.
              | NO .*        *.
              ----*.  (CH)   .*
                    *. STATUS IN .*
                      *.       .*
                        *.   .*
                          * YES
                          |
                          |
             NOTE =1      V
          *****E3*********
          *             *
          *  (CH)       *
          *  DROP       *
          * SELECT OUT  *
          *             *
          ***************
                |
                |
       -------->|
       |  NOTE =1   .V.
       |          F3  *.
       |         .*     *.
       |YES.*   *CU*     *.
       ----*.  SELECT OUT .*
             *.         .*
               *.     .*
                 * NO
                 |
                 |
                 |
                 V
          *****G3*********
          *             *
          *  *CU*       *
          *  DROP       *
          * STATUS IN   *
          *             *
          ***************
                |
                |          <-------
                |<---------       |
               .V.               |
              H3  *.             |
            .*     *.            |
          .*  (CH)   *. YES      |
          *. STATUS IN .*--------
            *.       .*
              *.   .*
                * NO
                |
                |
                |
                V
          *****J3*********
          *             *
          *  (CH)       *
          *  DROP       *
          * ADDRESS OUT *
          *             *
          ***************
                |
                |
                V
              *****
              *01 *
              * B3*
              * *
              *
```

NOTE =1
ALL MENTION OF SELECT OUT ASSUMES PROPER
OPERATION OF HOLD OUT AS WELL. THUS,
SELECT OUT UP MEANS BOTH SELECT OUT AND
HOLD OUT UP AND SELECT OUT DOWN MEANS EITHER
SELECT OUT OR HOLD OUT DOWN. IT IS ASSUMED
THAT THE CONTROL-UNIT SELECTION LOGIC
IS CONNECTED TO THE SELECT-OUT LINE. NOTE
THAT THE CONTROL UNIT MAY ACTUALLY HAVE THE
SELECTION LOGIC CONNNECTED TO THE
SELECT-IN LINE.

Figure D-16.   Flow Diagram - Control Unit Busy

INTRODUCTION

This appendix describes the actions of the 9020D/E System when errors
are detected in a 9020D/E element or unit.  The discussion is limited
primarily to a description and explanation of the way in which the
built-in equipment for error-processing functions.  It must be under-
stood, however, that the complete system response to an error is of
necessity a combination of reactions by both program and equipment.
Where it is important to the discussion, certain programming function
will be discussed.  Considerable flexibility of program action is
permissible, making possible a total system error response as soph-
isticated as desired.

  Errors occurring in the PAM, TCU, DASF, RCU, and DAU are also
treated in this appendix, although most errors which occur in those
elements are communicated to the system via the usual input/output
control programs.  Errors which result in an ELC from the PAM, TCU,
DASF, or RCU units will be handled as an external interruption by
the receiving CE(s).  There is no special hardware which causes
unusual action in these elements, such as exist in the CE, IOCE, DE
and SE.  The equivalent of logout information in PAM, DAU, RCU, DASF,
and TCU's is obtained as sense data through regular program operation.

GENERAL CONSIDERATIONS

A useful preliminary to a detailed discussion of error processing
will be a summary of the types of errors which affect each of the
elements, and a brief examination of the kind of action which can
result.

Computing Element (CE)

Four broad categories of errors are of concern to a CE:

    1.    The inability of a CE to obtain, upon request a cycle
          from a Storage Element, or Display Element.

    2.    Errors which the CE detects in its own error detection logic

    3.    Errors which are signalled to the CE by an SE or DE with
          which it is currently communicating or by an IOCE which the
          CE is controlling.

    4.    Errors which are manifested as External, Program, or I/O
          interruptions from other elements, or Condition Codes.

If a CE is unable to obtain a cycle from a storage unit, SE or DE,
it will conclude, in general, that either a program error or an

equipment malfunction has occurred. If the circumstances indicate
a program error, a program interruption will occur; otherwise a
machine check interruption will be taken with appropriate inter-
element error signals generated. Where the inability to obtain a
storage cycle occurs on a reference to the PSA, the CE will attempt
to obtain a corresponding location in an alternate PSA.

After a delay period of approximately 11 ms, errors detected by
the CE in its own error detection equipment will cause a machine
check interruption, logout, and appropriate inter-element error
signals to be generated. If the error detected is OBS, the CE will
set the OBS bit in the DAR register; if the error is an OTC, the
CE will set its CE Own Element Check bit in the DAR. An ELC signal
is not sent to other CE's.

If an SE or DE detects an error in its own equipment when work-
ing with a CE, this error signal is communicated to the using CE.
If allowed (ILOS or IDES bit off), the CE will cause the SE or DE to
stop, and a CE machine check interruption will occur, followed
(normally) by a programmed logout of the SE or DE. It is necessary
to proceed in this fashion in order to permit the system to obtain
sufficient data for malfunction isolation and subsequent recovery.
An error in the IOCE will be signalled to the CE as a special
Machine Check interruption. This mechanism is used to allow the CE
to respond quickly and orderly to IOCE malfunctions. The CE will not
logout, but can immediately enter a program for diagnosis of the
IOCE problem.

The last category of errors with which the CE is concerned
directly are those which are signalled via the various interruption
facilities. These are external, program, and I/O interruption;
their handling is a programming function and will not be of immediate
concern here since no unusual equipment functions are involved. It
should be pointed out again, however that the processing of these
interruptions must be considered in the overall sense as a sign-
ificant part of the system malfunction handling technique. The
type of error communicated via an interruption will usually orig-
inate in an element external to the CE. Hence, the programming
response must integrate these into a complete, cohesive malfunction
handling scheme.

Input/Output Control Element (IOCE)

There are three categories of errors in the IOCE which are of con-
cern here:

1. The inability of an IOCE to obtain, on request, a cycle from
a storage element.

2. Errors which the IOCE detects in its own error detection
logic.

3. Errors which are signalled to the IOCE by an SE with which
it is currently communicating.

If an IOCE is unable to obtain a cycle from a storage element, it
will in general conclude that either the address it is using is
invalid, indicating a programming error, or that an equipment
malfunction has occurred. If the circumstances indicate that the

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cause is an invalid address, and an I/O operation was in process, then the IOCE will notify the using CE via an I/O interruption with a program check in the channel status word that this has occurred. If the cause was an invalid address and an I/O operation was not in process, the IOCE will take a program interrupt into its own PSA area in MACH.

If the invalid address indication occurs during IOCE logout, the IOCE will request a new PSA from the CE. If the circumstances indicate an equipment malfunction, then the IOCE will generate the necessary inter-element signals and will perform a logout to the PSA.

Errors detected by the IOCE in its error detection logic include those which occur in the common logic area and those which occur in the channels. An error occurring in the IOCE common logic or multiplexor channel will cause the IOCE to request a logout via a special machine check interruption request to the controlling CE. An error occurring in the IOCE's selector channels will cause a logout of that channel via an I/O interruption, unless the selector channel is performing a Test Channel operation; in this case the logout will be done via the special machine check interruption. In both cases, appropriate inter-element error signals are generated.

If an SE working with an IOCE detects an error, it is communicated to the IOCE, which will cause the SE to stop if the ILOS bit is off. The IOCE will request, via the special machine check interruption, that the IOCE be allowed to logout. This would then (normally) be followed by a programmed logout of the SE by the controlling CE.

In each case of IOCE malfunction, every possible effort is made to reduce its effect on the IOCE's handling of data from channels not affected. It is assumed that most errors are of a transient, self-clearing nature, and that continuation is usually possible. In the case of a channel only logout, IOCE-Processor operation resumes at the completion of the channel logout. IOCE-Processor operation is always stopped as a result of a CLU logout, and is resumed only upon command from the controlling CE.

Storage Element (SE)

Malfunctions in the SE are classified in two groups:

1.  Storage Checks - these are malfunctions resulting from internal storage equipment parity check, address check, tag mismatch, normal Op check or multi-accept check. Detection of this type error will cause an ELC to all CE's plus a storage check signal to the using IOCE or Data or Address check to the using CE.

2.  Others - These including CCR parity check, Double Cycle Timeout, OBS, OTC, and power failure. CCR parity, OBS and OTC, cause a pulse ELC to all CE's. Power failure causes a static (level) ELC to all CE's including normal Power Off.

The significance of this grouping is that basic storage operations are not directly affected as a result of a malfunction in (2) above. These malfunctions are considered to be in equipment external to the basic accessing paths of the SE; thus, the SE does not take any action insofar as error processing or special procedures on these malfunctions.

Those malfunctions in (1), i.e., storage checks, could immediately affect the validity of the storage data; thus, a signal is sent to the using element. When a storage check occurs, the SE will complete its current cycle and wait 2.5 us before beginning a new cycle. During this 2.5 us, the using element may issue a logout stop signal to the SE (Figures E-1 and E-2). This signal will cause the storage to refuse any further requests for service until it has been logged out or told to resume action by a CE.

STORAGE ACCESS MALFUNCTIONS

This section describes the actions which occur in the CE and the IOCE when either of these elements is unable to obtain a requested storage cycle from an SE.

The diagrams which accompany the explanations in this and all following sections are intended as functional representations of the sequence of events. All actions shown are accomplished by 9020D/E hardware; however, the diagrams do not necessarily reflect the manner in which the functions are implemented.

For ease of reference, each separate function on a diagram is enclosed. These enclosures are numbered sequentially on the diagram. They will all be referred to as "boxes", e.g., box 12, in the text. The rectangular "boxes" indicate an action or procedure. The diamond shaped "boxes" indicate decision points in the flow, with exits reflecting the outcome of the decision.

CE Actions

Figure E-3 portrays the sequence of events which will occur when a CE requests access to an SE for a cycle, either to read or store a word. It is assumed that the address of the desired storage location has been determined in the CE and the CE then checks the selected SE interface lines. Assuming the SE is not stopped (no exit, box 2) and is ready (no exit, box 3), the CE will issue a Select to the SE and enter a 25 millisecond timedown period to await the SE's honoring its request (box 4). This delay is present to account for situations where the CE is low on the priority chain, with the possibility that an extended I/O operation is occurring in the SE. While the CE is in the 25 ms. timedown period it continues to monitor the SE Stopped and Not Ready lines (boxes 6 and 7). If the SE accepts the CE request within this interval (yes exit, box 5), the storage cycle is used by the CE.

Return to box 2. If the SE Stopped line is active (yes exit from box 2), then an exception condition has been encountered. The

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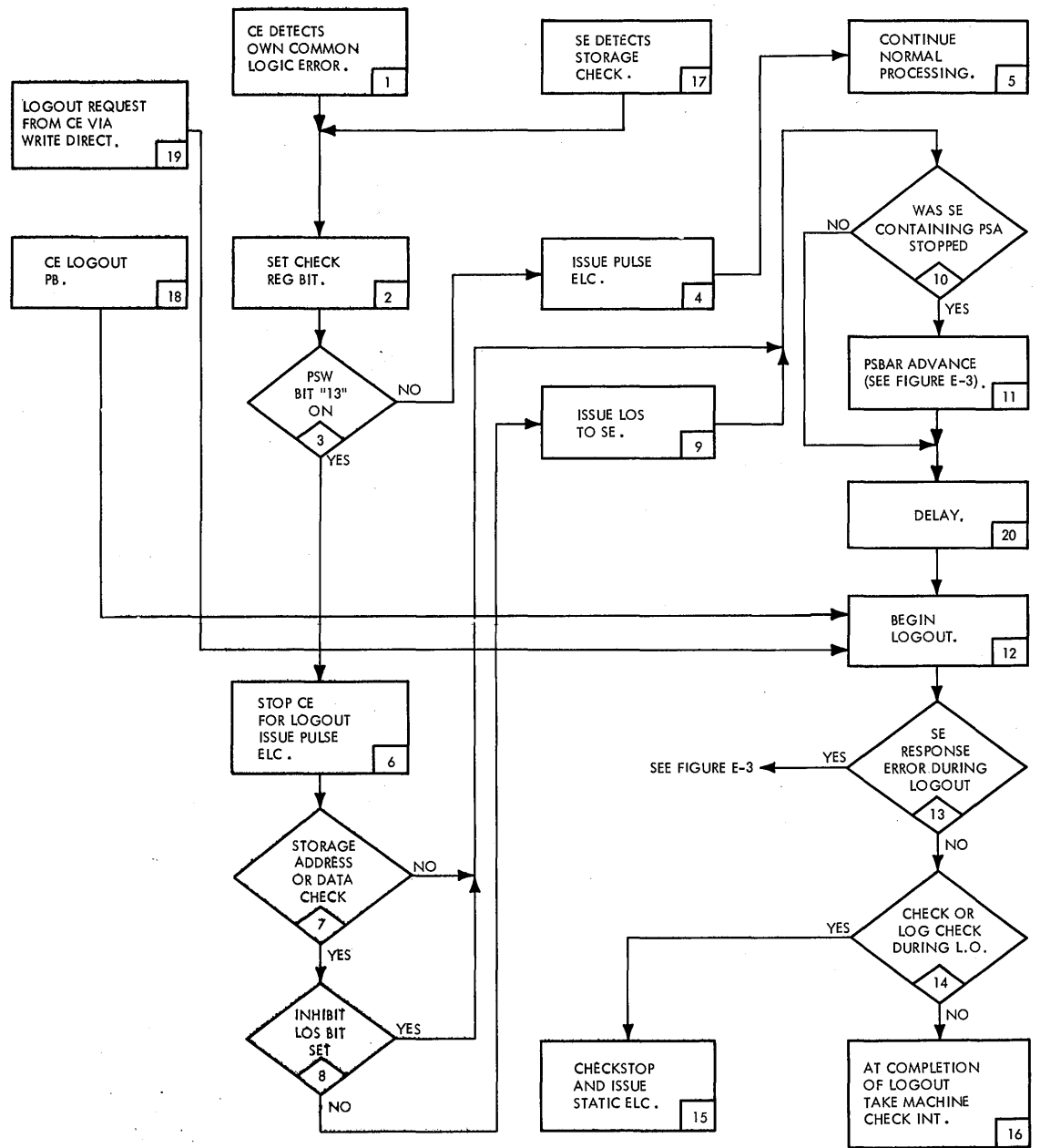
•Figure E-1.  CE Error Handling
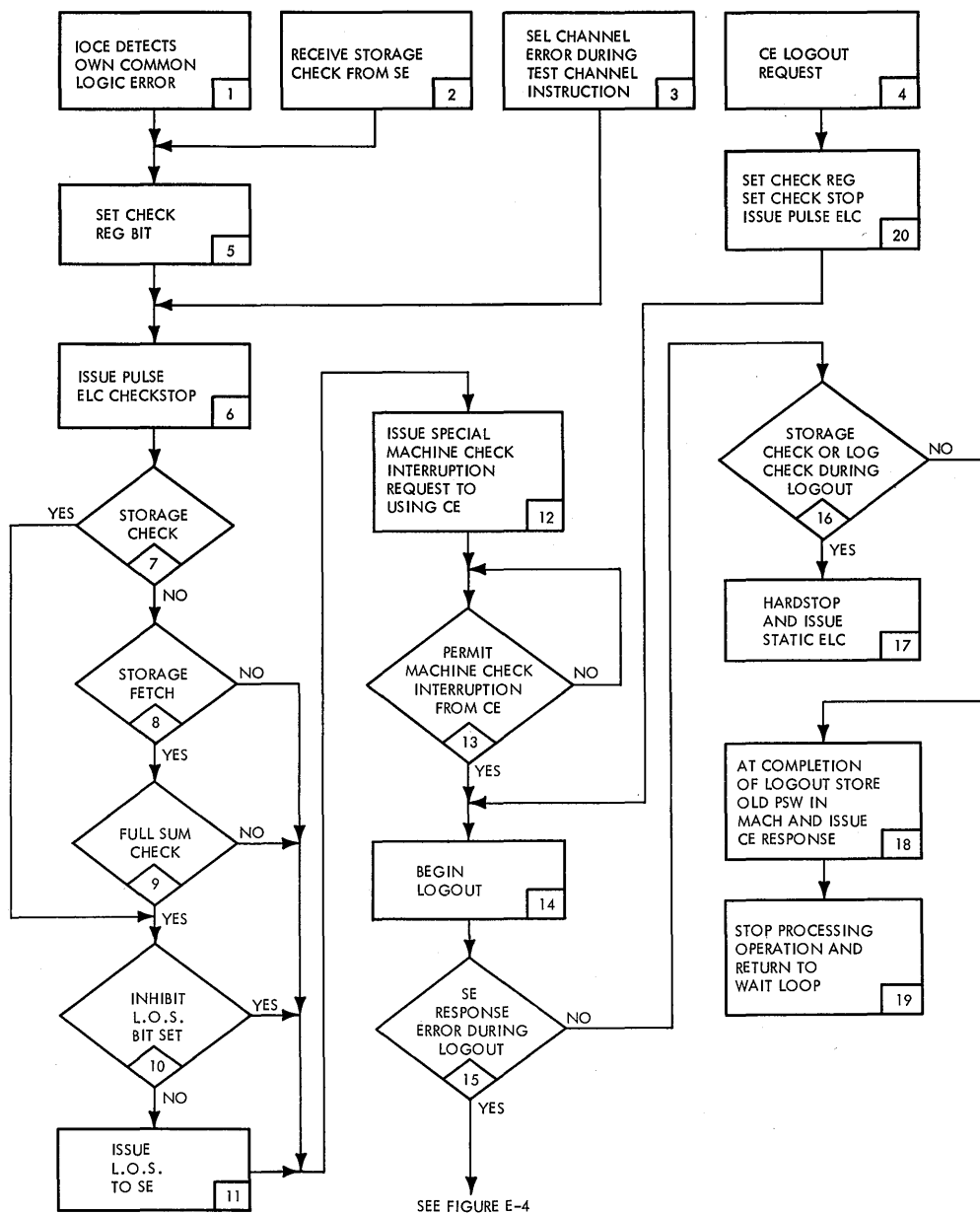
Figure E-2. IOCE Error Handling for Common Logic Errors

IOCE DETECTS OWN COMMON LOGIC ERROR — 1

RECEIVE STORAGE CHECK FROM SE — 2

SEL CHANNEL ERROR DURING TEST CHANNEL INSTRUCTION — 3

CE LOGOUT REQUEST — 4

SET CHECK REG BIT — 5

SET CHECK REG SET CHECK STOP ISSUE PULSE ELC — 20

ISSUE PULSE ELC CHECKSTOP — 6

ISSUE SPECIAL MACHINE CHECK INTERRUPTION REQUEST TO USING CE — 12

STORAGE CHECK — 7 — YES / NO

STORAGE CHECK OR LOG CHECK DURING LOGOUT — 16 — NO / YES

STORAGE FETCH — 8 — NO / YES

PERMIT MACHINE CHECK INTERRUPTION FROM CE — 13 — NO / YES

HARDSTOP AND ISSUE STATIC ELC — 17

FULL SUM CHECK — 9 — NO / YES

AT COMPLETION OF LOGOUT STORE OLD PSW IN MACH AND ISSUE CE RESPONSE — 18

INHIBIT L.O.S. BIT SET — 10 — YES / NO

BEGIN LOGOUT — 14

STOP PROCESSING OPERATION AND RETURN TO WAIT LOOP — 19

ISSUE L.O.S. TO SE — 11

SE RESPONSE ERROR DURING LOGOUT — 15 — NO / YES

SEE FIGURE E-4

Figure E-3.  Response Type Error Handling for CE-SE Accesses

program interrupt and SE Stopped bit is set (box 13). Box 15 indicates that a determination is next made as to the reason for the storage request, i.e., was it a PSA reference or was the request a normal one. If the reference was not to the PSA (no exit, box 15), a select is forced to the SE that contains the PSA (box 26). If the select was to the PSA (yes exit, box 15) a check is made to see if this is already the alternate PSA (box 16). If it is the alternate PSA, the CE check stops, turns on the alternate PSBAR Check (box 17) and issues a static ELC to the other CE's (box 18).

Had it been determined at box 16 that reference was not to the alternate PSA (yes exit, box 16), then the alternate latch is set (box 19) and a check made to see if the ILOS bit is on (box 20). If the ILOS bit is on (yes exit, box 20), a select is forced to the same PSA SE (box 26). Had the ILOS bit not been set (no exit, box 20), the PSBAR counter will be advanced to locate an alternate PSA. (An expansion of the PSBAR advance function is given in Figure E-3). Having advanced PSBAR, a check is made (box 22) to see if logout was being performed. If not (no exit, box 22), a select will be forced to the new PSA Storage Element (box 26).

If the reference to PSA was made during logout (yes exit, box 22) then the CE will set the 'split logout' bit (box 23) and force a select to the new PSA Storage Element (box 26). This will result in a so-called split logout, i.e., the part of the logout which had occurred prior to the access malfunction will be in the primary PSA, and the logout representing the machine environment at the time of the access malfunction will be in the alternate PSA. It will be possible to reconstruct the original environment from the combined contents of the primary and alternate PSA's.

Return to box 3. If the SE is not configured to the requesting CE or the SE is not ready (power down or in Test), yes exit from box 3, another type of exception condition has been encountered. The program interrupt 'Addressing Exception' would be set (box 14). The same paths used in the 'SE Stopped' interrupt are then followed beginning at box 15.

If SE Stopped or Not Ready are encountered during the 25ms. timedown interval (yes exits from boxes 6 and 7), the above same procedures for program interrupt are followed and the timedown is reset. (Boxes 13/14)

Returning to box 8, if no SE Accept signal is received before the 25ms. timedown (yes exit, box 8), a pulsed Element Check is issued to all CE's and the CE generates a 'pseudo accept' (box 31). At box 10 a check is made to determine if the Machine Check Mask is on. If not on, the CE will continue normal processing (box 12). If the mask bit is set (yes exit, box 10), a check is made to see if the SE that contains the PSA was referenced (box 11). If normal reference made (no exit, box 11) the CE will start a Machine Check logout (box 25). If the SE that contains the PSA was referenced (yes exit, box 11) the same paths are followed as for program inter-

rupts beginning at box 16. However, at box 24 the path will exit from the Timeout leg and the CE will start a Machine Check logout at box 25.

The right portion of Figure E-3 is an expansion of the PSBAR Advance function (box 21). At box 27 the PSBAR counter is stepped to the next configured SE. When the next configured SE is found (no exit, box 28) entry is made into box 22. If no other SE has been configured, i.e., the PSBAR counter makes one complete wrap, finding no other SE in the ATR, the PSBAR configuration check bit is set (box 29). The CE then check stops and issues a static Element Check to the other CE's.

CE handling of the Display Element accesses is similar to that of the Storage Element except that there are no references to PSA or 'split logout'. Referencing Figure E-3, the flow through boxes 1 through 9 are identical. The yes exits from boxes 2 and 6 (DE Stopped) would be to box 13, Program Interrupt with DE Stopped exception. The yes exits from boxes 3 and 7 (DE Not Ready) would be to box 14, Program Interrupt with addressing exception.

If a timeout was encountered (yes exit, box 8) a pulsed Element Check would be issued (box 31) and a check made to see if the Machine Check Mask bit is on (box 10). If not on, the CE continues processing (box 12). If the bit is on (yes exit, box 10) the CE will begin a Machine Check logout (box 25).

IOCE Action

Figure E-4 depicts the IOCE actions which occur when an IOCE makes a request for a storage cycle. It is presumed that the IOCE has developed the necessary address and makes the storage request at box 1.

If the IOCE is configured to listen to the selected SE, and the selected SE is configured to listen to the requesting IOCE, then a response to this request will be returned to the IOCE, (assuming power is up on the SE). A period of one usec nominal, referred to as 1 us timedown, is allowed for this request-response completion. Box 2 indicates this.

Assuming this response is returned to the IOCE within one us, (no exit from box 2), then the IOCE will wait for a maximum of 16 us for the SE to honor its request for a storage cycle. This is referred to as a 16 us timedown. This period is a convenient interval which is greater than the time that any IOCE should have to wait for a storage cycle due to its high place on the priority chain. If the request is honored within the 16 us interval (no exit from box 3), then a normal storage access is obtained at box 19.

If no response to the access request is received (yes exit from box 2), then the IOCE checks to see if a PSBAR reference was being made at box 4. If the PSA is not being referenced (no exit from box 4), then the IOCE will ascertain whether or not the SE reference was made as part of an I/O instruction at box 5. If an I/O instruc-
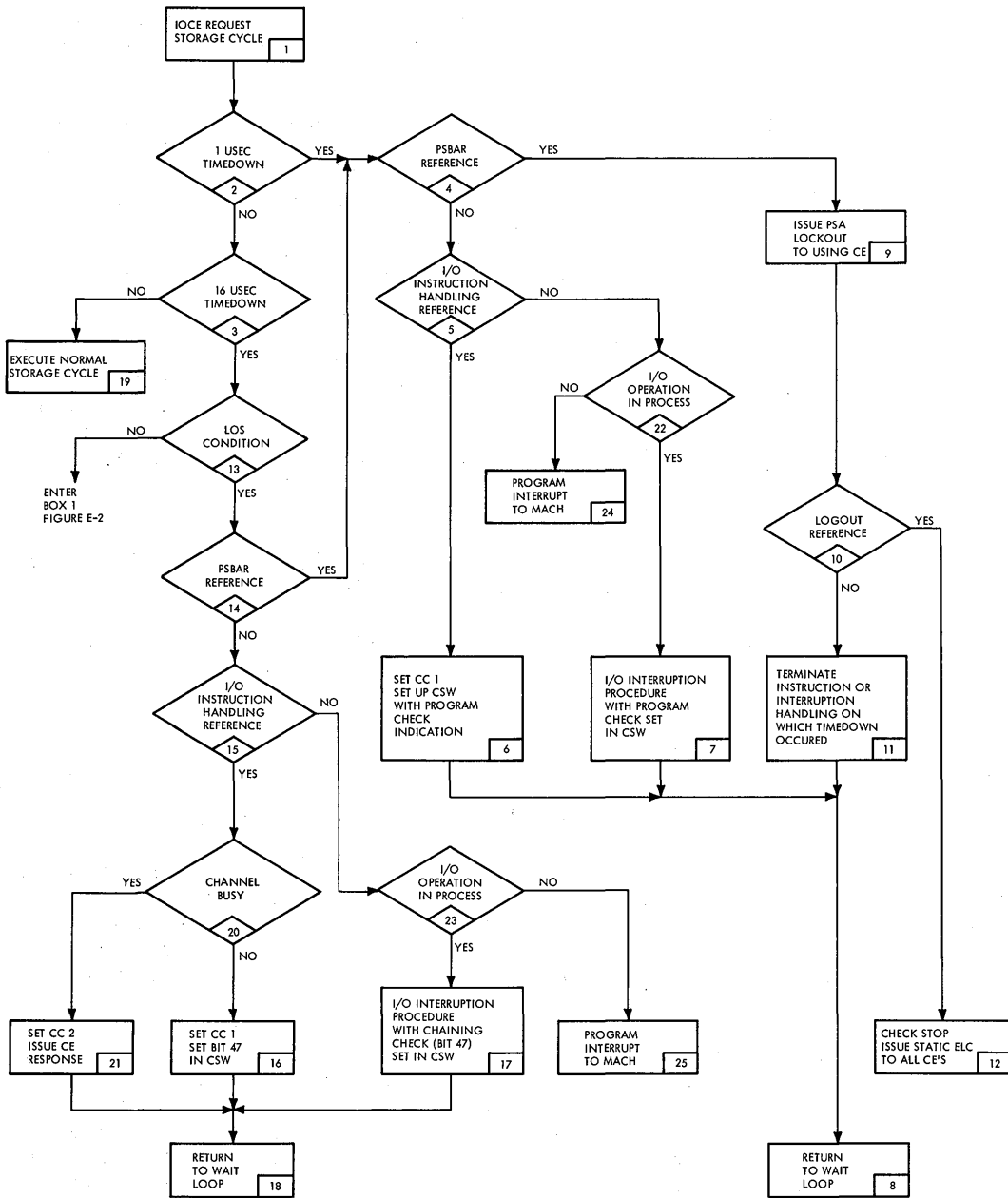
Figure E-4. Response Type Error Handling for IOCE-SE Accesses

tion is in progress (yes exit from box 5), then the IOCE will set
condition code 1 and set up a CSW with a program check indication
at box 6. It will then return to the wait loop, i.e., revert to
waiting for further instructions or data handling requests at box 8.
If an I/O instruction is not in process (no exit from box 5), then
the decision is made at box 22 whether an I/O operation was in pro-
cess. If the answer is no, then a program interrupt into MACH
(box 24) will occur. If instead an I/O operation was in process,
then the reference was for a normal data transfer cycle. The IOCE
will cause the usual invalid address indication to be returned to
the channel. At such time, then, as the channel signals an I/O
interruption because of this (box 7), a program check will be set
in the CSW. The IOCE will go to the wait loop until the occurrence
of the interruption. This is the usual method of operation when a
device presents an invalid address to the IOCE for storage access.

If the addressed location was a PSBAR reference (yes exit from
box 4), then the IOCE will present a PSA lockout signal (box 9) to
the using CE. This will cause a program interruption in the using
CE, which can respond with a new PSBAR setting, if it desires. If
the IOCE is doing a logout (yes exit from box 10), then it will come
to a stop and issue a static ELC to all CE's (box 12). If the CE
which is controlling the IOCE wishes to have it resume logout, it
must issue a logout to the IOCE presumably after changing PSBAR. In
this event, logout will be restarted from the beginning in the
alternate PSA. There will be, in general, no problem reconstructing
the logout formats since the CE has been notified by the PSA lockout
signal that a 'split logout' is going to take place, and the logout
contents will be available to deduce what has happened in detail.

If no logout is in progress (no exit from box 10), the IOCE
will terminate the instruction or interruption handling on which the
time down occurred (box 11). It returns to the wait loop at box 8.
The I/O interruption will be lost and is not recoverable. If an I/O
instruction is in progress, the CE will set condition code 3.

If the IOCE is not able to obtain a storage access within 16 us
(yes exit from box 3), it assumes that there has been either an
equipment malfunction or that it has attempted to reference an SE
which was stopped for logout. It determines at box 13 whether or
not the SE was stopped. If not, (no exit from box 13), then it
assumes an error. The logic then goes to the IOCE error handling
procedures on Figure E-2.

If the SE was stopped (yes exit from box 13), then the IOCE
determines whether or not a PSBAR reference was in progress at box
14. If so (yes exit from box 14), then the IOCE proceeds to the
logic previously described at box 4. (There will, in this case, be
a yes exit from box 4). If no PSBAR reference (no exit from box 14),
then it is ascertained whether or not an I/O instruction was being
executed at box 15. If it was, (yes exit from box 15), then it is
ascertained whether or not the channel is busy (box 20). If it was
(yes exit from box 20), then at box 21, condition code 2 is set and
a response is issued to the CE. The IOCE then returns to the wait

loop. If the channel is not busy (no exit from box 20), then at box 16 condition code 1 is set, and a CSW is stored with a chaining check indication. It will then go to the wait loop at box 18. If no I/O instruction is in process (no exit from box 15), then the decision is made at box 23 whether an I/O operation is in process. In any event, the action is the same as discussed earlier for box 22, except that if an I/O interruption takes place (yes exit from box 23) the CSW will be set with the chaining check bit. The IOCE will then return to the wait loop.

COMPUTING ELEMENT MALFUNCTIONS

The CE's actions in the event it detects an error in its internal hardware or is notified that the SE with which it is working has a malfunction are depicted on Figure E-1.

The action on Figure E-1 can be initiated by either the detection of a CE error (box 1) or the occurrence of a storage check from an SE (box 17). These signals are recovered in the CE's check registers (box 2). A decision as to whether or not machine check interruptions are masked is made at box 3. If machine check is masked off (no exit from box 3), then a pulse ELC is issued (box 4) and normal processing is continued. The masked interruption will remain pending. If machine check is not masked off (yes exit from box 3) then a CE stop for logout will occur and a pulse ELC is issued (box 6). This stop is not actually a true stop in the sense that the CE does not continue to operate. Rather, the stop indicates that execution of the current stored program is discontinued, and the CE's internal controls begin the necessary actions required to perform logout and begin the machine check interruption program.

If a storage, address or data check is present in the check register (yes exit from box 7) then the LOS inhibit bit in the CCR is interrogated at box 8. If it is not set (no exit from box 8), then LOS is issued to the SE at box 9 and the CE proceeds to determine at box 10 whether or not the initial logout should be to the primary or alternate PSA.

At box 10, the CE determines whether the PSA is contained in the SE causing the check condition, which was (perhaps) stopped. If the SE which was stopped by this CE contains the PSA (yes exit from box 10) then the PSBAR is stepped to the alternate PSA (see Figure E-3 for details) and logout is started at box 12. If the PSA is not contained in the SE which was stopped by this CE or if the Inhibit LOS bit was on, (no exit from box 10) then logout begins upon completion of the delay period (boxes 12 and 20). A logout request from another CE via Write Direct (box 19), or a signal from the CE Logout Pushbutton (box 18) also initiate a logout at box 12.

Should the CE be unable to get a storage cycle during logout (yes exit from box 13), the resultant actions are as shown on Figure E-3. At box 14 is the schematic indication that a storage check or log check (error in Read Only Storage) during logout (yes exit from box 14) will cause the CE to stop and and issue a static ELC

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(box 15). When this stop occurs, the CE will respond only to an external start from another CE, a logout signal from another CE, a SCON instruction, or IPL. If neither of the two types of errors occur (no exit from box 14), then the CE will proceed to take a machine check interruption at box 16.

IOCE MALFUNCTIONS

Common Logic Unit

Figure E-2 depicts the action taken by an IOCE upon the detection of an error in its own equipment, a storage check from the SE with which it is working, a selector channel error during the Test channel instruction, or when it is instructed to logout by a CE.

Assume the IOCE detects an error in its common logic (box 1) or receives a storage check from the SE with which it is working (box 2). The necessary bit is set in the check register (box 5) and a pulse ELC is issued to all CE's at box 6. If a selector channel error during the test channel instruction occurs (box 3), it enters the logic at box 6 by issuing a pulse ELC and executing a checkstop. No check bit is set since logout data will indicate that the selector channel error occurred.

At box 7, a determination of whether or not to stop the SE with which the IOCE is working is begun. If a storage check had occurred (yes exit from box 7), then a check is made at box 10 to determine if the inhibit logout stop bit is set. If not (no exit from box 10), then a logout stop (LOS) signal is sent to the SE at box 11.

If there was no storage check (no exit from box 7), then a check is made to see whether the IOCE was fetching data from the storage element. This is done to enable the IOCE to stop the SE if the error occurred at the data input point, since an interface error could have occurred. If not (no exit from box 8), the IOCE will proceed to initiate the necessary action for logout at box 12. If a fetch was in progress (yes exit from box 8), then at box 9 a check is made to see whether or not the error was a full sum check, which is the malfunction to be expected if an interface error had occurred. If there was a full sum check (yes exit from box 9), then the IOCE checks the LOS inhibit bit at box 10 to determine whether or not it is permitted to issue a LOS to the SE. If no full sum check had occurred (no exit from box 9), then the logic proceeds to box 12.

NOTE: If there was no storage check (no exit, box 7), depending on the subsequent activity in the SE, there is the possibility that the SE logout information will not be pertinent to the IOCE fetch check which caused the issuance of logout stop to the SE at box 11.

At box 12, the IOCE begins the sequence of actions which will result in a logout. The IOCE issues a request for a machine check interruption to the controlling CE. This machine check interruption

differs from the normal one in the CE in that the CE will not per-
form a logout, will honor it only at the completion of the current
instruction, and will result in an interruption code in the old PSW
as follows:

$$
\begin{array}{llll}
0000 & 0000 & 0001 & \text{IOCE 1} \\
0000 & 0000 & 0010 & \text{IOCE 2} \\
0000 & 0000 & 0011 & \text{IOCE 3}
\end{array}
$$

This machine check interruption is masked by PSW bit 13 in the CE.

Box 13 indicates that the IOCE will wait until the CE honors its
request before beginning its logout at box 14.

Should an SE response error occur during logout; i.e., the IOCE
cannot obtain a storage cycle (yes exit from box 15), it will proceed
as shown on Figure E-4.

Box 16 indicates that account is taken of errors which could
occur during the logout. These errors are storage check or a log
check (read only storage error). If one of these occurs (yes exit
from box 16), the IOCE will come to a check stop and issue a static
ELC to all CE's. It will not resume operation until an external
signal is received. This could be a signal from a CE requesting the
IOCE to attempt logout again, or a reset as a result of IPL. The
IOCE will respond to SCON instructions while in the check stop.

If no error occurred during the logout, the IOCE will store its
old machine check PSW in MACH and turn off process mode controls,
and will respond to the CE to clear the interruption hold and return
its normal operation (wait loop).

Box 4 at the top of Figure E-2 shows that if an IOCE receives a
logout signal from a CE, it will enter the checkstop mode at box 20.
It will set the proper bit in the check register to indicate what has
occurred and will issue a pulse ELC. It then proceeds to box 14 to
initiate the logout sequence.

Selector Channel

Figure E-5 shows the IOCE actions when an error is detected in a
selector channel. This sequence of actions differs from the usual
IOCE logout primarily in that logout is handled via an I/O inter-
ruption and is interleaved with the IOCE's normal operation, causing
no interruption in IOCE service on the non-failing channels.

At box 1, the IOCE detects a selector channel error. At box 1a,
a check is made to determine if the error was a channel data check.
If it was (yes exit for box 1a), then the parity is corrected (for
input bytes only), the check condition is recorded and command chain
ing is suppressed (box 15). The IOCE then resumes the I/O Operation
(box 16). If the error was not a data check (no exit from box 1a),
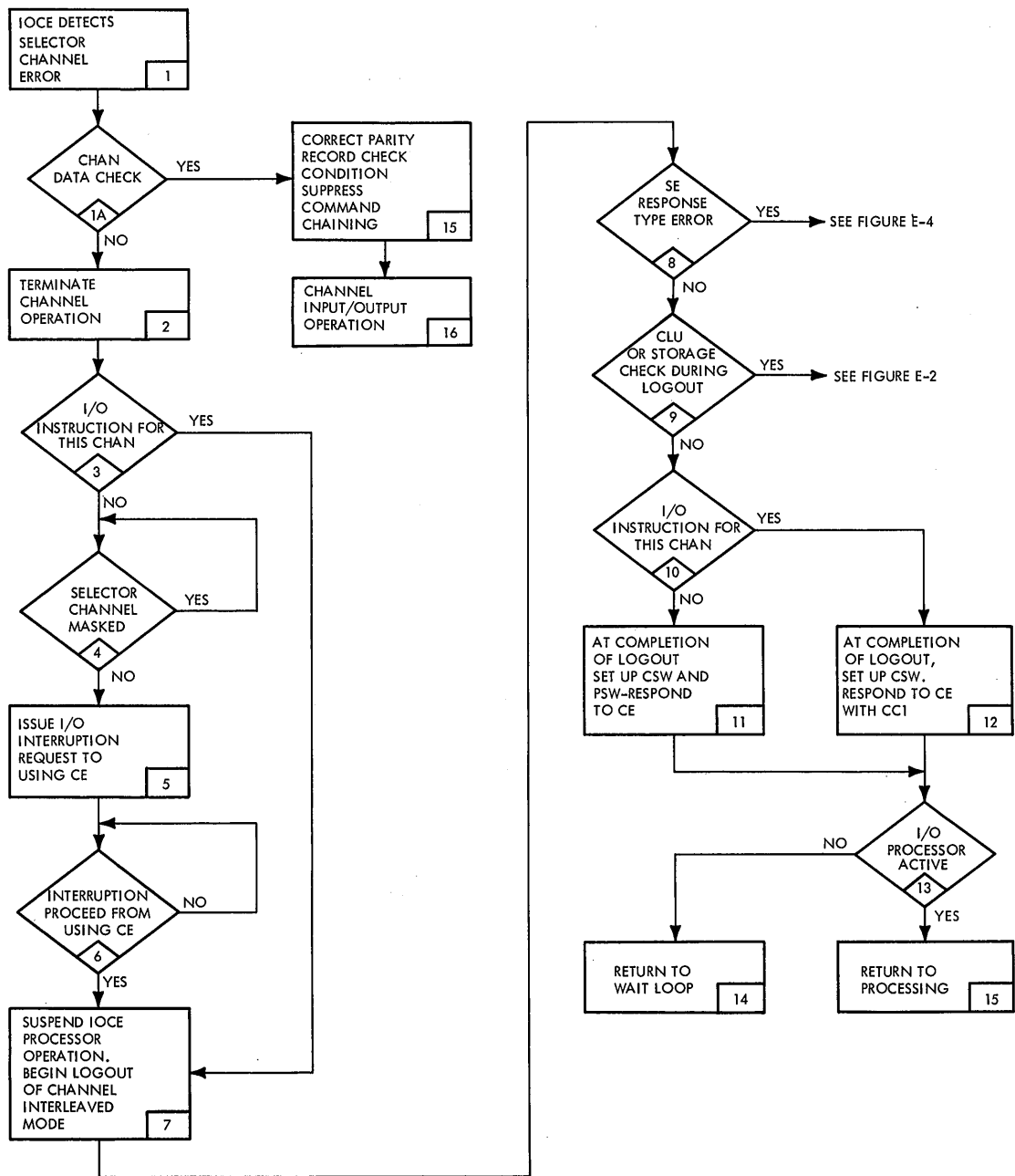then the IOCE terminates the channel operation at box 2. At box 3,

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**Figure E-5. IOCE Error Handling for Selector Channel Errors**

a check is made to see if there is currently an I/O instruction in process for that channel (except Test channel). If there is (yes exit from box 3), then the CE is waiting for its completion and a PSBAR setting is already available to the IOCE. The logic then sus-

pends IOCE-Processor operation and proceeds directly to the beginning of logout at box 7. If there is no I/O instruction in progress for that channel (no exit from box 3), the mask is checked at box 4. If the channel is masked, the interruption request will wait (yes exit from box 4). If the channel is not masked (no exit from box 4), then an I/O interruption request is made to the CE at box 5. Box 6 indicates that the channel will wait until the CE responds with a proceed signal, at which time it will suspend IOCE-Processor operation and will begin the channel logout at box 7. The interleaved mode indicates that the IOCE will service the selector channel for logout along with the other channels' normal requests.

Boxes 8 and 9 indicate that account is taken of the IOCE's failure to get a storage cycle or an error during logout. If a common logic unit error or a storage check occur during the logout, the IOCE will check stop and issue a static ELC to all CE's.

When the logout is complete, the IOCE will take alternate actions depending on whether or not an I/O instruction was in progress when the malfunction occurred. If an I/O instruction was in progress (yes exit from box 10), a CSW will be stored indicating logout has occurred, and condition code 1 will be set in the CE and a response sent to the CE to clear the interruption hold. If no I/O instruction was in progress (no exit from box 10), the IOCE will set up a CSW and set the I/O interruption code in the PSW. The response will be sent to the CE to clear the interruption hold.

At the conclusion of either of these terminal operations, the IOCE will return to processing if it was in process mode, or return to the wait loop if it was not in process mode.

STORAGE ELEMENT MALFUNCTIONS

Figure E-6 depicts the SE actions where it detects an error in its internal logic or parity or address error. This type of error is detected at box 1. The applicable error latches are set at box 2. Box 3 denotes the control conditions which can cause the suppression of transmitting error signals under various conditions. If the SE detects a data check and the Suppress Log Check line from the CE is active (yes exit from box 3), the data check signal lines are deactivated and the setting of the Block Select latches and Wait Timeout are inhibited and the SE will continue normal operation (box 4). If the Suppress Log Check line is not up (no exit from box 3), the SE then issues an Element Check to all CE's (box 5). If the check is due to a thermal condition, On Battery Supply, or CCR Parity Check the pulsed Element Check signal is the only signal sent to the CE's (yes exit box 6) and it will continue its normal operation (box 7) until power is turned off.

If the error was other than those mentioned above, the SE will issue the applicable Storage, Data, or Address Check to the user (box 8) and begin a 2.5 microsecond timeout (box 10) awaiting a Logout Stop signal from the user or any configured CE. The SE will not honor any further requests for service while awaiting the Stop

```
                    ┌─────────────────┐
                    │ SE DETECTED     │
                    │ LOGIC ERROR  ┌──┐│
                    │              │1 ││
                    └──────────────┴──┴┘
                            │
                    ┌─────────────────┐
                    │ RECORD ERROR    │
                    │ IN ERROR        │
                    │ LATCHES      ┌──┐│
                    │              │2 ││
                    └──────────────┴──┴┘
                            │
                        DATA
                    CHECK AND
            NO      SUPPRESS LOG      YES
                    CHECK UP
                        3
```
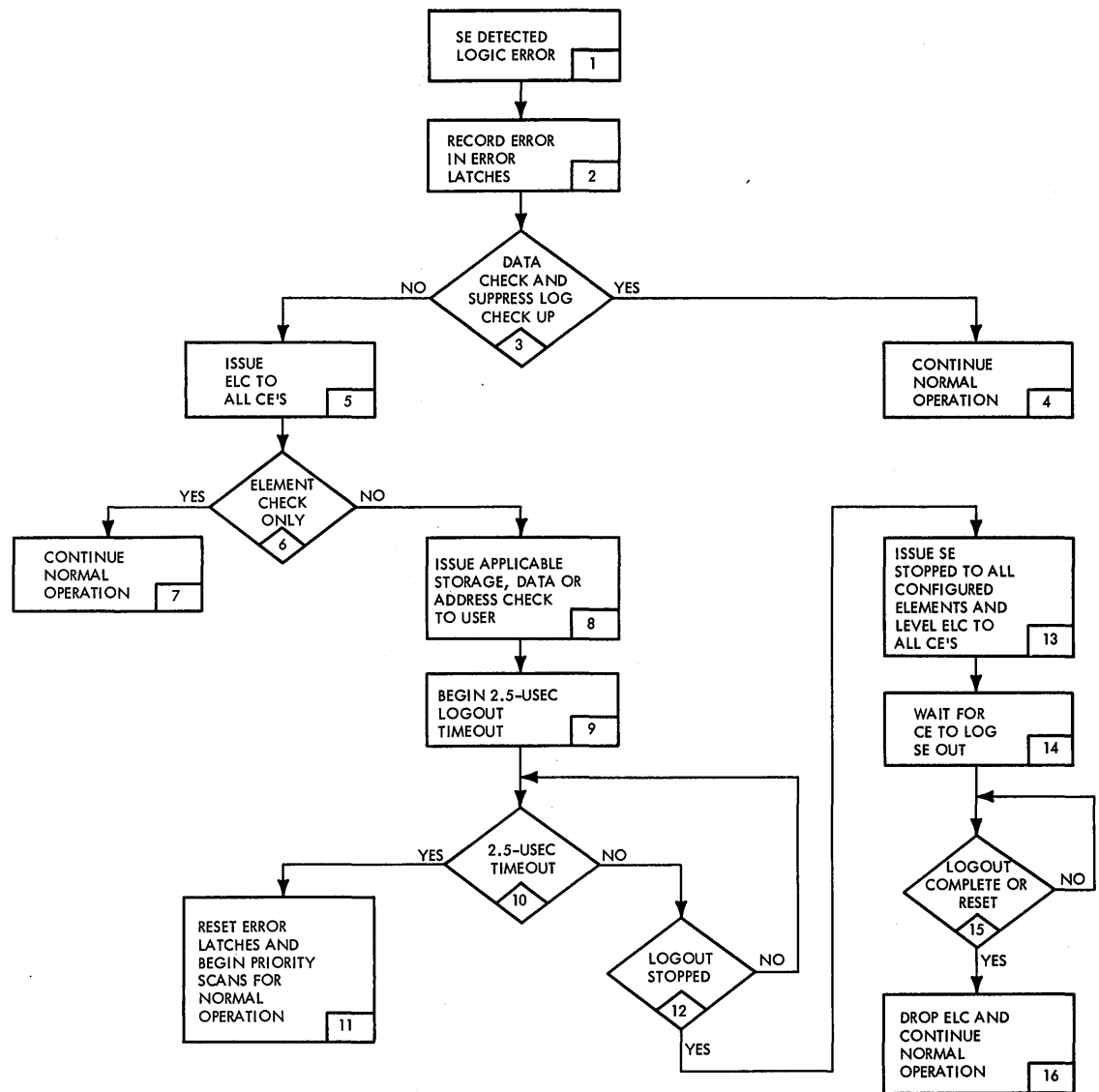
●Figure E-6.  SE Error Handling

signal.  If no Logout Stop signal is received before the SE times
out (yes exit box 10), the SE will reset its error latches and be-
gin priority scans for normal operation (box 11).

     At box 13, if the Logout Stop signal is received (yes exit
box 12) before timeout, the SE issues a SE stopped signal to all
configured elements and a level Element Check to all CE's.  It will
then wait for the Logout Select signal from the controlling CE to
begin logout (box 14).  The SE cannot proceed with regular operations

unless it is given a Logout Complete Signal from a CE or is reset
(box 15). Upon receipt of Logout Complete or a reset (yes exit
box 15), the SE will drop the Element Check line and resume normal
operation (box 16).

DISPLAY ELEMENT MALFUNCTIONS

Figure E-7 depicts the DE actions when it detects an error in its
internal logic or parity or address circuitry. The error detection
is indicated by box 1. The detected error is recorded in box 2 and
a pulsed ELC is issued to all CE's at box 3. If the CE has priority
out of box 4, a check is made at box 5 to determine if an ELC only
exists. If the 'yes' exit is taken, a further check is made at
box 6 to determine if the ELC was caused by a DG related error, i.e.,
a DG Data Register Parity Check, a Local Store Parity Check, or a DG
Referesh Counter Check. If the decision is 'yes', this indicates an
error has been detected in the circuitry of the user (DG) that had
the previous DE cycle, but whose operation is being finished during
the current CE's priority cycle. In this condition, a branch is
made to box 19. This path will be explained later. If at box 6,
the 'no' exit is taken, the ELC condition would have been caused by
a CCR Parity Check, a thermal condition, an OBS, or Power Off. If
any of these conditions exist, except Power Off, the DE will try to
resume normal operation, indicated in box 7; however, the check con-
dition may cause unpredictable results. In case of Power Off, a
level ELC is sent to all CE's. If the exit taken from box 5 is 'no'
then the error must be address or data check. In this case an add-
ress or data check is issued to the accessing CE as shown in box 9.
In box 10, the DE clocks* are stopped and a 2.5 microsecond count
down loop is entered awaiting a logout stop signal from the accesssing
CE (box 11, 12). If a timeout occurs as shown in box 11, then the
error registers are reset and normal operation continues. If a log-
out stop signal is sent from the accessing CE prior to the 2.5 micro-
second timeout (box 12), the DE goes to a logout stopped condition,
issues a DE stopped signal to all configured CE's, and a level ELC
to all CE's (box 13). At box 14, it is indicated that the DE will
wait for logout. It cannot proceed with regular operations unless
it is given a logout complete signal from a CE or is reset. This
is shown at box 15. The DE will respond to the SCON instruction
while stopped. Upon receipt of Logout Complete or a reset (yes exit
from box 15), the DE will drop the ELC line and resume normal oper-
ation.

   At box 4, the 'no' exit indicates that a DG Check has occurred
(box 17). Box 18 indicates that either address or data checks or
an Element Check may have occurred, in either case the error hand-
ling will be identical. At box 19, the Inhibit DE Stop (IDES) bit
is examined, and if the bit is on, exit is taken to box 22, where
the error registers are reset and normal operation continues. If,
at box 19, the IDES bit is not on (no exit), the DE clocks* are

---

      * The clocks associated with the DG's will run to the comple-
tion of the data transfer unless the error is within the DG cir-
cuits. If so, the associated clocks will be stopped immediately.
The clocks associated with the priority and BSM will run until the
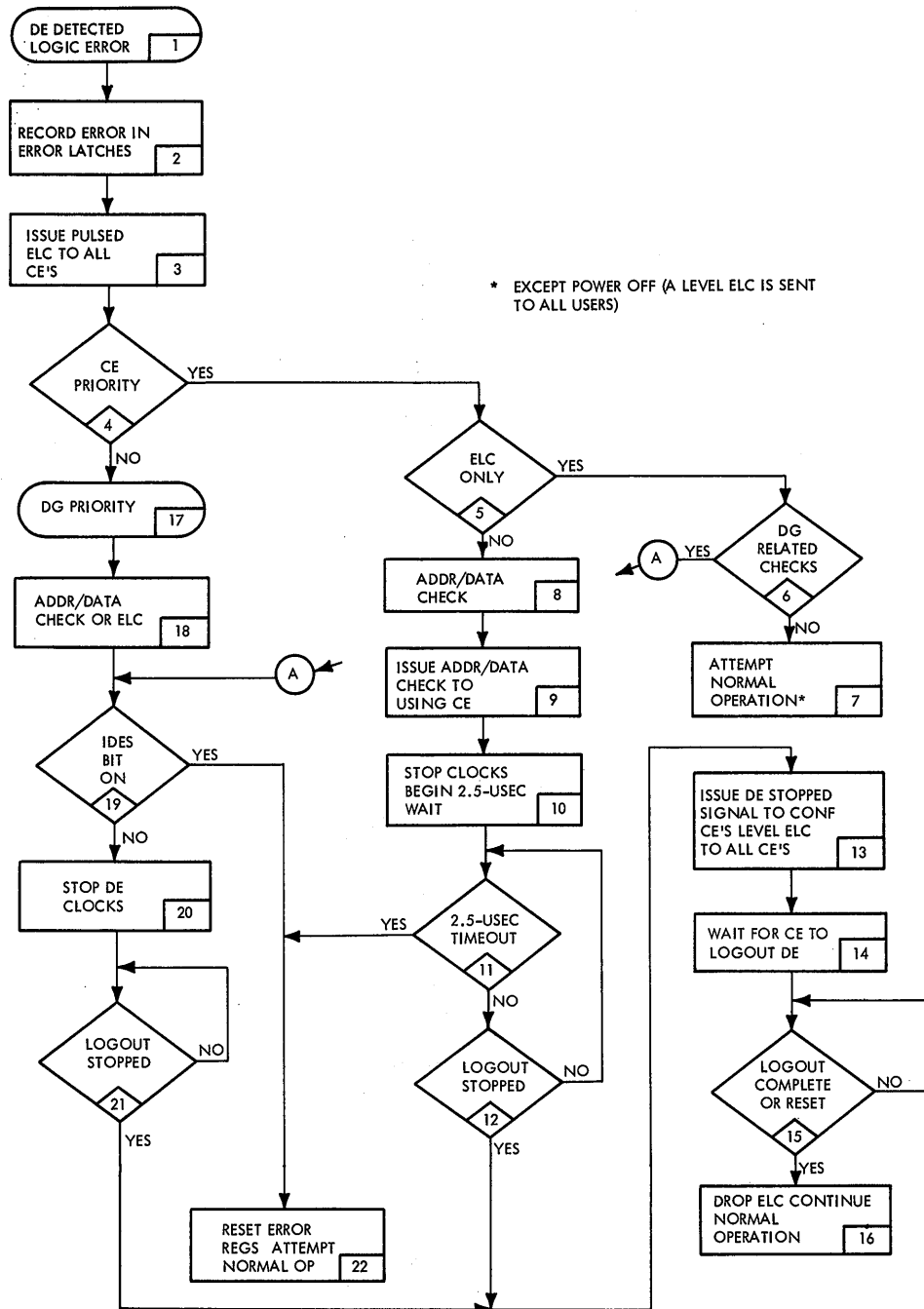current cycle is completed, then stop.

Figure E-7. DE Error Handling

stopped (box 15) and the DE waits to be logout stopped by a CE.
This is shown in box 21. When the 'yes' exit is taken from box 21,
box 22 is entered into and the progression of events from this
point are identical as when the CE had priority.

Note:  On DG related errors, the level ELC generated at box 13 will
       override the pulsed ELC issued at box 3.

TCU MALFUNCTIONS

Figure E-8 depicts the malfunction reporting actions taken by the
TCU when it detects a check condition (Start 0), a CCR Bad Parity
Condition (Start 10), or a temperature Out of Tolerance Condition
(Start 20). In all cases, there are three primary actions that
must take place to complete the reporting of a detected malfunction:

  1.  Identify the malfunction and set appropriate indicator.

  2.  Inform the program through the channel equipment or the
      system monitoring equipment that a malfunction has occurred.

  3.  Supply malfunction identification to the channel equipment.

Check Condition Reporting

(Start 0)  At box 1, the TCU equipment detects a check condition dur-
ing the execution of a command, identified the condition, stores
this information in the appropriate Sense Register Indicator at
box 4 (Action 1), and sets the Unit Check Indicator in the Status
Register at box 5. The operation in progress is not stopped at
this point but is allowed to continue to its normal conclusion at
box 31. At box 32, the TCU now attempts to inform the channel that
a malfunction has been detected by presenting the Status information
having the Unit Check Indicator set. At boxes 34, 35 and 36, the
IOCE, when able, elects to receive the Status information, either
through the I/O interruption facilities (yes exit, box 34) or by
use of the Test I/O command (yes exit, box 36). At box 37, the TCU
transfers the Status Register contents indicating Unit Check which
was set at box 5, to the IOCE channel (Action II). Having trans-
ferred the Status information, the TCU at box 38 resets the Status
Register. As a consequence of receiving the Unit Check bit, it is
expected that the program will request details of the malfunction
by issuing a Sense Command as indicated at box 41, 42, 43, and the
yes exit of box 44. As a result, at box 45 the TCU will transfer
the Sense data to the IOCE channel (Action III) for analysis and
subsequent appropriate action. Back at box 44, following the no
exit, the decision at box 46 is significant. If the Command to be
executed is Test I/O or I/O No-Op, the accumulated Sense information
is retained and still available to the program through a subsequent
Sense operation. However, if the exit from box 46 is no, indicating
that a new tape operation is to be performed, the Sense Registers
are reset at box 47 and the detail malfunction information contained
therein is lost.

CCR Bad Parity Condition Reporting

(Start 10)  At boxes 11 and 12, the TCU continuously monitors the
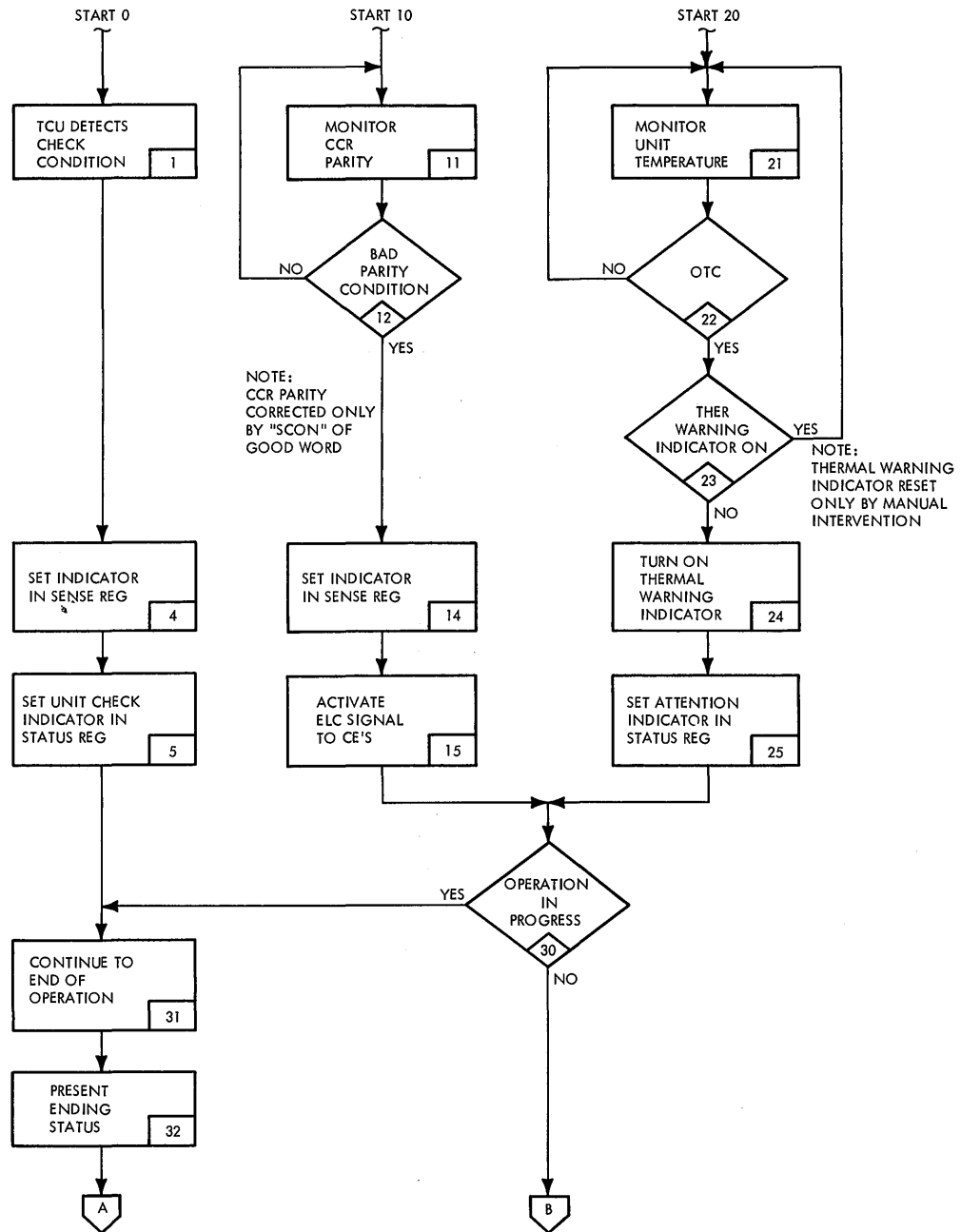CCR for a Bad Parity condition. When it detects this condition, it

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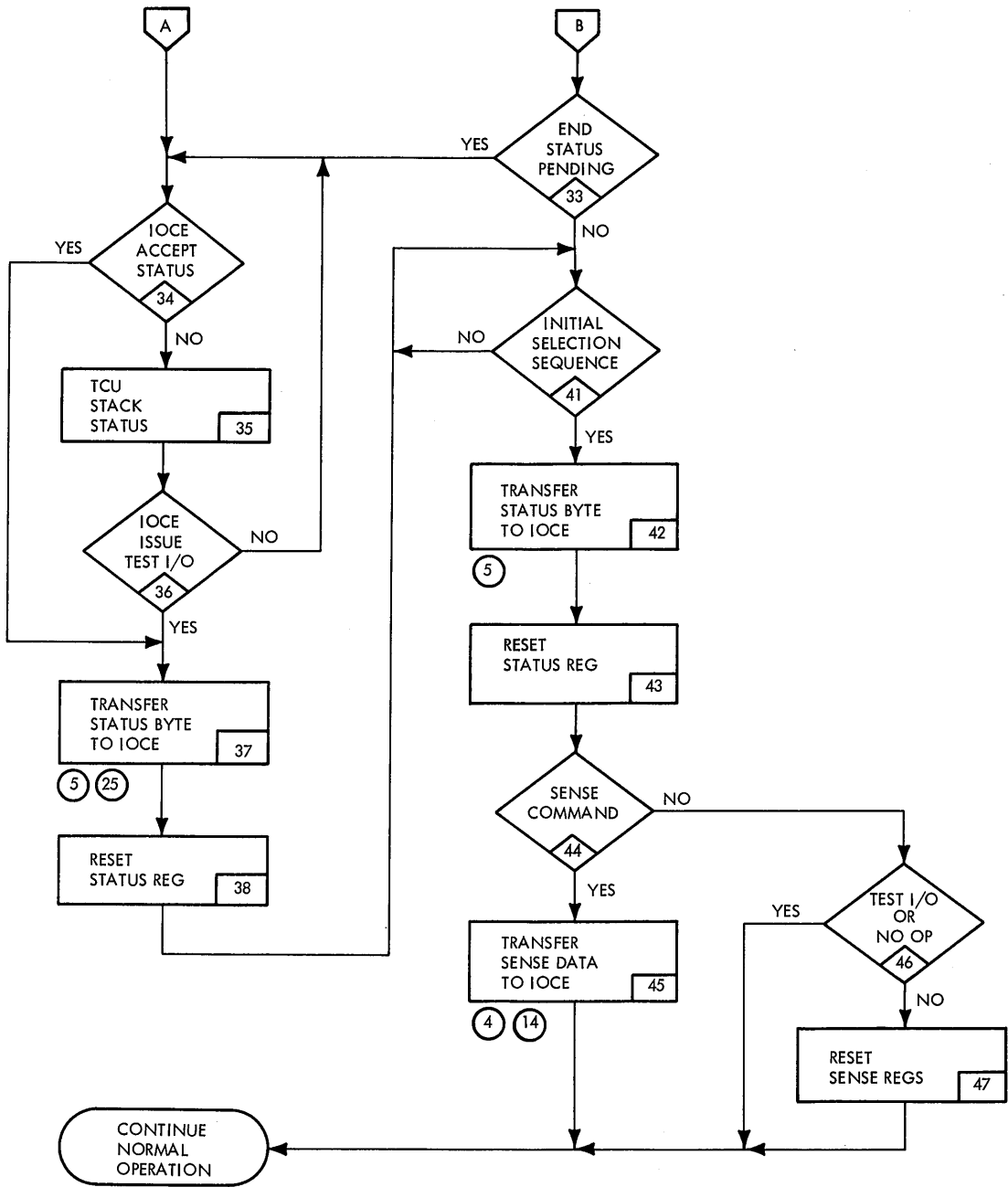Figure E-8. TCU Error Handling (Sheet 1 of 2)

Figure E-8.  TCU Error Handling (Sheet 2 of 2)

stores this fact in the appropriate Sense Register Indicator at
block 14 (Action I) and activates the ELC Signal to system monitor-
ing equipment in all CE's (Action II).  This signal will be held on

as long as the Bad Parity condition exists. The condition may be
corrected only by performing a SCON operation to replace the contents
of the CCR with data having proper parity. The exit options from
boxes 30 and 33 have little significance except to indicate the
alternate paths which are followed under varying conditions of
operation activity to culminate in the availability of the Sense
Indicator information (Action III) through boxes 41, 42, 43, 44
and 45.

Out of Tolerance Condition Reporting

(Start 20) At boxes 21 and 22, and TCU continuously monitors the
thermal sensing equipment for an out of tolerance condition. When
it detects this condition it determines, at box 23, whether the
Thermal Warning Indicator is presently on. If the indicator is not
on, the TCU will turn on the visual Thermal Warning Indicator at
box 24 (Action I) and will set the Attention Indicator in the Status
Register at box 25. If at box 30 it is determined that there is an
operation in progress, the path to box 31 will be taken and the
operation will continue to its normal end. At boxes 32, 34, 35, 36
and ultimately box 37, the TCU transfers the Status Register contents
indicating Attention which was set at box 25, to the IOCE channel
(Action II) and then resets the Status Register at box 38. Because
the Attention Indicator is unique to OTC in the TCU, the malfunction
requires no further identification and Action III has been effected
without the need for a Sense Operation. Back at box 30, if no oper-
ation is in progress, the no exit to box 33 is followed where it is
determined whether the Ending Status from the previous operation has
been accepted. If end

Status is pending, the "accept status loop" is entered at box 34 and
the Attention Status indicator is transferred to the IOCE channel
at box 37 as before. The no exit from box 33 enters a new operation
at box 41. At the conclusion of the Initial Selection Sequence
for the new operation, the Attention Status indicator will be in-
cluded in the Status Byte transferred to the IOCE at box 42 and is
reset after its contents are transferred to the channel (boxes 38
and 43), the Attention Status Indicator is presented once only for
any one occurrence of OTC. An attempt to manually reset the Thermal
Warning Indicator before the OTC is corrected will cause the Atten-
tion Status Indicator to be set again.

PAM MALFUNCTIONS

PAM Common

Figure E-9 depicts the action taken by PAM Common when it detects an
error in its internal logic, or an out-of-tolerance condition (OTC).
The sequence of actions does not apply to the case where PAM Common
detects a parity error on an address from the multiplexor channel.
In this case, PAM sets a sense bit in the Test and Monitor (TAM)
adapter and does not respond to the address. It does not set the
Attention bit. Errors occurring when the TAM adapter is the address-
ed unit (Bus Out Check or Command Reject) are covered under adapter
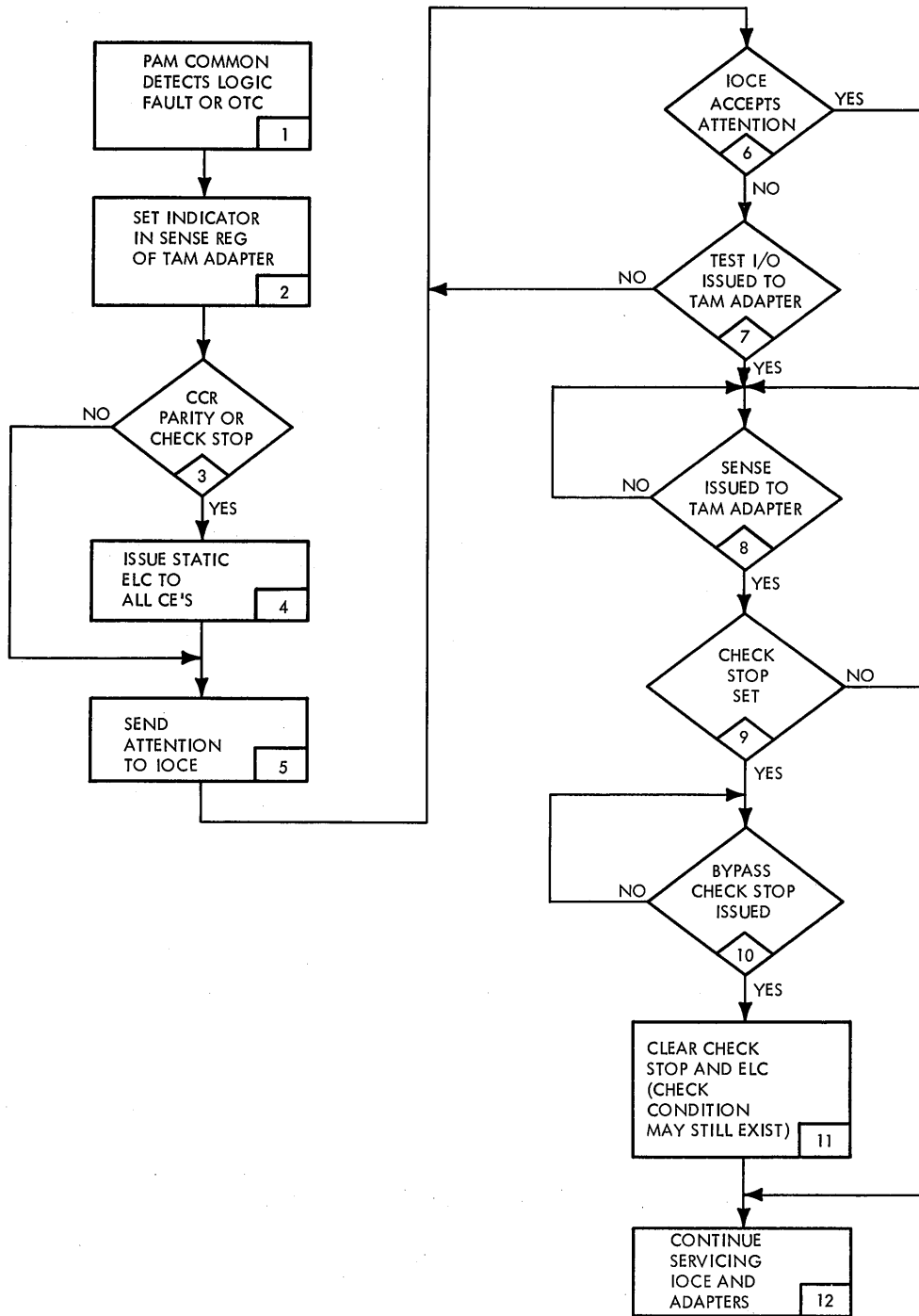malfunction handling.

Figure E-9. PAM Common Error Handling

At box 1, PAM Common detects the logic error or OTC. At box 2, the appropriate bit or bits are set in the TAM adapter's sense register, bytes 2 or 3. Box 3 denotes two check conditions which cause Element Check (ELC). If the check condition was caused by a CCR parity (Configuration Check) or Check Stop (check condition in the Priority circuitry), the yes exit is made to box 4. The ELC line is then raised to all CE's. ELC remains static until the condition causing it is cleared. After setting ELC or if neither above condition was detected (no exit from box 3), the Attention status bit is set at box 5 and presented to the channel. No further action takes place until the IOCE accepts the Attention status (yes exit from box 6) or issues TEST I/O to the TAM adapter (no exit from box 6 and yes exit from box 7).

After accepting Attention, the program can issue the Sense command to the TAM adapter (yes exit from box 8) to obtain information regarding the cause of the Attention status. If the Check Stop bit is not set (no exit from box 9) the program may try to continue I/O operations. A solid check condition will result in starting at box 1 again. If the Check Stop bit was set (yes exit from box 9), the cause of Check Stop is indicated in four other sense bits and may be examined. The program may then issue the Bypass Check Stop command (yes exit from box 10) which will clear the Check Stop latch allowing the next priority scan to begin. Clearing the Check Stop latch also clears the ELC line at box 11. If the cause of Check Stop was intermittent, the program will be able to continue with I/O operations in PAM (box 12). If the cause of Check Stop is solid, the cycle begins again at box 1.

If the Sense command is not issued (no exit from box 8), or if issued and Check Stop is present and not cleared by the Bypass Check Stop command (no exit from box 10), the I/O operations in PAM will stop at the respective boxes.

PAM Adapters

Figure E-10 depicts the actions taken by PAM adapters when a check condition is detected by the adapter. Check conditions can result from other than logic errors in the adapter; i.e., they may also be caused by errors in data transmission from the channel or device by conditions reported by the device through its control lines, or by failure of the channel to service an adapter in a particular period of time.

In box 1 the adapter detects a check condition and sets the associated bit in its sense register (box 2). If initial selection is in progress (yes exit from box 3), the I/O operation is not performed and the adapter presents status to the channel with Unit Check in response to the command (box 6).

If a data transfer operation is in progress (no exit from box 3), the adapter will either terminate the operation immediately or the device signals the end of transmission (yes exit from box 4 and yes exit from box 5).

Figure E-10.   PAM Adapter Error Handling
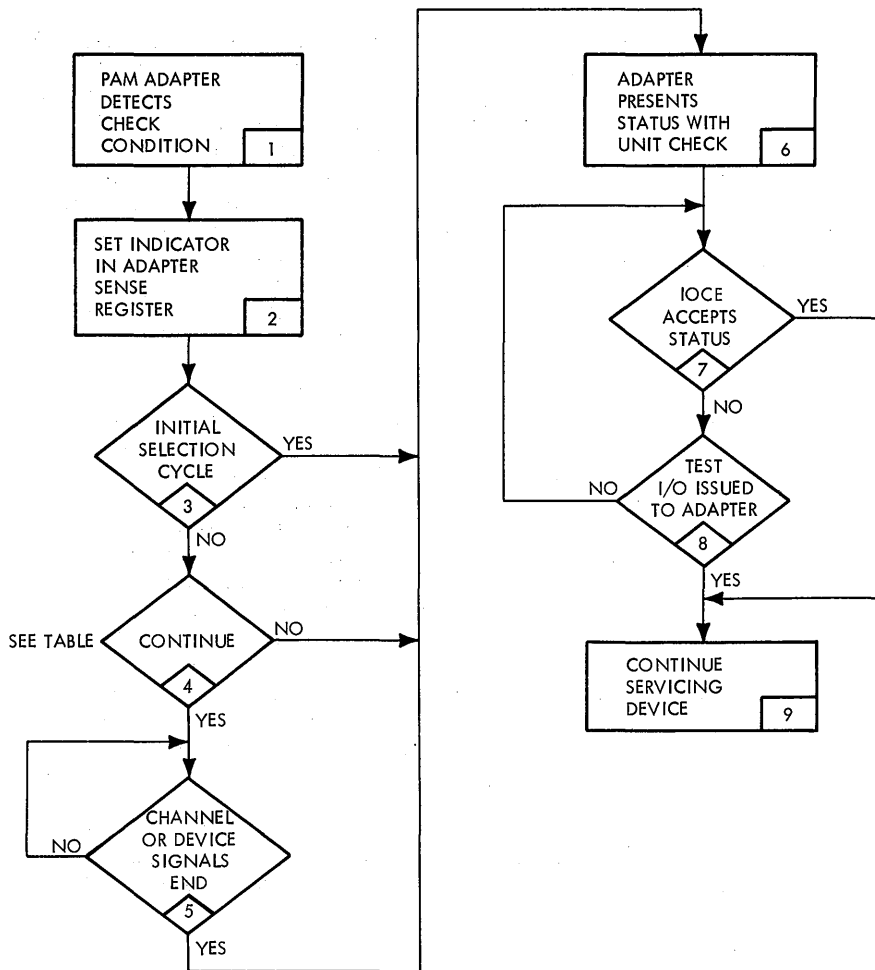
| | GPI | GPO | INTI | INTO | TTYLL | RVDP | 1052 | CD | FDEP |
|---|---|---|---|---|---|---|---|---|---|
| BUS OUT CHECK | | T | | C | C | | C | | C** |
| DATA CHECK | C | T | C | C | C | | | | C |
| EQUIPMENT CHECK | | | T | | | | C | | |
| OVERRUN | | | T | T | T | | | T | T |
| ECHO CHECK | | | T | | T | | | | T |
| LRC | | | C | | C | | | | C |
| DEVICE INOPERATIVE | | T | | | | | | | |
| DEVICE STATUS 3, 5, 6 | | T | | | | | | | |
| DEVICE STATUS 7 | | * | | | | | | | |
| INTERVENTION REQ'D | | | | | | | C | | T |
| TIMEOUT | | | | | | | | | T |

T = TERMINATE     C = CONTINUE

BLANK – NOT APPLICABLE DURING DATA TRANSFER OPERATIONS.
* MAY BE WIRED TO TERMINATE OR CONTINUE.
** IN CONTROL MODE, ADAPTER TERMINATES.

The Table in Figure E-9 indicates which adapters will continue and which will terminate data transfer for each applicable check condition.

When the data transfer is terminated, the adapter presents ending status with Unit Check (box 6). If the IOCE accepts status (yes exit from box 7) or clears status with a TEST I/O command (yes exit from box 8), the adapter is free to continue with the next command.

## 2701 MALFUNCTIONS

Figure E-11 depicts the action taken by the 2701 DAU when it detects an error condition in either the Transmission Interface Converter (XIC) or Transmission Adapter (XA). Upon detection of an error condition (box 1), the corresponding bit is set in the Sense register (box 3). The XIC will only check for an error condition on an Initial Selection Sequence (vox 4) and immediately present its status byte to the IOCE with the Unit Check bit set (box 9). If not Initial Selection Sequence the adapter continues to check for error conditions during normal data transfer cycles.

When an error is detected by the adapter during data cycles and it is a timeout (yes exit, box 5), the command is terminated (box 7) and the Unit Check bit is presented in the Status byte along with Channel End or Channel End and Device End (boxes 8 and 9). If the check detected is data parity error (no exit, box 5), the check bits are set but the command will continue until its normal end (box 6). Unit Check bit is then presented to the IOCE along with the normal ending status byte (boxes 8 and 9).

A Sense command should then be issued to the 2701 DAU to determine the exact cause of the Unit Check error indication (boxes 10 and 11). At the completion of the Sense command, the 2701 resumes its normal operation. If the Sense command is not the next command issued in sequence and the new command is not a Test I/O or NO-OP command (no exit, box 12), the Sense register will be reset (box 13).

## RCU MALFUNCTIONS

The RCU is capable of detecting abnormal conditions (box 1 of Figure E-12), both hardware (boxes 2 and 13) and operational (box 5).

Three of these conditions force an element check to be sent to all connected computer element DAR registers (boxes 22, 23, and 26). A pulsed Element Check is sent to all CEs when an OTC condition (box 23) is detected and a level Element Check is sent for CCR Parity (box 22) and Power Down (box 26) conditions. The Sense Register byte 2, bit 6 is set for a CCR Parity error (box 22) and byte 2, bit 7 is set for OTC (box 23). Both bits remain set as long as the condition exists. A valid Sense command (box 24) directed to any valid RCU address from the configured IOCE may interrogate bits 6 and 7 of byte 2 (box 10). The CCR parity bit 6, byte 2 of the Sense Register may be reset by issuing another SCON instruction (box 25).
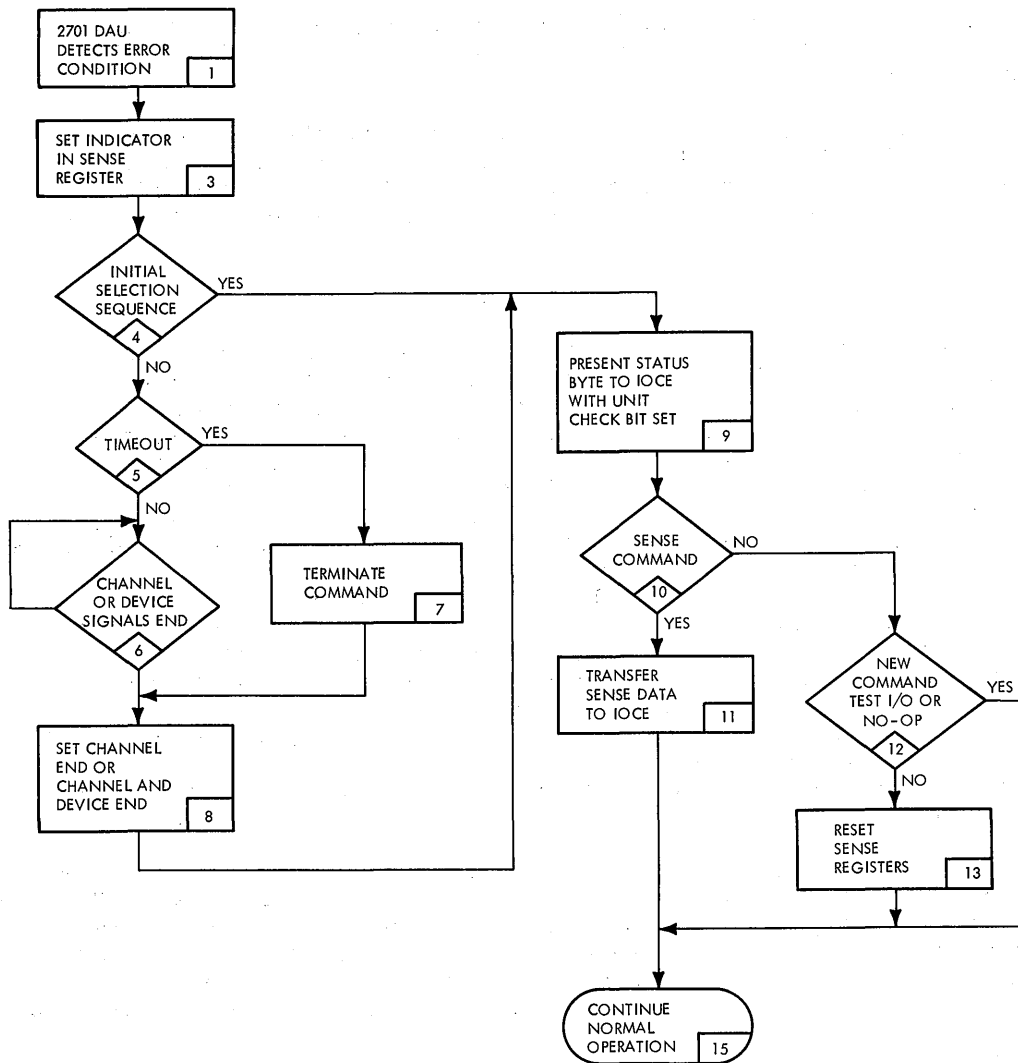
**Figure E-11. 2701 Error Handling**

Flowchart boxes:

1. 2701 DAU DETECTS ERROR CONDITION [1]
3. SET INDICATOR IN SENSE REGISTER [3]
4. INITIAL SELECTION SEQUENCE [4] — YES / NO
5. TIMEOUT [5] — YES / NO
6. CHANNEL OR DEVICE SIGNALS END [6]
7. TERMINATE COMMAND [7]
8. SET CHANNEL END OR CHANNEL AND DEVICE END [8]
9. PRESENT STATUS BYTE TO IOCE WITH UNIT CHECK BIT SET [9]
10. SENSE COMMAND [10] — NO / YES
11. TRANSFER SENSE DATA TO IOCE [11]
12. NEW COMMAND TEST I/O OR NO-OP [12] — YES / NO
13. RESET SENSE REGISTERS [13]
15. CONTINUE NORMAL OPERATION [15]

An error that is associated with the operation is a condition
where an attempt is made to issue a SCON instruction to set more
than one IOCE communication bit in the RCU CCR (boxes 5-8). In this
situation the RCU will not send a response to the SCON, but will
connect to the lowest logical IOCE, and also set bit 3, byte 2 of the
sense register (box 7). This may be interrogated by the program by
issuing a sense command to any valid RCU address through the lowest

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logical IOCE (boxes 9 and 10), or ignored by issuing a correct SCON instruction (boxes 9 and 11).

Other error conditions, both hardware and operational, will set Unit Check in the status byte (box 13) and data in the sense register (box 14). Error conditions occuring in the initial selection cycle (box 15) result in Unit Check status (box 18). Error conditions which occur during execution or termination of the command are indicated to the program by Channel End and Device End status along with Unit Check (boxes 16, 17 and 18).

In response to Unit Check status, a sense command (boxes 19 and 21) may be used to obtain detailed information as contained in the sense register or be ignored by issuing another command (box 20).
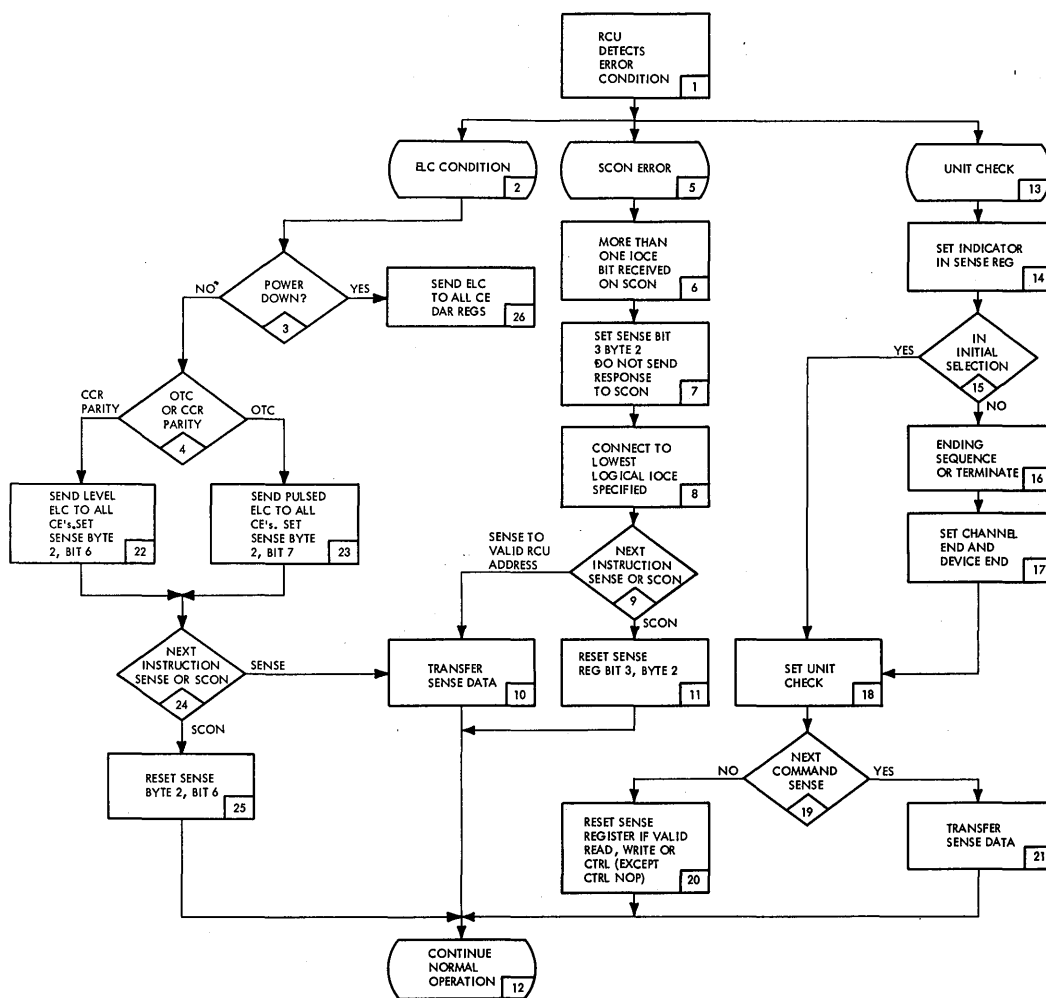


Figure E-12.   RCU Error Handling

## 2314 MALFUNCTIONS

Figure E-13 depicts the actions taken by the 2314 Storage Control
Unit upon detection of an error condition in either the SCU's own
logic or when notified of an unusual condition or check existing in
the DSU Disk Storage Unit.  When the SCU detects an unusual or check
condition (box 2) other than a SCON parity error or Element Check
condition, the appropriate information bit is set in a sense byte
(box 3).  If the check occurred during an Initial Select sequence
(box 4), the Unit Check bit is set in the Status Register (box 7).
The Status byte is then sent to the IOCE (box 8) to complete the
Initial Selection sequence.  The next instruction to the SCU should
be a Sense Command (box 9) to determine the nature of the failure
causing the Unit Check.  Sense data is then transferred to the
channel (box 10).  The SCU will then await further commands from the
IOCE (box 11).  If the check or unusual condition occurred during an
operation (box 4), the SCU would either continue to the normal end
of the operation or terminate immediately, depending on the nature
of the failure (box 5).  Channel End, Device End, and Unit Check will
be set in the Status Register (boxes 6 and 7), and the Status byte is
sent to the channel (box 8).  Operation then follows the flow
described above for boxes 9, 10, and 11.

     If the SCU detects an error which will cause an element check
bit to be sent to the CEs, the error path will be through box 12.
If power has dropped on the unit (yes exit box 13), a level Element
Check is sent to all CEs (box 21).

     When the error analysis program recognizes the level element
check, it will issue one SCON instruction to the SCU (box 16).  Upon
no reception of a 'Reconfigure Response' from the SCU (box 17), the
reconfiguration routine will drop the failing SCU from the system
configuration (box 18).

     Had the check condition been a detection of a CCR parity error
(box 14), the SCU would set bit 2 in Sense byte 4 and send a level
element check to all the CEs (box 15).  The error analysis program
would then proceed as described above for a Power Down condition
(boxes 16, 17, and 18) if the CCR parity error persists when the
SCON attempt is made.  Should the SCON be successful (no parity
error), the unit will resume normal operation (boxes 17 and 11).

     Again at box 14, should the SCU detect an OTC condition, it
will set bit 3 in Sense byte 4 and send a pulsed element check to all
CEs (box 19).  The error analysis program then has the option of
sending a Sense command to the SCU (box 20), in which case the SCU
will transfer the Sense data to the IOCE (box 23), or the reconfigu-
ration routine will configure the unit out of the active system
immediately (box 18).  The Sense byte will retain the OTC bit as
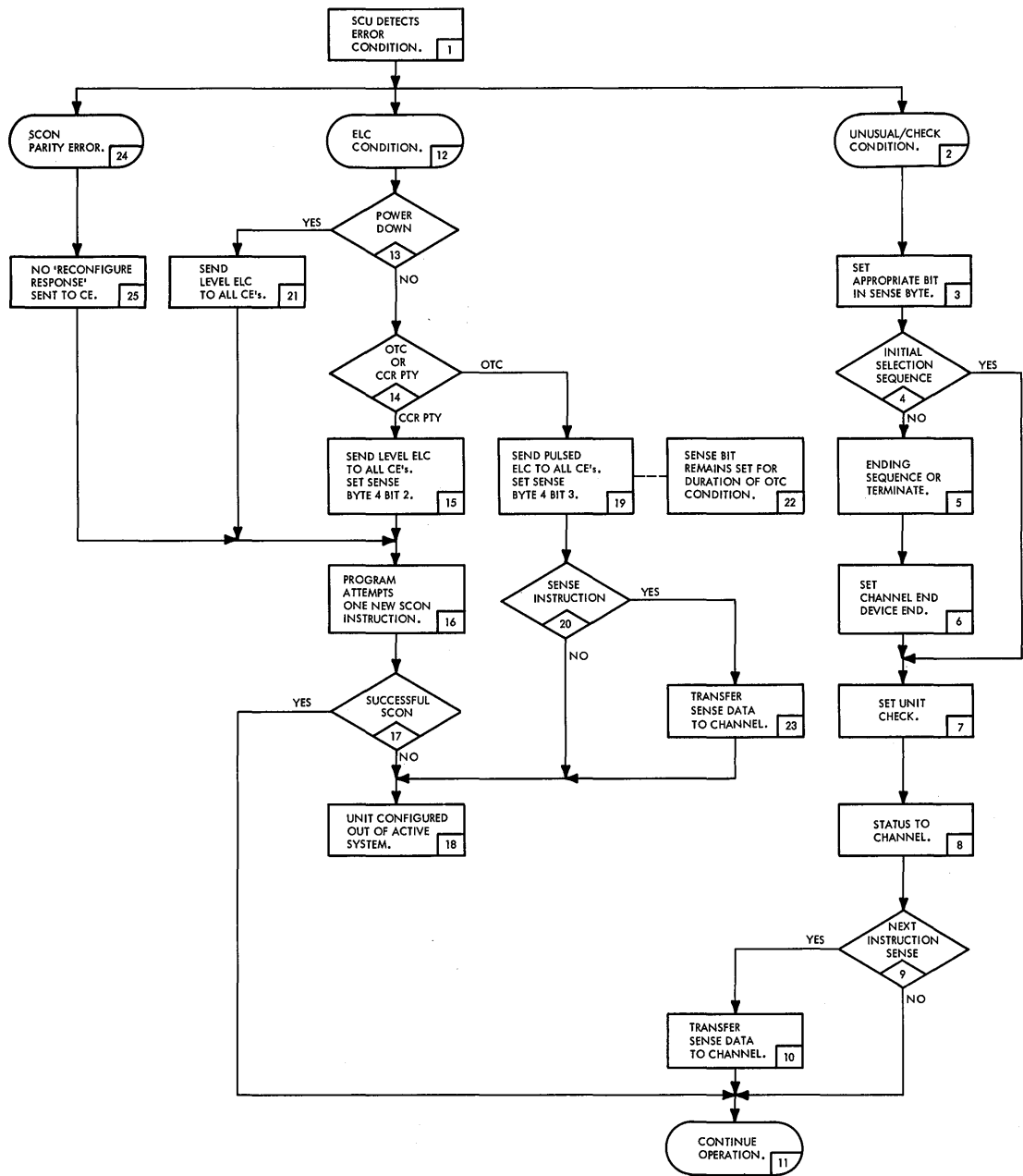long as the condition exists in the unit.

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Figure E-13.  SCU Error Handling

MAINTENANCE CONCEPTS FOR THE 9020D/E SYSTEMS

On-Line Maintenance

The on-line maintenance concept for the 9020D/E subsystems to be
followed when the CCC/9020E subsystems are used to perform the Opera-
tional Enroute Air Traffic function contains the following features
outlined below.   (The references to operational programs and routines
are for explanatory purposes only and do not constitute deliverable
items under this contract.)

1. Provide malfunction indications by detecting operational ele-
   ment malfunctions with built-in hardware and error analysis
   routines.

2. Record the element environment at the time of the malfunction
   (logout).

3. Each malfunction logout will be handled by an interrupt to an
   Error Analysis Program (OEAP-9020D/EAP-9020E).  OEAP/EAP will
   collect environmental information and will perform the follow-
   ing functions:

   a. Analyze the logout to determine the element or interface
      causing the malfunction.

   b. Count the malfunctions and record the incident rate.

   c. Retry/restart on malfunctions where practical.

   d. Record logout and other system environmental data on a
      maintenance history tape and an immediate hard-copy print-
      out.   (This data will be transmitted to the CCC for record-
      ing if malfunction occurs in the 9020E System.)

   e. Request reconfiguration when the malfunction is non-clear-
      ing (to exclude malfunctioning element from the operational
      9020D/E subsystem).

Malfunction Recognition

Malfunctions detected are outputted to the CCC operator as part of
the logout procedure.  Malfunction recognition is by the following
methods:

1. Audible Alarm - An audible alarm on the System Console will
   be energized by OEAP/EAP whenever a reconfiguration is made
   because of a malfunctioning element.

2. Printout - A message will be printed out on the CCC printer containing logout data pertinent to the 9020D/E subsystem environment at the time of the detected malfunction.

3. Operator - The operator can identify the malfunction(s) and the malfunctioning element(s) by monitoring the printer output.

4. Maintenance Personnel- Maintenance personnel will analyze the logout and along with information from the operator, determine the quickest approach to isolation and repair of the malfunction. Authorization must be received from responsible FAA personnel before actually acquiring the necessary maintenance subsystem to effect repairs.

SYSTEM HANDLING OF MALFUNCTIONS

The system provides detection, localization, count, and recording of malfunctions.

## Malfunction Detection

The primary method of malfunction detection is built in error detection circuitry supplemented with program support in the OEAP/EAP programs. A retry/restart program capability will be incorporated to minimize downtime caused by transient (intermittent) malfunctions.

## Malfunction Localization

The localization of a malfunction to a specific element or interface will be the responsibility of the 9020D Operational Error Analysis Program and/or 9020E Error Analysis Program. The OEAP/EAP, in conjunction with the hardware, must perform the following services:

1. Generate a logout signal to initiate the placing of the critical registers and pertinent malfunction conditions into a predetermined area of core storage.

2. Determine the origin or system element containing and/or generating the malfunction.

3. Determine whether a malfunction is transient (intermittent) or solid.

## Malfunction Count

A malfunction count, with its malfunction rate, will be maintained by OEAP/EAP for each individual element or interface area. The malfunction rate is defined as malfunctions per element, or per interface, per time increment. Upon encountering a malfunction, an entry will be made to the malfunction count routine which will update the count and determine the present element or interface malfunction rate. Should the malfunction rate exceed a predetermined prescribed limit, a request will be made to Reconfiguration Routine to remove the element(s) from the active system.

## Malfunction Recording

All malfunctions occurring in active 9020D/E subsystem elements will
be monitored by OEAP/EAP. A logout of the element's environment at
the time of a hardware-detected malfunction is recorded in the 9020
D/E storage element. This information is processed by OEAP/EAP
(and transferred to CCC if a 9020E malfunction) and is recorded on a
maintenance history tape and outputted in hard-copy form to the CCC
printer.

Logouts will be used to manually diagnose and identify the most
probable suspect area for transient malfunctions. This human ana-
lysis can be performed without using 9020D/E subsystem equipment.
The general content requirements of the logout are:

1. Type of check report (Element or I/O)

2. Date: Day/Month/Year

3. Time: Hours/Minutes/Seconds

4. Identity of erring equipment

5. Accumulated error counts, if applicable

6. Any additional information pertinent to machine repair such
   as:

   a. DAR bits set and English interpretation of each

   b. Type of Interrupt and Old PSW

   c. Element, Local Store, and/or Selector Channel Logouts

   d. Check register bits set and English Interpretation of
      each

   e. CSW, CCW, CAW and/or Sense information

7. Configuration at time of error (Element Check Report) or path
   used to reach device (I/O Check Report)

## Off-Line Maintenance

The off-line maintenance concept for the 9020D/E equipment to be
followed is outlined in the following procedure:

1. Perform analysis of hard-copy printout by maintenance person-
   nel to determine localized fault area within the malfunction-
   ing element.

2. Maintenance personnel request the CCC/9020E Operational
   Program to provide the minimum maintenance subsystem required
   to run off-line functional tests.

3. The OEAP/EAP reconfigures the required elements into the Maintenance Subsystem.

4. If the elements (other than the malfunctioning element) required for the minimum-sized maintenance subsystem are not available because of other malfunctioning elements, use the stand-alone maintenance facilities on the malfunctioning element to attempt a repair.

5. Use the logout as the source of information on intermittent malfunctions, thereby reducing the long repair attempts historically associated with intermittent malfunctions. This is accomplished by searching logouts for previous malfunctions made on the suspect element(s), and finding the common denominator of the intermittent malfunctions.

6. Use diagnostic Fault Locating Test Programs (FLT - on the CE and IOCE only) to isolate malfunctions to a few replaceable cards.

On elements where it is not feasible to write a fault-locating test, the Off-Line Maintenance Programs will exercise the elements and produce outputs that allow maintenance personnel to rapidly isolate the failure.

General Concepts

Concepts for the 9020D/E equipment include the following procedures:

1. Provide spare parts in quantities (specified by IBM) to ensure the availability of a spare part when required.

2. Produce maintenance manuals that complement the maintenance approach to the system.

3. Provide the minimum quantity of maintenance equipment specified by IBM required to support the system.

4. Use preventive maintenance time to maximum advantage by:

    a. Planned hardware and software tests which serve to maintain element operating levels.

    b. A maximum investigation effort of intermittent malfunctions and unresolved interface malfunctions to determine cause and resolution.

Logout Analysis

The logouts will be analyzed by maintenance personnel. The analysis will result in the following information:

1. Nature of the malfunction

2. Element or interface malfunctioning

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3. Area within element or interface malfunctioning

4. Type of maintenance program to be run.

5. Composition of the minimum size maintenance subsystem, including preferred element for interface testing when applicable.

## Maintenance Subsystem

The maintenance subsystem will be manually requested via the CCC Operators 1052 with prior authorization from responsible FAA personnel. A maintenance subsystem will comprise a minimum number of elements logically connected for performing scheduled or corrective maintenance. The operational system will configure itself so that no malfunctions may propagate through it from maintenance subsystems, providing the ability to perform scheduled or unscheduled maintenance during ATC operations without affecting ATC operations.

## Malfunction Isolation Within Element/Unit

After the logout analysis is complete and a maintenance subsystem including the malfunctioning element has been configured, the malfunction must be isolated to its cause. Maintenance programs will be the prime means of isolation.

## Maintenance Programs

The maintenance programs for the 9020D/E subsystems fall into two major categories: Checkout and Evaluation Test and Fault-Locating Test. A description of each follows.

Checkout and Evaluation Test

The checkout and evaluation tests are used to determine whether a system element is malfunction free. These tests provide malfunction detection, short running time, and minimal size. In general, checkout and evaluation tests have the following characteristics:

1. Have looping capabilities to aid in malfunction isolation

2. Localize a malfunction to a functional area

3. Have option to run in various size maintenance subsystems

4. Contain options to run all or portions of the programs

The checkout and evaluation tests are used to check the operation of the element and ensure that all operations pertaining to the element being tested are functioning properly. These checkout and evaluation tests are under control of a diagnostic monitor.

Diagnostic Monitors

All maintenance programs, except the initial CE and IOCE checkout programs, run under control of a Diagnostic Monitor (DM). The DM provides a standard means of communication between the Customer Engineer and the various maintenance programs. Common subroutines for message input/output, program loading, code conversions, and other control functions are provided by the Diagnostic Monitors. The Off-Line Maintenance Package for the 9020 D/E Systems includes three Diagnostic Monitors.

Initial Diagnostic Monitor (IDM). In the 9020 D and E Systems, IDM operates only in the IOCE. It provides a simple set of control functions required to run the IOCE Bringup Diagnostic Programs. IDM uses only the basic instructions previously checked out by the IOCE Go/No Go Tests. The Bringup Programs test the Standard Instruction Set. After insuring the functional operation of the Standard Instruction Set, IDM automatically loads the Sub-system Diagnostic Monitor (SDM) into the IOCE.

Sub-System Diagnostic Monitor (SDM). SDM is designed to operate in either the IOCE, or in one of the Computing Elements (C.E.) of the 9020 D/E System. When operated in the IOCE, it is loaded automatically by IDM. When operated in the 9020 D/E Computing Element it is automatically loaded by the C.E. Hardcore Program. The Hardcore Program performs a basic check of the instructions used by SDM. This monitor is designed to be used as the primary monitor for operating the CE and IOCE unit diagnostic programs. A set of standard input messages are available to the Customer Engineer for communication with the DM. In conjunction with these messages, SDM has the ability to search the program source for the diagnostic program section requested by the input message. This monitor can vary the sequence other than that in which they reside on tape.

Multi-Processing Diagnostic Monitor D/E (MDM D/E). MDM D/E is a Multi-Processing Diagnostic Monitor designed to operate in the Computing Elements of the 9020 D/E Systems. MDM can operate in a single processor or in a multi-processor environment. However, it will not operate in the IOCE. It has more instructions at its disposal than does SDM. Since it has the capability of controlling multiple processors, it is a much more complex monitor than is SDM. MDM is capable of executing individual diagnostic programs in any one of three modes. The first is sequential mode, one diagnostic at a time, to check individual elements serially in a single processor sub-system environment. The second mode is a multi-programming mode in which several non-conflicting diagnostic sections are executed together. The third mode of operation is a true multi-processing mode which can exercise all interconnected elements assigned to the maintenance task.

Fault Locating Tests (FLT's)

Fault Locating Tests are a set of tests that detect and locate malfunctions at the circuit level within the CE and IOCE. These tests

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are produced automatically from the same logic description as is used to manufacture the elements thus insuring that diagnostics are carried out on the element as constructed. This complete set of tests will be stored on tape. Manual controls and indicators (on the element control panel) are provided for controlling FLT operations and indicating necessary operating or failing conditions. A set of preprinted documents will be available for each malfunction, providing a suspect list, a sensitive path, and a scoping list.

FLT Options. In addition to the already mentioned controls, the following features are available:

1. Bypass the failing test - Through use of the FLT mode switch, on the IOCE or by-pass routine on the CE, a failing test may be bypassed. Thus, additional test information can be obtained.

2. Repeat a test continuously - Through use of the FLT control switch, a test may be repeated continuously without going on to the next test.

3. Stop on error - Through use of the FLT control switch, stoping on the test with the error is possible.

FLT Operation. Fault Locating Test will be read in from tape through one of the selector channels in the IOCE and will be loaded into storage. When checking the IOCE, the tests will be loaded into the MACH (Maintenance and Channel) Storage. When checking the 7201-02 Computing Element, the tests will be loaded into the 7251-09 Storage Element. Fault Locating Test patterns are designed to test the circuit elements in both the conducting and nonconducting states. The IOCE or CE being tested has a built-in automatic test feature. The automatic test feature has the ability of reading FLT patterns from an input tape, setting registers and controls accordingly, advancing the machine clock a controlled number of cycles, and comparing the selected hardware latch with a precomputed result. A failure to compare will cause the process to stop with a pattern displayed in lights tn the control panel. This pattern takes the servicing personnel to a reference document and a standard set of procedures.

These procedures enable him to find and replace, or repair, the malfunctioning circuit. If the test compares, it signifies the test passes, and this area of logic is free of failures. Tests cover ing the remainder of the logic will then be operated.

In addition to the FLT's, a set of ROS (Read Only Storage) tests will be provided. These tests are loaded from tape in a manner similar to FLT's. The ROS tests access each ROS address to ascertain that it contains the expected bit configuration.

A technique known as "Progressive Scan" will be available as a method of testing the common, multiplexor, and selector channels of the IOCE. A conventional program uses a Diagnose instruction to

execute one or more microprogramming steps of the channel operation.
These steps are followed by logouts which are compared against a
precomputed set of values. If the logout pattern and the precomput-
ed pattern are not equal, progressive scan establishes a list of
possible failing circuits.

Documentation. Fault Locating Tests do not require a printing device
to communicate with servicing personnel. Instead, all diagnostic
conclusions are displayed on the unit control panel when a diagnostic
stop occurs. Three distinct pieces of information may be obtained
by interpreting this display, and going to an applicable reference
document.

    1.   The suspect list - A list of SLT card locations containing
         those circuits which would account for the failure indication.

    2.   The sensitive path - That part of the logical network which
         is sensitive to a failure during application of this par-
         ticular test.

    3.   The scoping list - A list of the pins accessible to servicing
         personnel, with the values to be observed in a properly
         functioning circuit at those pins when the test is repeatedly
         applied.

## Maintenance Subsystem Configuration

Table F-1 lists the maintenance subsystem which will be required to
perform program analysis of a malfunction and/or checkout of an
element after scheduled or unscheduled maintenance. Maintenance
programs are run in the maintenance subsystem CE or IOCE once the
programs have been read from tapes.

In general, maintenance programs provide the primary means for
malfunction isolation as shown in column 2 of Table F-1. The second-
ary means (stand-alone) is shown in column 3 of Table F-1 and will be
used when subsystem or part of a subsystem (column 4) is not avail-
able.

## Element/Unit Repair

A malfunctioning element will be repaired primarily by removing and
replacing pluggable assemblies and/or subassemblies whenever pract-
ical. An element which malfunctions because of a logic card failure
will be repaired by replacing the logic card. The isolation of the
card causing the error will be by (dependent upon the criticality of
time):

    1. Group replacement

    2. Substitution method

    3. Scoping

## Table F-1. Maintenance Subsystems

| UNIT | MEANS OF MALFUNCTION ISOLATION | | MAINTENANCE SUBSYSTEM | |
| | PRIMARY | SECONDARY | | |
| --- | --- | --- | --- | --- |
| COMPUTING ELEMENT (7201-02) | MAINTENANCE PROGRAMS – FLT'S AND CHECKOUT AND EVALUATION TESTS | MAINTENANCE PANEL | FLT'S: | MALFUNCTIONING CE PLUS: IOCE SE TCU TAPE DRIVE |
| | | | CHECKOUT & EVALUATION TESTS: MDM | MALFUNCTIONING CE PLUS: IOCE SE TCU TAPE DRIVE 1052 |
| | | | INTERFACE: | ABOVE PLUS INTERFACE ELEMENT |
| INPUT/OUTPUT CONTROL ELEMENT (IOCE) (7231-02 | MAINTENANCE PROGRAMS – FLT'S AND CHECKOUT AND EVALUATION TESTS | MAINTENANCE PANEL | FLT'S: | MALFUNCTIONING IOCE PLUS: TCU TAPE DRIVE |
| | | | CHECKOUT & EVALUATION TEST SDM: | MALFUNCTIONING IOCE PLUS: TCU TAPE DRIVE 1052 |
| | | | CHECKOUT & EVALUATION TEST MDM | MALFUNCTIONING IOCE PLUS: CE SE TCU TAPE DRIVE 1052 |
| | | | INTERFACE: | ABOVE PLUS INTERFACE ELEMENT |
| STORAGE ELEMENT (7251-09) | MAINTENANCE PROGRAMS – CHECKOUT AND EVALUATION TESTS | MAINTENANCE PANEL | | MALFUNCTIONING SE PLUS: CE IOCE TCU TAPE DRIVE 1052 1403 2821 |
| DISPLAY ELEMENT (7289-04) | MAINTENANCE PROGRAMS – CHECKOUT AND EVALUATION TESTS | MAINTENANCE PANEL | | MALFUNCTIONING DE PLUS: CE SE IOCE TCU TAPE DRIVE 1052 1403 2821 |

Table F-1.  Maintenance Subsystems (Cont.)

| UNIT | MEANS OF MALFUNCTION ISOLATION | | MAINTENANCE SUBSYSTEM |
| | PRIMARY | SECONDARY | |
|---|---|---|---|
| DATA ADAPTER UNIT (2701-01 | MAINTENANCE PROGRAMS | I/O TESTER | MALFUNCTIONING 2701 PLUS:<br>IOCE<br>1052<br>TCU<br>TAPE DRIVE |
| CONFIGURATION CONSOLE (7265-03) | MAINTENANCE PROGRAMS | MAINTENANCE PANEL | MALFUNCTIONING CC PLUS:<br>CE<br>SE<br>IOCE<br>1052<br>TCU<br>TAPE DRIVE |
| SYSTEM CONSOLE (7265-02) | MAINTENANCE PROGRAMS | MAINTENANCE PANEL | MALFUNCTIONING SYSTEM CONSOLE PLUS:<br>FUNCTIONAL TEST #1<br>CE<br>SE<br>IOCE<br>PAM<br>TCU<br>TAPE DRIVE<br>1052 PRINTER/KEYBOARD (PAM)<br><br>FUNCTIONAL TEST #2<br>IOCE<br>TCU<br>TAPE DRIVE<br>1052 (SYS. CONS.) |
| INTEGRATED CONTROL UNIT (2821)<br><br>READER/PUNCH (2540)<br><br>PRINTER (1403) | MAINTENANCE PROGRAMS | I/O TESTER | MALFUNCTIONING 2821 PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE<br>1052<br><br><br>MALFUNCTIONING 2540/1403 PLUS:<br>ABOVE AND 2821<br><br>INTERFACE:   SYSTEM CONSOLE<br>                    2821<br>                    2540/1403 |
| TAPE CONTROL UNIT (2803) | MAINTENANCE TEST PANEL W/TAPE DRIVE(S) | MAINTENANCE PROGRAMS | MALFUNCTIONING 2803 PLUS:<br>9020D SYSTEM<br><br>IOCE<br>SYSTEM CONSOLE 1052<br>2821<br>2540<br>TAPE DRIVE(S)<br><br>9020E SYSTEM<br><br>IOCE<br>TAPE DRIVE(S)<br>TCU (NONFAILING)<br>1052 |
| TAPE DRIVE (2401-2/3) | MAINTENANCE PROGRAMS | TAPE DRIVE TESTER | MALFUNCTIONING 2401 PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE (NONFAILING)<br>1052 |

Table F-1.  Maintenance Subsystems (Cont.)

| UNIT | MEANS OF MALFUNCTION ISOLATION | | MAINTENANCE SUBSYSTEM |
| | PRIMARY | SECONDARY | |
|---|---|---|---|
| PAM COMMON & ADAPTERS (OTHER THAN 1052 ADAPTER)  (7289-02) | MAINTENANCE PROGRAMS | MAINTENANCE TEST PANEL | MALFUNCTIONING PAM PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE<br>1052 (SYSTEM CONSOLE 1052 IF PAM COMMON FAILING; FOR ADAPTER FAILURES THE PAM 1052 MAY BE USED) |
| PAM 1052 ADAPTER | MAINTENANCE PANEL ON 1052 PRINTER/KEYBOARD | 1.  MAINTENANCE PROGRAMS<br><br>2.  PAM MAINTENANCE TEST PANEL | MALFUNCTIONING PAM PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE<br>1052 (PAM) |
| PAM 1052 PRINTER/KEYBOARD | OLSA 1052 TESTER | MAINTENANCE PROGRAMS | MALFUNCTIONING 1052 PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE<br>PAM |
| DIRECT ACCESS STORAGE FACILITY (2314) | TEST PANEL<br><br>RESIDENT MICRODIAGNOSTICS-SCU<br><br>IN-LINE MICRODIAGNOSTICS-DSU | MAINTENANCE PROGRAMS | MALFUNCTIONING DASF PLUS:<br>IOCE<br>TCU<br>TAPE DRIVE<br>1052 |

## Verification

The malfunctioning element will be checked for verification of re-
pair.  The method used to isolate the malfunction will be repeated
to ensure that the repair has corrected the malfunction, that is,
the failing checkout and evaluation test or FLT will be repeated
after the repair is made.

The element may now be returned to a state recallable by the
operational system.  A manual intervention, via the 1052 Keyboard
Printer, is required to return any element to ATC at the completion
of any maintenance action.  A request is made to the reconfiguration
routine to return the repair element for assignment to a recallable
state.

## Preventive Maintenance

The 9020E subsystem preventive maintenance schedule will be integrat-
ed with the present 9020A CCC schedule.  The maintenance tasks will
be scheduled in such a manner as to enable the shortest time required
to cease maintenance and start performing ATC operational program
tasks.  Preventive maintenance time will also be the prime method
used for investigating all intermittent problems.

## Maintenance Features

The pertinent maintenance features of each 9020D/E equipment element
are listed under the appropriate equipment element name.

## 7201-02 COMPUTING ELEMENT

1. Failure Detection and Error Handling:

    a. The 7201-02 Computing Element contains logic for separate detection and handling mechanisms for both malfunctions and for program errors.

    b. Logout - facilities for the presentation of machine and program status at the time of failure detection, thus enabling program analysis of abnormal machine conditions and rapid accurate error isolation.

2. System Control Panel:

    a. Provides the ability to manipulate machine status so that pertinent data and control information can be used in the diagnosis and repair of any machine failure.

    b. Use of panel switches, indicators, and roll charts provides the means of checking areas not checked by programs.

    c. Provides power indicators, controls and marginal checking.

3. Maintenance Program Package (consist of two general categories:)

    a. Fault Locating Test.

    b. Off Line Maintenance Programs.

        (1) Diagnostic Monitors
        (2) Unit level programs
        (3) System Evaluation Program (SEVA)

## 7251-09 STORAGE ELEMENT

1. Failure Detection and Error Handling:

    a. Storage Data Checks will be flagged when a storage data register parity error occurs.

    b. Storage Address Checks will be flagged on a CE access when a parity error is detected in address, mark, key, or box tag, or box tag mismatch, multiaccept, or invalid operation on an IOCE access, Storage Check is flagged.

    c. Element Check only is sent to all CE's following error conditions:

        (1) Thermal Condition
        (2) On Battery Supply
        (3) CCR Parity Check
        (4) Logout Stop (not always an error condition)
        (5) Power Off

d. Logout – a presentation of storage status when an error is detected by the Storage Element.

2. Maintenance Panel:

   a. Manual controls to cause repetitive cycling of the storage for the purpose of testing and scoping.

      (1) Storage cycling (ones and zero's)
      (2) Repetitive beat tests (Store/fetch one location/byte)
      (3) Cycle test for addressing problems
      (4) Test priority and control logic of the Storage Switch Unit.

   b. Indicators of registers and check triggers for use in trouble shooting when in the manual situation and as they apply to logout.

3. Power Panel:

   a. Indicators and control for power and thermal fault conditions.

   b. Marginal Check control for biasing.

4. Maintenance Programs:

   a. Diagnostic routines for functional and diagnostic testing.

   b. Diagnostic routine for providing means for schmoo testing.

7289-04 DISPLAY ELEMENT

1. Failure Detection and Error Handling

   a. Storage Data Checks will be flagged when a Storage data register parity error occurs.

   b. Storage Address Checks will be flagged when a parity error is detected in address, mark, key, and box tag; or there is a box tag mismatch, or a multiaccept or normal operation check.

   c. Element Check only is sent to all users (CE's):

      (1) When a parity error is detected on a DG address, data, local store and DG register.

      (2) Thermal condition or On Battery Supply

      (3) CCR Parity Check

      (4) Logout Stop Check

      (5) Power Off

d. Logout, a presentation of storage status when an error is
　　　　 detected by the Display Element.

2.　Maintenance Panel

　　　a. Manual controls to cause repetitive cycling of the storage
　　　　 for the purpose of testing and scoping.

　　　b. Indicators of registers and check triggers of storage,
　　　　 priority and control circuits for use in trouble shooting
　　　　 when in the manual situation and as they apply to logout.

3.　Power Panel

　　　a. Indicators and control for power and thermal fault condition

　　　b. Marginal Check control for biasing.

4.　Maintenance Programs

　　　a. Diagnostic routines for functional and diagnostic testing
　　　　 of the Display Element control circuitry and arrays.

　　　b. Diagnostic routine to provide means for shmoo testing.

　　　c. Diagnostic routines for functional and diagnostic testing
　　　　 DG control circuitry (including wrap test).

INPUT/OUTPUT CONTROL ELEMENT (IOCE)

1. Failure Detection and Error Handling:

　　　a. If unable to obtain a cycle from a storage element; the
　　　　 IOCE notifies the using CE of program check via the channel
　　　　 status word.

　　　b. If an error is detected in its own common logic area, the
　　　　 IOCE notifies using CE of IOCE Machine Check and begins
　　　　 logout, when signalled to do so by CE.

　　　c. Occurrence of Channel Control Check or Interface Control
　　　　 Check during an I/O instruction (other than Test Channel)
　　　　 initiates a Selector Channel Logout.

2. Control Panel:

　　　a. In diagnostic mode the IOCE can perform a limited set of
　　　　 instruction executions.

　　　b. Capable of controlling Maintenance Operations using MACH
　　　　 storage.

　　　c. Switches and indicators provide the capability for storing
　　　　 and display of registers and storage locations.

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d. Provide power indicators and control and marginal checking.

3. Maintenance Programs:

   a. Fault Locating Tests for checking hardcore, read only storage, common logic unit data flow and control circuits, multiplex circuits, and the common channel and the selector channel. The FLT's may be loaded under their own (IOCE) control. Special FLT load circuitry is provided when the FLT Load switch is depressed on the control panel.

   b. Functional tests for interface checking, local store, MACH storage and an overall functional check of the IOCE.

2701 DATA ADAPTER UNIT

1. Failure Detection and Error Handling:

   a. Hardware detection circuits for both control failures and parity errors.

   b. Error indications sent to channel in sense and status words for program analysis and handling.

2. I/O Tester:

   a. The standard I/O testers with appropriate overlay panel when plugged into the 2701 can simulate all operations of the I/O channel for off-line diagnosis.

   b. The I/O tester may also be set-up for use while the 2701 is on-line for diagnosis of failure which may be occurring only during on-line operation.

3. Maintenance Programs:

   a. Diagnostic commands are provided to allow the Diagnostic Program to check the 2701 without the use of the Radar Keyboard Multiplexor (RKM).

7265-02 SYSTEM CONSOLE - 9020D SYSTEM

1. Failure Detection and Error Handling

   a. Status byte information at start and completion of each I/O operation.

   b. The sense byte information will indicate more specific details on the error condition encountered.

2. Maintenance and Operator's Panels.

   a. Manual controls and indicators (in conjunction with in-dicators on Operator's Panel) to test and diagnose mal-functions of unit controls and functions.

b. Power and thermal indicators and controls on Operator's panel.

c. Marginal checking facilities for biasing.

3. Maintenance Programs

a. Diagnostic routines for functional and diagnostic testing.

    (1) Functional Test #1.  This functional test will be run for complete checkout of the console control unit. Visual indications will be checked by maintenance personnel.

    (2) Functional Test #2. This functional test will provide a checkout of the system console 1052 Printer/Keyboard and its control unit.

7265-03  CONFIGURATION CONSOLE - 9020E SYSTEM

1. Failure Detection and Error Handling

a. Element check is sent to each CE upon detection of critical Reconfiguration Control Unit error.

    (1) Power down on the RCU

    (2) CCR Parity error

    (3) Overtemperature check

b. Status byte information at start and completion of each I/O operation.

c. The sense byte information will indicate more specific details on the error condition encountered.

2. Maintenance and Operator's Panels

a. Manual controls and indicators (in conjunction with indicators on Operator's Panel) to test and diagnose malfunctions of unit controls and functions.

b. Power and thermal indicators and controls on each operator's panel.

c. Marginal checking facilities for biasing.

3. Maintenance Programs

a. Diagnostic routines for functional and diagnostic testing.

2803 TAPE CONTROL UNIT

1. Failure Detection and Error Handling.

    a. On the 9020D/E System an Element check is sent to each CE upon detection of critical Tape Control Unit errors:

        (1) Overcurrent condition

        (2) Power off condition

        (3) CCR parity error

    b. On the 9020D/E Systems, status byte information at the start and completion of each I/O operation.

    c. The sense byte information will indicate more specific details on the error condition encountered.

2. Tape Control Unit Test Panel

    a. The test panel will be the prime means of malfunction isolation.  (On the 9020D System, localization of the malfunction within the control unit will be determined by the logout analysis)

    b. Marginal checking facilities for biasing.

3. Maintenance Programs.

    Maintenance programs will be used primarily for checkout and verification.

    (Note:  On the 9020D System, if the repair has not been made, program loading will be accomplished through the card reader.)

2401-02/03 TAPE DRIVE

1. Failure Detection and Error Handling

    a. Status byte information at the start and completion of each I/O operation.

    b. The sense byte information will indicate more specific details on the error condition encountered.

2. Tape Drive Tester

    a. The tape drive tester will be used for isolation and repair.

3. Maintenance Programs

The tape maintenance programs can be used for initial off-
line malfunction localization.  They will be used primarily
for checkout and verification.

7289-02 PERIPHERAL ADAPTER MODULE 9020D SYSTEM

PAM COMMON

1. Failure Detection and Error Handling

    a. Element check is sent to each CE upon detection of critical
       PAM Common errors:

       (1) Check-stop error in priority controls

       (2) Power Failure

       (3) Parity Check in the CCR

    b. Status byte information at the start and completion of
       each I/O operation.

    c. The sense byte information will indicate more specific
       details on the error condition encountered.

2. Maintenance Test Panel

    a. Manual controls and indicators used to test and diagnose
       malfunctions of unit controls and functions.

    b. Power and thermal controls and indicators.

    c. Marginal checking facilities for biasing.

3. Maintenance Programs

    a. Diagnostic routines for functional and diagnostic testing.

PAM 1052 ADAPTER

1. Failure Detection and Error Handling

    a. Status byte information at the start and completion of
       each I/O operation.

    b. The sense byte information will indicate more specific
       details on the error condition encountered.

2. Maintenance Test Panel

    a. Controls and indicators on the 1052 Printer/Keyboard can
       be used to diagnose and test the adapter.

b. Controls and indicators on the PAM maintenance panel to test and diagnose adapter malfunctions with or without the use of the 1052-7 Printer/Keyboard.

3. Maintenance Programs

a. Diagnostic routines for functional and diagnostic testing the 1052 adapter. Programs routines can be run with or without the 1052-7 Printer/Keyboard.

PAM 1052 PRINTER/KEYBOARD

1. Failure Detection and Error Handling

a. Status information through the 1052 adapter at the start and completion of each I/O operation.

b. The sense byte information will indicate more specific details on the error condition encountered.

2. Maintenance Test Panels

a. The 1052 Printer/Keyboard test panel controls and indicators, in conjunction with the PAM 1052 adapter can be used to diagnose and test unit malfunctions.

b. The PAM maintenance test panel controls and indicators, in conjunction with the PAM 1052 adapter, can be used to diagnose and test unit malfunctions.

3. Tester.

a. The off-line Selectric Analyzer (OLSA) for isolation of unit malfunction and testing.

4. Maintenance Programs

a. Functional test programs to check the 1052 Printer/Keyboard and interface.

PAM - Other Adapters

1. Failure Detection and Error Handling

a. Status byte information at the start and completion of each I/O operation.

b. The sense byte information will indicate more specific details on the error condition encountered.

2. Maintenance Test Panel

a. Controls and indicators for diagnosing and testing adapter malfunctions.

3. Maintenance Programs

   a. Diagnostic routines for checking and isolating adapter
      malfunctions.

      NOTE:  Adapter malfunctions may be deferred to non-peak
      periods.  Functional tests will be used for complete
      checkout of the PAM adapters.  The tests check the PAM
      adapters out almost to their interfaces, and do not
      exercise the devices connected to the PAM.

2821, 2540, and 1403

1. Failure Detection and Error Handling.

   a. Status byte information at the start and completion of
      each I/O operation.

   b. The sense byte information will indicate more specific
      details on the error condition encountered.

2. I/O Tester

   a. The I/O Tester is used to diagnose and check unit mal-
      functions.

3. System Console Maintenance Panel

   a. System Console maintenance panel to check out interface.

4. Maintenance Programs

   a. Diagnostic routines for diagnosing and checking unit
      malfunctions.

2314 DIRECT ACCESS STORAGE FACILITY

1. Failure Detection and Error Handling

   a. Element check to each CE of the 9020D System upon detection
      of critical errors:

      (1) Power down.

      (2) CCR Parity error.

      (3) Overtemperature check

   b. Status byte information at the start and completion of each
      I/O operation.

      (1) The sense byte information will indicate more specific
          details on the error condition encountered.

2. Maintenance Panels

   a. Manual controls and indicators to test and diagnose unit malfunctions.

   b. Marginal checking potentiometers are located on each power supply for biasing.

3. Maintenance Programs

   There are three types of maintenance programs which can be used for malfunction diagnosis, functional testing, and verification of repair:

   a. Resident Microdiagnostics - These are the primary means of malfunction diagnosis for the SCU (Storage Control Unit). Program is called in from the test panel.

   b. In-Line Microdiagnostics - These are the primary means of malfunction diagnosis for the DSU (Disk Storage Unit). Program is called in from the test panel.

   c. On-Line Diagnostics - Used to check functional operation of unit using channel interface. Can be used to verify repairs. Programs are under control of either MDM or SDM.

This appendix lists the worst case situations.  The probability of overrun cannot be calculated without a detailed operational analysis (program definition, specific timings, message size, and counts, etc.).

The maximum data transfer rate that may be sustained at each channel without overrun depends upon a complex channel inter-dependence, data transfer times between the channel and I/O device, and SE availability.  Table G-1 specifies data transfer rates for five programming modes:  no data chaining, data chaining with and without a Transfer-In-Channel (TIC) command, and with and without data blocks on word boundary.  These five modes, specified for seven combinations of one or more channels, have been selected as representative reference points for channel performance.  The data transfer rates were established within each mode by assuming all other channels in that particular combination were programmed in the same manner.  Higher rates are possible at other channels when programmed in a less restrictive mode, but it is incorrect to combine values from different modes.

The data transfer rate specified for each selector channel can be sustained, for the indicated assumptions, without overruns (loss of data bytes) at the attached control unit and/or I/O device.  The rate specified for the multiplexor channel can be sustained, for the indicated assumptions, at 1 to 256 I/O devices.  The specified data rates at the multiplexor channel do not relate to overruns, since there are other factors which enter into the determination of overrun conditions.  Overruns occur at an I/O device when the time to service one lower priority I/O device and all higher priority I/O devices exceeds the maximum waiting time associated with the data buffer.  The time for the channel to service these other I/O devices depends upon the type of operation (i.e., initial selection, data cycle, status cycle) at the I/O device.  The time of service also varies with chaining, burst mode, method of ending operation, and other channel interference and delay in accessing storage.

The maximum data transfer rate is possible at any channel when it is operating alone and without data chaining or storage delay.  The delay encountered when accessing the Storage Element is specified by the parameter D.  The columns D≠0 and D=0 are used to specify rates with and without storage delay, respectively.

Data chaining reduces the data rates at each channel, which is further reduced through the use of a Transfer In Channel (TIC) command and/or data blocks that use byte boundaries (i.e., don't begin or end on word boundaries).  The data rate reduction caused by data blocks of less than 12 bytes at the selector channels is not shown, but in the worst case the data rate would be approximately half of that shown in the byte boundary column.

# Table G-1.   Data Transfer Rates

| CHANNELS (PAM Assumed on MPX Chan.) | | NO DATA CHAINING (Command Chaining at Selector Channels Only) | | DATA CHAINING (Selector Channel Count ≥ 12 Bytes) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | NO TIC | | | | TIC | | | |
| | | | | Word Boundary | | Byte Boundary | | Word Boundary | | Byte Boundary | |
| | | $D=0$ | $D \neq 0$ | $D=0$ | $D \neq 0$ | $D=0$ | $D \neq 0$ | $D=0$ | $D \neq 0$ | $D=0$ | $D \neq 0$ |
| Multiplexor | | 40KB | $\frac{10^3}{25+1D}$ | 22KB | $\frac{10^3}{45.5+3D}$ | 22KB | $\frac{10^3}{45.5+3D}$ | 18KB | $\frac{10^3}{55.5+5D}$ | 18KB | $\frac{10^3}{55.5+5D}$ |
| Selector (1, 2 or 3) | | 800KB | $\frac{10^3}{1.25+.25D}$ | 500KB | $\frac{10^3}{2+.5D}$ | 200KB | $\frac{10^3}{5+D}$ | 400KB | $\frac{10^3}{2.5+.67D}$ | 125KB | $\frac{10^3}{8+2D}$ |
| 2 SEL | Sel #1 | 500KB | $\frac{10^3}{2+.5D}$ | 375KB | $\frac{10^3}{2.67+.7D}$ | 143KB | $\frac{10^3}{7+2D}$ | 285KB | $\frac{10^3}{3.5+D}$ | 83KB | $\frac{10^3}{12+4D}$ |
| | Sel #2 | 400KB | $\frac{10^3}{2.5+.5D}$ | 250KB | $\frac{10^3}{4+1.1D}$ | 71.5KB | $\frac{10^3}{14+3D}$ | 190KB | $\frac{10^3}{5.25+1.5D}$ | 50KB | $\frac{10^3}{20+6D}$ |
| 3 SEL | Sel #1 | 400KB | $\frac{10^3}{2.5+.33D}$ | 285KB | $\frac{10^3}{3.5+D}$ | 100KB | $\frac{10^3}{10+2.5D}$ | 214KB | $\frac{10^3}{4.67+1.33D}$ | 66.5KB | $\frac{10^3}{15+4D}$ |
| | Sel #2 | 300KB | $\frac{10^3}{3.3+.33D}$ | 200KB | $\frac{10^3}{5+1.25D}$ | 67KB | $\frac{10^3}{15+4D}$ | 160KB | $\frac{10^3}{6.25+1.8D}$ | 50KB | $\frac{10^3}{20+6D}$ |
| | Sel #3 | 200KB | $\frac{10^3}{5+.33D}$ | 143KB | $\frac{10^3}{7+2D}$ | 50KB | $\frac{10^3}{20+6D}$ | 107KB | $\frac{10^3}{9.33+2.67D}$ | 33.3KB | $\frac{10^3}{30+9D}$ |
| MPX, SEL | MPX | 37.5*KB | $\frac{10^3}{26.7+3D}$ | 14.3KB | $\frac{10^3}{70+14D}$ | 16.7KB | $\frac{10^3}{60+10D}$ | 11.1KB | $\frac{10^3}{90+20D}$ | 14KB | $\frac{10^3}{72+14D}$ |
| X = 1, 2 or 3 | Sel X | 500KB | $\frac{10^3}{2.0+.50D}$ | 200KB | $\frac{10^3}{5+D}$ | 80KB | $\frac{10^3}{12.5+2.5D}$ | 143KB | $\frac{10^3}{7+1.25D}$ | 41.7KB | $\frac{10^3}{24+4.5D}$ |
| MPX & 2 SEL | MPX | 36*KB | $\frac{10^3}{27.8+3D}$ | 11KB | $\frac{10^3}{92+20D}$ | 15KB | $\frac{10^3}{66.5+13D}$ | 10.5KB | $\frac{10^3}{94+21D}$ | 10.5KB | $\frac{10^3}{94+21D}$ |
| | Sel #1 | 400KB | $\frac{10^3}{2.5+.50D}$ | 125KB | $\frac{10^3}{8+1.4D}$ | 50KB | $\frac{10^3}{20+3.5D}$ | 91KB | $\frac{10^3}{11+2D}$ | 29.5KB | $\frac{10^3}{34+6D}$ |
| | Sel #2 | 360KB | $\frac{10^3}{2.78+.75D}$ | 83KB | $\frac{10^3}{12+2.1D}$ | 28KB | $\frac{10^3}{36+6.5D}$ | 59KB | $\frac{10^3}{17+3D}$ | 15.5KB | $\frac{10^3}{64+12D}$ |
| MPX & 3 SEL | MPX | 35*KB | $\frac{10^3}{28.6+4D}$ | 11.4KB | $\frac{10^3}{87.5+19D}$ | 11.4KB | $\frac{10^3}{87.5+19D}$ | 10.2KB | $\frac{10^3}{98+22D}$ | 10.2KB | $\frac{10^3}{98+22D}$ |
| | Sel #1 | 300KB | $\frac{10^3}{3.33+.50D}$ | 91KB | $\frac{10^3}{11+1.8D}$ | 33KB | $\frac{10^3}{30+5D}$ | 67KB | $\frac{10^3}{15+2.6D}$ | 25KB | $\frac{10^3}{40+7D}$ |
| | Sel #2 | 300KB | $\frac{10^3}{3.33+.75D}$ | 67KB | $\frac{10^3}{15+2.5D}$ | 21KB | $\frac{10^3}{47+8D}$ | 50KB | $\frac{10^3}{20+3.5D}$ | 16KB | $\frac{10^3}{63+11D}$ |
| | Sel #3 | 160KB | $\frac{10^3}{6.25+1.0D}$ | 45KB | $\frac{10^3}{22+3.8D}$ | 17KB | $\frac{10^3}{58+10D}$ | 33KB | $\frac{10^3}{30+5.25D}$ | 11KB | $\frac{10^3}{90+16D}$ |

*This value is 40KB average data transfer rate when using multiple devices at PAM

The following factors were considered in preparing Table G-1:

Multiplexor Channel

1. The data transfer rate assumes continuous requests for data transfers, but no requests for status transfers due to command chaining or ending an I/O operation. Initial selection of an I/O device does not occur.

2. The data transfer time is based on the worst case for PAM and the multiplexor channel. For PAM, this time is 12 usec, 4 usec of which are overlapped with channel operation. The time includes 200-nanosecond cable and wiring delay for each signal transmission.

3. PAM is the highest priority control unit, and no Select Out delay time occurs.

4. Data transfer rates are based on multiplex mode and any record length.

5. Interference from the selector channels is based on the maximum specified data transfer rates for these channels in the corresponding programming mode.

Selector Channel

1. The time corresponding to the specified data transfer rate must be consistent with the rules in Appendix D of Design Data which specifies control unit response times and cable delay times.

2. The byte count of a data block during data chaining is 12 bytes or more.

3. The control units do not permit data suppression, which is a method for the channel to request the control unit to momentarily stop data transfers.

4. The data transfer rate of the selector channel is established through clocking at the control unit so that the specified maximum rates are not exceeded. The rate may be fixed or variable if these rates are not exceeded.

5. Interference from the multiplexor channel was based on an instantaneous maximum rate that is variable and could approach 75 KB.

6. The first data byte for a selector channel write operation is located on a word boundary.

STORAGE ELEMENT

The value D represents the time waiting for the SE to be available.
The worst case value of D, dependent upon the number of IOCEs and
CEs using the SE, is as follows:

SE WAITING TIME (D)

| Number of IOCE's | Number of CE's | $D_1$ (Worst Case)* | $D_2$ (Worst Case)** | |
|---|---|---|---|---|
| 1 | 0 | 2.5 | 5.0 | |
| 1 | 1 to 4 | 4.3 | 6.8 | |
| 2 | 0 | 4.3 | 6.8 | (Note 1) |
|   |   | 4.3 | 6.8 | (Note 2) |
| 2 | 1 to 4 | 5.5 | 8.5 | (Note 1) |
|   |   | 5.6 | 8.6 | (Note 2) |
| 3 | 0 | 5.5 | 8.5 | (Note 1) |
|   |   | 5.5 | 8.5 | (Note 2) |
|   |   | 5.6 | 8.6 | (Note 3) |
| 3 | 1 to 4 | 7.3 | 10.3 | (Note 1) |
|   |   | 7.3 | 10.3 | (Note 2) |
|   |   | 7.3 | 10.3 | (Note 3) |

* With IOCE processor operating from Main Storage without any
  double-cycle operations.

** Added one IOCE double-cycle operation during each D.

NOTES: 1. Higher priority IOCE.
       2. Second highest priority IOCE.
       3. Lowest priority IOCE.

PRIORITY

Channel priority in the IOCE is dependent on the type of operation
at the channel; e.g., data transfer with Storage Elements, chaining
(command or data), and starting or ending a command.

The priority of channel operations, in order of decreasing
priority, is shown below:

| | |
|---|---|
| *Priority 0 | Selector 1 Data Transfer, L.S.<br>Selector 2 Data Transfer, L.S.<br>Selector 3 Data Transfer, L.S. |
| **Priority 1 | Selector 1 - Data Transfer<br>Selector 2 - Data Transfer<br>Selector 3 - Data Transfer |
| Priority 2 | Multiplexor - Data Transfer<br>Selector 1 - Data Transfer or Chaining<br>Selector 2 - Data Transfer or Chaining<br>Selector 3 - Data Transfer or Chaining |
| Priority 3 | Multiplexor - Chaining, starting, or<br>  ending<br>Selector 1 - Starting or ending<br>Selector 2 - Starting or ending<br>Selector 3 - Starting or ending |
| ***PCI | Multiplexor<br>Selector 1<br>Selector 2<br>Selector 3 |

*Data transfer to or from a buffer register in Local Storage.

**Special priority, controlled by a Selector Channel, which occurs
  when that channel determines that it is approaching an overrun
  condition. Normally, data transfers are Priority 2.

***Set up interruption for PCI flag bit in CCW or SPCI Instruction.

ABO –                  Address Bus Out

Activate –             A pushbutton which causes an operation to be
                       initiated, such as the changing of a Configura-
                       tion Control Register SCON bits.

Adapter –              The distinguishable hardware which provides the
                       controls and signals to control a specific input-
                       output device.

Address Keys –         These keys allow the addressing, by byte or word,
                       of any addressable location in main or local
                       storage.  These keys also serve as a final loop
                       address.

AR –                   Abbreviation for Address Register.

Back-up –              An alternative or fall-back position, used mainly
                       in conjunction with the power system.

Battery Power –        A temporary back-up power system for CE's,
                       IOCE's, DE's and SE's to be automatically avail-
                       able when main line power fails.

BSM –                  Abbreviation for Basic Storage Module.

BP –                   Abbreviation for Buffer Processor Adapter.

Burst Mode –           The mode of operation during which all channel
                       facilities are monopolized for the duration of
                       data transfer to or from a particular I/O device.

Bus –                  A set of common lines over which data and/or
                       controls can be transmitted.

Busy –                 A device status (Condition Code 2); indicates
                       that the device is active.

Byte –                 A group of 8 bits.

CAW –                  Abbreviation for Channel Address Word.

CB –                   Abbreviation for Circuit Breaker.

CC –                   Abbreviation for Configuration Console/Condition
                       Code.

CCR –                  Abbreviation for Configuration Control Register

| | |
|---|---|
| CCW - | Abbreviation for Channel Control Word. |
| CD - | Abbreviation for Common Digitizer Adapter. |
| CE - | Abbreviation for Computing Element. |
| CE Battery Frame - | Part of the main wall section located between two SE's or DE's. Provides battery packs and associated hardware for CE(s) contained on the wall. Inter Frame cabling is routed through this frame. |
| CE Check Control Switch - | A switch used for maintenance purposes which has three positions: Stop, Disable, and Process. When a CE check occurs, the setting of this switch controls the subsequent activity. Process is the normal position. |
| CCC - | Abbreviation for the Central Computer Complex portion of NAS. |
| Channel - | Associated with an IOCE; is the avenue through which data flows to or from the system. |
| Channel Address Word - | A word in preferential storage address 72 which contains the storage protection key and storage location of the Channel Command Word. |
| Channel Command Word - | A word located in Storage that specifies to the channel the I/O command to be executed. |
| Channel Status Word - | A word in preferential storage address 64 which provides the status of an I/O device or the conditions under which the I/O operation has been terminated. |
| Character - | Vary in bit length between four and eight bits depending on source and use. |
| Character Vector Generator - | An Adapter, (GFE), which interfaces the PVD and is contained in the DG. |
| CLU - | Abbreviation for Common Logic Unit; major portion of IOCE. |
| CM - | Abbreviation for Configuration Mask. |
| Command - | The first byte of the CCW as decoded by the channel and the I/O unit to specify the I/O operation to be executed. |
| Common Logic Unit - | The registers, latches, storage and controls which make up the heart of each IOCE. |

Computing Element –    The processor of the 9020 system which maintains system control and performs arithmetic and logic operations.

Configuration Control –    A hardware and program controlled system which defines system and subsystem communication paths and protects the operational system from malfunctioning system components assigned to a maintenance subsystem.

Configuration Console –    A unit in the 9020E which provides a central monitoring and control position for the system. Reconfiguration and error reporting paths for the IBM DAU's, DG's and RKM's are provided by duplexed Reconfiguration Control Units contained in the CC. The CC also interfaces the SMMC for error reporting.

Configuration Control Register –    A register in each system element and control unit, except the 2821 SC, and 2701 which controls communication between system components.

Configuration Mask –    The data used by the configuration control registers.

Console –    An aggregation of indicators and controls.

Control Panel –    Used interchangeably with Console. See Console.

CSW –    Abbreviation for Channel Status Word.

CTC –    Channel to Channel adapter.

CVG –    Abbreviation for Character Vector Generator.

DAR –    Abbreviation for Diagnose Accessible Register.

DARM –    Abbreviation for Diagnose Accessible Register Mask.

DASF –    Abbreviation for Direct Access Storage Facility

Data Keys –    These keys operate in conjunction with other keys and are used to provide data for subsequent storage or as a beginning address of a loop operation.

Data Interleave Mode –    A byte mode of input/output operation which is now referred to as Multiplex Mode.

DAU –    Abbreviation for Data Adapter Unit 2701.

DBI –    Abbreviation for Data Bus In

DBO –    Abbreviation for Data Bus Out

| | |
|---|---|
| DCP - | Abbreviation for the Display Channel Processor portion of NAS. |
| DE - | Abbreviation for Display Element. |
| DESAR - | Display Element Storage Address Register. |
| DESDR - | Display Element Storage Data Register. |
| Destination - | An addressed device or storage location |
| Device - | A system component, usually an input-output device; includes Tape Units. |
| DG - | Abbreviation for Display Generator. |
| DGAR - | Display Generator Address Register in the Display Element. |
| DGDR - | Display Generator Data Register in the Display Element. |
| Diagnose - | An instruction used primarily by maintenance programs to perform functions with parts of elements not possible with any other computer instruction. |
| Display Generator - | A non-IBM unit used to drive displays. |
| Diagnose Accessible Register - | A register in the CE used in conjunction with the External Old PSW to indicate source of some external interruptions; can be read only with the Diagnose instruction. |
| Diagnostic Monitor - | A supervisor program which controls the operation of diagnostic programs. |
| Diagnostic Program - | A program written to determine the malfunctioning parts of a system component. |
| Digit - | A group of four (4) bits; usually two digits to a byte. |
| Direct Access Storage Facility - | A large capacity, high speed, direct access storage consisting of a Storage Control Unit (SCU) and one or more Disk Storage Units (DSU). |
| Disk Storage Unit - | The unit which houses one (2312) or two (2318) Disk Packs (2316). The DSU attaches to the Storage Control Unit (2314). |
| Display Element - | An Element which interfaces the CE for display update and DG's for display regeneration. |
| DRG - | Abbreviation for Data Receiving Group. |

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| | |
|---|---|
| DSU - | Abbreviation for Disk Storage Unit. |
| Duplex System - | Configuration containing two CE's. |
| ELC - | Abbreviation for Element Check. |
| Element - | Major system components which also contain battery back-up; CE's, IOCE's, DE's, and SE's. |
| Element Check - | An equipment malfunction detected by an element or unit and indicated to a CE; detectable through the external interrupt system. |
| Element Control Panel - | Controls and indicators located on a panel at each element and unit frame. |
| Element MPO Pull - | Abbreviation for Element Master Power Off. |
| Element Master Power Off Pull - | A pull-type switch, which turns power off on each of the system elements and each PAM and TCU where it is located, and which is operative in any state. |
| Element Numbering - | Numbering scheme used to define physical location and order of expansion for main wall elements. |
| Element Reset- | Reset of an element or unit's registers and controls to an initial state. |
| Emergency Pull - | A pull switch located in the upper right-hand corner of the System Console and Configuration Console which is to be used in an emergency and which will turn off power to all system components. |
| Enable - | A pushbutton which allows an affiliated switch action to take place. |
| EOM - | Abbreviation for End of Message. |
| EPO - | Abbreviation for Emergency Power Off. |
| External Cables - | Protected covered cables used to interconnect normally separated elements, units or devices. External cables are routed under the floor. |
| External Interrupt Register - | External interruptions are stored either in the PSW, DAR or in the PIR; either may be considered external interruption registers. |
| Fault Locating Tests - | A fixed set of diagnostic or status tests used for isolation of equipment malfunctions in the CE's and IOCE's. |

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| | |
|---|---|
| Fetch - | The action whereby data is retrieved from storage. |
| FLT - | Abbreviation for Fault Locating Tests. |
| Frame - | The mechanical housing for the electronic mechanical and power equipment which constitutes each system element, unit and device. |
| GPI - | Abbreviation for General Purpose Input Adapter. |
| GPO - | Abbreviation for General Purpose Output Adapter. |
| High Order Bits - | Most significant bits of word, byte, or group of bits. |
| IA - | Abbreviation for Instruction Address. |
| IAR - | Abbreviation for Instruction Address Register. |
| IC - | Abbreviation for Instruction Counter. |
| IDES - | Inhibit DE Stop Bit. Absence of this bit will cause DE to stop on any DE error. |
| ILC - | Abbreviation for Instruction Length Code. |
| ILOS - | Abbreviation for Inhibit Logout Stop. |
| Indicator - | A visual indicator on a panel or console; also referred to as lamp or neon. |
| Input/Output Control Element - | The system component which provides the control for all system input/output operations and does processing under control of the CE. |
| Instruction - | An instruction is fetched from storage by a CE or IOCE and is executed by that CE or IOCE to perform a useful function. |
| Interface - | The matching of signal, data and control lines between system components. |
| Interlock - | A hardware control which requires another action to be performed for certain manual controls to make them effective. |
| Interruption - | The stopping of processing in a CE or IOCE. (See 9020 System Principles of Operation Manual and 9020D and 9020E System.) |
| INTI - | Abbreviation for Interfacility Input Adapter. |
| INTO - | Abbreviation for Interfacility Output Adapter. |

| | |
|---|---|
| IOCE - | Abbreviation for Input/Ouput Control Element. |
| IOCESAB - | IOCE Storage Address Bus in the SE. |
| IOCESBO - | IOCE Storage Bus Out in the SE. |
| IOCE Processor - | An IOCE that is processing instructions under control of a CE. |
| IPL - | Abbreviation for Initial Program Load. |
| ISK - | Abbreviation for Insert Storage Key. |
| Keys - | Hardware toggle switches, or storage Protect Codes. |
| Lamp - | Used interchangeably with Indicator. See Indicator. |
| Lamp Test - | A static test of indicators on a console with exceptions noted for each panel. |
| LAR - | Abbreviation for Local Store Address Register |
| Latch - | A hardware device which is capable of retaining a bit of information. |
| Load - | A pushbutton located on some system elements and the System Console and the Configuration Console to start the initial program loading sequence. |
| Load Unit - | Rotary switches on some system elements and, the System Console which are used to select an input/output device for the initial program loading process. |
| Local Storage - | A group of internal registers within a CE or IOCE used for instruction execution purposes. |
| Logic - | The circuits provided in an element which make decisions concerning the data provided to them. |
| Logic Check - | The determination that the logic is not performing in a correct manner; usually associated with incorrect parity of data. |
| Logout - | The storing of registers and latches from an element in selected locations of main storage. |
| Logwords - | Words contained in a Logout (32 bits). |
| Low Order Bits - | Least significant bits of word, byte or group of bits. |

LRC –                       Abbreviation for Longitudinal Redundancy Check.

LS –                        Abbreviation for Local Storage.

LSAR –                      Abbreviation for Local Storage Address Register
                            (IOCE).

LSB –                       Abbreviation for least significant bit.

LSFR –                      Abbreviation for Local Storage Function Register.

LSWR –                      Abbreviation for Local Storage Work Register.

MACH –                      Abbreviation for Maintenance and Channel Storage

Machine Cycle –             The time required to perform one micro-instruction.

Main Storage Select–        A rotary switch on the System Console, Configura-
                            tion Console and CE used to select a main (not
                            a Local) Storage element for initial program
                            loading purposes, FLT loading and store/display
                            operations.

Main Wall Section –         Joins CE and SE/DE elements into a contiguous
                            wall.  Contains inter-frame cabling and power
                            components.

Main Wall Spacer            Used between two SE's or DE's when not separated
Frame –                     by a CE.  Inter-frame cabling is routed through
                            this frame.

Maintenance and             Storage in the IOCE used for Channel UCW's,
Channel Storage –           IOCE Processor and maintenance operations.

Maintenance                 Controls located on all system components for
Controls –                  use by engineers responsible for maintaining
                            individual or subsystem components.

Marginal Condition –        A marginal condition may be caused by an Out
                            of Tolerance Check or On Battery Signal.

MC –                        Abbreviation for Machine Checks or Marginal
                            Check.

MCW –                       Abbreviation for Maintenance Control Word.

Micro-instruction           The commands which are stored in Read Only
or Micro-order –            Storage which control CE's and IOCE's actions.

Mode of Operation –         Indicators which display in alphanumeric
                            characters the operational system status on
                            the system console.

Module –                    A circuit package; part of the SLT technology.

Monitor –               The act of watching the display of information
                        through indicators and the manipulation of
                        operational controls.

MPLX –                  Abbreviation for Multiplexor.

MPDA –                  Abbreviation for Modified Parallel Data Adapter.

MPO –                   Abbreviation for Master Power Off.  See Element
                        Master Power Off.

MSB –                   Abbreviation for most significant bit.

MTU –                   Magnetic Tape Unit 2401-2/3.

Multiplex Mode –        The normal mode of operation for slow speed
                        devices which allows handling of single bytes
                        or multiple bytes whenever necessary.

Multiplexor Channel–    A channel in the IOCE which operates in the
                        multiplex mode.

NAS –                   Abbreviation for National Airspace System.

NBP –                   Abbreviation for Normal Bit Period.

OBS –                   Abbreviation for On Battery Signal.

On Battery Signal –     An indication from an element that it has lost
                        main line or standby power and is obtaining power
                        from its battery system.

Operator Controls –     Controls on the System Console, Configuration
                        Console and CE's which an operator may use to
                        affect a CE and the system operation.

Order –                 Orders are used to specify functions peculiar to
                        a device, such as rewinding tape, or spacing of
                        a printer.

OTC –                   Abbreviation for Out of Tolerance Check.

Out of Tolerance        An indication by temperature sensing circuits
Check –                 that there has been an increase in internal
                        temperature within approximately 10 degrees
                        of the thermal shut-down temperature.

PAM –                   Abbreviation for Peripheral Adapter Module.

Panel –                 An aggregation of indicator and controls; used
                        interchangeably with console.

PCI –                   Abbreviation for Program Controlled Interruption.

PDA –                   Parallel Data Adapter in the DAU.

PDU -                    Abbreviation for Power Distribution Unit.

Peripheral Adapter       A unit in the 9020 System for interfacing with
Module -                 various input/output devices.  PAM provides the
                         control for automatic sequential polling and
                         servicing for input/output devices.

PIR -                    Abbreviation for Processor Interrupt Register.

Power Check -            A power supply malfunction which results in an
                         indicator display on the system component where
                         the fault is located and on the System Console
                         under the appropriate component indication.

Power Controls -         Controls which allow the various power functions
                         to be performed.

Power Control            A panel located on most system components which
Panel -                  contains each component's power control switches
                         and indicators.

Power Distribution       Referred to as a power compartment; located
Unit -                   within each system element and unit and some
                         devices and contains the power supplies and
                         power distribution equipment.

Power On/Off -           A toggle type switch which is used, except when
                         interlocked, to turn power on or off on a system
                         component.

Power On/Off             A Power on/off switch located in the power
Remote Switch -          distribution unit.  It can be used in place
                         of the power on/off switch.

Power Sequence           When a system component has successfully se-
Complete -               quenced all its voltages to the operational
                         level, the power sequence complete indicator
                         is turned on.

Power Wall Frame -       Contains Power Circuitry for a related element.
                         Inter-frame cabling is routed through this
                         Frame.  This frame is part of main wall section.

Preferential Storage     Address in storage which contains the first byte
Base Address -           of the preferential storage area.

Preferential Storage     A hardware register in the CE which contains the
Address Register -       PSBA.

Primary Interface -      The path established between a like numbered
                         PAM and IOCE through which the maximum number
                         of devices attached to the PAM may be addressed.

Processor Interrupt      A 3-bit register in each CE to preserve external
Register -               interrupts from IOCE Processors.

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|---|---|
| Program Status Word - | Contains information that is required for proper program execution. |
| PSA - | Abbreviation for Preferential Storage Area. |
| PSBA - | Abbreviation for Preferential Storage Base Address. |
| PSBAR - | Abbreviation for Preferential Storage Base Address Register. |
| PSW - | Abbreviation for Program Status Word. |
| PVD - | Plan View Display. |
| QUAD System - | Configuration with four CE's. |
| Rate - | A switch which allows a CE or IOCE to process instructions at normal processing speed or an instruction at a time. |
| R/Console - | The enroute controller's console. |
| RCU - | Reconfiguration Control Unit portion of the CC. |
| Read Only Storage - | A capacitor type storage which is utilized in the CE and IOCE to hold the microinstructions necessary to control the element's operations. |
| Refetch - | When a piece of data is fetched and an error indication is noted by the checking circuits, another fetch, a refetch, can occur. |
| RKM - | Radar Keyboard Multiplexor. |
| RKM/R-Console - | RKM to R-Console Configuration Switch. |
| ROAR - | Abbreviation for Read-Only Address Register. |
| ROS - | Abbreviation for Read Only Storage. |
| ROS Address Stop - | Causes the CE or IOCE to stop when the specified microinstruction address is selected. |
| ROSDR - | Abbreviation for Read-Only Storage Data Register. |
| ROS Repeat - | A repeat of a selected microinstruction. |
| Running State - | The normal machine state for processing instructions, referred to as the processing state and/or the program or supervisor state. |
| RVDP - | Abbreviation for Radar Video Data Processor Adapter. |

SAB -                      Storage Address Bus.

SABR -                     Storage Address Buffer Register.

SAR -                      Abbreviation for Storage Address Register.

SC -                       Abbreviation for System Console.

SCI -                      Storage Control Interface.

Scan In -                  The filling of registers and triggers in an
                           element with the selected contents of
                           storage via special paths.

SCON -                     Abbreviation for the Set Configuration Instruc-
                           tion and Set Configuration function.

SCU -                      Abbreviation for Storage Control Unit.

SDBI -                     Storage Data Bus In

SDBO -                     Storage Data Bus Out.

SDC -                      Abbreviation for Station Directing Code.

SDR -                      Abbreviation for Storage Data Register.

SE -                       Abbreviation for Storage Element.

Secondary Interface -      The alternate path for a PAM-IOCE interface
                           through which an IOCE may address only part
                           (half-secondary) or all (full secondary) of
                           the PAM's attached devices.

Selection Mask -           The data that is used by the Configuration
                           Control equipment to address the Configuration
                           Control registers that are to be changed.

Selective Reset -          A reset signal sent to a selected adapter from
                           an IOCE as a result of an error detected on the
                           I/O interface.

Selector Channel -         A high speed channel which operates only in the
                           burst mode.

Sense Switch -             A switch (one of a set) located on the System
                           Console and Configuration Console which can
                           be used as a single or combination bit input.

SESAR -                    Abbreviation for Storage Element Storage
                           Address Register.

SESDR -                    Abbreviation for Storage Element Storage Data
                           Register.

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Set Configuration - An instruction which assigns communication paths between elements and units.

SM - Abbreviation for System Mask.

SMMC - System Maintenance Monitor Console.

SOBR - Storage Output Buffer Register.

SOM - Abbreviation for Start of Message.

SPAR - Storage Protect Address Register.

SPB - Abbreviation for Storage Protect Buffer.

SPCR - Abbreviation for Storage Protect Compare Register.

SPDR - Abbreviation for Storage Protect Data Register.

SPIKR - Storage Protect In Key Register.

SPOKR - Storage Protect Out Key Register.

SR - Abbreviation for Select Register.

SSK - Abbreviation for Set Storage Key.

Standby Power - A standby power system for main line power supplied by the customer.

STAT - Abbreviation for a hardware testable condition.

Start - In conjunction with the Rate switch, this pushbutton takes a CE or IOCE out of the Stopped State.

State - Used to define the state of a CE, stopped or wait, or the state or status of the operational system.

State One - An interpretation of the state bits in the Configuration Control Register; a state in which SCON may not be issued by a CE; some maintenance controls are operative.

State Three - An interpretation of the state bits in the Configuration Control Register: A state in which SCON may be issued by a CE; no manual controls normally operative in this state.

State Two - An interpretation of the state bits in the Configuration Control Register; a state in which SCON may not be issued by a CE; no manual controls normally operative in this state.

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| State Zero - | An interpretation of the state bits in the Configuration Control Register; a state in which the Test Switch is operative and, therefore, all manual controls may be used. |
| Status - | The various states of all system components automatically displayed on the System Console and Configuration Console. |
| Status Byte - | A portion of the information supplied by a channel or I/O unit as a result of an I/O operation. |
| Stop - | The placing of a CE or IOCE in the Stopped State without destroying control or register data. |
| Stopped State - | A machine condition where no instructions are executed, no interrupts accepted and the timer is not updated. Certain manual controls are operative only in this machine state. |
| Storage - | Either main or local storage registers which are used for storing data or programs. Read Only Storage holds microinstructions only. |
| Storage Control Unit - | The system unit which controls the operation of Disk Storage Units (2312, 2318). Each SCU may be selected through one of two IOCEs. |
| Storage Cycle - | The time required to read a word from and regenerate the word into main or local storage; and the time to read a word from ROS. |
| Storage Element - | The main storage element of the 9020D/E System which contains 131K words of addressable storage. |
| Storage Key - | Four bits placed in the storage protect buffer which is specified by the program and which protects a block of 2048 bytes. |
| Storage Protection - | The protection of selected parts of an SE, accomplished through programming and hardware means, to prevent destroying important data. |
| Storage Protect Buffer - | A 64-word storage which is used to hold the Storage Protection keys. |
| Storage Protect Key- | Used interchangeably with Storage Key. |
| Storage Select - | The two position switch which allows the addressing of main or local storage. |
| Storage Test - | A switch on IOCE's which allows hardware testing of the element's internal storage. |

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| Store - | To replace the contents of an addressable storage location. |
| SU - | Switch Unit. |
| Switchable Indicators - | Indicators on the CE and IOCE control panels which can be manually switched to one of several different positions in which different registers or functions are displayed. |
| System Components - | Element - CE's, IOCE's, DE's, and SE's; Units - PAM's, Tape Control Units, 2821 Control Unit, 2701 Data Adapter Unit, 2314 Storage Control Unit, System Console, Configuration Console; Devices - Tape Units, 1052's. Printer, Card Reader Punch, and other I/O devices. |
| System Console - | The main system monitor and control location. |
| System Control - | The function of controlling system components through programming and manual operations using configuration control, element checking and the Executive Control Program. |
| System Interlock - | A key-operated switch which, when in the normally "off" position, prevents certain manual controls from being operative which might jeopardize system operation. |
| System Reset - | A signal which resets system components to their initial state. |
| TCU - | Abbreviation for Tape Control Unit. |
| Tape Control Unit - | The system unit which controls the operation of up to eight tape units. Each tape control unit may be selected through one of two IOCE's only. |
| Thermal Condition - | Over temperature condition for a system element or unit. |
| TPS - | Abbreviation for Two Processor Switch. |
| Triplex System - | Configuration containing three CE's. |
| TU - | Abbreviation for Tape Unit. |
| UCW - | Abbreviation for Unit Control Word. |
| Unit - | System components which operate mainly as I/O device control units; PAM's, DAU's, SCU's, Tape Control Units, 2821 (Printer, Card Reader/Punch) Control Unit. Also the System Console and Configuration Console is classified as a Unit. |

Unit Control Word — An aggregation of information about a device and control unit which is maintained and used by the multiplexor channel in an IOCE: not available to the programmer.

VFL — Abbreviation for Variable Field Length.

Wait State — A machine state where instructions are not executed, unmasked interruptions are accepted and the timer is updated.

XIC — Transmission Interface Converter.

9020D — IBM System for the Central Computer Complex.

9020E — IBM System for the Display Channel Processor.