IBM Customer Engineering

Instruction-Reference

7909 Data Channel

IBM

Instruction-Reference

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Preface

This Instruction-Reference manual covers internal operations and maintenance of the IBM 7909 Data Channel as attached to IBM 7090/7094 Data Processing Systems.

Operations are not followed into the various adapters because the I-O interface is thoroughly explained in an initial section. Therefore, all explanations are with respect to the channel side of the interface. Specific information on the various devices may be obtained from the following publications:

IBM 7631 File Control CE-IR Manual, Form R23-2541-2

IBM 1301 Disk Storage CE Manual of Instruction, Form 227-5582

IBM 1301 Model 1 and Model 2 Disk Storage and IBM 1302 Model 1 and Model 2 Disk Storage with IBM 7090, 7094, and 7094-2 Data Processing Systems, Form A22-6785

IBM 7320 Drum Storage, Form A22-6747

IBM 7340 Hypertape Drive Model I, Form A22-6746

IBM 7340 Hypertape Drive Reference Manual, Form A22-6616

IBM 1414-Model 3, 4, 5, 6, 8 CE-IR Manual, Form R23-2590

IBM 1414-6 I-O Synchronizer CE-IR Manual, Form R23-9914

IBM 1414-6 Input-Output Synchronizer (7090/7094 Systems Bulletin), Form G22-6625

IBM 7750 Program Transmission Control 1410, 7000 CE Manual of Instruction, Form 223-2540

To satisfy the varied preferences of customer engineers using this manual, three types of figures are used: condensed logic, sequence charts, and flow charts. The condensed logic charts are as near to actual systems as possible with lines converted to positive-type logic. In maintaining this positive logic, in-phase outputs are used to indicate an active (conditions met) state from the condensed logic blocks. This is contrary to the S level NOR circuitry because NOR always produces a change in level between input and output. However, the condensed logic does not deal with plus (+) or minus (−) levels (only pure logic). Clearly labeled out-of-phase outputs are also used in some cases to simplify the figures by eliminating the cluttering effect of inverter blocks.

The material in this manual has been written to engineering change level 252610. Future engineering changes, however, may change the logic and machine operation from that presented in this manual.

For simplicity, the prefix 50 has been omitted from Systems numbers in flow charts, logic diagrams, and sequence charts.

Material contained in the Customer Engineering Instruction-Reference Manual Supplement *IBM 7909 Data Channel,* Form R23-2571 is included in this manual.

In this manual simplex I-O interface is the same as standard interface and simplex BCD translation is the same as standard BCD translation.

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Contents

Illustrations

The IBM 7909 Data Channel is a stored program device designed to increase the capabilities of the IBM 7090/7094 Data Processing Systems. It attaches to the IBM 7606 Multiplexor in the same manner as the IBM 7607 Data Channel, and controls data flow between core storage and a variety of input-output devices. Communication and data flow between the channel and I-O adapter are through a simplex I-O interface.

The many commands at its disposal give the 7909 Data Channel powerful capabilities for performing logic and testing operations in addition to the normal control of data transmission.

An automatic interrupt feature extends the computer trap concept to the channel and, therefore, gives the channel an ability to monitor continually and independently specific conditions either from within itself or from the I-O adapter.

The IBM 7302 Core Storage acts as a common storage medium for both the computer instructions and channel commands. Access to core storage to obtain these commands or transmit data is on a shared-time basis with the computer program.

To eliminate confusion and establish terminology, note the following:

Instructions are executed by the computer.

Commands are executed by the channel.

Orders are executed by the I-O adapter.

The computer is required to initiate a channel operation. Once started, however, the channel makes the necessary requests for storage cycles and executes its own program of testing, transferring, or transmitting data completely independent of the main computer. If previously enabled for control word traps, the channel has the ability to interrupt the computer program; thus, communications are available between the channel and computer at all times.

Optional features add flexibility to the channel's operation. The IBM 7909 Data Channel Switch Optional Feature permits attachment of one or two input-output control units to one 7909 Data Channel. The IBM 7909 Data Channel BCD Translation Optional Feature provides automatic BCD translation of information transmitted between an I-O adapter and the 7909 Data Channel. The IBM 7909 Data Channel Read Backward Optional Feature facilitates processing data received from a recorded tape being read in a backward direction. Characters are assembled in reverse order and stored in descending core storage locations.

7909 Attachments

A variety of input-output devices and appropriate adapters can be attached to a 7909 oriented system.

The IBM 7631 File Control with the IBM 1301 Disk Storage provides a capacity of more than 55 million characters of storage for each disk storage unit.

The IBM 7320 Drum Storage and IBM 7631 File Control with drum attachment feature bridge the gap between a high-speed, limited capacity core storage and slower, large capacity random-access disks and magnetic tape. The capacity of the 7320 is 1.12 million six-bit characters and the character rate is 202.8 KC.

The IBM 7640 Hypertape Control with the IBM 7340 Hypertape Drive introduces a new concept in magnetic tape devices. Character rates can be as high as 170,000 alphameric characters (28,330 words) per second.

The IBM 1414-6 Input-Output Synchronizer permits the attachment of communication-oriented and paper tape devices such as:

IBM 1009 Data Transmission Unit
IBM 1011 Paper Tape Reader
IBM 1014 Remote Inquiry Units
Telegraphic Input-Output Units

Figure 1 shows a 7090/7094 system with attached devices.

Maximum System Considerations

A maximum combination of eight 7607 and 7909 Data Channels may be attached to a 7090 or 7094 system. Individual channel character rates and physical limitation (cable lengths), however, may reduce this to less than eight.

A weight table has been prepared (Figure 2) as a guide to the system planner in determining the maximum possible 7090 or 7094 system configuration. The following are assumed:

1. 7909 Data Channel timings are assigned in accordance with the table under "7909 Data Channel timings."
2. No one channel will require more than three consecutive storage cycles.
3. Channel priority is assigned with the greatest weights on the highest priority channels.

The maximum operable system is then defined as that system where the sum of the weights of attached

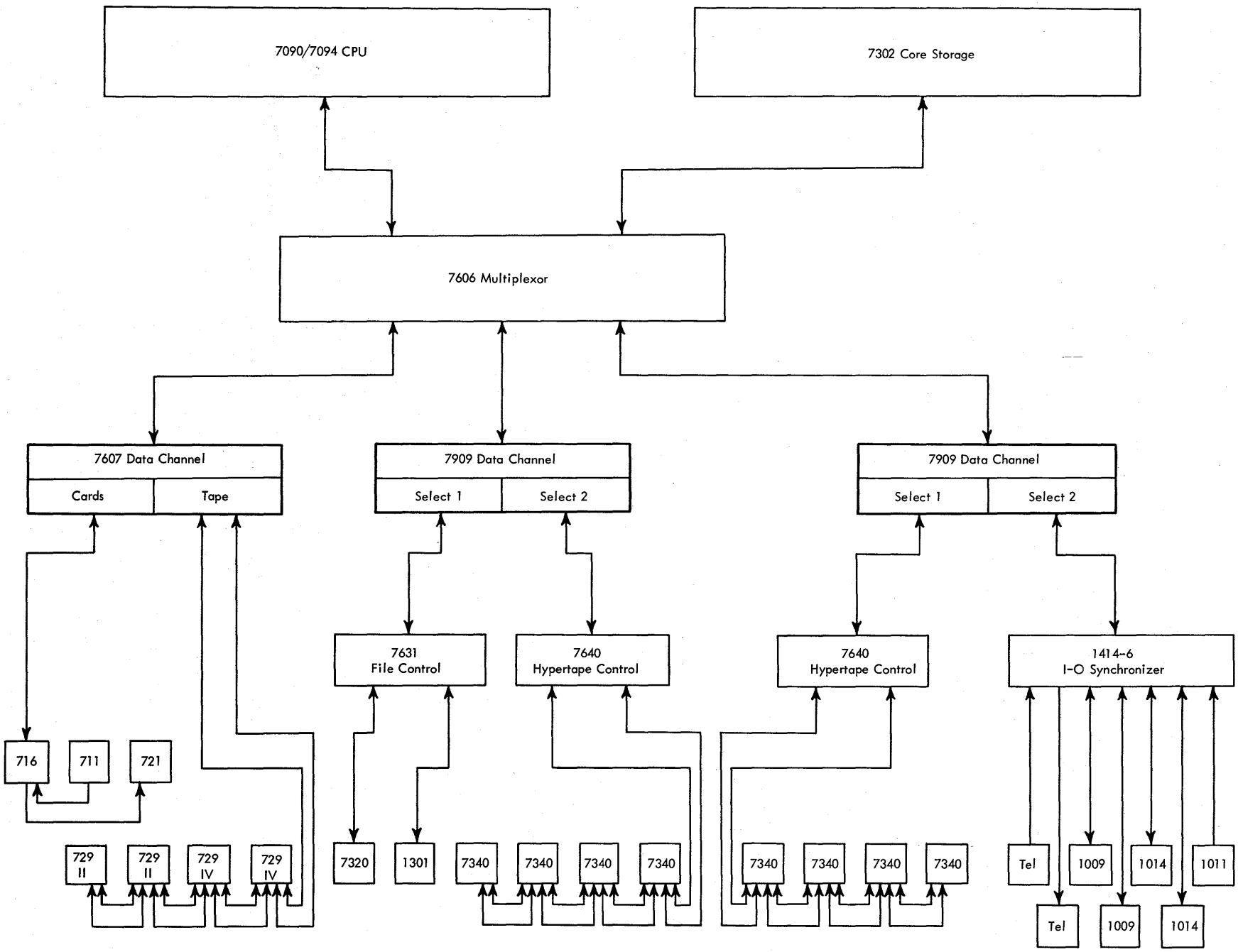


Figure 1. 7090/7094 Channel Configuration

Data Channel	Attached Device	Nominal Character Rate	Weight/Channel 7090	Weight/Channel 7094
7607 Mod 1,2,3,4	729 II/V at 200 BPI	15 KC	2.1	1.9
	729 IV/VI at 200 BPI	22.5 KC	3.2	2.8
	729 II/V at 556 BPI	41.7 KC	6.2	5.2
	729 V at 800 BPI	60 KC	9.4	7.6
	729 IV/VI at 556 BPI	62.5 KC	9.9	7.9
	729 VI at 800 BPI	90 KC	15.6	11.7
7909	7750 Programmed Transmission Control	71.5 KC	9.4	7.6
	1301 Disk Storage	90 KC	12.4	9.6
	1414 VI I-O Synchronizer	91 KC	12.0	9.7
	7340 Hypertape Drive	170 KC	37.2	23.0
	7320 Drum Storage	202.8	42.9	24.4

Note: If a channel has devices attached with two different weights, the highest weight of the two will be assigned for the channel.

Figure 2. System Weight Table

devices is less than or equal to 100. If assumption 3 cannot be satisfied, the sum of the weight must be less than or equal to 70. Operation cannot be guaranteed on a system that does not meet this criteria.

7909 Data Channel Timings

7909 Data Channel timings are determined by installation of an appropriate SMS card assembly in card location 05A3D21. These timings are dependent upon total systems weight as explained in the preceding section and must be assigned in accordance with the following table. These timings affect the execution of all 7909 operations except data transmission under COPY control. The time required to transmit one word under a transmit command (two storage cycles) is given as information for each timing.

Total Systems Weight From	To	Capcut	Average Time to Transmit One Word
0	15	9	13.1 μs
16	45	10	74.2 μs
46	75	11	96.0 μs
76	81	12	122.2 μs
82	89	13	152.7 μs
90	100	14	183.3 μs

7909 Timing Assignments

Physical Description

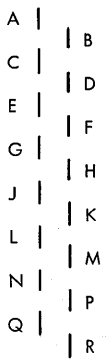
The 7909 Data Channel (Figures 3, 4, 5, and 6) is a rack and panel module containing four SMS panels. Each panel contains ten rows of 28 SMS card sockets. From the wiring side, the panels are designated 1-4, left to right, top to bottom. I-O connector rows are located below the two lower panels and designated row U (upper) and row L (lower).

A CE test panel is hinged to the upper right front section of the module and can be easily swung out of the way when scoping points on panel 2.

Hinged to the center post in the back of the module is a self-contained power supply capable of producing the various voltages required within the logic panels. Power to the 7909 is supplied by the IBM 7618 Power Control through two cable connections at the lower left front section of the module. The upper cable supplies 60 cps power while the lower cable supplies 400 cps.

Logic Panel

The 10 x 28 panel (Figure 5) contains 280 SMS sockets forming a matrix 28 columns wide by 10 rows long. The columns are designated 01 through 28 (left to right), and the rows are designated A through K (top to bottom). Each SMS socket has 16 pins, A through R (excluding I and O), as follows:



Interpanel Connections

Several methods of interpanel connections are used on the 7909. Eight-pin Y and Z row connector blocks are mounted above and below each of the four panels. Connections between panels 1-3 and 2-4 are made by short push-on, solderless jumper wires which run from the Z row of the upper panel to the Y row of the panel below (Figure 5).

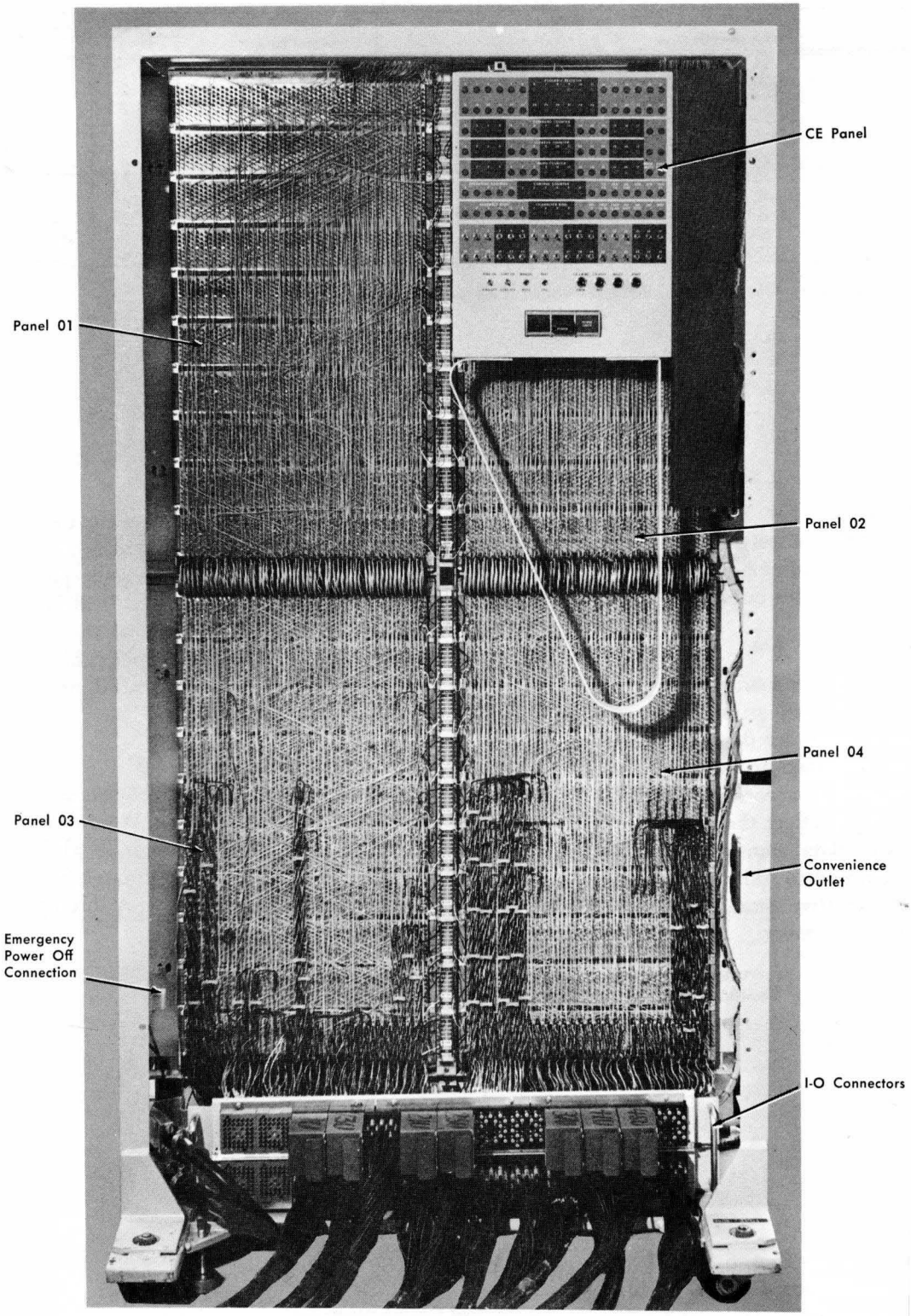


Figure 3. Physical Layout—Front View

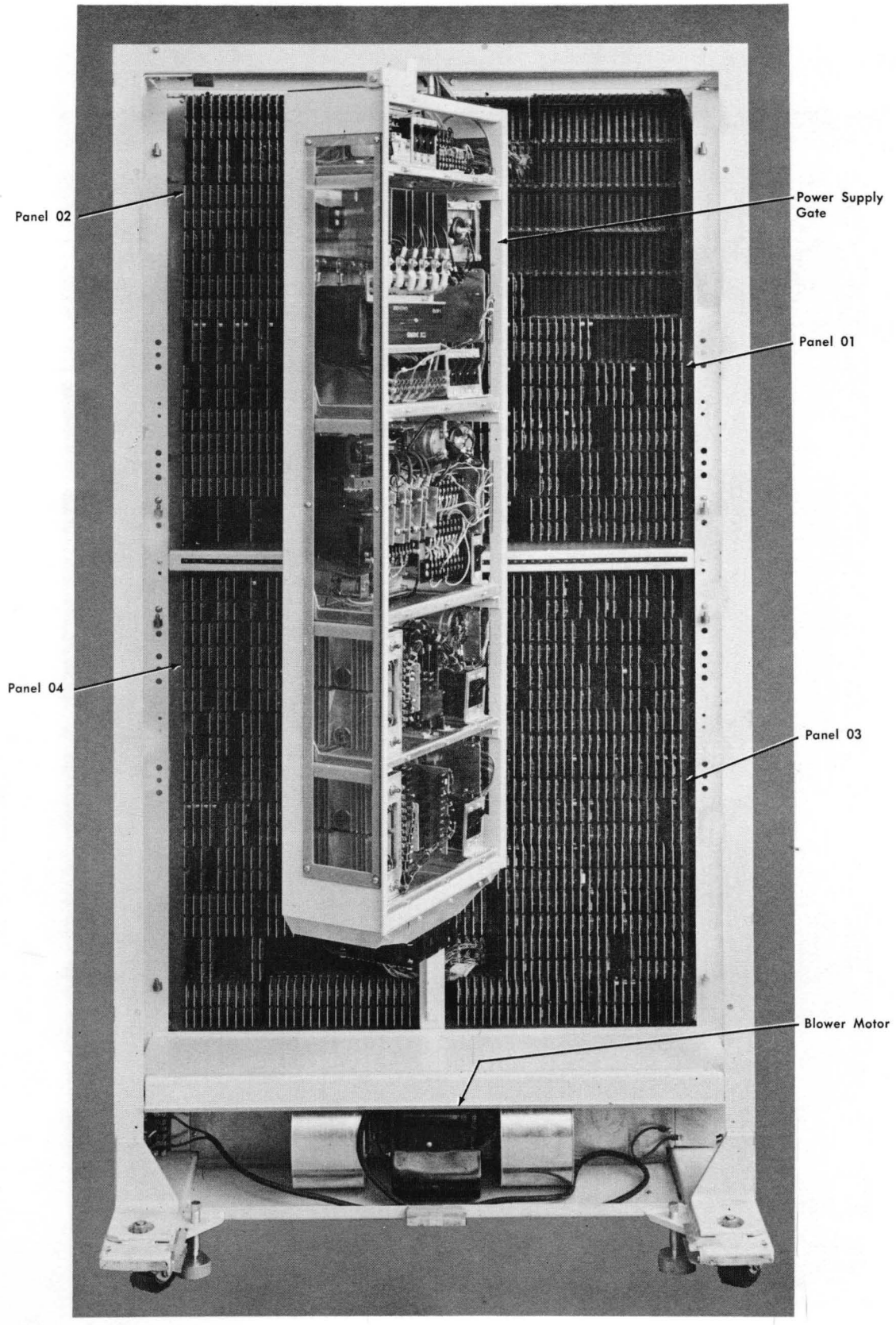


Figure 4. Physical Layout—Rear View

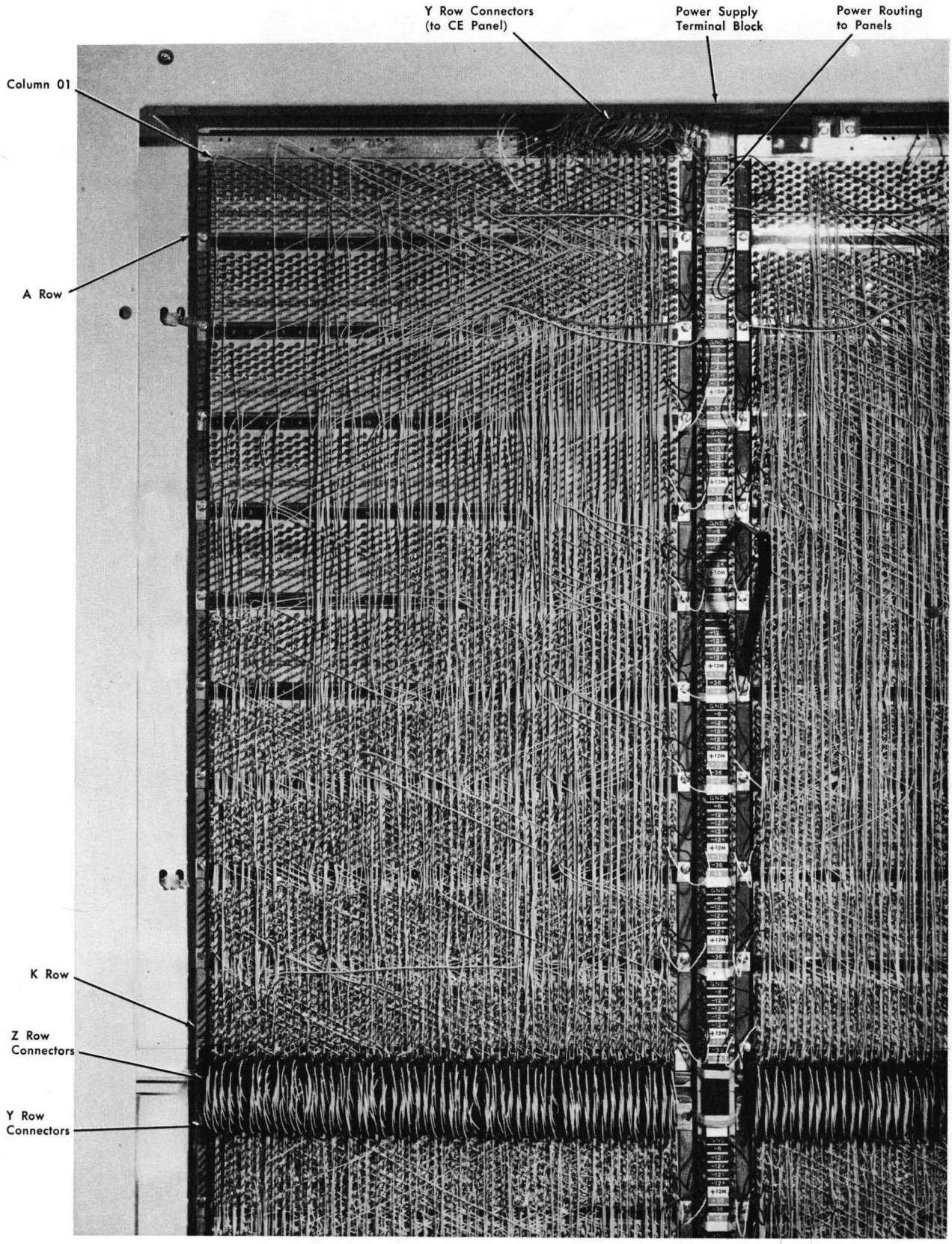


Figure 5. SMS Panel 01

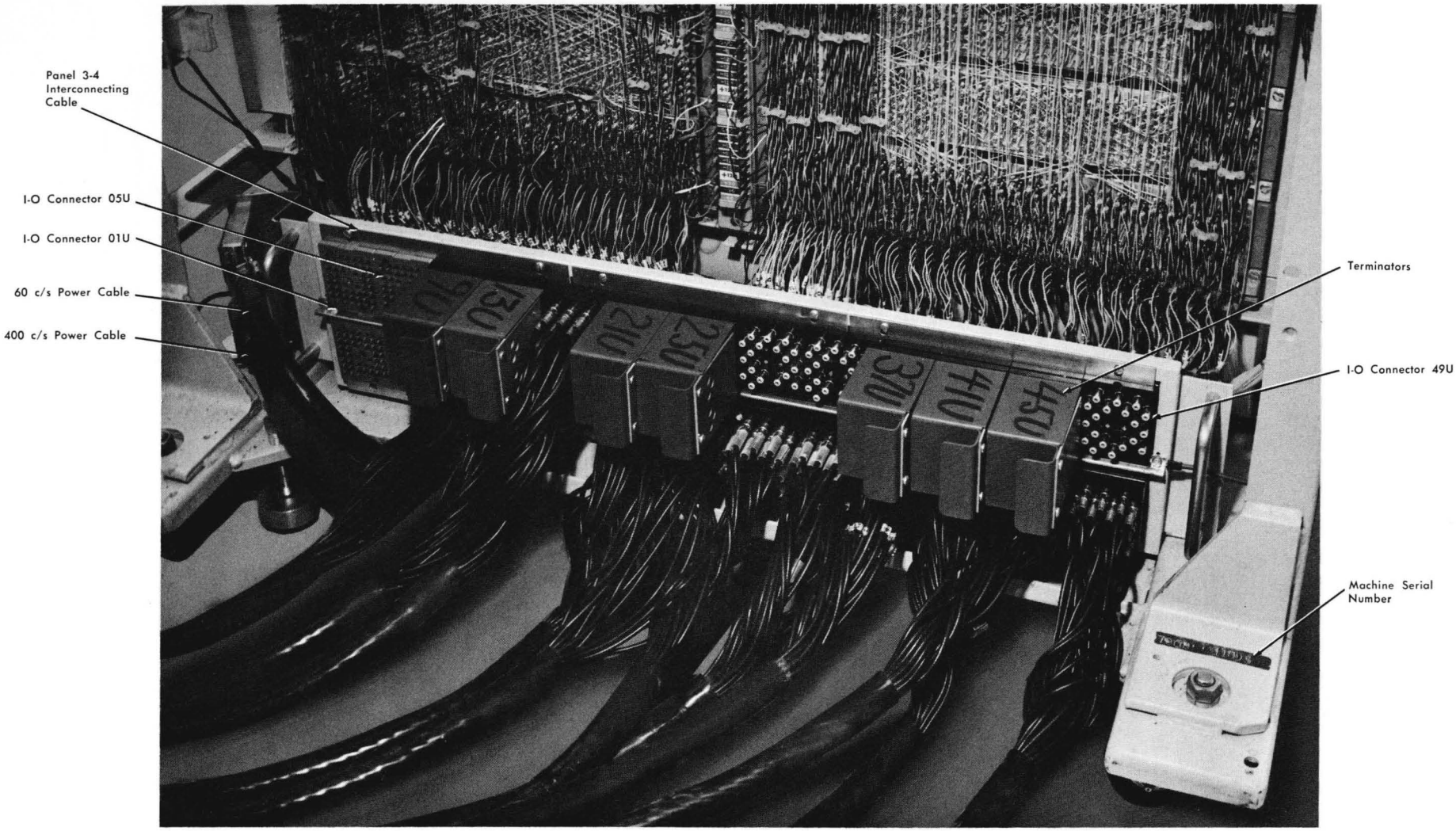


Figure 6. I-O Connectors

Connections between panels 3 and 4 are made by a short, laced jumper cable which runs between the Z connector blocks at the bottom of the module (Figure 6). Additional connections are made by means of paddle-terminated cables from positions J24-J28 of panel 3 to J01-J05 of panel 4.

Connections between panels 1 and 2 are made by paddle-terminated cables that are not visible from the wiring side of the machine. Positions B19-B28 of panel 1 connect to B01-B10 of panel 2. In addition, positions A27-A28 of panel 1 connect to positions A4-A5 of panel 2.

A partial set of Y connectors at the top of panels 1 and 2 provide connections to the hinged CE panel in the front of the machine.

Y and Z connector pins are labeled as follows:

```
A | 
  | B
C | 
  | D
E | 
  | F
G | 
  | H
```

Input-Output Connector Rows

I-O connector rows (Figure 6) for the module are located below the logic panels; the rows are designated row U (upper) and row L (lower), top to bottom. The 7909 uses 20- and 40-position biscuit connectors: 13 connectors per row numbered 01, 05, 09, 13 . . . 45, 49 from left to right as viewed from the wiring side of the machine. 7909 I-O connector Systems page designations are:

FRAME	MODULE	ROW	COLUMN	PIN
05	A	U or L	01-49	01-40

Examples: 05AU0130—Service Request
05AL0130—Service Response

Column position 01 upper and 01 lower (40-position connectors) connects interface 1; the upper connector receives signals from the adapter (read cable) while the lower connector sends signals to the adapter (write cable). Position 05 has a corresponding use for interface 2 when the data channel switch optional feature is installed.

The remaining eleven connectors (20-position connectors), positions 09-49, receive the necessary assignment cables from the 7606 multiplexor. These cables connect to the lower receptacles and are terminated, where necessary, by terminator boxes in the corresponding upper positions. If there are other channels on this bank, however, the eleven upper connectors act as a jumper point for the signal cables to the next channel in line.

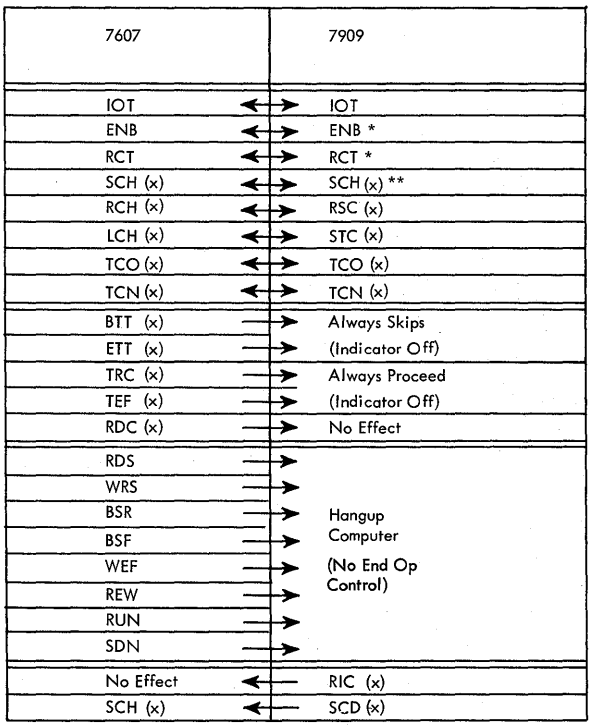
The twisted-pair wire connections receiving signals from the I-O cables are connected directly to the pins of panels 3 and 4.

7909-7607 Compatibility

The 7607 and 7909 Data Channels are not program compatible. A 7607 program presented to a 7909 will hang up the computer at the first select instruction (RDS, WRS, REW, BSR, and so on).

A 7909 program presented to a 7607 will cause an I-O check as soon as a channel operation is attempted. This results because a RCH (+0540) was not preceded by a select instruction.

A 7607 instruction, such as BTT, ETT, TRC, and TEF, which tests indicators in their execution, operates as though the indicator were always OFF. Select instructions receive no end operation signal from the 7909 and therefore cause the computer to hang up. Other instructions operate in an exact manner, have minor variations, or no effect whatsoever. Figure 7 shows computer instruction compatibility and Figure 8 shows a comparison of channel commands.



* Control word trap only available
** 7607 stores Location Cntr in decrement and Addr Cntr in address of location Y and saves op code and bit in 19.
7909 stores Cmmd Cntr in address and Addr Cntr in decrement of location Y (the 7909 does not store the operation register)

Figure 7. 7607-7909 Instruction Compatability

7607 Cmmd	7909 Command	
	WC $\geq 40{,}000_8$	WC $< 40{,}000_8$
IOCD	WTR	
IOCP	CPYP	
IORP	CTLW	CTL
IOCT	CPYD	
IORT	TWT	LAR
IOSP	TDC	X
IOST	X	SMS
IOCDN	XMT	
IOCPN	X	X
IORPN	SNS	CTLR
IOCTN	TCM	
IORTN	X	SAR
IOSPN	LCC	LIP
IOSTN	ICC	
TCH	TCH (IF 19 = 0)	LIPT (IF 19 = 1)

X = 7909 Hangup
No 7909 Commands will cause a hangup if loaded into a 7607

Figure 8. Channel Command Comparisons

Channel Priority

No two devices can use core storage during the same period of time. Therefore, with as many as eight individual channels and a computer sharing a common core storage, some method must be used to control these cycles without inter-conflict.

A priority system is used to provide this systematic dispensing of core storage cycles. Any channel having obtained priority has all of its immediate demands fulfilled before relinquishing priority to another channel. The immediate demands of all channels are satisfied before the computer can regain control and use core storage for its own purposes.

Priority System—Multi-Channel

Priority (Figure 9) is unnecessary with only one channel connected to the system; the computer allows B times as requested. The need for B cycles is determined by the commands and conditions within each individual channel and could occur simultaneously on two or all channels attached to the system. The order in which each channel is serviced is from "most remote" to "least remote."

Physical connections to the computer are made at the multiplexor as bank 1 and bank 2. The last channel on bank 2 is normally the most remote and the farthest channel on bank 1, the least remote. Actually, banks 1 and 2 play no logical part in the operation; the eight channels can be considered as one continuous series connection.

Note that a "B cycle required" generated by a channel causes a remote required signal to be propagated to the lower priority units. The effect of this line is to block lower priority servicing until the higher priority channels have their immediate needs completely satisfied. Channel H (Figure 9) has no remote required input signal and will be serviced first; channel A has no remote required output signal and will be serviced last. (Channel designations are independent of priority; those in Figure 9 are used as examples only.)

Internal Channel Priority Logic—B Time

Requests for B time (Figures 10 and 11) by the channel may be made immediately or, in other cases, delayed for a period of time. For simplicity, assume that the "demand delay" circuitry at the top of Figure 10 does not exist.

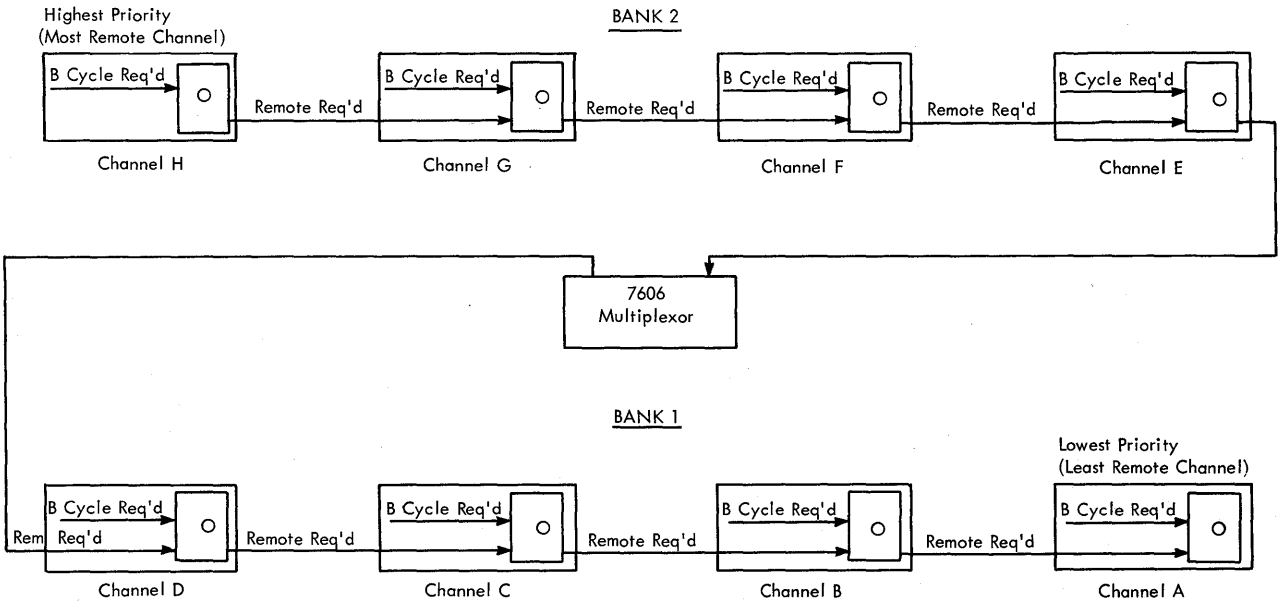


Figure 9. Inter-Channel Priority Connections

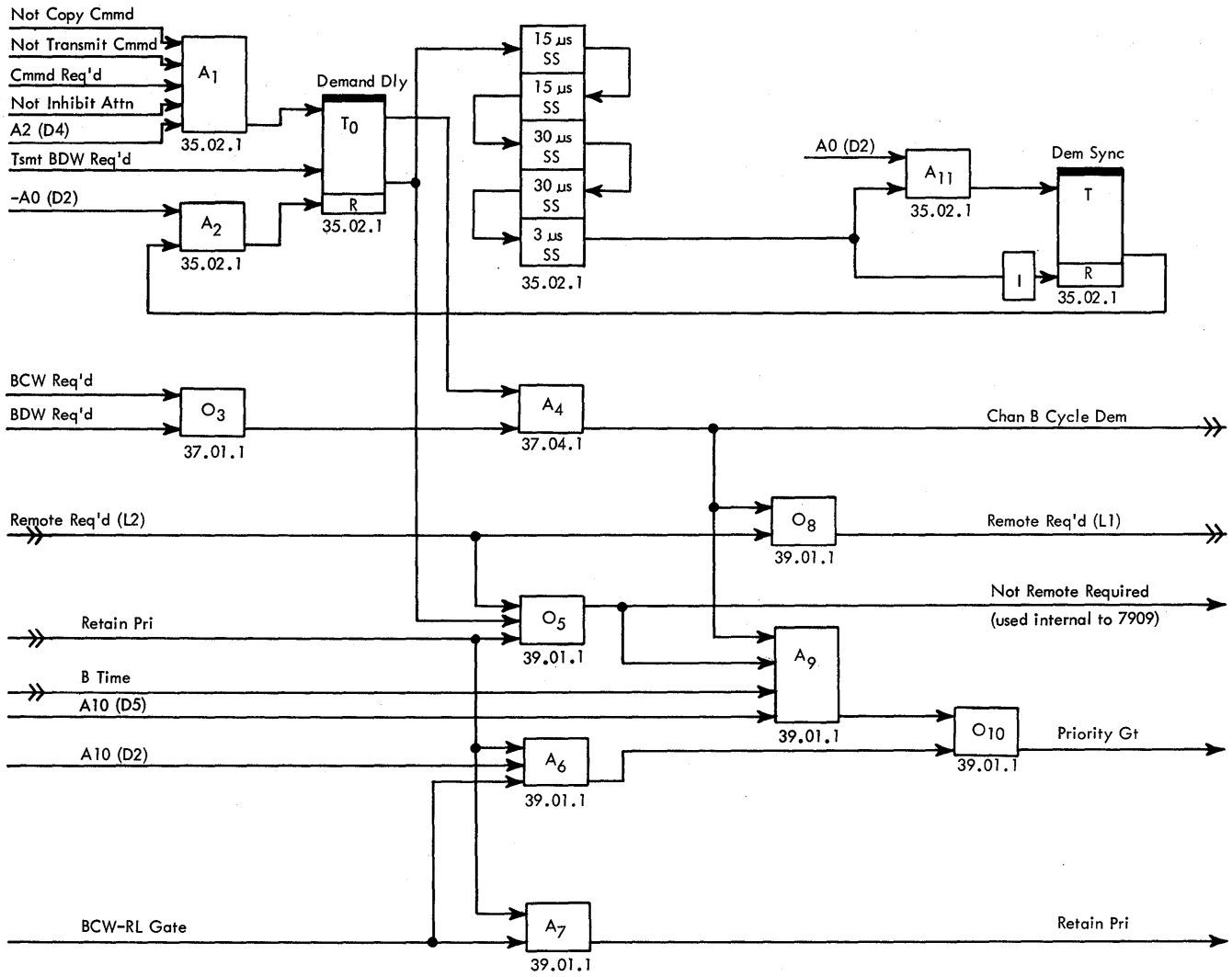


Figure 10. Channel Priority Logic

Item	System Page	Line Name	Level
A	37.01.1	BCW Req'd	+ S
B	37.04.1	B Cycle Dem	+ P
C	39.01.1	Remote Req'd (Line 2)	+ P
D	39.01.1	Remote Req'd (Line 1)	+ P
E	37.10.1	B Time	+ N
F	39.01.1	Priority Gt	+ S
G	37.01.1	BCW Tgr	+ S

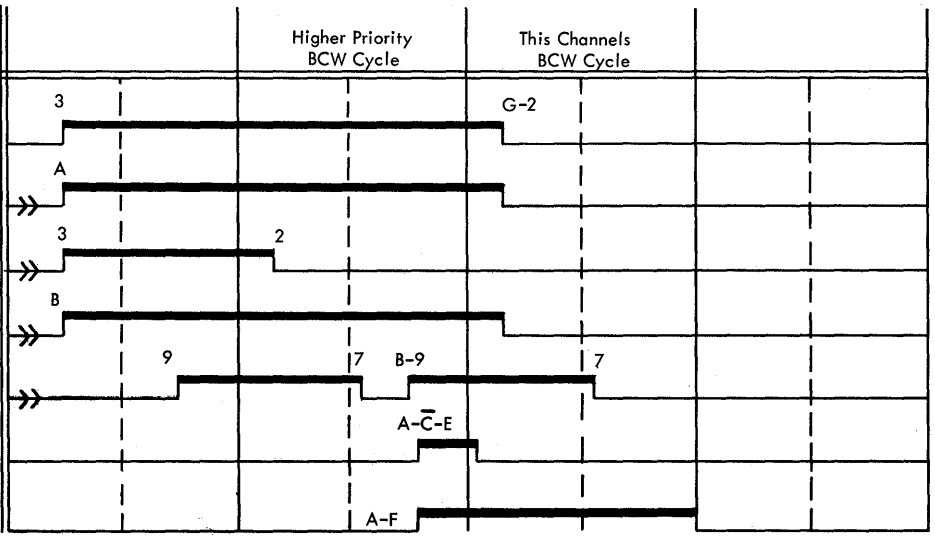


Figure 11. Channel Priority Sequence Chart

Either a BCW required or BDW required signal from the channel circuits will, via O_3 and A_4, demand a B-cycle from the computer. This demand line is common for all channels and may be activated by any one of them. At the same time that a request is made for B time (3 time of the cycle), a remote required line is initiated by O_8 and propagated to the lower priority channels as described in the previous section. With no other higher unit requesting, the next B time issued from the computer will be acceptable to this channel at A_9. "B time" becomes active at 9 time of the first available cycle as determined by the computer's program. "Priority gate" at O_{10} becomes active at 10 time, causing the appropriate BCW or BDW trigger to be set so that the next cycle will be either a BCW or BDW.

If a higher priority channel had requested B time simultaneously, "remote required" would have conditioned O_5 with the result of blocking A_9. At this point the decision is made as to whether the common B time line from the computer is for use in this channel or one of higher priority. When all higher demands are satisfied, the input remote required line falls and allows A_9 to become active. Note that as long as any channel is demanding, B times continue until all channel requirements are fulfilled.

Circuits A_6 and A_7 pertain to TCH or indirectly addressed commands as recognized by the multiplexor and is discussed under "Indirect Addressing." The purpose, however, is to retain priority within the channel so that an additional BCW cycle is made available.

Demand Delay

Data transmission commands such as reading, writing, control, and sense require B time almost immediately upon request because their operation is governed by the speed of the attached I-O device. The 7909, however, is really a small computer by itself with many logical and functional commands at its disposal. Each of these commands requires and requests either BDW or BCW cycles to perform its functions. If several of these commands were to be executed in quick succession, one channel could easily monopolize B time and prevent data in other channels from being properly stored.

To eliminate this problem, any non-essential requests for B time are delayed by an amount dependent on the number of operating channels attached to the system. The demand delay trigger (Figures 10 and 12) is turned on by the channel's request for a new command (BCW) cycle as indicated by the input, "CMMD required," at A_1. An exception to this is between CPYP commands for data transmission where the system is time-limited by the I-O device. "Inhibit attn" blocks A_1 in this particular case.

The demand delay trigger, coming on, blocks A_4 and prevents sending B cycle demands to the computer. At the same time, a chain of single-shots is started to produce an appropriate time delay before allowing the trigger to be reset by A_2. Five single-shots are available in the machine and may be inserted or eliminated to produce a delay of 0-90 μs. The last 3-μs single-shot must always be used, for it provides the

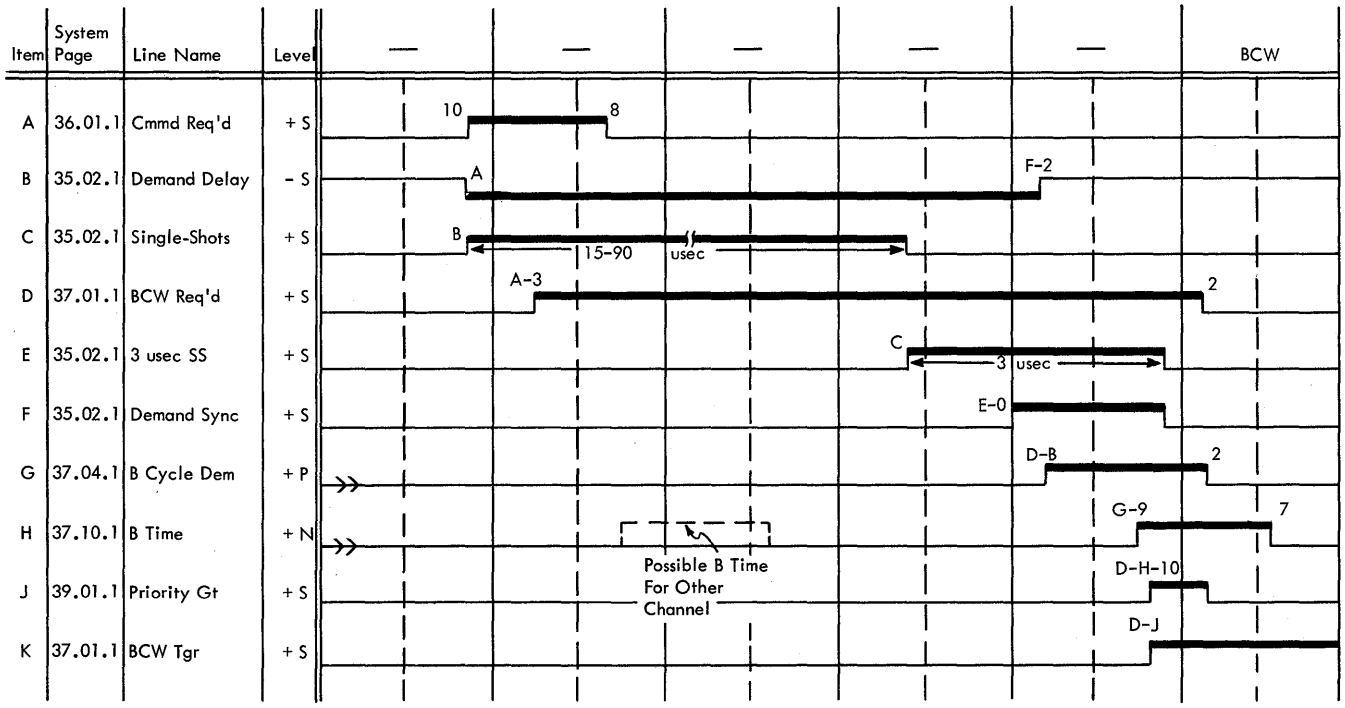


Figure 12. Demand Delay Sequence Chart

necessary synchronization. The first 0 time after the 3-μs single-shot starts timing out turns on the demand sync trigger through A_{11}. The trigger output gates A_2, and the demand sync trigger is reset at the next 2-time. A_4 becomes active and allows a "channel B cycle demand" to be sent to the computer.

The transmit command could consume many BDW cycles if large blocks of data were being shifted within storage. Because of this, "TSMT BDW required" also activates the demand delay circuitry so as not to fully monopolize core storage.

DEMAND DELAY SINGLE-SHOT TIMING

The total demand delay to be used is governed by the system configuration. Refer to Figure 2 and the table under "7909 Data Channel Timings" and also to the section on "Maximum System Configuration" to calculate the system weight and appropriate channel cap-cut. The Y3·· jumper card is located at 05A3D21. Systems 50.00.32.0 shows the cap-cut numbers and corresponding timings.

Each of the single-shots listed below is adjustable and must meet the specified timing durations within ±10 percent.

NAME	SYSTEMS	LOCATION	CARD	TIMING
Demand Delay	50.35.02.1	05A3C24	TBN	15 μs
Demand Delay	50.35.02.1	05A3D24	TBN	15 μs
Demand Delay	50.35.02.1	05A3E23	TBN	30 μs
Demand Delay	50.35.02.1	05A3D22	TBN	30 μs
Demand Delay	50.35.02.1	05A3E22	TBN	3 μs

The simplex I-O interface consists of two signal cables which connect an individual input-output adapter to a computer or channel. This is the extent of hardware; the most important part is the specific definitions associated with the signals within the cables. These signals are defined explicitly in regard to: function, timing, electrical characteristics, and connector pin assignments.

With the interface, it is possible to achieve a uniform means of communicating control information and data between computers and I-O equipment. The result is the design of a wide variety of processors and I-O devices for interconnections; adoption by I-O programming to standard I-O control program packages; elimination of redundancy in development and design effort; and reduction in manufacturing and service costs. In this manual the most important advantage is that, knowing the logic and demands of the simplex I-O interface, we need not concern our discussions with any particular I-O device.

Whether the channel is operating with a 7631 Disk Control, 7640 Hypertape, 1414-6 Synchronizer, 7750 Programmed Transmission Control, or any other present or future device need not directly concern the reader; all will operate on an identical request-response basis.

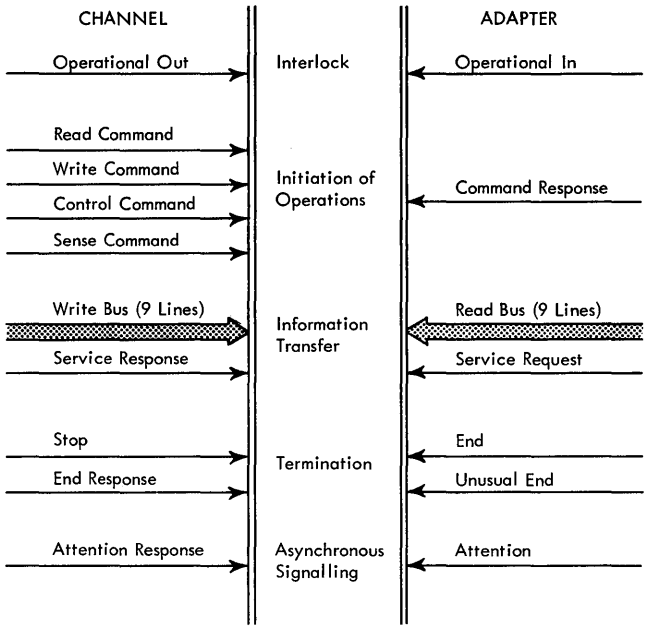


Figure 13. Interface Functional Grouping

Functional Description

The interface is divided functionally into five groups of lines (Figure 13). Generally, any signal must be maintained until its corresponding response is provided by the receiving unit.

Interlocks

Two lines are used to interlock completely the channel and I-O device. Each line reflects the operational status of the unit at its driver end.

Operational Out: Lines from the channel are significant only when "operational out" is up. The down-state of the operational out signal is used to reset the I-O. Unless the I-O is in an off-line mode, any down-state of sufficient duration to cause a response from the particular circuit family provides the reset. The meaning of the reset is defined by the I-O. To insure a proper reset, the operational out line must remain down for at least 6 μs.

Operational In: During simplex operation, lines from the I-O are significant only when "operational in" is up. When "Operational in" is down, the I-O normally will not respond to any signals from the computer.

Initiation of Operations

An I-O operation is initiated by one of the four commands (READ, WRITE, CONTROL, and SENSE) and their common response (COMMAND RESPONSE). Both READ and SENSE establish transfer of information from the input-output to the channel. READ is associated with the transfer of data while SENSE is associated with the transfer of status information of the input-output. Both WRITE and CONTROL establish transfer of information from the channel to the I-O. WRITE is associated with transfer of data while CONTROL is associated with the transfer of orders to the I-O. Commands are executed over the interface sequentially. An operation associated with any of the four commands must be properly terminated prior to issuance of the next command.

Read Command: The read command line is used to signal the I-O to cause the next block to be read into the computer. The read command signal, as well as all other command signals, is loop-checked by the command response line.

The read command signal must not be initiated unless "command response" is down, and unless "stop" and "end response" are either down or are dropped at the time "read command" is raised. The read command signal must remain up until the rise of "command response." It must fall before the rise of "end response."

Write Command: The write command line is used to signal the I-O to proceed with writing a block of data. Loop checking and signal timing specifications are the same as for "read command."

Control Command: The control command line is used to signal the I-O that it must accept orders from the computer over the write bus and must perform the operation encoded in the order. Examples are: rewind, backspace, and so on. Loop checking and signal timing specifications are the same as for "read command."

Sense Command: The sense command line is used to signal the I-O to send status information to the computer over the read bus. The information sent depends on the definition of the sense operation for the particular I-O concerned. Examples are: error indicators, rewind, or seek status. Loop checking and signal timing specifications are the same as for "read command."

Command Response: The command response line is used to signal the channel in recognition of a signal on any of the four command lines. It indicates the ability of the I-O to initiate the command.

The command response signal must rise within 6 μs of the rise of any of the four commands. If, because of skew, "stop" or "end response" from the preceding operation overlaps the command, "command response" cannot rise until "stop" and "end response" are down. "Command response" must not fall during the execution of the command; it must fall within 6 μs of the rise of "end of response."

Information Transfer

Information is transmitted over the "read bus" and the "write bus" on the demand and response basis. Demand is indicated by "service request" and response by "service response." Information is transferred parallel by byte. The byte may be up to eight bits in size. The 7909 Data Channel, however, uses only six of the eight available data lines. The remaining two positions are inoperative.

Organization of Information: The "read bus" and the "write bus" of the interface are insensitive to any codes. Information on the read and the write bus is arranged so that bit position 0 of a bus always carries the highest order bit, with bits in descending order being assigned to bit positions of the bus string in computer or I-O storage (the bit from bit position 0 of a byte always adjoins the bit from bit position 7 of the preceding byte). As a result, a message consisting of several bytes always appears as follows: bus bit positions 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, and so on.

When a byte transmitted over the interface consists of less than eight bits, the bits must be placed in the highest-numbered contiguous bit positions of the bus. Thus, when a channel or an I-O device transmits over the interface only the six bits of the BCD code, bit B is placed in bit position 2 of the bus, bit A in bit position 3, etc., and bit 1 is placed in position 7. When a channel or an I-O device places information on or receives information from only four lines of a bus, it must use bit positions 4, 5, 6, and 7 (sense data use bit positions 3, 5, 6, and 7). Any unused lines of the read or write bus must include the low-numbered bit positions of the bus, i.e., bit position 0 and adjacent bit positions. The parity bit of any byte must always appear in the parity bit position. Unused lines must always present logical zeros to the receiving end.

Write Bus: The write bus is used for sending both data and control information to the I-O. It consists of nine lines: eight data lines plus one line for odd parity. Not all of these lines need be used. Data must be valid on the write bus from the rise of "service response" until the fall of "service request." The assignment of bit positions on the nine lines on the write bus is:

Line Name	7909 Assignment
Parity Bit	Bit C
Bus Bit Position 0	Unused
Bus Bit Position 1	Unused
Bus Bit Position 2	Bit B
Bus Bit Position 3	Bit A
Bus Bit Position 4	Bit 8
Bus Bit Position 5	Bit 4
But Bit Position 6	Bit 2
Bus Bit Position 7	Bit 1

Read Bus: The read bus is used for sending both data and sense information to the channel. It consists of nine lines: eight data lines plus one line for odd parity. Not all of these lines need be used. Data must be valid on the read bus from the rise of "service request" until the rise of "service response" unless the permitted modification to the definition of service request is used. In the latter case, the availability of data on the read bus may lag the rise of "service request" by an adjustable time. This time may not be longer than the shortest interval in which the particular channel can accept data after the rise of "service request." The assignment of bit positions on the nine lines of the read bus is the same as for the write bus.

Service Request: The "service request" line is used to signal the channel when the I-O wants to transmit or receive a byte of information. During read and sense operations, "service request" rises when information is available on the read bus and "service response" is down. The rise of "service request" must be delayed

sufficiently to guarantee that it does not precede data when measured at the cable connectors at the channel under the worst case skew conditions. Skew that is caused within channel circuitry must be accommodated by the channel. Within the above skew limitations, data must be valid until the rise of "service response." During write and control operations, "service request" rises when, or before, information is required on the write bus and "service response" is down.

The service request signal must fall after the rise of "service response." During read and sense operations, "service request" must fall within 6 μs of the rise of "service response."

When the next cycle time is reached (in the case of cyclic devices), and "service response" has not occurred, the I-O must drop "service request" and must recognize an over-run condition. For these cyclic I-O, the minimum interval between the rise of "service response" and the fall of "service request" must be part of the I-O specifications.

To improve the system's performance, the rise of "service request" can be advanced relative to the time the data are valid on the read bus from the timing as just described. The rise of "service request" can precede the data by an amount of time that is the shortest interval in which the particular channel can accept data after receiving "service request." If this modification to the basic definition is used, the amount of this advance must be adjustable at the time of installation.

Service Response: The service response line is used to signal the I-O in recognition of a signal on the service request line. "Service response" indicates to the I-O that the channel is transmitting or has received information on the data busses.

During write and control operations, the rise of "service response" indicates that data are available on the write bus. The rise of "service response" must be delayed sufficiently to guarantee that it does not precede data when measured at the cable connectors at the channel under the worst case skew conditions. Skew that is caused within cables and I-O circuitry must be accommodated by the I-O. Within the above skew limitations, data must be valid from the rise of "service response" until the fall of "service request." During read and sense operations, "service response" must rise when the channel has accepted the information on the read bus.

The service response signal must rise before the fall of "service request." In the case of cyclic devices, "service response" must rise before the fall of "service request" by a time specified by the I-O. If "service response" rises too late, the I-O must recognize the over-run condition.

The service response signal must remain up until the fall of "service request." It must fall after the fall of "service request."

Termination of Operations

An operation may be terminated by either the channel or the I-O. The channel accomplishes this by the stop signal. The I-O indicates successful completion with "end" and abnormal completion by "unusual end." In either case the channel responds with "end response." The cause of "unusual end" may be determined by analysis of the status information obtained by a subsequent "sense command."

Stop: The stop line is used to signal the I-O that the channel has recognized the end of a record or operation. If the I-O recognizes the end of operation first and generates an "end" or "unusual end," no stop signal occurs.

Upon receipt of the stop signal, the I-O proceeds to its normal ending point. No further "service request" is sent and no further "service response" is expected. To complete the ending procedure, the I-O device sends an end or unusual end signal at the proper time and receives in return an "end response" from the channel.

The stop signal may rise any time when "command response" is up except when both "service request" and "service response" are also up. If "stop" is issued when "service request" is up, it replaces "service response." In this case, on read and sense operations data on the read bus are not accepted.

The stop signal must remain up until the fall of "command response" and must fall when or before a new command signal is sent to the I-O.

End: The end line is used to signal the channel that the I-O has recognized the normal ending of an operation. If anything abnormal such as data check, program check, end of file, or cancel condition has occurred, the end signal is not used and an unusual end signal is given instead.

The end signal cannot rise until "service response" for the last service request has been received. "End" must stay up until "end response" is received from the channel and must fall within 6 μs of the rise of "end response." No further service request may be sent after "end" rises.

After every normal operation, the I-O gives an end signal. The channel may or may not have previously given a stop signal. In any case, the channel gives an end response signal after receiving an end signal from the I-O.

Unusual End: The unusual end line is used to signal the channel that the operation being executed has resulted in an unusual condition and has been termi-

nated. This signal is a summary of all unusual conditions such as data check, program check, end of file, out of material, or cancel. If an unusual end occurs, the end signal is not given. The channel therefore sees "end" or "unusual end," but not both.

The unusual end signal must stay up until "end response" is received from the channel and must fall within 6 μs of the rise of "end response." No further service request may be sent after "unusual end" rises.

The channel may have given a stop signal before the I-O signals unusual end. In any case, the channel gives an end response after receiving an unusual end signal from the I-O.

End Response: The "end response" line is used to signal the I-O in recognition of a signal on the end or unusual end lines. The end response signal restores the I-O to the conditions necessary for accepting a new command. The end response signal must remain up until the fall of both "command response" and "end" or "unusual end" and must fall before a new command signal is sent to the I-O.

Asynchronous Signaling

An I-O can present an asynchronous signal to the channel by means of "attention." "Attention" indicates to the channel that a change in status in the I-O adapter has occurred which requires attention. It also might imply that a mechanical operation such as the positioning of the access arms in an IBM 1301 Disk Storage, or the completion of a rewind operation in an IBM 7340 Hypertape Drive has just been completed.

It is not possible to use one common trigger for two interfaces because of the asynchronous nature of the attention signals. Therefore, identical circuitry is used to recognize either attention 1 or attention 2 conditions. This signal may come at any time whether or not one of the command operations is in process. The channel signals to the adapter the recognition of the attention by sending "attention response."

The attention signal can rise any time except when "attention response" is up and must stay up until the I-O receives an "attention response" from the channel. Attention must fall within 6 μs of the rise of the "attention response."

Turning off the attention signal generally does not reset the conditions which caused the indication. The conditions may be available for transmission to the channel on a sense command.

ATTENTION OPERATION

All attention signals (Figure 14) should be serviced; however, there could be long time intervals (minutes in the case of a rewind and unload tape operation) between the initiation of an operation and the instant an attention signal is received. Because of this, the adapter might be in use by a sharing system at the time. The attention signal from the adapter arrives at A_2 but is blocked at this point until the adapter is operational to this channel. (The adapter need not be selected, however.) With these conditions met, the channel executes a normal interrupt. Any attention signal arriving during an interrupt program is temporarily ignored at A_2. As soon as the present interrupt program is completed, however, "check condition gate" allows A_2 to become active, turns on the attention trigger, and immediately initiates a second interrupt.

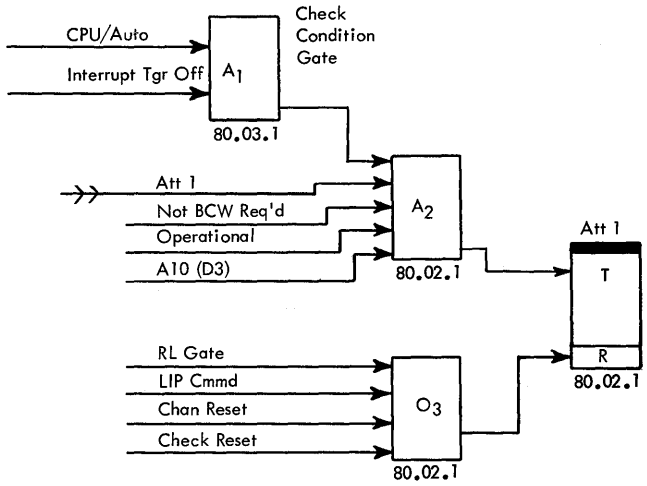


Figure 14. Attention 1 Condensed Logic

Attention Response: The attention response line signals recognition of action on the attention line to the I-O unit. The attention response signal causes the fall of the attention line. The attention response signal must remain up until the fall of "attention" and it must fall after the fall of "attention."

Electrical Characteristics

STANDARD SIGNALS

Regardless of circuit family, each interface must present the same electrical characteristics, i.e., any simplex interface driver is usable with any simplex interface terminator. Only single-load drivers and single-load terminators are required by this interface definition.

CABLE

One-hundred feet between the driving and terminating circuits is the maximum cable length. Ninety-five ohm coaxial is used, in general, although twisted pair is acceptable in favorable environments. The cable is terminated with the 40-position connector with pin assignments as shown in Figure 15. Signal lines are

CABLE 1		CABLE 2
Output from Chan (Input to I/O Adapter)	Shield - Signal	Input to Chan (Output from I/O Adapter)
Operational Out	1 - 2	Operational In
Read Cmmd	3 - 4	
Wt Cmmd	5 - 6	
Ctl Cmmd	7 - 8	
Sense Cmmd	9 - 10	
Parity Bit (Wt)	11 - 12	Parity Bit (Read)
Bus Bit Pos 0	13 - 14	Bus Bit Pos 0
Bus Bit Pos 1	15 - 16	Bus Bit Pos 1
Bus Bit Pos 2	17 - 18	Bus Bit Pos 2
Bus Bit Pos 3	19 - 20	Bus Bit Pos 3
Bus Bit Pos 4	21 - 22	Bus Bit Pos 4
Bus Bit Pos 5	23 - 24	Bus Bit Pos 5
Bus Bit Pos 6	25 - 26	Bus Bit Pos 6
Bus Bit Pos 7	27 - 28	Bus Bit Pos 7
Serv Resp	29 - 30	Serv Req
Stop	31 - 32	End
End Resp	33 - 34	
Att Resp	35 - 36	Att
	37 - 38	Unusual End
	39 - 40	Cmmd Resp

Figure 15. Cable Connector Assignments

assigned even-numbered pins; shields are assigned odd-numbered pins. This follows the established design automation rules.

PULSE DURATION

The minimum input signal pulse duration is determined by various factors including the response time of the receiving device, its type of circuitry, and the amount of logic within the device to provide the appropriate response. The speed boundary is not limited by the simplex interface.

DISCONNECTED CABLE

If the connecting cable is disconnected, the receiving and terminating circuits should assume an output signal condition making a down level available at at least one output.

POWER OFF

The design avoids exposure for damaging currents on connector pins if a power off condition occurs at one end of the cable.

GROUND REFERENCE

Any driver-terminator combination is able to tolerate ±0.75 volt differential in ground reference level. This ground shift includes DC as well as transient voltage difference.

The functional units of the 7909 Data Channel consist of registers, counters, half adders, rings, and other circuits using SMS cards. Since the 7090/7094 trained CE may not be familiar with the NOR logic used throughout the 7909, circuit card reference information has been included in Appendix C. Refer to Figure 16 for a diagram of all units and data flow.

Decoders

Instruction Decoder

This circuitry receives and decodes the various computer signals such as primary, secondary, and sense decoder outputs lines; unit address, enable channel control word trap address, and enable signals; and computer, E and L times. From these, the appropriate computer instructions are properly timed and executed.

Operation Decoder

This circuitry receives and holds the S, 1, 2, 3, and 19 bits from the storage bus during a channel control word cycle. With this information, the command is properly decoded and gated to the necessary circuits for execution.

Registers

Data Register

This 36-position register acts as a buffer for data flow between core storage and the assembly register. During a write or control operation, the data register is loaded with the next data word to be sent to the I-O device. On a read or sense operation, the input data word is kept in the data register until placed in core storage.

Assembly Register

The assembly register is a 36-position trigger register which assembles or disassembles data passing between the 7909 and I-O devices. Words are transferred between the data register and assembly register 36 bits at a time. From the assembly register to or from the character register, words are divided into characters (six bits) under control of the assembly ring and character in/out switches.

The contents of this register can also be loaded, stored, or compared against specific bit masks during various channel commands.

Character Register

The character register is a seven-position trigger register which acts as a buffer between the translators and the I-O adapter. Its purpose is to increase reliability at high data rates on a write operation. Characters pass from the character-out switches or translators through this register to the I-O adapter on write. On a read operation, characters enter the character register from the I-O adapter on their way to the read translators and character-in switches. The parity position does not accept information from the I-O adapter.

Check Condition Register

This six-position register stores the following channel interrupt conditions:

Position	Condition
1	Input-Output Check
2	Sequence Check
3	Unusual End
4	Attention 1
5	Attention 2
6	Adapter (Interface) Check

SCD Status Register

The store channel diagnostic (SCD) status register consists of circuits which gate the status of several triggers to the storage bus out switches. Bits are stored in the following positions of the storage location specified by the SCD instruction if the line was active:

Line	Bit Stored in
Prepare to Read	12
Prepare to Write	13
Read Status	14
Write Status	15
Interrupt	16

SMS Status Register

This seven-position register indicates the following channel status as set by set mode and select (SMS) command:

Channel Status	Address Bit
Enable Non-concurrence Interrupt	29
Read Backward	30
BCD Mode	31
Inhibit Unusual End Signals	32
Inhibit Attention 1 Signals	33
Inhibit Attention 2 Signals	34
Select 2	35

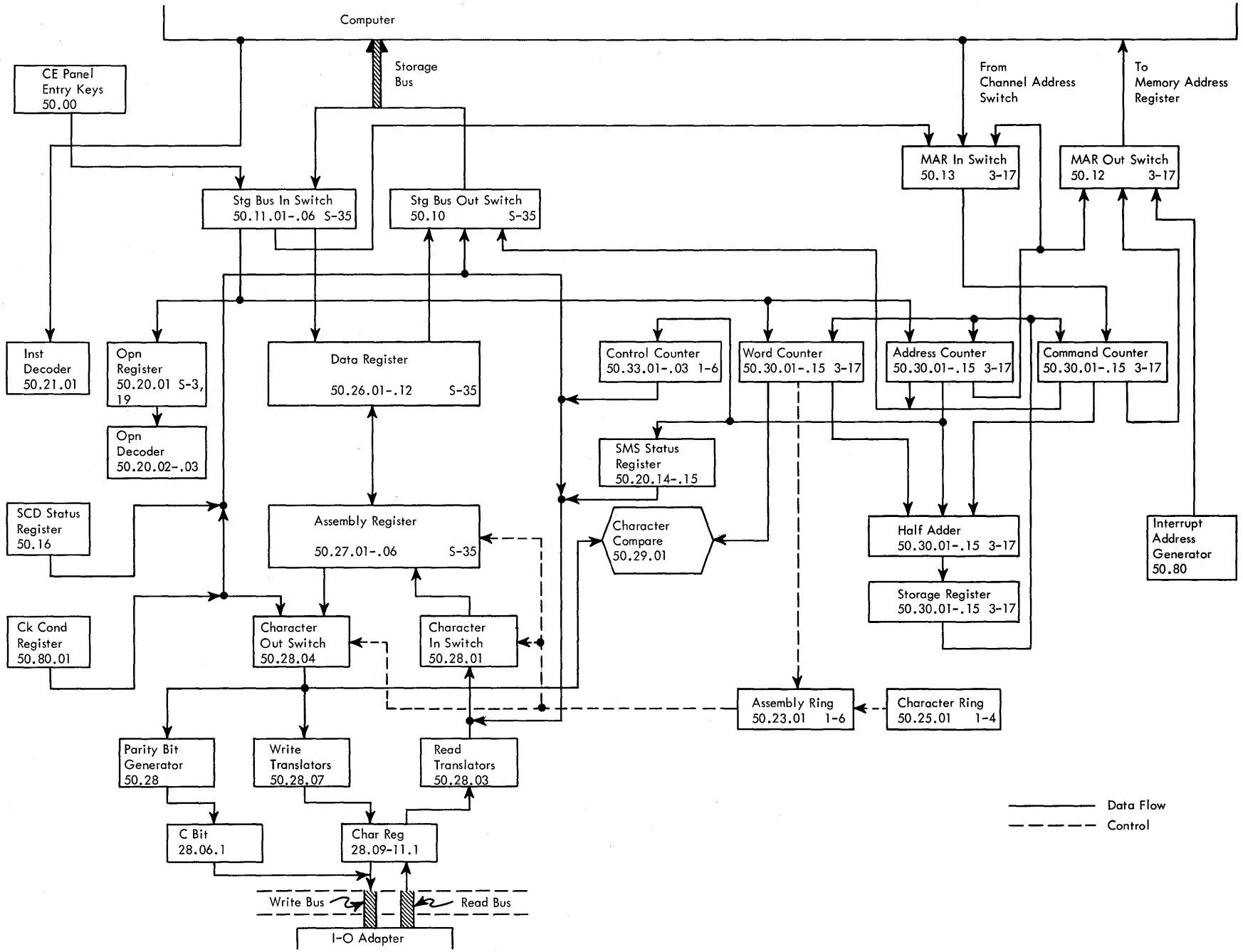


Figure 16. 7909 Functional Units and Data Flow

Storage Register

This 15-position trigger register acts as an intermediate buffer between the adders and counters when one of the counters is being stepped. A number from the counter is passed through the adders, incremented, and placed in the storage register; at this point the old counter value is reset and set again from the storage register.

Counters

Command Counter

This 15-position trigger register contains the core storage location of the next 7909 command. During automatic operation, the current value can be incremented by 1 or replaced from the multiplexor's address switches as the result of an RSC instruction or channel TCH or LIPT command. Successful channel transfers such as TDC or TCM cause the address in the command counter to be replaced by the value in the address counter. During a manual load-command counter operation, entry key settings will be routed, via the storage bus-in and MAR-in switches, to the command counter. Stepping the counter to indicate the next sequential command location is accomplished by a half adder.

INPUTS

There are four inputs to the command counter (Figure 17).

1. The storage register is an input during a cycle in which the counter is being incremented. A_{11} samples the outputs of the SR and, if a bit is present, causes the corresponding command counter trigger to be turned on.

2. The entry keys on the CE panel are an input during a manual load-command counter operation. During this operation, the entry keys are gated to the storage bus inputs where positions 21-35 are sampled into positions 3-17 of the command counter via A_8.

3. The memory address register is an input to the command counter on two conditions. The first condition is the result of a computer reset and start instruction which requires that the command counter be set to the location specified by positions 21-35 of the RSC. The other condition which causes sampling of the MAR is a TCH or LIPT command. In both cases, the multiplexor automatically routes positions 21-35 of the word from storage through positions 3-17 of the multiplexor address switches and onto the channel's MAR input bus.

4. The address counter is an input to the command counter when a transfer is made as the result of a transfer and decrement counter or a transfer on conditions met command.

Outputs of the address counter are fed to the command counter via A_{10} which is further conditioned by a successful transfer at A_7. Some of the operations which would cause this transfer are:

Computer Start Channel (STC) Instruction that causes the channel to transfer to the address specified by a wait and transfer (WTR) or trap and wait (TWT) command.

Transfer and Decrement Counter (TDC) Command that finds the control counter not equal to zero.

Transfer on Conditions Met (TCM) Command that results in a successful comparison of the mask with the check condition register or one of the assembly register characters.

Leave Interrupt Program (LIP) Command that loads fixed location of core storage into the channel registers and causes the channel to proceed to the location specified by the incoming positions 21-35.

Resets to the command counter are not shown in detail, but logically, the counter is reset just prior to the time when new information is to be entered.

OUTPUTS

The outputs of the command counter are fed to three different places (Figure 17). The normal sequential stepping through a series of channel commands, requires that the counter be incremented; thus, the command counter output is gated through A_{13} to the adders and from there via A_4 to the storage register. This incrementing of the command counter occurs during a command counter cycle (CCC) which is initiated by a channel BCW cycle.

The second output of the command counter feeds the storage bus and is gated through A_{15} as the result of a computer store channel instruction or a channel interrupt. In each case, positions 3-17 of the counter are placed on storage bus positions 21-35 so that the value will be placed in the address portion of a specified core storage location.

The third and probably most important functional output of the counter is that of controlling the memory address register. In this capacity, the command counter determines and controls where the next command will be obtained from storage. During normal BCW cycles, where no interrupts or conditional transfers are in effect, A_{14} causes the command counter to be placed on the channel address switch (CAS) bus to the multiplexor. The multiplexor, in turn, routes the information to the memory address register in core storage.

COMMAND COUNTER CYCLE

The sole object of the command counter cycle (Figure 18) is to increment the command counter by one. A request for the CCC cycle is made any time there is a control word cycle, as indicated by "BCW-RL gate." The

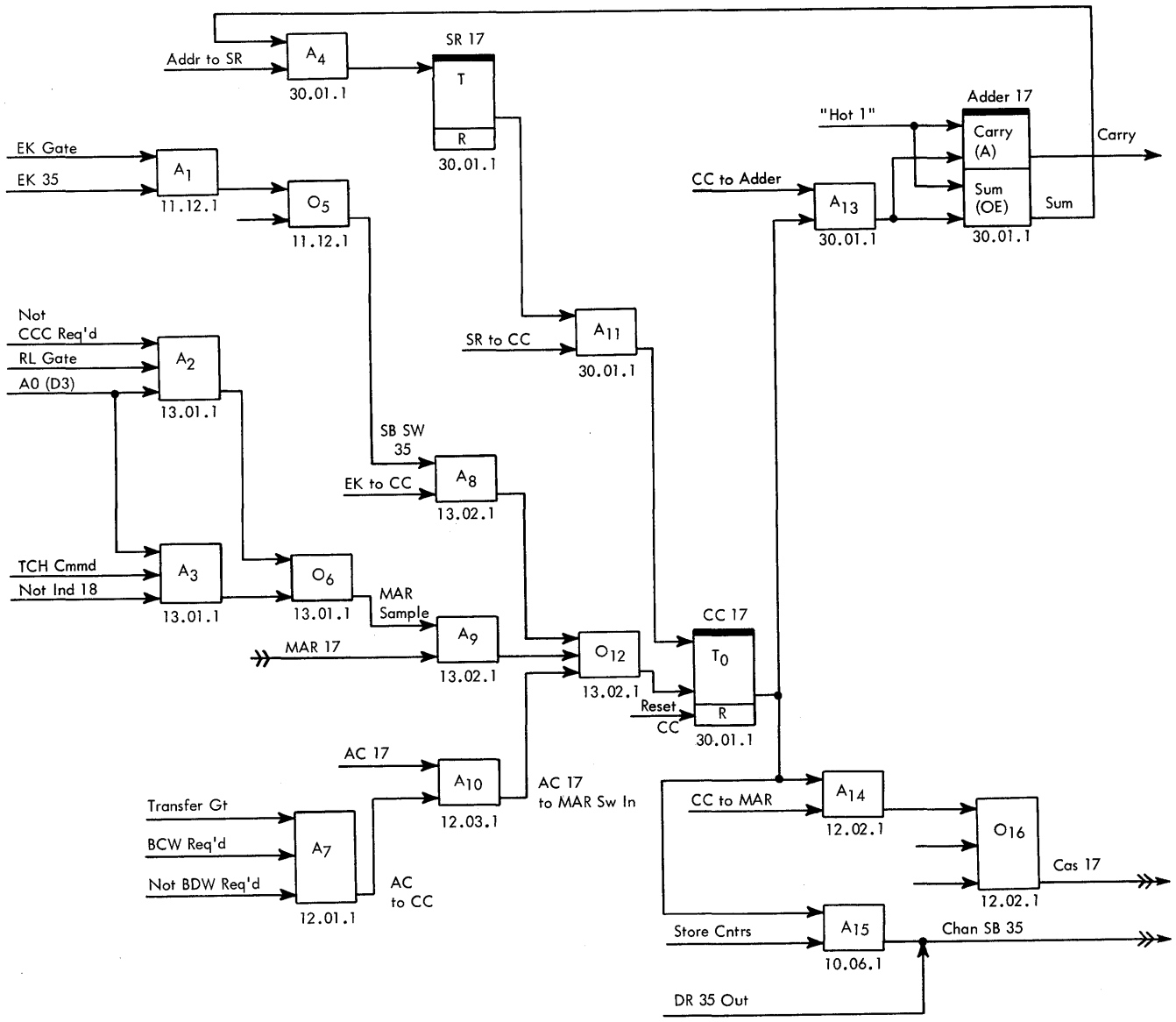


Figure 17. Command Counter Position 17

request is made at A5 time of the control word cycle, provided the incoming command is not a TCH or indirectly addressed command.

The channel storage register is reset early in the cycle to remove old information. Outputs from the command counter triggers are gated to the adders from A0-A10. This provides sufficient time for the necessary sums and carries to be generated so that the new value can be set into the SR at A8 time. With the incremented value now in the SR as an intermediate buffer, the control counter is cleared of its old value by an A9(D2) reset pulse and then immediately set again from the SR at A10(D2). Overlapping of the reset and set pulse delays the new value from being set into the control counter until 11 time of the cycle.

Word Counter

This 15-position trigger register accepts information from positions 3-17 of the storage bus. The basic function of the word counter is to control the amount of data flow between core storage and an input-output device. However, in addition to this, positions 3-17 of some channel commands may cause the word counter to perform other more specialized functions.

Operation of the word counter is somewhat different from that of its companions, the command counter and address counter, in that it must be decremented instead of incremented by one during each adder cycle. This presents a problem because the adders do not have the ability to subtract. Subtraction, however, is accomplished by complement addition which involves adding a +1 to the 1's complement of the actual number.

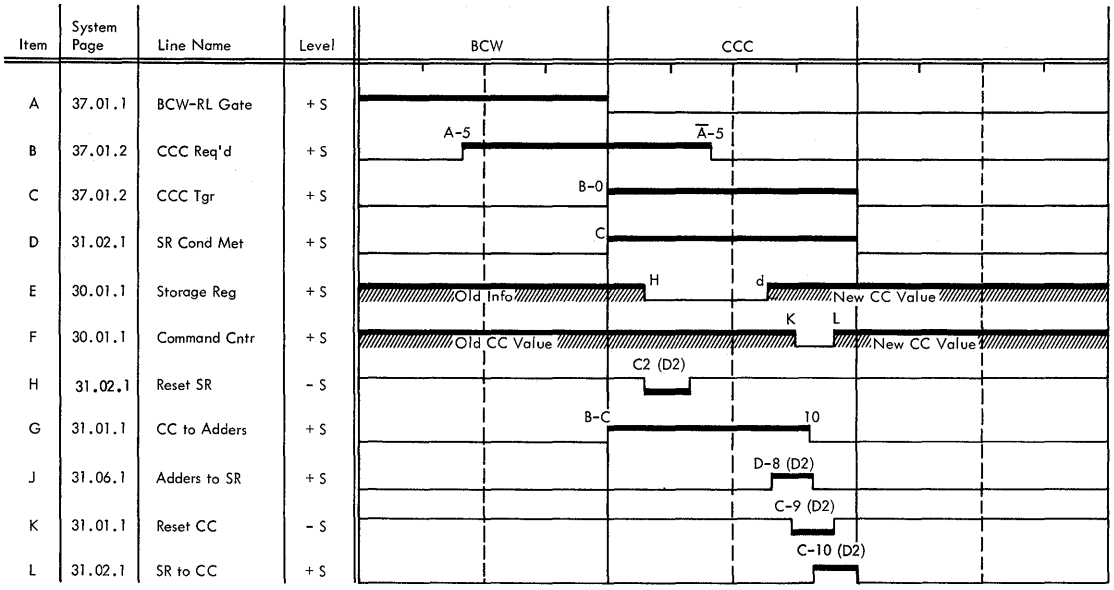


Figure 18. Command Counter Cycle Sequence Chart

The 1's complement is made available to the adders in the following manner. Note in Figure 20 that a control word cycle A_5 or a channel reset O_9 causes the word counter triggers to be reset on. Bits, then, coming into the channel on storage bus positions 3-17 (A_3) and gated to the operation registers via A_{10}, cause the corresponding triggers to be turned off. For example, if 4_8 were set into the counter, all triggers would be on except position 15 giving 77773_8. It might seem that this would present a false indication to the channel circuits but a closer examination of the trigger shows that both the CE panel indicators and active outputs are taken from the off side. Therefore, the *true* counter value is presented to the logic circuits and console indicators while the 1's complement of the number is made available to the adder circuits.

To illustrate word counter operation and how subtraction is accomplished by complement addition, take the examples of 4_8 being set into the word counter (Figure 19). The counter is initially reset on so that WC 15 can be turned off by the presence of a bit at SB position 15. Its indicator lights and displays the true value of 4.

During the next WC cycle, the counter's 1's complement value is routed to the adders where the "hot" 1 at position 17 causes a carry to propogate to position 15 leaving counter positions 16 and 17 off. This represents a value of 3 as indicated by the CE panel lights.

The next two adder cycles cause the value to be reduced by one each time. On the fourth adder cycle all counter positions are turned on (and all console indicators off) representing a word count of zero.

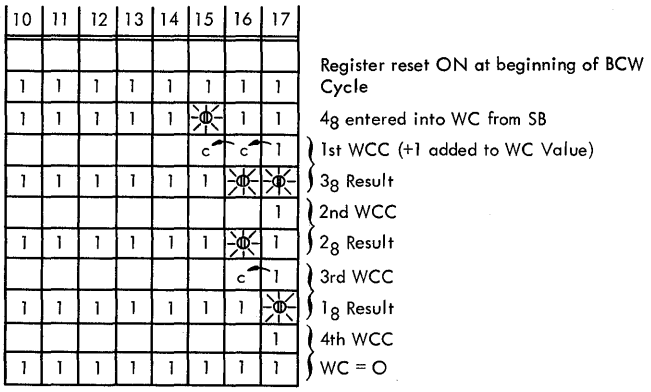


Figure 19. WC Complement Addition

WORD COUNTER INPUTS

One input source (Figure 20) is the storage register. During the latter portion of a WC cycle when a decremented value is set into the SR, the WC triggers are reset by A_2 and A_6 to allow setting again via A_8.

The other input sources are from the SB or CE panel entry keys. Both of these occur during BCW cycles; the first during automatic operation and the second during manual continuous-enter command. Again, note that the triggers are turned on by A_5 during the early portion of the control word cycle so that the complement value can be placed in the counter by turning off the appropriate triggers via A_{10}.

WORD COUNTER OUTPUTS

The on side of the word counter triggers feed the 1's complement of the actual number into the adder cir-

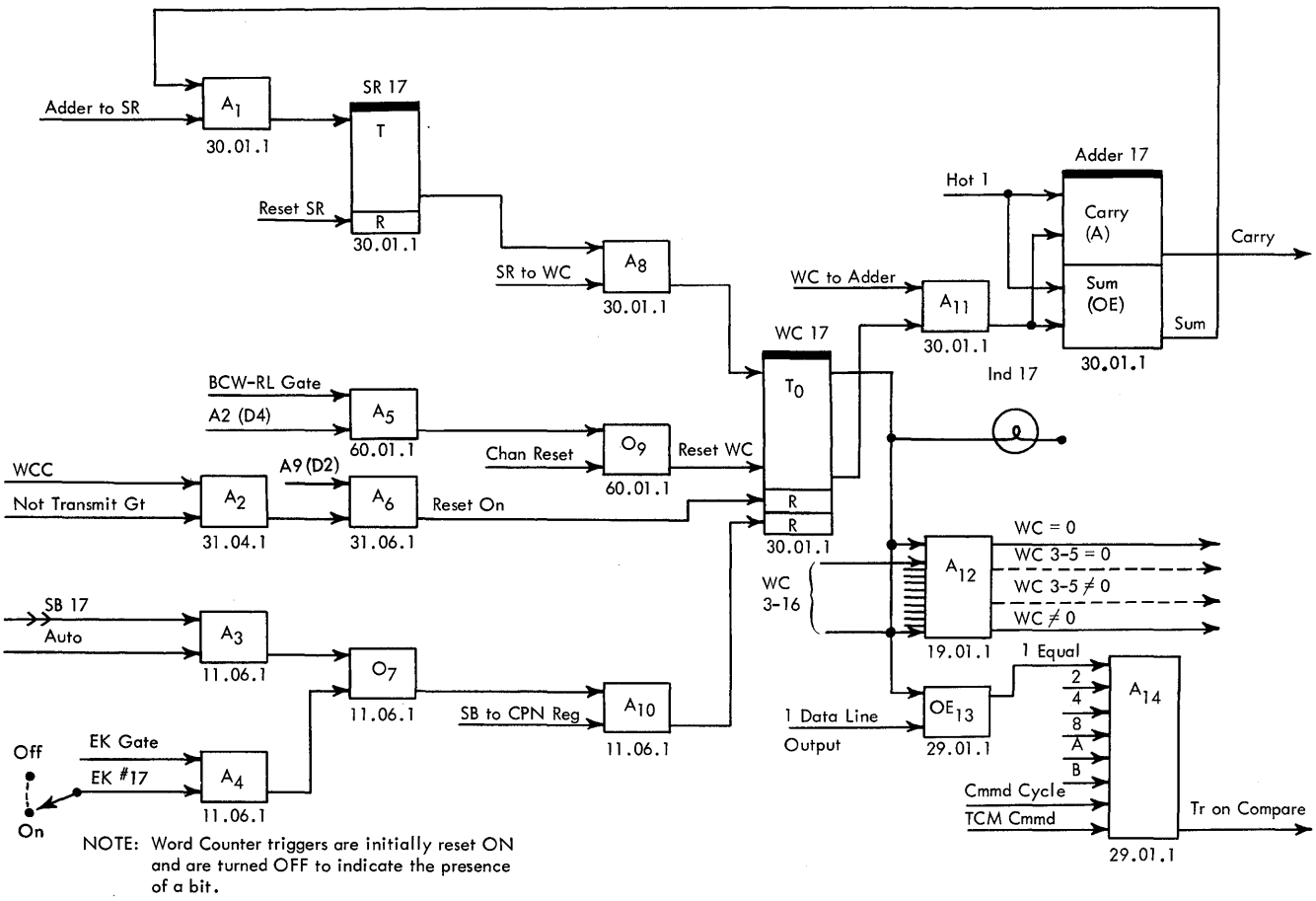


Figure 20. Word Counter Position 17

cuits (A_{11}) as was explained in a preceding section. A +1 introduced into adder position 17 causes decrementing the word count.

The off side of the triggers feed two types of conditions. First, they provide tests to determine whether or not a particular count is zero. Positions 3-17 are tested for zero at A_{12} and control data transmission during CPYP, CPYD, or XMT commands. Positions 3-5 also supply a count during insert control counter (ICC) and transfer on conditions met (TCM) commands to specify which one of the assembly register characters will be operated on.

The other function of the word counter occurs during a TCM command where positions 12-17 provide a six-bit mask for comparison purposes as shown at the EXCLUSIVE OR circuit OE_{13}. This output, further conditioned by the other bit comparisons at A_{14}, determines if a transfer will occur.

WORD COUNTER CYCLE

CPYP, CPYD, and XMT are the only channel commands that require a count control in the amount of data moved. Therefore, WC cycles will be allowed to take place only during these automatic operations. In manual status, WC cycles are also produced by "ring on."

A request for word counter and address counter cycles results from a channel BDW cycle. However, during a BDW cycle, the word counter performs no logic operations. Therefore, it is possible to combine the word counter cycle with the BDW cycle so that both the data transmission and the counter decrementing can be performed concurrently.

Operation within the cycle is straight-forward. The word counter outputs are gated to the adders from the rise of "wcc" until 10 time of the BDW cycle; the storage register is reset at A2(D2). The adder outputs have the new address ready by A8 time of the cycle and are sampled into the SR. The word counter is reset OFF at A9 time and the new value transferred from the SR at A11.

Word Counter and Address Counter Cycles

Word counter and address counter cycles (Figure 21) usually occur together since both are directly concerned with data transmission operations. As a result of data being transferred between core storage and an external device, or within core storage itself with a transmit command, both of the counters must be modified by a factor of one. With only one set of adders, it is not possible to do both the decrementing and incrementing within the same cycle. Therefore, two distinct cycles must be used.

Address Counter

The address counter is a 15-position trigger register which accepts information from positions 21-35 of the storage bus. It has multiple functions, but the basic one is that of controlling the place in core storage where data are to be operated on with an I-O device. This occurs during CPY commands while reading or writing data across the interface. As each data word passes through the channel, the address counter is normally incremented by 1 through the adders so that sequentially higher core storage locations are referred to. The logic of the address counter is changed somewhat if the read-backward feature is installed for Hypertape operation. In this case, the address value must be decremented by one each adder cycle.

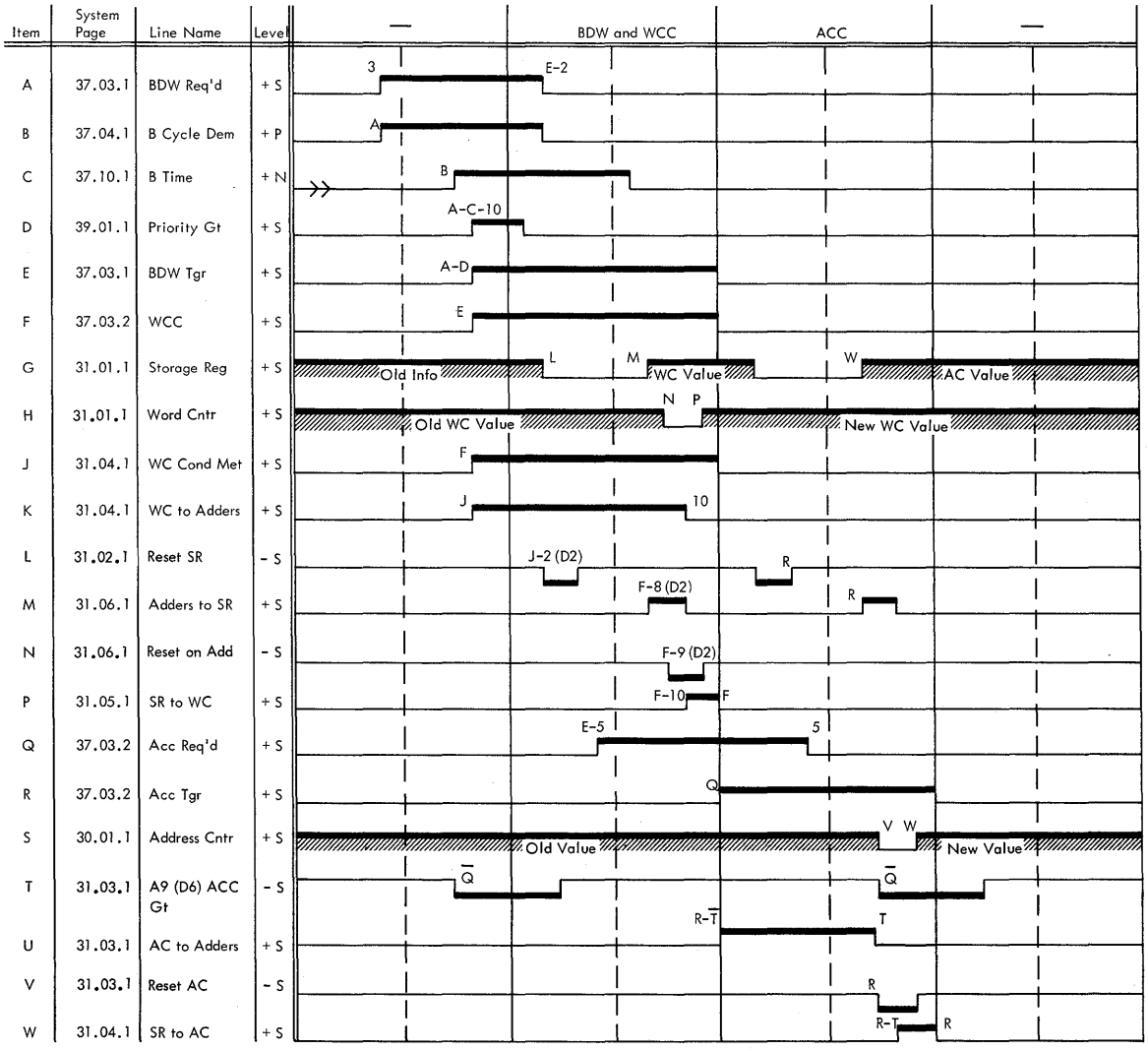


Figure 21. WCC and ACC Sequence Chart

During non-I-O operations, the address portion may have meanings other than core storage locations. These more specialized operations will be indicated under "Address Counter Outputs."

ADDRESS COUNTER INPUTS

One input is from the channel SR when the address is modified during an adder cycle. The new value is gated in through A_7.

The other inputs (Figure 22) to the address counter are either from the CE panel entry keys during a manual operation (A_2) or from the storage bus during a control word cycle (A_1). Here we must further qualify the operation. The channel is always considered to be in a forward status unless specifically programmed for a BKWD operation with the read-backward optional feature.

While in a normal, forward status, the value that appears at the storage bus during a control word cycle is set into the counter by A_6. Read-backward operations, however, require that data be stored in sequentially lower core storage locations. This implies subtraction, which is accomplished by using a 1's complement technique. Setting the 1's complement value is done by taking the out-of-phase output of A_1 and gating it via A_4 into the counter. Thus, triggers are turned on corresponding to SB positions which contain 0 bits. Because the AC indicators are taken from the on side of each trigger, the complement value is displayed to the operator.

ADDRESS COUNTER OUTPUTS

The most obvious output is through A_9 to the adders; whether the counter is incremented or decremented depends on the operation (see preceding section on "Address Counter Inputs").

The other outputs of the counter are gated by "rd fwd" at A_{10} or "rd bkwd" at A_{11}. Because these two lines originate from the OFF and ON outputs, respectively, of a single trigger (rd bkwd) one is always active. With a read-backward operation placing the 1's complement in the address counter, it is necessary to

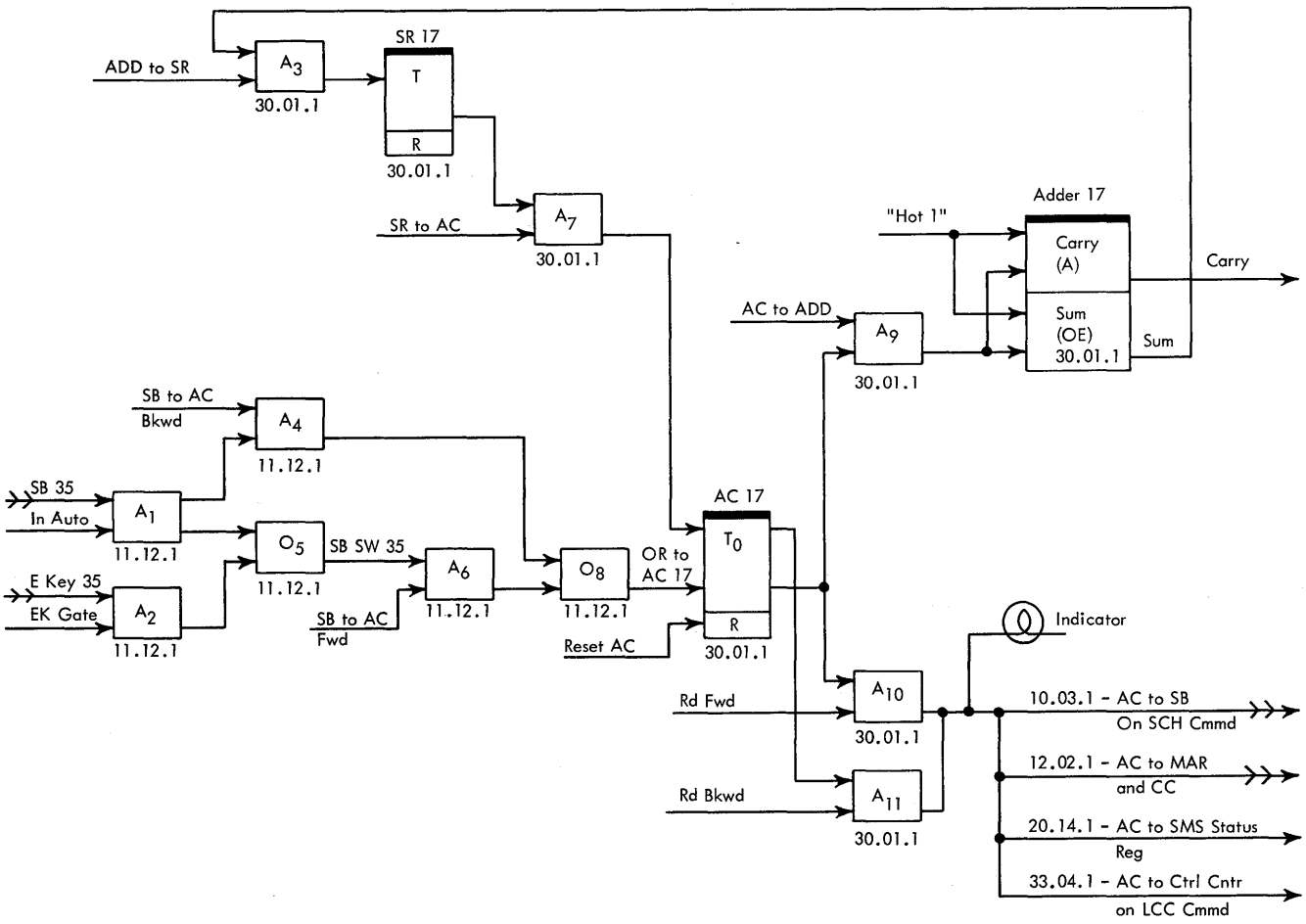


Figure 22. Address Counter Position 17

use the off-side trigger output at A_{11} to provide a true count to the logic circuits. When not in read-backward mode, the on-side outputs are gated to the circuits at A_{10} to again reflect a true value.

The AC outputs serve four functions. First, they feed storage bus positions 3-17 to store the address counter value during a store channel (SCH) instruction or channel interrupt command.

Next, they provide a core storage location to the memory address register (MAR) and command counter. Operations which require this function include: CPYP, CPYD, XMT, CTL, CTLR, CTLW, LAR, SAR, TDC, TCM, STC, WTR, TWT, and LIP.

Third, address counter positions 11-17, when loaded from SB 29-35 during a set mode and select (SMS) command, provide signals for setting appropriate indicators. Last, AC positions 12-17 provide a count to be placed in the control counter during a load control counter (LCC) command.

ADDRESS COUNTER CYCLE

The request for an AC cycle is made at A5 time of the BDW cycle and, therefore, immediately follows it. Operation is similar to the other counter cycles with the counter gated to the adders through A10 time. The SR is reset at A2 and sampled again at A8. The address counter is reset at A9 and set to the new value at A11. AC cycles occur during the following commands:

CTLR
CTLW
CTL
CPYP
CPYD
XMT
RING ON (manual operations)

Control Counter

The control counter is composed of six binary triggers. It is the only true counter in the machine and counts down one for each input pulse supplied by the transfer and decrement counter (TDC) command. Being a true binary counter, it does not rely on the half-adders for operation. The control counter is comparable to a small index register and may be set, tested, or decremented by a variety of channel commands.

All trigger positions are reset off as a normal state and may be set to any desired value from 0_8 to 77_8 by means of the load control counter (LCC) command.

The value in the counter can be retrieved by the insert control counter (ICC) command which places the counter contents in one of the assembly register character positions.

CONTROL COUNTER OPERATION

Figure 23 shows the interconnection between position 6 and position 5 of the control counter. For a detailed description and sequence chart on the operation of a binary trigger, refer to Figure 31 and the section on "Assembly Ring Drive."

Assume that position T5 and T6 of the counter contain 3_8 (both triggers are on) and three stepping pulses are supplied to the input of T6. The rise of each pulse causes T6 to change state by activating A_4, A_3, and A_4 in that order. The driving pulse for T5 is obtained from the output of A_3. Because A_3 is active for only half of its input pulses, only one drive pulse (the 2nd one) is sent along to T5. A_{10} allows this pulse to turn T5 off, leaving these two counter positions with a 0_8 value.

Stepping pulses are generated and fed to higher order positions in a similar manner, enabling the counter to handle numbers up to 77_8.

Adders

The command, address, and word counters in the 7909 do not have the ability, within themselves, to change their current value. They must rely on adders to accomplish the necessary incrementing or decrementing. Only one of the three counters can use the adders during any one machine cycle.

The only requirement of the adders is that they add +1 to the value introduced at the input and because of this only half adders are required to perform the operation. Half adders use only two inputs (i.e, one digit and a possible carry) while full adder circuits use three inputs (i.e., two digits plus a possible carry). Both types of adders, however, produce the same output results: a sum and a carry.

The 15 positions of half adders, as used in the 7909, consist of an AND circuit and an EXCLUSIVE-OR circuit (Figure 24).

A carry output will be available if both an adder input and carry input are present. This function is handled by the AND part of the circuit.

A sum output will be available if one, and only one, of the input sources is active: i.e., there is either an adder input or a carry. Either one and not both is known as an EXCLUSIVE-OR condition. The OE part of the circuit produces the correct sum output for this EITHER-OR condition. The output sum is fed to the storage register as an intermediate buffer while the carry output feeds to the next adder position (Figure 24).

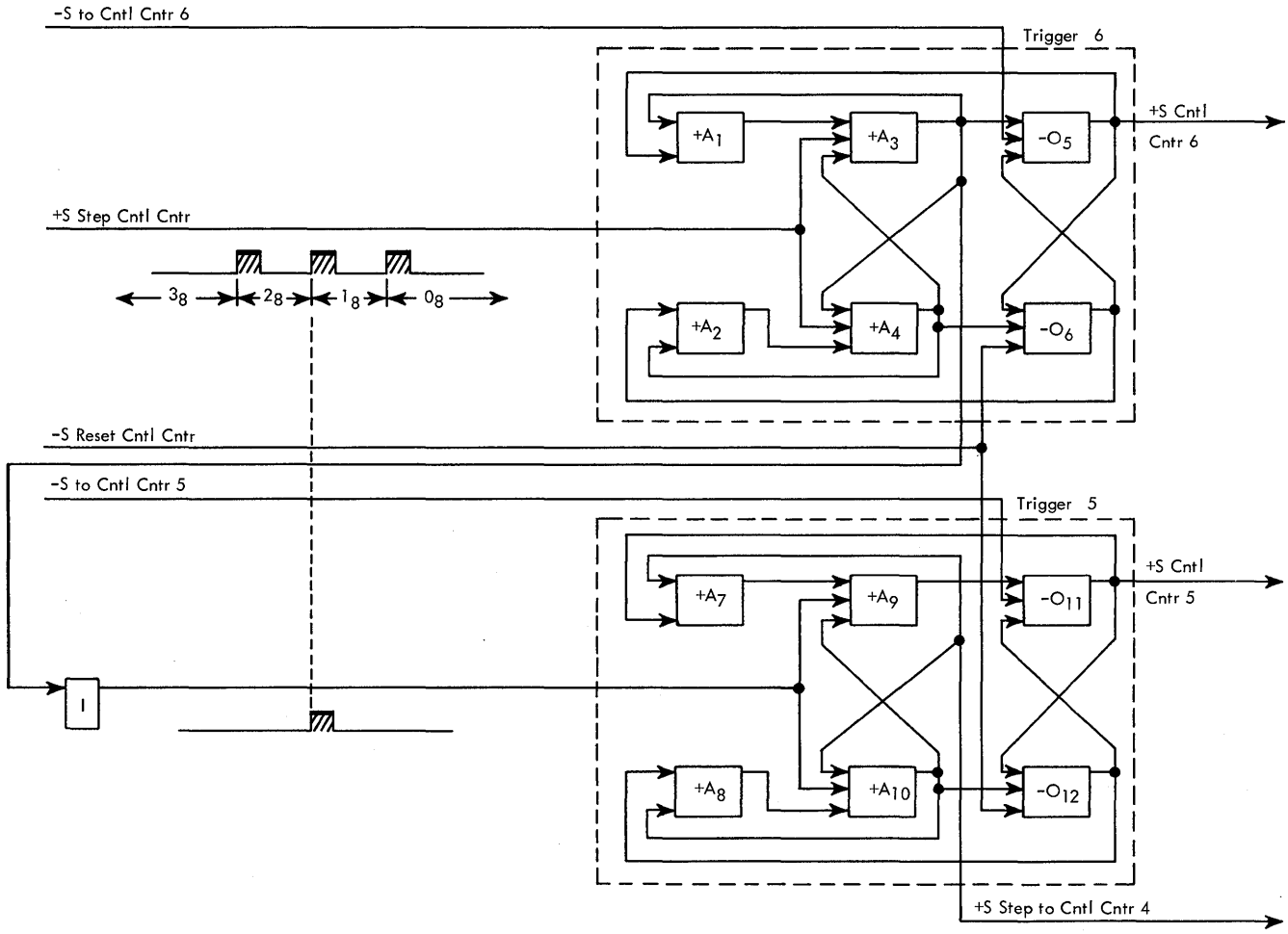


Figure 23. Control Counter

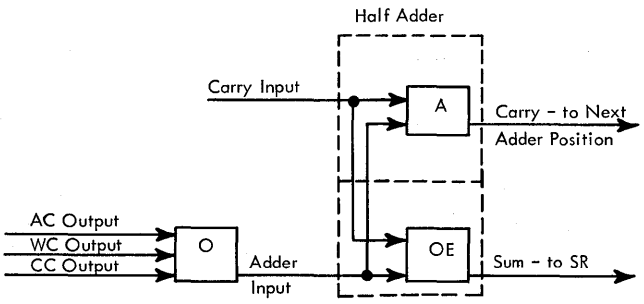


Figure 24. Half Adder Position

Adder Look-Ahead

Look-ahead carry (LAC) circuits (Figures 25 and 26) are used to eliminate the delay caused by a carry having to ripple through all of the adders.

To avoid this delay, the adders are formed into three groups; positions 17-14, 17-10, and 17-6. Carry ripple is reduced to less than ⅓ of the over-all circuit because it is confined within its own group; any propagation of the carry beyond a particular group is accomplished by the look-ahead circuitry. As seen in Figure 25, use of the LAC also eliminates need for the carry generating AND circuit in the high-order position of each group.

The adders, being designed to add +1 to the input value, always have a carry input to position 17 in the form of a "hot" 1. Therefore, any time there is a 1-bit input to adder position 17, there is also a carry output. If, at the same time, there is a 1-bit input to position 16, there will be a carry output to adder position 15. A 1-bit at position 15 will propogate a carry to adder position 14 where only a sum output is generated. At this point, a position 14 carry output is replaced by the LAC at A_1.

Note that the final sum outputs of positions 17, 16, 15, and 14 take time to reach their steady state because of the necessary carry inputs from preceding stages. A propogated carry out of the group, however, depends entirely on the individual adder inputs and, therefore, can be determined immediately. The logic of A_1 in Figure 25 or 26 indicates that if there are active inputs at positions 17, 16, 15, and 14, a carry is propogated

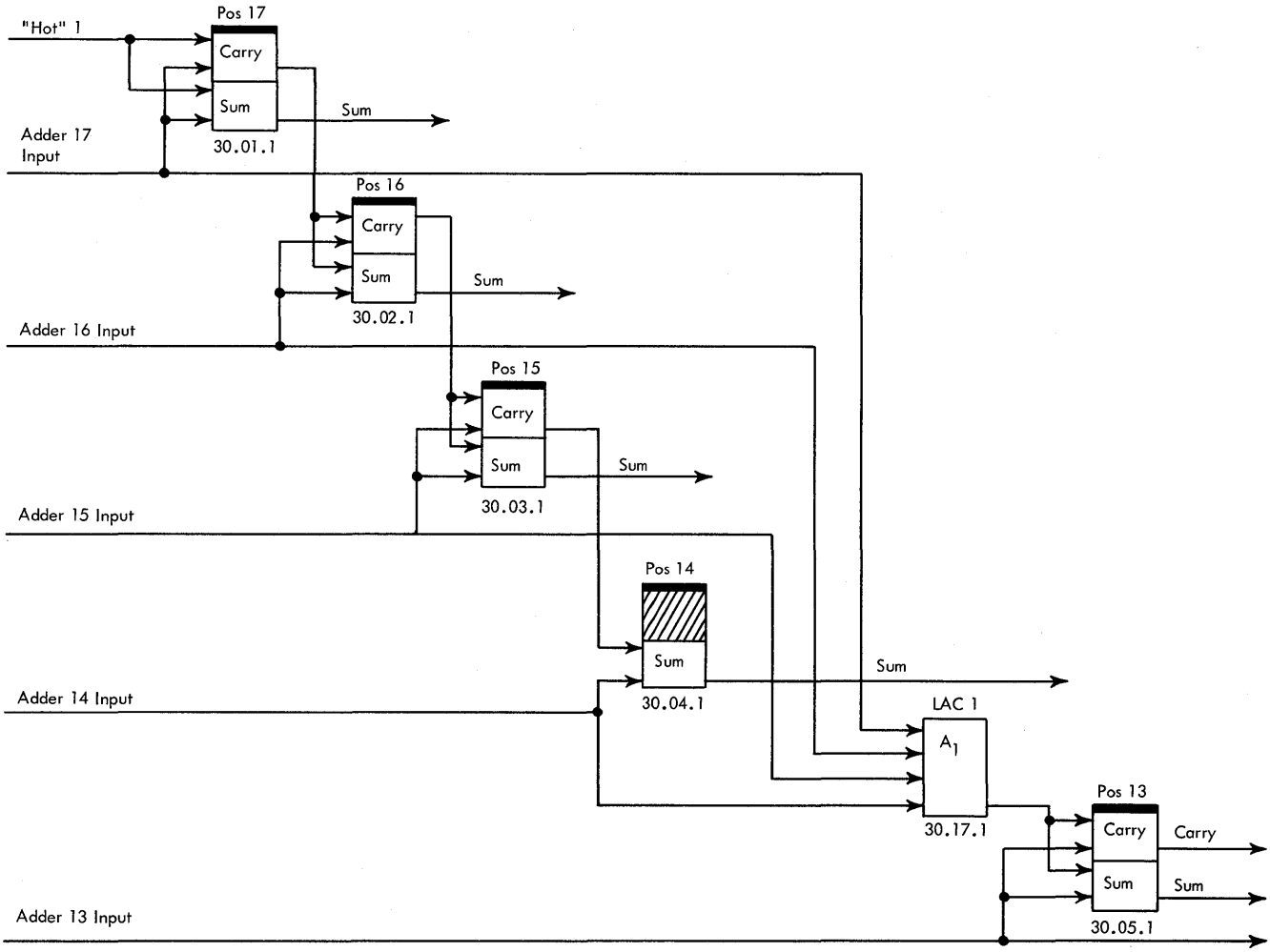
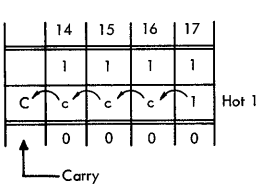
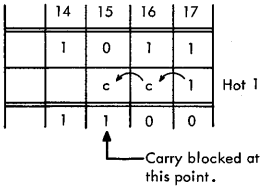


Figure 25. Adder Look-Ahead

out of the group. The lack of any input will immediately block this carry. Following are two examples of the above statements:





Carrying the LAC one step further, Figure 26 shows that A_2 immediately causes a carry to adder 9 if inputs 10-17 are active, and A_3 causes a carry to adder 5 if all inputs 6-17 are active.

Switches

Storage Bus In

This 36-position switch provides input paths from the multiplexor for data flow, channel commands, or entries from the CE panel entry keys.

Storage Bus Out

This 36-position switch provides an output path from the data register to the multiplexor for I-O data flow. During store channel (SCH) or store channel diagnostic (SCD) instructions, this switch also gates out information from the various status registers and counters.

MAR Switch In

This 15-position switch provides some of the input gating to the channel command counter. Its basic function is to receive an address from the multiplexor channel address switches during either a reset and start channel (RSC) instruction or transfer in channel (TCH) or leave interrupt program and transfer (LIPT) command. However, the switch circuitry is also used to receive information either from the CE panel (manual operations) or channel address counter (successful channel transfers).

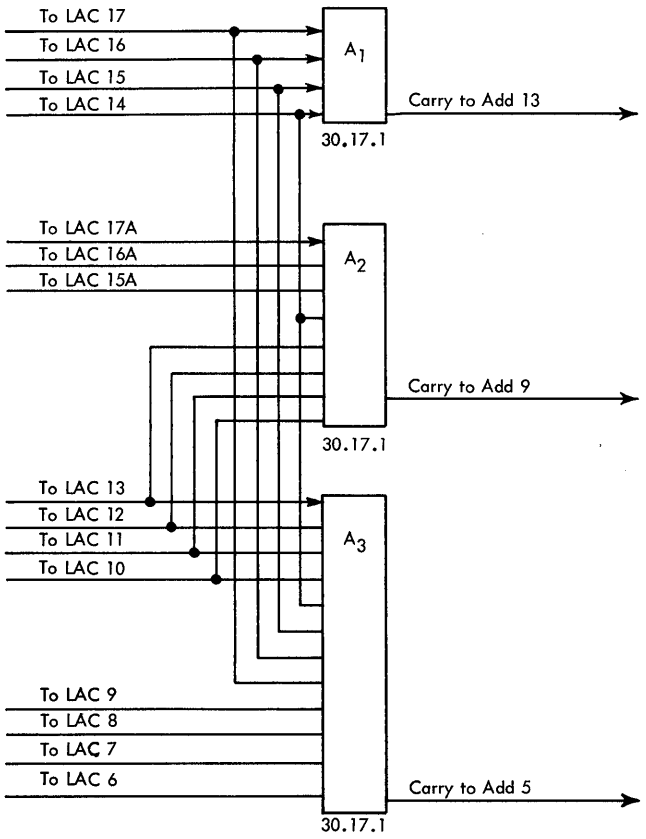


Figure 26. Adder Look-Ahead Grouping

MAR Switch Out

This 15-position switch provides core storage with an appropriate address during each channel reference (B) cycle. This address originates from the channel address counter, command counter, or interrupt address generator.

Character In Switch

This six-position switching circuit is used to gate information into one of the six assembly register character positions. Information can arrive either from the character register or from circuitry within the channel itself. Selection of the appropriate assembly register character position is under control of the assembly ring.

Character Out Switch

This six-position switching circuit is used to gate one of the six assembly register characters to either the character register (through the write translator if installed) or other circuitry within the channel. Selection of the appropriate character is under control of the assembly ring.

Rings

Character Ring

The character ring is a four-stage timing device used to synchronize and control data transfer between the channel and I-O adapter. Each service request from the adapter starts the ring; once started, odd and even drive pulses step it through all stages producing four timing pulses. These pulses are used to effect data transfer across the interface lines and also accomplish various other directly connected functions such as: resetting or stopping the assembly ring, initiating data transfer between the assembly register and data register, sending a service response to the adapter, and testing for error and stop conditions.

The four trigger outputs of the character ring (CRT1, CRT2, CRT3 and CRT4) are each three clock pulses in width and require a period of 12 multiplexor clock pulses (2 μs) to complete one character ring cycle. Output functions are shown in Figure 29.

CHARACTER RING OPERATION

Odd and even ring drive pulses are continuously being generated at O_1 and O_2 respectively (Figure 27). The odd drive pulses actually rise at even clock times but derive their name because of driving odd numbered ring triggers (CRT1 and CRT3). The even drive pulses, conversely, rise at odd clock times (Figure 28) but drive the even numbered triggers (CRT2 and CRT4). Normal status of the ring circuitry is with the CRT4 trigger on (reset on) and the remaining triggers off.

The first even drive pulse after the rise of "request" from the I-O adapter turns on the start trigger through A_3. Three clock pulses later, the odd ring drive turns on CRT1 through A_5. CRT1 turns on the one start trigger, gates A_6 so that CRT2 can be turned on with the next even ring drive, and turns off CRT4 and the start trigger. Each trigger, in turn, gates circuitry for the next and at the same time resets the previous position. In this manner, the ring continues to ripple through all four positions, ending with CRT4 on.

At CRT4 time a response signal is returned by the channel (50.51.01.1). As a result, the adapter drops "request"; the one start trigger is reset and the ring is again in proper status to handle another character of data.

CHARACTER RING OPERATION—REQUEST FAILURE

During normal operations a request from the adapter starts the character ring (Figure 27) and causes a character to be transmitted on the interface bus lines. "Response" is returned from the channel at CRT4 time and the adapter prepares for the next character transmission. If, during reading, for example, a second character is ready for transmission before the channel has

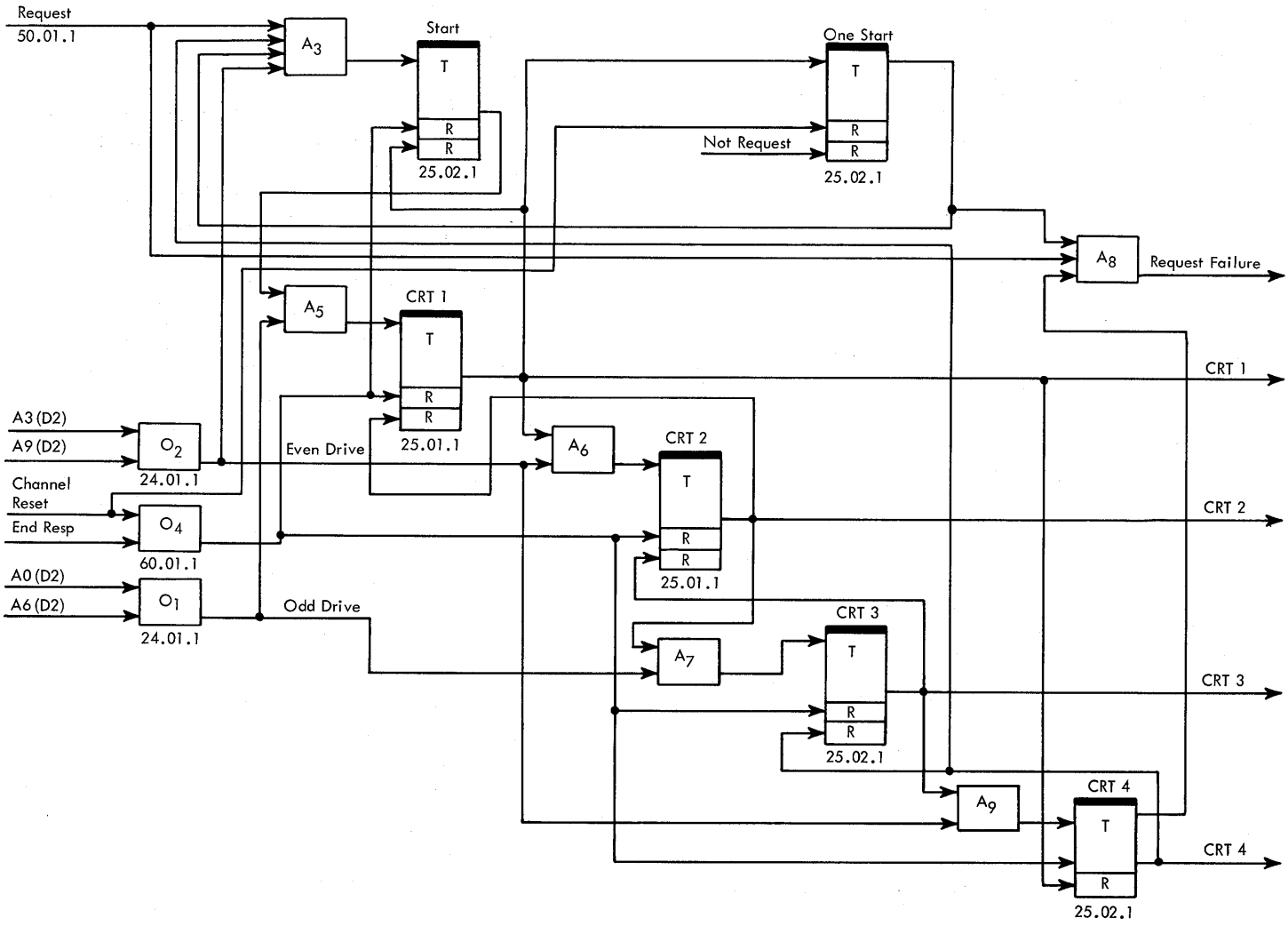


Figure 27. Character Ring Condensed Logic

returned a response signal, data are arriving at the adapter faster than the channel can accept it. If this condition arises, the adapter drops the old "request" (without waiting for "response") and brings up a second request signal. When the first "request" falls, the one-start trigger is turned off (Figure 27 and 29). The second request arriving before CRT4 time causes a request failure at A_8.

A character rate too fast for the channel ring to accept properly causes an immediate "stop" to the adapter and a corresponding channel interrupt.

Figure 30 shows sequence chart for request failure.

Assembly Ring

This is a six-position closed serial ring (Figure 33) which controls the gating of appropriate assembly register positions during data transfer between the channel and an I-O device. Each of the six trigger positions of the ring controls a group of six adjacent bits in the assembly register which represent a character or byte of information. Each request for data transfer across the interface causes the character ring to run one cycle. The character ring in turn advances the assembly ring at CRT2. In this manner, characters are stored or transmitted in proper sequence.

In addition to data transfer, the assembly ring outputs also function during insert control counter (ICC) and transfer on conditions met (TCM) commands.

ASSEMBLY RING DRIVE (Figures 31 and 32)

Figure 31 is the assembly drive circuit as shown on 50.22.01.1 of the 7909 Systems. Non-essential inverters have been eliminated and A_3 and O_6 have been reversed in designation (i.e., O to A and A to O) to aid in the explanation.

The circuit is essentially a DC binary trigger capable of changing its state (ODD or EVEN) with the rise of each

Item	System Page	Line Name	Level
A	24.01.1	A0 (D2)	+ S
B	24.01.1	A3 (D2)	+ S
C	24.01.1	A6 (D2)	+ S
D	24.01.1	A9 (D2)	+ S
E	24.01.1	Odd Drive	+ S
F	24.01.1	Even Drive	+ S
G	51.01.1	Request	+ S
H	25.02.1	Start	+ S
J	25.02.1	One Start	+ S
K	25.01.1	CRT 1	+ S
L	25.01.1	CRT 2	+ S
M	25.02.1	CRT 3	+ S
N	25.02.1	CRT 4	+ S

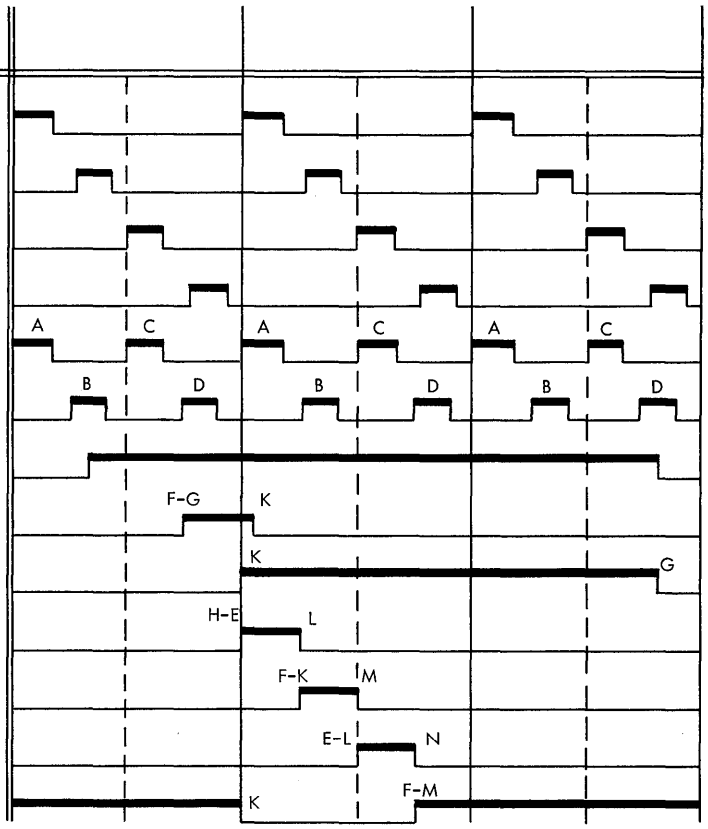


Figure 28. Character Ring Sequence Chart

	Read Or Write	Write Only	Read Only
Start	Gate ON CRT 1	Set C Reg on Write	Set C Reg on Read
CRT 1	Turn OFF Start Turn ON Resp Gate Gate ON CRT 2 Reset AS Reg on ASR 6 Reset End of Word ASR 6	ASR 6 - Turn ON Dem Sync Step Assem Ring Drive	
CRT 2	Gate ON CRT 3 Gate Out AS Ring Drive Turn OFF CRT 1		
CRT 3	Turn OFF CRT 2	Turn ON Write Stop if: AS Ring 1 DR Not Loaded Not Dem Gate	Data Accept Step AS Ring Drive If AS Ring 6 - Turn ON Dem Sync
CRT 4	Gate ON Start Turn OFF CRT 3		Request Failure if: One Start is OFF and Request is UP (Character rate too fast for channel)

Figure 29. Character Ring Functions

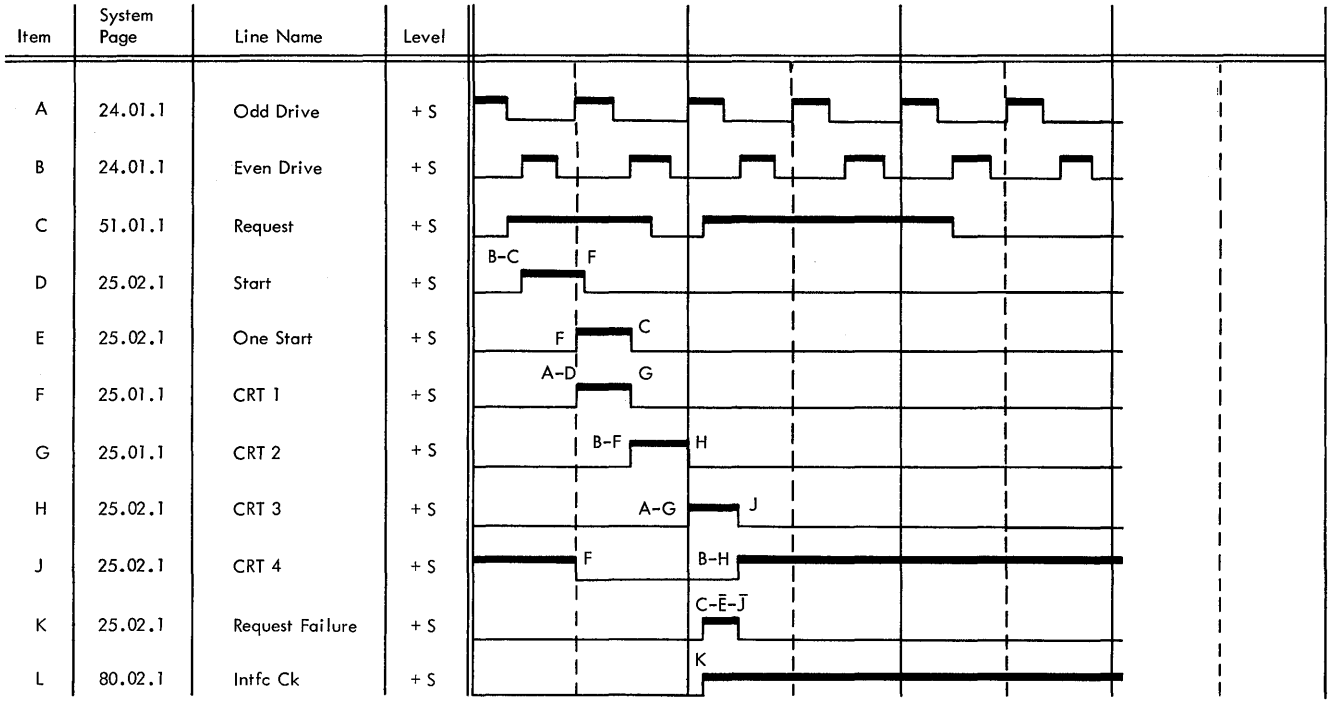


Figure 30. Request Failure Sequence Chart

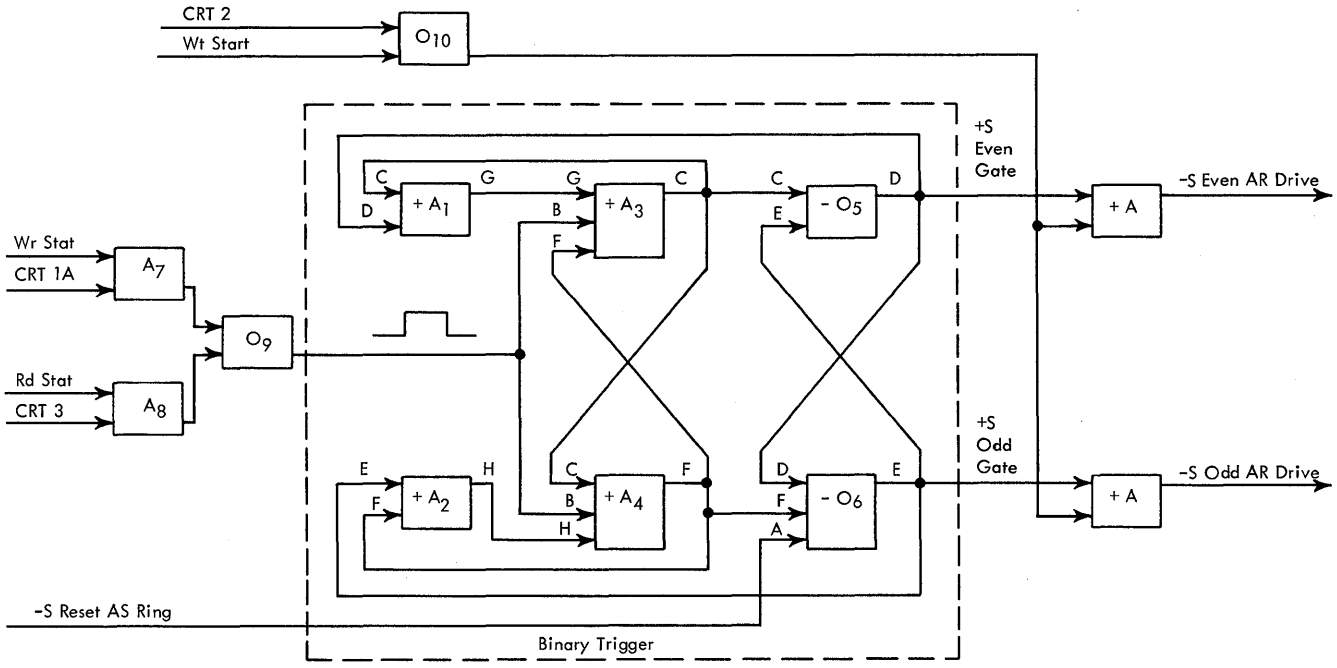


Figure 31. Assembly Ring Drive Circuit (Binary Trigger)

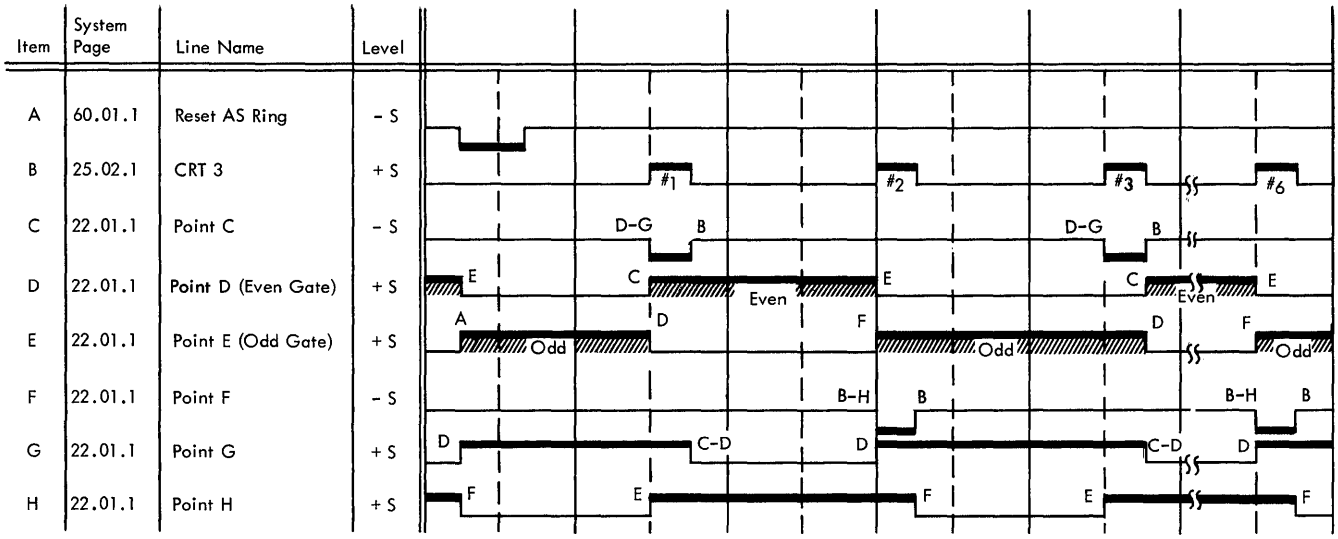


Figure 32. Assembly Ring Drive Trigger Sequence Chart for Read

input drive pulse. In addition, it can be initially reset to the ODD status. O_5 and O_6 are the outputs which indicate the present state of the trigger. Either point D or E will be up at any one time, but not both points. A_3 and A_4 affect the outputs of O_5 and O_6 under control of A_1, and A_2, and the input drive pulse. A_1 and A_2 are essentially gate switching circuits which allow the input drive pulse to alternately affect A_3 and A_4.

When the reset pulse goes minus (−S) at point A, the output of O_6 (point E) rises to +S. This causes the output of O_5 (point D) to go minus because both C and E are at an up level; the trigger is now in the ODD state. From the time that "reset AS ring" goes plus until a new reset is generated, point A has no further effect on the circuit operation and is, therefore, omitted from subsequent discussions.

During the periods when there are no incoming character ring trigger (CRT) drive pulses, points C and F are at a +S level and, therefore, cannot affect either O_5 or O_6. As a result, the trigger continues to maintain its present state.

Assume that the trigger has been reset (as explained above) and is in the OFF (ODD) status. As a result, points E and F are both at +S and fully condition A_2. Point H is minus and blocks A_4. Under the same initial conditions, points C and D are at −S and +S, respectively; the A_1 output, point G, is at a plus level and successfully gates A_3. The next CRT pulse which arrives at the circuit input, therefore, finds A_4 blocked but A_3 receptive. The final result is that point C goes minus for the duration of the pulse, O_5 is impulsed, and point D rises to a +S level indicating an EVEN status. Point D also degates O_6 causing E to go minus, and the trigger has completely reversed status.

The next CRT pulse finds A_3 blocked, but A_4 circuitry is active to condition O_6, and the trigger reverses to its original (ODD) status. The reversing continues with each new CRT pulse or until reset at point A.

ASSEMBLY RING OPERATION

Reset status of the ring (resulting from O_1—Figure 33) is with assembly ring (AR) position 6 on, the remaining trigger positions off, and the assembly ring drive trigger reset to the ODD status.

Each service request from the I-O adapter turns on the character ring start trigger (Figure 27) and produces the necessary CRT1, CRT2, CRT3, and CRT4 pulses to time the data flow. Note (Figure 34 or 35) that CRT2 or "write start" causes the assembly ring drive pulse at A_{10} or A_{11} to step the ring just prior to its use; i.e. first "write start" steps the ring from AR6 to AR1, then "request" causes CRT2 to step it from AR1 to AR2, and so on. Each trigger position when turned on gates the drive circuit for the next trigger in line, and, at the same time, resets the previous position. In this manner, the ring continues to ripple in a closed sequence throughout the entire period of data transmission.

At every CRT1 on write or CRT3 on read the assembly ring drive trigger reverses and is in proper status to step the assembly ring at the next data transfer request.

During normal operations, AR1 gates positions S-5, AR2 gates 6-11, . . . and AR6 gates 30-35. This is accomplished at A_{13}, A_{15}, . . . A_{23} (Figure 33). If the read-backward feature is operative on the channel, characters must be gated into the assembly register in reverse order. The assembly ring continues to step in the normal fashion; however, the assembly ring output lines are gated from the ring triggers in reverse order. For example: "AS ring 6" is produced at A_{22} by the output of AR1.

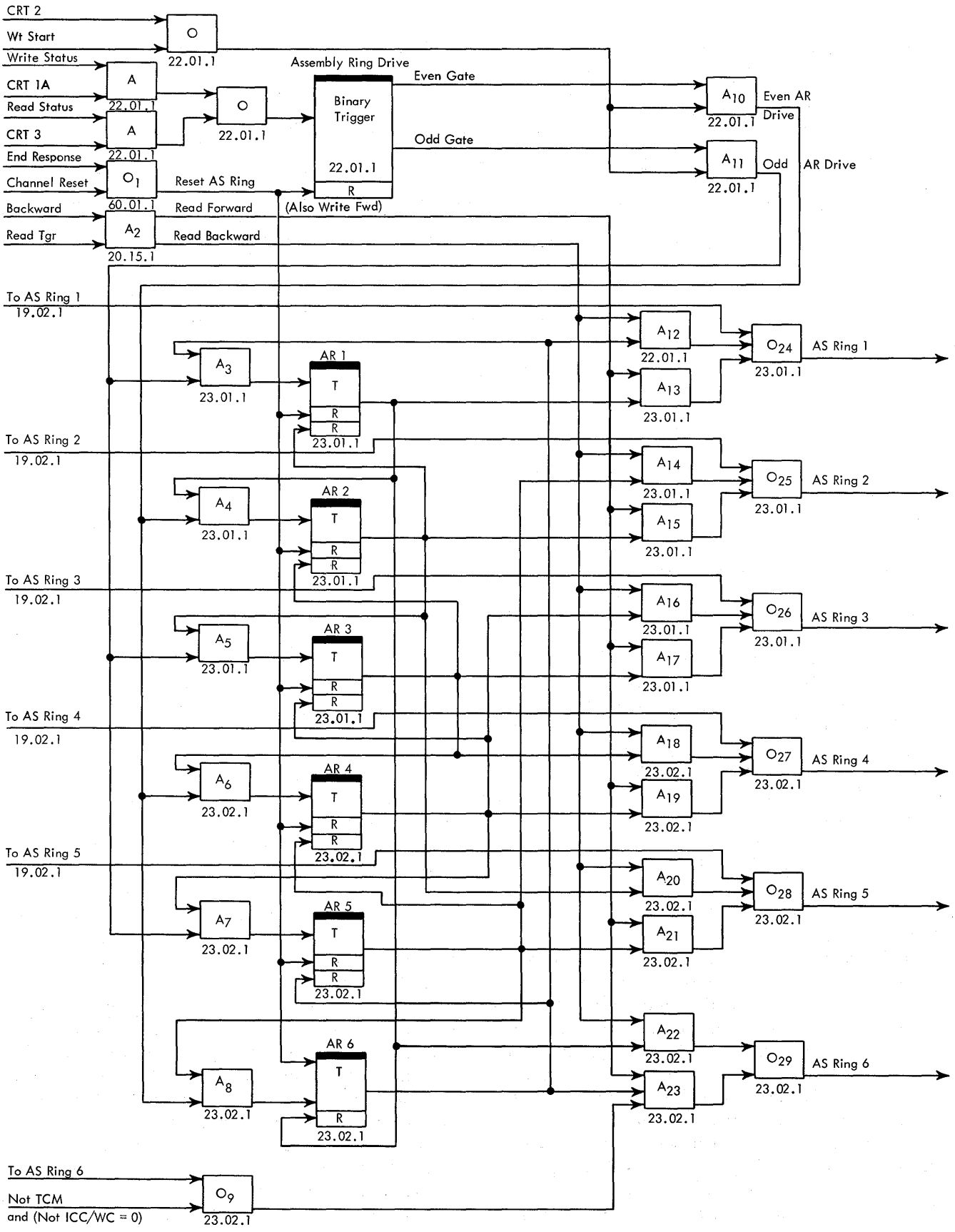


Figure 33. Assembly Ring Condensed Logic

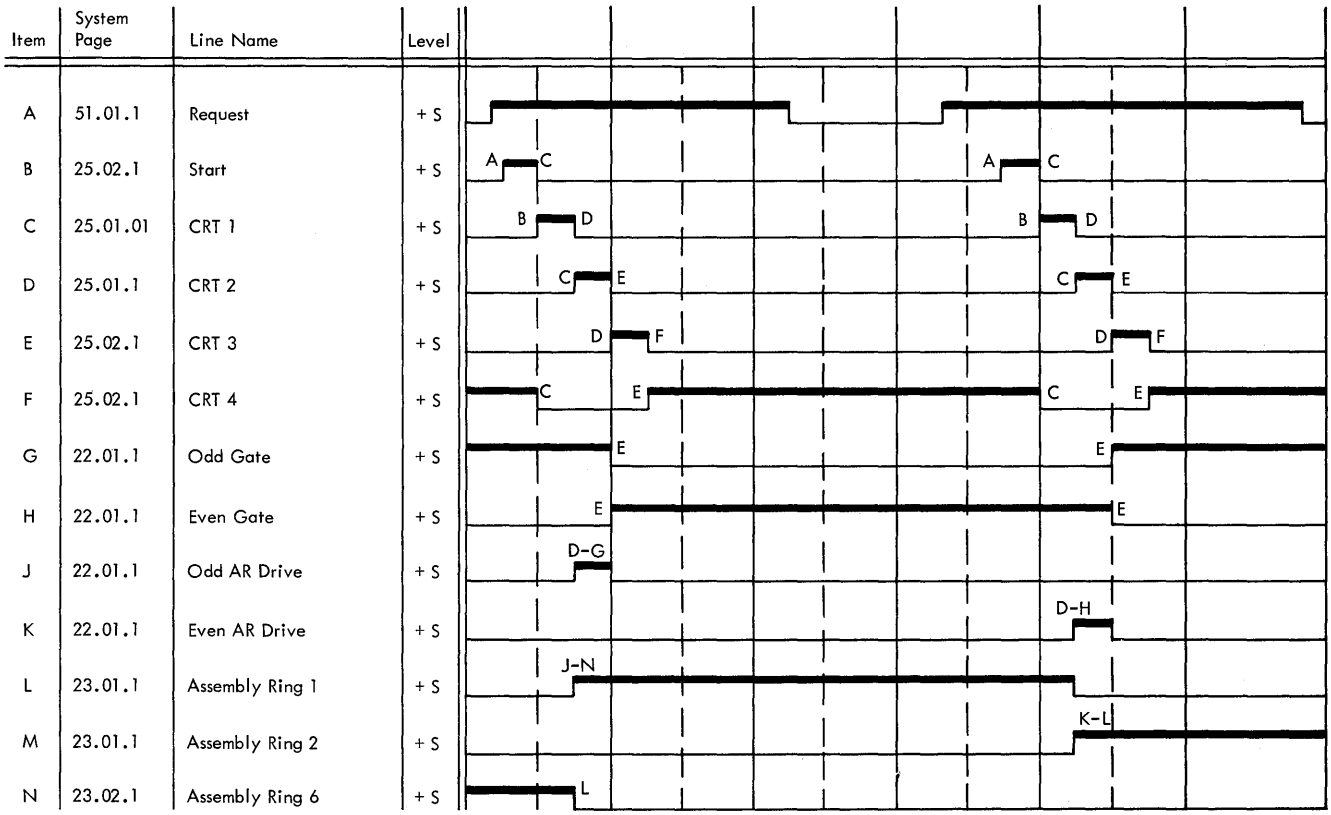


Figure 34. Assembly Ring Sequence Chart For Read

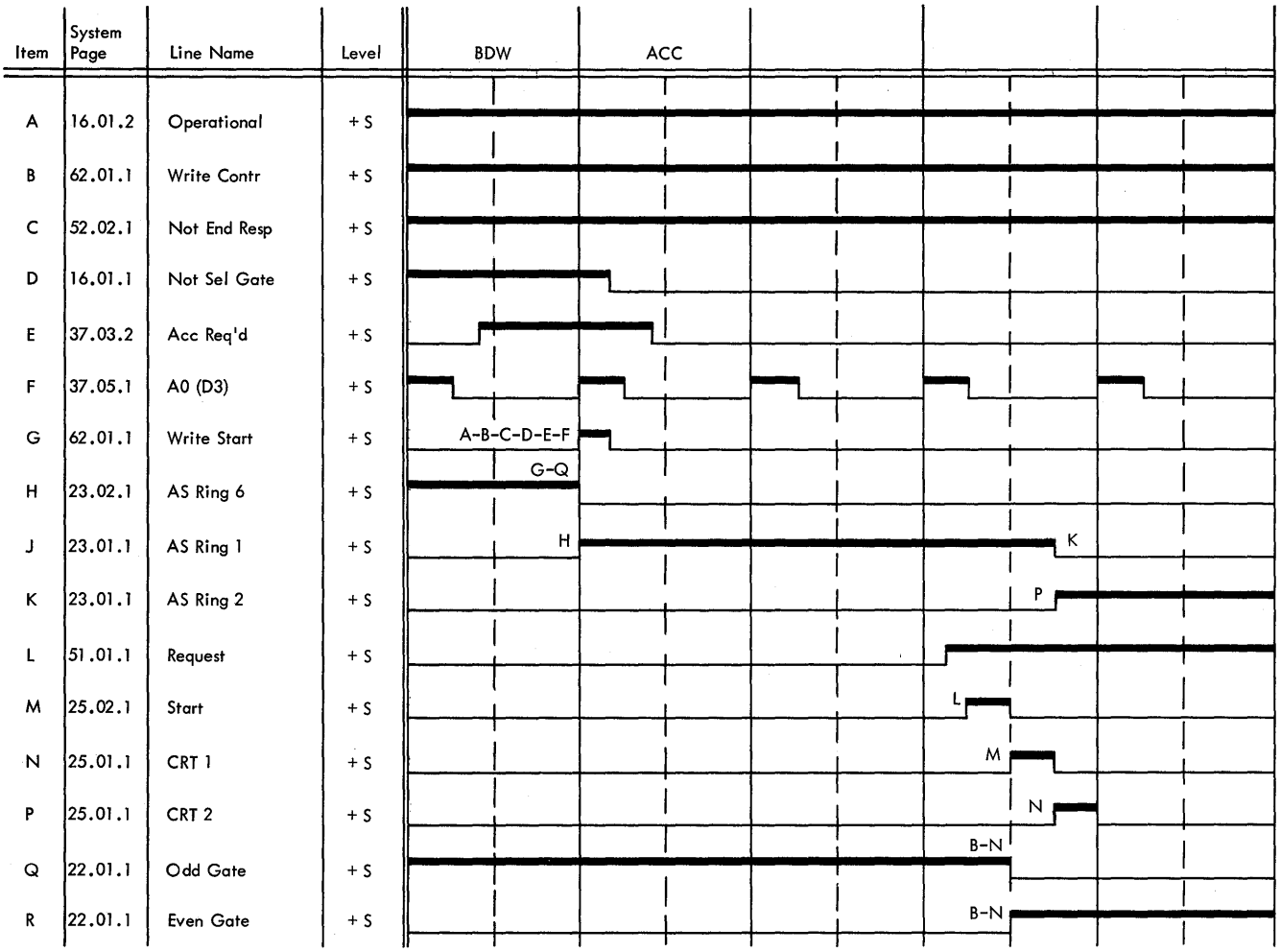


Figure 35. Assembly Ring Sequence Chart For Write

Since the introduction of large scale IBM computer systems, there have been two modes of operation: binary and BCD. Both have advantages. Data outputs from one system, however, must be readily available to another whether or not that second system operates in the same mode. BCD has been established as the common mode of exchange; the responsibility for conversion from BCD to binary and vice versa, therefore, falls on the binary system. As a result, the 7909 channel may contain additional circuits to accomplish this translation for data either arriving at the channel input or data on the way to an attached I-O device.

This BCD translation, performed on both input and output data, is concerned primarily with zoning; AB bit zoning is converted to an A bit, A bit zoning is converted to AB bits, and B bit zoning remains unchanged. In addition, however, certain special configurations are also changed to conform to a new simplex BCD standard as shown in Figure 36.

Core Storage	Simplex BCD
B A 8 4 2 1	B A 8 4 2 1
0 0 0 0 0 0	0 0 1 0 1 0
0 0 1 0 1 0	0 1 0 0 0 0
0 0 Other	0 0 No Change
0 1 Any	1 1 No Change
1 0 Any	1 0 No Change
1 1 0 0 0 0	0 0 0 0 0 0
1 1 Other	0 1 No Change

Figure 36. Simplex BCD Translation

As stipulated in simplex I-O interface standards, the byte parity will always be ODD regardless of binary or BCD mode of operation.

In the tape BCD conversion system there is a shortcoming in that one character, the BCD zero, cannot always be written and later re-read to its original form. Note in Figure 37 that both the 000 000 and 001 010 bit combinations produce the same tape BCD character. At this point there is no way of identifying what the original character was. When either of these tape BCD bit combinations is read into memory, a 000 000 character results and distinction between the two initial characters has been lost. Printers of the 407-type cannot make full use of the 64 possible bit combinations. Therefore, in most previous applications, this did not present problems; the 001 010 was considered an illegal combination of bits for BCD conversion.

Newer system printers and output devices have the ability to utilize the entire 64 possible characters formed by the B-A-8-4-2-1 bit combinations. As a result, the simplex BCD standard was devised to circumvent the short-coming of the tape BCD format just discussed. The changes are minor, but significant, and are summarized in Figure 36.

The 7909 Data Channel provides only simplex BCD conversion; for comparison purposes, however, a complete conversion chart for both simplex and tape BCD translation is shown in Figure 37.

Translators

Write Translators

The write translator circuitry is installed with the BCD optional feature. The function is to translate characters from the assembly register into simplex BCD format before sending them to the character register for transmission to the I-O adapter. If BCD mode is not specified, the translators have no effect and the character arrives at the write bus unaltered. The translators are not active during the transfer of control data.

Write Translation

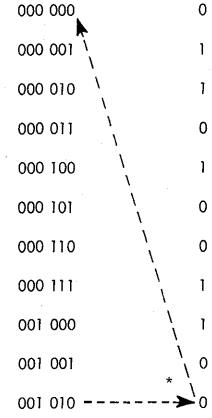
Write translation (Figures 38 and 39) requires that the B, A, 8, and 2 bit lines be broken and modified by the translator circuitry. As an example, the "8 data line out" between O_3 and A_{10} (Figure 38) is broken at the dotted area and wired to the translator. The 4 bit and 1 bit circuits must feed the translator but the direct lines from O_4 to A_{11} and O_6 to A_{13} remain intact. (See Figure 79 for comparison of circuitry without BCD translator.)

Translation must begin as soon as possible because of the transition time necessary for the output lines to reach their proper levels. The character to be translated from the assembly register is available as soon as the assembly ring is advanced by the I-O service request. At CRT3 time, the translator outputs are valid and gated to the character register by the set C register on write line.

Read Translators

This translator circuitry is installed with the BCD optional feature. The function is to analyze simplex BCD characters as they arrive at the input read bus and

Core Storage Character	Tape BCD C BA8 421	Simplex BCD C BA8 421	Character BCD	IBM Card Code	Core Storage Character	Tape BCD C BA8 421	Simplex BCD C BA8 421	Character BCD	IBM Card Code
101 011	0 101 011	1 101 011	$	11-8-3	001 011	1 001 011	0 001 011	=	8-3
101 100	1 101 100	0 101 100	*	11-8-4	001 100	0 001 100	1 001 100	'	8-4
101 101	0 101 101	1 101 101	]	11-8-5	001 101	1 001 101	0 001 101	:	8-5
101 110	0 101 110	1 101 110	;	11-8-6	001 110	1 001 110	0 001 110	>	8-6
101 111	1 101 111	0 101 111	△	11-8-7	001 111	0 001 111	1 001 111	√	8-7
110 000	1 010 000	1 000 000	BLK	No Punch	010 000	0 110 000	1 110 000	+	12
110 001	0 010 001	1 010 001	/	0-1	010 001	1 110 001	0 110 001	A	12-1
110 010	0 010 010	1 010 010	S	0-2	010 010	1 110 010	0 110 010	B	12-2
110 011	1 010 011	0 010 011	T	0-3	010 011	0 110 011	1 110 011	C	12-3
110 100	0 010 100	1 010 100	U	0-4	010 100	1 110 100	0 110 100	D	12-4
110 101	1 010 101	0 010 101	V	0-5	010 101	0 110 101	1 110 101	E	12-5
110 110	1 010 110	0 010 110	W	0-6	010 110	0 110 110	1 110 110	F	12-6
110 111	0 010 111	1 010 111	X	0-7	010 111	1 110 111	0 110 111	G	12-7
111 000	0 011 000	1 011 000	Y	0-8	011 000	1 111 000	0 111 000	H	12-8
111 001	1 011 001	0 011 001	Z	0-9	011 001	0 111 001	1 111 001	I	12-9
111 010	1 011 010	0 011 010	ǂ	0-8-2	011 010	0 111 010	1 111 010	?	12-0
111 011	0 011 011	1 011 011	,	0-8-3	011 011	1 111 011	0 111 011	.	12-8-3
111 100	1 011 100	0 011 100	(	0-8-4	011 100	0 111 100	1 111 100	)	12-8-4
111 101	0 011 101	1 011 101	ϒ	0-8-5	011 101	1 111 101	0 111 101	[	12-8-5
111 110	0 011 110	1 011 110	\	0-8-6	011 110	1 111 110	0 111 110	<	12-8-6
111 111	1 011 111	0 011 111	+++	0-8-7	011 111	0 111 111	1 111 111	ǂ	12-8-7
000 000	0 001 010	1 001 010	0	0	100 000	1 100 000	0 100 000	-	11
000 001	1 000 001	0 000 001	1	1	100 001	0 100 001	1 100 001	J	11-1
000 010	1 000 010	0 000 010	2	2	100 010	0 100 010	1 100 010	K	11-2
000 011	0 000 011	1 000 011	3	3	100 011	1 100 011	0 100 011	L	11-3
000 100	1 000 100	0 000 100	4	4	100 100	0 100 100	1 100 100	M	11-4
000 101	0 000 101	1 000 101	5	5	100 101	1 100 101	0 100 101	N	11-5
000 110	0 000 110	1 000 110	6	6	100 110	1 100 110	0 100 110	O	11-6
000 111	1 000 111	0 000 111	7	7	100 111	0 100 111	1 100 111	P	11-7
001 000	1 001 000	0 001 000	8	8	101 000	0 101 000	1 101 000	Q	11-8
001 001	0 001 001	1 001 001	9	9	101 001	1 101 001	0 101 001	R	11-9
001 010 *	0 001 010	0 010 000	⁂	8-2	101 010	1 101 010	0 101 010	!	11-0



* See text for this conversion

Figure 37. Character Coding and Translations

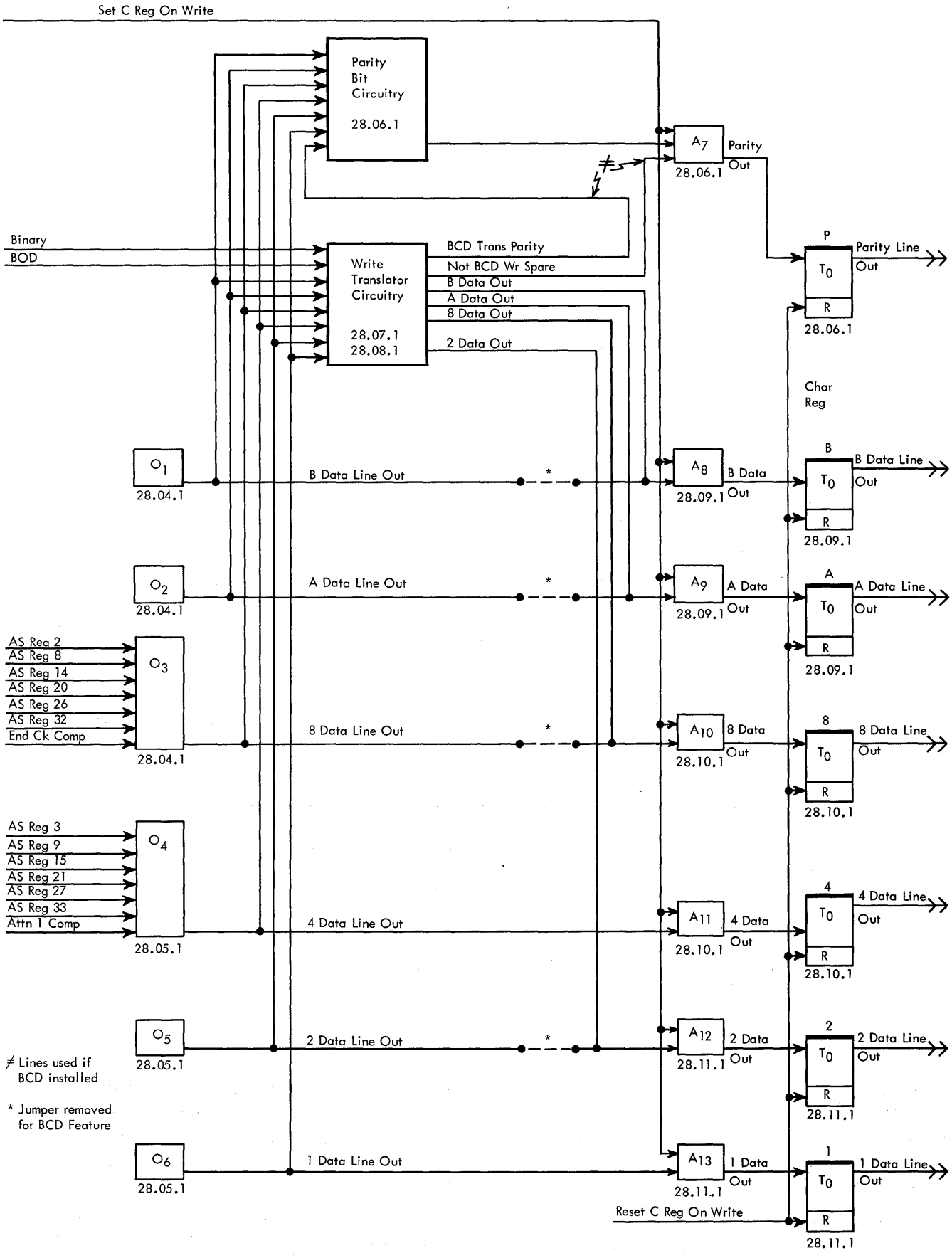
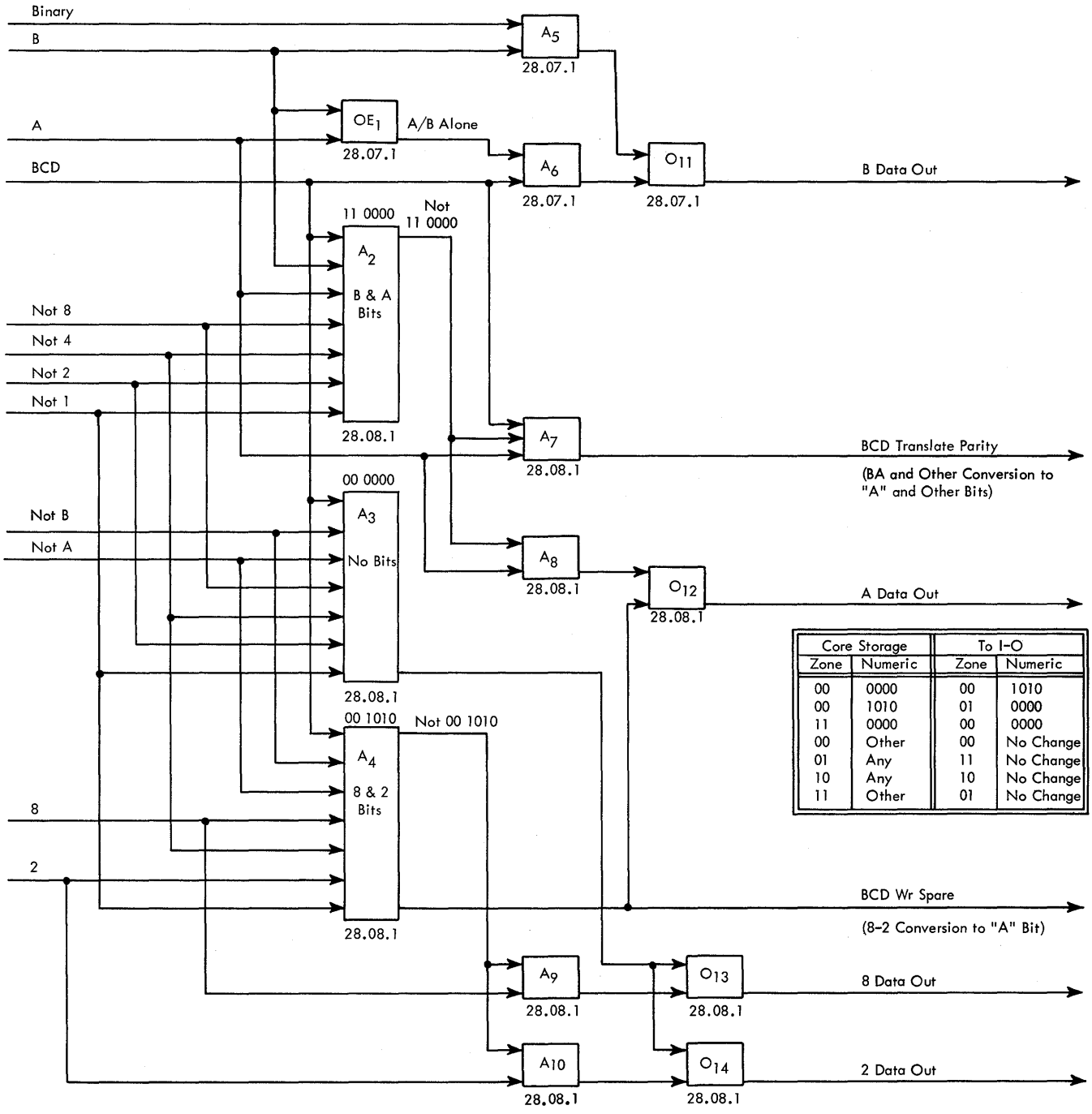


Figure 38. Write BCD Translation



Core Storage		To I-O	
Zone	Numeric	Zone	Numeric
00	0000	00	1010
00	1010	01	0000
11	0000	00	0000
00	Other	00	No Change
01	Any	11	No Change
10	Any	10	No Change
11	Other	01	No Change

Figure 39. Write BCD Translator

translate them into the correct computer core storage code. If BCD mode is not specified, the translators have no effect and the character arrives at the assembly register unaltered. The translators are not active during the transfer of sense data.

Read Translation (Figures 40 and 41)

Without BCD mode, the input data (for a B bit) are fed directly from the character register to A_{19} (Figure 40). When the BCD optional feature is installed, however, these direct lines are broken and the translator circuitry is inserted (see Figure 79 for comparison). Note that only the B, A, 8, and 2 bit lines require conversion. Even though the 4 bit and 1 bit conditions are required in the translator, their input paths remain unbroken from character register 4 to A_{22} and character register 1 to A_{24}, respectively.

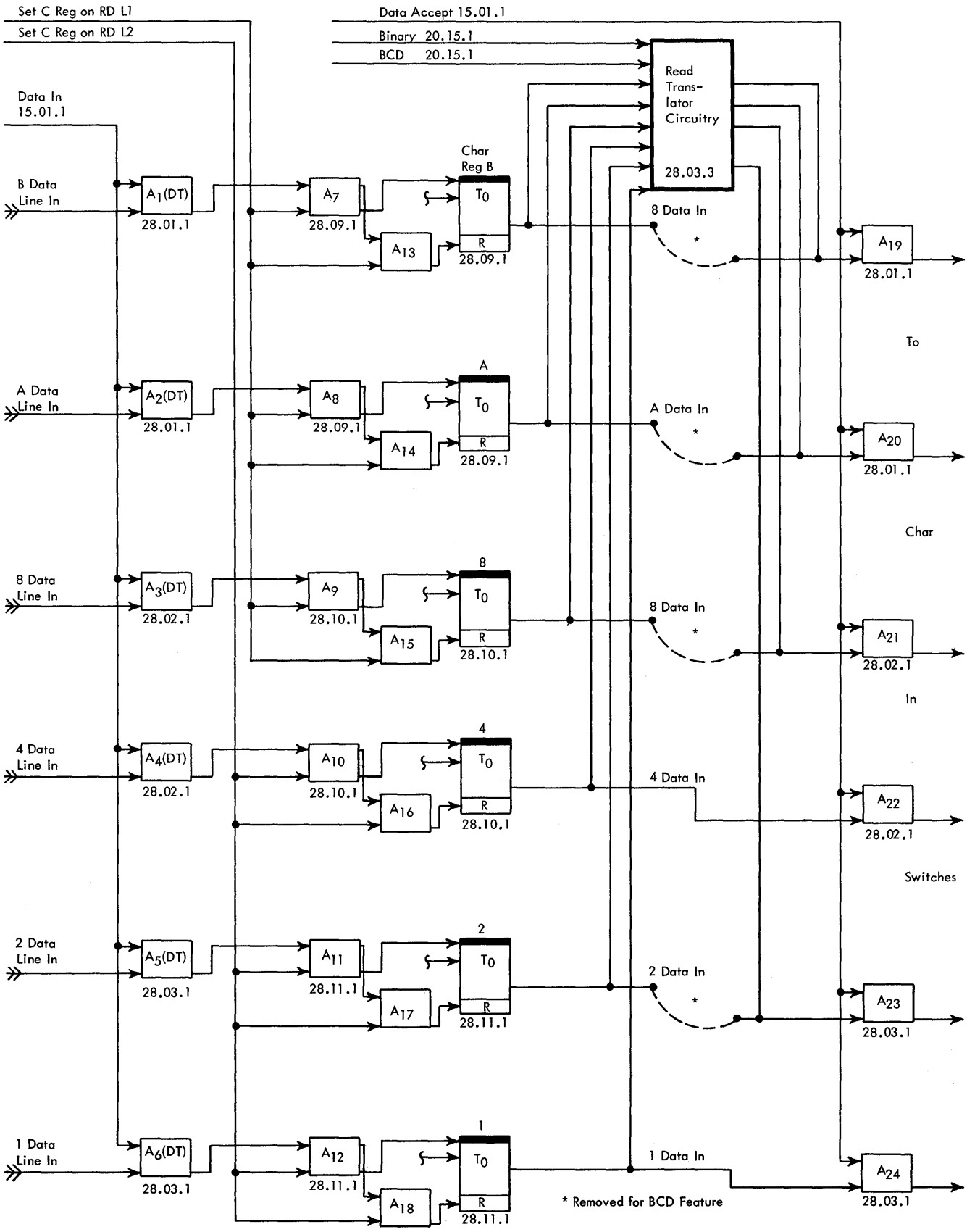


Figure 40. Read Simplex BCD Translation

Inputs from the adapter are gated to the character register through AND circuits 1-6 by "data in" and through AND circuits 7-12 by "set C register on read."

Translator circuits require transition time for the final outputs to reach their correct values; by CRT3 time of a service request, the outputs are valid and gated to the assembly register by "data accept."

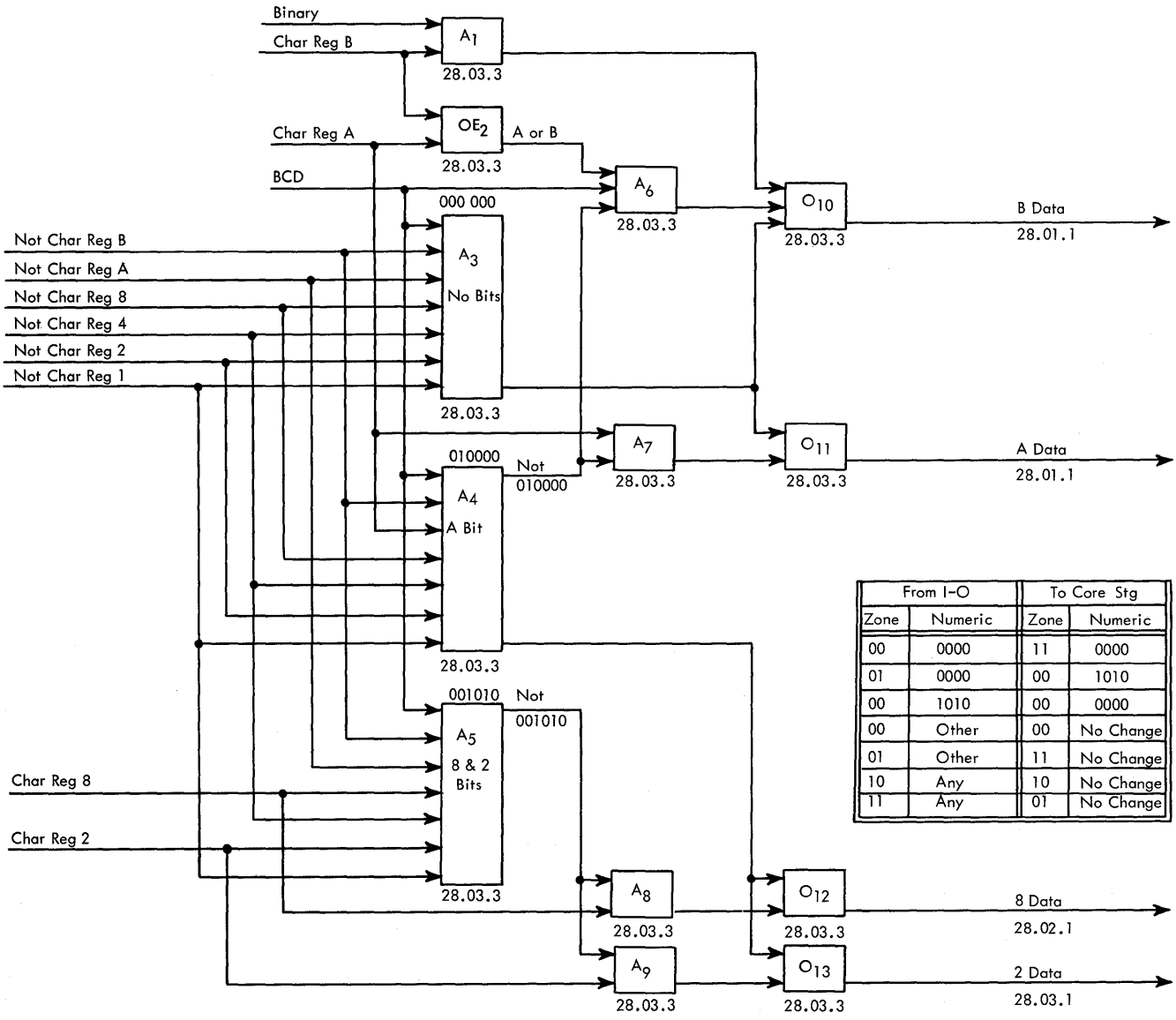
If the channel is operating in binary mode, the translators have no logical effect on the character and the bit configuration arrives at the assembly registers exactly as received on the read bus. Note that even though odd parity is sent by the I-O adapter, no attempt is made to check the validity of the input character.

Parity Bit Generation

Simplex I-O interface standards specify odd bit redundancy for either binary or BCD mode of operation. Parity bit generation (Figures 38, 39 and 42) therefore, consists essentially of counting the bits; if the count is even, generate a parity bit for the write bus; if odd, suppress a parity output.

This counting is accomplished by two EXCLUSIVE OR circuits (Figure 42) which begin operation at the same time that the character is initially available and fed to the character register. Note that the bit count is of the character *before* translation. OE_1 counts the 1, 2, 4, 8 bits and feeds OE_2 where the A and B bits are added. "BCD trans parity" is inserted at OE_2 to compensate for the case where the translator determines that an AB zone bit combination is being converted to an A bit as for example in the characters /, S-Z, and some special characters.

One other combination also occurs where the number of bits is changed by the translator; this is the conversion of an 8-2 bit to an A bit. The parity circuitry (OE_1 and OE_2) detects an even count and generates a parity output. However, in this special case, A_3 is blocked by "BCD write spare," the character register P trigger is not set ON, and the A bit alone is sent to the I-O adapter.



From I-O		To Core Stg	
Zone	Numeric	Zone	Numeric
00	0000	11	0000
01	0000	00	1010
00	1010	00	0000
00	Other	00	No Change
01	Other	11	No Change
10	Any	10	No Change
11	Any	01	No Change

Figure 41. Read BCD Translator

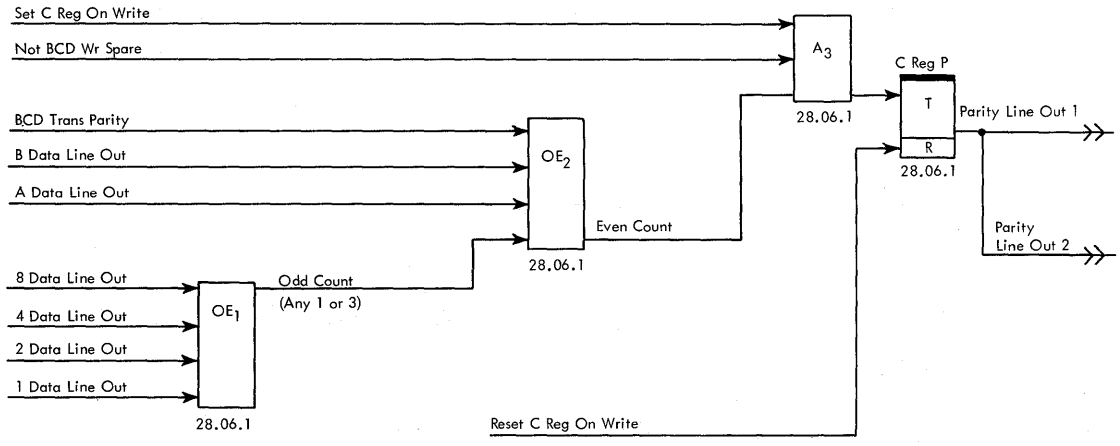


Figure 42. Parity Bit Generator

The instruction format is the same as that contained in the Reference Manual, *IBM 7090 Data Processing System,* Form A22-6528. Symbols used are:

C = Count Field
F = Indirect Addressing Flag
T = Index Register Tag
Y = Address Field

Reset and Start Channel—RSCA

Cyclic Makeup: I - L - E(ECW) - I(CCC) - CMMD

On execution of this instruction (Figures 43 and 44), the channel is selected and reset and takes its next command from location Y. The instruction is interlocked against channel activity. If the instruction is executed while the channel is busy, its execution is delayed until the channel is in WAIT status.

Instruction codes for other channels are:

−0540	RSCB—Reset and Start Channel B
+0541	RSCC—Reset and Start Channel C
−0541	RSCD—Reset and Start Channel D
+0542	RSCE—Reset and Start Channel E
−0542	RSCF—Reset and Start Channel F
+0543	RSCG—Reset and Start Channel G
−0543	RSCH—Reset and Start Channel H

Operation

The reset and start channel instruction takes the channel out of wait status and starts it in operation by loading the command specified by positions 21-35 of the RSC.

At 7 time of the I cycle "POD 54," "PR-7," and "select channel X" are sent from the computer to the various channels. The unique line is "select channel" which is specifically decoded for the intended channel (e.g., select channel A).

The following L cycle tests the status of the channel's wait trigger. If the channel is not in wait status, the computer hangs in L-time at this point until the channel has finished operation. Execution of a WTR or TWT command turns on the wait trigger and allows a proceed to E signal to be returned to the computer. During this last L cycle, the channel command counter is reset and made ready to receive the new address during the early part of the following E cycle.

The computer proceeds to an E cycle and a core storage reference is made to the location specified in positions 21-35 of the RSC instruction. This location contains the command which is to be loaded into the channel and executed. During the early portion of this E cycle, MAR contains the core storage address. An A0(D3) pulse in the channel samples the MAR contents and places the contents into the command counter so that the channel can proceed sequentially from this new address. In most respects, this E cycle functions like the BCW cycle, used to step sequentially through the channel program. The operation register, word counter, and address counter are reset at E2(D4) and set again to new values from the storage bus at 7 time, and a command counter cycle is requested.

The wait trigger is reset at E8 time and "channel in use" is sent back to the computer. At the same time, the trap sync trigger is reset to prevent trapping if the channel had gone into wait status because of a TWT command. The RSC instruction also forces a "check reset" during the E cycle to reset the check condition register.

E time causes the computer to end operation and proceed to the next I cycle. The channel's next cycle is a command counter cycle (CCC) followed by a CMMD cycle, and the new command is executed in a normal manner.

7090 COMPATABILITY MODIFICATION

A 7909 channel attached to a 7090 system requires a slight modification to the 7090 B time circuitry. A 7607 reset and load instruction (+0540) always executes immediately with an I-L-E cycle and makes no provision for servicing B-time requests during L time. A 7909 reset and start instruction (+0540) can hang in L cycles for a time, dependent on channel activity. The circuit modification now allows B time to occur during the L time of a primary op 54 instruction.

Start Channel—STCA

Cyclic Makeup: I - L - E - BCW - CCC - CMMD

Execution of this instruction (Figures 43 and 45) is delayed if the channel is not in wait status. If in wait

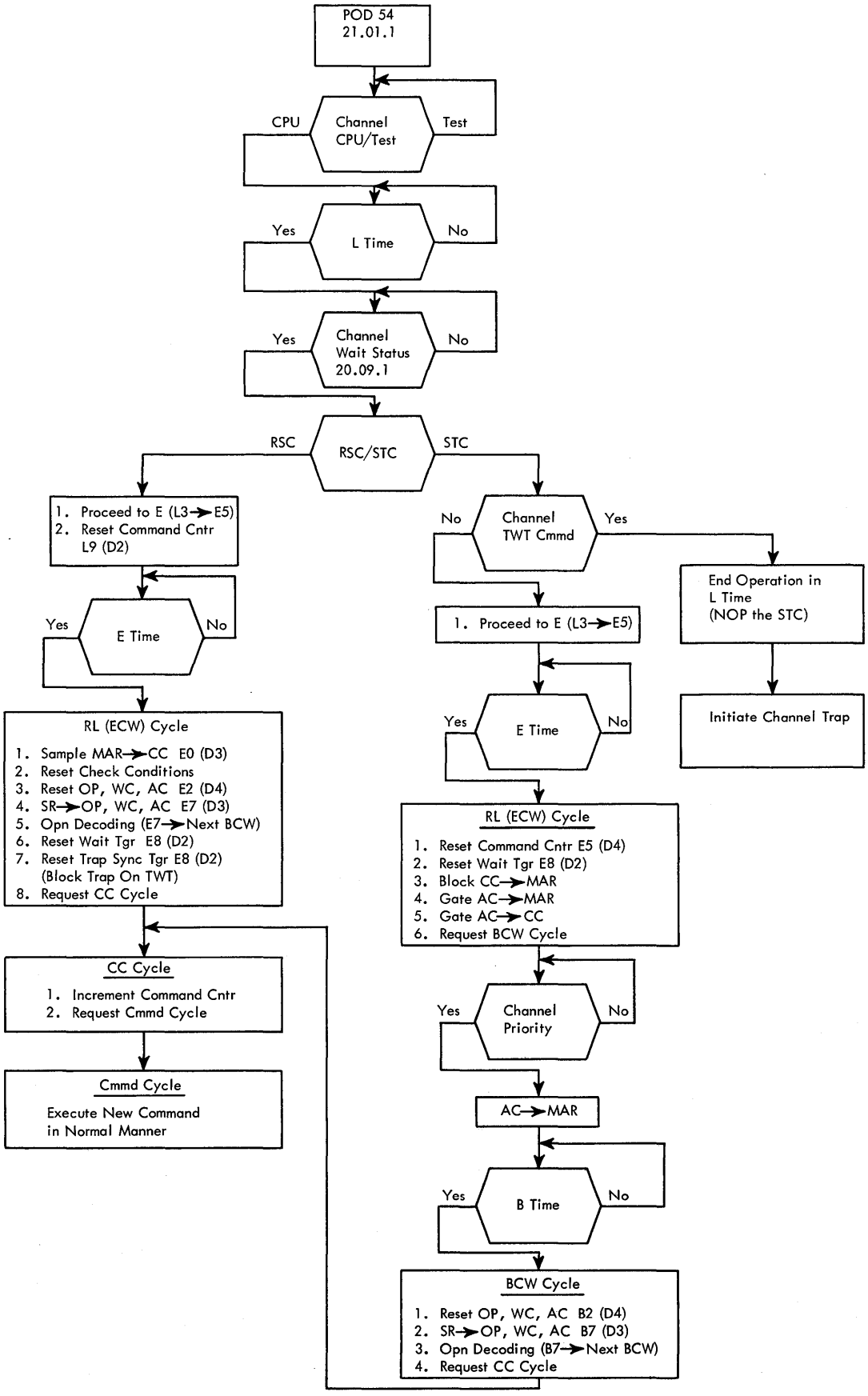


Figure 43. RSC/STC Flow Chart

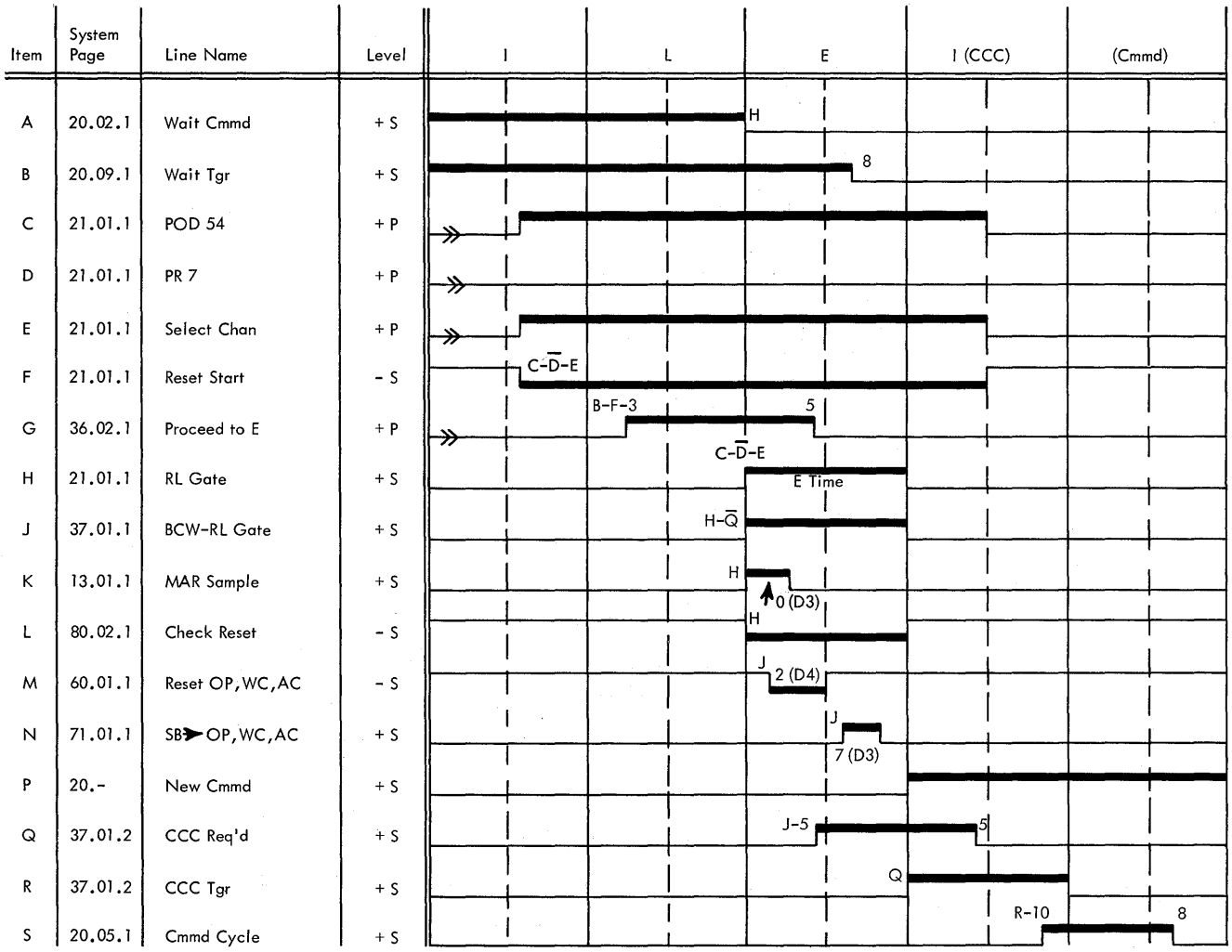


Figure 44. RSC Sequence Chart

status, the channel is started and takes its next command from the address part of the wait command.

Instruction codes for other channels are:

−0544	STCB—Start Channel B
+0545	STCC—Start Channel C
−0545	STCD—Start Channel D
+0546	STCE—Start Channel E
−0546	STCF—Start Channel F
+0547	STCG—Start Channel G
−0547	STCH—Start Channel H

Operation

At 7 time of the I cycle "POD 54," "PR 7," and "select channel X" are sent from the computer to the various channels. "Select channel" is the one line which is decoded in the computer for a specific channel (e.g., select channel A).

The following L cycle tests the status of the channel's wait trigger. If the channel is not in wait status, the computer hangs in L time at this point until the channel has finished operation. Execution of a TWT command turns on the wait trigger, placing the channel in wait status; if the channel is enabled for CW traps, an I-O end operation signal is returned to the computer and the STC instruction is effectively NO-OP'ed by ending operation in L time. The computer proceeds to I time and a channel trap is initiated.

Execution of a WTR command or a TWT command with the channel not enabled for CW traps also turns on the wait trigger and sends a proceed to E signal to the computer. E time of the STC resets the wait trigger at 8 time, resets the command counter at E5(D4), gates the address counter to the command counter and MAR, and requests a BCW cycle. The trap sync trigger is also reset at 8 time of this E cycle. (This trigger would be on if a TWT command had just been executed with the channel disabled for CW traps.) E time causes the computer to end operation through normal circuitry and proceed to the next instruction.

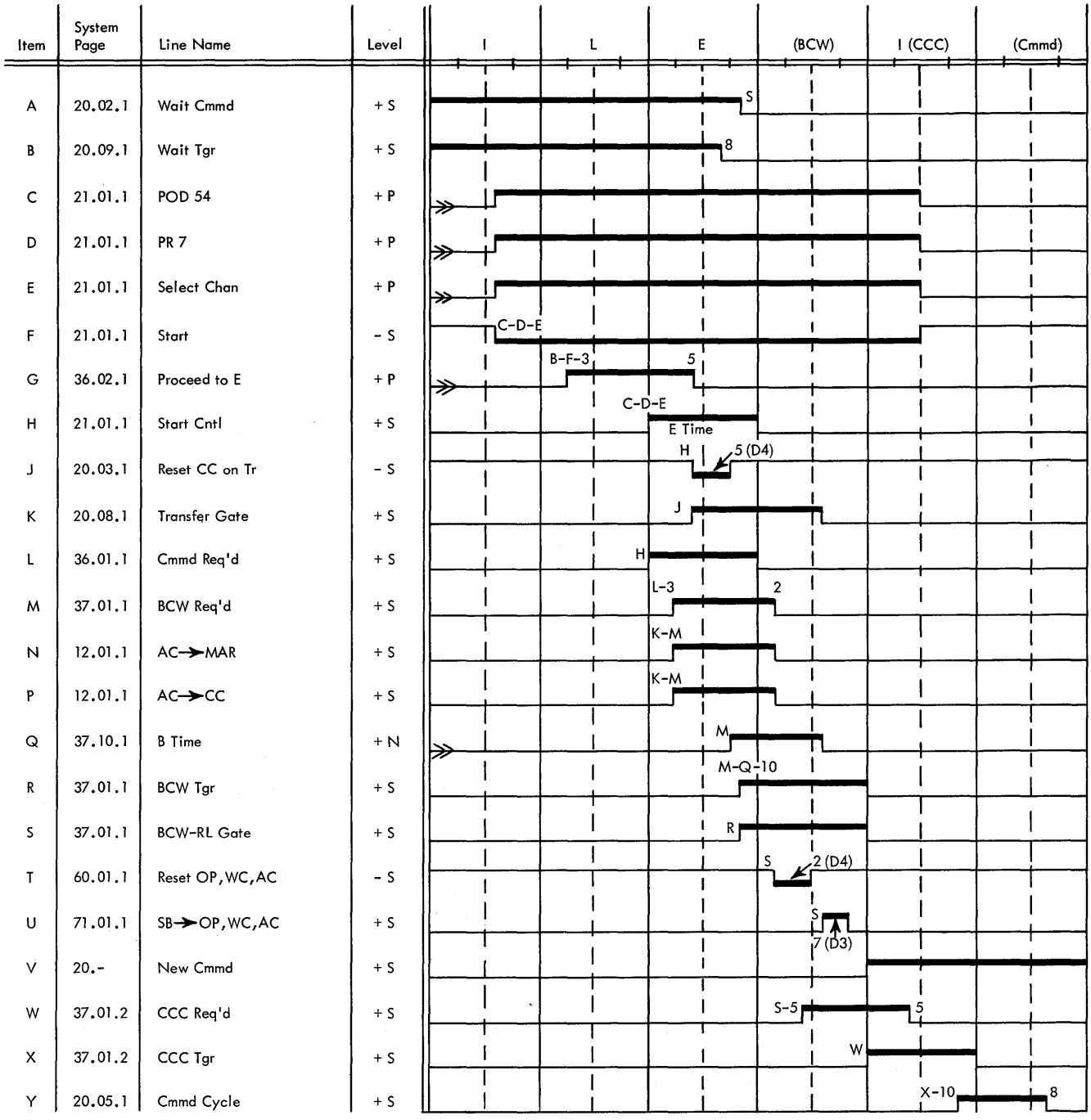


Figure 45. STC Sequence Chart

The BCW cycle is obtained through normal priority and B time circuitry. During this cycle the operation register, word counter, and address counter are reset at B2(D4) and set again with the new command from the storage bus at 7 time. The following cycle (CCC) increments the command counter and initiates a CMMD cycle. During the command cycle the new command is executed in a normal manner.

Store Channel—SCHA

Cyclic Makeup: I - E

Execution of this instruction (Figures 46 and 47) causes

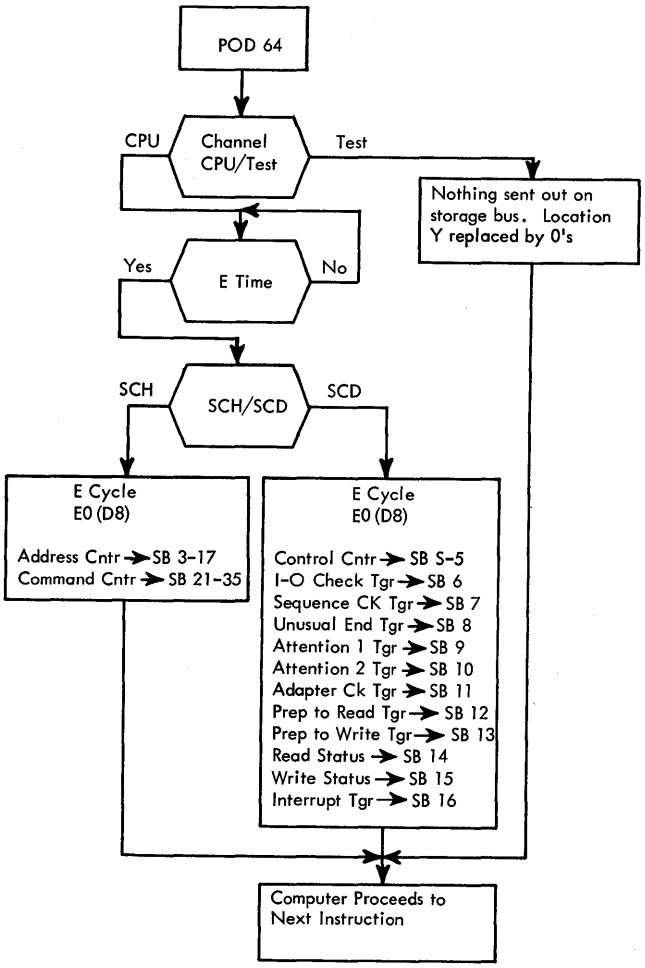


Figure 46. SCH/SCD Flow Chart

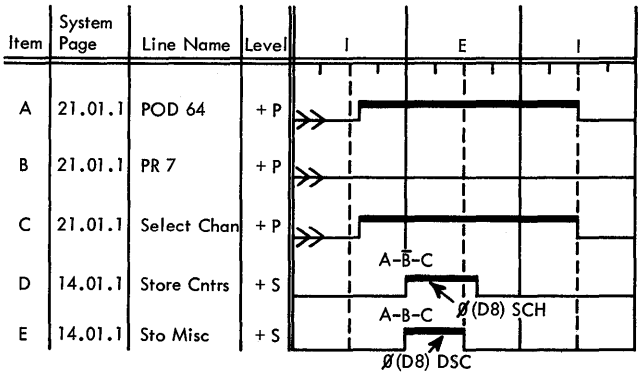


Figure 47. SCH/SCD Sequence Chart

the specified channel to be selected and that channel's command counter to be placed in positions 21-35 of location Y. The channel's address counter contents are placed in positions 3-17 of location Y. Positions S, 1, 2, 18, 19, and 20 of location Y are cleared.

Instruction codes for other channels are:

−0640	SCHB—Store Channel B
+0641	SCHC—Store Channel C
−0641	SCHD—Store Channel D
+0642	SCHE—Store Channel E
−0642	SCHF—Store Channel F
+0643	SCHG—Store Channel G
−0643	SCHH—Store Channel H

The store channel instruction samples the channel's address counter and command counter concurrently with channel operations. The A0(D8) sample pulse occurs at a time when the counters are not being changed. The value of the command counter is dependent on which channel cycle is functioning at the time of the SCH and may be the address of the command being executed, the next sequential address, or the address of a successful transfer.

Store Channel Diagnostic—SCDA

Cyclic Makeup: I - E

The store channel diagnostic instruction (Figures 46 and 47) samples the contents of the control counter and eleven status conditions of the machine and stores their indications in positions S-16 of location Y. This sampling is done concurrently with channel operations and does not affect the operations in any way.

Instruction codes for other channels are:

−0644	SCDB—Store Channel Diagnostic B
+0645	SCDC—Store Channel Diagnostic C
−0645	SCDD—Store Channel Diagnostic D
+0646	SCDE—Store Channel Diagnostic E
−0646	SCDF—Store Channel Diagnostic F
+0647	SCDG—Store Channel Diagnostic G
−0647	SCDH—Store Channel Diagnostic H

Execution of this instruction causes the specified channel to be selected; the contents of location Y are replaced by bits to indicate the status of the following channel triggers:

Channel Trigger	Location	
Control Counter 1-6	S-5	
I-O Check	6	Check Condition Register
Sequence Check	7	
Unusual End	8	
Attention 1	9	
Attention 2	10	
Adapter (Interface) Check	11	
Prepare to Read	12	SCD Status Register
Prepare to Write	13	
Read Status	14	
Write Status	15	
Interrupt	16	

The contents of positions 17-35 cannot be guaranteed.

Enable—ENB

Cyclic Makeup: I - E

When this instruction (Figures 48 and 49) is executed, the contents of location Y determine if a trap and wait (TWT) command may cause a trap operation. Execution of each enable instruction cancels the effect of a previous enable instruction. A channel may be disabled (traps will not occur) by executing an enable instruction whose operand contains a zero in the proper position.

Trapping signals are controlled as follows:

Signal Due to	Channel	Effective if a 1 in Position
Trap and Wait Command	A	35
	B	34
	C	33
	D	32
	E	31
	F	30
	G	29
	H	28

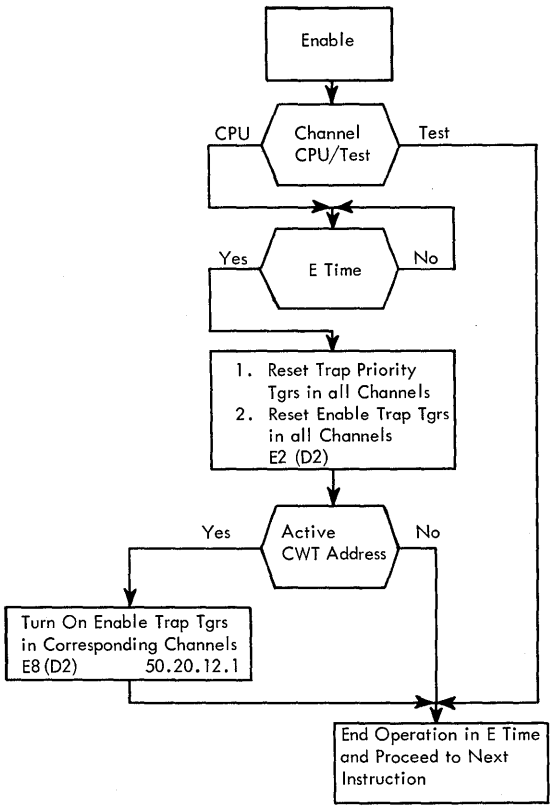


Figure 48. Enable Flow Chart

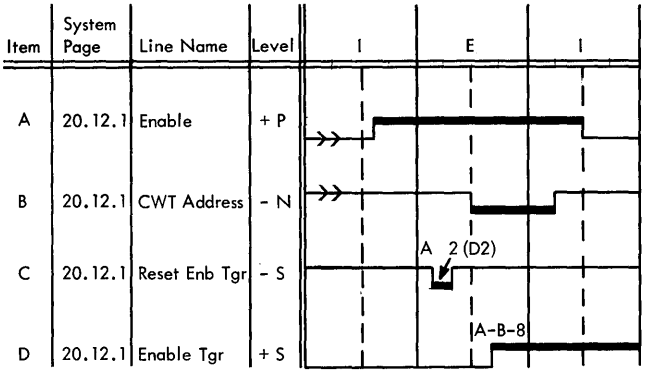


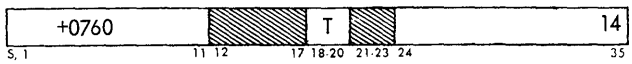
Figure 49. Enable Sequence Chart

Execution of a trap inhibits all further traps until a new enable instruction is executed or a restore channel trap instruction is executed. Depression of the reset or clear key or execution of a reset channel (RIC) instruction also disables the data channel.

This instruction can occur simultaneously with channel operations. "Enable" is sent to all channels at I7 time; the channel CW trap addresses are detected in the multiplexor and sent to the corresponding channels at approximately E6 time. Early in the E cycle (2 time) the enable trap triggers for all channels are reset; at 8 time all enable trap triggers are turned on where there is a corresponding address from the multiplexor. At 8 time, therefore, all channels with an active address are enabled; those with no active address are disabled.

If the trap sync trigger is on (50.20.12.1) as the result of a TWT command, the channel immediately begins trapping procedures.

Restore Channel Traps—RCT



Cyclic Makeup: I - L

The restore channel trap instruction (Figures 50 and 51) allows traps to occur as specified by the previous enable instruction. Since the address portion of this instruction is part of the operation code, modification by an index register may change the operation.

The computer's restore trigger (Figure 50) is turned on with an enable instruction and is turned off when a trap or an interlock reset occurs. Other traps are inhibited at A_2 until the restore trigger is turned on again by the restore channel trap or other enable instruction.

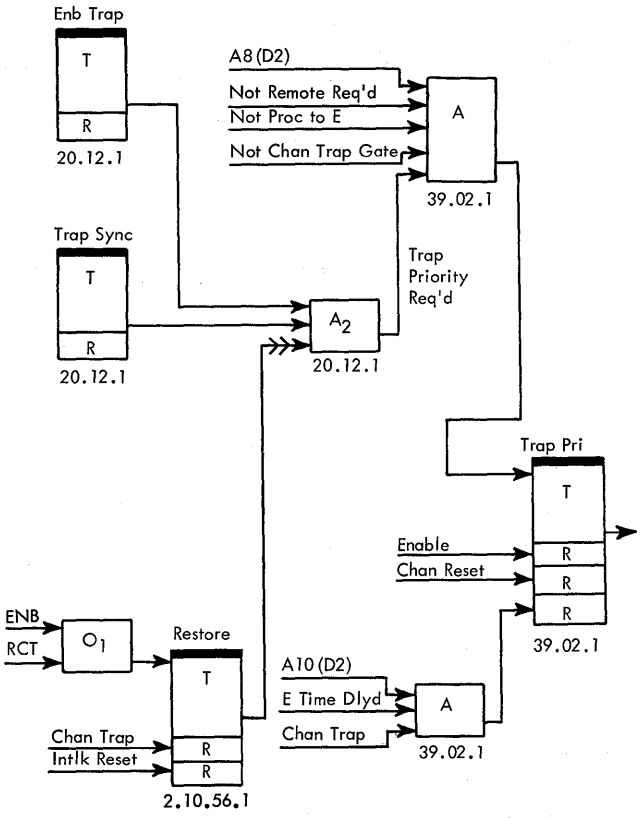


Figure 50. Restore Channel Trap Condensed Logic

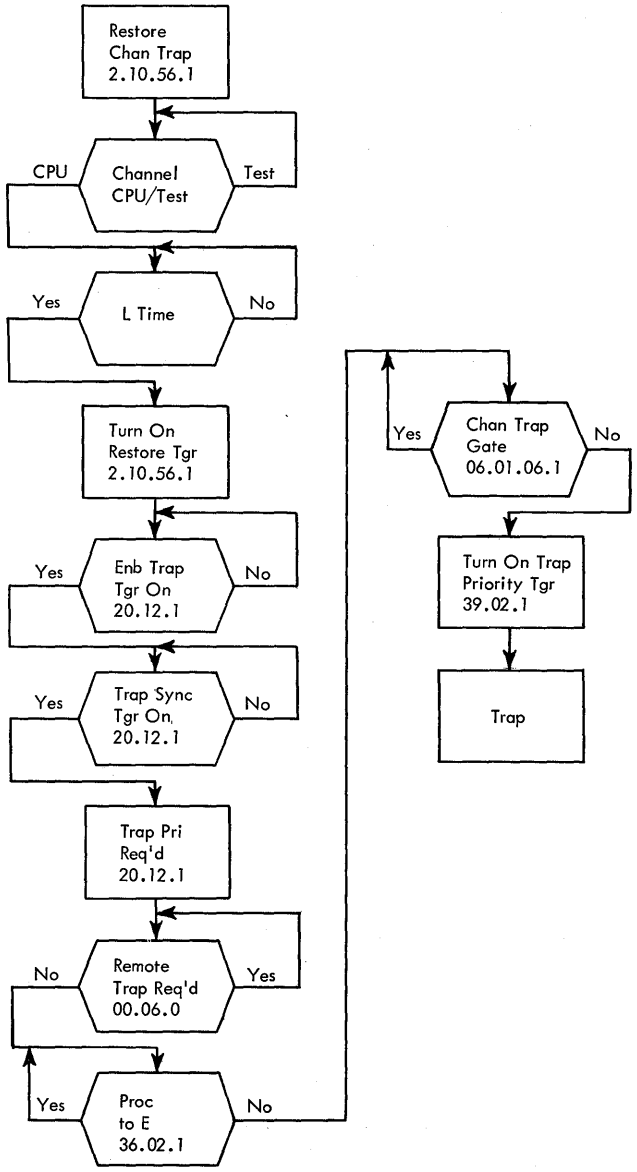
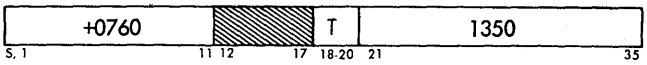


Figure 51. Restore Channel Trap Flow Chart

Reset Channel—RICA



Cyclic Makeup: I - L

The RIC (Figures 52 and 53) resets all conditions in the channel to normal initial status and also sends a reset pulse to the I-O adapter. The instruction is not interlocked against channel activity. If data transmission is taking place when an RIC occurs, validity of the data already transmitted cannot be guaranteed.

Instruction codes for the other channels are:

+0760-2350	RICB—Reset Channel B
+0760-3350	RICC—Reset Channel C
+0760-4350	RICD—Reset Channel D
+0760-5350	RICE—Reset Channel E
+0760-6350	RICF—Reset Channel F
+0760-7350	RICG—Reset Channel G
+0760-10350	RICH—Reset Channel H

The execution of this instruction takes the 7909 channel out of operation and causes a complete reset. The channel is placed in wait status by resetting the wait trigger on; the assembly ring is reset to position 6; the character ring is reset to position 4; and all other triggers, registers, and counters are reset to the normally OFF position. In addition, a 6 μs operational out signal is sent to the I-O adapters for use as a reset pulse for its circuitry and attached I-O devices; the specific function, however, depends on the particular adapter.

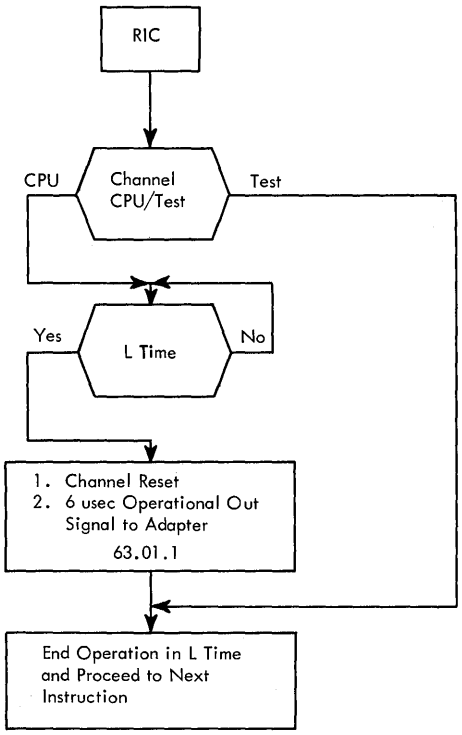


Figure 52. RIC Flow Chart

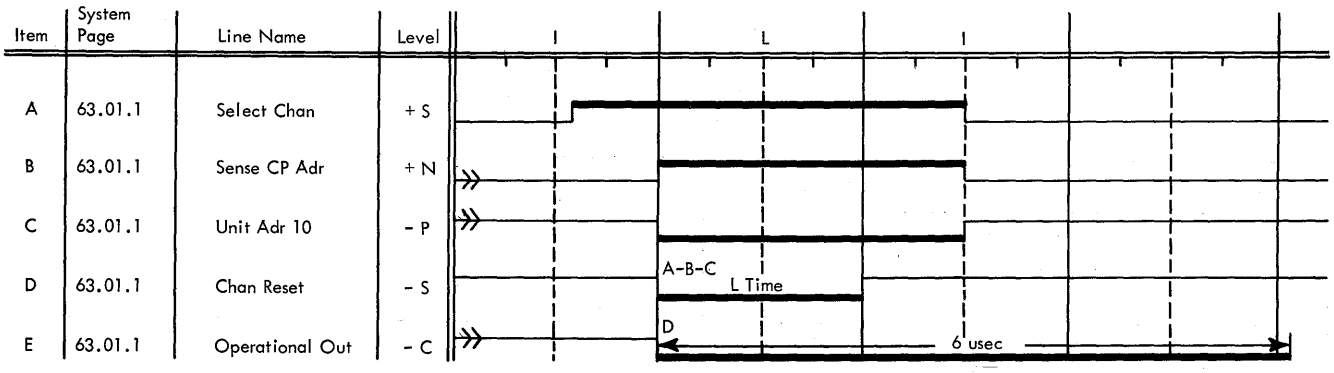


Figure 53. RIC Sequence Chart

All channel commands are decoded in the channel's operation decoder. Five bits define the command: S, 1, 2, 3 and 19. Note, however, that position 3 is located in the decrement portion of the word. Commands which do not require the decrement portion of the word can use this position for decoding purposes. Other channel commands that require either a full or partial decrement field (such as CPYP, CPYD, TCM, ICC, or XMT) cannot use position 3 bit for operation decoding. Bit configurations for the commands are shown in Figure 54.

Formats for these commands are shown in Figure 55 and use the following field nomenclature:

Y — Address
C — Count
M — Mask
F — Indirect Address Flag
N — Non Transmit

If position N(4) of the commands CTL, CTLW, or CTLR is a 1, the order is not sent to the I-O unit.

Command Cycle

With the logical capabilities of the 7909 Data Channel, a cycle must be designated as the time when the functions of the command are executed. The command (CMMD) cycle, therefore, is comparable to the logic (L) cycle of the attached 7090 or 7094 Data Processing System. A control word cycle (BCW or ECW) in the channel

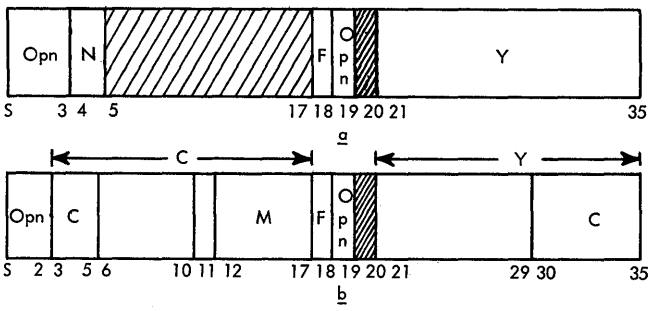


Figure 55. Command Formats

Operation Code						Mnemonic	Command
0 - 7			0/4	0/2	Octal		
S	1	2	3	19			
0	0	0		0	000	WTR	Wait and Transfer
0	0	0		1	002	XMT	Transmit
0	0	1		0	100	TCH	Transfer in Channel
0	0	1		1	102	LIPT	Leave Interrupt Program and Transfer
1	0	0		0	400	CPYP	Copy and Proceed
1	0	1		0	500	CPYD	Copy and Disconnect
1	0	1		1	502	TCM	Transfer on Conditions Met
1	1	1		1	702	ICC	Insert Control Counter
0	1	0	0	0	200	CTL	Control
0	1	0	0	1	202	CTLR	Control and Read
0	1	0	1	0	240	CTLW	Control and Write
0	1	0	1	1	242	SNS	Sense
0	1	1	0	0	300	LAR	Load Assembly Register
0	1	1	0	1	302	SAR	Store Assembly Register
0	1	1	1	0	340	TWT	Trap and Wait
1	1	0	0	1	602	LIP	Leave Interrupt Program
1	1	0	1	0	640	TDC	Transfer and Decrement Counter
1	1	0	1	1	642	LCC	Load Control Counter
1	1	1	0	0	700	SMS	Set Mode and Select

Figure 54. 7909 Commands

can be compared to I time in the computer; it is during this period that a new command is received from core storage and set into the various counters and registers.

Each time a command is received, the command counter must be stepped +1 to locate the next sequential command in core storage. This stepping requires a command counter cycle (CCC) for operation with the adders and occurs before the execution of the command. A sequence of cycles not requiring I-O data transmission is:

ICC COMMAND	TCM COMMAND
BCW—CCC—CMMD -----	BCW—CCC—CMMD ----

Generally, each channel command requires only one CMMD cycle to either initiate or complete its execution. Exceptions to this, however, are the LIP command which performs two distinct steps during its execution and, therefore, requires two CMMD cycles; and the XMT command which requires two CMMD cycles for each word transmitted.

Control—CTL

Cyclic Makeup: BCW - CCC - CMMD - BDW - ACC

The control command (Figures 56 and 57) sends information contained in C (Y) to the I-O adapter, starting with the high-order character, and continues until an end signal is received from the adapter or until the channel is reset. If more than one word location is needed to transmit all data required, the next word is taken from location Y + 1, and so on. This process continues until an end signal is received; the next command is then taken from the storage location following the control command. If N is a 1, the channel proceeds to the next sequential command.

Data words are sent to the adapter in a normal manner but the adapter is conditioned to treat this data as orders rather than data to be sent to an I-O device. No copy commands are required for this data transmission; data words are taken sequentially from the address specified by the CTL command. This continues until an end or unusual end signal is received from the adapter. Normally one or two data words will suffice but this is entirely dependent on the particular adapter. Some typical orders are: select TU, rewind, and set density, for Hypertape; seek, six-bit mode, release, for 1301 Disk Storage.

The operation register, word counter, and address counter are set during the BCW cycle. The S, 1, 2 bit positions immediately decode "interface CMMD" so that a possible sequence check can be detected at the beginning of the next cycle. This next (CCC) cycle increments the command counter and if a sequence check is appropriate (read, write, or sense trigger is on), it prevents execution of the CTL command, and causes a channel interrupt. The sequence check trigger turned on causes interrupt condition on 50.80.01.1. This causes inhibit commands (50.80.03.1) which immediately blocks the operation register decoders and prevents turning on the control gate trigger (50.20.07.1).

If there are no check conditions, the CMMD cycle turns on the control gate trigger. This operation involves data transmission to the adapter; therefore, the channel is placed in write status and a BDW cycle requested.

At the time of the first BDW cycle, "data register loaded" (50.38.01.1) causes the select gate trigger (50.52.02.1) to be turned on. The output from this trigger gates "control gate" (50.20.07.1) and sends a control signal across the interface.

From this point, data transfer is on a demand-response basis until an end condition is received from the adapter. Each BDW cycle is immediately followed by an address counter cycle (50.37.03.2) to increment the address counter. The word counter performs no logic and, therefore, is not decremented during the BDW cycle. Details on data flow and end conditions are covered in another section of this manual. End condition resets the control gate trigger and initiates a BCW cycle request for the next sequential command.

The N (4) position of CTL, CTLW, or CTLR is recognized in the channel by the output of word counter position 4 on control word cycles. Storage bus positions 3-17 are set into the word counter on BCW cycles and position 4 is used to perform the following functions:

1. Gates on control BCW gate (50.36.01.1), which in turn sets BCW required (50.37.01.1) and turns on the demand delay trigger (50.35.02.1).
2. Prevents turning on control gate trigger during the CMMD cycle (50.20.07.1).
3. Prevents interface command recognition (50.20.-03.1).

Control and Write—CTLW

Cyclic Makeup: BCW - CCC - CMMD - BDW - ACC

A control and write command (Figures 56 and 57) sends control data (orders) to the adapter and conditions the channel for a write operation in two steps. The control

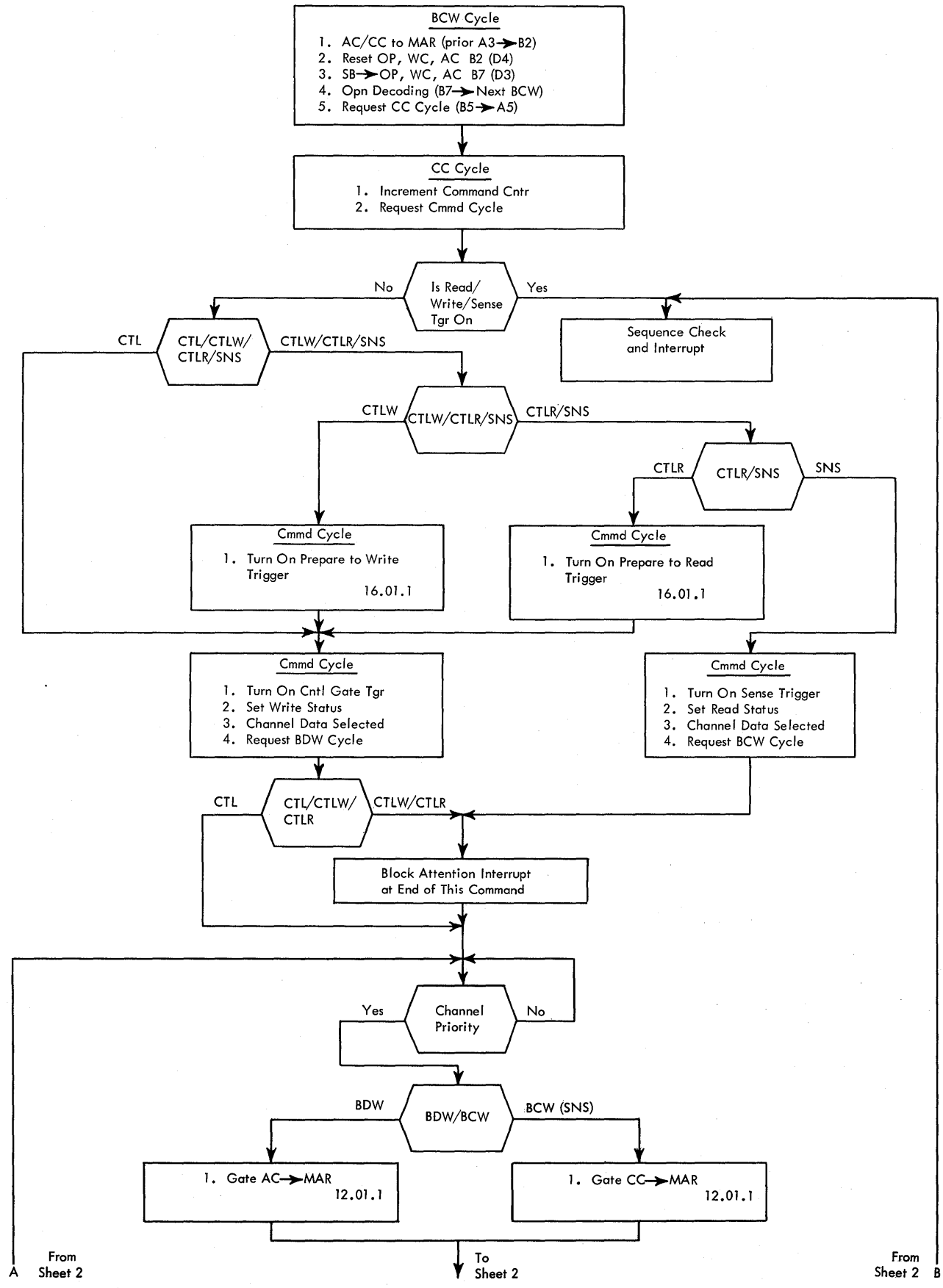


Figure 56. CTL/CTLW/CTLR/SNS Flow Chart (Sheet 1)

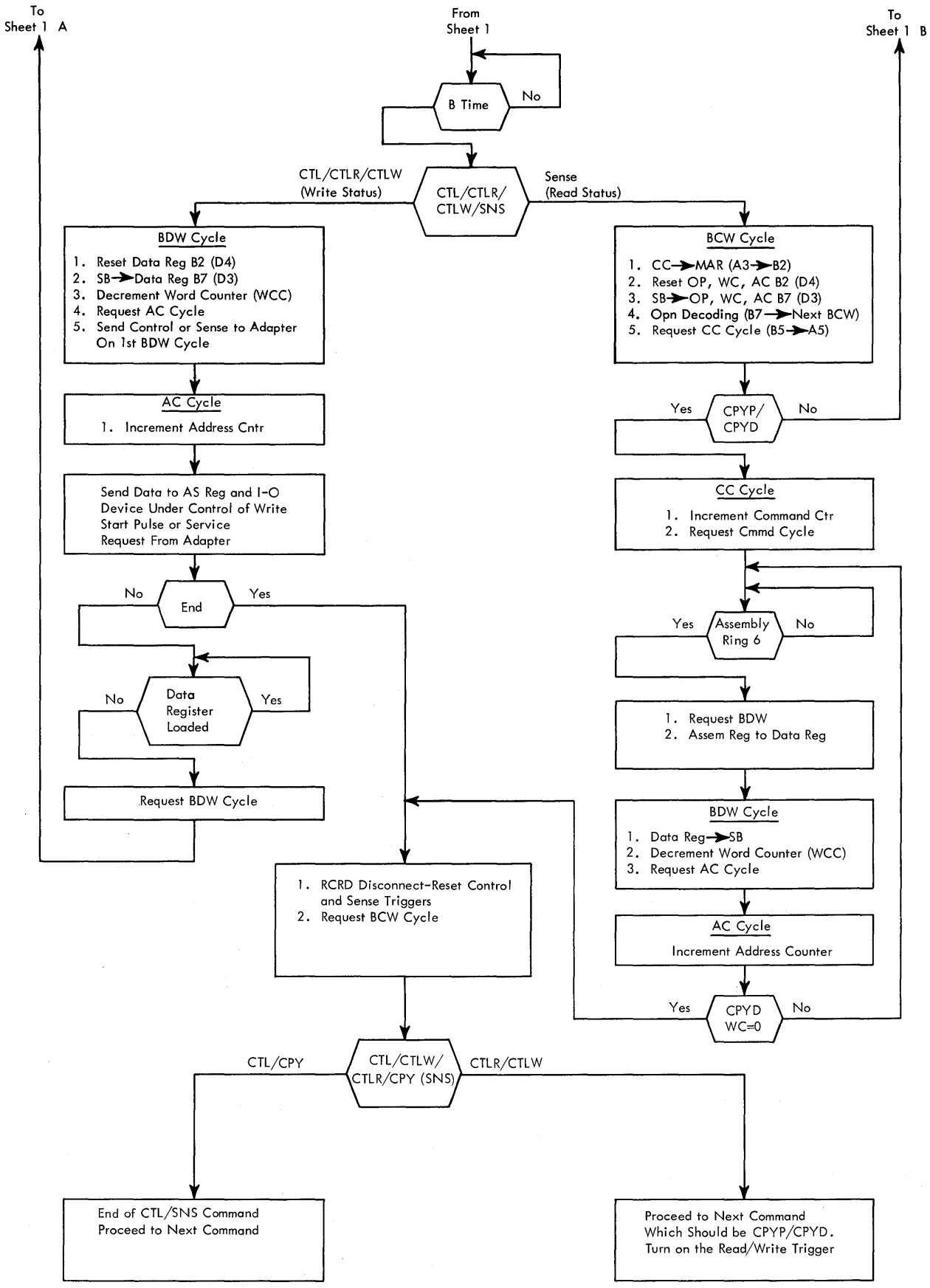
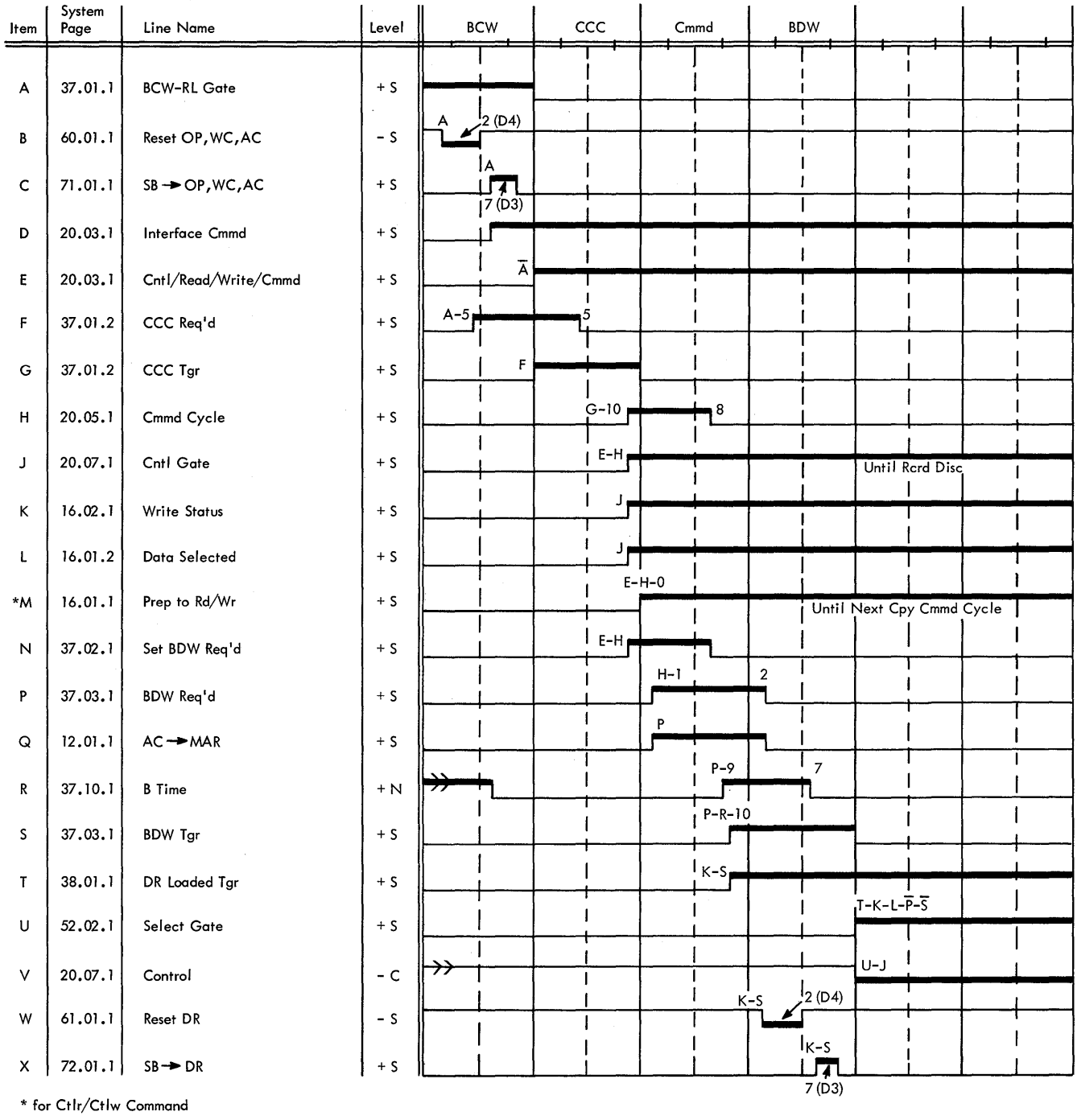


Figure 56. CTL/CTLW/CTLR/SNS Flow Chart (Sheet 2)



* for Ctlr/Ctlw Command

Figure 57. CTL/CTLW/CTLR Sequence Chart

phase functions like the CTL command. In addition, a prepare to write trigger is turned on to remember that a write operation is to follow. If N is a 1, this command prepares the channel to write and proceeds to the next sequential command. When a copy command is encountered, the channel is placed in write status, and data are transmitted from core storage to the control unit under control of the copy command.

The control gate and prepare to write triggers are turned on during the CMMD cycle. "Control gate" places the channel in write status and requests a BDW cycle during which a data word is obtained from storage. At the end of the first BDW cycle, the select gate trigger is turned on and a control signal is sent to the adapter. The signal initiates the request-response sequence to pass control data to the adapter.

As soon as an end condition is received from the adapter signaling the end of the control phase, a BCW

cycle is requested to obtain the next command, which must be a CPY or TCH to a CPY if data transmission is expected. The copy command specifies the place from core storage, and how many data words to transmit across the interface. The copy command resets the prepare to write trigger, turns on the write trigger, and places the channel in write status. The data register loaded trigger being initially off requests a BDW cycle (50.37.02.1) for the first data word. During the first BDW cycle, "data register loaded" (50.38.01.1) turns on the select gate trigger (50.52.02.1) for the second time. "Select gate" gated with the write trigger output (50.16.01.1) sends a write signal to the adapter. From this point, data transfer is on a demand-response basis until a stop signal is initiated by the channel or an end condition is received from the adapter. When under control of a CPYD command, this end condition resets the write trigger and initiates a BCW cycle request for the next sequential command.

During the CTL phase of the operation, each BDW cycle is immediately followed by an address counter cycle; the word counter performs no logic and will not be decremented. During the copy phase of the operation, however, each BDW cycle is also a word counter cycle and the word counter is decremented. Each of these BDW cycles is also immediately followed by an address counter cycle and the address counter is incremented. (Details on data flow and end conditions are covered elsewhere in this manual.)

A sequence check is possible at the beginning of the operation if the read, write, or sense trigger is on. In this case, the operation decoders are blocked as explained in the previous CTL section, the control gate and prepare to write triggers remain off, and an interrupt occurs.

Control and Read—CTLR

Cyclic Makeup: BCW - CCC - CMMD - BDW - ACC

A control and read command (Figures 56 and 57) sends control data (orders) to the adapter and conditions the channel for a read operation in two steps. The control phase functions like the CTL command. In addition, a prepare to read trigger is turned on to remember that a read operation is to follow. If position N is a 1, this command proceeds to the next sequential command. When a copy command is encountered, the channel is placed in read status, and data are transmitted to core storage under control of the copy command.

A sequence check is possible at the beginning of the operation if the read, write, or sense trigger is on. In this case, the operation decoders are blocked as explained under "Control," the control gate and prepare to read triggers remain off, and an interrupt occurs.

If there is no sequence check, the control gate and prepare to read triggers are turned on during the command cycle. "Control gate" places the channel in write status and requests a BDW cycle during which a data word is obtained from core storage. During the first BDW cycle, the select gate trigger is turned on and a control signal is sent to the adapter. This signal initiates the demand-response sequence to pass control data to the adapter.

As soon as an end condition is received from the adapter, signaling the end of the CTL phase, a BCW cycle is requested to obtain the next command. This should be a copy command to specify how many data words are to be received from the adapter and where in core storage they are to be placed. The copy command resets the prepare to read trigger, turns on the read trigger, and places the channel in read status. Read status (50.16.02.1) turns on the select gate trigger (50.52.02.1) for the second time. This output is further gated by the read trigger (50.16.01.1) to send a read signal to the adapter. Data words begin to flow from the adapter on a demand-response basis until a stop signal is initiated by the channel or an end condition is received from the adapter. When under control of a CPYD command, this end condition resets the read trigger and initiates a BCW cycle request for the next sequential command.

During the CTL phase of the operation, each BDW cycle is immediately followed by an address counter cycle; the word counter performs no logic and will not be decremented. During the copy phase of the operation, however, each BDW cycle is also a word counter cycle and the word counter is decremented. Each of these BDW cycles is also immediately followed by an address counter cycle, and the address counter is incremented. (Details on the data flow and end conditions are covered in other sections of this manual.)

Sense—SNS

Cyclic Makeup: BCW - CCC - CMMD

A sense command (Figures 56 and 58) signals the adapter to transmit sense data back to the channel and into core storage. This sense information is sent to the channel in the same manner as data from an I-O device.

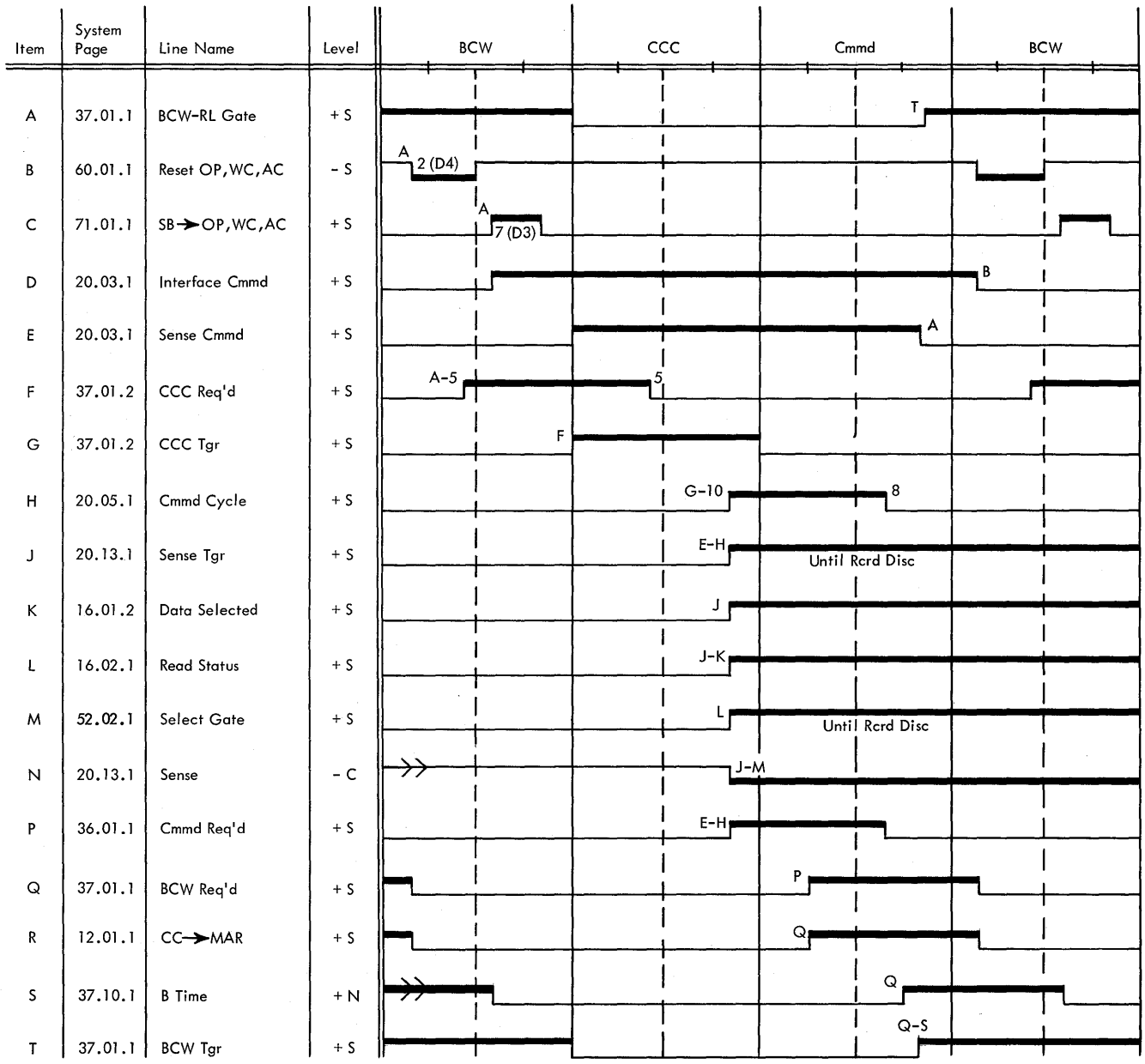


Figure 58. SNS Sequence Chart

SNS places the channel in read status and from this point the operation is similar to a normal I-O read operation with copy commands controlling the amount of data received and its location in core storage.

The operation register, word counter, and address counter are set during the BCW cycle; S, 1, 2 bit positions immediately decode "interface command" so that a possible sequence check can be detected at the beginning of the next cycle. This next (CCC) cycle increments the command counter, and if a sequence check is appropriate (read, write, or sense trigger is on), prevents execution of the SNS command, and causes a channel interrupt. The sequence check trigger turning on causes "interrupt condition" on 50.80.01.1. This causes "inhibit commands" (50.80.03.1) which immediately blocks the operation register decoders and prevents turning on the sense trigger (50.20.13.1).

If there is no sequence check, the following CMMD cycle turns on the sense trigger. This operation involves data transmission from the adapter to core storage; therefore, the channel is placed in read status. "Read status" (50.16.02.1) turns on the select gate trigger (50.52.02.1) and allows a sense signal to be sent to the adapter. At the same time, a BCW cycle is requested to obtain a copy command which will direct the flow of information into core storage.

From this point, data transfer is on a demand-response basis until a stop signal is initiated by the channel or an end condition is received from the adapter. This end condition resets the sense trigger and initiates

a BCW cycle request for the next sequential command. (Details on data flow and end conditions are covered elsewhere in this manual.)

If a copy command does not follow the SNS, a sequence check occurs. In this case, the operation is terminated and an interrupt is initiated. Because the sense command has already been sent across the interface, the operation must be terminated with a stop signal to the adapter (50.52.01.1). The adapter returns an end signal which causes a "record disconnect" (50.52.02.1) to reset the sense trigger and allow the interrupt to proceed.

Copy and Proceed—CPYP

Cyclic Makeup: BCW - CCC - CMMD - BDW - ACC

Copy and proceed (Figure 59) is used in conjunction with CTLW, CTLR, and SNS commands to specify the amount of data to be transferred between the computer and I-O adapter, and the core storage locations which are to receive or transfer the data. The word count being reduced to zero requests a BCW cycle and a subsequent command.

The operation register, word counter, and address counter are set at 7 time of the BCW cycle and the output becomes active at the next 0 time. The next (CCC) cycle increments the command counter and requests a CMMD cycle. A sequence check is possible at this point if the read, write, or sense trigger is not on. If this is the case, the operation register outputs are blocked, the operation is terminated, and an interrupt is initiated.

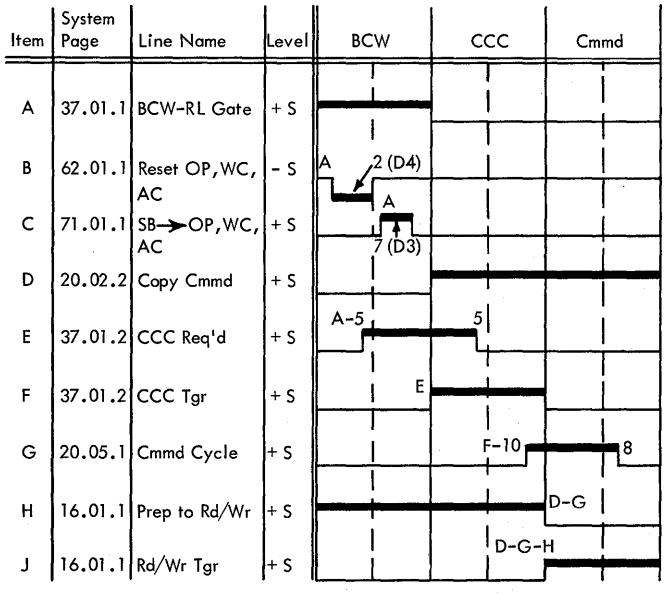


Figure 59. CPYP-CPYD Sequence Chart

If this is the first CPYP and there is no sequence check, the CMMD cycle turns on the write or read trigger and resets the prepare to write or prepare to read trigger, depending on whether the operation was initiated by a CTLW or CTLR command. A write operation immediately requests a BDW cycle for the first data word. At the time of this first BDW cycle, "write" is sent to the adapter and data transmission begins across the interface. A read operation immediately sends "read" to the adapter and data transmission begins as soon as characters are received from the I-O device. A sense operation is begun with the SNS command, and the copy command is obtained while the assembly register is being filled with the first data word.

BDW cycles occur for each data word transmitted; during each of these cycles, the word counter is decremented. An address counter cycle is requested to increment the address counter and immediately follows the BDW cycle. (Refer to the section on "Data Flow" for further explanations, sequence charts, and flow charts.)

Any end signals occurring during the CPYP are serviced without affecting the copy command; an "unusual end" terminates the operation and causes an interrupt. When the word count is reduced to zero, a BCW cycle is requested to bring in the next sequential command. If this command is a TDC, TCH, CPYP or CPYD data transmission is resumed; any other command causes a sequence check. A CPYD must terminate the operation.

An interface check or I-O check occurring during the data transmission initiates a stop signal to the adapter. When the end condition is returned, the operation is terminated and the channel interrupts.

Copy and Disconnect—CPYD

Cyclic Makeup: BCW - CCC - CMMD - BDW - ACC

The conditions explained for CPYP in the preceding section also apply for CPYD (Figure 59) with the following exceptions. A CPYD command is confined to one record. During a write operation, the word count going to zero initiates a stop signal to the adapter. When an end condition is returned, the adapter is disconnected and the channel proceeds to the next sequential command.

If the next command is other than a copy, the channel executes that command. If the next command is a copy, the channel interrupts on a program sequence check. The last word transmitted to storage under CPYD control remains in the assembly register if the word

count is equal to or greater than the number of words remaining in the I-O record.

During a read operation, the adapter may be disconnected because of two conditions. First, the channel may initiate a stop signal to the adapter when the word count goes to zero. If the count for the CPYD goes to zero before an end signal is received, the channel initiates a disconnect but does not get the next sequential command until an end or unusual end signal is obtained. Second, the adapter may send an end condition before the word count is reduced to zero. In general, when operating under CPYD control, the channel does not obtain the next sequential command until either an end (or unusual end signaling an error) occurs.

Further discussions with flow charts and sequence charts can be found in the sections on "Data Flow" and "End Conditions."

Transfer in Channel—TCH

Cyclic Makeup: BCW

A TCH command (Figure 60) produces an unconditional transfer in the channel. Look-ahead circuitry in the multiplexor actually causes the transfer by decoding the operation code of S, 1, 2 and routing the channel address switches (the transfer address) back into MAR. The command at location Y is loaded into the data channel and the command counter is increased to Y+1.

The TCH decoding also produces a "retain priority" which is sent to all channels causing this channel to retain priority and immediately request a second BCW cycle. This second cycle is a normal BCW cycle and accepts the new channel command at the transfer address.

At the same time that the TCH is detected in the multiplexor, a TCH trigger is turned on in the channel to perform the following:

1. Block the normal request for a CC cycle following the first BCW cycle.
2. Block setting the operation register and word counter. The address counter is set but performs no logic.
3. Reset the command counter at B10(D2) of first BCW cycle in preparation for receiving the transfer address from MAR.
4. Sample the MAR bus from the multiplexor into the command counter.

"Retain priority" received from the multiplexor also serves to block the normal command counter to MAR circuitry on 50.12.01.1.

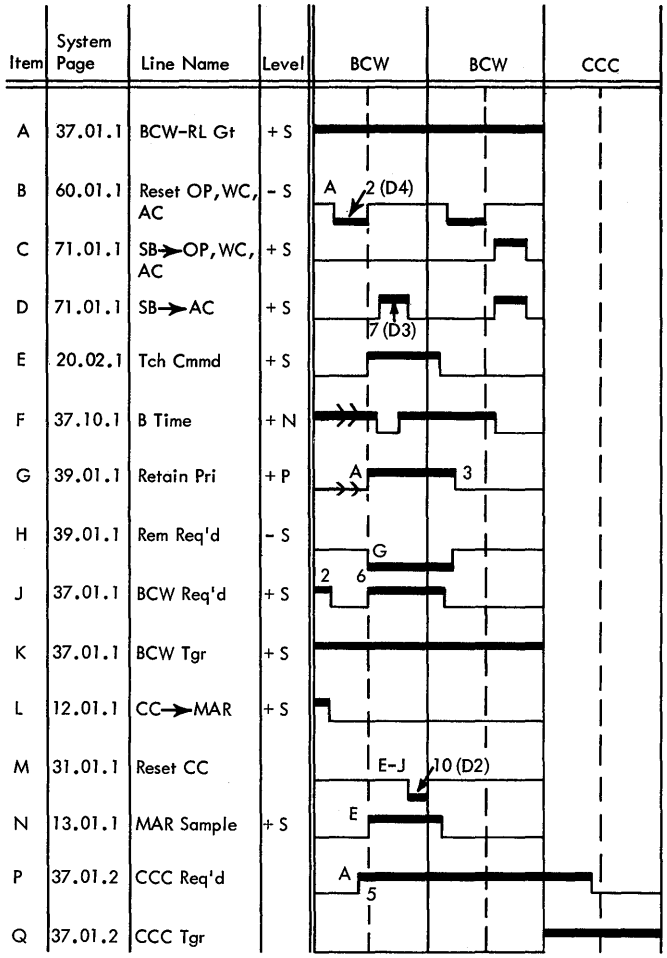


Figure 60. TCH Sequence Chart

Wait and Transfer—WTR

Cyclic Makeup: BCW - CCC - CMMD

The wait and transfer command (Figures 61 and 62) stops channel operations, puts the channel in wait status, and places an appropriate transfer address from the WTR command into the address counter. The channel command counter contains the location of the WTR command. If the WTR is indirectly addressed, the address counter contains the contents of the address portion of location Y.

The channel may be restarted by either an RSC or STC command or by an interrupt. When the channel is told to start by means of an STC command, the next command is taken from the location specified by Y of the WTR command. If an interrupt occurs while the channel

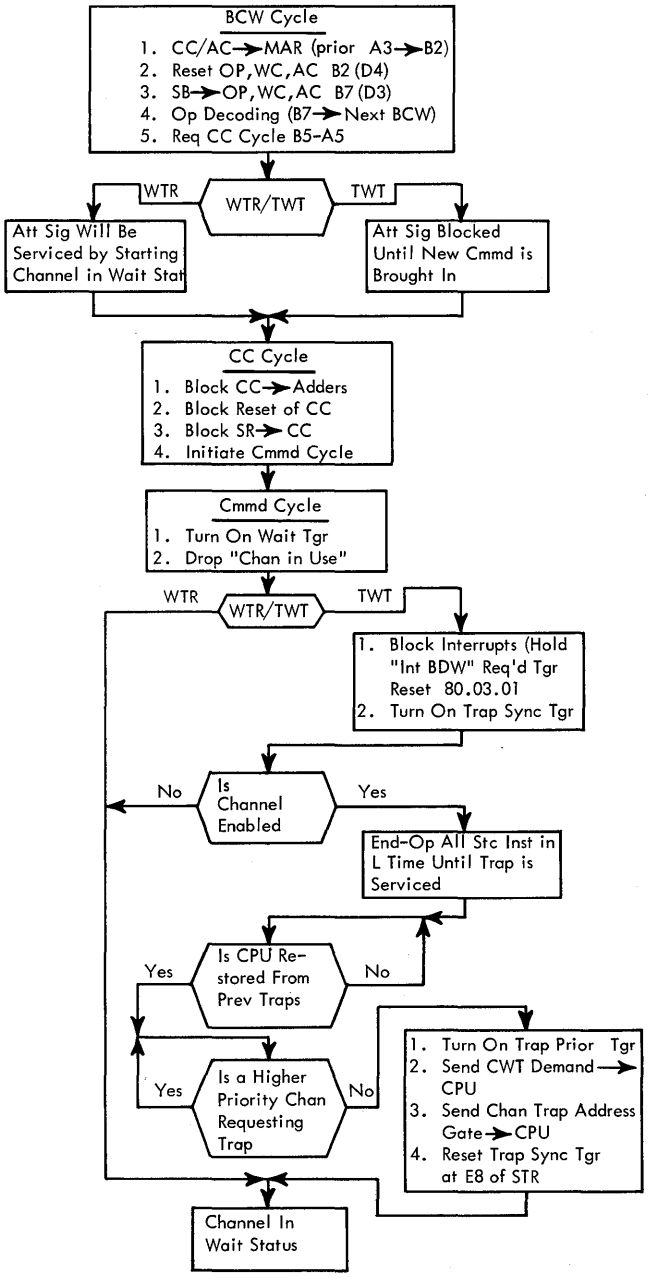


Figure 61. WTR/TWT Flow Chart

is in wait status, the return from the interrupt program by means of a LIP command puts the channel in wait status.

The operation decoders are set at 7 time of the BCW cycle and outputs become active at 0 time of the next cycle. Also during the BCW cycle the values in the address counter and word counter are reset and replaced by the contents of the address and decrement of the transfer location. Setting the word counter provides no useful function, however, but is accomplished because of circuitry.

The first cycle is a command counter cycle which would normally step the command counter through the adders. Execution of a WTR command, however, requires that the counter remain the same (i.e., the address of the WTR command). Because of this, adder circuitry is blocked so that the counter contents are not affected. This counter cycle, then, provides no logic within itself but instead acts merely as a means of obtaining a CMMD cycle.

Turning on the CMMD cycle trigger turns on the wait trigger and drops the channel in use line to the multiplexor.

At this point the channel stops operating; there is no circuitry to request a BCW cycle. If a computer start channel or reset and start channel is waiting in L time for execution, turning on the wait trigger allows a proceed to E signal to be sent to the computer (50.36.02.1).

Note that wait status is the normal reset status of the channel. "Power-on reset," "interlock reset," and RIC are a few of the ways to turn on the wait trigger.

Trap and Wait—TWT

Cyclic Makeup: BCW - CCC - CMMD - I (STR) - E (STR)

Execution of a TWT command (Figures 61, 63, and 91) places the channel in wait status and, at the same time, causes a channel trap if the channel was previously enabled. The value in the address portion of the TWT command is loaded into the channel address counter to be used as a transfer address during a subsequent STC instruction. If the TWT is indirectly addressed, the address counter contains the address from location Y. The word counter is also loaded with the decrement from location Y but serves no logical function.

The operation decoder becomes active at 0 time following the BCW cycle. At this time "trap command" holds the interrupt BDW required trigger (50.80.03.1) continually reset. This prevents any channel interrupts from being initiated until the computer has replaced the TWT command by means of either an STC or RSC instruction. An interrupt condition, such as an attention interrupt, is not lost, but saved until the channel is put in operation again.

If enabled to handle control word traps, the channel seeks its place in the area of priority. A remote trap required signal is propagated through the lower priority channels to prevent their obtaining priority in the case of simultaneous requests. With no higher priority channel requesting a trap, this channel's trap priority trigger is turned on and a control word trap (CWT) demand is sent to the computer. This signal is initiated at 8 time

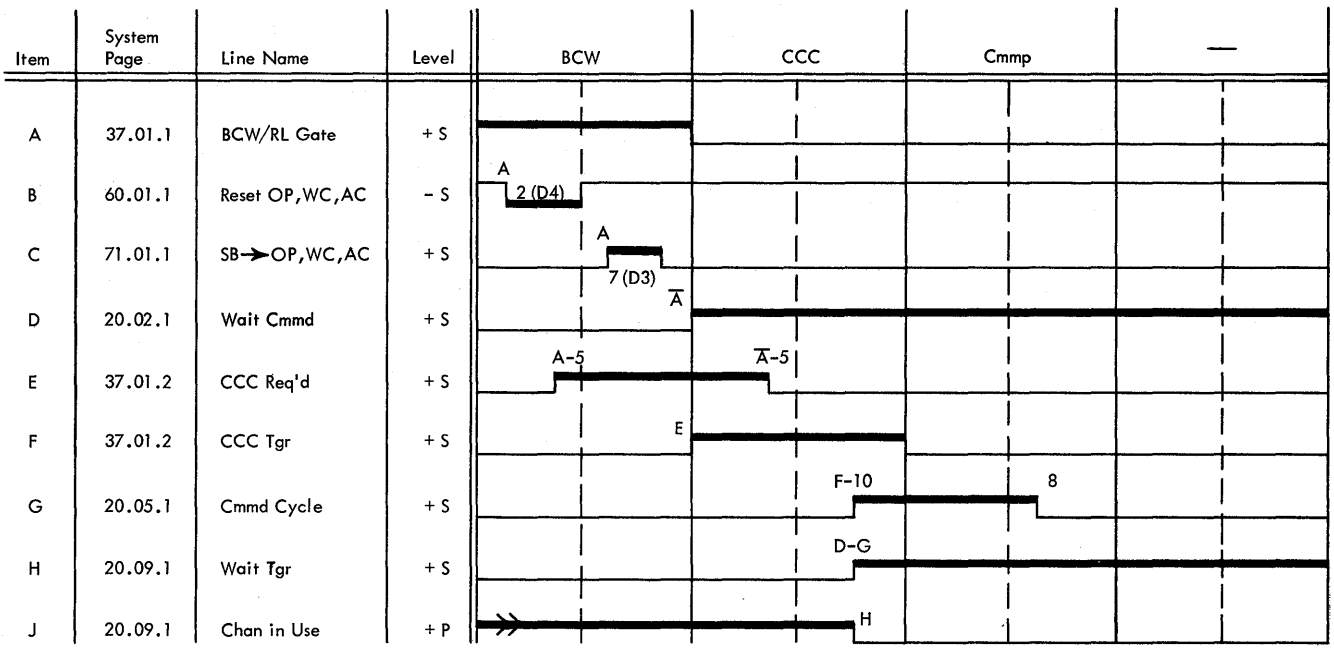


Figure 62. WTR Sequence Chart

of the cycle during which the channel obtains priority and turns on the computer's channel trap trigger at the next I6 time. The computer is now forced into a store and trap (STR) instruction during which time the PC value will be stored in a specified location and a transfer effected.

As soon as the computer's channel trap trigger is turned on, the corresponding signal is sent to the channel. This immediately brings "channel trap address gate" back to the computer to specifically define which channel caused the trap, where to store the IC, where to transfer at the end of the STR instruction, and what flag bits to store in the decrement portion of the trap location.

During the latter portion of the STR E-cycle, the channel's trap sync trigger and trap priority triggers are reset. The computer continues to the next scheduled instruction and the channel is left in wait status. Interrupts are still blocked until such time that the channel is started again by the computer. (An RSC resets the blocking conditions and starts the channel.)

Any STC instructions issued to this channel between the time that a trap is requested and the time it is actually serviced are NO-OP'ed by causing that instruction to end operation in L time.

If the channel is not enabled, the TWT operates in a manner similar to a WTR command. Either a reset and start channel instruction or start channel instruction resets the trap and causes the channel to resume operation.

When a trap occurs, the contents of the computer program counter is stored and the next instruction is taken from a fixed location as follows:

CHANNEL	PC STORED	NEXT INSTRUCTION
A	00012	00013
B	00014	00015
C	00016	00017
D	00020	00021
E	00022	00023
F	00024	00025
G	00026	00027
H	00030	00031

Load Assembly Register—LAR

Cyclic Makeup: BCW - CCC - CMMD - BDW

Execution of this command (Figures 64 and 65) causes the contents of Y to be sent through the storage bus switches and the data register to replace the contents of the assembly register. The contents of Y remain unchanged. After execution, the channel proceeds to the next sequential command.

The operation register, word counter, and address counter are set at 7 time of the BCW cycle and the operation decoder output becomes active at the next 0 time.

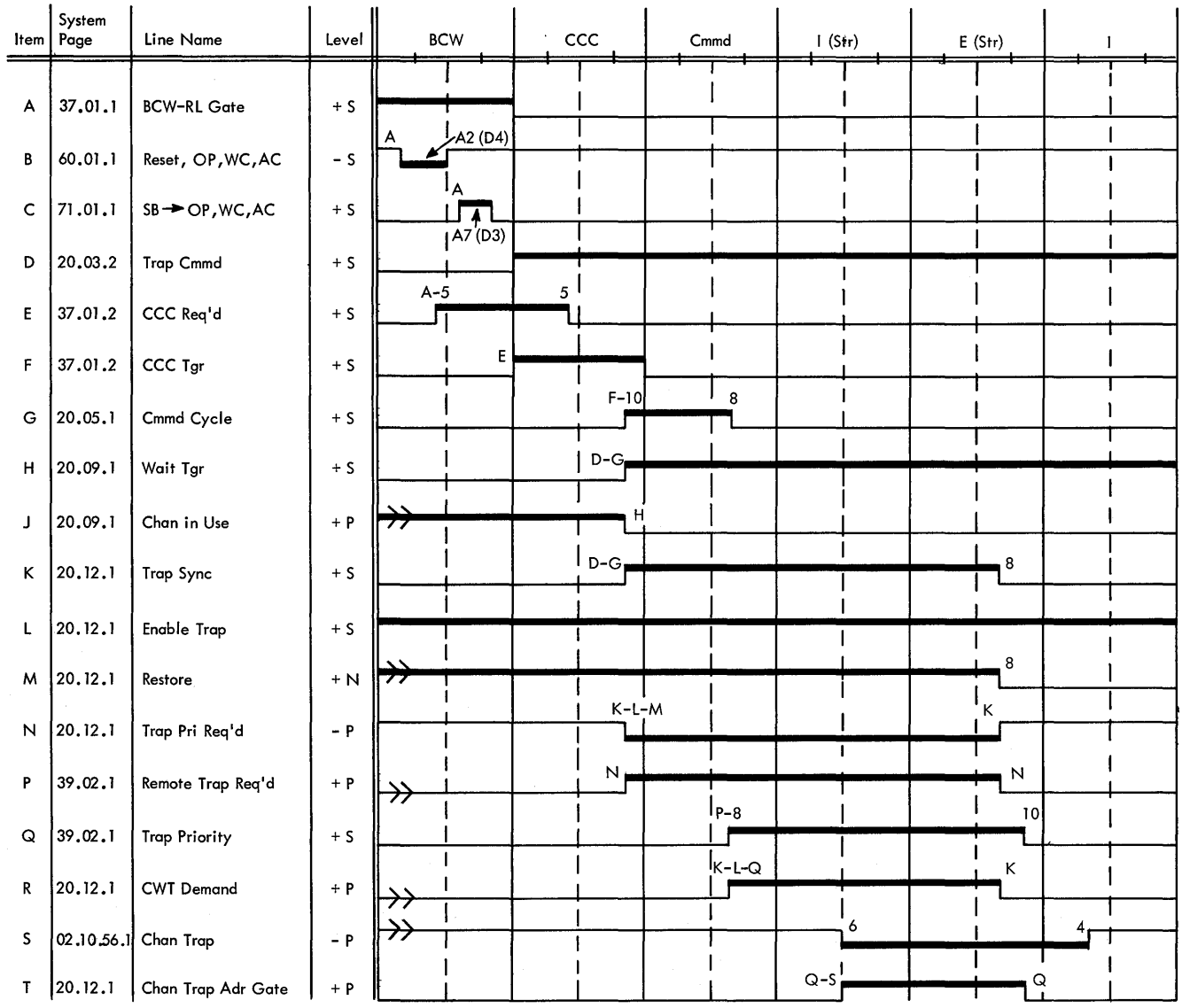


Figure 63. TWT Sequence Chart

The next cycle increments the command counter (CC cycle) and initiates a CMMD cycle. An LAR gate trigger is turned on at the beginning of the CMMD cycle and remains on until the operation has been completed and a request has been made for a new command (BCW cycle).

The word from core storage is obtained by placing the channel in write status and requesting a BDW cycle. The circuitry then functions in a manner similar to data transmission to an I-O device.

No logic is performed during the CMMD cycle except to reset the assembly register and request the necessary BDW cycle from the computer. The B-cycle does not immediately follow the CMMD cycle if other channels are attached to the system; priority must be obtained from the rest of the channels as well as from the computer. The B cycle demand is delayed by an amount dependent on the system configuration.

The address counter is gated to MAR at the beginning of the BDW cycle to obtain the designated word from core storage. The data register is reset early in the BDW cycle and set later in the cycle with the new data word when it is available on the storage bus. This B7(D3) pulse that sets the storage bus into the data register also conditions circuitry to gate the data register to the assembly register.

With the operation completed, a BCW request is made to obtain the next sequential command from core storage.

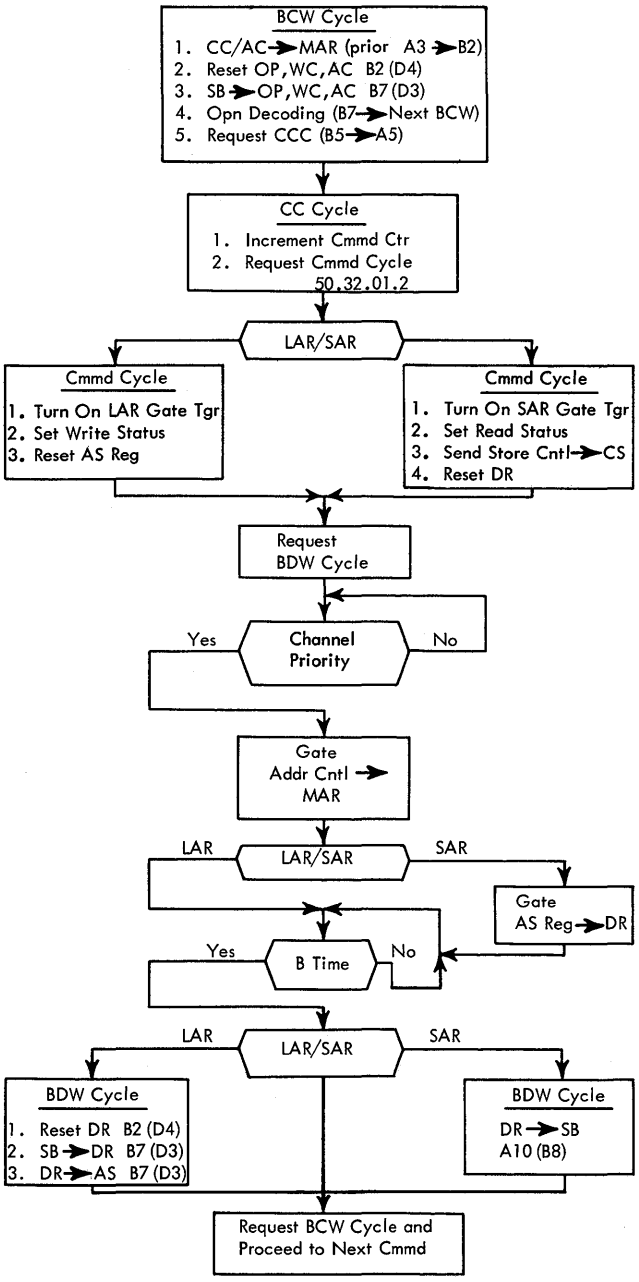


Figure 64. LAR/SAR Flow Chart

Store Assembly Register—SAR

Cyclic Makeup: BCW - CCC - CMMD - BDW

The SAR command (Figures 64 and 66) causes the contents of the assembly register to be stored at the address specified by the address portion of the SAR command. Contents of the assembly register remain unchanged. The operation register, word counter, and address counter are reset early in the BCW cycle and set to the new values at 7 time; the operation decoder does not become active until the following 0 time.

The next cycle (CCC) increments the command counter +1 and initiates a CMMD cycle. At the beginning of this CMMD cycle an SAR gate trigger is turned on and remains on until the operation is completed and a request is made for a new channel command.

Because this operation places data into core storage, a BDW cycle is requested from the computer and the channel is placed in read status. The data register, being an intermediate buffer between the assembly register and core storage, is reset during the CMMD cycle.

When B time is obtained through the normal channel delay and priority circuits, the address counter is gated to MAR to specify the correct core storage location. At the same time, the assembly register contents are gated and set into the data register in preparation for being placed on the storage bus. "Store control" is sent to core storage because of read status in the channel; this causes the old data in the core storage location to be destroyed.

During the BDW cycle, the data register contents are placed on the storage bus for sampling into memory and a request is initiated for a BCW cycle to obtain the next sequential channel command.

Set Mode and Select—SMS

Cyclic Makeup: BCW - CCC - CMMD

Execution of this command (Figures 67 and 68) causes the contents of positions 29-35 of this command to set or reset specific status indications as follows:

Bit	Function
29	Enable Non-Concurrence Interrupt
30*	Read Backward
31*	BCD Mode
32	Inhibit Unusual End Signals
33	Inhibit Attention 1 Signals
34*	Inhibit Attention 2 Signals
35*	Select 2 (1 is selected when reset)

*Optional Features

In all cases, the presence of the bit causes the status trigger to be set and the function to be enabled; absence of the bit resets the status trigger and disables the function. Machine and power-on resets also reset the triggers. With indirect addressing, the SMS command status triggers are set or reset with bits 29-35 of the location specified by bits 21-35 of the indirectly addressed command.

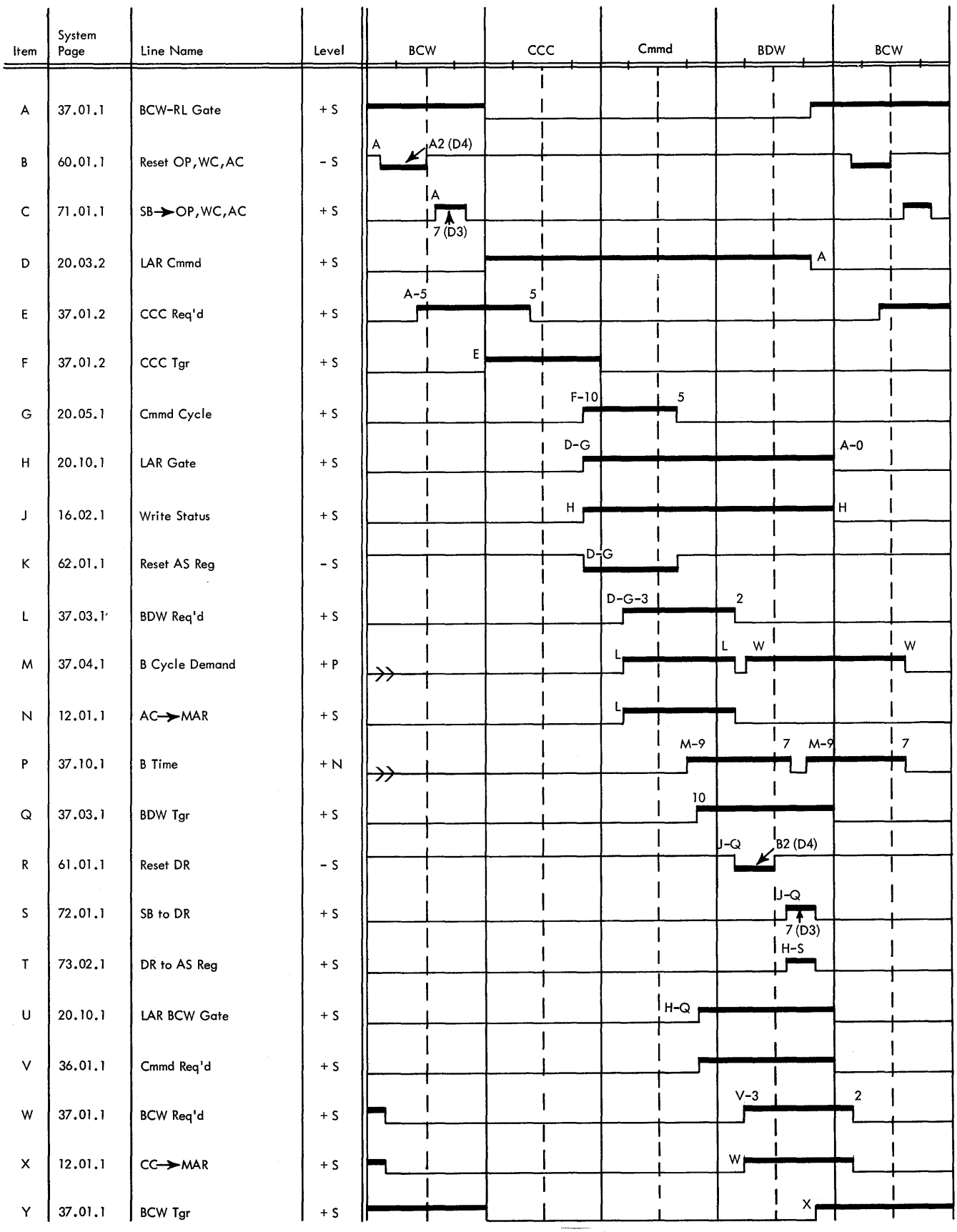


Figure 65. LAR Sequence Chart

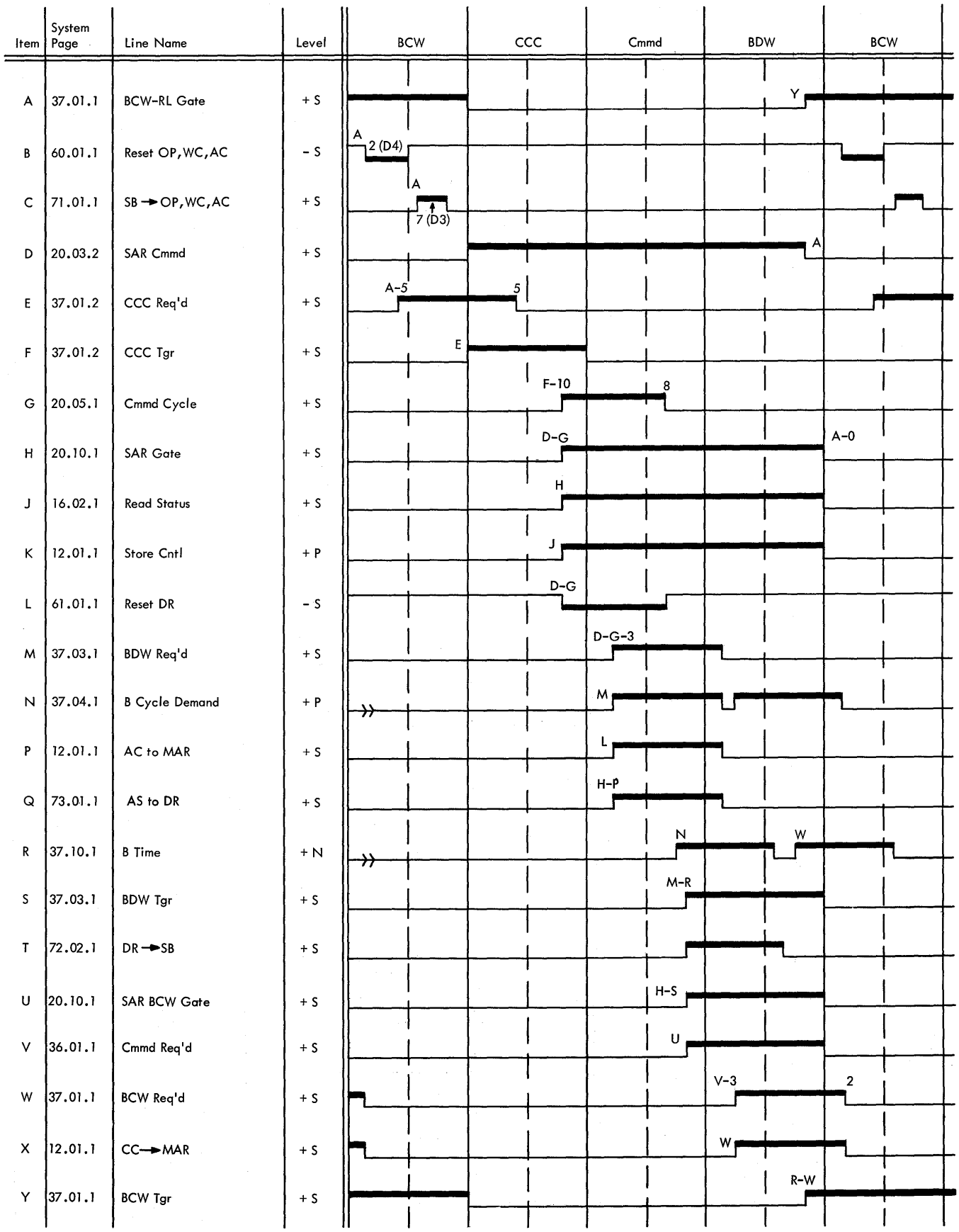


Figure 66. SAR Sequence Chart

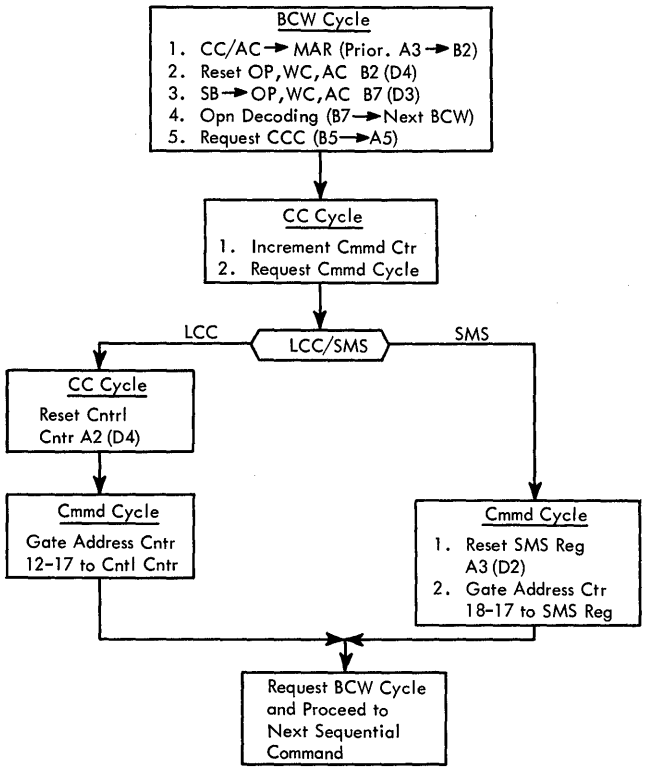


Figure 67. LCC/SMS Flow Chart

The mask configuration of bits is loaded into the address counter at 7 time of the BCW cycle; the operation register and word counter are also set at the same time.

The next cycle (CCC) increments the command counter +1 and requests a CMMD cycle. During the CMMD cycle the SMS register is reset and then set to the corresponding 11-17 mask bits of the address counter. The SMS set pulse is up for the full command cycle period and will produce an OR'ing condition of the SMS register and address counter from A10-A3. The SMS register is then completely reset with an A3(D2) pulse. Following this pulse, until A8 time of the CMMD cycle, the SMS register is set again to the correct value (positions 11-17 of the address counter). A request is also initiated for a BCW cycle and the channel proceeds to the next command in sequence.

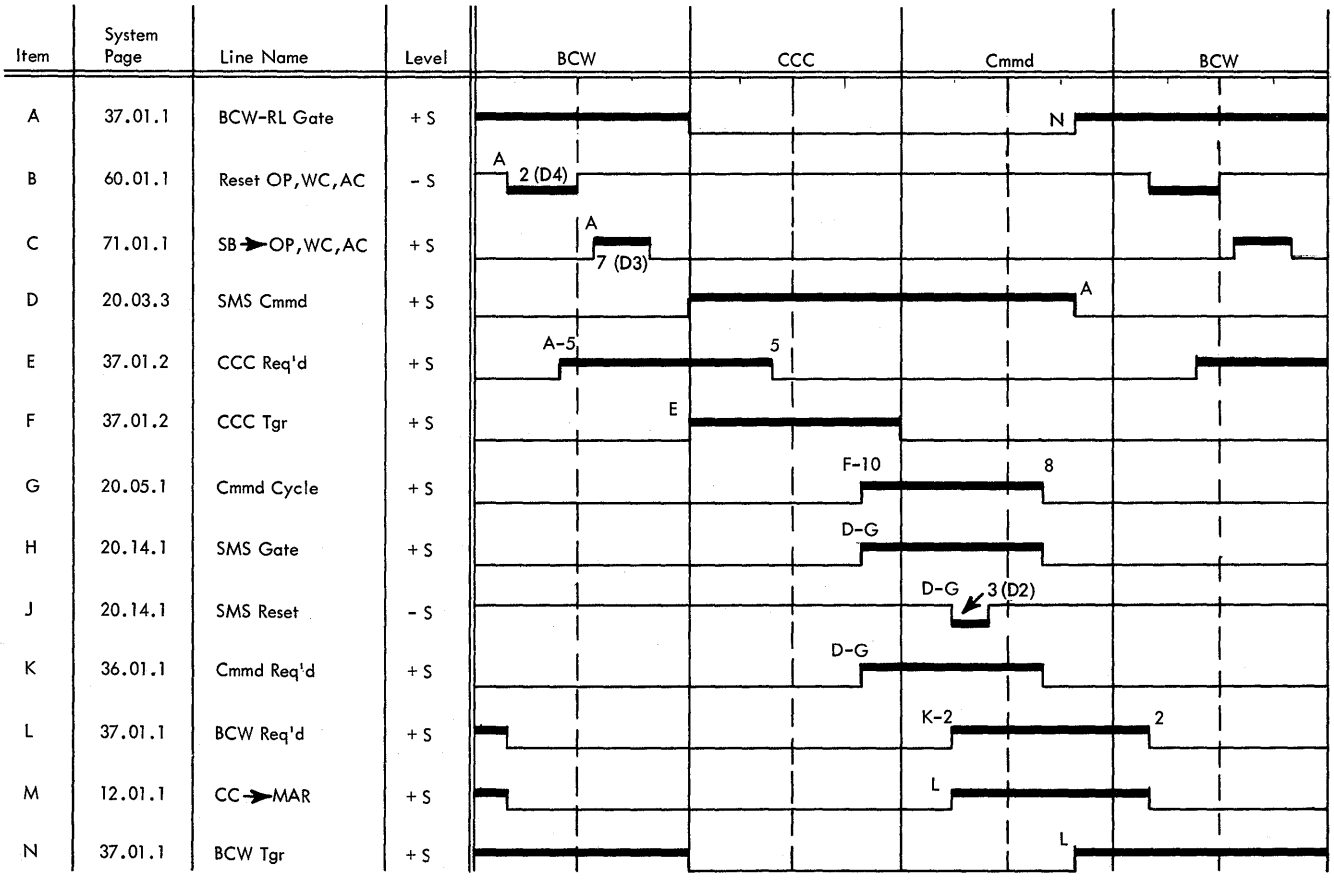


Figure 68. SMS Sequence Chart

Load Control Counter—LCC

Cyclic Makeup: BCW - CCC - CMMD

An LCC command (Figures 67 and 69) loads the six-position control counter with the value contained in address positions 30-35 of the LCC command. This value is loaded into the address counter at 7 time of the BCW cycle, the same time that the operation register and word counter are set.

The next cycle (CCC) increments the command counter +1 and requests a CMMD cycle. At the same time that the command counter is being stepped, through the adders, the control counter is reset in preparation to receive the new value during the following CMMD cycle.

The CMMD cycle samples positions 12-17 of the address counter and sets the corresponding value into the control counter. At the same time, a BCW request is sent to the computer and the channel proceeds to the next sequential command.

If the LCC is indirectly addressed, the contents of the control counter are replaced by the six low-order bits contained in the location specified by positions 21-35 of the LCC command.

Insert Control Counter—ICC

Cyclic Makeup: BCW - CCC - CMMD

This command (Figures 69, 70, and 71), for a count of 1-6 (in positions 3-5 of the command), inserts the control counter contents in the corresponding character position of the assembly register. A count of zero places the SMS status register contents in assembly register character position 6 (30-35). A count of seven has the effect of a NOP and the contents of the assembly register remain unchanged.

The operation register, word counter, and address counter are set at 7 time of the BCW cycle; the operation decoder output becomes active at the following 0 time.

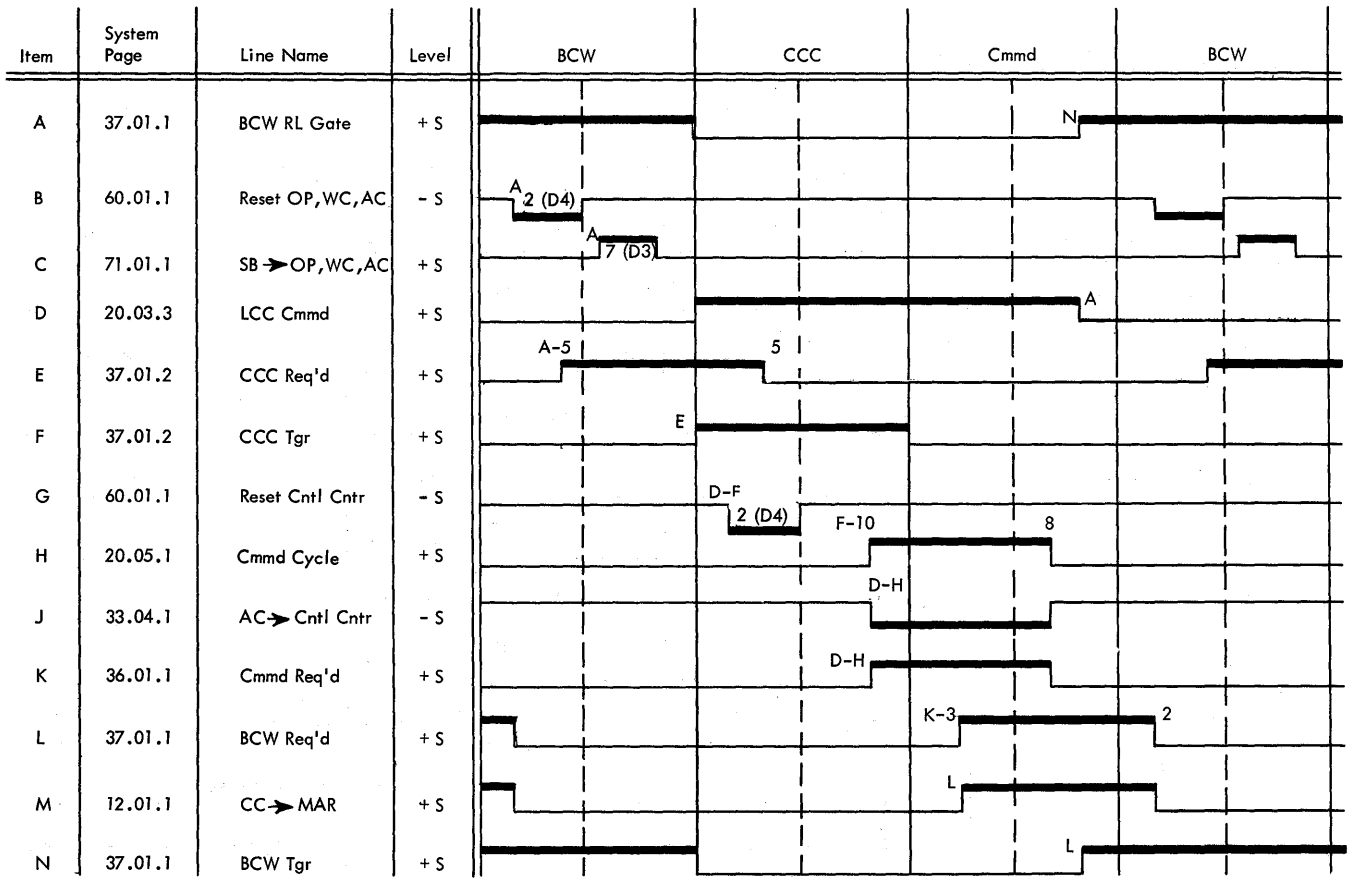


Figure 69. LCC Sequence Chart

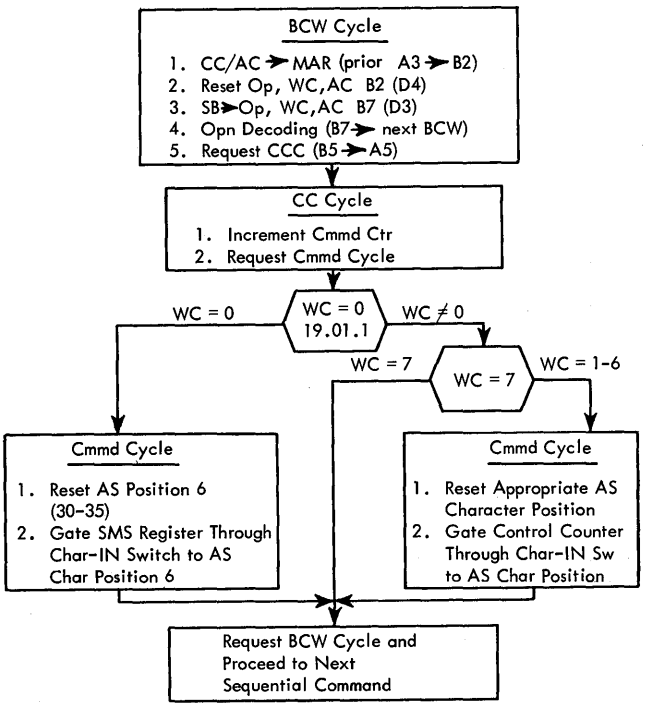


Figure 70. ICC Flow Chart

As soon as the word counter is set to the count value, circuitry decodes positions 3-5 for a zero or non-zero condition.

The next cycle (CCC) increments the command counter +1 and initiates a CMMD cycle but performs no ICC logic.

Normal character-in switching is used to set the control counter or SMS register into the assembly register. Therefore, the operation and circuitry used is similar to that of accepting data from an I-O device. The control effect of the assembly ring is directly forced by decodings from positions 3-5 of the word counter.

A reset pulse is generated early in the CMMD cycle, A0(D3), and gated to the appropriate assembly register character position. For a count of zero, the reset is forced to character position 6; just as if the ICC count were six. A count of seven produces no valid assembly ring decoding (50.19.02.1). As a result, the A0(D3) reset pulse fails to be directed to any of the assembly ring positions and therefore performs no logic.

All during the CMMD cycle either the control counter or SMS register is gated to positions B-A-8-4-2-1 of the character-in switch depending on whether the count is 1-6 or 0. Following the reset pulse, "data accept," A5(D4), gates the character through the character-in switch and into the proper assembly register character position. A count of zero gates into character position 6 in the same manner as a WC = 6.

With a count of seven, "data accept" gates the control counter through the character-in switch, but at this point there is no further gating available to actually take the information to the assembly register. As a result, nothing is changed; no reset pulse is sent to the assembly register, and no effective gating is sent to the assembly register.

During the CMMD cycle a BCW request is initiated to the computer and the channel proceeds to the next command in sequence.

Transfer and Decrement Counter—TDC

Cyclic Makeup: BCW - CCC - CMMD

The TDC command (Figures 72 and 73) provides the programmer with a TIX-type channel operation. Its function is to test the control counter for zero condition. If the control counter is not zero, the command decrements the counter by one and transfers to a location specified by the address portion of the TDC command. If the control counter is zero, no decrementing is performed and the channel proceeds to the next sequential command.

The operation register, word counter, and address counter are set at 7 time of the BCW cycle and the decoder output becomes active at the next 0 time.

The next cycle (CCC) increments the command counter +1 in case the TDC does not execute a successful transfer. Outputs of the control counter are also tested during the early portion of this command counter cycle and if the counter is zero, a counter zero trigger is turned on.

During the CMMD cycle two conditions can exist. If the counter is not zero, a step control counter pulse is generated for the duration of the CMMD cycle (A10-A8) and the counter steps on the rise of the signal. At the same time that the stepping pulse is generated, a transfer gate trigger is turned on. Because this involves a successful transfer, the command counter is reset during A5(D4) of the CMMD cycle.

"Transfer gate" performs three essential functions:

1. It blocks the normal gating of the command counter to MAR during the next BCW cycle.

2. The address counter which contains the transfer address specified by positions 21-35 of the TDC command is gated to MAR.

3. The address counter is also gated to the command counter so that program sequence can be continued at the new location.

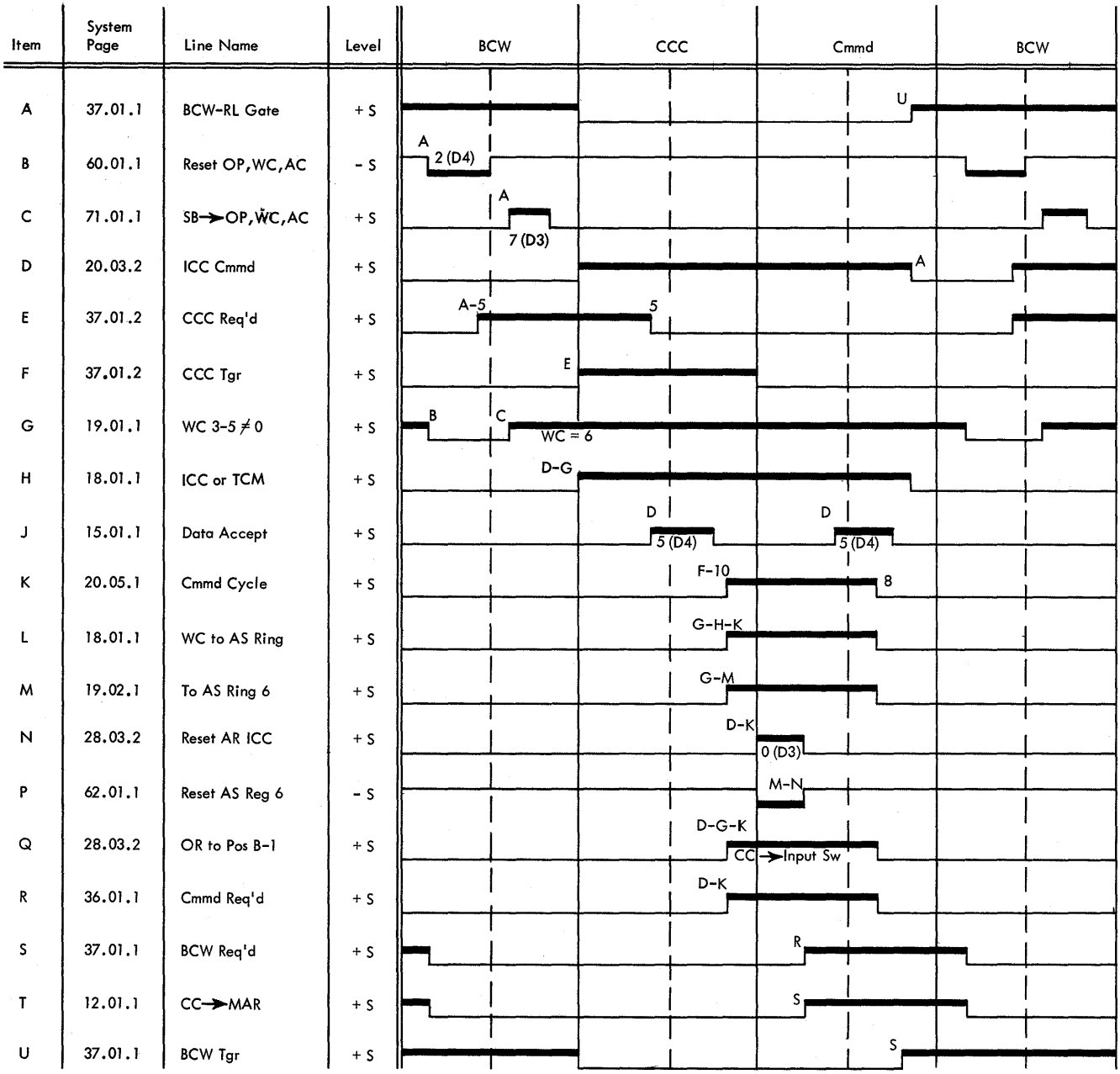


Figure 71. ICC Sequence Chart

If the counter is zero, the counter zero trigger blocks generation of a step control counter pulse, a reset to the command counter, and a "transfer gate." The result is that the command counter (containing the TDC location +1) is gated to MAR during the next BCW cycle and the program proceeds in sequence. The counter remains at zero and may be tested any number of times. The counter zero trigger is reset during each new BCW cycle.

Transfer On Conditions Met—TCM

Cyclic Makeup: BCW - CCC - CMMD

Transfer on conditions met (Figures 74 and 75) compares one of the six assembly register character positions or the check condition register to a mask con-

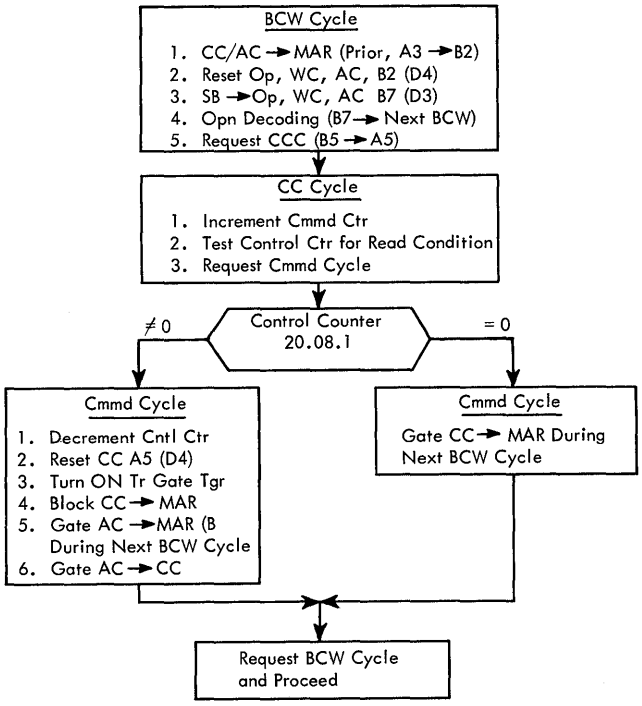


Figure 72. TDC Flow Chart

tained in positions 12-17 of the command. A count of 1-6 in positions 3-5 of the TCM command specifies character positions 1-6 of the assembly register; a count of zero specifies the six-position check condition register. A successful comparison results in a transfer to a location specified by positions 21-35 of the TCM command.

At 7 time of the BCW cycle, the operation register, word counter, and address counter are set; decoder outputs from 3-5 of the word counter immediately indicate a zero or non-zero condition.

The BCW cycle is followed by a command counter cycle (CCC) which increments the command counter in case of a non-transfer condition.

It is during the CMMD cycle that comparisons are made. A corresponding assembly ring output is brought up for a count of 1 through 6, and those assembly register bit positions are gated to the compare circuitry. The circuit consists of six EXCLUSIVE OR circuits which are fed information from the corresponding mask and assembly register positions. A match, which indicates that both conditions are the same (both +S or both −S), produces an active output to an AND circuit that also checks the other five EXCLUSIVE OR's.

A successful match results in a "transfer on compare" which causes an A5(D4) reset to the command counter. At the same time, a transfer gate trigger is turned on with the following effects:

1. The command counter to MAR circuitry is blocked during the next BCW cycle.

2. The address counter is gated to MAR to indicate the transfer location.

3. The address counter is gated to the command counter so that the sequence of commands can continue from the new address.

A non-successful match results in the contents of the command counter being sent to MAR during the next BCW cycle. The channel program continues in sequence.

A count of zero specifies a check condition register comparison against the mask. To accomplish this, "compare check conditions" is generated which gates the check condition triggers into the EXCLUSIVE OR comparison circuitry. The assembly ring in its reset condition, however, has trigger position 6 on; as a result, assembly positions 30-35 are always gated out. To eliminate this condition "AS ring 6" is blocked on 50.23.02.1 for any count other than six.

A count of seven prevents either the assembly register or check condition register from being routed to the EXCLUSIVE OR'ing. Therefore, an all-zero mask causes a match and corresponding transfer while any bit in the mask causes a non-match and no transfer.

A bit in position 11 of the TCM command specifies that a comparison should be made against only those mask positions which contain a 1. This is accomplished by bypassing the EXCLUSIVE OR circuitry and forcing a match for 0 bit positions; any positions containing a 1 bit must perform an EXCLUSIVE OR match, as explained previously.

When indirect addressing is used, control is transferred to the indirectly addressed location if the condition is met.

Transmit—XMT

Cyclic Makeup: BCW - CCC - CMMD - BDW (Write) - CMMD - BDW (Read) - ACC - CMMD - etc.

Transmit (Figures 76 and 77) moves data, commands or subroutines from one core storage location to another. The data to be transmitted must immediately follow the transmit command. Three counters keep account of the operation: the command counter specifies where data words are to be transmitted from (sending location); the address counter specifies where the data words are to be transmitted to (receiving location, specified by Y); and the word counter (C) specifies the number of words to be transmitted and stops the operation. If the initial count field is zero, the XMT com-

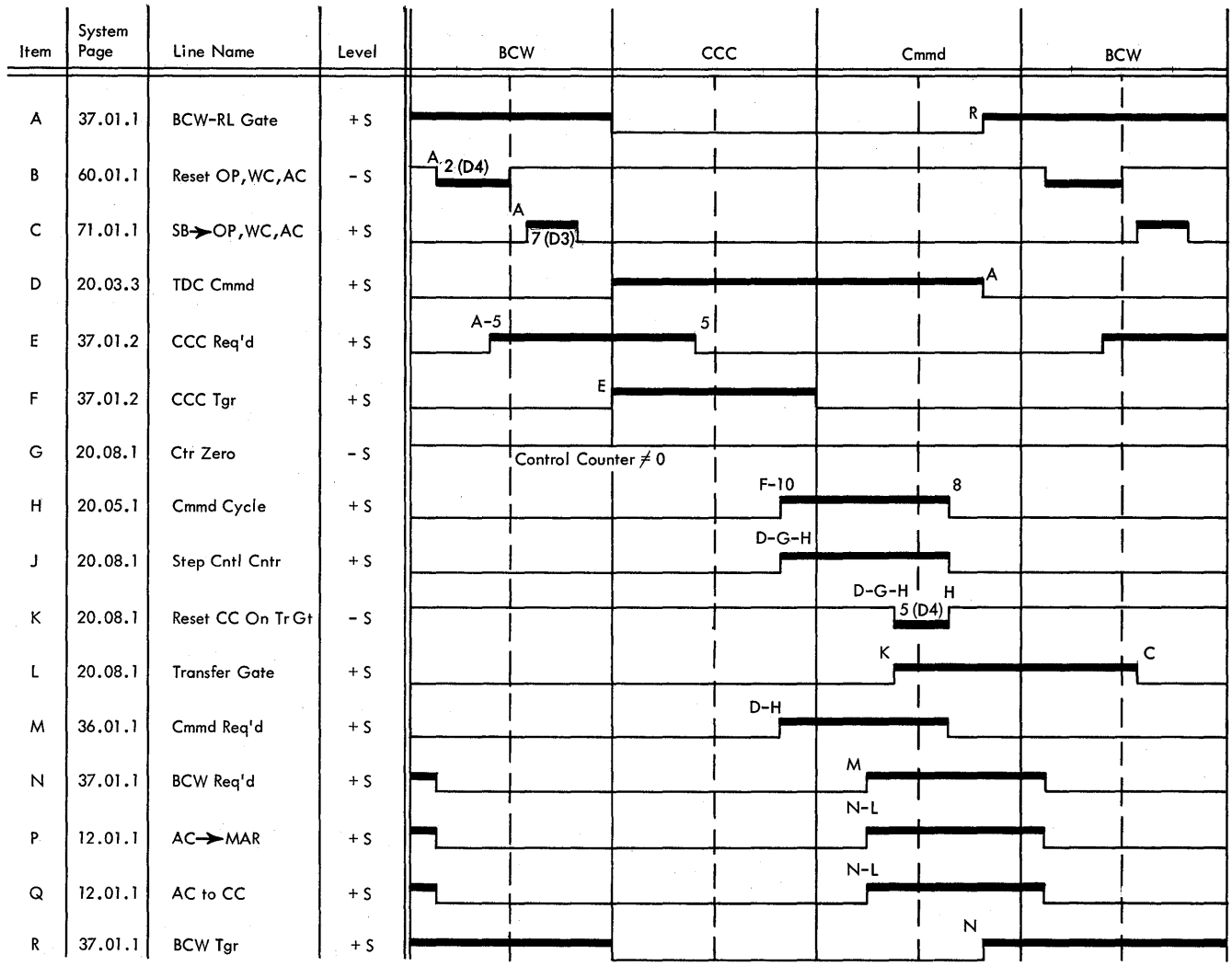


Figure 73. TDC Sequence Chart

mand is skipped and the channel proceeds to the next sequential command. The contents of the assembly register remain unchanged.

The operation is performed by requesting BDW cycles and alternating the channel between write and read status. The data register functions as an intermediate buffer during the operation; first, accepting the data from core storage during the write BDW cycle, and second, sending the data back to core storage during the following read BDW cycle. Two BDW cycles are required for each word transmitted. Each BDW cycle Transmit (Figures 76 and 77) moves data, commands, initiates priority and waits for B time; the amount of time is dependent on the system demands and configuration.

The transmit command is loaded into the operation register, word counter, and address counter at 7 time of the initial BCW cycle. The next cycle (CCC) increments the command counter value, which represents the first transmitting address of data. Only one command counter cycle occurs during the transmit operation; the command counter is incremented at other times but adder controls are initiated by other circuitry.

A binary trigger called "transmit gate" is used to alternately switch the channel between write and read status during the subsequent BDW cycles. It also determines whether the command counter or address counter is gated to MAR at the beginning of each BDW cycle. (The transmit command is the only case where the command counter is gated to MAR during a BDW cycle.)

The first CMMD cycle turns the transmit gate trigger on at 2 time, places the channel in write status, requests a BDW cycle, and gates the command counter to MAR.

The next BDW cycle resets the data register at B2(D4) and sets it again to the new data word at B7(D3). This cycle also functions as a CCC; the command counter is

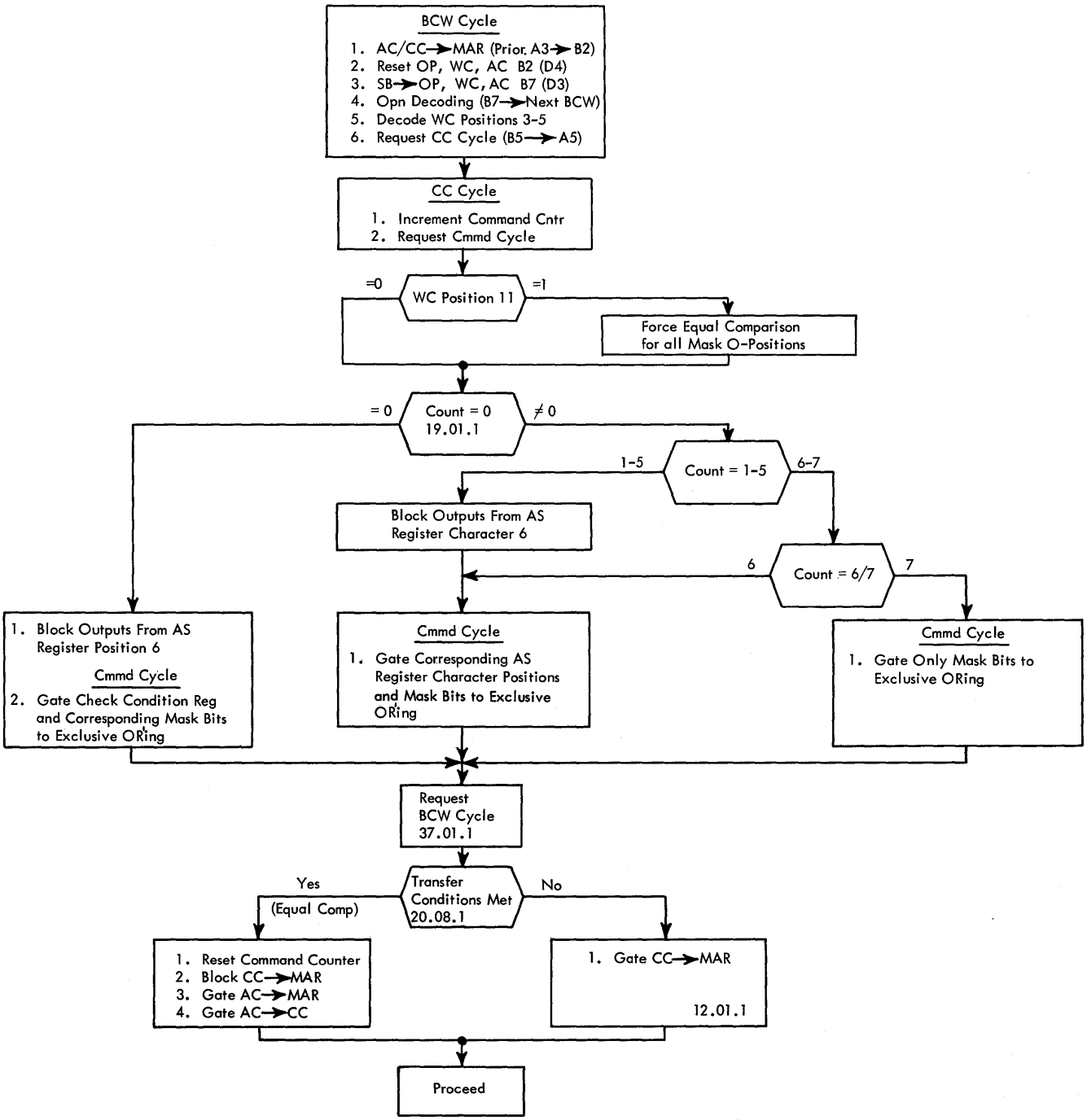


Figure 74. TCM Flow Chart

incremented through the adders to indicate the next data word location. Address counter and word counter circuitry are blocked and the CMMD cycle trigger turned on at 10 time of the BDW cycle.

The second CMMD cycle turns off (flips) the transmit gate trigger, places the channel in read status, requests a BDW cycle, and gates the address counter to MAR.

This second BDW cycle gates the data register to the storage bus through 8 time and therefore, completes the transmission of one data word. The BDW cycle, which normally functions as a word counter cycle, is allowed to decrement the word counter through the adders. At this point, the word counter indicates the number of words remaining for transmission.

During the prior BDW cycle a request is made for an address counter cycle. As a result, the next cycle increments the address counter through the adders to indicate where the next data word is to be transmitted.

The address counter cycle also requests a new CMMD cycle and the process repeats. If, at this point, the

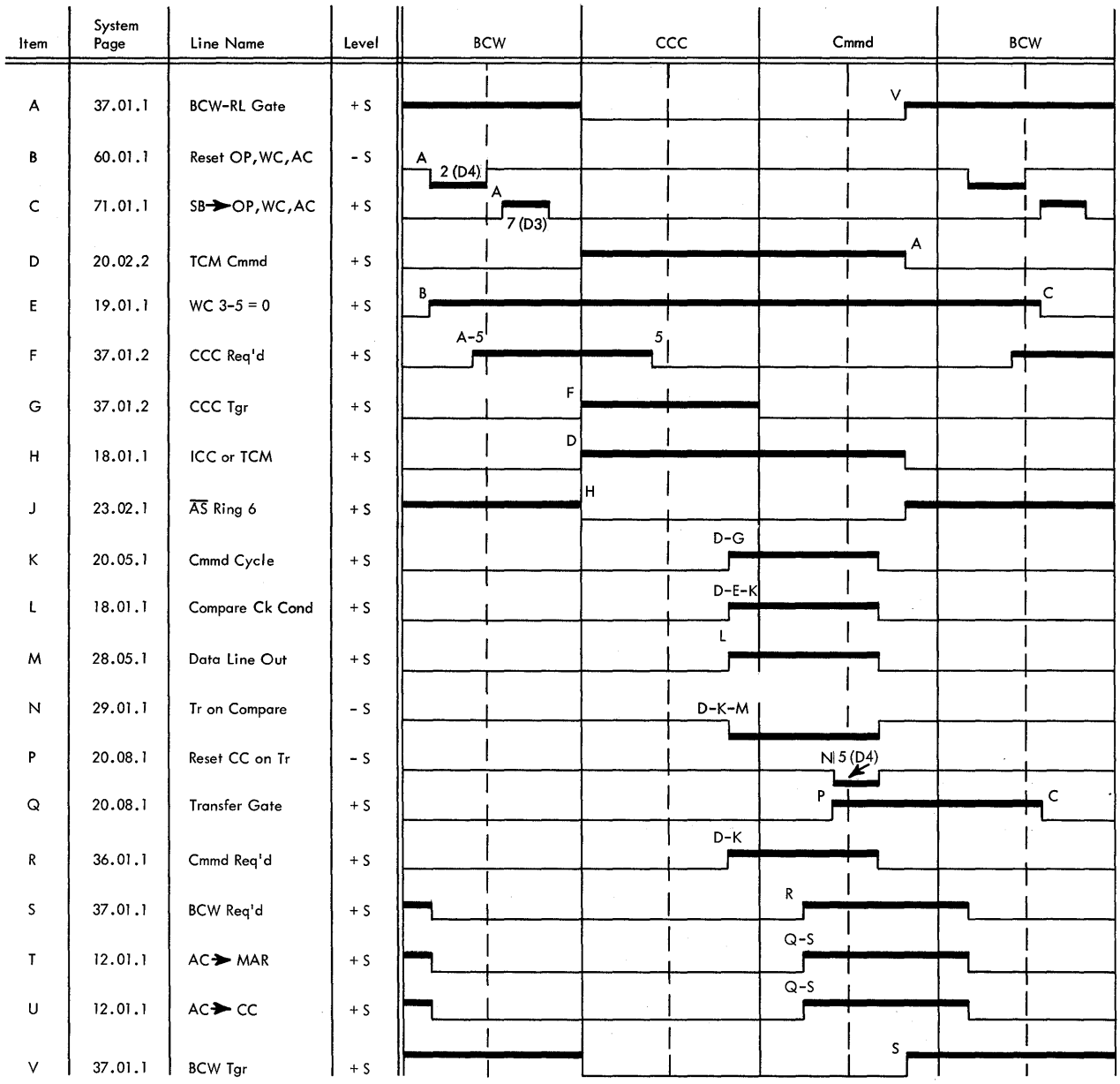


Figure 75. TCM Sequence Chart

word counter is zero, a BCW cycle is requested and the channel proceeds to the next command as indicated by the command counter.

A functional summary of the CMMD and BDW cycles is as follows:

Even CMMD Cycles

WC ≠ 0

Turn the transmit gate trigger on
Set write status in the channel
Request a BDW cycle
Gate CC to MAR

WC = 0

Request a BCW cycle
Gate CC to MAR

Odd CMMD Cycles

Turn the transmit gate trigger off
Set read status in the channel
Request a BDW cycle
Gate AC to MAR

Even BDW Cycles

Load the data register from core storage
Increment the command counter through the adders
Request a CMMD cycle

Odd BDW Cycles

Send contents of the data register to core storage
Decrement the word counter through the adders
Request an address counter cycle

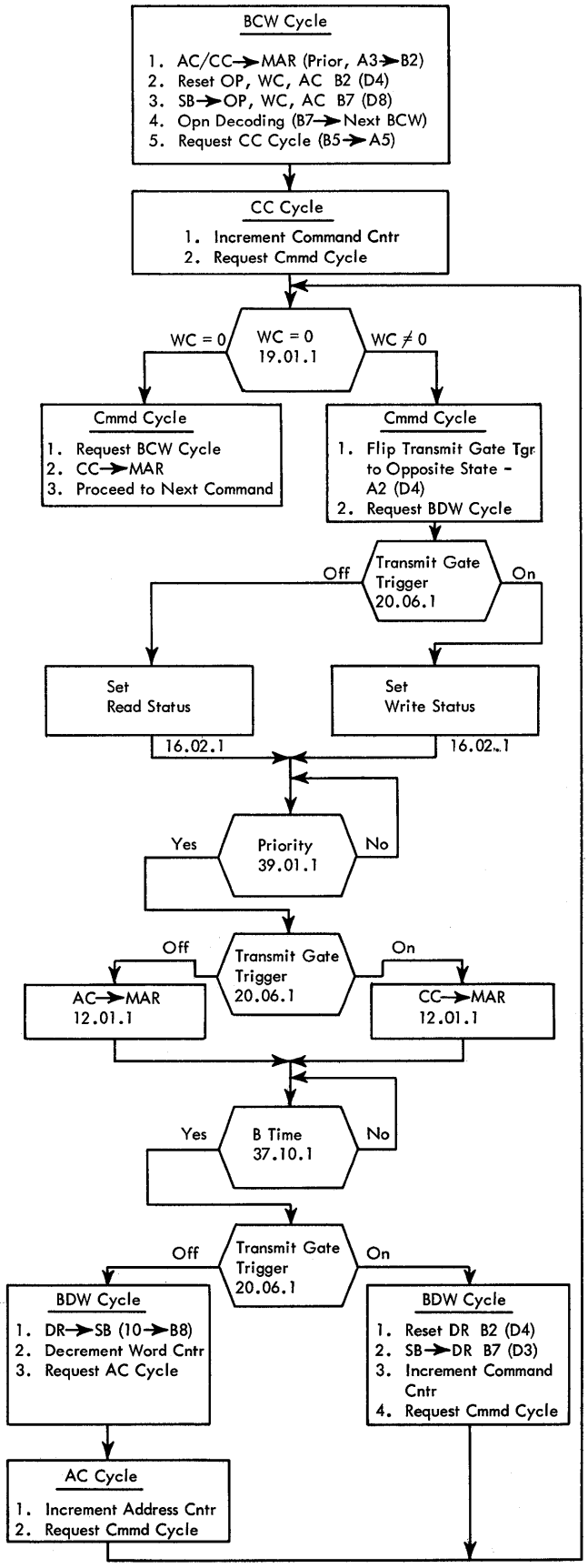


Figure 76. Transmit Flow Chart

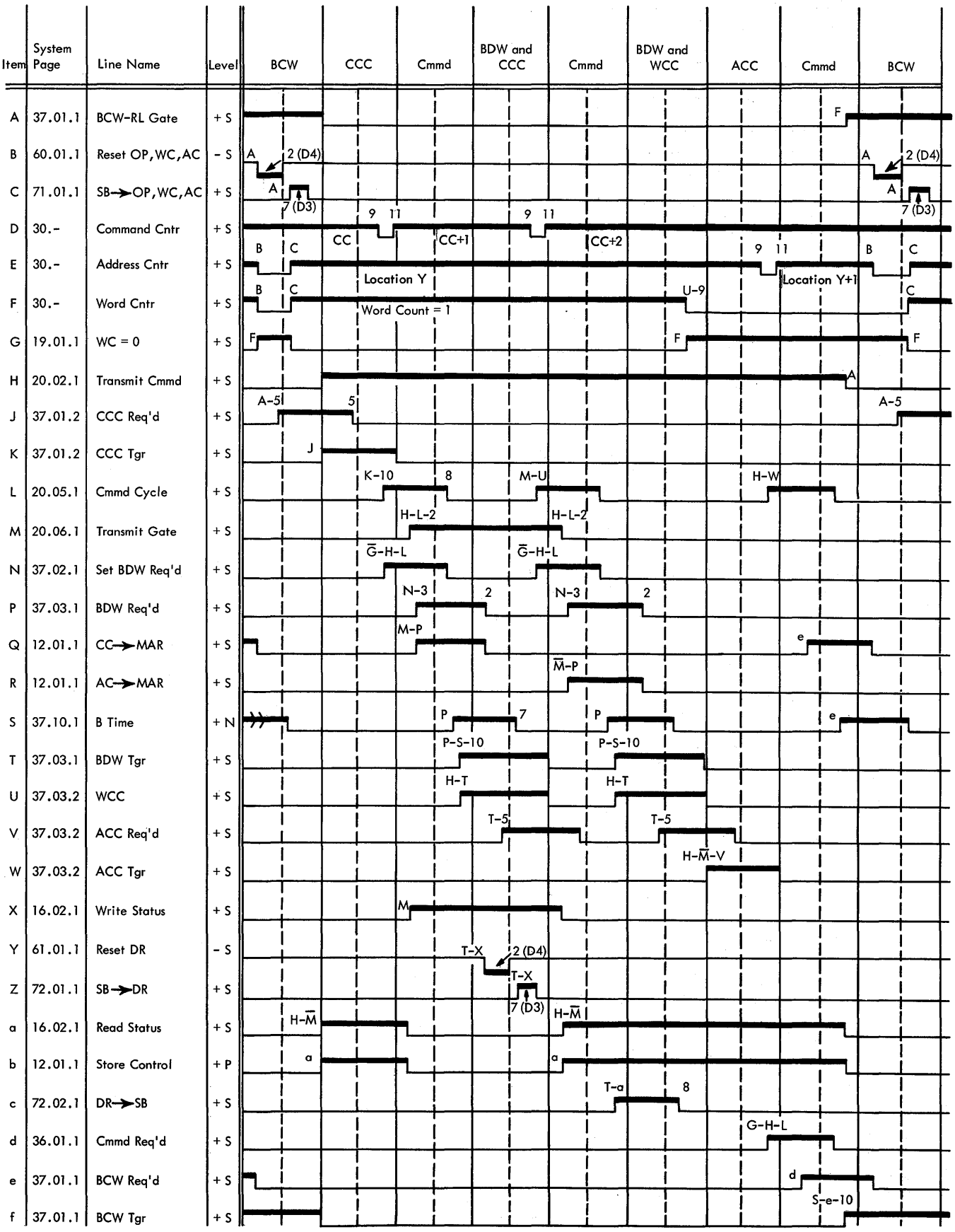


Figure 77. Transmit Sequence Chart

During data flow, the channel is in either a write or read status. Write status indicates that the system is in the process of taking data out of core storage. Read status, on the other hand, indicates that the system is in the process of placing data into core storage. These two status conditions are generally associated with I-O operations but could apply equally well to the internal data flow of transmit (XMT), load assembly register (LAR), store assembly register (SAR), or other channel commands.

The flow of data from computer core storage to the I-O adapter is accomplished as follows: a BDW cycle is obtained during which a data word is transmitted from a specified core storage location to the channel data register; then the data word is transferred to the assembly register where it is fed to the character register one character at a time. From the character register, the data are sent across the interface.

During read operations, the steps are reversed. A data word is assembled one character at a time until the assembly register is full. At this point, the complete word is transferred to the data register until such time that a BDW cycle can be obtained to place the data word into core storage. In both operations the data register is acting as an intermediate buffer between core storage and the assembly register to allow for differences in I-O character rates and time required to obtain core storage reference cycles.

Data flow across the interface lines must be controlled by the I-O adapter. This is necessary because the channel has no way of knowing the character rate or physical speed of the I-O device. "Service request" from the adapter signals the need for data flow; in return, "service response" from the channel signals mission accomplished. What specifically takes place during the time between these two pulses depends on the nature of the operation; i.e., read or write.

For continuity, the following discussions will be specifically directed at I-O operations even though other channel commands may produce a similar sequence of events. Also, to eliminate unnecessary and repetitious circuitry, the associated figures are limited to the eight-bit and four-bit lines as affecting data register and assembly register trigger positions 2 and 3.

Both the read and write BCD translator circuits are omitted here; they are covered in another section in detail.

Writing

Core Storage to Channel

The basic control line for a write operation (Figures 78, 79, 80, and 81) is "write status" and can be activated by any of the interface commands except SNS. Either CTLW, CTLR, or CTL turns on the control gate trigger (50.20.07.1) and brings up "write status" at O_1. Each of these commands is concerned with the transfer of an order to the I-O adapter and must, therefore, place the channel in a write status until end time. A CTLW followed by either a CPYP or CPYD command turns on the write trigger (50.16.01.1) which will in turn hold the channel in write status for the remainder of data transmission.

During writing operations there should always be a buffer of one data word available in the data register, ready to be sent immediately to the assembly register, character register, and out on the write bus. The data register loaded trigger constantly indicates the logical status of the data register contents; it is this trigger, therefore, that controls the requests for BDW cycles and the obtaining of new data words.

Logically, during a write operation whenever the data register is not loaded and the word count is not zero, a BDW cycle must be requested. These basic conditions are met at A_2 (Figure 78). The immediate result is that the BDW required trigger is turned on and a B cycle is requested from the computer at O_6 and A_{11}. With priority and B time available, the address counter value is sent to MAR at A_5 and the BDW trigger is turned on at A_{12}.

Since this is a write BDW cycle, information is brought from core storage and placed in the data register as follows:

1. The location specified by the channel address counter (CAC) is sent to the memory address register (MAR) as just explained.
2. The data register is reset early in the BDW cycle (A_{17}).
3. The storage bus lines are sampled into the data register (A_{21} and A_{22}).
4. The data register loaded trigger is turned on (A_{15}).
5. The word counter is decreased by one.
6. An address counter cycle is initiated to increase the address counter by one.

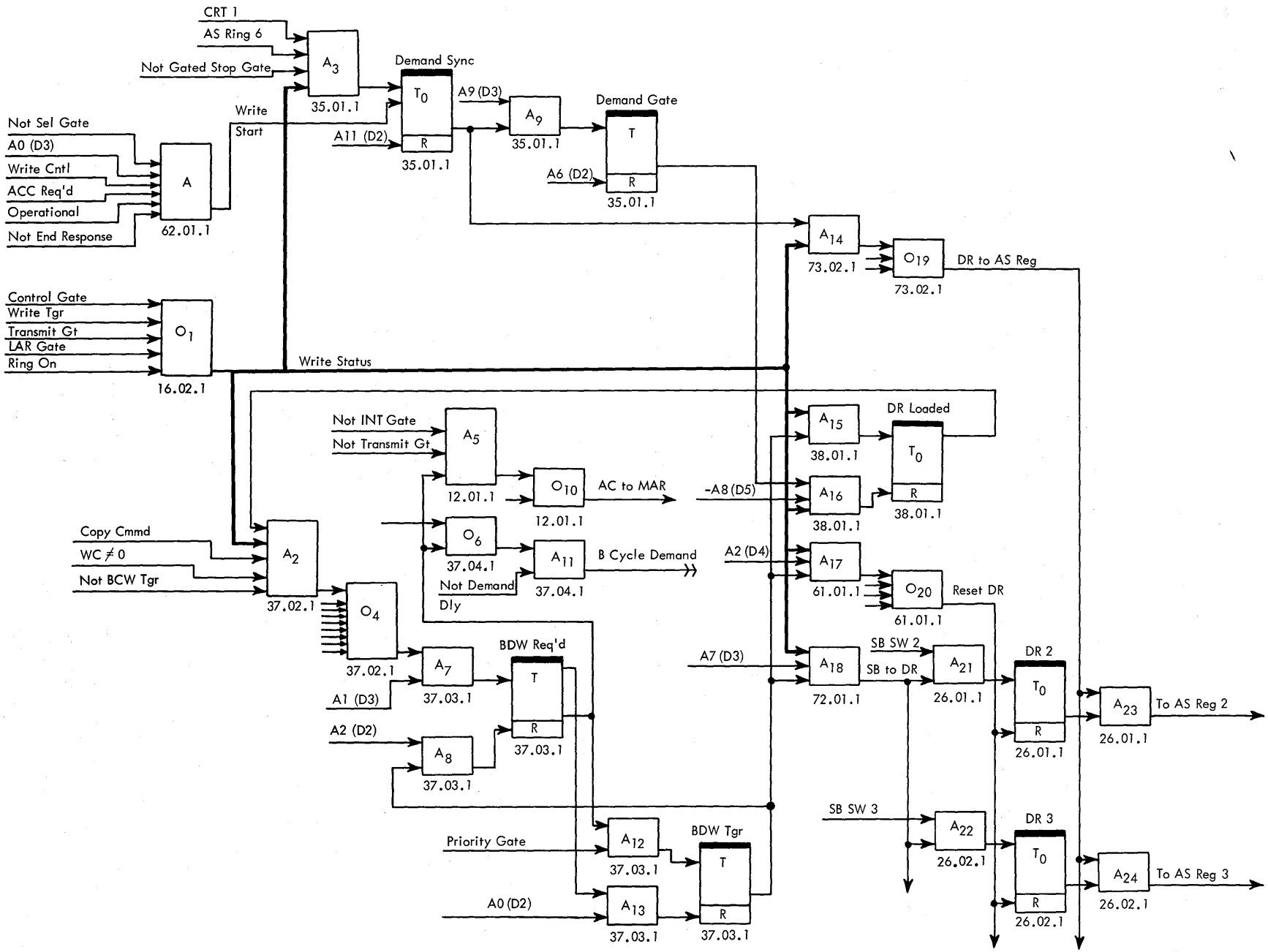


Figure 78. Core Storage to Channel

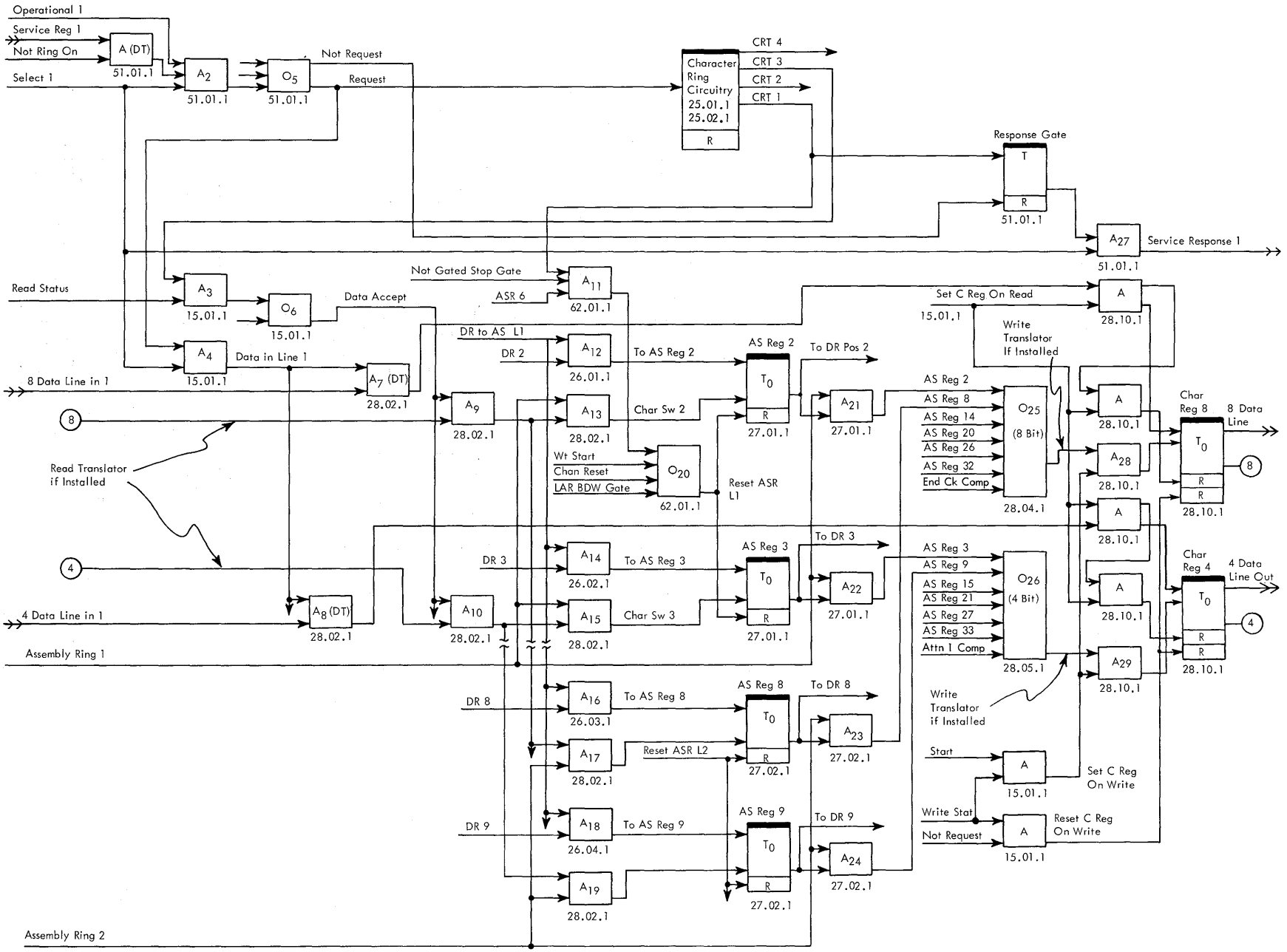


Figure 79. Assembly Register In/Out Character Switching

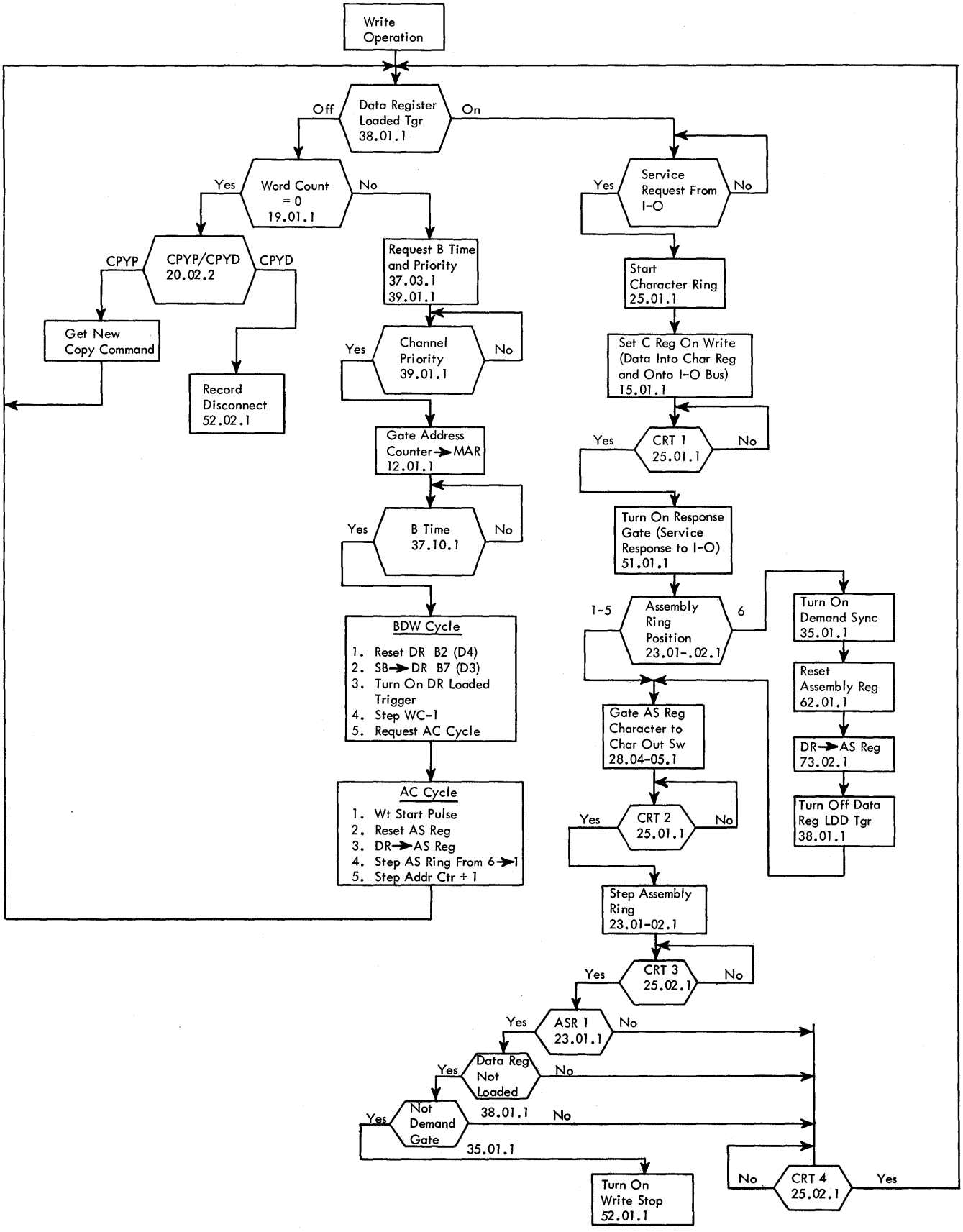


Figure 80. Channel Write Operation Flow Chart

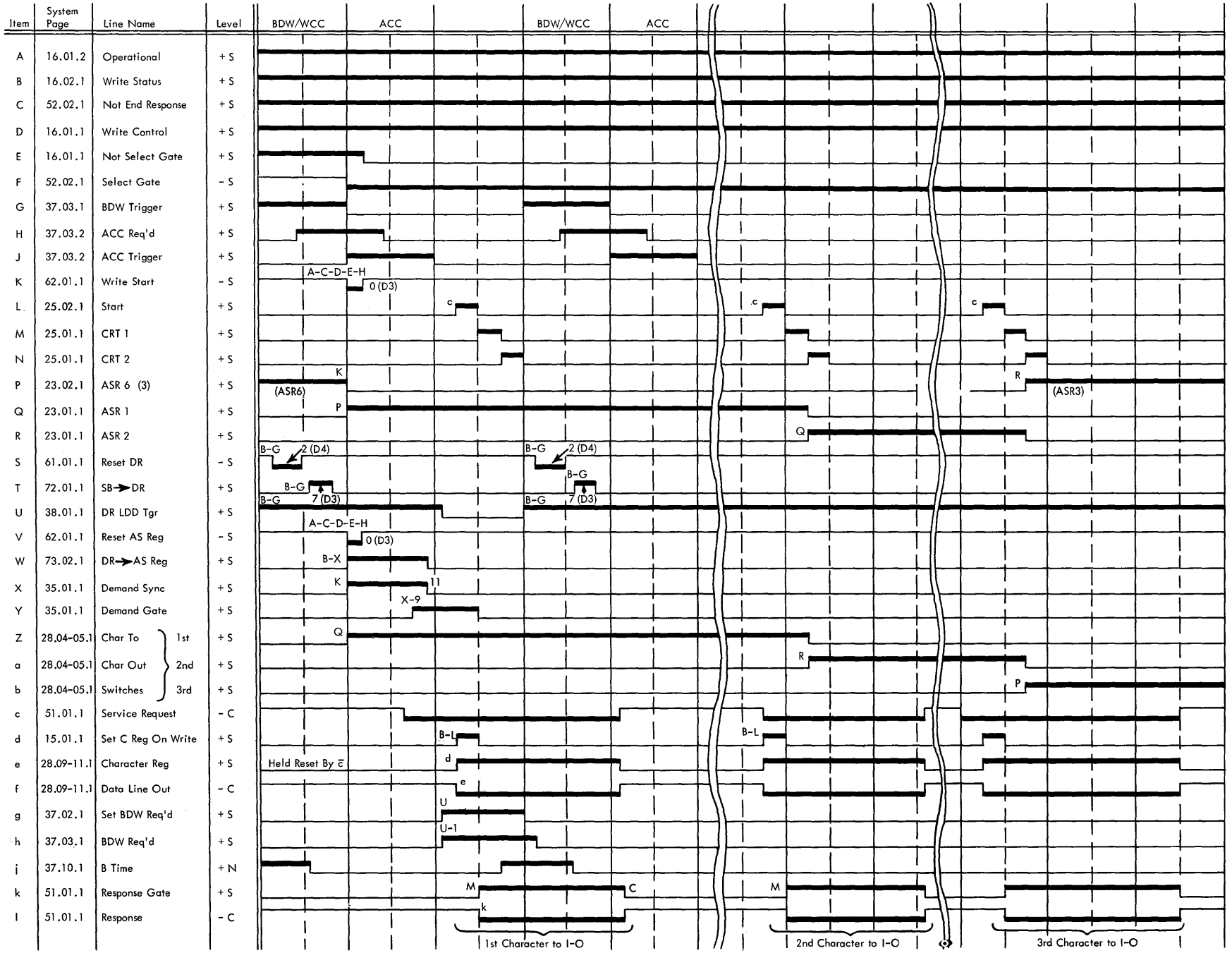


Figure 81. Channel Write Operation Sequence Chart

No further requests for B time are necessary until the data register contents are transferred to the assembly register. This transfer results from a "demand sync" which is generated either by the write start pulse for the first word or by assembly ring 6 and CRT1 for all succeeding words until disconnect. If the assembly register is at position 6, the demand sync trigger is turned on by A_3 (Figure 78). A_{14} produces DR to AS register and the data register outputs are gated to their respective assembly register trigger positions. With the data word now in the assembly register, the data register is no longer logically loaded; therefore, the data register loaded trigger is turned off by A_{16} and the channel immediately initiates a new B cycle request at A_2. Note that even though the trigger was turned off, the data register still contains the information and is not reset until the next BDW cycle. This sequence of events continues until an end or unusual end terminates the operation.

NOTE: Although select gate becomes active at 0 time of the AC cycle (Figure 81, line K), circuit delays prevent "not select gate" from falling instantaneously and thus the A0(D3) pulse gets through to generate "write start."

Channel to I-O

Data flow from core storage to the I-O device (Figures 79, 80, and 81) requires three steps:

1. A data word is obtained from core storage and placed into the data register during a BDW cycle.
2. The full word is then transferred in parallel from the data register to the assembly register.
3. The six character bytes are then sent, in sequence, over the interface write bus to the I-O adapter.

Items 1 and 2 were discussed in the previous section; item 3 is directly concerned with service requests from the adapter.

Initially, the write start pulse steps the assembly ring from 6 to 1 and turns on the demand sync trigger (Figure 78). Demand sync causes the data register outputs to be sampled into the corresponding assembly register positions. Using assembly register position 2 (Figure 79) as an example, A_{12} sets the trigger. The assembly register is reset by A_{11} at the same time that the data word is being transferred. However, the reset pulse is shorter than the demand sync and thus the transfer is successful. For all succeeding words, service request will generate CRT1 which will turn on demand sync at assembly ring 6 time to gate another word from the data register to the assembly register.

With the data in the assembly register, each of the six-bit characters must be gated to the character register and out onto the write bus line. The proper character sequence is under control of the assembly ring. The output of assembly register position 2 and AS ring 1 now conditions A_{21} (Figure 79) which in turn brings up the output of the character out switch at O_{25}.

The start pulse generates "set C reg on write" which gates the bits of the character into the character register. From the character register, the bit is immediately sent across the interface. The character register is reset by the fall of service request and held in the reset condition as long as "request" is down.

Response gate is turned on by CRT1 and 0.5 μs later gates out "service response" at A_{27}. The difference in time assures that the character is valid on the write bus by the time service response tells the adapter to accept it.

When the character has been accepted, "service request" falls at A_1, the out of phase output of O_5 turns the demand gate trigger off, and the service request and data output lines are deactivated.

The character is sent out on both interface write buses, but only one interface will be selected and able to accept the information.

Reading

I-O to Channel

During read operations (Figures 79, 83, and 84) information must be valid on the interface read bus at the time "service request" arrives at the channel. Each request from either interface will, again, start the character ring and step the assembly ring to its next position. If the assembly ring is at position 6, the assembly register must be reset because a new data word is being received. The reset pulse is produced at A_{11} (Figure 79) during CRT1 time. At CRT2 time, the assembly ring is stepped to position 1.

Two sets of read buses may feed into the data channel. The adapter, which is not selected by the system, may have information on its read bus because of a shared operation, but the correct read bus must be gated into the channel circuitry. "Data-in line 1" at A_4 gates the read bus information to the computer through A_7. "Set C register on read," which is generated by "read status" and "start" on 50.15.01.1, gates the character into the character register. At CRT3 time "data accept" (generated at O_6) gates the information into the character switch in circuitry at A_9. At this point, the assembly ring output determines which one of six-character positions of the assembly register receives the data. This character-in switching allows all of the bytes which come in on a common bus to be routed and stored into sequential character positions of the assembly register.

Sending a response back to the adapter is the same as explained for a write operation; the response gate

trigger is turned on at CRT1 time and "service response" is immediately gated to the I-O adapter by either "select 1" or "select 2."

Channel to Core Storage

Read status at O_1 (Figure 82) results from an SNS or CTLR command when operating with an I-O device. SNS is concerned with sense data from the adapter while CTLR is concerned with information data from the I-O device; however, the channel makes no distinction with respect to getting the data words into core storage.

As a byte of data fills assembly register position 6 at CRT3 time, A_4 senses that the assembly register is full and immediately initiates circuitry to transfer the data word to the data register. This transfer must be accomplished before the next byte of information arrives from the I-O adapter.

The demand gate trigger is turned on via A_4, the demand sync trigger, and A_{10}. At this time the channel performs the following functions:

1. The data register is reset (A_{17}, O_{22}).
2. The assembly register is sampled into the data register (A_{16}, O_{21}, A_{23}, and A_{24}).
3. The data register loaded trigger is turned on (A_{19}).
4. The BDW required trigger is turned on (A_2, O_5 and A_8).
5. A B cycle is requested from the computer (O_7 and A_{12}).
6. The channel address counter is gated to the memory address register (A_6 and O_{11}).
7. When B time and priority are available, the BDW trigger is turned on. Information in the data register is gated to the storage bus (A_{18}, A_{25}, and A_{26}), and the data register loaded trigger is turned off (A_{20}).

Note that a request for B time occurs simultaneously with the transfer of data from the assembly register. This provides a maximum possible amount of time for the channel to obtain priority and a core storage cycle from the computer before the assembly register is filled with a new word from the I-O device.

During read, it is possible to reach the end of a record without completely filling the assembly register with six characters. In this event, A_4 will not be active to initiate the data transfer to core storage. Instead, A_3 detects the fact that the end of the record has been reached without the assembly ring being at position 6 and initiates the circuitry to store this last incomplete word.

Stop Condition

A stop signal is concerned with data transmission and tells the I-O device that the channel has recognized an end of record or operation. When the I-O device receives the stop signal, it immediately proceeds to its normal ending point.

The four interface commands (CTL, CTLW, CTLR, or SNS) may be terminated either by end signals received from the adapter or specific conditions recognized within the channel itself. The latter causes the stop condition.

The channel produces a stop signal under two main conditions: the word count of a CPYD command has gone to zero during a read or write operation; or, an error condition (I-O, sequence, or interface check) has been detected while executing one of the four interface commands.

Stop Condition Operation

The normal stop condition (Figures 85, 86, and 87) occurs during a read or write operation when the word count of a CPYD command has been reduced to zero. This zero condition is recognized at A_1 (Figure 85). If the channel is in read status, an immediate stop is initiated by A_4 when the BDW cycle stores the last word.

During a write operation, the word count goes to zero when the last data word is brought to the data register; the stop condition must be delayed, however, until after these last six characters have been sent across the interface. These requirements are met at A_3. As the sixth character is sent from the assembly register to the I-O device, write status finds the data register not loaded. This signifies that no more data are coming (end of the record) and turns on the write stop trigger to stop the operation.

If an error occurs during data transmission, the record is invalid. Therefore, the operation should be terminated immediately so that an interrupt can allow the channel program to test and restart the operation with a minimum of lost time. The three error conditions are recognized at O_2, and, as explained previously, remain on throughout the interrupt program. Once in an interrupt program, an SNS command is normally executed to test the I-O status conditions. "Not interrupt" at A_5 allows the SNS command to execute properly, by preventing the generation of a second stop signal.

The main conditions initiating a stop are recognized at O_7; however, further restrictions are encountered at A_8. First, stop signals should not be sent to an adapter which is not operational. Second, to comply with the I-O interface standards, a stop signal may not occur when a "service request" and "service response" are both up. "Not request" delays the stop signal until the service request from the adapter has fallen. The 1.0 μs single-shot provides a one-time setting of the stop trigger.

It is possible for the word count of a CPYD command to become zero at the same time that the adapter rec-

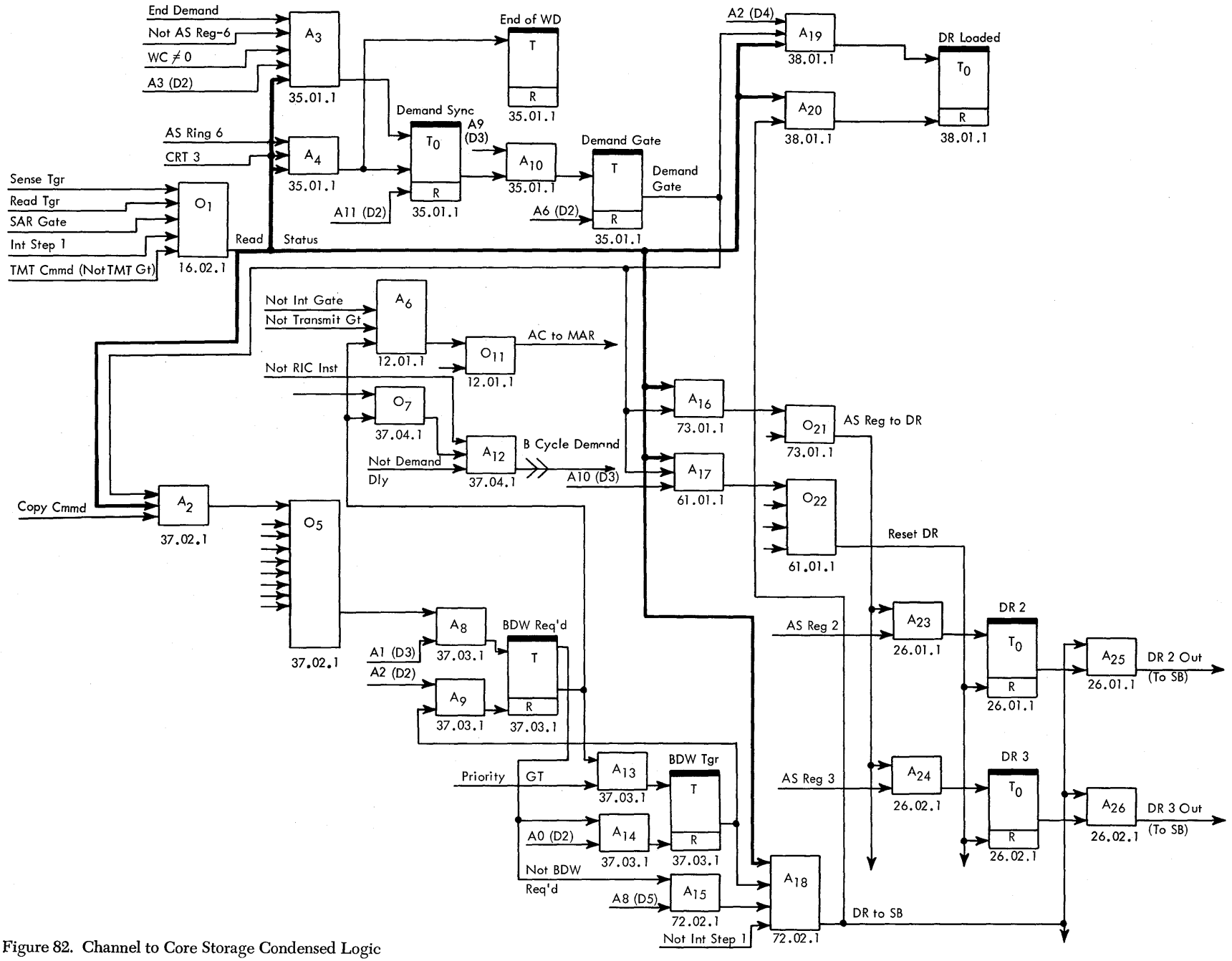


Figure 82. Channel to Core Storage Condensed Logic

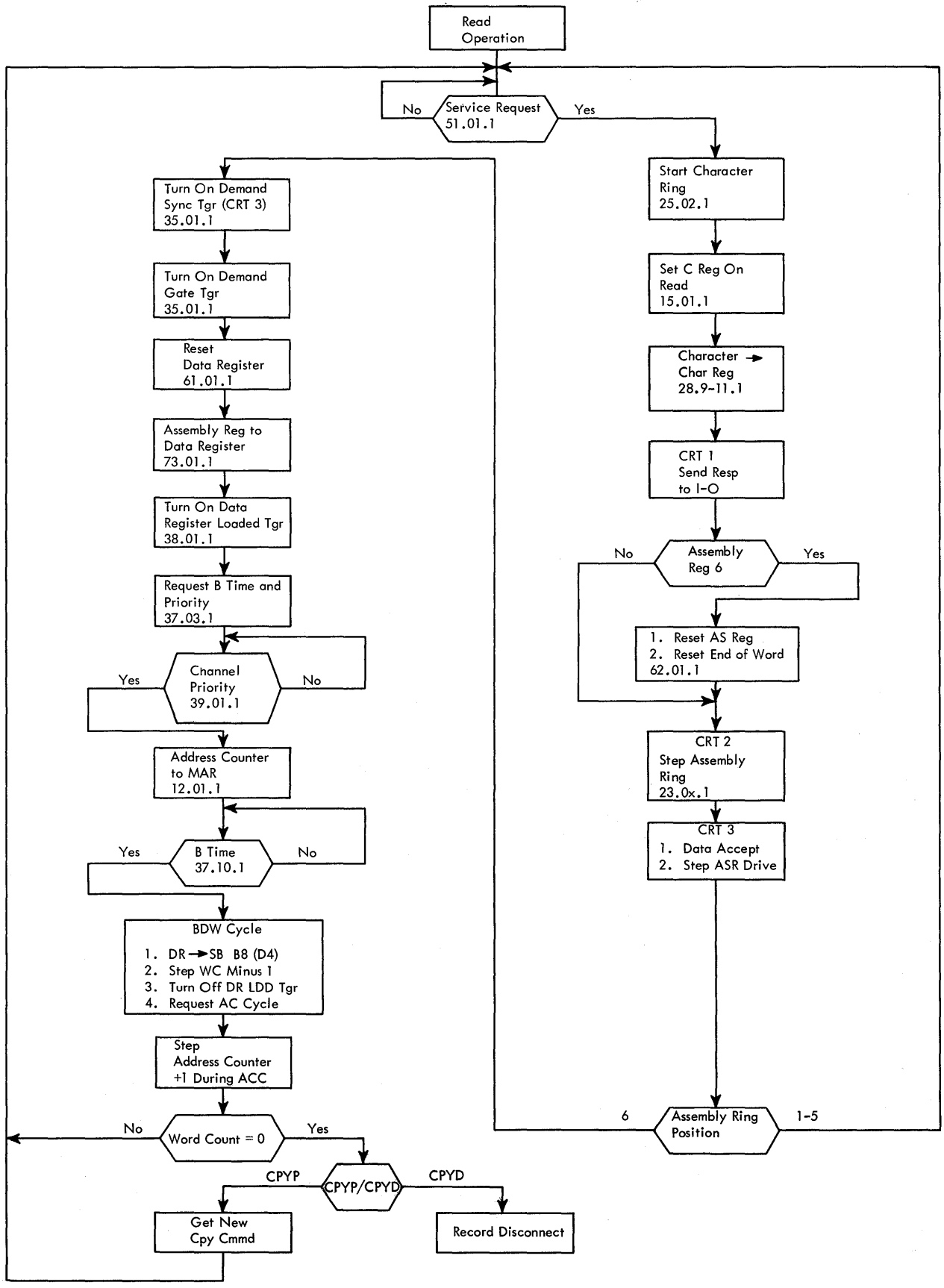


Figure 83. Channel Read Operation Flow Chart

Item	System Page	Line Name	Level
A	16.02.1	Read Status	+ S
B	26.01.1	Data Register	+ S
C	27.01.1	Assembly Register	+ S
D	28.02.1	8 Data Line In 1	- C
E	51.01.1	Service Request	- C
F	15.01.1	Data In Line 1	+ S
G	25.02.1	Start Tgr	+ S
H	23.01.1	AS Ring	+ S
J	23.02.1	AS Ring 6	+ S
K	25.01.1	CRT 1	+ S
L	25.01.1	CRT 2	+ S
M	25.02.1	CRT 3	+ S
N	25.02.1	CRT 4	+ S
P	62.01.1	Reset AS Reg	- S
Q	15.01.1	Data Accept	+ S
R	51.01.1	Response Gate	+ S
S	51.01.1	Service Response	- C
T	35.01.1	Demand Sync	+ S
U	35.01.1	Demand Gate	+ S
V	73.01.1	AS Reg to DR	+ S
W	61.01.1	Reset DR	- S
X	38.01.1	DR Loaded Tgr	+ S
Y	37.03.1	BDW Req'd	+ S
Z	37.04.1	B Cycle Demand	+ P
a	12.01.1	AC to MAR	+ S
b	37.10.1	B Time	+ N
c	39.01.1	Priority Gate	+ S
d	37.03.1	BDW Tgr	+ S
e	72.02.1	DR to SB	+ S
f	15.01.1	Set C Reg On Rd	+ S
g	15.01.1	Data In Line	- S
h	28.10.1	Char Reg 8	+ S
j	28.02.1	Char Reg ➔ ASR	

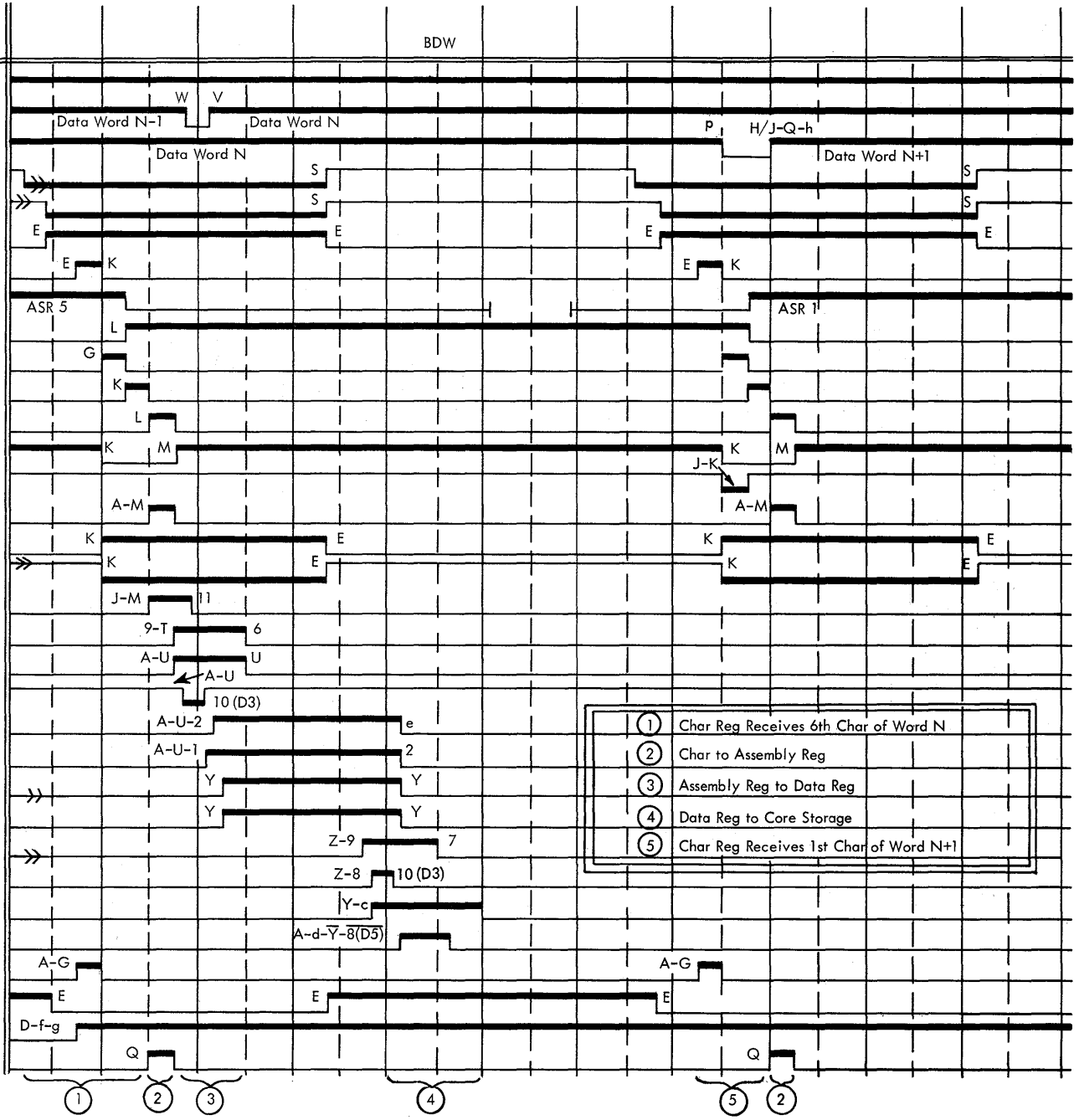


Figure 84. Channel Read Sequence Chart

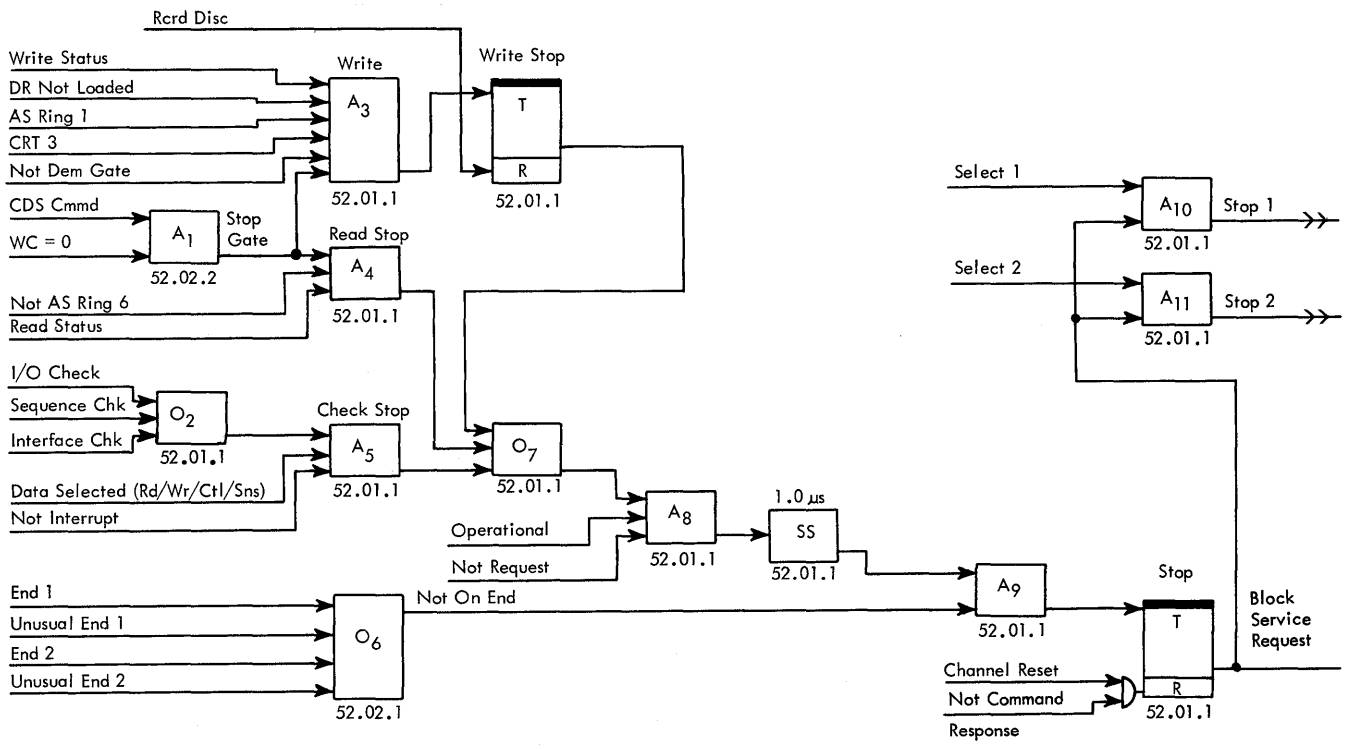


Figure 85. Stop Condition Condensed Logic

ognizes an end or unusual end condition. If the adapter recognizes an end first, the stop signal is prevented by the output of O_6 at A_9 to satisfy the interface standards.

The stop signal at A_{10} or A_{11} causes the adapter to complete its ending procedures and returns an end or unusual end signal to the channel. At this time the operation is completed; command response falls and the stop trigger is reset.

The sequence chart, Figure 87, shows a normal stop condition for a channel in write status and under control of a CPYD command. The word count is assumed to go to zero before an end signal is received from the adapter. The break in the sequence chart indicates that there could be a considerable time lag between the point of turning on the stop trigger and the arrival of a resulting end.

End Condition

"End" signals the channel that the I-O adapter has recognized the normal ending of an operation; "unusual end" signals that the operation being executed has resulted in an unusual condition and has been terminated. The adapter sends either one or the other—not both. In either case, the channel replies with an "end response."

Ends or unusual ends may have been preceded by a stop signal from the computer. (For further explanation, see the section on "Stop Condition.")

Unusual ends, if not disabled by an SMS command, cause a channel interrupt; normal ends do not.

Ends and unusual ends are concerned with the four interface commands and their transmission of data, control, or status information. The ultimate effect on the channel and adapter, after end response has been returned, is determined by whether the operation is under control of a CPYP or CPYD command.

A CPYP command services any normal end signal and then causes the adapter to continue with the read, write, or sense operation. (A CTL operation does not use copy commands.)

A CPYD command also services the end signal but does not reinitiate the operation to the adapter. The read, write, control, or sense operation is reset whether or not the word count has been reduced to zero, and a new control word cycle is requested.

End Condition Operation

End signals (Figures 88, 89, 90) are received from either interface at A_1, A_2, A_3, or A_4 (Figure 88), provided the channel is not in manual, off-line status. An A0(D2) pulse turns on the end demand trigger through A_9 or A_{10} and an A3(D2) turns on the end sync trigger through A_{13}. "End sync" degates A_9 and A_{10} to prevent a second setting of the end demand trigger from the same end signal.

If this end occurs during a read operation, the assembly register could contain a partial word which must

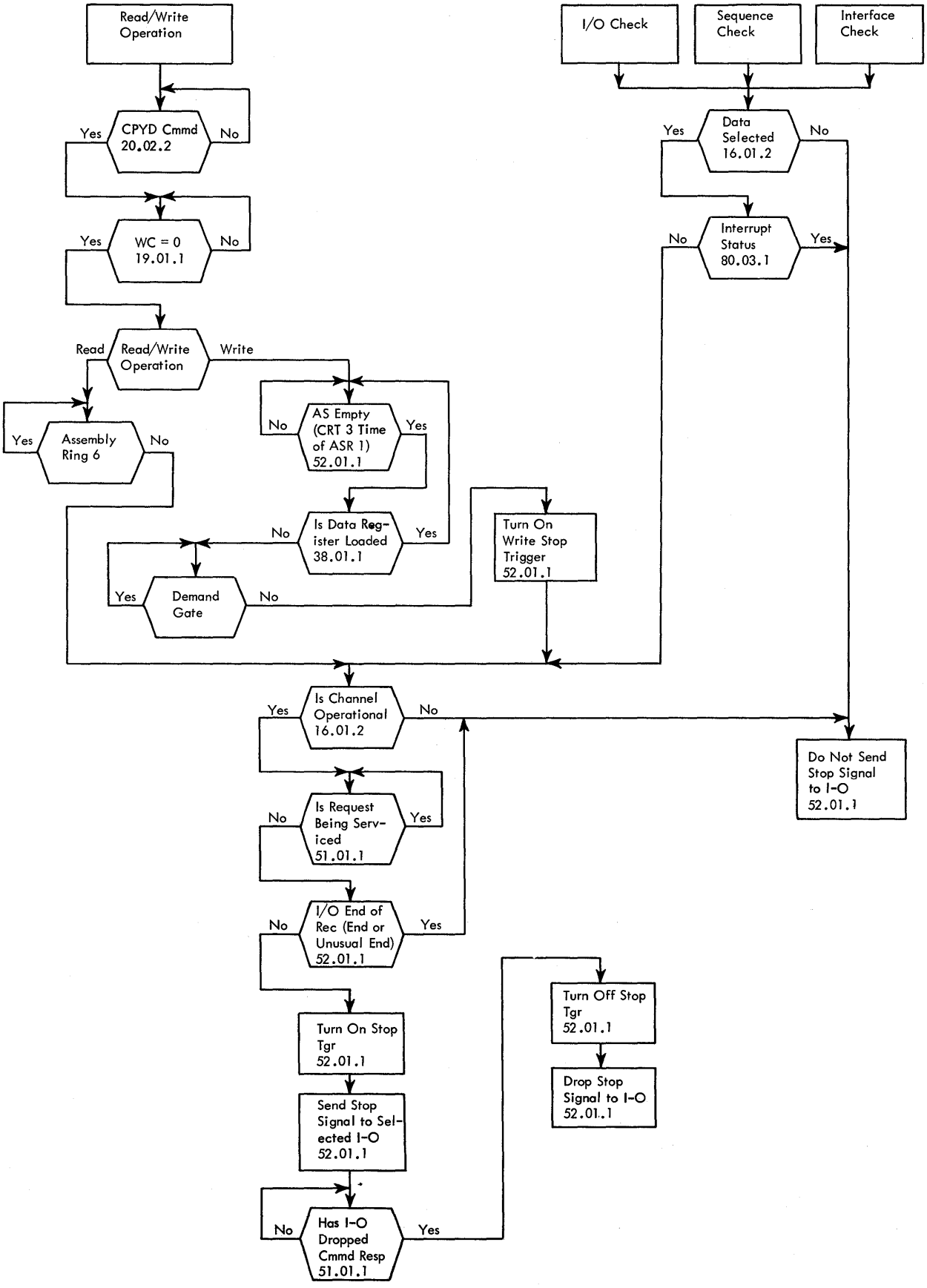


Figure 86. Stop Condition Flow Chart

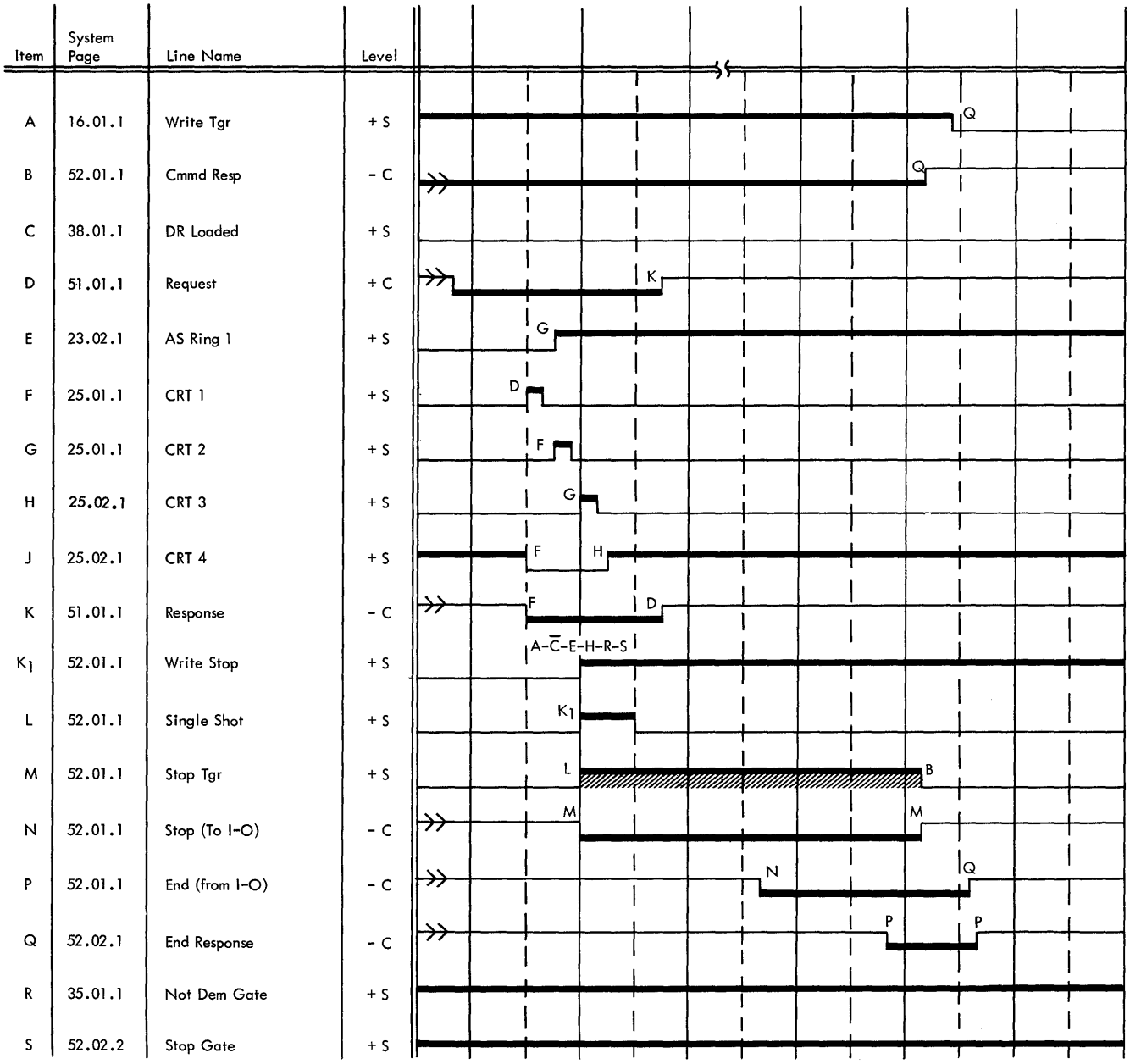


Figure 87. Stop Condition Sequence Chart

be stored before proceeding. "End demand" accomplishes this by turning on the demand gate trigger (50.35.01.1), transferring the partial word to the data register, and requesting a BDW cycle.

"End sync" holds the select gate trigger reset, dropping the read or write interface command line at A_{20} or A_{21}. Dropping this line tells the I-O adapter that the channel has completed this record; in return, the adapter drops its command response signal.

The end response trigger is turned on through A_{16} or A_{17}. If the channel is in write status, "end response 1" becomes active to the adapter at A_{22} a few clock pulses after the end sync trigger is turned on. If the channel is in read status, however, "end response" is delayed at A_{17} until after the last data word has transferred to the data register and been stored. At end response time, all data have been stored; therefore, the assembly ring and character ring are reset by O_{23} and O_{24}.

By interface standards, "end response" must remain up until the fall of both "command response" and "end" or "unusual end." These conditions are met at A_{25} where the inactive state of "on end" and "command response" are used as gating lines to signify that the adapter has completely ended its operation sequence

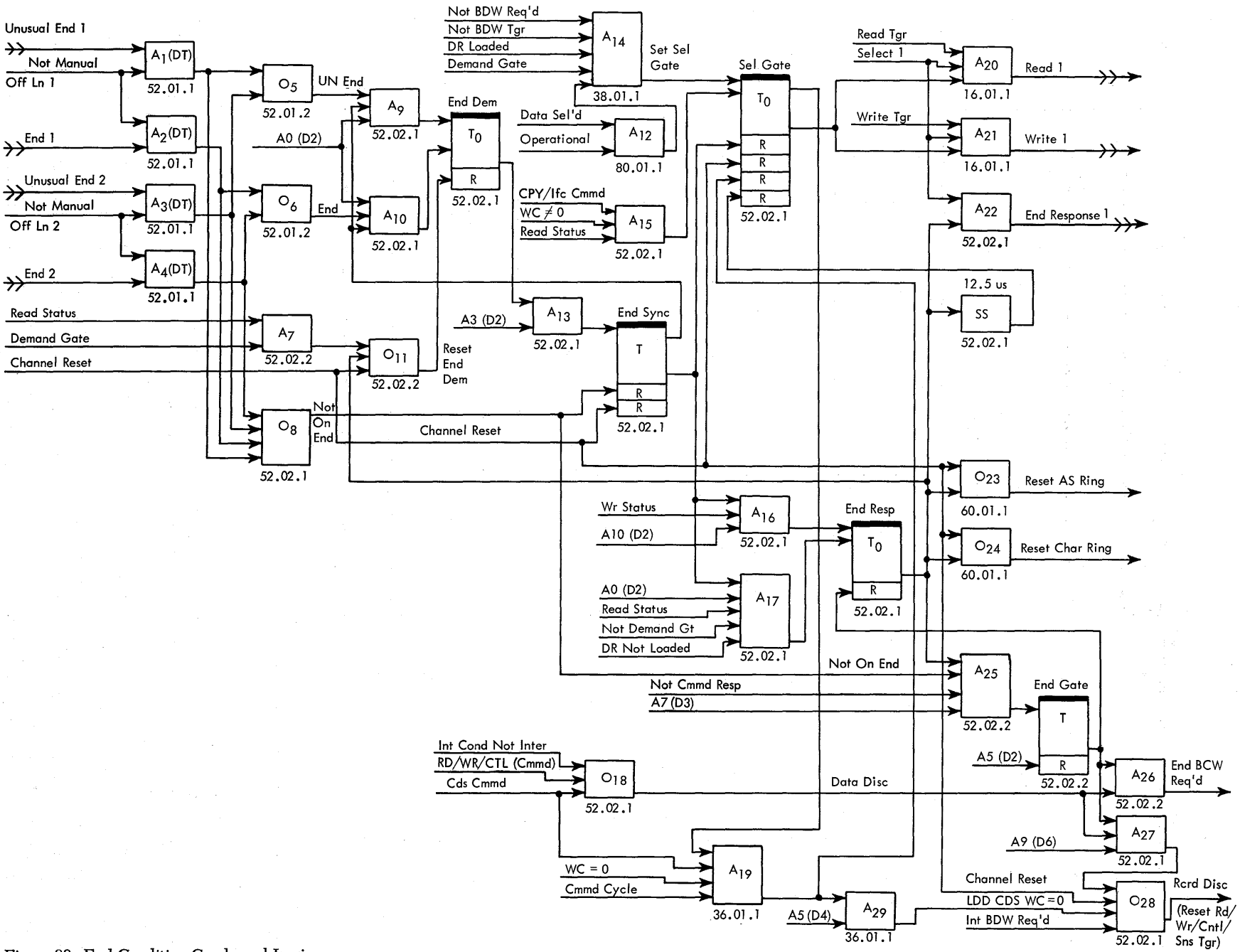


Figure 88. End Condition Condensed Logic

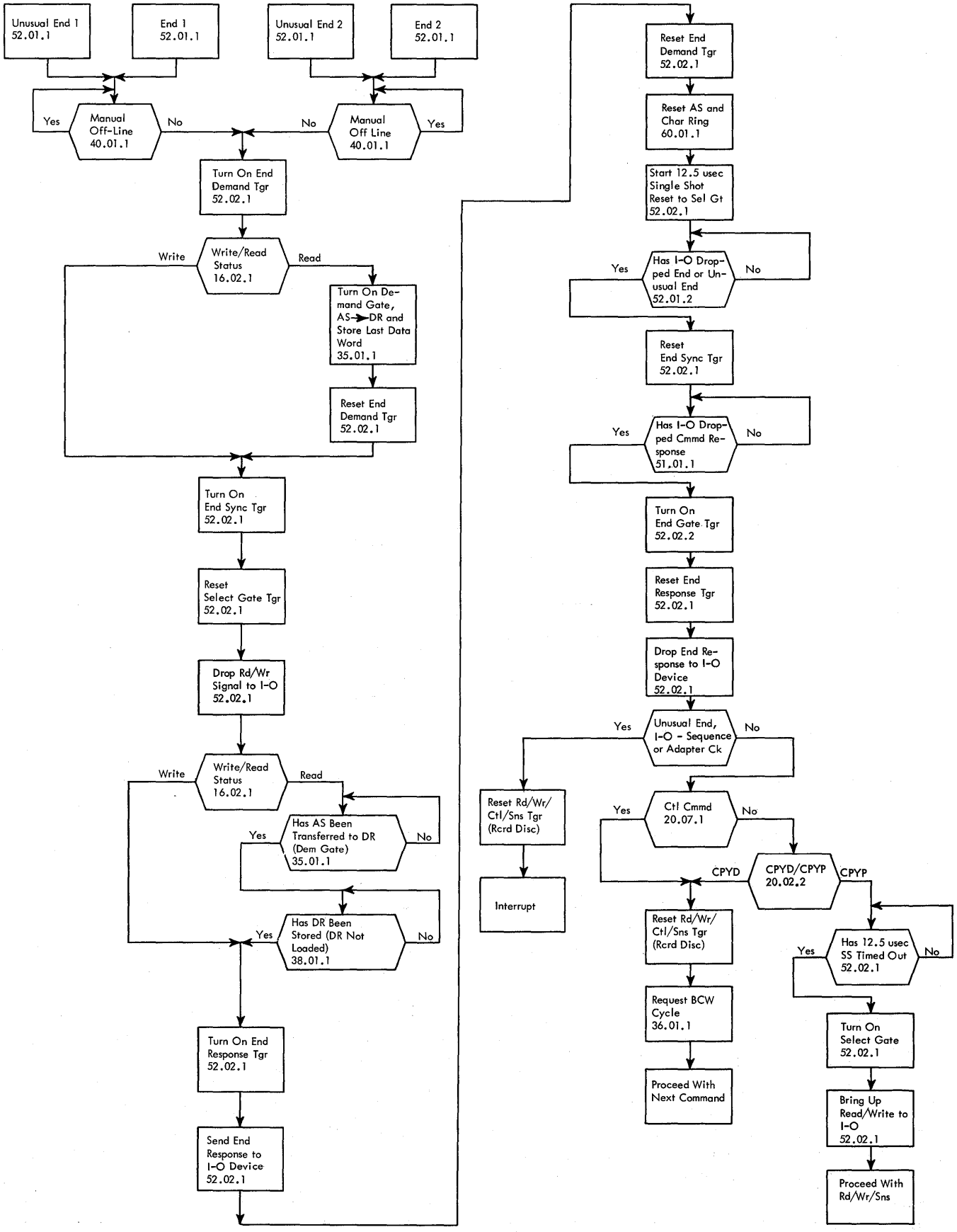


Figure 89. End Condition Flow Chart

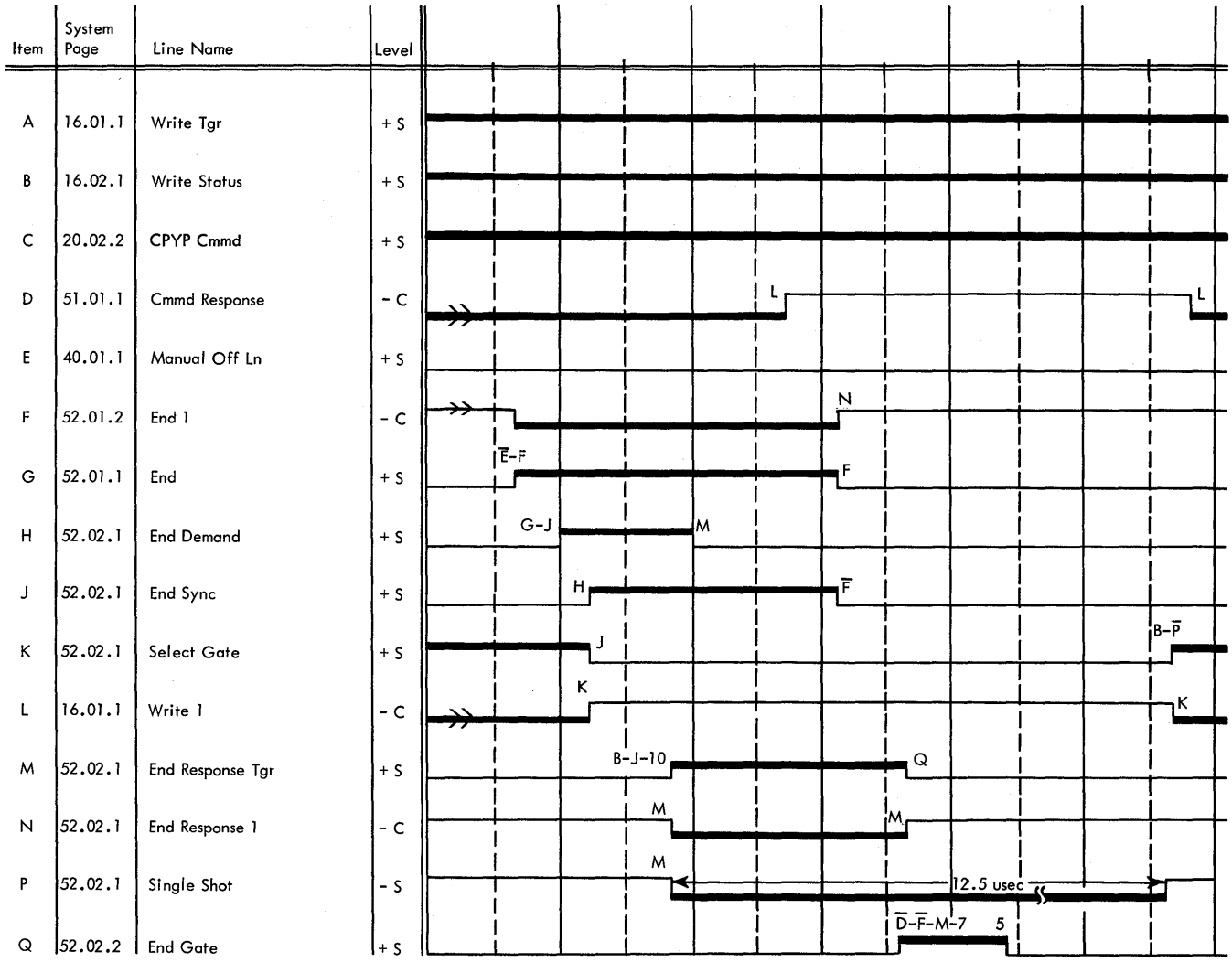


Figure 90. End Condition Sequence Chart

and disconnected from the channel. The end gate trigger, turned on by A_{25}, immediately resets the end response trigger and drops that signal to the I-O adapter.

At end gate time a decision must be made to either stop this operation (record disconnect) or continue until the word count of a CPYP command is reduced to zero. If the latter condition exists at this time, the adapter must be reselected and told to continue with the operation. When the end signal from the adapter drops, the out-of-phase output from O_8 becomes active to condition A_{25} as just discussed and, at the same time, resets the end sync trigger. This removes one reset to the select gate trigger. When the 12.5 μs single-shot (which started timing with end response) times out, the select gate trigger is turned on again by either A_{14} or A_{15}; A_{20} or A_{21} becomes active and the operation is restarted.

If a CPYD is in control of the operation at end gate time, the channel must terminate the operation and proceed to a new command. A CPYD at O_{18} gates A_{26} and initiates the request for a new BCW cycle. At the same time, it conditions A_{27} and O_{28} and causes a "record disconnect," resetting the read, write, control, or sense triggers. A 12.5 μs single-shot holds the select gate trigger reset until the channel is taken out of either read or write status by "record disconnect" and insures that the adapter will not be reselected.

The adapter is not selected if a CPYD command is initially loaded with a word count equal zero. A_{19} produces a "record disconnect" to reset the read, write, or sense triggers and also holds the select gate trigger reset. If the command is brought from core storage at some time during data transmission, however, A_{19} is blocked and "record disconnect" delayed until an end signal is received from the adapter.

If the operation is under control of a CPYP command with a word count large enough to span several records, any I-O, sequence, or interface check terminates

the operation at the next end time. This results from "interrupt condition not interrupted" at O_{18}. An unusual end also stops an operation without regard for word count by producing "interrupt BDW required" at O_{28}. In either case, an interrupt occurs immediately following the record disconnect.

Channel Trap

The 7909, as a small independent computer, can relieve the main computer program from the tedious and time-consuming process of continually monitoring and testing the various channel and I-O adapter conditions. By using the interrupt feature and the several logical commands at its disposal, the channel can decide if and when the computer should be brought into play. This is a trapping operation and is not an automatic function, but must be specifically initiated by the trap and wait (TWT) command.

Whether or not the channel is allowed to trap is dependent on the computer program. Trapping is ineffective unless the computer has previously enabled the channel. The result of a successful trap is the storing of the computer program counter plus one in the address portion of a specified core storage location and transferring to the instruction at the specified location plus one. The following chart shows the octal locations for channels A-H:

Channel	Program Counter Plus One Stored at	Next Instruction Executed at
A	00012	00013
B	00014	00015
C	00016	00017
D	00020	00021
E	00022	00023
F	00024	00025
G	00026	00027
H	00030	00031

Trap Operation

A computer enable instruction, at A_1 (Figure 91), resets the enable trigger early in the E-cycle (A_4), and if the enable control word address has a bit corresponding to this channel, the instruction turns the trigger on at E8 time via A_3. From this point, the channel remains enabled until reset by a subsequent enable instruction or channel reset.

Recognition of a TWT command in the channel at A_2 (Figure 91) turns on the trap sync trigger via A_5. The sequence of events from this point depends on other factors: Is the computer inhibiting traps at this time; if not, is a higher priority channel also requesting a trap?

After the computer has finished one trapping subroutine and is ready to handle another, the inhibiting effect is removed by means of a restore channel trap (RCT) or enable (ENB) instruction. Either instruction removes the inhibiting effect by resetting the computer's restore trigger. This restore line from the computer conditions A_8 so that the channel may now seek priority. A_8 and O_9 propagate a remote trap required line to the lower priority channels. Note that a higher priority channel can also propagate its signal through O_9 and, at the same time, block setting of the trap priority trigger at A_{10}. With no higher priority channel trapping at this time, A_{10} turns on the trap priority trigger and sends a control word trap (CWT) demand to the computer through A_{13}.

Early in the next instruction cycle, the computer recognizes the channel's signal and initiates its trapping procedures of storing the program counter and transferring. Once in E time of the trapping operation, the trap priority and trap sync triggers are reset by A_{11} and A_6, respectively.

Start channel (STC) instructions should be disregarded whenever the channel is enabled and waiting to be serviced for a trap. A_7 conditions A_{12} so that STC instructions end operation in L time instead of proceeding to E.

Channel Interrupt

The 7909 constantly monitors its circuits and functional operations and those of connected adapters; abnormal conditions are recognized and remembered in a six-position check condition register (explained in detail earlier). The channel interrupt feature makes direct use of this register and has been incorporated to eliminate constant program testing. The channel can automatically force an interrupt to a specific location where a subroutine may be employed to analyze the situation. A 7909 interrupt turns on the tape check indicator on the 7151 console.

An interrupt simulates a computer store channel (SCH) operation so that the command counter will be stored at a specified core location. The channel then immediately executes the command at the specified location +1 (normally a TCH or other unconditional transfer command) and proceeds from there.

I-O, sequence, or interface checks could occur during data transfer operations. If one of these checks is detected, a stop signal is sent to the adapter to terminate the operation; an interrupt is prevented from taking place until after the adapter has been logically disconnected. Unusual ends terminate the operation, disconnect the adapter, and initiate an immediate interrupt. Attention signals received during an interface operation are suppressed until all data have been transferred and the adapter disconnected.

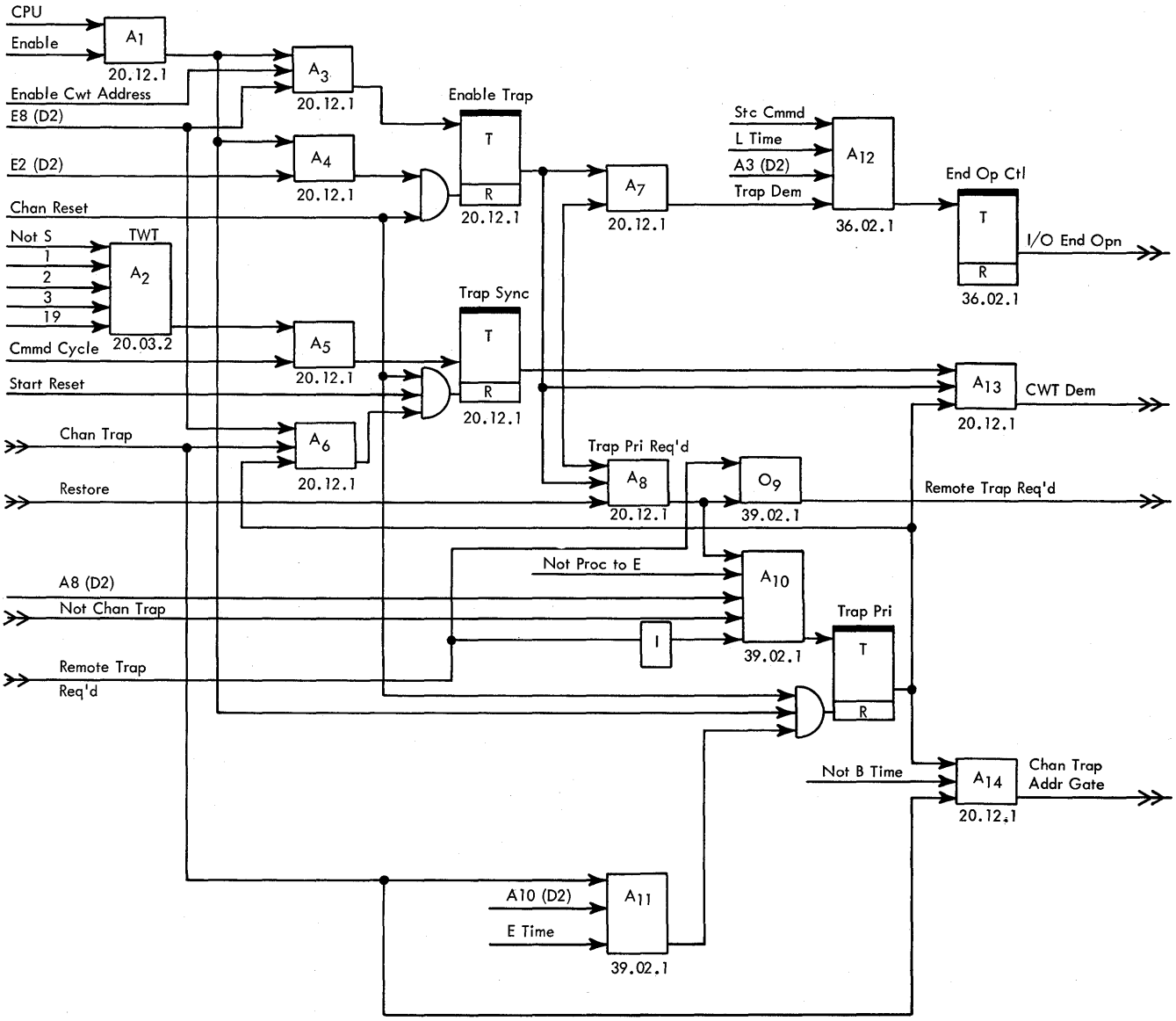


Figure 91. Channel Trap Condensed Logic

Once the interrupt is allowed to proceed, two B cycles are required: a BDW to store the command counter value, and a BCW to cause the channel transfer. Commands are executed starting at the new location, and subsequent interrupts are prevented until an LIP, LIPT, or RIC releases the inhibiting effect. Any check conditions, except attentions, are lost if they occur while the channel is in interrupt status.

Channel Assignments and Connections

Channel assignments are made by the proper cap-cut of a Y3—jumper card located at 05A4D28 (50.80.04.1 and 50.80.05.1). Instructions for making the cap-cut are shown on 50.00.32.0.

The channel assignment cable is inserted in the appropriate connector at the 7606 multiplexor as follows:

CHANNEL	INTERRUPT ADDRESS	MULTIPLEXOR CONNECTOR
A	42	03F53D
B	44	03F53E
C	46	03F53F
D	50	03F53G
E	52	03F49D
F	54	03F49E
G	56	03F49F
H	60	03F49G

Interrupt Operation

Turning on the interrupt BDW required trigger (Figure 92) is the first step in gaining interrupt control. All of the necessary circuit interlocking is located between this trigger and the condition trigger causing the interrupt.

An I-O, sequence, or interface check which occurs during an operation is recognized at O_{12} (Figure 92).

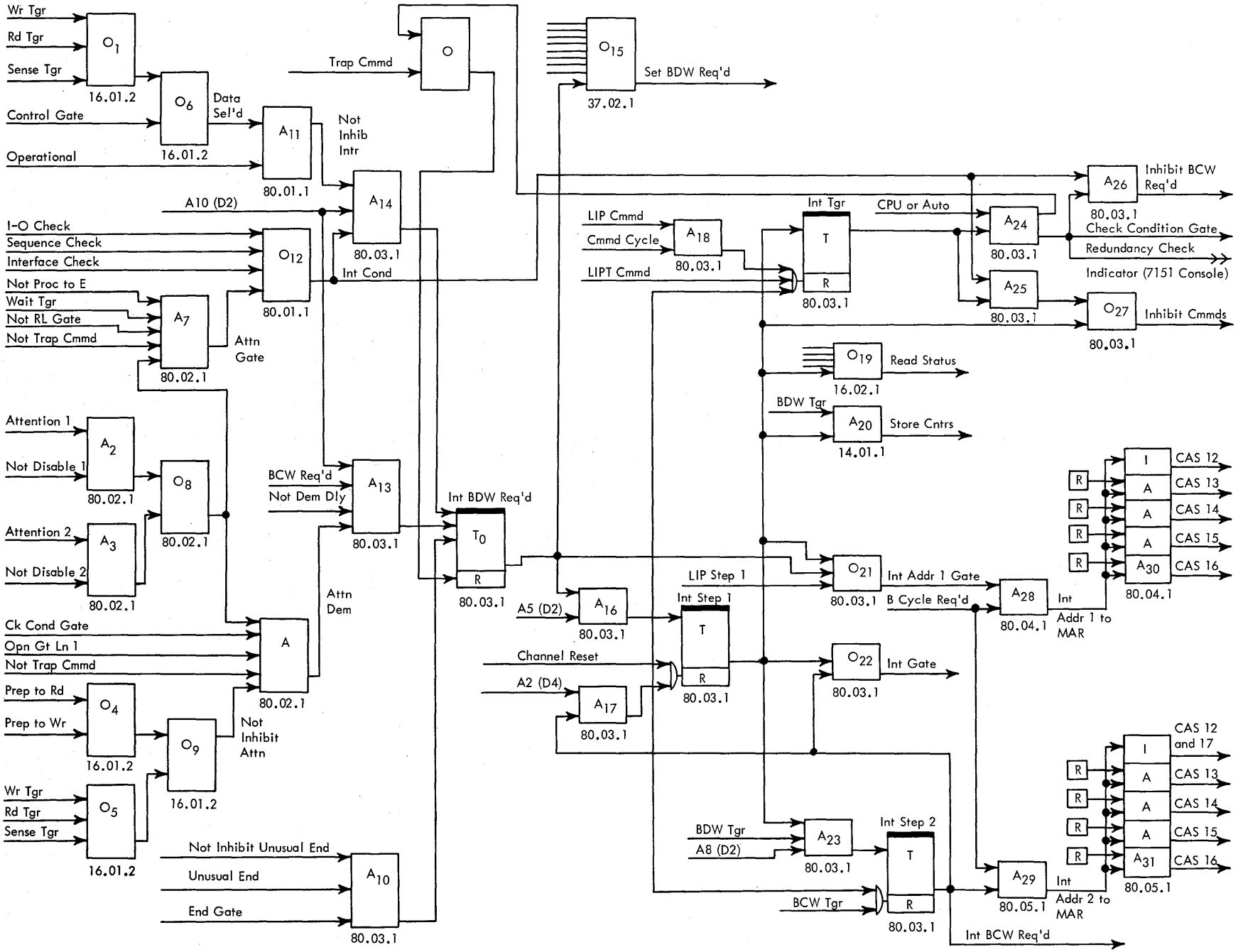


Figure 92. Channel Interrupt Condensed Logic

These checks also initiate a stop signal to the adapter causing an eventual record disconnect. Interrupts must be delayed, however, until the disconnect is completed and a new command is sought. O_1 and O_6 detect a data selected condition by testing for one of the four interface commands: CTL, CTLW, CTLR, or SNS. As soon as "data selected" falls, "not inhibit interrupt" becomes active from A_{11} and allows A_{14} to turn on the interrupt BDW required trigger.

Attention signals are the only ones which can occur asynchronously. They indicate a change in status of the I-O device and do not rely on the present command under execution. A signal could arrive while the channel is in wait status, data selected, or executing any one of the available commands.

An attention from either one of the interfaces is recognized at A_2 or A_3 and O_8 provided that neither has been disabled by a SMS command. If in wait status (WTR), the channel starts an interrupt through A_7, O_{12}, and A_{14}. If data-selected, O_4, O_5, and O_9 block an attention interrupt until disconnect time. "BCW required," at A_{13}, tells the circuits that the present command is completed and a new one is required. At this point the normal program sequence is broken and an interrupt occurs.

Unusual ends, at A_{10}, require no special synchronization for they occur at the logical end of the operation and are properly timed with "end gate."

Note that the interrupt BDW required trigger is turned on at the time a new command cycle is required. Because of this, the normal request for a BCW cycle is blocked by A_{26} to prevent conflict with the request for a BDW cycle at O_{15}. B time is received as soon as the channel obtains priority.

Now that the channel has started interrupt procedures, "interrupt step 1" is turned on at A_{16}. The interrupt trigger is also immediately turned on and is not turned off again until execution of an LIP at A_{18}, LIPT, or channel reset.

The object of "interrupt step 1" is to store the command counter value in location 42_8 (for channel A) so that the channel program knows at what point the interrupt occurred. To accomplish this, the channel is placed in read status (O_{19}) and forced into a simulated computer store channel operation through A_{20}. "Store counters" gates the command and address counters onto the storage bus where they are sampled and set into the specified location. The specified location is preset for each channel by a jumper card shown at A_{30}. O_{21} and A_{28} produce "interrupt address 1 to MAR" which gates the special preset address to channel address switches (CAS) 12-17.

During normal BDW cycles, the address counter supplies the memory address location. This circuit is now blocked by O_{22}, "interrupt gate," to eliminate any conflict of address from that generated at A_{30}.

As mentioned earlier, this interrupt is started when the channel requests a new command cycle. The BCW cycle is suppressed; however, the last command executed is left in the operation register. The decoder outputs are blocked by "inhibit commands" at O_{27}, to prevent circuit conflict between the old command and the store channel operation. Remember, that once the interrupt begins, all subsequent check conditions are blocked at A_{24} by dropping "check cond gate." A_{24} becoming inactive turns off the interrupt BDW required trigger.

To summarize the functions of "interrupt step 1":

1. A read BDW cycle is requested and obtained through normal channel priority circuits.
2. The operation decoders are blocked and a store channel operation is forced to store the command and address counters.
3. Normal gating of AC to MAR is blocked and a specified preset location is forced to the CAS.
4. Further interrupts from check conditions are blocked until such time that the interrupt program is properly terminated.
5. The interrupt BDW required trigger is reset.

Once the store operation has been completed, "interrupt step 2" requests a BCW cycle and transfers to location 43_8 (channel A) where a new command is read out and executed in the normal manner.

At A8 time of the interrupt step 1 BDW cycle, A_{23} turns on the interrupt step 2 trigger and immediately requests a BCW cycle. This request comes too late to retain priority and the BDW and BCW cycles are not successive machine cycles.

When the BCW cycle is obtained at A_{29}, "interrupt address 2 to MAR" gates a second set of preconditioned circuits. These lines from A_{31} control the channel address switches and determine which core memory location is affected. Note that "interrupt gate" at O_{22} blocks the normal gating of CC to MAR so that there is no conflict with the generated address at A_{31}. At the beginning of the BCW cycle, "interrupt step 2" has fulfilled its function. From A0 time of the BCW cycle then, the channel operates as it would during any other normal control word cycle.

To summarize the functions of "interrupt step 2":

1. A BCW cycle is requested and obtained through normal channel priority circuits.
2. Normal gating of CC to MAR is blocked and a specified preset location is forced to the CAS.
3. The interrupt step 1 trigger is reset.

A special case is that of a trap and wait (TWT) command. Any interrupts occurring while the channel is in wait status resulting from a TWT command are delayed

until the channel is started again from the computer program. "Trap command" applied to the interrupt BDW required trigger holds it reset until such time that a new command is brought in by an RSC instruction.

Figures 94 and 95 show the logic flow and time sequence of a channel interrupt operation.

Non-Concurrence Interrupt

If information written is of a known format, the 7909 Data Channel can check for exact record or word length when reading, by use of non-concurrence interrupt (Figure 93). This feature, if enabled, checks for records longer or shorter than the word count and also for partial or incomplete words.

The enable non-concurrence interrupt (NCI) trigger is turned on (Figure 93) by a bit in position 29 (address counter position 11) of an SMS command at A_6. The NCI trigger remains on until another SMS command or the channel is reset.

The word count going to zero while a copy disconnect command is in operation and AS ring is not at 6 indicate that the record is too long (A_{13} and A_{15}).

End gate and word count not zero at A_{16} indicate that the record is shorter than expected.

End demand coming on at any time other than assembly ring 6 of a copy disconnect command at A_{17} indicates that the word is incomplete.

Any of these conditions turns on the unusual end trigger. By use of a sense command, the I-O control unit indicates if an unusual end did occur. No indication from the control unit means that the interrupt was from an NCI and the I-O checking routine proceeds from there.

NOTE: The OR circuits of the unusual end trigger are on Systems 50.80.01.1 and 50.80.01.2.

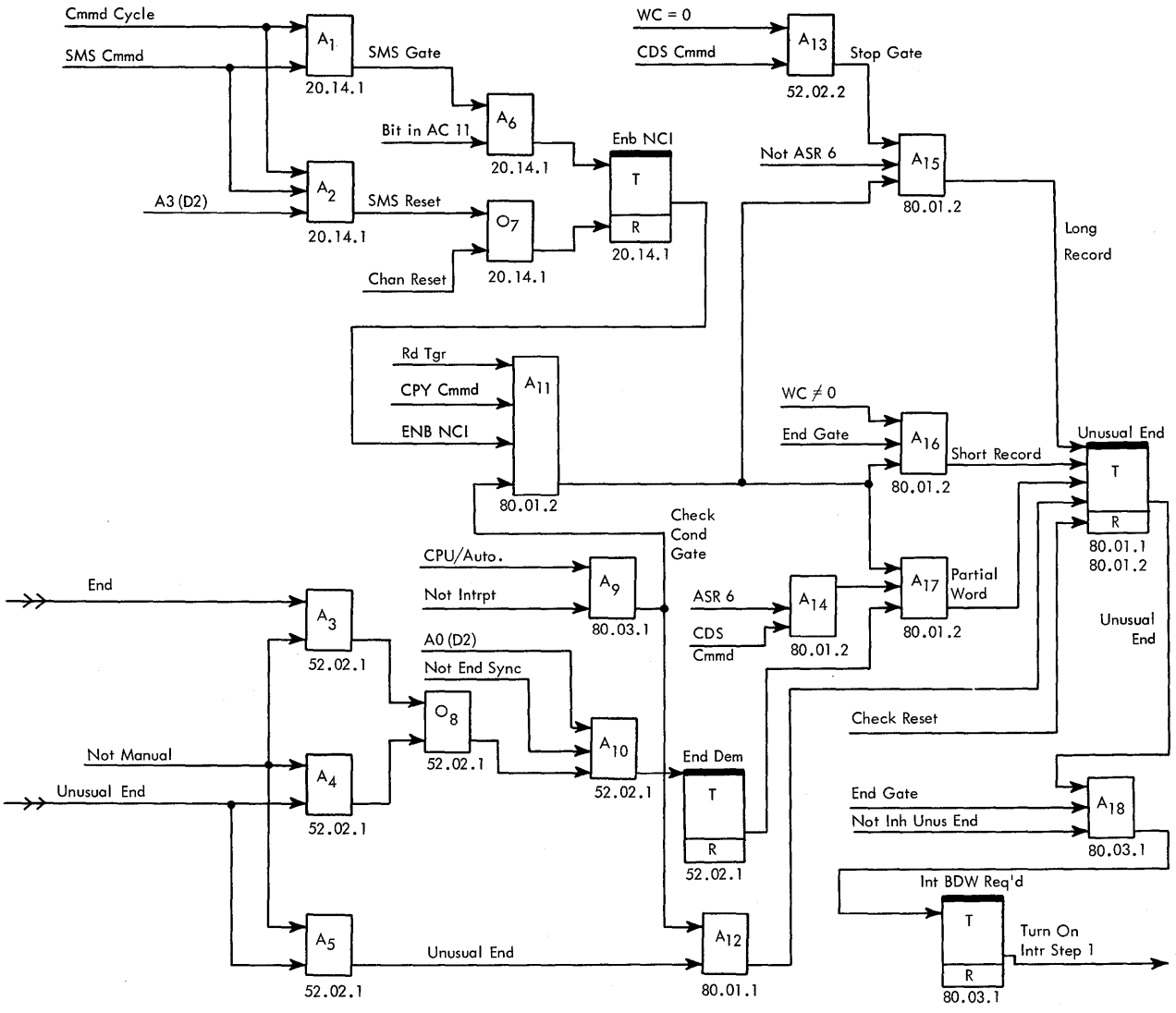


Figure 93. Non-Concurrence Interrupt Condensed Logic

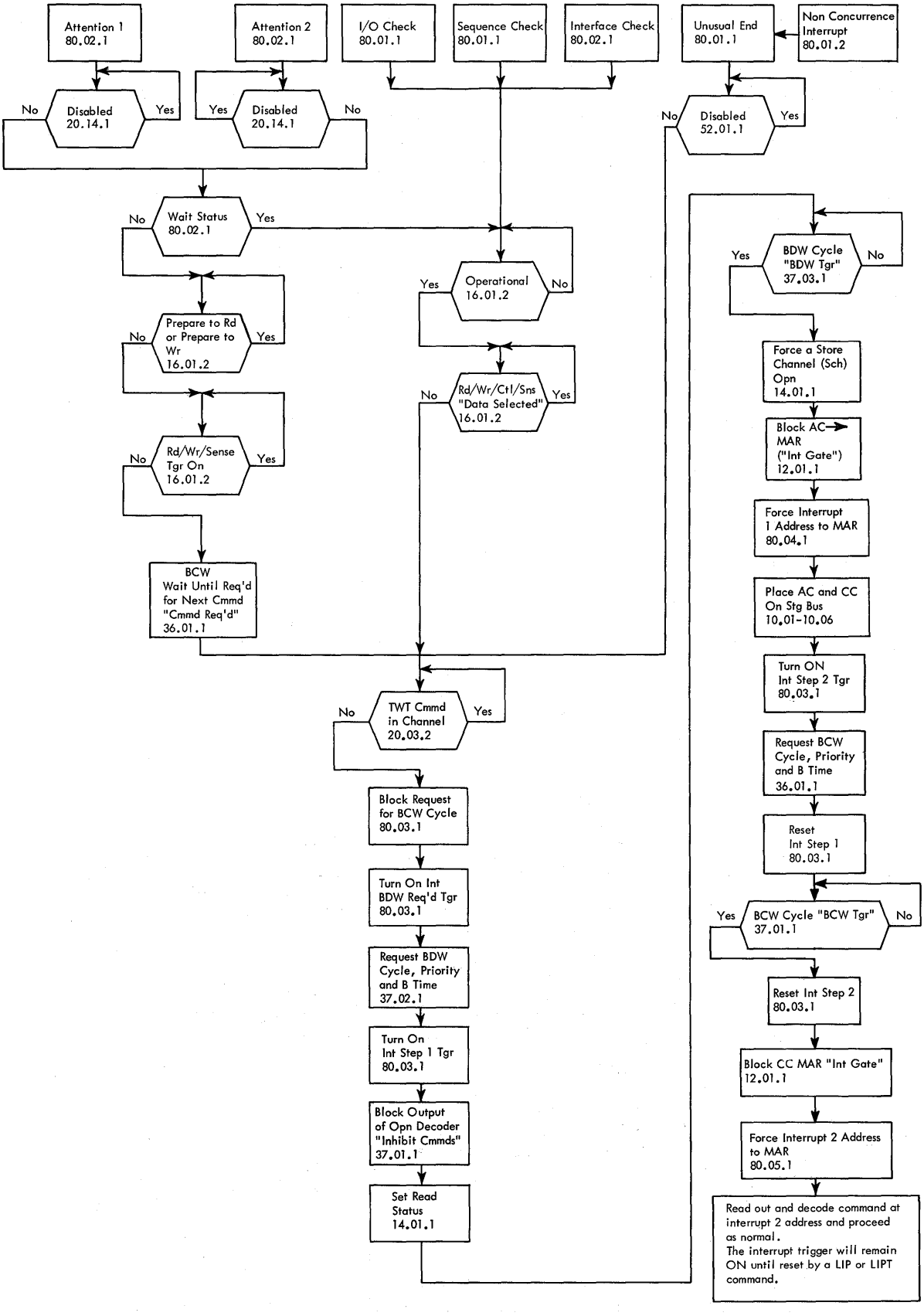


Figure 94. Channel Interrupt Logic Flow

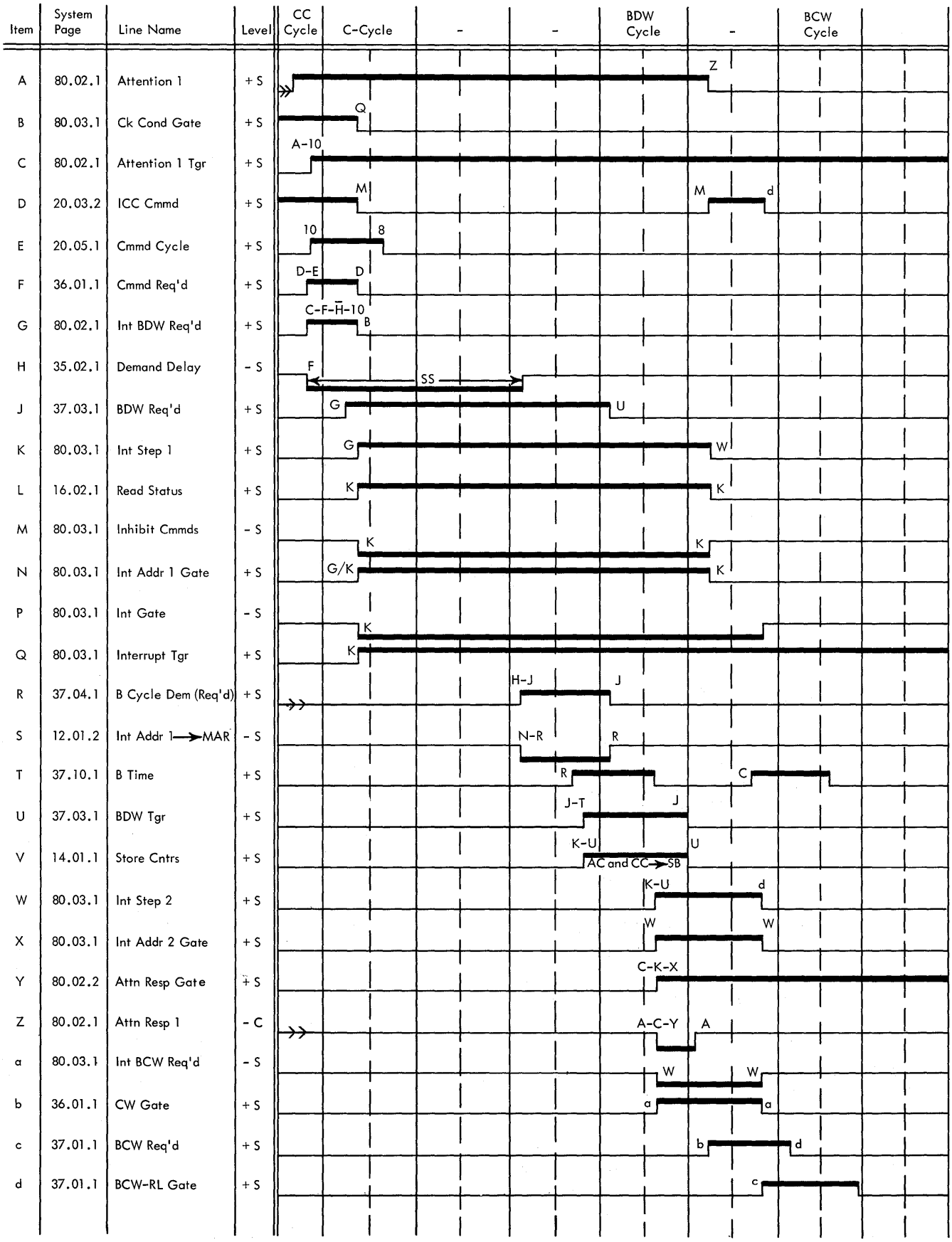


Figure 95. Channel Interrupt Sequence Chart

Unusual End

Unusual ends (Figure 96) may result from I-O operations on either of the channel interfaces. A signal is received at A_1 or A_2 depending on which interface is selected. Unusual ends are concerned with control or data transmission operations, and because of interlocking, it is not possible to receive simultaneous signals from both interfaces. A_3 blocks recognition of unusual ends if they should occur during an interrupt program. Unless disabled by an SMS command, they will cause channel interrupts in the normal manner.

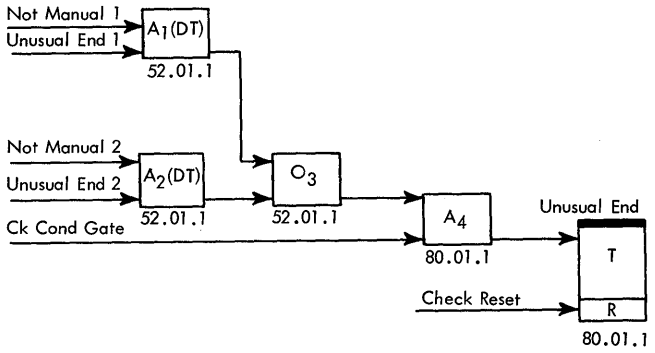


Figure 96. Unusual End Condensed Logic

Leave Interrupt Program—LIP

Cyclic Makeup: BCW - CCC - CMMD - BCW - CCC - CMMD

When a channel interrupt occurs, further interrupts are blocked, the command counter is stored in the address portion of a specified core location (location 42_8 for channel A), and a transfer should be programmed to a special subroutine. After executing the subroutine, it may be desirable to return to the main channel program at the point where the interrupt occurred. The LIP command (Figures 97 and 98) performs this by going to the specified location (42_8 for channel A), obtaining the data word, and transferring to the location specified by address positions 21-35 in two steps: LIP step 1 and LIP step 2.

The initial BCW cycle loads the LIP command into the operation register, word counter, and address counter at 7 time. The two counters are not used at this point but will be loaded. A CC cycle is requested during this BCW cycle and the LIP CMMD decoder output becomes active at the next 0 time.

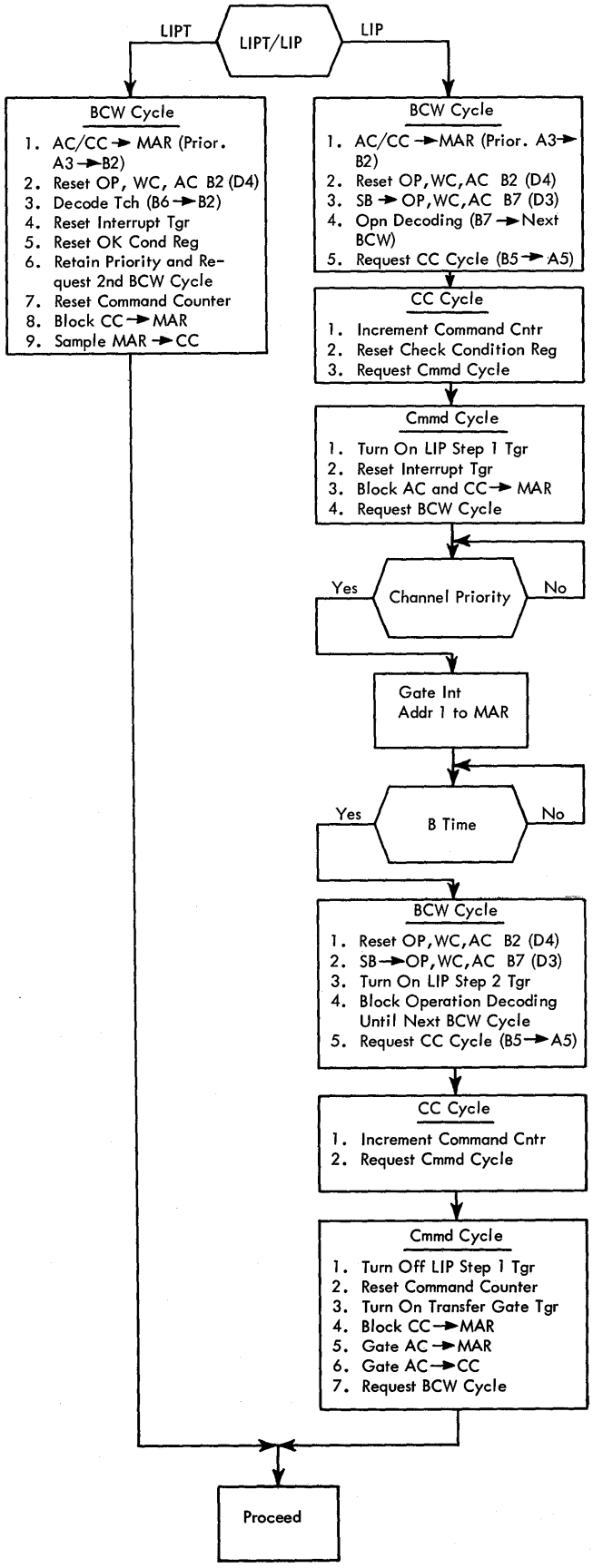


Figure 97. LIP/LIPT Flow Chart

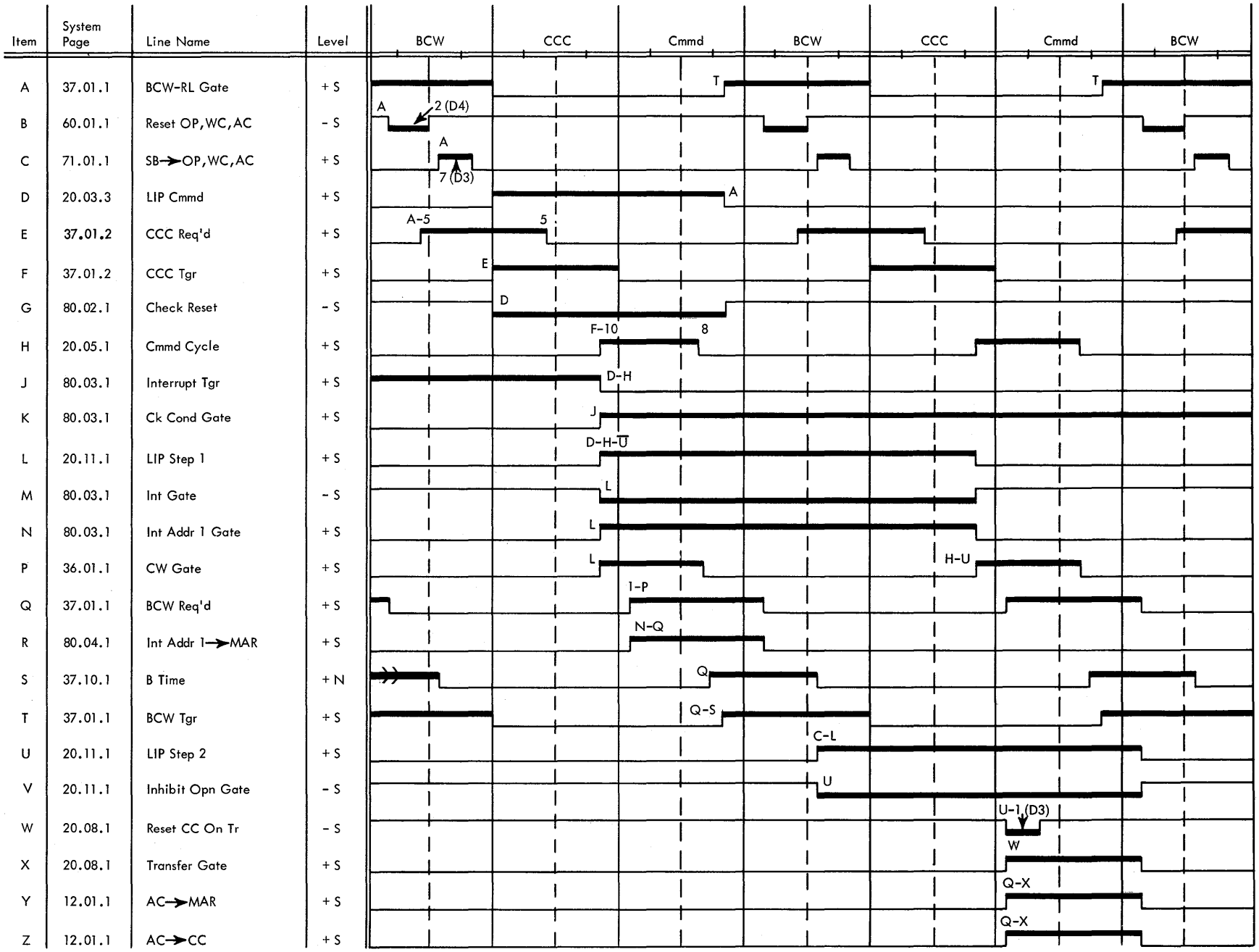


Figure 98. LIP Sequence Chart

Check conditions (except attentions) are lost when the command counter cycle (CCC) which follows, resets the check condition triggers. The command counter is incremented but performs no logic, for the counter will be reset. Instead, this cycle acts as a normal means of obtaining a CMMD cycle.

The CMMD cycle resets the interrupt trigger to prevent further blocking of subsequent interrupt conditions. A request is also made for a BCW cycle, and the LIP step 1 trigger is turned on with the following effects:

1. All gating from the command counter or address counter to MAR is blocked by "interrupt gate."
2. "Interrupt address 1 gate" gates the preset channel address to MAR (50.80.04.1).

The next BCW cycle is delayed an amount dependent on other channel priorities and system configuration. When obtained from the computer, the BCW cycle functions as any other BCW cycle; the operation register, word counter, and address counter are reset early in the cycle and set again to the data coming from the predetermined core storage location. At the same time, 7 time, LIP step 2 trigger is turned on.

The only useful data obtained during this BCW cycle is the transfer address now located in the channel's address counter. Any data set into the word counter at this time is ignored; however, any bits set into the operation register could cause trouble. Because of this, the LIP step 2 trigger produces "inhibit operation gate" which blocks operation decoding for the remainder of the operation; LIP step 2 may be thought of as the command in control of the channel at this time.

A second command counter cycle occurs but performs no logic other than requesting a CMMD cycle needed to complete the operation.

The second command cycle:

1. Resets the LIP step 1 trigger.
2. Causes a channel transfer.
3. Requests a BCW cycle.
4. Resets the command counter A1(D3).
5. Blocks command counter to MAR circuitry (transfer gate).
6. Gates address counter to MAR.
7. Gates address counter to command counter so that the channel can proceed in sequence at the new location.

It is possible that an attention interrupt is waiting to be processed at the end of the LIP operation. Circuitry on 50.80.02.1, however, prevents a second interrupt from occurring until after the channel has executed one command following the LIP.

Leave Interrupt Program and Transfer—LIPT

Cyclic Makeup: BCW

When leaving an interrupt program it may not always be desirable to return to the main channel program and continue from where the interrupt occurred. The LIPT command (Figures 97 and 99) resets the interrupt trigger and check condition triggers (as is done in the LIP command), cancels the inhibiting effect of a previous interrupt, and transfers to a location specified in the address portion of the LIPT command.

With exception of the interrupt and check condition resets, the LIPT functions exactly as a TCH command.

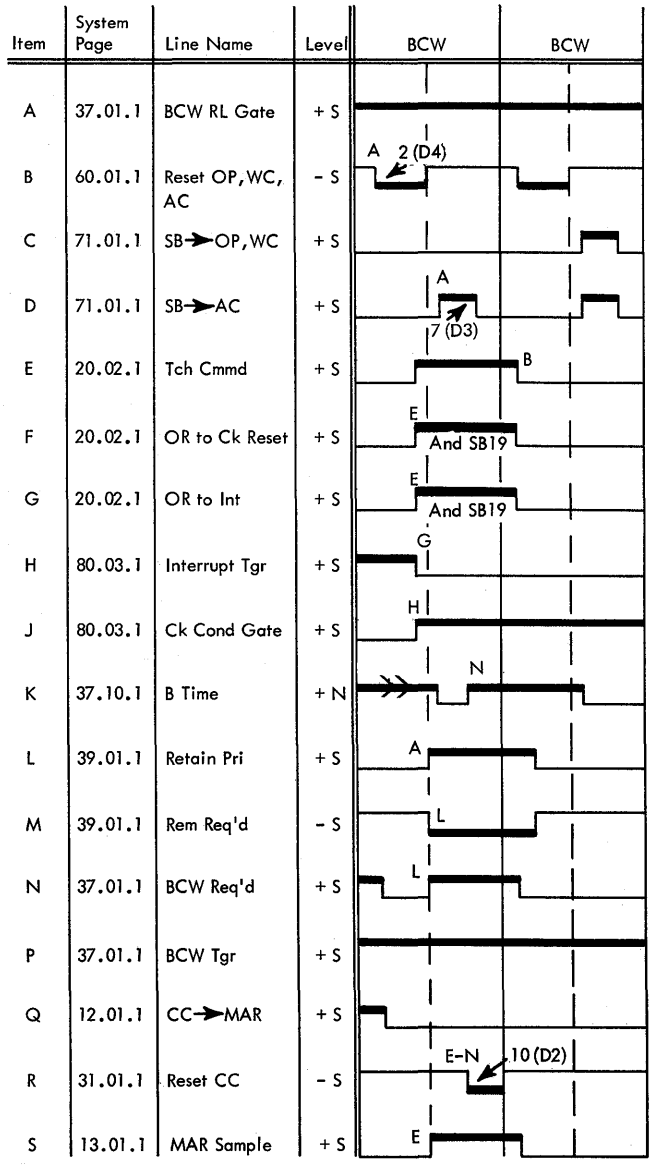


Figure 99. LIPT Sequence Chart

Look-ahead circuitry in the multiplexor causes the transfer when decoding S, 1, 2 (position 19 is not active in the multiplexor decoding). Address positions 21-35 from storage are routed back to MAR as the new reference address during the next cycle. "Retain priority" sent to the channel causes an immediate request for a second BCW cycle. This second cycle is a normal BCW cycle and accepts the new channel command at the transfer address.

During the LIPT BCW cycle, the TCH trigger is turned on in the channel to perform the following:

1. Block the normal request for a CC cycle following the first BCW cycle.
2. Block setting the operation register and word counter. The address counter is set but performs no logic.
3. Reset the command counter at B10(D2) of first BCW cycle, in preparation for receiving the transfer address from MAR.
4. Sample the MAR bus from the multiplexor into the command counter.

"Retain priority" received from the multiplexor also serves to block the normal command counter to MAR circuitry on 50.12.01.1.

It is possible that an attention interrupt is waiting to be processed at the end of the LIPT BCW cycle. Circuitry on 50.80.02.1, however, prevents a second interrupt from occurring until after the channel has executed one command following the LIPT.

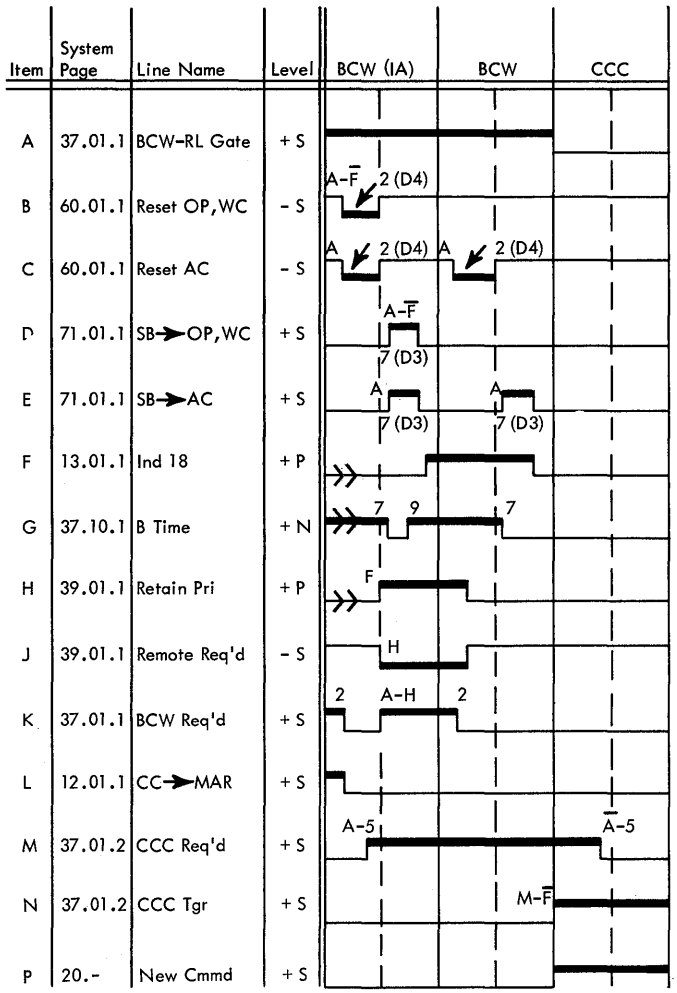


Figure 100. Indirect Addressing Sequence Chart

Indirect Addressing

Indirect addressing (Figure 100) is recognized during the initial BCW cycle of a command by a bit in position 18 of the command word as it arrives in the multiplexor from core storage. Indicator 18 decoding in the multiplexor look-ahead circuitry produces a retain priority line which is sent to all channels, causing this channel to retain priority and immediately request a second BCW cycle. The object of this second cycle is to make reference to a core location specified by positions 21-35 of the channel command.

During this second BCW cycle, only the address counter is reset and modified from the storage bus. "Indicator 18" blocks the resetting of the operation register and word counter so that they retain the information initially read in. "Remote required" blocks CC to MAR during the second BCW cycle because the new address is routed automatically back to core storage by the multiplexor circuitry.

A command counter cycle (CCC) is requested during the first BCW cycle, but the CCC trigger is blocked from turning on until after the second BCW cycle. At the end of this second BCW cycle, the outputs from the operation decoders become active, a command counter cycle begins, and the channel command proceeds into execution.

Check Conditions

The channel is continuously monitoring and checking various items such as: loss of data, channel commands out of sequence, unusual end conditions, attentions from the adapter, and so on. The normal sequence, when one of these conditions is recognized, is to interrupt to a testing subroutine. In this subroutine the condition triggers may either be tested immediately by means of the TCM command or stored into a memory location for future reference. For a more complete explanation of interrupt and its relation to check conditions, see the section on "Channel Interrupt."

To store the information, two commands are required: an insert control counter (ICC) with a count

of zero to set the contents of the SMS register into positions 29-35 of the assembly register, and a store assembly register (SAR) command to transfer them into the specified location.

With the item pinpointed, the channel program may now take corrective action by itself or call upon the computer for assistance by use of the TWT command.

I-O Check

An I-O check as applied to the 7909, signifies a loss of data between the channel and core storage during either a read or write operation. This failure usually means that the channel was unable to have its B time requirements fulfilled in time to meet the demands of the attached I-O device.

I-O checking a write operation indicates that new data were not obtained from core storage in time to be fed across the interface; during read, it indicates that data were not stored prior to the assembly of a complete new word from the I-O device.

Data Flow and I-O Checking

During the write operation, data flow (Figure 101) is from core storage to the data register as an intermediate buffer and from there to the assembly register where it is passed across the interface one character at a time. The data register loaded trigger is turned on during the BDW cycle to indicate that data are available. At the same time that the assembly register is reset by A_2 in preparation to receive a new data word, the status of the data register loaded trigger is tested at A_5. If the trigger is off, meaning that a BDW cycle was not obtained, data have been lost.

During a read operation, information is assembled in the assembly register until full, then transferred in parallel to the data register under control of "demand gate." During the latter portion of this demand gate pulse, the data register is loaded with the new information and the data register loaded trigger is turned on, initiating a BDW cycle. During this cycle, data are transferred to core storage via the storage bus and the data register loaded trigger is turned off, indicating that the data have been properly stored. Each time that "demand gate" rises at A_1, it causes a reset to the DR at O_3 and at the same time samples A_4. If the data register loaded trigger is still on at this time, data have been lost, and the I-O check trigger is turned on.

A_7 provides compatability with other channels for sending a signal to the computer to turn on the one common indicator located at the console.

When an I-O check occurs in the channel, it causes an interrupt in the normal manner. Check conditions are prevented from being set, however, if the channel is already in an interrupt program. This is accomplished by "check condition gate" which feeds A_4 and A_5.

Sequence Check

Passing data through the channel and across the interface requires specific sequences of commands. There are only four interface commands for transmitting data: control (CTL), control and write (CTLW), control and read (CTLR), and sense (SNS). The last three of these use copy commands; the first does not. CTL commands may be given at any time and any number of times without conflict. CTLW and CTLR must be followed by a CPYP or CPYD command if data transmission is expected. If the CTLW or CTLR command is to be used for control purposes only, no copy commands are necessary. An SNS command always requires the use

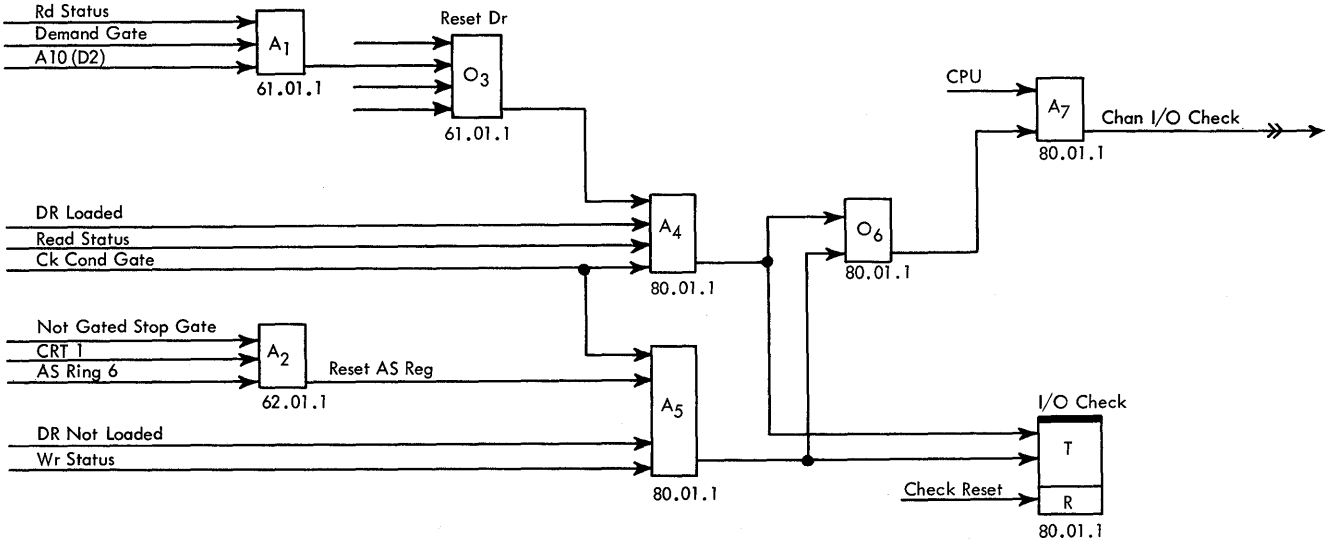


Figure 101. I-O Check Condensed Logic

of copy commands. When copy commands are used, the operation must be terminated by a copy and disconnect (CPYD).

Transfer in channel (TCH) and transfer and decrement counter (TDC) commands provide a programming method of transferring between successive CPYP commands and do not cause sequence checks. Various combinations of valid and invalid sequences are shown below; the invalid ones cause sequence checks. A sequence check causes a channel interrupt in the normal manner and blocks any subsequent checks until after a return from the interrupt program.

Channel Valid Sequences	Channel Invalid Sequences
1. CTL CTL CTL	1. CTL CPYD
	2. CTLW CTL
2. CTL CTLW CPYD	
	3. CTLW CPYP CTL
3. CTLW CPYP CPYD	
	4. SNS CTL
4. CTLW CPYP TCH CPYD	
	5. CTLW CPYP TCM
5. CTLW CPYP TDC CPYD	
	6. CTLW WTR
6. CTLW TCM	
	7. CTLW CPYP WTR
7. CTLW TCH CPYP	
	8. CTLW TCM/TDC CPYD

CTLR may be substituted in any of the above sequences for CTLW.

SEQUENCE CHECK OPERATION

A CTLW or CTLR command passes control information to the I-O device and prepares the channel for data transfer at O_1 (Figure 102). A subsequent copy command, then, resets the prepare to write or read conditions, turns on the channel write or read trigger, and sends a corresponding signal across the interface. These last two trigger conditions and sense commands are recognized at O_2.

A copy command that has not been properly preceded by a CTLW, CTLR, or SNS is an error, recognized at A_5. This corresponds to invalid sequence 1 as shown in the previous section.

The only interface command which can be followed by another interface command is a CTL. Others, such as invalid sequences 2, 3, and 4, produce sequence checks at A_7. A_3 recognizes any one of the four interface commands by decoding only the S, 1, and 2 operation register outputs.

A_8 detects sequences where copy or sense commands are not properly followed by a TCH, TDC, or CPYP. Any command which forces a command counter cycle (CCC) and is not a TCH, TDC, or COPY sets the sequence check trigger. This could result from invalid sequence 5. A first look at the A_8 input conditions shows no specific TCH gating, but a deeper look into the 7909 circuits shows that a TCH blocks setting the CCC trigger.

A_{10}, conditioned with "check condition gate," allows sequence check recognition only when the channel is not already in an interrupt program.

Interface (Adapter) Check

An interface check in 7909 system corresponds to an adapter check in sales and customer publications; both names are used in this manual but refer to the same thing.

Loss of data within the channel and improper command sequences were recognized by I-O and sequence checks; the interface check extends this checking to some of the 7909 hardware (character ring failure) and abnormal conditions of the adapter.

Adapter conditions that are recognized include character rates which are too fast for the channel to handle and non-operational conditions such as adapter power off, manual status, or not available because of use by a sharing system.

INTERFACE CHECK OPERATION

Timings to send and receive bytes across the interface are under control of the four-position character ring which steps at a predetermined rate. If requests arrive from the adapter at a rate faster than can be handled by the character ring, an interface check results at A_1 (Figure 103). In this particular case, the adapter may also recognize an over-run condition and respond with an unusual end. Both the interface check and unusual end indicators may be on, but only one interrupt occurs. A sense command to the adapter may be used to pinpoint the error.

A malfunction in the character ring could also produce a "request failure" and interface check at A_1. For a better understanding of timings involved, see the sections on "Service Request" and "Character Ring Operation."

If neither one of the selected adapters is operational (busy, power off, etc.), A_2 and A_3 remain active. An interface command (CTL, CTLW, CTLR, or SNS) finding "not operational" conditions at A_5, causes an interface

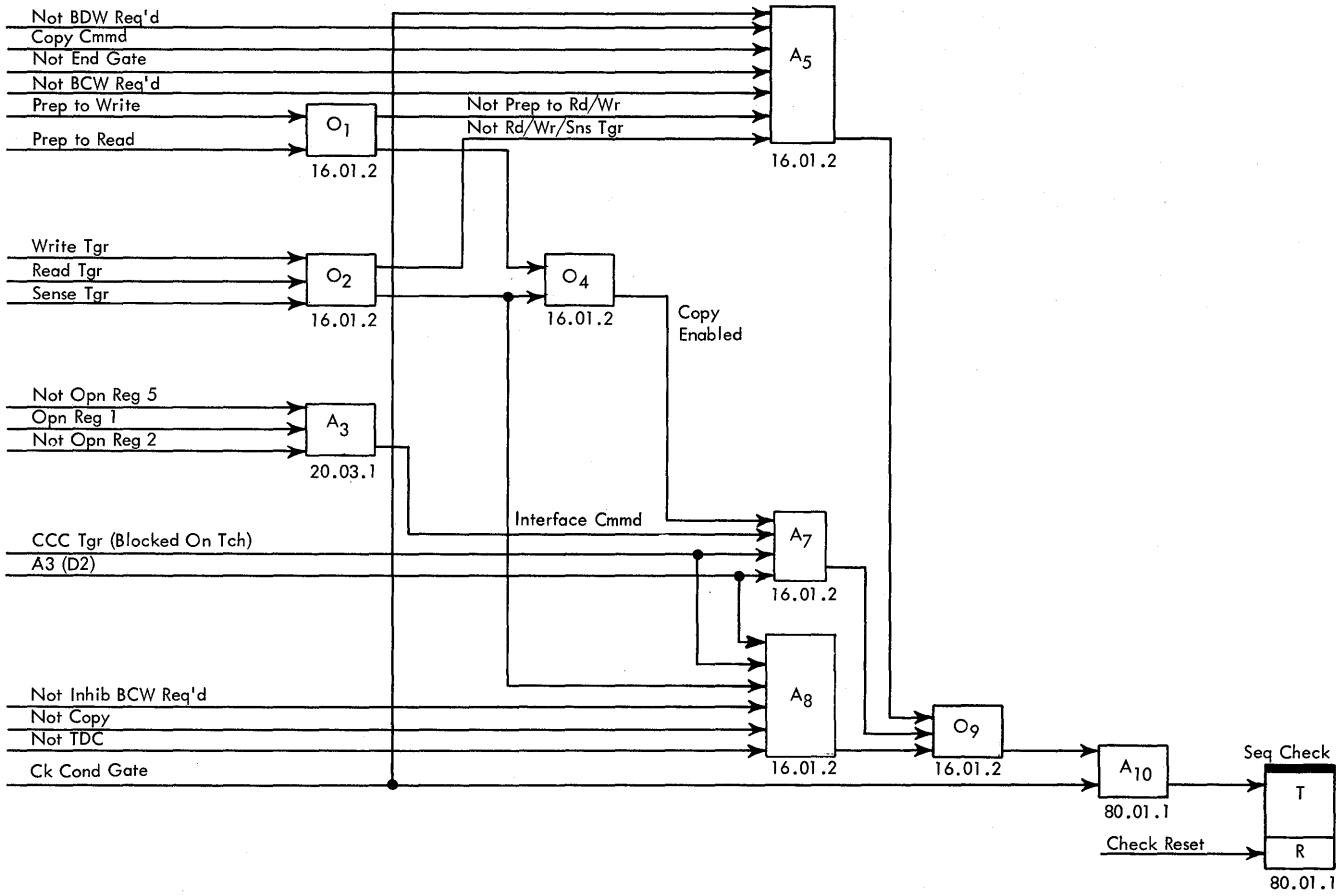


Figure 102. Sequence Check Condensed Logic

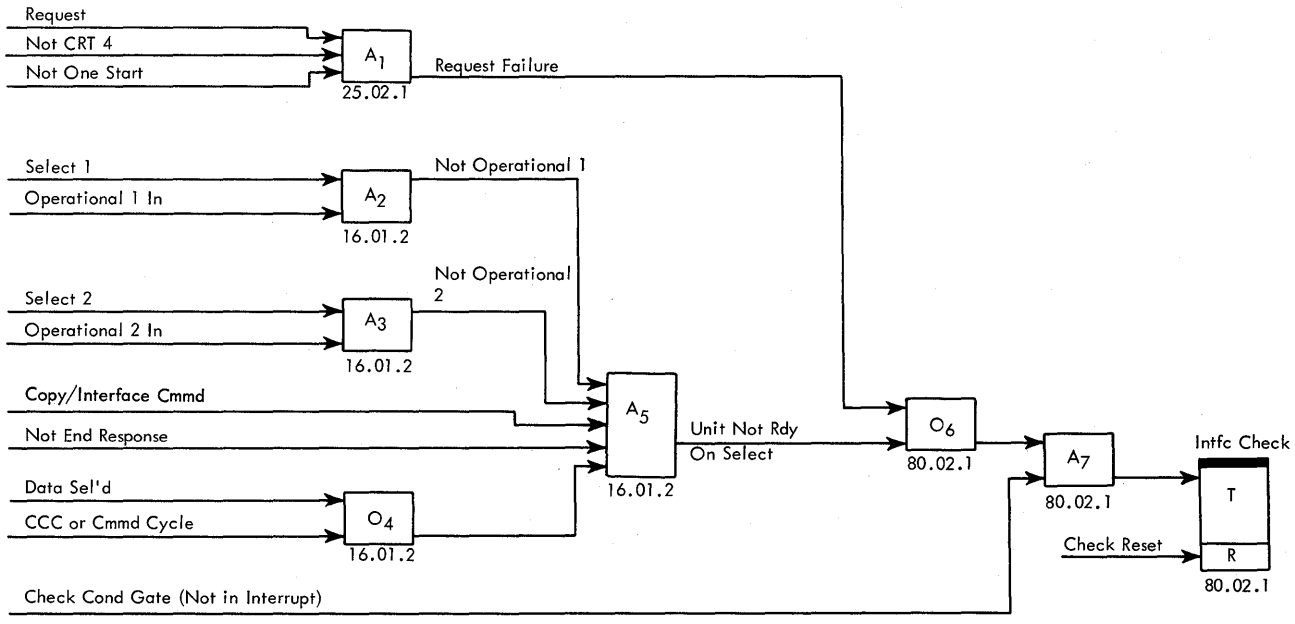


Figure 103. Interface Check Condensed Logic

check. This feature avoids hang-ups in the channel programs due to the adapter and, therefore, can allow other programming functions to continue.

Normal interrupts occur as a result of the interface checks; once in an interrupt program, subsequent checks will be ignored.

Check Reset

Once an interrupt occurs because of a check condition, the normal procedure is either to store or test these conditions and then take appropriate action. Therefore, when leaving the interrupt program, the indications have no further use and should be reset (Figure 104). This is accomplished by the LIP or LIPT commands at O_1 or O_2.

Two other conditions also reset the check triggers at O_1: a reset and start channel (RSC) instruction and a channel reset. The latter may occur with the usual power-on resets or by a computer reset channel (RIC) instruction which completely resets the channel circuitry.

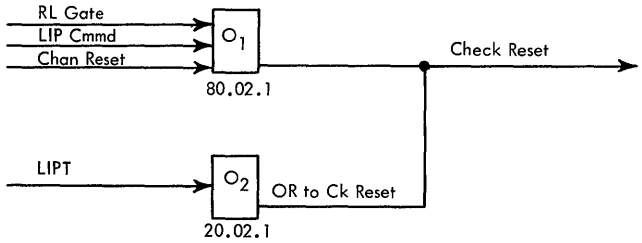


Figure 104. Check Reset Condensed Logic

CE Test Panel

The 7909 Data Channel test panel is a combination operator's panel and CE panel provided mainly as a service aid to the customer engineer (Figure 105).

Seven rows of lights indicate: assembly register, command counter, address counter, word counter, control counter, assembly ring, character ring, operation register, check condition register, and other status conditions.

Two rows of toggle switches provide 36-bit positions of entry into the channel circuits. Located below these entry keys are four toggle switches which set up various channel test conditions, and four spring-returned pushbuttons which either reset the channel or initiate test operations.

In addition to the above CE lights and switches, there are two power lights and a power ON/OFF switch available to the customer.

Panel Lights

The meanings of the various indications are self-explanatory from the labeling associated with each individual or group of lights.

In troubleshooting remember that only three lights should be on when the channel is reset: wait, assembly ring 6, and character ring 4.

Each of the indicator filaments has a small amount of current passing through it when in the OFF state. This pre-energization causes a faint glow and provides a quick positive check for a possibly burned out light.

There are no lights to show the status of the data register; its use is mainly that of a buffer between core storage and the assembly register. If information from core storage arrived correctly at the assembly register (as shown by its indicator lights) it can be assumed that the data register is functioning properly.

Panel Switches

CPU/Test Switch

When this switch is in the CPU position, the 7909 is under control of the computer and all other switches have no effect. When this switch is in the TEST position, 7909 operations are under control of the remaining test panel switches.

When the CPU/test switch on the 7909 CE panel is placed in the TEST position, computer operations shall be the same as if that channel were not connected to the system.

The following instructions are affected as follows:

INSTRUCTION	EFFECT
Reset and Start Channel	Computer hangs up
Start Channel	Computer hangs up
Reset Channel	No effect on channel
Transfer on Channel in Operation	Will not transfer
Transfer on Channel Not in Operation	Will transfer
Store Channel	Will store zeros
Store Channel Diagnostic	Will store zeros

The channel select light located at the computer console shall be on only when the 7909 is in CPU mode and not in wait status.

Ring On/Ring Off Switch

This switch, when in the ON position, simulates an I-O write operation and is a quick efficient method of checking a major portion of channel circuitry without danger of destroying information in the computer core storage.

The ring on circuitry places the channel in write status and simulates incoming I-O adapter service request pulses with a 240 KC oscillator. The character ring operates on each simulated "service request," stepping the assembly ring and routing data through the assembly register and onto the interface write bus. For each six characters sent from the assembly register, a BDW cycle is requested through normal priority circuits and a new data word is obtained from sequential locations in core storage. Each reference cycle decrements the word counter and increments the address counter.

This operation continues until the switch is returned to the OFF position. When the switch is at RING ON, the auto/manual switch should be in the MANUAL position to inhibit possible interrupts from I-O checks, interface checks, or attentions. (An I-O check always occurs initially because the data register is not loaded when the first service request is initiated.)

This switch must be in the RING OFF position in order to operate the remaining three switches.

Auto/Manual Switch

This switch operates in conjunction with the continuous on/off switch. When the start key is pressed, commands are executed once or continuously from either core storage locations or the CE panel entry keys.

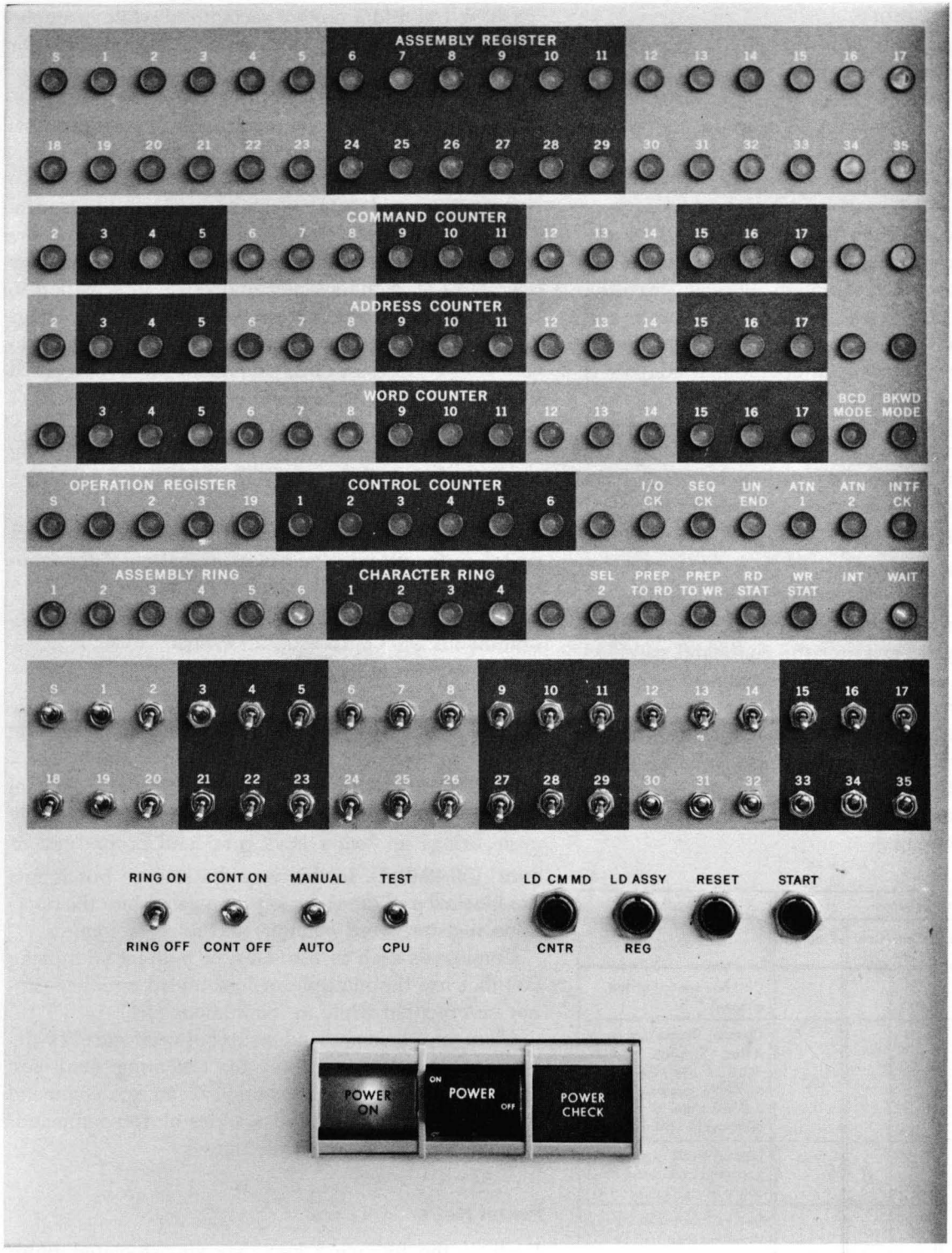


Figure 105. CE Test Panel

AUTO (MULTIPLE STEP MODE)

Pressing the start key with the continuous on/off switch in the OFF position turns off the wait trigger and causes the channel to execute a series of prestored commands from core storage. Locations are determined by either the command counter (for sequential commands) or address counter (for successful transfers).

The first command executed is determined by the command counter value. Once started, commands are executed and requested through normal circuitry. Commands such as CTL, CTLW, CTLR, SNS, CPYP, and CPYD that require service request pulses from an I-O adapter will be executed if an operational adapter is attached.

If the start key is pressed with the continuous on/off switch in the ON position, the 7909 repeatedly executes the command set into the CE panel entry keys.

A chart of operations for various positions of the CE test switch settings is shown in Figure 106.

MANUAL (SINGLE-STEP MODE)

Pressing the start key with the continuous on/off switch in the OFF position turns off the wait trigger, initiates a BCW cycle, executes the command specified by the command counter, and steps the counter +1. A command required signal (50.37.01.1) is prevented from initiating a new BCW cycle and the operation stops. Further depressions of the start key cause either the next sequential commands or, in the case of a successful transfer, the command at the transferred to address to be executed.

Test Switch Settings							Operation
Test/CPU		Man./Auto.		Cont/Cont On/ Off		Ring On	
	√						CPU has control of the channel
√						√	Channel forced into write status. Simulate "service requests" and take necessary BDW cycles. AC and WC steps for each BDW cycle initiated.
√		√			√		Depress start; execute command specified by CC and stop. CC stepped + 1
√			√		√		Depress start; execute command specified by CC and step to next command - continue through I-O program.
√		√		√			Depress start; execute command in CE entry keys once and stop.
√			√	√			Depress start; continually execute command in CE entry keys.

Figure 106. CE Panel Operations

Check conditions are not recognized while in single-step mode (Figure 107). This mode is not intended for interface operations. The speed of attached I-O devices makes it impossible to perform proper stepping between interface and copy commands. Service requests from the adapter are accepted and serviced; however, ends or unusual ends are blocked.

CTL, CTLW, and CTLR commands execute the control portion but hang up the channel at end time, and the reset pushbutton must be used before continuing. SNS operations start the adapter and cause information to be sent to the channel. However, the operation hangs up the channel at end time and no data are sent to core storage. CPYP or CPYD commands are not executed (channel hangs up) because of no previous read or write to condition the adapter.

Commands such as TCH, LIPT, or indirect addressing (IA), which use the multiplexor look-ahead circuitry, can be executed in single-step mode.

Pressing the start key with the continuous on/off switch in the ON position causes execution of the command set up in the CE panel entry keys.

Continuous On/Continuous Off Switch (Continuous Enter Keys)

This switch operates in conjunction with the auto/manual switch and when in the ON position causes the channel to obtain its next command from the CE entry keys. With the switch in the OFF position, the channel obtains its commands from core storage. Each BCW cycle brings up "enter keys gate" and drops "CPU or auto" (50.40.01.1). In this way the storage bus inputs are blocked and the entry keys are gated into the operation register, word counter, and address counter.

Commands such as TCH, LIPT, or indirect addressing (IA) that use the multiplexor look-ahead circuitry cannot be executed while in "continuous on."

Changing the command setup between start key depressions provides a means for executing small test routines. For example, execution of an LCC command with a 77_8 count field, and a series of TDC commands checks stepping the control counter.

Panel Keys

Each of the following keys has an associated pulse forming network (located in back of the CE panel) which produces a negative pulse of approximately .5 μs when the corresponding key is depressed.

Start Key

With the channel in TEST status, operation of this key turns off the wait trigger, initiates a BCW cycle, and starts the channel in operation as previously described.

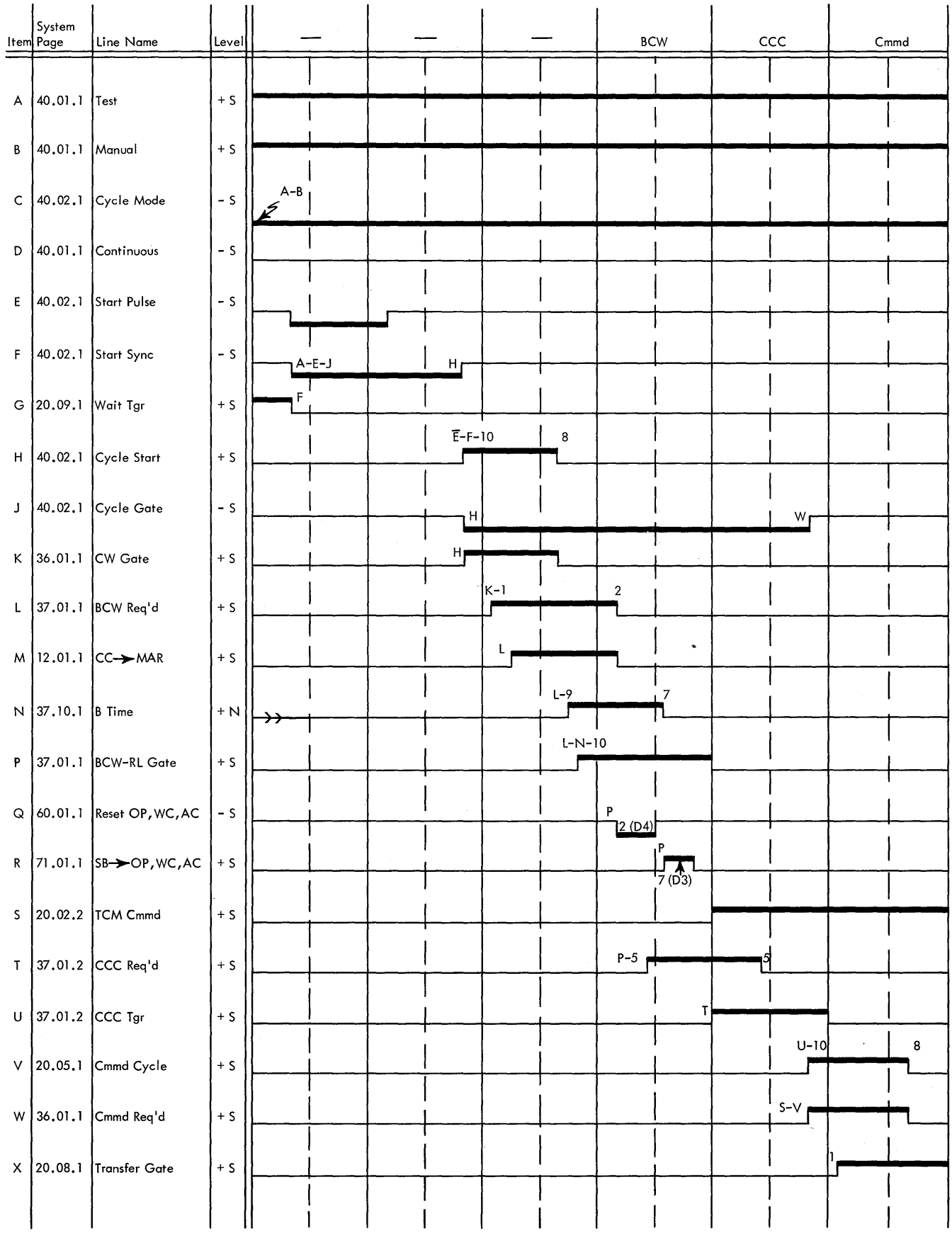


Figure 107. Manual (Single-Step Mode) Operation

Reset Key

With the channel in TEST status, depression of this key causes a complete channel reset and a 6 μs operational out pulse to be sent to the adapter.

Load Assembly Register Key

This key is operative only when the channel is in TEST status and the auto/manual switch is in the MANUAL position. Pressing the key causes the CE entry keys to be routed through the data register and into the assembly register. No BCW cycle is required to perform the operation. Also, because no reset pulse is generated to the assembly register, information routed from the entry keys will be OR'ed to those corresponding assembly register positions.

Pressing this key when the auto/manual switch is in the AUTO position has no effect.

Load Command Counter Key

This key is operative only when the channel is in TEST status and the auto/manual switch is in the MANUAL position. Pressing the key causes CE entry key positions 21-35 to be routed to the command counter. No BCW cycle is required to perform the operation. Also, because no reset pulse is generated to the command counter, information routed from the entry keys is OR'ed to those corresponding command counter positions.

Pressing this key when the auto/manual switch is in the AUTO position has no effect.

Operator's Lights and Switches

In addition to the various CE indicator lights and switches on the test panel, there are power check light, power on light, and power on/off switch.

The power on/off switch in the OFF position removes DC by cutting off 400 cps to the channel. AC power is also removed from the blower motors. Placing the switch in the ON position picks a contactor in the power distribution unit and applies necessary power to the channel (provided that power is properly available at the PDU).

The power on light indicates that 400 cps is available to the channel's DC power supplies and all DC voltages are on.

The power check light indicates that some type of power failure has occurred within the 7909 Data Channel.

More information concerning these lights and switches can be found in the section on "Power Supply."

The 7909 Data Channel has a self-contained DC power supply as shown in Figure 108. AC electrical power is fed to the channel by two connectors (Figure 6): a 24-position connector to provide 400 cps and a 34-position connector to supply 60 cps. Use of 400-cycle power within the 7909 to generate the required DC voltages provides compatability with other channels connected to the system. These 24- and 34-position connectors can be used with either 7909 or 7607 Data Channels.

Four different drawers in the power supply unit produce the necessary voltages. From top to bottom they are:

−12 volt 40 amp supply
+12 volt 15 amp supply
+30 volt and −36 volt 2 amp supplies
±6 volt 2 amp supplies

Each power supply has its own circuit breaker protection. The −12 volt supply has the heaviest demands placed on it and is divided into four sections. Each −12 volt section has its own protective CB and feeds one of the four logic panels within the channel (CB's 1, 2, 3, 4 feed panels 1, 2, 3 and 4, respectively). All of the CB's are wired in series such that the failure of one supply removes all DC from the channel by tripping the main CB.

The +12 volt supply is the only one capable of being biased. A marginal check relay located on the drawer can be activated from the CE panel on the 7151 console. When the relay is picked, the normal 400 cps supply is replaced by three special 400 cps lines to the channel.

Lights and Switches

Two lights and one switch (Figure 105) are located on the customer engineer's test panel.

Power On/Off Switch

This switch initiates the operation in the power distribution unit which brings up 400-cycle power to the 7909. This switch is ineffective, however, if the main CB on the 7909 power supply is tripped.

Placing the switch in the OFF position immediately removes the 400 cps supply from the PDU to the channel; however 115v is still present across the switch.

There is no power-off switch in the back of the 7909 channel. However, manually tripping any of the CB's on the various power supply drawers will trip the main CB and remove all power in the same way as the switch at the CE panel in front of the machine.

Power On Light

This light is on whenever 400 cps power is being supplied to the channel. It will be off when the 7909 power off switch is in the OFF position or when the main CB is tripped on the 7909 power supply.

Power Check Light

This light is on whenever there are −48 volts on the system and the 7909 main CB has been tripped. The power on light should be off when the power check light is on.

Power Supply Control and Protection Circuits

Assume that power is available to the system and all CB's are in their normally closed positions. The power on switch (Figure 109) placed in the ON position completes a circuit from the power on input cable, through the main CB SSW, and out the power on interlock cable. This picks a power contactor for this channel in the 7618 power distribution unit and sends 3-phase 208-volt 400 cps power to the channel. At the same time, duo relay (DR 1) picks to light the power-on light through the AU points and produce a 3 μs channel power-on reset (50.63.01.1) through the BU points.

Relay R1 has in series with it the normally closed points of nine power supply CB's, a normally closed blower failure detection contact, and two normally closed thermal contacts located in panels 1 and 2. R1 remains picked as long as all contacts remain in the normally closed position.

The tripping of any DC voltage CB, or opening of the thermals or blower failure points causes R1 to drop out. The R1 point energizes the main CB trip coil in the 7909 and removes all 400 cps power from the channel. In addition, the main CB (through its side switches) causes the contactors in the 7618 power distribution unit for this 7909 to drop out and remove 400 cps power from the channel input. The power check light on the 7909 is turned on and the power on light is turned off; the latter occurs as the DR 1 AU points open. In addition, the I-O power check light on the 7151 console is also turned on.

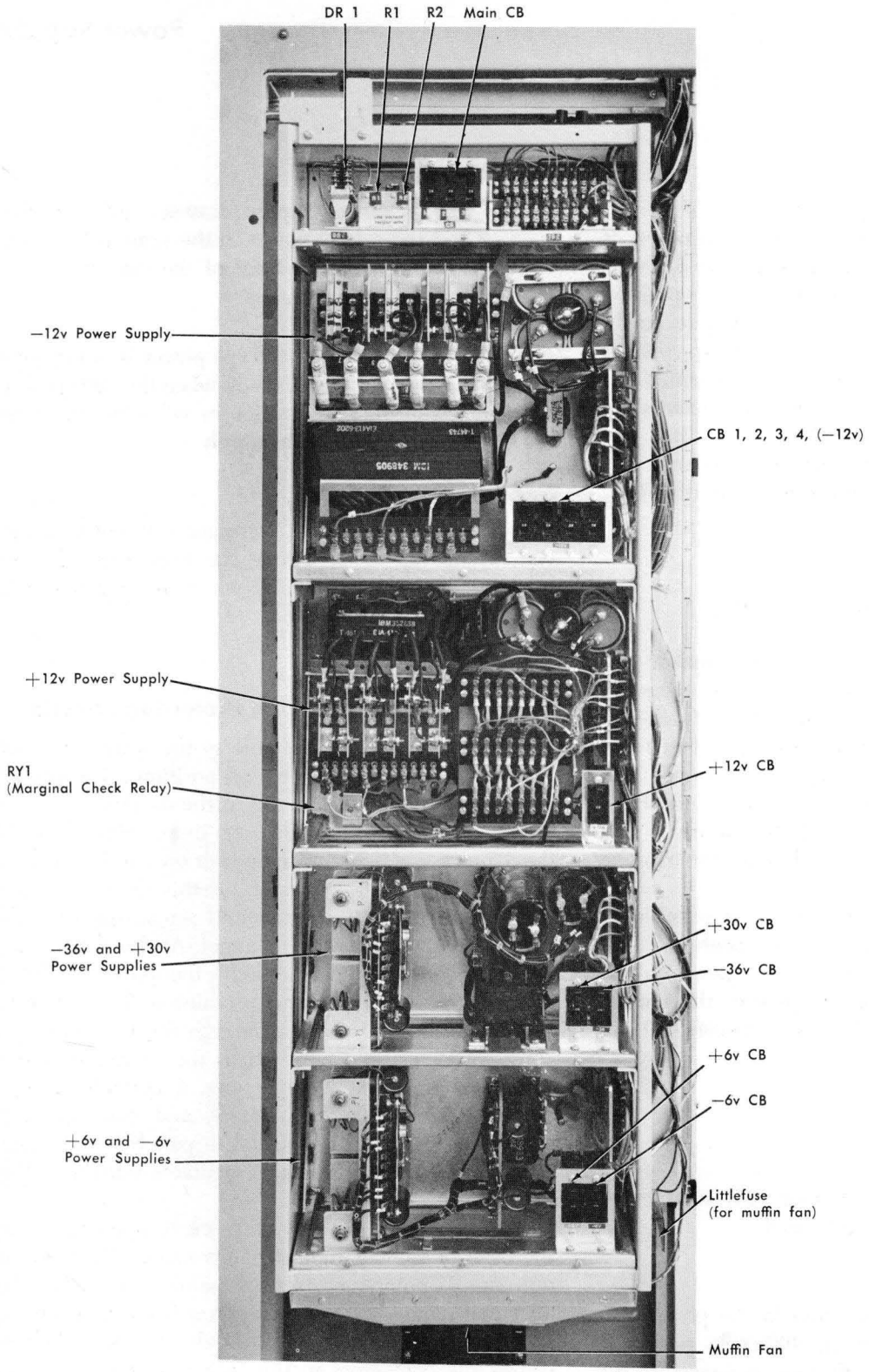


Figure 108. Power Supply Locations

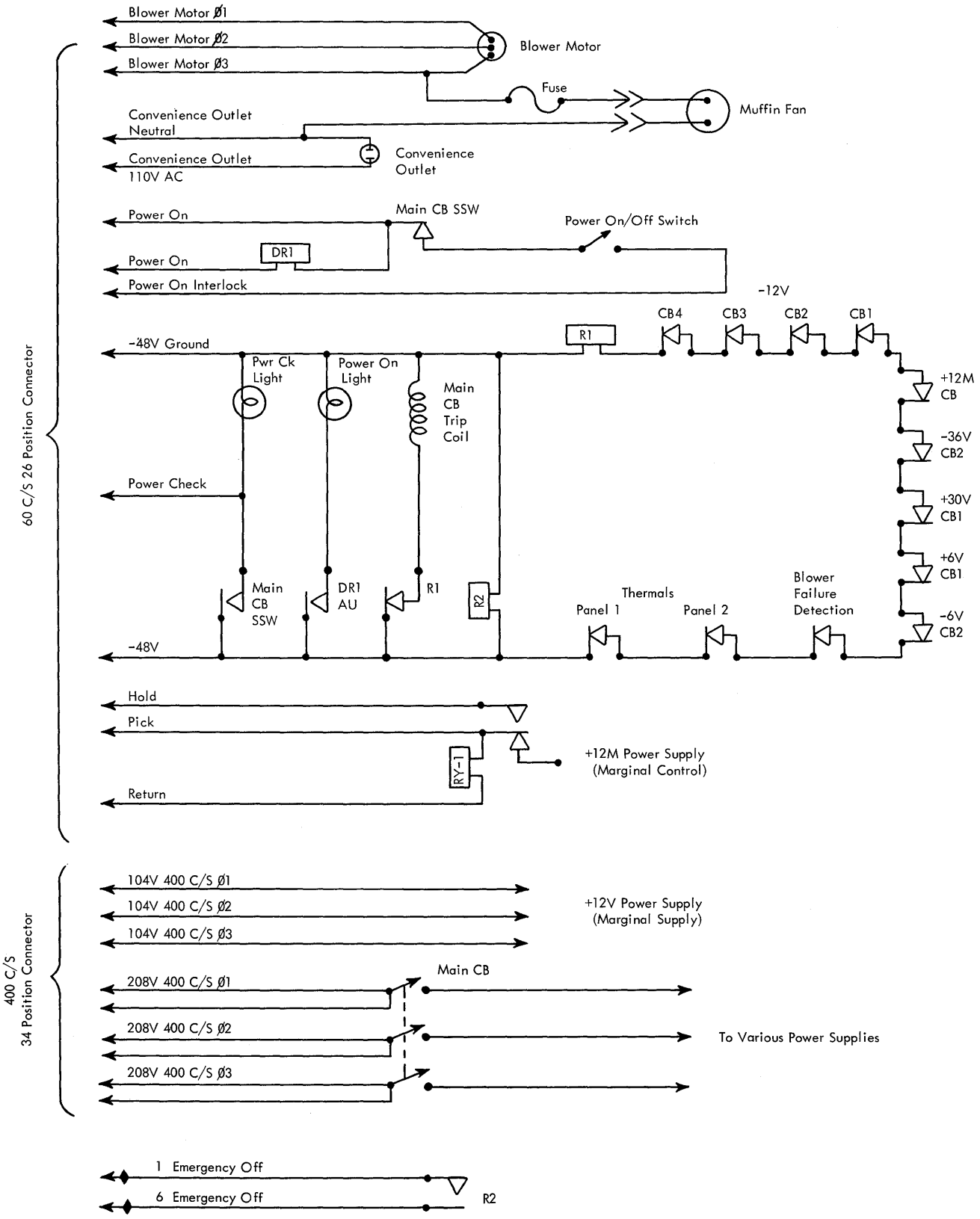


Figure 109. Power Supply Controls

Pulling the emergency power off switch on the 7151 console, a failure of the 48-volt supply, or removing the 60-cycle power cable from either the 7909 or 7618 causes relay R2 to drop out. The R2 points open the power interlocking circuitry to the channel adapters (Figure 108) and cause their power to be dropped. In this manner, an emergency power-off indication can remove power from the entire system.

Power Supply Color Coding

Ground	Black
− 6v	Blue
−12v	Purple
+12v	White
+30v	Pink
−36v	Brown
+ 6v	Orange

Marginal Voltage Requirements

The +12M voltage is the only voltage varied for marginal checking. This voltage is varied by depression of the −12v marginal voltage pushbutton on the 7151 console. The voltage at the 7909 logic panels shall vary ±3 volts; bias voltage limits for all 7909 channel programs shall be ±2.5v from the nominal setting of +12v for 7090 and ±2.0v for 7094.

It is necessary to mentally reverse the indicated voltage signs when reading the DC voltmeter and operating the −12v control switch on the 7151 CE panel. For example, the −12v control switch in the −15v position indicates a +15v for the 7909 channel, and the voltmeter indicates a plus rather than a minus value.

Appendix A—Test Panel Operation for Checking 7909 Registers

Switch Setting	Operation
1. Test on/Press Reset	Assem Ring 6, CRT 4, and wait lights should be on.
2. Ring on/Manual/Test Load Cmmd Ctr, Assembly Reg with	Ripples the assembly ring, char ring, word counter, address counter, command counter. Note any failing counter positions. All positions should ripple. If there is a bad position, ripple will go up to the bad position and stop. If this is common to all counters, look for a bad storage register or half-adder position.
3. Test/Auto/Cont on	a. Load assm reg with bits. Put store assm reg (SAR) to any location in the switches. b. Put LAR from the same location in the switches. The assembly register should contain all bits. This checks information flow from assembly register to data register and back.
4. Test/Auto/Cont on	Put LCC in op keys and load the control counter with bits. Check to see that all positions loaded.
5. Test/Manual Cont on	Put TDC in the op keys and step the control counter down. If in auto, operation is too fast to see.
6. Test/Manual Cont on	Reload control counter (test 4)
7. Test/Auto/Cont on	Perform ICC 1-6 and watch the assembly ring for proper gating. Also perform ICC WC = 7 to see if NOP comes on.
8. Test/Auto/Cont on	Perform SMS with bits in 29-35. Check to see which op features are on. Then perform ICC to see if proper assembly ring six bits come on.
9. Test/Auto/Cont on	Load assembly register with a random pattern. Perform a TCM with matching or unmatching bits in the mask (12-17). If conditions are met, TCM should transfer; this is indicated by the command counter failing to ripple. If conditions are not met, the CC ripples. Check with bit in 11. Check TCM with WC = 7 for transfer if no bits are in mask. TCM with WC = 0 cannot be checked in this manner as the check condition register is involved.
10. Test/Auto/Cont on	Perform a XMIT, WC = 60,000. All counters will ripple. Watch for read to write status change.
11. Test/Auto/Cont on	a. Perform CTLR. See that prep to read and write status triggers are on. b. Perform CTLRN (bit in 4) to see if prep to read only stays on. c. Repeat the step a using CTLW. Prep to write and write status should be on. d. CTLWN write status should go off.
12. Test/Auto/Cont on	Perform SNS to see if sense trigger comes on on the 7631 console.
13. Test/Auto/Cont on	Perform CTL from 500. At this point, store different control bytes at location using the 7151 console. a. Store bits at 500. The input/output reg and signal reg lights should come on at the 7631. b. Perform control ops by storing bytes at location 500 and watch corresponding 7631 lights to see that they come on.
14. Run Diagnostics	

Appendix B—Triggers and Locations

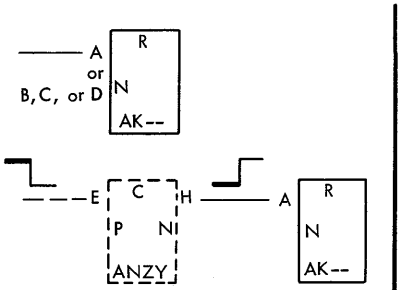
Trigger	Systems
Acc Req'd	50.37.03.2
Acc Tgr	50.37.03.2
Address Counter 3	50.30.15.1
Address Counter 4	50.30.14.1
Address Counter 5	50.30.13.1
Address Counter 6	50.30.12.1
Address Counter 7	50.30.11.1
Address Counter 8	50.30.10.1
Address Counter 9	50.30.09.1
Address Counter 10	50.30.08.1
Address Counter 11	50.30.07.1
Address Counter 12	50.30.06.1
Address Counter 13	50.30.05.1
Address Counter 14	50.30.04.1
Address Counter 15	50.30.03.1
Address Counter 16	50.30.02.1
Address Counter 17	50.30.01.1
Assembly Register S-5	50.27.01.1
Assembly Register 6-11	50.27.02.1
Assembly Register 12-17	50.27.03.1
Assembly Register 18-23	50.27.04.1
Assembly Register 24-29	50.27.05.1
Assembly Register 30-35	50.27.06.1
Assembly Ring 1-3	50.23.01.1
Assembly Ring 4-6	50.23.02.1
Assembly Ring Drive	50.22.01.1
Attention 1	50.80.02.1
Attention 2	50.80.02.1
Attention Response Gate	50.80.02.1
BCD	50.20.15.1
BCW Req'd	50.37.01.1
BCW Tgr	50.37.01.1
BDW Req'd	50.37.03.1
BDW Tgr	50.37.03.1
C Reg P	50.28.06.1
CCC Req'd	50.37.01.2
CCC Tgr	50.37.01.2
Char Reg B, A	50.28.09.1
Char Reg 8, 4	50.28.10.1
Char Reg 2, 1	50.28.11.1
Character Ring 1 & 2	50.25.01.1
Character Ring 3 & 4	50.25.02.1
CMMD Cycle	50.20.05.1
Command Counter 3	50.30.15.1
Command Counter 4	50.30.14.1
Command Counter 5	50.30.13.1
Command Counter 6	50.30.12.1
Command Counter 7	50.30.11.1
Command Counter 8	50.30.10.1
Command Counter 9	50.30.09.1
Command Counter 10	50.30.08.1
Command Counter 11	50.30.07.1
Command Counter 12	50.30.06.1
Command Counter 13	50.30.05.1
Command Counter 14	50.30.04.1
Command Counter 15	50.30.03.1
Command Counter 16	50.30.02.1
Command Counter 17	50.30.01.1
Control Counter T1 & T2	50.33.03.1
Control Counter T3 & T4	50.33.02.1
Control Counter T5 & T6	50.33.01.1
Control Gate	50.20.07.1
Ctr Zero	50.20.08.1
Cycle Gate	50.40.02.1
Data Register S-2	50.26.01.1
Data Register 3-5	50.26.02.1
Data Register 6-8	50.26.03.1
Data Register 9-11	50.26.04.1
Data Register 12-14	50.26.05.1
Data Register 15-17	50.26.06.1
Data Register 18-20	50.26.07.1
Data Register 21-23	50.26.08.1
Data Register 24-26	50.26.09.1
Data Register 27-29	50.26.10.1
Data Register 30-32	50.26.11.1
Data Register 33-35	50.26.12.1
Data Register Loaded	50.38.01.1
Delay Sync	50.35.02.1
Demand Delay	50.35.02.1
Demand Gate	50.35.01.1
Demand Sync	50.35.01.1
Disable 1	50.20.14.1
Disable 2	50.20.14.1
Enable NCI	50.20.14.1
Enable Trap	50.20.12.1
End Demand	50.52.02.1
End Gate	50.52.02.2
End of Wd	50.35.01.1
End Op Control	50.36.02.1
End Response	50.52.02.1
End Sync	50.52.02.1
I-O Check	50.80.01.1
Inhibit Unusual End	50.20.14.1
Interface Check	50.80.02.1
Interrupt	50.80.03.1
Interrupt BDW Req'd	50.80.03.1
Interrupt Step 1	50.80.03.1
Interrupt Step 2	50.80.03.1
LAR Gate	50.20.10.1
LIP Step 1	50.20.11.1
LIP Step 2	50.20.11.1
Operation Register S-3, 19	50.20.01.1
One Start	50.25.02.1
Prepare to Read	50.16.01.1
Prepare to Write	50.16.01.1
Proceed to E	50.36.02.1
Read	50.16.01.1
Read Backward	50.20.15.1
Resp Gt 1	50.80.02.2
Resp Gt 2	50.80.02.2
Response Gate	50.51.01.1
SAR Gate	50.20.10.1
Select	50.20.14.1
Select Gate	50.52.02.1
Sense	50.20.13.1
Sequence Check	50.80.01.1
Start	50.25.02.1
Start Cycle	50.40.02.1
Start Sync	50.40.02.1
Stop	50.52.01.1
Storage Register 3	50.30.15.1

Trigger	Systems
Storage Register 4	50.30.14.1
Storage Register 5	50.30.13.1
Storage Register 6	50.30.12.1
Storage Register 7	50.30.11.1
Storage Register 8	50.30.10.1
Storage Register 9	50.30.09.1
Storage Register 10	50.30.08.1
Storage Register 11	50.30.07.1
Storage Register 12	50.30.06.1
Storage Register 13	50.30.05.1
Storage Register 14	50.30.04.1
Storage Register 15	50.30.03.1
Storage Register 16	50.30.02.1
Storage Register 17	50.30.01.1
TCH	50.20.02.1
Transfer Gate	50.20.08.1
Transmit Gate	50.20.06.1
Trap Priority	50.39.02.1
Trap Sync	50.20.12.1

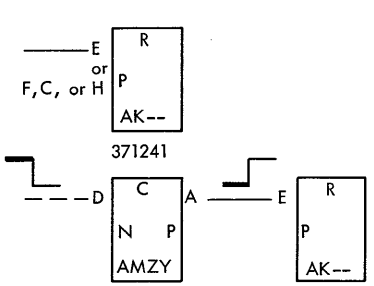
Trigger	Systems
Unusual End	50.80.01.1
Wait	50.20.09.1
Word Counter 3	50.30.15.1
Word Counter 4	50.30.14.1
Word Counter 5	50.30.13.1
Word Counter 6	50.30.12.1
Word Counter 7	50.30.11.1
Word Counter 8	50.30.10.1
Word Counter 9	50.30.09.1
Word Counter 10	50.30.08.1
Word Counter 11	50.30.07.1
Word Counter 12	50.30.06.1
Word Counter 13	50.30.05.1
Word Counter 14	50.30.04.1
Word Counter 15	50.30.03.1
Word Counter 16	50.30.02.1
Word Counter 17	50.30.01.1
Write	50.16.01.1
Write Stop	50.52.01.1

Coupling Network for N and P Blocks

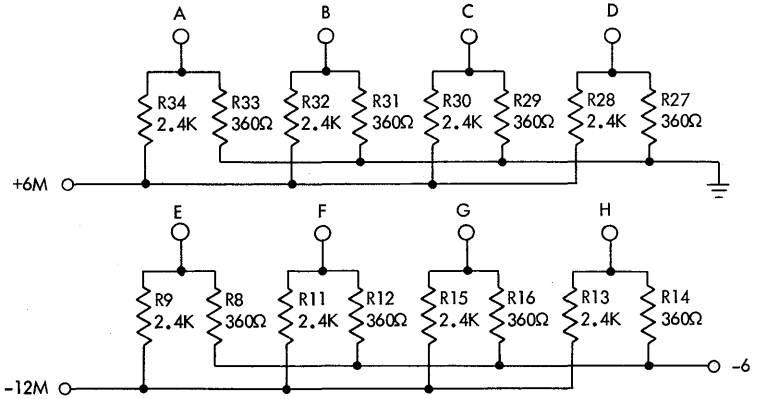
AK__
371241



Block Configuration and Typical Application



Block Configuration and Typical Application

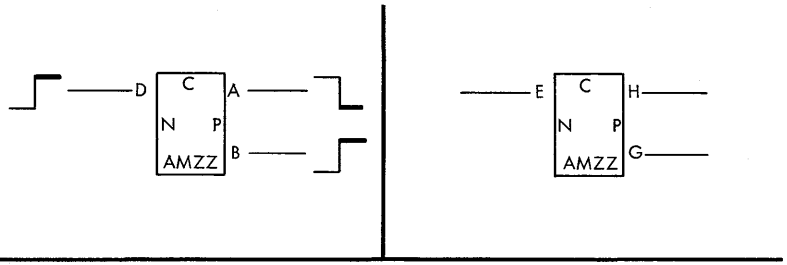


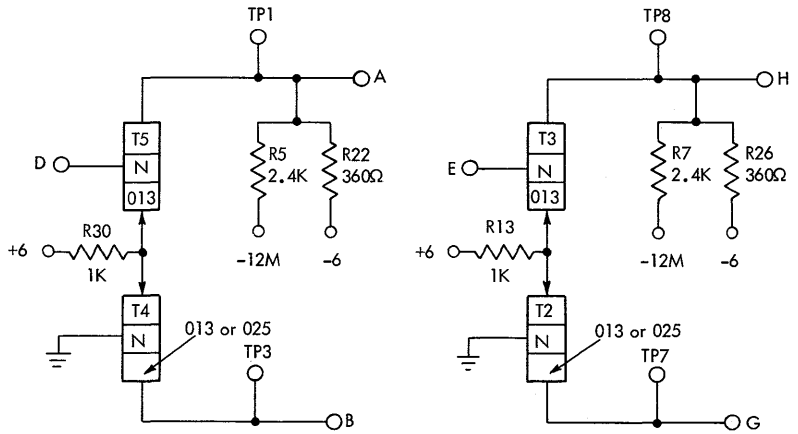
Note: The phase is determined by the phase of the output from the driving stage

N-Line Output				P-Line Output			
In Phase		Out of Phase		In Phase		Out of Phase	
Min	Max	Min	Max	Min	Max	Min	Max
+.4 / -.4	+1.15 / -2.5	+.4 / -.4	+1.15 / -3.0	— / -5.6 / -6.4	— / -3.5 / -7.15	— / -5.6 / -6.4	— / -3.0 / -7.15
EC Level	8-15-61	112388					

1-Way N to P Converter Circuit

AMZX
371202



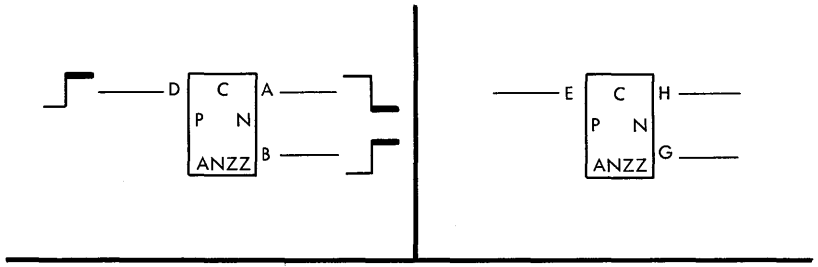


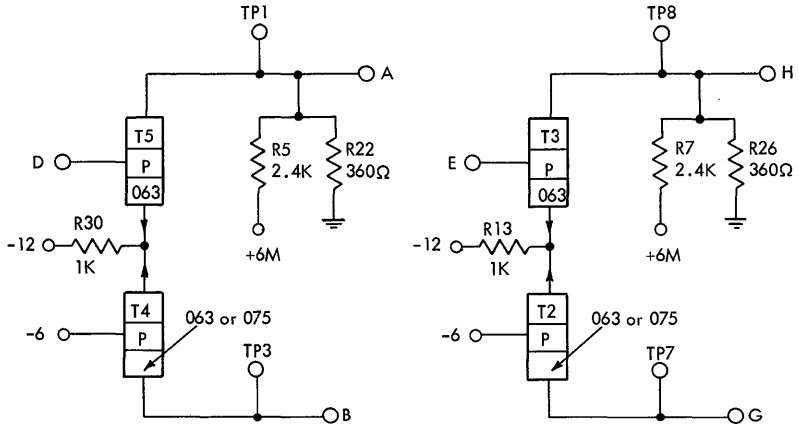
Input Levels	Output Levels			
	In Phase	Out of Phase		
Nominal	Nominal	Min	Max	
+.4 / -.4	— / -5.6 / -6.4	— / -4.86 / -6.71	— / -4.34 / -6.86	
EC Level	6-20-60	D109187		

	ns Delay per		
	Block	100 uufd Load	Driven Base
Min	30	20	30
Nom	65	25	35
Max	100	30	40

1-Way P to N Converter Circuit

ANZX
371211

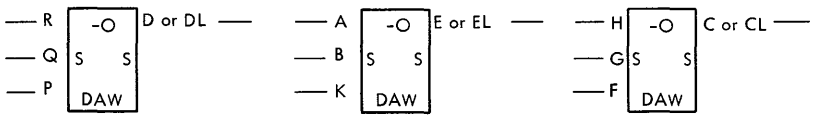


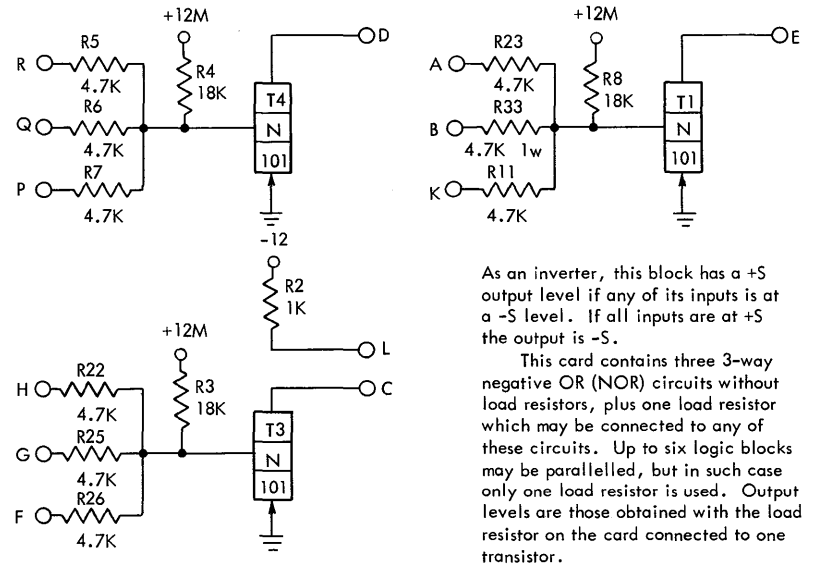


Input Levels	Output Levels			ns Delay per			
	In Phase	Out of Phase			Block	100 uufd Load	Driven Base
Nominal	Nominal	Min	Max				
				Min	30	20	30
				Nom	65	25	35
				Max	100	30	40
-5.6 / -6.4	+.8 / -.8	+.4 / -.4	+1.15 / -3.0				
EC Level	8-25-60	D109878					

3-Way NOR Inverter (SDTRL)

DAW
370083





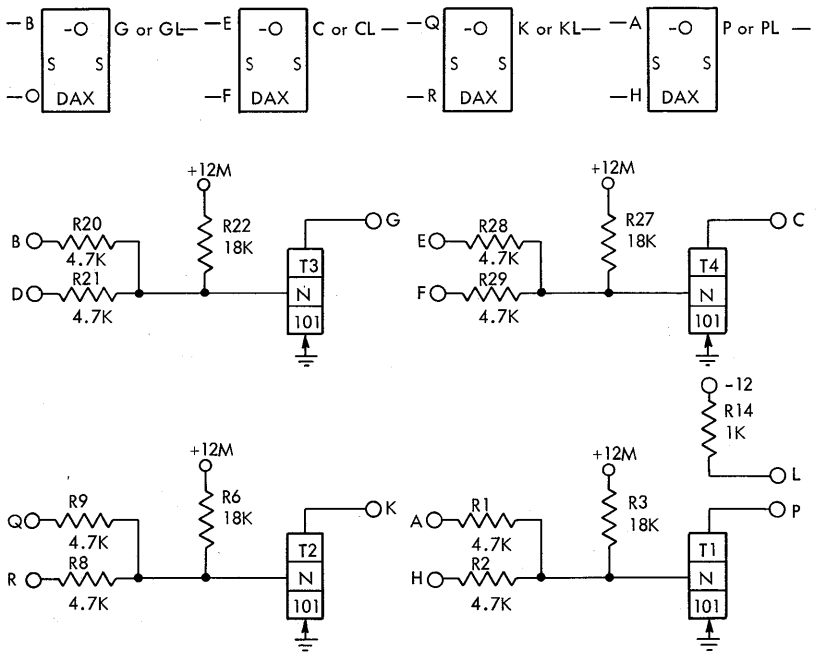
As an inverter, this block has a +S output level if any of its inputs is at a -S level. If all inputs are at +S the output is -S.

This card contains three 3-way negative OR (NOR) circuits without load resistors, plus one load resistor which may be connected to any of these circuits. Up to six logic blocks may be parallelled, but in such case only one load resistor is used. Output levels are those obtained with the load resistor on the card connected to one transistor.

Input Levels		Output Levels		ns Block Delays		
		Out of Phase			Turn On	Turn Off
Min	Max	Min	Max	Min	43	128
				Nom	84	191
-6 / -6.87	-.05 / -12.48	-.45 / -6.87	-.05 / -12.48	Max	125	254
EC Level		5-25-61	112019			

2-Way NOR Inverter (SDTRL)

DAX
370084



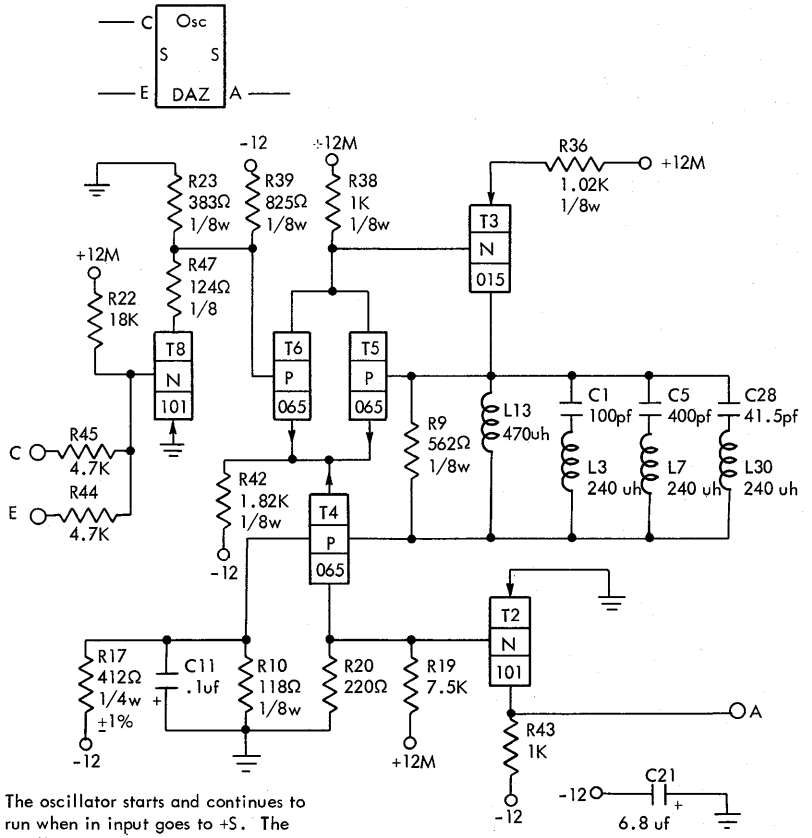
As an inverter, this block has a +S output if either of its inputs is a -S level. If both inputs are +S, the output is at a -S level.

This card contains four 2-way negative OR (NOR) circuits without load resistors, plus one load resistor which may be connected to any of these circuits. Up to six logic blocks may be parallelled, but in such case only one load resistor is used. Output levels are those obtained with the load resistor on the card connected to one transistor

Input Levels		Output Levels Out of Phase		ns Block Delays		
					Turn On	Turn Off
Min	Max	Min	Max	Min	43	128
-.6 / -6.87	-.05 / -12.48	-.45 / -6.87	-.05 / -12.48	Nom	84	191
				Max	125	254
EC Level	5-25-61	112019				

240 kc S-Line Gated Oscillator

DAZ
370127

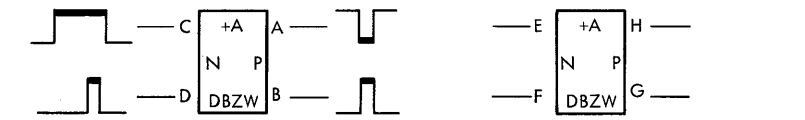


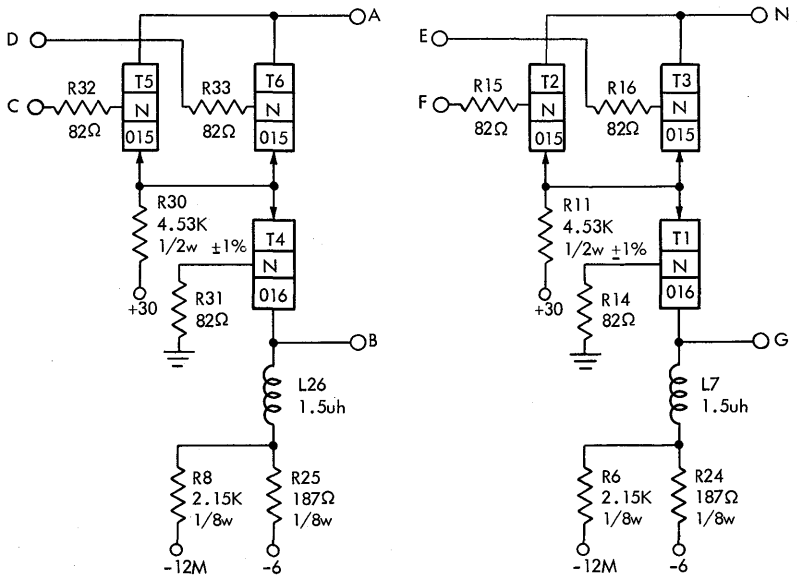
The oscillator starts and continues to run when in input goes to +S. The oscillator stops when the input goes to -S

Input Gate Levels		Osc Output Levels		Osc Output Frequencies	
Min	Max	Min	Max	Min	225.2 kc
-.45 / -6.87	-.05 / -12.48	-.45 / -6.87	-.05 / -12.48	Nom	239 kc
				Max	262.5 kc
EC Level	8-28-61	112437			

2-Way N to P Circuit

DBZV
371285

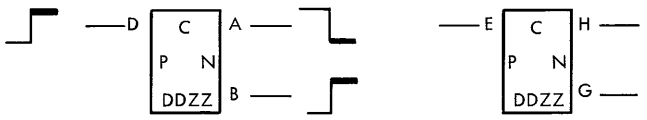


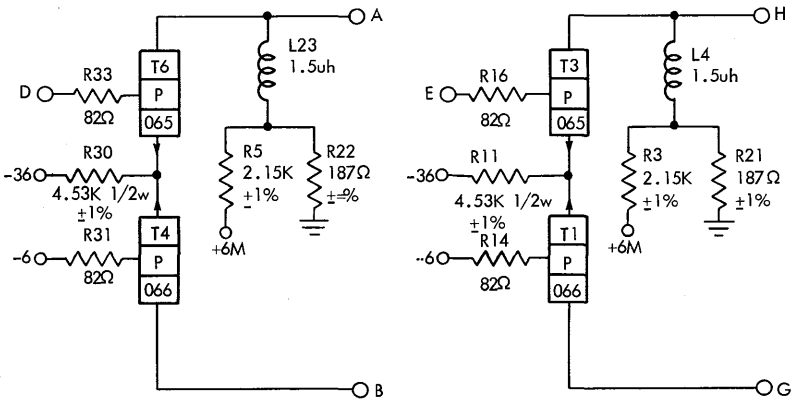


	Output Levels			ns Block Delays		
Input Levels	In Phase		Out of Phase		Turn On	Turn Off
Nominal	Min	Max	Nominal	Min	8	3
				Nom	17	8.5
				Max	26	14
+.4 / -.4	—	—	—			
	-5.6 / -6.4	-5.19 / -6.51	-5.6 / -6.4			
EC Level	9-28-60	D109899				

1-Way P to N Converter

DDZX
371310

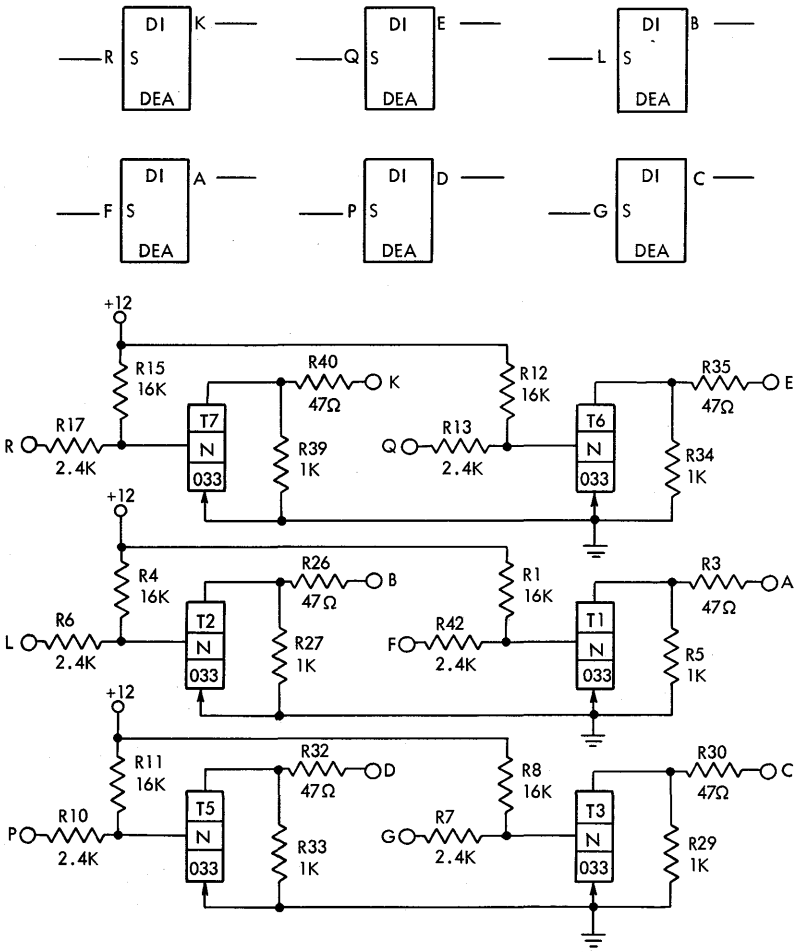




	Output Levels				ns Block Delays		
Input Levels	In Phase		Out of Phase			Turn On	Turn Off
Nominal	Min	Max	Min	Max	Min	4	7
					Nom	13	14
					Max	23	21
— / -5.6 / -6.4	+.4 / -.4	+.51 / -.75	+.4 / -.4	+.51 / -.81			
EC Level	6-16-60	109191					

Indicator Driver

DEA
371941



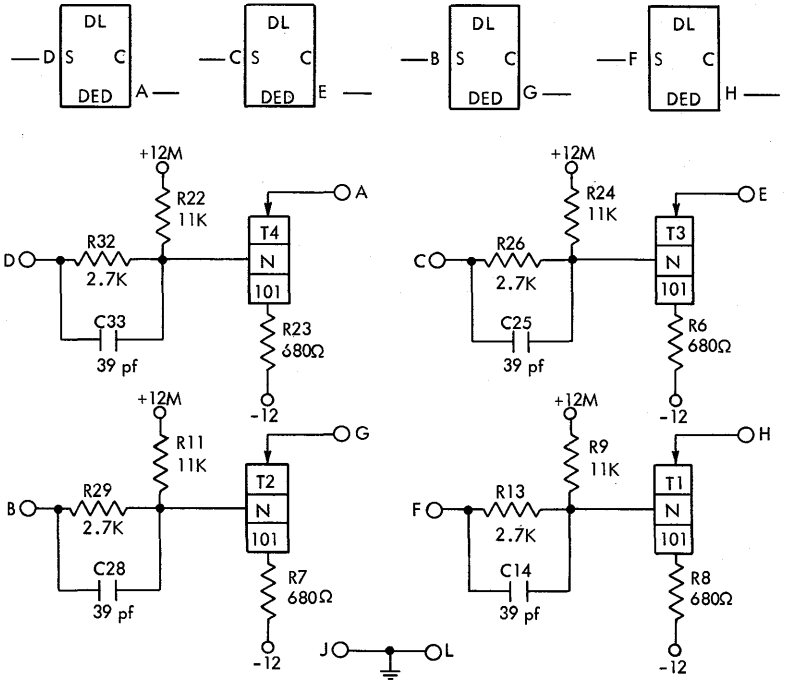
The DI illuminates a 10 ESB indicator with a -S level and turns off the indicator with a +S level

Input Levels	
Min	Max
-.65	-.1
-6.85	-12.48

EC Level	9-28-60	D110063

Standard S to C
Cable Driver (SDTRL)

DED
371987



The DL accepts an SDTRL input and converts it to drive a transmission line with 91-ohm to 120-ohm characteristic impedance. The line must be terminated with a "standard cable terminator" from any circuit family (-C level output current has a nominal current of 15.45 ma)

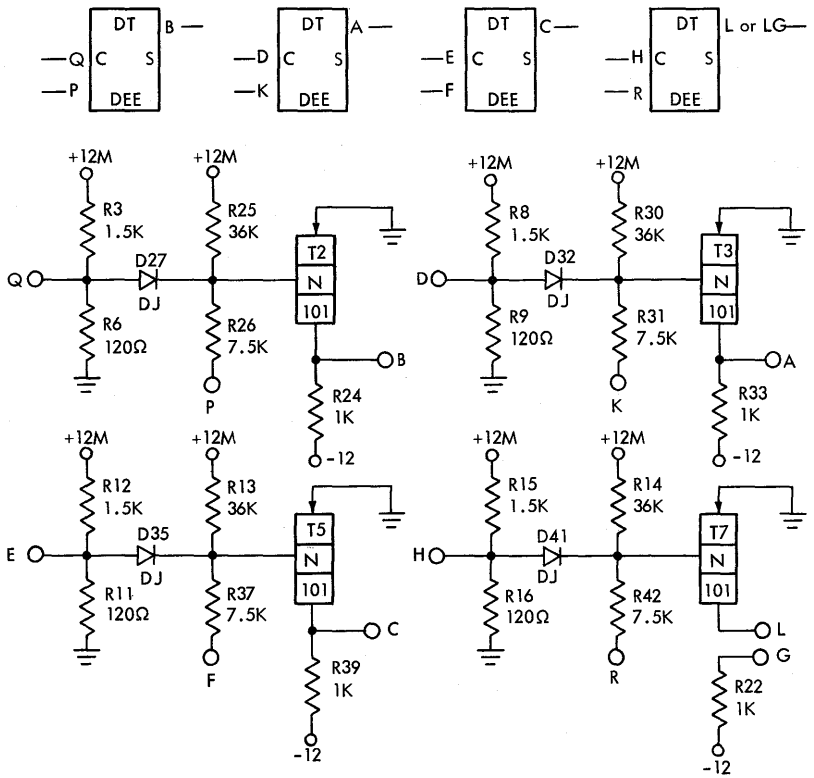
Note: In the UP level (+C), the circuit appears as a high impedance current source. No voltage levels are given

Input Levels		Output Levels Out of Phase		ns Block Delays	Turn On	Turn Off
Min	Max	Min	Max	Min	25	3
-.65	-.1	Note	Note	Nom	28	4.5
-6.85	-12.48	-1.232	-3.07	Max	31	6
EC Level	5-2-61	111806				

SDTRL NOR Standard Cable Terminator Gated (C to S Level)

DEE

371988



This circuit provides compatibility with any standard cable driver. It also provides the proper termination to any standard transmission cable

The gate input (pins P, K, F, or R) can be used to gate the incoming signal. If the gate is not used, it can be tied to -12v. One circuit (L-pin) has a disconnected load

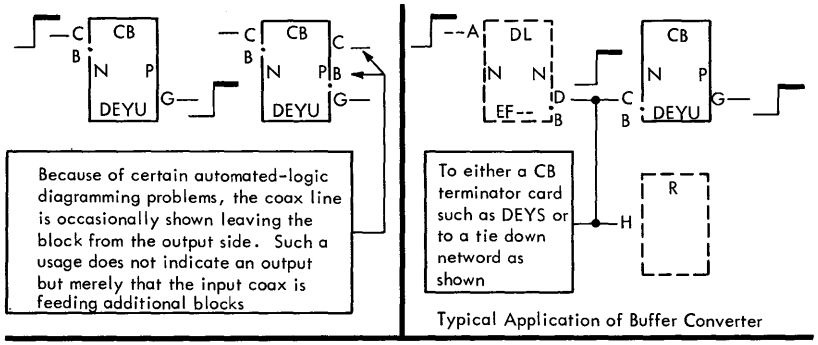
Input Levels				Output Levels		ns Block Delays			
Cable Input		Gate Input		Out of Phase				Turn On	Turn Off
Min	Max	Min	Max	Min	Max	Cable	Min	31	60
+.55 / -.37	+1.17 / -6.	-.65 / -6.85	----- / -12.48	-.45 / -6.85	-.05 / -12.48		Max	37	85
						Gate	Min	61	63
							Max	78	156

EC Level	10-2-61	112420

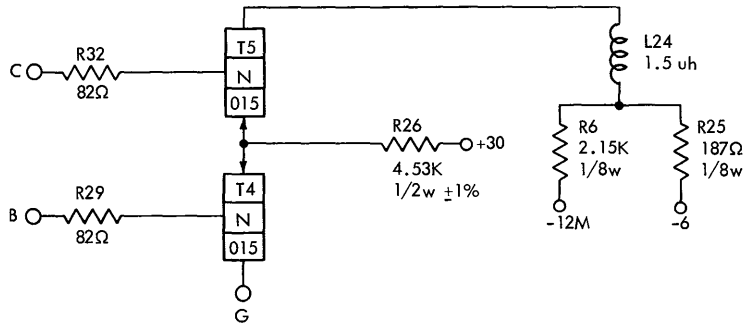
Differential Amplifier (N to P)

DEYT

371327



Typical Application of Buffer Converter



The CB is differential amplifier plus a network to terminate a 93-ohm coax line

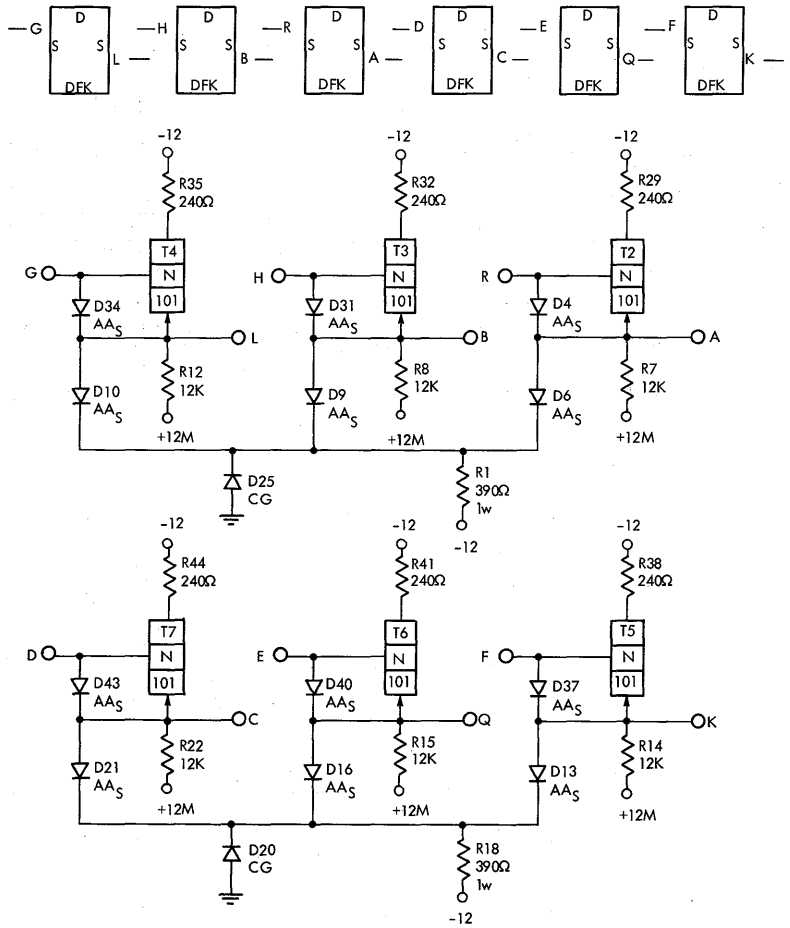
Note: A differential amplifier can be pulled out of the gate with power on without causing damage, but a differential amplifier terminator must not be removed with power on. Doing so can cause transistor failure on all the differential amplifiers on the same coax line. It can also cause failure of the electrolytic capacitor on the transmission line driver that is driving the coax line

Output Levels				ns Block Delays		
Input Levels	In Phase	Out of Phase			Turn On	Turn Off
Nominal	Nominal	Min	Max	Min	4	7
+.4 / -.4	— / -5.6 / -6.4	— / -5.6 / -6.4	— / -5.19 / -6.51	Nom	13.5	14
				Max	23	21

EC Level	12-15-61	113095

SDTRL-Driver - Low-Power Non-Inverting (LPNI)

DFK
370231

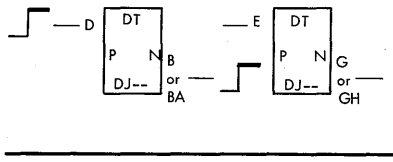


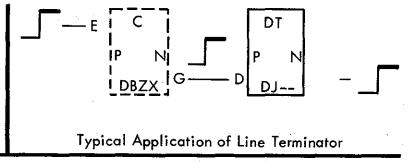
This circuit is basically an emitter follower which provides powering to a number of logic loads without inverting the input signal

Input Levels		Output Levels In Phase		ns Block Delays		
					Turn On	Turn Off
Min	Max	Min	Max	Min	0	2
-.45	-.05	-.7	-.1	Nom	4	6
-7.37	-12.48	-6.87	-12.48	Max	6	8
EC Level	6-7-62	113941				

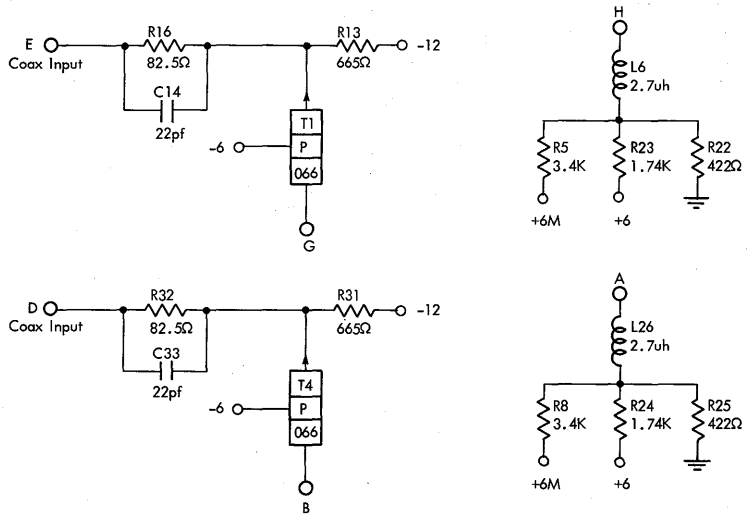
Translating Line Terminator (P to N)

DJ__
371139





Typical Application of Line Terminator



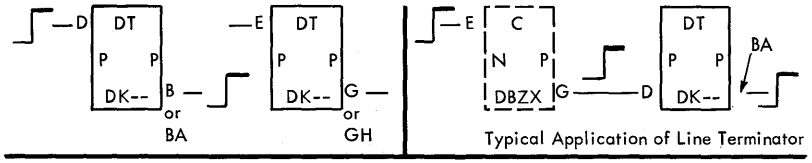
The translating line terminator consists of a single transistor class A grounded base amplifier used to terminate a 93-ohm transmission line. It may also be used just for translation and need not be driven from a transmission line

Output Levels		ns Block Delays		
Min	Max		Turn On	Turn Off
+.4	+1.41	Min	17	20
-.4	-1.36	Nom	21	23.5
		Max	25	27
EC Level	12-15-61	113094		

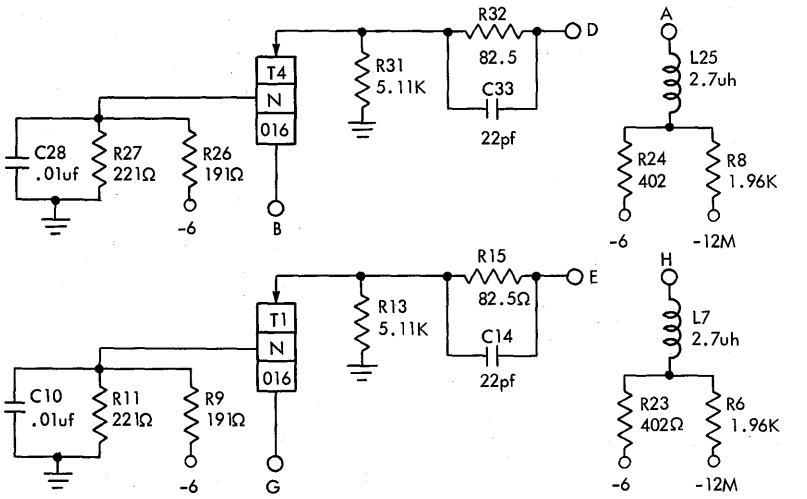
Non-Translating Line Terminator (P to P or N to N)

DK__

371140



Typical Application of Line Terminator



The non-translating line terminator consists of a single transistor class A grounded base amplifier used to terminate a 93-ohm transmission line.

The non-translating line terminator maintains the signal line; an N line remains an N line and a P line remains a P line

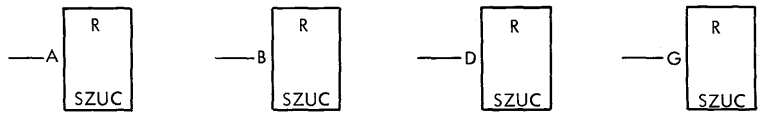
Note 1: Delays are measured from input terminal D of the terminator to the output of the logic block driven by the terminator

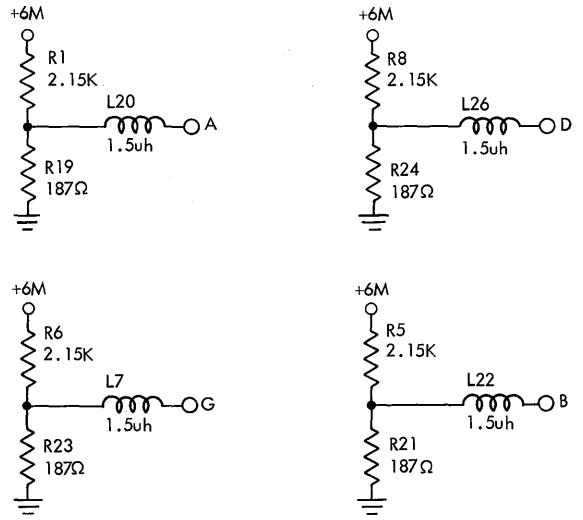
Output Levels (In Phase)				ns Block Delays		
N Line		P Line		Note 1	Turn On	Turn Off
Min	Max	Min	Max	Min	18	16
				Nom	23	22
				Max	28	28
+.4 / -.4	+.90 / -1.65	— / -5.6 / -6.4	— / -4.35 / -6.90			
EC Level	12-15-61	113094				

Load Card

SZUC

371393





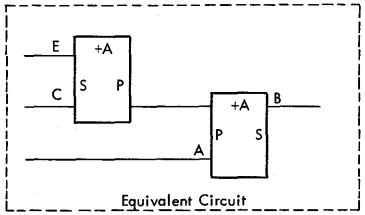
The networks on this card can supply an OFF level bias to six logical blocks or logical block equivalents

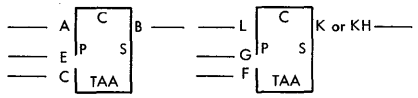
EC Level	12-15-61	113094

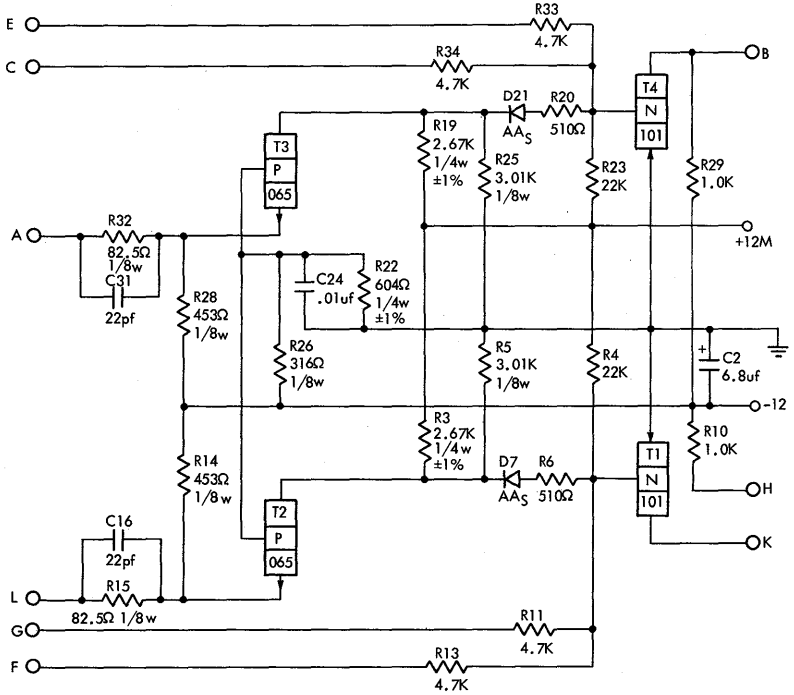
Voltage Levels	
Min	Max
+.4 / 0	+.51 / 0

Converter-Double Gated (P to S)

TAA
370102







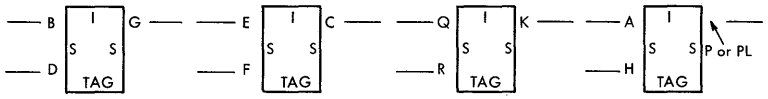
This converter terminates a 93-ohm line and accepts a P-line signal from the coax line and converts it to SDTRL level. By the use of a gate, it can accomplish a 2-way NOR function
Since the output is equivalent to that of a NOR block, circuits are provided with disconnected load resistors. The resistors are back-panel wired if the outputs are not used in a common collector configuration

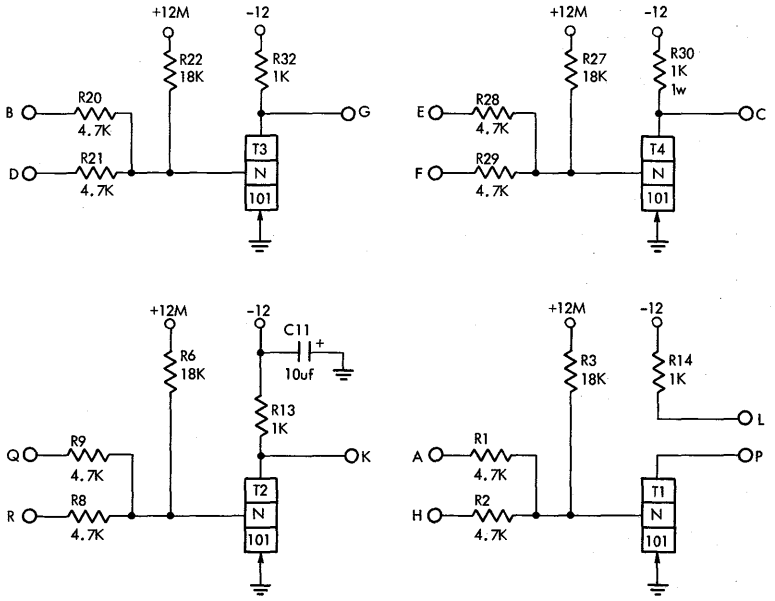
	Input Levels		Output Levels Out of Phase		ns Block Delays	
	Min	Max	Min	Max	Turn On	Turn Off
Min	-.45	-.05	-.45	-.05	50	50
Nom					72	68
Max	-6.87	-12.48	-6.87	-12.48	80	80

EC Level	5-25-61	112019

2-Way NOR Inverter (SDTRL)

TAG
370366





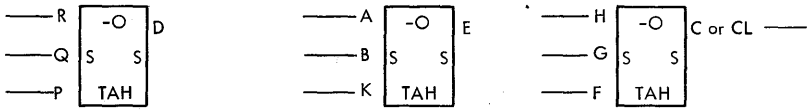
As an inverter, this block has a +S output level if any one of its inputs is at a -S level. When both inputs are at a +S level, the output is at a -S level
One of these circuits has a disconnected load resistor for extender purposes or to allow driving special circuits

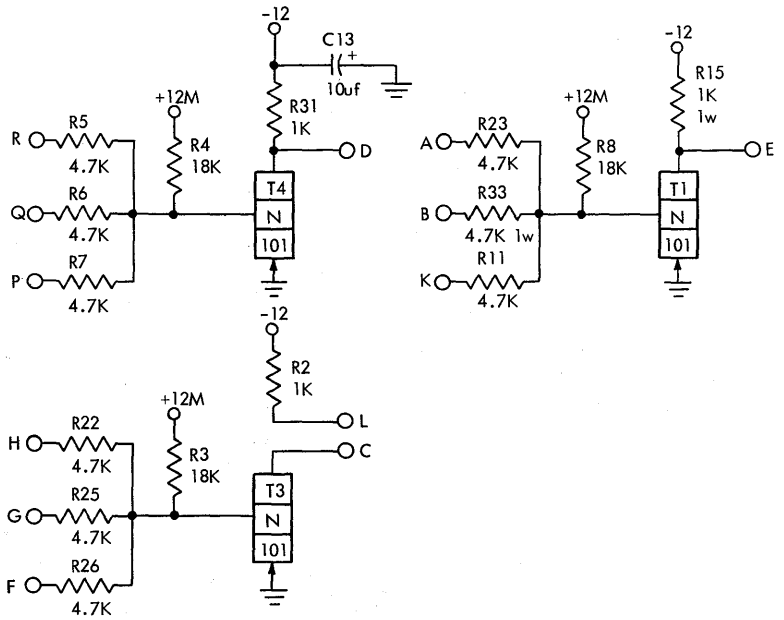
	Input Levels		Output Levels Out of Phase		ns Block Delays	
	Min	Max	Min	Max	Turn On	Turn Off
Min	-.6	-.05	-.45	-.05	43	128
Nom					84	191
Max	-6.87	-12.48	-6.87	-12.48	125	254

EC Level	11-29-61	112774

3-Way NOR Inverter (SDTRL)

TAH
370367





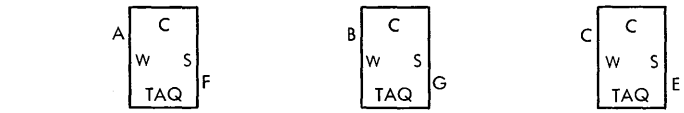
As an inverter, this block has a +S output level if any of its inputs is a -S level. When all three inputs are +S, the output is -S.

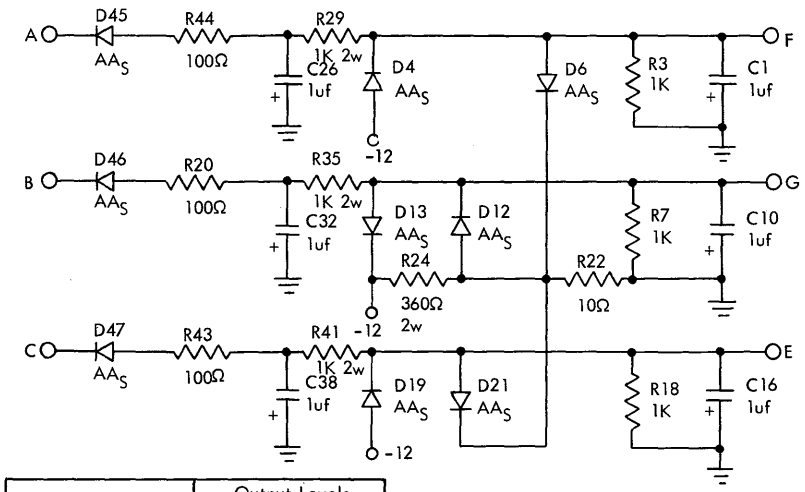
One of these three circuits has a disconnected load resistor for extender purposes or to allow driving special circuits

	Output Levels				ns Block Delays	
Input Levels		Out of Phase			Turn On	Turn Off
Min	Max	Min	Max	Min	43	128
-.6	-.05	-.45	-.05	Nom	84	191
-6.87	-12.48	-6.87	-12.48	Max	125	254
EC Level	11-29-61	112774				

Converter (W to S)

TAQ
370098



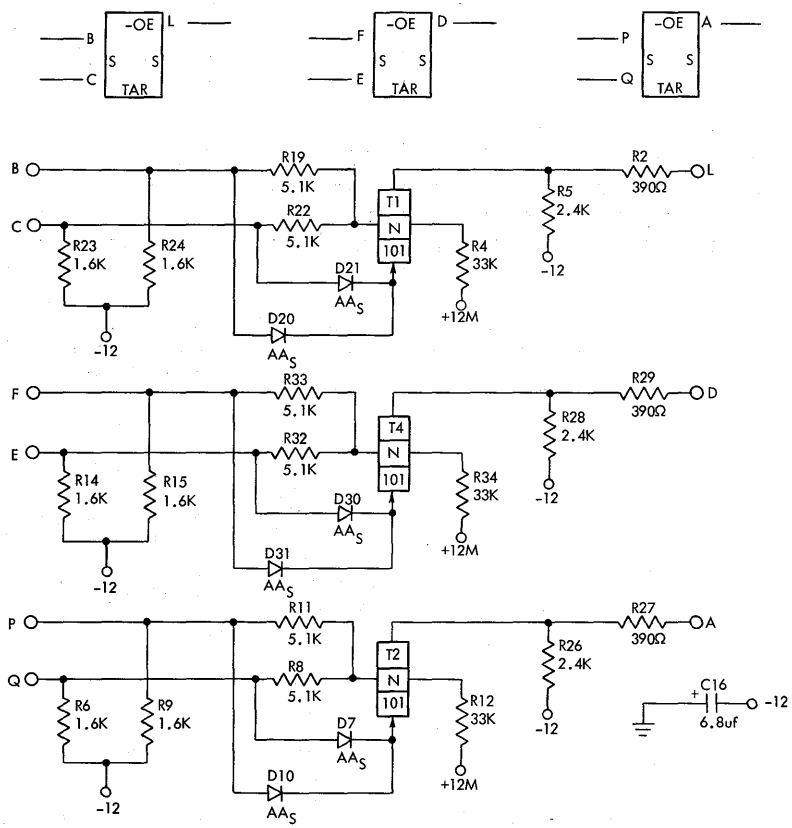


	Output Levels
Input Levels	Out of Phase
Nominal	Nominal
0	0
-36	-12
EC Level	6-16-60	109609

Note: Input level may be nominally -20, -36, or -48

2-Way Exclusive OR

TAR
370105

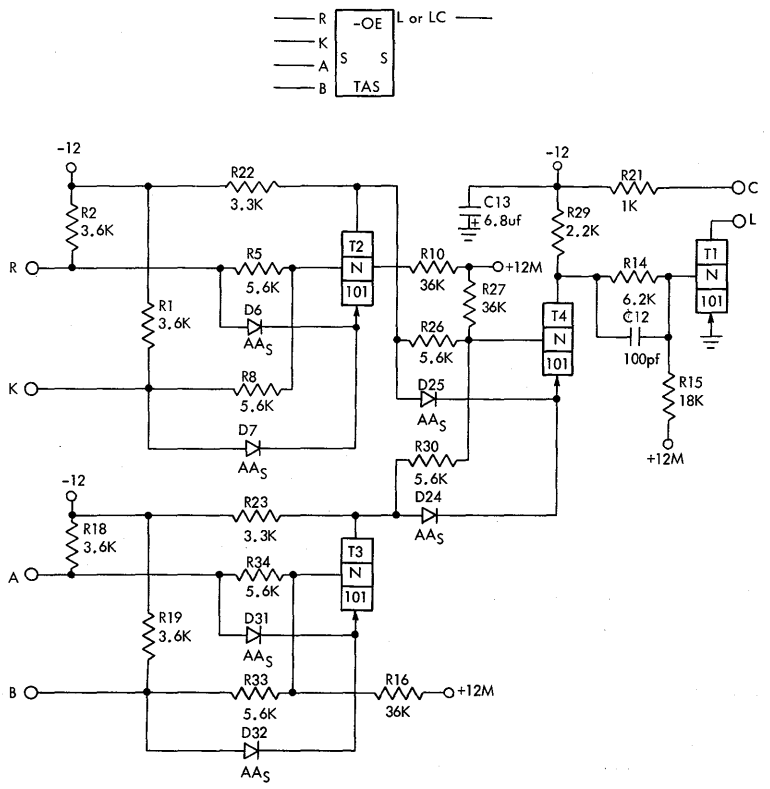


This circuit has a -S output level when both inputs are at a +S level or when both inputs are at a -S level. When one input is at +S and the other at -S, the output is at a +S level

Input Levels		Output Levels Out of Phase		ns Block Delays		
Min	Max	Min	Max		Turn On	Turn Off
-.45 / -6.87	-.05 / -12.48	-1.57 / -6.87	-.42 / -12.48	Min	65	135
				Nom	70	150
				Max	80	180
EC Level	5-25-61	112019				

4-Way Exclusive OR (Pyramid-SDTRL)

TAS
370106



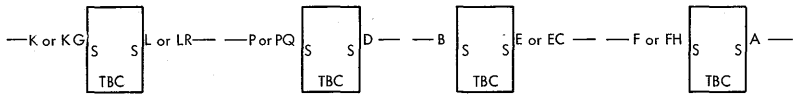
This circuit has a -S level output whenever one of its four inputs is different from the other three. The output collector resistor is left disconnected to allow driving other exclusive OR's or to use it in common collector configurations. This circuit can be pyramided with other 4-way exclusive OR's.
Note: Output levels are those obtained with the collector load resistor connected

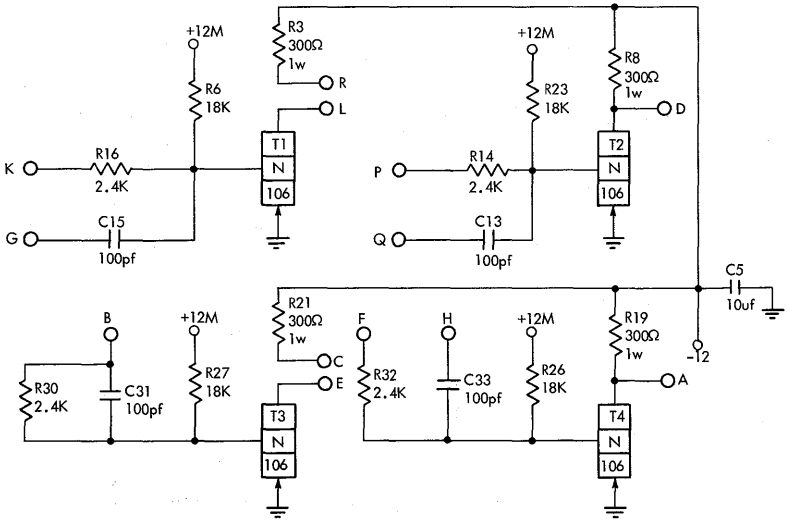
Input Levels		Output Levels Out of Phase		ns Block Delays			
Min	Max	Min	Max		Min	Nom	Max
-.45 / -6.87	-.05 / -12.48	-.45 / -6.85	-.05 / -12.48	Turn On: 3 Inputs at +S, 4th Input Switching from +S to -S	30	40	90
				3 Inputs at -S, 4th Input Switching from -S to +S	110	180	194
				Turn Off: 3 Inputs At +S, 4th Input Switching from -S to +S	60	75	85
				3 Inputs at -S, 4th Input Switching from +S to -S	160	180	246
EC Level	5-25-61	112019					

Power Inverter

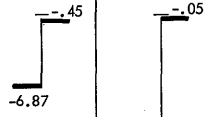
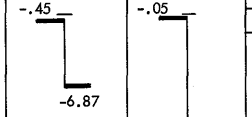
TBC

371815





This circuit is used to provide power for driving a number of logic blocks
Two of the circuits (pins L and E) have disconnected load resistors to enable using a common collector configuration or to drive special blocks
One circuit per card (E pin output) has a speed-up capacitor permanently wired in at the block input. The other three require back panel wiring to connect the capacitor
Min delays are input transition times. Max delays are input transitions plus worst case delays

	Output Levels		ns Block Delays		
Input Levels	Out of Phase			Turn On	Turn Off
Min / Max	Min	Max	Min	100	50
			Nom		
			Max	260	334

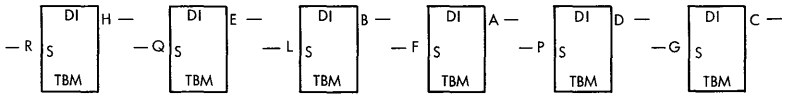
EC Level	8-1-61	112387

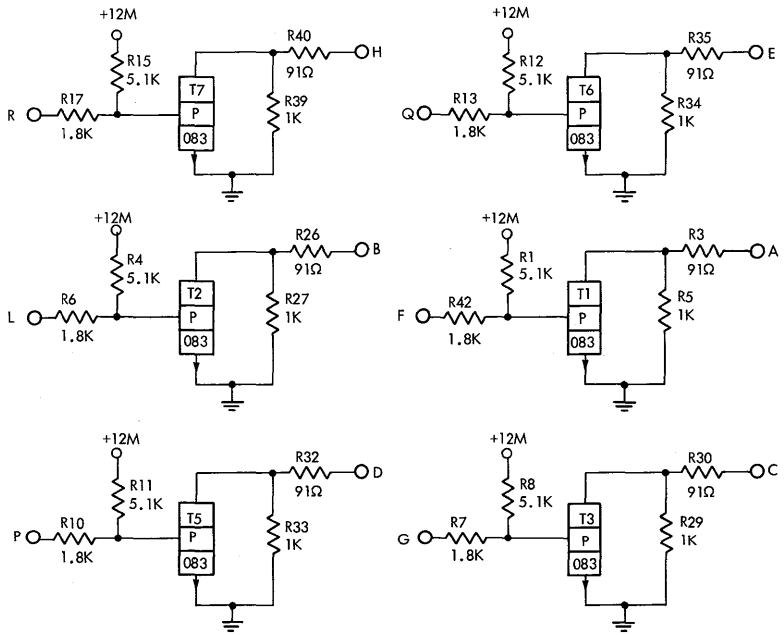
Appendix C 135

40-ma Light Driver

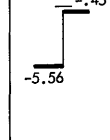
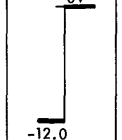
TBM

370300





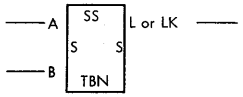
The light will be lit when the input is at +S and OFF when the input is -S. The rating of the lamps is 40 ma.
A pre-ignition current of 9-13 ma causes the light to glow faintly in the OFF condition

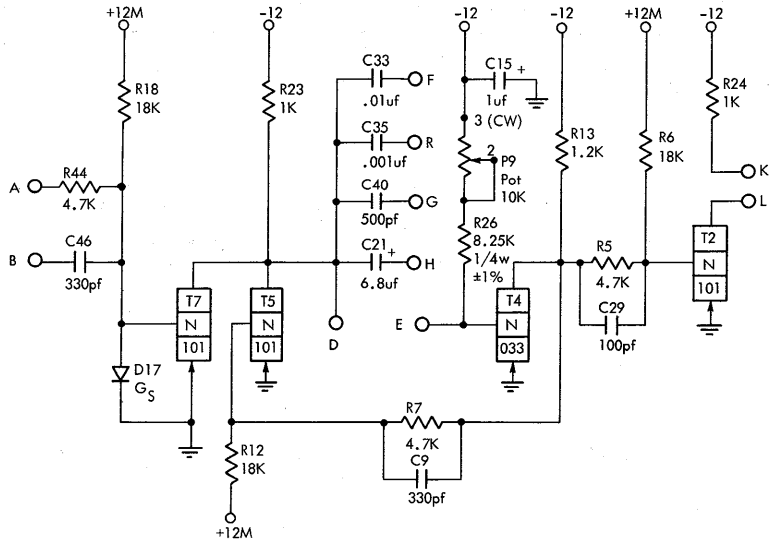
Input Levels	
Min	Max
	

EC Level	9-9-60	109914

Variable Single-Shot

TBN
370291





This single-shot produces a positive going timing pulse from a negative going input pulse. The output timing is independent of the trigger pulse duration and can be continuously adjusted from 3 usec to several seconds

Input Levels		Output Levels Out of Phase	
Min	Max	Min	Max
-.5 / -6.5	+.5 / -12.48	-.45 / -6.87	-.05 / -12.48

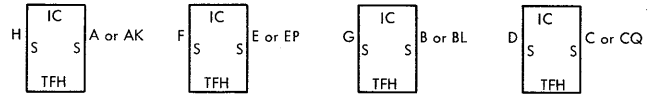
ns Block Delays Ton		
Input →	Pin B (Cap)	Pin A (Res)
Min	50	90
Nom	80	
Max	100	820

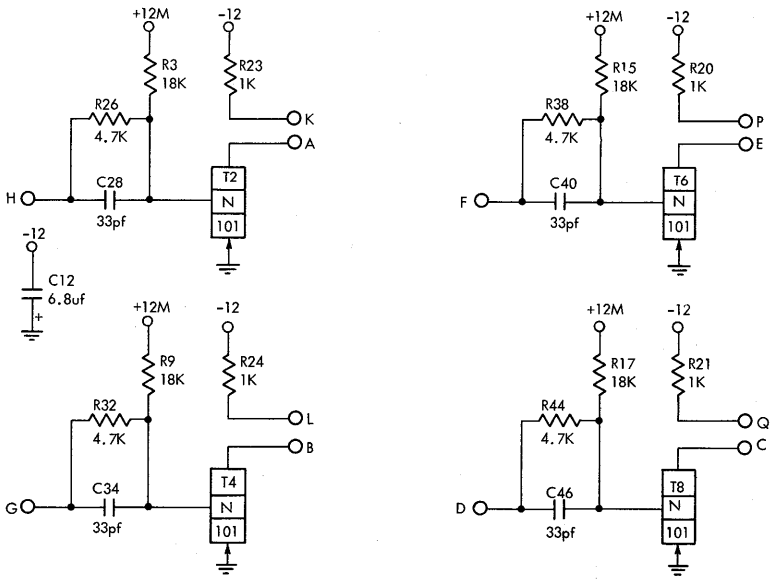
Output Timing - SS Card Only	
Connect Pin E to	Timing Range
G	3 to 5.5 usec
R	5.5 to 11 usec
G & R	9 to 16 usec
F	60 to 110 usec
H	43 to 78 ms

EC Level	5-25-61	112021

Compensated Inverter

TFH
370805





This circuit is a basic inverter with speed-up capabilities provided by the addition of a 33pf capacitor Each of the four circuits has a disconnected load resistor to enable extending or driving special circuits. Output levels are those obtained with the load resistors on the card connected

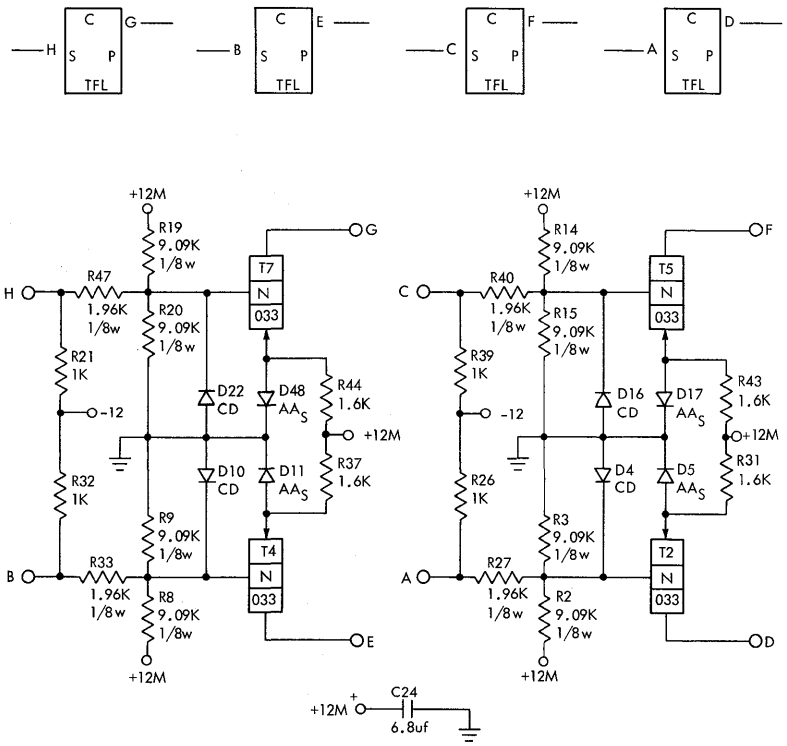
Input Levels		Output Levels Out of Phase	
Min	Max	Min	Max
-.45 / -6.12	-.05 / -12.48	-.45 / -6.87	-.05 / -12.48

ns Block Delays		
	Turn On	Turn Off
Min		
Nom		
Max		

EC Level	10-6-61	112724

Dot-OR Converter Driver (S to P)

TFL
370826

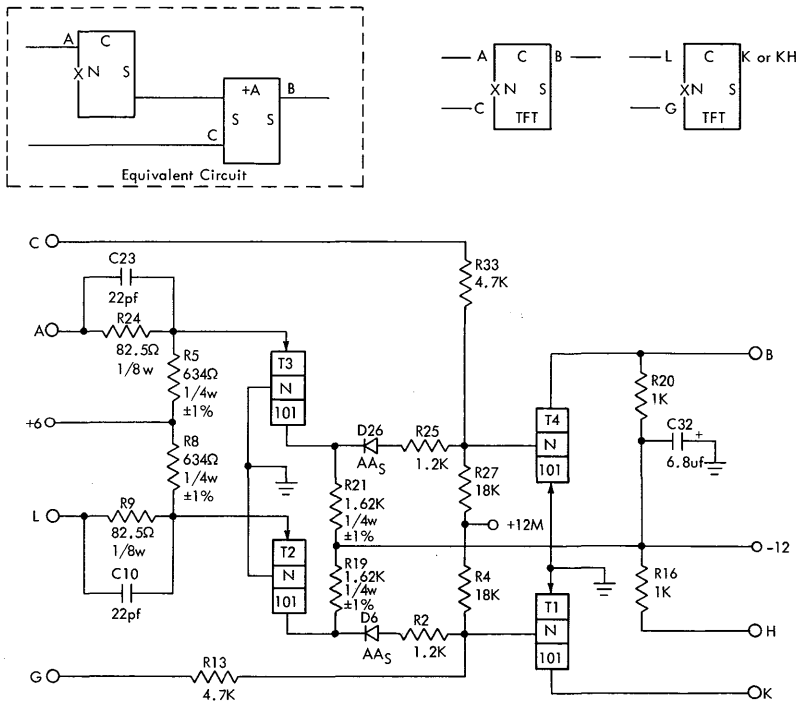


This circuit converts S-line signals to current pulses to be transmitted along a 93-ohm coaxial cable

Input Levels		Output Levels Out of Phase	ns Block Delays		
Min	Nominal	Nominal		Turn On	Turn Off
			Min	40	80
			Nom	85	105
			Max	130	130
EC Level	10-25-61	112753			

Converter-N to S

TFT
370516

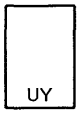


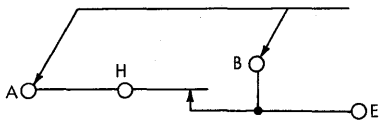
This circuit terminates a 93-ohm coaxial line and converts N-line signals to S levels
A gate input allows a 2-way NOR function to be accomplished if desired. Since the output is equivalent to that of a NOR block, one circuit is provided with a disconnected load resistor. This is back-panel wired if the outputs are not used in a common collector configuration

Input Levels		Output Levels Out of Phase		ns Block Delays		
Min	Max	Min	Max		Turn On	Turn Off
				Min	50	60
				Nom	68	66
				Max	72	72
EC Level	11-28-61	113101				

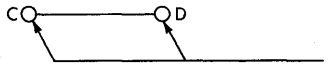
Thermal Switch

UY
371697





Pins A and B are not inputs or outputs. They insure positive indication when this card is accidently substituted for DCY-, UX-- and RE--



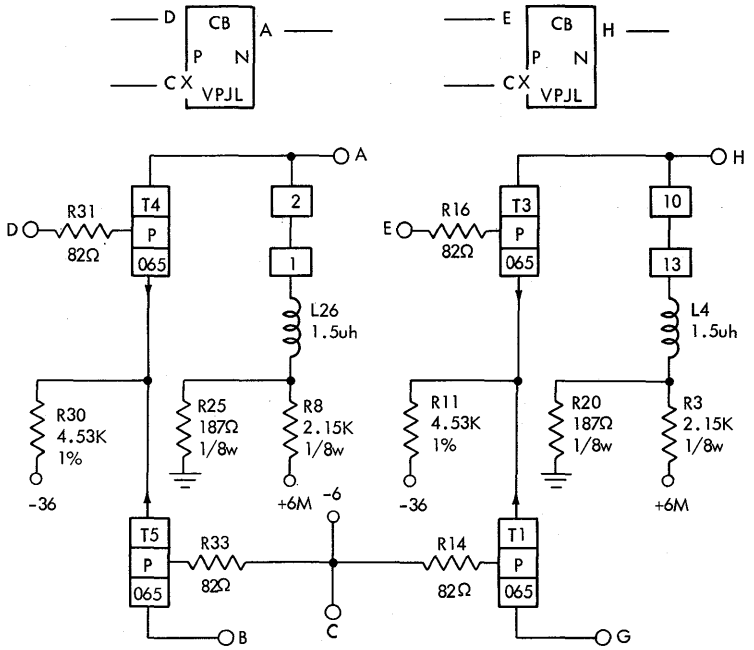
Pins C and D can be used to indicate that card is in position

Set to open at 107° F

EC Level	5-31-61	D111776

Differential Amplifier (P to N)

VPJL
370848



The differential amplifier is basically a 1-way logic block driven by a transmission line driver through a coaxial line. In addition, the amplifier is a terminator for the 93-ohm coaxial line.

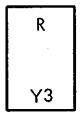
Note: The differential amplifier can be pulled out of a gate without causing any damage. But a differential amplifier terminator must not be removed with power on. Doing so can cause transistor failure on all the differential amplifiers on the same coaxial line. It can also cause failure of the electrolytic capacitor on the transmission line driver that is driving the coaxial line

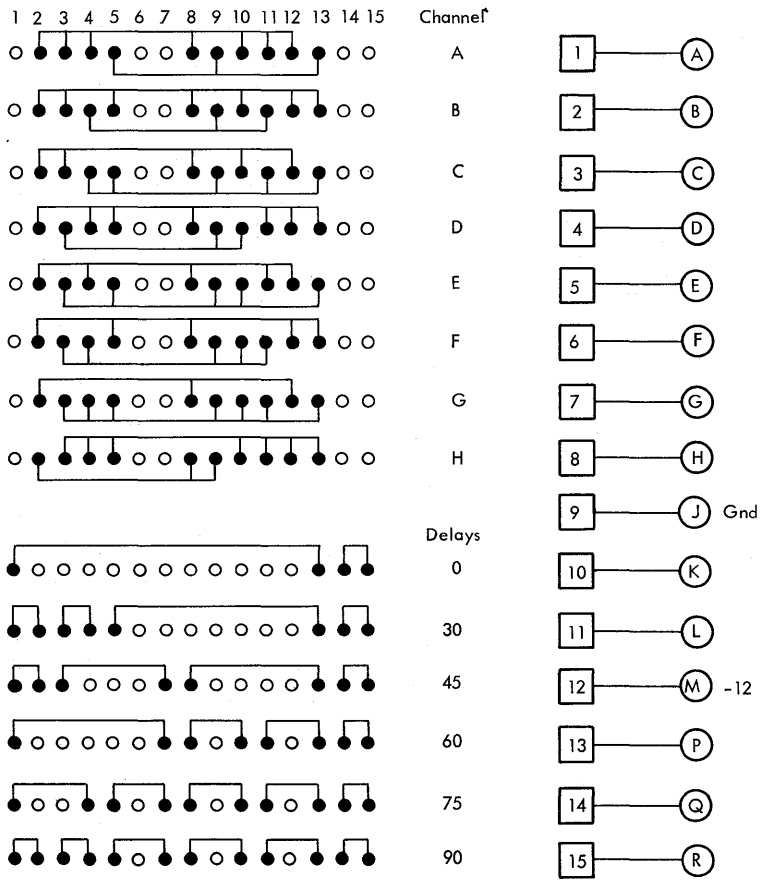
Input Levels		Output Levels Out of Phase		ns Block Delays		
Min	Max	Min	Max		Turn On	Turn Off
				Min	7	4
				Nom	14	13.5
				Max	21	23
— -5.6 -6.4	— -5.14 -6.56	+.4 -.4	+.51 -.81			
EC Level	12-7-61	113109				

Cap Cut Card

Y3

370858





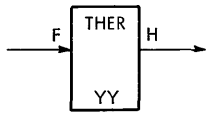
This card is used for channel assignment and demand delay single-shot timings

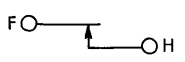
EC Level	11-29-61	113105

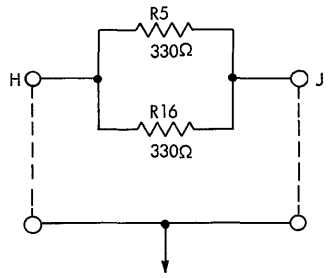
Air Flow Switch

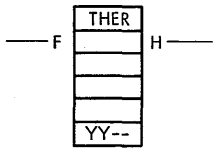
YY

371751









Set to open at 93° F

EC Level	1-9-61	D110956

Appendix D—Hypertape Reference Information

IBM 7640 Hypertape Control Orders

Alpha Code	Num Code	Binary Positions 2 3 4 5 8 9 10 11	Orders
HNOP	00	1 0 1 0 1 0 1 0	Hypertape No Operation
HEOS	01	1 0 1 0 0 0 0 1	Hypertape End of Sequence
HRLF	02	1 0 1 0 0 0 1 0	Hypertape Reserved Light Off
HRLN	03	1 0 1 0 0 0 1 1	Hypertape Reserved Light On
HCLN	05	1 0 1 0 0 1 0 1	Hypertape Check Light On
HSEL	06	1 0 1 0 0 1 1 0	Hypertape Select
HSBR	07	1 0 1 0 0 1 1 1	Hypertape Select for Backward Reading
HCCR	28	0 0 1 0 1 0 0 0	Hypertape Change Cartridge and Rewind
HRWD	30	0 0 1 1 1 0 1 0	Hypertape Rewind
HRUN	31	0 0 1 1 0 0 0 1	Hypertape Rewind and Unload Cartridge
HERG	32	0 0 1 1 0 0 1 0	Hypertape Erase Long Gap
HWTM	33	0 0 1 1 0 0 1 1	Hypertape Write Tape Mark
HBSR	34	0 0 1 1 0 1 0 0	Hypertape Backspace
HBSF	35	0 0 1 1 0 1 0 1	Hypertape Backspace File
HSKR	36	0 0 1 1 0 1 1 0	Hypertape Space
HSKF	37	0 0 1 1 0 1 1 1	Hypertape Space File
HCHC	38	0 0 1 1 1 0 0 0	Hypertape Change Cartridge
HUNL	39	0 0 1 1 1 0 0 1	Hypertape Unload Cartridge
HFPN	42	0 1 0 0 0 0 1 0	Hypertape File Protect On
HICE	43	0 1 0 0 0 0 1 1	Interrupt on Correctible Error
HECO	44	0 1 0 0 0 1 0 0	Error Correction Off
HFCB	45	0 1 0 0 0 1 0 1	Fix Check Bits
HWCF	46	0 1 0 0 0 1 1 0	Write Clock Fast
HWCS	47	0 1 0 0 0 1 1 1	Write Clock Slow
HLWR	49	0 1 0 0 1 0 0 1	Loop Write to Read

7640 Sense Status Data Bit Assignment

Byte	Bit	BCD Bit	Indication	Comment
1	3	A	Operator Required	Summary Bits Summary Bits
	5	4	Program Check	
	6	2	Data Check	
	7	1	Exceptional Condition	
2	3	A	B	Selected Tape Unit Address
	5	4	4	
	6	2	2	
	7	1	1	
3	3	A	Selected Drive not Ready	Operator Required
	5	4	Selected Drive not Loaded	
	6	2	Selected Drive File Protected	
	7	1	Operation not Initiated	
4	3	A	Invalid Order Operation Code	Program Check Check
	5	4	Selected Drive Busy	
	6	2	Selected Drive at BOT	
	7	1	Selected Drive at EOT	
5	3	A	Correction Occurred	Data Check
	5	4	Channel Parity Check	
	6	2	Code Check	
	7	1	Envelope Check	
6	3	A	Overrun Check	
	5	4	Excessive Skew Check	
	6	2	Track Start Check	
	7	1	Not Used	
7	3	A	Selected Drive Read a Tape Mark	Exceptional Condition
	5	4	Selected Drive in EWA	
	6	2	Not Used	
	7	1	Not Used	
8	3	A	Read Section Busy	
	5	4	Write Section Busy	
	6	2	Backward Mode	
	7	1	Not Used	
9	3	A	Drive 0	Attention
	5	4	Drive 1	
	6	2	Drive 2	
	7	1	Drive 3	
10	3	A	Drive 4	
	5	4	Drive 5	
	6	2	Drive 6	
	7	1	Drive 7	
11	3	A	Drive 8	
	5	4	Drive 9	
	6	2	Not Used	
	7	1	Not Used	
12		A	Not Used	Diagnostics
		4	Diagnostic Mode	
		2	Interrupt on Correctable Error	
		1	Error Correction Off	
13		A	Loop Write to Read	
		4	Write Clock Fast	
		2	Write Clock Slow	
		1	Fix Check Bits	
14			Not Used	

7640 CONDITIONS WHICH RESULT IN PROGRAM CHECK & OPERATOR REQUIRED

	KLN	RLN	RLF	SEL	BS	BSFL	SP	SPFL	ERG	SBR	FPN	WTM	CHCR	CHC	UNLC	RUNL	REW	ECF	LWR	ICE	WCF	WCS	READ	READ (BACKWARD)	WRITE
Operator Required																									
Not Ready	X	X	X		X	X	X	X	X		X	X	X	X	X	X	X						X	X	X
Program Check																									
Not Loaded					X	X	X	X	X		X	X					X						X	X	X
Busy	X	X	X		X	X	X	X	X		X	X	X	X	X	X	X						X	X	X
File Protected									X			X													X
Load Point					X	X																		X	
End Point							X	X	X			X											X		X
Not Loop Write to Read																					X	X			

Appendix E—7631 File Control Reference Information

IBM 7631 File Control Orders

Alpha Code	Num Code	Binary Positions 2	3	4	5	8	9	10	11	Orders
DNOP	00	1	0	1	0	1	0	1	0	Disk No Operation
DREL	04	1	0	1	0	0	1	0	0	Disk Release
DEBM	08	1	0	1	0	1	0	0	0	Disk Eight Bit Mode
DSBM	09	1	0	1	0	1	0	0	1	Disk Six Bit Mode
DSEK	80	1	0	0	0	1	0	1	0	Disk Seek
DVSR	82	1	0	0	0	0	0	1	0	Disk Prepare to Verify -- Single Record
DURF	83	1	0	0	0	0	0	1	1	Disk Prepare to Write Format
DVTN	84	1	0	0	0	0	1	0	0	Disk Prepare to Verify -- Track With No Addresses
DVCV	85	1	0	0	0	0	1	0	1	Disk Prepare to Verify -- Cylinder Operation
DWRC	86	1	0	0	0	0	1	1	0	Disk Prepare to Write Check
DSAI	87	1	0	0	0	0	1	1	1	Disk Set Access Inoperative
DVTA	88	1	0	0	0	1	0	0	0	Disk Prepare to Verify -- Track With Addresses
DVHA	89	1	0	0	0	1	0	0	1	Disk Prepare to Verify -- More Address

7631 Sense Status Data Bit Assignment

Bytes	Bits	BCD Bit	Indication	Comment
1	3	A	Reserved	
	5	4	Program Check	Summary Byte
	6	2	Data Check	Summary Byte
	7	1	Exceptional Condition	Summary Byte
2	3	A	Invalid Sequence	Program Check
	5	4	Invalid Code	Program Check
	6	2	Format Check	Program Check
	7	1	No Record Found	Program Check
3	3	A	Invalid Address	Program Check
	5	4	Response Check	Data Check
	6	2	Data Compare Check	Data Check
	7	1	Parity or Check Char Code Check	Data Check
4	3	A	Access Inoperative	Exceptional Cond
	5	4	Access Not Ready	Exceptional Cond
	6	2	Disk Storage Circuit Check	Exceptional Cond
	7	1	File Control Circuit Check	Exceptional Cond
5	3	A	Reserved	
	5	4	6-bit Mode	Data Check
	6	2	Reserved	
	7	1	Reserved	
6	3	A	Module 0	Attention
	5	4	Module 1	Attention
	6	2	Module 2	Attention
	7	1	Module 3	Attention
7	3	A	Module 4	Attention
	5	4	Module 5	Attention
	6	2	Module 6	Attention
	7	1	Module 7	Attention
8	3	A	Module 8	Attention
	5	4	Module 9	Attention
	6	2	Reserved	
	7	1	Reserved	
9&10			Reserved	

Appendix F—1414-6 Reference Information

1416-6 Address and Buffer Assignments

Adapter	Operation	Adapter Address (decimal)	Buffers Required
Telegraph	Read Write	10, 11, 12 14, 15, 16	2, 3, or 4 2, 3, or 4
IBM 1009	Read Write	20 24	2 2
IBM 1014	Read Write	60, 61 64, 65	2 or 4
IBM 1011	Read	70	1

Any combination of the above adapters may be attached to the 1414-6 if the combined buffer requirements do not exceed six.

1414-6 Sense Status Data Bit Assignment

Byte	Bits	BCD Bits	Identification	Comment
1	3	A	Not Used	
	5	4	Program Check *	Summary Byte
	6	2	Data Check **	Summary Byte
	7	1	Exceptional Condition	Summary Byte
2	3	A	Not Ready ***	Exceptional Cond
	5	4	Busy ***	Exceptional Cond
	6	2	Condition ***	Exceptional Cond
	7	1	No Transfer ***	Exceptional Cond
3	3	A	Not used	
	5	4	Tens Digit	Address
	6	2	Tens Digit	Address
	7	1	Tens Digit	Address
4	3	A	Not used	
	5	4	Units Digit	Address
	6	2	Units Digit	Address
	7	1	Units Digit	Address

* A Program Check is caused by selecting a write adapter followed by a read instruction or vice versa, or giving a sense command and not preceded by: (1) a control command, or (2) either an unusual end or attention signal from the 1414-6.

** A Data check is caused by either: (1) a character parity check in the 1414-6, or (2) a 1414-6 machine check.

*** See Status Byte 2 Detail Information Chart.

Adapter Number	Device	Status Data Information			
		A Bit (Not Ready)	4 Bit (Busy)	2 Bit (Condition)	1 Bit (No Transfer)
1	Telegraph Read	Buffer not on line or power off	Buffer is being filled	Missed message	No request
	Telegraph Write	Buffer not on line or power off	Buffer is being filled	Last message in error; not transmitted to remote telegraph *	Last message transmitted but received incorrectly.
2	IBM 1009 DTU Read	DTU not on line or power off	Buffer is being filled	Missed message	No request
	IBM 1009 DTU Write	DTU not on line or power off	Buffer is being filled	Last message in error; transmitted to local 1009, but not to remote 1009	Last message transmitted but received incorrectly.
6	IBM 1014 Read	Buffer not on line or power off	Not Applicable	Not Applicable	No request or Buffer being filled
	IBM 1014 Write	Buffer not on line or power off	Buffer being emptied	Last message in error; not transmitted	Last message not transmitted; station inoperative.
7	IBM 1011 Read	Paper tape power off or out of tape	Buffer being filled	Not applicable	Not applicable

* May be transmitted to local telegraph

CUT ALONG LINE

COMMENT SHEET

IBM 7909 DATA CHANNEL

CUSTOMER ENGINEERING INSTRUCTION-REFERENCE, FORM 223-2551

FROM

NAME _____

OFFICE NO. _____

FOLD FOLD

CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

☐ SUGGESTED ADDITION (PAGE , TIMING CHART, DRAWING, PROCEDURE, ETC.)

☐ SUGGESTED DELETION (PAGE)

☐ ERROR (PAGE)

EXPLANATION

FOLD FOLD

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES, STAPLE, AND MAIL

FOLD

FOLD

FIRST CLASS
PERMIT NO. 81

POUGHKEEPSIE, N. Y.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

POSTAGE WILL BE PAID BY

IBM CORPORATION
P.O. BOX 390
POUGHKEEPSIE, N.Y. 12602

ATTN: CE MANUALS, DEPARTMENT B96

CUT ALONG LINE

FOLD

FOLD

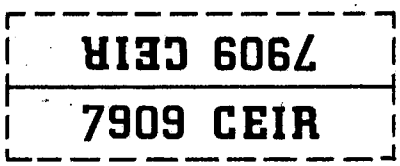
12/63:1500-VO

STAPLE

STAPLE

CUT ALONG DOTTED LINE

FOLD



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