IBM Customer Engineering

Manual of Instruction

7607 Data Channel

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1.0.00 INTRODUCTION

GENERALLY speaking, most large scale computers are much faster than their associated input/output equipment. Where this condition exists, there is a need for synchronization between the computer and input/output devices. This is the case of the IBM 7090 Data Processing System.

To meet this need for synchronization, the 7090 incorporates the IBM Data Channel. The data channel accomplishes the synchronization by acting as a buffer between the computer's internal storage and the input/output equipment.

1.1.00 READING

The process of bringing a word from an input device to the computer's internal storage is defined as reading. During the reading operation, a word is transmitted from the selected input device to the data channel. The data channel performs a buffering action by holding the word until the computer's internal storage is able to accept it. It is important to note that the word being held by the data channel must be accepted by the computer's internal storage before the data channel receives another word from the selected input device.

1.2.00 WRITING

Writing is the process of taking a word from the computer's internal storage to a selected output device. While writing, the buffering action is accomplished by holding a word transmitted from the computer's internal storage in the data channel. The word is held in the data channel until the selected output device signals it is ready to accept it. Once the selected output device accepts the word, the data channel is able to accept another word from the computer's internal storage. The data channel must receive the word prior to the next signal from the selected output device.

1.3.00 USE WITH THE 7090

There is a possibility of having up to eight data channels on the 7090. Each data channel incorporates circuitry to make it independent of other data channels on the system. This design allows reading and writing simultaneously if a 7090 has two or more data channels.

Functioning as a buffer, the data channel gives the 7090 the unique capability of being able to transmit a word to or from the computer's internal storage with a minimum delay in a CPU program. It takes one core storage cycle to transmit a word to or from the computer's internal storage and data channel. If the CPU is not using core storage at the time a word is being transmitted, the CPU program is not interrupted. The possibility exists that a CPU program and eight prestored input/output programs might be operating simultaneously. The eight prestored input/output programs may be intermixed read and write operations.

To sum up, the primary function of the data channel is to synchronize input/output devices with the computer's internal storage by means of buffering. The design of the

data channel plays a major role in allowing the 7090 to operate on up to nine programs simultaneously. Listed below are five advantages of the data channel:

1. Up to eight data channels on a 7090
2. Automatic priority processing using data channel trap, Section 5.0.00
3. Compute simultaneously with multiple input/output operations under automatic control
4. Use of indirect addressing with input/output commands
5. Compatibility with all IBM data processing systems

2.0.00 INTERNAL AND EXTERNAL FUNCTIONS

2.1.00 REGISTERS

The data channel incorporates six registers in order to perform its function as a buffer. They are the data register, word counter, channel address counter, operation register, location counter, and tape register.

2.01.01 Data Register (DR)

The data register is a 36-position trigger register. A better name for this register might possibly be "buffer register," as it is the data register that acts as the buffer between the computer's internal storage and input/output equipment.

Data Register Inputs

As can be seen from Figure 2.1-1, the data register has three inputs: the channel input switches, tape register, and calculator entry, all with positions S, 1-35.

Channel Input Switches. The channel input switches are gated to the data register when the system is writing on the printer, writing to the punch, writing on tape, reading from the printer(printing with echo-checking), and loading the data register from entry keys (manual operation).

Tape Register. The tape register is gated to the data register when the data channel is reading from tape.

Calculator Entry is gated to the data register when the system is reading cards or reading from the printer (echos).

Data Register Outputs

Figure 2.1-1 also shows the data register's three outputs. They are the channel storage bus switches, the tape register, and the calculator exit, all with positions S, 1-35.

Channel Storage Bus Switches. The data register is gated through the channel storage bus switches S, 1-35 when it is reading from cards, reading from the printer (printing with echo-checking), reading from tape, or storing from the data channel (manual operation).

Tape Register. The data register is gated to the tape register when writing on tape.

Calculator Exit. The data register is gated to the calculator exit when it is writing on the printer, writing on the punch, or reading from the printer (echo-checking).

2.1.02 Word Counter (WC)

The word counter is a 15-position trigger register. The word counter is wired as a binary count-down counter. Like the shift counter in the CPU, its function is that of

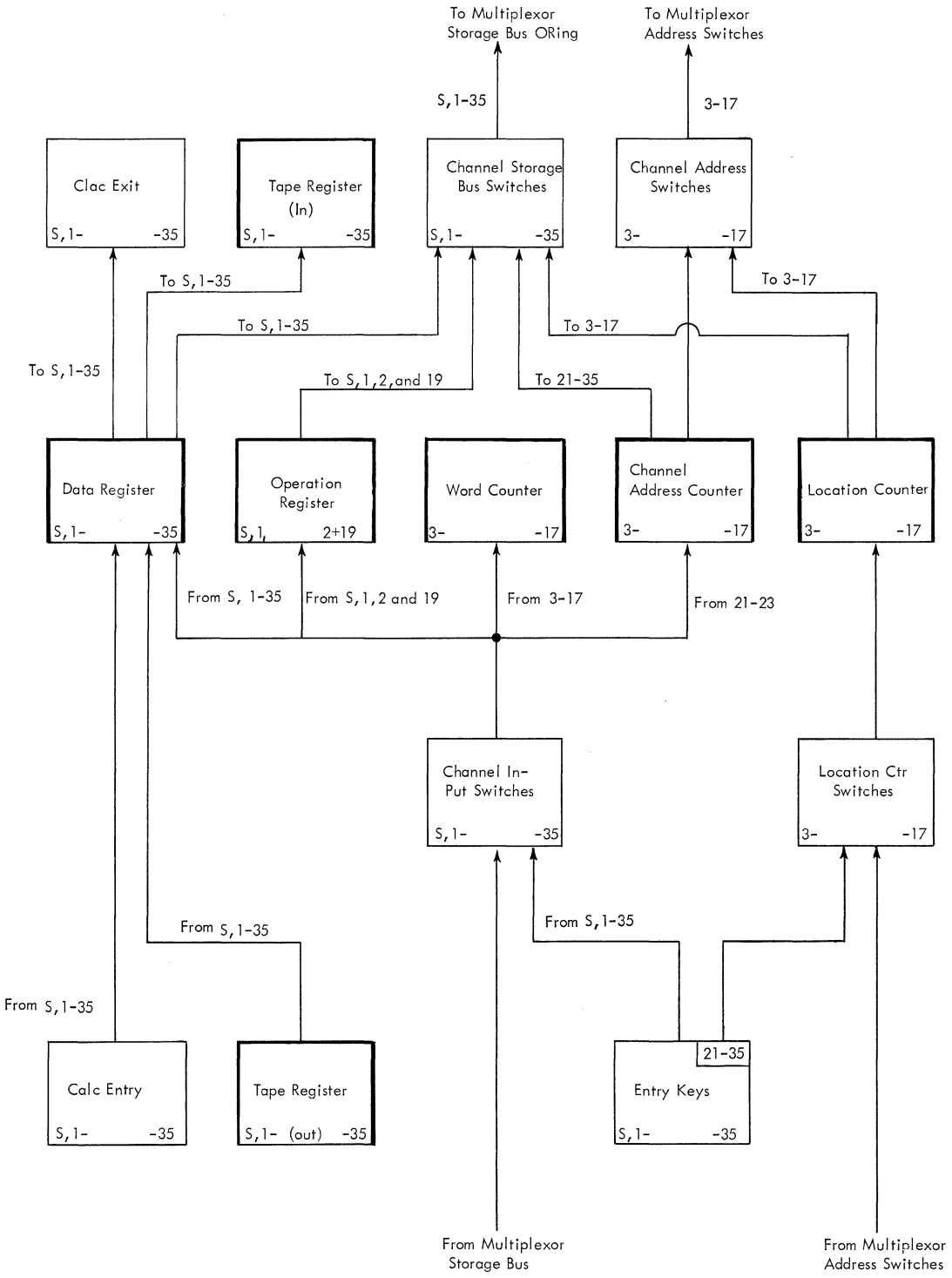

FIGURE 2.1-1. DATA FLOW

control. The word counter contains the number of words to be transmitted to or from the data channel. After each word is transmitted, the word count is reduced by one.

The word counter is loaded with a number gated through channel input switches 3-17 during the following four operations (Figure 2.1-2):

Reset and load channel instruction
Load channel instruction
"BCW" cycle (not IA "BCW" cycle)
Loading a command from the entry keys (manual operation)

2.1.03 Channel Address Counter (CAC)

The channel address counter is a 15-position trigger register. This counter is wired to count up. The contents of the channel address counter specify which address in core storage is used. The contents of the counter are increased by one after each transfer of data. Notice that data are taken to or from sequential addresses in core storage.

Channel input switches 21-35 are the only inputs to the channel address counter. These switches are gated to the channel address counter during the following operations (Figure 2.1-2):

Reset and load channel instruction
Load channel instruction
"BCW" cycles
Loading a command from the entry keys (manual operation)

The channel address counter has two outputs. They are the channel storage bus switches 21-35 and the channel address switches 3-17.

During "BDW" cycles, channel address counter 3-17 is gated through channel address switches 3-17. During the E cycle of a store channel instruction, channel address counter 3-17 is gated through channel storage bus switches 21-35.

2.1.04 Operation Register

There are four operation register triggers located in the data channel. The operation register controls what operation is to be performed by the data channel in regard to data transmission. The various combinations of triggers in the operation register form commands.

The four operation register triggers and their control follows:

Operation Register Position	Control
Sign (S)	Data transmission under count control
One (1)	Data transmission under record control
Two (2)	Data transmission under transfer control
Nineteen (19)	Data transmission inhibited under read control

Channel input switches S, 1, 2, and 19 are gated to operation register positions S, 1, 2, and 19 during the following four operations (See Figure 2.1-2.):

Reset and load channel instruction
Load channel instruction
"BCW" cycle (not IA "BCW" cycle)
Loading a command from the entry keys (manual operation)

The operation register is gated through channel storage bus switches S, 1, 2, and 19 during the E cycle of a store channel instruction.

Operation Register 18

There is a fifth operation register trigger located in the multiplexor. Its function of control is common to all data channels, but when it is active, it only affects that data channel specified. This trigger controls indirect addressing of commands.

2.1.05 Location Counter

The location counter is a 15-position binary count-up counter. The location counter contains the location +1, from which the last command has been taken. The location counter also specifies from what address in core storage the next command is to be taken, except in the case of transfer type commands or a reset and load channel instruction.

Location counter switches 3-17 are gated to the location counter during the following four operations (Figure 2.1-3):

Reset and load channel instruction
Load channel instruction
"BCW" cycle of a transfer in channel command
Loading the location counter from the entry keys (manual operation)

The location counter is gated through channel address switches 3-17 during "BCW" cycles that are initiated by "proceed type commands." During the E cycle of a store channel instruction, the location counter is gated through channel storage bus switches 3-17.

2.1.06 Tape Register

The tape register is a 36-position trigger register associated with the tape adapter unit (TAU).

When writing tape, the data register is gated to the tape register.

The tape register is gated to the data register when reading tape.

2.1.07 Calculator Entry and Exit

Calculator entry and exit are discussed in the Card Adapter Unit (CAU) Customer Engineering Manual of Instruction, Form 223-6842.

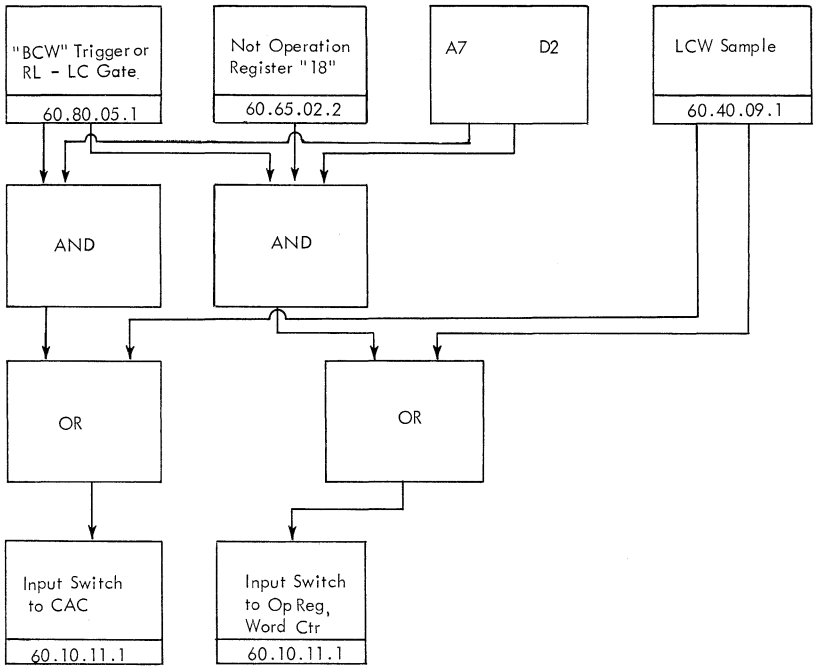

FIGURE 2.1-2 INPUT SWITCHES TO OPERATION REGISTER, WORD COUNTER AND CHANNEL ADDRESS COUNTER

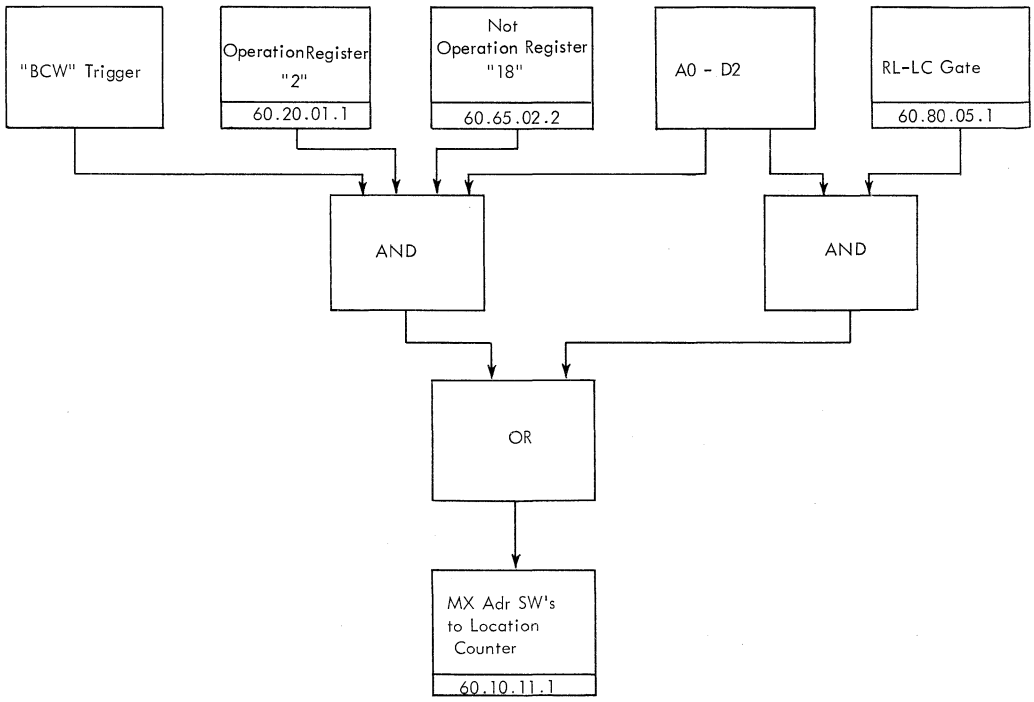

FIGURE 2.1-3. MULTIPLEXOR ADDRESS SWITCHES TO LOCATION COUNTER

2.2.00 COMMANDS

There are eight basic commands associated with the data channel. These commands are formed by the various settings of the four operation register triggers. The four operation register positions and their control follows:

Operation Register Position	Control
Sign (S)	Data transmission under count control
One (1)	Data transmission under record control
Two (2)	Data transmission under transfer control
Nineteen (19)	Data transmission inhibited under read control

2.2.01 Format

The format of a command is as shown.

Positions S, 1, 2, and 19 form the operation register field. Position 18 of the command is reserved for indirect addressing of commands. However, position 18 is located in the multiplexor.

Positions 3-17 of the command form the word count field. When a command is brought to the data channel, the word count field is gated to the word counter.

Positions 21-35 of the command form the address field. The address field of the command is gated to the channel address counter when a command is brought to the data channel.

2.2.02 Input/Output Count and Disconnect (IOCD)

Operation Register Position	Setting
Sign (S)	Off
One (1)	Off
Two (2)	Off
Nineteen (19)	Off

The IOCD command is input or output under control of the word count. When the word count is reduced to 0, the selected input or output device is disconnected. When writing tape, an end of record gap is written as the output device is disconnecting.

When reading, this command ignores end of records sensed by the input devices until the word count is reduced to 0. When the word count is reduced to 0, the input device is disconnected and positions itself to the beginning of the next record.

2.2.03 Input/Output Count and Proceed (IOCP)

Operation Register Position	Setting
Sign (S)	On
One (1)	Off
Two (2)	Off
Nineteen (19)	Off

The IOCP command is input or output under control of "word count and proceed." When the word count is reduced to 0, the data channel proceeds with the next sequential command in core storage automatically. The address of the next sequential command is specified by the data channel's location counter. The location counter is increased by one each time a new command is brought to the data channel. It is important to note that the proceed type command allows continuous data transmission without assistance from the CPU program.

2.2.04 Input/Output Record and Proceed (IORP)

Operation Register Position	Setting
Sign (S)	Off
One (1)	On
Two (2)	Off
Nineteen (19)	Off

The IORP command is input or output under record control and proceed to the next sequential command. Data transmission continues until the word count is reduced to 0, or an end-of-record is sensed at the selected input/output device. When the end-of-record is sensed, a new command is loaded in the data channel. The address of the new command, as with the IOCP command, is specified by the contents of the location counter. The IORP command allows reading or writing multiple records with one selection of an input/output device.

2.2.05 Input/Output Count and Transfer (IOCT)

Operation Register Position	Setting
Sign (S)	On
One (1)	Off
Two (2)	On
Nineteen (19)	Off

The IOCT command is input or output under control of the word count and then transfer control to the CPU program. Data transmission continues until the word count reaches 0. At this point, the data channel transfers control to the CPU program. A load channel instruction must be waiting in L time. The load channel instruction brings a new command to the data channel and the address from which the new command is taken is set to the location counter.

2.2.06 Input/Output Record and Transfer (IORT)

Operation Register Position	Setting
Sign (S)	Off
One (1)	On
Two (2)	On
Nineteen (19)	Off

The IORT command is input or output under record control and then transfer control to the CPU program. Data transmission continues until the word count is reduced to

0 or an end of record is sensed at the selected input/output device. When the end-of-record is sensed, control is transferred to the CPU program. A load channel instruction must be waiting in L time. The load channel instruction brings a new command to the data channel. The address from which the new command is taken is set to the location counter.

2.2.07 Input/Output Signal and Proceed (IOSP)

Operation Register Position	Setting
Sign (S)	On
One (1)	On
Two (2)	Off
Nineteen (19)	Off

The IOSP command is input or output under signal control (word count or end of record) and then proceed to the next sequential command. Data transmission continues until the word count is reduced to 0 or and end of record is sensed at the selected input device. When the word count is reduced to 0 or an end of record is sensed, a new command is brought to the data channel. The address of the new command is specified by the contents of the location counter.

During write operations, end of records sensed by a selected output device are ignored while using the IOSP command. Operation register position 1 is effectively ignored. Therefore, the data channel proceeds to the next sequential command only when the word count is reduced to 0.

2.2.08 Input/Output Signal and Transfer (IOST)

Operation Register Position	Setting
Sign (S)	On
One (1)	On
Two (2)	On
Nineteen (19)	Off

The IOST command is input or output under signal control (word count or end-of-record) and then transfer control to the CPU program. Data transmission continues until the word count is reduced to 0 or an end of record is sensed at the selected input device. When either of these conditions are met, control is transferred to the CPU program. A load channel instruction must be waiting in L time. The load channel instruction brings a new command to the data channel. The address from which the new command is taken is set to the location counter.

As it is with the IOSP command, operation register position 1 is effectively ignored during write operations that use the IOST command. When the data channel is writing, control is only transferred to the CPU program after the word count is reduced to 0.

2.2.09 Transfer in Channel (TCH)

Operation Register Position	Setting
Sign (S)	Off
One (1)	Off
Two (2)	On
Nineteen (19)	Off

The TCH command is a means of transferring from a sequential block of commands to another sequential block of commands. The TCH command is not seen at the data channel; the command is decoded and executed in the multiplexor.

When a new command is called for by the data channel, its route is from the core storage, to the multiplexor, and then to the data channel. If the new command is a TCH, it is decoded at the multiplexor. The decoding calls for a new command from an address specified by the address field of the TCH command.

The address field is gated to the data channel's location counter and the new command is brought to the data channel.

From the standpoint of a customer engineer, it is important to note that the TCH command takes one core storage cycle for decoding and another core storage cycle to bring out the new command. It is during the second core storage cycle that the address field is gated to the location counter and the new command is loaded in the data channel.

2.2.10 Operation Register Position 19

Operation register position 19, when used with data transmission commands (IOCD, IOCP, IORP, IOCT, IORT, IOSP or IOST), is a means of skipping over a designated number of words or a record when reading. The data channel receives data from the selected input device under control of the present command. With operation register 19 on, data are not transmitted to core storage. Operation register position 19 is only effective while reading. Actually, operation register position 19 does nothing more than inhibit data transmission to core storage when reading. The seven data transmission commands are designated with the following mnemonic codes if operation register position 19 is to be effective:

Normal Command	Operation Register Position 19 On
IOCD	IOCDN
IOCP	IOCPN
IORP	IORPN
IOCT	IOCTN
IORT	IORTN
IOSP	IOSPN
IOST	IOSTN

2.2.11 Operation Register Position 18

Operation register position 18, as stated previously, controls indirect addressing of commands. Like the TCH command, it is decoded and executed in the multiplexor.

When a new command calling for indirect addressing is brought to the multiplexor, operation register 18 is turned on. The command is loaded in the data channel, but the indirectly addressed command calls for another core storage cycle. It is during this core storage cycle that the indirect addressing takes place. Logically, the address field of the command loaded in the data channel during the previous core storage cycle is going to be changed. The address field of this command looks up a new word which, in turn, is brought to the multiplexor. It is the address field of this new word that replaces the original address field. The operation register and word count of the original command are not affected. This cycle is defined as an IA "BCW" cycle.

2.2.12 Count Control During Reading

During a read operation, a command may be skipped when using the following commands: IOCP, IOSP, IOCT, or IOST.

This possibility exists only when reading a record whose length is exactly equal to that of the word count. Under these conditions, when the word count goes to 0, a new command is loaded into the data channel. This command is skipped if these two conditions are met: The new command is loaded into the data channel prior to the time that the end of record is sensed at the selected input/output device (output device only if reading from the printer) and the new command is IORP, IOSP, IORT, or IOST. Notice that all have operation register position 1 on (record control).

It is important to note that the transfer commands are dependent on a load channel instruction waiting in L time. For what happens if load channel is not waiting in L time, see Section 2.3.03, Load Channel.

2.2.13 Count Control During Writing

When writing printer or punch, the possibility exists that a command may be skipped when using the IOCP, IOSP, IOCT, or IOST commands.

This possibility exists only when writing printer or punch with a word count of 30 octal. Under these conditions, a new command is loaded into the data channel after the word count is reduced to 0. This new command is skipped if the two following conditions are met: The new command is loaded into the data channel prior to the time that the end of the record is sensed at the selected output device and the new command is either IORP or IORT. These two commands are record control commands (operation register position 1). Notice that the signal type commands are not skipped when writing (record control not active with signal type commands).

2.3.00 SELECTION

With the possibility of having up to eight data channels on a 7090, there must be a way of making various operations unique to one data channel. The process of making a particular operation unique to a data channel is accomplished by decoding a channel address at the CPU. In some cases, the channel address is decoded by the operation code of the instruction associated with the data channel. On read and write operations, the channel address is determined by the address field of the individual instruction. By definition, read and write operations the data-select data channel (data transmission

occurs). Instructions that control operations performed by the input/output equipment, but do not involve data transmission, are defined as non-data selects. The address field of the non-data selects also decodes the channel address.

Data-selects are write-select channel A-H and read-select channel A-H.

Non-data selects are backspace record, backspace file, write end-of-file, and rewind.

There are several instructions that also must be unique to a data channel. These instructions control data transmission, monitor the progress of input/output operations, or test conditions met by the input/output equipment. These instructions are:

1. Reset and load channel
2. Load channel
3. Store channel
4. Transfer on channel in operation
5. Transfer on channel not in operation
6. Transfer on redundancy check
7. Transfer on end-of-file
8. Beginning-of-tape test
9. End-of-tape test
10. Sense type instructions
11. Input/output check test

2.3.01 Data Selection (Figure 2.3-1)

A data channel is data-selected if a read or write instruction can end operation. The four conditions governing the end operation are the secondary operation read/write, channel address, not data-selected, and not channel interlock.

Secondary Operation Read or Write

The secondary operation of a read or write select instruction is decoded at the CPU and cabled to all channels on the system.

Channel Address

The channel address (A-H) is decoded from the address field of the read or write select instruction. It is cabled to the individual data channel.

Not Data Selected

The data channel can not be data-selected if it is already data-selected. If this is the case, the read or write select instruction waits in L time until the data channel is data-disconnected.

Channel Interlock

The data channel cannot be data-selected if the channel is interlocked. The channel is interlocked if any of the four following conditions exist (See Figure 2.3-2.):

Card machine selected
Unit selected

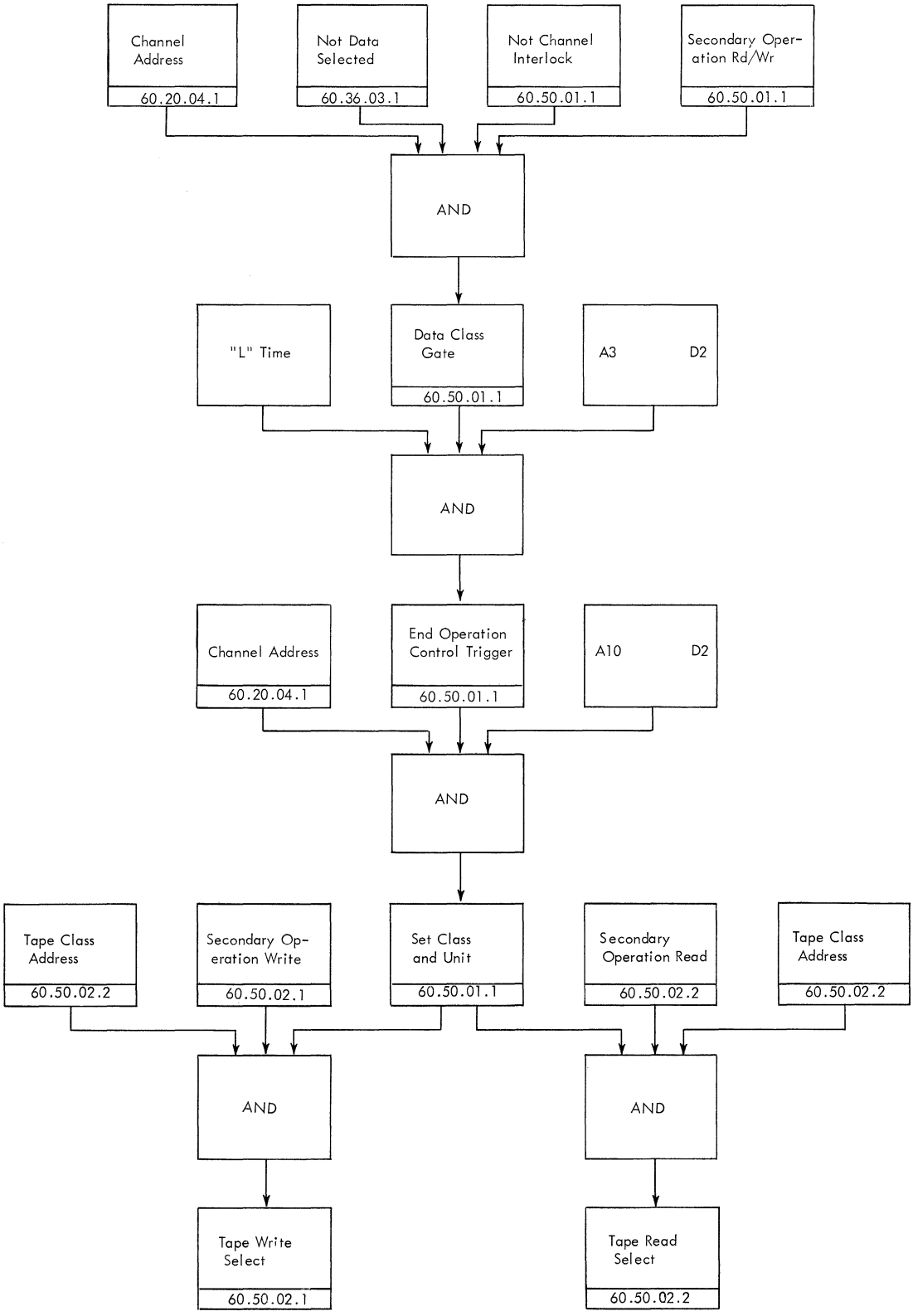

FIGURE 2.3-1. DATA SELECT END OPERATION AND TAPE DATA SELECTION

Write end-of-file select
Manual operation

The channel interlock is concerned mostly with non-data select instructions. However, the channel interlock prevents data-select instructions from ending operation.

Class and Unit Selection

The data channel may be data-selected if: it is not already data-selected, it is not non-data selected, or it is not in manual status.

When the end operation trigger is turned on, a "set class and unit" address gate is developed. See Figure 2.3-1. "Set class and unit" sets the class and unit triggers in the data channel or card adapter unit. Class and unit triggers to be set are determined by decoding the address field of the data-select instruction. In the case of card machines, the decoded class and unit address is cabled to the card adapter units by way of the data channels on the 7090. The tape class and unit address is cabled to the data channel and sets the specified triggers. (See Figure 2.3-1.) The binary coded decimal (BCD) mode trigger is also set if specified by the address field of the data-select instruction. One of ten unit select triggers is set. The unit select trigger specifies which of ten logical magnetic tape units are to be used (See Figure 2.3-3.) The unit select triggers are also set by sense type instructions associated with card machines. As can be seen from Figure 2.3-4, once one of the data select triggers is set, the channel is data-selected. The data select trigger remains set until the data channel is data-disconnected. However, the unit select trigger is turned off once it is received by TAU or CAU (allowing a non-data select instruction to follow). A "channel in use" line is cabled to the CPU for use with the transfer-on-channel in operation and transfer-on-channel not in operation instructions (Figure 2.3-4).

2.3.02 Non-Data Selection

A data channel is non-data selected if any of the non-data select instructions can end operation. The four instructions are: write end-of-file, backspace record, backspace file, and rewind.

Channel Interlock

The channel interlock prevents all non-data select instructions from ending operation (Figure 2.3-5).

Channel Address

The address field of the non-data select instructions contains the channel address. class address, and the unit address. The class and unit address is decoded at the CPU and then cabled to all the data channels on the 7090. The channel address is also decoded at the CPU, but it is cabled only to the addressed data channel.

Class and Unit Selection

When the end operation trigger is turned on, the "set class and unit" address gate is developed. This gate sets the non-data select trigger and the unit select trigger (Figures 2.3-5 and 2.3-3). At this point the data channel is non-data selected. The data

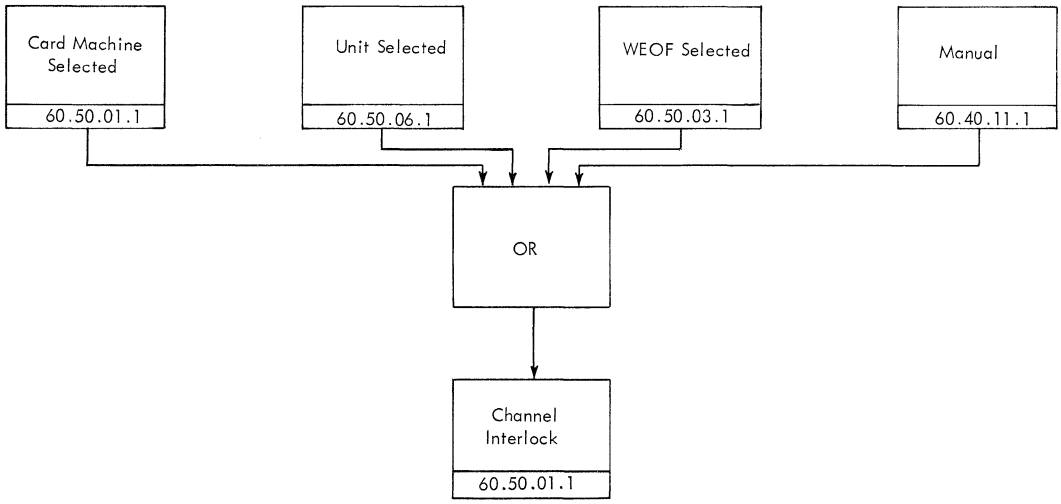

FIGURE 2.3-2. CHANNEL INTERLOCK

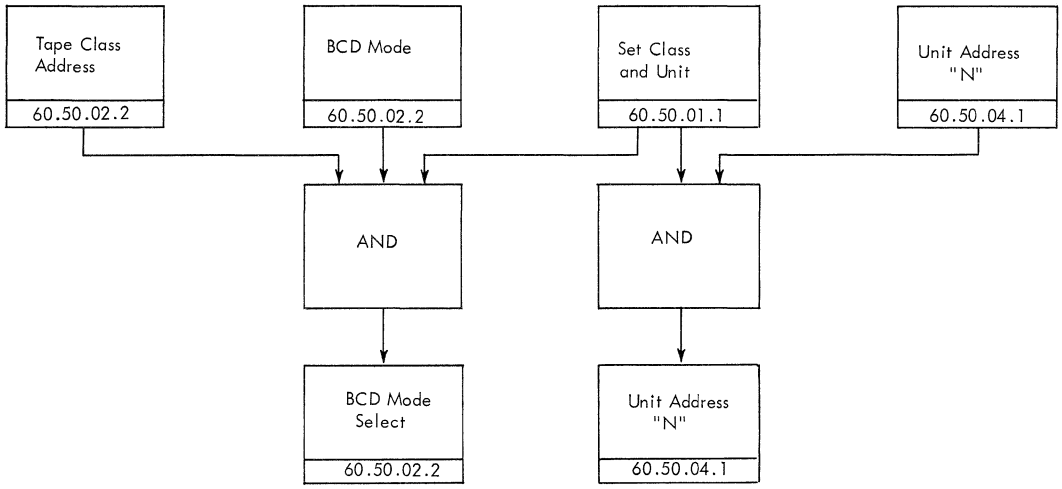

FIGURE 2.3-3. BCD AND UNIT SELECTION

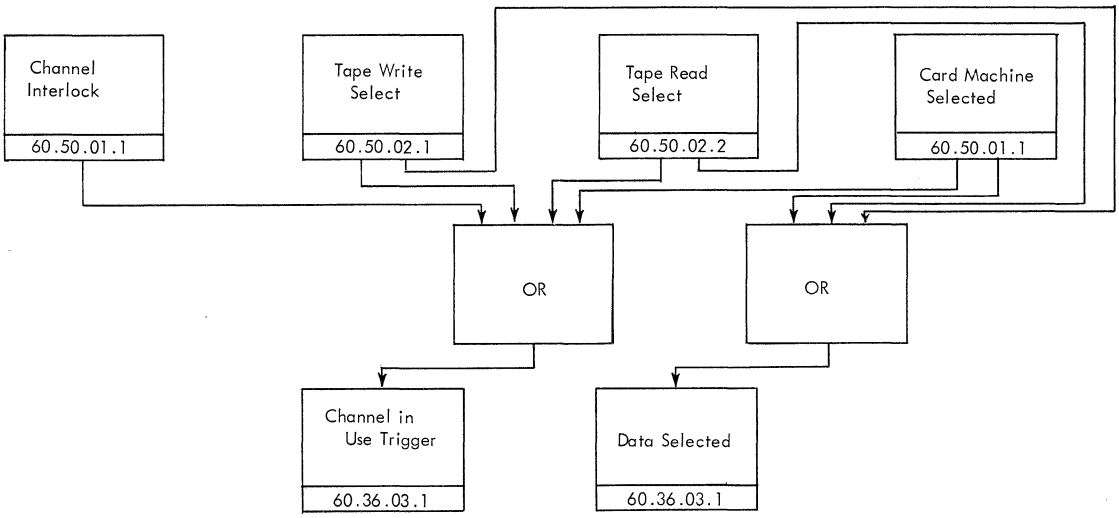

FIGURE 2.3-4. CHANNEL IN USE AND DATA SELECTED

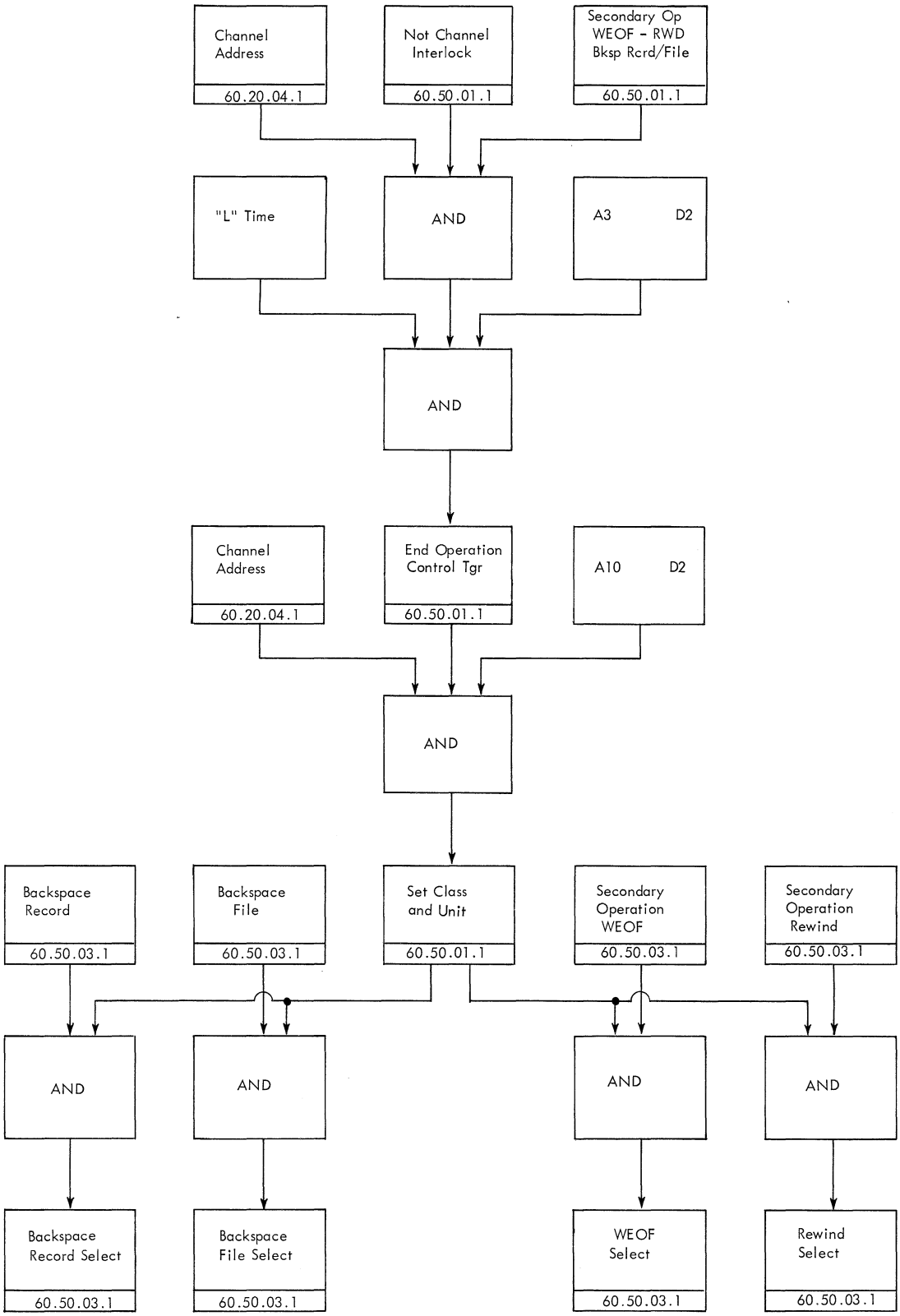

FIGURE 2.3-5. NON-DATA SELECT END OPERATION CONTROL AND NON-DATA SELECTION

channel is interlocked because a unit is selected. (Figure 2.3-2). As long as the data channel is non-data selected, further data-selects or non-data selects hang up in L time at the CPU. With the exception of write end-of-file, the data channel remains non-data selected until the tape adapter unit sends a pulse to reset the non-data select and unit select triggers, respectively. Write end-of-file is a special case. When writing an end-of-file, there is a possibility of turning on the end-of-tape indicator or of having a redundancy check on tape. The data channel is held in use (Figure 2.3-4) until the tape adapter unit is completely through writing the end-of-file. This facilitates the use of a transfer-on-channel in operation or transfer-on-channel not in operation prior to the end-of-tape test or transfer-on-redundancy check instruction. It is important to note, (with the exception of write end-of-file) that, once the tape adapter unit receives the non-data select, it sends a pulse to reset the non-data select and unit select triggers, respectively. At this point, the non-data select instruction has not been completed by the tape adapter unit, but the data channel is free to accept another data-select or non-data select instruction.

A data channel may be data-selected and non-data selected at the same time. With the exception of card machines selected (Figure 2.3-2), a data channel can be non-data selected during the time it is data-selected if the unit triggers are free.

With card machines selected, it is a special case. The unit triggers are reserved for sense type instructions associated with the card machines.

2.3.03 Instructions

The instructions shown control data transmission, monitor the progress of input/output operations, or test conditions met by the input/output equipment.

Reset and Load Channel

The reset and load channel instruction usually follows a data-select instruction. The reset and load channel instruction loads a command into the data channel specified by the operation code of the instruction. The address field of the reset and load channel instruction determines from what address in core storage the command is taken. In the process of executing the instruction, the address from which the command is taken is gated into the data channel's location counter. (See Figure 2.1-3.) The reset and load channel instruction is indexable and it may be indirectly addressed. This instruction is executed if the data channel is not data-selected. In the event it is given when the data channel is not data-selected, the input/output check trigger is turned on. The programmer now has the use of up to eight extra registers (Figure 2.3-6). Note that Figure 2.3-8 shows the "multiplexor retain priority" line.

Load Channel

The load channel instruction is very similar to the reset and load channel instruction. However, the load channel instruction does not load a command into the data channel until the data channel signals for it. Actually, the signal for a new command is initiated by one of the transfer type commands (Figures 3.2-10, 3.2-12, and 3.3-8). At the time the respective data channel signals, the load channel instruction must be decoded and waiting in L time. If it is not, the data channel is disconnected.

The load channel instruction is indexable and it may also be indirectly addressed. See Figure 2.3-7 for the control and flow of load channel. Note that Figure 2.3-9 shows the end operation control for a load channel instruction that is given when a data channel is not data-selected.

Store Channel

The store channel instruction stores the indicator register, location counter, and the channel address counter at an address in core storage specified by the address field of the instruction. This instruction is indexable and it also may be indirectly addressed.

The operation register is stored at positions S, 1, 2, and 19, respectively. The location counter is stored at positions 3-17. The channel address counter is stored at positions 21-35.

Skip and Transfer Instructions

The programmer can test the input/output operation in several ways. He can determine:

How far the prestored input/output program has progressed.
Is the input/output operation completed?
Has the input/output device reached some particular point?
Did a transmission error occur?

The load channel and store channel instructions allow the programmer to answer how far the prestored input/output program has progressed. The other three questions are answered by appropriate skip and transfer type instructions in a program. The results of the skip and transfer instructions can alter the instruction counter and change the course of the stored program.

Transfer on Channel A-H in Operation (TCO A-H), Not in Operation (TCN A-H). For each channel, two transfer instructions are provided to test whether a channel is in operation. The channel is in operation if the "channel in use" line is active (Figure 2.3-4).

Transfer on Redundancy Check, Channel A-H (TRCN A-H). While reading or writing tape, the lateral and longitudinal checking circuits monitor correct data transmission. In the event of an error, the redundancy check indicator is turned on. The status of this indicator may be checked by the transfer on redundancy instruction. If the indicator is on, the transfer on redundancy instruction turns off the indicator and then transfers.

Transfer on End-of-File, Channel A-H (TEF A-H). Each data channel has an end-of-file indicator. Its status can be tested by the transfer on end-of-file instruction. When given, this instruction turns the indicator off.

When reading, the sensing of an end-of-file not only turns on the end-of-file indicator, but initiates a data disconnect.

Beginning-of-Tape Test, Channel A-H, (BTT A-H). Each data channel is provided with a beginning-of-tape indicator. This indicator is turned on if a backspace instruc-

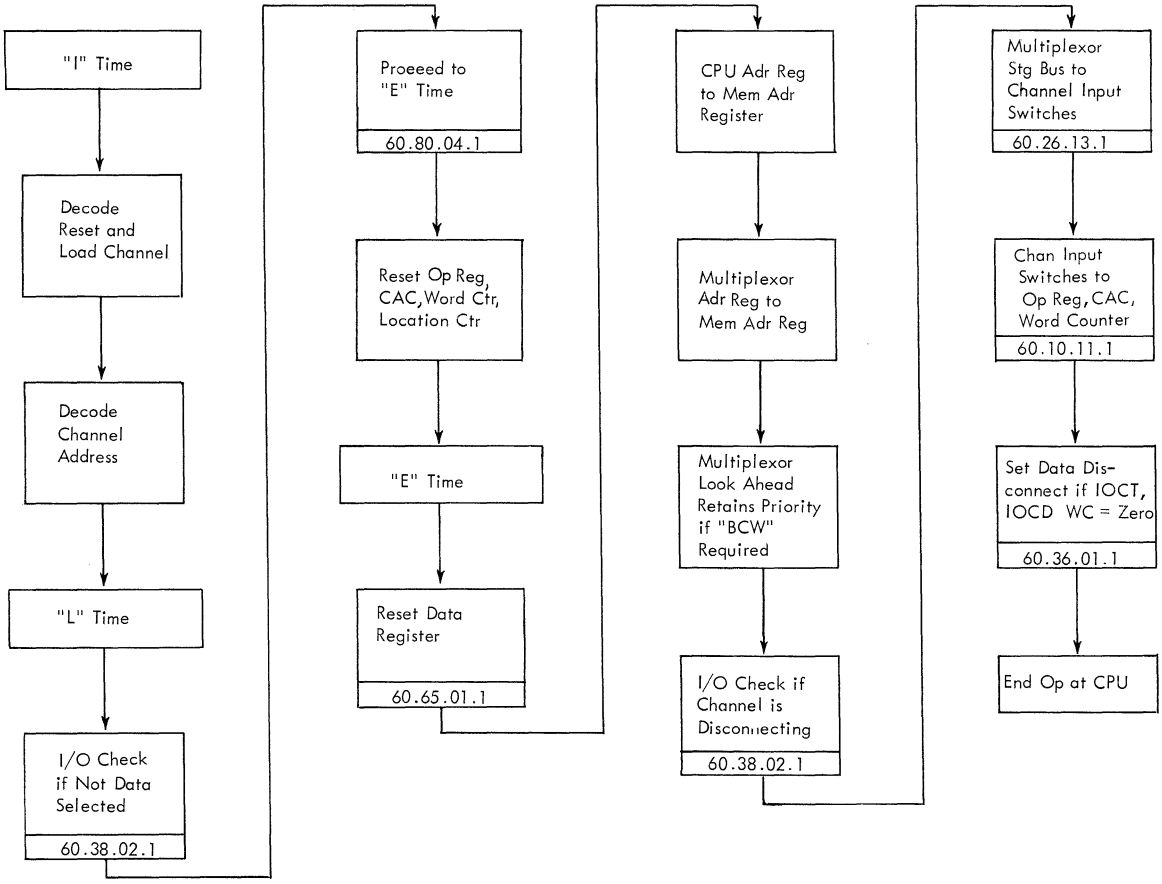

FIGURE 2.3-6. RESET AND LOAD CHANNEL

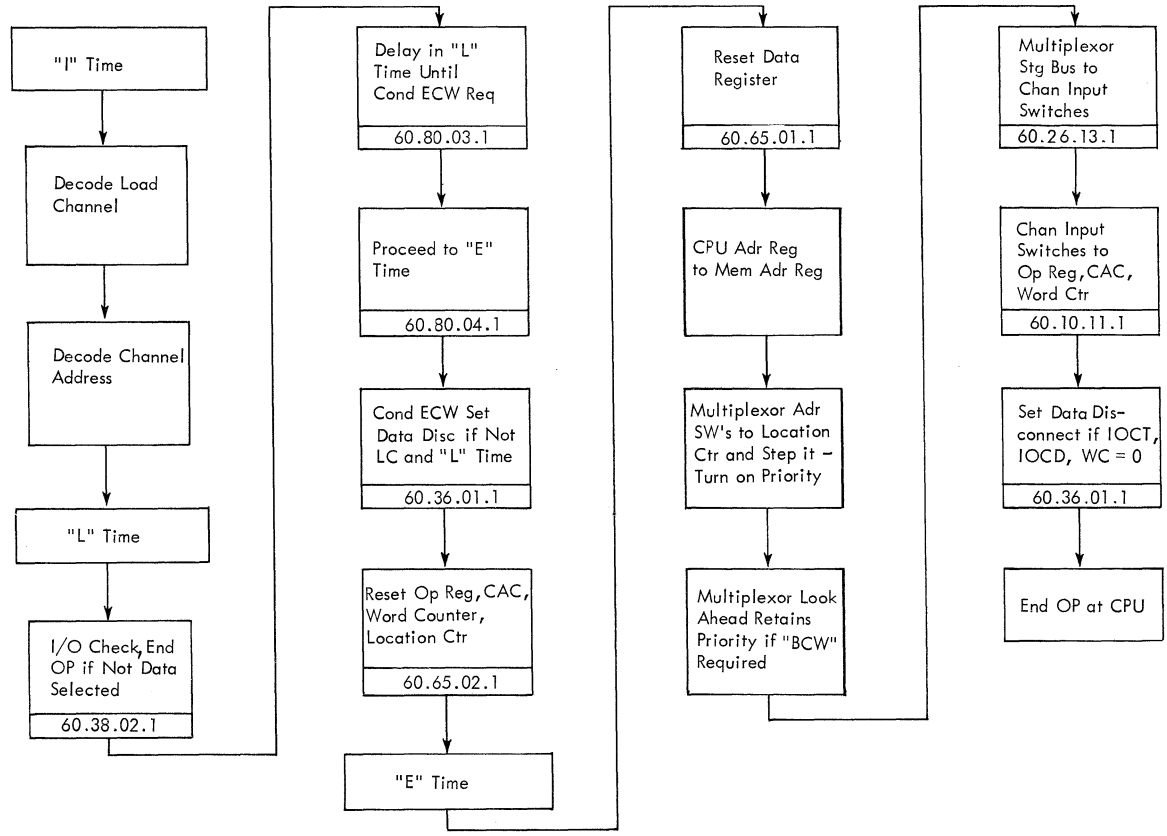

FIGURE 2.3-7. LOAD CHANNEL

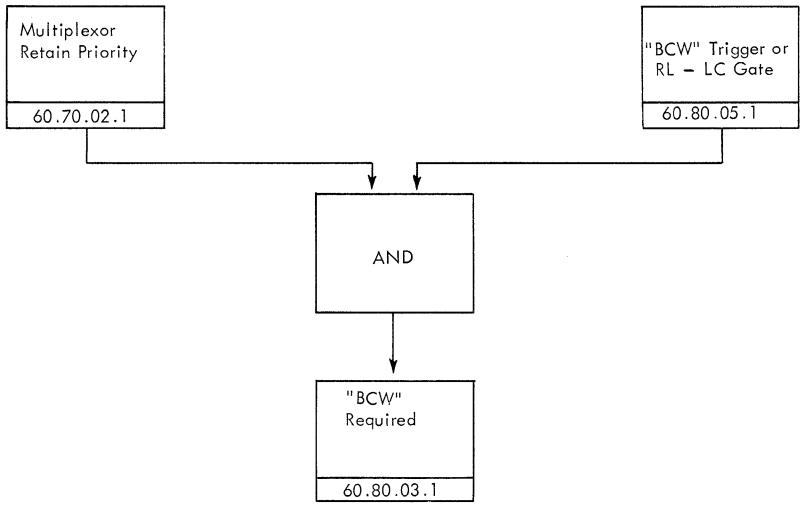

FIGURE 2.3-8. BCW REQUIRED BY MULTIPLEXOR RETAIN PRIORITY

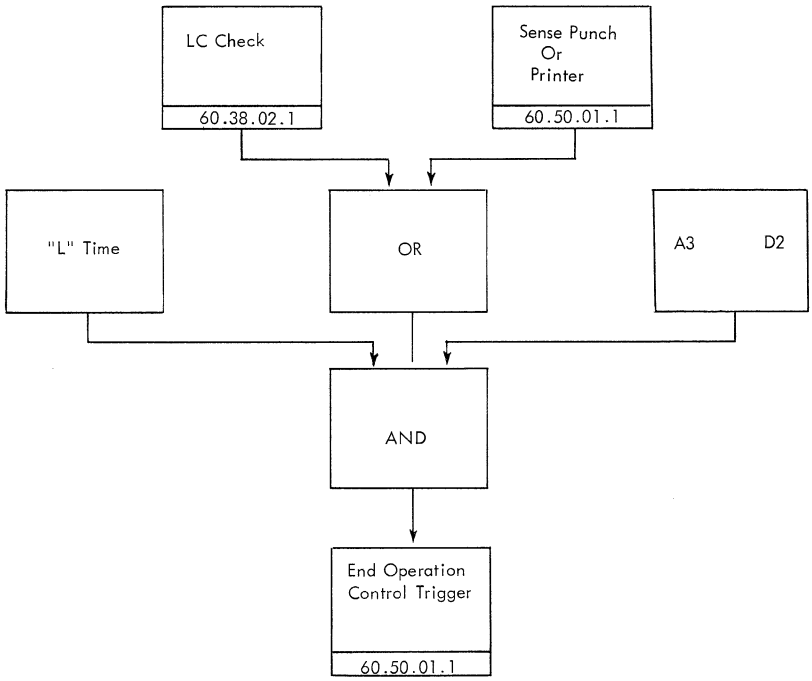

FIGURE 2.3-9. LOAD CHANNEL CHECK AND SENSE PUNCH OR PRINTER END OPERATION CONTROL

tion addresses a tape at load point or in the load point gap. The beginning-of-tape test instruction tests the status of the indicator. If the indicator is off, the CPU program skips the next instruction.

If the indicator is on, the beginning-of-tape test instruction turns it off, and the CPU program takes the next sequential instruction.

End-of-Tape, Test Channel A-H, (ETT A-H). Each data channel has an end-of-tape indicator. It is turned on when a tape unit writes over the end-of-tape reflective spot. Both write select and write end-of-file hold "channel in use" until their respective operations are completed. Thus, a programmer may use a transfer-on-channel in operation to itself prior to executing an end-of-tape test instruction. The operation of this instruction is the same as beginning-of-tape test; that is, they skip the next instruction if the indicator is off. They reset the indicator and take the next sequential instruction if it is on.

Plus Sense Instructions. There are several plus sense instructions associated with card machine operation. These instructions facilitate carriage control of the printer, co-selector pick up and pilot selector pick up by causing hubs to be hot on the various control panels. The address field of the plus sense instructions determines which card machine is to be sensed. These instructions also allow for sensing the conditions of the printer sense entry hubs. If the respective plus sense instruction tests the condition of the sense entry hub and an impulse is present, the CPU program skips the next instruction. If no impulse is present, the CPU program takes the next instruction in sequence. Figure 2.3-9 shows the end operation control for these instructions.

I/O Check Test Instruction (IOT). This instruction tests the status of the I/O check trigger located in the CPU. This trigger is turned on by:

1. A reset and load or load channel instruction, given while the addressed data channel is not data-selected, or
2. The arrival of a new I/O demand, if the previous demand has not been serviced (did not get B time). See Figures 3.2-14 and 3.3-9.

If the indicator is on, the next sequential instruction is executed and the indicator is turned off. If the indicator is off, the CPU program skips the instruction following the I/O check test.

3.0.00 OPERATIONS

3.1.00 TYPES OF CORE STORAGE CYCLES

A core storage use cycle is an I or an E cycle in which the memory address register is set from the CPU address register. A core storage cycle in which the memory address register is set from a data channel register is a B cycle.

3.1.01 "BDW"

A "BDW" cycle is defined as a core storage cycle used to transmit data to or from the data channel and core storage. This is a B cycle because the memory address register is set from the channel address counter. A "BDW" cycle is unique to the data channel that has priority. Both the channel address counter and the word counter are stepped during a "BDW" cycle (Figure 3.1-1).

3.1.02 "BCW"

When a proceed type command signals for a new command, the address of the new command is specified by the contents of the location counter. The core storage cycle that is used to bring the new command to the data channel is defined as a "BCW" cycle. The core storage cycle that is initiated by a transfer-in-channel command, or an indirectly addressed command, is also defined as a "BCW" cycle. The "BCW" cycle is unique to the data channel that has priority.

3.1.03 "ECW"

When a load or reset and load channel instruction is executed, the address of the command to be loaded into the addressed data channel is specified by the address field of the instruction. This address is set to the storage address register. During the E cycle of these instructions, a new command is loaded into the addressed data channel. The E cycle of these two instructions is defined as an "ECW" cycle (RL/LC gate in the data channel), Figure 3.1-2.

3.1.04 Priority of B Cycles

Because of the possibility of having more than one data channel asking for B time simultaneously, the data channel must incorporate priority circuits. These circuits do nothing more than determine which data channel gets B time first. By definition, the most remote data channel asking for B time gets priority. The most remote data channel is the last physical channel on that bank, predetermined by multiplexor cabling (Figure 3.1-3).

A B cycle demand is cabled to the CPU at the same time a data channel asks for priority, (Figure 3.1-3). The B time trigger is turned on at the CPU and its output is cabled to all data channels on the 7090. With the B time trigger on, the next core storage cycle is either a "BDW" cycle or a "BCW" cycle.

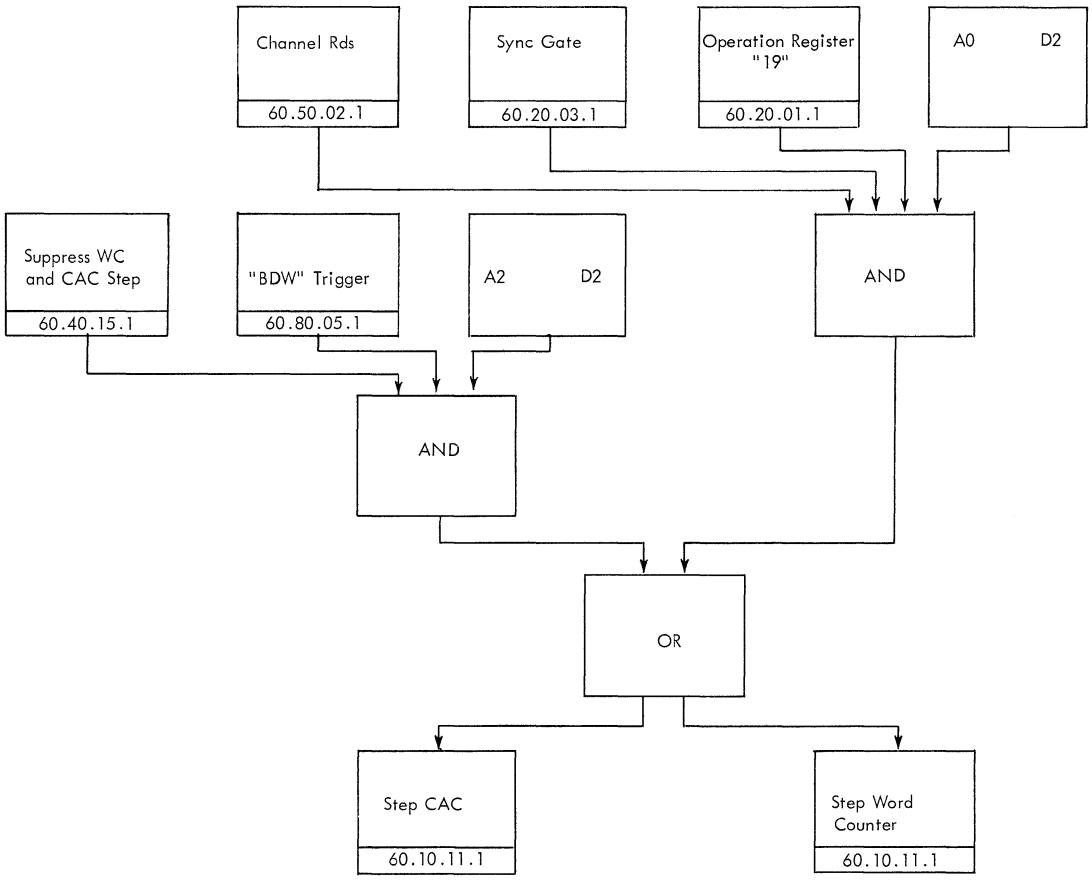

FIGURE 3.1-1. STEP CHANNEL ADDRESS COUNTER AND WORD COUNTER

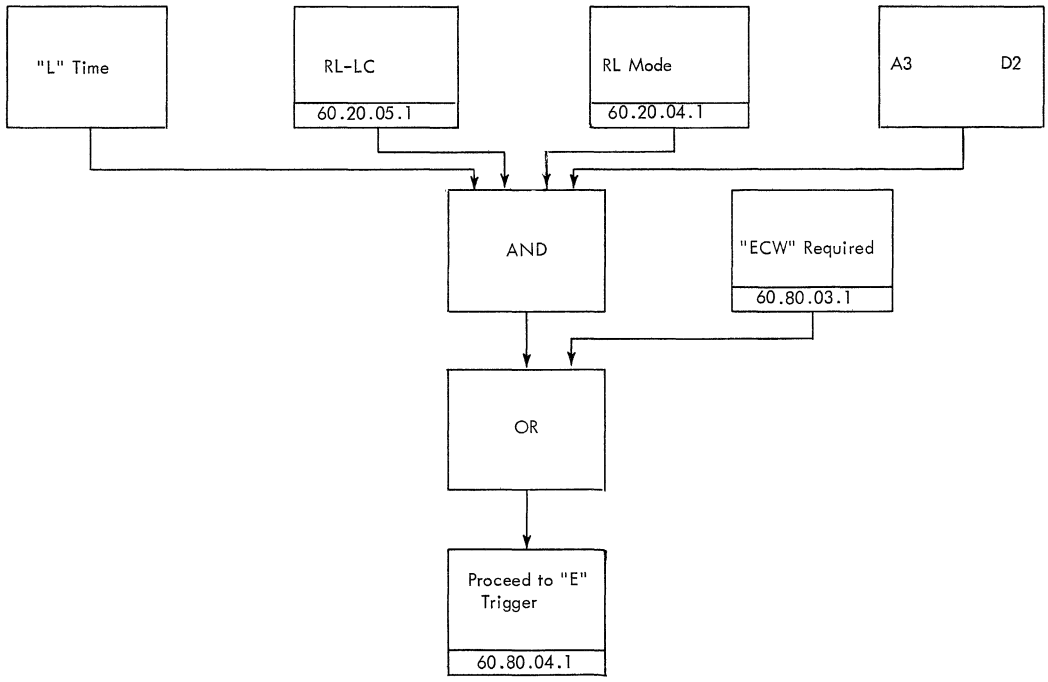

FIGURE 3.1-2. PROCEED TO "E" TIME

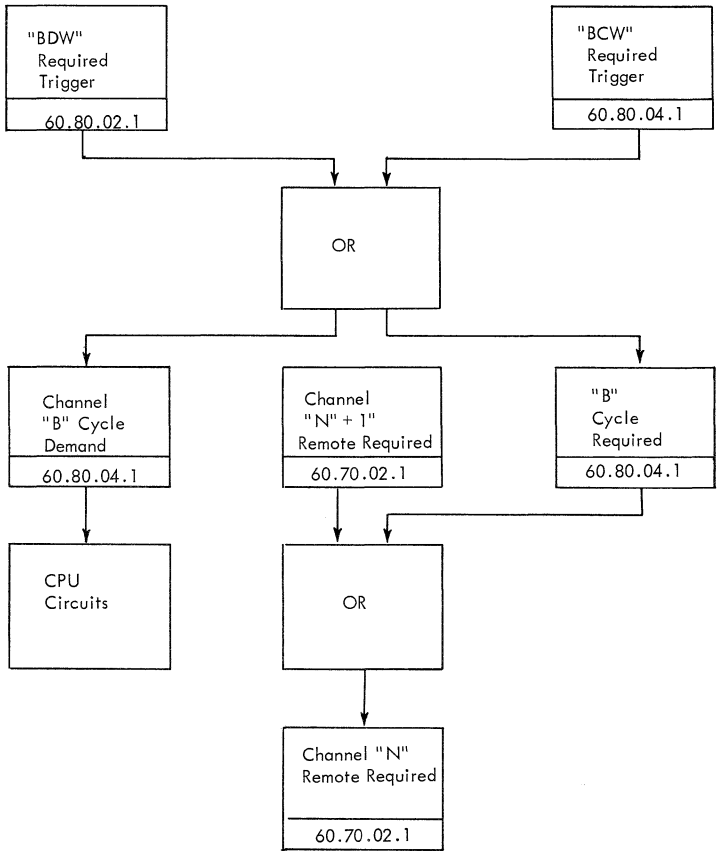

FIGURE 3.1-3. B CYCLE REQUIRED AND REMOTE REQUIRED

With B time available at all data channels, the differentiation as to which data channel receives priority is depicted in Figure 3.1-4. The priority trigger is the differentiation as to which data channel is executing a "BDW" or "BCW" cycle (Figure 3.1-4).

The priority trigger is turned on during an "ECW" cycle (RL/LC gate) because there is a possibility that the data channel executing the "ECW" cycle might require a "BCW" cycle in succession (Figure 3.1-5).

3.2.00 WRITE

Writing is the process of taking a word from the computer's internal storage to a selected output device. While writing, a buffering action is performed by the data channel by holding the transmitted word in the data register until the selected output device sends a "demand." At this time, the contents of the data register are transmitted to the output device (tape register if writing tape). The "demand" initiates a "sync gate" that turns off the data register loaded trigger (Figure 3.2-1). With the data register loaded trigger off and the word count not zero, a request for a "BDW" cycle is developed (Figure 3.2-1). Once the data channel gets its "BDW" cycle, the data register loaded trigger is turned on and stays on until another "sync gate" is developed.

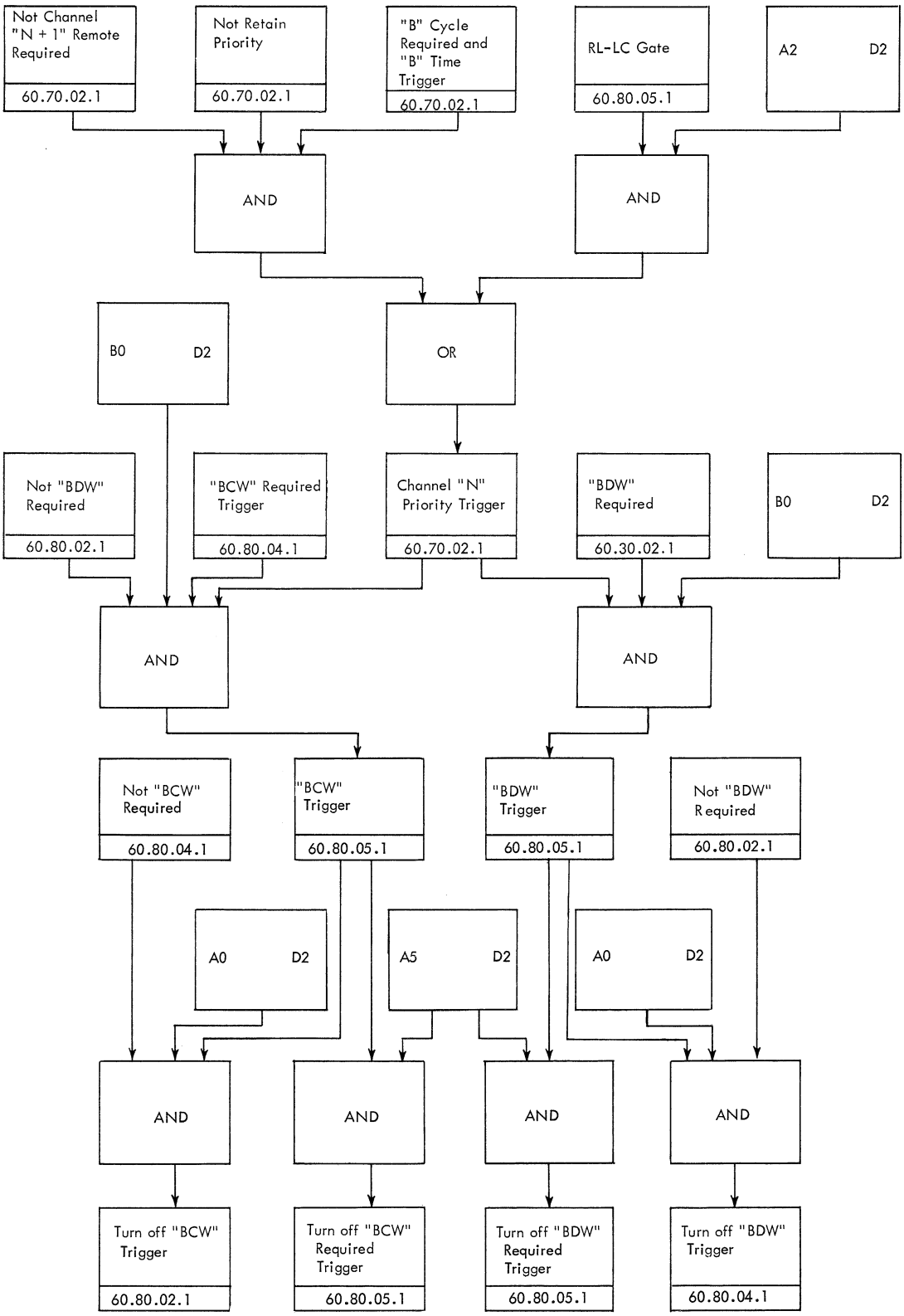

FIGURE 3.1-4. CHANNEL PRIORITY, "BCW" TRIGGER, AND BDW TRIGGER

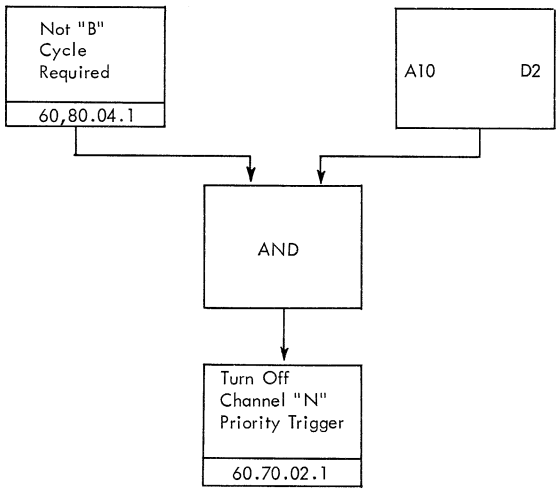

FIGURE 3.1-5. TURN OFF CHANNEL PRIORITY

When writing tape, the word to be written is gated from the data register to the tape register ("tape demand" gates it). From the tape register, the characters are gated through the "write translator" to the tape adapter unit under control of the group counter. The group counter is stepped once for each character that is written on tape. When it reaches 6, this indicates a full word (six characters) has been written. At this time a "demand" gates the next word into the tape register if the data register is loaded.

3.2.01 Input/Output Count and Disconnect (IOCD)

Figure 3.2-2 shows the control during a write operation using an IOCD command with a word count of 2. Note that after the word count is reduced to 0, the data disconnect gate is not set until the next "sync gate" (turns off data register loaded trigger, Figure 3.2-3). This insures transmitting the last word from the data register to the selected output device.

3.2.02 Input/Output Count and Proceed (IOCP)

When writing with an IOCP command, the data transmission occurs in the same manner as when using an IOCD command. However, after the word count is reduced to 0, a request for a "BCW" cycle is developed. This request is delayed until the last word is transmitted from the data register to the selected output device. The "sync gate" turns off the data register loaded trigger. With the word count equal to 0, and the "sync gate," a "control word gate" is developed (Figure 3.2-4). It is the "control word gate" that initiates the "BCW" request (Figure 3.2-4).

Figure 3.2-5 shows the control of an IOCP command starting with the BDW cycle in which the word count is reduced to 0. Notice during the "BCW" cycle the address of the new command is specified by the contents of the location counter. The contents of the location counter also are increased by one (Figure 3.2-6). The new command now controls further data transmission. The IOCP command thus facilitates automatic look-up of a new command without assistance from a CPU program.

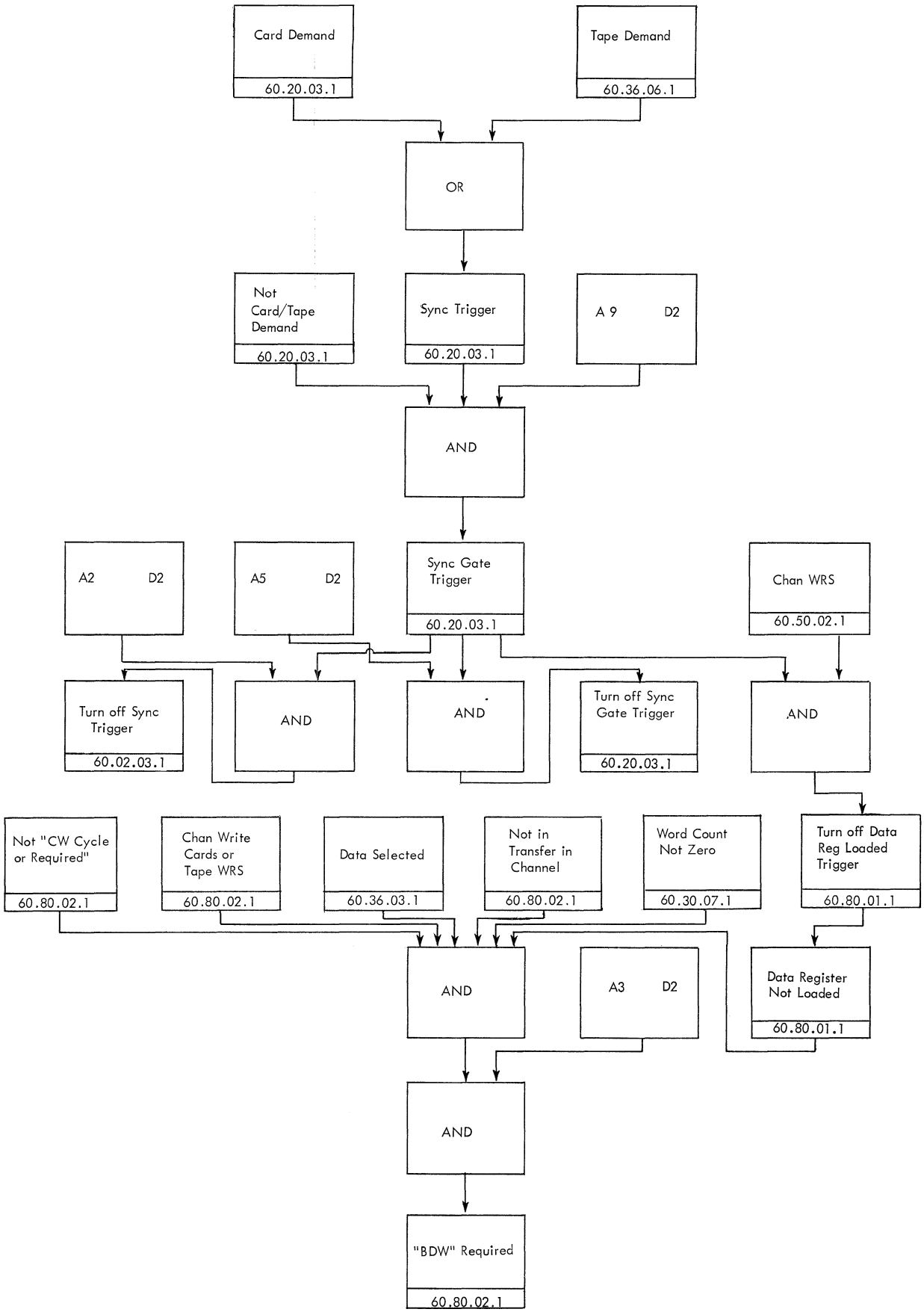

FIGURE 3.2-1. SYNC GATE AND "BDW" REQUIRED WHILE WRITING

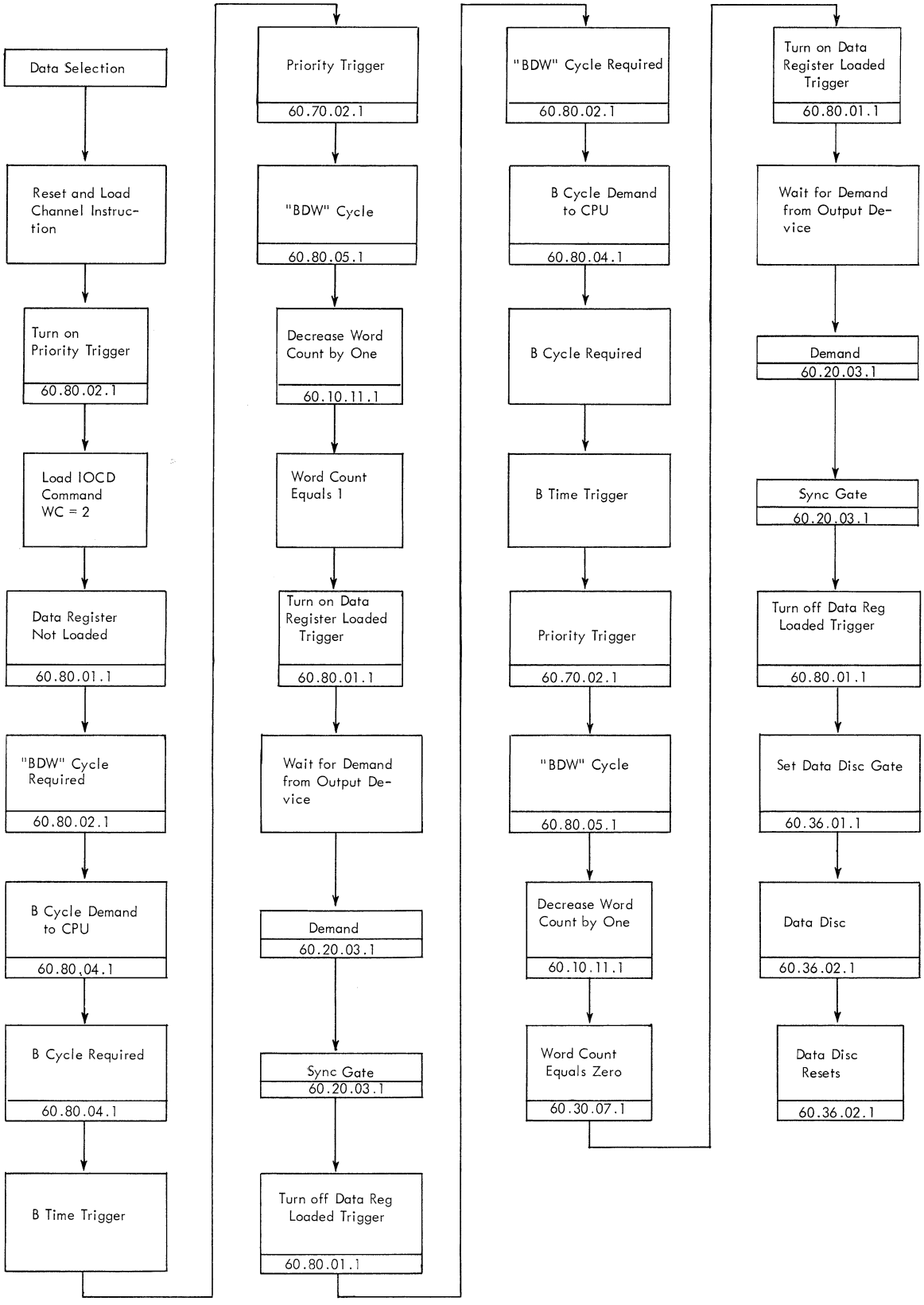

FIGURE 3.2-2. WRITING WITH AN IOCD COMMAND, WORD COUNT OF 2

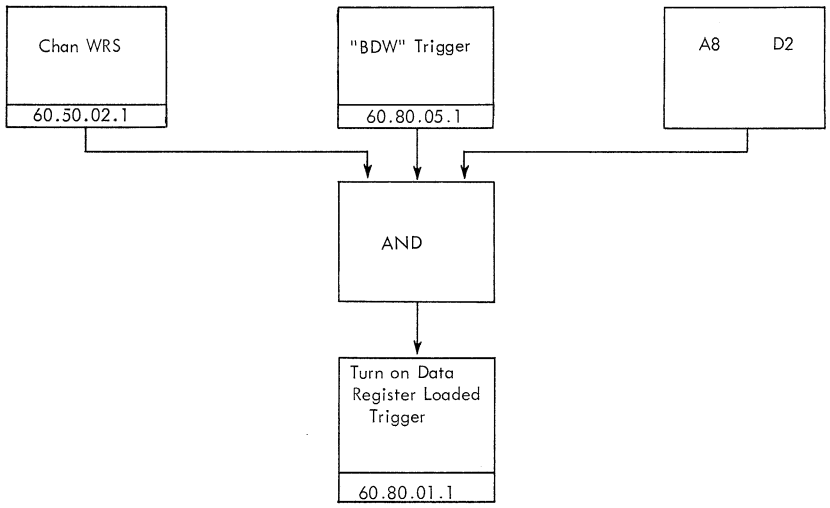

FIGURE 3.2-3. TURN ON DATA REGISTER LOADED TRIGGER WHILE WRITING

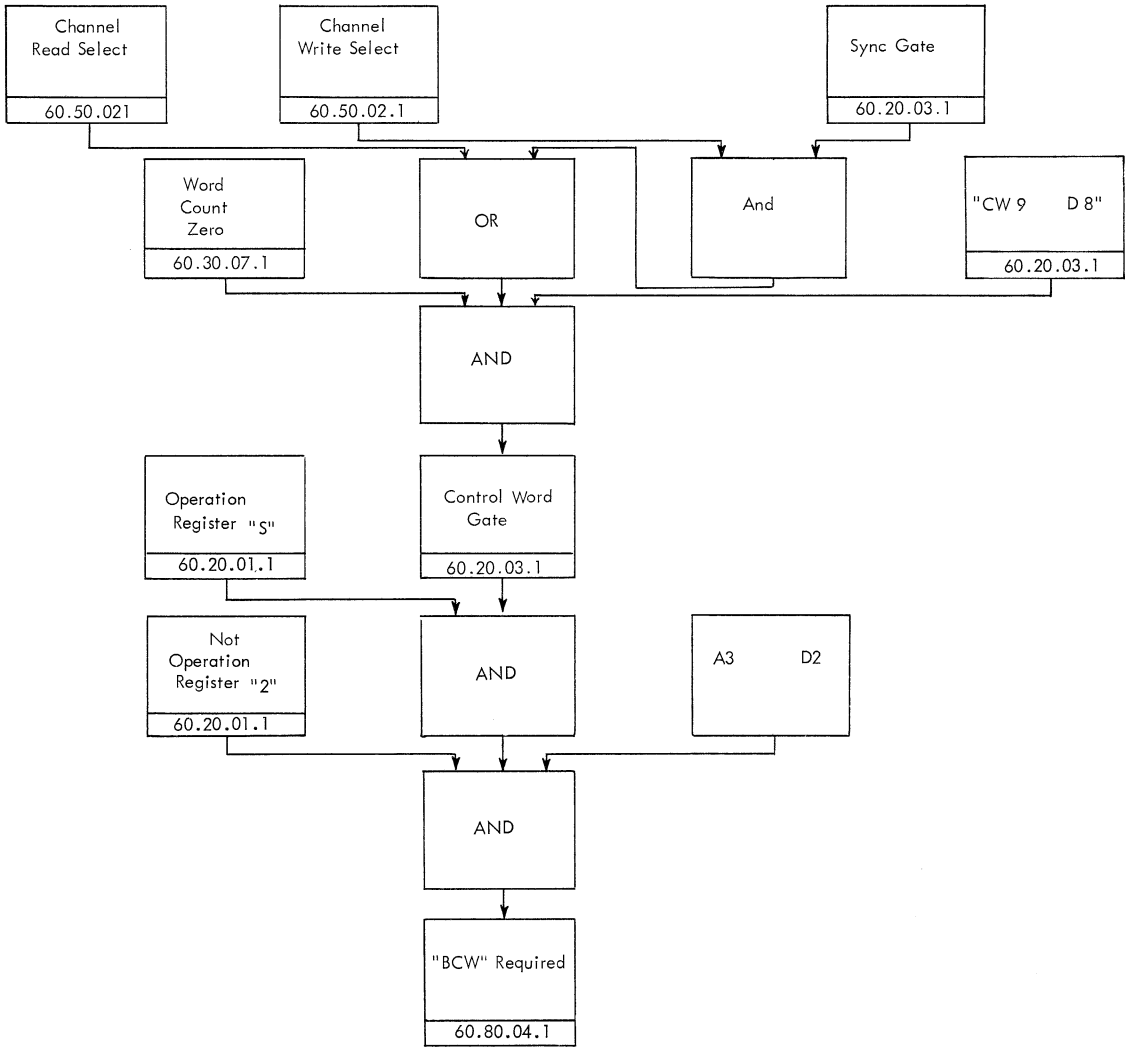

FIGURE 3.2-4. CONTROL WORD GATE AND "BCW" REQUIRED IOCP COMMAND

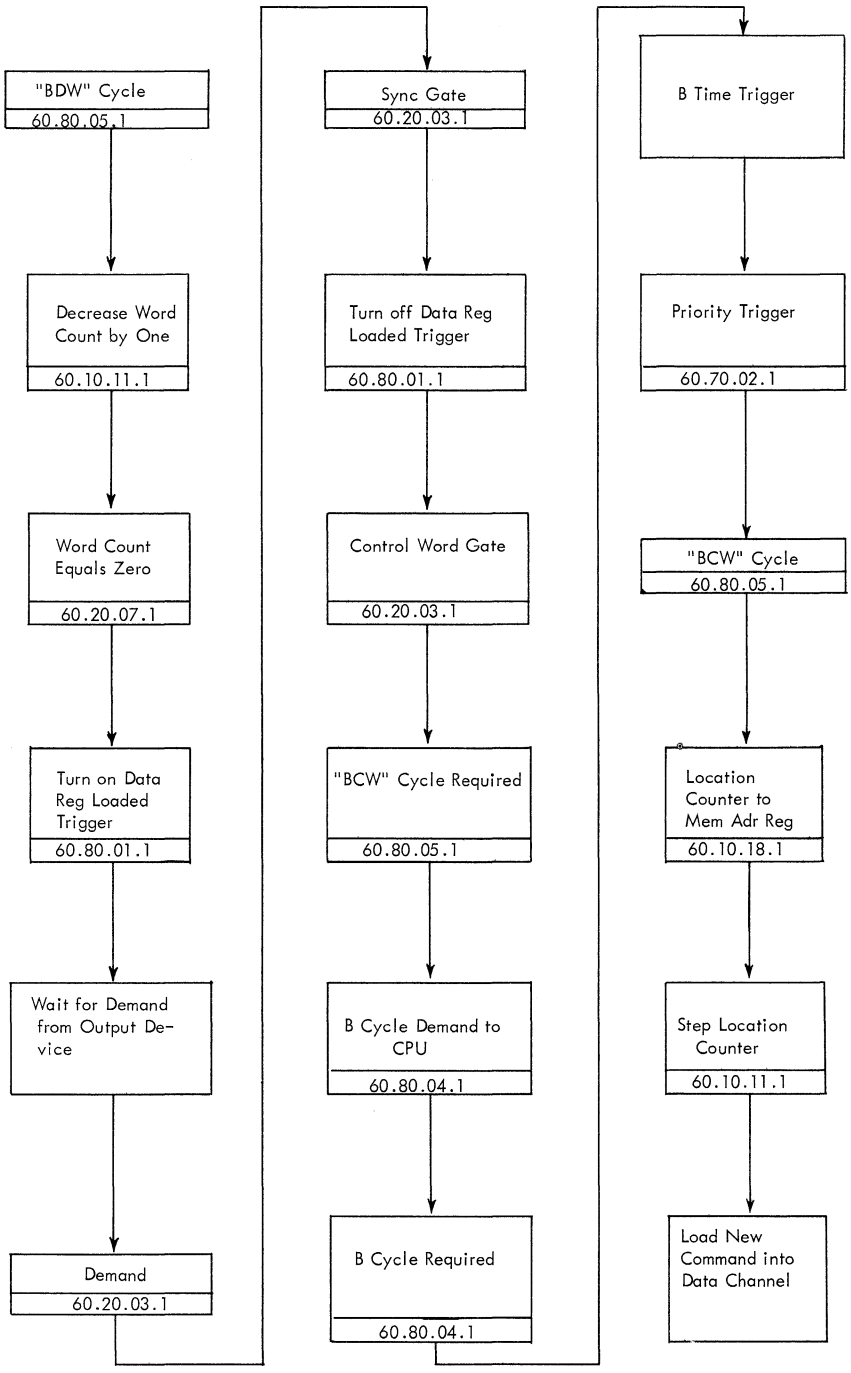

FIGURE 3.2-5. WRITING WITH AN IOCP COMMAND

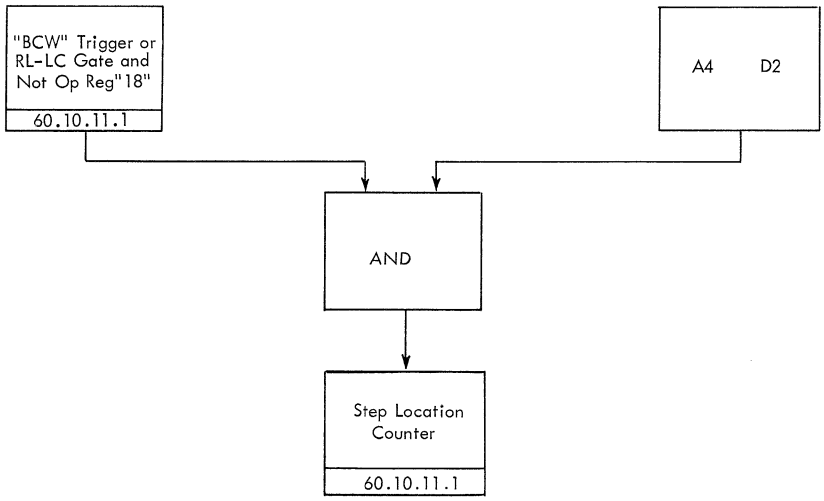

FIGURE 3.2-6. STEP LOCATION COUNTER

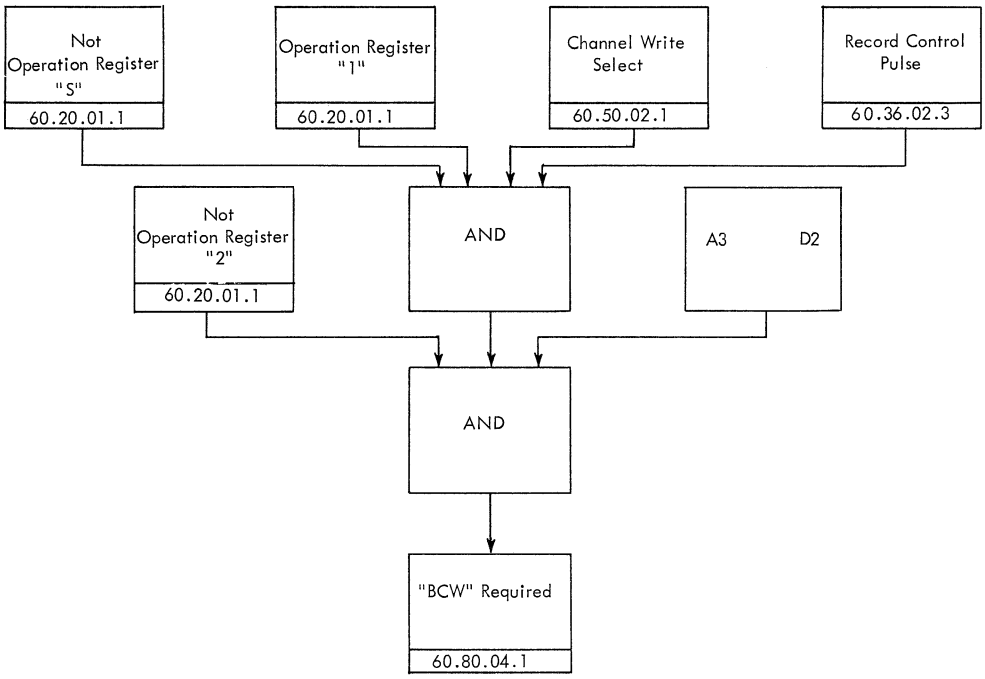

FIGURE 3.2-7. "BCW" REQUIRED WHILE WRITING WITH AN IORP COMMAND

3.2.03 Input/Output Record and Proceed (IORP)

Figure 3.2-7 shows that a request for a BCW cycle is delayed until a "record control pulse" is developed. The "record control pulse" is developed after an entire record has been written.

Writing on Tape

The "record control pulse" is developed after the word count of the IORP command is reduced to 0, At this time, the entire record has been written and a new command may be loaded into the data channel (Figure 3.2-8).

Writing on Printer or Punch

The "record control pulse" is developed at a fixed time when writing printer or punch. The word count of the IORP command may or may not be reduced to 0 at the time the "record control pulse" is developed. In either case, the request for a "BCW" cycle comes with the development of the "record control pulse" (Figure 3.2-9).

The IORP command thus facilitates writing multiple records with one write select instruction. That is, the next record to be written is under control of the new command.

3.2.04 Input/Output Count and Transfer (IOCT)

The use of the IOCT command is identical to that of the IOCP command in regard to data transmission. When the word count is reduced to 0 and the last word is written, a "control word gate" is also developed. When using the IOCP command, the "control word gate" initiates a "BCW" cycle. With the IOCT command, it initiates an "ECW" cycle if a load channel instruction is waiting in L time (transfer control to the CPU program, 3.2-10). A "load channel mode disconnect" is initiated by the "control word gate" if the load channel instruction is not waiting in L time. Logically, the data channel is data-disconnected because the CPU program did not provide the load channel instruction in time.

Figure 3.2-11 shows the control of an IOCT command starting with the BDW cycle in which the word count is reduced to 0.

3.2.05 Input/Output Record and Transfer (IORT)

The IORT command does not transfer control to the CPU program until a "record control pulse" is developed (Figure 3.2-12). The "record control pulse" is developed in the same manner as discussed in Section 3.2.03. Figure 3.2-13 shows the transfer control to the CPU program when using the IORT command.

3.2.06 Signal Type Commands

When writing, signal type commands act as count control commands. The proceed or transfer control is not initiated until the word count is reduced to 0. Note that during a read printer operation, writing does occur but the signal type commands are active. This is because the echo checking is a read operation.

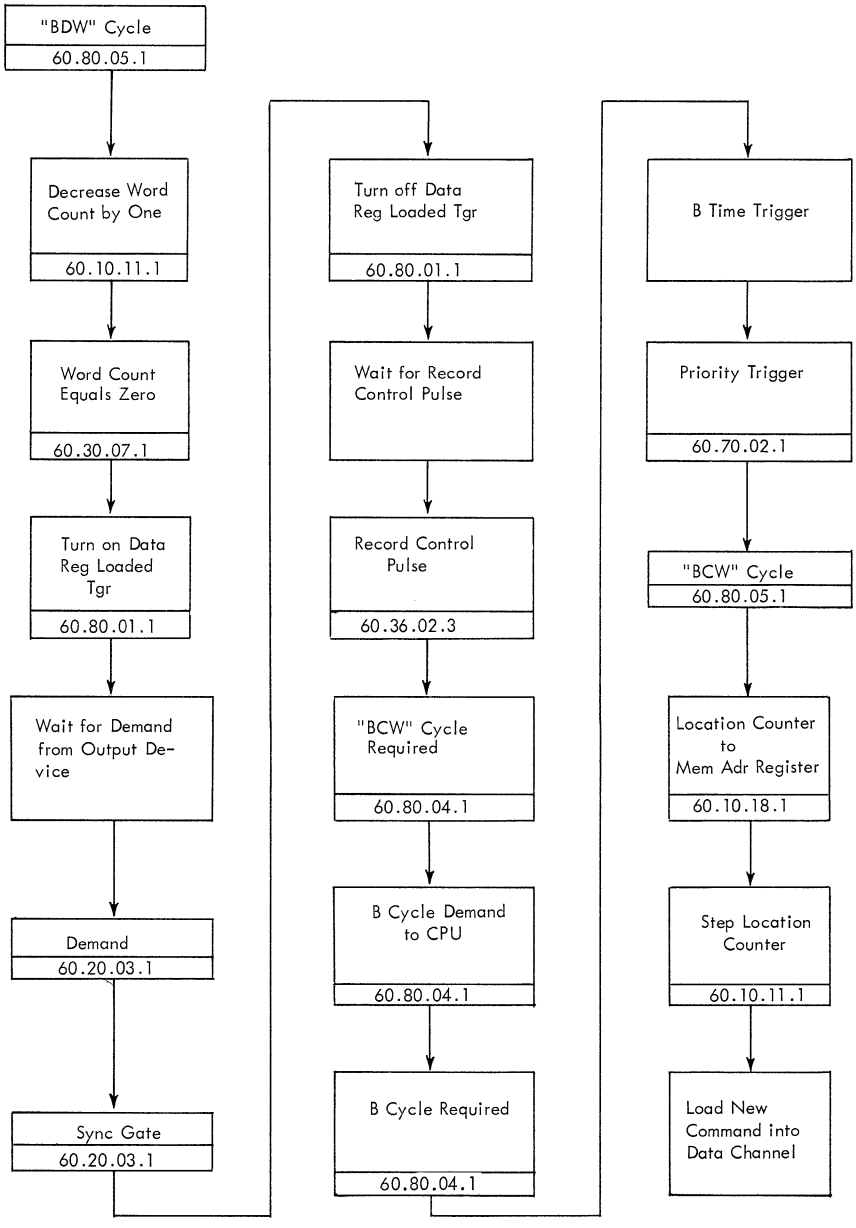

FIGURE 3.2-8. WRITING ON TAPE WITH AN IORT COMMAND

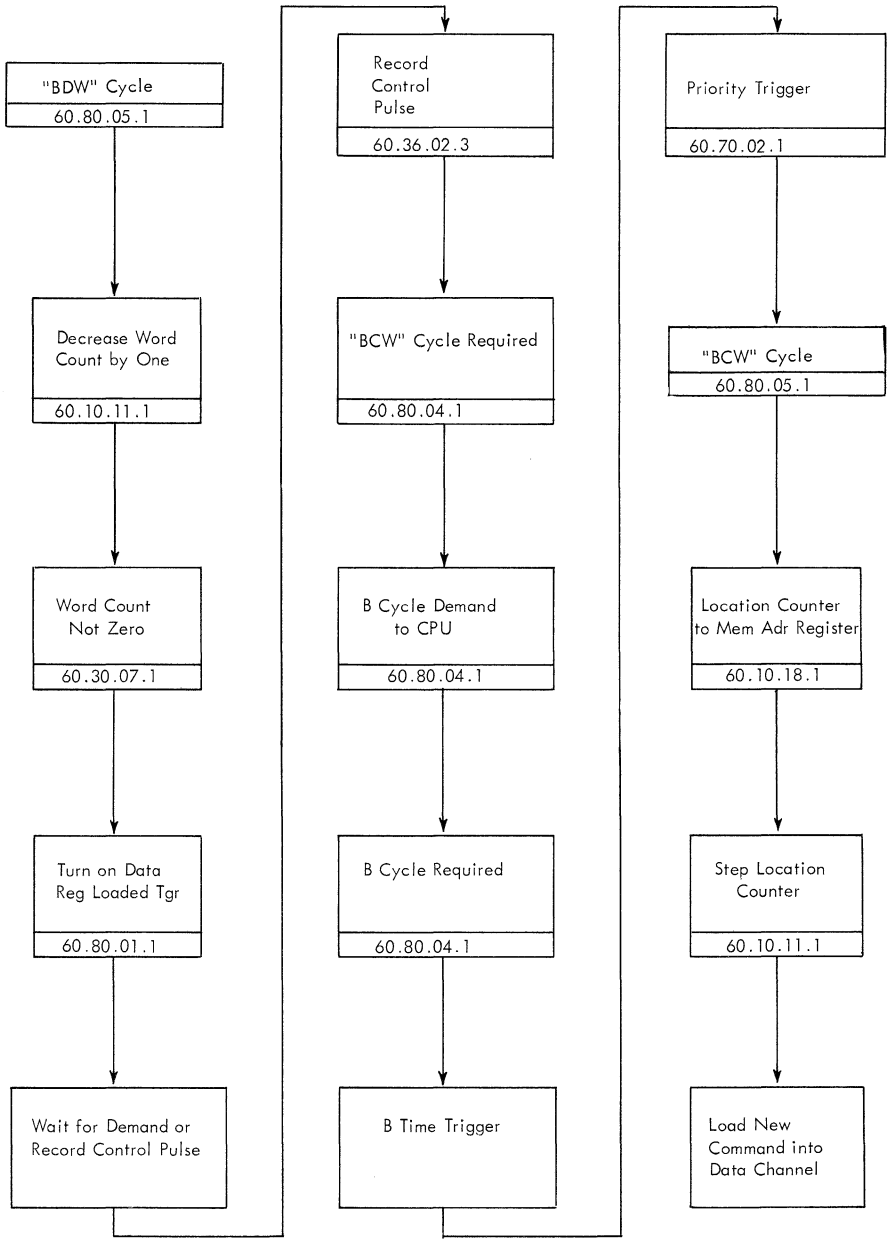

FIGURE 3.2-9. WRITING ON PRINTER OR PUNCH WITH AN IORP COMMAND

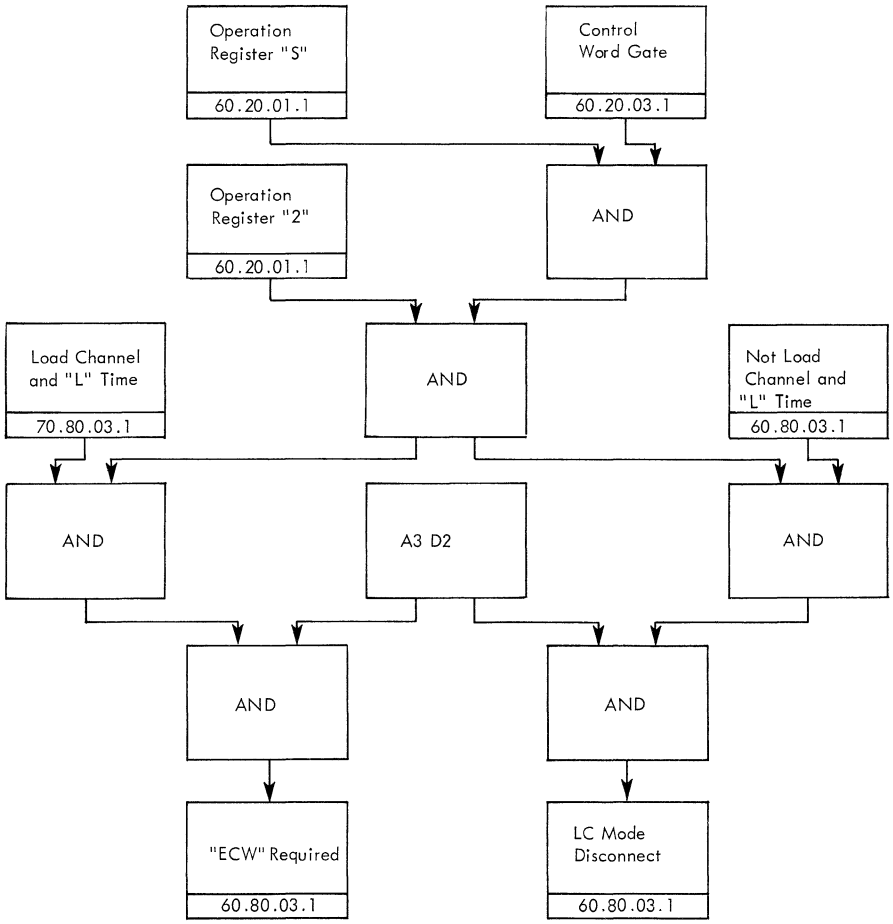

FIGURE 3.2-10. "ECW" REQUIRED, IOCT COMMAND

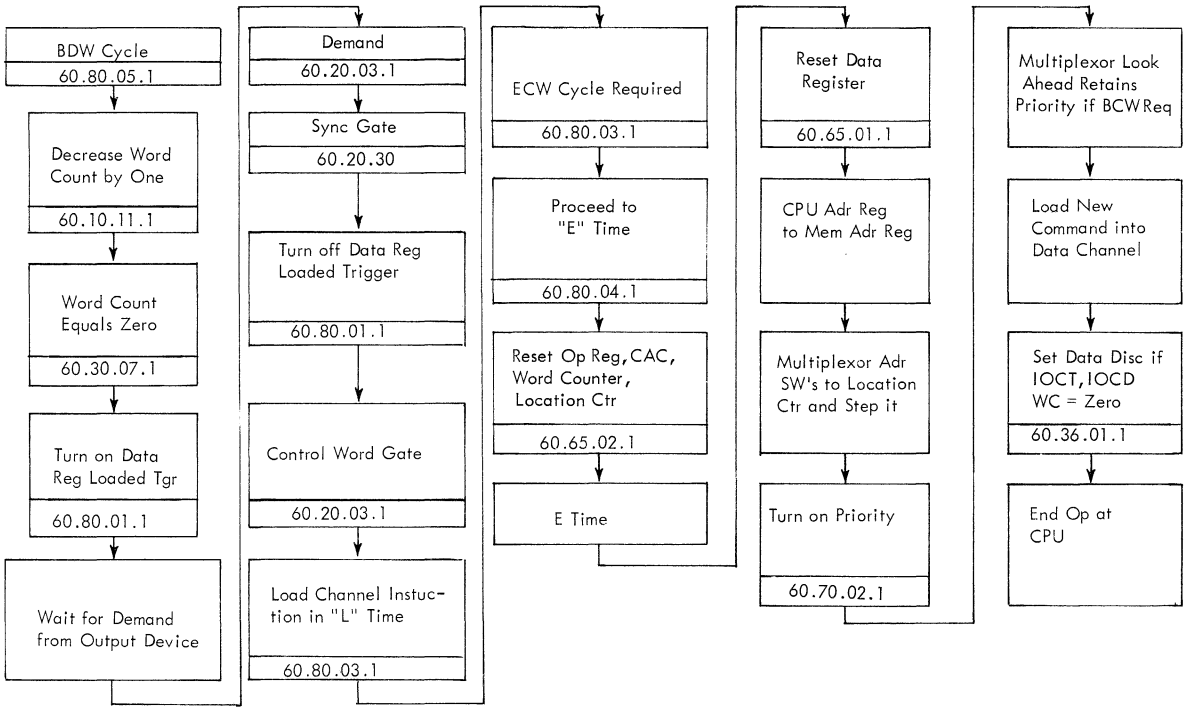

FIGURE 3.2-11 WRITING WITH AN IOCT COMMAND

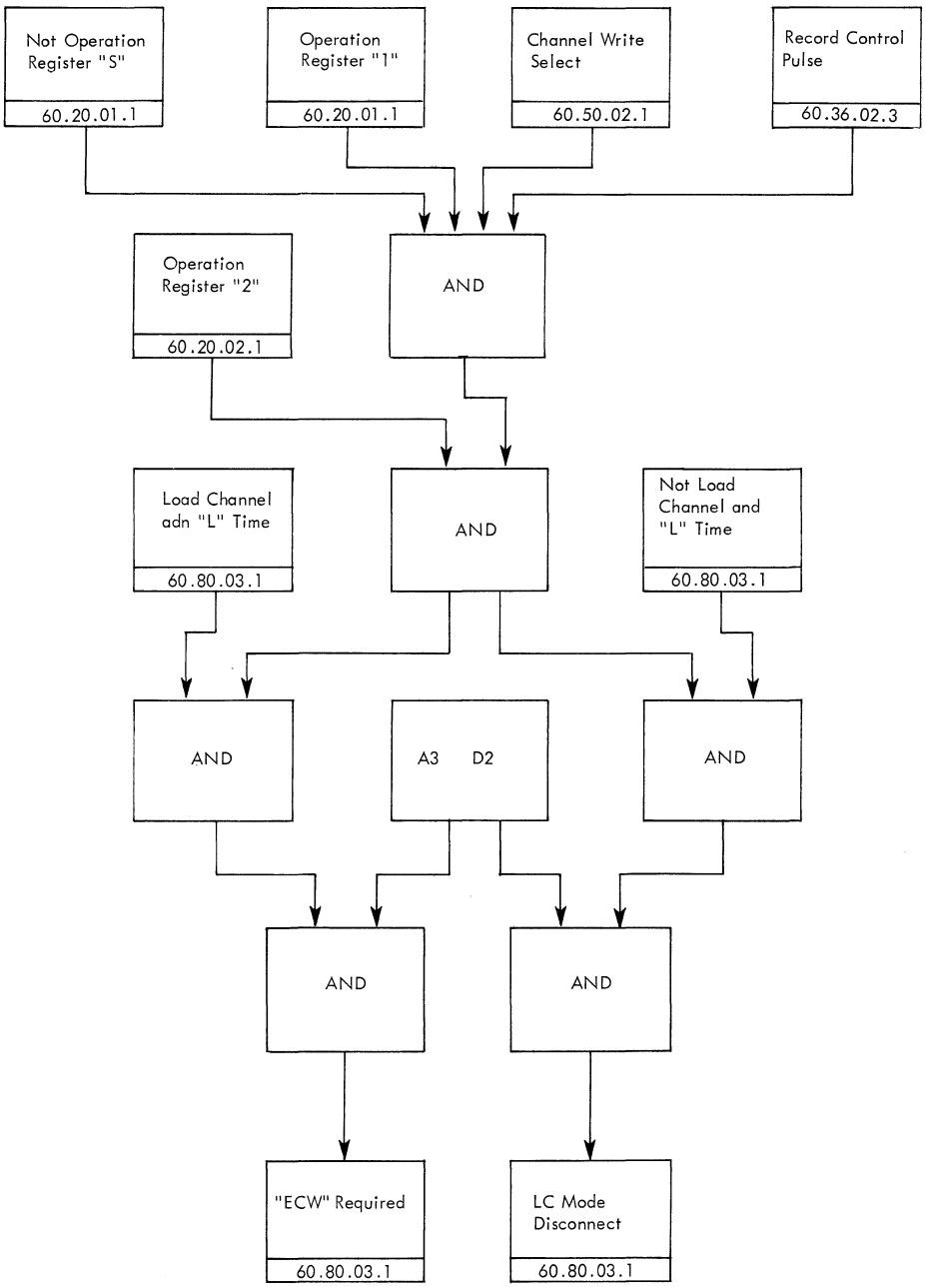

FIGURE 3.2-12. "ECW" REQUIRED WHILE WRITING WITH AN IORT COMMAND

3.2.07 Input/Output Check While Writing

Figure 3.2-14 shows that a data channel will "I/O check" if the data register is not loaded by the time the next "demand" is received by the data channel. The I/O check trigger located at the CPU is turned on and may be tested with the I/O check test instruction. The I/O check also data-disconnects the respective data channel.

3.3.00 READ

When reading is taking place, a word is transmitted from the selected input device to the data channel. The data channel performs a buffering action by holding the word in the data register until the computer's internal storage can accept it. A "demand" from the selected input device develops a "sync gate." At this time, the word being read is being held in the data register. The "sync gate" turns on the data register loaded trigger. The data register loaded trigger initiates a request for a "BDW" cycle (Figure 3.3-1). During the data channel's "BDW" cycle, the data register is stored at an address in core storage. The address is determined by the contents of the channel address counter (Figure 3.3-2).

During tape reading, characters are gated from the tape adapter unit, through the read translator, to the tape register. The characters are counted by the group counter. The group counter performs two functions. It acts as a commutator. That is, it controls the gating of successive characters to respective positions of the tape register. It also counts the characters that are gated to the tape register. When the count reaches 6 (six characters being held in the tape register), a "demand" is developed. The "demand" develops the "sync gate." It is the "sync gate" that gates the tape register to the data register.

3.3.01 Input/Output Count and Disconnect (IOCD)

Figure 3.3-3 shows the control during a read operation using an IOCD command with a word count of 1. After the word count is reduced to 0, the disconnect is delayed until the next "demand" or "record control gate" is received from the selected input device. Note that the data register loaded trigger is turned off during the "BDW" cycle (Figure 3.3-4).

3.3.02 Input/Output Count and Proceed (IOCP)

When reading with an IOCP command, the data transmission occurs in the same manner as when using an IOCD command. A request for a "BCW" cycle is developed during the "BDW" cycle in which the word count is reduced to 0. Figure 3.3-5 shows the control of data transmission ("BDW" cycle), the request for a "BCW" cycle, and the "BCW" cycle.

3.3.03 Input/Output Record and Proceed (IORP)

When using the IORP command, the request for a "BCW" cycle is delayed until the "record control pulse" is developed, (Figure 3.3-6). Data transmission is terminated with word count of 0 or "record control pulse."

Note that the record control pulse is delayed during a read printer operation. This insures the transmission of echoes when desired.

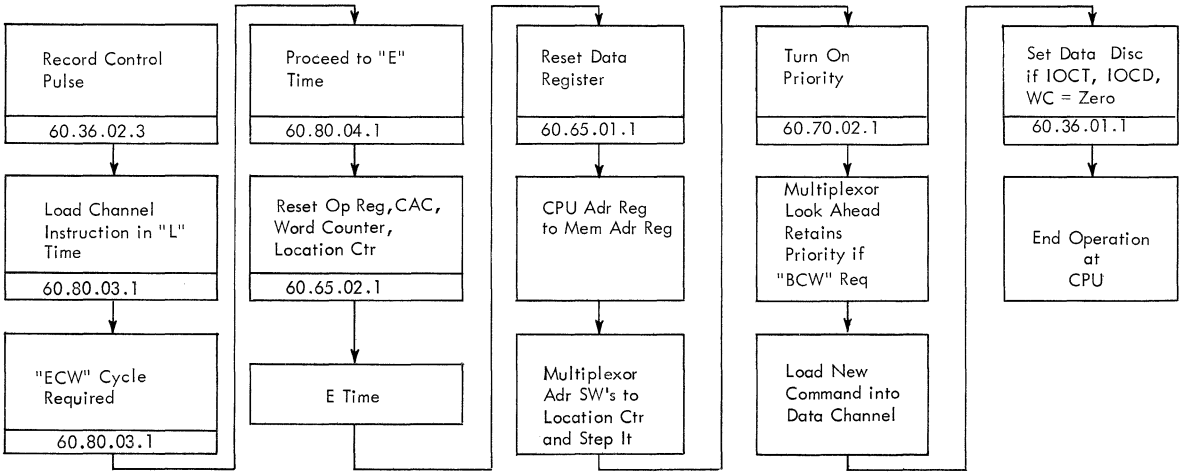

FIGURE 3.2-13. READING OR WRITING WITH AN IORT COMMAND

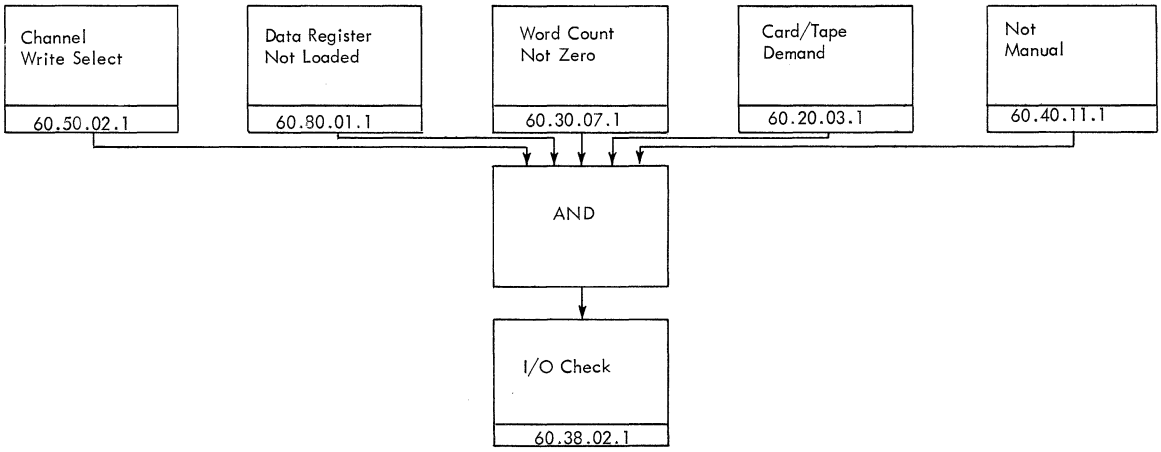

FIGURE 3.2-14. I/O CHECK WHILE WRITING

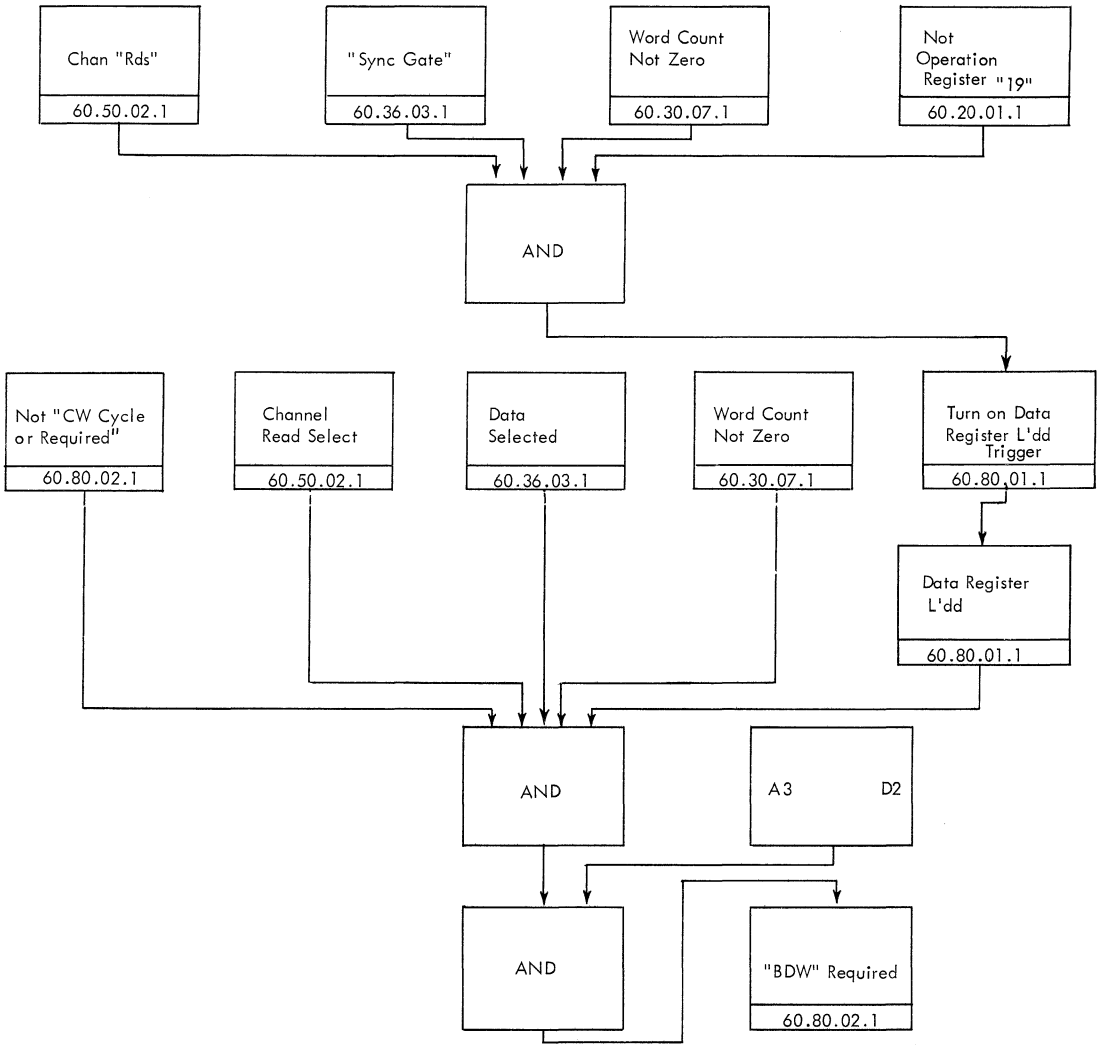

FIGURE 3.3-1. "BDW" REQUIRED WHILE READING

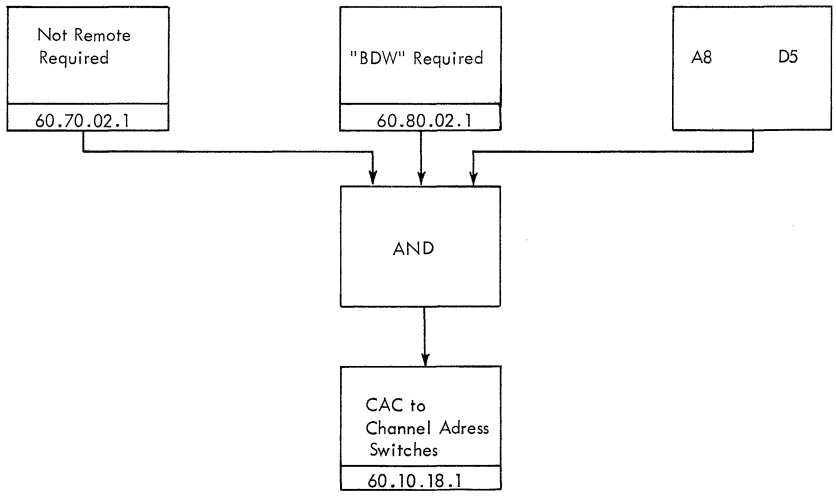

FIGURE 3.3-2. CHANNEL ADDRESS COUNTER TO CHANNEL ADDRESS SWITCHES

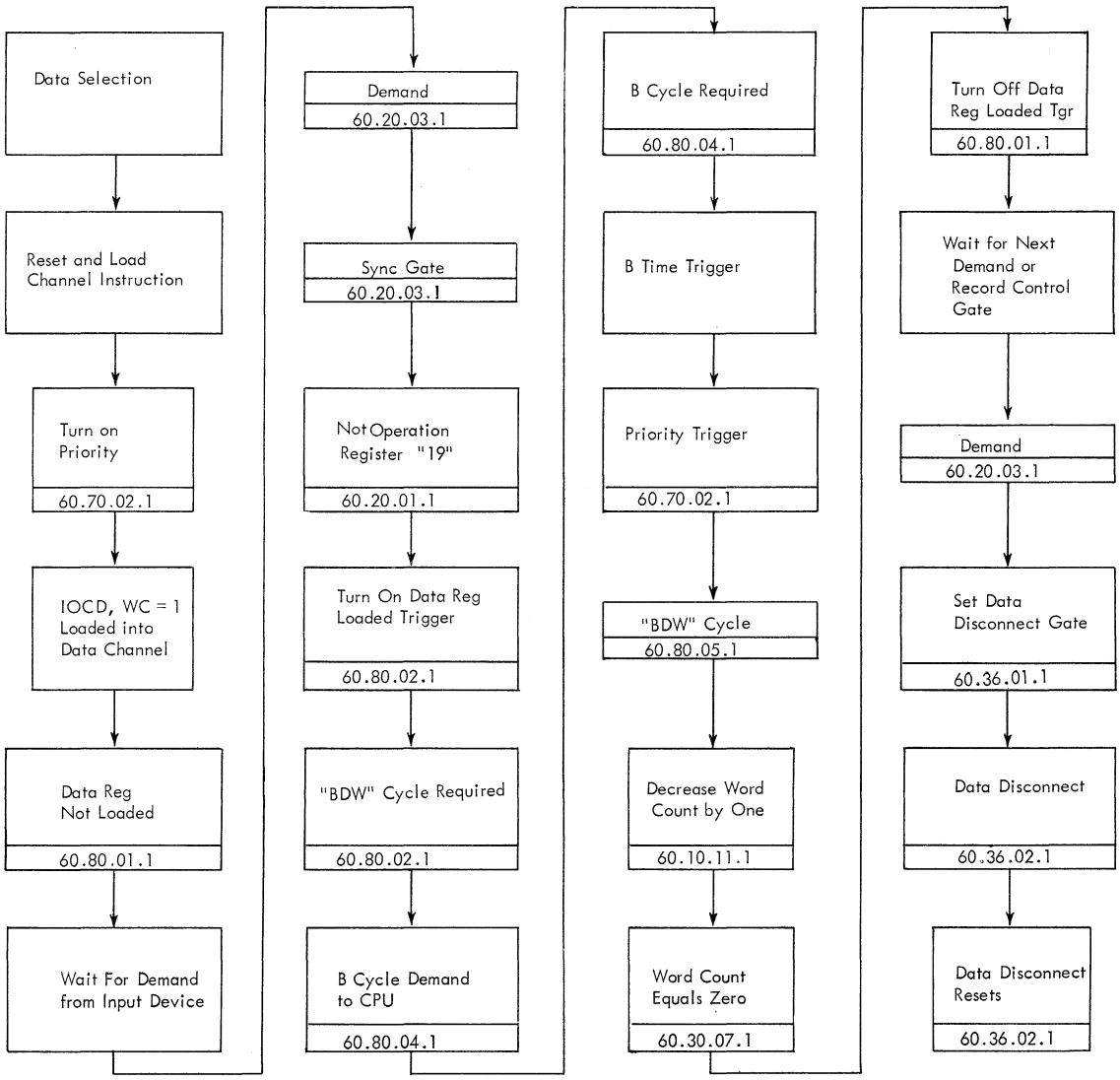

FIGURE 3.3-3. READING WITH AN IOCD COMMAND, WORD COUNT OF 1

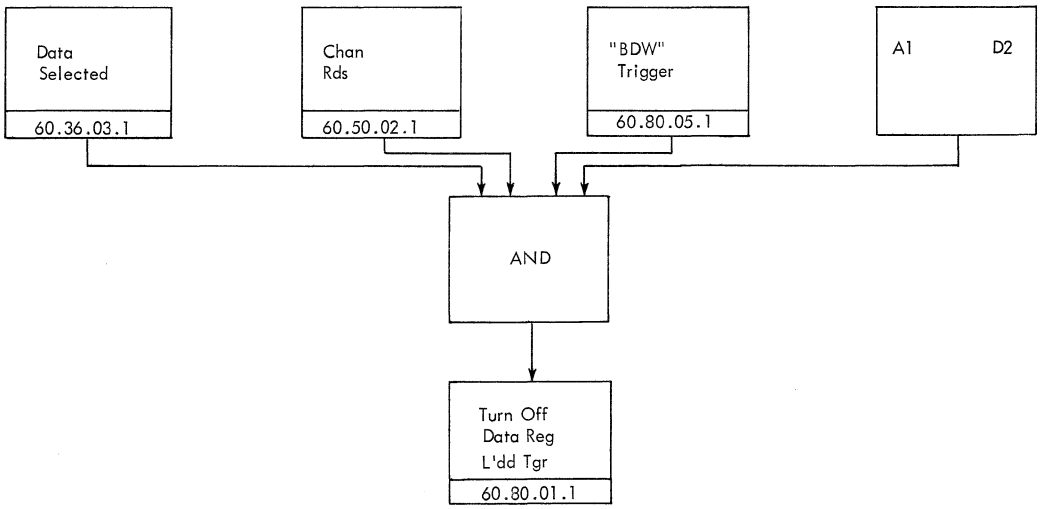

FIGURE 3.3-4. TURN OFF DATA REGISTER LOADED TRIGGER WHILE READING

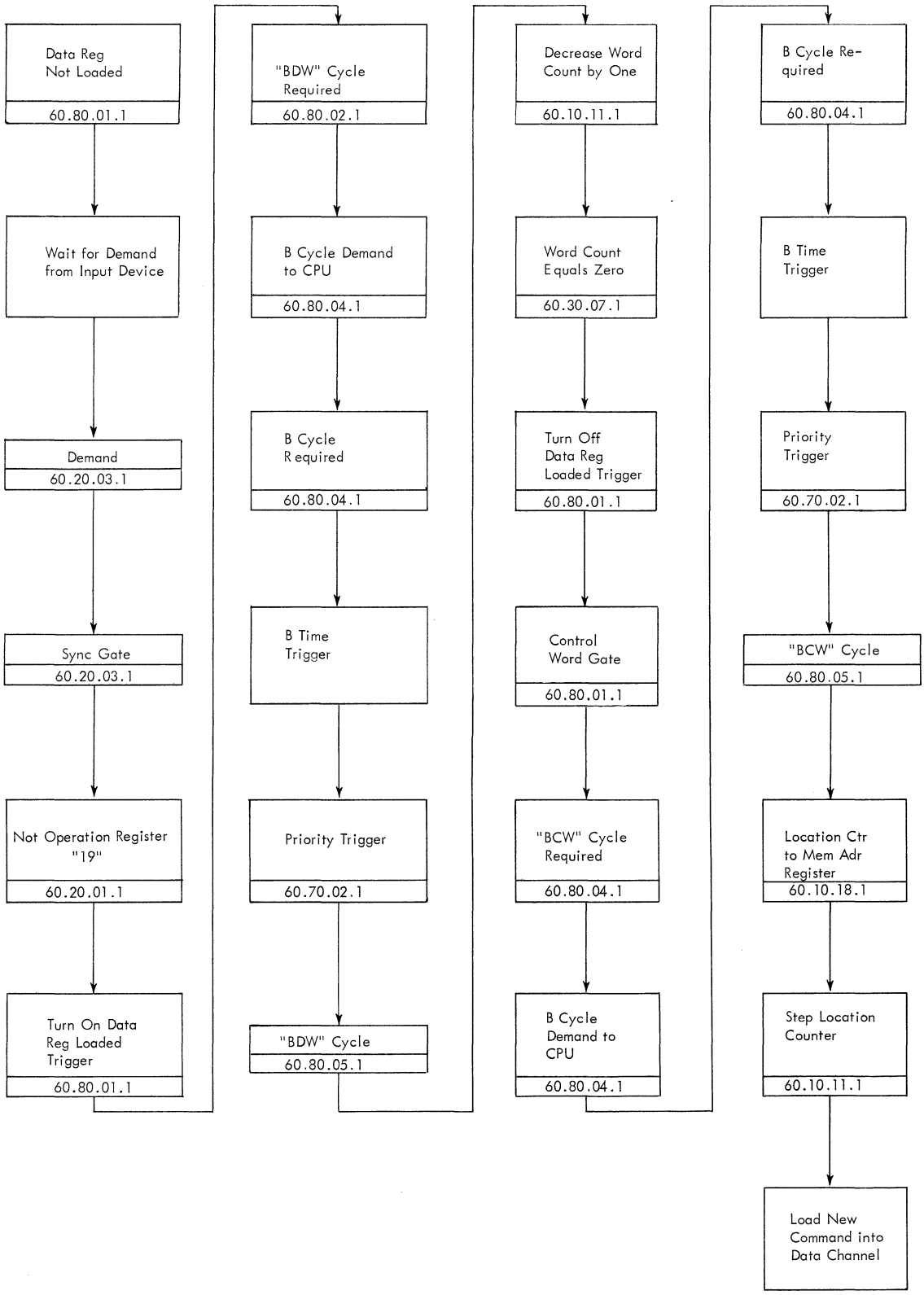

FIGURE 3.3-5. READING WITH AN IOCP COMMAND

3.3.04 Input/Output Count and Transfer (IOCT)

Transfer control to the CPU program when using the IOCT command is identical on both read and write operations (Figure 3.2-10). While the data channel is reading, the "control word gate" is developed during the "BDW" cycle, in which the word count is reduced to 0. The cycle following this "BDW" cycle is the E cycle of the load channel instruction if this instruction is waiting in L time (Figure 3.3-7). If load channel is not waiting in L time, a "load channel mode disconnect" takes place (data disconnect). Notice the similarity between the IOCP and IOCT commands.

3.3.05 Input/Output Record and Transfer (IORT)

The IORT command does not transfer control to the CPU program until the "record control pulse" is developed. Notice in Figure 3.3-8 the "record control pulse" is active when reading from the printer. As with all transfer type commands, the load channel instruction must be waiting in L time. The operation from the development of the "record control pulse" is identical on both read and write operations (Figure 3.2-13).

3.3.06 Signal Type Commands

The signal type commands (IOSP, IOST) employ the same circuitry used during the operations of IOCP, IORP, and IOCT, IORT, respectively. "Proceed control" or "transfer control" is activated when either the word count is reduced to 0 or a "record control pulse" is developed.

3.3.07 Input/Output Check While Reading

Figure 3.3-9 shows that a data channel will I/O-check if the data register is still loaded, at the time the next "demand" is received by the data channel. The I/O check data-disconnects the data channel and sets the I/O check trigger at the CPU. This trigger may be tested by the programmer with the I/O check test instruction.

3.4.00 MANUAL

Several operations may be performed from the data channel console when in the manual status. These operations include data selection, non-data selection, and load, display, and store operations. Figure 3.4-1 shows the 7617 Data Channel Console.

3.4.01 Data and Non-Data Selection

Each data channel console has nine keys associated with data and non-data selects.

Data Select Keys

Of the nine keys associated with data and non-data selects, five perform data select functions. These keys are: write printer, write punch, write tape, read cards, and read tape. When depressed, these keys initiate read or write operations. It is important to note that a command must be loaded prior to depressing any data select key (timing condition). When data-selecting tape, the tape unit is specified by the "unit select switch" located on the data channel console.

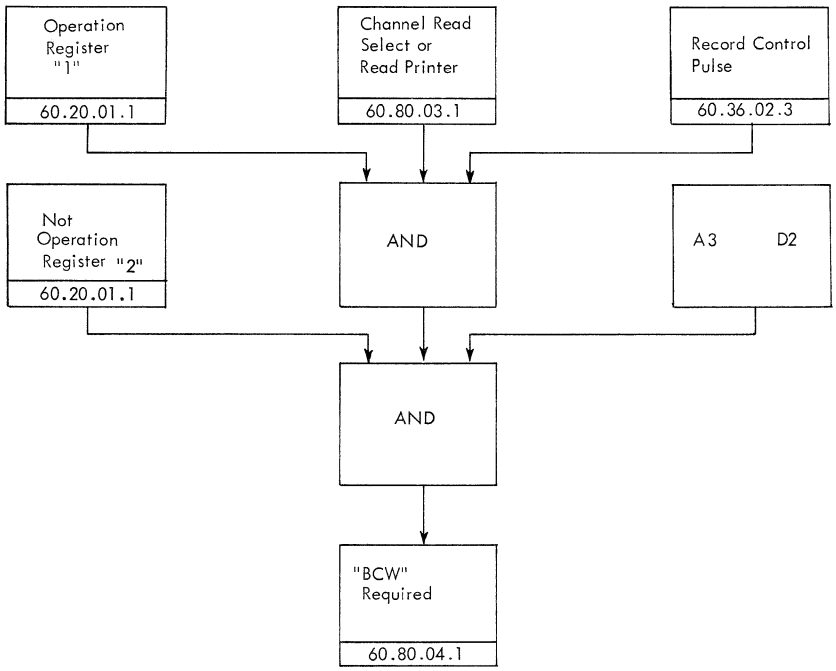

FIGURE 3.3-6. "BCW" REQUIRED WHILE READING WITH AN IORP, COMMAND

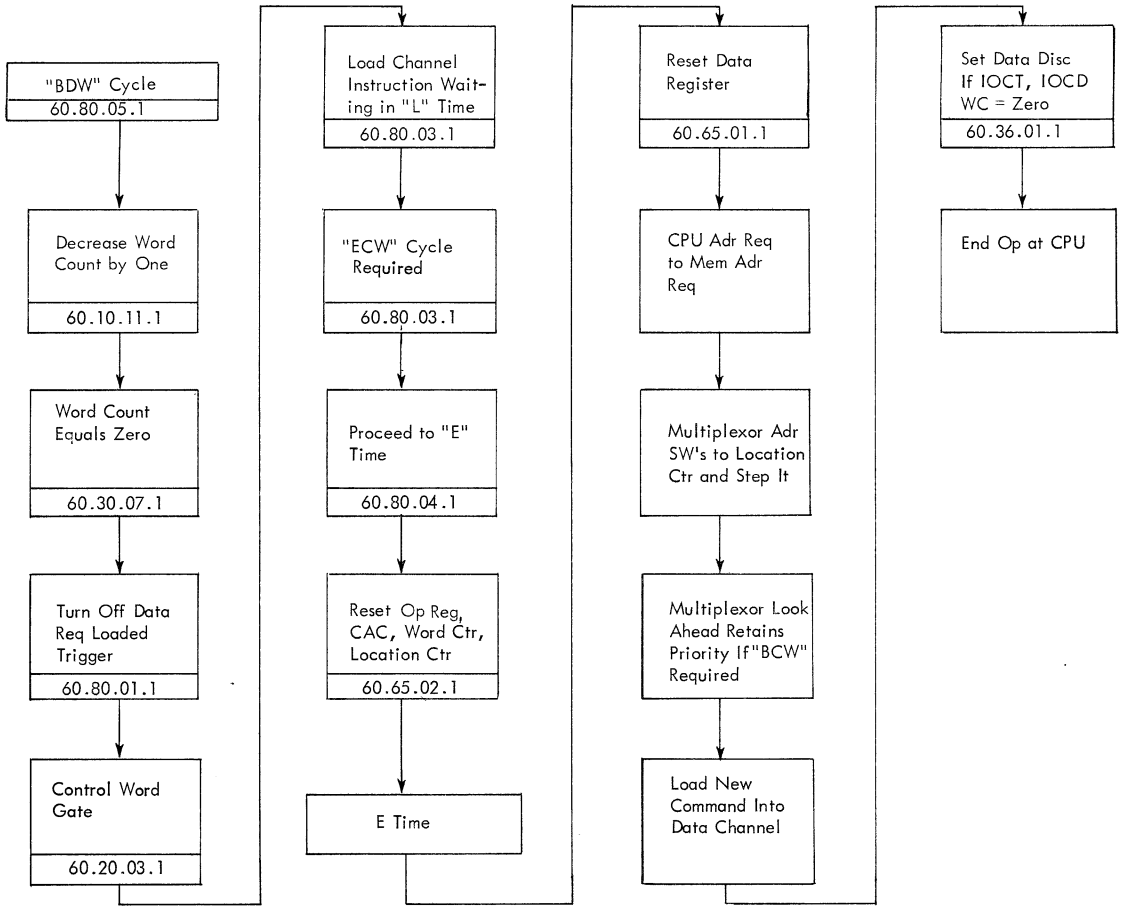

FIGURE 3.3-7. READING WITH AN IOCT COMMAND

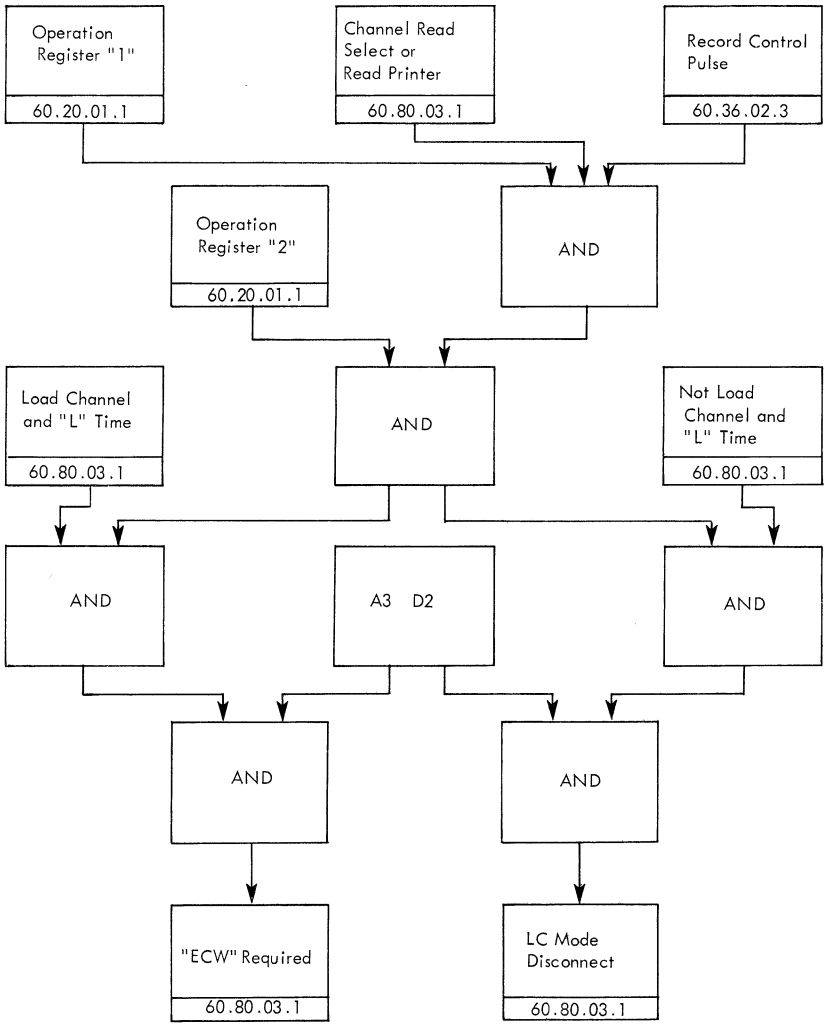

FIGURE 3.3-8. "ECW" REQUIRED WHILE READING WITH AN FORT COMMAND

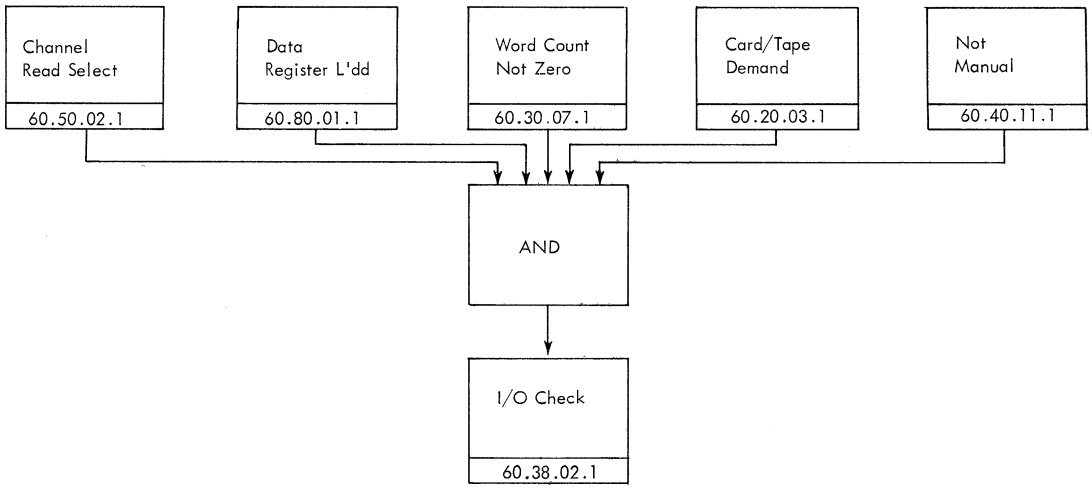

FIGURE 3.3-9. I/O CHECK WHILE READING

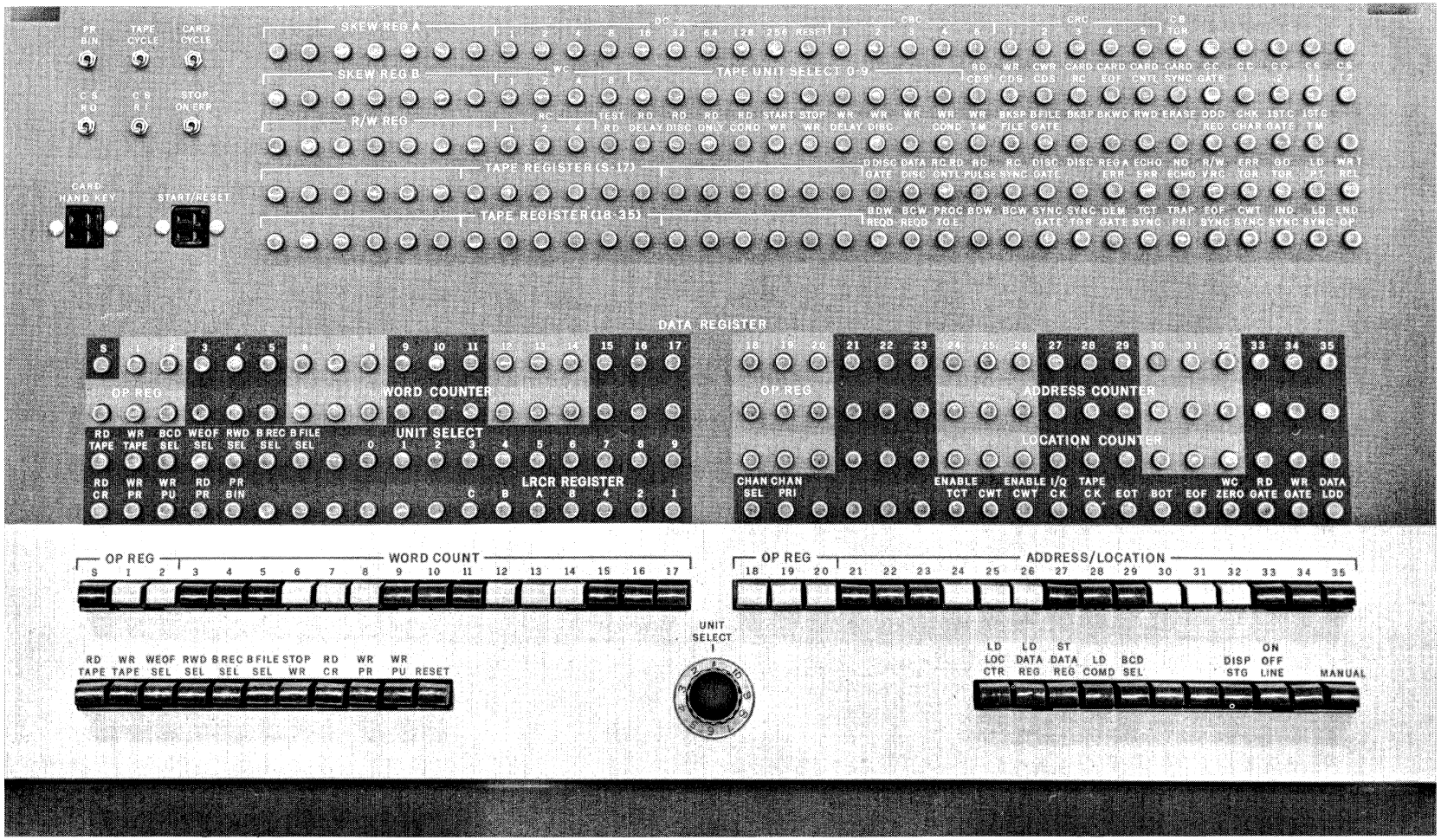

FIGURE 3.4-1. IBM 7617 DATA CHANNEL CONSOLE

Non-Data Select Keys

There are four non-data select instructions available to the programmer and each of these instructions may be performed from the data channel console. The four keys for the respective non-data selects are: backspace record, backspace file, write end-of-file, and rewind. When depressed, the respective non-data select is performed on the tape unit specified by the "unit select switch."

3.4.02 Load Operations

There are three load operations thay may be performed from the data channel console. These are: load data register, load command, and load location counter.

Load Data Register

This operation loads the contents of the entry keys S, 1-35 into the data register. This operation does not require B time. The entry keys are gated through the channel input switches (Figure 2.1-1) by a pulse that is developed when the load data register key is depressed.

Load Command

When depressed, the load command key loads the contents of the entry keys into the following registers:

Register	Entry Keys
Indicator	S, 1, 2, and 19
Word Counter	3-17
Channel Address Counter	21-35

This operation does not require B time and should precede the data-selection of any device while in the manual status. The entry keys are gated through the channel input switches, and then gated into the respective registers. It is important to note that whenever data are gated through the channel input switches, the data automatically sets respective positions of the data register. Therefore, during the time a command is being loaded into the respective registers, the data register is held reset. If a load data register operation precedes a load command operation, the data being held in the data register are reset out.

Indirectly addressed commands cannot be loaded when in the manual status, because operation register position 18 circuitry must be shared by all channels. The same holds true for a transfer in channel command (TCH).

Load Location Counter

Entry keys 21-35 are gated through the location counter switches and set respective positions of the location counter when the load location counter key is depressed (Figure 2.1-1). This operation does not require B time and the location counter is not stepped.

3.4.03 Display Storage

This operation displays, in the data register, the contents of an address in core storage specified by the channel address counter. B time is required (normal "BDW" controls). The word counter and channel address counter are stepped (Figure 3.1-1). Stepping the channel address counter facilitates sequential display operations by merely depressing the display storage key successively.

3.4.04 Store Data Register

Depressing the store data register key stores the contents of the data register at an address in core storage specified by the channel address counter. B time is required (normal "BDW" controls). The word counter and channel address counter are stepped during the "BDW" cycle. Stepping the channel address counter facilitates sequential store operations by merely depressing the store data register key successively.

3.4.05 Customer Engineer Test Operations

There are several test operations that may be initiated by the customer engineer. These are:

1. Continuous storage read-in
2. Continuous storage read-out
3. Print binary
4. Sample and drive pulse generator functions
5. On/off line functions
6. Tape cycle
7. Stop on error
8. Stop write

Continuous Storage Read-in

The continuous storage read-in feature allows repetitious transmission of a word in the data register to an address in core storage specified by the channel address counter. Requests for a "BDW" cycle occur every fourth core storage cycle. The word counter and channel address counter are only stepped when the data channel is in automatic (not manual) status. If the data channel is in automatic status, the transmission takes place until the word count is reduced to 0 and the contents of the data register are stored at sequential addresses in core storage.

From the standpoint of a customer engineer, this feature is excellent for scoping the B time circuits, priority circuits, and the individual storage bus lines. This feature was designed to be used on one data channel at a time. The interlocking between this feature and the CPU is such that difficulty may arise in trying to start a CPU program.

Continuous Storage Read-out

The continuous storage read-out feature allows repetitious transmission of a word in core storage to the data register. The address of the word is specified by the channel address counter. A request for transmission is developed every fourth core stor-

age cycle. The stepping of the word counter and channel address counter is the same as for a continuous storage read-in operation; that is, they step during the "BDW" cycle only if the data channel is in automatic (not manual) status.

Print Binary

The print binary switch, located on the data channel console, activates circuits in the card adapter unit. These circuits allow the printer, upon depression of the write printer key, to print at one time. The logic of print binary is discussed in the Card Adapter Unit (CAU) Customer Engineering Manual of Instruction, Form 223-6842.

Sample and Drive Pulse Generator Functions

There is a card cycle switch associated with the sample and drive pulse generator and it is located on the data channel console. This switch activates the circuits in the card adapter unit. It allows for the operation of the sample and drive pulse generator at low speeds. This allows visual checking of its operation. The logic performed by this switch is discussed in the Card Adapter Unit (CAU) Customer Engineering Manual of Instruction, Form 223-6842.

On/Off Line Operation

The on or off line switch differentiates as to whether normal manual operations (B time occurs) are performed or whether the manual operations are limited to the channel controls.

On Line. With the switch in the on line position, the manual operations performed from the data channel console are interlocked with the CPU. This means that read and write operations are under control of the present command. Normal B time circuitry is active and data transmission is the same as when in the automatic status.

Off Line. With the switch in the off line position, the manual operations performed from the data channel console do not include normal CPU interlocking. The present command does not control data transmission. A word must be loaded into the data register prior to initiating a write operation. This word is written on tape until the stop write key is depressed.

During read operations, the characters on tape form a word in the tape register (six characters). This word is transmitted to the data register. This sequence continues until an end-of-record gap is sensed, or an end-of-file is read.

The off line switch also activates the following switches: the cyclic, stop on error, and stop write switches.

Tape Cycle

When in the tape cyclic mode, a series of one-word records may be written on the tape unit specified by the unit select switch. The word to be written is loaded into the data register. The tape cycle switch is set, and the write cyclic operation is then initiated by depressing the write tape key.

In the process of writing the one-word records, the contents of the data register are gated to the tape register. From the tape register, the word is written on tape in a series of six characters, and then an end-of-record gap is recorded. During the time the end-of-record gap is being recorded, the operation is automatically restarted. The on/off line switch must be in the off line position if the tape cycle switch is to be effective.

Records may be read in the tape cyclic mode also. With the tape cycle switch active, the read tape key is depressed. Each character on tape is read and set to the respective positions of the tape register (under control of the group counter). After the sixth character is gated to the tape register (full word now being held in the tape register), its contents are gated to the data register.

This process continues until and end-of-file is read. The sensing of an end-of-file automatically rewinds the tape. The read cyclic operation automatically continues after the tape rewinds to the load point.

Stop on Error

The stop on error key is only effective when in the tape cyclic mode. If a character is written incorrectly, it is sensed as an error by the redundancy checking circuits which are located in the tape adapter unit. The error condition stops the write operation if the stop on error key is active.

When reading in the tape cycle mode, an error condition stops the read operations, but the tape positions itself to the beginning of the next record.

Error conditions on read and write operations are discussed in the Tape Adapter Unit (TAU) Customer Engineering Manual of Instruction, Form 223-6847.

Stop Write

The stop write key is used to stop a tape write operation. It is not effective unless the channel is in the manual status. When depressed, the tape write operation is terminated after completing the present record.

Notice that one-word records are written when in the tape cycle mode.

4.0.00 DATA CHANNEL TRAP

A PROGRAM TO keep eight input/output operations operating simultaneously would be very complex, not to mention the compute time. The 7090 incorporates data channel trap to minimize the complexity of input/output monitors. The result is efficient operation of up to eight data channels on a 7090.

4.1.00 SIGNAL TO CPU

The data channel trap feature allows respective data channels to signal the CPU to initiate a trapping operation. The data channel trap may be initiated by transfer type commands if the load channel instruction is not writing in L time (not TCH), an end of file, or a redundancy check.

When a trap occurs, the present contents of the instruction counter is stored in the address field (21-35) of a fixed address in core storage. An identification code is stored in positions 15, 16, and 17 of the same address. After storing this information, the computer takes its next instruction from a fixed address. The following list shows the allocation of addresses per channel.

Channel	Identification Code in 15, 16, 17, of:	Instruction Ctr in 21-35 of:	Next Instruction from:
A	12	12	13
B	14	14	15
C	16	16	17
D	20	20	21
E	22	22	23
F	24	24	25
G	26	26	27
H	30	30	31

Notice that the stored information is at the even addresses starting with 12 octal. The next instruction is always taken from an odd address starting with 13 octal.

4.1.01 To Subroutine

If the programmer wishes to investigate why the trap occurred, the first instruction after the execution of the trap (located at the odd addresses, 13 octal through 31 octal) must be: an unconditional transfer instruction, which transfers to a subroutine or an execute instruction which, in turn, executes an unconditional transfer instruction.

If these instructions are not provided by the programmer, the instruction located at the odd addresses is executed, and then the main program continues from where it was interrupted (value of instruction counter at the time of the trap). This is because the instruction counter was not altered by the trap.

4.1.02 Identification Code

As stated previously, an identification code is stored in the decrement field of the address to which the data channel traps (even addresses, 12 octal to 30 octal). The identification code indicates in what status the three "trap indicators" were at the time of the trap. Positions 15, 16, and 17 form the identification code. The following list shows the significance of these positions:

Identification Code	Status
15 = 1	End-of-file trap indicator was on.
16 = 1	Redundancy check trap indicator was on.
17 = 1	Command word trap indicator was on.

4.2.00 INSTRUCTIONS

Along with the data channel trap feature come two new instructions: enable (ENB) and restore channel traps (RCT). These instructions give the programmer the flexibility of specifying which channel trap signals are to be effective and the control as to when remembered trap signals are processed.

4.2.01 Enable (564---Y)

When this instruction is executed, the contents of the address specified by 21-35 of the instruction determine which channel trap signals can cause traps to occur (Figure 4.2-1). The channel trap indicators are enabled by the enable instruction, as shown.

Command-word trap indicators and end-of-file trap indicators in the respective channels are enabled by 1's contained in the address field of the operand specified by the enable instruction.

Data Channel	Operand Position
A	35
B	34
C	33
D	32
E	31
F	30
G	29
H	28

The redundancy check trap indicators in the respective channels are enabled by 1's contained in the decrement field of the operand, specified by the enable instruction.

Data Channel	Operand Position
A	17
B	16
C	15
D	14
E	13
F	12
G	11
H	10

The execution of each enable instruction cancels the effect of the previous enable instruction. Therefore, all channels may be disabled (traps not permitted to occur) by giving an enable instruction whose operand is all 0's. Pressing the reset or clear keys also disables all channels.

The execution of a channel trap inhibits further trap signals from being processing until: the enable instruction or the restore channel traps instruction is given.

4.2.02 Restore Channel Traps (760---14)

The execution of a restore channel traps instruction allows channel traps to occur as specified by the previous enable instruction. If a trapping signal is generated while a data channel is disabled or inhibited, the trap signal is remembered until the data channel is restored. As stated previously, the execution of an enable instruction or a restore channel traps instruction restores all channels (Figure 4.2-2).

4.3.00 PROGRAM CONTROL

The instruction following enable, restore channel traps, read select, or write select, always is executed prior to processing a trap signal. In the case of enable and restore channel traps, it allows the execution of an unconditional transfer instruction to take the 7607 out of the trapping subroutine. This could also be an execute to an unconditional transfer instruction. The main purpose here is to allow the return to the main program prior to processing another channel trap.

The instruction following a read or write select is usually reset and load channel. If provisions were not made to allow its execution, the possibility exists that the CPU could enter a trapping subroutine during the I cycle following the read or write select instruction. If this did occur, chances are that the CPU would not exit from the subroutine and execute the reset and load channel instruction within specified time limits.

4.3.01 Remembered Trap Signals

Channel trap signals that occur when a channel is disabled or inhibited are remembered in one of the trap indicators. The execution of certain instructions when a channel is disabled causes the remembered trap signal to be lost. These instructions and their effects follow:

Instruction	Trap Indicator
1. Read or write selection of corresponding channel	Command trap indicator is turned off.
2. Transfer on end-of-file instruction for corresponding channel	End-of-file trap indicator is turned off.
3. Transfer on redundancy check instruction for corresponding channel.	Redundancy check trap indicator is turned off.

These indicators are also turned off whenever a channel trap occurs as a result of their being on.

The execution of the transfer on end-of-file and transfer on redundancy check instructions acts as though the respective indicator is off if the respective channel is enabled. It is important that all trap signals data-disconnect the respective data channel if they are enabled.

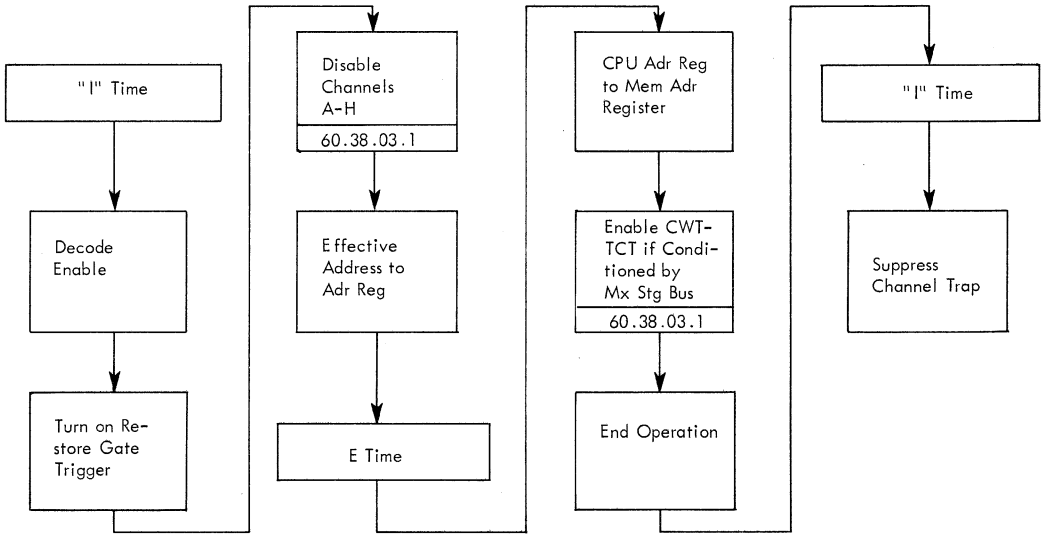

FIGURE 4.2-1. ENABLE

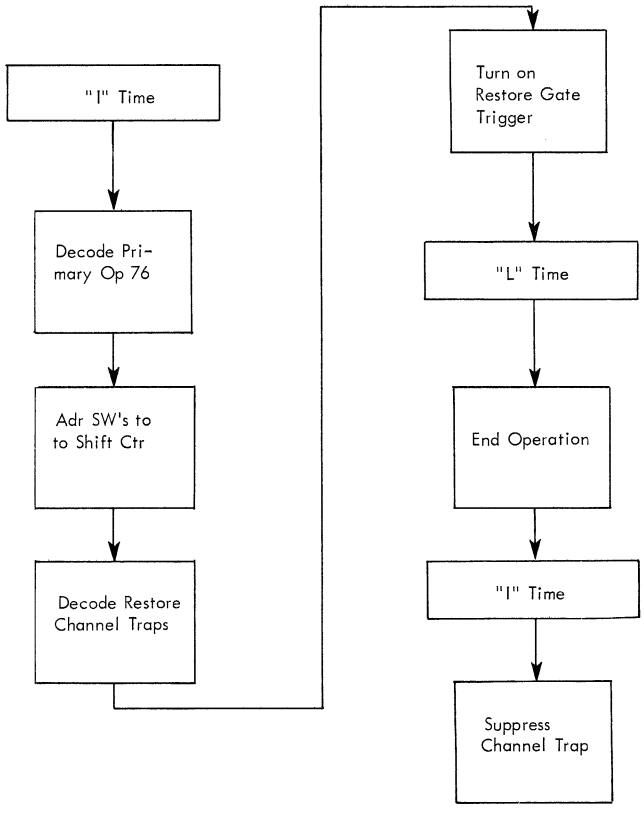

FIGURE 4.2-2. RESTORE CHANNEL TRAPS

4.3.02 Trap Signals Subsequent to Halt Operations

If a trap request is called for, subsequent to certain halt operations, one of three procedures occurs.

Halt and Transfer. The trap is performed and the CPU resumes the execution of instructions. At the time the trap signal is processed, the instruction counter contains the address of the halt and transfer instruction.

Halt and Proceed. The procedure is the same for halt and transfer; however, at the time the trap signal is processed, the instruction counter contains the address of the halt and proceed instruction plus one.

Divide or Halt. The procedure is the same as halt and proceed, assuming the halt occurred as a result of a divide check.

A trap signal is normally processed at the completion of the instruction's being executed (normally I time). If a trap is called for while the CPU is in manual status, the trap is not processed until the CPU is put in automatic status and the start key is depressed.

4.4.00 TRAP PRIORITY

There is a possibility that all eight data channels on a 7090 might signal for a trap simultaneously. Because of this possibility, the data channel incorporates trap priority circuits. The priority circuits give priority to the most remote data channel that asks for it. The most remote data channel is the last physical channel on that bank, predetermined by multiplexor cabling (Figure 4.4-1). Once a data channel has trap priority (Figure 4.4-2) a demand is sent to the CPU (Figure 4.4-2).

The control and flow of a trapping operation because of a "load channel mode" disconnect is shown in Figure 4.4-3).

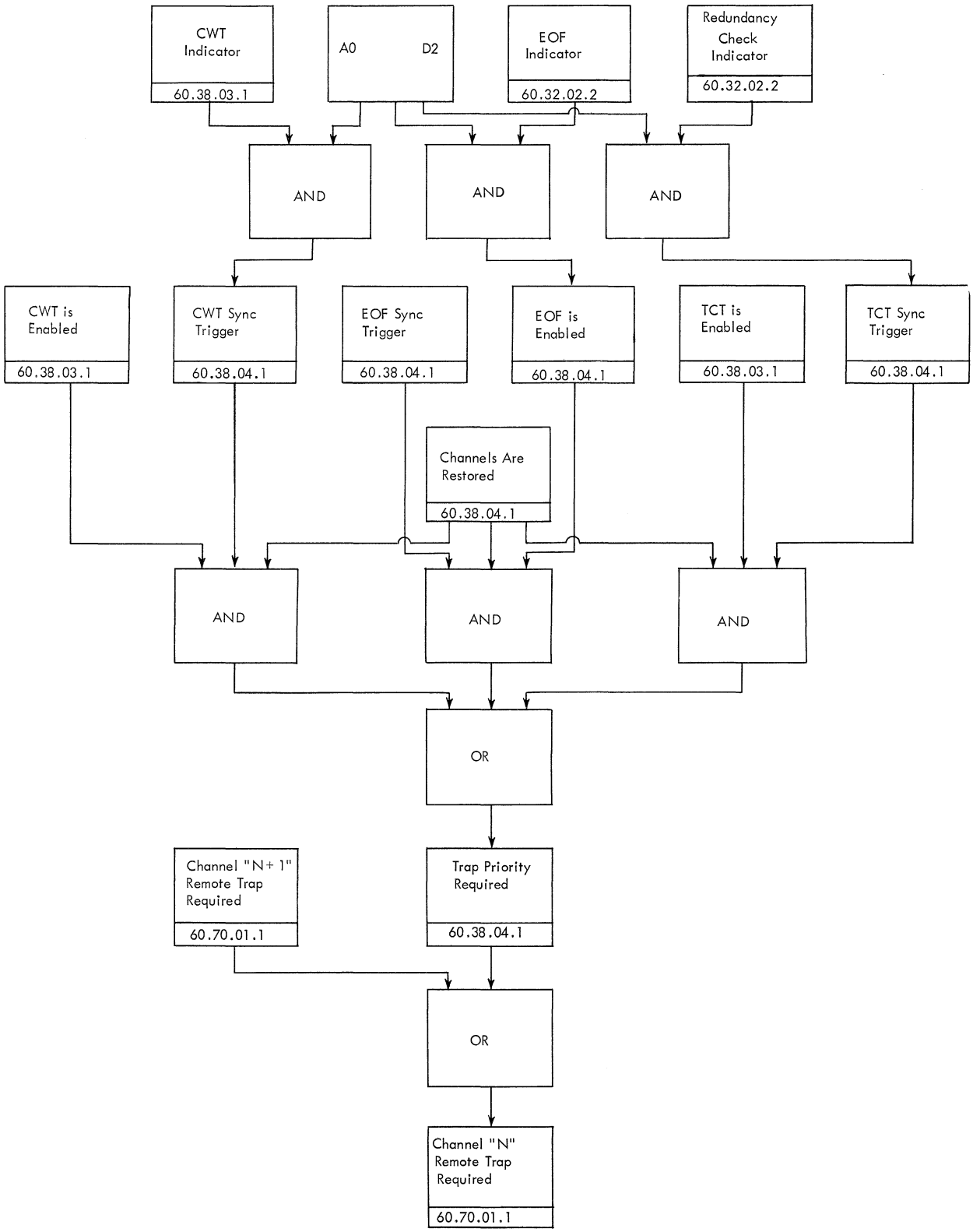

FIGURE 4.4-1. CHANNEL TRAP PRIORITY REQUIRED

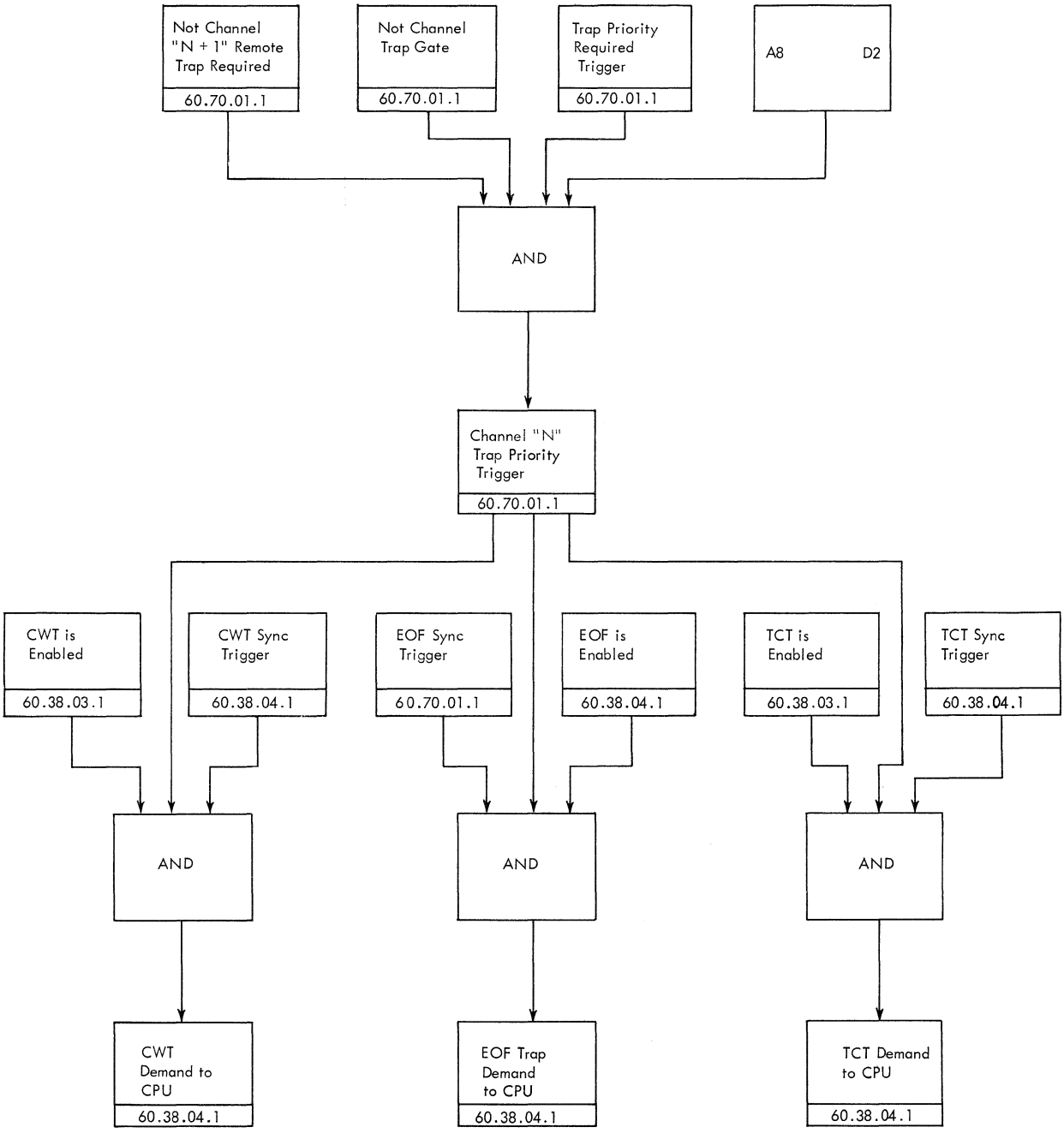

FIGURE 4.4-2. TRAP PRIORITY AND TRAP DEMANDS

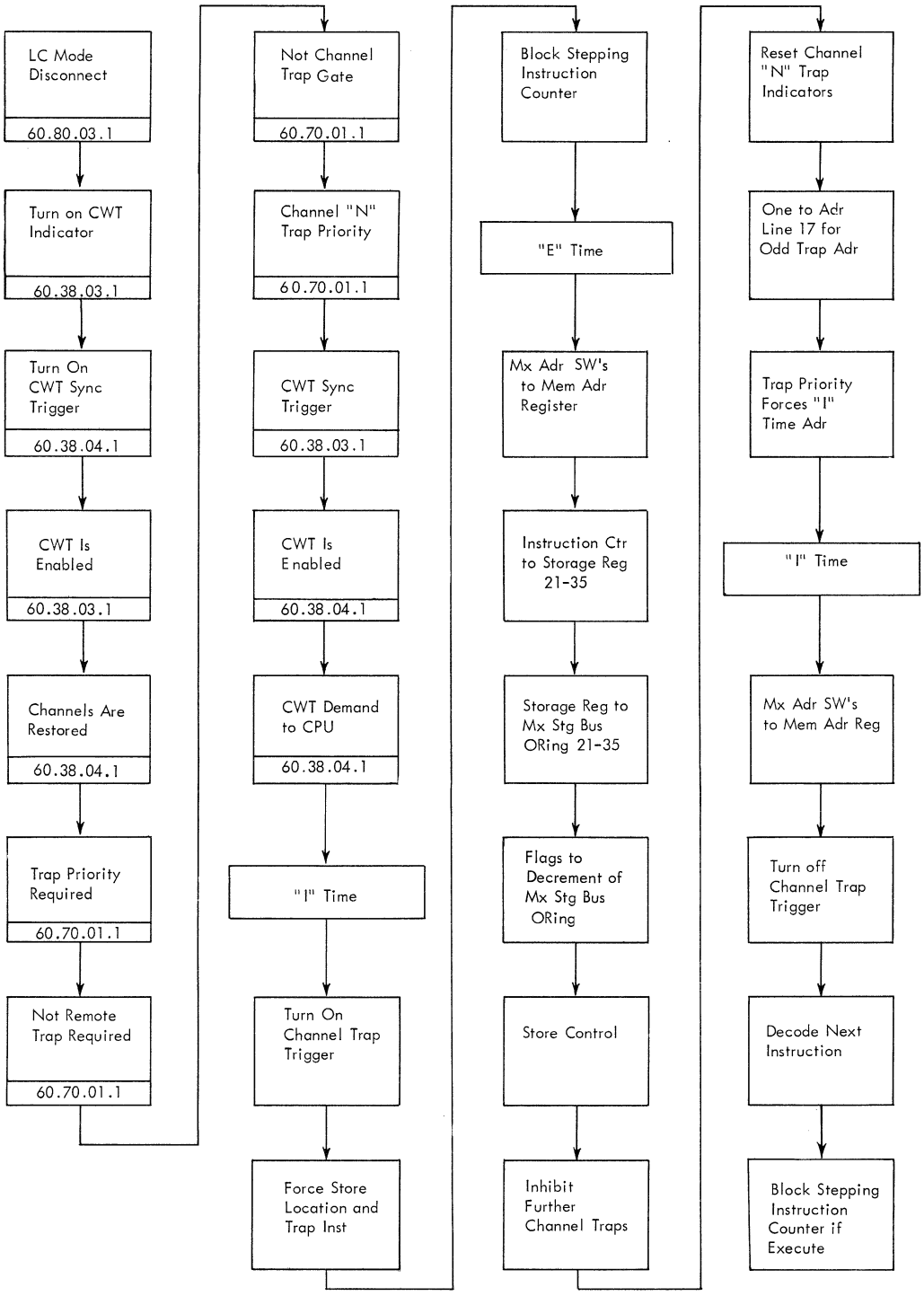

FIGURE 4.4-3. COMMAND WORD TRAP

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International Business Machines Corporation
Data Processing Division, 112 East Post Road, White Plains, N.Y.