IBM Customer Engineering

Manual of Instruction

7606 Multiplexor

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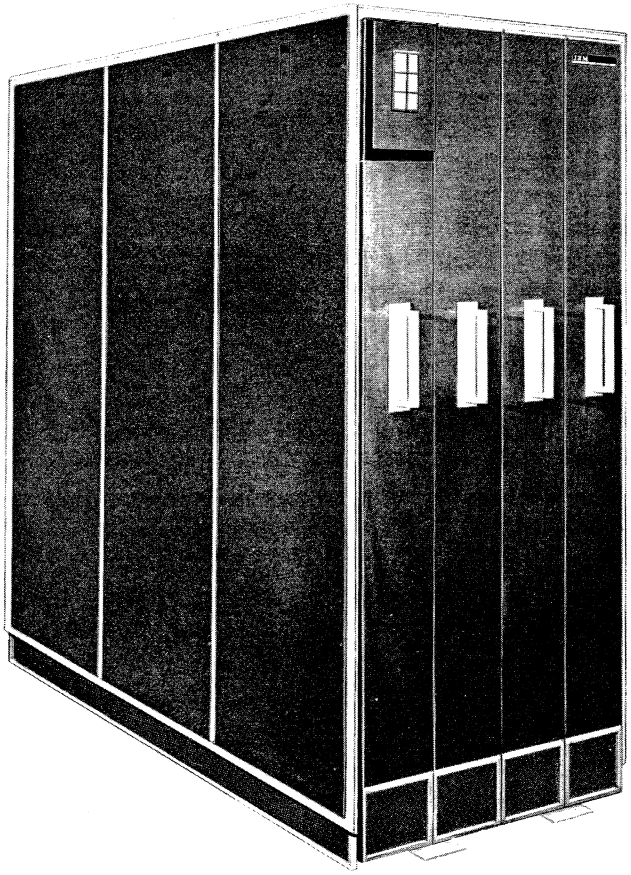


IBM 7606 MULTIPLEXOR

1.0.00 GENERAL INFORMATION

1.1.00 INTRODUCTION

The IBM 7606 Multiplexor is best described as the unit of the 7090 system that passes all data to or from core storage. These data may be CPU instructions, data channel commands, data to be processed by the CPU, data that has been processed by the CPU, or input-output words. Data that go to core storage come to the multiplexor from the CPU and data channels.

Multiplexing is the forming of a serial path from parallel paths when data are going to core storage. When data are coming from core storage, multiplexing is the forming of parallel paths from a serial path. Multiplexing, then, allows the transmission of two or more independent signals on the same circuit.

In addition to its function of multiplexing, the multiplexor contains the clock for the CPU and data channels, and a matrix for zero testing data coming from core storage. The multiplexor also contains look-ahead circuits that are used in conjunction with the data channel operations.

Two of the four standard modular system (SMS) sliding gates in the multiplexor frame are reserved for special features. The remaining two SMS sliding gates house the multiplexor circuitry.

1.2.00 GENERAL MACHINE LOGIC

Data flow from core storage to the multiplexor storage bus, then to either the CPU or any one of the data channels. See Figure 1.2-1. The address field (21-35) of the data coming from core storage also flows to the multiplexor address switches. The flow through the multiplexor address switches is controlled by the look-ahead circuits in the multiplexor.

Data going to core storage flow through the multiplexor storage bus OR'ing. This bus is a group of OR circuits that multiplex data going to core storage. It is completely independent of the multiplexor storage bus.

The multiplexor address switches receive addresses from the CPU, data channels, and the multiplexor storage bus. These switches multiplex the address sent to core storage and the location counter switches in each data channel.

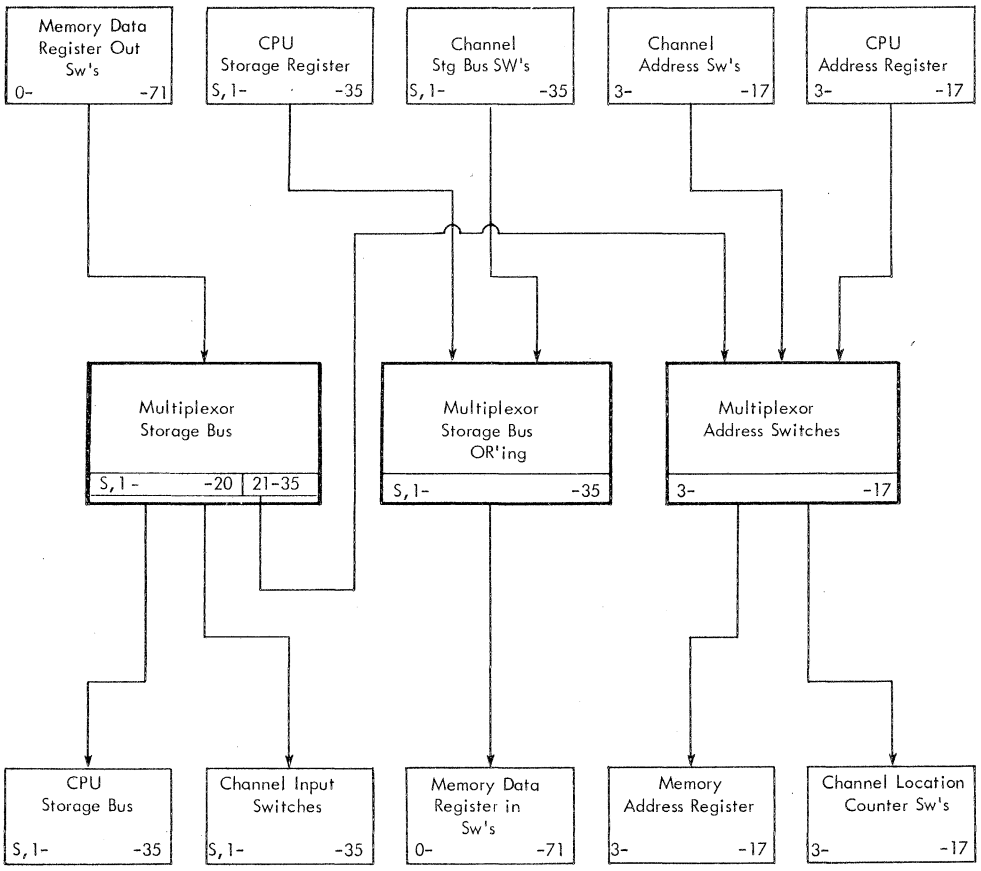


FIGURE 1.2-1. FLOW TO AND FROM THE MULTIPLEXOR

2.0.00 INTERNAL AND EXTERNAL FUNCTIONS

2.1.00 FUNCTIONAL UNITS

The multiplexor contains several groups of circuits best described as functional units. These include the multiplexor clock, storage bus, storage bus OR'ing, and the address switches.

2.1.01 Multiplexor Clock

The multiplexor clock (Figure 2.1-1) supplies timing pulses to the 7090 system. The clock consists of a 12-stage ring. The clock is started by turning on the zero clock trigger with a start clock pulse. The A0(D1) clock pulse is obtained by gating the last half of the zero clock trigger pulse with the negative portion of the even ring drive pulse. The rise of the A0(D1) pulse turns on one clock trigger. The A1(D1) pulse is obtained by gating the last half of the 1 clock trigger pulse with the negative portion of the odd ring drive pulse. The rise of the A1(D1) pulse turns on two clock trigger, and the turning on of the two clock trigger turns off zero clock trigger. This sequence continues through 11 clock trigger. The rise of the A11(D1) pulse turns zero clock trigger on again. The following chart shows the controls significant to each stage of the ring.

Clock Tgr	Turned on by	Turned off by	Duration	Output	Gated Output
0	A11(D1)	2 clock tgr	A11(D2)	A11(D2)	A0(D1)
1	A0(D1)	3 clock tgr	A0(D2)	A0(D2)	A1(D1)
2	A1(D1)	4 clock tgr	A1(D2)	A1(D2)	A2(D1)
3	A2(D1)	5 clock tgr	A2(D2)	A2(D2)	A3(D1)
4	A3(D1)	6 clock tgr	A3(D2)	A3(D2)	A4(D1)
5	A4(D1)	7 clock tgr	A4(D2)	A4(D2)	A5(D1)
6	A5(D1)	8 clock tgr	A5(D2)	A5(D2)	A6(D1)
7	A6(D1)	9 clock tgr	A6(D2)	A6(D2)	A7(D1)
8	A7(D1)	10 clock tgr	A7(D2)	A7(D2)	A8(D1)
9	A8(D1)	11 clock tgr	A8(D2)	A8(D2)	A9(D1)
10	A9(D1)	0 clock tgr	A9(D2)	A9(D2)	A10(D1)
11	A10(D1)	1 clock tgr	A10(D2)	A10(D2)	A11(D1)

Note that the pulse width of each clock trigger is twice that of an individual clock pulse. This slower switching of the clock triggers provides for increased reliability in the operation of the clock.

The multiplexor clock pulse distribution enables the individual clock pulses to be distributed to the CPU and data channels. Because of inherent delays in logic blocks, clock pulses distributed to the CPU arrive about one clock pulse late. For this reason, those clock pulses distributed from the multiplexor to the CPU are labeled one higher than the actual clock pulse. Therefore, an A0(D1) pulse going to the CPU would be labeled A1(D1). This pulse leaves the multiplexor at A0 time but, when it arrives at the CPU, the A1(D1) pulse is rising at the multiplexor. It is important to notice that

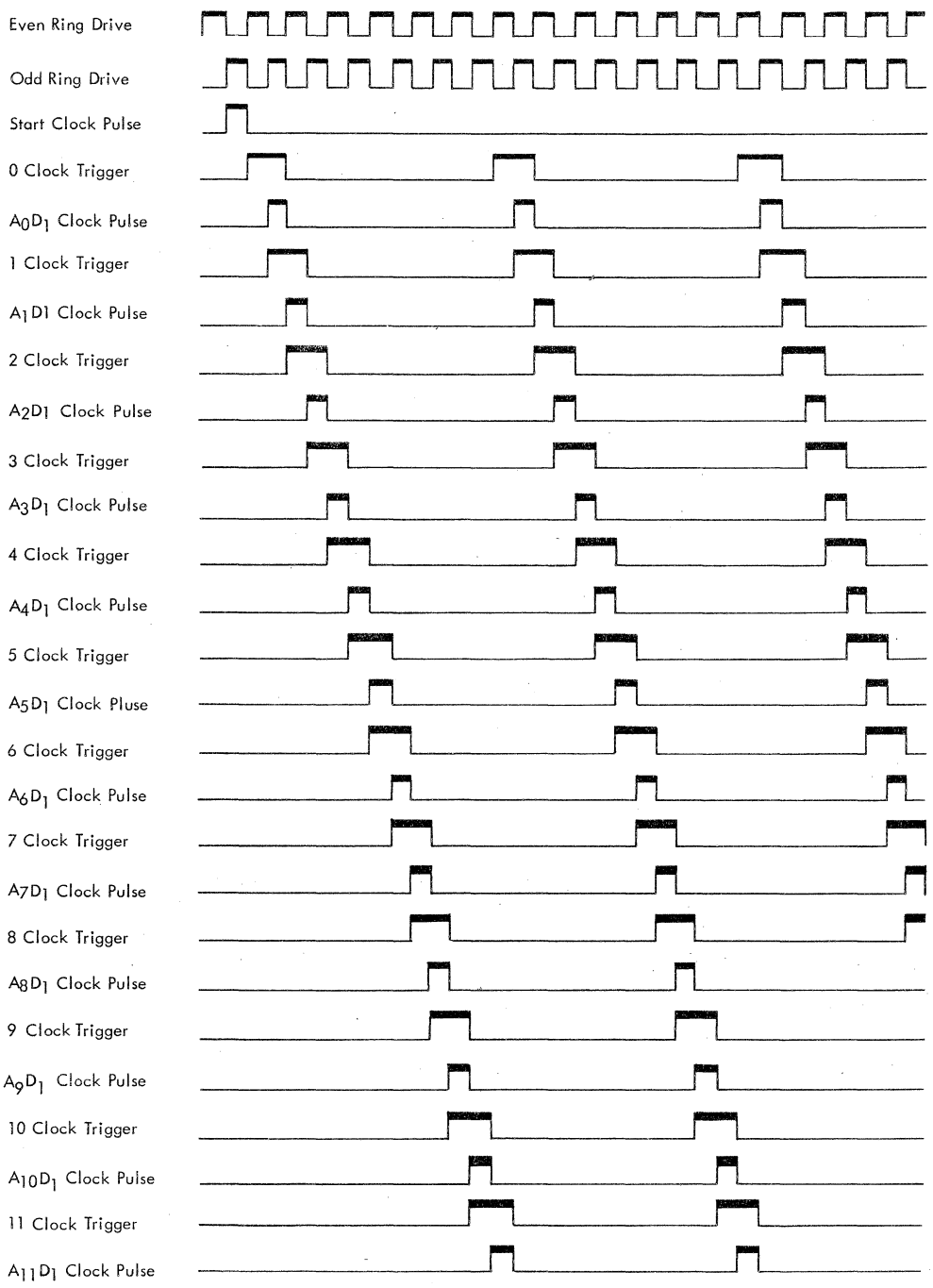


FIGURE 2.1-1. MULTIPLEXOR CLOCK

A1(D1) pulses at the CPU and multiplexor now are in coincidence, although developed from different clock triggers. This provides for continuity in the timing relationship between the CPU and multiplexor.

2.1.02 Multiplexor Storage Bus

The multiplexor storage bus (Figure 2.1-2) routes all data from core storage to either the data channels or the CPU. Seventy-two lines from core storage feed the bus, 36 of which lines carry data at a given time. Lines 0-35 are logically OR'ed with lines 36-71, respectively.

The bus feeds a group of 36 AND circuits that act as inputs to the CPU. The bus also feeds both banks of the data channel by way of the channel buses. The channel buses are logical OR circuits that provide for the proper isolation and powering of data lines. Positions 21-35 of the bus feed the multiplexor address switches. These positions are gated through the multiplexor address switches during a look-ahead address control operation. The look-ahead address control operations are explained in further detail in Section 2.3.00.

In a multiplexor storage bus test, positions 1-35 of the multiplexor storage bus feed a matrix, which tests positions 1-35 and 3-17 for a zero condition. The zero test on positions 3-17 is used in conjunction with the multiplexor look-ahead circuits. Zero testing positions 1-35 provide for minimum execution time of various CPU instructions.

2.1.03 Multiplexor Storage Bus OR'ing

All data going to core storage are routed through the multiplexor storage bus OR'ing circuits. See Figure 2.1-3. These circuits consist of OR circuits that multiplex data coming from either bank of the data channels or the CPU. Positions S, 1-35 of the CPU storage register are logically OR'ed with positions S, 1-35 of both banks of channel storage bus switches. This provides the proper isolation between the three sets of inputs to the bus, and allows for the proper matching of the output.

It is important to notice that data being routed through these circuits are gated at the CPU storage register or the channel storage bus switches.

The output of the OR circuits consists of 36 (S, 1-35) lines, powered and matched, to route data to core storage.

2.1.04 Multiplexor Address Switches

The address, where data are taken to or from, must be switched through the multiplexor address switches (Figure 2.1-4). These switches determine whether the address going to core storage is from a data channel, the CPU, the multiplexor storage bus, or is a forced address due to a channel trap. The switches also provide isolation between the various inputs. The switches have three outputs, all of which are active simultaneously. Two of the outputs feed both banks of the data channels and terminate at the location counter switches. The third output feeds the memory address register in core storage.

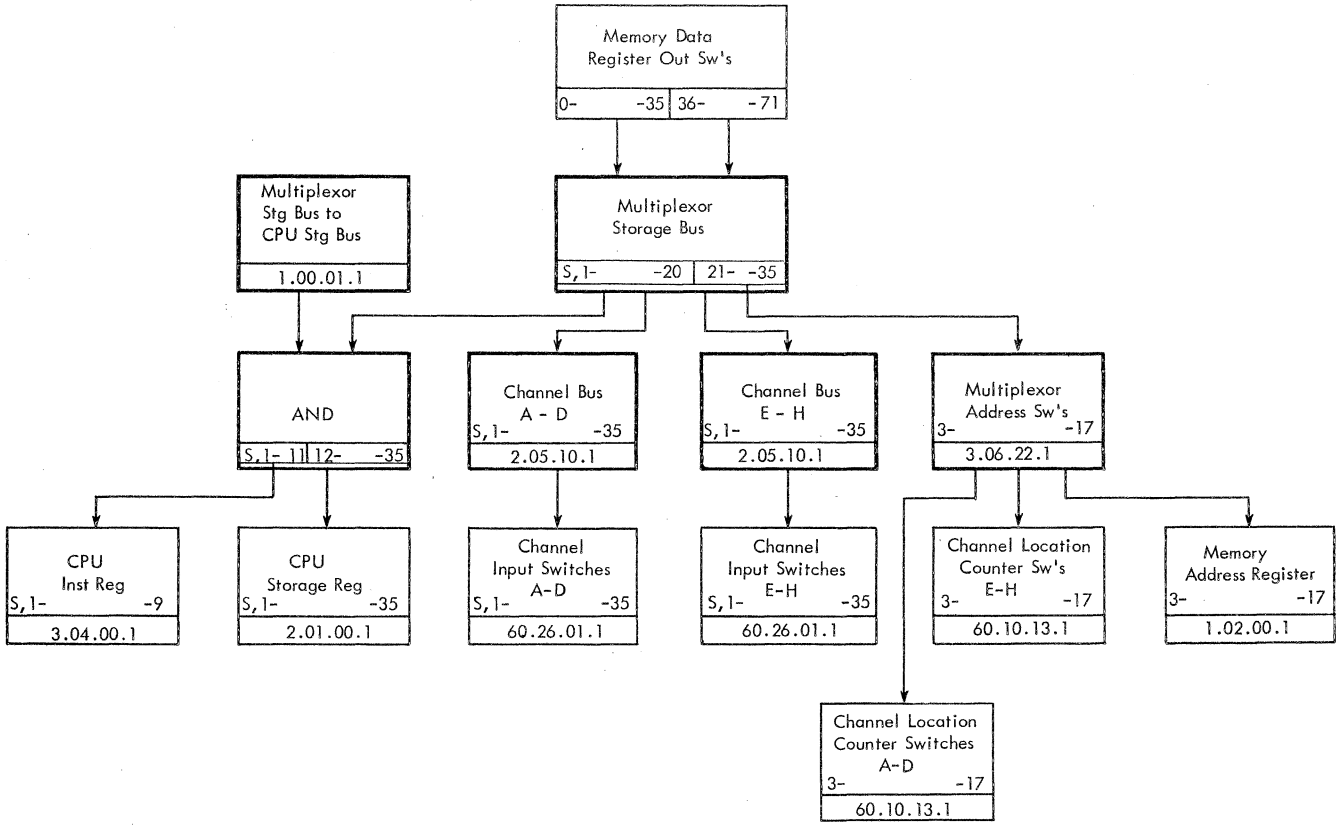


FIGURE 2.1-2. FLOW FROM MULTIPLEXOR TO CPU AND DATA CHANNELS

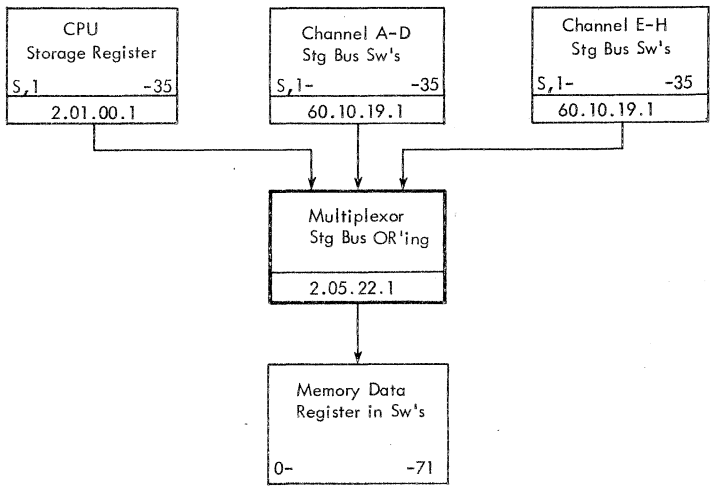


FIGURE 2.1-3. FLOW FROM CPU AND DATA CHANNELS TO MULTIPLEXOR

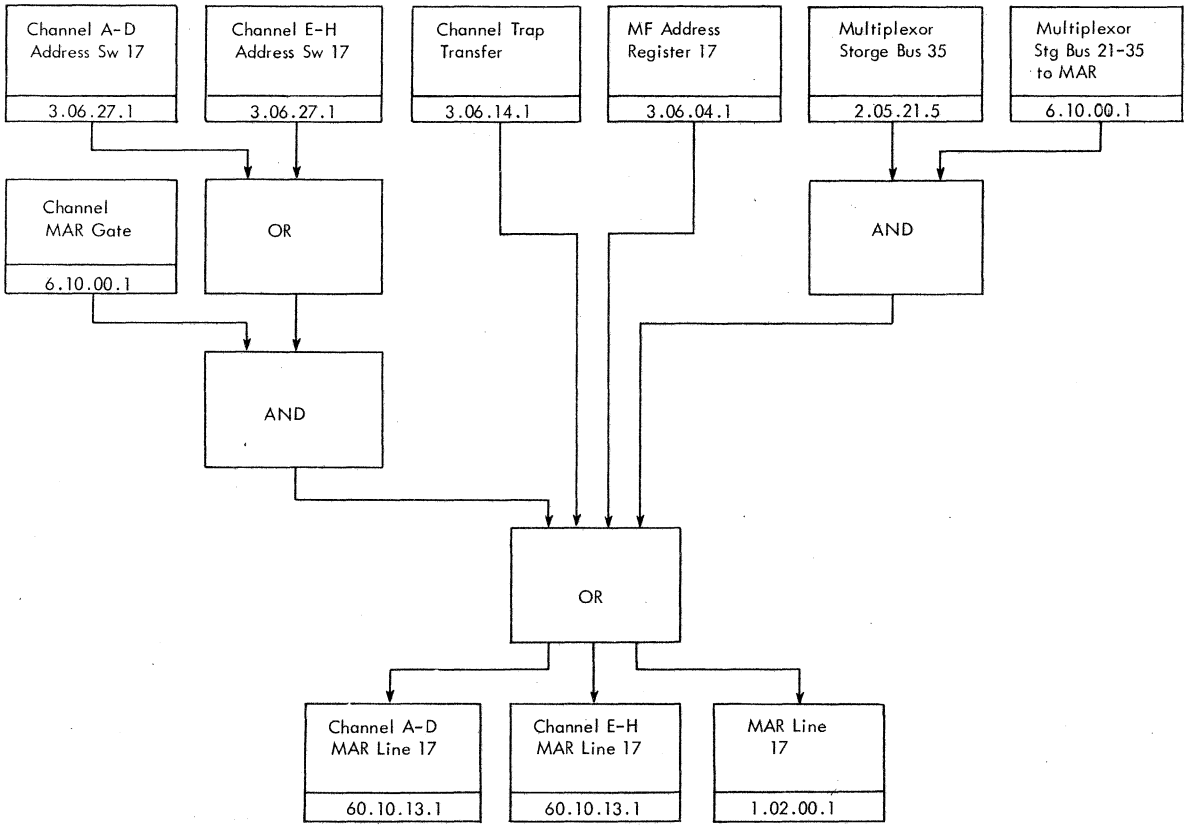


FIGURE 2.1-4. MULTIPLEXOR ADDRESS SWITCH 17

2.2.00 DATA FLOW AND CONTROL

Data flow through the multiplexor and its associated control circuitry can best be described by examining each of the following four paths:

CPU to core storage
Data channel to core storage
Core storage to CPU
Core storage to data channel

2.2.01 CPU to Core Storage

Data that flow from the CPU to core storage (Figure 2.1-3) are routed from the storage register through the multiplexor storage bus OR'ing circuits to the memory data register. Data flow is controlled by gating at the output of the storage register. The data are gated during an E cycle in which CPU control circuitry calls for store control.

The address at which the data are being stored is switched through the multiplexor address switches. The CPU address register output is gated through these switches as long as the B time trigger is not on. The address is sampled at the memory address register at a given time.

The data flow from the multiplexor to core storage on 36 data lines. At core storage, the data must be set to either 0-35 or 36-71 of the memory data register. The address set to the memory address register specifies which half of the memory data register is set.

2.2.02 Data Channel to Core Storage

Data transmitted to core storage from one of the data channels (Figure 2.1-3) are routed from the particular channel storage bus switches, through the multiplexor storage bus OR'ing circuits, to the memory data register. The data are transmitted during a BDW cycle while reading input, or during the E cycle of a store channel instruction. Data that may be in the storage register are not gated to the multiplexor at the same time. The data being transmitted to core storage are gated at the channel storage bus switches.

The address at which the data are being stored is gated both at the data channel and at the multiplexor. The address is gated through the channel address switches to the multiplexor address switches while reading input during a BDW cycle. Further gating is done at the multiplexor address switches by "channel MAR gate" (Figure 2.1-4). "Channel MAR gate" is an AND function of B time and not a look-ahead address control operation. Notice that B time is required to switch a channel address through the multiplexor, whereas B time must be off to switch a CPU address through the multiplexor. A store channel instruction then transmits data from a data channel to core storage, but switches the CPU address register through the multiplexor. As with a CPU to core storage operation, the address is sampled at the memory address register, and this address determines which half of the memory data register is set.

2.2.03 Core Storage to CPU

When in automatic status, data flow from core storage to the CPU (Figure 2.1-2) always occurs during I cycles and may occur during E cycles. In either case, the data are routed to the multiplexor storage bus where they are gated to the CPU. Data trans-

mitted to the CPU during I cycles are in the format of instructions, whereas data transmitted to the CPU during E cycles may be in any format.

Notice that the bus unconditionally feeds both banks of data channels. However, data are gated through the channel input switches only during B cycles or the E cycle of a reset and load or load channel instruction. The address field (21-35) of the bus also feeds the multiplexor address switches. These positions are gated through the switches only during a look-ahead address control operation.

I Cycle Flow

At I6(D3), data on the multiplexor storage bus are gated to the CPU. CPU storage bus positions S, 1-35 are set to the storage register at I7(D2), while positions S, 1-11 are routed to the instruction register. If the CPU storage bus positions 1 or 2 hold a one at I8(D1), bus positions S, 1, and 2 are set to instruction register positions S, 8, and 9, respectively. If the CPU storage bus positions 1 or 2 do not hold a one at I8(D1), bus positions S, 3-11 are set to instruction register positions S, 1-9 respectively.

E Cycle Flow

During all E cycles in which store control is not up, the multiplexor storage bus is gated to the CPU at E6(D3). At E7(D1), positions S, 1-35 of the CPU storage bus are set to the storage register.

2.2.04 Core Storage to Data Channel

Data flow from core storage to a data channel (Figure 2.1-3) during BCW cycles, BDW cycles while writing output, or the E cycle of a reset and load or load channel instruction.

The data are routed unconditionally to all the data channel input switches. At A3(D7), the data are gated through the input switches of the data channel that either has priority or was addressed by a reset and load or load channel instruction.

Notice that at E6(D3) of a reset and load or load channel instruction, the multiplexor storage bus is gated to the CPU, and at E7(D1) the CPU storage bus is set to the storage register. This is a service aid that checks data flow from core storage to the multiplexor when the machine cycle key is used in conjunction with the reset and load or load channel instruction.

2.3.00 MULTIPLEXOR LOOK-AHEAD CIRCUITS

The multiplexor look-ahead circuits decode those commands being routed to a data channel and that request a successive BCW cycle. These are the transfer in channel command and indirectly addressed commands.

The look-ahead circuits are justified in that a command arrives at a data channel too late to initiate a successive BCW cycle. The logic block delays of the circuitry devoted to decoding requests for BCW cycles at an individual data channel are such that the request must be initiated early in a cycle. The look-ahead circuits, then, activated control circuitry that allows data channels to take sequential BCW cycles when required.

2.3.01 Transfer in Channel Address Control

In bringing a transfer in channel command to a data channel, address control functions (Figure 2.3-1) are initiated at the multiplexor. Logically, the multiplexor addresses a new command specified by the address field of the transfer in channel command which, in turn, is loaded into the data channel. To accomplish this, the control circuitry does the following:

1. Suppresses any channel address from being switched through the multiplexor address switches
2. Retains priority by turning on the B time trigger at the CPU, and the BCW required trigger at the individual data channel
3. Switches the address field of the transfer in channel command through the multiplexor address switches to the memory address register

Transfer in Channel Flow

The transfer in channel command is loaded into the individual data channel and activates "operation register 2." See Figure 2.3-2. "Operation register 2" works in conjunction with the look-ahead circuits to set the output of the multiplexor address switches to the location counter during the following cycle.

At the completion of the second cycle, a new command has been loaded into the individual data channel, and the location counter contains the address of that command plus one. Notice that a transfer in channel command addressed to itself ties up a data channel in BCW cycles and therefore is construed as an illegal operation.

2.3.02 Not Transfer in Channel Commands with Word Count Equal to Zero

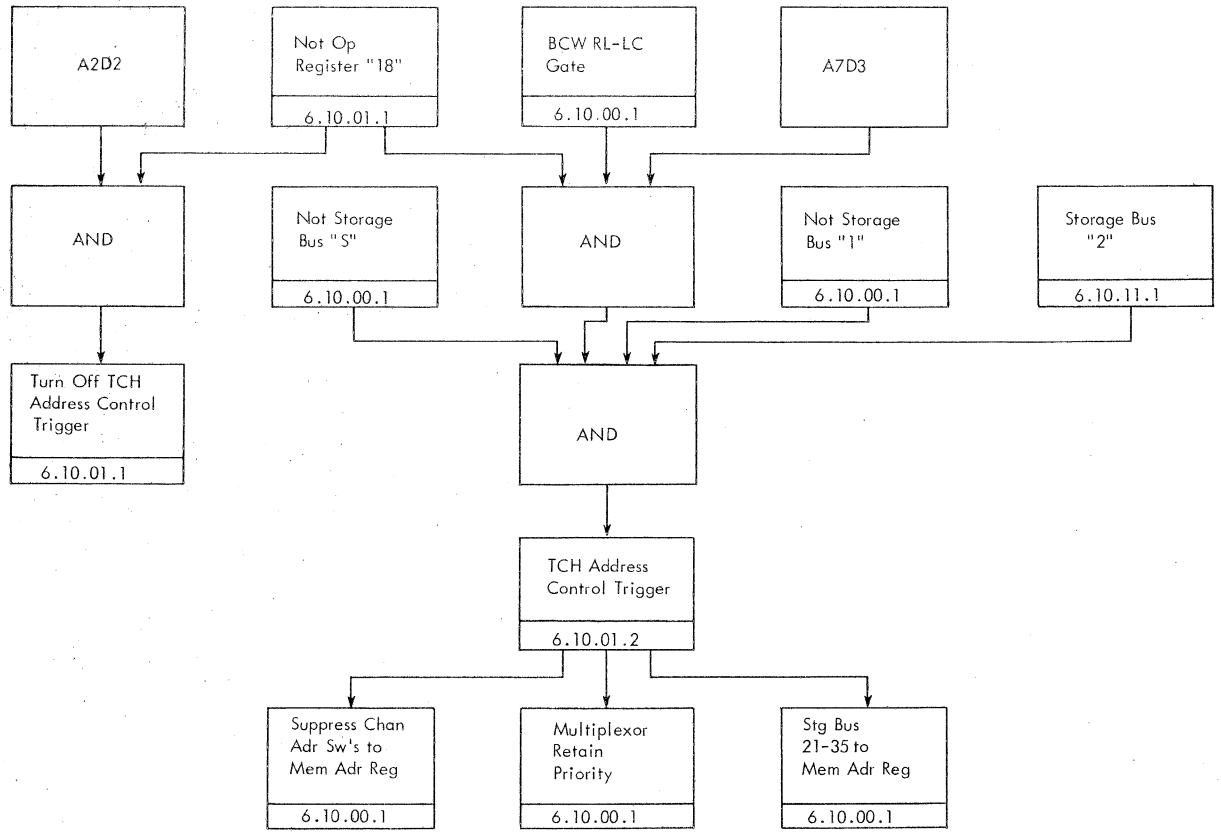
When a command with a word count of zero is decoded at the multiplexor, and this command is not a transfer in channel command, the look-ahead circuits are activated to prevent indirect addressing of such commands. See Figure 2.3-3.

If the command is a proceed type command, the address of the next sequential command is specified by the location counter. Normal BCW controls at the data channel gate the location counter through the channel address switches to the multiplexor address switches. "Channel MAR gate" switches the address through the multiplexor address switches to the memory address register (Figure 2.1-4).

During the BCW cycle the addressed command is loaded into the data channel and the location counter is increased by one.

2.3.03 IA Address Control and "Operation Register 18"

A command being routed to a data channel that contains a 1 position 18 initiates address control functions and turns on "operation register 18." See Figure 2.3-4. The indirectly addressed command is loaded into the data channel, but the address control functions call for another core storage cycle. During this core storage cycle indirect addressing takes place. Logically, the address field of the indirectly addressed command is changed. The address field of the indirectly addressed command addresses a new word which, in turn, is brought to the multiplexor. The address field of this new word is gated to the channel address counter. The "operation register 18" and word count field of the indirectly addressed command are not affected.



LOOK-AHEAD

FIGURE 2.3-1. TCH ADDRESS CONTROL

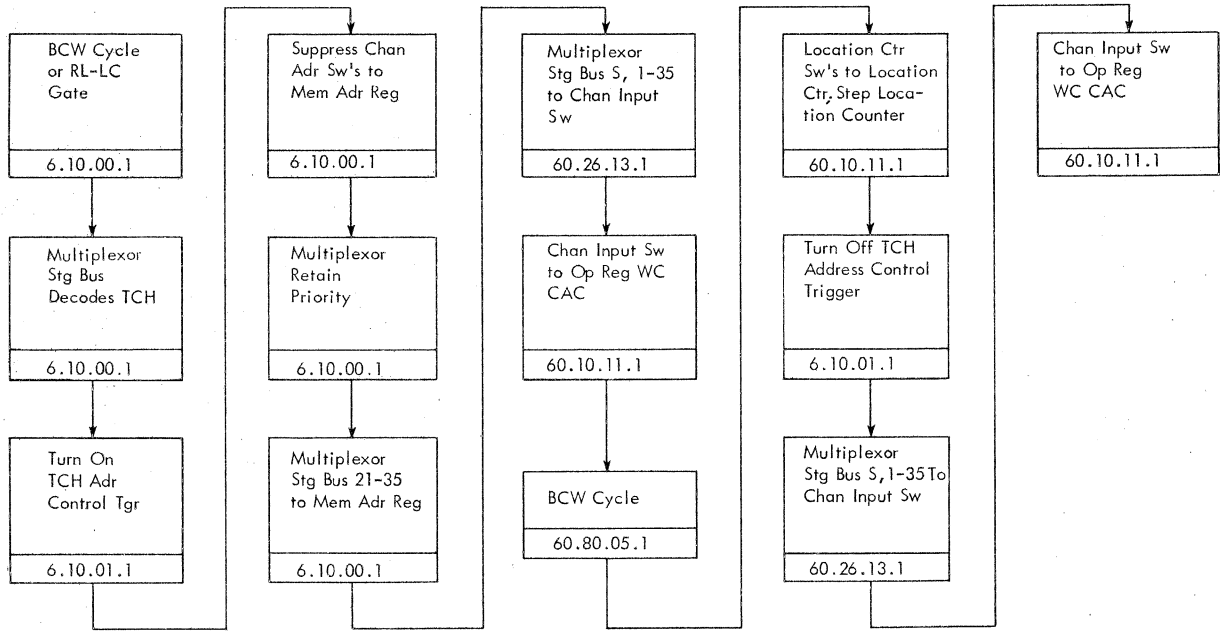


FIGURE 2.3-2 TRANSFER IN CHANNEL FLOW

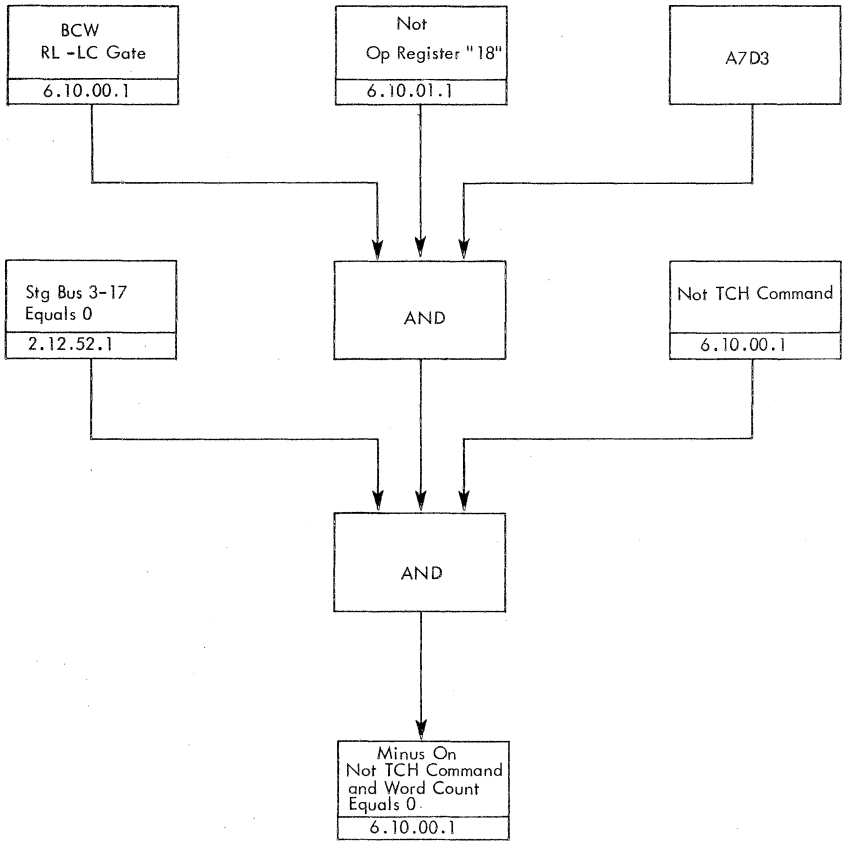


FIGURE 2.3-3 DECODING FOR SUPPRESSION OF INDIRECT ADDRESSING

To accomplish indirect addressing of commands (Figure 2.3-5), the look-ahead circuits do the following:

1. Suppress any channel address from being switched through the multiplexor address switches
2. Retain priority by turning on the B time trigger at the CPU, and the BCW required trigger at the data channel
3. Switch the address field of the indirectly addressed command through the multiplexor address switches to the memory address register
4. Prevent the address field of the indirectly addressed command from being loaded into the location counter ("Operation register 18" controls gating.)
5. Prevent the new word from initiating indirect addressing
6. Prevent the indicator and word count fields from being loaded into the data channel ("Operation register 18" controls gating.)

Notice that commands other than transfer in channel commands with a word count of zero and a 1 in position 18 are not allowed to initiate address control functions and turn on "operation register 18" (Figure 2.3-4).

2.3.04 Indirectly Addressed Transfer in Channel Command

An indirectly addressed transfer in channel command (Figure 2.3-6), when routed to a data channel, initiates both IA address control functions and TCH address control functions at the multiplexor. The IA address control functions are performed, followed by the TCH address control functions. The decoding of an indirectly addressed transfer in channel command results in three sequential BCW cycles.

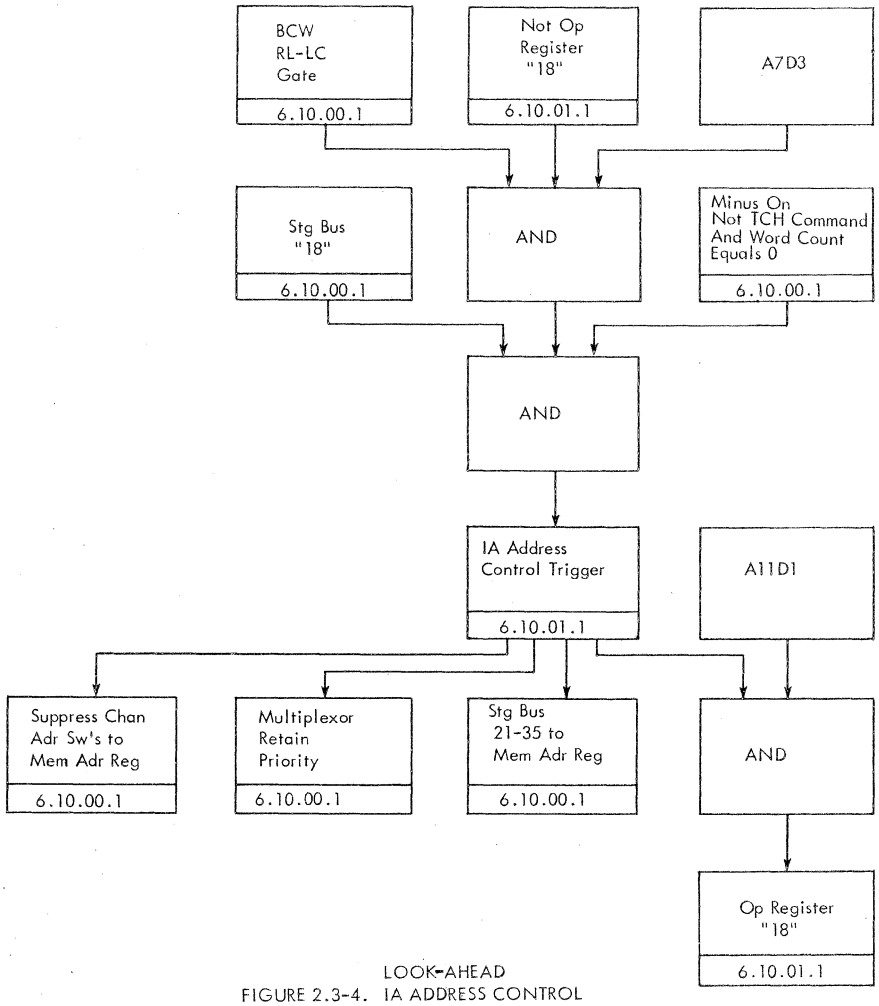
2.4.00 TAILGATE ASSEMBLY

The tailgate assembly on the multiplexor receives cabling from the multiplexor sliding gates. It also serves as a connector for cables that go to or from the multiplexor.

2.4.01 Logical Assignment of Data Channels

The multiplexor tailgate contains eight connectors for data channel assignment cables. The assignment cables feed respective data channels on the 7090 system and contain those control lines unique to a data channel.

The eight connectors on the tailgate assembly are labeled A through H, corresponding to data channel addresses. An assignment cable may be connected to any one of the eight connectors, permitting any physical data channel to have a logical address of A through H by merely changing the connection of the assignment cable.



LOOK-AHEAD

FIGURE 2.3-4. IA ADDRESS CONTROL

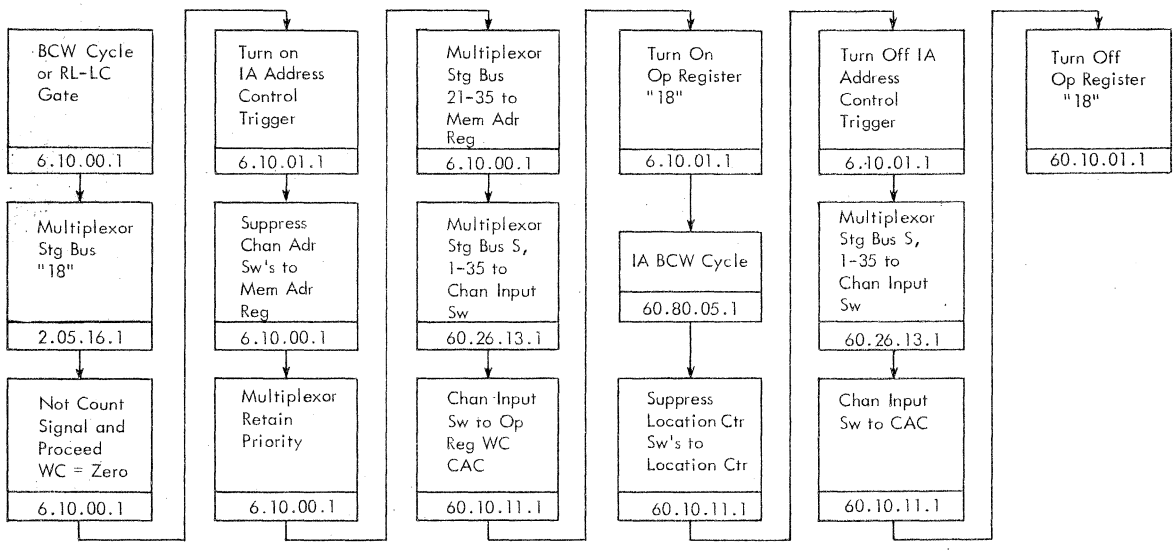


FIGURE 2.3-5. FLOW OF AN INDIRECTLY ADDRESSED COMMAND

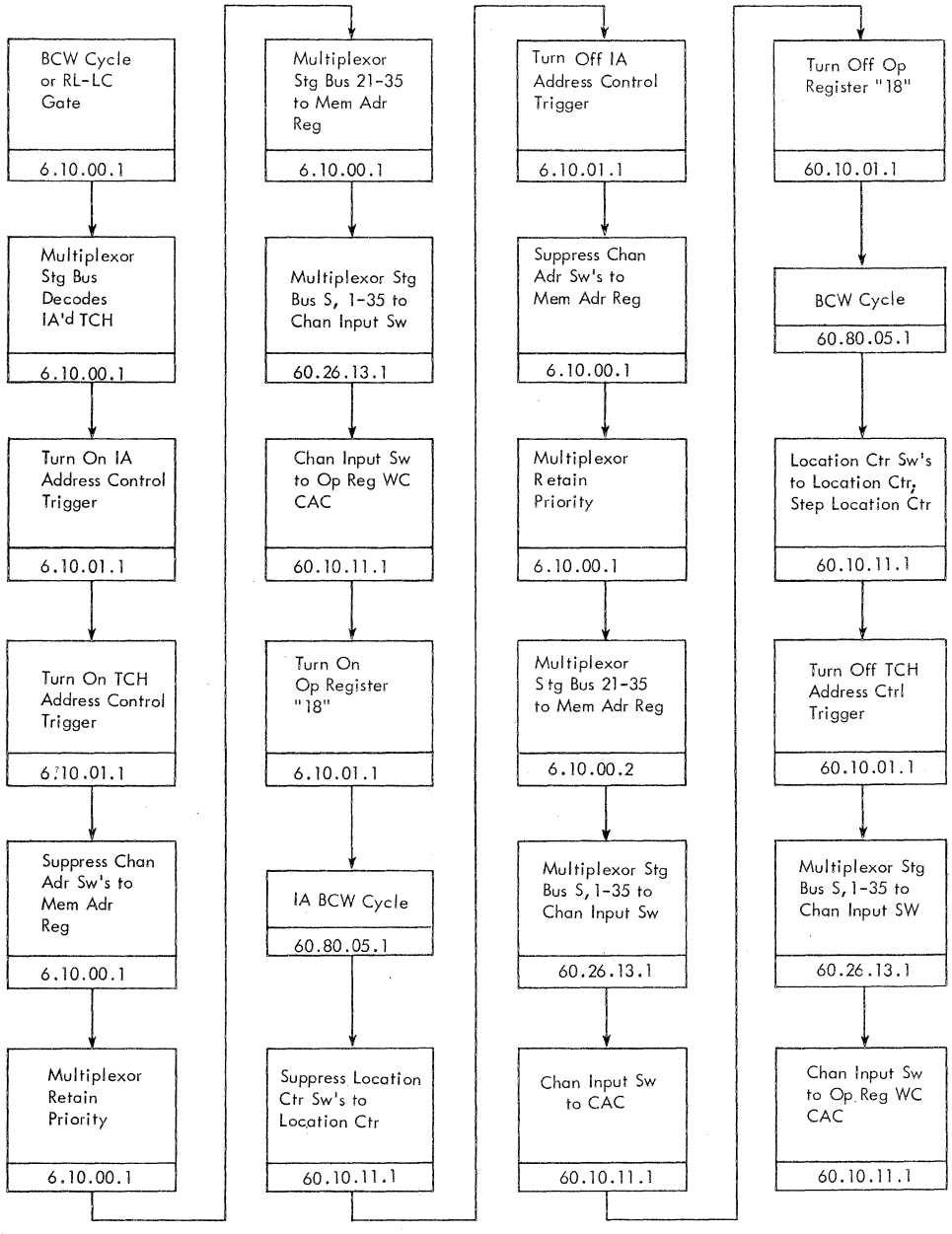


FIGURE 2.3-6. FLOW OF AN INDIRECTLY ADDRESSED TRANSFER IN CHANNEL

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