

IBM[®] Customer Engineering Reference Manual

704 Data Processing System 704 Central Processing Unit

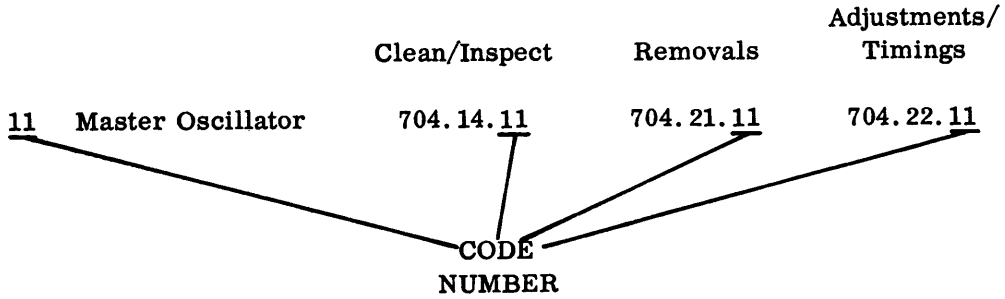
CONTENTS

SECTION	TITLE	PAGE
704.10.00	PREVENTIVE MAINTENANCE	10-1
	In this section the necessary maintenance is covered to cut down on machine troubles. This includes the P. M. guide and record; the P. M. procedures; the lubrication chart; the points to check, places to clean, and the waveforms and wave-shapes you should see at different test points.	
704.20.00	CORRECTIVE MAINTENANCE	20-1
	In this section all the items cover methods of correcting machine troubles. The items cover removals and assembly procedures, adjustments and any timings to keep the 704 in an operating condition.	
704.30.00	DIAGNOSTIC OR RELIABILITY TESTS	30-1
	In this section are the brief write-ups on the diagnostics to use in checking out a 704 CPU, the reliability acceptance tests, programs used to load the machine, the diagnostic format and print routines used, and many of the CPU diagnostic tests, showing when they can be used and what to expect from them.	
704.40.00	SERVICE TECHNIQUES	40-1
	In this section an approach to trouble shooting is covered. There is a chart where general machine problems are brought to a specific area, point or cause. This is made available for the C. E. for many CPU problems. Also, a chart of oscilloscope problems and fixes are listed.	
704.50.00	SERVICE AIDS	50-1
	In this section is a general list of items that might prove helpful in servicing a 704 CPU. The things covered are machine specifications, test point locations, tube and panel locations in relation to operations, I/O shoe connections, neon locations, scope aids and 704 CPU troubles and their fixes.	
704.60.00	AUTOMATIC MACHINE LOGIC	60-1
	In this section the general data flow within the CPU and data flow from CPU to I/O units is given. Data and machine operations during an instruction cycle and also data flow and machine operations of many of the instructions as well as sequence charts are provided for reference material.	
704.70.00	MANUAL MACHINE LOGIC	70-1
	In this section some of the internal circuitry sequence charts are given. Included in this is the clock and cycle timer, and the card control circuits. Also sequence charts of the key routines, load, enter MQ, and display effective storage are provided.	

NOTICE

Each different unit, item and test of this machine has been assigned a "Reference Manual Code Number." This code number is located in the tens and units position of each section number. All numbers over .50 have been assigned to wave-shapes in each section. Therefore, waveforms between each manual will not have the same numbers. Numbers in the tape drive also will differ.

The following index chart can be used to find the location of the appropriate maintenance information.



ABBREVIATIONS

The following abbreviations are used throughout this manual.

AC	alternating current	IR	instruction register
acc	accumulator	KC	kilocycle
add	adder	lb	pound
adj	adjustment	loc	location
adr	address	lt	left
AL	A lower points on a duo relay	LV	low voltage
amp	amplitude	max	maximum
amp	ampere	MF	main frame
AU	A upper points on a duo relay	min	minimum
BCD	binary coded decimal	mo	month
bksp	backspace	MQ	multiplier quotient
BL	B lower points on a duo relay	msec	millisecond
BU	B upper points on a duo relay	n/c	normally closed
C	centigrade	n/o	normally open
cal	calibration	No	number
CE	customer engineer, customer engineering	op	operation
CF	cathode follower	oper	operation
cm	centimeter	opn	operation
cntl	control	oz	ounce
col	column	PCF	power cathode follower
cond	condition	PM	preventive maintenance
CPU	704 Central Processing Unit	pnl	panel
CRT	740 Cathode Ray Tube	pos	position
CT	control trigger	pr	printer
ctr	counter	reg	register
ctrl	control	res	resistor
DC	direct current	Rd/Wr	read or write
def	deflection	RMS	root mean square
disc	disconnect	RPM	revolutions per minute
DP	double pole	rt	right
DT	double throw	rwd	rewind
EOF	end of file	SB	storage bus
EOR	end of record	SBR	storage buffer register
ext	external	SP	single pole
F	fahrenheit	spec	specifications
FP	floating point	SR	storage register
ft	feet	ST	single throw
gen	generator	stg	storage
hr	hour	sw	switch
HV	high voltage	sync	synchronizer
IC	instruction counter	tgr	trigger
I/O	input or output	thy	thyatron
in, "	inch	usec	microsecond
inst	instruction	UL	Underwriter's Laboratories
int	interval	V, v	volt
intlk	interlock	vert	vertical
		XR	index register

Type	Name	Weight	Length	Width	Height	KVA	KW	Amps	Speed
704	Central Processing Unit	3440	72	37	66	40.3	32.2	112.0	12 usec
711	Punched Card Reader	560	32	30	32	.7	.5	1.7	150 cd/min 250 cd/min
716	Alphabetic Printer	1910	59	30	47	3.1	2.3	8.0	150 ln/min
721	Punch Card Recorder	670	40	26	50	3.5	2.6	9.0	100 cd/min
727	Magnetic Tape Unit	920	29	31	69	2.2	1.2	6.0	75 in/sec.
733	Magnetic Drum Reader & Recorder	1930	55	31	67	10.4	7.8	25.7	
737	Magnetic Core Stg	1500	105	31	64	6.4	4.8	17.8	
738	Magnetic Core Stg	4000	159	95	64	23.4		65.0	
740	CRT Output Recorder	740	26	37	52	2.4	1.8	6.7	
780	CRT Display Unit	250	24	28	22				
753	Tape Control Unit	2240	60	32	67	6.0	2.7	16.7	67.2 usec
736	Power Frame 1	2770	61	34	65	5.8	4.3	15.0	
741	Power Frame 2	3610	61	34	65	5.8	4.3	15.0	
746	Power Dist. Unit	1070	41	34	65	1.2	.9	3.1	

236.7 Amperes

Total Current Load is 350 Amperes per line

MACHINE SPECIFICATIONS

INDEX CHART

AREA	REF. MAN. CODE NO.	ITEM	CLEAN & INSPECT	WAVE FORMS & LEVELS	REMOVALS	ADJUST. & TIMINGS
MAIN	1	General heat problems	704.14.01			
FRAME	2	Appearance and filters	704.14.02		704.21.02	
	3	Motor and blowers	704.14.03		704.21.03	
	4	I/O shoes and receptacles	704.14.04			
	4	Pluggable units & panel pins	704.14.04			
	5	Thermals	704.14.05			
	9	Resistors & filament transformer	704.14.09			
	11	Master oscillator assembly	704.14.11		704.21.11	704.22.11
	13	Tube testing	704.14.13			
	14	Vibration checking	704.14.14			
	15	Pulse checking	704.14.15	704.15.00		
	16	Marginal checking		704.15.16		
	19	Special pulses		704.15.19		
RIGHT END	2	Appearance and filters	704.14.02		704.21.02	
RESISTOR	3	Motor and blower	704.14.03		704.21.03	
PANEL	5	Thermal	704.14.05			
	8	Relay gate	704.14.08			704.22.08
	9	Resistor panel	704.14.09			704.22.09
	10	Rectifier	704.14.10			
OPERATOR'S	6	Keys and buttons	704.14.06		704.21.06	704.22.06
PANEL	6	Switch Assy	704.14.06		704.21.06	704.22.06
	6	Neons and lights	704.14.06		704.21.06	
	6	Test panel switches	704.14.06			
	7	Test panel sockets	704.14.07			
MASTER	19	Sync. clamp and clock spec.		704.15.19		
PULSES	8.06.04	50	Oscillator output	704.15.50		
	8.06.02	51	Sync clamp output	704.15.51		
	8.06.03	52	Inverted sync line	704.15.52		
	8.06.04	53	Inverted clamp line	704.15.53		
	8.06.03	54	Clock drive	704.15.54		
	8.05.04	55	Master I time	704.15.55		
	8.05.04	56	Master E time	704.15.56		
	8.05.04	57	Master ER time	704.15.57		
CLOCK	8.04.01	58	A0	704.15.58		
AND	8.04.01	58	A1	704.15.58		
GATE	2.09	59	I _g to CT ₁	704.15.59		
PULSES	2.09	59	E _g to CT ₂	704.15.59		
	3.20	60	Instruction counter advance	704.15.60		
	3.20	60	Position (17) binary input	704.15.60		
	3.40	61	Gated minus on A0 (D1)	704.15.61		
COUNTER	8.04	62	Shift counter drive	704.15.62		
DRIVES &	8.04	63	Tally counter drive	704.15.63		
CONTROLS	3.05	64	Binary input to shift counter (17)	704.15.64		
	2.07.02	65	Conditional transfer ctrl	704.15.65		

SECTION	TITLE	PAGE
704.10.00	PREVENTIVE MAINTENANCE	10-4
704.11.00	DP Preventive Maintenance Guide and Record	10-5
704.12.00	Preventive Maintenance Procedure	10-6
704.13.00	Lubrication Chart	10-6
704.14.00	Clean/Inspect	10-7
704.14.01	General Heat Problems	10-7
704.14.02	Appearance and Filters	10-7
704.14.03	Motors and Blowers	10-7
704.14.04	I/O Shoes, Receptacles, Pluggable Units, Contacts and Signal Cables	10-7
704.14.05	Thermals	10-7
704.14.06	Keys, Buttons, Lights, Neons and Oper- ator's Panel	10-8
704.14.07	Test Panel, Receptacles and Sockets	10-12
704.14.08	Relays and Relay Gate	10-12
704.14.09	Resistor Panel and Transformers	10-12
704.14.10	Rectifiers	10-13
704.14.11	Master Oscillator Assembly	10-13
704.14.13	Block Tube Testing	10-13
704.14.14	Vibration Checking	10-13
704.14.15	Pulse Checking	10-13
704.15.00	Waveforms and Levels	10-13
704.15.16	Marginal Checking	10-13
704.15.19	Special Pulse Specifications	10-13
	A. Inverted Sync Pulse	
	B. Inverted Clamp Pulse	
	C. Clock Drive Pulse	
704.15.50	Oscillator Output	10-14
704.15.51	Sync Clamp Output	10-14
704.15.52	Inverted Sync Line	10-14
704.15.53	Inverted Clamp Line	10-15
704.15.54	Clock Drive	10-15
704.15.55	Master I Time	10-15
704.15.56	Master E Time	10-15
704.15.57	Master ER Time	10-15
704.15.58	Clock Pulses	10-16
	A. A0	
	B. A1	
704.15.59	Pulse and Gate Generator	10-16
	A. I _g to Ct 1	
	B. E _g to Ct 2	
704.15.60	Instruction Counter	10-16
	A. Advance	
	B. Pos. (17) Binary Input	
704.15.61	Gated Minus on A0(D1)	10-17
704.15.62	Shift Counter Drive	10-17
704.15.63	Tally Counter Drive	10-17
704.15.64	Sync Pulse with Binary Input to Shift Counter	10-17

SECTION	TITLE	PAGE
704.15.65	Conditional Transfer	10-18
704.15.66	Routing Lines	10-18
	A. Storage Register to Adders	
	B. Storage Bus to Storage Register	
	C. True Accumulator to Adders	
	D. Adders to Accumulator	
	E. Index Register to Adders	
	F. End Operation	
704.15.67	Interlock Reset	10-19
	A. Load	
	B. Start	
704.15.68	Key Operations	10-19
	A. Single Step	
	B. Enter Instruction	
	C. Storage Display	
	D. Turn Off Master Stop	
704.15.69	Start Bias Reset	10-20
704.15.70	Sync Pulse Used on Rd/Wr	10-20
704.15.71	Card Control Ring	10-20
	A. Even Ring Drive	
	B. Odd Ring Drive	
	C. Even and Odd Relationship to Sync Pulse	
	D. Even Ring Drive to Sync Pulse	
704.15.72	Rd/Wr Pulse	10-21

704.10.00 PREVENTIVE MAINTENANCE

A customer engineer is called upon to perform two types of maintenance - corrective and preventive. Corrective maintenance is the finding and correcting of a trouble after it has occurred. Preventive maintenance is the work which is performed on a regularly scheduled basis to correct potential trouble, minimize service calls, and maintain machine availability to the customer.

The importance of regularly scheduled preventive maintenance is shown in two ways. First, it is important to the customer, because the work is done on the machine during off-peak load periods. Second, it is important to the customer engineer, because it enables him to schedule his activities and use his time to the greatest advantage.

By applying preventive maintenance techniques, more machine time is available to the customer. Overscheduling of preventive maintenance is as undesirable as underscheduling. The objective is to increase machine availability to the customer by reducing total maintenance time.

For the first three months of operation, preventive maintenance should be performed as recommended in section 704.12.00 (P. M. Procedure). By this time, the customer engineers of each installation should have filled in the frequency of inspection on the P. M. Guide and Record (Section 704.11.00). Also by this time, they should have developed their own preventive maintenance schedule.

704.12.00 PREVENTIVE MAINTENANCE PROCEDURE

Air Filters
2 mo. .4 Hr. Remove and inspect air filters, replacing those that are dirty.

Tube Checking
3 mo. .8 Hr. Block check only after biasing and pulse checking fail to locate general failures. An occasional visual check should be made for open filaments of parallel cathode followers.

Visual Inspection of pulses during customer operation
Once in each 3 months of operation pulse check the following circuits. Use the following pages of test points as a guide.

Abnormal DC Bias Tests
Monthly .8 Hr. Using 4M31, vary each DC supply. Operation should be error free for one minute at each limit.

+ 150	+ 142	± 1
	+ 162	± 1
+ 220	+ 198	± 1
	+ 242	± 1
- 250	- 230	± 1
	- 263	± 1
- 100	- 90	± 1
	- 110	± 1
- 30	- 33	± .5
	- 27	± .5
Oscillator	920 KC	5 to 6 division
	1090 KC	marks each way

704.13.00 LUBRICATION CHART

The CPU components should be lubricated about every three months, unless trouble occurs from the lack of lubrication;

Code No		Type of lubrication				
		6	9	12	17	20
2	Cover and door hinges (If it does not have sealed bearings)		X			
2	Cover latch cams				X	
2	Cover door rollers		X			
3	Motor-resistor stacker (If it does not have sealed bearings)		X			
8	Duo relay pivots (pipe cleaner)	X				
8	Duo relay operating pods (light film)				X	
8	Wire relay pivot	X				
8	Wire relay latch (if latch type)	X				

704.14.00 CLEAN AND INSPECT

704.14.01 General Heat Problems

Following are the general rules to follow on checking the operating temperature of motor bearings, transformers and resistors. A reliable method of checking panel temperatures is also given.

Motors, Generators and Blowers

These must operate in the allowable range of a 20° C (78° F) temperature rise over ambient room temperature. An allowable winding temperature is 63° C (145° F). This cannot be effectively measured in the field, but for motors without moving air over them, there is a 10° - 12° C (50° - 54° F) difference in temperature between bearing temperature and winding temperature. This means that bearings without moving air moving over them may operate up to about 130° F. Motors with air flowing over the bearings should operate at a lower temperature. There is no easy sure way to measure bearing temperatures in the field, but the simplest and most accurate way is to mount a thermometer in putty on the outside of the bearing surface. Another possible means is the use of graded Tempilstiks*. Use of the thermometer actually gives the exact operating temperature and this is normally desired.

Transformers and Rectifiers

The general rules of motors also apply to transformers and rectifiers. A 20° C (78° F) temperature rise over ambient room temperature is allowable. An effective way to measure the operating temperature is to tape or putty a thermometer to the external surface. Tempilstiks can also be used. Tempilstiks are wax sticks that melt at graded temperatures. These can be held or marked on the external surface.

Resistors, Inductors and Capacitors

Probably the most effective way to measure operating limits on suspected components is to measure the voltage drop across, and the current through, the component and check against the rated voltage of the component. Remember that feeling a surface to check for temperature is ineffective, unreliable and dangerous.

Panels

An effective method of measuring panel temperatures is to mount a thermometer on the left end of panel 1, right end of panel 1, left end of panel 2, right end of panel 2 and the right end resistor panel after the machine is installed. These temperatures should be recorded and kept available with the machine. Periodically these temperatures should be checked, and any variation of over 15° F should be examined further. The exhaust temperature of the different parts of the panels may vary widely between machines, panels, and even ends of panels, because of blower speed, type of tubes used, and other variables.

All panels are protected by thermal switches and the preventive maintenance procedures are found in 704.14.05.

704.14.02 Appearance and Filters

Clean windows with clean water or any window cleaner. Clean any large accumulation of dust or dirt on machine with a vacuum cleaner. Clean all covers with IBM polish and check all covers for good latching. Check for loose hinges or loose arm on the operator's panel.

Check the air filters in each main frame unit and replace when dirty. **Do not clean** any filters. Check the air filter in the right end resistor panel and replace when dirty. Be sure to check the operation of the blower motor when replacing air filters, particularly on the smaller motors which cannot be heard above the general room noise.

*Registered trademark of Tempil Corp.

704.14.03 Motors and Blowers

Central Processing Unit

Check motors and blowers with power off to be sure the motor shafts are free of binds. With blowers running, check all panels for a good air flow and check exhaust temperature as described in 704.14.01. Check motors for quiet operation by putting one end of a large dowel to the bearing surface and the other end to your ear. Check bearing temperatures as described on 704.14.01.

Right End Resistor Panel

Check motor shaft to be free of binds. Check for a good air flow throughout the panel. Check the motor for quiet running operation as above, and the bearings to see that they are not running hot, also as described on 704.14.01.

704.14.04 I/O and Signal Shoes, Receptacles, Pluggable Unit Contacts and Signal Cables

I/O and Signal Shoes and Contacts

Check all I/O and SP shoes and receptacles for dirty, bent or broken contacts and for loose or corroded connections. Prongs and contacts are cleaned by using a cleaning solvent. Never stone, sand or burnish for the plating may be removed.

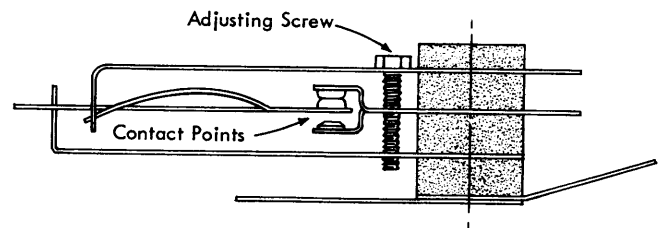
Pluggable Units

Some jumper wires between pluggable units are too tight. Check to see if the insulation on the tight wires is broken and occasionally grounding out.

Panel Pins

Check for spread panel pins on the pluggable unit being installed on the machine. Some crack near bottom of contact area giving poor contact.

704.14.05 Thermals



Description

A thermal switch consists of two bimetal elements mounted in a rigid ceramic assembly which supports the operating spring. The movement of the bimetallic elements caused by temperature changes provides the force to operate the switch. This recycling switch automatically returns the center spring member to its normal position when the temperature returns to normal.

Preventive Maintenance

Check the thermal light for proper operation. Check contact alignment and clean the points for good "make" surface. Test to be sure power is knocked down when contact points are operated. Check connections to see they are not loose, grounded or shorted.

The thermals in MF 1 and 2 are set to operate at $131^{\circ} \pm 5^{\circ}$ F. The thermal in the right hand resistor panel is set to operate at $194^{\circ} \pm 5^{\circ}$ F. The adjusting screw can be reset if thermals do not operate in the correct range of temperatures.

Operator's Panel Keys and Buttons

Clean any dirty keys or buttons with IBM Cover polish. Do not use IBM cleaning fluid or Tape Developer Medium Transport Cleaner because it melts the plastic operating mechanism. Check all keys to see they are not binding or broken.

Operator's Panel Key Blank Lever Switches (piano key switches):

Check for loose or grounded connections. Check the n/o points and the n/c points, when transferred, for a .015" - .020" clearance.

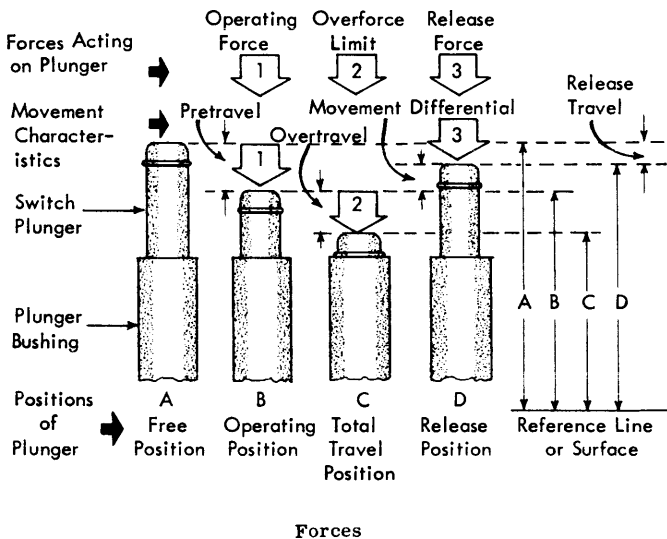
Check the n/o and n/c strap for a tension of 30-35 grams. There should be a minimum of 35 grams' tension to move the operating strap.

Microswitches

Preventive Maintenance. There is very little preventive maintenance to be done on microswitches; the contact life is the greatest source of trouble. The contacts are made of silver and the movable contacts are mounted on a three-bladed beryllium copper spring. This gives the switch extremely fast action (.005 seconds) and operates the contacts in the same direction as the plunger for the dependability of accuracy needed. Contact wear determines the actual life of these switches.

Check to be sure that when under vibration some of the normally closed switches which are very sensitive do not put spikes on the lines.

Definition of Terms. Following are some of the definition of terms used in different microswitches.



- a. Operating Force- The force which is applied to the actuator to cause the moving contact to snap from the normal contact position to the operated contact position.
- b. Overforce Limit- The force which is applied to the actuator to cause it to move to the overtravel limit position.
- c. Release Force- The value to which force on the actuator is reduced to allow the contacts to snap from the operated contact position to the normal contact position.
- d. Differential Force- The difference between Operating Force and Release Force.

Position

- a. Free Position- The initial actuator position when there is no external force (other than gravity) applied on the actuator. The term "Free Position" is understood to mean actuator free position.
- b. Operating Position- The position of the actuator at which the contacts snap from the normal position to the operated contact position.
- c. Release Position- That position of the actuator at which the contacts snap from the operated contact position to the normal contact position.

Movement

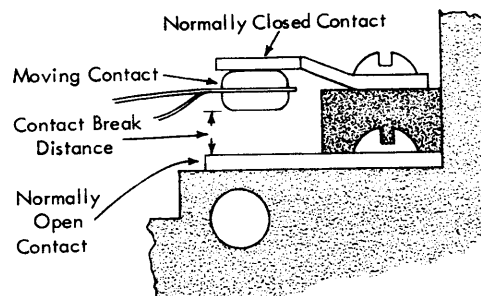
- a. Pretravel- The distance or angle through which the actuator moves when traveled from the actuator Free Position to the Operated Position.
 - b. Overtravel- The distance or angle through which the actuator moves when traveling from the Operating Position to the Overtravel Limit position.
 - c. Total Travel- The distance or angle from the actuator Free Position to the Overtravel Limit position.
- If it is necessary to imply direction in addition to distance or angle, this term may be modified as Operating Total Travel, Releasing Total Travel, or Resetting Total Travel.
- d. Movement Differential- The distance or angle from the Operating Position to the Releasing Position.

Snap Action

The rapid motion of contacts from the normal contact position to the operated contact position, or their return. This action is relatively independent of the rate of travel of the actuator or resetting mechanism, and will occur without further travel of the actuator beyond the Operating Position, Releasing Position, or Resetting Position.

Contact Break Distance

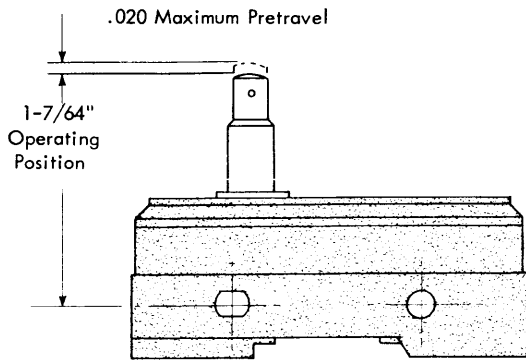
The Contact Break Distance of a switch is the maximum distance by which the moving and stationary contacts are separated.



Types of Microswitches

"S" Plunger Switches

"S" Plunger Switches are used as general purpose safety switches, limit switches and control switches, where a small amount of overtravel in the plunger is desired. Applications include instruments and automatic machinery.

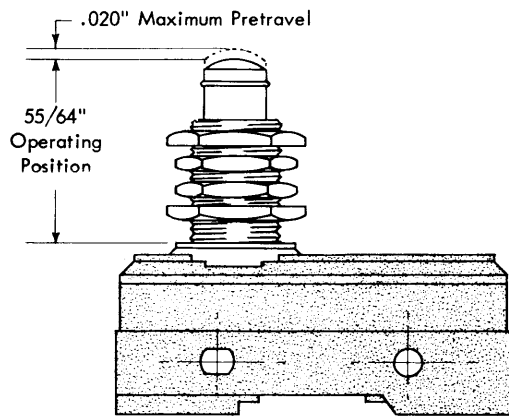


Characteristics

Operating Force 9 to 13 oz. Overtravel.....0.062 in.,
 Release Force...4 oz., min.
 Pretravel...0.020 in., max.
 Overtravel.....0.062 in., min.
 Movement Differential 0.0004 to 0.0020 in.
 Net Weight.....0.067 lb., max.

"Q1" Plunger Switches

"Q1" panel mounting switches are used as door switches, manual or mechanical push button switches in safety, limit or control applications. This switch design is especially useful for its panel mounting provisions and in applications where the actuating motion cannot be accurately controlled.

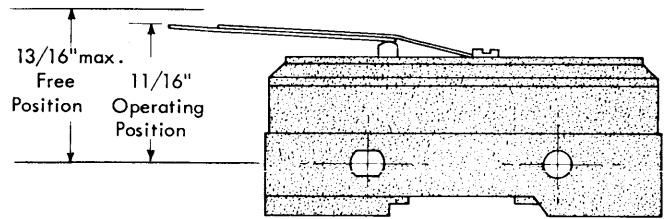


Characteristics

Operating Force 9 to 13 oz.
 Release Force...4 oz. min.
 Pretravel...0.020 in., max.
 Overtravel.....7/32 in., min.
 Movement Differential 0.00004 to 0.0020 in.
 Net Weight.....0.097 lb. max.

"L" Leaf Actuator Switches

The "L" Leaf Actuator is especially useful where the switch is required to operate on small force. Larger actuating movement is required to operate the "L" Leaf switches than for plunger type switches. Cams may be used against the leaf actuator.

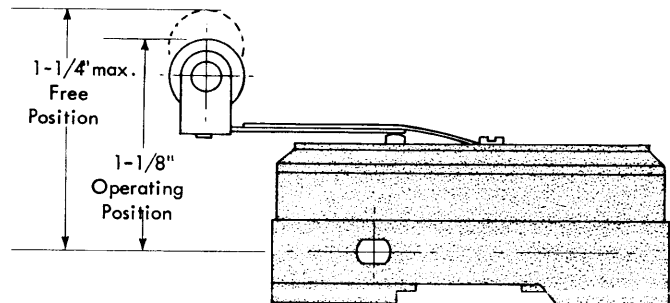


Characteristics
(at tip of leaf)

Operating Force 5 oz. max.
 Release Force...1/2 oz., min.
 Pretravel...5/32 in., max.
 Overtravel..... must not be permitted in excess of 1/16 in.
 Movement Differential...0.050 in., max.
 Net Weight.....0.064 lb., max.

"L2" Roller Leaf Actuator Switches

"L2" Roller Leaf Actuator Switches are useful in applications that combine extremely low operating force with relatively large operating movement. Typical applications are those that employ synchronous clock motors or other low power means.



Characteristics

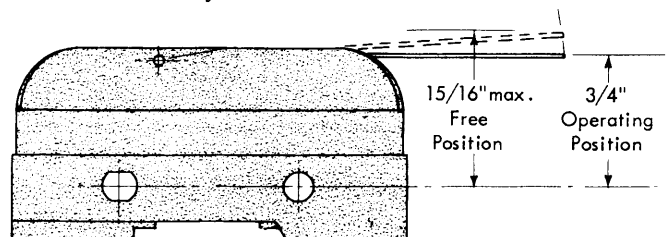
Operating Force...6 oz., max.
 Release Force....1/2 oz., min.
 Pretravel.....5/32 in., max.
 Overtravel..... must not be permitted in excess of 1/16 in.
 Movement Differential...0.050 in., max.
 Net Weight.....0.073 lb., max.

Actuator Not Adjustable

Depressing the leaf beyond 1/16 in. limit of overtravel or bending the leaf will affect the switch life. Should the application require greater overtravel or require adjustment by bending the leaf or lever, the type "M" or "W" switches may be more suitable.

"M" Lever Actuator Switches

"M" Basic Switches are for operation by cams and non-linear movements, as well as by straight line actuation. The straight flat lever is particularly useful on applications where the cam motion is relatively slow.



Characteristics

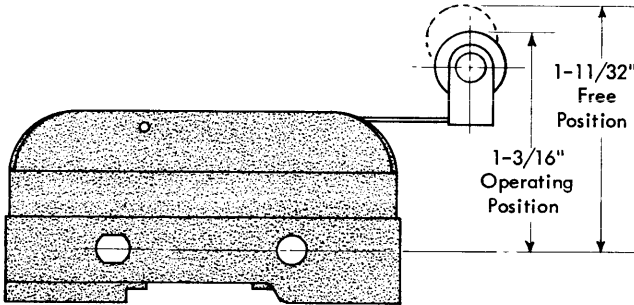
Operating Force... 6oz., max.
 Release Force... 1 oz. min.
 Pretravel... 7/32 in., max.
 Overtravel... 7/32 in., min.
 Movement Differential 0.004 to 0.035 in.
 Net Weight... 0.074 lb., max.

Reverse Action

The action of the "M" switch is the reverse of that of other Basic Switches. A spring on top of the switch case holds the switch plunger depressed. Actuating force applied to the lever overcomes the spring force, releasing the switch plunger. Terminal arrangement is likewise the reverse of other types of Basic Switches. The lever may be bent to change and adjust operating position, without affecting other characteristics.

"M2" Roller Lever Actuator Switches

"M2" Roller Lever switches are for actuation by fast moving cams as well as straight line motion.



Characteristics

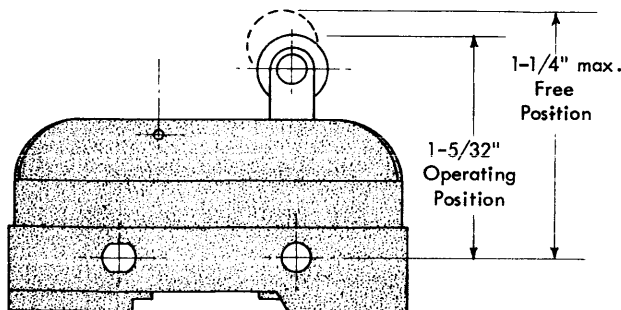
Operating Force... 8 1/2 oz., max.
 Release Force... 2 oz., min.
 Pretravel... 3/16 in., max.
 Overtravel... 5/32 in., min.
 Movement Differential 0.003 to 0.025 in.
 Net Weight... 0.081 lb., max.

Reverse Action

Like the "M" above the switch action is the reverse of other Basic Switches. A spring around the lever pivot bears against the switch cover and the lever holding the switch plunger fully depressed. Force applied to the roller overcomes the spring force thus permitting the internal snap-action spring to snap to its other position. Note that terminal arrangement is likewise reversed. The lever arm may be bent for adjustment.

"M22" Roller Lever Actuator Switches

"M22" Basic Switches are designed for operation by fast moving cams in applications where a compact switch unit is required.

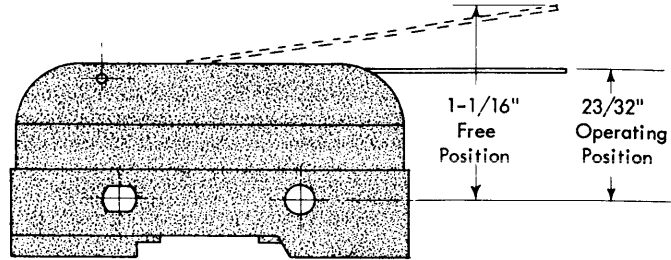


Characteristics

Operating Force... 19 oz., max.
 Release Force... 6 oz., min.
 Pretravel... 7/64 in., max.
 Overtravel... 5/64 in., min.
 Movement Differential... 0.001 to 0.011 in.
 Net Weight... 0.079 lb., max.

"W" Lever Actuator Switches

"W" switches are distinguished from other Basic Switches by their low operating force requirements. The flat lever actuator may be operated by cams or slides.



Characteristics

2RW (with coil spring)
 Operating Force... 1 to 2 1/2 oz.
 Release Force... 1/2 oz., min.
 Pretravel... 11/32 + 1/16 in.
 Overtravel... 3/16 in., min.
 Movement Differential... 0.016 to 0.078 in.
 Net Weight... 0.076 lb., max.

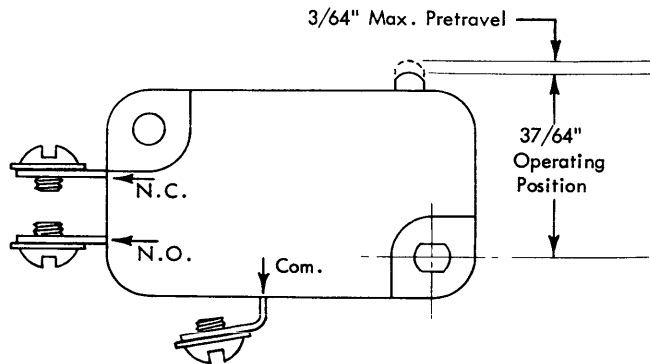
2RW4 (without coil spring)
 1/4 to 1 oz.
 1/4 oz. nominal
 3/8 in., max.
 3/16 in., min.
 0.016 to 0.078 in.
 0.075 lb., max.

Coil Spring Optional

"W" switches are available either with or without an auxiliary coil spring under the lever. This coil spring stiffens the lever action and improves the resistance of the switch to vibration. Without the coil spring this switch is extremely sensitive in respect to operating force.

The lever may be bent for adjustment.

Part Number 228093



Characteristics

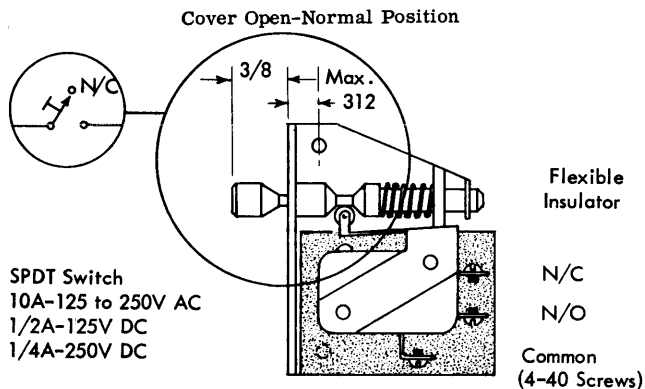
Operating Force- 8 oz; max.
 Release Force- 2 oz; min.

Differential
 Travel- .006 to .016 in.
 Overtravel- .031 in; min.

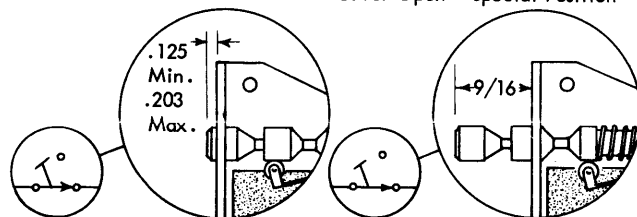
Ratings

- 5.0A- 125-250 VAC (UL Listed)
- 5.0A- 30 VDC
- Resistive
- Inductive*
- Motor**
- .5A - 125VDC (UL Listed)
- .25A 250 VDC (UL Listed)

Switch, Cover Interlock



Cover Closed - Normal Position Cover Open - Special Position



Toggle Switches

Part No.	Poles or Circuits	Current Ratings			Max. Voltage to Ground (3)	Average Toggle Actuating (4) Force	Expected Life (5)
		Steady State (1)	Non-Inductive	Induc-Induc- (2)			
121-756	SPST		6A 125V 3A 250V				
309-749	DPST	15A	6A 125V 3A 250V		600V	15 oz	
128-455	DPDT		6A 125V 3A 250V				
817-779	DPDT Center Off		10A 250V				
340-517	Momentary SPST N/O	10A	6A 125V 3A 250V	2A 50V	750V	21 oz	166000 266000
276-30	Two Circuit		6A 125V 3A 250V				

S= Single D= Double P= Pole T= Throw

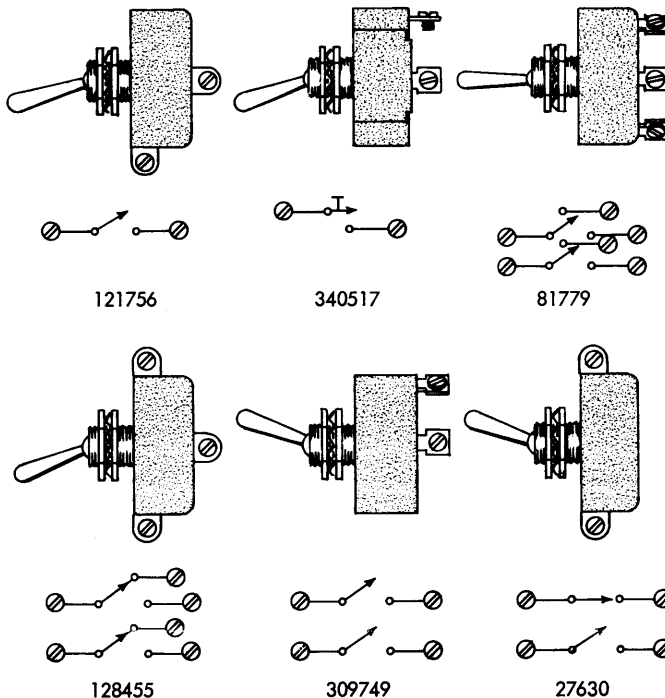
1. Maximum allowable RMS or DC (I^2R) current for a temperature rise of 30 degrees C or less.

2. For R/L values of

3. Maximum continuous Sinewave RMS voltage which may exist between the terminals and the non-current carrying metallic parts.

4. An average force of 15 to 21 ounces is recommended where high rates of operation are expected. This helps to prevent bruising the operator's finger.

5. Number of complete cycles of operation to first failure; and average number of operations of all samples tested. Occasionally one sample will have extremely long or short life and will not be included in the information above. Life may be defined as mechanical or electrical failure with the load shown in the "Inductive DC" column.



Operator's Panel Neons and Lights

Check all neons and lights for correct operation. If neon does not light after changing bulb check neon inverters below right hand resistor panel

Operator's Panel Operating Keys

Enter Quotient. With the machine in manual status the enter-quotient and operator's panel entry keys are used to enter any 36-bit binary number into the MQ register. The MQ register neons show the information which is contained in the MQ. The enter-quotient key is inoperative when the machine is in automatic status.

Enter Instruction. With the machine in manual status and the I/O interlock off, depressing the enter-instruction key will perform any legitimate instruction entered on operator's panel entry keys. The contents of the instruction counter will remain unchanged when any but a transfer type of instruction is executed. The key is not effective with the machine in automatic status.

Display Storage. The display-storage key is capable of displaying, in the storage register, the contents of any address in core storage regardless of what the contents may be. Under no circumstances is the display-storage key capable of modifying the contents of any storage location. This key is effective only when the machine is in manual status and the I/O interlock is off.

Display Index. The display index keys is capable of displaying, on the index register neons of the operator's panel, the contents of the index register associated with the name of the key (A, B or C).

The information remains on the neons until the machine is put into automatic status, another manual operation using an index register is performed, or the reset key is depressed. The contents of the index register does not affect the accuracy of the display. Depressing the display index keys does not modify the contents of any index register. These keys are effective only when the machine is in manual status and the I/O interlock is off.

Display Effective Address. This key is depressed to display in the address portion of the storage register the address portion of the instruction located in the storage register, immediately previous to depressing the key, modified by the contents of the index register designated in the instruction word. The accuracy of the effective address displayed is not affected by the contents of the address or tag portions of the instruction or the contents of any of the index registers. Depressing this key does not change any core storage location or index register. This key is effective only when the machine is in manual status, the I/O interlock is off, and no index register is being displayed.

Single Step. The single-step key is depressed once to execute the instruction located in core storage at the address which appears in the instruction counter immediately before the key was depressed. The machine stops after the execution of a single instruction, unless that instruction is an input-output instruction in which case the machine continues to execute the stored program until the I/O interlock is turned off. The instruction counter is advanced or modified by the execution of an instruction with the single-step key the same as it is when the instruction is performed in automatic operation. The single-step key is effective only if the machine is in manual status, the I/O interlock is off, and the program stop, I/O check, and card machine blown-fuse triggers are off.

Multiple Step. The multiple-step key held depressed results in a series of single-step instruction executions. All specifications for single-step operation apply, except that the machine does not stop until either the multiple-step key is released, or a program or check stop occurs. The frequency of instruction execution is 2+1 instructions per second.

Normal Off. The normal-off key is depressed to immediately remove all DC and all regulated AC voltages from the power distribution frame. Blower motors continue to run for 9+1 minutes after the normal-off key has been depressed. At the end of this time the unregulated AC voltages are no longer applied to the power distribution frame and the blowers stop.

Power On. Within 9+1 minutes after depressing the power-on key, all AC and DC voltages and the ready light are on.

DC-Off. The DC-off key is depressed to remove all DC but no AC voltages from the power distribution frame.

DC-On. Within 2+.5 minutes after depressing the DC-on key, all DC voltages are present at the power distribution frame.

Reset. The reset key is capable of turning off any microsecond delay unit or trigger whose neon or incandescent indicator appears on the operator's panel, except the power light. The ready light is on and the automatic light off as a result of the reset. When the reset key is depressed, -250 volts is removed from all -250 reset lines in the machine for a period of 200+40 milliseconds. This reset affects neither the contents of core storage nor the machine clock.

Clear. With the machine in automatic status, the clear key is depressed to perform all the functions of the reset key and, in addition, resets the machine clock and resets all core storage locations to 0's. This key is not effective when the machine is in manual status.

Load (Cards, Tape, Drum). Any of the load keys are depressed to reset the instruction counter, the address register, EOR

and EOF interlocks, the program stop and I/O check indicators. All other indicators remain unchanged. The load keys are effective only when the machine is in automatic status.

Start. The start key is capable of resetting the EOR and EOF interlocks, the card machine blown-fuse trigger and the program-stop and read write check indicators. This resetting function is effective any time the machine is stopped, regardless of the status of the automatic-manual switch. When the machine is in automatic status, the start key is also capable of resetting the master stop trigger.

Test Panel Switches

Check each toggle switch for make and break of the circuit it controls.

704.14.07 Test Panel Receptacles and Sockets

Make sure that there are no broken wires or bent or broken prongs.

704.14.08 Relay Gate

Duo-relay Visual Check

Make the following visual check of duo-relays:

1. Secure the core firmly to the frames.
2. Check for loose or burned contact points.
3. Check contact point alignment; Points should be aligned both vertically and horizontally.
4. Make sure that contact pile holding screws are tight.
5. Clean contact points by removing loose dust with a wire brush, caked or oily dust by flushing with IBM cleaning fluid, and film from points by burnishing with the metallic burnishing tool.
6. Remove armature to check for a worn, sticking, or damaged armature pivot pin. It must turn freely in the armature ears. Worn pivots affect the amount of rise and point wipe lost. Saturate a pipe cleaner with light oil and draw it through the pivot holes in the armature to remove the foreign matter and lubricate the pivot points.
7. Remove foreign particles between armature and magnet core and between armature and brass stop pin.
8. Lubricate the armature pad with a small amount of light oil at the point where the contact pedestals rest on the pad. This prevents wearing of the pad and the accumulating of reddish dust at this point.

Wire Contact Relay Visual Check

Make the following check:

1. Check the relay contact terminal prongs. They should be clean and in alignment with each other.
2. Check the contact spring of the relay terminal receptacle on the relay gate. These springs must have sufficient tension to insure good electrical contact. If they are burned, have lost their tension, or are badly bent they must be replaced. To remove, use relay puller tool No. 45065. The tool is attached to the relay and the pulling motion is straight out.
3. Check the relay contact wires for burned or pitted conditions and replace any bad wires.
4. Apply one drop of light oil to the latching surfaces of the latch and armature. Apply a drop of light oil at both pivot points of the latch armature.

Relay Gate Cables

Check cables to the relay gate for any that are too tight or for worn or damaged insulation.

704.14.09 Resistor Panel and Transformers

Resistor Panel

Check resistors for loose connections and for any operating at extreme temperatures. If temperature seems abnormal, cut off power and check resistance with an ohmmeter.

Filament Transformers

Check transformers for loose connections and also for any accumulation of dirt or red rust in the immediate area.

704.14.10 Rectifier

This rectifier is used for 40v supply to pick relays in the operator's panel. Check the voltage across the relays for 40v and visually check for hot spots, burned plates, and blown-out expansion plugs on capacitors around the rectifier.

704.14.11 Master Oscillator Assembly

Check to make sure that in turning the control varies the frequency of the clock. Test the machine monthly for correct machine operation of the main frame diagnostic at both 920KC and 1090KC.

When the machine is installed, check approximate positions on the scale to reach 920 KC and 1090 KC. In frequency biasing afterwards, if these points change greatly, it may indicate approaching trouble. Occasionally, block test the tubes in the oscillator.

704.14.13 Block Tube Testing

Block test only after biasing and pulse checking fail to locate general failures. An occasional visual check should be made for open filaments on the parallel cathode follower.

704.14.14 Vibration Checking

Vibration testing should only be done where no other means of locating a trouble can be accomplished. Vibrate only the trouble area and check for any other troubles put on in vibrating. See "vibration checking" in core storage Section 737.14.14 for testing of 6136 tubes. However, the 704 CPU must be capable of performing all normal operations without failure, while the pluggable units and pluggable unit panels are vibrated sufficiently to cause the failure of faulty electrical components and connections.

Vibration should only be done by tapping the tubes lightly with your finger or the eraser of a pencil. Vibrating any harder usually puts on more troubles than can be shown up by vibration.

704.14.15 Pulse Checking

A scheduled procedure must be set up to check on critical and important pulses. These pulses and shapes will be found in Section 704.15.00, "Waveforms and Levels." Refer to that section for any scope setups, shapes, levels and test points needed.

704.15.00 WAVEFORMS AND LEVELS

704.15.16 Marginal Checking

One minute of error free operation shall be obtained at each bias voltage limit while the CPU is operating a suitable diagnostic using all the main frame instructions.

Nominal Voltage	Recommended Test Limits	
+150V	+142 + 1 Volt	+162 + 1 Volt
+220V	+198 + 1 Volt	+242 + 1 Volt
-250V	-230 + 1 Volt	-263 + 1 Volt
-100V	- 90 + 1 Volt	-110 + 1 Volt
- 30V	- 33 +.5 Volt	- 27 +.5 Volt

704.15.19 Special Pulse Specifications

Inverted Sync Pulse

The Inverted Sync Pulses and Inverted Clamp Pulses should meet all requirements of Figure 15-1 and Figure 15-2.

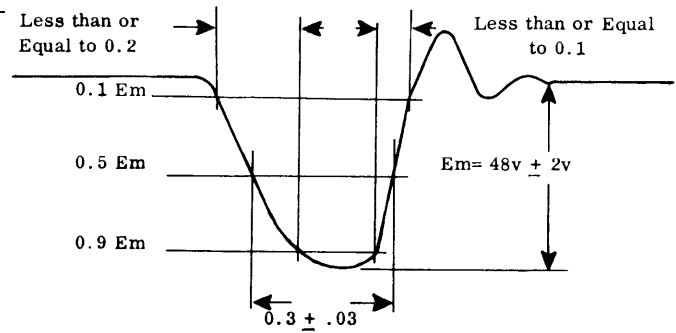


Figure 15-1

Inverted Clamp Pulse

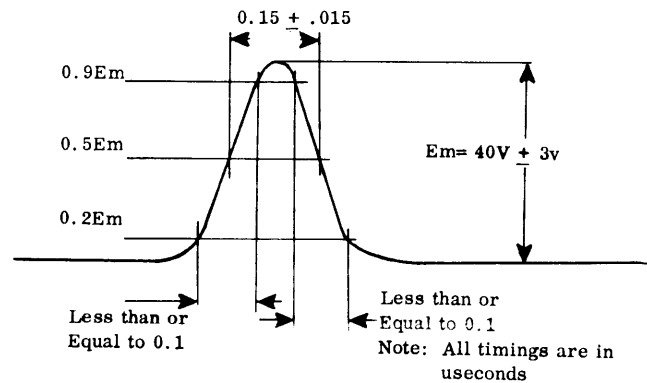


Figure 15-2

Clock Drive Pulse

Clock Drive Line Pulses should conform to the specifications of Figure 15-3, when observed at the termination of the associated coax line.

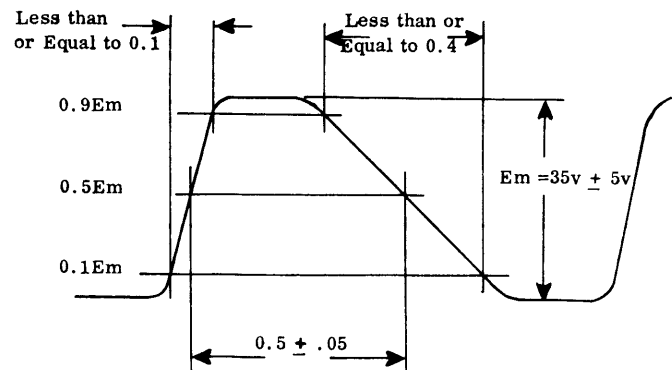
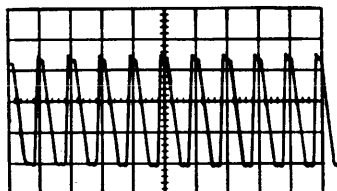


Figure 15-3

704.15.50 Oscillator Output

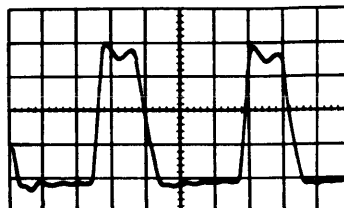
A.



MF2-K39-1
1 usec/cm
Sync - MA0

8.06.02
10 Volts/cm

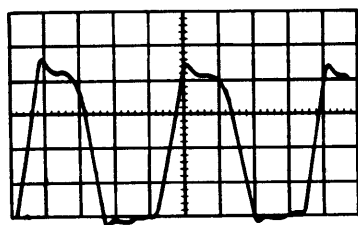
B.



MF2-L40-2
.2 usec/cm
Sync - MA0

8.06.02
10 Volts/cm

B.

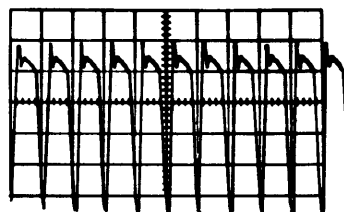


MF2-K39-1
.2 usec/cm
Sync - MA0

8.06.02
10 Volts/cm

704.15.52 Inverted Sync Line

A.

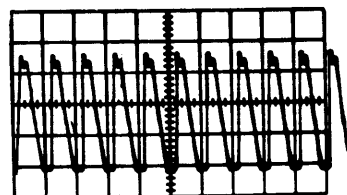


MF2-R40-6
1 usec/cm
Sync - MA0

8.06.02
10 Volts/cm

704.15.51 Sync Clamp Output

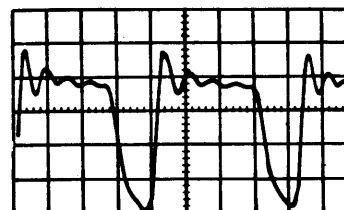
A.



MF2-L40-2
1 usec/cm
Sync - MA0

8.06.02
10 Volts/cm

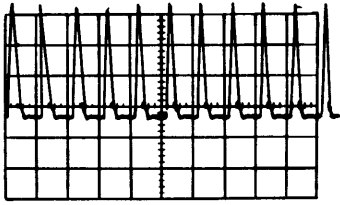
B.



MF2-Q30-2
.2 usec/cm
Sync - MA0

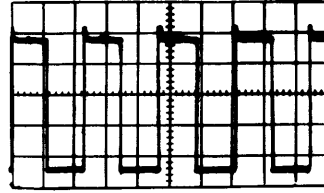
8.06.04
10 Volts/cm

704.15.53 Inverted Clamp Line
A.



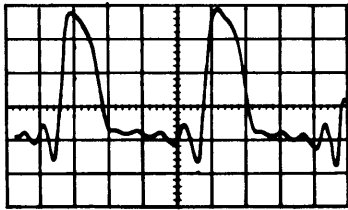
MF2-R39-1 8.06.03
1 usec/cm 10 Volts/cm
Sync - MA0

704.15.55 Master I Time



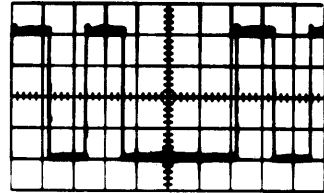
MF1 - A18-4 8.05.04
10 usec/cm 10 Volts/cm
Sync - MA0
0000 TRA (0000)

B.



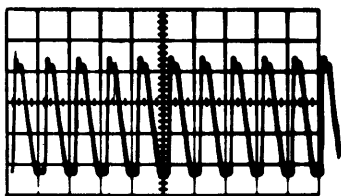
MF4-H36-5 8.06.04
.2 usec/cm 10 Volts/cm
Sync - MA0

704.15.56 Master E Time



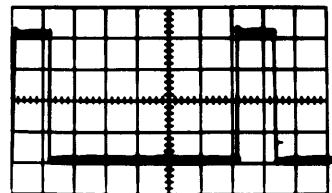
MF1-CB-2 8.05.04
10 usec/cm 10 Volts/cm
Sync - MA0
CLA (0000), ADD (0000), TRA (0000)

704.15.54 Clock Drive



MF2-R39-6 8.06.03
1 usec/cm 10 Volts/cm
Sync - MA0

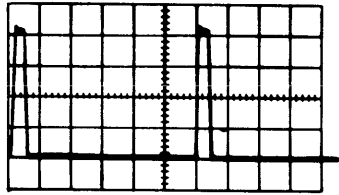
704.15.57 Master ER Time



MF1 -B18-6 8.05.04
10 usec/cm 10 Volts/cm
Sync - MA0
CLA (0000), ADD (0000), TRA (0000)

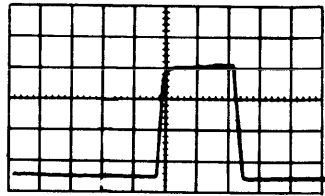
704.15.58 Clock Pulses

A. A0



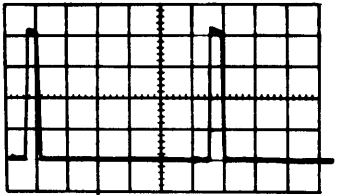
MF1-P13-1 8.04.01
 2 usec/cm 10 Volts/cm
 Sync - MA0

B. E9 to CT2



MF1-B09-1 2.09
 2 usec/cm 10 Volts/cm
 Sync - MA0

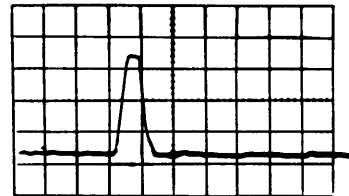
B. A1



MF1-M13-1 8.04.01
 2 usec/cm 10 Volts/cm
 Sync - MA0

704.15.60 Instruction Counter

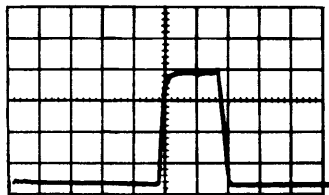
A. Advance



MF2-P08-3 3.20
 1 usec/cm 10 Volts/cm
 Sync - MA0

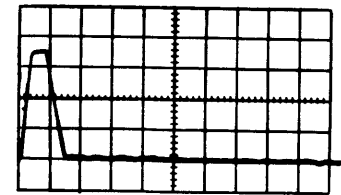
704.15.59 Pulse and Gate Generator

A. I9 to CT1



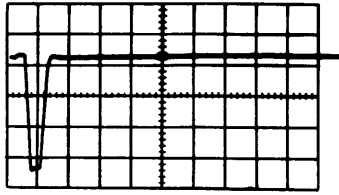
MF1-A13-7 2.09
 2 usec/cm 10 Volts/cm
 Sync - MA0

B. Pos (17) Binary Input



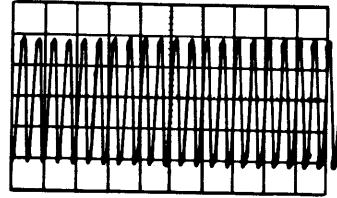
MF3-M22-2 3.20
 1 usec/cm 10 Volts/cm
 Sync - MA0

704.15.61 Gated Minus on A0 (D1)



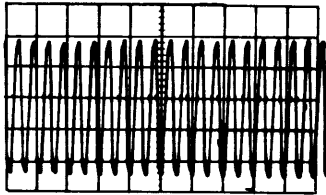
MF3-M22-2 3.40
 1 usec/cm 10 Volts/cm
 Sync - MA0

704.15.63 Tally Counter Drive
 A.



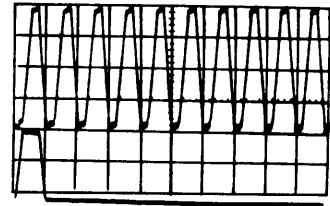
MF1-C12-6 8.04
 5 usec/cm 10 Volts/cm
 Sync - MA0

704.15.62 Shift Counter Drive
 A.



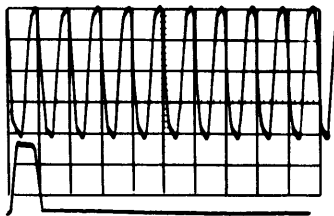
MF1-E12-5 8.04
 5 usec/cm 10 Volts/cm
 Sync - MA0

B. Tally Counter Drive Over
 Sync Pulse



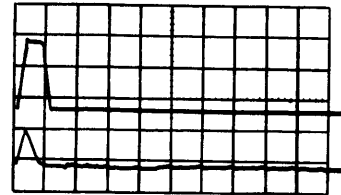
MF1-E12-5 8.04
 1 usec/cm 10 Volts/cm
 Sync - MA0 20 Volts/cm

B. Shift Counter Drive Over
 Sync Pulse



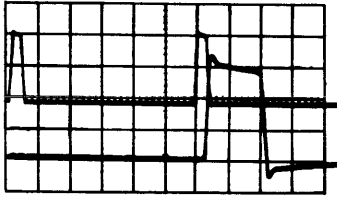
MF1-E12-5 8.04
 1 usec/cm 10 Volts/cm
 Sync - MA0 20 Volts/cm

704.15.64 Sync Pulse Over Binary
 Input to Shift Counter (17)



MF3-C28-7 3.05
 1 usec/cm 20 Volts/cm
 Sync - MA0

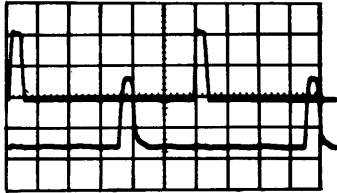
704.15.65 Sync Pulse Over Conditional Transfer Cntl.



MF1-B26-1 2.07.02
 2 usec/cm 10 Volts/cm
 Sync - MA0 20 Volts/cm

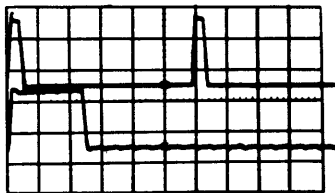
704.15.66 Routing Lines

A. Storage Register to Adders Under Sync Pulse



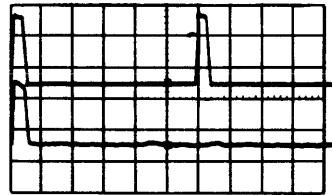
MF1-H35-6 2.08.05
 2 usec/cm 20 Volts/cm
 Sync - MA0

B. Storage Bus to Storage Register Under Sync Pulse



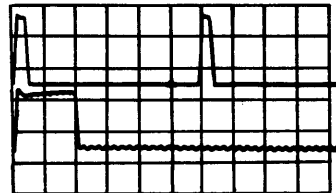
MF1-Q33-6 2.08.01
 2 usec/cm 20 Volts/cm
 Sync - MA0

C. True Accumulator to Adders Under Sync Pulse



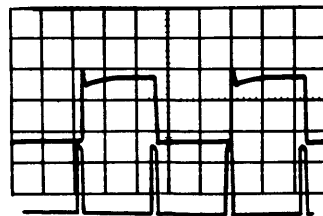
MF3-C35-4 2.08.06
 2 usec/cm 20 Volts/cm
 Sync - MA0

D. Adders to Accumulator Under Sync Pulse



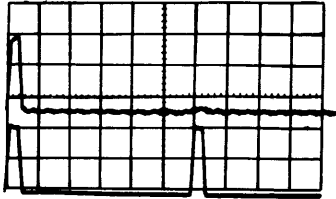
MF1-H32-5 2.08.09
 2 usec/cm 20 Volts/cm
 Sync - MA0

E. Index Registers to Adders Over Sync Pulse



MF4-B22-5 2.08.49
 2 usec/cm 20 Volts/cm
 Sync - MA0

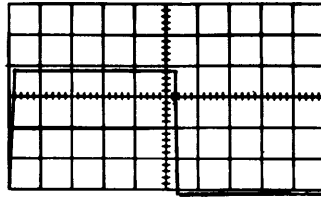
F. End Operation



MF1-L27-7 2.08.31
 5 usec/cm 20 Volts/cm
 Sync - MA0

704.15.68 Key Operations

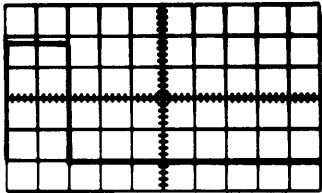
A. Single Stop



MF4-G21-2 4.07
 200 usec/cm 10 Volts/cm
 Sync - Int.

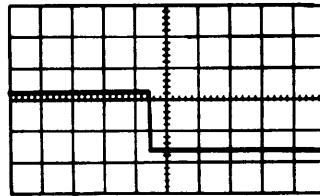
704.15.67 Interlock Reset

A. Load



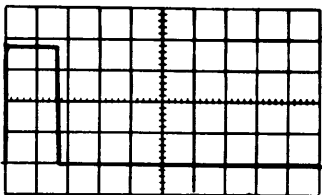
MF4-G23-6 4.05.01
 500 usec/cm 10 Volts/cm
 Sync - Int.

B. Enter Instruction



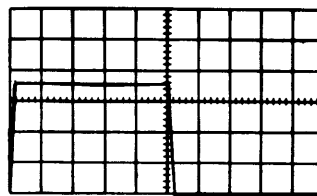
MF4-D29-1 4.17
 20 msec/cm 20 Volts/cm
 Sync - Int.

B. Start



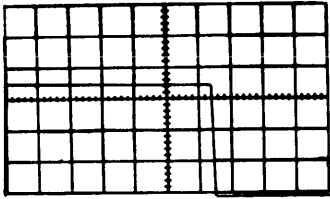
MF4-B26-7 4.08
 500 usec/cm 10 Volts/cm
 Sync - Int.

C. Storage Display



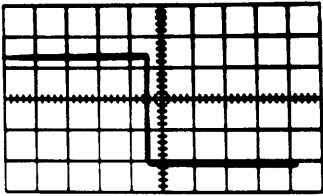
MF4-C20-4 4.18
 20 msec/cm 10 Volts/cm
 Sync - Int.

D. Turn Off Master Stop Trigger
From Start Key



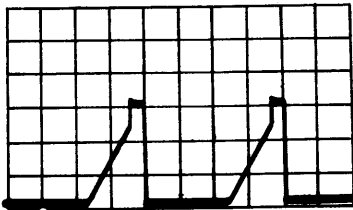
MF4-023-1 4.05.01
200 usec/cm 10 Volts/cm
Sync - Int.

704.15.69 Start Bias Reset



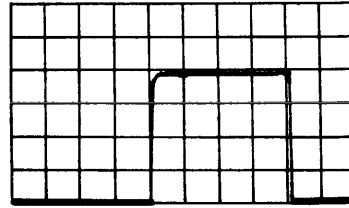
MF4-F26-1 4.08
50 msec/cm 10 Volts/cm
Sync - Int.

704.15.70 Sync Pulse Used
On Rd/Wr



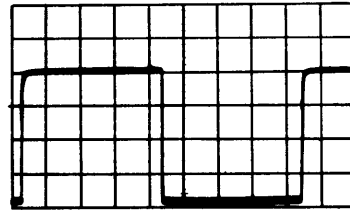
MF4-M01-8 5.11.01
100 usec/cm 10 Volts/cm
Sync - Fall of test Point M01-8
lower leg of AND ckt A

704.15.71 Card Control Ring
A. Even Ring Drive



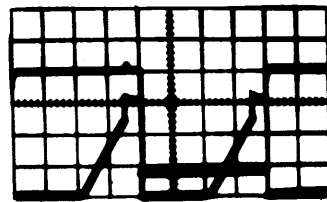
MF4-N01-8 5.11.01
100 usec/cm 10 Volts/cm
Sync - M01-8

B. Odd Ring Drive



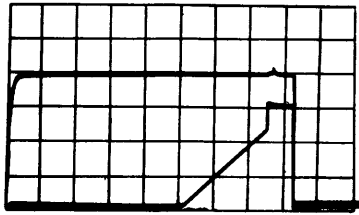
MF4-P01-3 5.11.01
100 usec/cm 10 Volts/cm
Sync - M01-8

C. Even and Odd Drive Relationship
to Sync Pulse



MF4-P01-3 5.11.01
100 usec/cm 10 Volts/cm
Sync - M01-8

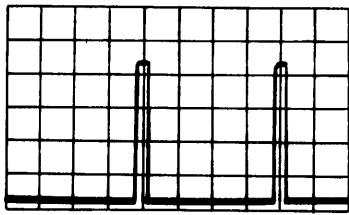
D. Even Ring Drive Relationship to Sync Pulse



MF4-N01-8 5.11.01
 100 usec/cm 10 Volts/cm
 Sync - M01-8

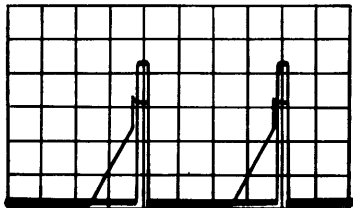
705.15.72 Rd/Wr Pulse

A.



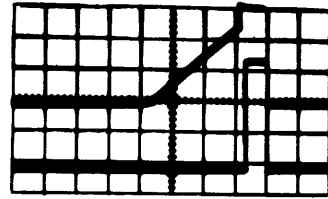
MF4-L01-2 5.11.01
 200 usec/cm 10 Volts/cm
 Sync - M01-8

B. Rd/Wr pulse Over Sync Pulse



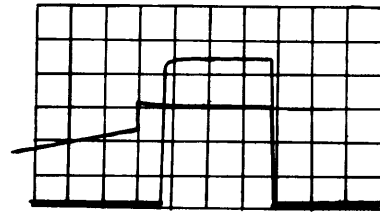
MF4-L01-2 5.11.01
 200 usec/cm 10 Volts/cm
 Sync - M01-8

C. Rd/Wr Pulse Over Sync Pulse



MF4-L01-2 5.11.01
 100 usec/cm 10 Volts/cm
 Sync - M01-8

D. Rd/Wr Pulse Over Sync Pulse



MF4-L01-2 5.11.02
 20 usec/cm 10 Volts/cm
 Sync - M01-8

SECTION	TITLE	PAGE
704.20.00	CORRECTIVE MAINTENANCE	20-2
704.21.00	Removals	20-2
704.21.02	Filters	20-2
704.21.03	Blowers and Motors	20-2
704.21.06	Operation Panel	20-2
704.21.11	Master Oscillator Assembly	20-2
704.22.00	Adjustment and Timings	20-2
704.22.06	Operator's Panel	20-2
704.22.08	Relays	20-3
704.22.09	Bleeder Resistors	20-5
704.22.11	Master Oscillator Assembly	20-5

704.21.00 REMOVALS

704.21.02 Filters

Main Frame

Remove back covers from panels. Filters can be lifted out after the holders are unscrewed.

Right-Hand Resistor Panel

The lower right-hand cover must be removed to unlatch the relay gate and pull it open. The filter can now be lifted out.

704.21.03 Blowers and Motors

CPU

The motors and blowers are held to the base by four bolts. These bolts must be removed from the under side of base after the filters are removed.

Right-Hand Resistor Panel

The blower and motor are held to the base by four bolts which are accessible from the rear of the panel.

704.21.06 Operation Panel

This panel is held to the main frame by two hinges. An arm extending to the top of panel holds the panel in position.

Keys and Key Assembly. The keys are held to the key assembly by a small four-fluted bristol screw. Remove the bristol screw from the key lever and pull it off. The front covers of the

key assemblies are held to the base by screws. Each key assembly is held in place to the base by four screws. Remove four screws from the rear side of the key assembly and remove from rear of the panel.

Button and Switch Button Assembly. Loosen the hex nut in the rear of the panel on the button assembly. Push the assembly to the front and remove the button by loosening the set screw in the button. Remove the button assembly from the rear of the panel.

Neon Assembly. Remove the screw at the back of the panel and remove the complete neon assembly to replace a neon.

Lamp Assembly. Remove the cover of the light by inserting a screw driver. Pull out the lamp from the front of the panel.

704.21.11 Master Oscillator Assembly and Crystal

Remove the input and output cables. Remove the screw at the top, letting unit drop down on its hinges. Remove the four screws in the hinges, and the complete assembly can be removed. Four screws in each end can be removed to take the covers off the assembly.

704.22.00 ADJUSTMENTS AND TIMINGS

704.22.06 Operator's Panel

Key Blank and Key Switch Assemblies. There should be .015-.020" air gap on n/o points and n/c points when they are transferred. There should be 30-35 grams' strap tension on the n/o and n/c points.

Button and Switch Assembly. Check to see the operation of the button or switch is completed when it is operated. For a complete writeup on switches as used on the operator's panel, refer to 704.14.06. Some ratings of microswitches are given in the following chart.

CURRENT RATINGS, BASED ON FOLLOWING CONTACT LIFE RATINGS:							
Conservative Minimum Contact Life -- 25,000 Operations							
Probable Contact Life -- 50,000 Operations							
INDUCTIVE LOADS					NON-INDUCTIVE LOADS Sea Level to 50,000 Ft. Incandescent Filament, Maximum Heated Filament Load		
		Max. Continuous Current Rating	Max. Permissible Starting Inrush				
DC Volts	Contact Break Distance	Sea Level to 20,000 Ft.	Normally Closed Contacts	Normally Open Contacts	Heater Loads	Normally Closed Contacts	Normally Open Contacts
Volts		Amperes	Amperes	Amperes	Amperes	Amperes	Amperes
6	.070 in.	25	40	20	25	3	1.5
to	.036 in.	25	40	20	25	3	1.5
8	.020 in.	25	40	20	25	3	1.5
12	.070 in.	25	40	20	25	3	1.5
to	.036 in.	25	40	20	25	3	1.5
14	.020 in.	15	40	20	25	3	1.5
24	.070 in.	20	40	20	25	3	1.5
to	.036 in.	10	40	20	10	3	1.5
28	.020 in.	5	40	20	6	3	1.5
110	.070 in.	0.4	40	20	1	1.0	1.0
to	.036 in.	0.2	40	20	0.6	0.6	0.6
115	.020 in.	0.05	40	20	0.5	0.5	0.5
220	.070 in.	0.2	40	20	0.4	0.4	0.4
to	.036 in.	0.1	40	20	0.3	0.4	0.4
230	.020 in.	0.03	40	20	0.25	0.4	0.4

Current ratings are based on a maximum permissible temperature rise of 30° C, a value which is generally employed in rating by the Underwriters' Laboratories. A maximum of 25 amperes of continuous loading will produce a temperature rise that will not exceed 30° C.

Ratings are based on a "make-and-break current" cycle of 8 per minute. The term "conservative minimum contact life" is an arbitrary definition which, in the case of direct current ratings, means a value so selected that almost all switches tested under the given conditions will display substantially longer contact life values than the given value. With the exception of an extremely small group of cases, the value of minimum contact life may be considered the practical minimum value of contact life under rated life.

704.22.08 Relays

Duo Relay Adjustments

Armature Freeness. The armature should be free on its pivot pin with a slight end play of .010" ± .006". The pivot pin and ears of the armature should be free of burrs. Bend the armature ears to adjust for end play.

Armature Squareness. With the armature held in the attracted position, the residual pin should rest squarely against the core face and the armature should be parallel with the core face.

Residual Pin. The residual pin should project .005" (+.005", -.002") from the armature. Check this by inserting the required thickness gauge between the fully attracted armature and core on each side of the residual pin. In all cases a .003" gauge should be free and a .010" gauge should not go. This is also the method to check armature squareness.

Armature Air Gap. This is one of the most important relay adjustments, for any deviation affects pickup and drop-out time. Variations in this adjustment may improve operations in one application but cause failures in another. A specific air gap dimension is determined for proper operation on all applications for which a duo relay is selected to operate. For special applications, decreasing the air gap will decrease the pickup time and increase the drop-out time, and increasing the air gap will increase the pickup time and decrease the drop-out time.

Duo relays are of two general types, single core and double core. Several different air gap dimensions are specified below for the relays within these two classifications.

With the armature in the fully de-energized position, insert the specified thickness gauge completely through the residual to measure the gap. To adjust, bend the armature at the 90° turn.

The armature core air gap dimensions for double-core relays are measured between the armature and the lower core. With the armature fully attracted there should be .003" to .005" clearance between the armature and upper core.

Relay Type	Measured Through Air Gap	Remarks
1. Single Core	.013" (+000", -.001") .016" (+000", -.002") .021" (+000", -.003")	
2. Double Core a. Lower Core b. Upper Core	.028" (+000", -.003") .036" (+000", -.003") .004" (±001")	Measured at lower core Measured at lower core Measured at upper core (Clearance, no residual)

Copperplated Armature. Some duo relays use a copperplated armature with no residual instead of the cadmium-plated type. Copperplated armatures are used because:

1. The copperplating tends to limit the formation of "red rust" in the armature pivot holes, thus preventing freezing of the pivot pin to the armature.
2. Removing the residual pin eliminates variations in armature travel and in residual magnetism effects due to flattened residual pins. The residual pin effect is provided by using a brass screw and a brass washer to hold the core and yoke together.

The armature-core air-gap dimensions are the same in either type of armature. Measure the air-gap dimensions by inserting the thickness gauge completely through the core face. However, do not replace the copperplated armature with a cadmium plated armature (with residual pin) unless the brass screw and washer are replaced with a standard screw.

Relay Contact Points. Most relay contact points are made of solid silver but some are made of tungsten. Silver points are generally used where the pressure is light, and the point is not breaking a heavy current. Tungsten points are generally used where the pressure is heavy, and the point is breaking a heavy current circuit. Silver points tarnish and appear black and dirty. This does not cause trouble normally, for the tarnish is conductive.

Maximum current and voltage capacities for a duo-relay contact point are 5 amperes at 130 volts. Contacts are mounted on duo relays in two piles. Facing the armature side of the relay, the pile to the left is the A side with an AU and AL contact point. The pile to the right is the B side with a BU and BL contact point. Before checking and adjusting the contacts, it is absolutely necessary that the armature-core air-gap dimensions be adjusted and that the residual pin be checked for proper projection.

The method used to adjust the contact points of a duo-relay is:

1. Insert the specified thickness gauge between armature and core and press on the armature to hold the thickness gauge in place.
2. Holding the armature in this position, adjust all contact point air-gaps for a minimum clearance (.001" to .002") between points. Points should not touch but the slightest perceptible movement should cause them to touch.
3. Remove the adjustment gauge and check the making and the breaking conditions of the points with the armature in both the energized and de-energized positions. In the energized position the n/o point stationary strap, should be lifted approximately .010" off supports or have enough flex to insure good contact. The n/c points should have an air gap of .012" to .020". In the de-energized position the n/o points should have an air gap of .012" to .020". For n/c points, the stationary strap should be lifted approximately .010" off the support strap.

Transfer Contact Check. In checking transfer contact point operation be sure the normally closed points break before the normally open points make.

Contact Strap Tension. Tension on the operating straps is 15 to 20 grams of pressure measured with a gram gauge on the tip of the contact point. Tension on the stationary points are 25 to 35 grams for fast operating relays and 45 grams for slower operating relays, measured at the tip of the operating contact.

Anti-Bounce Bumper Straps. Adjust the bumper straps so that the contact strap just touches the bumper when the armature is fully attracted.

Wire Contact Relay

Pickup and Drop-out Time. The pickup time is considered as 6 milliseconds for all wire contact relays in the 704 system. The drop-out time is 4 milliseconds for all wire contact relays.

Adjustment Procedure

1. The contact air gap is machined to .025" + .001" and should not be adjusted. Adjust for a .003" to .005" clearance air gap between the armature and core with the armature attracted. This adjustment is made by forming the center section of the armature. The residual must be flat against the face of the yoke and the armature and core must be free from dirt or metal chips. There must be about .050" travel at the free end of the armature.
2. With no wire tension on the armature, the compression spring must exert 8 to 12 grams of tension measured on the free end of the armature.
3. The contact wires must be positioned near the center of the contact. Armature end shake must not let the wires reach the edge of the contact.
4. Adjust tension on the contact wires by shifting the wire holder so that a 50 gram pressure applied at the center of the free end of the armature is needed to move the wires away from the contacts of the n/c side. A 70 gram and 130 gram pressure is needed on the 6 and 12 position relays, respectively.
5. Adjust the magnet yoke assembly so that with a .010" thickness gauge between the armature and yoke at the free end

of the armature, and the armature attracted, all contact wires make contact on the n/o side. With a .015" thickness gauge inserted and the armature attracted, none of the wire must make contact on the n/o side. Make this adjustment by moving the yoke assembly at the lower end so that the wire holder adjustment will not change.

6. Adjust the damper screw to allow .005" to .010" movement between the vinylite damper and the wire bracket before the wire bracket can move any contact wires.

Latch Type Wire Relays

Adjustments

1. The adjustments are the same as for the non-latch type except on adjustment 5 above; with .015" the wires make contact and with .020" the wires do not make contact.
2. With the relay coil energized there is .003" to .005" latching clearance between the relay armature and the latch at the latching point. To adjust, add or remove shims between the relay magnet yoke and latch magnet yoke.
3. With the latch magnet energized the latch armature must clear the relay armature by .003" to .006" at the latch point. Minimum clearance of .010" is checked between the bottom of the latch armature and the relay moulding. Make this adjustment by forming the latch.
4. With the relay armature in the latched position, the point of contact of the latch is 90° to the armature residual.
5. Pressure of 25 to 40 grams on the core end of the latch armature must release the relay armature. Pressure of 100 to 125 grams would be needed in a six position relay.

Duo Relays and the Adjustments Used on the 704 Relay Gate

Relay Position Number	Relay Part Number	Armature Core Air Gap Through	Contact Adjustment	Operating Time in Milliseconds	
				Pickup	Drop-out
50	282745	.016	.010	20-26	2-4
51	281077	.020	.012	17-23	2-4
52	281077	.020	.012	17-23	2-4
53	281077	.020	.012	17-23	2-4
54	111401	.021	.012	16-20	3-6
55	111401	.021	.012	16-20	3-6
56	206672	.017	.010	16-20	3-5
57	111351	.021	.012	12-16	3-5
58	121841	.016	.010	17-23	3-5
59	281077	.020	.012	17-23	2-4
61	111351	.021	.012	12-16	3-5
62	111351	.021	.012	12-16	3-5
63	281077	.020	.012	17-23	2-4

704.22.09 Bleeder Resistors

The slide resistors which are used for bleeder resistors in the -30v and +15v power supplies are located in both the front and back side of the right hand resistor panel. The resistor numbers are found on Systems Diagrams, 9.29, sheet 4 of 5. The method of using the resistors in circuit logic is found in Systems Diagrams, 9.29, sheet 1 of 5. Numbers 2-25 are located on the outside of the resistor panel and 32-60 are located on the inside of the resistor panel.

There are several methods used in adjusting these adjustable slide resistors. In the chart below is given the ohmic resistance from the slide terminal to ground. This value is pre-set before power is applied. After power is brought up, a good DC meter is used and the slide can be adjusted slightly to get either the +10v or -30v output. The adjustment should be slight from the original setting and must be done only with power down. Under no circumstances will the slide be adjusted more than halfway toward the ground end of the resistor to get the +10v output.

Another method that may be used is to set the slide resistors for minimum resistance and then measure the voltage at the input terminal. Be sure the voltage supply is adjusted so the input is very close +15v or -30v. Adjust the slide for the exact voltage needed for the output. Again be sure the slide is never adjusted past the halfway point toward the ground end for the +10v output.

Resistor Number	Res. Value	Adj. Value	Remarks
2 } Series	10 ohms	Fixed	-30 volts
3 } Series	10 ohms	Fixed	-30 volts
4 } Parallel	50 ohms	44 ohms	-30 volts *
5 } Parallel	50 ohms	44 ohms	-30 volts *
7 } Series	10 ohms	Fixed	-30 volts
8 } Series	5 ohms	Fixed	-30 volts
9	25 ohms	21.4 ohms	-30 volts
10	25 ohms	Fixed	-30 volts
12 } Series	50 ohms	Fixed	-30 volts #
13 } Series	25 ohms	64.2 ohms	-30 volts #
14 } Series	50 ohms	Fixed	-30 volts #
15 } Series	5 ohms	53.2 ohms	-30 volts #
25 } Series	25 ohms	Fixed	-30 volts #
19 } Series	25 ohms	43.6 ohms	-30 volts #
20	100 ohms	Fixed	-30 volts
32	5 ohms	3.3 ohms	+15 volts
33	5 ohms	3.3 ohms	+15 volts
34	10 ohms	6 ohms	+15 volts
35	10 ohms	7.9 ohms	+15 volts
36	10 ohms	7.9 ohms	+15 volts
37	10 ohms	6.7 ohms	+15 volts
38	5 ohms	3.3 ohms	+15 volts
39 } Parallel	10 ohms	6.4 ohms	+15 volts *
40 } Parallel	10 ohms	6.4 ohms	+15 volts *
42	10 ohms	6.1 ohms	+15 volts
43	10 ohms	9.2 ohms	+15 volts
44	10 ohms	8.5 ohms	+15 volts
45	10 ohms	6 ohms	+15 volts
46 } Series	25 ohms	Fixed	-30 volts #
47 } Series	10 ohms	32 ohms	-30 volts #
48	25 ohms	13.9 ohms	+15 volts
49	5 ohms	3.3 ohms	+15 volts
50	5 ohms	3.3 ohms	+15 volts

Resistor Number	Res. Value	Adj. Value	Remarks
51 } Series	10 ohms	Fixed	-30 volts #
52 } Series	10 ohms	19.6 ohms	-30 volts #
53 } Series	25 ohms	Fixed	-30 volts #
54 } Series	10 ohms	29.5 ohms	-30 volts #
55 } Parallel	50 ohms	45 ohms	-30 volts *
56 } Parallel	50 ohms	45 ohms	-30 volts *
57 } Series	10 ohms	Fixed	-30 volts
58 } Series	10 ohms	Fixed	-30 volts
59 } Parallel	50 ohms	42 ohms	-30 volts *
60 } Parallel	50 ohms	42 ohms	-30 volts *

All resistors are 100 watt resistors.

Jumpers of series combination left on and resistance measured over combination.

* Jumpers of parallel combinations are removed and resistance measured over each separate resistor.

704.22.11 Master Oscillator Assembly

Occasionally check the oscillator frequency against the scope multivibrator. Even though the scope oscillator is not as accurate as the CPU oscillator, any wide variance can be seen. If one is seen to vary, check the CPU oscillator against the second scope to see whether the CPU or scope oscillator is varying.

Master Oscillator Check

The master oscillator is designed to give either a variable frequency output or a crystal controlled frequency of 1 megacycle. The crystal is located in the feedback circuit and is brought into or out of use in a manner designed to minimize irregularities in the output waveform at the time of change.

The tuning condenser forms part of the tank circuit, during the time the oscillator is crystal controlled, and must be at approximately the correct value or the crystal will not control the frequency. For this reason the dial of the condenser is provided with a notch to position it accurately during crystal control. The dial must always be in this position when changing between crystal and variable control.

A test terminal is provided on the oscillator unit for use when checking and adjusting capacity setting. To make the check attach an oscilloscope having a good response at 1 megacycle to the test point with a high impedance probe. Connection can most easily be made with the aid of a male coax connector to fit the connector on the unit.

Set the switch to "crystal," and observe the behavior of the test output while varying the frequency control dial from minimum frequency to maximum frequency. This output goes through three variations. At the start there will be a uniform output that will vary in frequency (Figure 22-1). At the time that the crystal takes control the output suddenly doubles in size (Figure 22-2). Further change of the frequency control dial will leave the frequency constant, but will cause a gradual distortion of the wave shape until the limit of the crystal control range is reached (Figure 22-3). Further change in the frequency control will again cause the crystal to lose control. Reversing the direction of rotation shows that the hold-in range is greater than the lock-in range.

To adjust the capacitor setting, allow the oscillator to run long enough to reach normal operating temperature. Lock the dial in its crystal operation position. With a small screw driver adjust the trimmer condenser located above the tuning dial to determine the settings to give the conditions in Figures 22-2 and 22-3. Adjust the trimmer to set half-way between the two settings. This will give a wave shape similar to that shown in Figure 22-4.

If for any reason the tuning dial has been removed, set the trimmer condenser to 25% of capacity. Adjust the variable frequency control capacity to locate the proper settings, keeping this setting; replace the dial so that catch falls in the notch and tighten the set screws holding the dial on the shaft. Recheck setting by varying the trimmer as described above.

The output wave shapes observed here are not the output wave shapes since the test points are located in the feedback circuit.

After the dial is set, rotate it clockwise (minimum capacity) to the limit of travel. Pointer should be between marks 13 and 17. If it is outside these limits, adjust dial to read 15 with the condenser at minimum capacity. Fasten the dial, adjust trimmer condenser to 25% of maximum capacity. Turn the dial to the lock position. Remove cover and adjust inductance of the coil by means of the core to give test output of Figure 22-4. This adjustment is not necessary for routine adjustment checks.

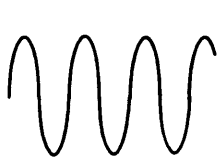


Figure 22-1

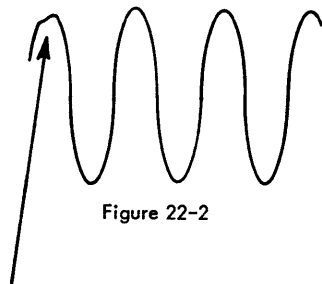


Figure 22-2

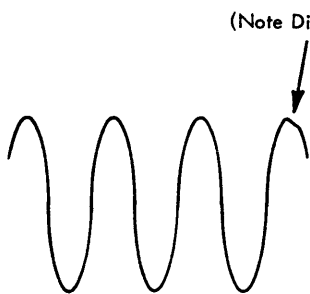


Figure 22-3

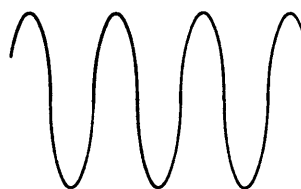


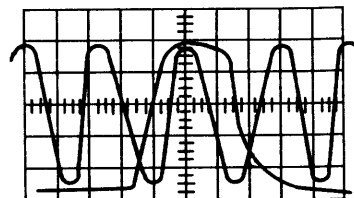
Figure 22-4

Clock Line Delay (Systems Diagram, 8.04)

Shift Counter Drive Line. This line is used to step the shift counter on Systems Diagram, 3.05. As a starting point for setting this tap in the delay unit, the input to tube A12-05A should be set 2 sections from the 1K load or pin A-18 in PU9029 MF1-A12.

Next sync scope on MF3-G21-7 (primary oper. 76 for a shift instruction). Put the machine into continuous storage read in using LLS instruction. With one probe scope MF1-L28-1 (step shift counter, Systems Diagram, 2.08.34) and with the other probe scope MF1-E12-7 (shift counter drive line, Systems Diagram, 8.04).

The tap is set to obtain the figure as shown below.



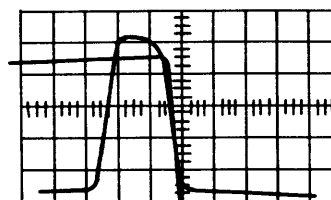
10 volts/cm
.4 usec/cm

Tally Counter Drive Line. This line is used to step the FP tally counter. As a starting point for setting this tap in the delay unit of Systems Diagram, 8.04, the input to tube A12-03A should be set 0 sections from the 1K load or in C-17 in PU9029 MF1-A12. It is imperative that the fall of the line coincide with the fall of a clock pulse shown below.

Insert the following program.

```
0 LDQ 0003
1 MPY 0003
2 TRA 0000
3 +00000000010
```

Sync scope of MF3-H19-5 (primary oper. of MPY on Systems Diagram, 3.10). With one probe scope MF1-N05-7 and with the other probe scope MF1-P12-1 which is an A2(D1) pulse (Systems Diagram, 2.09, sheet 2). Adjust the tap until the figure below is observed.



10 volts/cm
.4 usec/cm

SECTION	TITLE	PAGE
704. 30. 00	DIAGNOSTIC OR RELIABILITY TESTS	30-2
704. 31. 00	Machine Check Out Diagnostics	30-2
704. 31. 01	Main Frame Tests	30-2
704. 31. 02	Core Storage Tests	30-2
704. 31. 03	Drum Tests	30-2
704. 31. 04	Printer Tests	30-2
704. 31. 05	Card Reader Tests	30-2
704. 31. 06	Punch Tests	30-3
704. 31. 07	Tape Tests	30-3
704. 32. 00	Machine Reliability Acceptance	30-3
704. 33. 00	Load Programs	30-4
704. 33. 01	Non/Iterative Loading Using the Load Button and a Pre-Punched Copy Card	30-4
704. 33. 02	Iterative Loading Using an Index Loading Loop (Punched in 9 Row L, 9 Row R, 8 Row L)	30-4
704. 33. 03	Key In and Punch Load Routine - 4M09	30-4
704. 33. 04	Load Key Test - 4M13	30-4
704. 33. 05	One Card Absolute Binary Loader - 4M16	30-5
704. 33. 06	A Non/Iterative Binary Loader (Low End) - 4M24	30-5
704. 33. 07	Binary Loader (High End) - 4M27	30-5
704. 34. 00	Diagnostic Format	30-5
704. 34. 01	Diagnostic Engineering Print Subroutine - 4 DEPR	30-5
704. 34. 02	Sense Switch Control	30-6
704. 34. 03	Print Outs A. CPU B. I/O	30-6
704. 35. 00	CPU Reliability Tests	30-6
704. 35. 01	MF Reliability Program and Diagnostic - 4M31	30-6
704. 35. 02	Execution Controls Diagnostic - 4M32	30-6
704. 35. 03	Floating Point Diagnostic - 4M33	30-7
704. 35. 04	Floating Point and Floating Point Trap Diagnostic - 4FPT	30-7
704. 35. 05	CPU Reliability - 4M34	30-7
704. 36. 00	Other CPU Tests	30-7
704. 36. 01	Tests of Adders and Accumulators - 4M28	30-7
704. 36. 02	Fortran	30-8

704.30.00 DIAGNOSTIC OR RELIABILITY TESTS

704.31.00 MACHINE CHECK-OUT DIAGNOSTICS

704.31.01 Main Frame Tests

Program No.	Program Name	Time of Test	Freq.	Main Power Supply					
				+220	+150	-30	-100	-250	-130
4M34	Main Frame Reliability	2 passes	920KC	+198	+142	-27	-90	-230	
			1090KC	+242	+162	-33	-110	-263	
4M33 OR	Floating Point Diagnostic	2 min.	920KC	+198	+142	-27	-90	-230	
			1090KC	+242	+162	-33	-110	-263	
4FPT	F. P. & F. P. Trap Diag.	3 min.	920KC	+198	+142	-27	-90	-230	
			1090KC	+242	+162	-33	-110	-263	

704.31.02 Core Storage Test

4S05 AND	Complimenting Pairs	1 min.		+198	+142	-27	-90	-230	-117
4S06	Checkerboard	each		+242	+163	-33	-110	-263	-143

704.31.03 Drum Tests

4D10	Combined Drum Test	5 min.	910KC	+198	+143	-27	-96	-230	
			1090KC	+234	+163	-33	-108	-259	

704.31.04 Printer Tests

4P01	Read Printer Test			+198	+143	-28	-90	-225	
				+241	+122	-33	-110	-263	

704.31.05 Card Reader Tests

4C02	Card Reader Timing Test	1 min.	Timing Test Only						
------	-------------------------	--------	------------------	--	--	--	--	--	--

704.31.06 Punch Test

Program No.	Program Name	Time of Test	Freq.	Main Power Supply					
				+220	+150	-30	-100	-250	-130
4R01	Random No. Punch Test	1 pass		+198	+143	-27	-90	-230	
				+242	+163	-33	-108	-264	

704.31.07 Tape Tests

	Program Name	Time of Test	Main Power Supply					Tape Control		
			+220	+150	-30	-100	-250	+140	-60	-130
4T01	Random No. Tape Test	1 pass	+198	+142	-28	-90	-235	+133	-54	-117
			+242	+163	-33	-110	-262	+150	-78	-137
4T04	Test Tape Unit Addresses	1 min.	+198	+142	-27	-90	-230	+133	-54	-120
			+242	+162	-33	-110	-263	+150	-78	-137
4T07	Write on 3 tapes	1 min.						+133	-54	-120
								+150	-78	-137

704.32.00 MACHINE RELIABILITY ACCEPTANCE

Program No.	Program Name	Time of Test
4M34	Main Frame Reliability	8 Hours
4M33/4FPT	Floating Point Test	30 Minutes
4S05	Complimenting Pairs Checker-Board	30 Minutes
4S06	Complimenting Pairs Checker-Board	30 Minutes
4T01	Tape Diagnostic	1 Hour/Tape Unit
4D10	Combined Drum Test	8 Hours
4P01	Echo Check	1000 Lines
4R01	Punch Test	1000 Cards
4T09	Tape Read Interchangeability	Write a tape on each Tape Unit. Read each tape on every tape drive.

704.33.01 Non/Iterative Loading Using the Load Button and a Pre-punched Copy Card

1. The first automatic copy puts what is punched in the 9-row left of the card into storage location 0000.
2. The second automatic copy puts the 9-row right into location 0001.
3. The automatic TRA 0000 starts the load program at 0000. In storage at this time: 0000--CPY 0001; 0001--00--00.
4. The main frame completes the instruction at 0000, which means it copies into location 0001 in storage what is punched in 8-row left. In storage at this time: 0000--CPY 0001; 0001--CPY 0002.
5. The main frame steps to the next instruction (CPY 0002) and completes it. This time we copy into 0002 in storage what is punched in 8-row right. In storage at this time: 0000--CPY 0001; 0001--CPY 0002; 0002--TRA 0000.
6. After the main frame steps to the instruction at 0002 (TRA 0000), it transfers to 0000. At 0000 we have CPY 0001, which now means copy into storage location 0001 what is punched in the 7-row left of the card. In memory at this time: 0000--CPY 0001; 0001--CPY 0003; 0002--TRA 0000.
7. When the instruction at 0000 is completed we step to 0001 where we now have CPY 0003. This means copy into storage location 0003 what is punched in the 7-row right of the card. This will be the first instruction of the program being put on the pre-punched copy card.
8. This operation will continue until we come to the 12-row left, where either a TRA 0003 or a RDS card reader will be punched. In the case of a TRA 0003, the CPU will transfer and start the program. In the case of RDS 0321, the card reader will take another cycle and the first instruction punched in the 9-row left of the second card will be CPY 0014. The right side of the second copy card may have instructions punched from the 9-row right to the 11-row right. In both of the above cases it may be seen that there must not be anything punched in the 12-row right.
9. There may be any number of copy cards following each other if the RDS 0321 is punched in the 12-row left, if the pre-punched copy locations are sequential, and if the final card to be read has a TRA 0003 punched in the 12-row left.

704.33.02 Iterative Loading Using an Index Loading Loop (Punched in 9 Row L, 9 Row R, 8 Row L)

An example of an iterative loading loop is:

Location	Operation	Decrement	Tag	Address
0000	LXD		A	0001
0001	CPY	0044	A	0046
0002	TIK	0001	A	0001

The automatic copies put the LXD and the CPY instructions into storage at locations 0000 and 0001. The automatic TRA 0000 starts the load program operating. Upon execution of the copy at 0001 we copy into location 0002 what is punched in the 8-row left. This is accomplished by bringing the amount in the index register to the address in the 2's complement, and adding the address of the instruction being used (0046):

011	100	2's complement
100	110	address
000	010	effective address

When TIK is executed, the index register is reduced by the amount in the decrement of the TIK instruction and we transfer as long as the index register is larger than the decrement. We repeat the mixing of the index register as before, and thus the next effective address is 0003 (the first instruction of the program being loaded). The row copied would be what is punched in the 8-row right of the card. This procedure would be repeated until the

index register is reduced to 0001; the main frame would not transfer (TIK) but would step to the next sequential address, which is 0003, and the program that was loaded would then start operating.

704.33.03 Key-In and Punch Load Routine - 4M09

This load routine is used to aid in keying-in routines with either bootstrap, non-bootstrap, or R. H. check sum format, and to have cards punched accordingly. This program contains instructions and cards to place program on tape.

Bootstrap Operation With All Sense Switches Up

When program stop occurs at 0072, set the machine in manual and push enter MQ key. Return to automatic and press the start key. This enters the first piece of data in 8 right of the card image. The entry appears in the accumulator and the MQ is cleared after each entry is completed; thus, there is no question as to whether the entry was made or as to which entry was made last. Repetition of the above steps will enter data at each subsequent position of the card image. When the last desired position of the card image is ready for entry, depress sense switch 1 before pressing the start key. This will fill all unused positions with zeros, punch out the card, and reset conditions for a new bootstrap card.

Non-Bootstrap Operation With Sense Switch 3 Down

This is exactly the same as the bootstrap operation except that all 24 positions of the card image are available for entry.

Right-Hand Check Sum Format Operation With Sense Switch 6 Down

When the program stops for origin entry at 0035, enter origin in operator's panel keys to the MQ. Set in automatic and press the start key. This step enters the origin only; subsequent operation of the program enters the number of card image entries into the decrement of 9-row left and computes the check sum entry for 9-row right. The program now stops for regular program data entry at 00438. Data are entered in the same manner as in the case of a bootstrap card except that the first item is stored in 8-row left of the card image. If entries total less than a full card, operate sense switch 1 with the last entry and press the start key. The card will punch out with a proper 9-row left decrement entry and check sum, and the program will return to 0035 for a new origin entry.

To change card format, set the desired format in the sense switches and press the reset and start keys in automatic and the new format will be ready for entry at the appropriate program stop. To examine any position of the card image, store the card image at 1000 to 1027; it may be examined by keying in the desired display storage address in manual. Corrections may be keyed in by the enter MQ and enter-instruction keys without disturbing the rest of the card image or the key-in program as long as the machine remains in manual, and entries may then be continued from the last previous entry. Corrections may be made by resetting and restarting.

704.33.04 Load Key Test - 4M13

This is not a loader but a test of the load key routine.

RDS
CPY 0000
CPY 0001
TRA 0000

If the machine does not stop at addresses 0001 or 0002, display address 0000. If 0000 contains no transfer, the automatic copy is not working. If 0000 contains a transfer to 0001 or 0002 and the machine did not transfer, the machine is not resetting the instruction counter on load.

704.33.05 One Card Absolute Binary Loader - 4M16

Place this program card 00 in front of the binary deck to be loaded in the card reader hopper. Press the load key. Cards will be loaded until either a transfer card or an end-of-file is reached.

To obtain automatic transition, a transfer card (P 3/4) may follow the binary deck, with a minus transfer instruction punched in area A. The transfer may be placed in area B, in which case area A may be used for another instruction to be executed prior to transfer.

This program will only load cards which conform to the following layout. Referring to the load card layout, in the ABSOLUTE BINARY card 9 row:

- Columns 1-8: These columns are not seen by the calculator and may be punched in any way (all rows).
- 9: Absence of a punch in this column indicates that this is a binary card, rather than a transfer card.
- 22-26: Contain a number V, ($0 > V \geq 26_8$) which specifies the number of words in the card, beginning with 8-row left, which are to be stored and checked.
- 30-44: Contain the address R ($00000 \geq R \geq 77777_8$) at which the first word is stored (8-row left). The remaining words are stored in sequence.
- 45-80: Contain the check sum for the stored portion of the card, formed by adding the stored words of the card to the contents of 9-row left. In this addition, signs (columns 9 and 45) are treated as numerals and all carries from the most significant position are added in the least significant position.

In the TRANSFER card 9 row:

- Columns 1-8: Same as above.
- 9: A punch in this column identifies a transfer card.
- 9-80: Contain two words which are stored at locations 26_8 and 27_8 . After storing -A at 26_8 and B at 27_8 , calculator control is transferred to 26_8 .

704.33.06 A Non-Iterative Binary Loader (Low End) - 4M24

This loader is used when 4M16 or 4M27 will not load in a diagnostic deck. This loader provides the necessary program to load a diagnostic program without using index registers and without checking check sums.

This loader loads cards punched with check sums in 9-row right and first address and number of instructions to be read in 9-row left. The loader recognizes a transfer card that has a transfer preceded by a minus sign punch in 9-row left.

704.33.07 Binary Loader (High End) - 4M27

This loader provides a means of loading instructions from cards having the same format as those described in 4M16. These cards can be loaded into the low end of memory, even including positions 0-26.

There is one restriction in using this loader. The machine cannot be loaded when it is in trapping mode.

704.34.00 DIAGNOSTIC FORMAT

704.34.01 Diagnostic Engineering Print Subroutine - 4 DEPR

This diagnostic subroutine will interrogate sense switches and print a detailed account of error indications that may occur as a result of running diagnostic test routines. The information that is printed will include the test location; the primary instruction being tested in SHARE mnemonics operation codes; the address of where the error was detected in the program; the status of the sense lights and switches; the contents of the accumulator, quotient, and index registers; status of the overflow/underflow triggers, tape check indicator, and trap trigger indication which will specify that the test routine is using some form of trapping mode. The contents of location zero are printed in octal code. When an input-output type print-out is desired, the word written or generated and the word read are printed in octal along with the word number and record number. This print subroutine may be used only with test routines that have been written that include the basic linkage to the subroutine. Index register C is used in the subroutine.

Some of the internal workings of the print routine are:

1. Insert a BCD word of a SHARE mnemonics operation code at the beginning of each section of a test to indicate the primary instruction to be tested; i. e., BCD ICLA test instruction -- Clear and Add.
2. The basic linkage to the subroutine in symbolic notation should be as follows:
 - a. Main Frame Test I/O Test
TSX Error, 4 TSX Error, -4, 4
TSX OK, 4 TSX OK, 4
TRA X TRA X
The return address for continuation of the program will be two locations beyond the TRA X instructions. For repetition of the same test, the return address will be to address X, where the address X in TRA X specifies the start of the test location. When the program enters the TSX error, 4 instruction, it will cause a CPU type of print-out, if printing is desired. Entry to the TSX error -4, 4 instruction will produce an I/O type of print-out. Entry to the TSX OK, 4 instruction will cause interrogation of the sense switches for repetition of the test or continuation of the program.
 - b. Main Frame Test I/O Test
TSX Error, -1, 4 TSX Error, -2, 4
TRA X TRA X
When entry is made to the above TSX instructions, the program returns from the subroutine to the next location immediately following the TRA X instructions. Address X specifies the start of the test location.
3. When writing an I/O test, index register A should be used for the word count of each record and index register B should be used for the record count where possible. The total word count 1 and record count 1 should be stored in symbolic locations WDNO and RECNO, respectively, prior to entry to the basic linkage of the subroutine.
4. Whenever a routine uses the trapping mode, the BCD SHARE operation should be followed by a hyphen; i. e., BCD IETM - Test INST Enter Trapping Mode.

704.34.02 Sense Switch Control

SSW 1 UP -- Test Sense SW 4
SSW 1 DN -- Repeat Test Loop
SSW 2 UP -- Indicate errors - Test SSW 3 to print or halt
SSW 2 DN -- Bypass error indications - Test SSW 1
SSW 3 UP -- Print on error if SSW 2 is up, then test SSW 1
SSW 3 DN -- Stop on error if SSW 2 is up, then test SSW 1
SSW 4 UP -- Proceed to next test
SSW 4 DN -- Repeat section N times or, if error occurred, go to next section
SSW 5 -- Free to use in each particular diagnostic
SSW 6 UP -- End Test - call in next test
SSW 6 DN -- Repeat entire program

704.34.03 Print-Outs

CPU Print-Out

Following is the type of CPU print-out:

Test Loc 00031, Opn Stp, Error Loc 00052, 0 Loc 402000000031, Sw 000000, Lite 0000, MQ 000001010100, XRA 00001, XRB 00001, XRC 07726, Trap Tgr 0 Acc & Q 0, P 0, 300001010101, Tape Ck 0, Div Ck 0, Ovfl MQ 0, Acc 0.

Test Loc 00031. Indicates the start of the section of the program in error. Program begins at location 00031.

Opn STP. Indicates the primary SHARE operation being tested. Test instruction is store prefix.

Error Loc 00052. Indicates the location where the error was detected. Error in program occurred at location 00052.

PSE Sw 000000. Indicates the status of the six sense switches. A 0 implies that the switch is up and a 1 implies that the switch is down. Sense switches and sense lights are read sequentially from left to right.

Light 0000. A binary 1 implies that a light is on, and a binary 0 implies that a light is off.

The contents of the accumulator, MQ, and indices are in octal.

I/O Print-Outs

Following is the type of I/O print-out:

Test Loc 00202, Opn RTB 1, Error Loc 00230, 0 Loc 000000100001, Sw 000000, MSE 0000, Comp Error, Word Generated 010 000 101 100 001 001 100 111 011 011 Rec 00001, Word 00002, Word Read 100 000 101 100 001 001 100 111 011 011.

Opn RTB 1. Indicates that the error occurred as a result of reading tape 1 in binary.

Word Generated. Refers to the word written or generated in storage that is being compared to the word read from tape unit 1.

Word Read. Indicates the word of the record that was read into storage in error from tape 1.

MSE 0000. Indicates the status of the four sense lights.

704.35.00 CPU RELIABILITY TESTS

704.35.01 MF Reliability Program and Diagnostic - 4M31

This program gives a comprehensive test of all the CPU instructions, except floating point. The program is divided in two parts. The first part is a test of all CPU instructions except floating point and indexing instructions. The second part is a test of all indexing instructions. The first part of the test is under control of a general print routine, which is located after the constants. If one reads the first page of the control program, which immediately follows the constants, a general understanding of its operation will be derived. The general print routine has essentially two conditions:

1. On OK Program examines Sw 1 to loop and then Sw 4 for reliability run.
2. On Error Program examines Sw 2 to either bypass or stop on error, Sw 1 to loop, and then Sw 3 to either print or stop on error.

The TSX instruction is the connecting instruction for the control program; for this reason it is given a cursory test at the beginning of the test. The plan used in this test is to start with basic instructions and build upon them; that is, an instruction is not used until it has been tested. Therefore, on an error we can say that all previous instructions before the error work correctly and our error lies somewhere in the section where the program failed.

The index test does not make use of the control program, but is written in the format of PSE stops. The storage deflection test is placed at the beginning of the CPU program. The loader here is used in checking the HTR instruction by giving an incorrect check sum in one of the cards. A card of 4M31 is given an incorrect check sum to check the HPR instruction. The 4M27A loader has been changed to check HPR. Both check sum stops were placed near the front of the decks so that the operator will not have to wait long for the stop to occur.

Both loaders have been released with this deck. When the storage deflection test does not load, remove the cards for the storage deflection test and insert the 4M24A loader in place of the 4M16 loader on 4M31 and try loading. If the cards do not load, try loading 4M32. The last card of 4M32 has the row of nines punched for your use. In the event it is impossible to load cards, this becomes a useful means of determining whether or not the load key routine brought any information into the MQ by trying to load this card. To bypass the index register test, enter transfer to 30 at 4300.

One of the most important functions of the error indication is the error address. This address will permit the customer engineer to refer to the routine in the program which failed. By analyzing the routine with the aid of the comments on the listing, it is hoped that he will be able to determine the manner in which the machine failed and hence have sufficient information to diagnose the cause of the malfunction.

It is important that this test be followed by 4M33. These programs are logically one diagnostic. The only limitation on the length of the test is the size of storage. Any additional routines that may be incorporated into 4M31 in the future will be a separate memory load.

704.35.02 Execution Controls Diagnostic - 4M32

This program is written in PSE stop format to aid the customer engineer in forcing the repeated execution of some failing instruction with a minimum of programming complexity. The test covers all CPU instructions except floating point and indexing. The program is essentially the first part of 4M31. The program deck is made up of copy cards so that it may load when other programs do not load.

The format of the test is essentially the same as that of 4M31 except that the format is PSE stops instead of TSX and general print routine. This program is to be used when 4M01 will not load with either of its loaders, or when a tighter loop is desired for scoping a CPU instruction other than floating point or indexing. There is a restart in the program which is reset after trapping routines. Restart is to the beginning of the program. The last card of the deck has all of the nine row punched for the customer engineer to use.

704.35.03 Floating Point Diagnostic - 4M33

This is a comprehensive test of the floating point instructions. It also is written in the print routine format. The program is divided in two parts. The first part is a test of floating point instructions having no underflow or overflow conditions. The second part is a test of floating point instructions having either underflow or overflow conditions. The general print routine gives control over the program. A minimum of instructions was used in the control program to provide a close loop for scoping purposes.

704.35.04 Floating Point and Floating Point Trap Diagnostic - 4FPT

This is an addition put on 4M33 to test the floating point trap feature. When the program starts, an alternator is set off to be in one of the three phases of this diagnostic.

Phase 1 is the basic execution test of 4M33 without overflow or underflow and not in floating point trap. Then set alternator on, and enter phase 2. Phase 2 repeats the 4M33 basic execution test without overflow or underflow in floating point trap mode. The alternator is tested and found on. It is set off and CPU goes to phase 3. Phase 3 is the floating point trap diagnostic with both overflow and underflow trap conditions.

When the program begins, all unused portions of core storage are filled with a TSX instruction, so that if the program skips wildly into space, the special space routine may recover control.

704.35.05 CPU Reliability - 4M34

This test was written specifically to include floating point in the reliability test. The program is a combined deck or 4M31, less the 4S03 program, and an added floating point random number test. At completion of one pass of 4M31, with sense switch 6 up, the cards for floating point random number test are called in. If more than one pass of the combined program is desired, depress switch 6 at this time. The floating point random number program is read into storage in the area used to adjust storage constants for 4M31. After one pass this information is no longer needed so we may write over that area. The starting address in core storage for the constants used by floating point random number test is at 7550.

The same sense switch control is used as in the standard print routine. However, to allow the floating point random number test to be included, which is a must, leave switch 6 up to allow one pass to be made and then call in the rest of the cards, at which time it is suggested that switch 6 be depressed. The standard print-outs are the same as for 4M31. To run this program correctly, load with switch 6 up. After one pass the full program is read in from the card reader; at this time depress switch 6.

This addition of the floating point random number test loads over the storage adjusting routine of 4M31 in core storage area 4310 to 4410 and constants are placed in addresses 7550-7751, then the transfer is to the beginning at 0030. There is no storage deflection test at the beginning of this deck, and there is not a check sum stop in the program as in 4M31.

704.36.00 OTHER CPU TESTS

704.36.01 Test of Adders and Accumulator - 4M28

This test checks the adders and accumulator by placing different combinations in the accumulator and tests each column for a possible error. This test will show which column is in error. This test includes instructions and cards to place a program on tape. There are five phases of the test. Each is performed by an ARS, and LBT to test each column in the accumulator. The first phase of the test clears the accumulator and tests for 0's. 1's are placed in the accumulator; CAL 0's and test for 0's. In the second phase 1's are put in the accumulator and it is tested for 1's. Then CAL 1's over 0's; and test Acc for 1's. In the third phase clear the accumulator and complement; test for 1's; CAL 1's over 0's; complement Acc; recomplement Acc and test for 1's. In the fourth phase clear the accumulator; CAL 1's and add 1; test for 0's; test Q for a 1 and test of overflow. In the last phase put 1's in accumulator; ACL 1's and test for 1's. Then the test puts 1's in accumulator; ACL 0 and tests for 1's.

The first card is non-iterative and self loading; this tests the instructions used in the program, and also with sense switch 5 up it tests the HTR instruction. If sense switch 5 is down, the program continues. The test tries to use a minimum number of instructions in performing the program. These instructions are ARS, LBT, TRA, HPR, LDQ, LGL, PSE, and MSE. The instructions tested are CLA, ACL, ADD, and COM.

There are no print-outs in this test and the sense switch controls are modified for this.

Switch 1 Up	Proceed to test next column.
Switch 1 Down	Go to error routine.
Switch 2 Up	Stop on error.
Switch 2 Down	Bypass error stop.
Switch 3	No effect.
Switch 4	No effect.
Switch 5 Up	Stop in first card read to test HTR.
Switch 5 Down	Allows program to be read in.
Switch 6 Up	Bring in the next program after the completion of one pass.
Switch 6 Down	Repeat test indefinitely.

If the error routine is selected, reference is again made to switch 2 as follows:

Switch 2 Up	Repeat entire subtest up to the column which failed.
Switch 2 Down	Go to a tight loop of the failing instructions for scoping purposes.

Sense lights are used to indicate the phase of the test being tested.

- 1 on phase 1A of program being run.
- 2 on phase 2A of program being run.
- 3 on phase 3A of program being run.
- 2 and 3 on phase 4 of program being run.
- 4 on phase 5A of program being run.

This is a short description of the operation of FORTRAN.

Fortran Tape has Three Files

The first record on the first file is a special tape-loading program. This is stored in core storage positions 0-27. To start FORTRAN, either load the call card, or rewind tape 1 and press the load tape key. If the input is on-line, it follows the call card or is ready in the reader if "load tape" is used. The second record on the first file of the FORTRAN tape is a version of CTH. If the card reader is empty, this is skipped. Now the FORTRAN tape is skipped to the beginning of the second file. Each record on the tape is a program, or part of a program, which will be executed sequentially. Sometimes these records are copied to the drum and used over again.

The first section of FORTRAN reads tape 2, using programs copied from tape and drum (4 drums 1, 2, 3, 4). During this section tape 3 is written. Also, tables of information are written on drums and tape 4. At the end of this section, tables from the drums and tape 4 are written as additional files on tape 2. The second section processes table information from the drums and tape 2 (additional files) and writes a new tape 4; it also writes the tables on drums. The third section merges the tapes

3 and 4 using another file on tape 2 intermediately, and finally prepares a tape 3. The fourth section examines this tape 3 and writes tables on drums and in core storage. The fifth section writes a tape 4, and tables on drums, then uses the tables from section 4 and tape 4 to write a new tape 3. The last section takes the tables from the additional files on tape 2 and writes them on the drums, then, using these tables, writes the first part of the output storage map as a new second file on tape 2.

Then the first pass of a special assembly program is made over tape 3; following this a library search is made. The library is the third file on the FORTRAN tape. When this is finished, the FORTRAN tape rewinds, spaces over the first two records on the first file, and makes the second pass of the assembly. The binary output from this assembly is written on tape 4. More of the storage map is written on tape 2. If sense switch 1 is up, tape 4 is punched on-line; if not, no punching takes place. If sense switch 2 is down, a third file is written on tape 2. (This is obtained by translating tape 3.) This is the symbolic version of the "Object" program. If sense switch 3 is down, tape 2 is rewound and printed on-line. Finally all tapes (1, 2, 3, 4) are rewound and the load key sequence is executed. If the programmer has made errors which the FORTRAN diagnostic can catch, these errors are printed on-line and at the end of section 1. The words "End of Diagnostic" are printed, tapes are rewound, and the 704 stops at 17777.

SECTION	TITLE	PAGE
704.40.00	SERVICE TECHNIQUES ON THE 704 CPU	40-2
704.41.00	Trouble Shooting Chart	40-2
704.41.01	CPU	40-3
	Figure 41-0 CPU Trouble Shooting Chart	40-3
	Figure 41-1 Clock & Basic Pulse Troubles	40-4
	Figure 41-2 Storing Troubles	40-5
	Figure 41-3 Load Button Troubles	40-6
704.41.02	Load Operation Trouble Approach	40-7
704.42.00	Trouble Chart - Oscilloscope	40-8

704.40.00 SERVICE TECHNIQUES ON THE 704 CPU

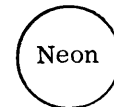
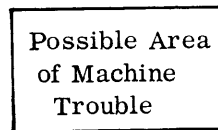
704.41.00 TROUBLE SHOOTING CHART

This chart was developed to provide procedures that can be followed when a 704 suffers complete breakdown (defined as inability to load programs by non-iterative techniques). If a diagnostic program can be entered into the 704, it is felt that the program is the best trouble shooting guide available. Therefore, this procedure only covers the techniques used when not able to load any diagnostic.

Three types of failure can produce inability to load programs. These are: (1) failure to execute instructions due to basic main frame troubles; (2) failure to transfer correct information caused by input-output circuit failures; (3) failure to retain correct information due to storage troubles. The customer engineer should be alert to the possibility of troubles caused either by insufficient action or by extra action. Time can usually be saved by observation of the general status and operation of the machine before trying detailed trouble shooting techniques.

These techniques were developed with the idea of trying to show up the intermittent troubles. Special little loops and tests were included for this purpose. They have also been designed to correspond to the diagnostic program for the machine, so the technique and diagnostic can be used together in most cases. These techniques are performed with the machine diagnostic as the program that is loaded and run.

These are not in final form so revisions will be made when necessary. Symbols used have the following meanings.



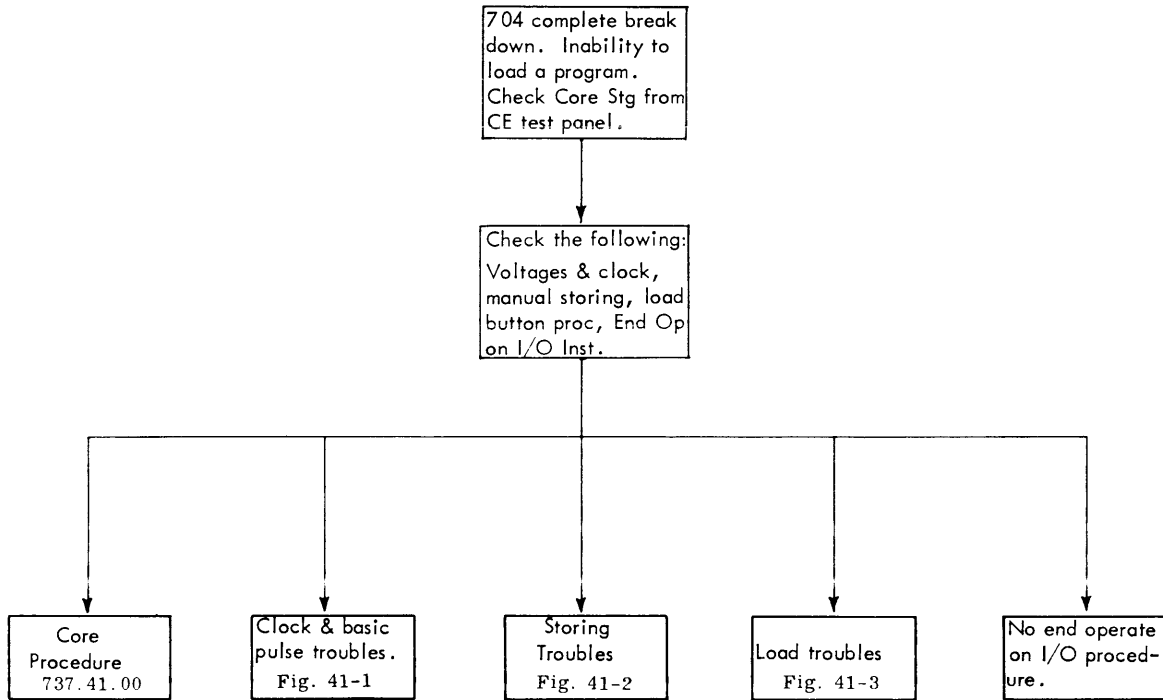
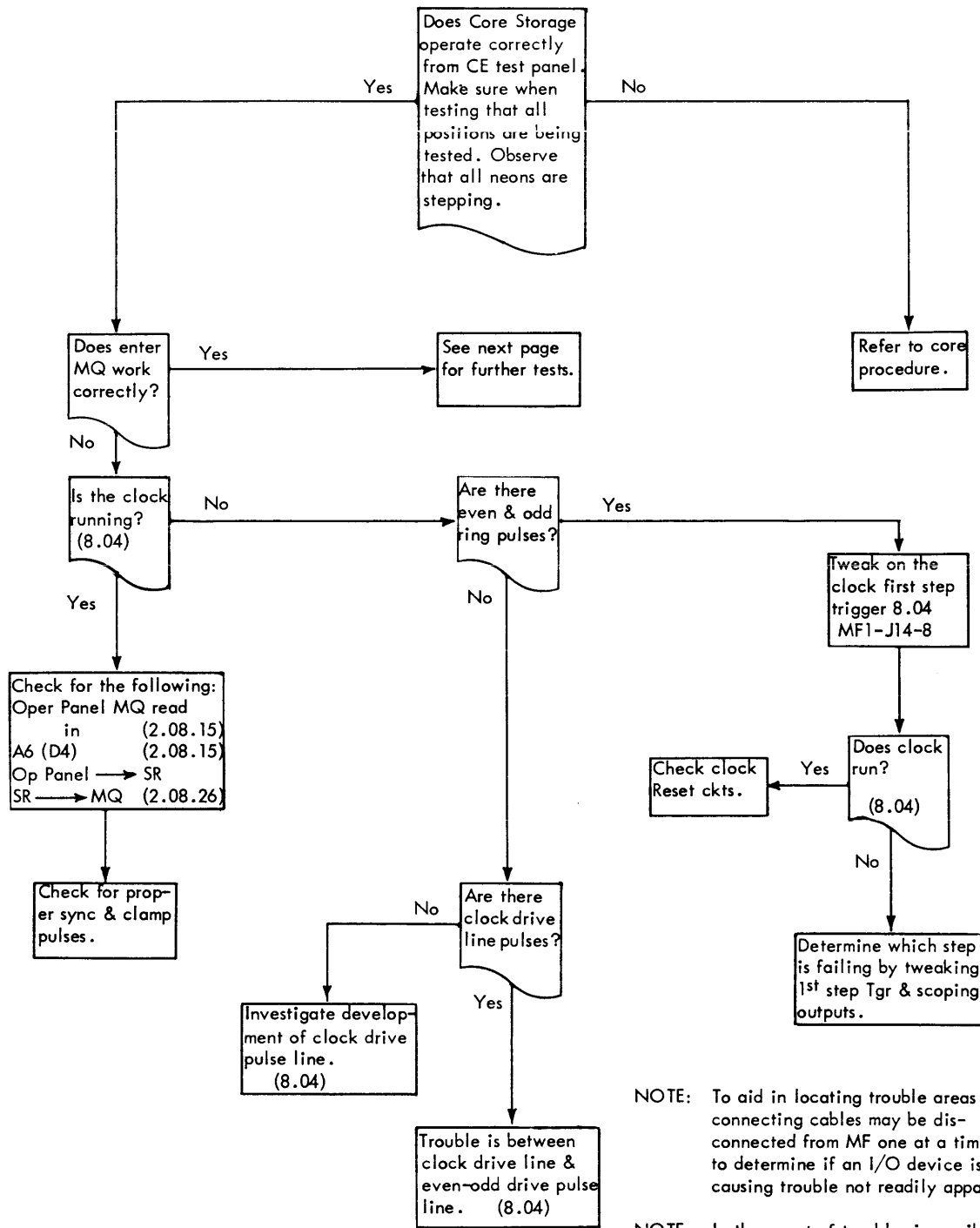


FIGURE 41-0. CPU TROUBLE SHOOTING CHART



NOTE: To aid in locating trouble areas connecting cables may be disconnected from MF one at a time to determine if an I/O device is causing trouble not readily apparent.

NOTE: In the event of troubles impossible to analyze check for proper voltages and blown fuses that failed to indicate.

FIGURE 41-1. CLOCK AND BASIC PULSE TROUBLES

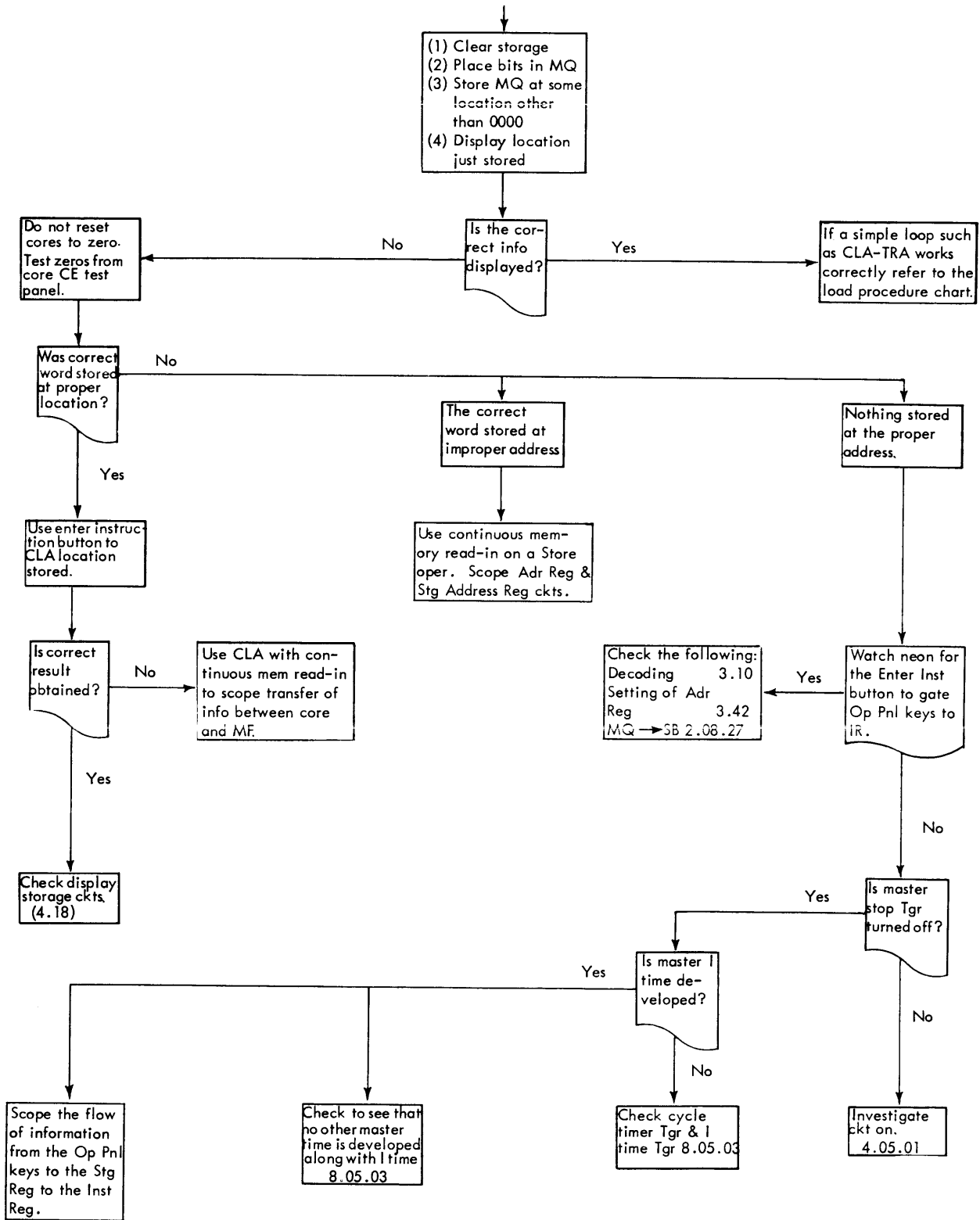


FIGURE 41-2. STORING TROUBLES

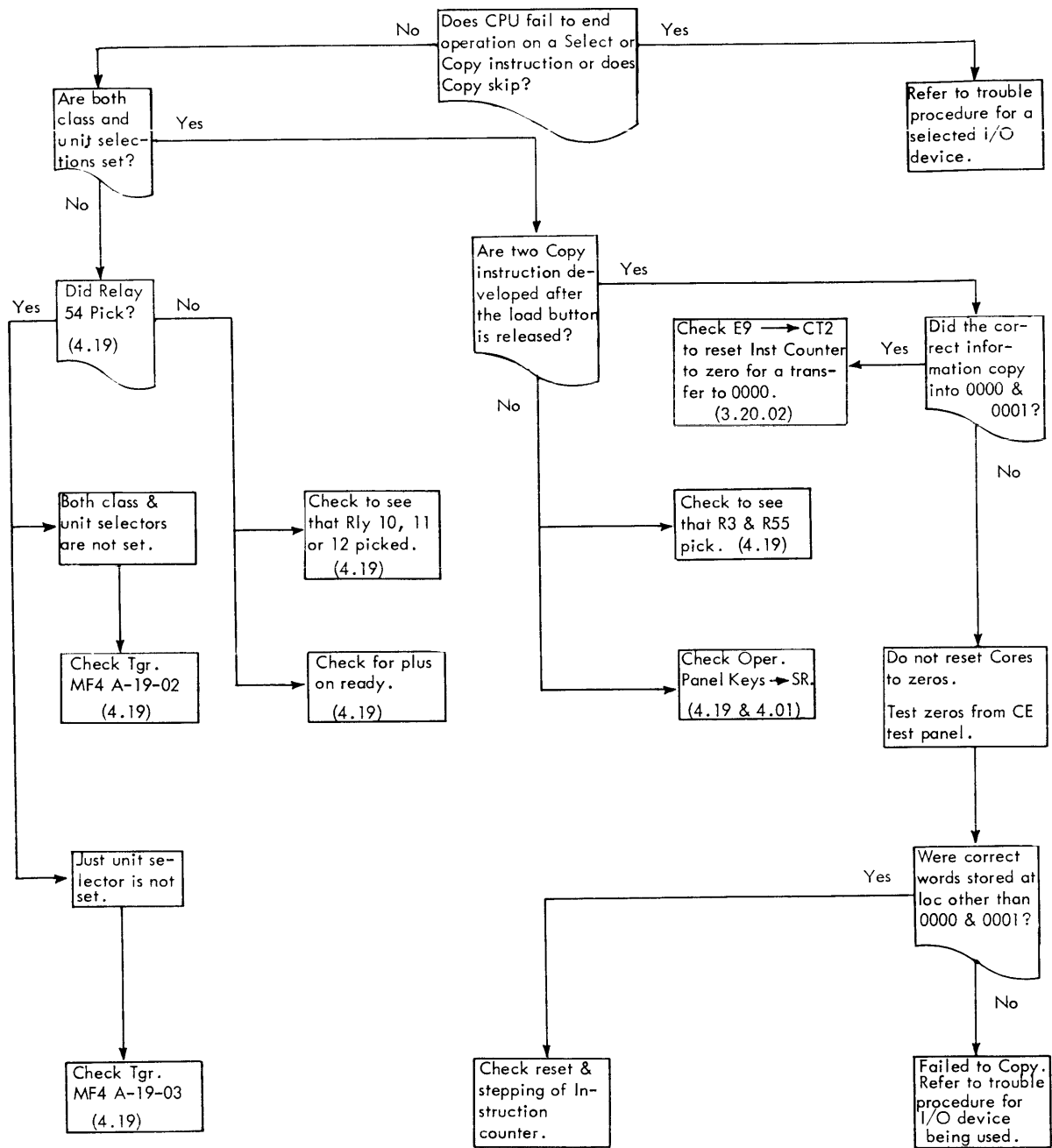


FIGURE 41-3. LOAD BUTTON TROUBLES

704.41.02 Load Operation Trouble Approach

Try loading from cards, tape and drum. This is used to indicate troubles in the I/O units. It is possible to check the unit selection in this manner.

Observe panel, cycle timer and storage address register neons on reset and clear operations. The neons may indicate the trouble area.

Load into 00000 and 00001 and then display these positions. This will check if we are loading correct information at the right address from the operator's panel.

Isolate the main frame by pulling out the cable shoes. This can point out some troubles caused by I/O circuit failures.


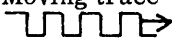
Check operation of the instruction counter. This is done from the test panel on the core storage frame. The "test on" switch causes the instruction counter to be stepped, by A3 pulses as long as there is no check stop.








Try keyboard operations to try and separate or locate troubles. Some of these are:

1. Complementing after reset to give all ones, and then re-complementing.
2. STO and STQ operations to check information flow to storage.
3. Use simple instructions such as TZE and TNZ and check data flow.
4. Set up a transfer loop from the low to high end of storage and then transfer back.
5. Enter short test routines from the keyboard.

Make sure the storage register, adders and accumulator are not giving the trouble. These are used in almost all operations.

704.42.00 TROUBLE CHART-Oscilloscope

Trouble	Location	Tube Designation	Tube Type	Parts	Components
Flickering Trace	Rear of scope			Clean contacts on relay	
Flickering and shift in trace	Ext. Sweep Amp. Vert. Amp.	V115 V606 V570 V580	2-6BQ7 2-12BY7		
No trace No Hi voltage	Vert. Amp. Sweep Gen.	V606 V55	6BQ7 6BQ7		
High Voltage - no trace	Sweep Amp. Vert. Amp.	V240, V246 V606	2-6BQ7 6BQ7		
Vertical sweep only	Sweep Gen.	V40	6BQ7		
Squarewave Def 	Calibrator	V670	6U8		6672 & C673 330 mmf
Sweep to left or right Sweep not stable	Sweep Amp.	V272 V265 V282	6BQ7		
Sweep in up position			12BY7		400K 1% rest. R259 or R260
Sweep not stable	+225 Power Sup.	V748 V784	6080		
No sweep on 100 microsec.	Sweep Gen.	V40	6BQ7		
Trace off screen	Vert. Amp.	V558 V535	6BQ7		
Moving trace 	Sweep Trigg.	V8	6BQ7		
Trace on top - no vert. adj.	Vert. Amp.				R570 or 580 3K res.
Sweep squeezing in up & down position	Output Amp.	V570 V580	12BY7		
Trace up - no adj.	Vert. Amp.	V508 or 509	6BQ7		
Trace down - no adj.	Vert. Amp.	V508 or 509	6BQ7		
Trace to the left	Sweep Amp.	V240	6BQ7		
Trace to the right 1 and 2 neon on	Sweep Gen.	V90	6CL6		

Trouble	Location	Tube Designation	Tube Type	Parts	Components
Poor triggering		V20 V8	6U8 6BQ7		
No sweep pulling V80 NE 96 will not go on	Sweep Gen.	V80	LAL5		
Voltage pin 6-V-90 +10 volts more or less*	Sweep Gen.	V90	6CL6		*C-96 82 mmf
Shortsweep left side only 	Sweep Amp.				R286 -30K Special rest.
Shortsweep right side only 	Sweep Amp.				R278 -25K Special rest.
Def. sweep 	Output Amp.	V606 (short)	6BQ7		
Def. sweep 	Driver	V508-V509 Noisy		*Cathode ray tube	
Loss in sweep length & amp.	CRT Circuit	V810			
Scope cuts out poor ventilation - clean screen	L. V. power sup.			Thermal cut- out 128° F	TK701
Sweep Top 	CRT Circuit			Geom. adj.	
Sweep Bottom 	CRT Circuit				
No squarewave 	Calibrator	V670	608		
Short sweep left - no hor. adj.	Calibrator	V246	6BQ7		
Sweep no adj. to the right	L. V. power sup.	V742	6AU6		
Sweep no adj. to the left	L. V. power sup.	V782	6AU6		
No sweep *	L. V. power sup.	V748 short one side			*R756, R780 3-10WR
D. C. shift	Driver	V508 V509 (match)			
Sweep free running no adj.	Internal Tgr. Amp.	V527	6U8		
500 volts to high no adj.	L. V. power sup.				R978 720K 1% R

Trouble	Location	Tube Designation	Tube Type	Parts	Components
500 volts to low no adj.	L. V. power sup.				R787 R788 1.84M, 780K 1% R
Amplitude Cal.	Output C. F. 's	V3503	12 at 7 balance		
Vertical adj. B ^A	Input C. F. 's	V4053 V3053	2-6AK5		
Section A	Input Amp.	V3083	2-12 AU6 Bal.		
Section B	Input Amp.	V4083	2-12 AU6 Bal.		
<p>500V, 350-V are dangerous. 10,000-V accelerating potentials. Check power supply voltages, 500-V, 350-V, 225-V, 100-V, -150 volts adjust controls all four positive voltages. Voltage check on ceramic-terminal right rear deck.</p>					
<u>TRIGGERING</u>					
#1.	Triggering - mode Trigger - slope Triggering - level Stability Square wave calibrator Amplitude Triggering level center adj. Trigger sensitivity		A. C. Slow + Int. O Adj. until display of square wave Time/cm - 100 mic. sec. 1 cm Adj. until sweep will trigger Adj. for stable sweep. Sweep should trigger equally well on + and - and + ext .		
#2.	Triggering - mode Trigger - slope Int. D.C. level Sweep will not trigger on + and - and + ext . Sweep will not trigger on + ext . Check or replace		D. C. + int. Adj. until stable square wave appears Repeat step #1 Repeat step #2 Tubes V8, V20, V527		

Trouble	Tube Designation	Tube Type	Components
<p>X1 Normal X2 Short X5 Very Short Chopped Sweep 53c Unit Chopped Sweep is over compensated No adjustment can be obtained using trimmers C3613 and C3653. Adjust trimmers C3583 and C4583. Trimmers interact Also check tubes No Horizontal Positioning Control acts like a magnifier, one side of tube weak Time CM Switch Sweep squeezing on left side when scope time/CM switch is set on 10 microsec. HV Supply High voltage drops as scope heats up Tubes go out Leaky capacitor</p> <p>Calibrator switch Calibrator settings 10V preamplifier 5 volts 10V preamplifier 10 volts If out of calibration resistors have changes their value</p>	<p>V-265 - V272 Not Matched</p> <p>2-V3553, 2-V4563 V272</p> <p>V824, V823 V822, V821</p>	<p>2-6BQ7</p> <p>4-12AUG 1-6BQ7</p>	<p>readjust variable C-240 3-12 mmf trimmer</p> <p>C830 - 0068mf 3000 volts</p> <p>R686-1 025K 1% R685-2 1K 1% R684-6 375K 1%</p>

SECTION	TITLE	PAGE
704.50.00	704 CPU SERVICE AIDS	50-2
704.51.00	Service Aids	50-2
704.52.00	Test Point Chart	50-3
704.53.00	Central Processing Unit Location Chart	50-4
	A. Figure 53-1 CPU Panel 1 Location Chart	
	B. Figure 53-2 CPU Panel 2 Location Chart	
	C. Figure 53-3 CPU Panel 3 Location Chart	
	D. Figure 53-4 CPU Panel 4 Location Chart	
704.54.00	I/O Shoe Connector Chart	50-8
	A. Figure 54-1 I/O Shoe Connector Chart	
704.55.00	704 CPU Neon Locations	50-2
	A. Figure 55-1	
704.56.00	Oscilloscope	50-3
704.56.01	Scope Calibration	
704.56.02	Z Input - Oscilloscope	
704.57.00	704 Troubles and Fixes	50-5
704.57.01	Timing, Sliver or Noise Troubles	
704.57.02	Reliability	
704.57.03	Bias Troubles	

704.50.00 704 CPU SERVICE AIDS

704.51.00 SERVICE AIDS

In this section a collection of reference material is listed. Anything that might aid the customer engineer to fix or avert troubles was included. A method to calibrate the scope is also included.

Also included, without relation to any order, is a list of 704 troubles with a specific fix. These are not guides but an aid for a specific problem.

704.52.00 TEST POINT CHART

1	Master Times - 8.05.04		5	Instruction Register - 3.02-04	
	I Time	MF1 - A18 - 4		Sign Plus	MF3 - D16 - 2
	E Time	MF1 - E18 - 2		Sign Minus	MF3 - D16 - 6
	ER Time	MF1 - B18 - 6		Not 1	MF3 - G16 - 6
2	Master Clock Pulses - 8.04.01-03			1	MF3 - G16 - 1
	A0	MF1 - P13 - 1		Not 2	MF3 - D17 - 6
		MF2 - P02 - 7		2	MF3 - D17 - 2
		MF3 - M33 - 3		Not 3	MF3 - G17 - 6
		MF4 - A18 - 4		3	MF3 - G17 - 1
	A1	MF1 - M13 - 1		Not 4	MF3 - D18 - 6
		MF2 - B03 - 2		4	MF3 - D18 - 2
		MF3 - K18 - 1		Not 5	MF3 - G18 - 6
	A2	MF1 - P12 - 1		5	MF3 - G18 - 2
		MF2 - Q01 - 8		Not 6	MF3 - E23 - 6
		MF3 - B02 - 2		6	MF3 - E23 - 3
	A3	MF1 - M12 - 1		Not 7	MF3 - F23 - 7
		MF3 - C32 - 3		7	MF3 - F23 - 3
	A4	MF1 - P11 - 1		Not 8	MF3 - E24 - 6
		MF3 - B04 - 2		8	MF3 - E24 - 3
		MF4 - D25 - 3		Not 9	MF3 - C24 - 4
	A5	MF1 - M11 - 1		9	MF3 - F24 - 3
		MF4 - G27 - 8	6	Shift Counter - 3.06	
	A6	MF1 - M19 - 1		10	MF3 - D25 - 3
		MF3 - B32 - 5		11	MF3 - F25 - 7
	A7	MF1 - P19 - 1		12	MF3 - H25 - 6
		MF2 - Q01 - 4		13	MF3 - E26 - 4
		MF3 - B02 - 6		14	MF3 - F26 - 3
		MF4 - E18 - 3		15	MF3 - E27 - 2
	A8	MF1 - M18 - 1		16	MF3 - F27 - 2
		MF3 - K18 - 2		17	MF3 - G28 - 1
	A9	MF1 - P18 - 1	7	Address Lines - 3.42	
		MF4 - B17 - 6		5	MF3 - Q29 - 8
	A10	MF1 - K17 - 3		6	MF3 - M25 - 3
		MF3 - L19 - 7		7	MF3 - P25 - 3
		MF4 - E17 - 3		8	MF3 - R25 - 3
	A11	MF1 - P16 - 2		9	MF3 - M26 - 3
		MF4 - G17 - 4		10	MF3 - P26 - 3
3	Primary Operation - 3.10			11	MF3 - R26 - 1
	00	MF3 - A19 - 8		12	MF3 - M27 - 3
	02	MF3 - B19 - 5		13	MF3 - P27 - 3
	04	MF3 - E19 - 7		14	MF3 - R27 - 1
	06	MF3 - B19 - 6		15	MF3 - M28 - 3
	10	MF3 - C19 - 7		16	MF3 - P28 - 3
	12	MF3 - D19 - 5		17	MF3 - R28 - 1
	14	MF3 - F19 - 6	8	Instruction Counter - 3.21	
	16	MF3 - H19 - 5		5	MF3 - P27 - 6
	20	MF3 - H19 - 5		6	MF3 - R24 - 5
	22	MF3 - D19 - 7		7	MF3 - N24 - 4
	24	MF3 - G19 - 7		8	MF3 - N24 - 1
	26	MF3 - A20 - 8		9	MF3 - K24 - 7
	30	MF3 - B20 - 5		10	MF3 - K24 - 3
	32	MF3 - E19 - 8		11	MF3 - R23 - 5
	34	MF3 - B20 - 6		12	MF3 - N23 - 4
	36	MF3 - D20 - 7		13	MF3 - N23 - 1
	40	MF3 - E20 - 7		14	MF3 - K23 - 7
	42	MF3 - G20 - 7		15	MF3 - K23 - 3
	44	MF3 - D20 - 5		16	MF3 - Q22 - 1
	46	MF3 - F20 - 6		17	MF3 - P22 - 3
	50	MF3 - F20 - 5	9	Pulse Generator - 1.05.02-03	
	52	MF3 - C20 - 7		Turn off read and read bias gate.	MF3 - H32 - 1
	54	MF3 - D20 - 5		Turn on read gate.	MF3 - E32 - 2
	56	MF3 - A21 - 8		Turn on inhibit and write gate.	MF3 - H31 - 1
	60	MF3 - B21 - 5		Read in sample.	MF3 - E31 - 2
	62	MF3 - B21 - 6		Read out sample.	MF3 - J32 - 4
	64	MF3 - C21 - 7		Turn off inhibit gate.	MF3 - R33 - 6
	66	MF3 - F21 - 6		Turn off write gate.	MF3 - J33 - 4
	70	MF3 - E20 - 8		Reset SAR and buffer reg.	MF3 - A33 - 4
	72	MF3 - F21 - 5		SAR read in and turn on read bias gate.	MF3 - H33 - 6
	74	MF3 - H21 - 5	10	Special Timed Pulses - 2.09	
	76	MF3 - G21 - 7		Step/Shift, shift Ctrl Ctr.	MF1 - E19 - 6
4	Secondary Operation - 3.11			I _g to CT ₁	MF1 - A13 - 7
	00	MF3 - D22 - 5		E _g to CT ₂	MF1 - B09 - 1
	01	MF3 - D22 - 7		Minus on I _g to CT ₁	MF1 - F10 - 6
	02	MF3 - A22 - 8		XR to adders	MF4 - G33 - 4
	03	MF3 - E22 - 7		Stg Reg (24-35) to adder (6-17).	MF4 - D01 - 5
	04	MF3 - B22 - 5		Adders to Acc Ctrl	MF1 - F32 - 7
	05	MF3 - F22 - 6		Comp Acc to adders	MF1 - G29 - 7
	06	MF3 - B22 - 6		True Acc (9-35) to adder.	MF3 - C35 - 4
	07	MF3 - E22 - 8		SR (9-35) to adder.	MF1 - H35 - 6
	10	MF3 - C22 - 7	11	Sync and Clamp - 8.06.02-03	
	11	MF3 - F22 - 5		Oscillator	MF2 - K39 - 1
	12	MF3 - G22 - 7		Sync Gen and clamp	MF2 - L40 - 2
	13	MF3 - H22 - 5		Invert Sync	MF2 - R40 - 6
				Invert clamp	MF2 - R39 - 1
				Clock drive.	MF2 - R39 - 6

FIGURE 52-1. 704 CPU TEST POINTS

CENTRAL PROCESSING UNIT LOCATION CHART

35	9043	SR to Adders	2.08.05	9050	MQ Reg Hold Ckts	2.04.07
34	9042	Carry to Adder (35) 2.08.08	CLA & AND Ctrl 2.08.29	9051	Stg Bus (18-35) to SR (18-35) 2.08.01	SR Hold Ckts 2.01.05 & 04
33	9041	Acc Hold Ckts	2.03.06	9052	Stg Bus to SR	2.08.01
32	9040	Acc to Stg Bus	2.08.25	9053	OP Pnl. Key to SR	2.08.26
31	9039	MQ Reg to Stg Bus	2.08.27	9054	Shift MQ Left	2.08.17
30	9038	Add (Q-B) to Acc	2.08.09	9055	(1) to MQ (35) 2.08.20	SR (5-35) to MQ 2.08.15
29	9037	Adder to Acc Ctrl	2.08.23	9056	Adder (1-8) to MQ (1-8) 2.08.46	Shift MQ Right 2.08.16
28	9036	Adri Sw to Storage Bus	2.08.28	9057	2.08.21	2.08.22
27	9035	ORs 2.07. 23 ORA 2.07.25	FP ADD/ SUB 2.07.10	9058	2.08.22	2.08.22
26	9034	(+) to Acc (5) 2.08.13	True Acc CAS 2.07.34	9059	2.08.21	2.08.22
25	9033	Comp Acc	2.08.07	9060	2.08.21	2.08.22
24	9032	Late A6 (D4) 2.09	ER Time 2.09	9061	2.08.21	2.08.22
23	9031	Divide Ctrl	2.07.08	9062	2.08.21	2.08.22
22	9030	(-) to Sense 3.12	ACC (5) 2.08.14	9063	2.08.21	2.08.22
21	9029	MPY Ctrl	2.07.27	9064	2.08.21	2.08.22
20	9028	T1 - Tgr Rotate MQ 2.04.07	2.10.02	9065	2.08.21	2.08.22
19	9027	Cond Transfer Ctrl	2.07.02	9066	2.08.21	2.08.22
18	9026	LRS 2.07.18	LLS 2.07.17	9067	2.08.21	2.08.22
17	9025	F.P. ADD/SUB	2.07.10	9068	2.08.21	2.08.22
16	9024	2.07.04	2.07.05	9069	2.08.21	2.08.22
15	9023	2.07.11	2.07.05	9070	2.08.21	2.08.22
14	9022	Acc/SUB, Clear & ADD/SUB	2.07.05	9071	2.08.21	2.08.22
13	9021	FP MPY	2.07.11	9072	2.08.21	2.08.22
12	9020	Store Ctrl	2.07.13	9073	2.08.21	2.08.22
11	9019	FP Divide Ctrl	2.07.12	9074	2.08.21	2.08.22
10	9018	FAD/FSB	2.03.05	9075	2.08.21	2.08.22
9	9017	Acc (S) Hold	2.07.10	9076	2.08.21	2.08.22
8	9016	FP ADD/SUB Crls	2.07.10	9077	2.08.21	2.08.22
7	9015	Sign (S) Mixing Ckts	2.11.01	9078	2.08.21	2.08.22
6	9014	Zero Sh Ctr 3.07	2.06.01	9079	2.08.21	2.08.22
5	9013	Overflow Tgr	2.11.01	9080	2.08.21	2.08.22
4	9012	Sign (S) Mixing Ckts	2.11.01	9081	2.08.21	2.08.22
3	9011	Pulse and Gate Generator	2.09	9082	2.08.21	2.08.22
2	9010	Pulse & Gate Generator	2.09	9083	2.08.21	2.08.22
1	9009	Pulse and Gate Generator	2.09	9084	2.08.21	2.08.22

FIGURE 53-1. CPU PANEL 1 LOCATION CHART

704.53.00 CENTRAL PROCESSING LOCATION CHARTS

CENTRAL PROCESSING UNIT 3 LOCATION CHART

35	9193	True Acc to Addr	2.08.06																						
34	9117	Store Control in Storage	1.04.05																						
33	5101	Pulse Gen II	1.05.03						5104	Turn off Inhibit and Wr Gate	1.05.03														
32	5102	Turn on Read Gate & Turn off Read & Rd Bias Gate	1.05.02						5110	Read Out Sample	1.05.02														
31	5103	RI Sample & Turn on Inhibit & Write Gate	1.05.02						5110	Read Out Sample	1.05.02														
30	5106	RI Sample	1.05.02						5106	Drum Addr Gate	7.02.01														
29	5107	Use Time	1.05.01						5112	IC 17 Input	3.20														
28	9134	IR 17 (-) ERB(01) 3.06	3.05						5113	Inst Reg (10-17) - 3.06 (-) ERB(01) 3.05															
27	9138	Inst Register (10-17)							5113	Trap TRA	3.20.02														
26	9110	Inst Reg (10-17) 3.06	(+) on Set (9) to Sh Ctr 3.05						5105	Instruction Register (10-17)	3.06														
25	9107	Instruction Register (10-17)							5105	Adr Register (6-8)	3.42														
24	9106	Inst Reg (6-9) 3.04	(-) on Set (2) to Sh Ctr 3.05						2403	Instruction Register (6-9)	3.04														
23	9105	Adv Ic 3.20	Binary Input to Sh Ctr Adv Ic 3.05						2408	Instruction Register (6-9)	3.04														
22	9104	Secondary Operation Decoder							9122	Adr to Instruction Counter	3.20.02														
21	9103	Primary Operation Decoder																							
20	9102	Primary Operation Decoder																							
19	9101	Primary Operation Decoder							9021	I Time	3.40														
18	9109	Instruction Register (4 & 5)							9126	Inst Reg (5) 3.02															
17	9109	Instruction Register (2 & 3)							9129	Inst Reg (5) 3.02															
16	9108	Instruction Register(0&1)																							
15	9163	Unit Select Matrix							9112	Class Decoder	5.01.01														
14	9132	Unit Selector							9116	Class Selector	5.01.03														
13	9076	I/O Selection Inlk	5.01.04						9115	Tr Ctrl	3.10.06														
12	9114	Class Selector							9125	Class Select	5.01.03														
11	9161	Disconnect Synchronizer							9172	EOR Intlk	5.09.01														
10	9201	Unit Selector	5.01.05						9193	Drum Disc	7.01														
9	9007	Drum Counter (6-11)							9011	Drum Adder Gate	7.02.01														
8	9006	Gated No Carry	7.02.02						9012	Drum Read/Write Control	7.01														
7	9005	Drum Counter (1-5)							9010	Drum Read/Write Control															
6	9004	Drum Interface Counter							9009	Drum Read/Write Control															
5	9044	F. P. Tally Counter							9008	Drum Counter Switching															
4	2611	Tape Group Counter							9192	Suppress TU Disc	6.02.04														
3	9187	Tape Word Comp	6.02.03																						
2	9185	Tape Write Ctrl	6.02.01						9186	Start Time Cycle	6.02.02														
1	9188	Tape Proceed	6.02.01						9189	Tape Function Selector															

FIGURE 53-3. CPU PANEL 3 LOCATION CHART

704.54.00 I/O SHOE CONNECTOR CHART

I/O Bus	MF Edge Conn	Shoe Conn	PR1				PR2		STORAGE BUS				TAPE BUS			DRUM		
			Calc	Exit	Calc	Entry	MF Edge Conn	MF Shoe	CF Shoe	CF1 Panel Conn	SYS	Shoe Conn	Edge Conn	SYS	Shoe Conn	Edge Conn	SYS	
Col (5)	2-03e	1 Lt	4-03e	5.12.01	4-03b	5.12.01	2-03h	69	67	J08-4	1.03.01	MF-TS (19)	MF4-03K	70.04.05	MF-DF (7)	01-a	7.03	
"	"	130 Rt	4-03f	"	4-03c	"	"	"	"	"	&2.05.01	"	"	"	"	"	"	
Col (1)	2-04e	9 Lt	4-04g	"	4-04b	"	2-04h	85	83	J09-4	1.03.01	MF-TS (17)	MF4-04L	"	MF-DF (5)	01-b	"	
"	"	138 Rt	4-04h	"	4-04c	"	"	"	"	"	&2.05.02	"	"	"	"	"	"	
Col (2)	2-05e	17 Lt	4-05e	"	4-05b	"	2-05h	101	99	J10-4	1.03.01	MF-TS (16)	MF4-05K	70.04.06	MF-DF (3)	01-c	"	
"	"	146 Rt	4-05f	"	4-05c	"	"	"	"	"	&2.05.02	"	"	"	"	"	"	
Col (3)	2-06e	25 Lt	4-06g	"	4-06b	"	2-06h	117	115	J11-4	1.03.01	MF-TS (14)	MF4-06L	"	MF-DF (1)	02-a	"	
"	"	154 Rt	4-06h	"	4-06c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (4)	2-07e	33 Lt	4-07e	"	4-07b	"	2-07h	133	131	J12-4	1.03.01	MF-TS (12)	MF4-07K	70.04.07	MF-DF (16)	02-b	"	
"	"	3 Rt	4-07f	"	4-07c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (5)	2-08e	41 Lt	4-08g	"	4-08b	"	2-08h	149	147	J13-4	1.03.01	MF-TS (10)	MF4-08L	"	MF-DF (14)	02-c	"	
"	"	11 Rt	4-08h	"	4-08c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (6)	2-09e	49 Lt	4-09e	5.12.03	4-09b	5.12.03	2-09h	78	76	J14-4	1.03.01	"	"	"	MF-DF (12)	03-a	"	
"	"	19 Rt	4-09f	"	4-09c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (7)	2-10e	57 Lt	4-10g	"	4-10b	"	2-10h	94	92	J15-4	1.03.01	"	"	"	MF-DF (10)	03-b	"	
"	"	27 Rt	4-10h	"	4-10c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (8)	2-11e	65 Lt	4-11e	"	4-11b	"	2-11h	110	108	J16-4	1.03.01	"	"	"	MF-DF (23)	03-c	"	
"	"	35 Rt	4-11f	"	4-11c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (9)	2-12e	73 Lt	4-12g	"	4-12b	"	2-12h	126	124	J17-4	1.03.01	"	"	"	MF-DF (21)	04-a	"	
"	"	43 Rt	4-12h	"	4-12c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (10)	2-13e	81 Lt	4-13e	"	4-13b	"	2-13h	142	140	J18-4	1.03.01	"	"	"	MF-DF (19)	04-b	"	
"	"	51 Rt	4-13f	"	4-13c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (11)	2-14e	89 Lt	4-14g	"	4-14b	"	2-14h	119	113	J19-4	1.03.01	"	"	"	MF-DF (17)	04-c	"	
"	"	59 Rt	4-14h	"	4-14c	"	"	"	"	CF2	&2.05.03	"	"	"	"	"	"	
Col (12)	2-15e	97 Lt	4-15e	"	4-15b	"	2-15h	67	69	H08-1	1.03.02	"	"	"	MF-DF (32)	05-a	"	
"	"	67 Rt	4-15f	"	4-15c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (13)	2-16e	105 Lt	4-16g	"	4-16b	"	2-16h	83	85	H09-1	1.03.02	"	"	"	MF-DF (30)	05-b	"	
"	"	75 Rt	4-16h	"	4-16c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (14)	2-17e	113 Lt	4-17e	"	4-17b	"	2-17h	99	101	H10-1	1.03.02	"	"	"	MF-DF (28)	05-c	"	
"	"	83 Rt	4-17f	"	4-17c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (15)	2-18e	121 Lt	4-18g	"	4-18b	"	2-18h	115	117	H11-1	1.03.02	"	"	"	MF-DF (26)	06-a	"	
"	"	91 Rt	4-18h	"	4-18c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	
Col (16)	2-19e	129 Lt	4-19e	"	4-19b	"	2-19h	131	133	H12-1	1.03.02	"	"	"	MF-DF (39)	06-b	"	
"	"	99 Rt	4-19f	"	4-19c	"	"	"	"	"	&2.05.03	"	"	"	"	"	"	

FIGURE 54-1. I/O SHOE CONNECTOR CHART

I/O Bus	MF Edge Conn	Shoe Conn	PR1		PR2		STORAGE BUS					TAPE BUS			DRUM		
			Calc	Exit	Calc	Entry	MF Edge Conn	MF Shoe	CF Shoe	CF1 Panel Conn	SYS	Shoe Conn	Edge Conn	SYS	Shoe Conn	Edge Conn	SYS
Col (17)	2-20e	137 Lt	4-20g	5.12.03	4-20b	5.12.03	2-20h	147	149	H13-1	1.03.02				MF-DF (37)	06-c	7.03
		107 Rt	4-20h	"	4-20c	"					&2.05.03						
Col (18)	2-21e	145 Lt	4-21e	"	4-21b	"	2-21h	76	78	H14-1	1.03.02				MF-DF (35)	07-a	"
		115 Rt	4-21f	"	4-21c	"					&2.05.02						
Col (19)	2-22e	153 Lt	4-22g	"	4-22b	"	2-22h	92	92	H15-1	1.03.02				MF-DF (33)	07-b	"
		123 Rt	4-22h	"	4-22c	"					&2.05.02						
Col (20)	2-23e	2 Lt	4-23e	"	4-23b	"	2-23h	108	110	H16-1	1.03.02				MF-DF (48)	07-c	"
		131 Rt	4-23f	"	4-23c	"					&2.05.02						
Col (21)	2-24e	10 Lt	4-24g	"	4-24b	"	2-24h	124	126	H17-1	1.03.02				MF-DF (46)	08-a	"
		139 Rt	4-24h	"	4-24c	"					&2.05.03						
Col (22)	2-25e	18 Lt	4-25e	"	4-25b	"	2-25h	140	142	H18-1	1.03.02				MF-DF (44)	08-b	"
		147 Rt	4-25f	"	4-25c	"					&2.05.03						
Col (23)	2-26e	26 Lt	4-26g	"	4-26b	"	2-26h	128	122	H19-1	1.03.02				MF-DF(42)	08-c	"
		155 Rt	4-26h	"	4-26c	"					&2.05.03						
Col (24)	2-27e	34 Lt	4-27e	"	4-27b	"	2-27h	65	71	J08-4	1.03.03				MF-DF (55)	09-a	"
		4 Rt	4-27f	"	4-27c	"					&2.05.03						
Col (25)	2-28e	42 Lt	4-28g	"	4-28b	"	2-28h	81	87	J09-4	1.03.03				MF-DF (53)	09-b	"
		12 Rt	4-28h	"	4-28c	"					&2.05.03						
Col (26)	2-29e	50 Lt	4-29e	"	4-29b	"	2-29h	97	103	J10-4	1.03.03				MF-DF (51)	09-c	"
		20 Rt	4-29f	"	4-29c	"					&2.05.03						
Col (27)	2-30e	58 Lt	4-30g	"	4-30b	"	2-30h	113	119	J11-4	1.03.03				MF-DF (49)	10-a	"
		28 Rt	4-30h	"	4-30c	"					&2.05.03						
Col (28)	2-31e	66 Lt	4-31e	"	4-31b	"	2-31h	129	135	J12-4	1.03.03				MF-DF (64)	10-b	"
		36 Rt	4-31f	"	4-31c	"					&2.05.03						
Col (29)	2-32e	74 Lt	4-32g	"	4-32b	"	2-32h	144	138	J13-4	1.03.03				MF-DF (62)	10-c	"
		44 Rt	4-32h	"	4-32c	"					&2.05.03						
Col (30)	2-33e	82 Lt	4-33e	5.12.04	4-33b	5.12.04	2-33h	74	80	J14-4	1.03.03	MF-TS (35)	MF4-33K	70.07.02	MF-DF (60)	11-a	"
		52 Rt	4-33f	"	4-33c	"					&2.05.03						
Col (31)	2-34e	90 Lt	4-34g	"	4-34b	"	2-34h	90	96	J15-4	1.03.03	MF-TS (33)	MF4-34L	70.07.02	MF-DF (58)	11-b	"
		60 Rt	4-34h	"	4-34c	"					&2.05.03						
Col (32)	2-35e	98 Lt	4-35e	"	4-35b	"	2-35h	106	112	J16-4	1.03.02	MF-TS (32)	MF4-35K	70.07.03	MF-DF (71)	11-c	"
		68 Rt	4-35f	"	4-35c	"					&2.05.03						
Col (33)	2-36e	106 Lt	4-36g	"	4-36b	"	2-36h	122	128	J17-4	1.03.03	MF-TS (30)	MF4-36L	70.07.04	MF-DF (69)	12-a	"
		76 Rt	4-36h	"	4-36c	"					&2.05.03						

I/O SHOE CONNECTOR CHART

I/O Bus	MF Edge Conn	PR 1			PR 2		STORAGE BUS					TAPE BUS			DRUM		
		Shoe Conn	Calc	Exit	Calc	Entry	MF Edge Conn	MF Shoe	CF Shoe	CF Panel Conn	SYS	Shoe Conn	Edge Conn	SYS	Shoe Conn	Edge Conn	SYS
Col (34)	2-37e	114 Lt	4-37e	5.12.04	4-37b	5.12.04	2-37h	138	144	J18-4	1.03.03	MF-TS (28)	MF4-37k	70.07.03	MF-DF (67)	12-b	703
		84 Rt	4-37f	"	4-37c	"					82.05.03						
Col (35)	2-38e	122 Lt	4-38g	"	4-38b	"	2-38h	135	129	J19-4	1.03.03	MF-TS (26)	MF4-38l	70.07.04	MF-DF (65)	12-c	"
		92 Rt	4-38h	"	4-38c	"					82.05.03						
Adr Reg (5)							3-Qf	80	74		3.42						
AR (6)							3-25g	7	1	1-Ka	"						
AR (7)							3-25f	16	10	1-Kd	"						
AR (8)							3-25e	5	3	1-La	"						
AR (9)							3-26h	14	12	1-Ld	"						
AR (10)							2-26g	3	5	1-Ma	"						
AR (11)							3-26f	19	21	1-Md	"						
AR (12)							3-27g	12	14	1-Na	"						
AR (13)							3-27f	1	7	1-Nd	"						
AR (14)							3-27e	17	23	1-Pa	"						
AR (15)							3-28h	10	16	1-Pd	"						
AR (16)							3-Ne	23	17	1-Qa	"						
AR (17)							3-29b	32	26	1-Qd	"						
Turn off Rd & Rd Bias Gate							3-De	21	19	2-Eb	1.05.02						
Turn off Write Gate							3-33g	26	32	2-Jd	1.05.03						
Read in Sample							3-31d	28	30		1.05.02						
Reset SAR & Buffer Reg							3-He	30	30	1-Jd	1.05.03						
Turn off Inhibit Gate							3-33e	33	39	2-Md	1.05.03						
Turn on Inhibit & Wr Gate							3-31b	35	37	2-Ka	1.05.02						
SAR RI & Turn on Read Bias Gate Stg 2							3-Ng	37	35	1-Rd	1.05.03						
Reset SAR & Buffer Reg Stg 2							3-Fh	48	42	1-Jd	1.05.03	MF-TS (48)	3-Kb	6.01			
SAR RI & Turn on Rd Bias Gate							3-34h	51	53	1-Rd	1.05.03	MF-TS (51)	3-Dc	6.03.04			
RO Sample							3-30h	53	51	2-Mb	1.05.02						
Turn on Rd Gate							3-31e	55	49	2-Ga	"						
RI Sample Stg 2							3-31m	71	65	2-Nd	"						
RO Sample Stg 2							3-Qh	96	90		"						
Pr Select		7	4-Lb	5.01.06								MF-TS (7)	3-Qd	6.01	Intlk Reset		
		14			4Fd	5.05.05	Pr Sense	Thy Plates									
Pr Rd Set		23	4-Lc	5.01.06													
	Pr Sense (1)	29			4Ja	5.05.05											
Pr Wr Sel	" (2)	30	4-Ld	5.01.06	4Jc	5.05.05											
	" (3)	31			4Fb	"											
	" (4)	32			4Fc	"											
Pr Disc	" (5)	37	4-Jd	5.01.06	4Ga	"						MF-TS (37)	2-Rb	6.03.03	Tape Exit		
	" (6)	38			4Gb	"											
	" (7)	39	4-Ka	5.01.06	4Gc	"	3-Qg	39	46	1-Pb	1.04.05	MF-TS (39)	3-Cb	6.02.04	Clock Gate Delay		
	" (8)	40			4Gd	"											

I/O Bus	MF Edge Conn.	Shoe Conn.	PR1		PR2		STORAGE BUS					TAPE BUS			DRUM				
			Calc	Exit	Calc	Entry	MF Edge Conn.	MF Shoe	CF Shoe	CF Panel Conn.	SYS	Shoe Conn.	Edge Conn.	SYS	Shoe Conn.	Edge Conn.	SYS		
Pr Sense (9)		45			4-Ha	5.05.05													
" " (10)		46	4-01a	5.11.01	4-Hb	"	3-Gh	46	44	1-Ab	1.04.05	MF-TS (46)	MF3-Qb						
CB Signal		47			4-01f	5.11.01													
Pn/Pr Thy Plate		53 Lt	4-Qa	5.12.01								MF-TS (53)	MF3-Nd	6.01					
" " " "		54-Rt	4-Ra	"															
" " " "		55 Lt	4-Qe	5.12.03								MF-TS (55)	MF3-Ga	6.02.01					
" " " "		56 Rt	4-Re	"															
CR-EOF		62	3-12g	5.09.01			2-39e	62	60	2-Ma	4.08	MF-TS (62)	MF3-Da	6.02.04					
" "		63	3-12h	"															
CR-EOR		69	3-13e	"								MF-TS (69)	MF3-Fd	6.03.04					
" "		72	3-13f	"															
Fuse Blow		78	4-26f	4.05.03								MF-TS (78)	MF3-Dd	6.02.01	MF-DF (78)	3-05g	7.05		
Cr Sel & Pn Sel		101	4-Ma	5.01.06	4-Mc	5.01.06													
Cr & Pn Disc		103	4-Kd	"	4-Kb	"													
Cr & Pn Sel		110	4-Mb	"	4-Md	"									128	4-39a	4.10		
Cr & Pn Disc		112	4-La	"	4-Kc	"													
Pr Sense Entry		117	4-Ep	5.05.06															
Pn Sense		125			4-Hc	5.05.06													
" "		126			4-Hd	"													
Pr Sense		127			4-Jb	"													
							3-Gf	42	48	1-Jb	1.04.05	MF-TS (42)	MF3-Qc	6.01					
							3-Qe	44	46	1-Pb	"	MF-TS (44)	MF3-Lc	"					
							3-Mh	49	55	2-Qa	1.07	MF-TS (49)	MF3-Ha	"					
							1-21h	58	64	2-Db	1.06.02	MF-TS (58)	MF3-11b	6.02.04					
							4-22m	60	62	2-Nc	"	MF-TS (60)	MF3-11c	"					
							1-Fe	64	58	1-Ja	2.07.23	MF-TS (64)	MF3-Db	6.01.01					
												MF-TS (65)	MF3-Bc	6.02.01					
												MF-TS (67)	MF3-Cc	6.03.01					
												MF-TS (74)	MF3-Ga	6.02.02	MF-DF (74)	3-06h			
												MF-TS (76)	MF3-Gc	6.02.04	MF-DF (76)	3-07f	7.03		
												MF-TS (80)	MF3-Bd	6.01	MF-DF (80)	3-05f	7.01.01		
												MF-TS (89)	3-Eb	5.01.05	MF-DF (81)	3-07e	7.01.01		
												MF-TS (90)	3-Ed	"	MF-DF (83)	3-06g	7.01.01		
												" (91)	3-Ec	"	MF-DF (85)	3-07g	7.03		
												" (92)	3-Fb	"	MF-DF (87)	3-06f	7.03		
												" (93)	3-Fa	"	" (97)	3-08g	7.04		
												" (94)	3-Fc	"	" (99)	3-09f	"		
												" (95)	3-Aa	"	Drum (101)	3-10e	"		
												" (96)	3-Ab	"	Sel (103)	3-09e	"		
												" (97)	3-Ac	"	106	3-08f	"		
												" (98)	3-Bb	"	108	3-10f	"		
												" (129)	3-Ea	6.02.01	110	3-08h	"		
															112	3-09g	"		

704.55.00 704 MAIN FRAME NEON LOCATIONS

MF 1		A09-3 Drum Ctr 7	7.02.01
A01-7 after 8 CB	5.11.04	A09-4 Drum Ctr 8	7.02.01
A04-2 MQ loaded by copy	5.03.03	A11-4 Intlk. Reset Timing	5.09.02
A06-4 ER3 (D1)	5.08.01	A12-1 Tape RWD Select	5.01.03
A07-2 A10 (D5)	5.08.04	A12-3 Drum Read Select	5.01.03
A09-5 MQ RI Gate Tgr.	5.10	A12-6 Tape Write EOF Select	5.01.03
A09-6 MQ RI Ctrl. Tgr.	5.10	A12-8 Tape Read Select	5.01.03
A10-5 I8 to CT1	2.09	A14-1 I/O Select 2	5.01.05
A10-7 E8 to CT1	2.09	A14-3 I/O Select 1	5.01.05
A12-6 Clock Drive	8.04	A14-6 I/O Select 3	5.01.05
A14-3 End Op Tgr.	8.05.01	A14-8 I/O Select 4	5.01.05
A17-7 A6 (D4)	2.09	J01-2 Tape Write Call	6.01
A18-3 Not used		J01-4 Tape BKSP Call	6.01
A18-7 Q Carry Tgr.	2.06.01	J01-6 Tape Read Call	6.01
A22-7 Overflow Tgr.	2.06.01	J01-7 Tape Select	6.01
J01-3 On Read/Write Time	5.11.04	J02-2 Start Tape Cycle	6.02.02
J01-4 CB Ctr	5.11.04	J02-5 RDN Error	6.03.01
J01-5 CB Ctr	5.11.04	J04-2 Tape Disconnect	6.02.04
J01-6 CB Ctr	5.11.04	J04-5 Tape Coding Selector	6.01.01
J03-2 Read Right	5.11.02	J04-6 Tape Coding Selector	6.01.01
J03-3 Read Left	5.11.02	J05-2 15 MS Delay	7.02.01
J03-6 Write Right	5.11.02	J05-3 Minus on SW Delay	7.02.01
J03-7 Write Left	5.11.02	J06-4 14 MS Delay	7.01
J04-2 T02 Copy Proceed	5.03.04	J05-5 Interrogate 9 Carry	7.02.01
J04-6 T04 On Copy Proceed	5.03.04	J06-6 Index received	7.01
J07-3 RD/WR Execution timer	5.02	J06-7 Index pulse received	7.01
J14-2 Clock A0	8.04	J07-6 Drum Copy	7.01
J14-3 Clock A2	8.04	J07-7 Delayed Read Gate	7.01
J14-5 Clock A4	8.04	J10-2 Write Disc. Cond.	7.01
J14-7 Clock A6	8.04	J11-2 EOR Interlock	5.09.01
J14-8 Clock A8	8.04	J11-6 Interlock reset timing	5.09.02
J15-2 Clock A1	8.04	J11-7 EOF Interlock	5.09.01
J15-3 Clock A3	8.04	J12-1 CR EOR Initiate	5.09.01
J15-5 Clock A5	8.04	J13-3 CR Read Select	5.01.03
J15-7 Clock A7	8.04	J13-6 Drum Write Select	5.01.03
J15-8 Clock A9	8.04	J13-8 Tape Write Select	5.01.03
J16-2 Clock A10	8.04	J14-1 PR Write Select	5.01.03
J16-3 Clock A11	8.04	J14-3 Tape Read Select	5.01.03
J20-6 I Time	8.05.03	J14-6 PR Read Select	5.01.03
J21-6 E Time	8.05.03	J14-8 Punch Write Select	5.01.03
J22-3 E/R Time	8.05.03	J25-3 Adr. Line 6	3.42
J23-6 CT Tgr.	8.05.03	J25-5 Adr. Line 7	3.42
J24-4 9 Overflow Tgr.	2.06.02	J25-7 Adr. Line 8	3.42
J24-6 9 Carry Tgr.	2.06.02	J26-3 Adr. Line 9	3.42
MF 2		J26-5 Adr. Line 10	3.42
A03-4 Acc P Pos.	2.03.02	J26-7 Adr. Line 11	3.42
A03-3 Tape Redundancy Ctr	6.03.03	J27-3 Adr. Line 12	3.42
J01-6 Ring Shift Ctr Tgr	6.03.02	J27-5 Adr. Line 13	3.42
J02-5 Tape Gate Tgr.	6.03.01	J27-7 Adr. Line 14	3.42
MF 3.		J28-3 Adr. Line 15	3.42
A03-4 Start Sync. Clock	6.02.01	J28-5 Adr. Line 16	3.42
A03-7 Tape Cpy Proceed	6.02.01	J28-7 Adr. Line 17	3.42
A04-3 RD/WR End Op On Tape	6.02.03	J29-1 Used for Two Core Frame Operation	
A04-7 Tape Word Complete	6.02.03	MF 4	
A04-8 Minus on Tape Word Complete	6.02.03	A06-3 Adder 6 Carry Tgr.	2.06.04
A05-2 Tally Ctr First Step	2.10.01	A19-1 T _k Turn on Ld Ctr Tgr	4.19
A05-3 Tally Ctr Second Step	2.10.01	A19-3 Load Ctr Tgr	4.19
A05-6 Tally Ctr Third Step	2.10.01	A20-1 Stg Display Ctr Tgr	4.18
A05-7 Tally Ctr Fourth Step	2.10.01	A21-1 Full & Multi step key tgr.	4.07
A06-2 Interlace Ctr	7.02.02	A22-2 Turn off MST Synchronizer	4.05.01
A06-3 Interlace Ctr	7.02.02	A22-5 Master Stop Tgr.	4.05.04
A06-4 Interlace Ctr	7.02.02	A23-8 Start Button Key Tgr.	4.05.01
A06-7 First Word Located	7.02.02	A27-6 Reset Button Key Tgr.	4.09
A07-1 Drum Ctr 1	7.02.01	A28-3 Enter MQ Key Tgr.	4.03
A07-3 Drum Ctr 2	7.02.01	A28-7 Op. Panel Tgr.	4.05.01
A07-4 Drum Ctr 3	7.02.01	A29-6 Enter Inst. Key Tgr.	4.17
A07-6 Drum Ctr 4	7.02.01	A34-2 Hold Tag Tgr.	
A07-7 Drum Ctr 5	7.02.01	J01-7 CB Signal Set Key Tgr.	5.11.01
A08-1 Minus on no Gated Carry	7.02.02	DISTRIBUTOR	
A08-3 Drum Ctr 11	7.02.01	MF 4	
A08-5 Drum Ctr 9	7.02.01	J03 to J38, 01 Read Left Key Tgr.	5.12.01 to 5.12.04
A08-6 True end Carry	7.02.01	J03 to J38, 08 Read Right Key Tgr.	5.12.01 to 5.12.04
A09-1 Drum Ctr 6	7.02.01		

704.55.00 704 CPU NEON LOCATION

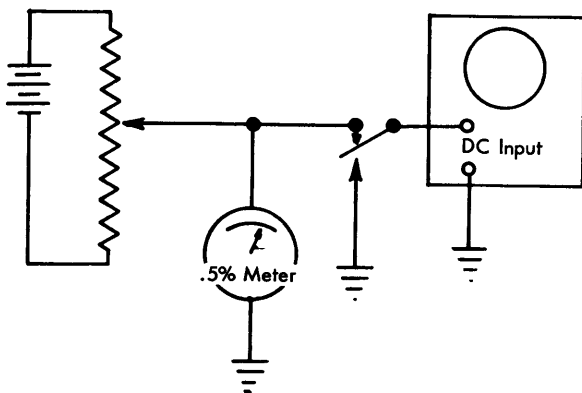
704.56.00 OSCILLOSCOPE

704.56.01 Scope Calibration

Of the two dimensions which have to be calibrated in an oscilloscope, the vertical deflection is the most difficult. The sweep time can be calibrated by using the output of the one megacycle oscillator in the main frame clock.

An acceptable method of calibrating the vertical deflection of a scope is illustrated in the Figure 45-1. Essentially it consists of deflecting the oscilloscope beam a known number of volts and adjusting the gain of the D. C. amplifier to make the voltage represent a certain number of centimeters of deflection. There are certain points which should be emphasized to insure accuracy. They are:

1. The meter used to measure the voltage should be a single range, high quality meter (accuracy of .5% at full scale). A single range meter is one with a separate terminal for each voltage range.
2. A meter of this type usually has a relatively low impedance and should remain in the circuit throughout the calibration process.
3. The range of the meter and the calibration voltage should provide a meter deflection of at least 75% of full scale. This is to insure maximum meter accuracy.
4. There will always be a certain amount of error introduced in adjusting the deflection. This is due to parallax, beam width and poor judgment. This error is independent of the magnitude of the deflection. Therefore, greater accuracy can be achieved by making the beam deflection as large as possible. For example: If it is desired to calibrate the vertical deflection to 10v per cm., a more accurate calibration can be made by having 50v give a deflection of five centimeters than by having 10v give a deflection of one centimeter.
5. The calibration should allow a reasonably sized waveform to be displayed on the oscilloscope screen. A larger waveform provides more accuracy.
6. The oscilloscope should have a direct probe, when measuring the waveforms from low impedance circuits. An improperly compensated probe attenuator will give erroneous results when measuring short pulses, after this type of calibration.



Battery or DC Supply from Machine

FIGURE 56-1. CALIBRATION CIRCUIT

One advantage of this method of calibration is that it requires no special equipment. It can be assembled from parts already at the installation. The voltage source can be one of the machine power supplies when calibrating in the machine room. However, a self-contained calibrator can be assembled, using a dry cell for calibrating in the CE room.

704.56.02 Z Input - Oscilloscopes

The "Z" input of Tektronix Scopes, 535, 531, and 310 is a capacity input to the cathode of the scope. In operation, a positive going pulse to this input will blank the main trace and a negative input will intensify the main trace. Therefore, for example, if the sense amplifier output of the 737 is being displayed on the main trace and the sample is connected to the "Z" input; the memory sense amplifier output will be displayed with a "hole" where the rise of sample occurs. Thus, a 310 type scope or a scope without alternate sweep can be used to observe this timing.

This procedure is useful under the following conditions:

1. To observe the overlap of a pulse and its sample, with either a single input scope or where "chopped-sweep" is too slow, (memory sense amplifier output 704).
2. Adds a third input to the dual input scopes to check three conditions at once.

To accomplish this, it is recommended that the pulse giving the timing to the circuit under observation (example - "704" sample for mem.) be first displayed to ascertain its size and shape for meeting specs; it can then be connected to the "Z" input and the main gate or pulse displayed in the normal manner except that as the rise of the "Z" input pulse occurs it will "blank" the main trace leaving a "hole" in the trace and as the "Z" input falls it will intensify the main trace. The former condition is the more noticeable and very useful.

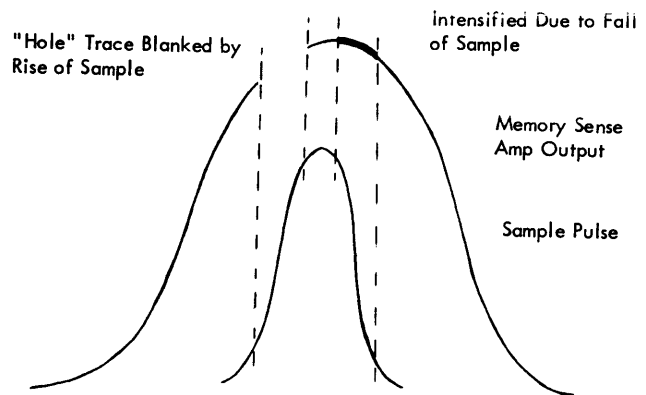
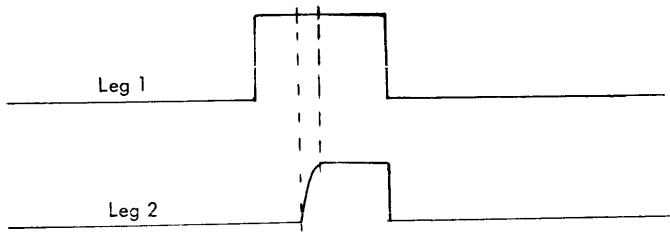


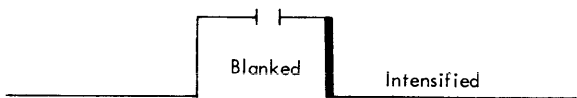
FIGURE 57-2. Z INPUT

Assume any two legs of an "and" circuit.



Using this procedure, display leg 2 for proper shape and levels, then connect to the "Z" input.

The following should then occur when displaying leg 1.



In the case of fast pulses where chopped-sweep frequency is too slow, this is the only sure way to compare pulses, since if the "hole" ever fills up you know your sampling pulse failed, but if displayed individually you might not recognize the failures.

It is also useful to display and sync on the occasional pulse with the "Z" input connected to the frequent pulse. This allows turning up intensity to observe the infrequent pulse and still not have the second pulse always present burning up the face of the scope (but still available for comparison when the trace does occur).

704.57.01 Timing, Sliver or Noise Troubles

Picking Up Bits on Clearing Storage

Installation of EC 243523 on Systems Diagrams, 1.05.02 will solve any problems of picking up bits on clearing storage.

The fall of the "reset storage to zeros" single shot affects a pulse on the input to the 4PCF, read control cathode followers, and tubes 07 and 08 CSF2J07. Tube 08 is very close to the ACS in column 24 and a large spike due to pickup is noted at N08-2 synchronizer on the fall of the "reset storage to zeros" single shot. This pulse was gated through with the RQ sample giving erroneous operation. The RO sample pulse is now gated with "minus on reset to zeros" from 1.05.01 so the spike will not be gated through.

Echo Checks on Write Card Line

Installation of EC 243522 on Systems Diagrams, 5.11.05 can be used to avoid echo checks caused by the 1 usec sliver on the write cards line.

During a read printer operation, a short sliver appears on the write cards line (5.11.05) caused by the fact that the "plus on write time" line falls after the "minus after 12 CB" line. This sliver can, if it is coincident with a copy, cause a premature "go to E" and "end opn". This change adds a 100 uuf capacitor on the output of AND circuit E on 5.11.05, thereby tying the output to ground through the capacitor which effectively removes the sliver.

Storage Register to Adders on TSX

A sliver carry condition due to the poor fall time of storage register (1-35) to adders (1-35) line on TSX can be cured by reducing the load resistor for OR circuit M in PU9014 on Systems Diagrams, 2.08.48.

MPR Troubles

The fall of the stg. reg. to adder line during the last ER time in MPR starts late in ER5 time and is not down till ER6.5 to ER7 time. This makes possible sliver adder outputs because of the "overlap" of the acc to adder gate ER6 (D4). No reasonable improvement of stg. reg. to adder fall time would eliminate this source of error. By delaying the acc to adder gate, the one to adder 35 gate and the adder to acc sample to I time removes the possibility of sliver type errors. This is easily done by changing the inputs to AND Circuit G on 2.07.07 (PU 9035) adding AND Circuit W on 2.08.23 (PU 9040) and one input to OR Circuit F on 2.08.06 (PU 9038).

Line Capacity in MF1 During ER Time

If noise is picked up in MF1 during ER time, or troubles occur during ER time, and ER9 (D1) or ER11 (D1) pulses are suspected, rerouting these pulses in MF1 to B/M 561673 will cut down on stray capacitance. This has given some trouble in the field.

Loading Troubles From Copy Checks

If loading troubles from copy checks show up from any I/O unit then the trouble could be in the copy proceed circuits. A noisy tube in pluggable unit MF1-J04 (Systems diagram, 5.03.04) is the chief cause. Particular attention should be given to the two trigger tubes (MF1-J04-02 or MF1-J04-04).

Distributor Thyratrons

Occasional failure of thyratrons to fire in the distributor (Systems 5.12.01, 5.12.03, 5.12.04) indicates necessity for higher bias on the shield grid. Replacement of the 680 ohm resistor with a 100 ohm resistor in the cathode resistor network on CF drives the shield grid to an up level of +10 volts. This is in contrast to the former up level of +3 volts, and results in pre-ionization grid current which increases firing reliability.

Adder P

At present "one to adder (P)", D40-7 Systems 2.08.43 has a down level of -20 to -22 volts. Addition of an amplifier between OR circuit D and CF 03B on Systems 2.08.43 in Pluggable Unit 9064 results in obtaining proper down level of -30 volts. With a poor down level, the "one to adder (P)" was coming up when it should not.

Adder X Carry Trigger

Poor rise time and up level of pulse on adder carry output line on Systems 2.02.03, results in the adder 4 carry trigger (adder 6 carry trigger with one 737) on Systems 2.06.04 to be turned on late or not turned on at all. The poor pulse form is due to an improper compensating capacitor in the output circuit of amplifier 03 on Systems 2.02.04. A 33 uuf capacitor must be inserted instead of the 15 uuf capacitor to cure this problem.

Card Control CB Counter Input (B/M 562883)

For a more reliable operation of the card control CB counter, a 5.1K limiting resistor in PU2521 on Systems 5.11.01 improves the down level on the "on end CB" pulse by reducing the current supplied by the -12v clamp in Ts01. Increasing the drives for this line to 2CF improves the fall time of the pulse.

MQ Sign Loading

If in ring shift operations the sign position fails, add 2CF to the output of the microsecond delay unit in PU9120 Systems 2.03.01 to drive the MQ register column S output.

Information Loading From Operator's Panel

If information from the operator's panel is loaded into the wrong place or at consecutive addresses, the trouble may be the loss of the -30 volts to the instruction entry keys of the address register. The keys float at about -5 volts instead of the required -30 volts. The trouble indication is when information is loaded at two consecutive full word addresses with each succeeding address displaced by one full word.

Replacing SS Tubes

If a single shot in a critical circuit becomes out of time, replace the SS with a tube that has been run-in on a less critical circuit and put the new tube in the less critical circuit.

704.57.03 Bias Troubles

Compare Accumulator (9-35) to Adder

If on ANS when biasing the -250v, a sliver is developed by the poor fall time of the compare acc (9-35) to adder line (Systems 2.08.07). If this puts wrong bits in storage, then EC 243687 should be installed.

On certain machines, dependent on wiring capacitance and the time required to change the acc reg. from one to zero, and during worst case problems in ANS, a sliver is developed which causes errors in the word stored on -250v bias and potentially at normal voltage. Addition of PCF 08B in PU9037 to power this line improves the fall time sufficiently to give good operation.

Sign Position of Storage Bus on FAD/FSB

If the sign position is unreliable when biasing the -150v to -142v in FAD/FSB then remove the 300 ohm resistor from the cathode of the storage bus S position PCF 08B in PU9190 in MF2A03, Island Pin E36-F36. A jumper must then be added from K36 to F36.

Address Register 14 & 17 Grid Inputs

These are the only two triggers in the address register with three grid inputs. If at low bias you have trouble turning them on, then B/M 562507 should be installed. This lays out the inputs to cut down on the capacitance.

Accumulator Sign

In biasing the acc sign position fails and cable capacity is suspected, replace the 15 uuf plate divider on the amplifier feeding CF05B on PU9036 with a 33 uuf compensating capacitor on Systems 2.08.14.

SECTION	TITLE	PAGE
704.60.00	AUTOMATIC MACHINE LOGIC	60-4
704.61.00	Machine Logic	
	Figure 61-1 704 Central Processing Unit	60-5
	Figure 61-2 704 Information Flow	60-6
	Figure 61-3 Information Processing Section Flow Diagram	60-7
704.62.00	I Cycle Data Flow	
	Figure 62-1 I Cycle Data Flow	60-8
	Figure 62-2 Basic True/Complement Circuits	60-9
	Figure 62-3 Storage Bus Switching	60-9
704.63.00	Instruction Timings and Data Flow	
	Figure 63-1 Indexable Transfer Instruction	60-10
	Figure 63-2 Accumulator Left Shift	60-11
	Figure 63-3 Long Left Shift Instruction	60-12
	Figure 63-4 Store Instruction	60-12
	Figure 63-5 Add Instruction	60-13
	Figure 63-6 Composite of Add, Subtract, Add Magnitude and Subtract Magnitude	60-14
	Figure 63-7 Multiply Instruction	60-15
	Figure 63-8 Multiply Instruction	60-16
	Figure 63-9 Example of Divide	60-17
	Figure 63-10 Divide Instruction	60-18
	Figure 63-11 Divide Instruction	60-19
	Figure 63-12 And to Accumulator Instruction	60-20
	Figure 63-13 And to Storage Instruction	60-21
	Figure 63-14 Transfer and Set Index Instruc- tion	60-22
	Figure 63-15 Store Index In Decrement Instruc- tion	60-22
	Figure 63-16 Transfer on Index Instruction	60-23
	Figure 63-17 Composite on TIX, TNX, TVH and TXL	60-24
	Figure 63-18 Composite on ANS and ANA	60-24
	Figure 63-19 Transfer in Trap Mode	60-25
	Figure 63-20 Compare Accumulator with Stor- age	60-25
	Figure 63-21 Floating Point Information Flow	60-26
	Figure 63-22 Floating Point Add and Subtract Instruction	60-27
	Figure 63-23 Unnormalized Floating Add Instruction	60-28
	Figure 63-24 Floating Point Add Instruction	60-28
	Figure 63-25 Floating Point Multiply Instruction	60-29
	Figure 63-26 Floating Point Multiply Instruction	60-30
	Figure 63-27 Floating Point Divide Instruction	60-31
	Figure 63-28 Floating Point Divide Instruction	60-32
704.64.00	I/O to CPU Data Flow	
	Figure 64-1 Information Paths Between the MQ and the I/O Units	60-33

SECTION	TITLE	PAGE
Figure 64-2	Card Machine Information Flow	60-34
Figure 64-3	Logic Flow of Information From Card Reader to MQ Register	60-34
Figure 64-4	Selection of a I/O Device	60-35
Figure 64-5	Card Machine Selector (5.01.06)	60-36
Figure 64-6	Card Machine Reading and Writing Data Flow	60-37
Figure 64-7	Drum Reading and Writing Data Flow	60-38
Figure 64-8	Logic Flow of 0762 RDS...0321	60-39
Figure 64-9	Read Select Reader 0762 RDS... 0321	60-40
Figure 64-10	Write Printer 0766 WRS...0361	60-41
Figure 64-11	Copy Instruction Following RDS ...0321	60-42
Figure 64-12	Copy Instruction Following RDS ...0321	60-43
Figure 64-13	Write Punch Records 0766 WRS ...0341	60-43
Figure 64-14	Copy Instruction Following WRS ...0361	60-44
Figure 64-15	Copy Following Write Select Printer	60-45
Figure 64-16	Copy Instruction After WRS... 0361	60-46
Figure 64-17	Disconnect from Card Punch	60-47

704.60.00 AUTOMATIC MACHINE LOGIC

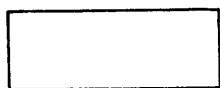
704.61.00 DATA FLOW

In this section we have tried to concentrate on the logic of the machine. We have tried to cover logic paths of instructions, key and button routings, internal wiring logic, internal data paths, timed sequences and data sequences of many of the machine operations.

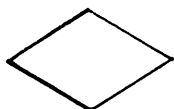
As in the trouble shooting charts, the shapes on the instruction data flow charts have a definite meaning.



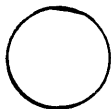
Overall objective of what is to be accomplished by the following blocks.



These will accomplish the overall objective of the above block.



Switch or decision



End of Operation

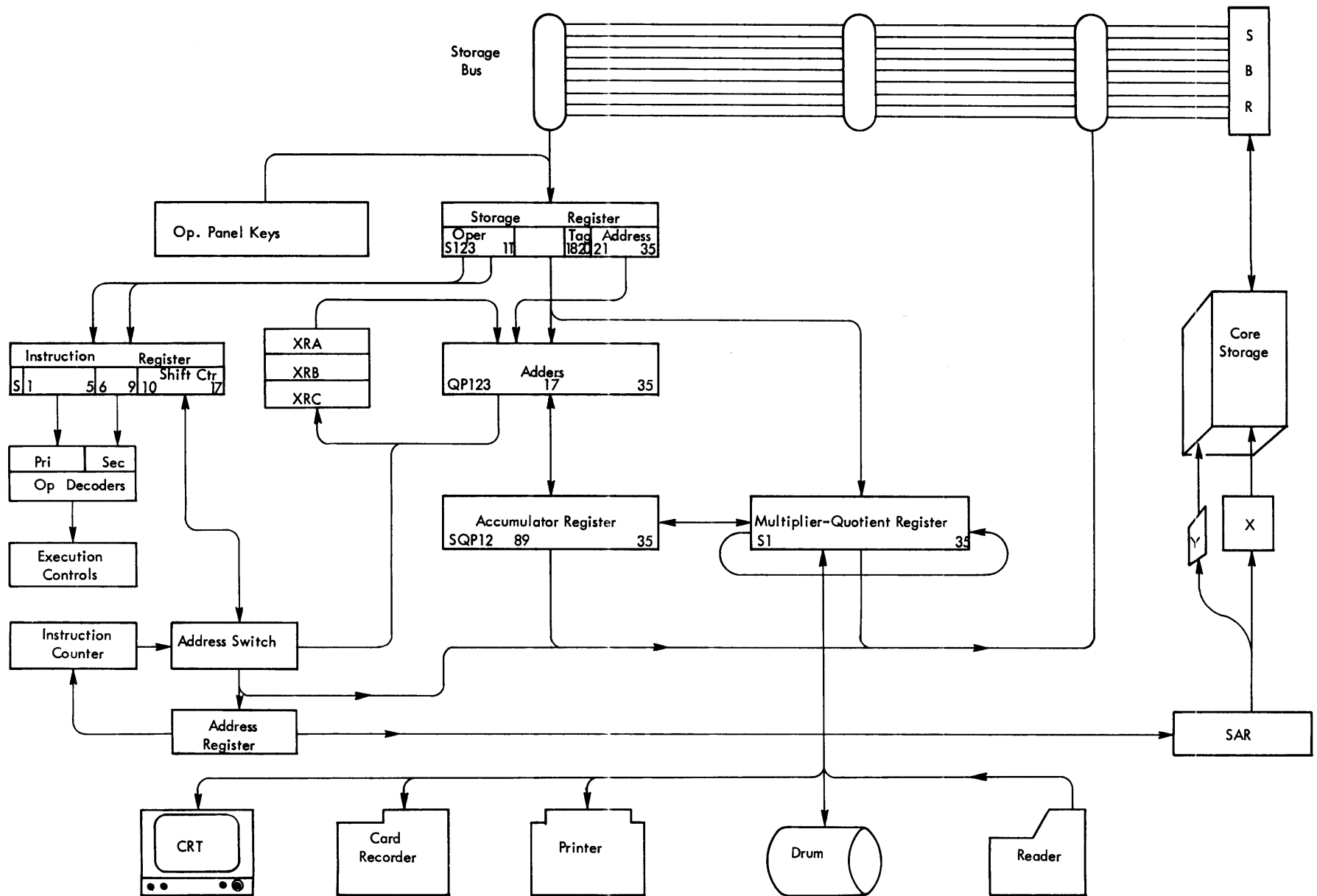


FIGURE 61-1. 704 CENTRAL PROCESSING UNIT

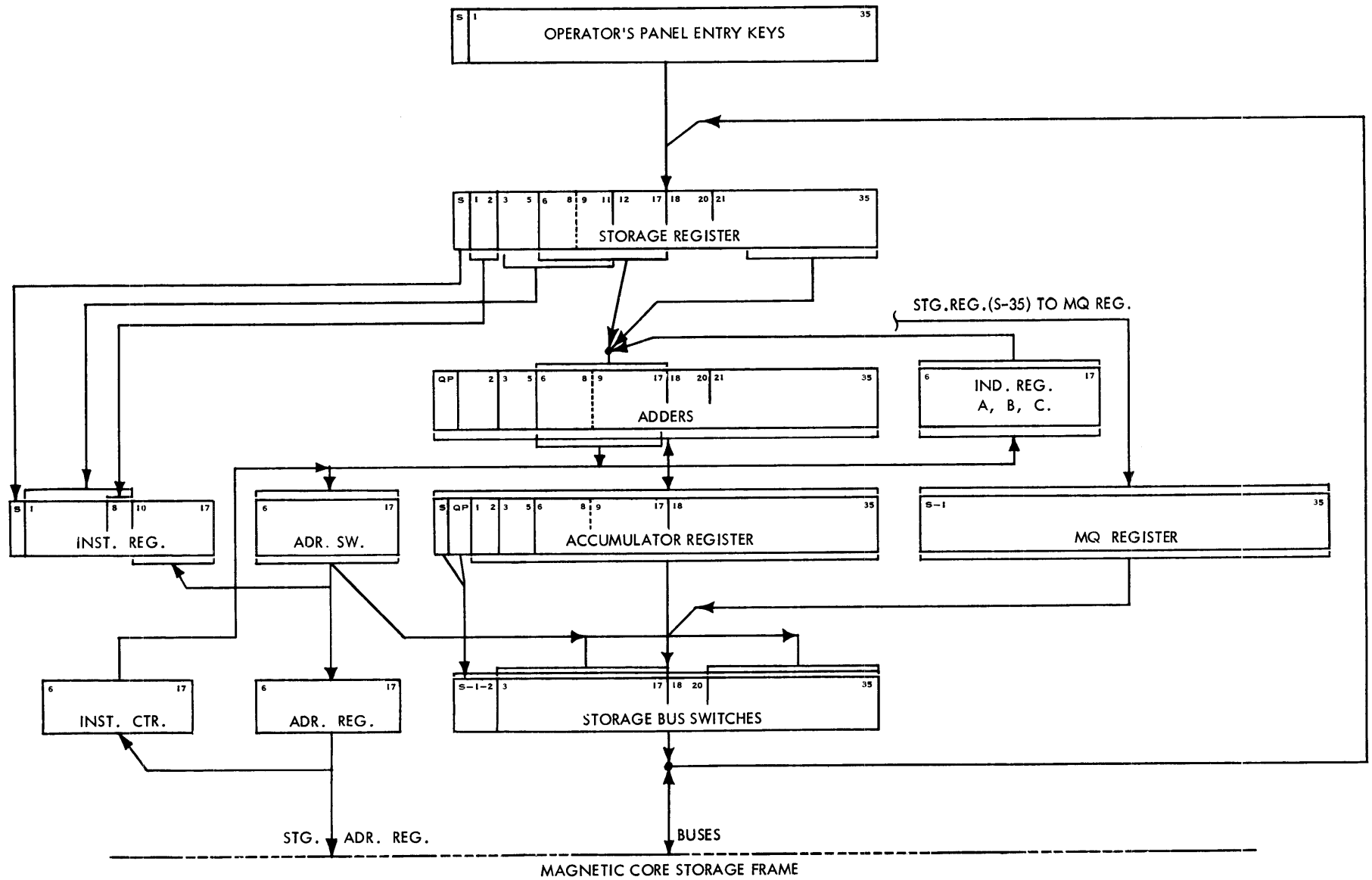


FIGURE 61-2. 704 INFORMATION FLOW

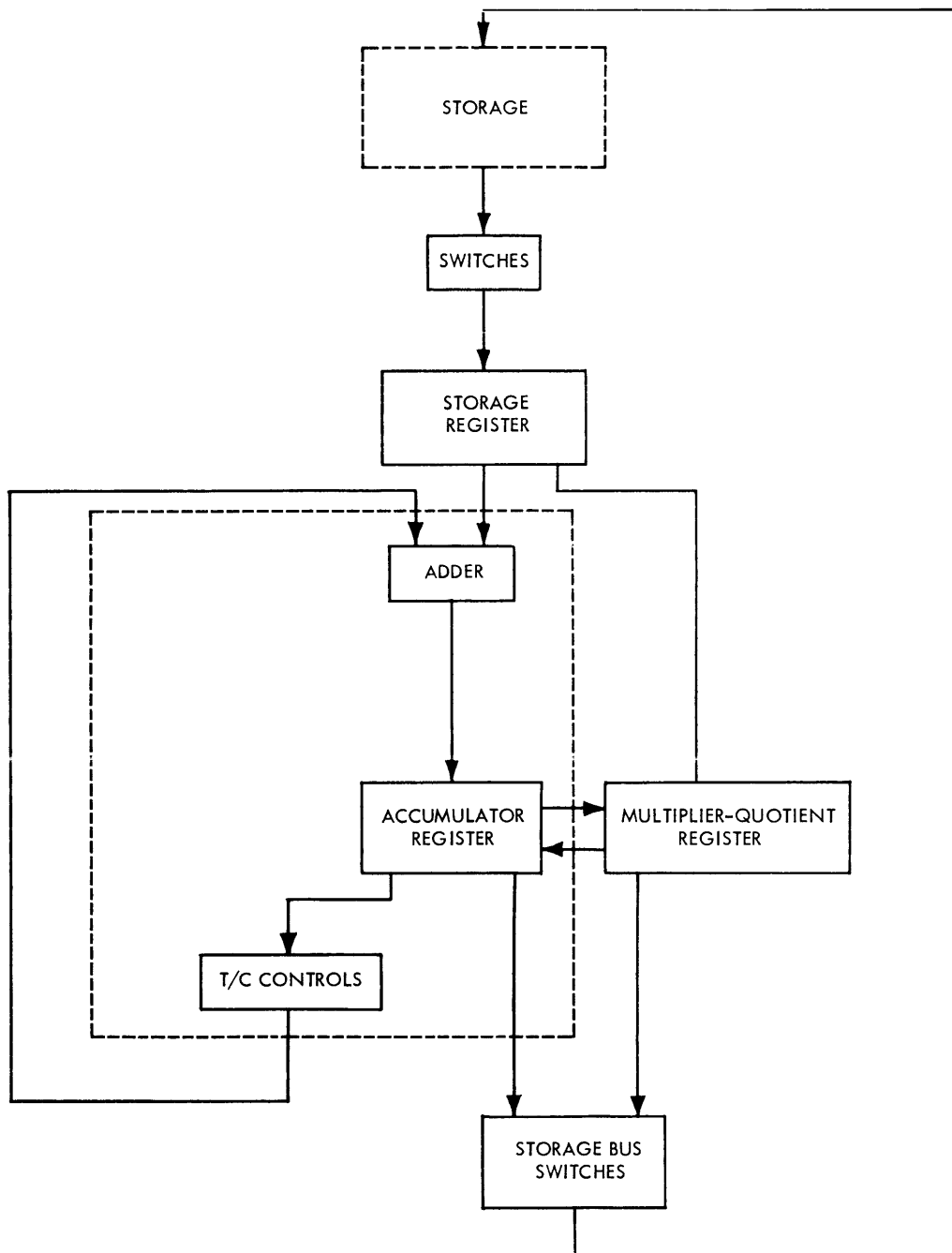


FIGURE 61-3. INFORMATION PROCESSING SECTION FLOW DIAGRAM

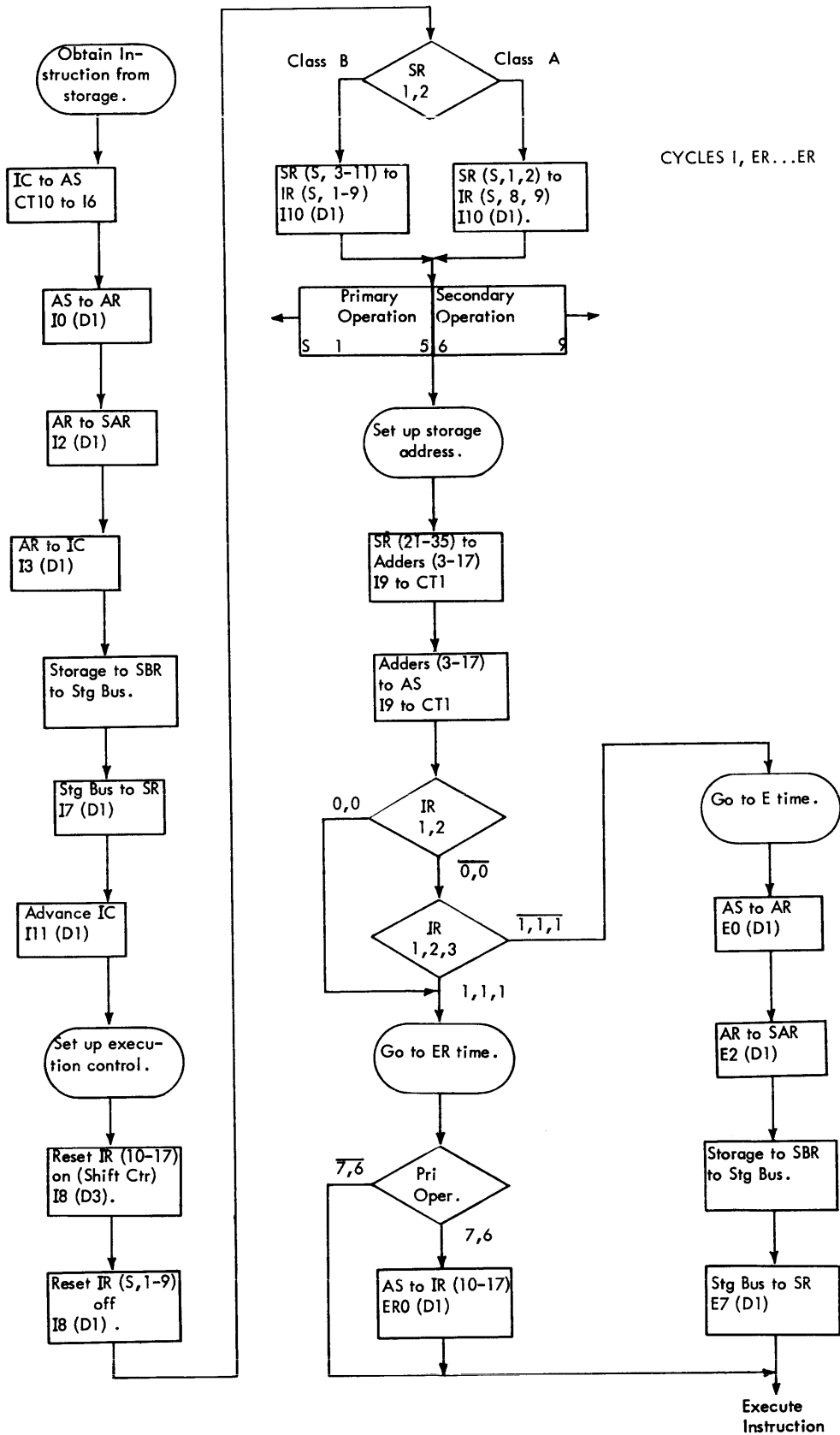


FIGURE 62-1. 704 I CYCLE DATA FLOW

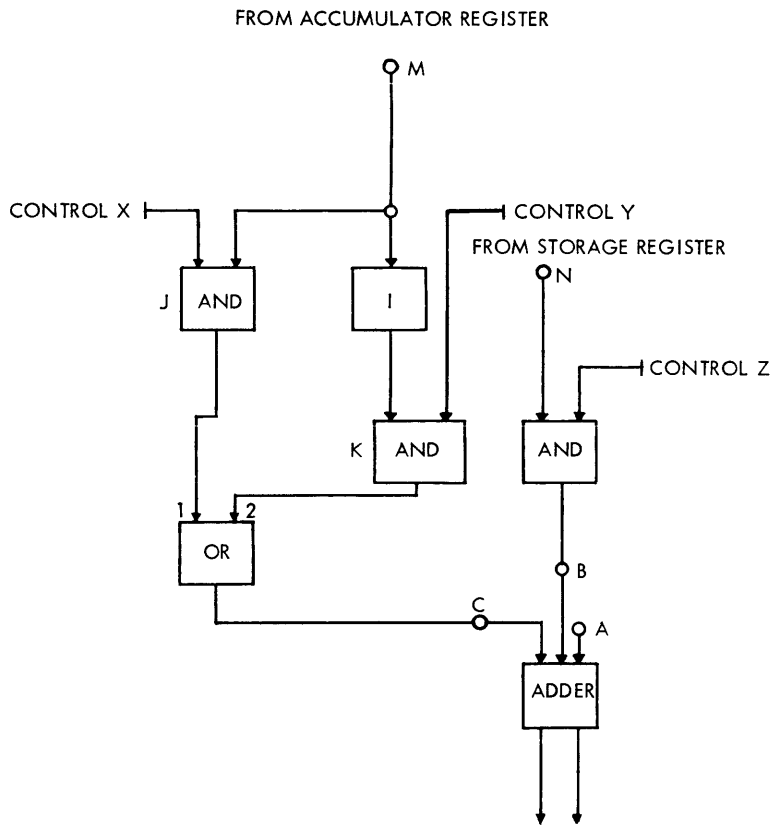


FIGURE 62-2. BASIC DIAGRAM OF TRUE/COMPLEMENT CIRCUITS

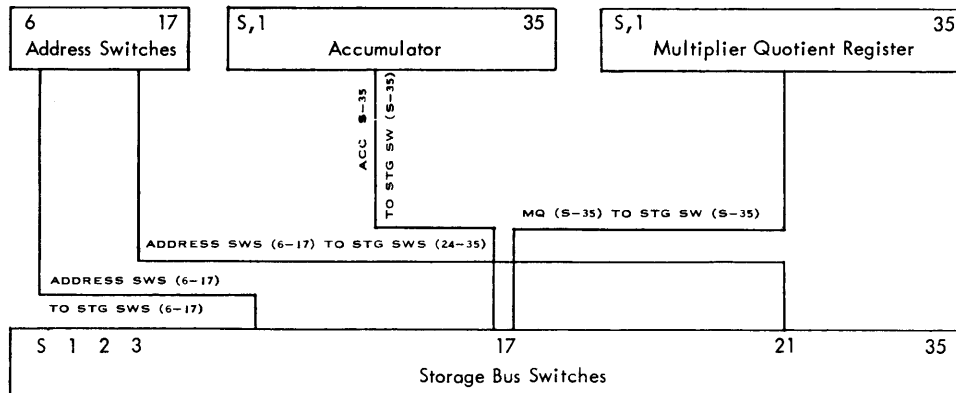


FIGURE 62-3. STORAGE BUS SWITCHING

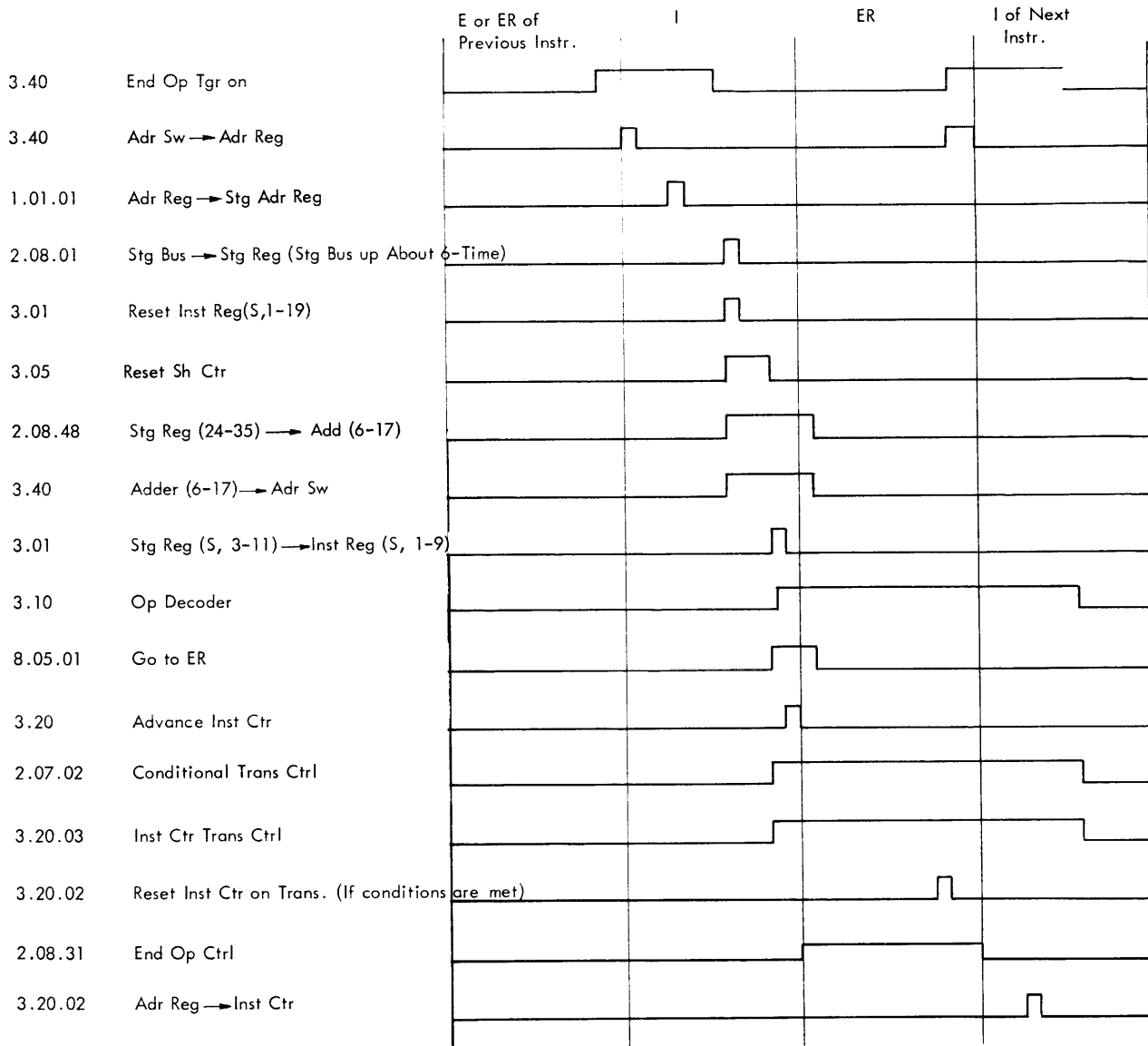


FIGURE 63-1. INDEXABLE TRANSFER INSTRUCTION

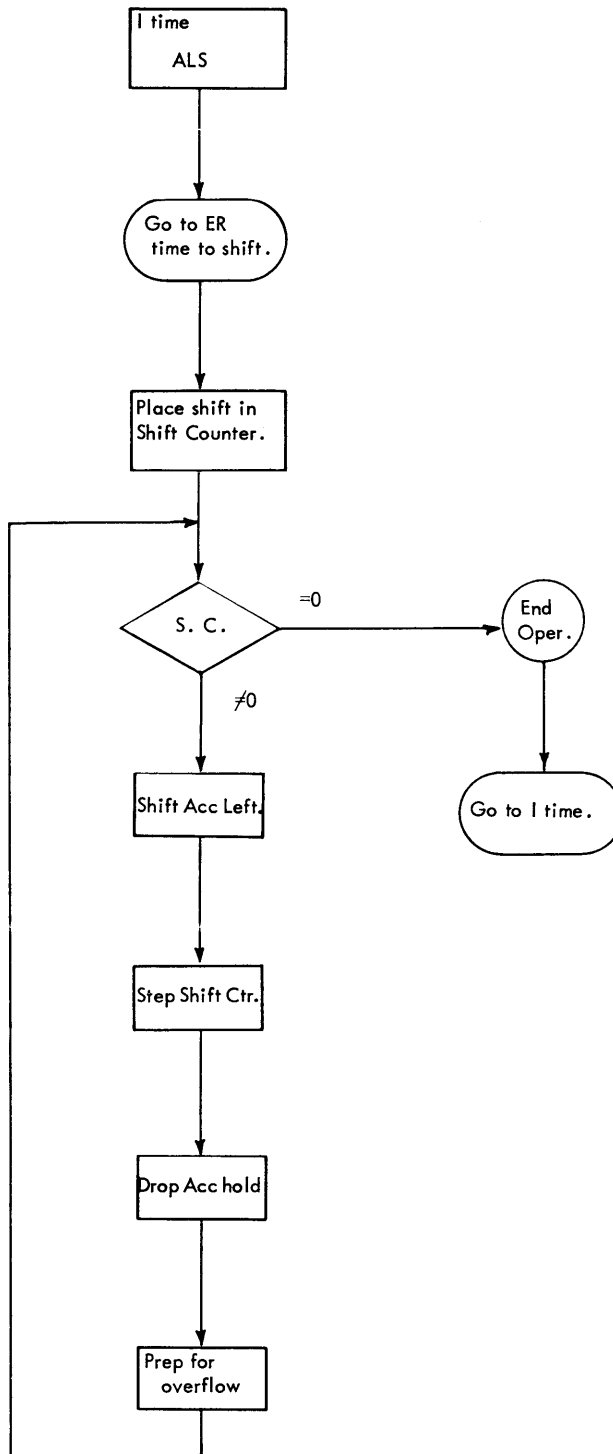


FIGURE 63-2. ACCUMULATION LEFT SHIFT +0767

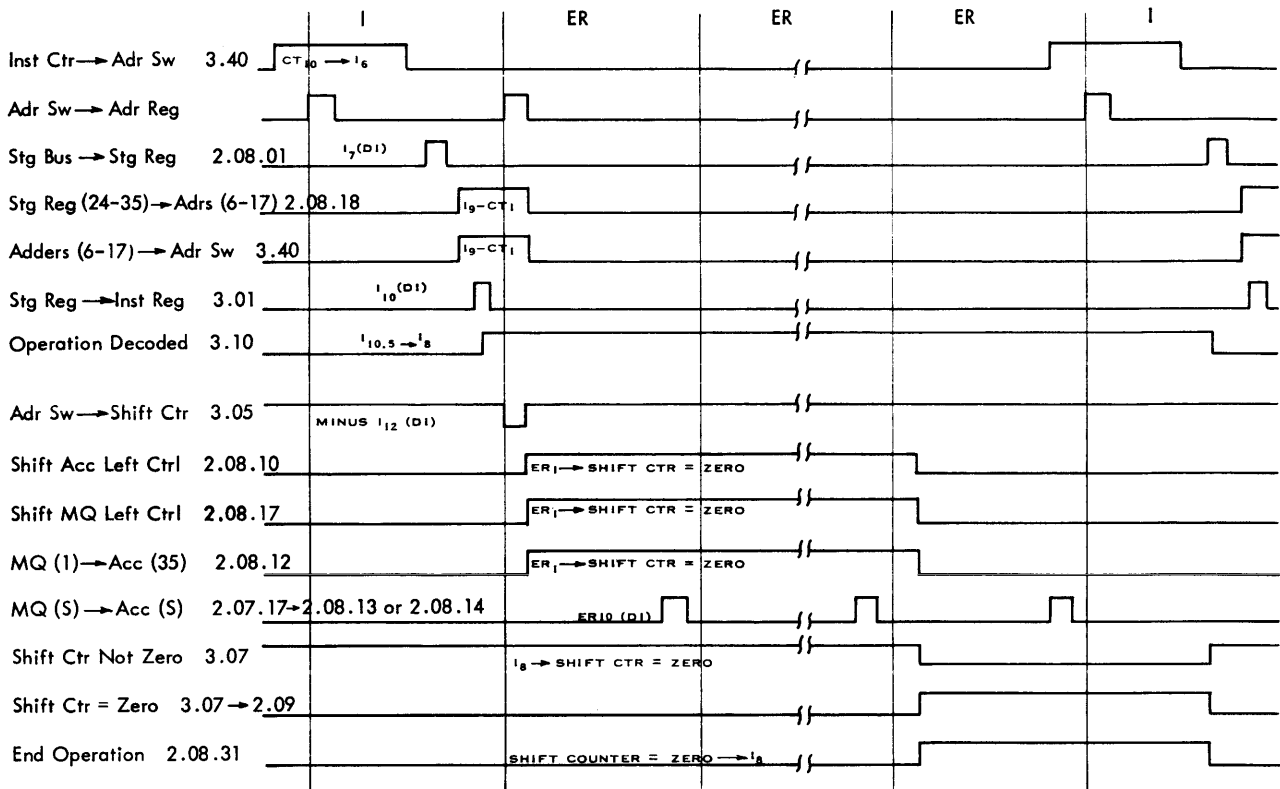


FIGURE 63-3. LONG LEFT SHIFT INSTRUCTION + 0763

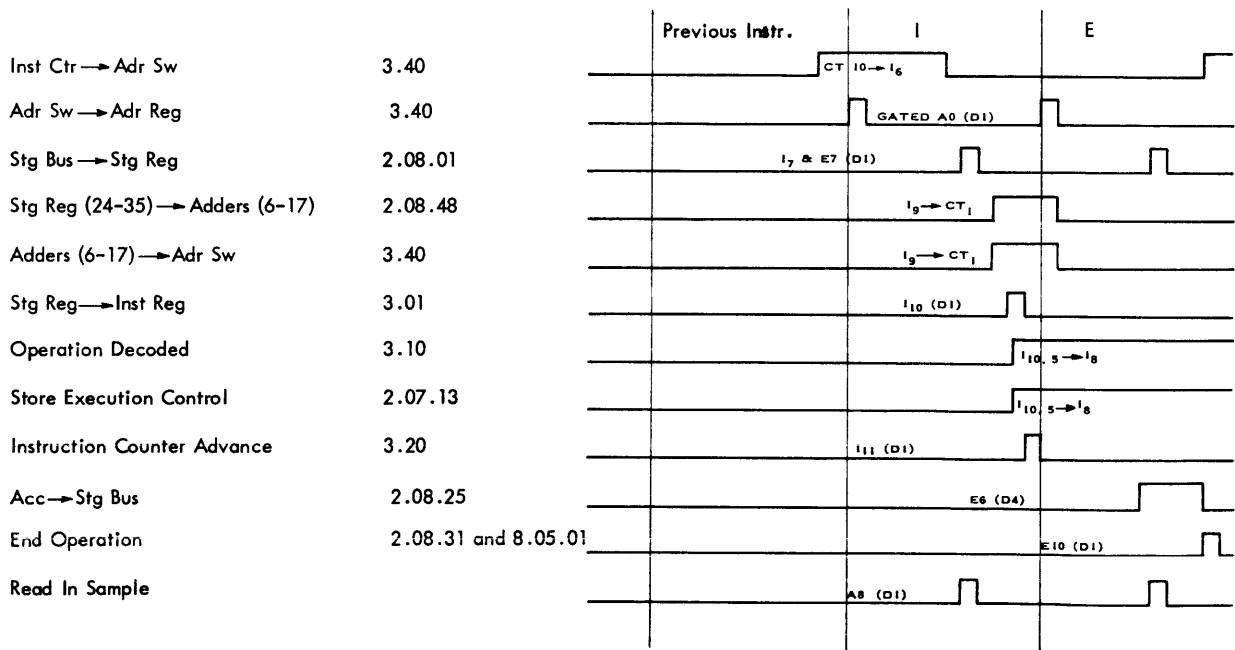
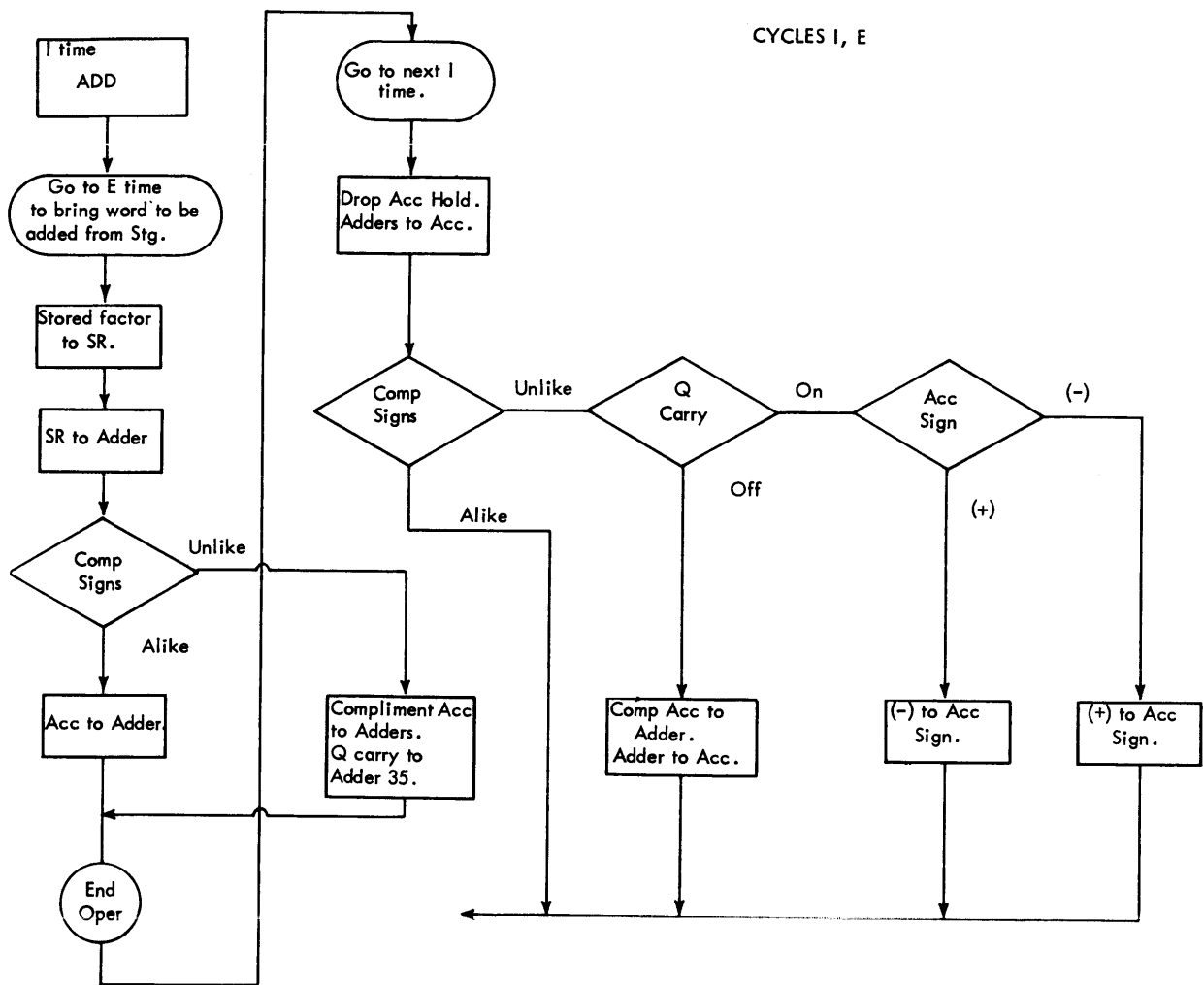


FIGURE 63-4. STORE INSTRUCTION + 0601



- Inst Ctr → Adr Sw 3.40
- Adr Sw → Adr Reg 3.40
- Stg Bus → Stg Reg 2.08.01
- Reset Inst Reg (S, 1-9) 3.01
- Stg Reg (24-35) → Adders (6-17) 2.08.48
- Adders (6-17) → Adr Sw 3.40
- Stg Reg (S, 3-11) → Inst Reg (S, 1-9) 3.01
- Operation Decoded 3.10
- Prepare for Overflow 2.08.39
- Go to E-Time 8.05.01
- Advance the Inst Ctr 3.20
- Stg Reg → Adders 2.08.05
- True Acc → Adders Or Comp Acc → Adders 2.08.06 Or 2.08.07
- Adders - Acc 2.08.23
- Recomp if Nec - Comp Acc → Adders 2.08.07
- Recomp If Nec - Adders → Acc 2.08.23
- End Operation 2.08.31 & 8.05.01
- Adr Reg → Inst Ctr 3.20.02

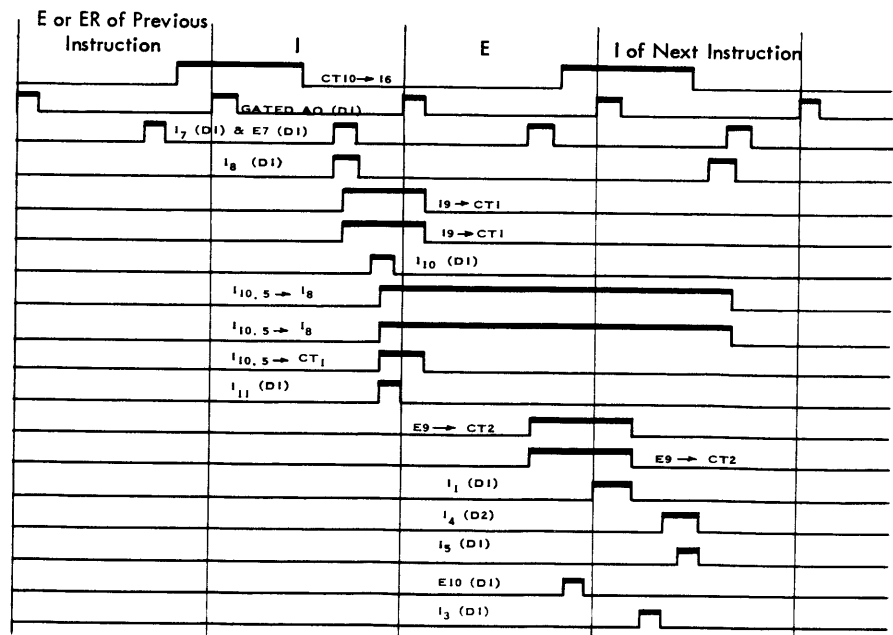


FIGURE 63-5. ADD INSTRUCTION + 0400

CYCLES I, E

ADD +0400
ADM+0401
SUB +0402
SBM - 0400

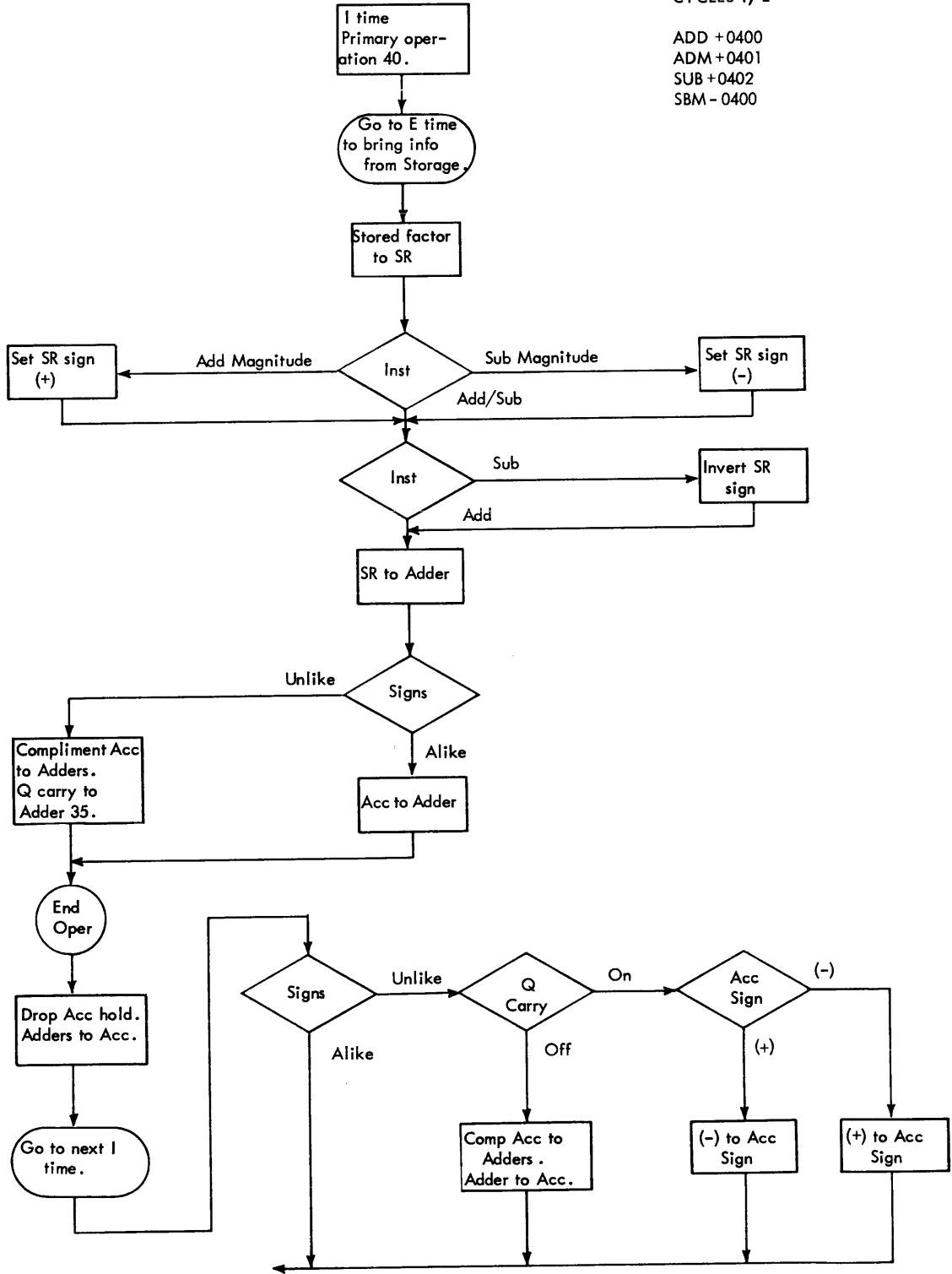


FIGURE 63-6. COMPOSITE OF ADD, SUBTRACT, ADD MAGNITUDE AND SUBTRACT MAGNITUDE

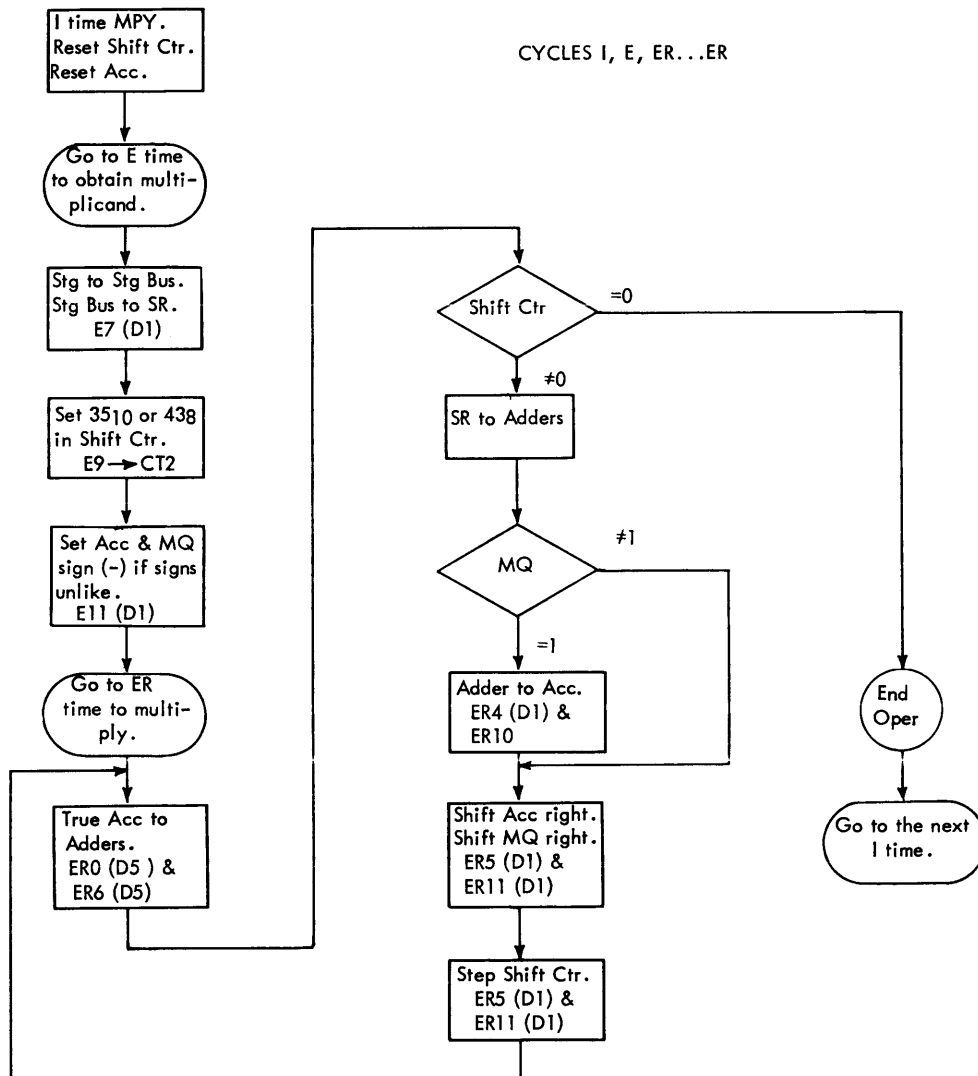


FIGURE 63-7. MULTIPLY INSTRUCTION MPY +0200

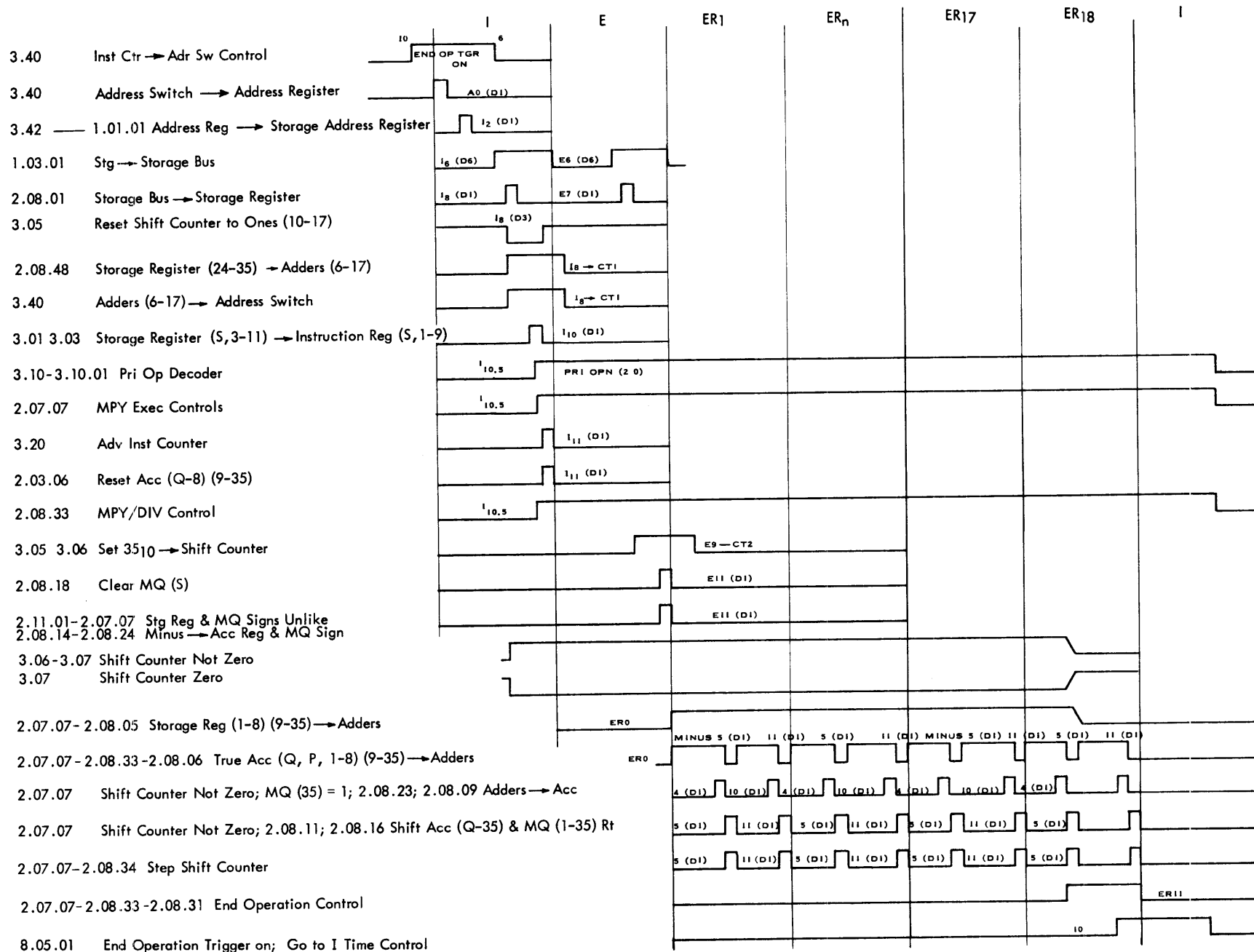


FIGURE 63-8. MULTIPLY INSTRUCTION +0200

$$\frac{0100100010}{01010} = 11101$$

		STG REG	ACCUMULATOR	MQ REG		
		0 1 0 1 0	0 0 0 1 0 0 1	0 0 0 1 0		
		Divisor	Dividend			
		ACC	MQ	Shift CTR		
E Time		0 0 0 1 0 0 1 1 1 1 0 1 1 0	0 0 0 1 0 0 0 0 1 0	5	Complement Acc.	
FIRST ER.	ER 4	0 1 0 1 0 1 0 0 0 0 0 0			Check for carry indicating that quotient will fit in MQ register No adder to ACC.	
		1 1 1 0 1 1 0 1 1 0 1 1 0 1	0 0 0 1 0 0 0 1 0 0	4	Accumulator (retaining the complement valve). Shift left	
	ER 5	0 1 0 1 0				
	ER 10 ER 11	1 1 1 0 1 1 1 1 1 0 1 1 1 1	0 0 1 0 0 0 1 0 1 0	3	No carry; successful reduction. Put 1 in MQ (5). Bring adders to ACC. Shift left	
SECOND ER.	ER 4	0 1 0 1 0 1 1 1 1 0 0 1 1 1 1 0 0 1 1	0 1 0 1 0 1 0 1 1 0	2	No carry; put 1 in MQ (5). Bring adders to ACC. Shift left	
	ER 5	0 1 0 1 0				
	ER 10 ER 11	1 1 1 1 1 0 1 1 1 1 1 0 1 0	1 0 1 1 1 0 1 1 1 0	1	No carry; put 1 in MQ (5). Bring adders to ACC. Shift left	
	LAST ER.	ER 4	0 1 0 1 0 0 0 0 0 1 0 0			Carry overdraw; no 1 to MQ (5). No adders to ACC.
ER 5		1 1 1 1 0 1 0 1 1 1 0 1 0 1	0 1 1 1 0 1 1 1 0 0	0	Shift left (shift ctr 0; no more shifting).	
ER 10		0 1 0 1 0 1 1 1 1 1 1 1	1 1 1 0 0		No carry; put 1 in MQ (5). Bring adders to ACC.	
NEXT	15	0 0 0 0 0 0 0 Remainder	1 1 1 0 1 Quotient		Recomp. ACC.	

Note: (a) 5-bit registers
(b) Shift ctr. set to 5

FIGURE 63-9. EXAMPLE OF DIVIDE (WITH A SIMULATED 5-BIT MACHINE)

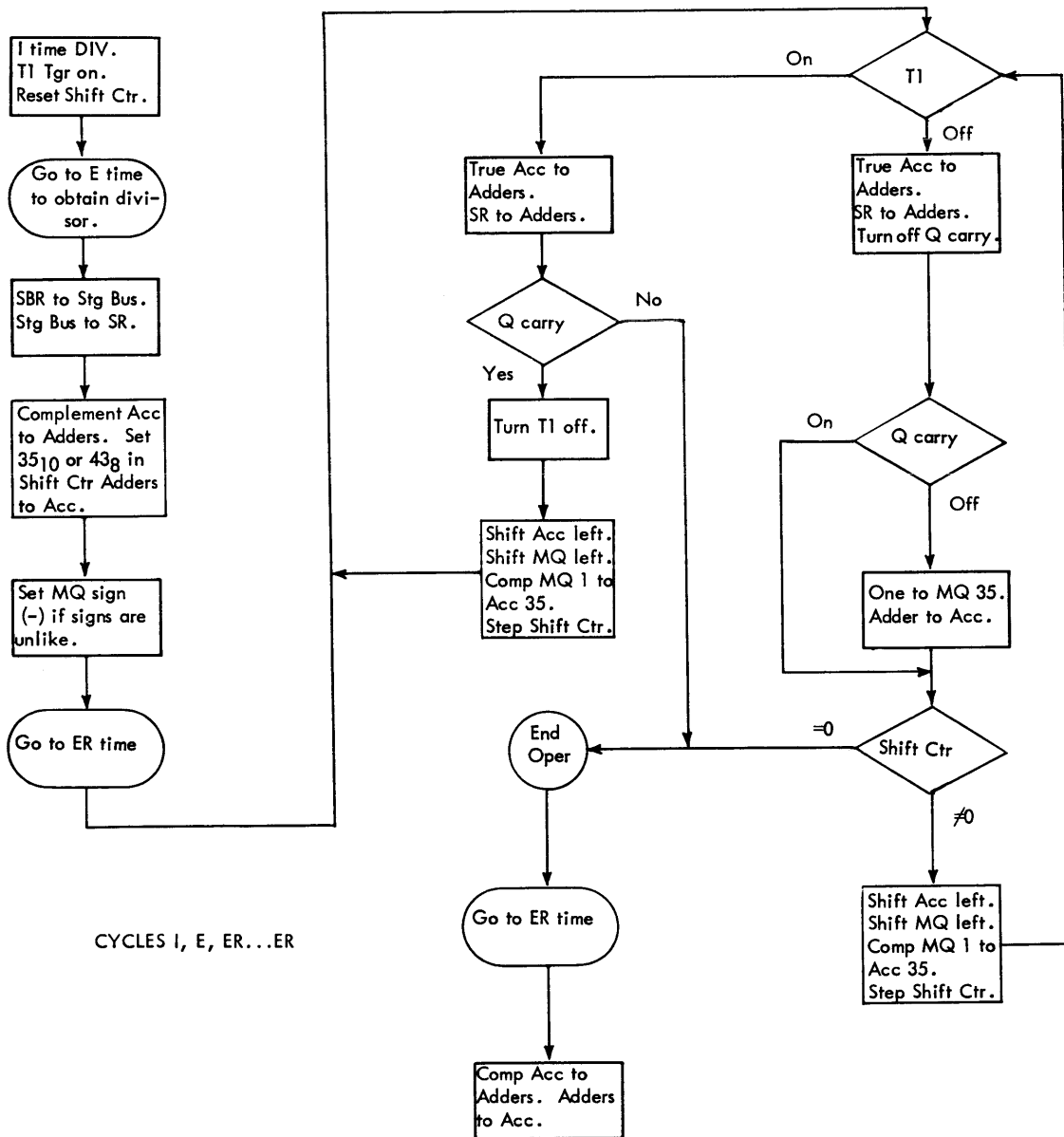


FIGURE 63-10. DIVIDE INSTRUCTION + 0220

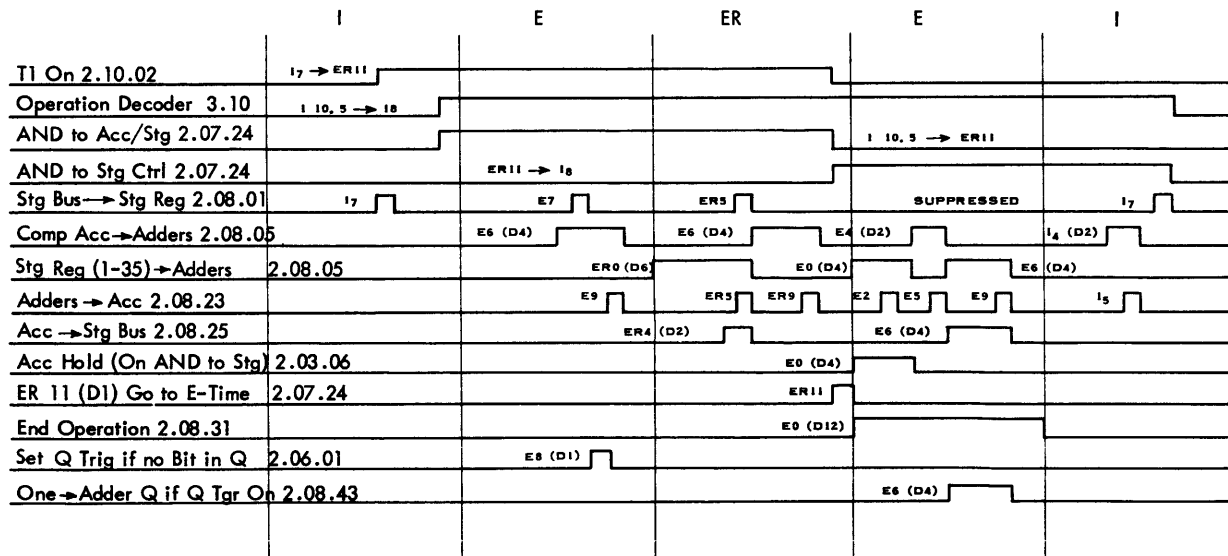
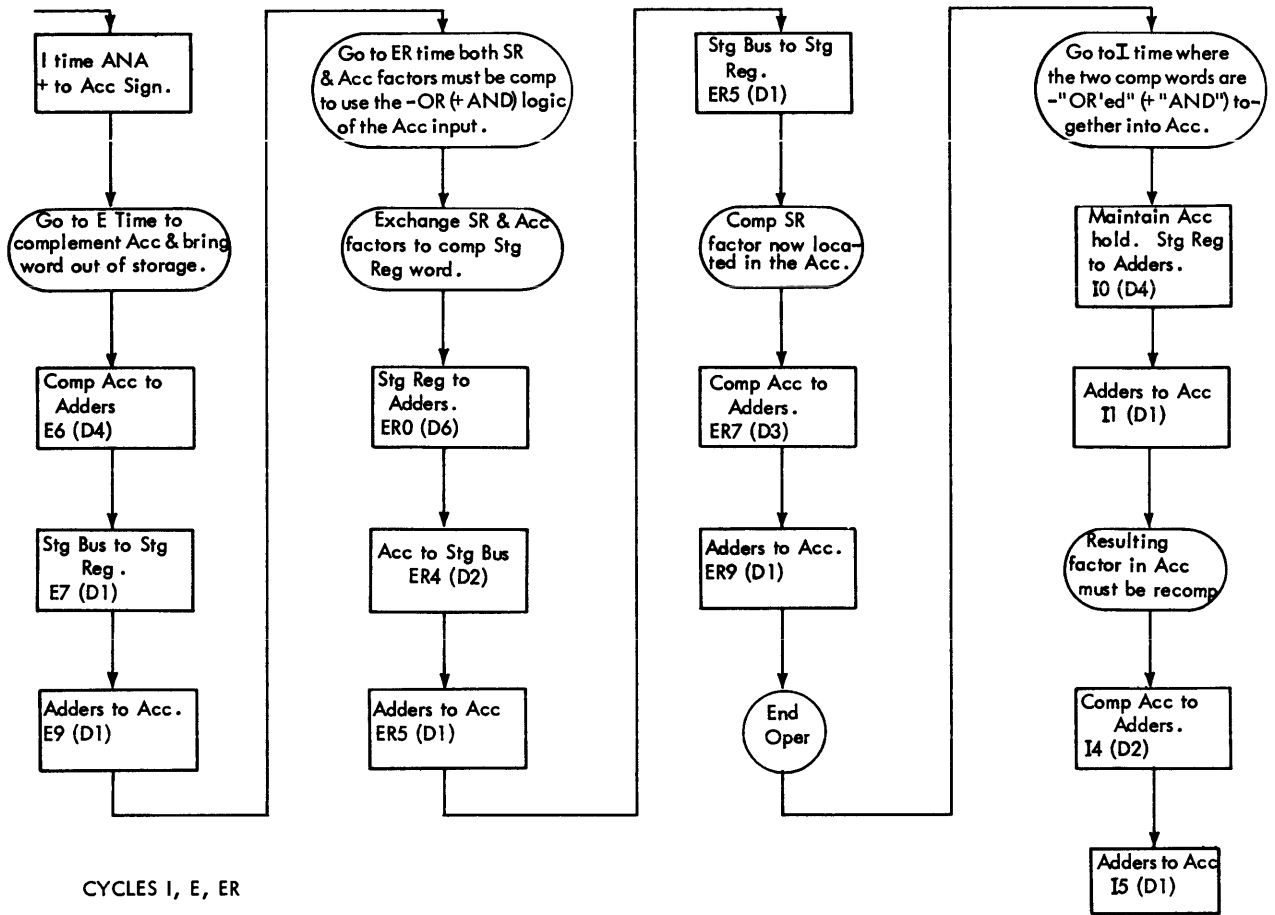


FIGURE 63-12. AND TO ACCUMULATOR INSTRUCTION ANA-0320

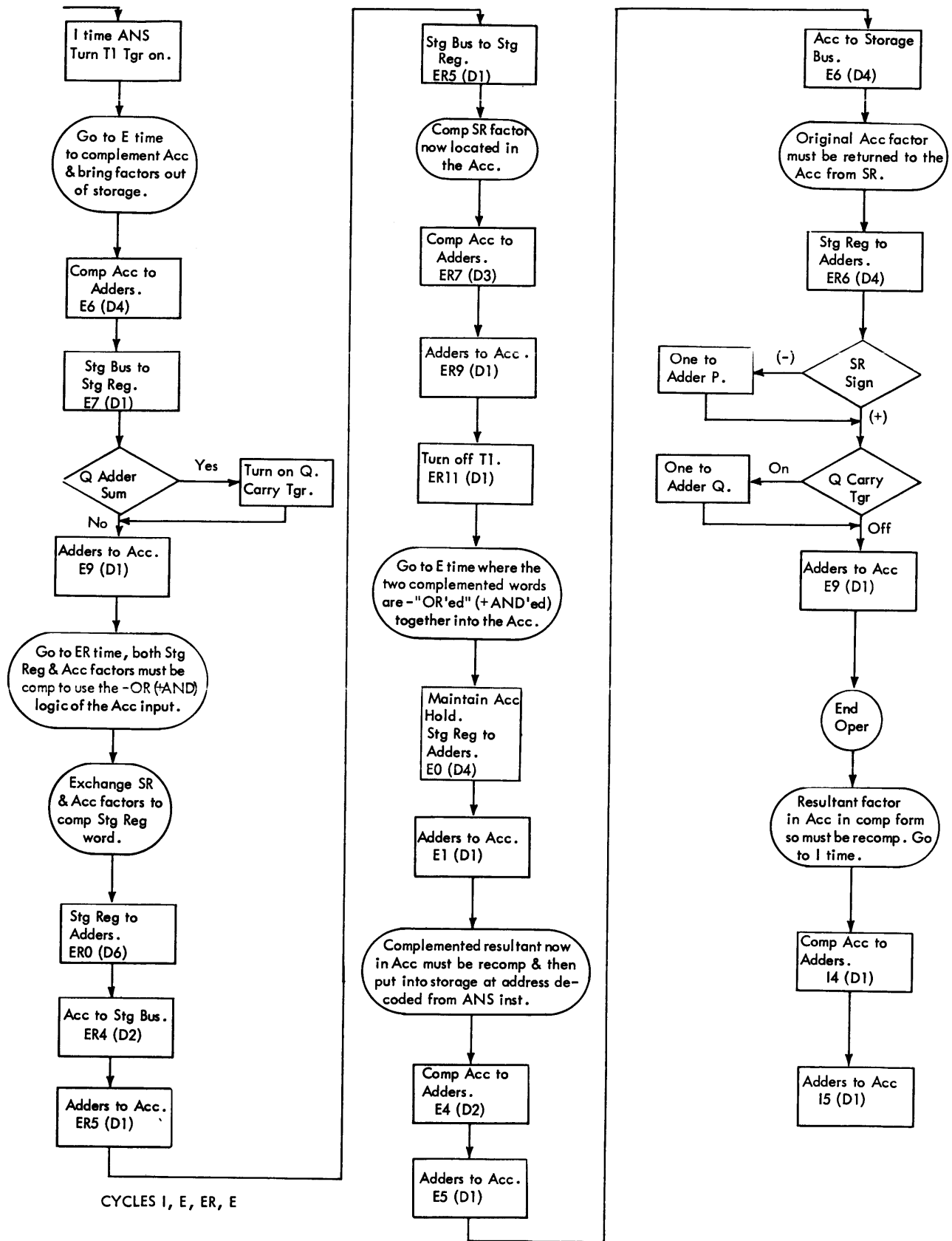


FIGURE 63-13. AND TO STORAGE INSTRUCTION + 0320

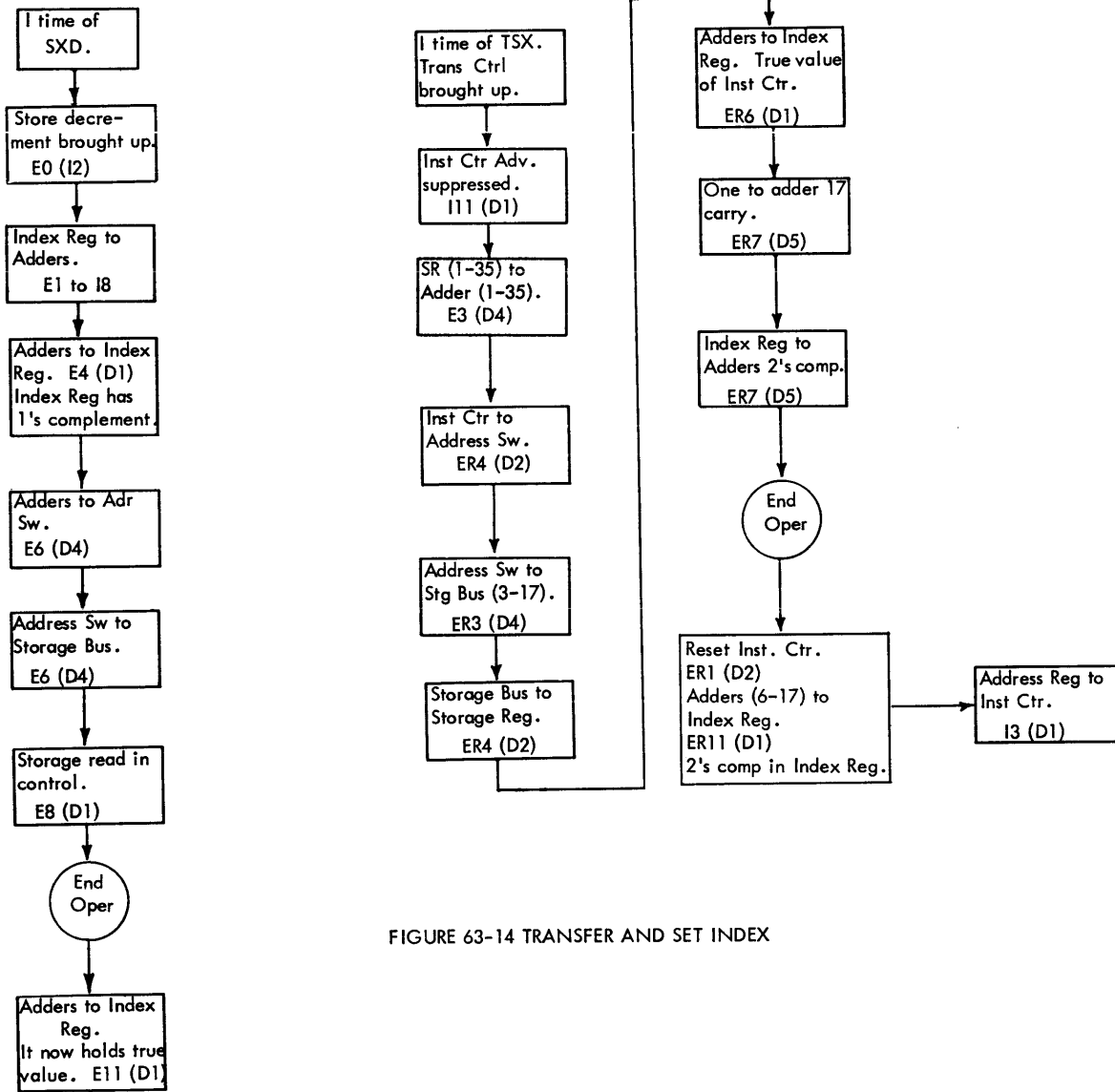


FIGURE 63-14 TRANSFER AND SET INDEX

Operation Decoded 3.10
 SxD Command 2.07.57
 XR → Adders 2.08.49
 Adders → XR 2.08.53
 Adders → Adr Sw 3.40
 Adr Sw → Stg Bus (3-17) 2.08.28
 Store Decr Ctrl 1.04.05
 End of Ctrl 2.08.31

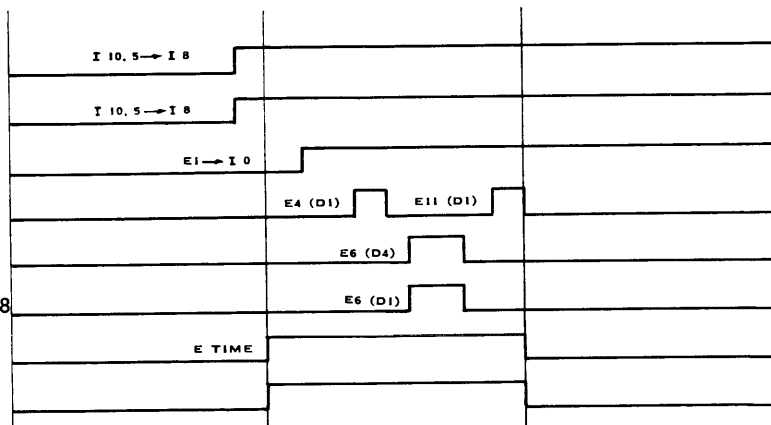


FIGURE 63-15. STORE INDEX IN DECREMENT INSTRUCTION

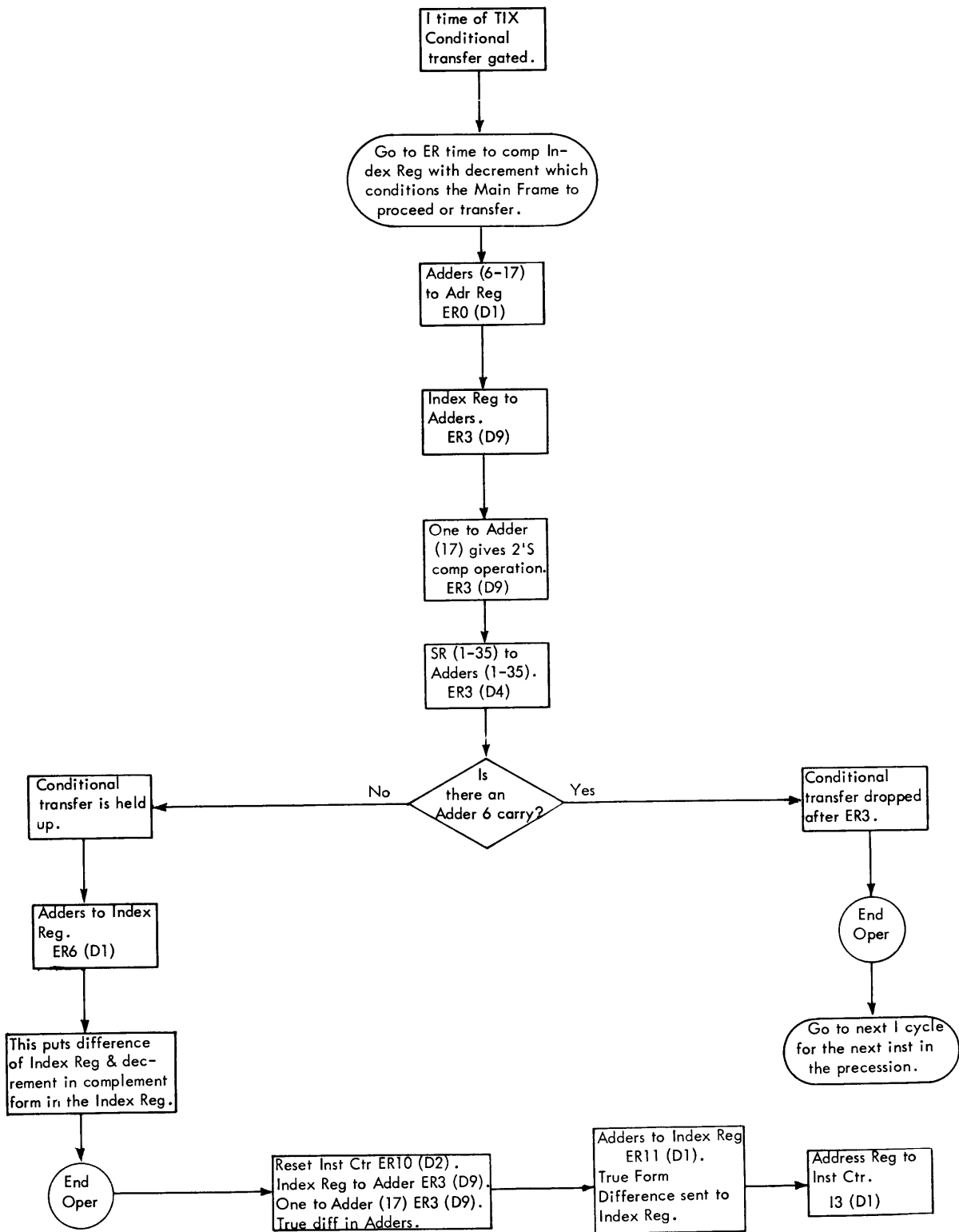


FIGURE 63-16. TRANSFER ON INDEX INSTRUCTION

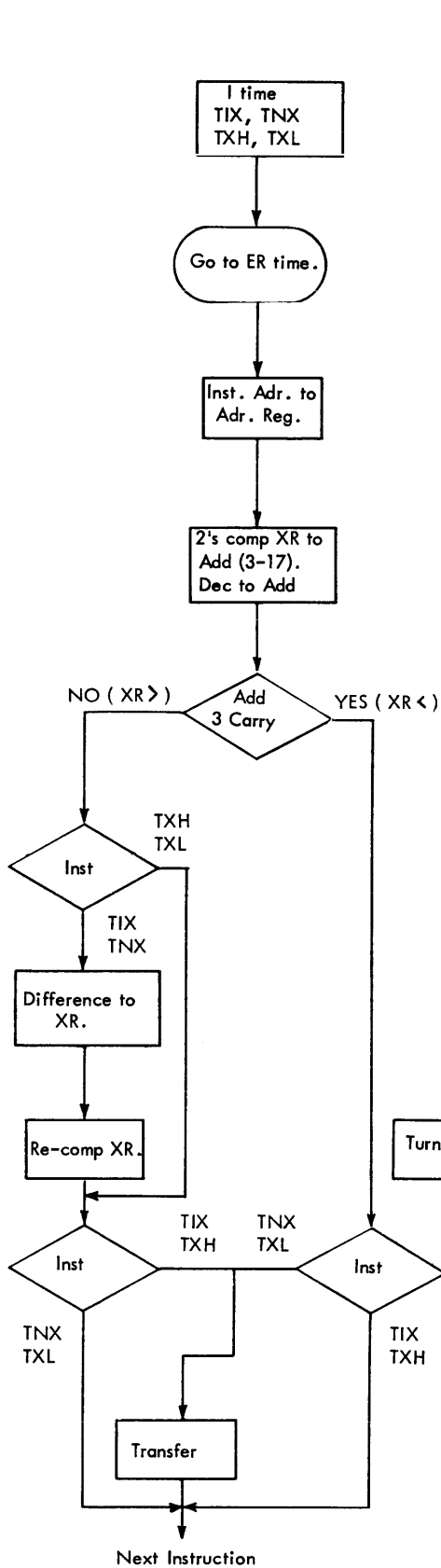


FIGURE 63-17. TIX, TNX, TXH AND TXL

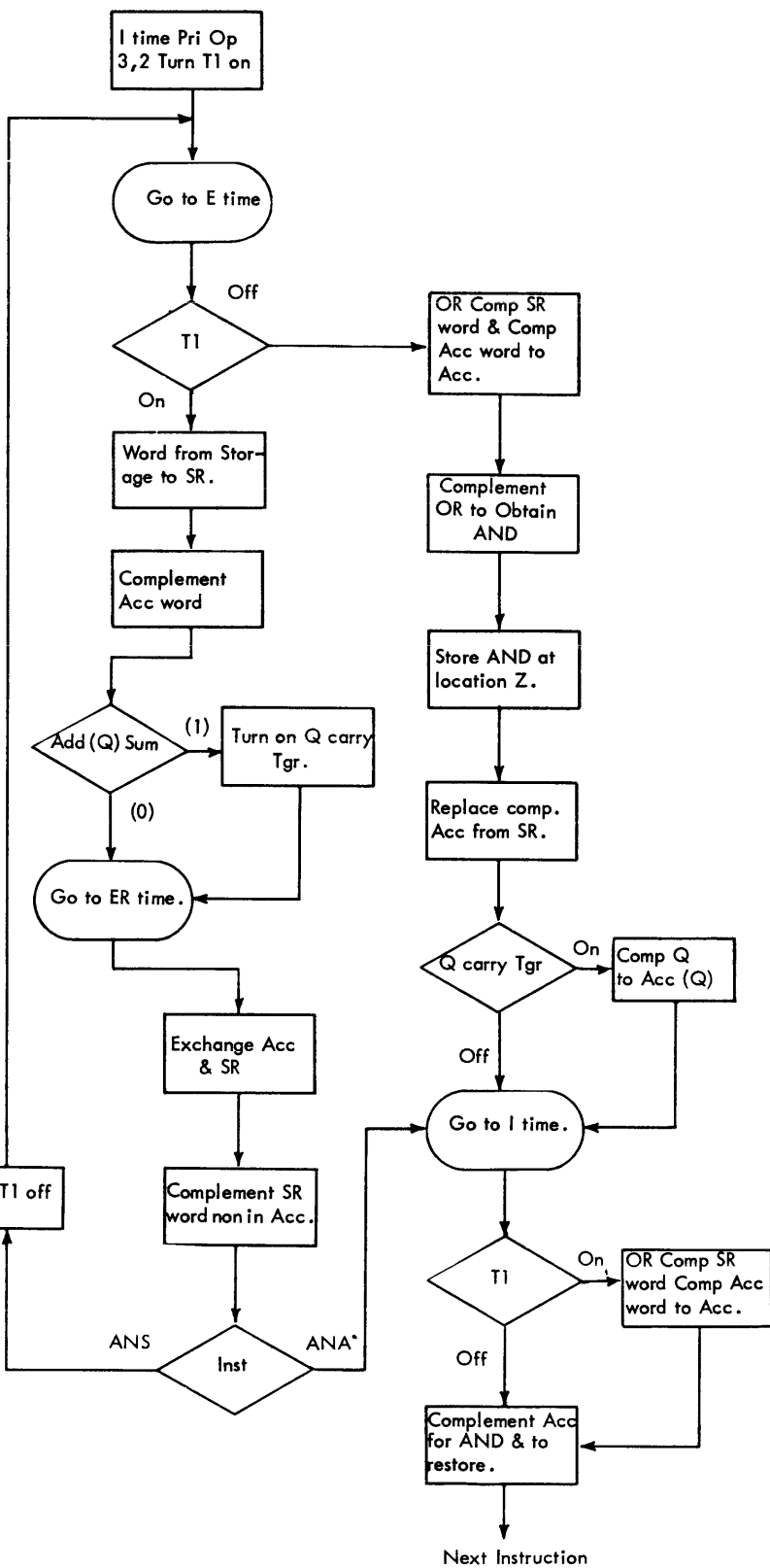


FIGURE 63-18. ANS, ANA*

- 3.10.01 Pri Op Decoder
- 3.10.06 Minus on Transfer (T.M)
- 3.10.06 Minus on go to E time

- 3.10.06 Transfer Control
- 3.40 Adder → Adr Sw (SUP)
- 3.40 Gated Minus A0 (D1)
- 8.05.01 Go to E Time Control
- 3.20 Adv Inst Ctr (SUP)
- 1.01.01 Adr Reg → Stg Adr Reg
- 3.40 Inst Ctr → Adr Sw Control
- 2.08.28 Adr Sw → Stg Bus
- 8.05.01 Go to ER Time Control
- 8.05.03 Set Cycle Timer
- 2.08.31 Stg End Opn
- 2.08.31 End Opn Control
- 3.20 Adv Inst Ctr (Unseccessful Transfer)
- 3.20.03 Inst Ctr Tr Control (Successfull Tr Only)
- 3.20.02 Reset Inst Ctr On Tr
- 8.05.01 End Opn Tgr on - Go to I Time
- 3.40 Inst Ctr → Adr Sw
- 3.40 Gated A0 (D1) Adr Sw → Adr Reg Blocked by Minus on Inst Ctr Tr Ctrl
- 3.42 One → Adr Reg 17

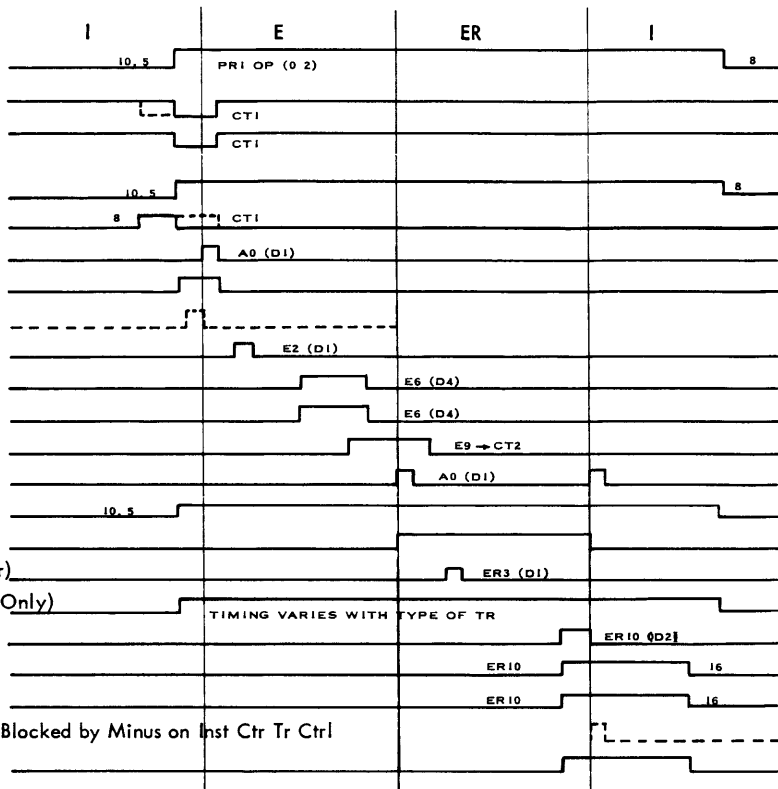


FIGURE 63-19 TRANSFER IN TRAP MODE

Condition	Sign		Skip		2.07.27
	Acc	SR	ER4	ER9	CQT
SR > Acc	+	+	x	x	And S
	-	-	x	x	And R
	-	+	x	x	And Q
SR = Acc	+	+	x		And R
	-	-		x	And S

If SR < Acc, Normal I 11 (D1) Advance

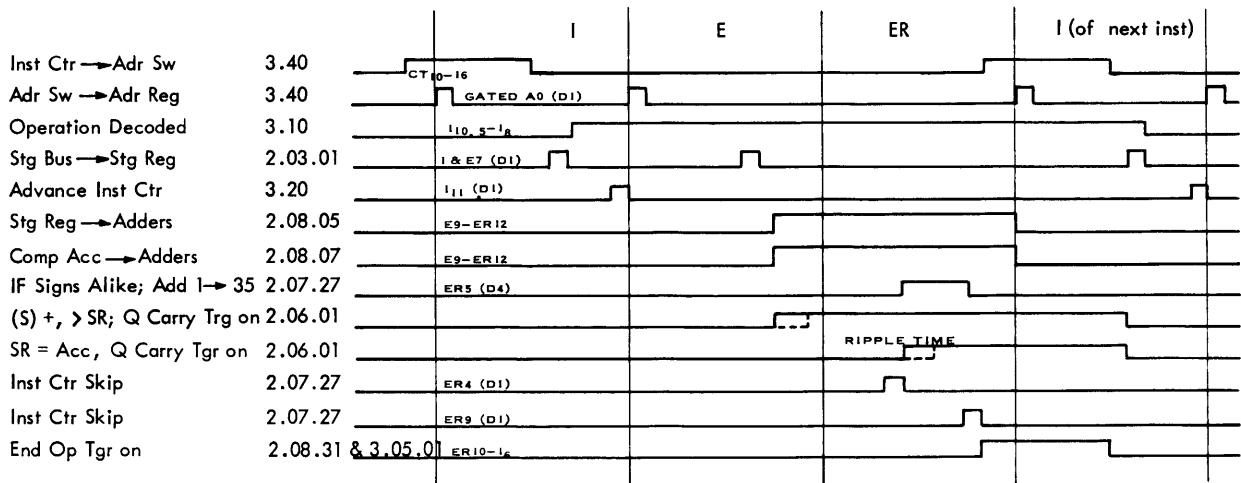


FIGURE 63-20. TRANSFER IN TRAP MODE

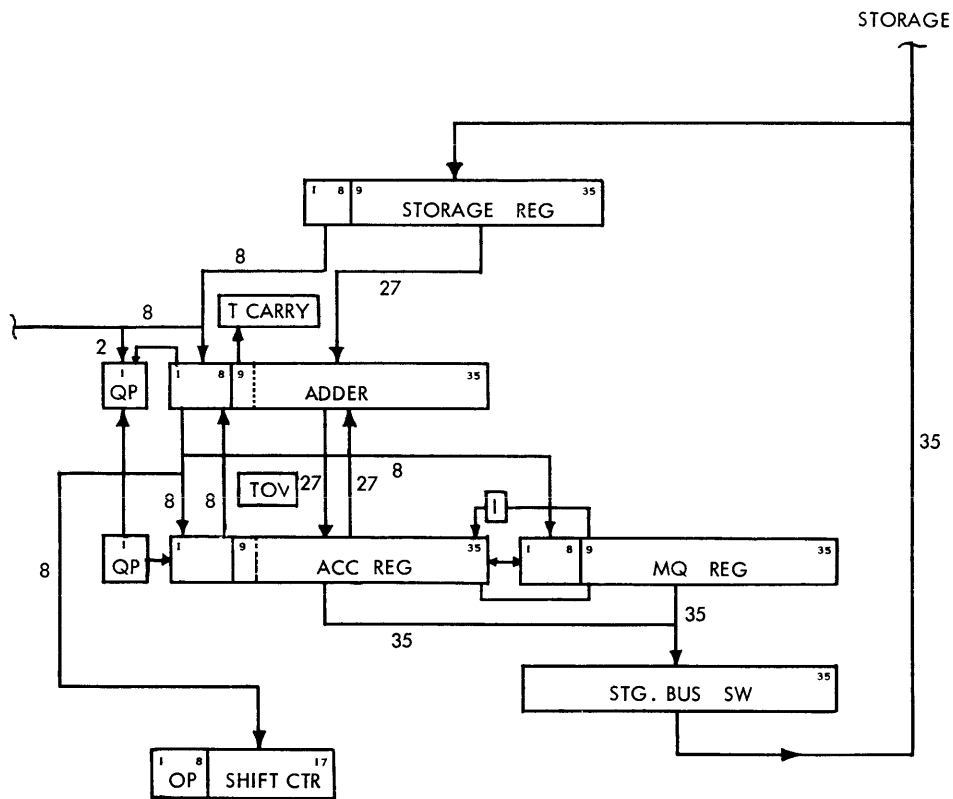


FIGURE 63-21. FLOATING POINT INFORMATION FLOW

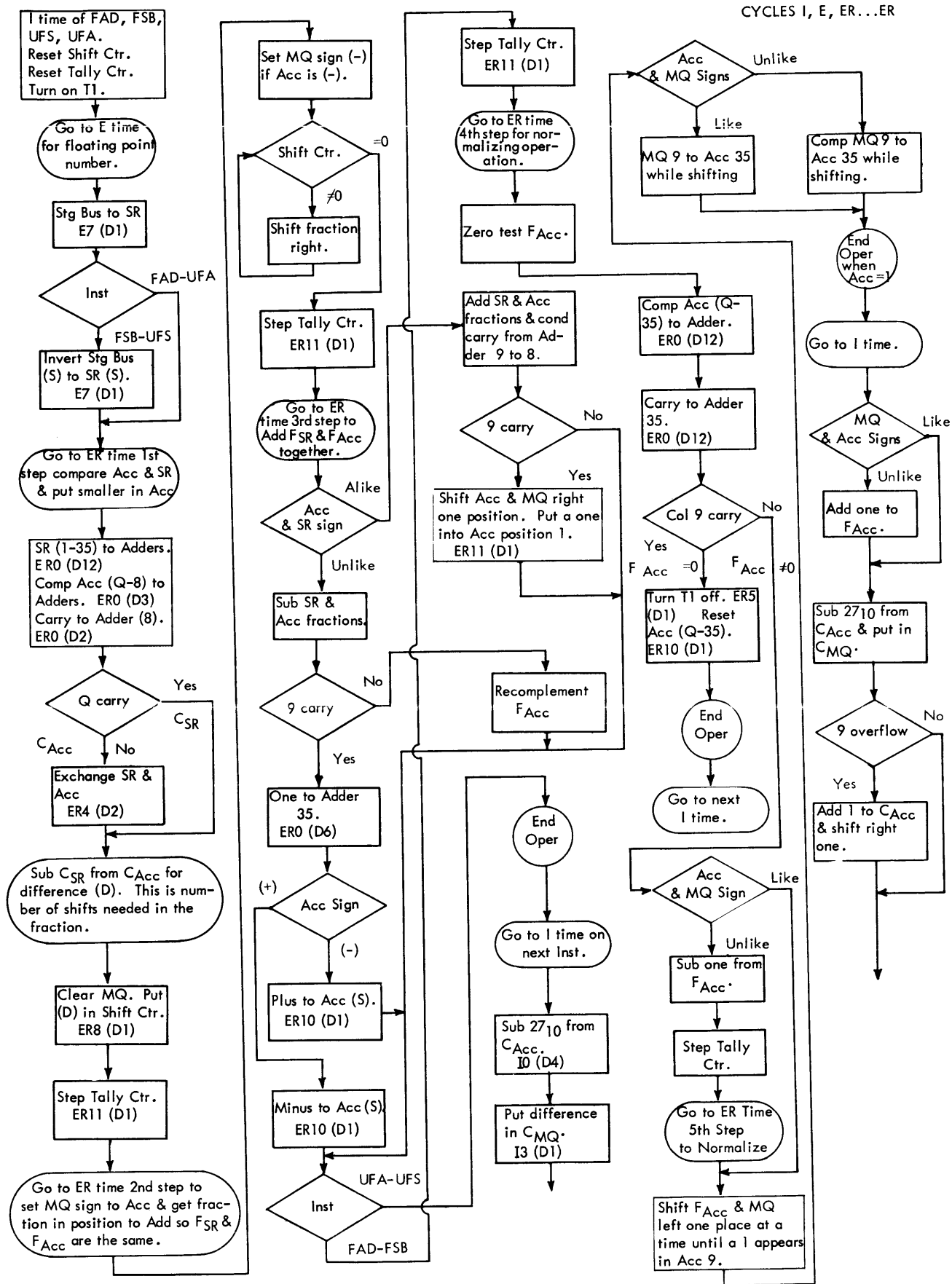


FIGURE 63-22. FLOATING POINT ADD AND FLOATING POINT SUBTRACT INSTRUCTION

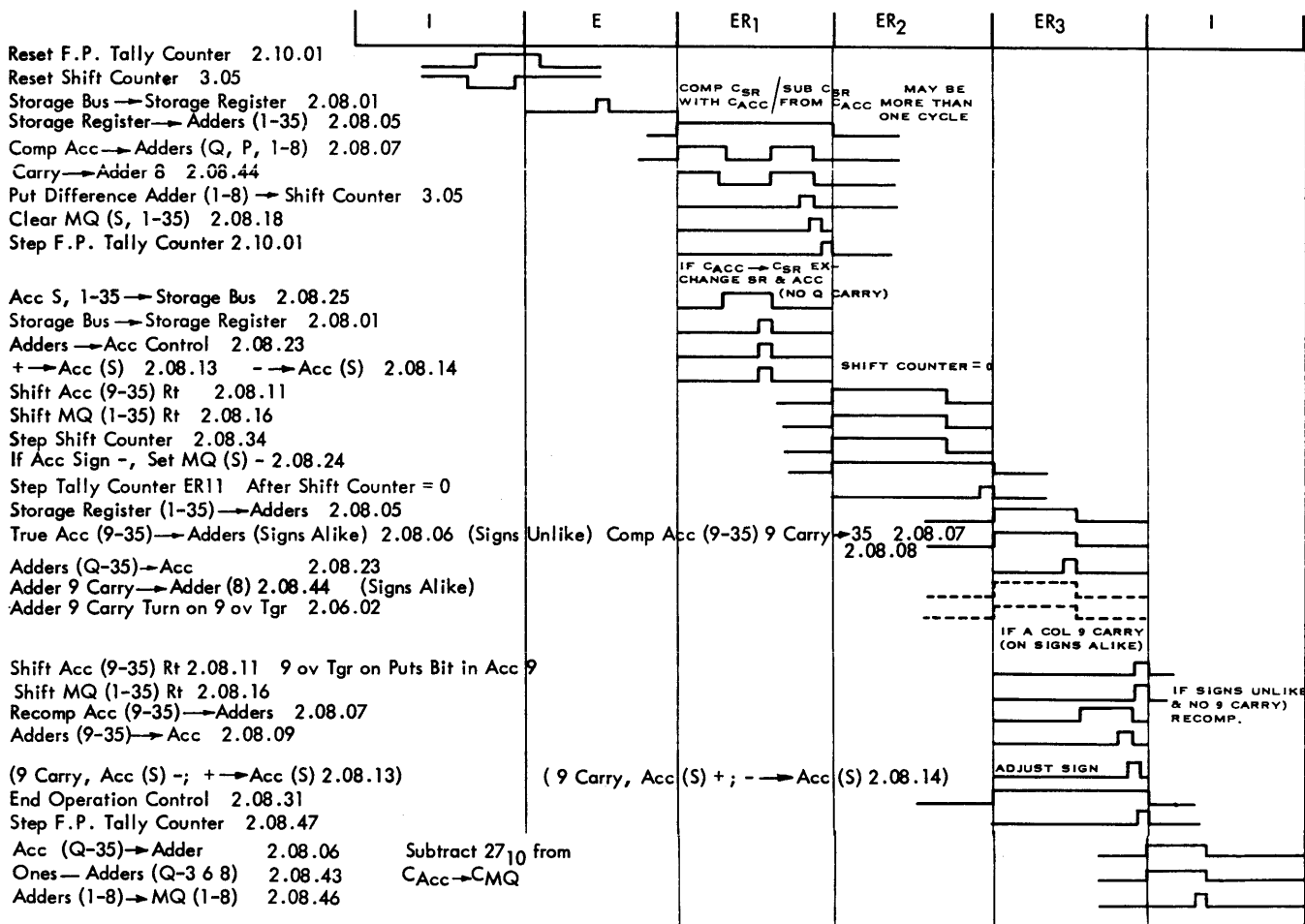


FIGURE 63-23. UNNORMALIZED FLOATING ADD INSTRUCTION = 0300

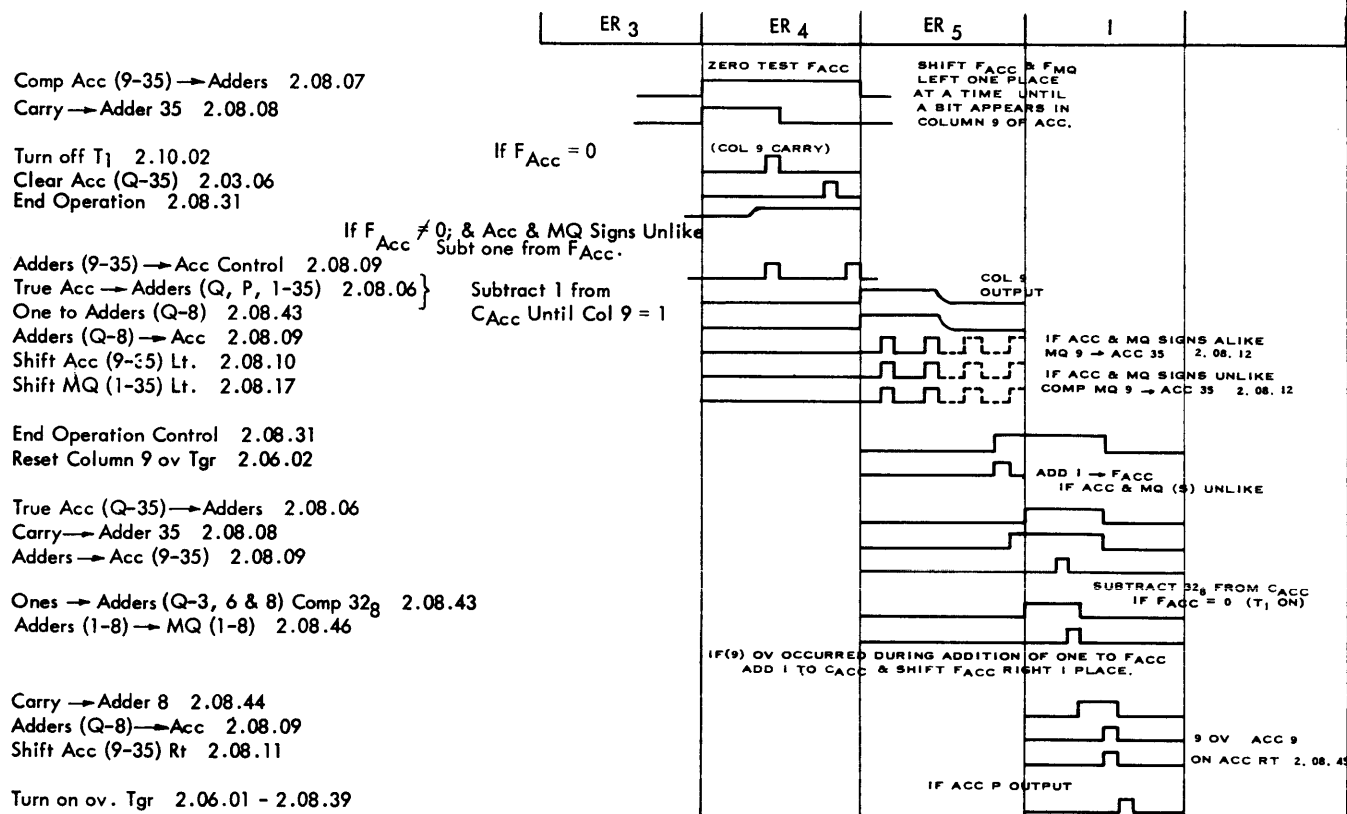


FIGURE 63-24. FLOATING POINT ADD INSTRUCTION + 0300

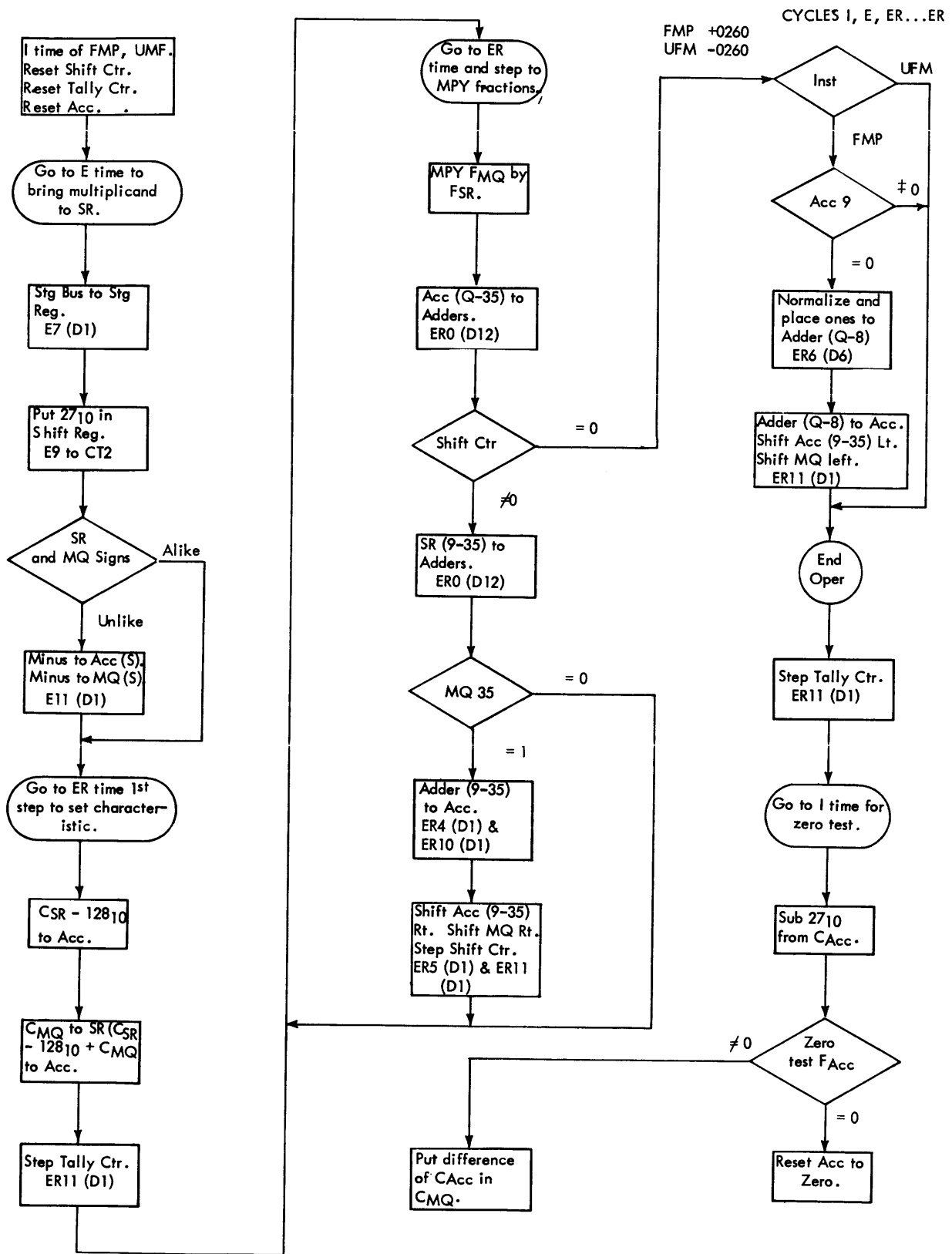


FIGURE 63-25. FLOATING POINT MULTIPLY INSTRUCTION

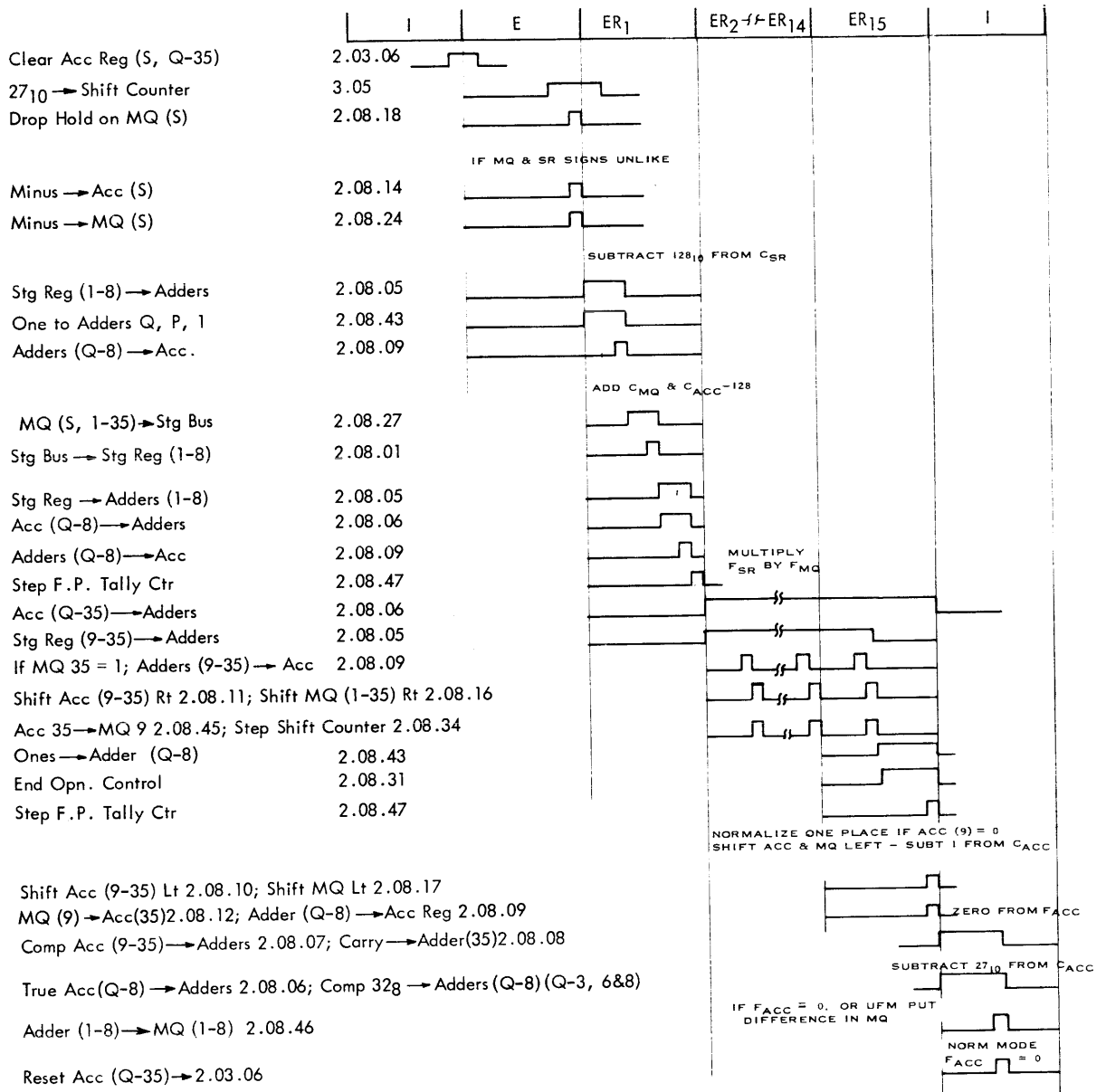


FIGURE 63-26. FLOATING POINT MULTIPLY INSTRUCTION + 0260

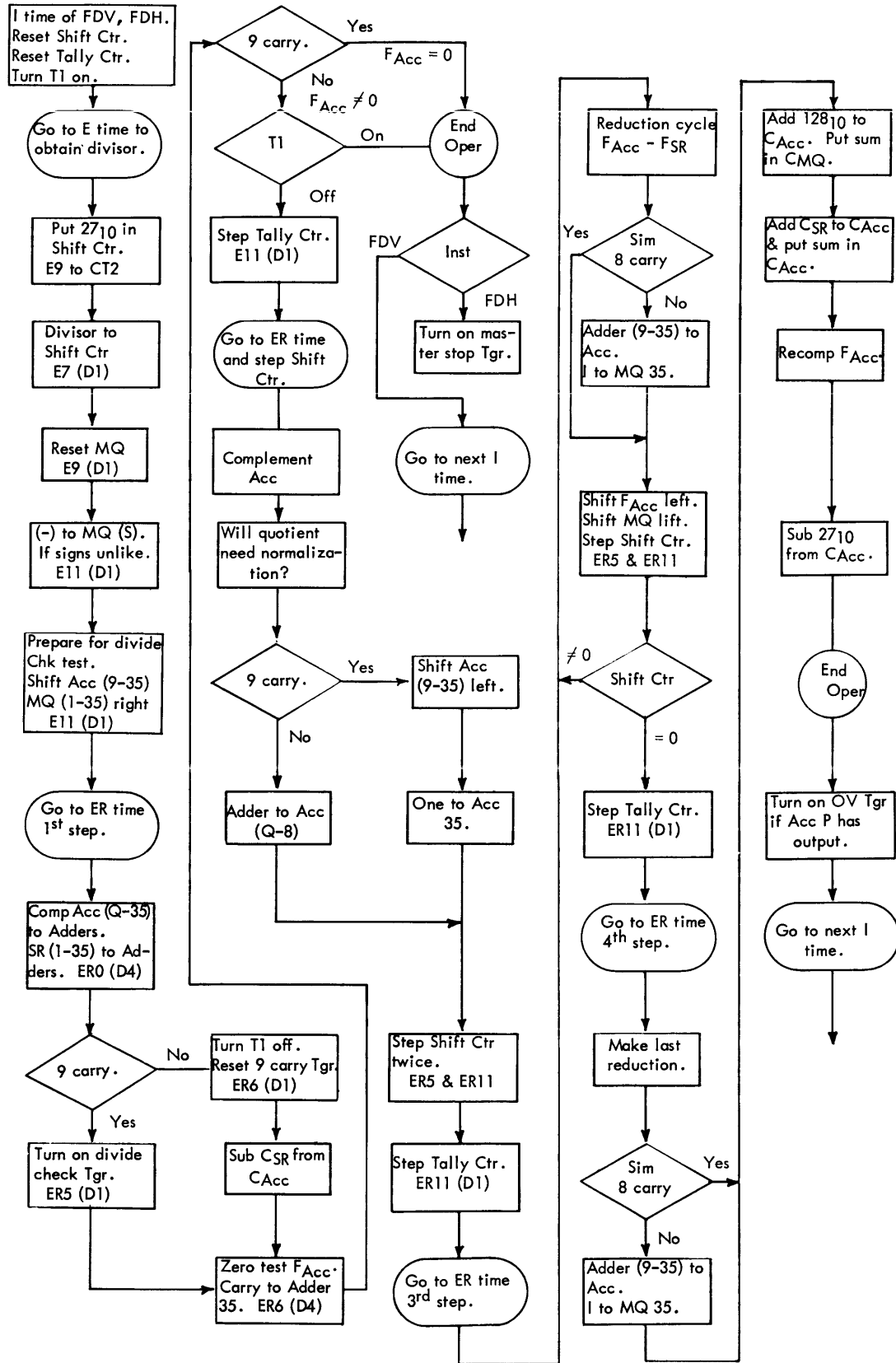


FIGURE 63-27. FLOATING POINT DIVIDE INSTRUCTION

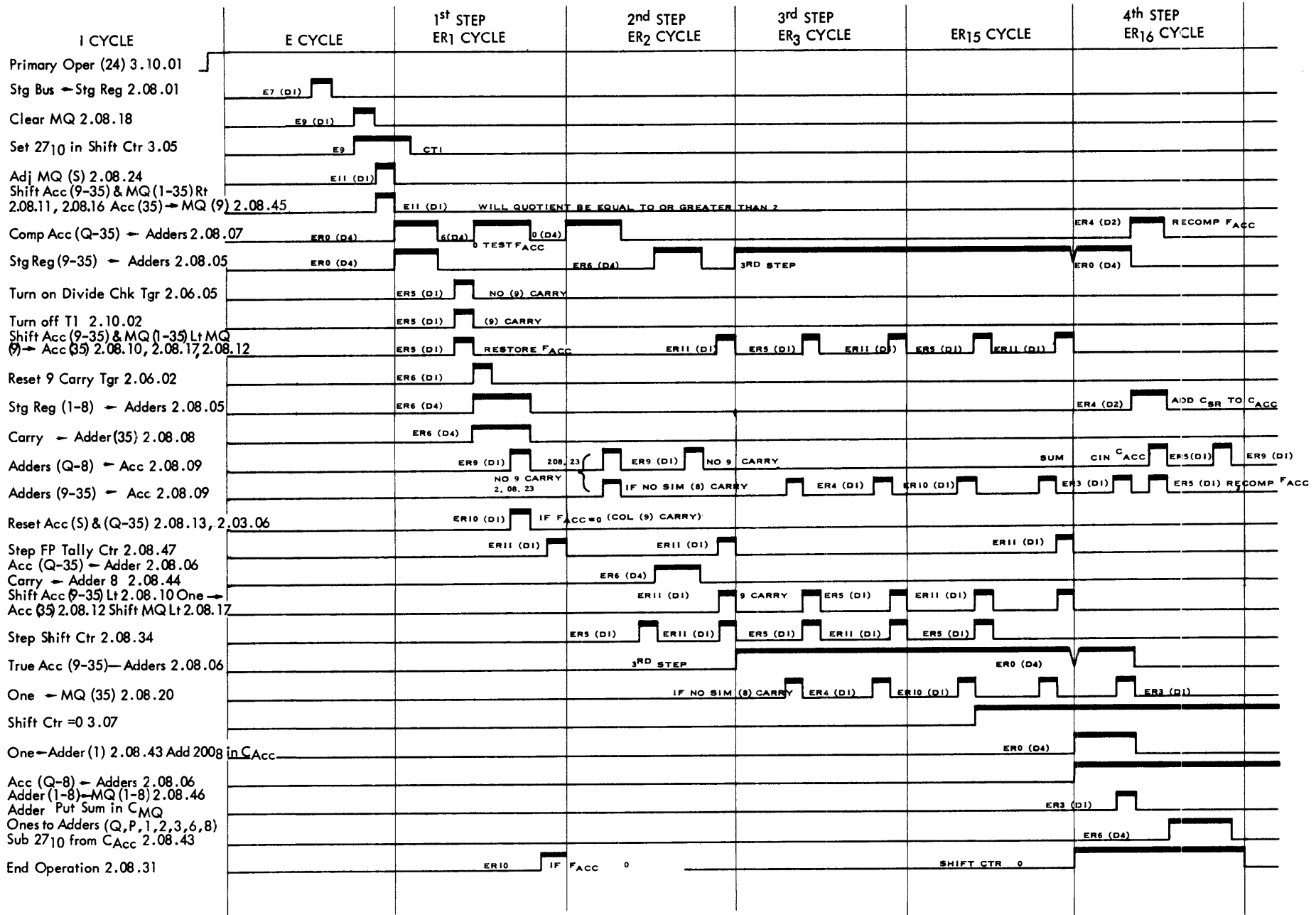


FIGURE 63-28. FLOATING POINT DIVIDE INSTRUCTION + 0241

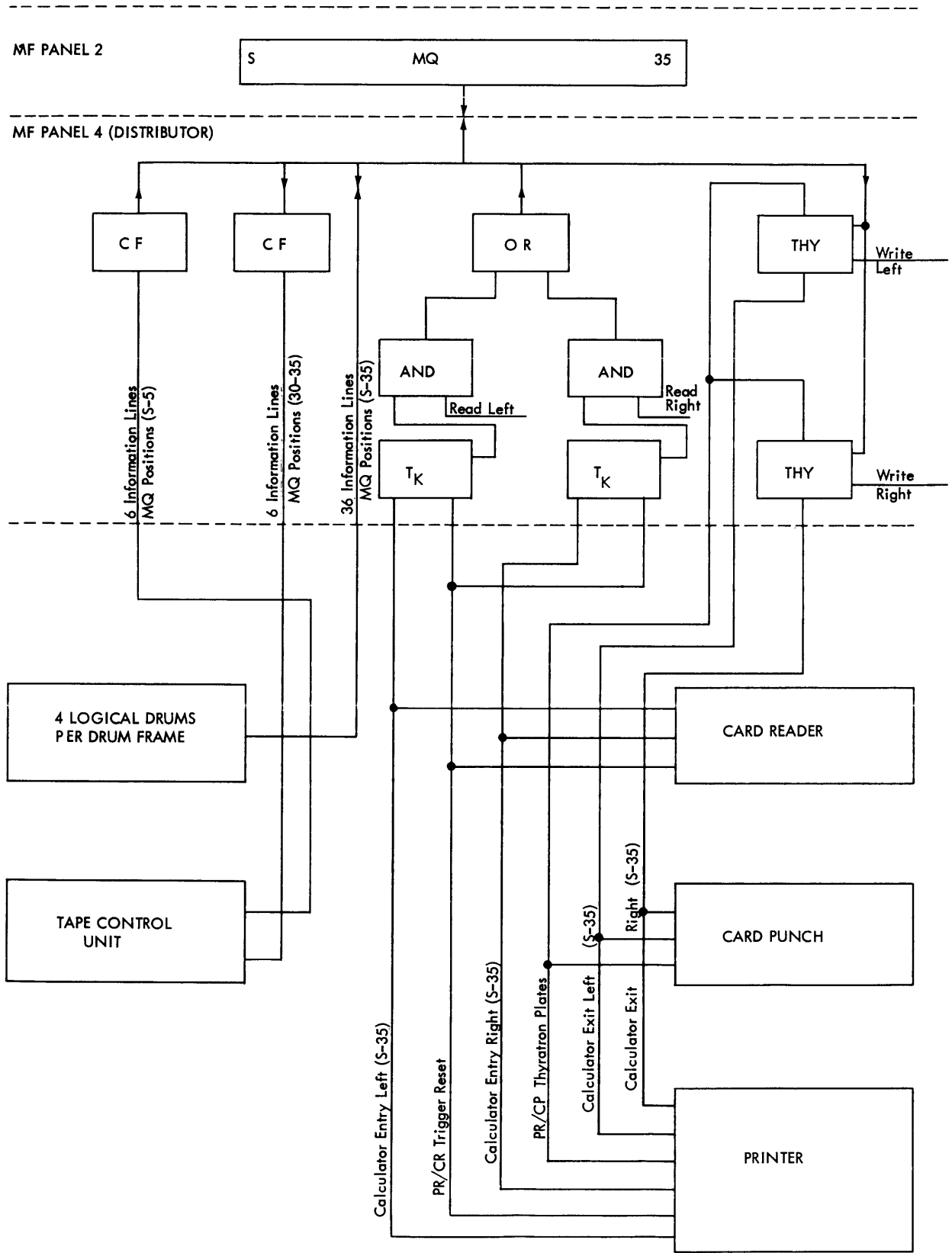


FIGURE 64-1. INFORMATION PATHS BETWEEN THE MQ AND THE I/O UNITS

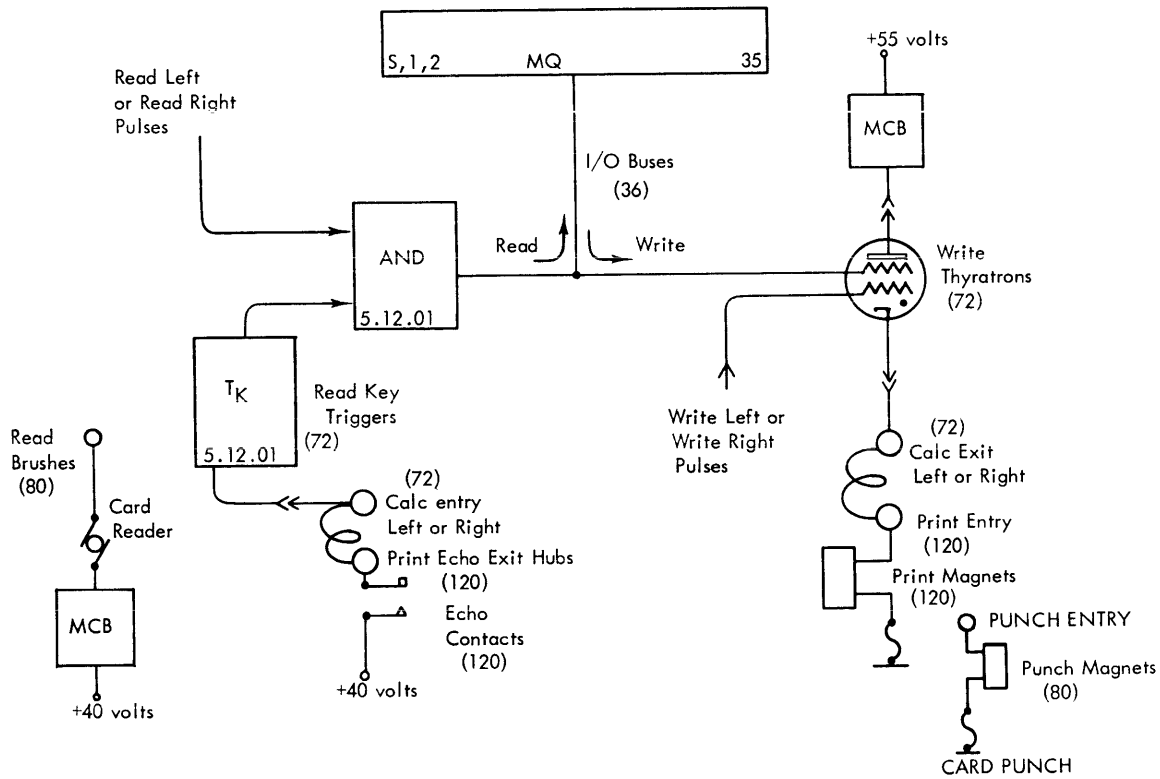


FIGURE 64-2. CARD MACHINE INFORMATION FLOW

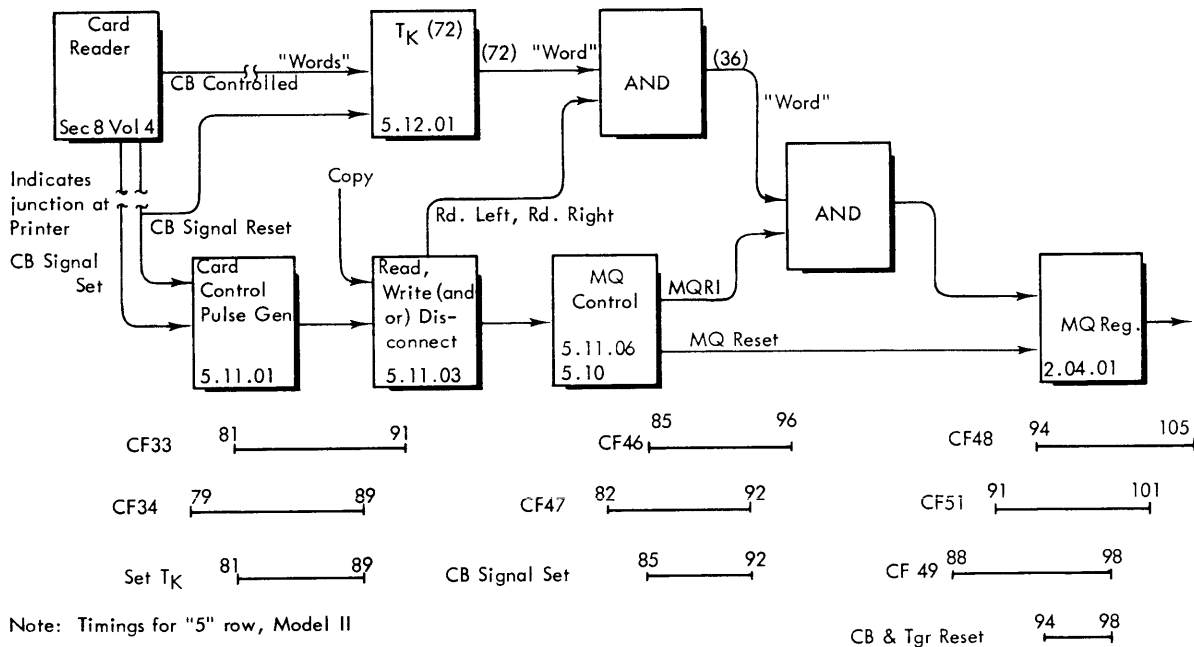


FIGURE 64-3. LOGIC FLOW OF INFORMATION FROM CARD READER TO MQ

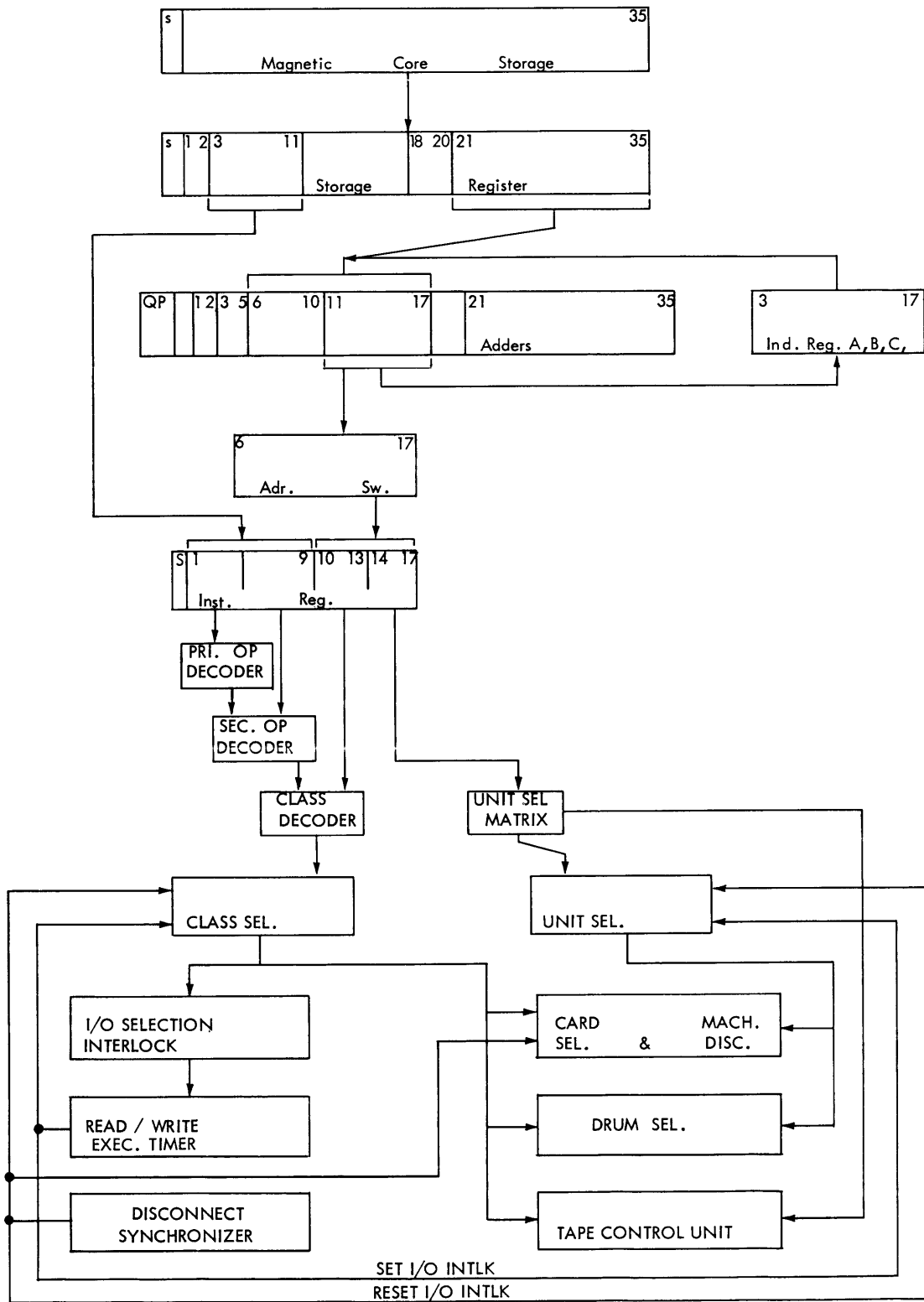


FIGURE 64-4. SELECTION OF AN I/O DEVICE

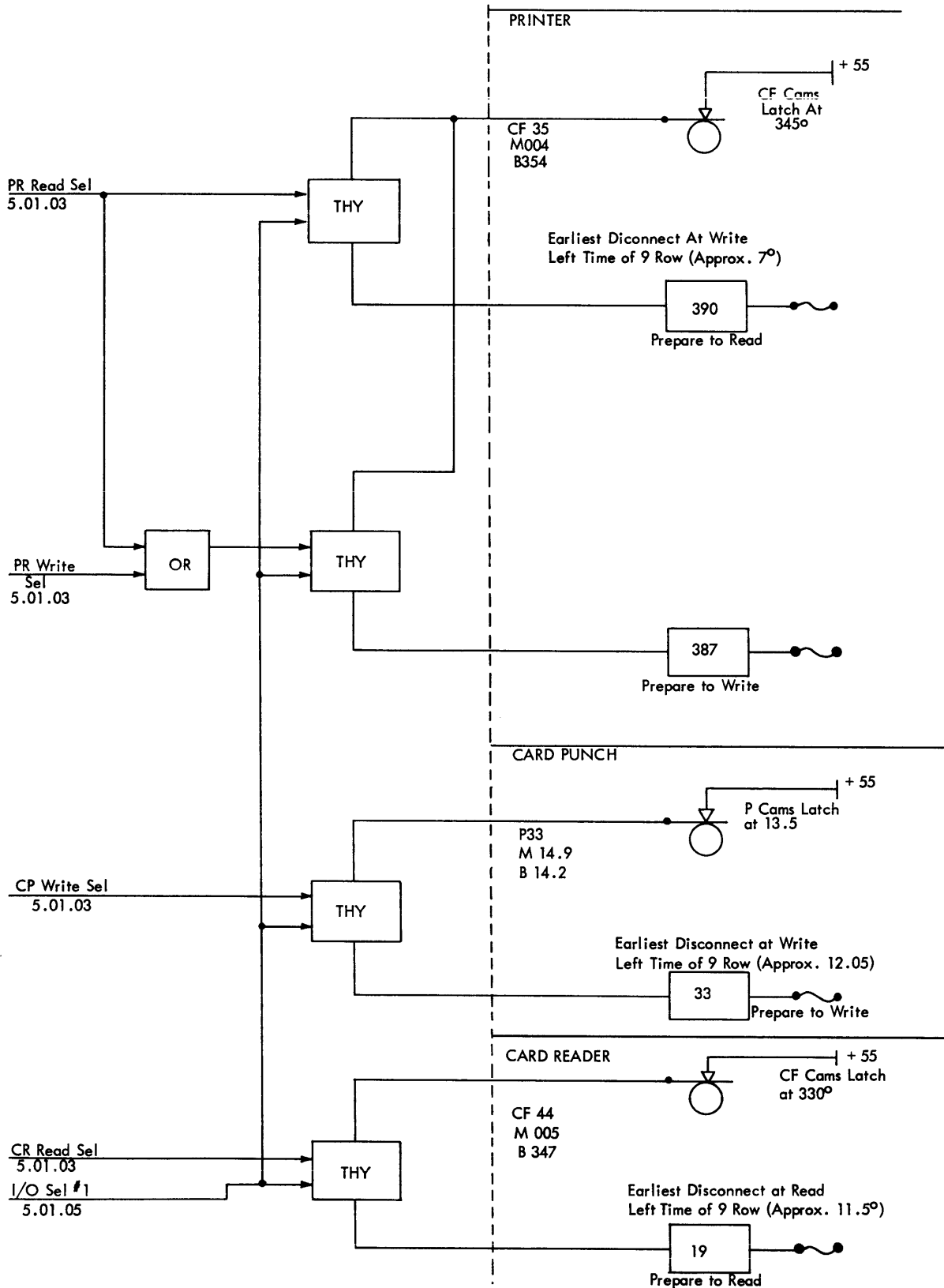


FIGURE 65-5. CARD MACHINE SELECTOR (5.01.06)

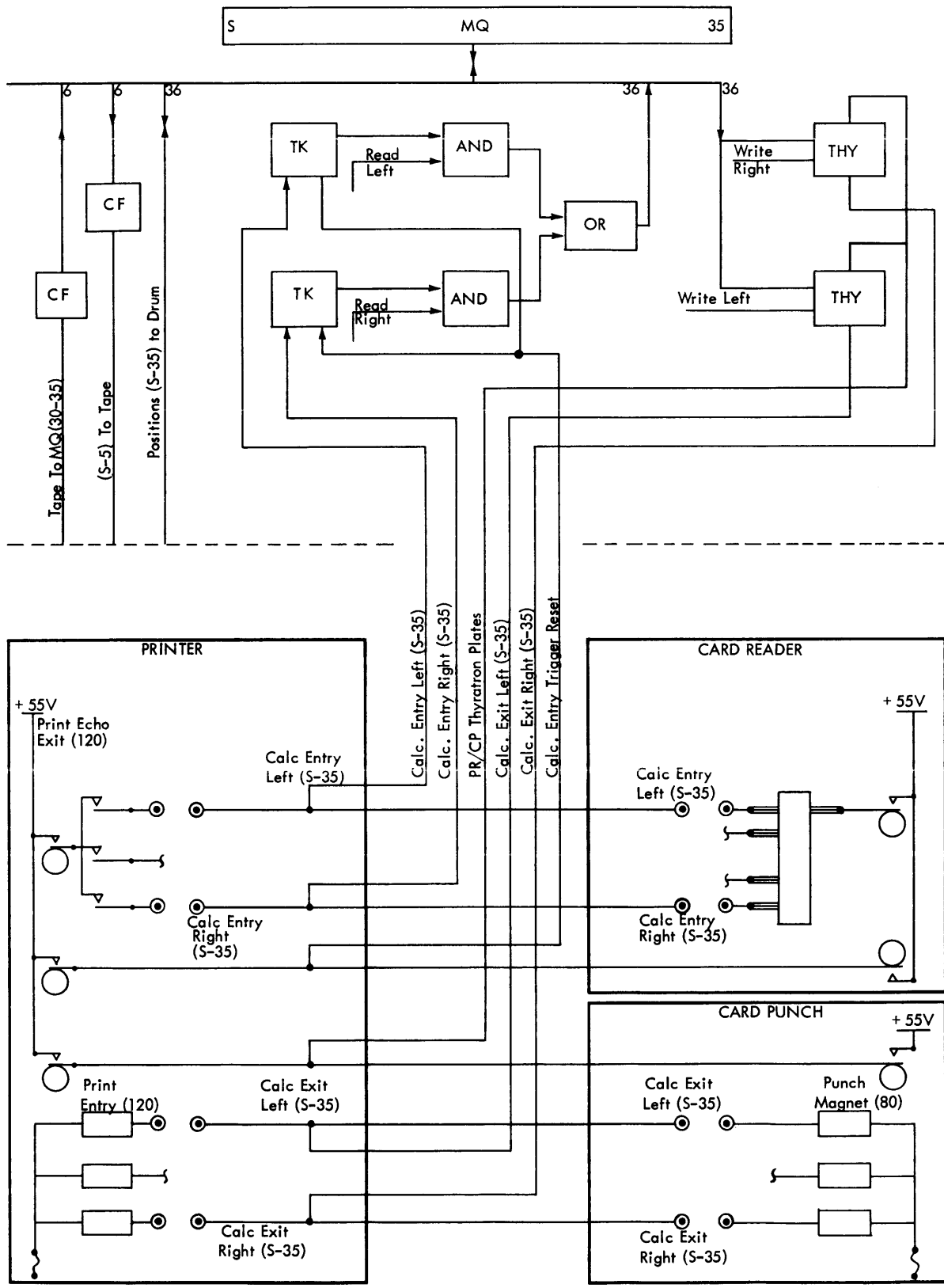


FIGURE 64-6. CARD MACHINE READING AND WRITING DATA FLOW

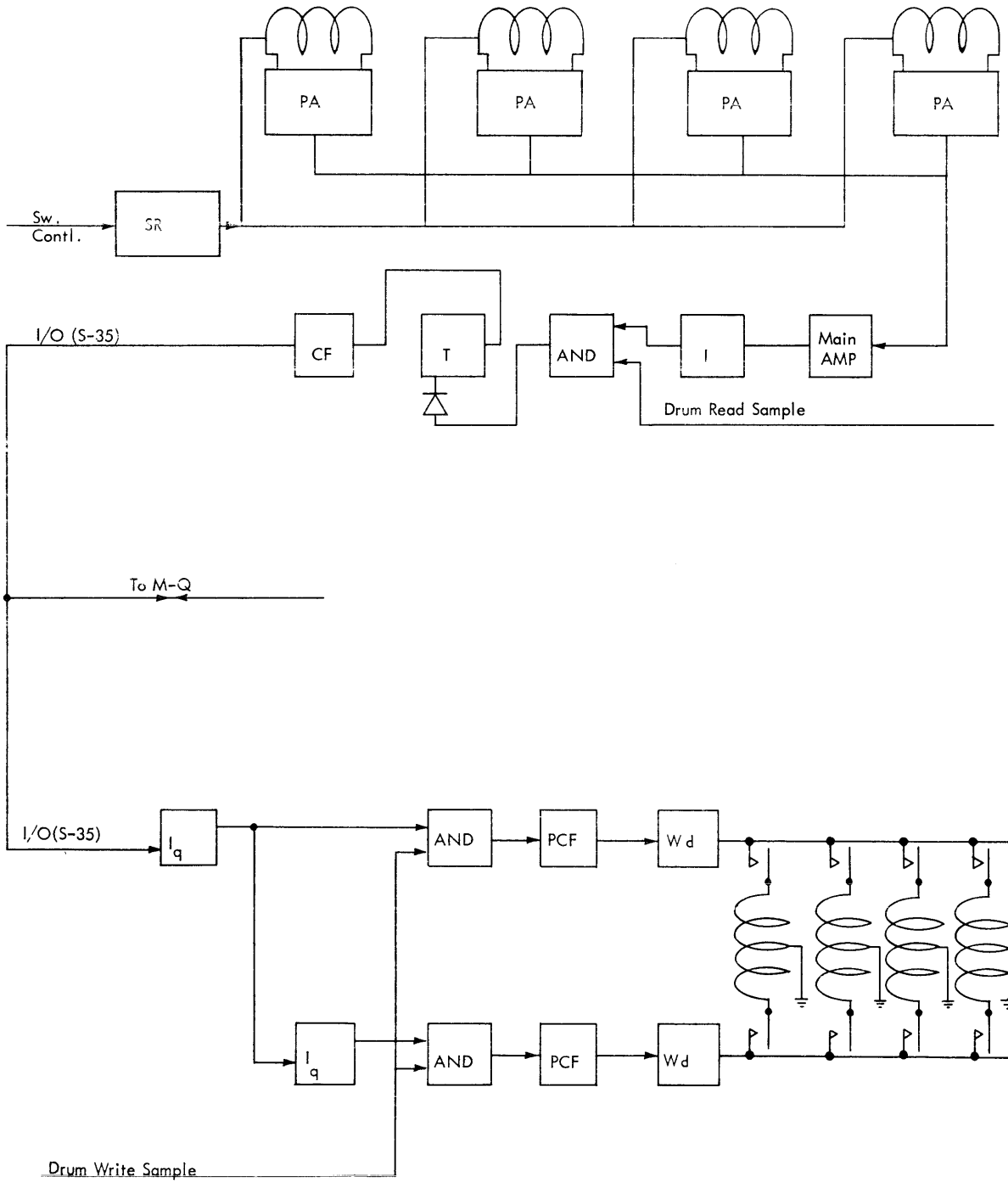


FIGURE 64-7. DRUM READING AND WRITING DATA FLOW

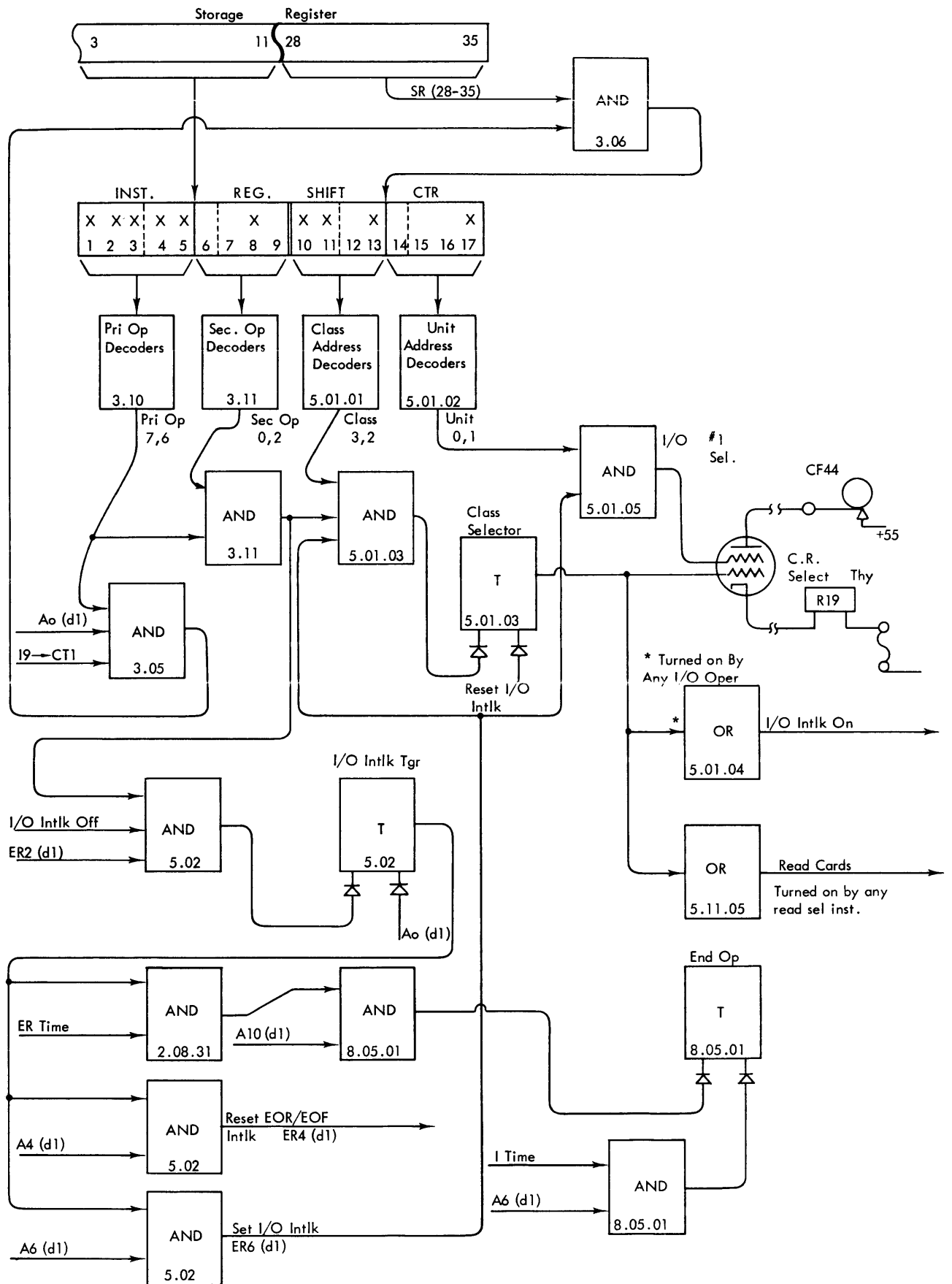


FIGURE 64-8. LOGIC FLOW OF 0762 RDS...0321

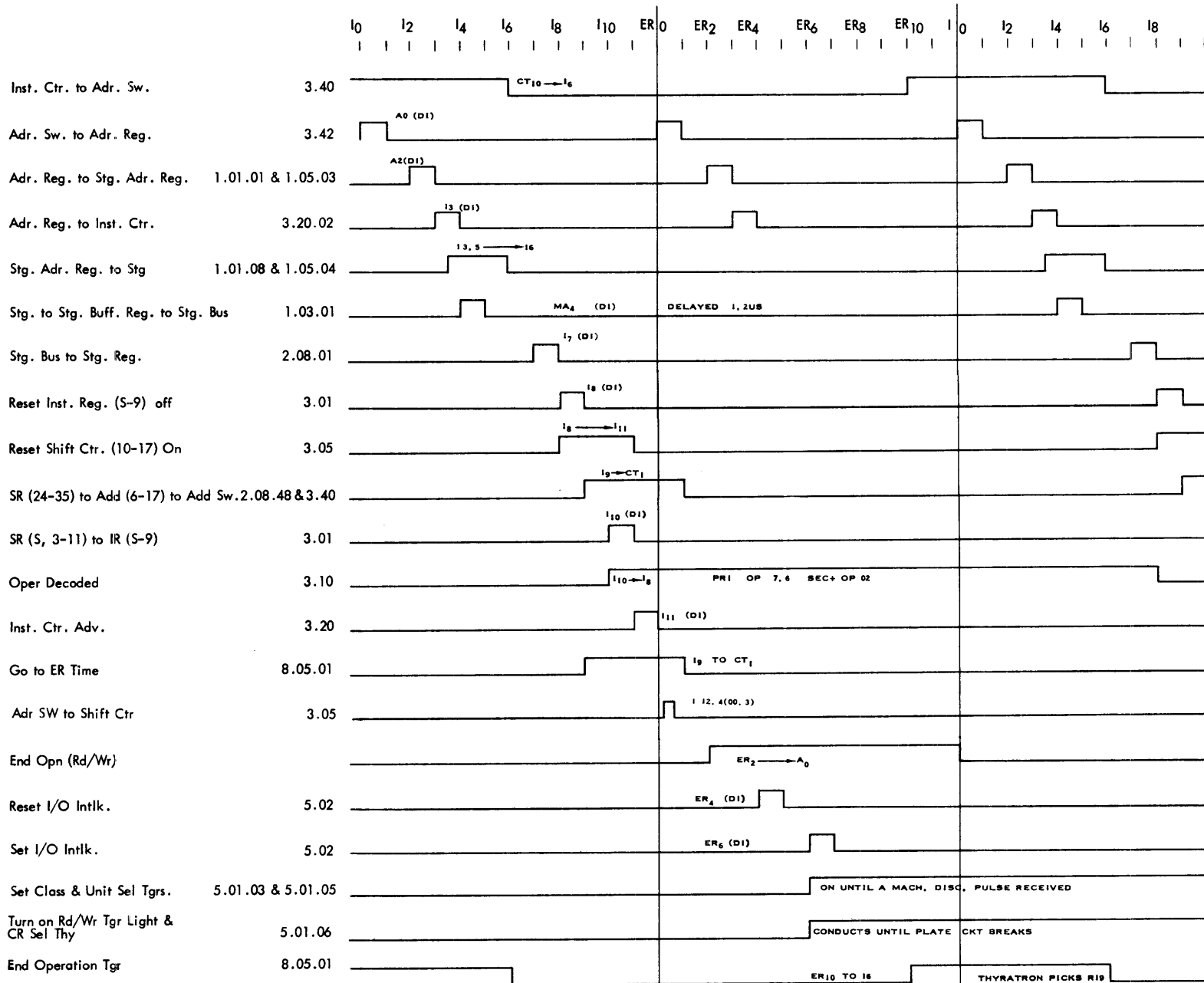


FIGURE 64-9. SELECT READER 0762 RDS...0321

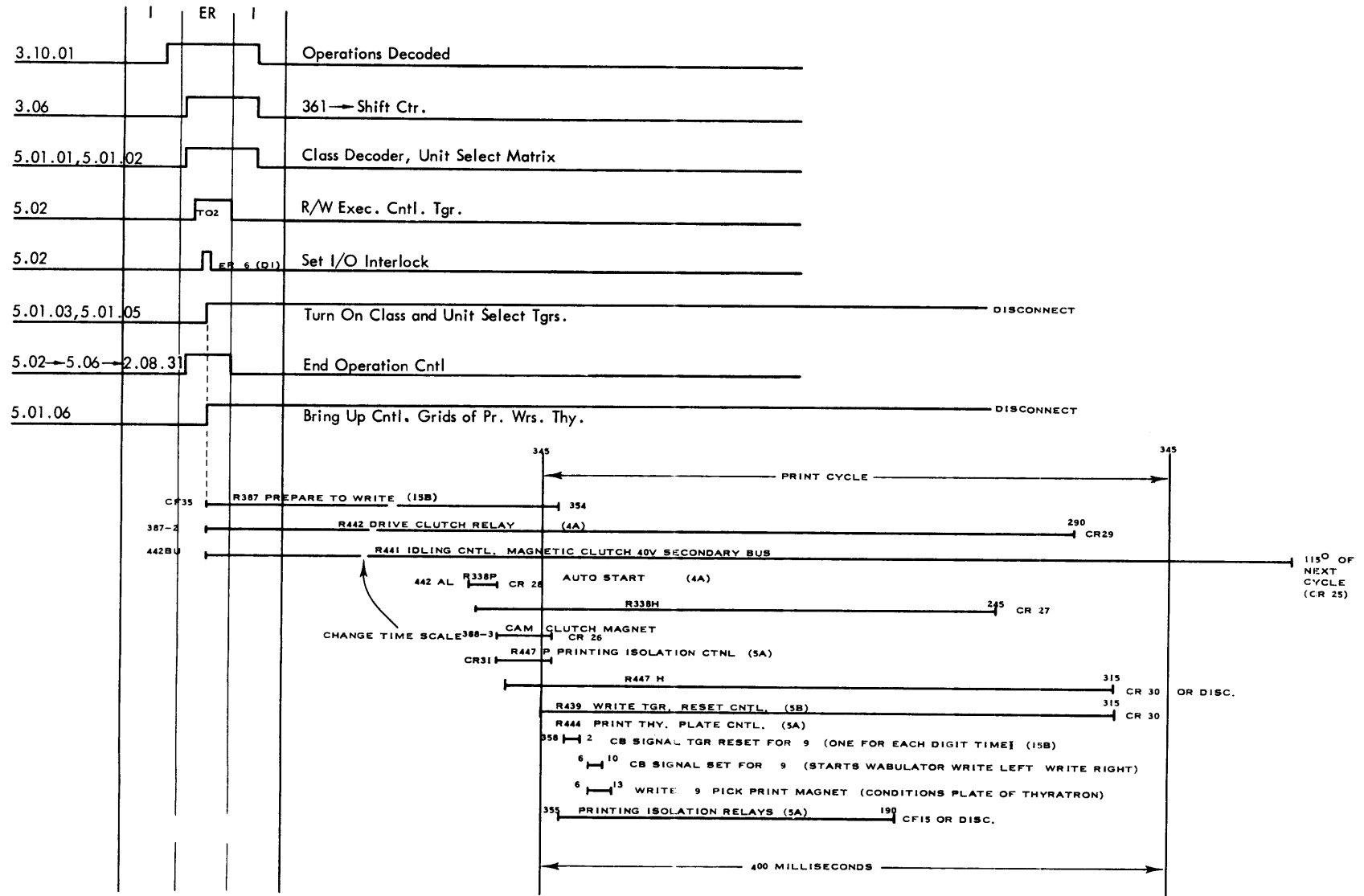
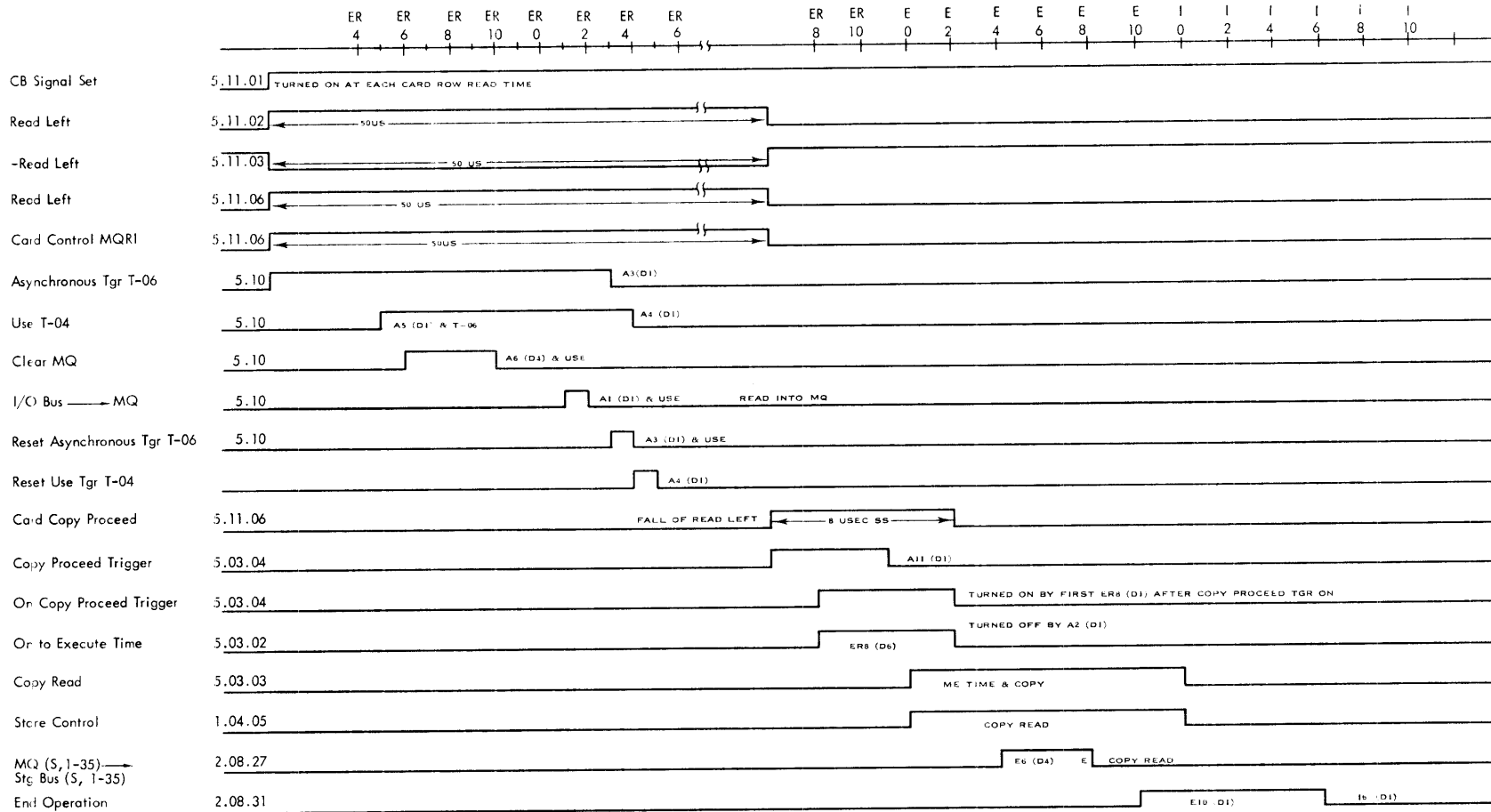


FIGURE 64-10. WRITE PRINTER 0766 WRS...0361



The I time of a copy instruction is the same as the I time of a RDS. When the main frame goes into ER time no end operation can be brought up so the machine hangs up in ER time of copy waiting for the CB signal set pulse generated during a reader feed cycle.

FIGURE 64-11. COPY INSTRUCTION FOLLOWING RDS 0321

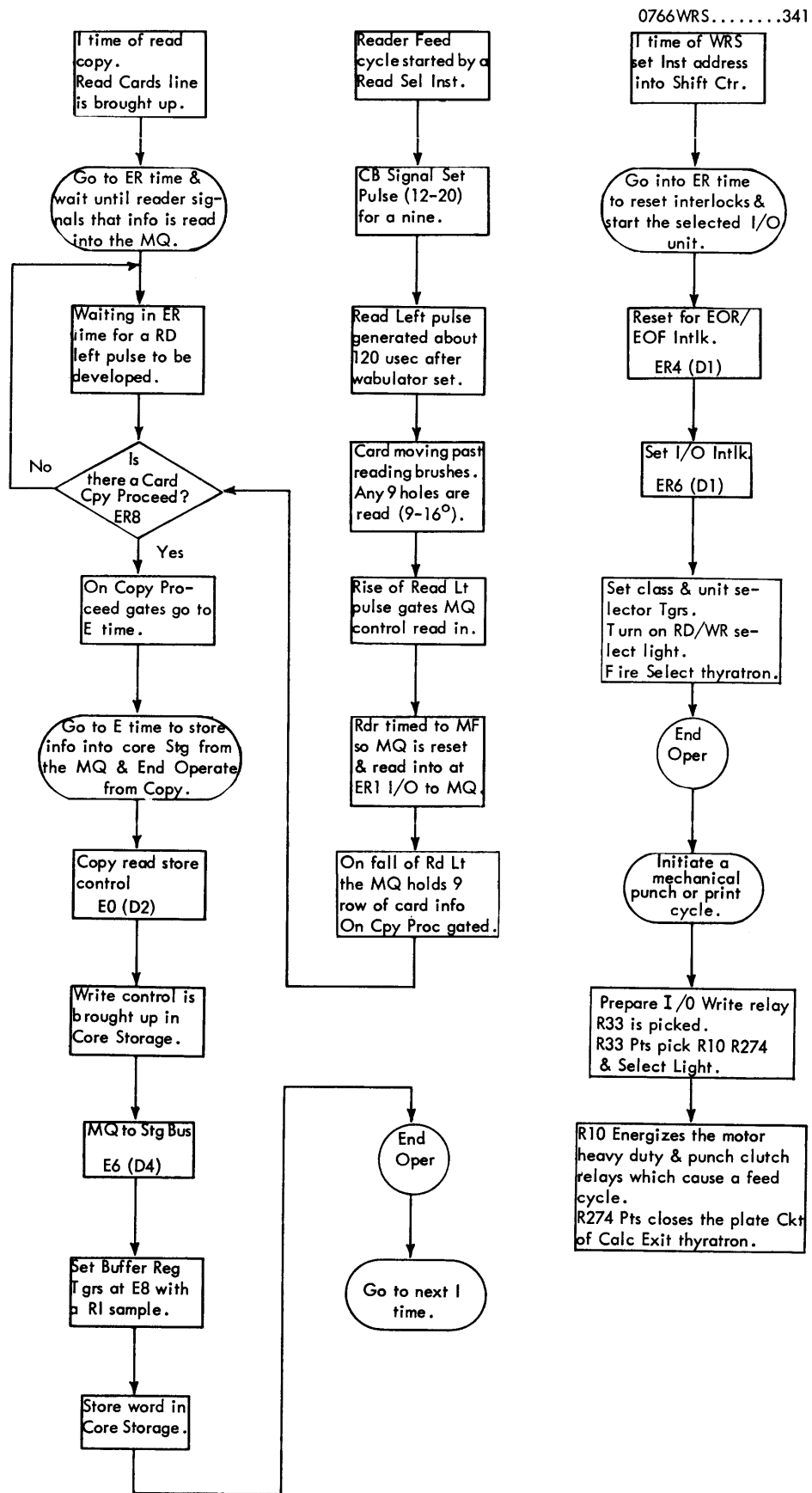


FIGURE 64-12. COPY FOLLOWING RDS 0321

FIGURE 64-13. WRITE PUNCH RECORDS 0766WRS -0341

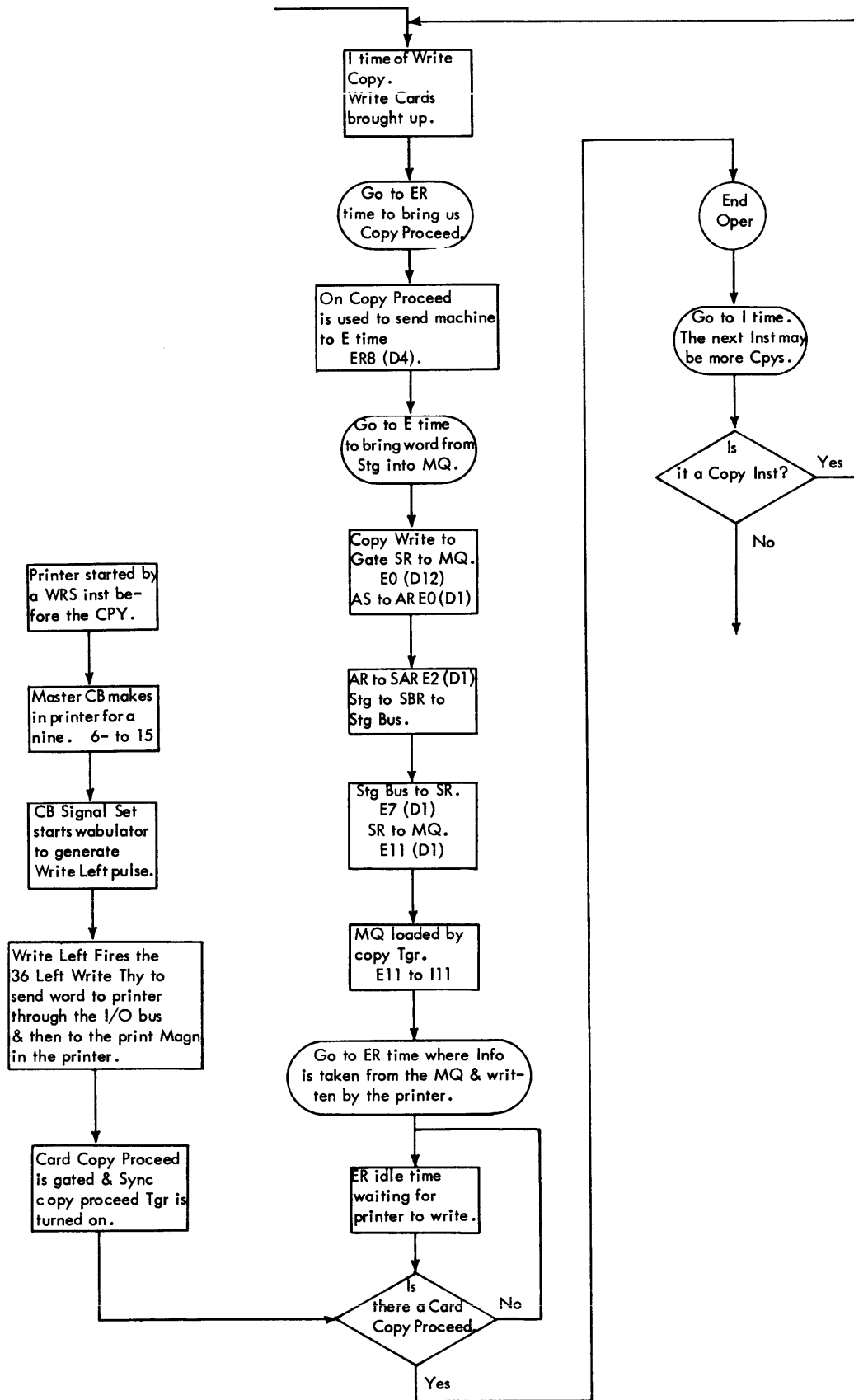


FIGURE 64-14. COPY FOLLOWING WRITE SELECT 0361

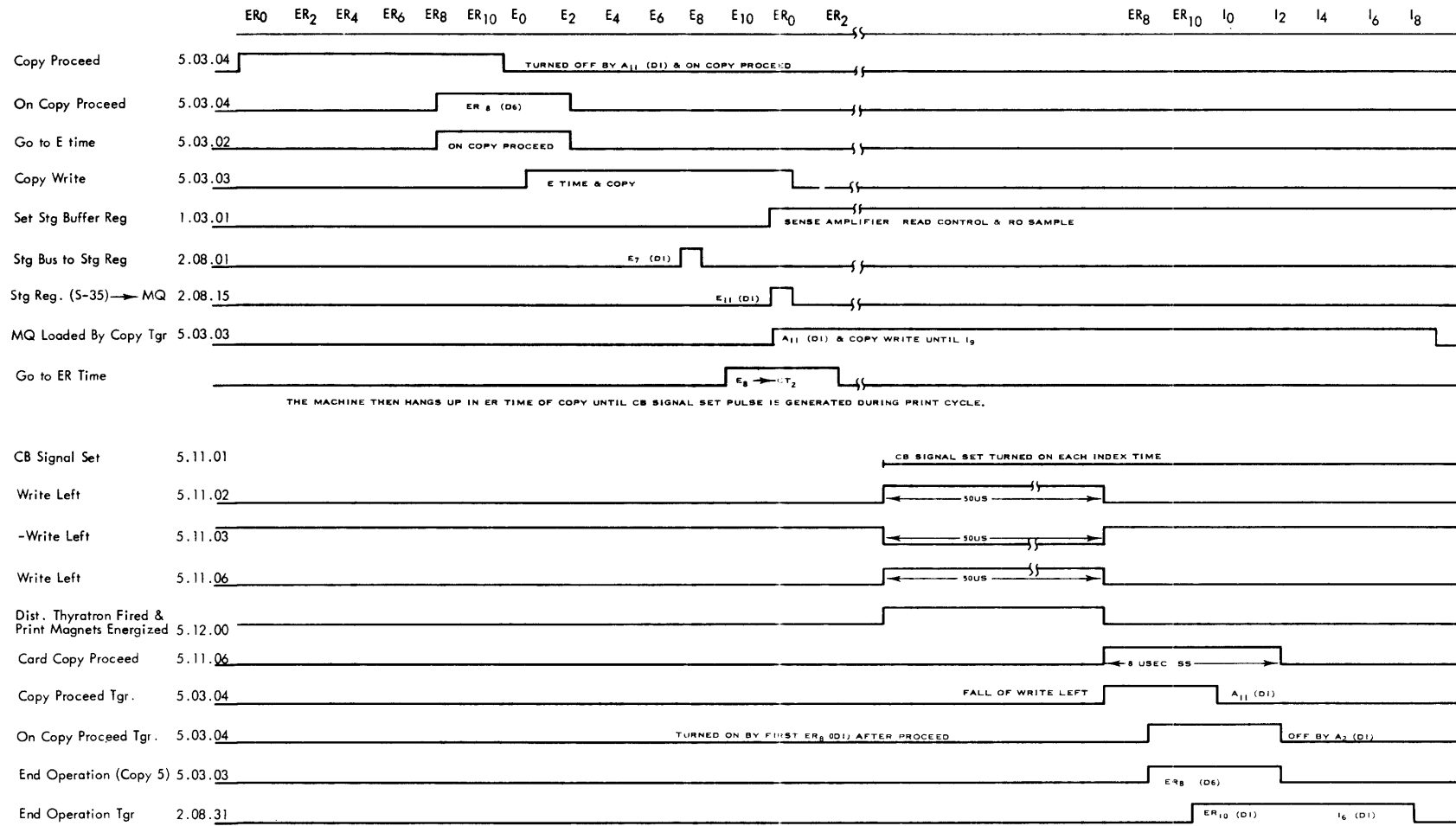


FIGURE 64-15. COPY FOLLOWING WRITE SELECT PRINTER

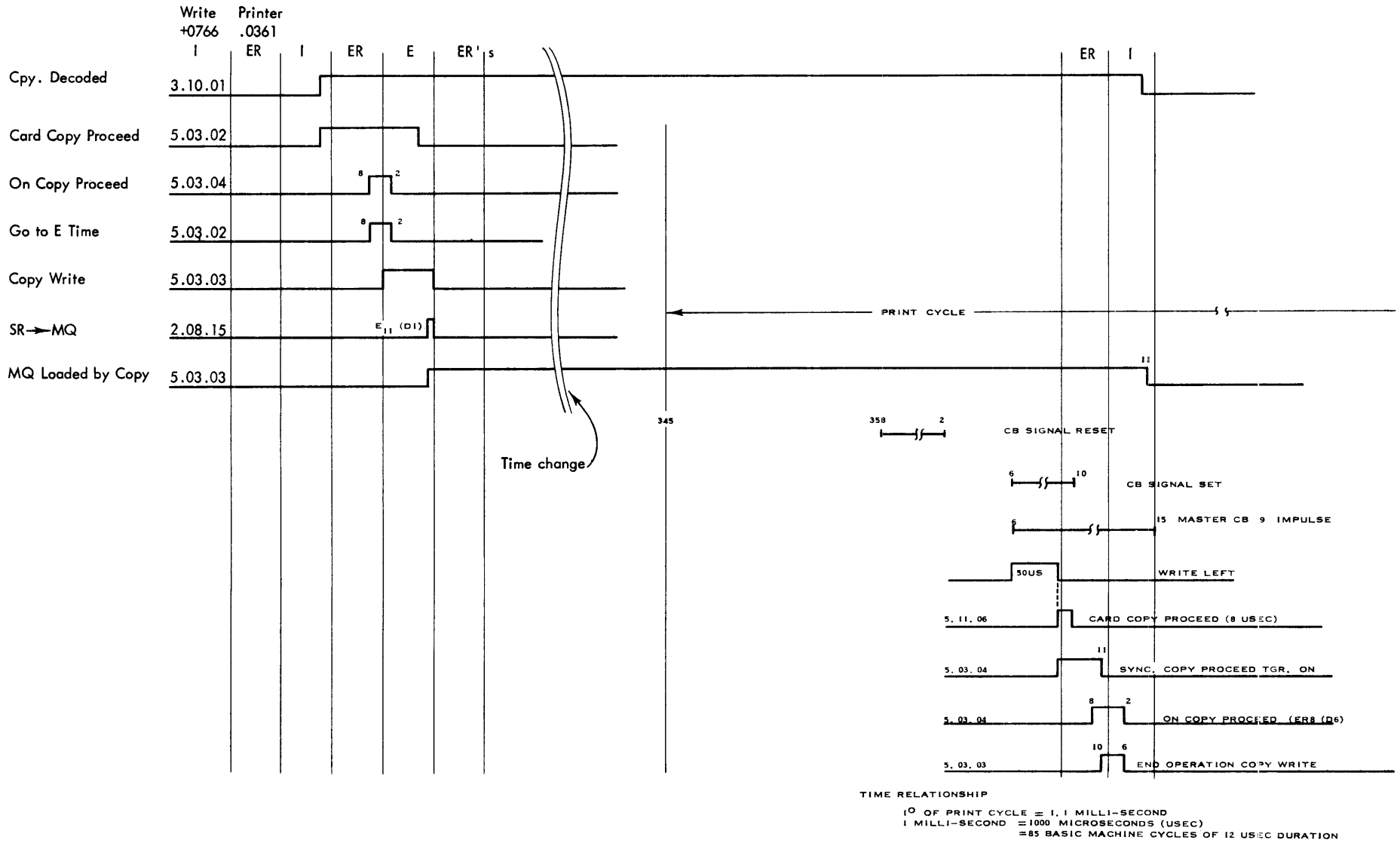


FIGURE 64-16. COPY INSTRUCTION AFTER WRS 0361

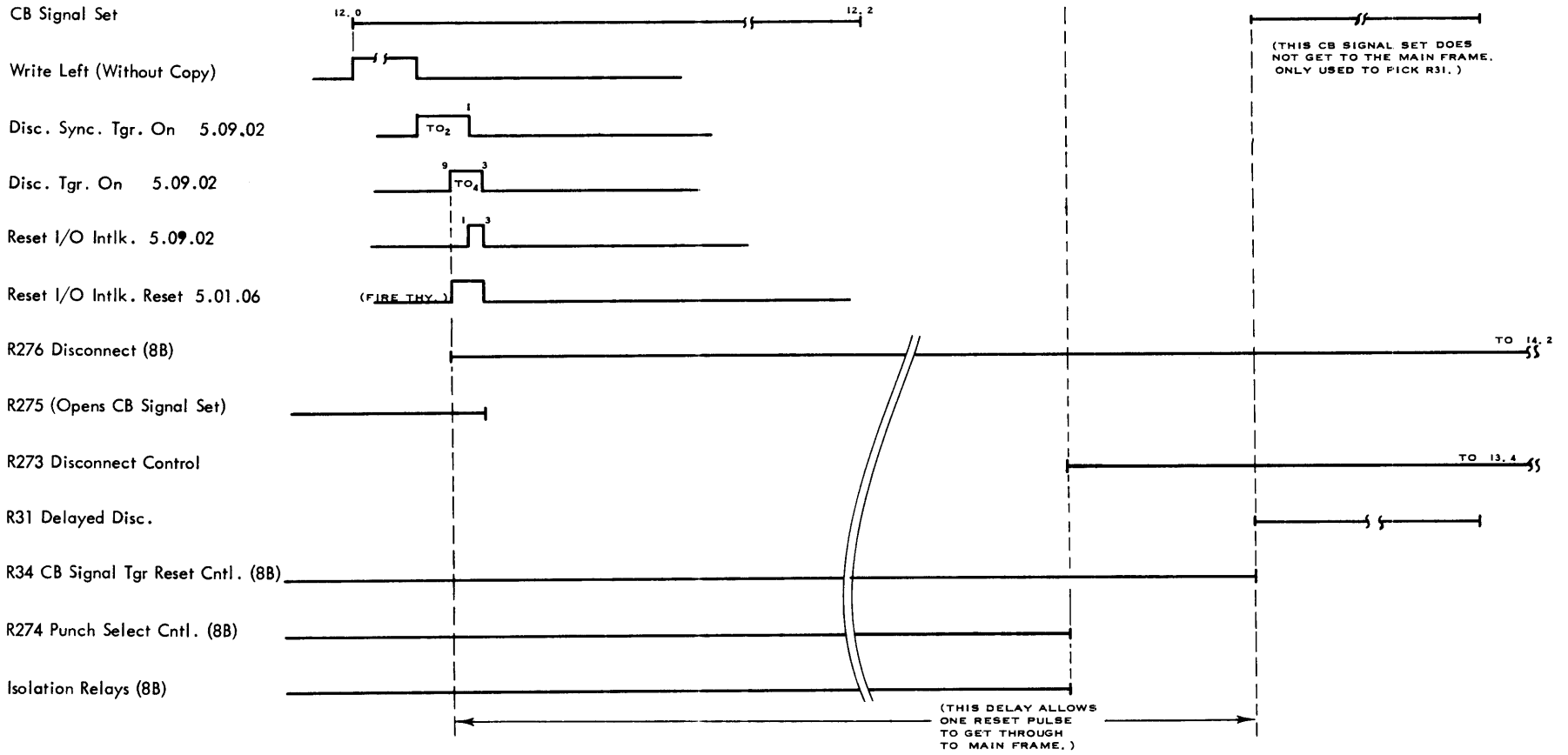


FIGURE 64-17. DISCONNECT FROM CARD PUNCH

SECTION	TITLE	PAGE
704.70.00	MANUAL MACHINE LOGIC	70-2
704.71.00	Clock and Cycle Timer	70-2
	Figure 71-1 Primary Drive Circuits	70-3
	Figure 71-2 Arithmetic Column Units	70-4
	Figure 71-3 Inverted Sync and Clamp Pulse	70-4
	Figure 71-4 Cycle Timer and Control Circuits	70-5
704.72.00	Card Control Circuits	70-6
	Figure 72-1 Card Control Pulse Generator (Wabulator)	70-6
	Figure 72-2 Card Control Ring (5.11.02)	70-6
	Figure 72-3 Card Control CB Counter	70-7
704.73.00	Key Routines	70-8
	Figure 73-1 Load Timer	70-8
	Figure 73-2 Display Effective Address	70-9
	Figure 73-3 Enter MQ	70-9

704.70.00 MANUAL MACHINE LOGIC

704.71.00 CLOCK AND CYCLE TIMER

In this section all the manual logic and logic that can be manually controlled is covered. Also any item that does not seem to logically fall into any other category is found in this section. Two of these items are the clock and cycle timer logic. The card control circuits are also covered here as well as some of the key routines.

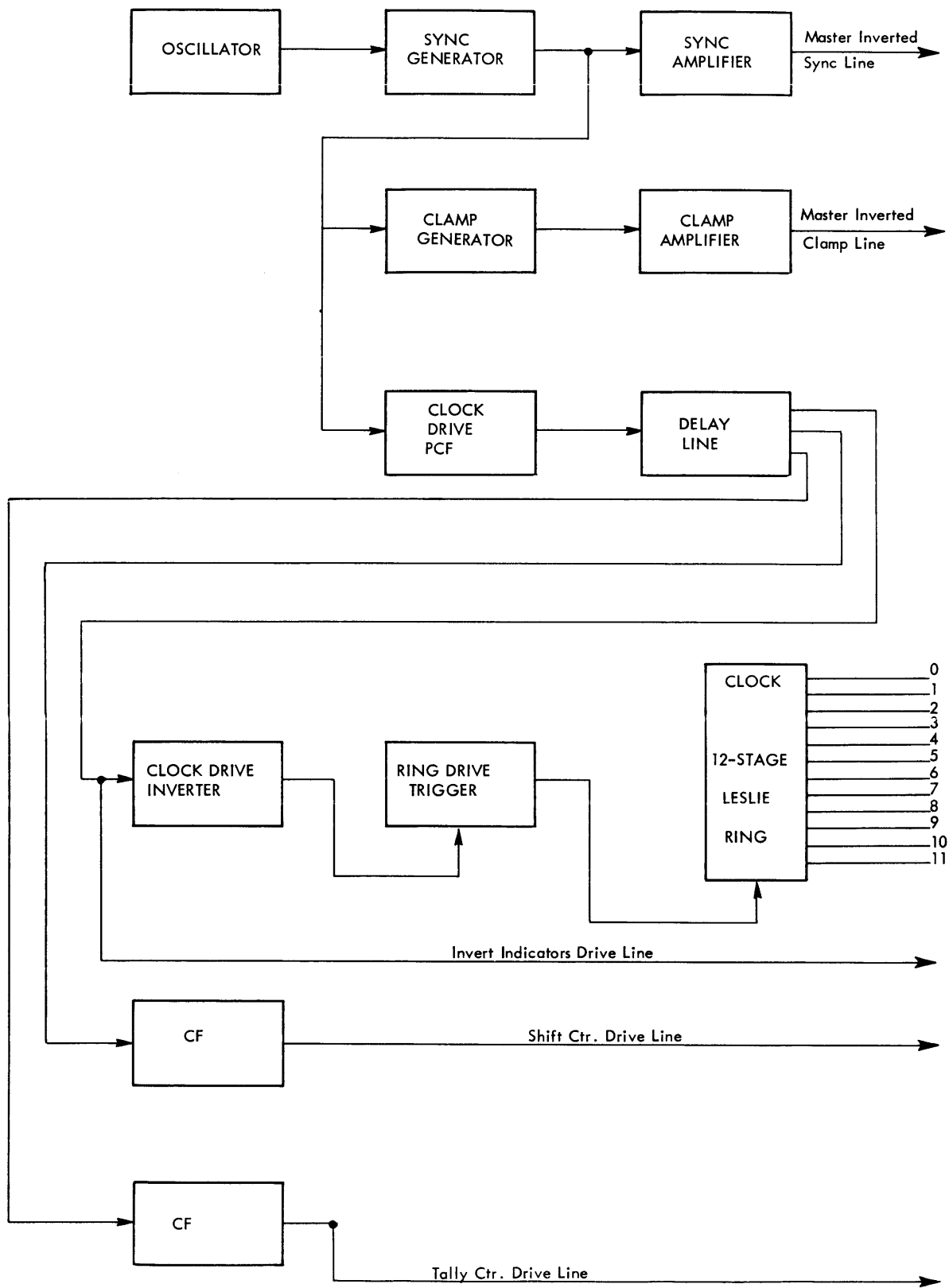


FIGURE 71-1. PRIMARY DRIVE CIRCUITS

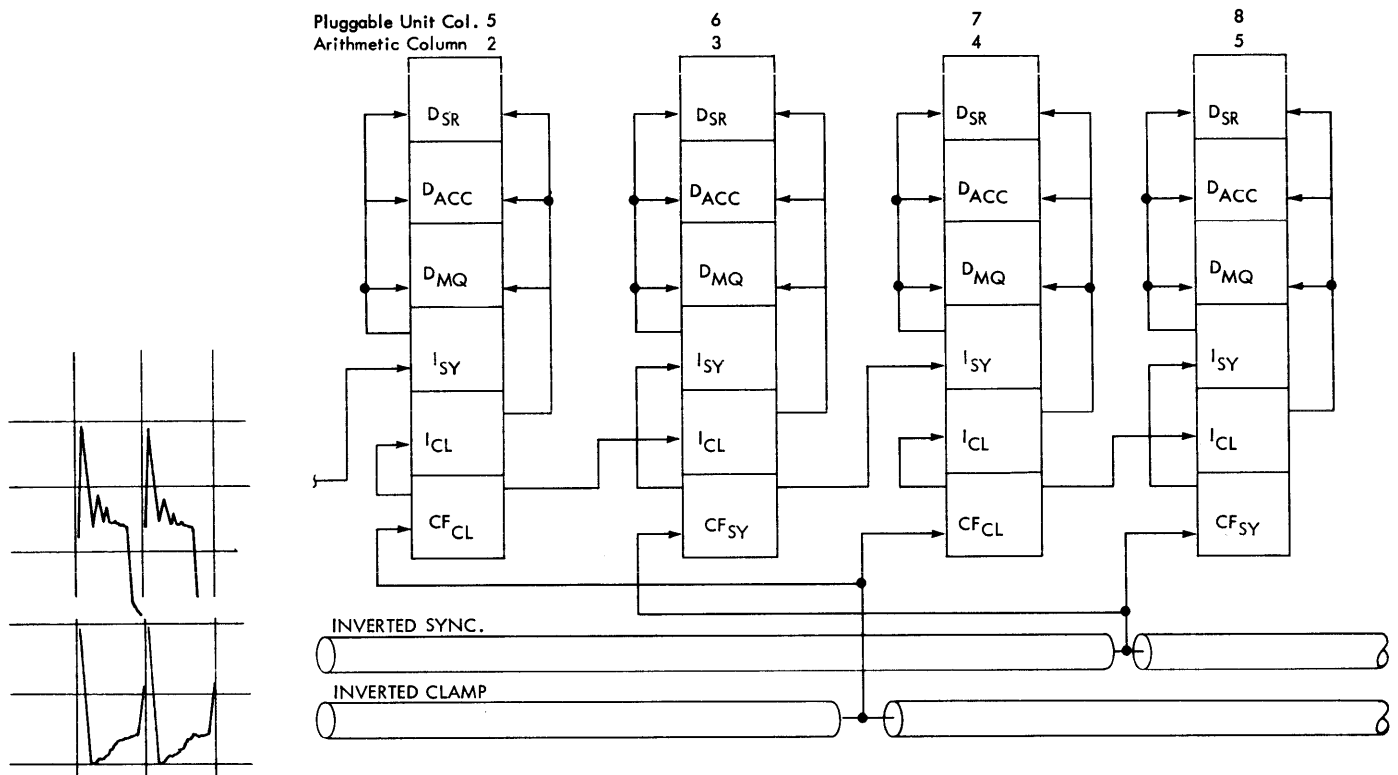


FIGURE 71-2. ARITHMETIC COLUMN UNITS

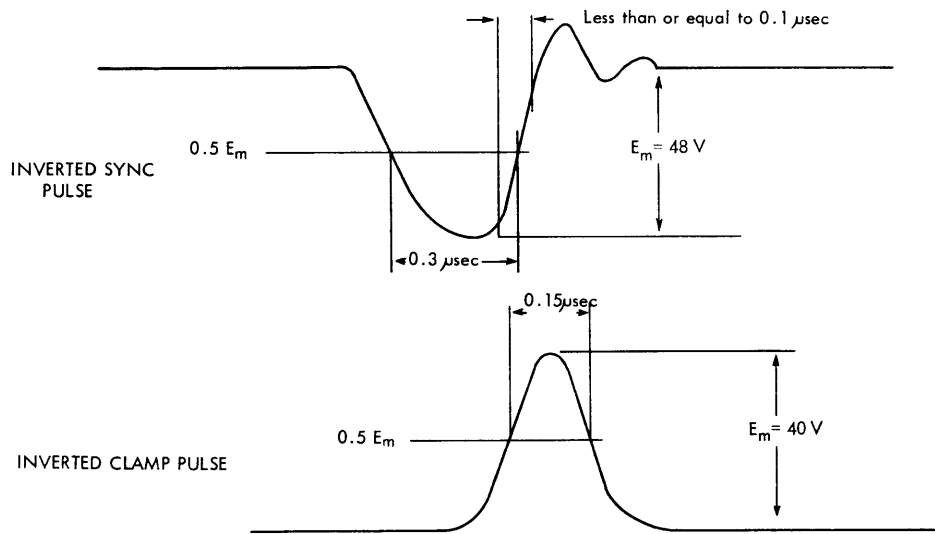


FIGURE 71-3. INVERTED SYNC AND CLAMP PULSE

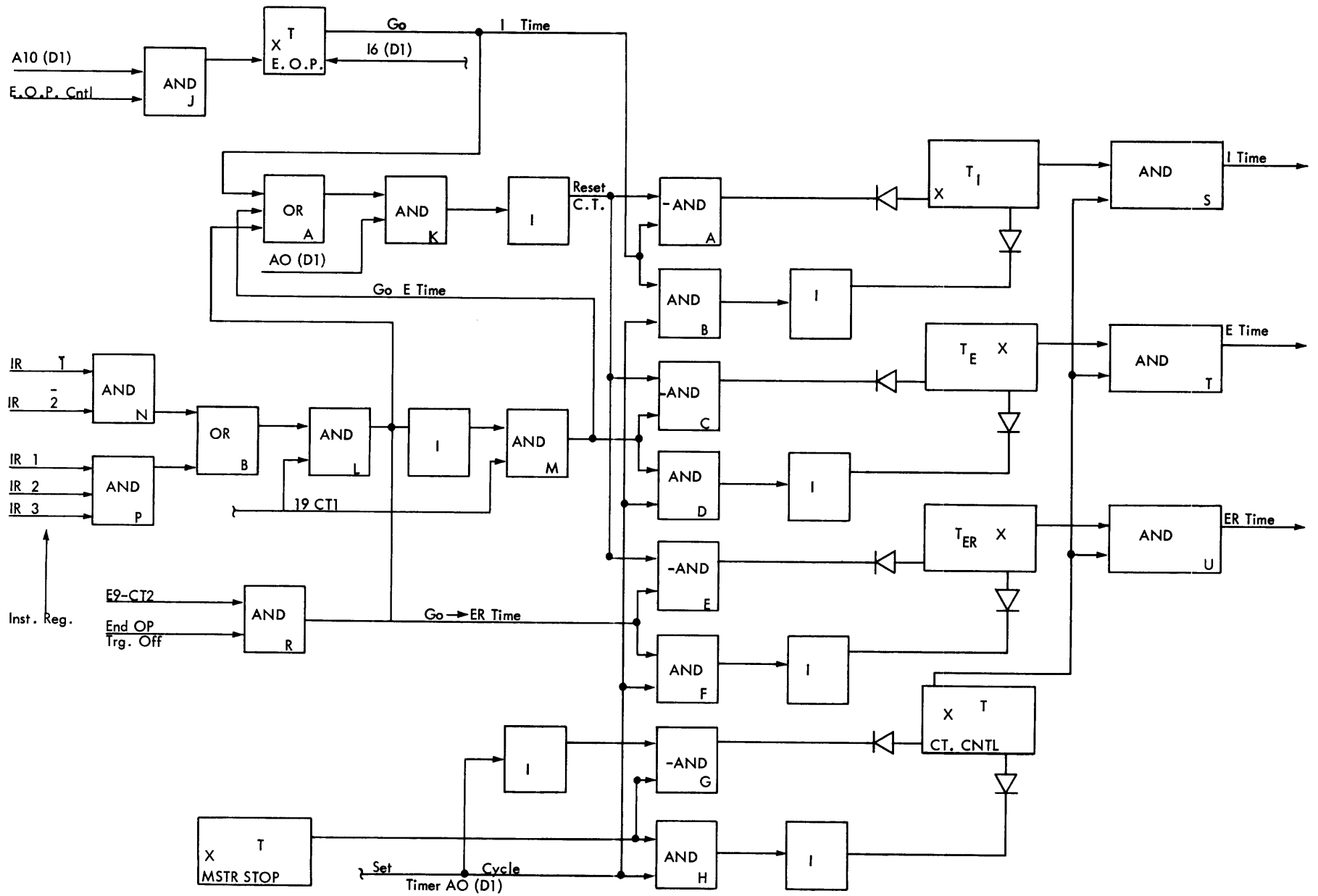
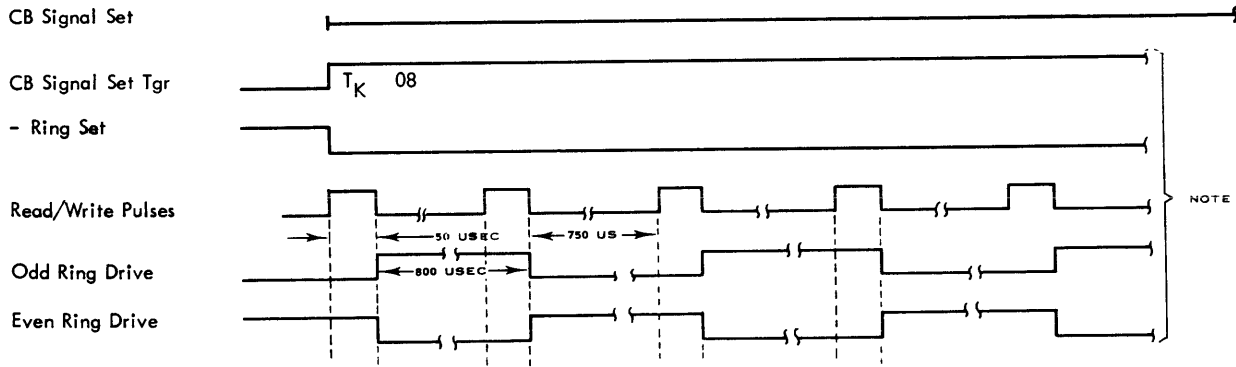


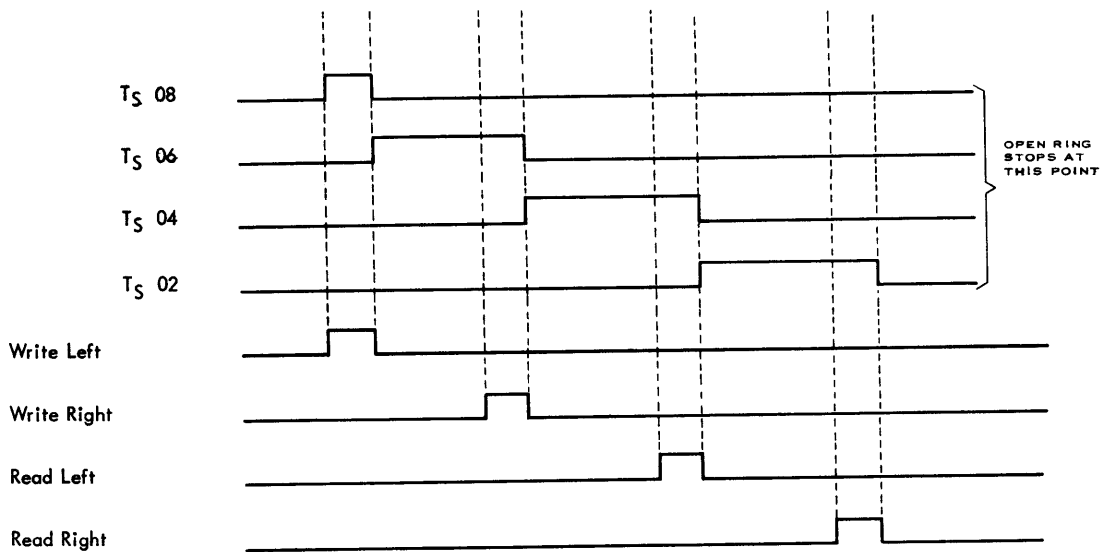
FIGURE 71-4. CYCLE TIMER AND CONTROL CIRCUITS

704.72.00 CARD CONTROL CIRCUITS



Note: Wabulator Pulses Continue Until Next CB Signal Tgr Reset

FIGURE 72-1. CARD CONTROL PULSE GENERATOR (WABULATOR)



The Card Control Ring stops even though the "Wabulator" continues to run.
The Card Control Ring can only be started after - Ring Set.

FIGURE 72-2. CARD CONTROL RING (5.11.02)

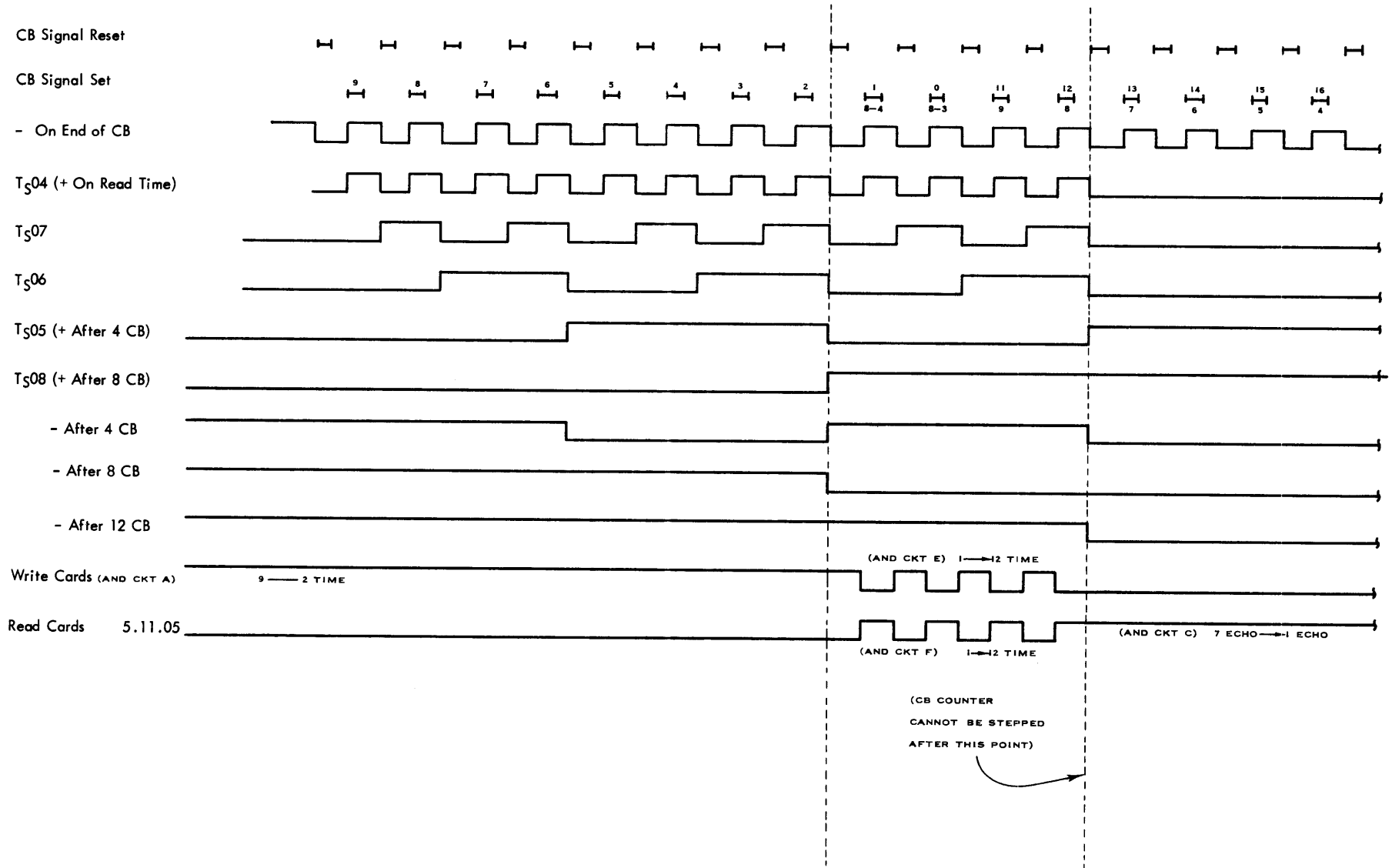


FIGURE 72-3. CARD CONTROL CB COUNTER

704.73.00 KEY ROUTINES

I/O Unit Ready

Push Load Button 4.19 - R 10

R54-4.19

R3 Puts Copy in Op Panel Keys 4.01

Load Button Key Trigger 4.19

Load Tr Ctrl Trigger 4.19

R55 Kills Op Keys Except Copy 4.19

Reset I/O, EOR/EOF, Copy Check, Blown Fuse, Halt Ctrl H (E)

Reset Inst Ctr, Adr Reg, SR (9-35) & Clear MQ

Set Cr Read Sel Tgr Causing Feed Cycle 5.01.03

Set I/O Intlk 5.01.04 & Read Cards 5.01.05

Load Ctrl Trigger 4.19

Unit Sel[#]1 Tgr 5.01.05 & Sel Thy 5.01.06 On until Disconnect M (L)

Op Panel Ctrl Tgr 4.05.01

Master Ctrl Tgr 4.05.01

Master Stop Trigger 4.05.04

Ready & Auto Light 4.05.04

+ On Ready 4.19 Kills Pick of R54 (C)

I/O Cycle Timer Trigger 8.05.03

Op Panel Key to Stg Reg Supp Stg Bus to Stg Reg 4.17

Copy in Stg Reg

Stg Reg (24-35) to Add (7-17) to Adr Sw 3.40

SR (S, 3-11) to Inst Reg (S-9) 3.01

Copy Decoded & Executed Waits for 9 Row Left & Then 9 Row Right to be Read into MQ & Stored at 0000 & then 0001' Inst Ctr Adv 3.20

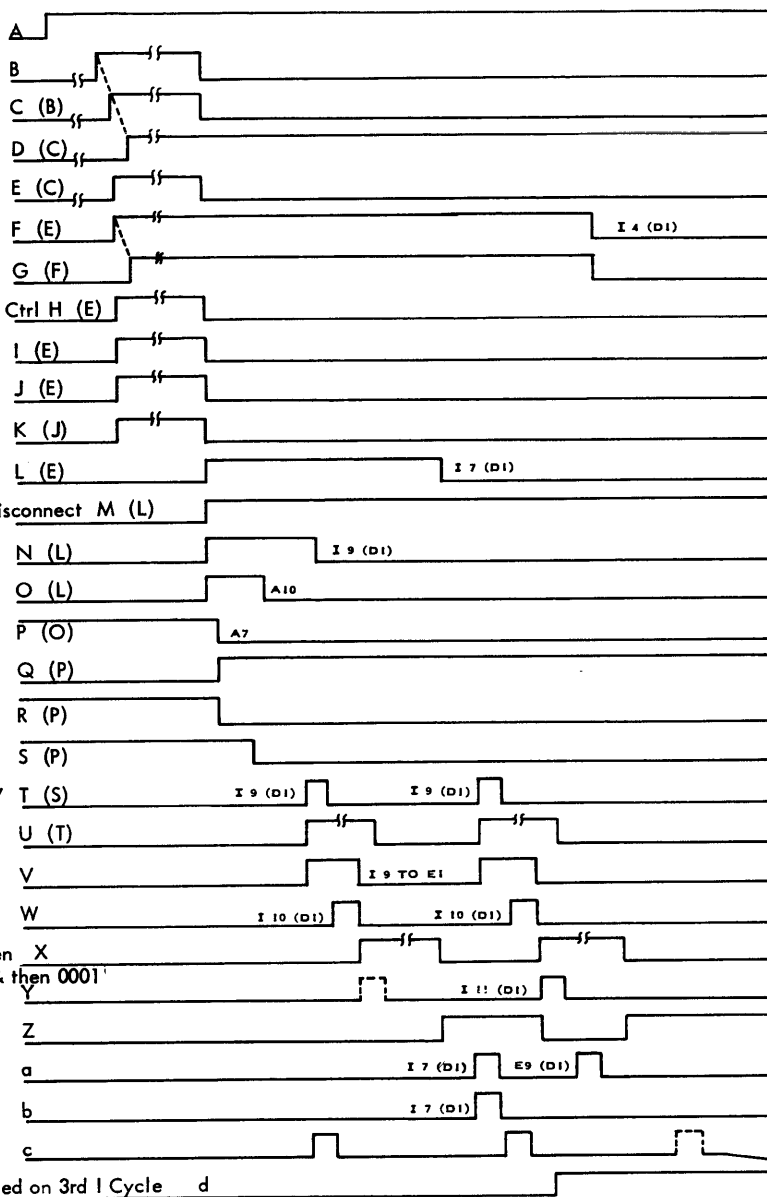
Second I Cycle

Reset Inst Ctr

Add 1 in Adr Reg

Inst Ctr to Ads Sw

Next Instruction taken from Stg 0000 & Executed Killed on 3rd I Cycle d



Note: The load cards button was pushed once; the card reader is taking a feed cycle; row 9 left is read into storage position 0000; row 9 right is read in storage position 0001, the machine has transferred to position 0000 of storage and is executing the instruction located there.

FIGURE 73-1. LOAD TIMER

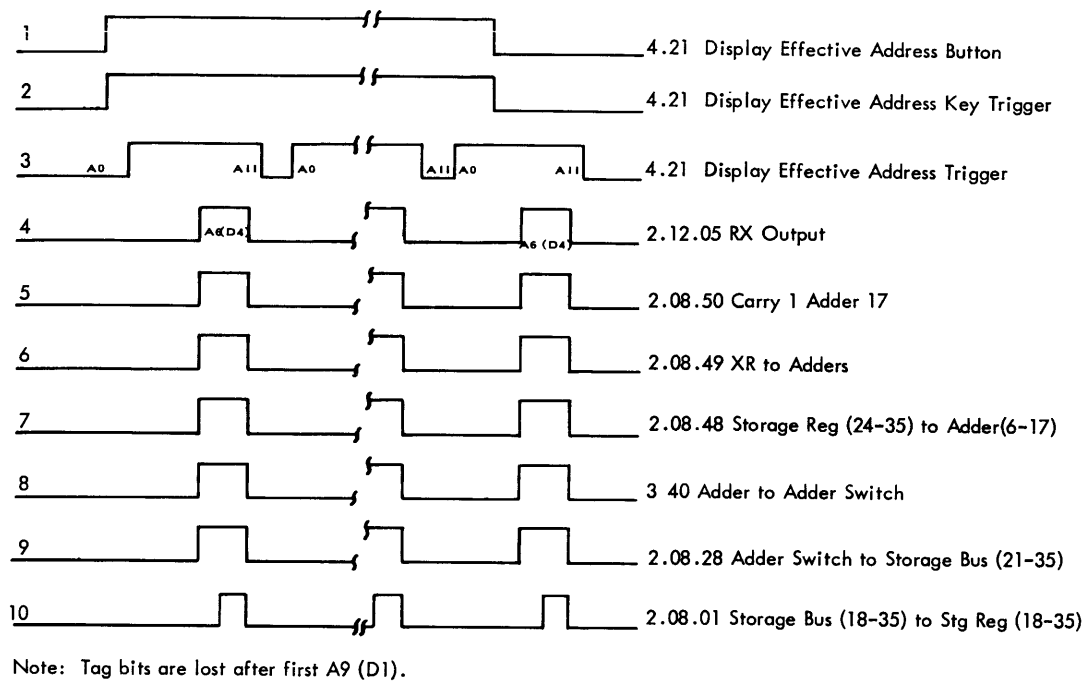


FIGURE 73-2. DISPLAY EFFECTIVE ADDRESS

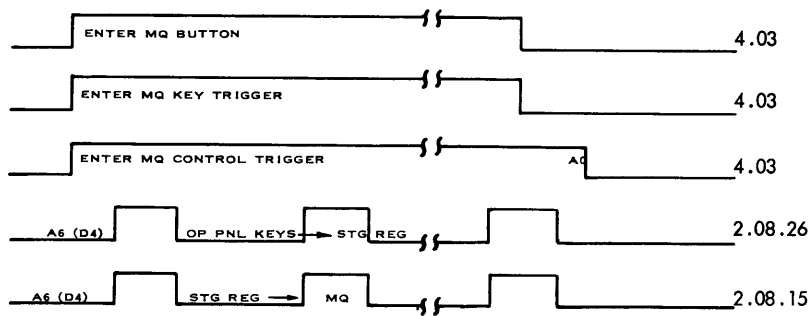


FIGURE 73-3. ENTER MQ

