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IBM 4331 Processor Functional Characteristics and Processor Complex Configurator





This major revision of <u>IBM 4331 Processor Functional</u> <u>Characteristics and Processor Complex Configurator</u> obsoletes the second edition, GA33-1526-1. Information is added on the 4331 Processor Model Group 2 and on new DASD compatibility features. Other sections of the manual have been brought up to date.

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Preface

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The characteristics of the IBM 4331 Processors with their I/O adapters, standard channels and data communication facilities are described in this publication for the use of sytem analysts and programmers.

The reader is assumed to have a working knowledge of the <u>IBM 4300 Processors Principles of Operation for ECPS:VSE</u> <u>Mode</u>, Order No. GA22-7070, and the <u>IBM System/370</u> <u>Principles of Operation</u>, GA22-7000, and to have had programming experience with System/360, System/370, or other 4300 Processors.

Note: The term "principles of operation manuals" used in this publication refers to the two manuals listed above.

The main chapters of the manual cover:

- Introduction to the 4331 Processor
- 1/0 and data communication characteristics
- Model-dependent information
- Compatibility features

Appendixes present a calculation of available processor storage, machine instruction timings, definitions of the abbreviations and special terms, and code tables for the communications adapter.

Prerequisite Reading

IBM 4300 Processors Summary and Input/Output & Data Communications Configurator, GA33-1523

Associated Publications

<u>IBM 4300 Processors Installation Manual-Physical Planning</u>, <u>GA24-3667</u> <u>IBM 4331 Operating Procedures and Problem Determination</u> <u>Guide, GA33-1525</u> <u>IBM 4331 Processor Channel Characteristics, GA33-1527</u> <u>IBM 4331 Processor Compatibility Features GA33-1528</u> <u>IBM 3270 Information Display System</u> <u>Component Description, GA27-2749</u> <u>IBM 3289 Model 4 Printer Component Description and</u> <u>Operator's Guide, GA27-3159</u> <u>IBM 3262 Printer Models 1 and 11 Component Description</u>, <u>GA24-3733</u>

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> IBM 8809 Magnetic Tape Unit Introduction, GA26-1659 IBM 3310 Direct Access Storage Reference Manual, GA26-1660 IBM 5424 and 5425 Multifunction Card Units Operator's Guide and Programmer's Reference Manual, GA21-9167 IBM 4331 Processor: DASD Adapter for 3370 Direct Access Storage: Reference Manual, GA33-1539 IBM 3540 Diskette Input/Output Unit Operator's Guide and Programmer's Reference, GA21-9197 IBM 4331 Processor Loop Adapter Functional Characteristics GA33-1534

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Figure 1. IBM 4331 Processor with Input/Output Devices

Chapter 1. Introduction

The IBM 4331 Processor (Figure 1) is a compact general purpose data processor designed to give new standards of performance and simplicity in small-to-medium sized applications. Its concept includes:

- Ease of installation, with minimum disturbance of existing input/output (1/0) configurations.
- Reduced processor time on certain frequently-used functions, provided in ECPS:VSE mode.
- Selectable System/370 mode.
- Compatibility features for easy transfer from System 3, System/360, System 370, 1401/1440/1460-Series, and from existing to new DASD.
- I/O adapters for direct connection of teleprocessing lines and selected input/output devices.
- Standard channels for 4300, System/360 and System/370 input/output devices.
- DASD adapter and magnetic tape unit adapter.
- Multiuse communications loop adapter.
- Internal processing speed reaching 200,000 machine instructions per second (Model Group 1) and 420,000 machine instructions per second (Model Group 2).

Relationship to System/370

The 4300 Processors are a further development of the System/370. The non-privileged instructions in the two systems are identical. The main difference in the 4331 is the simplified dynamic address translation (one-level address translation) which uses only one table to generate an address from a storage of up to 16,777,216 bytes.

A further simplification in the 4331 processors is that storage addresses for 1/0 operations are also handled by the address translation. This concept of address translation is supported under DOS/VSE by new privileged instructions which allow the storage blocks to be controlled with less overhead. This mode of operation is called ECPS:VSE mode.

The more complex dynamic address translation of the System/370, which allows multiple virtual storages to be created, is available in the 4331 Processors at the selection of the operator. This mode of operation is called System/370 mode.

Compatibility

Any program written for the 4300 Processors operates on a 4331 provided that it:

- 1. Is not time-dependent.
- 2. Does not depend on system facilities (such as storage capacity, 1/0 equipment, or optional features) being present when the facilities are not included in the configuration.
- 3. Does not depend on system facilities being absent when the facilities are included in the 4331. For example, the program must not depend on interruptions being caused by operation codes not installed in some processors but installed in the 4331.
- Does not depend on results or functions that are defined in the principles of operation manuals (see 'Preface') to be unpredictable or processor-dependent.
- 5. Does not depend on results or functions that are defined in this publication to be deviations from the principles of operation. See the chapter entitled ''Model-dependent Information'' for a description of the deviations.

Any program written for System/370 or System/360 operates on a 4331 in the System/370 mode, provided that the program follows the preceding rules and, if written for System/360, does not depend on functions that differ between System/360 and System/370.

For more details about compatibility, see the <u>IBM 4300</u> <u>Processors</u> <u>Principles</u> of <u>Operation</u> for <u>ECPS:VSE</u> Mode, GA22-7070.

Programming Support

The 4331 runs under the following operating systems:

- DOS
- DOS/VS
- DOS/VSE
- 0S/VS1
- VM/370

Please refer to your IBM representative for the appropriate release numbers. The one-level addressing described above

is supported only in ECPS:VSE mode. More information on programming support is given in programming publications.

Processor Configuration and Features

The processor configuration and features are shown in the final chapter of this manual, ''4331 Processor Complex Configurator''. For details of local and remote I/O configurations see IBM 4300 Processors Summary and Input/Output & Data Communications Configurator, GA33-1523.

Maintenance Concept

The maintenance of the 4331 Processor is based on reference codes displayed on the operator's console and logged on the system diskette for later retrieval by the service representative. Each reference code leads the service representative to a specific procedure for replacing a failing unit. The reference code is automatically generated from the failure symptoms developing in the machine.

Remote Support Facility

This facility (with customer authorization) permits the 4331 to be controlled from a remote IBM site and gives the on-site service representative access to the latest service aids and information.

With this mode, the IBM remote support representative can perform online diagnosis as though he were at the customer's site. Logout data stored on the system diskette can be saved during the data link operation for offline analysis. Microcode patches may also be applied remotely.

The remote connection is supplied by the customer. For details of the customers's responsibilities, see <u>IBM 4300</u> <u>Processors</u> <u>Installation</u> <u>Manual-Physical</u> <u>Planning</u>, GA24-3667.

The operator's console is used as a control monitor to check the content of data to be transmitted. A line disconnect key is provided for the customer to stop data transmission immediately.

1-4 4331 Functional Characteristics

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2. System Structure

The central element of the 4331 (Figures 2 and 3) is a processor that communicates internally with a basic storage module (BSM) and an integrated channel. Model Group 1 has an integrated channel connected by a bus-system designed for a maximum of seven internal input/ouput adapters.



Figure 2. Simplified Processor Data Flow (4331-1)

Model Group 2 has an extended integrated channel connected by two bus systems designed for a maximum of eight internal input/output adapters. The number of adapters installed depends on the processor configuration. Each adapter controls a subsystem, provides an interface, or satisfies the demands for input/output placed on a modern data processing system.



Figure 3. Simplified Processor Data Flow (4331-2)

Machine Summary

The basic characteristics of the 4331 are:

BSM size BSM type BSM refresh rate BSM refresh duration BSM access width BSM read cycle BSM write cycle Data flow width Instruction buffer Translation look-aside buffer High-speed buffer storage RCS size RCS type RCS refresh rate RCS refresh duration Control buffer size Control buffer access time Control word size Read-only store Number of standard channels Speed of byte MPX (byte/burst) Speed of block MPX Speed of high-speed block MPX Number of internal I/O adapters 7 (maximum) Service subsystem 1

Model Group 1 0.5 or 1.0 megabytes Single-cell 11.2 usec 1.0 usec 4 bytes 0.9 usec(4 bytes) 1.3 usec (4 bytes) 4 bytes 16 bytes 2-way, 32 entries None 64 or 128 kilobytes Dual cell 50 usec 400 nanosec 64 bytes 100 nanosec 4 bytes None 2 (maximum) 18/500 kilobytes/sec 0.5 megabytes/sec Not applicable

Model Group 2 1,2,3 or 4 megabytes Single-cell 19.2 usec 1.0 usec 16x4 bytes 2.6 usec (64 bytes) 3.1 usec (64 bytes) 4 bytes None 2-way, 32 entries 8 kilobytes 128 kilobytes Dual cell 50 usec 400 nanosec 64 bytes 100 nanosec 4 bytes 12 kilobytes 4 (maximum) 18/500 kilobytes/sec 1.25 megabytes/sec 1.86 megabytes/sec 8 (maximum)

BSM = Basic storage module IC = Integrated Channel RCS = Reloadable control storage MPX = Multiplexer

Storage

The storage (Figure 4) consists of up to 16,777,216 bytes, of which 0.5 to four megabytes, depending on the 4331 model, are processor storage (see configurator in chapter 10). The processor storage is a basic storage module (BSM) that is part of the processor and is controlled by it. There is no separate storage control unit. In Model Group 1, bytes of information are fetched in groups of 4, 16, or 32, and stored in groups of 4, as determined by the processor microcode. In Model Group 2, the bytes are fetched in groups of 64 into a high-speed buffer storage

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(see following description) and are also stored from this buffer in groups of 64. The BSM communicates with the processor over a 4-byte bus used for transferring commands, addresses, and data in both directions.

Depending on the feature configuration, part of the BSM is occupied by microcode and is therefore not available to the user. See the description of microcode under "Processor" in this chapter.



Figure 4. Storage Concept

Storage Features

The BSM has single-bit error correction within four bytes (Model Group 1) or within eight bytes (Model Group 2), and double-bit error detection.

High-speed Buffer Storage (Model Group 2 Only)

The Model Group 2 has eight kilobytes of high-speed buffer storage between the BSM and the processor. This buffer storage accelerates the traffic to and from the processor and compensates for the relatively slow access of the BSM. To the processor, the high-speed buffer storage is the location from which all instructions and operands are fetched (at 200 nanoseconds per word). The high-speed buffer is also the location where all results are stored. When the desired information is not found in the buffer storage, the BSM is signaled to supply a further 64 bytes of information. A corresponding group of the 64 least-recently used bytes is then either overwritten (or stored back in the BSM and overwritten) by the incoming bytes. Only data changed during processing is stored back. The processor is microcode-controlled and has a data flow four-bytes wide. Its main elements are shown in Figure 5. The time for executing a microinstruction varies from 200 nanoseconds (Model Group 2) or 300 nanoseconds (Model Group 1) to 1.6 microseconds depending on the complexity of the operation. A microinstruction which addresses processor storage may take up to four microseconds.



Figure 5. Processor, Main Elements

The microcode executes the machine instructions defined in the principles of operation manuals, including input/output instructions and commands. In Model Group 1 up to eight trap levels handle the various logical and input/output tasks according to fixed priorities. The processor operates on a ninth level which has the lowest priority. Model Group 2 has two entries per trap level, giving in effect sixteen levels, plus a seventeenth for the processor.

The microcode resides in a reloadable control storage located in the processor. Model Group 2 has 128 kilobytes of reloadable control storage and Model Group 1 has 64 bytes or 128 kilobytes, depending on the configuration. Model Group 2 contains additional microcode in a read-only storage. The microcode is loaded from the system diskette at IML. None of the reloadable control storage is available to the user. Microcode that exceeds the limit of this storage is located in a protected area of processor storage. This code is mainly for handling machine checks and exceptional conditions; it consists partly of UCWs and other control information which is not constantly used. When required, the code is fetched by an automatic mechanism. The processor storage reserved for microcode depends on the system configuration. To determine the processor storage available to the user, see Appendix 'A'.

When microcode from reloadable control storage is to be used, sixteen microwords at a time are read into a buffer to counteract the effect of access delay. When microcode from processor storage is to be used, eight microwords (Model Group 1) or four microwords (Model Group 2) are read at a time into the same buffer. An address compare network determines if the code needed is in the buffer, in the reloadable control storage, or in the processor storage. The microinstruction addresses are then routed accordingly.

The processor hardware consists of a fullword (4-byte) arithmetic and logic unit, a fullword shift unit, two kilobytes of local storage, an additional 128-byte local store (Model Group 2 only), and hardware for address decoding, floating-point acceleration, and condition code generation. The local storage provides space for the work registers needed for addressing and accumulating the results of operations. It also holds the general registers, floating point registers, control registers, and most of the UCWs for the transfer of channel data. The additional local store in Model Group 2 contains a duplicate of the general purpose registers. Duplication allows two register operands to be fetched simultaneously, thus saving an access cycle and increasing the speed of processing.

The processor converts instruction and operand addresses to addresses in processor storage before processing. The

conversion is done through a table in a protected area of processor storage. To avoid using this table for every reference, the processor keeps a copy in a translation look-aside buffer (TLB). The TLB holds the virtual addresses and corresponding BSM addresses equivalent to 64 pages (a total of 128 kilobytes), and is capable of rapid conversion. When an address that is not stored in the TLB is referenced, a microcode trap occurs and the TLB is updated. Information passing to or from BSM is adjusted by aligners which compensate for the fixed access width of four bytes.

IBM 3278 Model 2A Display Console

The 3278-2A Display Console (Figure 6) is an input/output device used for communication between the system and the operator. It consists of a keyboard, a display and a control panel. Operator commands and console messages allow interaction between the operator, the operating system, and the processor hardware. For instance, the operator may receive a message from the operating system that an input/output device needs attention.



Figure 6. 3278 Model 2A Display Console

Or the operator can have access to the processor hardware. For example, the operator may display assigned processor storage locations or general registers, or set up diagnostic operations such as instruction stepping. The three parts of the operator console: display, control panel, and keyboard, are described in the following text. The POWER ON switch, located on the right-hand side of the processor, is also described. Procedures for the operator are given in <u>Operator's Library</u>: <u>IBM 4331 Processor</u> <u>Operating Procedures and Problem Determination Guide</u>, GA33-1525.

Control Panel

The control panel (Figure 7) is used for basic operations such as powering down, loading microcode, and indicating modes of machine operation. The panel consists of three keys and five lamps.



Figure 7. Operator's Control Panel

BASIC CHECK Lamp

The red BASIC CHECK lamp turns on when a failure requiring attention by service personnel occurs. BASIC CHECK is also on when the processor is set to service mode.

SYS Lamp

The green SYS (system) lamp is on when instructions are being processed. Pressing this button while power is on starts an IML sequence.

WAIT Lamp

The amber WAIT lamp is on when the wait bit in the current PSW is set. The processor waits for an interruption.

POWER IN PROCESS Lamp

The amber POWER IN PROCESS Light indicates that a power-on or power-off sequence is in progress.

POWER COMPLETE Lamp

The green POWER COMPLETE light goes on when the power-on sequence is complete.

IML Key

Pressing this key while power is on starts an initial microcode load (IML) sequence.

LAMP TEST Key

When the LAMP TEST key is pressed, the lights of the control panel go on, and so do the lights of the 5424 (if installed). The lights go out when the key is released.

POWER OFF Key

When POWER OFF is pressed, the power-off sequence is started. The contents of the storages are not preserved when power is off. Power-off is completed in 5 - 7 seconds. POWER OFF should not be pressed until all jobs are completed and the processor is in the wait state. Pressing POWER OFF then causes the usage and error counters in the DASD adapter to be saved before the processor shuts down.

POWER ON SWITCH

The red power-on toggle switch is located on the right-hand side of the processor. When power is switched on, the ON/OFF switch on the 3278-2A display must be in the 'on' position. The NORMAL/TEST switch of the display must be at 'Normal', otherwise the 3278-2A is not available.

Keyboard

The keyboard (Figure 8) is used by the operator for entering commands, data, and parameters into the system, and for selecting modes of operation. It is also used by service personnel when running tests.



Function is only active when ALT key is pressed at the same time

Typomatic key



The keyboard has 48 alphameric keys, five cursor keys, a backspace key, a tabulator key, 22 function keys, and a space bar. Each key allows up to three EBCDIC codes to be entered depending on whether it is pressed alone, with the shift key, or with the ALT (alternate) key.

The main function keys are:

Change Display Key

Pressing the CHG DPLY key causes the screen display to switch from one display buffer to the other display buffer. If the screen was displaying the system message buffer, it now displays the manual operations buffer, and vice versa. Cancel Key

The CNCL key has the effect of:

- Clearing data keyed into the display buffer
- Returning control to the operating system after manual operations
- Recording a log on the system diskette when 'log pending' is on the console.

Erase Input Key

Pressing the ERASE INPUT key erases all input fields on the screen. The cursor moves to the first character location

Interrupt Key

Pressing the INTR key generates a request for an external interruption. The line disconnect (LINE DISC) function of this key is for service personnel only. available for entering data.

Tabulator Key

The cursor moves right to the first unprotected character position. If held down it traverses all first character positions of unprotected fields in a left-to-right, top-to-bottom direction. Finally it returns to the leftmost character position of the topmost unprotected field.

Erase to End of Field Key

Pressing the ERASE EOF key erases character positions in the input field in which the cursor is located. All character positions from the cursor location to the end of the field (or the end of the line, if this is detected first) are erased. The cursor does not move. The SPM/O function of this key is for service personnel only.

Request Key

When the 1052 command set is active, pressing the REQ key causes an attention interruption and the keyboard is unlocked if the operating system honors the request. When the 3270 command set is active, the DOS attention routine is called. The communication request (COMM REQ) function of the key is for service personnel only. Lock Key

Pressing the lock key locks the keyboard in upper case. The keyboard returns to lower case when one of the shift keys is pressed.

Mode Select and Diagnostic Key

Pressing the MODE SEL DIAG key brings the list of manual operations for the user to the screen. Manual operations are performed by manual selection without the aid of a program. They include alter/display of storage or registers, address compare operations, instruction stepping, and other operations for debugging and reconfiguring.

Alternatively, the MODE SEL DIAG key, pressed while the ALT key is held down, calls up the Diagnostic Mode Select display. This display is used for maintenance.

Copy Key

When the copy key is pressed during manual operations and a console printer is attached, the screen display is copied. If the copy key is pressed with the ALT key held down, a console test is invoked.

Shift Keys

There are two shift keys, one on each side of the keyboard. Pressing a shift key causes the upper character of a two-character key or the upper case of an alphabetic character to be entered.

Reset Key

The RESET key is used to free the keyboard when it is inhibited.

Backspace Key

The cursor moves right to left and line by line upwards. Finally it returns to the bottom right-hand corner of the screen and repeats the same path. The cursor-to-left key performs the same function as the backspace key. Start Key

When the START key is pressed and the 'MAN' indicator is on, the processor begins to carry out instructions.

Stop Key

When the STOP key is pressed, the processor completes execution of the current instruction and stops after any waiting interruptions have been serviced.

Back Tabulator Key

The current position of the cursor affects the operation of the back tabulator key. When the cursor is in an input field at a location other than the first character location, the back tabulator key repositions it to the first character position in the field. When the cursor is in a protected field, or at the first character position of the input field, the back tabulator key repositions it to the first character position of the first input to the left of the present field.

Using this key together with the ALT key repositions the cursor to the home position, that is to the first unprotected position of the display.

Insertion Mode Key

Pressing the insertion mode key creates a space in a string of characacters on the screen for another character to be inserted.

Delete Key

When the delete key is pressed, the character underlined by the cursor is deleted from the screen and any characters to the right close up.

Cursor-to-New-Line Key

The cursor moves to the first unprotected character position in the next lower line, which offers such a position traversing all protected lines between.

Cursor-Up Key

The cursor moves upward in the same character column. Finally it returns to the bottom of the screen and repeats the same path upwards if the key is held down. The PAGE UP function of this key (cursor-up pressed with ALT) allows you to display the next higher storage section in ascending order when a storage display is on the screen.

Cursor-Down Key

The cursor moves downward in the same character column. Finally it returns to the top of the screen and repeats the same path downwards if the key is held down. The PAGE DOWN function of this key (cursor-down pressed with ALT) allows you to display the next lower storage section in descending order when a storage display is on the screen.

Cursor-to-Left Key

The cursor moves right to left and line by line upwards if the key is held down. Finally it returns to the bottom right-hand corner of the screen and repeats the same path. The backspace key performs the same function as the cursor-to left key.

Cursor-to-Right Key

The cursor moves left to right and line by line downward if the key is held down. Finally it returns to the top left hand corner of the screen and repeats the same path.

Alternate Key

Pressing the ALT key allows the second function of two-function keys to be selected. The second function (if any) is shown at the base of a key.

Enter Key

When ENTER is pressed, an attention interruption is sent to the operating system, which causes the data typed into a display to be read. **Display Screen**

The display screen allows visual communication between the operator and the system. It is used by the operating system to pass messages to the operator, to present operating modes for selection and further definition, and to display information accessed or entered at the keyboard. Lines 21-25 provide a permanent display of the machine status.

Pressing the mode selection key breaks any chain of messages being written on the screen and invokes a menu that allows the operator to choose from the following modes:

Mode Selection Address Compare Check Control Display/Alter Capacity Counts **Control Registers** Current PSW Floating-Point Regs General Registers Storage Key Main Storage Main Storage Real Main Storage Virtual Page Description Page down Page up Main Storage Size Communication Lines Instruction Step Interval Timer Machine Save Native Displays and Printers Program Load (IPL) * Restart Clear Reset **Reset Instruction Step** Program Reset Store Status TOD Enable User Diskette Control Diskette Device Address

*Includes selections for compatibility features

System Operation

As a prerequisite for system operation the operator presses the power-on switch at the right-hand side of the processor. After the power sequence is completed, the microcode is automatically loaded from the system diskette and a system clear reset is performed. The clear reset initializes the program registers and all main storage to the values specified in the principles of operations manuals. The IPL picture appears on the operator console. After the operator has performed IPL the processor begins to execute programs, or, if the loader program is so designed, the operator is requested to press START.

Program execution follows the rules laid down in the appropriate principles of operation manuals.

<u>Note</u>: Unless otherwise stated, the descriptions in this manual generally refer to the ECPS:VSE mode of operation described in <u>IBM 4300 Processors</u> <u>Principles</u> of <u>Operation</u> for ECPS:VSE Mode, GA22-7070.

During operation, processor storage is always addressed by a 24-bit address designating one of the 16,777,216 byte locations.

All bytes that are not directly accessible at a given time are stored on external disk-files by the operating system. The storage addresses never refer directly to processor storage but are translated automatically by translation tables in an internal storage not accessible to the program. To speed up operation, the processor keeps a copy of this table in a translation look-aside buffer (TLB) which is an associative array with 64 entries. The array holds the corresponding real addresses for up to 64 pages (128K bytes). Referencing a page which is not in the TLB causes the TLB to be updated.

Interruptions of six different classes (machine check, supervisor call, program, external, input/output, and restart) can occur during operation. An interruption consists of storing the current PSW as the old PSW, storing a code identifying the cause of the interruption, and fetching a new PSW. Processing is resumed according to the new PSW. The interruptions to the 4300 Processors in ECPS:VSE mode vary slightly to those of the System/370. The differences mainly concern storage access exception. The System/370 concept of imprecise interruptions does not apply and has been deleted. Certain exceptional conditions no longer occur or are simplified because of the deletion of multiprocessing. Machine-check handling has been redefined to eliminate the model dependencies found in machine-check handling in the System/370.

Chapter 3. I/O Adapter Characteristics

Integrated Channel

To handle data transfer between the 1/0 adapters and processor storage an integrated channel (1C) system is provided. The IC system (Figures 9 and 10) consists of a data mover (hardware register and buffers), the processor access facilities to processor storage, an IC bus or buses connecting the 1/0 adapters, and the microcode to control the hardware.



Figure 9. Integrated Channel, 4331-1

Model Group 1 has a data mover which accesses processor storage in units of four bytes and serves one IC bus connecting up to six I/O adapters. The data mover in Model Group 2 accesses buffer storage or processor storage in units of 64 bytes and serves two IC buses connecting a maximum of eight I/O adapters. A 64-byte buffer is assigned to each I/O adapter. During IC operation, the processing ability of the processor is briefly seized for the tasks of transferring data and updating data addresses and the byte count. This updating service is known as cycle stealing.



Figure 10. Integrated Channel, 4331-2

The IC interconnects the I/O adapters by one or two ring-bus systems described as IC buses.

The adapters collect data from the 1/0 devices under their control and send it in blocks over an IC-bus. The adapters also request data from the IC in blocks for transfer to the 1/0 devices.

The tasks of the IC are to:

- Select the appropriate adapter
- Transfer command codes
- Handle subsequent data transfer requests.

This handling includes tasks for which help is needed from the processor, such as:

- Updating data addresses through unit control words (UCWs)
- Controlling length counts
- Observing CCW flags
- Conducting command and data chaining
- Handling 1/0 interruptions at termination

IC activity is initiated by 1/0 instructions (which address a specific device) and associated channel command words (which specify the operation to be performed). After an 1/0 instruction has been given, microroutines set up UCWs and notify the adapters that cycle-steal requests may be raised. Processing cycles and storage-cycles are stolen from the processor as they are needed.

If several adapters raise requests at the same time, the IC can transfer data from the various sources over the IC-bus in multiplex mode. The adapters are serviced in order of priority.

Input/Output Adapters

The task of converting the information on the IC-bus into a form acceptable by the I/O devices (and vice versa) is performed by I/O adapters. The adapters have an interface of common design at their point of connection to the IC-bus, but each adapter presents a special interface to the I/O subsystem that it serves. The following I/O adapters are available on the 4331 Processor:

- Support subsystem adapter (for operator's console, workstations, terminal printers, diskette drive, line printers, and service support)
- I/O subsystem adapter (for 5424 Multi-function Card Unit or multiuse communications loop).
- Communications adapter (for remote terminals and systems)
- DASD adapters (for direct access storage devices)
- 8809 Magnetic Tape Unit adapter (for magnetic tape units)
- Standard channel adapters (for byte multiplexer channel, and block multiplexer channels)
- Special adapter (Model Group 2 only) for high-speed block multiplexer channel

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Channel and Device Addresses

Channel 0 Addresses

Channel 0 is provided on Model Group 1 and Model Group 2 to address the byte multiplexer, the communications adapter, and the direct attachments for the display console, keyboard/displays, terminal printers, line printers, multi-function card unit or loop terminals, and diskette drive. Channel 0 has the following address range:

4331	Model	Group	1
------	-------	-------	---

	Range	Available for
-	09-1F	24 nonshared subchannels for the display console, keyboard displays, terminal printers, line printers, and diskette drives (see Note).
	30-37, 3B	Up to eight data communication lines (CA- attached), plus line address 3B for the trace facility.
	40-7E 4C	Loop terminals. Address 40 is shared by all non-SNA terminals (except 3644). Each SNA terminal and each 3644 terminal requires its own address (subchannel). The maximum number of terminals is 80. 5424 Multi-function Card Unit.
	24-3D, 3F	27 nonshared subchannels on the byte multiplexer channel. (See address restrictions.)
	80-BF	4 shared subchannels (providing 16 addresses each) on the byte multiplexer channel.
		ce addresses for the 3278-2A Display (ached keyboard displays, terminal prin

Note: The device addresses for the 3278-2A Display Console, the direct-attached keyboard displays, terminal printers, user diskette, line printers and loop terminals can be assigned at the operator console. The channel address (channel 0) is fixed.

Address Restrictions.

The following addresses are not available on the 4331-1 in the given circumstances:

Not available Circumstances

3D	When a block multiplexer channel is installed.

3C and 38 When the DASD adapter is installed.

3A and 39 When the 8809 Magnetic Tape Unit adapter is installed.

30-37, 3B These 9 nonshared subchannel addresses of the byte multiplexer channel overlap with the maximum of 8 data communication lines (plus trace facility) of the same addresses (30-37, 3B). Depending on the number of data communication lines installed, the corresponding number of MPX subchannels (and their addresses) are not available. The trace feature address (3B) is available when any data communication line is installed.
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4331 Model Group 2

Range	Available for
09-1F	24 nonshared subchannels for the display console, keyboard displays, terminals printers, line printers, and diskette drive. See restrictions below.
30-37, 3B	Up to eight data communication lines plus trace feature.
40	5424 Multi-function Card Unit.
40-7E	Loop terminals. Address 40 is shared by all non-SNA terminals (except 3644). Each SNA terminal and each 3644 terminal requires its own address (subchannel). The maximum number of terminals is 80.
20-3F	32 nonshared subchannels on the byte multiplexer channel. Subchannels 2A-2E are fast (see Note).
80-BF	4 shared subchannels (providing 16 addresses each) on the byte multiplexer channel. 80-BF are all fast subchannels (see Note).
and the second	

Address Restrictions:

Each communication line on the 4331-2 takes one nonshared subchannel address from the byte multiplexer (in the address range 30-37 and 3B).

Note:

Fast subchannels are permanently available and may therefore sustain higher data rates in byte mode than other subchannels. Channel 1 is a block multiplexer channel on Model Group 1 and Model Group 2 with the following address range:

Range	Assigned to			
00-7F	Up to 128 nonshared subchannels			
80-FF	Up to 16 shared subchannels			

The block multiplexer channel is configured by means of a selection menu at installation time. Up to 128 nonshared subchannels, together with their addresses, can then be specified. The number of shared subchannels, and the number of addresses assigned to each shared subchannel, up to a total of 128 addresses, is also specified.

Special 2311/2314 Restriction (4331-1 only)

When a 2311/2314 is connected to the block multiplexer the following devices cannot be connected:

- 3340/3344 disks
- 3370 disks
- 8809 magnetic tapes
- High speed data communications line (above 9,600 bps).
- Any magnetic tape on the byte multiplexer channel.

These devices would overrun because of the high trap priority assigned to the block multiplexer when 2311/2314 disks are attached.

Note:

Only channel 1 provides the means to connect 2311 or 2314 disks. Such devices must use a shared subchannel in 2311/2314 mode which includes selector mode.

Special 2311/2314 Restriction (4331-2 only)

When a 2311 or 2314 is connected to a correctly configured block multiplexer, the following devices cannot be connected:

- High-speed data communications line (above 9,600 bps)

- High-speed channel

Channel 2 addresses

Channel 2 is a DASD adapter for 3310, 3370, and 3340/3344 direct access storage. It has the following address range which can be assigned by menu selection.

4331 Model Groups 1 and 2

Range	Assigned to
00-07	Up to 32 nonshared subchannels for physical
10-17	disk drives (see "Addressing Restrictions
20-27	for DASD" in the following text).
30-37	
40-47	
50-57	
60-67	
70-77	
80-FF	Emulated disk devices (see <u>IBM</u> <u>4331 Processor Compatibility</u>

Addressing Restrictions for DASD

- Up to four strings can be installed at any one of the eight string address locations shown above.

Features, GA33-1528).

- Not more than two of these four strings may be 3340s or 3340/3344s, the others may be 3310s or 3370s in any combination.
- If no 3340/3344s are installed, all four strings may be 3310s or 3370s in any combination, but types cannot be mixed within a string.
- 3340 or 3340/44 strings must have an address that begins with 0 or 1, for example:

AddressesAssigned to (Device Type)00-073340 or 3340/3344 string (first)10-173340 or 3340/3344 string (second)

A full 3340/3344 installation can have, for example, the following addresses:

	3340-A2		3340-B2		3340-B2		3340-B2	
String 0	X00	X01	X02	XO3	X04	XO5	X06	X07
String 1	X10 	X11	X12 	X13 	X14 	X15	X16 	X17
			33	44-B2	334	4-B2	334	4-B2
	String	0	X02 X2A X4A X6A	XO3 X2B X4B X6B	X04 X2C X4C X6C	XO5 X2D X4D X6D	X06 X2E X4E X6E	X07 X2F X4F X6F
	String	1	X12 X3A X5A X7A	X13 X3B X5B X7B	X14 X3C X5C X7C	X15 X3D X5D X7D	X16 X3E X5E X7E	X17 X3F X5F X7F

Note: X is the channel number

Channel 3 Addresses

Channel 3 provides the following address range for the 8809 tape drives:

4331 Model Groups 1 and 2

Range	Assi	igned	to

00-05

6 nonshared subchannels

<u>Note</u>: The control unit address portion delivered by 1/0instructions must be zero. The device address portion may range from 0 to 5. The 8809 knows only one type of address, the "8809 controller address". This address is set up in each drive during installation with three address switches which have the binary values 4, 2, and 1.

The following rules apply to the setting of the 8809 controller (i.e. device) addresses: - The addresses must be contiguous in ascending order without gaps. For example: 0, 1, 2, 3, etc. Up to six tape drives may be connected.

- The first tape drive in the installation must have device address 0. The highest address is 5.

Channel 4 (4331-2 Only)

Channel 4 is a second block multiplexer which consists of a standard channel adapter with a standard 1/0 interface. Channel 4 operates at a speed of 1.25 megabytes per second, except when the high-speed channel (channel 6) is installed in which case the block multiplexer speed is reduced to 625 kilobytes per second. Channel 4 can be configured with up to 128 nonshared subchannels plus up to 16 shared subchannels. Channel 4 is exclusive with channel 3.

Channel 5 (4331-2 Only)

Channel 5 is a DASD adapter exclusive with channel 6.

Channel 6 (4331-2 Only)

Channel 6 is the high-speed byte multiplexer channel operating at an average speed of 1.86 megabytes per second, and providing a standard interface implemented by a special hardware attachment. The high-speed channel is specially suited for the connection of high-speed disk storages. Channel 6 is exclusive with channel 5 and channel 3.

Support Subsystem

The standard support subsystem operates under the control of support processor 1 to provide initialization, monitoring, system control, maintenance, and servicing for the 4331 Processors. Three adapters, an interface, and a logic element (Figure 11), communicate with console 1/0 devices and other elements of the system to provide microcode-loading, messenger, and routine checking facilities. Support processor 1 also controls direct-attached line printers. The support subsystem is connected both to the IC-bus and to the support bus. The various elements of the subsystem are: <u>Support Processor 1</u>: A microcode driven processor that controls:

- System diskette drive
- Diskette drive for input/output in 3540 mode
- Display/printer adapter
- Support bus adapter
- Power control interface





<u>System Diskette Drive</u>: A diskette drive used for loading microcode into the processor. The diskette also contains storage areas for in-line tests, error logs and analysis data. The system diskette is not accessible to the user.

Diskette Drive: A drive, similar to the system diskette drive, available as a user-accessible 1/0 device. The drive has characteristics similar to those described in <u>IBM 3540</u> Diskette <u>Input/Output Unit Operator's Guide and</u> Programmer's Reference, GA21-9197. See the chapter "Diskette Drive" in this manual. One-sided diskettes with 128 bytes per record can be used.

<u>Note</u>: Diskettes provide for ease of media handling and storage. It should be recognized, however, that during recording and reading, the read/write head is in contact with the media causing wear in time. Care in storage, use, and handling can also affect diskette life. (See guidelines in IBM Diskette - General Information Manual, GA21-9192.)

<u>Display/Printer Adapter</u>: An adapter that controls the operator console (consisting of a video display and keyboard), and up to fifteen devices. The devices can include 3289-4 and/or 3262-1 or -11 line printers, 3287-1 or -2 terminal printers, and a string of 3278-2 display stations.

Support Bus Adapter and Support Bus: A link connecting the support subsystem to the processor (with the BSM and the IC) and to support processor 2. The adapter serializes and deserializes information so that it can pass between the halfword processor bus (see Figures 2 and 3) and the serial-bit support bus.

The link enables the support subsystem to monitor the processor hardware and to review the status of various elements of the 4331 Processor by sensing and setting latches, or reading and writing storage locations or registers.

<u>Power</u> <u>Control</u> <u>Interface</u>: A facility that allows the support processor to perform power-on and power-off sequences and to monitor voltage levels. Page of GA33 - 1526 - 2 Revised September 15, 1980 by TNL GN33 - 1733

I/O Subsystem

The I/O subsystem (Figure 12) provides an adapter for controlling a 5424 Multi-function Card Unit.



Figure 12. I/O Subsystem

From the user's viewpoint, the subsystem is part of the byte multiplexer channel, the attachment performing the tasks of the conventional channel interface and control unit. The subsystem consists of:

<u>Support</u> <u>Processor</u> <u>2</u>: A standard microprogram-controlled processor, identical to the support processor 1.

5424 Adapter: An adapter for controlling a 5424 Multi-function Card Unit. The 5424 adapter cannot be installed if the loop adapter is installed.

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Loop Adapter: An adapter that provides direct attachment for a variety of terminals without the need for a loop controller or communications controller. The loop adapter has all the functions of a controller and supports the following devices:

Terminals

3641 Reporting Terminal, Models 1 and 2 3642 Magnetic Stripe Encoder, Models 1 and 2 3643 Keyboard Display, Models 2, 3, and 4 3644 Automatic Data Unit 3645 Printer 3646 Scanner Control Unit, Model 1 3647 Time and Attendance Terminal 3287 Terminal Printer, Models 11 and 12 8775 Display Terminal, Models 1 and 2

Loop Control Units 3843 Loop Control Unit (for data link)

Control Units

3276 Control Unit Display Station, Models 11-14 3274 Control Unit, Model 51C and 52C

The loop adapter supports up to two directly attached loops and up to two data links. Each directly attached loop can consist of two lobes, formed by ring cables up to 3.0 km (about 2 miles) long. The usable cable length is a function of the selected speed of transmission (9,600 or 38,400 bps on the directly attached loop).

The loop cable is backed by a rerouting facility which corrects certain failures. A failure in one lobe does not affect the other lobe, nor does a failing terminal affect the other terminals on the lobe. The maximum number of terminals supported is 62 per lobe, but no more than 80 can be controlled on the directly attached loops and data links by the loop adapter.

Each of the data link interfaces can attach one remote loop controller as point-to-point, or up to four remote loop controllers as multipoint connection. The transmission speeds on the data link are 2,400, 4,800, or 9,600 bps. Because of the limited capacity of the control storage, not all types of terminals can be configured in one

installation. For example, if the 3642, 3643, 3644, 3645, 3646, 8775, and 3287 are configured together, the 3641 and 3647 must be excluded (see <u>IBM 4331 Processor Loop Adapter</u> <u>Functional Characteristics</u>, GA33-1534). The loop adapter cannot be installed if the 5424 Multi- function Card Unit adapter is installed.

The communications are in SDLC procedure and are supported by ACF/VTAM or ACF/VTAME, together with the appropriate CICS programs.

3-14.2 4331 Functional Characteristics

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DASD Adapters

The DASD adapter (Figure 13) is a specialized attachment for operating disk devices compatible with the control interface (CTLI). Model Group 1 can have one DASD adapter and Model Group 2 can have up to two DASD adapters.



CTLI = Control Interface

Figure 13. DASD Adapter and 8809 Magnetic Tape Unit Adapter

The design of the adapter is determined by the concept of the control interface which does not transfer the command code of a channel command word but transmits sequences of tag signals instead.

A tag sequence, used to communicate with an 1/0 device, consists of a 5-bit control instruction sent over a 5-bit tag bus, and an 8-bit field of data or tag-modifier information. Tag sequences are typically used for device and controller selection, polling, read/write control and status reading. The adapter issues and receives tag sequences over the CTLI, and transfers information on the IC-bus in cycle-steal or sense/control mode. The use of tag sequences frees the adapter from the peculiarities of different 1/0 devices, but for command decoding and the handling of exceptional situations, support comes from the processor microcode.

8809 Magnetic Tape Unit Adapter

The 8809 Magnetic Tape Unit adapter (Figure 13) is a specialized attachment for operating 8809s over the CTLI. The attachment has the same characteristics as the DASD adapter which is briefly described above.

A string of six 8809 drives can be attached to the adapter. This 8809 subsystem provides direct attachment of tape for use as back-up and for data security. The data transfer rate can be programmed for speeds of either 20kb/sec (start/stop mode) or 160 kb/sec (streaming mode). The 8809 adapter is exclusive with the 1401/1440/1460 compatibility feature. For information on the 8809 see <u>IBM</u> <u>8809</u> <u>Magnetic</u> Tape Unit Introduction, GA26-1659.

Note on Programming: Unlike many tape subsystems currently in use, the 8809 raises the channel end bit and the device end bit at the same time. Care should therefore be taken in programming tape rewind operations because the channel remains busy until the rewinding of any tape in a string of 8809s is completed.

Standard Channel Adapter

The standard channel adapter (SCA) provides the basis for multiplexer channels with standard interfaces on the 4331 Processor. Model Group 1 can have up to two SCAs to provide the hardware for a byte multiplexer and a block multiplexer channel. Model Group 2 can have up to three SCAs, allowing a maximum configuration of one byte multiplexer and two block multiplexer channels. The hardware for byte and block multiplexer channels is the same. The functional difference for the two types of channels is provided by microcode. The task of the SCA (Figure 14) is to coordinate the transfer of information over the standard I/O interface under the control of the IC microcode in the processor. Note: The above description does not include the high-speed block multiplexer channel (4331-2 only) which is described under "High-Speed Channel Adapter" in this chapter.

The SCA is connected on the one side to the IC bus and on the other side to the I/O control units over the standard I/O interface. The basic functional units are (1) two 4-byte registers which load and unload alternately, (2) IC interface controls which transfer data and sense bytes in cycle-steal mode, and other information in sense/control mode, (3) standard I/O interface controls which transfer data over the standard interface with the aid of the IC microcode.



- The IC control program gives the SCA the characteristics of either a block multiplexer or a byte multiplexer.
- The IC-bus transmits four bytes per cycle-steal operation.
- During cycle-steal operations, the two halves of the data buffer register are used alternately. While one half is being filled from one interface, the other half is being emptied by the other interface.

Figure 14. Standard Channel Adapter

Byte Multiplexer Channel

The byte multiplexer channel is provided for operating low-speed I/O devices. Its characteristics conform with the definitions in the principles of operation manuals.

The task of the byte multiplexer channel is to interpret I/O instructions, translate them into controls and commands at the I/O interface for operating the I/O devices, transfer data between the devices and the data mover, and control interruptions raised by device requests or by error conditions.

Data Rate.

The byte multiplexer channel operates in interleaved mode at speeds up to 18kb/sec in single byte mode, 36kb/sec in dual byte mode, 62kb/sec in 4-byte mode, and 0.5 megabytes/sec in burst mode.

<u>Note</u>: On the 4331-2 the 18kb/sec in single byte mode can only be sustained on the fast subchannels. The other subchannels have a data rate between 18kb/sec and 9kb/secdepending on the continuity of 1/0 requests.

Subchannels.

A byte multiplexer channel contains up to 31 subchannels in Model 1 and up to 36 subchannels in Model 2. Each subchannel, which can be viewed as a special register, holds the information necessary for controlling the current operation at an 1/0 device. A subchannel may be shared by more than one device or it may be nonshared. A shared subchannel is used for a control unit which serves several 1/0 devices, only one of which needs the subchannel at any one time; a non-shared subchannel is typically used for a control unit serving only one 1/0 device. Some control units which serve several devices require a nonshared subchannel for each device. Of the 31 subchannels available on the byte multiplexer channel of Model 1, the first four can be shared or nonshared, whereas the remaining 27 are nonshared only. Of the 36 subchannels on the byte multiplexer of Model 2, four can be shared. Each shared subchannel provides 16 addresses, thus allowing sharing by 16 devices.

The number of subchannels in the byte multiplexer is reduced by two for the DASD adapter, two for the magnetic tape unit adapter, one for the CA and one for each CA line, and one for the block multiplexer channel. In Model 2, the number of subchannels for the byte multiplexer is reduced by one for the CA and one for each CA line.

Addressing.

The addressing of units on the byte multiplexer channel, and the applicable restrictions, are shown under ''Channel and Device Addressing''. The high-order bit of the address byte (bit 0) shows whether the subchannel is nonshared (bit 0 = 0) or shared (bit 0 = 1), and is ignored for addressing purposes.

A nonshared subchannel is addressed by the seven low-order bits of the address byte.

Operation.

Channel operations are initiated when an 1/0 instruction is detected in the machine program and the SCA is set up for the input/output operation. The device is selected and the initial status is returned over the IC-bus to the processor.

Data Transfer.

During data transfer on the byte multiplexer the following tasks are carried out:

- Aligning data on a fullword boundary
- Controlling cycle steal operations
- Detecting the end of data transfer

Controlling transmission over the IC-bus Data is aligned under the control of a buffer address counter, which holds the three low-order bits of the CCW data address (starting address), and which is updated with each buffer access. The cycle-steal data is handled by the data buffers (see Figure 13), loading and unloading alternately. While one buffer is filled from one interface, another buffer is emptied by the other interface. Transfers over the IC bus to or from SCA are in units of four bytes for each cycle steal operation, either one, two, or all of these bytes being significant, depending on whether single or multiple byte mode has been forced by the control unit. Cycle steal operations are requested by the SCA in single byte mode when the 'operational in' signal drops, and in multiple byte mode either when 'operational in' drops or the data buffers are full or empty. For each request by a control unit, the SCA is set up again so that the buffer address counter is primed for correct byte alignment. Transfers over the standard 1/0 interface (between the channel and the I/O control units) occur one byte at a time.

By successive cycle-steal requests, successive loads from the data buffers (left and right) pass over the IC-bus. The contents of a four-byte data buffer are transferred in two 2-byte shots, the number of significant bytes being signaled to the data mover by two control lines. If a data transfer causes the length count in the data mover to fall below eight bytes, the IC signals an end-condition on the outbound control lines. From then on, the contents of the buffer address counter are continuously compared with the end-address in the op-register. When the two values are equal, no more bytes are accepted from the 1/0 device. After the last fullword has been transferred to the 1C, the SCA signals the number of significant bytes and indicates the end of data transfer.

Block Multiplexer Channel

The block multiplexer channel is provided for relatively high-speed operations in which bursts of data are transferred over the channel. It allows several channel programs for high-speed 1/0 devices to run concurrently on one channel.

A block multiplexer channel is suitable for control units that serve a number of 1/0 devices. It is most effective when the 1/0 devices perform their mechanical and electronic operations independently of the control unit. After channel end has been signaled for one device, the control unit can then be freed for operations with another device, while the first device is still busy with the electro-mechanical part of its operation.

Data Rate.

The data rate on the block multiplexer channel is up to 0.5 megabytes/sec in Model Group 1 and 1.25 megabytes/sec in Model Group 2.

Subchannels.

128 nonshared subchannels, plus 16 shared subchannels for a total of 128 addresses (devices) are provided. The number of subchannels and the address distribution are selected at installation time.

Operation.

Based on the SCA hardware, the block multiplexer channel operates similarly to the byte multiplexer channel except that whole data records are transferred over the channel in bursts. When a fullword transfer reduces the length count in the IC below eight bytes, outbound control lines signal an approaching end-condition to the SCA. From then on, the contents of the buffer address counter are compared with the ending address in the op-register for each further byte transferred from the 1/0 device. A match of these two values prevents further transfer of bytes from the 1/0device. On receipt of the last fullword the end of data transfer is signaled. Any transfer of less than four significant bytes prompts the IC to request a partial store-cycle from the BSM to store the last fragment of data. End-conditions may also be signaled to the IC if the 1/0 device is transferring less bytes than specified in the length count.

High-Speed Channel Adapter (4331-2 Only)

The high-speed channel (HSC) adapter provides the basis for the high-speed block multiplexer channel on the 4331 Model Group 2. The HSC adapter differs in two ways from the SCA. It has twice the number of data buffers (four) and a special tag control logic which handles most control tasks by hardware. Microcode is rarely needed. This design enables the HSC to transfer data at up to 1.86 megabytes/sec and guarantees the fast chaining times required by modern high-speed DASD.

Communications Adapter

The characteristics of the communications adapter are described in a separate chapter in this manual.

Chapter 4. Keyboard/Displays and Terminal Printers

The operator console consists of an IBM 3278 Model 2A Display Console, that is controlled either by the standard 3270 command set, which is the default command set, or by the optional 1052 command set. If both command sets are installed, the desired set can be selected by the operator at initial program loading.

When the 3270 command set is selected, the characteristics of the operator console are that of a 3274 Model 1B Control Unit with a 3278 Model 2 Display attached.

<u>Note</u>: The 3270 commands also apply to the locally attachable 3278-2 Keyboard/Displays and 3287 Terminal Printers.

When the 1052 command set is selected, and a terminal printer is installed, the terminal printer and the display console operate together under a single device address as a 1052 Printer keyboard.

Different graphic sets are available to satisfy national requirements. The graphic sets comprise national characters for the 3278-2, 3278-2A, and 3287, and corresponding markings on the keys. If Katakana is installed, messages from the operating system are displayed in Katakana, but all messages initiated by the microcode or hardware (for example, maintenance displays) are displayed in English.

The following text describes the channel command words, the channel and unit status, and the orders or control characters belonging to each command set.

3270 Commands

The 3270 commands are the standard commands for the 3278 Model 2A Display Console and are automatically in effect when no other command set is selected. For the locally attachable 3278-2 Keyboard/Displays and 3287 Terminal Printers, the 3270 commands are the only commands available. Command Code Command Hex CCW bits: 01234567 01 00000001 Write -00000101 Erase/write 05 00001101 Erase/write alternate OD 0F 00001111 Erase all unprotected 06 00000110 Read modified 00000010 Read buffer 02 04 00000100 Sense E4 11100100 Sense 1/0 00000011 No-operation 03

<u>Note</u>: The 'copy' and 'read modified all' commands are not supported and cause command rejection. The 'select' command has no function but is treated for compatibility as a no-op.

'Write' Command, Hex '01'

A 'write' command places a message onto the screen without erasing or modifying other messages already there. When the 'write' command is issued to a printer, the print buffer is loaded and printing may be ordered immediately or later by means of the 'write control character' (see 'Orders and Control Characters' for details).

The write command causes two actions: a data transfer from processor storage to a 256-byte controller storage area, followed by a translation from EBCDIC into character generator addresses. These addresses are placed into another 256-byte controller storage area for transfer to the display or print buffer.

The transfer to the display buffer is selective because control characters are inspected and acted upon during the transfer.

The data transfer from processor storage begins at the location specified in bits 8-31 of the CCW and continues until either the count (CCW bits 48-63) has been reduced to zero or a 'halt 1/0' or 'halt device' instruction is given, whichever occurs first. The buffer has 1920 character positions, but the write command does not stop at the buffer end if the count is larger. This is because buffer addressing automatically wraps around to the beginning of the buffer and continues until the count is exhausted.

The operator console buffer does not make all character positions available to the write command. The last four lines on the operator console are reserved for the machine status display which is protected by forcing the wrap-around earlier than it would occur on a regular 3278 display unit. However, the remainder of the buffer (all but the last four lines) is available for data transfer by the 'write' command. On the 3278-2 display stations, the entire buffer (including the last four lines) is available for data transfer.

The data transferred consists of message text with interspersed control characters which define the extent of display fields, the location of the fields on the screen, and various other properties of the fields. Specific sequences of control characters are known as 'orders' which constitute subcommands within the basic 'write' command.

Fields may, for example, be declared as displayable (and printable) or as invisible. They can be protected against overwriting by the operator, and they can be designated as modified, in which case, they can be selectively retrieved from the screen by a 'read modified' command and put back into processor storage. The properties of a field are defined by the 'attribute character'. The screen location of a field is defined by the 'buffer address' and a special code is used to identify the buffer address, as otherwise, it would not be detected in the data stream. Other control characters reset the keyboard or sound the alarm. For details, see 'Orders and Control Characters'.

None of the control characters (except attribute characters) are transferred from the controller storage to the display or print buffer. In controller storage the character codes are translated and the control characters are examined. The results of this examination determine where text will be located on the screen, whether text is printed or not, and where the cursor goes. If no cursor position is given, the cursor remains where it is.

Channel end is indicated when the last transfer to the control buffer is completed. Device end follows after the message has been placed into the display buffer, or (in the case of printing) when the mechanical operation is completed.

'Erase/Write' Command, Hex '05'

An 'erase/write' operation erases the entire display or print buffer and places a new message or messages onto the screen (or into the print buffer). The 'erase/write' command causes the entire buffer (except the last four lines on the operator console) to be cleared to null characters, whether fields have been protected or not. Thereafter, the data is transferred from processor storage to the controller storage, and from the controller storage to the buffer until the length count is reduced to zero or a 'halt' instruction is given.

The control characters are examined as they appear in the controller storage and this determines the transfer details. The control characters are not transferred to the buffer (except attribute characters which are not visible). Channel end is indicated when the data transfer to the controller storage is complete. Device end is indicated when the buffer has been loaded or when the mechanical portion of any print operation has been completed.

The video screen (or the printer form if printing was ordered) shows the message or messages, whereby all character positions which have been cleared to nulls and have not been overwritten by new text are empty (dark or blank). If no cursor location has been introduced by the 'erase/write' command, the cursor is set to screen position zero (top line, leftmost position).

'Erase/Write Alternate', Hex '0D'

The 'erase/write alternate' command is executed as an 'erase/write' command.

'Erase all Unprotected' Command Hex '0F'

The 'erase all unprotected' command provides space for the operator to put a message on the screen. All unprotected fields are erased. Protected fields remain unchanged.

Only the command code is transferred from processor storage to the attachment, after which channel end is indicated in the initial status report.

The attachment sets the 'modified data' tags of all unprotected fields in the buffer to zero, clears these fields to nulls, restores (unlocks) the keyboard, and sets the cursor to the beginning of the first cleared field. The cursor thus indicates to the operator where his input will be entered on the screen. In addition, the attention identifier is reset (to hex 60) by the command. At the completion of these actions, device end is indicated. If there are no unprotected fields (for example, the entire buffer is protected), the command has no effect other than resetting the attention identifier, unlocking the keyboard, and setting the cursor to screen position zero (although data entry will be inhibited). For details, see 'Orders and Control Characters'.

'Read Modified' Command, Hex '06'

The read modified command allows all modified data to be transferred from the display buffer to processor storage. Modified data is any data that has been introduced into the display buffer by the operator or by the program. As data is keyed in, the attribute character of the field into which the operator writes is automatically altered by turning the modified data tag bit to logical 1 level. The program can, however, also specify messages as modified data by assigning to the written field an attribute character with the modified data tag bit on. Modified fields written by the program are not distinguished from those written by the operator. It is thus possible to retrieve modified fields from a print buffer, although this is not normally required. If the buffer contents are unformatted, that is, there are no attribute characters, all the data in the buffer is assumed to be modified.

A 'read modified' command is usually issued after an attention interruption. The command can, however, be issued at any time. The attention interruption occurs whenever the operator has requested program service by pressing a program function key (PF1 to PF24) or a program attention key (CNCL, REQ, ENTER, CLEAR or a cursor key).

To indicate the reason for the attention interruption, the attachment generates one byte as an attention identifier (AID) and this is the first byte of information retrieved via a 'read modified' command. If one of the resetting actions such as cancel or clear causes the attention interruption, a subsequent 'read modified' command retrieves only the attention identifier (which indicates cancel or clear) without further information. This situation which is caused by pressing the cancel key, request key, or clear key, is termed a 'short read'.

If the enter key causes the attention interruption, the identifier indicates this and subsequently the attachment microprogram searches the buffer for modified data tag bits to identify (and retrieve) modified fields.

The same action occurs if the 'read modified' command is issued for reasons other than an attention interruption. In this case, the attention identifier (hex '60') indicates that the command is unsolicited, that is, no operator action has occurred. In either case, a search for modified fields begins in the buffer. The location where the search begins depends on the way in which the 'read modified' command is chained.

If the command is not chained, or chained from a 'sense', 'erase all unprotected' or 'control no-op' command, the search begins at buffer location zero. If the 'read modified' command is chained from a 'write', 'erase-write', read buffer, or another 'read modified' command, the search begins at the current buffer address.

The search terminates either at the buffer end address (if the last field in the buffer is not a modified field) or wraps to the first attribute character on the screen (if the last attribute character found had the data modified bit (bit 7) set).

If the buffer is formatted but no modified fields have been found, only the attention identifier (one byte) and the buffer address of the cursor (two bytes) are transferred to processor storage. These three bytes are termed the 'read heading'.

If modified fields have been found, a 'modified data stream' is assembled in the controller storage. This modified data stream consists of:

Read heading (attention ID, cursor addr)
 Buffer address order code (Hex '11')
 Buffer address (2 bytes)
 Text data

The text data is compressed by elimination of all empty buffer positions (nulls) and of all attribute characters. In this manner, only the actual text with its buffer address (or addresses) is assembled to form the modified data stream. Consequently, the length count of a retrieved field will not be the same as it was at the time of writing. If the screen display is unformatted (no attribute character), the read heading is followed by all alphameric data in the buffer, whether or not such data has been modified. Nulls are, however, eliminated.

The modified data stream is then transferred from the transient area to processor storage. Depending on the size of the data stream, several alternating transfers from display buffer to control buffer, and from control buffer to processor storage may be required (this is, however, transparent to the program). The transfer begins at the storage location addressed by CCW bits 8-31 and continues in ascending order until either the count (CCW bits 48-63) has been reduced to zero or the modified data stream ends. At that time, channel end and device end are both indicated in the CSW. In all other cases, channel end and device end are indicated earlier, that is, when the attention identifier (alone) or the read heading has been transferred.

For details of control characters that may accompany the text fields, see 'Control Characters'.

'Read Buffer' Command, Hex '02'

The 'read buffer' command permits the entire display (or print) buffer to be read into processor storage. The reading begins either at buffer location zero or any other location, depending on how the 'read buffer' command is issued, chained or unchained (stand-alone).

When the command is issued alone or chained from a 'sense', 'erase all uprotected', or 'control no-op' command, reading starts at buffer location zero and continues to the end (unless the length count is exhausted prematurely). In a 'read buffer' operation there is no wraparound to the beginning of the buffer.

When chained from 'write', 'erase/write', 'read modified' or another 'read buffer' command, reading starts at the current buffer address and continues to the end (unless the length count is exhausted prematurely).

The data thus transferred begins with the 3-character read heading (attention identifier plus cursor address) and contains all buffer locations including start field orders, attribute characters, and nulls. The read buffer command is intended mainly for diagnostic purposes.

'Sense' Command, Hex '04'

The 'sense' command, when issued, causes information on errors or unusual conditions to be transferred to processor storage for inspection. A 'sense' command is used to retrieve the causes of a unit check so that recovery action can be taken. The command causes one sense byte to be stored at the location specified in bits 8-31 of the CCW. For details, see video display sense information.

'Sense I/O' Command, Hex 'E4'

The 'sense 1/0' command transfers seven bytes of device identification from the attachment to storage. The identification is given whether the addressed device is ready or not. The bytes contain:

Byte Contents

0 Hex 'FF'
1 Control unit type number
2 Control unit type number
3 Control unit model number
4 Device type number
5 Device type number
6 Device model number

As the console has no separate control unit, the type and model number of the host processor are stored as control unit identifiers. The device type number is 3278, and the model number for the display console is 2A. If the console is in 1052 mode, the device type is 1052 and the model is 00.

'No operation', Hex '03'

This command performs no function at the device, but status information is presented.

Orders and Control Characters

Orders and control characters are used in the data stream of 'write' and 'erase write' commands to specify details of the screen (or print buffer) location of a message, and the nature of this message (that is, whether it is protected, unprotected, or modified). The following control codes are available:

Write Control Character

The write-control character is the first (and possibly the only) character in the data stream of every 'write' or 'erase/write' command. The character specifies subcommands associated with the keyboard, the audible alarm, and a terminal printer as follows:

Bit Meaning

- 0 Depends on bits 2-7
- 1 Always set
- 2 Print format
- 3 Print format
- 4 Start printer
- 5 Sound alarm
- 6 Restore keyboard and attention identifier
- 7 Set modified data tags to zero

<u>Bit 0</u>. This bit is either 1 or 0 depending on the value of bits 2-7 because the internal representation of the write control character is a 6-bit code. The translation from 6-bit to EBCDIC determines the setting of bit 0.

<u>Bit 1</u>. Bit 1 must always be 1 so that the write control character cannot be interpreted as a teleprocessing control $\frac{1}{2}$

character (ETX, ETB, etc). The console attachment does not check whether bit 1 is really set to 1.

<u>Bits 2 and 3</u>. These print-format bits specify the print line length (which has no effect on a video display but affects a printer) as follows:

Bit 2,3 Meaning

00	The 'new line' (NL) order in the data stream determines line length
01	Specifies 40 characters length
10	Specifies 64 characters length
11	Specifies 80 characters length

<u>Bit 4</u>. This start printer bit in the write control character starts the printer (if the 'start 1/0' instruction addresses a terminal printer). The buffer contents are then printed in the following way: fields with an attribute character that allows the field to be displayed are printed. Fields with an attribute character declaring the field as 'nondisplay' are not printed.

<u>Note</u>: In a chain of commands only the last CCW can have the start printer bit set in the write control character, otherwise an operation check occurs.

<u>Bit 5</u>. The sound alarm bit is used to alert the operator to an important message. The alarm sounds for a fixed time and is then silenced automatically. The audible alarm is a standard feature on the display and has volume control.

<u>Bit 6</u>. The restore keyboard bit is used to unlock the keyboard and to reset the attention identifier (created by a previous keyboard operation) and the input inhibited indicator on the screen.

<u>Bit 7</u>. The reset modified data tag bit sets all modified data tag bits to zero before the execution of the 'write' operation, so that new modified data tags can be written.

Note: When a 'write' or 'erase/write' command is specified, data does not have to follow the write control character. Both commands can be used for control operations only (such as, sounding the alarm, or restoring the keyboard). Actions which do not apply to the addressed device (for example, increased brightness for a terminal printer), have no effect on the device. For control purposes it is sufficient to transfer just the write control character. Any data following the write control character, however, enters a screen location depending on the presence or absence of a 'set buffer address' order (see 'Set Buffer Address' Order).

'Set Buffer Address' Order, Hex '11'

The buffer address order, if used, follows the write control character in a 'write' or 'erase/write' command. The set buffer address order is a sequence of three adjacent bytes. The first byte is the 'set buffer address' order code (Hex 11) and the next two bytes are assumed to represent the buffer address. The buffer address can range from 0 to 1919 (decimal), or 1599 on the operator console, and specifies where the text data is to be located on the screen. The bits in the two buffer address bytes represent a binary number as follows:

Byte 1 Value

0	lgnored
1 2	lgnored 2048
3	1024
4	512
5 6	256 128
0 7	64

Byte 2 Value

0	lgnored
1	Ignored
2	32
3	16
3 4	8
5	4
6	2
7	1

The buffer address is checked for validity and if it is outside the available screen area (beyond 1599 on the operator console or beyond 1919 on the data entry stations), the command is terminated with unit check, and operation check is indicated in the sense byte. If the buffer address is valid but the length count in the associated 'write' command is larger than the space available to the buffer end, data will continue to be transferred through a wrap-around to the buffer beginning. The data stream transferred by a 'write' or 'erase/write' command may contain as many set buffer address orders as required for text distribution. If the data stream in a write operation contains no 'set buffer address' order, the destination of the data depends on the chaining of the 'write' command.

If the 'write' command is issued alone or chained from a 'no-op', 'erase all unprotected', or 'sense' command, the data enters the current location of the cursor. If there is

no 'set buffer address' order and the 'write' command is chained from another 'write' or 'read' command, the data enters the current buffer address.

'Start Field' Order, Hex '1D'

The 'start field' order consists of two bytes. The first byte is the start field order code (Hex '1D') which indicates that the next byte is to be interpreted as the attribute character defining the properties of the field. The 'start field' order code follows the buffer address bytes to open the field. A data stream such as the one transferred by a 'write' or 'erase/write' command may be subdivided into as many fields as necessary by means of the 'start field' order. If each of these fields is to be located in a different area of the screen, each must be preceded by a 'set buffer address' order, otherwise the fields are stored (and displayed) sequentially.

Attribute Character

The attribute character describes the characteristics of the field that follows it. The field extends from the attribute character to the next following attribute character (if any). The attribute character is the byte following the 'start field' order. The attribute character is protected against overwriting by the operator. The program can, however, overwrite any attribute character (either by a 'write' or 'erase/write' command or by a 'repeat to address' order).

The attribute character occupies a buffer position but is not displayed. The attribute character is the only control character that is placed on the screen. Since the attribute character is invisible, its position is dark and cannot be used for display. When structuring a message, in some cases, not all positions of a line can be used for display owing to the attribute character. An attribute character formats a screen display and affects the retrieval of data by a 'read modified' command.

The attribute character is one byte in which each bit is assigned a specific function, as follows:

Bit Meaning

- 0 Value determined by bits 2-7
- 1 Always set to 1
- 2 Data unprotected (0)/protected (1)
- 3 Alphameric (0)/numeric (1)
- 4 Display control
- 5 Display control
- 6 Reserved (must be 0)
- 7 Data modified (1)/not modified (0)

The bits of the attribute character have the following functions:

<u>Bit 0</u>. This bit has no program function. Depending on the configuration of bits 2-7, bit 0 is automatically set to 0 or 1 to ensure that the attribute character is always a printable and punchable EBCDIC character. This is done to prevent errors during the dumping of program code.

<u>Bit 1</u>. This bit has no function but must always be set to 1 for compatibility. With bit 1 set to 1, the attribute character can never be decoded as a line control character (ETX, EOT, etc) by a remote 3270 information display system. The console attachment does not check whether bit 1 is set.

<u>Bit 2</u>. This protect/unprotect bit specifies whether or not the data in the field is to be protected against overwriting by the operator. This protection is required for certain fields (such as headlines) because the operator can move the cursor to any location on the screen via the cursor positioning keys and can thus destroy a message. Protected data fields, however, cannot be disturbed by the operator and cannot be erased by an 'erase all unprotected' command. Unprotected fields are typically used as input areas for the operator or as message areas.

<u>Bit 3</u>. Alphameric/Numeric. This bit defines for data entry keyboards whether the keyboard is automatically shifted or not. When set to 1, bit 3 causes an upshift so that the numeric values on the keys are entered. This relieves the operator from pressing the numeric key before entering digits. If the numeric lock feature is installed, attempts to enter alpha characters into a field for which bit 3 is on inhibit the keyboard. If the numeric lock feature is installed on a 3278-2 Keyboard/Display, this bit, if set, causes an automatic downshift to allow numeric entries.

<u>Bit</u> 4, 5. These two display control bits define whether data in a field is to be displayed and, if so, whether it is displayed with normal or increased brightness, or is pen-detectable as follows:

Bits <u>Meaning</u>

- 00 Display not selector-pen detectable
- 01 Display selector-pen detectable
- 10 Intensified display
- 11 Non-display, non-print, non-detect

Any display control can be combined with another attribute, for example a pen-detectable field may be protected or unprotected.

It should be noted that data entered into a non-display field is not lost, the data exists and can be retrieved into storage. The data is, however, invisible and not printed, which may be desirable for security or privacy.

<u>Bit 7</u>. This data modified/not modified bit specifies whether or not the field is made available for retrieval by a 'read modified' command. Data keyed-in by the operator will always have bit 7 of the attribute character turned on. Bit 7 may also be set by the program. A field that has bit 7 off is ignored by the 'read modified' command. An 'erase all unprotected' command sets bit 7 of the attribute characters of all unprotected fields to zero so that none of these fields can be read by a 'read modified' command.

'NL', 'EM', and 'FF' Print Orders

The print orders concern terminal printers only and do not affect the operator console. For terminal printers, the orders should be placed into the print buffers as described.

'NL', Hex '15':

NL means 'new line' and causes a line feed unless the write control character contains a format. In which case, the NL order is ignored and the line feed occurs when the line limit (as defined by the format specification) is reached. The 'NL' order is also ignored if it is in a non-display or non-print field.

'EM', Hex '19':

EM means end of message and ends the print operation if no format is specified for the write control character. If a format is specified, or if the order is located in a non-display/non-print field, the 'EM' order is ignored, and printing continues until the buffer is empty.

'FF', Hex '0C':

FF means forms feed and is accepted as valid when encountered in a buffer location corresponding to the first position of a print line in a field designated either as print or non-print. When a valid 'FF' order is encountered, the form moves vertically to a predetermined line where printing begins. The first print line position (which holds the 'FF' order) is printed as a blank. If the 'FF' order is not in the first position of a print line, the form does not move because the order is invalid.

'Insert Cursor' Order, Hex '13'

The 'insert cursor' order consists of one byte (containing Hex '13') that relocates the cursor at the buffer position reached when the order is detected in the data stream (current buffer position). A data stream may contain as many insert cursor orders as required and each of them causes the cursor to be moved to the current buffer address. If a data stream contains no insert cursor order, the cursor position is not changed.

'Program Tab' Order, Hex '05'

The 'program tab' order consists of one byte (containing Hex code '05') which advances the current buffer address to the first available position of the next unprotected field. For example, if the current buffer address points to the attribute character of an unprotected field, the address is increased by 1 and will thus point to the first available position of this unprotected field. The order may thus be used to find the next input field and to fill the current field (up to the next unprotected field) with nulls.

When the 'program tab' order immediately follows a write control character, an order or an order sequence, the buffer address is set to the first character position of the next unprotected field without changing data in between. When the 'program tab' order does not immediately follow a control character or order, but is located among data, nulls are inserted from the current buffer address up to the first character position of the next unprotected field.

The search for the next unprotected field begins at the current buffer address and stops at the last buffer location. If no unprotected field is found, or if the last buffer location contains the attribute character for such a field, the buffer address zero is set, and the search and null insertion (if any) stop. There is no wrap-around. To continue the search, a second program tab order must be given after the first. The second order begins the search for unprotected fields at location zero and, if the previous order inserted nulls, this order also inserts them to the end of the current field.

'Repeat To Address' Order, Hex '3C'

'Repeat to address' is used to insert any alphameric character (including null) repetitively into consecutive character positions beginning at the current buffer address and ending at (but not including) a stop address. All existing characters, including attribute characters are overwritten, regardless of the protection status of any field.

The 'repeat to address' order consists of a sequence of four bytes. The first byte is the order code (containing Hex '3C') and must be followed by the 2-byte stop address and the 1-byte character which is to be inserted. The order can be put into any data stream (for example, to produce a dotted line).

The character insertion ends with the last location prior to the stop address (the stop address location itself is excluded). If the stop address is identical to the current buffer address, the character is inserted into every location on the screen. If the stop address is lower than the start address, the insertion wraps around from the bottom of the screen to the top. If the stop address exceeds the screen capacity (higher than 1599 on the operator console or 1919 on the data entry stations) a unit check (with operation check) occurs.

'Erase Unprotected To Address' Order, Hex '12'

'Erase unprotected to address' inserts nulls in all unprotected buffer locations beginning at the current buffer address and ending with the location before the stop address. It is thus possible to erase unprotected areas up to a defined point. Attribute characters are, however, not erased. The order consists of three bytes, the first byte being the order code (hex '12') and the following two bytes being the stop address.

If the stop address is identical to the start address (current buffer address), the entire screen has all of its unprotected fields replaced by nulls. If the stop address is smaller than the start address, the nulling operation wraps around from the bottom to the top of the screen.

Attention Identifier

The attention identifier is a byte that is generated by the controller when a program attention key (such as ENTER. CANCEL, or a clear key) is pressed or when one of the 24 program function keys is operated. The attention identifier is also generated when an unsolicited 'read modified' command is given. The attention identifier interprets the meaning of the attention status (Bit 32 in the CSW) so that the operating system can react accordingly. If the operating system issues a 'read modified' command upon detection of an operator action (such as function key pressed), this command is a solicited command. If the operating system volunteers a 'read modified' command, the command is unsolicited. A read modified command that follows a solicited read modified command is also considered to be a solicited command. The attention identifier is generated as follows:

Hex Meaning

7D	ENTER pressed (or cursor select)
6E	CANCEL pressed (or PA2)
60	Unsolicited 'read modified' issued to display
E8	Unsolicited 'read modified' command issued to printer
6B	PA3 key
6C	REQUEST pressed (or PA1)
6D	CLEAR pressed
F1-F9	Program function keys 1-9 pressed
7A-7C	Program function keys 10-12 pressed
FO	Test request key pressed*

<u>*Note</u>: Test request, cursor select, clear and PA3 are available on the display stations but not on the display console. The cancel key on the display console corresponds to the PA2 key on a display station, and the request key corresponds to PA1. Once the identification character has been generated, it is stored in the support processor. The next 'read modified' command receives the attention modifier as the first byte of the data stream transferred to processor storage. The identifier is not reset by this read operation. Reset (to 60) occurs the next time either an 'erase all unprotected' or a 'write' or 'erase/write' command specifies 'keyboard restore' in its write control character.

Display Status

The support processor, which operates the display, the keyboard, and the (optional) console printer, provides unit status and channel status as follows:

Unit Status

The unit status is given in bits 32-39 of the CSW. The bits are assigned as follows:

Bit Meaning

32 Attention

- 33 Status modifier (not used)
- 34 Control unit end (not used)
- 35 Busy
- 36 Channel end
- 37 Device end
- 38 Unit check
- 39 Unit exception (not used)

<u>Bit 32</u>. This 'attention' bit may be indicated either alone ('attention interrupt') or in the initial or the ending status for a command, depending on the time at which 'attention' is generated. 'Attention' is, however, always indicated at the earliest moment possible.

'Attention' itself does not indicate the reason for which it is signaled. The operating system should, therefore, issue a 'read modified' command. The first (and possibly the only) byte transferred to processor storage indicates the reason for the 'attention interrupt' as follows:

Byte Value Meaning (in hex)

7D	ENTER pressed
6E	CANCEL pressed (PA2)
6B	(PA3 Data entry)
60	REQUEST pressed (PA1)
6D	CLEAR pressed
F1-F9	Program function keys 1-9 pressed
7A-7C	Program function keys 10-12 pressed
F0	Test request key pressed *

* The test request key is not available on the operator console.

 $\frac{'7D'}{}$, means that the operator has entered a message into the display buffer.

<u>'6E'</u> is interpreted by the operating system but usually indicates deletion or clearing of the input area.

 $\frac{16C'}{16C'}$ is interpreted by the operating system but usually is a call for the attention routine (AR) of the operating system.

'6D' indicates that the entire display buffer has been filled with nulls and the cursor is repositioned to location zero.

 $\frac{PF}{7C}$ codes, the program function key codes (F1-F9, 7A, 7B, 7C) are at the discretion of any application programs and may be used for any purpose.

 $\underline{F0}$ is interpreted by the program, usually to call a test program.

<u>Bit 35</u>. Busy indicates that the display is either executing a previously initiated command or manual operation, or has an interruption condition (such as device end or attention) pending, or the display console is in diagnostic mode.

<u>Bit 36</u>. This bit is set when the data transfer from processor storage to the transient area (or vice versa), or the command transfer has been completed.

<u>Bit 37</u>. This bit indicates that the device is free to execute another command. Depending on the command type, device end either accompanies channel end or is set later. Device end is presented alone when (1) the operator turns the power switch from off to on, which makes the device ready or (2) when a manual operation is completed, provided the console was addressed while busy with the manual operation.
Device end is presented alone when:

- (1) The operator switches processor power on and the device becomes ready, or
- (2) The operator switches the console from diagnostic mode to operating-system mode at a time when the console had previously reported busy to an SIO command.

<u>Bit 38</u>. Unit check is a summary indication for errors or unusual conditions such as incomplete control codes, and invalid buffer address specification. Unit check requires that a 'sense' command is issued to retrieve the cause of errors or unusual conditions. See 'Sense Information' for details.

Channel Status

The channel status is indicated in bits 40-47 of the CSW which are assigned as follows:

Bit Meaning

- 40 Program-controlled interrupt
- 41 Incorrect length
- 42 Program check
- 43 Protection check
- 44 Channel data check
- 45 Channel control check
- 46 Interface control check (not used)
- 47 Chaining check (not used)

For 'read' commands, incorrect length is indicated when the number of bytes transferred does not agree with the count in the command. For 'write' commands, incorrect length is always indicated.

Video Display Sense Information

The support processor provides only one byte of sense information, as follows:

Sense Byte 0

Sense byte 0 contains the following bit assignments:

<u>Bit</u> <u>Meaning</u>

- 0 Command reject
- 1 Intervention required
- 2 Bus-Out check (not used)
- 3 Equipment check
- 4 Data check (not used)
- 5 Unit specify
- 6 Control check
- 7 Operation check

<u>Bit 0</u>. This bit is set when an unassigned command is received by the support processor.

<u>Bit 1</u>. 'Intervention required' is indicated whenever a command (other than 'sense' or 'sense 1/0') is issued to a not-ready device. The intervention should consist of turning on the power or on-line switch or, when a terminal printer is involved, in supplying new forms or removing the jam. 'Intervention required' can also be set by a bad connection of the coaxial cable between the processor and the device.

<u>Bit 3</u>. 'Equipment check' is set when malfunctions or parity checks are detected in the device cluster adapter or when a hardware malfunction occurs during a print operation. Malfunctions of this type are a failure to reset to a defined state, failure to send request pulses during a write operation, or a parity error.

<u>Bit 5.</u> 'Unit Specify' is set when an error causing an equipment check is detected during a print operation by the terminal printer itself.

Bit 6. 'Control check' is set when

- A request from a terminal is not handled within the proper time.
- The system diskette performs an unsuccesful read operation (bit 3 is also set.)

Bit 7. Operation check indicates one of the following conditions at the time channel end or device end is presented:

- An invalid buffer address is detected in the data stream of a 'write' or 'erase/write' command. An address above 1599 (decimal) is invalid on the operator console, and a value above 1919 (decimal) is invalid on all data entry stations.
- An incomplete order is detected in the data stream of a 'write' or 'erase/write' command. An order is incomplete when the order code is detected but no further data follows (for orders which require additional data, such as 'program tab', 'start field', 'set buffer address').
- The start printer bit is on in the write control character of any CCW other than the last in a chain of commands to a terminal printer.

Visual Status Indicators

For the operator's convenience, graphic symbols show the state of the keyboard (inhibited or free, data entry to be repeated, and so on). The symbols are a subset of the 3278 set, although not all the subset symbols are available on the operator console because of a special feature limitation. The symbols are described in <u>IBM 4331 Processor</u> <u>Operating Procedures and Problem Determination Guide</u>, GA33-1525.

1052 Commands

The optional 1052 command set is selected at IPL time as described in <u>Operators Library</u>: <u>IBM</u> <u>4331</u> <u>Processor</u> <u>Operating Procedures and Problem Determination Guide</u>, GA33-1525. The following descriptions include the functions of the terminal printers, which only apply when the 3278 Model 1 or 2 is installed. The operator console and the 3278-2 displays give the same results whether terminal printers are attached or not. This command set is identical to the 1052 set, although the 3287-1 and -2 terminal printers do not operate like a 1052

(which is a printer keyboard). The console printer may be physically remote from the 3278-2A display console. The display copies the functions of a 1052 in addition to the print operations that are executed on the console printer. This copy-effect is, however, transparent to the program. When the 1052 command set is selected, the display and the printer both operate under the unique device address assigned to the operator console. The 3287 printer's own address then no longer exists. If several 3287s are installed, the 3287 on the lowest-numbered printer port has the 1052 mission. The following description explains the main purpose of each command and mentions the action of the display, where applicable. The following commands are provided:

<u>Cmd</u> Code	Command
Hex	<u>CCW</u> <u>Bits</u> 01234567
01	00000001 Write inhibit carrier return
09	00001001 Write auto carrier return
0A	00001010 Read inquiry
03	00000011 Control no-op
OB	00001011 Control alarm
04	00000100 Sense
Е4	11100100 Sense 1/0

<u>Programming Note</u>: With the 1052 command set, the internal control automatically provides one attribute character per screen line. This reduces the number of 'useful' display positions by one character per line (for all 'write' commands). The first position is occupied by the attribute character. Print control characters such as used in the original 1052 are accepted as data but do not have control power.

'Write Inhibit Carrier Return', Hex '01'

The 'write inhibit carrier return' command causes a 'plain' display of data on the screen whereby printing is suppressed for the time being. The term 'plain' display means that the message begins at the first available position in line 19, and ends at the position next to the last character (ready for continuation). Depending on the starting position and the message length, the message may extend to line 20. Lines 19 and 20 are the designated write input lines on the screen. The cursor appears in the upper left corner (its default position) but has no function.

The command execution begins with a data transfer from the processor storage location specified in bits 8-31 of the CCW to the console attachment. This data transfer continues in ascending order of address until the length count in the CCW has been reduced to zero or the input area has been filled with a maximum of 125 characters, whichever occurs first. At that time, channel end is indicated. The limitation to 125 characters is made for compatibility reasons (the 3287 printer has 132 positions). The data thus transferred is translated and distributed to the console display buffer after which device end is indicated. The text is then visible on the display but not yet printed.

Actual printing occurs the next time a 'write auto carrier return' command is given or another carrier return action occurs. For example, the carrier is automatically returned upon pressing the Enter key or the Cancel key at the console and this action would terminate a pending 'read' operation. If several 'write inhibit carrier return' commands are given in succession (without any intervening carrier returning command or carrier return action) all data up to 125 bytes is stored and printed whenever the next carrier return action occurs. This means that the total (cumulative) number of bytes which such commands may transfer should not exceed 125. If more than 125 bytes are transferred (with a single command or a chain of commands), the excess bytes are lost.

If a 'write inhibit carrier return' command or several such commands have filled the controller storage input area and a 'read inquiry' command is issued prior to a carrier returning command (which would have started the printer), the read command is cancelled with unit exception indicated (see 'read inquiry' command for details). This cancellation will, however, return the carrier and start the printing of the 125 characters.

'Write Auto Carrier Return', Hex '09'

The 'write auto carrier return' command displays data on the screen and prints the same data on the printer. The display begins at the first available position in line 19 (or 20, as the case may be). Thereafter, the data on the screen is moved up to free the write input lines and simultaneously text printing commences. If data is stored from a previously issued 'write inhibit carrier return' command (or several such commands), that data is printed with the new data following in one continous operation.

The command execution begins with the data transfer from processor storage to the controller storage area after which channel end is presented. The message is translated then displayed on the screen and printing of previously transferred text (if any) and the new text is started. After the printing of the last character, the carrier stops at the next position (either to the right or left of the text, depending on the print sweep direction), the form is advanced by one step then device end is signaled. The 3287 printer can sweep from right to left and vice versa during printing but once printing is completed on a line, the printer cannot continue on that same line regardless of any space still available. If the print operation is terminated by a parity check in the printer, unit exception is indicated in addition. A normal condition such as end-of-forms causes a unit check with intervention required only when the operator does not react within the prescribed time.

<u>Note</u>: Operator actions on the console do not interfere with the print operation. If the operator presses the Mode Select key during the print operation, the 'write' command (print operation) continues to completion even though the display meanwhile shows the mode select picture. Upon pressing the change display key, the full message as printed will be seen on the screen.

'Read Inquiry', Hex '0A'

This command is usually given by the operating system only when requested by the operator. The operator requests service by pressing the Request key on the keyboard. The request is stored in the controller unless the display works as sytem console (that is, performs manual operations such as alter/display, instruction step, etc.). When manual operations are in progress, the Request key has no function. The request eventually leads to an attention interruption. If the system cannot accept the request for the time being, the wait symbol is shown.

When the attention interruption is taken, the program will generally issue the 'read inquiry' command. Execution of this command is indicated to the operator via audible alarm and by the cursor moving to the first available position of the operator's input area on the screen which is comprised by lines 19 and 20. In addition, the word 'proceed' appears with increased brightness. The operator may now key-in data.

Any data thus keyed-in appears with high intensity at, and adjacent to, the location marked by the cursor. Depending on the details of a preceding write operation, data entry may start either at position 2 of line 19 or later. For example, if the preceding operation was writing with carrier return, the input area is free (blank) and data entry starts at position 2 of line 19. If the preceding operation was writing without carrier return, the message still occupies the input area and the cursor is located two positions after the last character of that message. The inserted 'blank' character is actually the attribute character for the operator's input field. The operator may enter data adjacent to the existing text up to the end of the input area. Attempting to write beyond the input area inhibits the keyboard and requires pressing the Keyboard Reset key before action is resumed.

The read operation is not completed until the operator terminates it by either one of the following actions:

• Pressing the Enter key

• Pressing the Cancel key

As soon as any of these keys are depressed, the cursor returns to the upper leftmost corner and the keyboard is inhibited. The resulting actions differ depending on the type of termination, as follows:

If Enter is pressed, the contents of the data input area are moved upward by one or two lines (to free the input area) and are transferred to processor storage after which channel end is signaled. At the same time the transferred data is also printed on the console printer. However, only the number of characters defined by the count of the 'read' command are transferred, displayed, and printed. If the operator has entered more data than allowed by the count, the excess data is cut off (and erased on the screen). When the last character has been printed, the carrier stops at the next character position and the form advances by one step, then device end is presented. This completes the 'read inquiry' command.

If <u>Cancel</u> is pressed, the status channel end and unit exception is returned and the contents of the data entry area are not transferred to processor storage but they are nevertheless printed. To mark the text as obsolete, an asterisk is displayed (and printed) next to the last character.

If the Mode Select key is pressed, the mode select picture appears on the screen but the 'read inquiry' command is not terminated. It remains available for the moment when the operator presses the change display key (to restore the previous situation) and then continues or terminates the 'read inquiry' command, as previously described.

Notes:

 If the controller buffer is full with 125 bytes from a previously issued 'write without carrier return' command that has not been mechanically executed, a 'read inquiry' command is terminated with unit exception because there is no space for the operator to enter his data. However, after cancellation of the 'read inquiry' command, printing is initiated and the 'read inquiry' command may then be repeated. 2. If the Request key is pressed, the command is not terminated but an attention interruption is nevertheless requested.

'Control No-Op', Hex '03'

This command causes no action at the console. When it is issued, channel end, device end, and any other status that may exist at that time are presented in the initial status.

'Control Alarm', Hex '0B'

'Control Alarm' causes the audible alarm to sound. The audible alarm is a standard feature on the display. The command is of the immediate type, that is, channel end is presented in the initial status: device end follows as soon as the command code has been transferred to the attachment. The alarm sounds for a predetermined time.

'Sense', Hex '04'

The 'sense' command causes sense information to be transferred from the attachment to the processor storage location designated in CCW bits 8-31. At the completion of this data transfer, channel end and device end are both indicated. The 'sense' command does not reset the sense indicators. These are reset by any other command that may follow (except 'sense'). For details, see 'Console Printer Sense Information'.

'Sense I/O', Hex 'E4'

A 'sense I/O' operation transmits seven bytes of identification to storage as follows.

Byte Contents

0	Hex 'FF	I	
1	Control	unit	type
2	Control	unit	type
3	Control	unit	model

- 4 Device type
- 5 Device type
- 6 Device model

The control unit type and model number are those of the 4331, into which the console is integrated. The device type number is 1052 and the device model 00.

Console Printer Status

Status information is provided in bits 32-47 of the channel status word whenever an 1/0 instruction and/or command has been terminated, completed, or rejected. Bits 32-39 represent the unit status specific to the console printer/video display combination, whereas bits 40-47 represent the channel status, which is standard.

Unit Status

The unit status indicators are represented by the following bits:

CCW Bit Meaning

32 Attention

- 33 Status modifier (not used)
- 34 Control unit end (not used)
- 35 Busy
- 36 Channel end
- 37 Device end
- 38 Unit check
- 39 Unit exception

<u>Bit 32</u>. Attention is generated in the support processor when the Request key is pressed. When no other operation is in progress or, when the current operation ends the attention status is presented to the channel immediately. If interruptions are disabled, the attention condition remains pending until interruptions are allowed or until an 1/0 instruction such as 'start 1/0' or 'test 1/0' clears the condition. The program reacts to attention by issuing the 'read inguiry' command.

Bit 33. Not used

Bit 34. Not used

<u>Bit 35</u>. The busy bit accompanies any pending status (such as device end or attention) to mark such a status as one that has been presented previously but was not accepted at that time. The presentation of status with the busy bit clears this status.

<u>Bit 36</u>. Channel end is set when the transfer of the command code and/or data over the channel-like facilities is completed or terminated.

<u>Bit</u> <u>37</u>. Device end is presented when the device (that is, the console printer) is available to execute the next command. Thus, device end is set when the mechanical print

cycle is completed, or is presented alone when the printer changes from the not-ready to the ready state.

<u>Bit 38</u>. This status is an indication for various error conditions. The bit is set whenever conditions are found that indicate sense information on the detailed cause to be available (see 'Sense Information').

<u>Bit 39</u>. This status indicates termination of a 'read inquiry' command either by pressing the Cancel key or because an operation was disrupted by the operator making the printer not ready (for example, operating any safety interlocks). If a print operation is disrupted, the full message is on the screen but the printed text may be a fragment. In this case, an asterisk is printed next to the last character. Upon finding unit exception the operating system repeats the last 'write command'.

Channel Status

For the console printer, only the following channel status bits are set:

CSW Bit Meaning

- 40 Program controlled interruption
- 41 Incorrect length
- 42 Program check
- 43 Protection check
- 44-47 Not used

<u>Bit 40</u>. The program controlled interruption is indicated when the channel fetches a CCW with the PCI flag on. The PCI remains pending throughout a chain of CCW's if it cannot be taken when first detected. PCIs are not stacked. If several PCIs in a chain have not been processed, only the last one will take effect.

Bit $\underline{41}$. This bit is indicated when the SLI flag in the CCW is off and the length count in a 'write' command is greater or smaller than 125 characters. For the 'read inquiry' command, incorrect length is set whenever the number of input bytes does not agree with the length count in the CCW.

Bit 42. This bit is set whenever one of the following errors is detected:

Invalid CCW address specification Invalid CCW address Invalid IDAL Invalid IDAW Invalid command code Invalid count Invalid data address Invalid key Invalid CAW format Invalid sequence (TIC refers to TIC)

<u>Bit 43</u>. This bit is set when the protection key in the CAW does not match the key in storage or when the protection key is not zero but an attempt is made to refer to the protected area.

Console Printer Sense Information

Upon indication of unit check in the CSW, the console printer provides the following sense information in sense byte 0.

Sense Byte 0

Bit Meaning

- 0 Command reject
- 1 Intervention required
- 2 Not used
- 3 Equipment check
- 4 Not used
- 5 Not used
- 6 Not used
- 7 Not used

<u>Bit</u> $\underline{0}$. This bit is set when a command outside the assigned command set is issued to the operator's console.

<u>Bit 1</u>. This bit is set when the operator's console is addressed with a valid command, other than, 'sense', 'sense 1/0', or 'control alarm', while it is in the not-ready state, that is, when the display console or printer has any error condition or power off.

Correction of these conditions causes device end to be set to indicate the ready state.

<u>Bit 3</u>. This bit is set when the printer fails during print operations.

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Chapter 5. Diskette Drive

This section describes the commands, status reports, sense information, and error recovery procedures for the optional diskette drive. The drive, which uses one-sided diskettes with 128 bytes per record, 26 records per track, is compatible with the IBM 3540 Diskette Input/Output Unit. For further information see IBM 3540 Diskette Input/Output Unit Operator's Guide and Programmer's Reference, GA21-9197.

Commands

Command Code		Command Name
CCW 0123	Bits 4567	
0000 0000 0000 0000 0010 0000	0111 0010 0110 0101 0001 0100	Define operations Seek Read IPL Read data Write data Write control Sense
0000	0011	Sense 1/0 No-op Feed
	CCW 0123 0010 0000 0000 0000 0000 0010 0000 1110	CCW Bits 0123 4567 0010 1111 0000 0111 0000 0110 0000 0101 0000 0101 0010 0001 0000 0100 1110 0100 0000 0011

Define Operations (2F)

The define operations command opens the program. The command is a prerequisite for other data transfer commands except read IPL and sense. Four bytes of control information are transferred from processor storage to the attachment and stored until the next define operations command or read IPL is issued or a power-on reset (IML) occurs. The four bytes define the following:

Byte	Function

0	CCW count
1	Allowed operations

2	Not	used,	must	be	zero

.

3 Reserved

After the transfer of the control bytes, channel end is

presented. After verifying control information, device end is presented. If less than four bytes are transferred or control information is erroneous, the command ends with device end and unit check in the status and command reject in sense byte 0. Channel end, device end, and unit check may be combined as described under 'diskette unit status'.

The following text describes the meaning and use of the control bytes including the effect of invalid specifications.

CCW-Count (Control Byte 0)

Byte 0 specifies the number of write commands to be issued between seek commands. For read commands, the CCW-count is ignored and may be any value including zero.

For write operations the count in byte 0 must be a binary number ranging from 1 to 26. The count specifies the number of records to be written on one track between seek operations. No more than 26 records can be written on one track. If byte 0 is greater than 26, the attachment stores zero as CCW count, and no error is indicated. Subsequent write commands are then rejected.

A CCW-count smaller than the allowed maximum is permitted and has no adverse effect on recording or CRC-checking.

<u>Programming Note</u>: Record 26 represents the boundary that cannot be crossed without a seek command. Consequently, a CCW-count smaller than the allowed maximum can be too large if writing starts at a record number higher than 1.

Allowed Operations (Control Byte 1)

This byte specifies whether read or write commands are allowed in the chain following the define operations command. Byte 1 also specifies whether control records starting with character D or F are to be unit checked or not. Control records marked with a period character are always unit checked. (See "write control" for details on control records). The bits in byte 1 have the following functions:

Bit Meaning

1

0 Allow read commands

Allow write commands

2 Suppress unit check (for D or F- flagged records) 3 through 7 Not used, should be zero

<u>Bits 0 and 1 (allow read, allow write</u>). Either bit, but not both, may be set. If both bits are on (read and write), the define operations command is terminated with unit check in the status and command reject in sense byte 0.

If both bits are off, the 'define operations' command is valid but subsequent commands are affected as follows:

 A seek command is accepted without error indication (because the attachment assumes "read allowed" for a seek command).

- Read or write commands are rejected.

When the read bit is on and the write bit is off, read commands are allowed but write commands are rejected. The reverse applies when bit 0 is off while bit 1 is on. When bit 1 is on, a valid CCW-count is required.

<u>Bit 2</u> (suppress unit check). This bit has no effect when write commands are allowed because the attachment then ignores bit 2. However, bit 2 is checked whenever reading is allowed and control records with flag character D or F are read. D means that a record has been logically deleted. F indicates that the surface is defective within the sector and that the record/block has been displaced to the next sequential sector. See also "Record Format". When reading such a record while bit 2 is set, no unit check occurs. However, when bit 2 is off while D-flagged or F-flagged control records are read, the records are transferred but, upon completion, unit check, data check, and "special record transferred" are indicated. The unit check suppression is provided to improve performance when processing HDR 1 labels on cylinder 0.

Bytes 2 and 3

These bytes are not used and must be filled with zeros.

Seek (07)

The seek command must precede any individual read or write command (except read IPL) or any sequence of read or write commands. The seek command performs two tasks.

- The four-byte seek address (cylinder number, head number, record number) is transferred from processor storage to the attachment.
- The access mechanism is positioned at the specified cylinder and head. If read operations are allowed in the associated define operations command, the seek command additionally transfers the specified record and the remainder of the track (up to 1024 bytes) to the buffer in the attachment whereafter device end is given.

The number of bytes transferred by this implicit read operation varies up to 1024. However, the implicit read occurs only when the length found in the ID field of the specified record is 128. Unit check is set in the unit status field of the CSW with "equipment check" and "permanent error" set in the sense bytes. No data is transferred. In this case the diskette has the wrong format (or no format).

The cylinder address is a logical address which is resolved to a physical diskette address by the diskette attachment. The four bytes have the following meaning:

Byte 0 Reserved

This byte must be zero.

Byte 1, Cylinder Number

This byte may contain any binary number from 0 to 74.

Byte 2, Head Number

Must be binary zero.

Byte 3, Record Number

This byte may contain any binary number ranging from 1 to 26.

If less than four bytes are transmitted, or if the seek address is invalid, the command is terminated with unit check at device end time, and command reject is set in sense byte 0. Channel end, device end and unit check may be combined as described under "diskette unit status". A seek address is invalid if the cylinder number is greater than 74, the head number is greater than 0, or the record number exceeds 26. In this case, any mechanical motion is suppressed. Subsequent read or write operations are rejected until a valid seek command is issued. If the seek command is valid but an unformatted or non-standard diskette is mounted on the drive, unit check with an appropriate indication in the sense bytes (for example intervention required or equipment check in sense byte 0, and an error message such as "no ID field found") is given, depending on the type of error detected.

Channel end is presented:

- After the four-byte seek address has been transferred from processor storage to the attachment, or
- When the count in CCW bits 48 through 63 has been reduced to zero, or
- When a Halt I/O or a Halt Device instruction is given for the device.

Device end is presented depending on the operation allowed by the define operations command:

- If write operations are allowed, device end occurs after the access mechanism is positioned at the specified cylinder.
- If read operations are allowed, device end occurs after the access mechanism has been positioned at the specified cylinder, and the required records indicated have been transmitted to the attachment buffer.

Read IPL (02)

To perform initial program loading, the 'read IPL' command:

- Initializes the "allowed operations" byte to allow read operations.
- Moves the access mechanism to cylinder 0, if it is not already positioned there.
- Reads records from track 0 starting at record 1 and stores them in the attachment buffer.
- Transfers record 1 from that attachment buffer to processor storage.

Channel end is presented:

- When the 128 bytes of record 1 have been transmitted to processor storage, or
- When the count in CCW bits 48 through 63 has been reduced to zero, or
- When a Halt I/O or Halt Device instruction is given for the device.

If record 2 is available in the attachment buffer device end is presented, otherwise device end is presented after record 2 and subsequent records are read. If a unit check occurred at channel end time, device end accompanies channel end. In that case, Read IPL must be reissued after restoring the ready state.

Read Data (06)

The 'read data' command:

- Reads one record from the attachment buffer into processor storage, and
- If the attachment buffer is empty, transmits the next record group from the diskette to the attachment buffer unless the record transferred to processor storage was the last on the track.

Channel end is presented:

- After the record has been transmitted, or

- When the count in CCW bits 48 through 63 has been reduced to zero, or

- When a Halt I/O or Halt Device instruction is given for the device.

Device end is presented when the next record is available in the buffer. Device end always follows channel end for the last record on a track. If a unit check condition exists at channel end time, device end accompanies channel end. If the count is smaller than the record size, incorrect length is indicated (if not suppressed) and only the specified number of bytes is transferred. If the count is greater than the record size, data transfer ends at the record boundary and incorrect length is indicated (if not suppressed).

When a read data command has been executed for the last record on the track, a seek command must be given, before reading from the next track can continue, because implicit seeks to the next track are not executed.

If this rule is violated, further read data commands end with unit check (command reject) in the initial status.

For read operations, the CCW count of the define operations command is ignored, that is, there is no limit on the number of read commands that may be issued, except that no reading beyond record 26 is possible without a seek operation.

When a control record with the flag character D or F is encountered, the control flag is sent as the first byte, and the remaining 127 bytes follow the flag byte in ascending order. The logical sequence of this record is maintained relative to the other records on the same track. Unit check presentation for these two types of control records is controlled by the define operations byte 1, bit 2 (see "Define Operations").

If a control record with the flag character '.' is encountered (the sector has a surface defect), the result is a data check and "permanent error" set in the sense data. The operating system can mark a record as defective to force the operator to reformat the diskette. If a diskette has been re-initialized after an error, a record marked '.' can normally not be encountered because the attachment checks the record ID which shows where the track is physically located and thus finds the alternate track. Therefore, if a data check is encountered, the diskette should be re-initialized on a device such as 3740, or equivalent. The standard diskettes have on the applicable surface(s) 75 good tracks one of which (track 0) is used as label track, and the others (tracks 1-74 or 1-75) are used for data exchange. Either one or two tracks can be used as alternates, the choice being made at initialization time.

Any data checks or equipment checks from causes other than reading a control flag result in a unit check at channel end time, "automatic retry" being indicated in the sense information. The unit check is given to the command that attempted to read the record associated with the error. Automatic retry is an indication that advises the operating system to perform a seek operation with subsequent re-issuing of the read data command.

After every unit check associated with a read data command, a seek command must be given. Otherwise, a unit check with 'command reject' in the sense data occurs to alert the program to the fact that orientation may be lost.

For programming similarity to "write" channel programs, a no-op command should be chained to the last read data command in a read chain. The purpose of such a no-op is explained under "No-Operation".

Write Data (05)

The 'write data' command writes a data mark and transfers one record from processor storage to the diskette. If less than 128 bytes are specified, incorrect length is indicated (if not suppressed) and the record is padded with zeros up to the record boundary. If the count exceeds the record size, incorrect length is indicated (if not suppressed) and the record is written up to the boundary.

Channel end is presented:

- When the 128 bytes have been transferred to the buffer, or
- When the count in CCW bits 48 through 63 has been reduced to zero, or
- When a Halt I/O or Halt Device instruction is given for the device.

Device end for all write commands other than the last one in a "diskette block" is presented when space is available for the next record in the attachment buffer. If no space is available device end will be presented after the attachment buffer is written onto the diskette. A diskette block consists of the number of records allowed between seek commands (which may range from 1 to 26).

For the last write command, device end occurs when all records issued since the last seek command have been written and CRC-checked.

If there are write or CRC errors, device end and unit check are presented with an "automatic retry" in the sense data. The record number in error will be indicated in the sense data. To simplify retry, a no-op command should be chained to the last write command (see No-Operation below).

When a write command has been executed for the last record on the track, a seek command must be given before writing can continue on the next track. Implicit seeks to the next track are not executed. If this rule is violated, the write command receives unit check with 'command reject' in the sense data at initial selection.

Following a seek command, the number of write commands issued must not exceed the CCW count specified in the define operations command. Excess write commands are rejected at initial selection (see the "define operations" command).

No-Operation (03)

The no-operation command has no effect on the diskette. Channel end and device end are presented at initial selection.

If the device is not operational because of an 'intervention required' condition, a unit check occurs.

This command is used to enhance error recovery from write errors. The no-op command is used to provide a channel interrupt after all CRC checking has been done, and consequently, to allow retry of a failing write channel program. In system architecture, only one channel end interrupt is given to a source program. This single channel end interrupt is always associated with the last command in the chain. If a unit check occurs before or with channel end, the channel program can be retried by data management routines. If a command-chained channel program ends with a write command that results in a device end unit check, it cannot be retried by data management routines. Therefore, so that the channel program can be retried, the last channel end should not come from the last write command in the chain.

Write Control (21)

The 'write control' command writes a control mark and transfers data like the write data command except that the first byte transferred should be a valid control flag, otherwise data check will occur when this record is read (see "read data" command). However, the write control command transfers data from storage without checking if the first byte is a valid control flag (any code is accepted). Valid control flags are the characters D and F. The expressions F and D are not hex codes but graphics in EBCDIC. Only the flag byte is of logical significance in a control record, the remainder may be any data (pad characters) which are nevertheless required for CRC generation and checking. If less than the applicable number of bytes has been specified, incorrect length is indicated (if not suppressed) and the remainder of the record is padded with zeros by the attachment.

Channel end is presented when the data transfer from processor storage to the attachment buffer is completed (or stopped). Device end is presented when space is available for the next record in the attachment buffer. If no space is available, device end will be presented after the attachment buffer is written onto the diskette.

For the last write command in a diskette block, device end occurs when all records in the diskette block have been written and CRC-checked.

Sense (04)

The sense command transfers up to 6 sense bytes (byte 0 to 5) from the attachment to processor storage. The first three bytes contain error information, the last three bytes contain orientation information, i.e. cylinder, head and record number. The error information is always tied to the unit check which signals the error.

The orientation information belongs to the error-record when unit check is indicated. However, if no unit check occurred, the orientation information pertains to the next record, i.e. the record that would be transferred by the next read or write command. Consequently, a sense command can be used for program reorientation or look-ahead operations. (For details, see sense information).

Channel end and device end are presented together for a sense command after the last sense byte has been transferred, or when the count is reduced to zero, or a Halt 1/0 or Halt Device instruction is issued.

The error information (first 3 bytes) of the sense data is reset by any next command other than sense or no-op. The orientation information is always updated for each data transfer command. This sense command transfers seven bytes of device identification data from the attachment to storage. The information is transferred regardless of whether the device is ready or not. The bytes contain the following:

Byte 0 = always hex 'FF' Byte 1 = Control unit type number (43) Byte 2 = Control unit type number (31) Byte 3 = Control unit model number (00) Byte 4 = Device type number (35) Byte 5 = Device type number (40) Byte 6 = Device model number (01)

The control unit type and model number (Bytes 1 to 3) is the model number of the processor into which the diskette drive is integrated. The diskette drive is identified as 3540 Model 1.

Feed (17)

The feed command makes the device not-ready and brings the message "load next diskette" to the user diskette control screen. The operator is thus requested to remove the mounted diskette (if any) and insert another one. In this way a feed opeation is "emulated" on a device that has no feed mechanism. The command presents channel end and device end in the initial selection. The diskette drive enters the operational state automatically when a diskette is mounted, that is, when the cover is opened, then closed, and the diskette reaches operating speed.

Diskette Drive Reset States

The diskette drive is affected by various types of reset, as follows:

<u>Power-On Reset</u>. The attachment is set to an error-free state with the buffers and internal controls set to zero, and the drive set to the ready state. The access mechanism is positioned to track zero when the first command is issued to the device.

<u>Program-</u>, <u>Initial</u> <u>Program-</u>, <u>and</u> <u>Clear</u> <u>Resets</u>. These operator-initiated machine resets preserve the ready state of the diskette drive, but conclude data transfer (if any) and reset all status information and interruption conditions. The diskette drive's subchannel is placed into the available state.

The buffer contents are preserved and the access mechanism's position is retained. Any error conditions are reset.

<u>Halt 1/0</u>, <u>Halt Device</u>, and <u>Clear 1/0</u>. These instructions terminate data transfer at the next record boundary if data transfer is in progress. If the instruction is given after channel end but prior to device end presentation, the drive continues to the point where device end is signaled.

Manual Operations

When the character G is entered in the mode select picture, the "user diskette control" menu appears with the following options:

<u>Stop Device</u>: When the character S is entered, the device becomes unavailable as soon as the current operation (if any) is completed. The device remains unavailable until the start function is performed, or a reset occurs, or a new diskette is inserted (cover opened, then closed).

<u>Start</u> <u>Device</u>: When the character N is entered, the stopped state is removed and a device end status is presented. The device is now conditioned to receive I/O commands. The device end status is given each time the start function is executed, regardless of whether the drive was stopped or not (attention function).

<u>Note</u>: Even though the device is started, a subsequent 1/0 command (other than Sense, Sense 1/0, or No-op) is executed successfully only when a diskette is mounted and the cover is closed.

<u>Reset Device</u>: When R is entered, the start function is performed as described above and the device is conditioned to move the access mechanism to its home position on receipt of the next command. The recalibrate motion occurs prior to the execution of that command. The reset function resets all sense bytes to zero, and generates a device end (attention function).

Diskette Unit Status

The unit status is reflected in CSW bits 32 through 39. The meaning of the individual bits is as follows:

<u>CWS</u> <u>bit</u>	Meaning
32	Attention (not used)
33	Status modifier (not used)
34	Control unit end (not used)
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception (not used)

<u>Busy</u> (<u>Bit</u> <u>35</u>). This bit indicates that the diskette drive is either executing a previous command, or device end from some previous operation is pending in the status byte. Busy is not reset as long as device end is pending.

Busy is also presented together with device end when a Start 1/0 instruction clears a pending device end condition.

<u>Channel End</u> (<u>Bit 36</u>). Indicates that the channel has completed the data transfer and is free again. If no data transfer is involved, channel end is given at initial selection.

<u>Device End (Bit 37)</u>. Indicates that the device is free to accept a new command. Device end may coincide with channel end or may be presented later, depending on the type and timing of commands. Device end is also presented alone when the operator gives the start or reset command at the console. The operating system then knows that the device is no longer in the stopped state and access is now possible. A Test I/O or Start I/O instruction would receive condition code O in response.

<u>Unit Check (Bit 38)</u>. Unit check is a summary indication for errors which are detailed in sense bytes 0 and 1. Unit check can be presented at initial selection or channel end or device end time, depending on the command and the type of error. Unit check is, however, usually presented with channel end and device end.

Diskette Sense Information

When a sense command is issued, the attachment provides 6 bytes of sense information. The first 3 bytes contain error information associated with the unit check indication, the last 3 bytes contain orientation information.

Sense Byte O

Bit Number	Meaning
0 1 2 3 4 57	Command reject Intervention required Bus out check Equipment check Data check Not used
<u>Sense Byte 1</u>	
Bit Number	Meaning
0 1 2 3 4 57	Permanent error Automatic retry Motion malfunction Retry after intervention complete Special record transferred Not used
<u>Sense Byte 2</u>	
Bits 07	Represent a hexadecimal number which uniquely identifies each error situation. The number is a directory for recovery actions, as well as a log for the service representative.

Sense Bytes 3, 4, and 5 (orientation)

Byte 3 = Cylinder number in binary notation

Byte 4 = Head number

Byte 5 = Record number in binary notation

Sense bytes 3, 4, and 5 point to the next record to be read or written when no unit check occurred. In case of unit check, the orientation information belongs to the record for which the unit check was given. If a seek command with an invalid seek address is issued, bytes 3, 4, and 5 reflect the current position of the access mechanism.

In detail the sense bytes are:

Sense Byte O

Sense byte 0 contains information required for recovery, as follows:

Command Reject.

Bit 0 can be set either at initial selection or at device end time.

At initial selection, bit zero refers to violation of programming rules, for example:

- an invalid command (not in the command set) was issued
- a command not permitted by the define operations command was issued.
- a write command exceeded the CCW count specified in the define operations command (i.e. the write command is the first excess command).
- a command (read or write) was issued after a unit check and no preceding seek command was issued.
- a read or write command is issued but no define operations command was issued.

At device end time, bit zero refers to incorrect detail specifications in a define operations command or seek command. The following violations are included:

- a define operations or seek command specifies less than four bytes (insufficient count).
- a define operations command allows both read and write commands (conflicting statement).
- a define operations command allows write commands but specifies an invalid CCW-count. (All write commands are then rejected).
- A seek command contains an invalid seek address

Error Recovery: The program must be corrected. Read the applicable parameters from the label cylinder of the currently mounted diskette (using the Read IPL command).

Intervention Required.

This indication informs the operating system that operator intervention is required to continue operations. The basic cause is an unavailable condition of the drive. For example, the drive may be in the stopped state, there may be no diskette mounted or the cover may be open. If the operator fails to react to the feed command (which makes the drive not-ready), the drive remains likewise unavailable. Hardware malfunctions such as a torn drive belt, a defective index pulse sensor, or a jamming diskette lead to the same indication.

Error Recovery: Issue a message to the operator calling for intervention (load diskette, start drive, etc). The "Disk" indicator appears on the operator console automatically so that he can get further information from the menu.

Bus Out Check.

Bus-out check indicates that the diskette attachment received data with bad parity from the bus-to-bus adapter through the IC-bus.

Error Recovery: Immediate reissuing of last command (without any other intervening action).

Equipment Check.

Can be indicated at channel end or device end time. Equipment check is associated with malfunctions in the attachment such as failure to recognize address markers, ID field errors, parity checks in registers or a mismatch between the record length specified by the define operations command and the record length found in the ID-field of a record.

Error Recovery: as indicated by sense byte 1 bits 0 or 1.

Data Check.

Is set at channel end or device end time when errors associated with the contents of data or control records have occurred. Such errors are caused by invalid CRC or not equal CRC comparison, or invalid control record flags detected during a read command. Any data other than the characters D or F are considered invalid as control record flags (that is, as contents of the first byte). Therefore, it is possible to force a data check simply by writing some invalid flag, a technique which is commonly used to mark a record as defective so as to force reformatting of the diskette.

Error Recovery: as defined by sense byte 1, bits 1 or 4.

Sense Byte 1

Sense Byte 1 contains error recovery information for the operating system. The information in sense byte 1 is appropriate for the conditions indicated in sense byte 0, as follows:

Permanent Error.

Permanent error may be set together with command reject, equipment check, or data check. Permanent error warns the operating system to issue a message to the effect that either the diskette is the wrong type or damaged (and should be reinitialized) or, in certain cases of equipment check, that assistance from a service representative may be required. In any case, a retry is usually not successful, the job should be terminated and the sense bytes logged. A message based on the error information contained in sense byte 2 should be given to the operator.

Automatic Retry.

Is an indication for the operating system that immediate repetition of the failing command (without issuing any intervening commands) is recommended. Automatic retry accompanies those cases of equipment check or data check where a temporary malfunction is suspected (e.g. bus-out check). In any case, the operating system should retry the failing operation ten times. Operator assistance is not required. If a retry is successful, continue normal program execution, otherwise post a permanent error condition and proceed with the appropriate corrective action (see "Permanent Error" above). It is suggested that the retry starts at a disk block boundary. A retry must always include a seek command.

Motion Malfunction.

Is set where intervention required is indicated for abnormal reasons such as mechanical inability. A message should be issued indicating to the operator that the old diskette should be removed and a new diskette inserted. The motion malfunction causes the device to lose the ready state.

Retry after Intervention Complete.

Is indicated where intervention required is indicated for normal reasons (e.g. next diskette required) where the intervention will restore normal operating conditions. The indication is also given for certain abnormal cases (e.g. inability to recognize the ID-field, or use of an unformatted diskette) where the error can possibly be overcome by re-inserting the same or a new diskette. To the operating system, the indication means to wait for the not-ready to ready transition, (single device end), then to issue the failing command again.

Special Record Transferred.

Is indicated when control records with a character 'D' or character 'F' flag have been read while unit check was not suppressed in the allowed operations byte, hence, data check was indicated in sense byte 0. The operating system should check the first byte of the input record in processor storage. This first byte is the flag which specifies whether the record is deleted or relocated, as the case may be. Further disposition is program dependent. The attachment recognizes the D and F characters in EBCDIC (Hex C4, C6) and ASCII (Hex 44, 46).

Sense Byte 2

Sense byte 2 contains a Hex code for all errors, except command reject cases (which are programming errors). The information in sense byte 2 is a directory to recovery actions as well as an error log. The contents of sense byte 2 should be recorded on SYS REC for later retrieval via EREP.

Error Definition

The errors that may occur in the diskette drive are:

- Feed errors
- ID field errors (both when writing or reading data)
- Data record errors (both when writing or reading data)
- Miscellaneous errors (including invalid combinations of commands or control flags)

These categories (except miscellaneous errors) are listed by hex code and console indication in the following text.

Visual Error and Status Indications

Whenever the diskette needs attention, the word "Disk" appears in the status area of the operator console screen. The operator should then select the "user diskette control" menu (by entering the character G into the mode select picture). The diskette control menu shows the actual diskette status by one of the following messages:

- Started
- Not Ready
- Load next diskette
- Defective diskette

The messages have the following meaning:

<u>Started</u>: Indicates that a stopped state (if any) has been removed so that the diskette drive may be accessed by commands.

<u>Note</u>: Commands other than sense, sense I/O, and no-op can be executed successfully on a started drive only when a diskette is inserted and the cover is closed.

<u>Not-Ready</u>: Indicates that a command was issued either to a stopped drive or to a started drive which has no diskette inserted or the cover open. Not-ready can also indicate a hardware malfunction such as a torn drive belt, a defective index pulse sensor, or a wrong type of diskette (diskette wrongly inserted, diskette with offset index pulse perforation, etc). Some form of operator intervention is required, e.g. inserting new diskette, closing the cover, or performing the start function. <u>Note</u>: Not-ready is the normal state when a feed command was issued.

Load Next Diskette: Indicates that a feed command was issued. The drive is automatically not-ready so that the operator may safely insert a new diskette. It is sufficient to insert the new diskette, then close the cover to make the drive operational.

<u>Defective</u> <u>Diskette</u>: Indicates some form of malfunction such as inability to read an ID. A defective or unformatted diskette is suspected. The operator should insert a new diskette (or call for service, if required).

ID Errors During Read or Write Operations

Most errors associated with the ID field are announced to the operating system by equipment check, permanent error or automatic retry and the console indication "defective diskette" error code is given because the operator cannot intervene. The error code displays the contents of sense byte 2 when an error has occurred.

However, two types of ID errors, "no ID address marker found", and "incorrect cylinder" (access malfunction), may be recoverable. For these two cases, intervention required is indicated and retry after intervention complete. The idea is to re-insert the same (or perhaps another) diskette and try again. The error code in sense byte 2 is as follows:

Error Code	Type of ID field Error	<u>User Diskette</u> Control <u>Indica</u> 1
AE	No ID field addr. marker found (intervention required, motion malfunction, and retry after intervention complete)	Not ready, defective disk¢
AF	<pre>ID field read with wrong cylinder number (intervention required, motion malfunction, retry after intervention complete)</pre>	Not ready, defective diske
E9	ID field read with correct CRC but with incorrect head number, (something other than 0 or 1), or unknown length (equipment check, permanent error)	No indication
E2	Record not found but at least one valid ID found, CRC good (equipment check, auto retry)	No indication
Ε3	Fast or slow diskette speed (equipment check, auto retry) Note: This error is used as an interim error when an 1/0 operation is issued to the attachment which is not ready (cover is opened). Because the error is retriable, a subsequent retry operation will result in unit check with inter- vention complete indicated in the sense data.	Not ready

Read or Write Data Errors

Write and read data errors during plain reading or readback after writing (as occurs on the last record) are indicated by equipment check and automatic retry (or permanent error). The hex code for the individual case is as follows:

Error Code	<u>Type of Read Data Error</u>	<u>User</u> <u>Diskette</u> Control Indication
D3	Data or delete control record CRC-error (data check, auto retry)	No indication
Ε4	Attachment overrun (equipment check, auto retry)	No indication
DO	Special record transferred (data check, spec record transf.)	No indication
D9	Control flag invalid, that is, contains something other than C4 or C6 (EBCDIC) or 44 or 46 (ASCII) (data check, permanent error)	No indication

Miscellaneous Errors

These errors are not indicated by a hex code in sense byte 2. Instead, command reject is given. This indicates errors such as:

- violating the CCW count in the define operations byte (by excess write commands).
- invalid specifications in the define operations command.
- invalid seek address.
- command retry without preceding seek command (after unit check).
- omitting a define operations command but issuing read or write commands.

Chapter 6. 3340/3344 Direct Attachment

The 3340/3344 direct attachment is a feature that allows up to two 3340-A2s to be connected to the DASD adapter. Up to three 3340/3344 model B units can be attached to each 3340-A2. The feature consists of microcode which is loaded during the IML process. At this time the necessary data areas are initialized or generated and a buffer to hold one track of 3340 data is assigned in processor storage. To improve performance on the sequential processing of disk files the operator can specify up to seven additional buffers at IPL. Usable processor storage is reduced according to the number of buffers specified.

The 3340/3344 direct attachment operates in ECPS:VSE mode or in System/370 mode. Either block multiplexer or selector mode can be set. The direct attachment is served by unshared subchannels. One subchannel is provided for each 3340 and 3344 drive. No conversion is required when System /370 users transfer 3340/3344 data to the 4331.

The 3340/3344 direct attachment supports all 3340/3344 operations, including string switch operations (see note below) but excluding rotational position sensing and diagnostic operations.

Note: If a 3340-A2 with string switch is attached to the DASD adapter, only the static assignment of a shared string to one processor at a time is supported.

Commands and Instructions

With the exceptions noted below, the commands and operations are as described for the 3340/3344 in <u>Reference Manual for IBM Integrated Storage Control</u> GA26-1620. Operations are compatible with the results obtained on channel-attached 3340/3344s.

Diagnostic Commands

The 'diagnostic load', 'diagnostic write', and 'read diagnostic status 1' commands are not accepted by the 3340/3344 direct attachment. When given, these commands cause the unit check bit and the command reject bit to be set.

Write Commands

During write operations used to transfer a 3340/3344 track from a processor storage buffer to the direct access storage, an error may occur. For all errors except 'invalid track format' the write operation is retried up to ten times and if the operation is still unsuccessful the 'channel control check' bit is set.

String Switch Commands

The 'device reserve' and 'device release' commands are carried out only in a 4331 which has string switch support. Otherwise, these commands are carried out like a 'sense I/O' command.

Restore Command

For compatibility with other IBM direct access storage devices the 'restore' command is accepted and treated as a no-operation.

Halt Instructions and Clear I/O Instruction

The 'halt 1/0', 'halt device', or 'clear 1/0' instructions may terminate a chain of operations without transferring back to the 3340/3344 the data accumulated in the processor storage buffer from write operations in the user's program. If a command chain containing write commands is halted, the CSW may therefore not reflect the true status of the disk track.

Sense I/O Command

A 'sense 1/0' operation identifies the device on which it is executed. The identification is seven bytes long.
Byte	Contents	Meaning
0	FF	ldentifies data as sense 1/0 data
1	43	
2	31	Defines control unit (4331 Processor)
3	00	
4	-33	Defines device type
5	40/44	<i>,</i> ,,
6	XX	10=35 mega module, 20=70 mega module,
		00=not applicable

Status Information

The following text provides information on the unit status and channel status additional to that given in <u>Reference</u> <u>Manual for IBM Integrated Storage Control</u>, GA26-1620. The status is available in bits 32-47 of the CWS after a command chain has been normally or abnormally ended:

Unit Status

Attention (Bit 32)

The attention bit is set when an asynchronous device status is detected.

Unit Exception (Bit 39)

The unit exception bit is set when an end-of-file condition is detected during the operations listed under "unit exception" in the above referenced manual. In the 3340/3344 direct attachment, however, a 'multiple count, key, data' command does not recognize an end-of-file condition.

Note: When a command chain is terminated during initial selection (if, for example, the first CCW has an invalid op-code), a so-called short store is performed in the CSW. Only the unit and channel status is replaced. Channel end and device end are not included in the status.

When a command chain is terminated during the initiation of a command other than the first (for example, during an invalid command sequence), a full CSW is stored, but without channel end and device end indication. The following paragraphs supplement the information on channel status given in the principles of operation manuals.

Program-Controlled Interrupt (Bit 40)

The program-controlled interrupt (PCI) bit is set in the ending status of a chain if any of the CCWs in the chain had this bit on. The full function of PCI is not supported by the attachment.

Channel Data Check (Bit 44)

This bit is not used by the attachment.

Channel Control Check (Bit 45)

The channel control check bit is set when an unusual condition occurs at the channel that can be related to the attachment. Channel control check is also set when a permanent unit check other than 'invalid track format' occurs during a write operation.

Interface Control Check (Bit 46)

This bit is not used by the attachment.

Sense Information

The sense information for the 3340/3344 is stored in 24-byte buffers in processor storage. There is one buffer for each device.

The seven formats of sense data described in <u>Reference</u> <u>Manual for IBM Integrated Storage Control</u>, GA26-1620, apply also to the <u>3340/3344</u> Direct Attachment, except for formats 2 and 3 which are not used.

Sense Bytes 0-7

Sense bytes 0-7 are common to all formats. The following exceptions and additions to the above referenced manual should be noted.

Sense Byte 0

Intervention Required (Bit 1)

This bit is set if the addressed device is not on-line (not ready, in maintenance mode, or not attached although the subchannel is installed). The bit is also set if execution of a command chain is terminated due to an asynchronous device end occurring while no native operation is in progress at the addressed device. In this case, the CSW may not reflect the true state of the disk track.

Data Check (Bit 4)

This bit is set if an uncorrectable data error occurred during reading or searching. The message code in sense byte 7 gives further details. (Correctable data checks are corrected by the attachment).

Sense Byte 1

Permanent Error (Bit 0)

This bit is not used.

Invalid Track Format (Bit 1)

This bit indicates an attempt to write data exceeding the track capacity. It is also set if during a read or search operation the index is detected in the gap following the count or key field.

Format 4 and 5 - Byte 13

The sector number is not provided. Instead, the byte contains X'80' if the drive has RPS, otherwise X'00'.

Format 4 - Message 5

This condition (no synchronization byte found for the count field) does not produce an error, since it is interpreted by the attachment as 'normal end of track'. Thus, if the condition is actually caused by an error, it will appear to the user as a 'no record found' condition.

Format 6 - Usage and Error Statistics

There is no direct relationship between channel program execution and usage and error counter updates as for other 3340/3344 attachments. Instead, these counters are updated on request from the 3340/3344 attachment during internal operations executed by the DASD adapter. The counter values may therefore be different from those obtained by other 3340/3344 attachments.

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Chapter 7. Communications Adapter

Teleprocessing facilities are available for the 4331 through the optional Communications Adapter (CA) which enables communication between the processor and communication terminals and/or other processors at remote locations.

This chapter outlines the capabilities of the CA and then describes the line control procedures. The characteristics, commands, status reports, and sense information for each line control procedure are also described.

The CA of the 4331 performs all the functions of, and is equivalent to, a byte multiplexer channel with a maximum of eight subchannels. Each subchannel consists of a line attachment to provide the control functions for the communication line connected. A total of eight communication lines (start/stop, binary synchronous control, and synchronous data link control) may be attached.

For start/stop and binary synchronous lines the CA operates functionally as a 2703.

<u>Programming note on initial status reporting</u>: The CA presents exceptional situations as early as possible. The ending conditions that arise for an SIO operation may therefore be different from those occurring with a 2703. For instance, an intervention required causing a unit check may be presented in response to an SIO instruction with condition code 1 (meaning that a CSW has been stored), instead of being reported by a separate interruption. If the unit check bit is presented in response to an SIO instruction it is not accompanied by channel end and device end.

The CA allows for a total aggregate data rate of 64 kbps. Speeds above 9,600 bps are limited to line number 1.

Suitable modems can be connected as separate units. An integrated 1200 bps modem is available. A maximum of two autocall interfaces can also be provided.



Figure 15. Structure of Communications Adapter

Figure 15 shows the types of communication lines that can be served by the CA. Three different line control procedures may be used depending on the characteristics of the data terminal equipment on the other end of the communications line. They are:

- IBM Terminal Control Type 1 for transmission speeds from 75 to 1200 bps. This line control is asynchronous (start/stop).
- Binary Synchronous Communication (BSC) for transmission speeds from 600 bps to 56,000 bps or 64,000 bps.
- Synchronous Data Link Control (SDLC) for transmission speeds from 600 bps to 56,000 bps or 64,000 bps.

Note: When BSC or SDLC lines are operated with the 1200 bps integrated modem, a low-speed option of 600 bps is selectable by the operator.

All three types of line control are available when IMPL has been performed. If low-speed lines are operating at the same time as the high-speed line, the maximum speed of the high-speed line is reduced to 50,000 bps.

IBM Terminal Control - Type 1

The command set, the line control characters, and the transmission code comprising the IBM Terminal Control - Type 1 are designed for asynchronous start/stop communication with the following remote data terminal equipment (DTE):

IBM 1050 Data Communication System (using 6-bit BCD with shift)

IBM 1060 Data Communication System (using 6-bit BCD without shift)

- IBM 2740 Communication Terminal (using 6-bit BCD with shift)
- IBM 2741 Communication Terminal (using 6-bit BCD with shift)
- IBM 3767 Communication Terminal
 - IBM 5010 Processor

• IBM 5100 Portable Computer

The code structures are shown in Appendix D, Figures 24-28.

Line Control Characters

Six line control characters are used for Type 1 terminals:

(B) End of Block

The (B) ('circle B') character indicates the end of a block of text.

(C) End of Transmission

The (C) character indicates the end of a transmission or the beginning of either a polling or a selection operation.

(D) End of Address

The (D) character indicates the end of an address (if any) and, consequently, the beginning of text. It is a positive response to polling.

(N) Negative Response

The (N) character indicates for polling that a polled terminal has nothing to send, or for addressing, that the terminal cannot receive (or has detected a transmission error).

(S) Start of Address

The (S) character indicates a start-of-address and is used, for example, when the Station Control feature is installed in a 2740 Communication Terminal. (S) is used during addressing and concerns only the remote station.

(Y) Positive Response

The (Y) character indicates that the addressed terminal is ready to receive or has accepted a block of text. Note: For a listing of all applicable characters see 'Appendix D, CA Code Tables'.

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Transmission Code

The transmission code for Type 1 terminals is six-bit BCD, also known as the paper tape transmission code (PTTC). The code structure is shown in the following table:

Storage Byte:	0	1	2	3	4	5	6	7	
Interpreted as:	S	B	Α	8	4	2	1	C	
Transmission code:	start	B	Α	8	4	2	· 1.	C	stop

The S represents the shift bit, which indicates upper case when set, and lower case when zero. During transmission, the line attachment inspects the shift bit of each character before it is stripped off. The inspection shows whether or not the shift bit is the same as that of the preceding character. If a shift change is detected (a change from upper case to lower case, or vice versa), the line attachment generates an appropriate shift character (upshift or downshift) which is the 'n' transmitted ahead of the character that caused the shift change. This allows the remote DTE to operate its shift mechanism.

When the line attachment is receiving, it inspects incoming shift characters but does not transfer them to processor storage. The characters that follow the shift character are stored with a shift bit that reflects the change effected by the shift character. The start and stop bits are added for transmission and deleted upon reception.

Commands

Hex	<u>Command</u> Code <u>Command</u> <u>CCW Bits</u>
	0 1 2 3 4 5 6 7
02	0 0 0 0 0 0 1 0 Read
01	0 0 0 0 0 0 1 Write
OA	0 0 0 0 1 0 1 0 Inhibit
06	0 0 0 0 1 1 0 Prepare
27	0 0 1 0 0 1 1 1 Enable
2F	0 0 1 0 1 1 1 1 Disable
29	00101001Dial
OD	0 0 0 0 1 1 0 1 Break
09	0 0 0 0 1 0 0 1 Poll
03	0 0 0 0 0 0 1 1 Control no-op
13	0 0 0 1 0 0 1 1 No-op ('sadzero')
17	0 0 0 1 0 1 1 1 No-op ('sadone')
1B	0 0 0 1 1 0 1 1 No-op ('sadtwo')
1F	0 0 0 1 1 1 1 1 No-op ('sadthree')
2B	0 0 1 0 1 0 1 1 No-op ('set line mode')
04	0 0 0 0 0 1 0 0 Sense
Ε4	1 1 1 0 0 1 0 0 Sense 1/0

Note: The 'sadzero', 'sadone', 'sadtwo', 'sadthree', and 'set line mode' commands (hex 13, 17, 18, 1F, and 2B) are accepted and treated as no-operations.

'Read'

The 'read' command causes data to be transferred from the addressed line to the processor storage address specified in CCW bits 8 to 31. Data transfer continues in ascending order of this address. To ensure that data is actually received on the communication line, a three-second timeout is started when a 'read' command is given. If the time elapses before data is received, the 'read' command ends with unit check (bit 38 in the CSW) set and the timeout complete bit is set in sense byte 0. If a character is received before the three-second timeout has elapsed, a 25-50 second timeout is started for each subsequent character.

The data received is normally in the form of a stream that consists of line control characters and text characters. The operations within the CA and the way in which the 'read' command is terminated depend on the data received, as described in the following text.

If a (D) is received, it is recognized as a line control character if the line attachment is in control mode (the line attachment is in control mode after enable, disable, or end of transmission). Recognition of a (D) causes the line attachment to set text-in and lower case modes. The data that follows (D) will be text.

In text-in mode, when the next incoming character is received, the line attachment begins to accumulate the longitudinal redundancy check (LRC) character. Each text character causes the LRC to be updated. Reception continues as long as successive text characters arrive within 25-50 seconds. All characters are stripped of their start and stop bits (these bits do not enter processor storage). Shift bits are inserted into the byte prior to storing the byte into processor storage.

In text-in mode, further (D), (N) or (Y) characters are not recognized as line control characters, but are treated as text characters.

The read operation continues until a timeout occurs, a (B) or (C) is received, or the length count is exhausted, whichever occurs first.

Delete and Idle Characters.

If delete (BA8421C all equal to ones) and idle characters (BA8421C equal to 1011110) are received, they are included in the LRC accumulation, but are not transferred to processor storage.

Shift Characters Received.

If a shift character is received it is inspected but not transferred to processor storage. The following characters received are stored with a shift bit that corresponds to the shift change effected by the shift character. The shift character is included in LRC accumulation.

(B) Received.

Receipt of (B) indicates that the end of the text block has been reached and the line attachment stops LRC accumulation. The next character received is assumed to be the LRC character from the remote terminal. This LRC character is compared with the LRC accumulated in the line attachment and if both are the same, channel end and device end are presented for the 'read' command, otherwise unit check is presented together with channel end and device end, and the data check bit is set in sense byte 0. The attachment remains in text-in mode.

(C) Received.

Receipt of (C) indicates the end of transmission, and channel end, device end, and unit exception (bits 36, 37, and 39 in the CSW) are presented to terminate the 'read' command. The line attachment goes back to control mode and lower case mode.

Timeout.

If a timeout elapses, the 'read' command ends with channel end, device end, and unit check. The timeout complete bit in sense byte 0 will be set if 'data carrier received line signal detect' (a modem signal) is still on.

'Write'

The 'write' command causes data from the processor storage location specified in CCW bits 8 to 31 to be transmitted over the addressed communication line. One or more characters can be sent. If more than one character is sent, the additional characters are taken from processor storage in ascending order of address. The action taken by the CA depends on the data being transmitted, as described in the following text.

(D) Transmitted.

If a (D) is transmitted, any data that follows will be text. Transmission of (D) places the line attachment in text-out mode, provided that it was previously in control mode or text-in mode. The (D) also puts the line attachment in lower case mode.

When the text-out mode is set, the line attachment begins to accumulate an LRC character. The LRC character is updated with each additional character that is transmitted. Text-out mode causes the shift bit of each text character to be inspected before it is removed. If a text character has its shift bit set and the immediately preceding character had its shift bit at 0, the line attachment generates, and transmits, an upshift character. Simultaneously, it sets upper case mode before the next text character is transmitted. If the line attachment detects a change to lower case, the converse happens. The LRC character is also updated with the shift characters.

Transmission (writing) continues until a (B) is detected in the output stream or until the length count reaches zero. Transmission occurs at the speed associated with the addressed line. The line attachment converts the processor storage data to the appropriate code (6-bit BCD) and provides the start bit at the beginning and the stop bit at the end of each character.

(C) Transmitted.

If a (C) is transmitted, the LRC characters are reset in both the line attachment and the receiving station. The 'write' command does not end. (Usually a polling or addressing character follows (C).)

(B) Transmitted.

If a (B) is transmitted, LRC accumulation stops and the LRC character is transmitted immediately after the (B). Then channel end and device end are presented for the 'write' command. (B) is the only character that ends a 'write' command.

Steady Space Level Sensed.

If a steady space level for more than 2 character times is sensed on the 'received data' line and the CA is configured for write interruption, the 'write' command ends with unit check, and intervention required is set in sense byte 0.

Notes:

- 1. The write interruption feature requires a four-wire line and/or a duplex modem.
- A 'write' command need not necessarily transmit an address and text. Instead, it may be used to transmit a positive or negative acknowledgement, such as (Y) or (N).

Polling and Addressing with Alternate Read and Write Commands. 'Read' and 'write' commands can be used alternatively to poll or address Type 1 terminals in a multipoint network. The line control sequences for IBM Terminal Control-Type 1 are shown in Figures 16 to 19.

inals (hinal address t select code rd sponse-no send me polling ng hinal address t select code 1	ine Attachment 105	 Reset terminals Terminal address Component select code for printer 1 Terminal ready to receive End of address Message transmission End of block
ninal address t select code rd sponse-no send me polling ng ninal address t select code	 A 1 D Text B 	 Terminal address Component select code for printer 1 Terminal ready to receive End of address Message transmission End of block
t select code rd sponse-no send me polling ng ninal address t select code 1	0 Text B	 Component select code for printer 1 Terminal ready to receive End of address Message transmission End of block
rd sponse-no send me polling ng ninal address t select code 1	0 Text B	for printer 1) Terminal ready to receive End of address Message transmission End of block
send me polling (ng ninal address 7 t select code (1	0 Text B	 End of address Message transmission End of block
ng ninal address 7 t select code (1	B	 Message transmission End of block
t select code (1	B	End of block
1		
	_RC	
dy L		 Check character generated by line attachment
Insmission	<(N	Inaccurate message received
ck T	Fext	 Message repeated (pro- gram-controlled)
acter generated	B	End of block
ssage received L cked and correct chment)	LRC	Check character generated by line attachment
smission	•	Positive message received at terminal
	©	 End of transmission (reset)
	chment)	ismission

Figure 16. Line Control Sequence for IBM Terminal Control-Type 1 with 1050 Data Communication System

Polling

Addressing



Legend

 = Optional loopback (operation repeats before transmission ends)



Polling

Addressing

Line Attachment	2740	Comments	Line Attachment	2740	Comments
©		Reset terminals	©	>	Reset terminals
A	•	Polled terminal address	§	>	Address select
SP	>	Space character	Α	>	Terminal address
4	- D	End of address	SP	>	Space character
4	—Text	Message transmission	4	(Y)	Positive response (ready to receive)
4	- B 4	End of block	0	>	End of address
4	LRC	Check character generated by 2740	Text	>	Message
Ø	,	Positive response	▶ ®	>	End of block
4	-©	End of transmission	 LRC-*		Check character generated by the line attachment
			L	(Y)	Positive response (message correct)
			©	>	End of transmission

Legend

 * Used only on 2740 equipped with the Record Checking feature

---- ->= Optional loopback (operation repeats before transmission ends)

Figure 18. Line Control Sequences for IBM Terminal Control-Type 1 with 2740 Communication Terminal





Figure 19. Line Control Sequences for IBM Terminal Control-Type 1 with 2741 Communication Terminal

Addressing.

Addressing is used to find out if a terminal is ready to receive data. Before addressing can be performed, the line attachment must be in control mode. This can be accomplished by giving a 'write' command that transmits a (C) (end of transmission) followed by the terminal address. The 'write' command must be chained to a 'read' command so that the response can be received as soon as possible. If (N) is received (negative response), the remote DTE cannot receive and the 'read' command ends with channel end, device end, and unit exception set. If a (Y) is received, the remote DTE is ready to receive and the 'read' command ends with channel end and device end.

Polling.

Polling is used to find out if any remote DTE has a message to send. Before polling can be performed, the line attachment must be in control mode. This can be accomplished by giving a 'write' command that transmits a (C) followed by the polling address. The 'write' command should be chained to a 'read' command to obtain the response as quickly as possible. If an (N) is received, the remote terminal has nothing to transmit and the 'read' command ends with channel end, device end, and unit exception set. If nothing is received within three seconds, the command ends with channel end, device end, and unit check. In either case, the line attachment remains in control mode so that polling (or addressing) can continue. If a (D) is received, however, the polled terminal will transmit text. The line attachment therefore goes to text-in and lower case modes, and starts the 25-second timeout for the next character.

'Inhibit'

The 'inhibit' command is similar to the 'read' command, except that neither the three-second timeout at the beginning nor the 25-50-second timeouts between characters are started. The 'inhibit' command may be used whenever it is necessary for the line attachment to wait an unlimited period of time for data.

'Prepare'

The 'prepare' command allows the program to check for meaningful signals on the addressed communication line, and thus find out when a 'read' command should be given. The command is similar to a 'read' although no data is transferred to processor storage. When given, the 'prepare' command checks the communication line for a valid start bit. If a valid start bit is detected, the timing circuits next attempt to detect one complete character including the stop bit. If a character can be assembled, channel end and device end are presented for the 'prepare' command. The assembled character, however, is lost and is not transferred to processor storage.

If no stop bit is found after detection of a start bit and associated character, a 25-second timeout is started. If the timeout elapses before a stop bit is found, the 'prepare' command ends with unit check, and the timeout complete bit is then set in sense byte 0. The lost data bit in sense byte 0, however, is not set, because no data is tranferred to processor storage during execution of a 'prepare' command.

'Enable'

The 'enable' command is a prerequisite for data transmission and reception because it enables the addressed

line attachment to operate. The command also sets the line attachment to downshift mode. If the 'enable' command is given to a line attachment operating a leased line, channel end and device end are set in the initial status. If it is given to a switched line, channel end and device end are set only when the connection with the remote terminal has been established. No data is transferred.

'Disable'

The 'disable' command makes the addressed line attachment unavailable to commands other than 'enable', 'sense', 'disable', 'no-op',or 'dial'. Other commands issued to a disabled line attachment end with unit check set in the CSW, and intervention required set in sense byte 0. If the line to which the 'disable' command is given is a leased line, channel end and device end are set in the initial status. If the addressed line is a switched line, a line disconnect occurs and then channel end and device end are presented.

'Dial'

The 'dial' command can be used only when the autocall interface feature is installed and the line attachment associated with the modem is disabled, otherwise the command is rejected. The 'dial' command causes dial digits (which form the subscriber number) to be transferred from the processor storage location specified in CCW bits 8 to 31. The transfer continues in ascending order of this address to the automatic calling unit (ACU) until the count in CCW bits 48 to 63 is reduced to zero, or the ACU signals 'abandon call and retry'. The ACU uses the dial digits to produce dial pulses suitable for the switched network. Channel end and device end are presented for the 'dial' command when the last digit has been transferred and the ACU indicates connection established. If the connection cannot be made, unit check is set together with channel end, and device end and the timeout complete bit is set in sense byte 0.

'Break'

The 'break' command is used to stop transmission from a remote DTE. The 'read' command in progress must be terminated with a 'halt device' instruction, then the 'break' command can be given. The CA treats a 'halt device' instruction like a 'halt 1/0', so both instructions can be used in the same way. The 'break' command causes a steady space level to be placed on the line for a duration that is determined by the count in CCW bits 48 to 63. The count causes an appropriate number of bytes to be fetched from processor storage for timing purposes: at least five bytes must be specified. These bytes may contain any bit pattern because they are not transmitted over the line. When the count is reduced to zero, channel end and device end are presented.

Note: The 'break' command must only be used if the remote DTE is equipped with a receive interrupt feature, which allows detection of the 'break' signal. For this reason, use of the 'break' command for Type 1 terminals should be established individually for each line when the CA is installed. If its use is prohibited, a 'break' command is rejected.

'Poll'

The 'poll' command allows the program to search a multipoint network for remote terminals that have a message to transmit. The 'poll' command provides an automatic procedure that relieves the program from having to give alternate 'read' and 'write' commands.

The 'poll' command causes data to be transferred from the processor storage location specified in CCW bits 8 to 31 to the addressed communication line. The data thus transmitted is a 'polling character sequence', which usually consists of a character that sets the control mode, the terminal address, and a character that specifies an 1/0 device such as a card reader or card punch (if any) at the remote station.

After transmission of the polling characters, the line attachment is put into receive status until either a reply is received or a timeout occurs. If a negative response (N) is received, the next polling character is fetched from processor storage and transmitted over the line. The line attachment again checks for a reply. This continues until the polling list is exhausted (all polling characters have been transmitted, which is detected by the length count reaching zero). The command will then be terminated with channel end and device end set. At this point it is recommended to branch back to the 'poll' command via a 'TIC' command to keep a polling loop running until a reply is received.

If a timeout occurs before a reply is received, channel end, device end, and unit check are presented. If, however, a (D) is received, the 'poll' command ends with channel end, device end, and the status modifier (bit 33) set in the CSW. If command chaining has been specified, the current CCW address is incremented by 16 and the CCW at this location is fetched (this should be a 'read' because (D) indicates that a message will arrive). The first

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character thus read in will be the index character (which is excluded from LRC accumulation). The index character identifies the terminal from which the message is being received.

Examples of polling and addressing are shown in Figures 16 to 19.

'Control No-op'

The 'control no-op' command performs no function at the line attachment. Channel end, device end, and any other status conditions that may exist are presented in the initial status.

'Sense'

The 'sense' command causes up to two bytes of sense information to be transferred from the line attachment to processor storage for inspection. A 'sense' command can be given at any time but should always be given when unit check is set in the CSW. For details of the sense information available for Type 1 terminals, see 'Sense Information' in this section. Channel end and device end are set when the transfer of sense information to processor storage is complete.

Sense I/O

The 'Sense 1/0' operation transfers up to seven bytes defining the line congiguration, as follows:

Byte 0:	Always X'FF'
Byte 1:	CPU Identification 1
Byte 2:	CPU Identification 2
Byte 3:	CPU Identification 3
Byte 4:	X'CA' for communication adapter
Byte 5:	Bit 0: zero
	Bit 1: zero
	Bit 2: one
	Bit 3: zero
	Bit 4: Not used
	Bit 5: Not used
	Bit 6: Autocall unit installed
	Bit 7: Not used

<u>Byte 6</u>: Bit 0: Permanent request to send Bit 1: Switched line Bit 2: Unit exception suppress Bit 3: Write interrupt Bit 4: Read interrupt

Bit 5: Delay select 2

Bit 6: Delay select 1

Dit 0. Delay select 1

Bit 7: Integrated modem with manual answer

Unit Status

The unit status shows the state of the addressed line attachment (which works as a subchannel). The unit status is recorded in bits 32 to 39 of the CSW. The bits have the following assignments:

Bit	Meaning
32	Attention (not used)
33	Status modifier
34	Control unit end
35	Busy
36	Channel end
37	Device end
38	Unit check
39	Unit exception

<u>Bit 33</u>. The status modifier bit is set (together with channel end and device end) when a 'poll' command ends because a (D) is received from the polled terminal. The (D) indicates that text will follow. If command chaining is in progress, the status modifier causes the current CCW address to be incremented by 16, to indicate the CCW after the next sequential CCW to be fetched. This should be a 'read' or 'inhibit' command.

If an inline test is active on a line addressed by a 'start 1/0' instruction, the busy and status modifier bits are presented. Secondary interrupt and control unit end follow.

<u>Bit 34</u>. The control unit end bit is presented with secondary interrupt if a 'start 1/0' instruction is issued to a line already being addressed by an inline test (see status modifier above).

Bit 35. The busy bit is set if an inline test is running and the subchannel is busy. If a 'start 1/0' or 'test 1/0' instruction is given, condition code 1 is set in response.

<u>Bits 36 and 37</u>. The channel end and device end bits are always presented together when the line attachment becomes available for a new command. Depending on the command, this may occur at an initial selection or later. Channel end and device end, with or without the status modifier, indicate normal or successful completion of a command. If unit check accompanies this status, a 'sense' command must be given to find the exact circumstances in which the command was completed.

<u>Bit 38</u>. The unit check bit can be set by several errors or unusual conditions which may have caused the termination of a command. For example, a timeout during a 'read' command or during a 'dial' command sets unit check. An unassigned command or a command during which a parity error occurs also causes the setting of unit check. A 'sense' command must be given to retrieve the actual error condition. For a more detailed description of the causes of unit check being set, see 'Sense Information'' in this section.

<u>Bit 39</u>. The unit exception bit, when set, indicates either a specific response or a situation that is unexpected. The meaning of unit exception is specific for each of the following commands:

- 1. For 'write' and 'poll' commands, unit exception indicates that the line was receiving at the time the command was issued.
- 2. For a 'read' or 'inhibit' command, unit exception indicates that a (C) (end of transmission) or (N) (negative response for polling/selection) has been received.
 <u>Note</u>: In order to allow command chaining, it is necessary to inhibit unit exception. Therefore, it is possible to define, when the CA is installed, whether or not unit exception is to be presented on reception of a (C) (end of transmission) character.
- 3. For a 'prepare' command, unit exception indicates that the command was ended prematurely by a 'halt I/O' or 'halt device' instruction.
- 4. For an 'enable' or 'dial' command in switched network operation, unit exception indicates that the command was successfully halted by a 'halt 1/0' instruction before the call was established.

Sense Information

Two bytes of sense information are available.

The bits in sense byte 0 have the assignments shown in the following table. See the last part of each bit description for the meaning of sense byte one, which contains a check code associated with the bit last set in sense byte 0.

- Bit Designation
- 0 Command reject
- Intervention required 1
- 2 Bus out check (not used)
- 3 4 Equipment check
- Data check
- 5 6 **Overrun**
- Lost data
- 7 Timeout complete

A 'sense' command with a length count of one transfers this sense byte only, and no incorrect length indication is given. A 'sense' command with a length count of two or more transfers the two sense bytes. However, an incorrect length indication is given if the length count is greater than two when the SLI bit (suppress length indication) is not set.

All conditions indicated in sense byte 0 set unit check in the CSW.

Sense byte 1 consists of a CA check code (in hex), which indicates the reason (or the last reason, if more than one) for setting a bit in sense byte 0. These reasons are listed below under the relevant bit of sense byte 0.

Comamnd Reject (Bit 0)

This bit is set during command initialization if an invalid command is issued to a line attachment, or if the line attachment is in a state that does not allow the command to be executed. The command is immediately terminated, and unit check status is set in the CSW. The conditions causing command rejection are indicated by the hex code in sense byte 1 as follows:

Hex

- 01 The 'break' command is issued to a line that does not have the read interrupt bit on in feature byte 1 in the configuration table.
- 04 The 'dial' command is issued to a line attachment not equipped with the autocall unit interface feature, or not assigned for switched lines.

- 05 The 'dial' command is issued to a line attachment that has not been disabled (data terminal ready (DTR) was found on).
- 08 Eight immediate commands are executed consecutively.
- 09 The command code in the CCW is invalid.

Intervention Required (Bit 1)

The intervention required bit, when set, normally causes immediate termination of the current command, and channel end, device end, and unit check are set in the CSW when stored at 1/0 interruptions. The conditions causing intervention required to be set are indicated by the hex code in sense byte 1 as follows:

Hex

- 20 The signal 'data set ready' is inactive during a 'read', 'inhibit', 'write', 'break', 'prepare', or 'poll' command; or the signal 'receive line signal detect' is inactive during the execution of a 'read', 'inhibit', 'prepare', or 'poll' command in the read state.
- 21 The 'data set ready' signal is inactive at command initiation of a 'read', 'inhibit', "break', 'prepare', 'write', or 'autopoll' command.
- 22 The 'clear to send' signal is not activated by the modem before the three second timeout ends during 'write', or 'poll' command initiation, or autopoll read to autopoll write turnaround.
- 23 The 'clear to send' signal is inactive during execution of a 'write' or 'break' command, or during execution of the 'write' part of an 'autopoll' command.
- 25 In half-duplex operation (not 'permanent request to send'), the 'clear to send' signal is not dropped within three seconds after resetting 'request to send' during execution of a 'write', or 'poll' command.
- 26 A continuous space signal has been received for one character time or longer during a 'read', 'inhibit', 'prepare', or 'poll' command.
- 27 A timeout has occurred on a switched line with permanent 'request to send' and no 'receive line signal detect'.
- 28 During a 'write' command, a space is found on 'receive data' for two consecutive characters, and the write interrupt feature is installed (reception of a break signal).

- 29 'Data line occupied' (DLO) signal of the ACU is on during initiation or has turned off during execution of a 'dial' command.
- 2A The ACU's 'power indicator' signal is inactive at initiation or execution of a 'dial' command.
- 2C During the execution of the dial command the ACU does not turn off or on 'present next digit', or does not turn on 'abandon call and retry', within 25 seconds in the following cases:
 - 1. 'Call request' to the ACU is on, and 'present next digit on' is not presented.
 - 2. 'Digit present' to the ACU is on, and 'present next digit off' is not presented.
 - Digit present' to the ACU is off, and 'present next digit on' is not presented.
- 2D The ACU and modem have presented neither 'distant station connected' nor 'data set ready' nor 'abandon call and retry' within 60 seconds after all dialing digits and the 'digit present off' signal were presented to the ACU during execution of the 'dial' command.
- 2E The 'data set ready' signal is not found active on the modem within three seconds of the 'data terminal ready' signal being presented during the execution of an 'enable' command on a leased line.
- 30 The line attachment is not enabled ('data terminal ready' bit is off in the UCW) during command initiation of a 'write', 'poll', 'break', 'read', 'inhibit', or 'prepare' command.
- 31 An 'enable' command is issued to an already enabled line ('data terminal ready' on in the UCW), but 'data set ready' is not active, or 'data set ready' is on when 'enable' is issued to a switched line.

Bit 2. Not used.

Bit 3. The equipment check bit is set if a CA or integrated modem hardware check is detected. A detected equipment check causes immediate termination of the current command, and channel end, device end, and unit check to be set in the CSW when stored at 1/0 interruptions. The hex code in sense byte 1 shows the reason for setting the equipment check bit as follows: Hex

60 An unexpected trap has occurred.

61 A hanging situation has occurred so that traps (basic status available) are continously generated for a line. The line is disabled.

- 62 A machine check has been detected indicating an error on the processor bus. The line is disabled.
- 63 The loss of the internal clock signal is detected during the execution of a read type command or write type command. The line is disabled.
- 64 No valid basic status is available. The line is disabled.

<u>Bit 4</u>. The data check bit is never set during execution of an 'enable', 'disable', 'break', 'sense', 'l/O no-op', or 'dial' command. It is set in the following situations, as indicated by the hex code in sense byte 1:

Hex

- 80 An LRC error is detected during execution of a 'read' or 'inhibit' command. The command continues until its normal end.
- 82 A VRC error is detected in a character fetched from program storage during execution of a 'write' or 'autopoll' command. The command continues to its normal end.
- 84 A VRC error has been detected or the receive data is found to be at space level at stop bit time while receiving during a 'read', 'inhibit', 'prepare', or 'autopoll' command. The 'autopoll' and 'prepare' commands are terminated immediately, but the other commands continue to their normal ends.
- 85 The response to polling characters in an 'autopoll' command is neither circle (N) nor circle (D). The command is terminated immediately.
- 86 Circle (N) was received in text-out mode, indicating that the remote terminal received data with incorrect parity or an LRC error. The command is terminated immediately.

<u>Bit 5</u>. The 'overrun' bit can only be set, together with data check, during execution of a 'read' or 'inhibit' command. The setting of the 'overrun' bit does not cause the command to terminate immediately but allows it to continue to its normal end. It is set in the following conditions as indicated by the hex code in sense byte 1:

Hex

AO A character overrun condition has been detected in the line attachment at stop bit time during execution of a 'read' or 'inhibit' command.

<u>Bit 6</u>. The conditions under which 'lost data' is set are as follows, as indicated by the hex code in sense byte 1:

Hex

- CO The receiving bit in the UCW for the addressed line is found on during the initiation of a 'read' or 'inhibit' command, indicating that at least one full character was received and lost before the command was issued. The command continues to its normal end.
- C2 During the initiation of a 'dial' command, 'present next digit' is found on. The command is terminated immediately.
- C4 During the initiation of a 'dial' command, 'distant station connected' is found on. The command is terminated immediately.
- C5 During the execution of a 'dial' command, 'data set ready' or 'distant station connected' goes on during the dialing sequence before the last digit is dialed. The command is terminated immediately.
- C6 'Channel stop' occurs during the execution of a 'read', 'inhibit', or 'autopoll' command. The command is terminated immediately. 'Channel stop' is set during data transfer when the length count is decremented to zero and the last character is not an ending character (assuming that chain data has not been specified). 'Channel stop' is also set if program check, protection check, or channel control check is detected during data transfer or data chaining.
- C7 A 'halt I/O' instruction has been issued when the line attachment is processing a 'read' or 'inhibit' command.

Note: The 'lost data remember' condition can only be reset by a 'read', 'inhibit', or 'enable' command, or by a system reset.

Bit 7. 'Timeout complete' is never set during execution of a 'sense', '1/0 no-op', 'write', or 'break' command. When set for the other commands, the command is terminated immediately. The conditions under which 'time complete' is set are indicated by the hex code in sense byte 1 as follows:

Hex

E2 'Receive data' was not in mark condition for one or two character times before the end of the 28-second timeout. This timeout is started during the execution of a 'read' command.

- E5 A three-second timeout occurs during the execution of a 'read' or 'autopoll' command while control mode is still set. A 25 to 50-second timeout occurs during the execution of a 'read' command while text mode is set. 'Timeout complete' is not set if 'data set ready' drops; intervention required is set instead. Similarly, if 'receive line detect' drops on a line which is connected to a switched network with 'permanent request to send' on, (that is, a duplex modem is installed) 'intervention required' is set, not timeout.
- E6 The 'abandon call and retry' signal of the ACU turns on during initiation of a 'dial' command.
- E7 The 'abandon call and retry' signal of the ACU turns on during execution of a 'dial' command.
- E8 'Data set ready' does not fall before the end of the 25-second timeout during execution of the 'disable' command on a line connected to a switched network.
- E9 'Receive line signal detect' or 'clear to send' is not activated by the modem before end of the 25-second timeout. This timeout is initiated after 'data set ready' is activated during execution of an 'enable' command on a line connected to a switched network with 'permanent request to send'.

Binary Synchronous Communications Control

The binary synchronous communication (BSC) line control procedure comprises the command set and the line control characters and sequences required to communicate with any other BSC terminal or processor attachment. The code structures are shown in Appendix D, Figures 27 and 28.

Line Control Characters

SOH and STX

SOH (start of heading) and STX (start of text) both cause the same action in receive as well as transmit operations: they set the line attachment to text mode. In text mode, block-check character accumulation is started and subsequent SOH or STX characters are treated as data.

ETX and ETB

ETX (end of text) and ETB (end of transmission block) both cause the same action in transmit and receive modes: they end text mode and the operation (unless transparent mode is set). If error index byte mode was specified (by a 'set mode' command), reception of ETX or ETB causes an error index byte to be stored next to ETX or ETB.

ENQ (Inquiry)

ENQ ends a 'read' command but has no effect on a 'write' command. When used in the data string transmitted during a 'poll' command, ENQ causes a line turnaround (a change from transmit to receive mode).

ACK (Positive Acknowledgement)

ACK ends a read command and causes channel end and device end to be set. The line attachment remains in receive mode; ACK has no effect on a 'write' command.

NAK (Negative acknowledgement)

NAK ends a 'read' command and causes channel end and device end to be set. The line attachment remains in receive mode; NAK has no effect on a 'write' command.

EOT (End of Transmission)

EOT ends a 'read' command (if received while the line attachment is not in text mode) but has no effect on a 'write' command.

ITB (Intermediate Text Block)

The ITB character does not end a 'read' or 'write' command but resets block check character accumulation, causing the accumulated value to be transmitted (during a 'write' command) or an error index byte (EIB) to be stored (during a 'read' command if error index byte mode was specified). Transmission or reception then continues with new block-check character accumulation.

DLE (Data Link Escape)

The DLE character has no function when transmitted or received alone. If one specific character immediately

follows DLE, a sequence with control functions is recognized. For example, DLE coupled with 70(hex) is the ACK-0 reply; DLE coupled with 61 (hex) is the ACK-1 reply; DLE with 7F (hex) is the wait before transmit (WACK) reply. All of these sequences terminate a 'read' command. Other sequences such as DLE/STX set transparent mode. (For details, see the descriptions of individual commands in this section.)

SYN (Synchronization)

The SYN character is used ahead of a transmission and is inserted into the message stream at one-second intervals to establish and maintain synchronization. Note: For a listing of applicable characters, see 'Appendix

D. CA Code Tables'.

Transmission Code

The transmission code used for binary synchronous communication is either EBCDIC or ASCII (1SO 646 or CCITT No.5). The code structure as defined by the International Organization for Standardization (1SO)/International Telephone and Telegraph Consultative Committee (CCITT) is:

Storage byte: 0 1 2 3 4 5 6 7 ASCII relation: - 7 6 5 4 3 2 1

When ASCII characters are transmitted, the bit position shown as a dash (this bit is zero while in storage) is replaced by an odd parity bit. When ASCII characters are received, the parity bit is stripped off and zero is stored in its bit position. Regardless of the code used, the low-order bit (bit 7 in EBCDIC, bit 1 in ASCII) is always transmitted first.

Commands

02 0 0 0 0 1 0 01 0 0 0 0 1 Write 06 0 0 0 1 1 0 Prepare 1E 0 0 1 1 1 0 Address Prepare (Adprep) 27 0 1 0 1 1 1 Enable 2F 0 0 0 1 1 1 Disable 09 0 0 0 1 0 1 1 29 0 1 0 1 1 No-op ('Set Line Mode') 23 0 1 0 1 No-op ('Set Line Mode') 23 0 1 0 1 Set Mode 04 0 0 0 1 Control No-op 13 0 0 1 No-op ('sadzero') 17 0 0 1 1 No-op ('sadone')	Comman <u>Hex</u>	<u>CC</u>	W	B	its	<u>5</u> 4	5	6	7	Command
1B 0 0 1 1 No-op ('sadtwo') 1F 0 0 1 1 1 No-op ('sadthree') E4 1 1 0 0 Sense 1/0	01 06 1E 27 2F 09 29 28 23 04 03 13 17 1B 1F		000000000000000000000000000000000000000	0 0 0 1 1 0 1 1 0 0 0 0 0 0 0 0 0	0 0 1 0 0 0 0 0 0 0 1 1 1	0 0 1 0 1 1 1 1 1 0 0 0 0 0 1 1 1	0 1 1 1 1 1 0 0 0 0 1 0 0 1 0 1 0	1 1 1 1 1 0 0 1 1 0 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Write Prepare Address Prepare (Adprep) Enable Disable Poll Dial No-op ('Set Line Mode') Set Mode Sense Control No-op No-op ('sadzero') No-op ('sadtwo') No-op ('sadthree')

Notes:

1. Bits 0 and 1 are 'don't care' bits.

 For compatibility purposes, the 'sadzero', 'sadone', 'sadtwo', 'sadthree', and 'set line mode' commands (hex 13, 17, 18, 1F, and 2B) are accepted and treated as no-operations.

Read

Whenever the binary-synchronous line attachment is enabled and is not executing a write-type command, it monitors the 'receive data' for activity. The line attachment decodes the last eight bits received. If these eight bits do not represent a SYN character, monitoring continues. If a SYN character is decoded, the next eight bits are gated in and are subsequently checked for their identity with a SYN character. If the second byte thus received is a SYN character, then the line attachment has established character phase, which is a prerequisite for read operations.

When a 'read' command is given, the line attachment may or may not have character phase. If character phase has already been established, execution of the 'read' command progresses. If, however, more than one non-SYN character comes in before the 'read' command is given, the command initiation ends with unit check and the lost data bit is set in sense byte 0. The 'read' command causes a three-second timeout to be started. If character phase cannot be established before the three seconds have elapsed, the command ends with unit-check set and the timeout complete bit is set in sense byte 0.

If character phase can be established in time, the line attachment checks whether a control character is received within three seconds after reception of a SYN character. If a control character (other than SYN) cannot be found in time, the command ends with unit check set and the timeout complete bit set in sense byte 0.

If character phase can be established and there is no timeout, further actions within the line attachment depend on the data that is actually received, as described in the following text:

- If a DLE acknowledgement sequence, NAK, or ENQ is received, the 'read' command ends with channel end and device end set. If an EOT is received, unit exception is also set.
- 2. If an SOH or STX character is received, the line attachment sets text mode. In text mode, further SOH or STX characters are no longer recognized as control characters, but are treated as text. In addition, the block check character accumulation begins. The SYN characters (which are included in the data stream at one-second intervals) are not transferred to processor storage but are used to maintain character phase. If characters are received while the line attachment is in text mode, a SYN non-SYN sequence must be received before three seconds have elapsed. This is to prevent a situation in which the line attachment has lost character synchronization.

As text reception continues, each character received updates the block-check character (BCC) accumulation. Being in text mode, the line attachment is sensitive to the following ending characters:

a. If ETX or ETB is received, the line attachment leaves text mode. Block-check character accumulation stops and the attachment awaits the BCC characters from the remote station. Upon reception, these characters are compared with the value accumulated locally. The block check characters are equal to two CRC bytes when EBCDIC characters are transferred, and one LRC byte in the case of ASCII characters. If the result is equal, channel end and device end are presented for the 'read' command. If the result shows not equal, unit check is also presented and the data check bit is set in the sense byte. If EIB mode is specified when the CA is installed or is set by a 'set mode' command, an error index byte is stored next to the ETX or ETB character. b. If ENQ is received, the line attachment leaves text mode but does not compare BCC characters. Channel end and device end are presented for the 'read' command.

The foregoing description covers the basic aspects of a 'read' command. There are three variations, however, which alter the behavior of the line attachment during execution of a 'read' command.

1. If an ITB character is received, the attachment stops block-check character accumulation, waits for the BCCs from the remote station, and compares these with the accumulated value without ending the 'read' command. Reading continues with the next block for which BCC accumulation is started from an initial value. If the BCC comparison gives an unequal result, data check is set in the sense byte, but this data check is presented to the program only at the end of the read operation.

If error index byte mode is specified when the CA is installed, or is set by a 'set mode' command, reception of an ITB character causes the same BCC comparison but, in addition, an error index byte is stored next to every ITB. This error index byte may contain all zeros or have bit 4 (data check) and/or bit 5 (overrun) turned on, depending on the type of error. In this way, each data block has its own ITB character (and its own error index byte, if EIB mode is in effect). The 'read' command ends when ETX or ETB is received. If EIB mode is specified, an error index byte is stored next to the ending character. At that time, unit check is set in the status (and data check overrun in the sense byte) if such an error occurs.

- 2. If the DLE/STX sequence is received, the line attachment sets transparent mode. In transparent mode, the line attachment is insensitive to all single control characters; which means that all possible codes are treated as text. However, in transparent mode the attachment is sensitive to the data link escape sequences, which all start with the DLE character. To differentiate between DLE as text data and a DLE sequence, the line attachment examines each DLE and the character that immediately follows it. The action depends on the character that follows DLE. Four control actions are specified:
 - a. If DLE is followed by another DLE, the first DLE is ignored and the second DLE, inserted by the transmitting station, is transferred to processor storage. Transparent reading continues.

- b. If a SYN character follows DLE, the DLE and SYN characters are ignored. The three-second timeout is restarted and transparent reading continues. SYN characters that do not follow DLE characters are recognized as data.
- c. If an ITB character follows DLE, the line attachment leaves transparent text mode and continues reading. The BCC is compared and the error index byte is stored (if EIB mode is specified). If, thereafter, DLE/STX is received again, the line attachment returns to transparent mode.
- d. If an ETB or ETX character follows DLE, the 'read' command ends with channel end and device end set. This terminates transparent mode. ETB or ETX characters that do not follow a DLE character are treated as data.
- 3. During execution of a 'read' command, the line attachment may not receive a character that sets text mode (or transparent text mode). When not in text mode, the line attachment is sensitive not only to the control characters that set text mode or end the command, but also to all DLE sequences that consist of DLE followed by any of the characters in column 3 of the ASCII code table (or columns 6 and 7 in the EBCDIC table). Most of these sequences have no particular assignment but some have been agreed upon as a programming convention in IBM support programs (access methods). ACKO, ACK1, WACK, RVI (reverse interruption), DLE/EOT (switched line disconnect signal), are examples of some of these conventions. All of these assignments, however, concern the program only. For example, ACKO and ACK1 are positive acknowledgements with a built-in count that alternates 0, 1, 0, 1 so that the program can determine whether an acknowledgement is missing. Reverse interruption is a request from the remote station asking the program to stop transmitting and issue a 'read' command so that a message can be put through. The logical meaning of these DLE sequences is ignored by the line attachment.

When not in text mode, the line attachment recognizes any of the DLE sequences consisting of DLE followed by any of the characters in column 3 in the ASCII code table (or columns 6 and 7 in the EBCDIC table) as a signal to terminate the command with channel end and device end. The 'write' command causes data to be transferred from the processor storage location specified in CCW bits 8 to 31 to the line attachment, for transmission to the remote terminal. When the 'write' command is given, the line attachment stops its continuous search for synchronization unless it is in character phase. If character phase is already established (which is an exceptional condition), the 'write' command ends with unit exception. Unit exception in response to a 'write' command indicates that a 'read' command should be issued because of incoming data (some data may already have been lost). If character phase has not been established at the time a 'write' command is given (which is the normal case), the line attachment transmits a pad character. If modem clocking is used, the pad character is followed by two SYN characters. If business machine or internal clocking is used, that is, the line attachment maintains the bit synchronization, the pad character is followed by two bit-synchronization characters (hex '55'), and two SYN characters.

The SYN characters are immediately followed by the data from processor storage. The data is interspersed with single SYN characters at one-second intervals. The detailed actions within the line attachment depend on the data transmitted, as follows:

- If control characters such as ENQ, NAK or EOT, or character sequences such as ACKO, ACK1, WACK or RVI are transmitted, no action occurs and the 'write' command does not end. The receiving station, however, does terminate the corresponding 'read' command.
- If the SOH or STX character is transmitted, the line attachment sets text mode, which means that BCC accumulation is reset and begins from an initial value. Further SOH or STX characters are not treated as control characters, but as ordinary text data.
- 3. If an ETX or ETB character is transmitted, the line attachment leaves text mode and transmits the accumulated BCC characters. Channel end and device end are then presented for the 'write' command.

The foregoing text describes a basic 'write' operation. If, however, EIB mode or transparent text mode have been specified, the line attachment is sensitive to certain control characters as follows:

1. If an ITB character is transmitted, the line attachment transmits the BCC value accumulated up to this point. This value allows the receiving station to compare and to store the appropriate error index byte if ElB mode has been specified. Execution of the 'write' command continues, with a new BCC accumulation.

- 2. If the character sequence DLE/STX is transmitted, the line attachment sets transparent text mode. Transparent text mode has the following consequences:
 - a. Whenever a DLE character is transmitted, the line attachment generates a second DLE, which it sends out following the first DLE. This allows the receiving station to differentiate between a DLE control sequence and a DLE character that is treated as data.
 - b. If a SYN character is fetched from processor storage and transmitted , no action occurs. The automatically inserted SYN characters for maintaining synchronization are, however, each preceded by a DLE. This allows the receiving station to differentiate between SYN characters that are data and SYN characters that are inserted for synchronization only.
 - c. If the sequence DLE/ETX or DLE/ETB is transmitted, the block ending sequence is not recognized. Any DLE is automatically doubled by insertion of another DLE, thus altering the sequence to DLE/DLE ETX or DLE/DLE/ETB and this has no effect. For this reason, a 'write' command in transparent mode continues until the count in CCW bits 48 to 63 is reduced to zero. Another 'write' command must be given within three seconds unless the explicit 'write' command is chained to the first one. The line attachment is in the transparent wait state, in which it rejects all commands except 'write' and 'control no-op'. In the second 'write' command, the sequence DLE/ETX is not altered by the extra DLE and is therefore accepted as a block ending sequence by the remote station.
 - d. If DLE/ITB is to be transmitted, this sequence must also be sent by a separate 'write' command. DLE/ITB ends transparency and must be followed by transparent or non-transparent text, or by ETX.

Prepare

The 'prepare' command provides a means of telling the program that character phase has been obtained at the addressed line attachment. Since character phase is a prerequisite for a successful read operation, the 'prepare' command may be chained to a 'read' command.

When the 'prepare' command is given, the attempts to obtain character phase are monitored. If character phase has already been established, channel end and device end are presented in the initial status for the 'prepare' command, otherwise they are given when character phase is actually obtained. No data transfer occurs and no timeouts are associated with the 'prepare' command. The first data byte of the incoming message is read into storage by the next 'read' command. No commands other than 'No-op' or 'TIC'
are allowed before the 'read' command, otherwise unpredicted results may occur.

Address Prepare

The 'address prepare' command provides the means to monitor the receive line for its own polling or selection addresses. The command thus allows the line attachment to operate as a tributary (non-control) station on a multipoint line.

Up to two different polling selection addresses may be specified for each line using the CA tributary station address(es) update tool of the customer manual operations.

The address prepare command is a pseudo-read command in that the line attachment performs the actions of a 'read' command, yet does not transfer data to processor storage.

When the line attachment accepts the 'address prepare' command, it monitors all data on the line. It starts a three-second timeout and attempts to establish character phase, unless character phase has already been established (which is not the normal case).

Further actions within the line attachment depend on the activities found on the receive line, as described below.

- If the three-second timeout expires, the line attachment enters monitor mode and starts a new three-second timeout. The line attachment remains in monitor mode until it receives the sequence SYN, SYN, EOT, pad character. This is a valid EOT sequence which sets the line attachment to control mode, the only state in which the line attachment can recognize poll or selection addresses. The 'address prepare' command can be terminated only when a poll or selection address is recognized.
- 2. If character phase is already established when the 'address prepare' command is given, the line attachment enters monitor mode, starts a three-second timeout and waits for the SYN, SYN, EOT, pad character sequence. When this sequence is received, another three-second timeout is started, because if there is any polling in progress, the address should follow EOT before three seconds have elapsed.
- 3. If character phase is established and a control character such as SOH or STX is received, the line attachment sets monitor mode and text mode but does not transfer data to processor storage. The line attachment is capable of looking for its station addresses only after it has recognized the EOT character because this character sets 'control mode'.

- 4. If character phase is established, the line is in 'address prepare control mode', and one of the tributary station addresses of the line attachment is recognized, further action depends on the type of address received. The line attachment has two pairs of selection and polling addresses and reacts to these as follows:
 - a. If one of its selection addresses has been recognized, the 'address prepare' command ends with channel end and device end. This allows chaining to a 'read' command that will read the selection address into processor storage.
 - b. If one of its polling addresses is recognized, the 'address prepare' command ends with channel end, device end and status modifier. This allows chaining to the command after the next sequential command, which should be a 'read' that transfers the polling address to processor storage. No commands other than 'No-op' or 'TIC' are allowed before the 'read' command, otherwise unpredicted results may occur.

Enable

The 'enable' command puts the line attachment into the operational state. If the line attachment is not enabled, all commands (except 'no-op', 'enable', 'dial', and 'set mode') are rejected with unit check set in the CSW and the command reject bit set in sense byte 0. If the 'enable' command is issued to a privately-owned or leased line, channel end and device end are presented when the line attachment detects the 'data set ready' signal being raised by the modem. If 'data set ready' is not detected within one second of the line attachment raising the 'data terminal ready' signal, the 'enable' command ends with unit check set and the intervention required bit is set in sense byte 0. If the 'enable' command is given to a switched line, the modem is then conditioned to answer an incoming call automatically, assuming that the modem has auto-answer capability. Channel end and device end are presented when an incoming call is received. No timeout is associated with the 'enable' command for a switched line.

Disable

The 'disable' command sets the addressed line attachment into the non-operational state. The disabled line attachment no longer searches for character phase, nor executes any command (except 'no-op', 'enable', 'dial', 'sense', 'disable' or 'set mode'), nor reacts to incoming calls. If the 'disable' command is given to a private or leased line, channel end and device end are indicated after one second. If given to a switched line, the command causes the modem to disconnect. A 32-second timeout (for modems

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using the CCITT option - Connect Data Set to Line (CDSTL) function) or a one-second timeout (for all other modems) is started, and if the modem has not disconnected before the timeout expires, the 'disable' command ends with unit check set and the timeout complete bit set in sense byte 0.

Poll

The 'poll' command provides a means of requesting several remote stations, one after the other, to transmit data to the line attachment. The command is normally used in a multipoint network where several satellite stations are connected to the same receive line, but it can also be used in a point-to-point installation.

When the 'poll' command is given, the line attachment transmits the pad character followed by two SYN characters. The SYN characters are followed by data that is fetched from the processor storage location specified in CCW bits 8 to 31, and ascending addresses. This data usually consists of a station address and ends with the ENQ character. Up to this point there is no difference between the 'poll' command and a normal 'write' command.

As data is being transmitted, however, the line attachment monitors the outgoing data stream, and when ENQ is detected the next character is fetched from storage but not transmitted; it is retained in the line attachment as the index character. The line attachment goes into receive mode without ending the 'poll' command. A three-second timeout is started and the search for character phase begins. Further actions by the line attachment depend on the state of the remote station, as described in the following text. <u>Note</u>: The 'poll' command must end with an EOT as the last character in the poll list.

Unsuccessful Poll.

If the remote station is inactive, character phase cannot be obtained. The three-second timeout elapses in the line attachment, causing the 'poll' command to end with channel end, device end, and status modifier bits set. If the 'poll' command is chained, the next command is skipped (because the status modifier is set) and the next sequential command after the skipped command (which is usually a 'read') is terminated with unit check set and the timeout complete bit set in the sense byte. The index byte (previously fetched) is returned to processor storage to an address specified by the 'read' command.

Remote Station Has Nothing to Send.

If the remote station is transmitting SYN characters, the line attachment obtains character phase before the timeout

elapses. When character phase is obtained, the line attachment checks whether the first non-SYN character received is the EOT character. If the first non-SYN character is EOT, the remote station has nothing to send. The line attachment goes back to transmit mode and starts again to transmit the pad characters followed by two SYN characters. The polling data is then fetched from processor storage and, when the ENQ character is detected, the line attachment fetches the next index byte and changes to receive mode as before.

Successful Poll.

If character phase is obtained and the first non-SYN character is not EOT, the 'poll' command ends with channel end, device end, and status modifier bits set. If the 'poll' command is chained, the status modifier bit causes the next sequential command to be skipped and the next sequential command after the skipped command is executed. Since this command is usually a 'read' command, the line attachment then reads in the message from the remote station. Before the first character is transferred from processor storage, however, the line attachment returns the index byte (previously fetched) to processor storage as an identifier for the message that follows, so that the program knows which remote station has responded. <u>Note:</u> Polling can also be done by properly chained alternate 'write' and 'read' commands.

Dial

The 'dial' command enables an autocall interface, and digit signals are transferred from processor storage to the automatic calling unit. If no ACU is installed, the 'dial' command is rejected.

The digit signals are transferred as data from the location specified in CCW bits 8 to 31 and ascending locations until the count in CCW bits 48 to 63 is reduced to zero. In the data thus transferred, only bits 4 to 7 of each byte are actually placed on the digit signal lines of the ACU.

The program is responsible for ensuring that only the following are sent to the ACU:

- 1. Decimal values from 0 to 9, required to present the correct dial number.
- 2. The end of number (EON) or separator (SEP) character, if these characters are required by the ACU.

Whether or not EON is used depends on the type of ACU connected. Some ACUs recognize EON, some do not. ACUs that recognize EON may use the character as a signal that

dialing is complete (avoiding a timeout).

The digit signals are presented to the ACU at a rate set by the ACU. If the ACU timeout elapses before connection is established, the 'dial' command ends with unit check, and the 'timeout complete' bit is set in the sense byte. If the ACU has the power indicator off, the 'dial' command ends with unit check in the initial status and intervention required is indicated in sense byte 0. <u>Note</u>: The line attachment associated with the autocall interface must be disabled before the 'dial' command is given, otherwise the command is rejected.

Set Mode

The 'set mode' command allows the program to specify whether or not the line attachment is to operate in error index byte (EIB) mode. See the 'read' command description for more information on EIB mode. One byte is used for specifying EIB mode; the bits have the following meanings:

Bit Meaning

0	Not	used
1	EIB	mode
2	Not	used
3	Not	used
4	Not	used
5	Not	used
6	Not	used
7	Not	used

Sense

The 'sense' command causes two bytes of sense information to be transferred to the processor storage location specified in bits 8 to 31 of the CCW. The contents of the sense bytes are described in 'Sense Information' in this section. Sense I/O

The 'Sense I/O' operation transfers up to seven bytes defining the line configuration, as follows:

Byte O Always X'FF! Byte 1 CPU Identification 1 Byte 2 CPU Identification 2 Byte 3 CPU Identification 3 Byte 4 X'CA' for communication adapter Byte 5 Bit 0: zero Bit 1: one Bit 2: zero Bit 3: zero Bit 4: ASCII mode Bit 5: Business machine clocking Bit 6: Autocall unit installed Bit 7: Not used Byte 6 Bit 0: Permanent request to send Bit 1: Switched line Bit 2: New synchronisation Bit 3: Connect data set to line Bit 4: Not used Bit 5: Error index byte (EIB) mode Bit 6: High speed line Bit 7: Integrated modem with manual answer

bit 7. Hitegrated modeli with mandar a

Unit Status

The unit status is recorded in bits 32 to 39 of the CSW. The bits are assigned as follows:

Bit Meaning

- 32 Attention (not used)
- 33 Status modifier
- 34 Control unit end
- 35 Busy
- 36 Channel end
- 37 Device end
- 38 Unit check
- 39 Unit exception

<u>Bit 33</u>. The status modifier bit is set in specific cases during polling operations or during the execution of the 'address prepare' command to allow chaining to the command after the next sequential command. When a 'poll' command has progressed to the point where the polling data has been sent out and the line attachment is in receive mode, the status modifier is set if the first character received after the SYN characters is not an EOT character. The status modifier bit is also set if no response (neither positive nor negative) is received from the polled tributary station within three seconds following the poll transmit sequence. For an 'address prepare' command this bit is set if one of the two possible polling addresses was detected after a valid EOT sequence.

If an inline test is active on a line addressed by a 'start 1/0' instruction, busy and status modifier bits will be presented. Secondary interrupt and control unit end will follow.

Bit <u>34</u>. The control unit end bit is presented together with secondary interrupt if a 'start 1/0' is issued to a line already being addressed by an inline test (see status bit 33 above).

<u>Bit 35</u>. The busy bit is set if an inline test is running and the subchannel is busy. If a 'start 1/0' or 'test 1/0' instruction is given, condition code 1 is set in response.

<u>Bits 36 and 37</u>. The channel end and device end bits are always presented together when a command ends (that is, when the subchannel is free). For some commands, the presentation of channel end and device end is, in itself, an indication that a specific event has occurred. For example, when channel end and device end are presented for the 'prepare' command, this indicates that character phase has been established.

Bit 38. Unit check is a summary indication that can be set by several different errors or unusual conditions. For example, if a disabled line attachment is addressed, or if a timeout has elapsed, unit check is set. For more detailed information on the conditions that set unit check, see ''Sense Information'' in this section.

<u>Bit 39</u>. The unit exception bit is set when certain conditions occur during the execution of a command. These conditions, which are described in the following list, are unique to each command.

- If a 'write' command is given when character phase is already being established, unit exception is set because a transmission from the remote station has started or is in progress. The 'write' command is not executed, but is terminated immediately. The same applies to the 'poll' command under the same circumstances.
- 2. If the EOT character is recognized during execution of a 'read' command, the command is terminated with unit exception set.
- 3. For all other commands, unit exception is set whenever the command is terminated by a 'halt I/O' or a 'halt device' instruction before any action could occur.

Sense Information

Two bytes of sense information are available. The bits in sense byte 0 are assigned as follows:

Bit Meaning

- 0 Command reject
- 1 Intervention required
- Bus out check (not used) 2
- 3 4 Equipment check
- Data check
- 5 **Overrun**
- 6 Lost data
- 7 Timeout complete

A 'sense' command with a length count of one transfers only the first byte, and no incorrect length indication is given. A 'sense' command with a length count of two or more transfers the two sense bytes, however, an incorrect length indication is given if the length count is not equal to two and the SLI bit (suppress length indication) is not set. All the conditions indicated in sense byte 0 set unit check in the CSW.

Sense byte 1 consists of a CA check code (in hex) which indicates the reason (or the last reason, if more than one) for setting the bit in sense byte 0. The reasons are listed below under the relevant bit of sense byte 0.

Bit 0. This bit is set during command initiation if an invalid command is given to a line attachment, or if the line is in such a state that the command cannot be executed. The command is terminated immediately with only unit check set in the CSW. The following conditions (shown in hex code in sense byte 1) cause command rejection:

Hex

- 04 A 'dial' command given but no ACU installed, or the line attachment is not assigned for switched lines.
- 05 The 'data terminal ready' signal is detected when a 'dial' command is initiated (that is, the addressed line is not in the disabled state when the 'dial' command is initiated).
- 06 A 'read', 'write', 'autopoll', 'prepare', or 'address prepare' command is given to a BSC line that has not been enabled ('data terminal ready' off during command initiation).
- 07 'Data terminal ready' was off at chaining to a 'read',

'write', 'prepare', 'address prepare' or 'poll' command.

08 Eight immediate commands have been executed consecutively.

09 The command code in the CCW is invalid.

OA A command other than 'write', 'sense', or 'control no-op' has been given to a BSC line while in transparent wait condition.

Bit 1. The intervention required bit, when set, normally causes immediate termination of the current command, and channel end, device end, and unit check are set in the CSW when stored at 1/0 interruption. The conditions causing intervention required to be set are shown in sense bytes as follows:

Hex

- 20 The 'data set ready' signal is inactive during execution of a 'write', 'read', 'prepare', 'address prepare' or 'autopoll' command.
- 21 The 'data set ready' signal is inactive at command initiation of a 'read', 'prepare', 'write', 'address prepare' or 'autopoll' command.
- 22 The 'clear to send' signal is not found active on the modem before the three-second timeout ends during 'write' command initiation, 'autopoll' command initiation, or an autopoll read to autopoll write turnaround.
- 23 The 'clear to send' signal is inactive during execution of a 'write' command, or (in the autopoll write state) during execution of an 'autopoll' command, when there is no 'permanent request to send' signal.
- 24 In modem-clocked applications, a clock-check is presented (while the 'data set ready' signal is still present) during the execution of a 'write' command or an 'autopoll' command in the autopoll write state.
- 25 In half-duplex (not 'continuous request to send'), the 'clear to send' signal is not de-activated by the modem before the one-second timeout occurs either at 'write' command termination, or at 'autopoll' write-to-read turnaround.
- 29 The ACU's 'data line occupied' signal is active when a 'dial' command is initiated or has turned off during the execution of a 'dial' command.

- 2A The ACU's 'power indicator' signal is inactive at initiation or execution of a 'dial' command.
- 2C During execution of the 'dial' command the ACU does not turn off or on 'present next digit', or does not turn on 'abandon call and retry', within 25 seconds in the following cases:
 - 1. 'Call request' to the ACU is on, and 'present next digit on' is not presented.
 - 2. 'Digit present' to the ACU is on, and 'present next digit off' is not presented.
 - 3. 'Digit present' to the ACU is off, and 'present next digit on' is not presented.
- 2D The ACU and modem have presented neither 'distant station connected' nor 'data set ready' nor 'abandon call and retry' within 60 seconds after all dialing digits and the 'digit present off' signal was presented to the ACU during the evaluation of a 'dial' command.
- 31 An 'enable' command is given to an already enabled line ('data terminal ready' signal active), but the 'data set ready' signal is not active, or 'data set ready' is on when 'enable' is issued to a switched line.
- 34 The 'data set ready' signal is not found active on the modem within three seconds of the 'data terminal ready' signal being presented during the execution of an 'enable' command on a leased line.
- Al A character underrun condition is detected during a 'write' command. Intervention required is set together with the overrun bit. The command continues to its normal end.

Bit 2. Not used.

<u>Bit 3</u>. This equipment check bit is set if a CA or integrated modem hardware check is detected. A detected equipment check causes immediate termination of the current command, and channel end, device end, and unit check to be set in the CSW when it is stored at the next 1/0 interruption.

The hex code in sense byte 1 shows the reason for setting the equipment check bit as follows: Hex

- 61 A hanging situation has occurred so that traps (basic status available) are continously generated for a line. The line is disabled.
- 62 A machine check has been detected indicating an error on the P10 bus. The line is disabled.
- 63 The loss of the internal clock signal is detected during

the execution of a read type command or write type command. The line is disabled.

64 No valid basic status is available. The line is disabled.

Bit $\frac{4}{1}$. The data check bit is set during the execution of a 'read' command only. It is set in the following situations: Hex

- 80 A BCC error (EBCDIC), or an LRC and/or VRC error (ASCII), is detected during the execution of a 'read' command. The command is allowed to continue to its normal end.
- 84 A DLE character in transparent read operation is not followed by an ETB, ETX, ITB, ENQ, DLE, or SYN control character. The data check condition may occur during execution of a 'poll' command but the unit check and data check sense bits will not appear until the succeeding 'read' command.

<u>Bit 5</u>. The setting of the overrun bit does not cause the command to terminate immediately but allows it to continue to its normal end. It is set in the following conditions, as shown by hex codes in sense byte 1:

Hex

- AO An overrun condition has been detected during execution of a 'read' command, or during execution of an 'autopoll' command while the line attachment is in receive state.
- Al An underrun condition has been detected during execution of a 'write' command. Intervention required is set together with overrun.

Bit 6. The conditions under which 'lost data' is set are shown by hex codes in sense byte 1 as follows:

Hex

- CO The lost data remember flag in the UCW is detected during 'read' command initiation, indicating that at least one full character was received and lost before the command was given. The command is allowed to continue to its normal end.
- C2 The 'present next digit' signal is active during initiation of a 'dial' command.
- C4 The 'distant station connect' signal is active during initiation of a 'dial' command.

- C5 The 'data set ready' or 'distant station connect' signal is active during the dialing sequence of a 'dial' command before the last digit is dialed.
- C6 Channel stop occurred during execution of a 'read' command or 'autopoll' in read state. The command is terminated immediately. Note: Channel stop is set during data transfer when the length count has been reduced to zero, without having received an ending character (assuming that chain data is not specified). Channel stop is also set when program check or protection check is detected during data transfer. The command is terminated immediately.
- C7 A 'halt I/O' instruction was issued when the line attachment was processing a 'read' command.

Note: The lost data remember condition can only be reset by a 'read', 'write' (transparent stop condition), or 'enable' command, or by a system reset.

<u>Bit 7</u>. This timeout complete bit is never set during execution of a 'sense', an 1/0 'no-op', 'write', or 'break' command. When set for other commands, the command is terminated immediately. The conditions under which it is set are shown by hex codes in sense byte 1 as follows:

Hex

- E3 The line attachment is executing a 'read' command and does not receive two consecutive SYN characters within three seconds of the beginning of the command.
- E4 The line attachment is executing a 'read' command and does not receive SYN/non-SYN sequence within three seconds of the previous SYN/non-SYN while in text mode; or does not receive DLE/SYN/non-DLE within three seconds of the previous DLE/SYN/non-DLE while in transparent text mode.
- E6 The 'abandon call and retry' signal of the ACU becomes active during initiation of a 'dial' command.
- E7 The 'abandon call and retry' signal of the ACU becomes active during execution of a 'dial' command.
- EA The line attachment is operating as a control station on a data link executing a 'poll' command. After transmission of an autopoll sequence to a tributary station, the control station (in the autopoll receive state) waits for three seconds for an answer from the tributary station. If no answer is received within three seconds, the 'poll' command is ended and chained to a 'read' command. During initiation of the 'read'

command, the index byte is transferred to processor storage and the 'read' command is immediately ended with the timeout complete bit set in sense byte 0.

- EB A second 'write' command is issued more than three seconds after termination of the 'write' command that placed the line attachment in transparent mode. The second 'write' ends immediately with the timeout complete bit set.
- EC The 'data set ready' signal is not de-activated by the modem within one second (modems without CDSTL function), or 25 seconds (modems with CDSTL function) after the 'data terminal ready' signal has been dropped, during execution of a 'disable' command on a switched line.

Synchronous Data Link Control

Synchronous data link control (SDLC) is supported in the CA by a group of 4331 commands described in the following pages. When issued, these 4331 commands are converted by the SDLC-CA microcode to the commands and responses used in synchronous data link control. The SDLC commands and responses are not the subject of this text but are described in <u>IBM Synchronous Data Link Control General</u> <u>Information</u>, GA 27-3093. Of the commands and responses listed in the above publication, the following are supported by the SDLC-CA and by ACF/VTAME

Acronym	Command	Response	<u>Meaning</u> of <u>Acronym</u>
CMDR		x	Command reject
DISC	Х		Disconnect
DM		X	Disconnected mode
1	Х	Х	Information
RNR	Х	Х	Receive not ready
RR	Х	Х	Receive ready
SNRM	X		Set normal response mode
TEST	Х	Х	Test
UA		Х	Unsequenced acknowledgment
XID	X	X	Exchange station identification

The CA recognizes I-frames, RR frames and RNR frames only when 'autopoll', 'write PIU', and 'sense SCB' commands are executed.

The following text shows other features which are supported or not supported by the SDLC-CA and ACF/VTAME.

Supported:

- Half duplex data mode only
- Broadcast and single unique station addresses only

Not Supported:

- Group addresses
- Format extensions
- Selective retransmission recovery
- Nonsequenced poll (NSP)
- Asynchronous response mode (ARM), asynchronous disconnect mode (ADM), and asynchronous balanced mode, (ABM)

The 4331 commands for SDLC operation, together with the status and sense information, error recovery, and synchronization rules are specified in this chapter. There are two kinds of command in the SDLC-CA:

- 1. Basic commands, similar to corresponding BSC commands, for initializing the line interface, termination, and some error processing.
- 2. High-level commands for wider control of station polling and transfer of information frames. Details of each station are transferred from the access method to the line interface in the form of a station control block (SCB). An SCB contains the station's SDLC address, the number of frames sent (Ns) and received (Nr), and the station's status flags. With this information, the line interface builds an SDLC poll and interprets the response. A table of SCBs forms an autopoll list which can be cycled repeatedly under channel-program control until a poll is successful. Thus the CA absorbs the overhead due to negative polling.

The CA also builds the frames to be transmitted, and checks the frames received. The current SCB is used as the source for address and count information. Only the information field which forms the path information unit (PIU) defined in <u>Systems Network Architecture General</u> <u>Information</u>, GA27-3102, is transferred across the channel interface. A series of PIUs for one station can be transmitted or received without intervention from the access method. In this text, the basic commands are described first, followed by the high-level commands. The description of the high-level commands is preceded by details of the station control block on which the commands are based.

Commands

Comma	and Code		
Hex	CCW Bits	Command	Туре
	0 1 2 3 4 5 6 7		
01	0 0 0 0 0 0 0 1	Write	Basic
02	0 0 0 0 0 0 1 0	Read	Basic
03	0 0 0 0 0 0 1 1	No-op	Basic
04	0 0 0 0 0 1 0 0	Sense	Basic
05	0 0 0 0 0 1 0 1	Write PlU	High level
06	0 0 0 0 0 1 1 0	Read PIU	High level
08	0 0 0 0 1 0 0 0	Transfer-in-channel	Basic
09	00001001	Autopoll	High level
OB	0 0 0 0 1 0 1 1	Control SCB	High level
OF	0 0 0 0 1 1 1 1	Po11	High level
14	0 0 0 1 0 1 0 0	Sense SCB	High level
23	00100011	Set mode	Basic
27	0 0 1 0 0 1 1 1	Enable	Basic
29	00101001	Dial	Basic
2F	0 0 1 0 1 1 1 1	Disable	Basic
Ε4	1a 1 1 0 0 1 0 0	Sense 1/0	Basic

Basic Commands

Transfer-in-channel

This is the standard branch command. Two 'transfer-in-channel' commands may not be chained together, nor may a 'transfer in channel' be the first command in the chain. Data chaining is allowed across a 'transfer-in-channel' command.

No-op

This command terminates immediately with the channel end and device end bits set in the unit status.

Enable

The 'enable' command puts the line attachment into the operational state. If the line attachment is not enabled, all commands (except 'no-op', 'sense', 'sense 1/0', enable', 'disable', 'dial', and 'set mode') are rejected with unit check set in the CSW and the command reject bit set in sense byte 0. If the 'enable' command is issued to a privately-owned or leased line, channel end and device end are presented when the line attachment detects the 'data set ready' signal being raised by the modem. If 'data set ready' is not detected within three seconds of the line attachment raising the 'data terminal ready' signal, the 'enable' command ends with unit check set. If the 'enable' command is given to a switched line, the line attachment is conditioned to answer an incoming call automatically, assuming the modem has auto-answer capability. Channel end and device end are then presented when an incoming call is received. No timeout is associated with the 'enable' command for a switched line.

Disable

The 'disable' command puts the addressed line attachment into the non-operational state. A disabled line attachment no longer searches for character phase, executes any command (except 'no-op', 'enable', 'disable', 'dial', 'sense', 'sense 1/0' or 'set mode'), or reacts to an incoming call. If the 'disable' command is given to a private or leased line, channel end and device end are indicated after one second. If given to a switched line, the command causes the modem to disconnect. A 25-second timeout (for modems using the CCITT option - Connect Data Set to Line (CDSTL) procedure) or a one second timeout (for all other modems) is started, and if the modem has not disconnected when the timeout expires, the 'disable' command ends with unit check set and the timeout complete bit set in sense byte 0.

Dial

The 'dial' command causes the line attachment to be enabled and a data transfer from processor storage to the automatic calling unit (ACU) to be performed. If the autocall feature is not installed in the CA or if the line attachment is not defined as switched, the 'dial' command is rejected and the line attachment is not enabled. The 'dial' command is also rejected if the line has not been disabled.

The program is responsible for sending to the ACU the following characters only:

- 1. The correct number of dial digits, which are decimal values from 0 to 9.
- 2. The end of number (EON) or separator (SEP) character, if this character is required by the ACU.

The data is transferred from the location specified in CCW bits 8 to 31 and ascending locations until the count in CCW bits 48 to 63 is reduced to zero. In the data thus transferred, only bits 4 to 7 of each byte are actually placed on the interface (the digit lines) of the calling unit. The line attachment does not check the validity of the data sent to the ACU. The following table shows the relationship between the processor storage byte and the dial digit:

	Storage Byte	Equivalent
	0 1 2 3 4 5 6 7	Dial Digit
	x x x x 0 0 0 0	0
	x x x x 0 0 0 1	1
	x x x x 0 0 1 0	2
The dial	x x x x 0 0 1 1	3
operation	x x x x 0 1 0 0	4
ignores	x x x x 0 1 0 1	5
bits 0, 1	x x x x 0 1 1 0	6
2, and 3	x x x x 0 1 1 1	7
	x x x x 1 0 0 0	8
	x x x x 1 0 0 1	9
	x x x x 1 1 0 0	EON
	x x x x 1 1 0 1	SEP

The EON (end of number) character is an optional character which marks the end of the dial-digit group for those ACUs that require such an end character. Whether or not EON is used therefore depends on the type of ACU connected. Some ACUs recognize EON, some do not, and some can be set either to recognize or not recognize EON. ACUs which recognize EON may use the character as a signal that an answer may be expected from the remote station, or as a signal that dialing is complete (avoiding a timeout). The EON character should be inserted in processor storage as the last dial digit. EON is not required in the USA.

The separator character (SEP) can optionally be inserted in processor storage and included with the dial digits, following an access digit. For a private automatic branch exchange (PABX) extension, this character delays dialing to allow the dial tone to be returned from the public exchange.

The dial digits are presented to the ACU at a rate set by the ACU.

If a connection is not established before the timeout set by the ACU elapses, the 'Abandon Call and Retry' (ACR) signal is activated by the ACU. This condition initiates a 60-second delay in the autocall feature which prevents an immediate retry of the 'dial' command by delaying termination of the current 'dial' command, thereby preventing excessive use of the public exchange. This delay is one second on systems delivered in the USA and Canada. After the delay, the 'dial' command ends with unit check set in the CSW and the timeout complete bit set in sense byte 0. The 'dial' command may now be retried. The number of retries is controlled by the program.

A long timeout (60 seconds) is set in the autocall feature to monitor the progress of the ACU. If this timeout expires, the 'dial' command ends with unit check set and intervention required in sense byte 0.

If the ACU has its power indicator off, or if the 'data line occupied' (DLO) signal is active during command initiation, the 'dial' command ends with unit check in the initial status and intervention required in sense byte 0.

Certain other error conditions in the ACU or associated modem cause the 'dial' command to terminate with unit check set and the lost data bit set in sense byte 0. The section "Error Information" describes all error conditions which cause sense bits to be set.

Set Mode

This command is used to change the status of a line attachment or the SDLC-CA. Up to eight bytes of control data may be transferred with one 'set-mode' command. If less than eight bytes are transferred, no change occurs in the setting of the remaining bytes. For instance, a 'set mode' command with a field length of one will only cause a change in control byte 0. The control bytes are:

Byte O: Dynamic changes

<u>Bit</u>	Setting	Meaning
0	1	Change the datapoll index. Byte 1 contains the new value of the datapoll index. If byte 1 is not provided, that is, the field lenth of the 'set-mode' is one, the datapoll index is reset to zero.
	0	Do not change the datapoll index. Byte 1, if provided, is not used.
1	1	Change the contactpoll index. Byte 2 contains the new value. The contactpoll is reset if byte 2 is not provided.
	0	Do not change the contactpoll index. Byte 2, if provided, is not used.

2-7

Reserved, must be zeros.

- <u>Byte</u> 1: Datapoll index. This byte defines an index start value. The index is used to point at a specific entry in a table of station control blocks (SCBs). The table is used during the data poll function of autopoll operations. The index can have any value from 0 through 255.
- <u>Byte 2</u>: Contactpoll index. This byte defines an index start value. The index is used to point at a specific entry in a table of station control blocks (SCBs), to be used during the contact polling function of autopoll operations. The index can have any value from 0 through 255.
- <u>Byte</u> 3: Contactpoll frequency. The value in this byte specifies how many times data polling operations of the 'autopoll' command are to be encountered before a contactpoll function on the line is performed. The contactpoll frequency can be set to any value from 0 through 255.
- <u>Byte 4</u>: Service seeking pause. This byte specifies how long the line attachment will pause during the contactpoll function of an 'autopoll' command before it terminates when no contactpoll operation has been performed. No pause is made when a contactpoll operation is performed. The purpose is to reduce unnecessary overhead from nonproductive polling. The service seeking pause is specified in tenths of a second. Any time from 0 through 25.5 seconds can be specified.

<u>Byte 5</u>: Idle detect timeout (primary station) or nonproductive receive timeout (secondary station). This byte defines a timeout value as follows:

1. Operation as primary station.

Whenever the line attachment detects the poll bit set to one in a transmitted frame, it turns to receive mode, starts an idle detect timer, and waits for an incoming frame. If no frame is received before the idle detect timeout elapses, the line is monitored for 15 ones. If they are received the line turns to outbound direction. The timeout is specified in tenths of a second. Any value from 0.1 through 25.5 seconds can be specified. A value of 0 indicates no timeout, and the line attachment waits indefinitely for incoming frames. A 'halt 1/0' or 'halt device' instruction may now have to be issued to terminate the channel program.

2. Operation as secondary station.

Whenever the line attachment detects the final bit set to one in a transmitted frame, it turns to receive mode, starts an inactivity timer, and waits for an incoming frame. If no frame is received before the inactivity time elapses, the channel program terminates. The inactivity timeout is specified in seconds. Any value from 1 through 255 seconds can be specified. A value of 0 indicates no timeout, that is, the line attachment waits indefinitely for incoming frames. A 'halt 1/0' or 'halt device' instruction may now have to be issued to terminate the channel program.

Byte 6: Mode setting during initialization.

Bit Setting Meaning

1

0

- 0
- Secondary station. The line attachment is to act as a secondary station on this line. Primary station. The line attachment is to act as a primary station on this line.
- 1-7 Reserved, must be zeros.
- <u>Byte</u> 7: SDLC address as secondary station. This byte contains the SDLC address for which the line attachment as a secondary station will monitor in receive mode when a 'read' command has been given. (If an SCB was passed to the line attachment after the 'set mode' command with secondary address, the station address of the SCB will be used.) This

byte must be transferred if byte 6 specifies a secondary station.

The command is terminated with data check if the data has the format; for example, if reserved fields are not zero or the secondary station address is not transferred although specified in byte 6. The secondary station address is not accepted in these cases.

Sense

The 'sense' operation transfers up to 24 bytes of sense information to the processor storage location specified in bits 8 to 31 of the CCW. (For details see 'Sense Information'.)

Sense I/O

The 'sense 1/0' operation transfers up to seven bytes defining the line configuration, as follows:

- Byte 0: Always X'FF' Byte 1: CPU Identification 1 Byte 2: CPU Identification 2 Byte 3: CPU Identification 3 Byte 4: X'CA' (communications adapter) Byte 5: Bit 0: one Bit 1: zero Bit 2: zero Bit 3: zero Bit 4: Not NRZI mode Bit 5: Business machine clocking
 - Bit 6: Autocall unit installed
 - Bit 7: Secondary station

Byte 6:

- Bit 0: Permanent request to send
 - Bit 1: Switched line
 - Bit 2: New synchronisation
 - Bit 3: Connect data set to line
 - Bit 4: Integrated modem
 - Bit 5: Not used
 - Bit 6: High speed line
 - Bit 7: Integrated modem with manual answer

£ ¥ %

R e a d

The 'read' command transfers an incoming frame into processor storage.

Starting Conditions.

The command will only be accepted if:

- 1. The line is enabled
- 2. The line is set to inbound direction
- In secondary mode an address has been transferred by a 'set mode' command
- 4. The CCW has the right format

Otherwise the command is rejected and the line status is not changed.

Normal Flow.

Incoming data is transferred to the processor storage area defined in the command. Included is all data after the starting flag, up to and excluding the frame check sequence (FCS) bytes.

If a P/F bit is received, the line is turned to the outbound direction.

Exceptional Conditions.

- 1. Frame with wrong address received.
- This condition applies only to a line in secondary mode.
 The address field of the incoming frame is compared with the address transferred by a 'set mode' command or by a past SCB. If the address does not match, the frame is ignored. The line attachment starts searching for a new frame. The 'read' command remains active.
 Invalid frame or 'abort' sequence received.
- 2. Invalid frame or 'abort' sequence received. If the line is secondary and the FCS bytes indicate an invalid frame, the frame is too short or, if the frame is terminated with an 'abort' sequence, the frame is ignored. The line attachment starts searching for a new frame and the command remains active. In the case of a primary line, a unit check (with data check set in sense byte 0) is generated.
- 3. Buffer too short, overruns. If the count field is exhausted before all incoming data is transmitted into processor storage, or if the line cannot be serviced in time, a unit check (with data check or overrun set in sense byte 0) is generated.

Write

The 'write' command causes data to be transferred to the line attachment from the processor storage location specified in the CCW. The data specified in the CCW by the address and count field is furnished with surrounding flags and FCS bytes to make a frame which is transmitted over the line. If an F/P bit is specified in the command field of the frame, the line is turned to the inbound direction.

Starting Condition.

The 'write' is only accepted if:

1. The line is enabled

2. The line is in outbound direction

3. The count field is greater than or equal to two

4. The CCW has the correct format

Otherwise the command is rejected and the line status is not changed.

Overrun.

If the line cannot be serviced in time by the CA, a unit check is generated with overrun set in sense byte 0. The transmission of the frame is terminated with the 'abort' sequence. The line stays in the outbound direction if working in primary mode. Otherwise the line is turned to the inbound direction.

High-Level Commands

The description of high-level commands is preceded by details of the station control block on which these commands are based.

Station Control Block

New capabilities are provided in the SDLC-CA by high level commands. The line attachment can repeatedly poll all stations for outstanding messages or for initial contact. The line attachment can also handle the address and control fields of the SDLC frames transmitted or received. For each station being serviced, specific information is required in the line attachment. This information is contained in a station control block (SCB). The 'autopoll', 'control-SCB', 'read-PIU', 'write-PIU', 'poll', 'sense-SCB', and 'sense' commands require or use one or more SCBs. The 'autopoll' command points at a contiguous table of SCBs, which are sequentially fetched during polling. The 'control-SCB' command is used to transfer one specific SCB to the line attachment. The 'read-PIU', 'write-PIU', and 'poll' commands must be preceded by an 'autopoll' or 'control-SCB' so that one SCB, called the <u>current SCB</u>, is available in the line attachment. The current SCB is retrieved by the access method with a 'sense-SCB' command. In addition the 'sense' command may be used to read out the sense information together with the current SCB after a unit check occurs.

SCB format

Each SCB contains 20 bytes, 12 of which are transferred from the access method to the line attachment with the 'autopoll', or 'control-SCB' commands. The 'sense-SCB' command returns all 20 bytes. The extra bytes reflect the outcome of the channel program executed with respect to the number of data buffers used and any exceptional conditions.

0 (0) OFFSET 	1 (1) ADDRESS	2 (2) RESERVED	3 (3) CTLFLAGS
+ 4 (4) NSCUR 	5 (5) RESERVED 	6 (6) NSACK	7 (7) NRACC
+ 8 (8) 	+	+	++
12 (C) CMDIN 	13 (D) RESERVED 	14(E) CFRS	15 (F) CRBUF
16 (10) RESERVED 	17 (11) RESERVED 	18 (12) EXCFLAGS1	19 (13) EXCFLAGS2

SCB layout:

Notes:

- 1. Hex values are shown in brackets.
- Bytes 12 through 19 (hex 'OC' through '13') are only transferred from the line attachment to the access method with the 'sense-SCB' command or the sense instruction. They are never transferred in the reverse direction.

Byte 0. Offset: This byte contains the buffer offset. When data is transferred to processor storage during the execution of a 'read-PIU' command, the offset is added to the data address of the CCW and the data is stored beginning at this modified address. Similarly, during a 'write-PIU' operation the data is transferred from processor storage to the line attachment starting from an address formed by adding the offset to the CCW data address. The offset may range from 2 through 255. If an SCB is transferred to the line attachment with an offset of 0 or 1, the channel program terminates with data check. Note: This mechanism is provided mainly to handle 1-frames, but it also applies to other frames.

Byte 1, Address: This byte contains the SDLC station address. The CA uses the address field when building outbound I-frames or poll frames. Inbound, the address field of frames received in response to poll is checked against the address field. In a mismatch, a soft error is indicated if the CA is running as primary station; the frame is ignored if the CA is running as secondary station.

<u>Byte 2, Reserved:</u> The reserved field must be zero.

Byte 3, Control Flags: The bits in the control flags are defined as follows:

Bit 0, Skip
1 = Inactive station, do not poll
0 = Active station, poll

Bit 1, Autopoll

Bit 2, Slowout 1 = Send 'RNR' poll 0 = Send 'RR' poll

Note: Bit 2 is also defined as a global value for the SDLC-CA using the 'set-mode' command in any subchannel with SDLC operation. A logical 'or' is formed between the global bit and the slowout bit. A result of one indicates a slowout condition. Therefore, when slowdown mode has been set by the 'set-mode' command, 'RNR' polls are sent regardless of the SCB contents.

Bit 3, Slowin 1 = 'RNR' reply to poll expected 0 = 'RR' reply to poll expected

Note: Whenever the expected reply is received from a station, the autopoll operation continues; it terminates with the channel end, device end, and status modifier bits set when an unexpected reply is received.

Bits 4-7, Reserved: Must be zeros.

Byte 4, NSCUR: This byte contains the SDLC number (modulo 8 number) of the next I-frame to be sent. The number is set into the I-frame control field during 'write-PIU' operations. NSCUR is incremented by one modulo 8 after each I-frame transmitted. If NSCUR becomes equal to NSACK, this indicates that outstanding I-frames must be acknowledged before more can be sent. Any further 'write-PIU' command is therefore terminated with command reject and unit check indicated.

Byte 5, Reserved: Must be zero.

Byte 6, NSACK: This field contains the SDLC number (modulo 8 number) of the latest I-frame acknowledged by the remote station. Whenever a response containing an Nr field is received from a station, the line attachment uses it to update NSACK. The absolute difference is also set into the CFRS field. If the received Nr is outside the range from NSACK to NSCUR (modulo 8), unit check is presented with sense information indicating an unexpected Nr field. (The control byte received is set into the CMDIN field of the SCB.)

Byte 7, NRACC: This field contains the SDLC number plus one (modulo 8) of the last valid I-frame received. The line attachment sets the contents of this field into the Nr part of the SDLC control field during polling and I-frame transmission. The NRACC field is also used when valid I-frames are received. The line attachment compares the received Ns field with the contents of NRACC. The I-frame is accepted if they are equal. The NRACC field is then incremented by one modulo 8. If an invalid frame is received, NRACC is frozen and no more I-frames are accepted until a valid frame with the poll/final bit equal to one has been received or a timeout has occurred. If the received Ns does not correspond with the NRACC value and the CA is not skipping invalid frames, unit check is presented, with sense information indicating that received I-frames were out of order. CMDIN now contains the control field from the erroneous frame. (The channel program is not terminated, however, until a valid frame with the poll/final bit equal to one is received or a timeout occurs.)

Bytes 8-B, <u>IDENT</u>: This field is used by the access method to identify each SCB-entry. It is passed without change between the access method and the line attachment.

<u>Byte C, CMDIN</u>: This byte is the command received field. If the frame received does not contain the control byte defined in the flags field, this field is stored in the CMDIN field for further examination by the access method.

Byte D, Reserved: Must be zero.

<u>Byte E, CFRS</u>: This byte contains the count of frames sent and acknowledged. The field is zero based. When the line attachment changes NSACK because of a newly received Nr, the absolute difference is accumulated in the CFRS-field. The contents of this field are used by the access method to release the appropriate 'write-PIU' buffers containing the frames acknowledged. If CFRS is not equal to the number of frames transmitted, some frames have been lost. The access method must now back NSCUR to NSACK and modify the channel program to retransmit the lost frames.

Byte F, CRBUF: This byte contains the count of receive buffers used. The line attachment sets into this field the number of productive 'read-PIU' commands executed by the channel program, that is, 'read-PIU' commands with data transfer of valid frames. This field can be used by the access method to determine the number of unused buffers to be released.

Byte 10, Reserved: Must be zero.

Byte 11, Reserved: Must be zero.

Byte 12, EXCFLAGS1: This field contains byte one of the exception flags, and stores information about exceptional conditions which occurred during the execution of the previous channel program. This field is inspected by the access method and if it is all zeros, no exceptional conditions occurred.

Bit O, SOFTERR (soft error indicator). This bit is set to one by any soft error. The EXCFLAGS2 byte indicates the reason.

Bit 1, LFNSI (last frame contains non-sequenced information). This bit is set to one if non-sequenced information is received during the execution of the channel program. The information is set into the last receive buffer used so that the access method can interrogate.

Bit 2, STRANS (remote station transition occurred). This bit is set to one if RNR is received from the remote station when the CTLFLAGS field indicates that the station is expected to send RR, or vice versa.

Bit 3, CIUSE (CMDIN field used). This bit is set to one when an SDLC command is set into the CMDIN field. This occurs when any unexpected command is received. Bit 4, DIRECTION (line direction). This bit is set to one when the line direction is outbound.

<u>Byte 13, EXCFLAGS2</u>: This field represents byte two of the exception flags and contains (in encoded form) the reason for the soft error indicated in the summary bit SOFTERR. For the list of codes see 'Soft Errors and RECOVERY'.

All SCB fields transferred from the access method to the line attachment are initialized by the access method.

The ADDRESS, OFFSET, CTLFLAGS and IDENT fields are never altered by the line attachment.

The CFRS, CRBUF, EXCFLAGS and CMDIN fields are updated by the line attachment only.

The remaining fields (NSCUR, NSACK, and NRACC) are normally managed by the line attachment but are altered by the access method in exceptional situations.

The reserved fields must be zero and the offset must be greater than one. The five leading bits of the sequence count fields are ignored on outbound commands and are undefined on inbound commands and instructions.

High level commands

Autopoll

This command provides two functions, which are executed in sequence: a data polling function and a contact polling function. In the data polling function, several remote stations are requested in turn to transmit data to the line attachment. The command is normally used in a multipoint network (where several secondary stations are connected to the same line); it can also be used in a point-to-point installation.

A datapoll index per line attachment is used to point to the next SCB to be interrogated. This index is normally maintained by the line attachment; it may also be changed with the 'set-mode' command.

The contactpoll function is only executed for primary stations. It is used to invite disconnected stations to

enter normal response mode. The stations are specified in a table of SCBs. Flag bits in the SCB indicate whether a station is disconnected and should be contactpolled, or whether the station is in normal response mode (NRM) for datapoll operation.

There are two tuning parameters for the contactpoll function:

- 1. A frequency counter, which determines how often the stations should be contactpolled when they are found in the table of SCBs.
- 2. A service seeking pause, which defines a time to delay command termination during low traffic periods in order to reduce processor interference due to nonproductive polling.

Both parameters can be changed with the 'set-mode' command.

A contactpoll index per line attachment is used to point at the next SCB to be interrogated. This index is normally maintained by the line attachment but may also be changed with the 'set-mode' command.

Starting Conditions.

The command is only accepted if:

- 1. The line is enabled.
- 2. The line is set for outbound operation.
- 3. The CCW has a valid format. The general rules must be kept and data chaining must not be specified.
- 4. The data address is on a fullword boundary and the count is at least 12 and not greater than 2K.

Otherwise the command is rejected and the line status is not changed.

Normal Flow for Data Polling Function.

The 'autopoll' command points at a table of SCBs, one for each station on the line. The line attachment initially fetches the SCB indicated by the datapoll index, making it the current SCB. If the index points outside the SCB table, the index value is reset to zero, making the first SCB entry current.

If the SCB flags indicate that the station is inactive or a contactpoll operation is requested, the line attachment updates the datapoll index by one and fetches the next SCB. If the flags indicate datapolling for this station, a poll frame is sent.

The address and command fields are constructed using the information of the current SCB. The P/F bit is always set to one.

The line attachment then goes into receive mode. Further actions by the line attachment depend on the reply of the remote station, as described in the following text. The received reply may be one of the following:

- a. RR or RNR received as specified in the SCB. This indicates that the remote station has nothing to send and has not changed its mode between slowdown and normal data transfer mode. The line attachment updates the datapoll index by one and repeats the same actions as described above, until the SCB table is exhausted.
- b. Unexpected command, that is:
 - RR received when RNR was expected, or
 - RNR received when RR was expected, or
 - RR or RNR received as expected but the Nr value is different from the corresponding field of the current SCB, or
 - Any other command including l-frame and nonsequenced frame, or
 - Erroneous frames such as frames with a wrong address (primary mode only), invalid frames, and frames which terminate with an ABORT sequence. (Note: Frames with a wrong address are ignored in secondary mode.)

The command is terminated with the channel end, device end, and status modifier bits set. This situation normally causes a transfer in the channel program to a 'read PIU' or 'sense SCB' command which will process the incoming frame. (See 'read PIU' and 'sense SCB' commands.)

The datapoll index is not updated when the status modifier is presented. If, therefore, I-frames have been received from a remote station, this station will be the first polled the next time the datapoll operation is resumed. This is normally the correct mode of operation but the access method may turn to another station using the 'set-mode' command to change the datapoll index.

When the datapoll index returns to the value it had at the beginning of the datapoll operation, one complete scan has been made. The command now executes the contactpoll function.

Error Conditions of Data Polling Function.

Overruns.

If the line cannot be serviced in time by the CA, an overrun indication is generated. If this happens during outbound transmission, the frame is terminated with the ABORT sequence. The line stays set to the outbound direction if working in primary mode. In secondary mode the line is turned to inbound.

Normal Flow of Contact Polling Function.

The execution of the 'autopoll' command is as follows:

Each time the contactpoll function of an 'autopoll' command is executed the frequency counter is decremented by one until it reaches zero.

- If the counter is not zero the contactpoll command is terminated without updating the contactpoll index.
- If the frequency counter has reached zero, the line attachment scans the SCB-table until it finds an entry to be contactpolled or until a complete scan of the table has been made. If the contactpoll index initially points outside the SCB table, the index is reset to zero before the scan begins. If Possible, a contactpoll operation is performed, or if no station is found for contactpolling, a service seeking pause is made.

A contactpoll operation proceeds as follows:

- 1. AN 'SNRM' frame with the station address of the current SCB is transmitted. The P/F bit is set.
- 2. The line attachment goes into receive mode. The idle detect timer is started. One of the following situations then arises:
 - a. No reply: If the remote station is inactive, the idle timer elapses in the line attachment. This is the normal situation. The contactpoll function of the autopoll command now ends with channel end and device end set. The contactpoll index is updated by one.
 - b. Reply is disconnected mode (DM): The service seeking timer is started. If it has elapsed the command ends with channel end and device end set.

c. Any other reply: If any frame is received, the command terminates with channel end, device end, and status modifier set. This normally causes a transfer in the channel program to a 'read PIU' or 'sense SCB' command to process the incoming frame. (See 'read PIU' and 'sense SCB'.)

Error Conditions for Contact Poll Function.

Overrun.

If the CA cannot service the line in time, an overrun soft error indication is generated. If the overrun occurs during an outbound operation, the transmission of the frame is terminated with the ABORT sequence. The line stays set to the outbound direction.

All following line-affecting commands in the same channel program are treated as no-ops.

Error Conditions for Data and Contact Poll.

Errors during SCB-Fetch.

If errors occur during the fetching of the SCB, the channel program is terminated with the appropriate channel status.

A wrongly formatted SCB (the reserved fields are not zero or the offset is not greater than one) is indicated as a data check. A following 'sense SCB' or 'sense' operation delivers undefined values.

Poll

The 'poll' command is used after a chain of 'write-PIU' commands to transmit a final 'RR' or 'RNR' (depending on the state of the line attachment). The poll/final bit is set; it is never set in I-frames transmitted by a 'write PIU' command. All information required is taken from the current SCB. The line is turned to inbound when the 'poll' command has been executed.

Starting Conditions.

- The 'poll' command is accepted only if:
 - 1. The line is enabled.
 - 2. The line is set to outbound.
 - 3. An SCB was passed to the line attachment in the current channel program.
 - 4. The CCW has the right format.

Otherwise the command is rejected without change to the line status.

Overrun.

If the CA cannot service the line in time, an overrun unit check condition is generated.

The transmission of the frame is terminated with the ABORT sequence. The line stays set to outbound if operating in primary mode. Otherwise the line is turned to inbound.

Read PIU

The 'read PIU' command transfers the path information unit of an incoming I-frame and the length of it into processor storage.

Starting Conditions.

The 'read PIU' command is only accepted if:

- 1. The line is enabled.
- 2. The line is set to inbound.
- 3. An SCB was passed to the CA in the current channel program.
- 4. The CCW has a valid format. In addition to the general rules, the first two bytes must not cross a page boundary and data chaining must not be specified.
- 5. At least one byte of the I-field must be accommodated in the first buffer, that is, the CCW length must be at least equal to the offset plus 1.

Otherwise the command is rejected without change to the line status.

Normal Flow.

1. A valid I-frame is received.

The 1-field is transferred to processor storage. The starting address is the command data address plus the offset field of the current SCB. The data transfer continues until the terminating flag is found or the storage area is exhausted. The frame check sequence bytes are not transferred.

If the storage area is exhausted a test is made to determine whether the frame has ended and another 'read PIU' command is chained. (This situation is referred to as 'data spanning'.) If so, the chained 'read PIU' command specifies the next data area to continue the data transfer, and the CRBUF field of the current SCB is bumped, that is, a one-bit is added. Otherwise, the frame is read up to the ending flag without further data transfer. In any case the total length of the frame plus offset is stored into the first two bytes of the first buffer. The Nr count of the frame received is used to update the NSACK and CFRS fields of the SCB.

If the total frame was transferred into processor storage the CRBUF and NRACC fields of the current SCB are bumped.

The 'read PIU' command ends with channel end and device end set.

2. Valid non-I frames received.

Non-sequenced Frames

The command field is stored into the CMDIN field of the current SCB. The CIUSE bit in the exception flag byte of the current SCB is set.

If the frame has an I-field it is treated the same way as the I-field of an I-frame. Data spanning applies and the length field is stored into the first buffer. The LFRNSI bit in the exception flag byte of the current SCB is set.

After one non-sequenced frame is received, all further inbound data is ignored except for a P/F bit (see 'P/F bit received'), and the remaining channel program is flushed.

<u>Programming Note:</u> The term flushing means to execute all commands except for their line-affecting parts; that is to:

- Perform chaining.
- Test the validity of the command code and format (raising unit check and discontinuing flushing if any error is present), but not to test the data address and whether the data buffer is fixed.
- For an 'autopoll' command, to set the status modifier.

Supervisory Frames

The Nr count is used to update the NSACK and CFRS field in the current SCB. If an RR was expected but the RNR was received or vice versa, the STRANS bit in the exception flag byte of the current SCB is set.

The command field is stored into the CMDIN field of the current SCB, and the CIUSE bit in the exception flag byte of the current SCB is set.

When one supervisory frame is received, all further inbound data is ignored except for a P/F bit (see 'P/F bit received'), and all following line-affecting commands in the same channel program are treated as no-ops. 3. P/F bit received.

When a P/F bit is received the line is turned to outbound. The remaining channel program is flushed.

Error Conditions.

1. Frame with wrong address received.

The address field of the incoming frame is compared with the address in the current SCB. If the addresses do not match, the action depends on the line mode:

- a. If the CA is acting as a primary SDLC station, a soft error indication is generated.
- b. If the CA is acting as a secondary station, the frame is ignored. The line attachment starts searching for a new frame. The 'read PIU' command remains active.

2. Erroneous I-frame received.

If the Ns field is out of sequence, that is, the NRACC field of the SCB does not match the Ns field, or if the Nr field is out of sequence, that is, the Nr is not between the NSCUR and NSACK values (modulo 8), a soft error indication is generated.

3. Invalid frame received.

If the FCS bytes indicate an invalid frame or if the frame is too short, a soft error indication is generated.

4. ABORT sequence received.

If a frame is terminated with an ABORT sequence, a soft error indication is generated.

5. Overruns.

If the line cannot be serviced in time by the CA a soft error indication is generated.

In cases 1a and 2 to 5, the remaining channel program is flushed.

Write PIU

The 'write PIU' command transmits an I-frame. The address and command fields are generated by the line attachment using the current SCB. A 'control-SCB' command should therefore precede the first 'write-PIU' command in the channel program to transfer the appropriate SCB.

The 'write-PIU' command is symmetrical with respect to the 'read-PIU' command: the length of the PIU plus offset is transferred as the first two bytes of the buffer area and the OFFSET field of the SCB is added to the data address field of the 'write-PIU' command to form the starting address of the PIU to be transmitted.

Starting Conditions.

The command is only accepted if:

- 1. The line is enabled.
- 2. The line is set to outbound.
- 3. An SCB was passed to the CA in the current channel program.
- 4. The CCW has a valid format. In addition to the general rules, the first two bytes must not cross a page boundary, and data chaining must not be specified.
- 5. The length of the I-field specified must be at least one, and at least one byte must be specified in the first buffer if data spanning applies (see below).

Otherwise the channel program is rejected without a change to the line status.

Normal Flow.

A total I-frame is transmitted.

The address byte is taken from the current SCB.

The command field is constructed using NSCUR and NRACC from the current SCB for Ns and Nr respectively.

The P/F bit is always at zero.

The I-field is transferred from processor storage. The starting address is the command data address plus the OFFSET field of the current SCB.

The I-field length plus offset is specified in the first two bytes of the data area.

The 1-field may extend over more than one data area. Consecutive data areas are specified in chained 'write PIU' commands. Data is taken from the start of the succeeding areas, the offset scheme not being used. The length given in the first data area continues to apply (this situation is referred to as 'data spanning').

The FCS characters accumulated by the CA and the trailing flags are sent after the I-field.

The NSCUR field of the current SCB is updated.

The outbound direction of the line is maintained.

Invalid Frame Length.

If the data count is exhausted during transmission and the frame length specifies further I-field bytes, a test is made to determine whether data spanning is specified. If so, a 'write PIU' command must follow. If not, unit check and command reject are set.
The transmission of the frame is terminated with the ABORT sequence. The line stays set to outbound if working in primary mode. Otherwise the line is turned to inbound.

Overrun.

If the CA cannot service the line in time a soft error indication is generated and the command is terminated.

The transmission of the frame is terminated with the ABORT sequence. The line stays set to outbound if working in primary mode. Otherwise the line is turned to inbound.

Too Many Frames To Be Sent.

If too many frames were sent without being acknowledged (NSCUR reaches NSACK) a further 'write PIU' command generates unit check and command reject.

Control-SCB

The 'control-SCB' command is used to transfer a specific SCB to the line attachment. It normally precedes a 'write-PIU' or a chain of 'write-PIU' commands, giving the line attachment the information necessary to build outbound I-frames. The line attachment must be enabled before a 'control-SCB' command is accepted. Otherwise a unit check termination is generated with command reject set.

Twelve data bytes are transferred with the 'control-SCB' command to form the current SCB. The data address specified must be on a fullword boundary and the length count must be at least twelve. Otherwise the command is terminated with unit check and command reject set.

Data chaining must not be specified.

Errors during SCB-Fetch.

If errors occur during the fetching of the SCB, the channel program is terminated with the appropriate channel status.

A wrongly formatted SCB (reserved fields not zero or offset not greater than one) is indicated as a data check. A following 'sense SCB' or 'sense' operation delivers undefined values.

Sense SCB

The 'sense SCB' command is used to retrieve the current SCB after a line 1/0 operation is completed. Twenty bytes are transferred. They contain indications of errors and unusual conditions plus updates to the frame/buffer and Ns/Nr counts. Since the 1/0 operation may have started as a

result of an autopoll or contactpoll operation, the current SCB has the only indication as to which station responded. The access method transfers appropriate fields to its copy before restarting the channel program.

If the line is set to the inbound direction, the 'sense SCB' command functions in addition as a 'read PIU' command with the exception that no incoming I-field is transferred to processor storage.

With this subfunction the 'sense SCB' is a line-affecting command.

If no SCB was transferred after an 'enable' operation, all zeros are returned.

The line attachment must be enabled before a 'sense SCB' command is accepted, otherwise a unit check termination is generated with command reject set.

The data address specified must be on a fullword boundary and the length count must be at least twenty, otherwise the command is terminated with unit check and command reject set. Data chaining must not be specified.

Channel Program Rules

- 1. The line must be enabled for the following commands:
 - Control SCB
 - Sense SCB
 - Autopoll
 - Poll
 - Read
 - Write
 - Read PIU
 - Write PIU
- 2. Only 'no-ops' and 'TICs' are allowed between 'read PIUs' or 'write PIUs' during data spanning.
- 3. When the line is active (no P/F bit was received) any commands that do not affect the line may cause overruns.
- 4. No more than 127 channel commands will be accepted in a flushing situation.
- No more than seven immediate commands ('no-op', 'set mode', sense', 'sense I/0') in sequence will be accepted.

Channel Program Examples

The examples in this section do not necessarily reflect actual use of the channel commands. They are valid sequences to illustrate operations. Primary station on a multipoint line during normal operation.

Channel Program:

START:	NOP Notes: TIC to AUTOP(TIC to XMIT)	1 2
AUTOP:	AUTOPOLL TIC to START	1, 3
RECV:	READ PIU READ PIU READ PIU SENSE SCB	1 1 1 4
XMIT:	CONTROL SCB WRITE PIU WRITE PIU WRITE PIU POLL TIC to RECV	1, 5 1 1 1, 6 7

Notes:

1. Command chained.

- 2. This command becomes a TIC to the XMIT path when frames are ready to be sent.
- 3. 'Autopoll' points to a table of SCBs. The SCB fields indicate the kind of poll to send to each station and the response expected. If the response is unexpected, the status modifier bit is set, causing the subsequent TIC to be skipped.
- 4. This 'sense SCB' command transfers the current SCB to processor storage. It shows:

• Which station responded to the 'autopoll' command.

• How many frames were received.

• Whether any errors occurred.

- If the RECV path followed XMIT, how many frames were successfully sent.
- 5. The 'control SCB' command provides a new current SCB. It indicates for the line attachment:
 - Where to send the data.
- What Ns/Nr values to put in the l-frame control field. 6. The station is polled to find out how many of the frames
- just sent were successfully received.
- 7. The XMIT path transfers to the RECV path for the response to the outbound frames (the response may be in an I-frame).

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Secondary station during initialization and normal operation.

Channel Program

INIT:	SETMODE ENABLE READ	Notes:	1,2 1 3
INTA:	CONTROL SCB SETMODE WRITE TIC to RECV		1,4 7 1,5
NORMAL:	NOP TIC to AUTOP (TIC to XMIT)	Notes:	1
AUTOP:	-	-	6
RECV:	READ PIU READ PIU READ PIU SENSE-SCB	_	1 1 1
XMIT:	CONTROL SCB WRITE PIU WRITE PIU WRITE PIU POLL		1 1

TIC to RECV

Notes:

1. Command chained.

- 2. A flag in the 'set mode' parameters indicates that the line is to be operated as a secondary. The address used in the 'read' command as station address is transferred. The nonproductive receive timer is set to infinite, so that the 'read' command will not terminate with timeout.
- 3. The 'read' operation is not completed until the primary station sends a frame, normally a contact poll frame (SNRM) with the address from the preceding 'set mode' command.
- 4. A new channel program is started after an SNRM is received (to be checked by the access method).
- 5. The 'write' command sends an unsequenced acknowledgement (UA) in response to the SNRM.The station address in the SCB is the expected address for all subsequent inbound data read by 'read PlU' or 'sense SCB' commands.
- 6. This 'autopoll' command serves for the datapoll function only.
- 7. This command sets a new value for the nonproductive receive timeout.

Primary station initialization on a switched autocall line.

Channel Program:

CONNECT:	D I SABLE D I AL	Notes:	1, 2 1, 3
	WRITE		1,4
	READ		5
CONTACT:	WRITE		1, 5
	READ		5
NORMAL:	• • • •		6

Notes:

- 1. Command chained.
- 2. The 'disable' command protects against a race condition if a previous 'enable' command for an incoming call was halted.
- 3. The 'dial' command sends the dial digits to the autocall unit associated with this line. The 'dial' command also implies 'enable'.
- 4. The first 'read'/'write' sequence sends the XID request and reads the terminal ID in the XID response. The ID information is used to build an SNRM and find or build the SCB for the station.
- 5. 'Write'/'read' can be used to send SNRM and read UA.
- 6. From this point on, operation is the same as for leased lines. The SCB table for this line will have only one entry since a switched line implies point to point.

Primary station error recovery in multipoint operation.

Error recovery involves retransmitting 1-frames sent but not acknowledged or repolling for bad frames received. Errors in retriable operations are detected by the line attachment but the retries themselves are initiated by the access method. No new channel programs are necessary to perform retries but awareness is needed to avoid retrying indefinitely.

The first bad I-frame received stops the transfer of data into the buffers. The NRACC and CRBUF fields are frozen and the READERR indicator is set in the current SCB. The 'read PIU' command is terminated normally when a frame with the P/F bit set to one is correctly received, or when a timeout occurs.

In this situation the timeout is handled as a retriable condition because the P/F bit may have been missed in a bad frame. The line attachment continues to look at frames and examine block check characters even though no data is transferred. The channel program ends with a 'sense SCB' command. The access method determines from the READERR indicator that an error has occurred. At this point everything is set up properly for repolling the station for the missed frames. The SCB must be updated with fields from the CA's copy and the channel program must be restarted. The autopoll index still points to the SCB last used and NRACC acknowledges only the good frames received. Before restarting however, the access method must determine whether a retry limit has been exceeded or whether some other station should be serviced.

For outbound frames, acknowledgement is found in the Nr field of the next RR, RNR, or I-frame received from the station. The access method determines an error when a mismatch is found between the number of frames sent and the number acknowledged (NSCUR with NSACK). To retry, NSCUR is reset to NSACK and the 'write PlUs' are started from the first frame missed. In this case the access method must maintain its own retry count.

Status Information

The following paragraphs describe the meanings of the status indications given in response to SDLC-CA commands.

Unit Status

The unit status is indicated in bits 32 to 39 of the CSW. The unit status shows, for example, the conditions under which an 1/0 operation ended.

- Bit Meaning
- 32 Attention
- 33 Status Modifier
- 34 Control Unit End
- 35 Busy
- 36 Channel End
- 37 Device End
- 38 Unit Check
- 39 Unit Exception

Note: If the channel detects errors when fetching the first CCW or when fetching a chained command, program check is set in the channel status. No unit status such as device end or channel end is presented.

Attention

This bit is not used by the CA and is therefore always zero.

Status Modifier

The status modifier is presented together with channel end and device end at command end time in the following cases:

- 1. In the datapoll function of the 'autopoll' command. The 'autopoll' command ends with the status modifier set if the reply from a remote station is an unexpected command or an I-frame, or if no reply at all is received within the timeout period.
- 2. In the contactpoll function of the 'autopoll' command. The 'autopoll' command ends with the status modifier set if a reply other than a DM frame is received from the remote station within the timeout period.

3. The 'autopoll' command is flushed.

Control Unit End

This bit is not used by the CA and is therefore always zero.

Busy

Busy is presented if an in-line test is active on a line addressed by an SIO instruction. A secondary interruption with device end follows.

Channel End and Device End

Channel end and device end are always presented together to indicate that the channel program is terminated. The setting of channel end and device end without unit check indicates normal termination.

Unit Check

Unit Check is presented in two different situations:

 If, during the initialization sequence, the line attachment detects that the first command cannot be executed, a CSW is presented with unit check set, but without channel end or device end. This unit status indicates that the line attachment does not accept the channel program for execution. The situation may occur as a result of one or more errors detected before the channel program has become active and the first command is not a 'sense', 'no-op', or 'sense 1/0'.

2. Unit check is presented together with channel end and device end if the line attachment finds the first sense byte to be non-zero when a command is about to terminate. This happens if one or more errors are detected during execution of this command. The section 'General Synchronization Rules' explains at what time (in relation to line activity and channel program) a unit check is generated.

Unit Exception

Unit exception is presented together with channel end and device end at command end time for 'enable' and 'dial' commands, as follows:

1. Enable

In switched network operation, when the command is successfully halted by a 'halt 1/0' or 'clear 1/0' instruction before a call is answered.

2. Dial

When the command is successfully halted by a 'halt 1/0' or 'clear 1/0' instruction before the channel stop signal is raised to signal the end of the dialing digits.

Channel Status

Bit	Meaning

- 40 Program controlled interruption (PCI)
- 41 Incorrect length
- 42 Program check
- 43 Protection check
- 44 Channel data check (not used)
- 45 Channel control check
- 46 Interface control check (not used)
- 47 Chaining check (not used)

Program Controlled Interruption

The PCI bit is set in the UCW of the addressed line when the PCI flag is found on during the initiation of a CCW.

The interruption condition due to the PCI is generated during the initiation of the command containing the PCI bit.

Incorrect Length

This bit is set in accordance with standard channel practice.

<u>Programming Note</u>: If the byte count is not decremented to zero at command termination, the incorrect length bit is set. This will suppress command chaining if the SLI bit is not set in the CCW.

All 'read' and 'write' type commands, where the message length is either unknown or not as specified, must have the SLI bit set to avoid suppression of command chaining.

The 'enable' and 'disable' commands must always have the SLI bit set to avoid suppression of command chaining.

Program Check, Protection Check

These bits are set in accordance with standard channel practice.

Channel Control Check

This bit is set if a parity or trap check occurs in the adapter.

Sense Information

The line attachment transfers up to 24 bytes of sense data in response to a 'sense' command.

Sense byte 0 is the standard sense byte followed by a three byte extension field. This extension field is followed by the twenty bytes of the current SCB.

The first byte of the extension field (sense byte 1) is a check byte. Sense bytes 2 and 3 are reserved.

The check byte shows why a bit is set in sense byte 0. The check code has two purposes:

- 1. To notify the access method of different classes of errors, such as errors with or without the possibility of a retry.
- 2. To act as entry to the maintenance documentation.

Sense Bytes 0 and 1

Descriptions of the bits in sense byte 0 follow. See the last part of each bit description for the meanings of the associated check codes in sense byte 1.

<u>Bit</u>	Meaning	Log
0	Command reject	No
1	Intervention required	No
2	Bus out check (not set by CA)	
3	Equipment check	Yes
4	Data check	No
5	Overrun	Yes
6	Lost data	Yes
7	Timeout complete	No

Command Reject (bit 0)

This bit is set during command initiation if an invalid command is issued to a CA line, or if the state of the line does not allow the command to be executed. The command is terminated immediately with unit check set when the CSW is stored. No logging is performed. Sense byte 1 shows additional information as follows: Hex

- 04 The 'dial' command is issued and there is no autocall adapter for a switched network associated with the addressed line.
- 05 The 'data terminal ready' (DTR) signal is on when a 'dial' command is initiated, i.e. the addressed line is not in the disabled state when the 'dial' command is initiated.
- 06 DTR is off at command initiation for a read type command or write type command on an SDLC line, i.e. the line is not enabled.
- 07 DTR is off during chaining to a read or write type command.
- 08 Eight immediate type commands ('no-op', 'sense', 'sense 1/0', 'set mode', 'sense SCB', or 'control SCB') are executed consecutively.
- 09 The command is not a valid SDLC-CA command.
- 10 The line direction is outbound during a read type operation.
- 11 The line direction is inbound during a write type operation.
- 12 The first two bytes of the data area of a 'read PIU' or 'write PIU' operation cross a page boundary.
- 13 Seven outstanding I-frames in a "write PIU' operation have not been acknowledged.
- 14 In a 'read PIU' or 'write PIU' command the offset exceeds the CCW length count, or in a 'write PIU'

command the frame length field exceeds the CCW length count and data spanning is not specified.

- 15 No current SCB is defined for a 'read PlU', write PlU' or 'poll' operation.
- 16 The CCW length count is less than 12 in a 'control SCB' command, or less than 20 in a 'sense SCB' command, or not between 12 and 2K in an 'autopoll' command.
- 17 The data address is not on a fullword boundary in an 'autopoll', 'control SCB', or 'sense SCB' command.
- 18 More than 127 commands have been flushed consecutively.

Intervention Required (bit 1)

A detected intervention required condition normally causes immediate termination of the current operation. The channel end, device end, and unit check bits are set when the CSW is stored at the time of the 1/0 interruption. No logging is performed. The intervention required bit is set for errors in external modems (or in the channel service unit in case of the Digital Data Service attachment, or in the digital service unit in case of the X21 attachment). For errors in integrated modems, equipment check is raised. Sense byte 1 shows additional information as follows: <u>Hex</u>

- 20 'Data set ready' (DSR) is off during the execution of a read type or write type command. The line is disabled.
- 21 DSR is off at the initiation of a read type or write type command. The line is disabled.
- 22 'Clear to send' (CTS) is not activated by the modem as a response to 'RTS on' before the 3-second timeout ends either in the initiation of a write type command or an 'autopoll' 'read' to 'autopoll' 'write' turnaround. The line is disabled.
- 23 CTS is off during the execution of a write type command or in the 'autopoll' 'write' state (not 'permanent request to send'). The line is disabled.
- 24 The loss of the external clock signal (modem clock) is detected during the execution of a write type command. The line is disabled.
- 25 In 'switched request to send' operation (not 'permanent request to send') CTS is not de-activated as a response to 'RTS off' by the modem before the 1-second timeout expires either at the termination of a 'write'/'write PIU' command or at 'autopoll' 'write' to 'read' turnaround. The line is disabled.
- 29 The ACU's 'data line occupied' signal is on when a 'dial' command is initiated.
- 2A The ACU's power indicator signal is off at 'dial' command initiation or execution.
- 2C During execution of a 'dial' command the ACU has not turned on or off 'present next digit' (PND) or turned on the 'abandon call and retry' (ACR) signal within 25 seconds in the following cases:

- 1. 'Call request' (CRQ) to the ACU is on and 'PND on' is not present.
- 2. 'Digit present' (DPR) to the ACU is on and 'PND off' is not present.
- 3. 'DPR off' to the ACU is present and 'PND on' is not presented by the ACU.
- 2D The ACU and the modem do not present 'distant station connected' (DSC) and 'data set ready' (DSR) nor ACR within 60 seconds after all dialing digits and the signal 'not digit present' have been presented to the ACU during the execution of a 'dial' command.
 2E DSR is not found on within 3 seconds after 'data
- 2E DSR is not found on within 3 seconds after 'data terminal ready' (DTR) is presented during the execution of an 'enable' command on a leased line.
 31 An 'enable' command is issued to an already enabled
- 31 An 'enable' command is issued to an already enabled line (DTR found on), but the DSR signal is not active, or DSR is on during an 'enable' operation to a switched line, and DTR is off.

This bit is set if a hardware check is detected in the CA, including integrated modems or local attachment hardware. A detected equipment check causes immediate termination of the current command, and causes channel end, device end, and unit check to be set at the time of an 1/0 interruption. Logging is performed. Sense byte 1 shows additional information as follows: Hex

- 60 An unexpected trap has occurred.
- 61 A hanging situation has occurred so that traps (basic status available) are continuously generated for a line. The line is disabled.
- 62 A machine check has been detected indicating an error on the processor bus. The line is disabled.
- 63 The loss of the internal clock signal is detected during the execution of a read type command or write type command. The line is disabled.
- 64 No valid basic status is available. The line is disabled.
- 70 DSR is off during the execution of a read type or write type command. The line is disabled.
- 71 DSR is off at the initiation of a read type or write type command. The line is disabled.
- 72 CTS is not activated by the modem in response to 'RTS on' before the 3-second timeout ends either in the initiation of a write type command or in an 'autopoll' 'read' to 'autopoll' 'write' turnaround. The line is disabled.
- 73 CTS is off during execution of a write type command or in the 'autopoll' 'write' state (not 'permanent request to send'). The line is disabled.
- 74 In 'switched request to send' operation (not 'permanent request to send'), CTS has not been de-activated by the modem in response to 'RTS off' before the 1-second timeout expires, either at the termination of a 'write'/'write PIU' command or at 'autopoll' 'write' to 'read' turnaround. The line is disabled.
- 75 RTS is down while the line is in the outbound state although 'permanent request to send' is on. The line is disabled.
- 76 DTR is off while the line is enabled. The line becomes disabled.

This bit is set in receive mode when commands are executed and frame check sequence errors or format errors occur. No logging is performed. Sense byte 1 shows additional information as follows: Hex

- 90 A frame check sequence error is detected during the execution of a 'read' command. The check applies to both primary and secondary lines.
- 91 The offset value in an SCB transferred to the line attachment is specified as 0 or 1, or any reserved fields are not zero.
- 92 Any line receives an invalid frame (too short) or an abort sequence during the execution of a 'read' command. The invalid frame check applies to both primary and secondary lines.
- 93 An SDLC sequence is invalid on a line in the inbound state with a 'read' command active.
- 95 Any reserved fields in the information provided by a 'set mode' command are not zero, or the line is specified as secondary without the secondary station address being provided.
- 96 An 'Nr out of range' is received.

Overrun (bit 5)

The overrun bit is set if the line attachment is too late to serve a request for data transfer from the associated hardware. Logging is performed. Sense byte 1 shows additional information as follows: Hex

- A0 An overrun condition has been detected during the execution of a read type command.
- A1 An underrun condition has been detected during the execution of a write type command. Intervention required is set together with overrun.
- A2 Data chaining is specified in a 'read PIU' or 'sense SCB' command.
- A3 Data chaining is specified in a 'write PIU', 'control SCB', or 'autopoll' command.

Lost Data (bit 6)

This bit is set during the execution of commands when the line attachment has exhausted its buffer space with received data before a read type command is active. Logging is performed only on 'dial' commands. Sense byte 1 shows additional information as follows: <u>Hex</u>

- C0 At least one full character has been received and lost because no inbound command was active. Unit check is not set if:
 - 1. Some inbound data has already been accepted in the current channel program, or
 - 2. For a secondary station, no channel program is active.
- C1 The length count is decremented to zero without a flag for a read command being received.
- C2 'Present next digit' (PND) is on during the initiation of a 'dial' command.
- C4 'Distant station connected' (DSC) is on during the initiation of a 'dial' command.
- C5 The 'data set ready' or 'distant station connect' signal is prematurely active during a 'dial' operation. The command is terminated immediately.
- C7 A 'halt I/O' instruction is issued while a 'read' command is active. The command is terminated immediately.

Timeout Complete (bit 7)

This bit is set when an unexpected timeout occurs. No logging is performed. Sense byte 1 shows additional information as follows: Hex

E6 The 'abandon call and retry' (ACR) signal of the ACU becomes active during the initiation of a 'dial' command.

- E7 The ACR signal becomes active during the execution of a 'dial' command.
- EC 'Data set ready' (DSR) is not de-activated by the data set within one second (modems with DTR procedure) or 25 seconds (modems with 'connect data set to line' procedure) after the signal 'data terminal ready' has been dropped during the execution of a 'disable' command (valid only for switched networks).
- F0 A nonproductive receive timeout occurs while a read type command is active. In a primary station no leading flag is received after the line has turned to inbound. The line is not idling. In a secondary station no leading flag has been received after the line has turned to inbound. The line is either receiving garbage or is idling. See 'Description of Timeouts' at the end of this chapter.
- F1 An idle timeout occurs on a primary station when no current SCB exists or a 'read' command is active. No frame has been received after the line has turned to inbound and the line is idling.
- F2 A fill character timeout occurs. A write type command is outstanding after a frame has been transmitted with the P/F bit at zero.
- F3 Too many SCBs have skip specified in the control flag during an 'autopoll' operation.

Sense Bytes 2 and 3

These two bytes are zero.

Sense Bytes 4-23

These bytes are the twenty bytes of the SCB. See 'SCB Format' and 'Sense SCB' in this chapter.

Soft Errors and Recovery

There is another group of errors, ('soft errors'), which do not cause an abnormal termination of the channel program. Although soft errors are communicated to the access method they are not given special recovery action. A soft error is indicated in bit 0 (SOFTERR) of the first exception flag byte of the SCB (EXFLAGS1). The second exception flag byte (EXFLAGS2) specifies which kind of soft error has been detected.

If no SCB exists, or if an SCB exists but a 'read' command is active when an exceptional condition is detected, a unit check is generated rather than an exception indication. (There are two reasons for a nonexisting SCB: either a channel program is running but no 'control SCB' or 'autopoll' command has been issued, or no channel program is active). If a soft error is indicated in the exception flag bytes, the counter fields in the SCB have not been updated for the frame in which the error has been detected.

If several soft errors are detected during a channel program, only the first error is reported.

The soft error conditions are:

Second Exception Flag	Meaning	Action
01	An idle timeout, followed by 15 marks, is detected when an 'autopoll' command is active.	 If primary, turn line to outbound. Set status modifier (simulate nonexpected reply). Flush channel program.
02	Same as O1, but for 'read PIU' or 'sense SCB'.	- lf primary, turn line to out- bound. - Flush channel program.
04	Non productive receive timeout when an 'autopoll' command was active or the received frame length exceeds 2**16 in case of a 'read PIU' (11 overflow).	Same as O1.
05	Same as O4, but with 'read PIU' or'sense SCB'. Note that a nonproductive receive timeout is also reported in case of length count overflow for an I-frame received by 'read PIU'.	Same as O2.
06	NS out of sequence.	Same as 02.
08	An abort sequence, followed by 15 marks, or an invalid SDLC sequence has been received.	Same as 02. If an 'autopoll' command is active, set status modifier before start of flushing, that is, this error is con- sidered an unexpected reply.

OB	Address mismatch detected in primary station.	Same as 08.
00	Frame received too short, (less than 4 bytes).	 Synchronize and flush. If an 'autopoll' command is active, set status modifier before flushing, that is, this error is considered an unexpected reply.
OE	FCS bad on 'autopoll' response.	Same as OC.
OF	FCS bad (except for 'autopoll' response).	Same as OC.
11	Overrun	Synchronize and flush.
12	Not enough buffer space. a.ln a data spanning situation, no subsequent 'read PIU' has been found in the channel program to accommodate the rest of the frame, or no buffer was provided at all, or	 Store the total length of the incompletely stored frame at the beginning of the first buffer area as usual. Synchronize and flush.
	b. A frame with an I-field is received in response to a 'sense SCB' command.	
81	Underrun	Abort and flush. If secondary, turn line to inbound.
82	Frames acknowledged fewer than frames sent.	- Synchronize and flush.

CCW Flags

Chaining Flags

Command chaining is executed according to standard channel practice.

Data chaining is performed as soon as the length count field is decremented to zero and the chain data flag (CCW bit 32) is found on. 'Read PIU' and 'write PIU' commands cause an overrun if chain data is specified. A test is made for command chaining in the command terminating routine and the request is queued for later execution.

Channel Indirect Data Addressing (IDA) Flag

The IDA flag (CSW bit 37) is valid only in System /370 mode. The data address is exchanged if the IDA bit is found on when the CCW is fetched during: • Command initiation • Chaining of commands The data address is also exchanged during data transfer operations when the CA detects a page boundary crossing, and the IDA flag is set in the current CCW. Bits 0-7 in the IDA word must contain all zeros, otherwise program check is set. The data address in the CCW must be on a fullword boundary, otherwise program check is set.

Program Controlled Interrupt

A program controlled interrupt is enqueued during command initiation or during chaining.

Suppress Length Indication Flag and Skip Flag

The suppress length indication flag (CCW bit 34) and the skip flag (CCW bit 35) are handled according to standard channel practice.

Termination of Operations

Termination at Initiation of Operation

When the CA detects an unusual condition during the initiation of an operation, the command is rejected. Condition code 1 is set, and the status portion of the CSW is stored. No interruption condition is generated.

When an unusual condition causes a command to be rejected during command chaining, an interruption is generated, and the chain of commands is broken.

Termination of Immediate Operations

If no command chain is specified with an immediate operation such as no-op, the channel end and device end condition is brought to the attention of the program by storing the CSW, and by setting the condition code to 1.

If command chaining is specified with an immediate operation such as no-op, condition code 0 is set when the immediate command is initiated. The subsequent CCWs are handled normally, and the channel end/device end condition for the last CCW generates an interruption.

Termination of Command Execution

- - -

At command termination, channel end and device end are signaled in the CSW, and an interruption request is generated.

Any unusual condition causes command chaining to be suppressed and a terminating condition to be generated. The unusual condition is signaled in the channel status or unit status portion of the CSW, together with channel end and device end. An interruption request is generated.

Interruptions

There is a common interruption queue for PCIs and primary interruptions. Secondary interruptions are handled differently, as explained below.

Enqueuing a primary early interruption results in an entry in a common interruption queue. The subchannel status is also updated to reflect the pending interruption. A common interruption handler in the system clears the pending interruption condition.

In the case of secondary interruptions, the system interruption handler does not automatically clear the condition, but control is returned to the CA to store the appropriate status.

The following table shows the results of initiating an 1/0instruction to the CA when interruption conditions are

Pending Interrupt 	Start /0 SIOF			
In addressed	CC2	CC1*	CCO	CC1*
subchanne1				

pending for command termination. * The interruption condition is cleared and the CSW is stored. CCO = CSW is not stored CC1 = CSW is stored

CC2 = subchannel busy

A PCI and an interruption for command termination pending for a subchannel are indicated as only one interruption. A 'test 1/0' or 'clear 1/0' instruction clears both interruptions at the same time.

Ending Condition Classification

The following is a description of all possible ending conditions, classified by error severity. For a more detailed list of error conditions see 'Sense information' and 'Soft Errors and Recovery'.

- <u>Group</u> Ending Condition <u>Indications</u> 1 Normal Ending. CSW: CE, DE
 - 2 Soft Error. CSW: CE, DE This group covers retriable errors that occur during high level CCW operation. A bit is set in the SCB exception byte. Unit check is not presented.
 - 3 Retriable Hard Error. CSW: CE, DE, UC This group covers retriable errors on low level CCWs. It is composed of nearly all unit checks with data check, overrun, lost data and timeout, and has only a few exceptions. For example, unit checks with vertical redundancy check and data check in the SCB (hex 91 in sense byte 1) are not included in this group, nor are unit checks for lost data which refer to 'dial'.
 - 4 Intervention Required. CSW: CE, DE, UC This group covers non-retriable errors related to system parts external to the processor. It is composed of all unit checks with intervention required, plus (in case of an external modem) those unit checks with lost data which refer to 'dial'.
 - 5 Equipment Check. This group covers CA hardware (including integrated modems) or microcode errors. It is composed of all unit checks with equipment check, plus those units with lost data which refer to 'dial'. CSW: CE, DE, UC or channel status
 - 6 Program Error. CSW: CE, DE, UC This group covers channel programming errors. or channel status These situations should not occur.

Independent of the semantics of each command, the CA has to maintain synchronization between line activities and the execution of the channel program.

Line Direction Transitions

The line goes from outbound to inbound in the following situations:

- A P/F bit has been sent.
- In a secondary station, a fill character timeout has occurred.
- In a secondary station, an abort sequence has been sent because of underrun.
- In a secondary station, an 'enable' command has been given.

The line goes from inbound to outbound in the following situations:

- A P/F bit has been received.
- In a primary station, nothing has been received and either idle detection (15 marks received after idle timeout) or nonproductive receive timeout has occurred.
- In a primary station, an 'enable' command has been
 - given.
- In a primary station, an abort sequence has been received.

Note: On a line set to outbound, continuous flags are sent out.

Channel Program Synchronization Rules

As a rule, if no channel program is active, the line direction is normally outbound.

As an exception, the line direction is inbound in the following cases:

- A P/F bit has been transmitted with the last line-affecting command of the preceding channel program. Note, however, that, for a primary station, the line will be turned back to outbound after idle timeout or nonproductive receive timeout.
- For secondary stations only:
- a. A fill character timeout has occurred.
- b. An abort sequence has been sent out because of underrun.
- c. A nonproductive receive timeout has occurred.
- d. A frame with no matching address has been received. Such a frame is ignored. A P/F bit causes no line turnaround.
- e. Data has been received but no channel program was active. The station remains at inbound even if the P/F bit is set. A unit check, with the lost data bit set, is not raised.

A channel program is never complete until the line status is as described in the preceding rules. Channel program termination is suspended if necessary. The only time when synchronization is not established is after the rejection of a command, when the line direction is undetermined until the next timeout establishes a unique situation. The same is true when a program check or protection check occurs. These checks, when detected, cause immediate program termination.

Description of Timeouts

Nonproductive Receive Timeout

Line direction:

Inbound.

Reason:

 In a primary station no leading flag is received after the line has been turned to inbound. The line is not idling (otherwise, an idle timeout would have been detected), that is, garbage only has been received.

- In a secondary station no leading flag is received after the line has been turned to inbound. The line is either receiving garbage or is idling (because no idle timeout has been defined for the secondary station).
- In a primary or secondary station at least one leading flag has been received after the line has been turned to inbound, but no trailing flag has been received.
- In a primary or secondary station a 'read PIU' is active and the accumulated frame length of an I-frame exceeds 2**16.
- When turning the line to inbound.
- After a valid frame has been received.

• Generate a soft error or unit check.

- For a primary station, turn the line to outbound
- If no channel program is active, keep the generated unit check.
- If a channel program is active, raise a unit check and terminate the channel program.

Started:

Actions:

Idle Detect Timeout

Line direction:	Inbound
Reason:	In primary stations only, no frame has been received and the line is idle (no garbage). The idle timeout can have a time value of O if an abort sequence has been received.
Started: Actions:	 When the line is turned to inbound. If following this timeout 15 marks are not received, no action is needed (a nonproductive receive timeout will come up later). If no command is active, no action is needed.
	 If a command is active (it can only be a 'read' type) and an SCB exists: Set the soft error indication into the SCB. Flush the channel program and terminate it (no synchronization).
	 If a command is active and no SCB exists: Generate a unit check. Raise the generated unit check and terminate the channel program (without flushing).
Fill Character Timeout Line	• Turn the line to outbound.

direction:	Outbound
Reason:	A write type command is outstanding; that is, too many continuous flags have been transmitted after line turnaround or after transmitting a frame with the P/F bit at zero. This is a programming error.
Started:	Whenever the CA starts transmitting continuous flags, that is, after turning the line to outbound, and after transmitting a frame with the P/F bit at zero.
Actions:	 Generate a unit check and raise at the next opportunity (that is at the first CCW of the next channel program). For a secondary station, turn the line to inbound.

Unit Check and Soft Error Handling

In addition to the synchronization of line activities with the channel program, there is also a rule governing the synchronization of error situations with the channel program and line activities.

The general rule is that if a unit check comes up, it is raised and the channel program is completed as soon as possible. This can be done if the following three conditions are fulfilled: a command is active, no prior sense information is pending, and the line direction is correct.

Dynamic Trace Feature

The dynamic trace standard feature allows the CA to obtain trace data for a communication line using any line protocol (SDLC, BSC, or IBM Terminal Control Type 1). This trace data shows line information at the end of each CA microcode trap, that is, the trap type, the channel command active, the data byte received or transmitted and the error sense information.

The trace data is collected in an internal buffer which holds 2560 trace entries. The buffer wraps around when full. The trace data can be dynamically transferred to customer storage. When the dynamic trace has been stopped, the last 2560 trace entries may be displayed on the 4331 operating console by a maintenance selection option. The trace feature is supported by a trace program which runs under VSE/Advanced Functions as described in VSE/Advanced Functions Serviceability Aids and Debugging Procedures, SC33-6099.

The 'Dynamic Trace' feature has the following characteristics:

- One subchannel I/O address hex '03B' is reserved exclusively for this feature.
- The use of the dynamic trace excludes the use of the
- other CA inline tests (ILTs) and the DASD adapter ILTs.
- Before the dynamic trace feature may be activated by a channel program the feature must have been invoked from the 4331 operator console as one of the CA inline tests (maintenance selection '9 - 64')
- The trace may be started for one line from the operators console (maintenance selection 9 - 64xx) or by a channel program for the trace subchannel with a 'set trace options' command (x'01').

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- The trace data is collected in an internal buffer of 10k bytes which holds up to 2560 trace entries.
- The trace data may be dynamically transferred to the customer storage by a 'dynamic trace dump' command (hex '42') or displayed on the operators console after the trace has been stopped using the CA display trace data option (maintenance selection D C).
- The trace may be stopped either from the operator console (maintenance selection '9 - P') or by the 'write break' (hex '0D') command or the 'set trace options' (hex '01') command. If the 'dynamic trace dump' command is being executed the operations may be stopped by issuing a 'halt 1/0', 'halt device', or 'clear 1/0' instruction.

Trace Analysis

The trace analysis is described in <u>VSE</u> <u>Advanced Functions</u> Serviceability <u>Aids and Debugging</u> Procedures, SC33-6099.

Command Code

Trace Channel Commands

Hex	CCW Bits 0 1 2 3 4 5 6 7	Command
04 06 09 0D 27 2F	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	<pre>* Disable (executed as no-op)</pre>
		* Accepted for compatibility reasons.
		<pre>** "Not supported" means for compatibility reasons unit check, together with equipmen</pre>

command is issued.

check in sense byte 0, are set when the

Set Trace Options

The 'set trace options' command is used to specify dynamic trace options.

The command will only be accepted if the dynamic trace has been invoked through CA inline test selection. Otherwise the command is terminated with unit check. Equipment check is indicated in sense byte 0.

Four bytes are read from the storage location specified in bits 8 to 31 of the CCW. If an invalid trace option is specified, the command ends with unit check and equipment check indicated.

Valid options in hexadecimal:

4010xx..Start trace for line xx4011xx..Stop trace for line xx

Byte 0 must be always Hex '40' (function byte)

Byte 1 must be either hex '10' or hex '11' (trace option) The option byte is invalid if:

- the byte is hex '10' and the trace is already started for specified line.

Byte 2 contains the address of the CA line to be traced. The specified address must belong to an installed CA line (range hex '30' to hex '37').

Byte 3 can be any value.

Sense

The 'sense' command causes one byte of sense information to be transferred to processor storage. Only two bits are used:

Bit 0 = command reject Bit 3 = equipment check

The reasons for setting these sense bits are specified in the description of the other trace channel commands.

Write Break

The 'write break' command can be used instead of the 'set trace option' command (see description above) to stop the dynamic trace. No data is transferred by this command. If the dynamic trace is not active the command is handled as no-op. Programming Note: This command cannot be used to stop the 'dynamic trace dump' command, because the trace subchannel is busy until the command is terminated.

Dynamic Trace Dump

The 'dynamic trace dump' command transfers the trace data to processor storage in segments of four bytes.

The command is only accepted if:

- 1. The data address specified in bits 8....31 of the CCW starts on a fullword boundary and the length count is a multiple of four. Otherwise the command is terminated with unit check. Command reject indicated in sense byte 1.
- 2. The dynamic trace is invoked. Otherwise the command will be terminated with unit check. Equipment check is indicated in sense byte 1.
- 3. The dynamic trace is active for one CA line. Otherwise the command is terminated with unit exception indicated.
- 4. Data chaining is not specified in the CCW, that is, the flag is off. Otherwise the command is terminated with unit check and command reject indicated in sense byte 0.

Trace entries if available in the dynamic trace area, are transferred to storage until the length count is exhausted. If the trace data runs out before the count is exhausted, the command remains active and resumes operation when the next trace entry is available, that is, when a new trace event occurs.

If a trace area wraparound occurs before the command is started or while the command is active (trace entries not transferred to storage or overwritten by new trace data), the current trace entry byte one is set to hex 'FF' and all other trace entries are lost. The command resumes operation by transferring the trace entry from the last trace event.

The command may be stopped during execution by a 'halt 1/0', 'halt device', or 'clear 1/0' instruction or by an operator command (ILT maintenance selection 9, parameter P). In this case the command is terminated with channel end, device end, and unit exception indicated in the channel status word.

The 'sense 1/0' operation transfers seven bytes to processor storage as follows:

Byte 0: always hex 'FF' Byte 1: CPU Identification 1 Byte 2: CPU Identification 2 Byte 3: CPU Identification 3 Byte 4: hex 'CA' for communication adapter Byte 5: hex '00' dynamic trace not invoked hex '01' dynamic trace invoked Byte 6: always hex '00'

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Chapter 8. Model-Dependent Information

This section describes the implementation of the 4331 Processor in design areas where the principles of operation manuals permit a choice. The information is grouped alphabetically under 'Channels', 'Controls', 'Machine Check Handling', and 'Storage'.

Channels

Implementation

There are two timeouts for the standard interface, one to detect lack of activity on the interface (45 secs), and the other to detect lack of progress in initial selection (approximately 0.8 sec). The 45-second timeout can elapse when an operator mounts an unwritten tape on a drive. This timeout can also elapse when a tape is searched but the file is not closed by a tape mark, thus causing an endless search. A console message indicates which unit caused the timeout to elapse. Both the 45-sec and the 0.8 sec timeouts cause a selective reset in the channel, with interface control check indicated in the CSW.

During data chaining on input, CCWs are prefetched for 3310 and 3370 files only. One CCW is prefetched, both for normal processing and for initial program loading.

Limited Channel Logout

D:+

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DIL	Meaning
0	Logout stored
1-3	Storage control unit ID
4-7	Detect field
8-12	Source field
13-15	Unassigned
16-23	Field validity flags
24-25	Termination code
26-27	Unassigned
28	Error alert
29-31	Sequence code

In the 4331 Processor, the limited channel logout bits are set under the following conditions:

<u>Bit 0</u>. This logout stored bit is reset (zero) when a limited channel logout is stored due to a channel data check, a channel control check, or an interface control check. The operating system sets this bit to 1 to ensure indication of each incident.

Bits 1-3. These three bits are permanently at zero.

<u>Bits</u> $\frac{4-7}{100}$. The detect field bits are permanently set to 0100, thus identifying the channel as the unit which detected the error.

<u>Bits</u> $\frac{8-12}{2}$. The five source field bits are permanently zero.

<u>Bits</u> <u>16-23</u>. The field validity flags, when set, indicate that the field contents are logically valid and may be used for recovery purposes. The following bits are set:

- Bit Meaning
- 16-18 Unassigned
 - 19 Sequence code valid
 - 20 Unit status valid
 - 21 Command address and key valid
 - 22 Channel address valid (see note)
 - 23 Device address valid

Note: If the channel address cannot be established, the $\overline{4331}$ presents a machine-check interruption showing system damage instead of a limited channel logout.

The operating system is recommended to cancel all tasks with queued I/O requests on any channel for which a limited logout with an invalid device address is stored. Bits 19-21 should only be tested when the associated field is required for error recovery.

Bits 24-25. These termination code bits are coded as follows:

Bit Setting Meaning

- 00 Interface disconnect
- 01 Stop, stack,
- or normal termination
- 10 Selective reset
- 11 Not used

Bit 28. This error alert bit is set only by control units capable of signaling error alert to the channel. The alert indicates to the operating system that the error originated in the control unit rather than in the channel. If the error recurs, the control unit should be removed from the configuration, or ignored.

<u>Bits 29-31</u>. The sequence code shows how far the operation has progressed at the time of error.

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<u>Bit</u> Setting	Meaning
000	Channel-detected error during 'test I/O' or 'clear I/O' instruction.
001	Command sent out but no device status was received (typical for initial selection).
010	Status received but no data transferred.
011	At least one byte of data transferred.
100	Command code in current CCW either not yet sent or sent but not accepted by the device.
101	Command accepted but data transfer is unpredictable (discontinued).

The sequence code should be used by the device error recovery management programs.

Channel Logout Recording

The 4331 Processor does not request recording on behalf of the operating system of anything but unit-check records. Machine-independent logs are, however, recorded.

Partial Results

Conditions in which channels can observe partial results do not occur because all processing takes place in one processor, controlled by an hierarchical trap system that excludes overlapping.

Controls

Clock Resolutions

CPU Timer and Clock Comparator

The CPU timer and the clock comparator have a 16usec resolution. The accuracy of the oscillator is $5x10^{-5}$.

Interval Timer

The interval timer has a resolution of 10 msec. The timer is emulated at storage location 80 when the system is set to System/370 mode. The need to decrement the interval timer is checked before each machine instruction is executed. Any missing decrement is provided at the following update by an accumulating register.

Time-of-Day Clock

The resolution of the time-of-day clock is 16 usec. This means that bit position 47 is modified by one every 16 usec. The accuracy of the oscillator is 5×10^{-5} .

Instructions

'Store CPU ID' Instruction

Bits 0-7, representing the version code, are zeros for Model Group 1, and 02 for Model Group 2. Bits 8-31 contain six digits selected from the serial number stamped on the frame of the machine. Of these, the three low-order digits are compared, for security reasons, with a wired three-digit number. Bits 32-47 contain the model number.

Manual Operations

Storage Address Compare

In address stop mode the 4331 stops at the completion of the instruction during which the address match was detected. The main criterion for recognizing an address match is an equal comparison over the 24 bits of the address. The stop condition is recognized when the referenced data is fetched from or stored into processor storage. The storage operation is not affected.

In the 4331 Model Group I there is an exception to this byte-precise rule. When the function is specified as "stop", and "any", "data store", or "1/0 data" has been entered, the match criterion is the storage word designated by the compare address, the two low order bits of the The 1/0 mode address being ignored in the comparison. includes all references to CCWs, the CSW, and the CAW. When using the 1/0 stop mode as diagnostic aid for outbound 1/0operations, the user should note that the integrated adapters and channels prefetch data on outbound operations to a varying degree. For this reason, an address compare stop may be indicated when the data is fetched from processor storage, independent of the actual transfer of such data to the 1/0 device. From a minimum of eight (Model 1) to a maximum of 256 (Model 2) bytes can be prefetched by the data mover. The I/O stop is always recognized when the designated word (Model 1) or byte (Model 2) is fetched from storage. The I/O compare mode is useful on inbound operations since it can show that an 1/0 operation alters a specific storage location. The processor enters the stopped state at the completion of the instruction during which the stop condition was recognized, just as if the stop key had been pressed.

In instruction count mode, the processor stops at the completion of the instruction that caused the address match.

When the location of a branch instruction is the target address, the stop occurs at the completion of the branch instruction, that is, after the branch (if any) is taken. When the start key is subsequently pressed, operations resume at the next sequential instruction if no branch was taken, or at the branch address if the branch was taken.

Note: When the location of the instruction that immediately follows the branch instruction is the address compare target, two stops (Model 1 only) are provided for the seven most commonly used branch instructions. The first stop occurs after the branch is taken (provided the instruction branches). The second stop occurs at the actual address compare target, that is, at the instruction that would have been executed next if the branch had not been taken. The stop occurs at the completion of that instruction. On Model 1 the following branch instructions have two stops:

BAL BALR BCR BXH BXLE

BCT BCTR

On Model 2 the instructions listed have only one stop.

Specifying Storage Addresses

In ECPS:VSE mode all target addresses specified for address compare operations are virtual addresses within the range of 16 megabytes. In System/370 Mode the specified addresses are processor storage addresses (see "Storage" in Chapter 1 for definition.) If only the virtual address is known, the corresponding processor storage address can be obtained by the manual operation Display/Alter Main Storage Real.

Power-On State

The power-on state is reached in the 4331 when support processor 1, the processor, and the channel adapters are under power, have completed their reset routines, and the loading of microcode for support processor 1 has been carried out. If a power-up failure occurs in an externally-connected control unit, the system will still reach the power-on state, but the POWER COMPLETE lamp will be off and the POWER IN PROCESS lamp will be on.

Program Event Recording

For emulated instructions, all events which have the corresponding mask bit set are indicated, whether the event occurred or not.

Program event recording (PER) reduces the instruction execution time by a factor of up to 20, depending on the type of event handled. Processing speeds are reduced whenever the PER bit in the PSW is set, even if no event is specified.

Machine Check Handling

Control Register 14

The 4331 uses bit 6 (external damage report mask) and bit 7 (warning mask). The 4331 does <u>not</u> report recovery and degradation, that is, bits 4 and 5 are not used.
Time-Outs Leading to Machine Checks

None.

Time-Outs Leading to Check-Stop

Two time-outs supervise communication between the processor and support processor 1. One is a 1-second timeout which monitors the data transfer. The other is a 3-second timeout which monitors the logical response from a micro routine. To avoid deadlocks, both timeouts cause a check-stop.

The byte and block multiplexer channels have two timeouts which lead to an interface control check when they elapse (see "Implementation" under "Channels" in this chapter).

Check Stop State

The 4331 enters the check-stop state when:

- Any exigent machine-check condition arises while the machine-check interruption mask in the current PSW disables machine-check interruptions.
- 2. Any machine-check condition arises while hard stop mode is set.
- 3. Any machine-check conditions arise while the machine-check handler is processing a machine-check interruption.
- 4. The communication between support processor 1 and the processing unit is hung up because a timeout has elapsed.
- 5. The microcode cannot return to (or continue at) a predetermined point. For example, some routines store a return address in a reserved area in processor storage. If a protection check occurs when attempting to fetch the saved return address, the check-stop state is entered. The same happens if the microcode cannot leave the current trap level.
- 6. An uncorrectable storage error occurs.
- 7. A key storage error occurs.

Note: If the system has become inactive and there is no response to the stop key, the processor may be in a PSW loop. In this situation, the only manual operation

possible is a reset (a program reset is recommended). Any attempt to display the PSW or other facility brings the message "CPU stop not possible" to the screen.

A program or clear reset must be performed to recover from the check-stop state.

Machine Check Interruption Code

<u>Bit</u>	Meaning
0	System damage
1	Instruction processing damage
2	System recovery (not used)
3	Interval timer damage
4	Timing facilities damage
2 3 4 5 6 7 8	External damage (not used)
6	(Not assigned)
7	Degradation (not used)
	Warning
9-14	(Not assigned)
15	Delayed
16	Storage error (not used)
17	(Not assigned)
18	Key error (not used)
19	(Not assigned)
20	'PSW-EMWP ^T validity
21	PSW mask and key validity
22	Program mask and condition code validity
23 24	Instruction address validity
	Failing storage address validity (not used)
25-26	
27 28	Floating point register validity General registers valid
29	Control registers valid
30	(Not assigned)
31	Storage logical valid
	(Not assigned)
46	CPU timer valid
47	Clock comparator valid
48-63	

Some of the machine check interruption code bits described in the Principles of Operation manuals are not needed in the 4331 Processor. The bits that apply are described in the following text.

<u>Bit 0</u>. The system damage bit is set with the aid of support processor 1 when an internal error cannot be isolated to a less severe indication. For example, the bit is set when a check occurs during a switch between trap

levels in the 4331. At this time the continuation address and other data is unpredictable. System damage is also set if a storage error occurs when another instruction step has been started, and the instruction which initiated the store cycle is no longer known.

The operating system issues a message advising the operator to restart by IPL, or it initiates a hard-wait state if no message can be issued. The instruction address in the machine-check old PSW is invalid when system damage is indicated.

<u>Bit 1</u>. The instruction processing damage bit is set when an internal error can be clearly attributed to the processing of a specific instruction. Since the error may arise during various steps of the processing, the instruction address in the machine-check old PSW may not point to the next sequential instruction. This unpredictability occurs, however, only when the instruction address register (IAR) or its access mechanism is damaged. The instruction address is then marked invalid.

For an invalid instruction address, the operating system should cancel the affected task. For an invalid instruction address, the operating system should initiate a hard-wait state.

<u>Bit 3</u>. The interval timer damage bit is turned on (together with bit 4) when an error occurs in the timer update mechanism or the timer registers. The operating system should issue a message that time accounting is no longer valid, and continue normal processing.

Bit 4. The timing facilities damage bit is turned on (together with bit 3) when an error occurs in the timer update mechanism or the timer registers. No distinction is made between the individual timing facilities (interval timer, CPU timer, clock comparator, TOD clock). The operating system should issue a message and continue normal processing.

<u>Bit 8</u>. The warning bit is set to indicate to the operating system that the machine will shut down in about 20 seconds. The reason is either a power problem (voltage drift or failure) or support processor 1 check (console failure).

The operating system reacts by shutting down 1/0 activities, that is, either by preventing further 'start 1/0' instructions or issuing 'halt 1/0' or 'halt device' instructions. The intent is to avoid loss of 1/0 data during the shutdown. No message should be issued to the operator because the support processor 1 (which handles the messages) may be non-operational. In this case the shutdown would be disrupted.

<u>Bit 15</u>. The delayed bit is set when the machine-check interruptions are disabled at the time of occurrence (and the condition is repressible, such as warning or timer damage). The bit indicates that at least one instruction was executed after the machine check condition was recognized. The operating system can ignore the delayed bit and process the interruption as if its reporting had not been delayed.

<u>Bit 20</u>. This PSW-EMWP validity bit, when 1, indicates that the extended control (EC), machine-check mask, wait state, and problem state bits are valid in the machine-check old PSW.

Bit 21. This PSW mask and key validity bit indicates that all PSW bits, other than the interruption code, instruction length count, EMWP bits, instruction address, condition code, and program mask of the machine-check old PSW are valid.

<u>Bit 22</u>. This program mask and condition code validity bit indicates that the program mask and the condition code in the machine-check old PSW are correct.

<u>Bit 23</u>. This instruction address validity bit indicates that the instruction address in the old PSW is valid.

Note: The operating system should always check the validity of the machine-check old PSW because conditions for continuing the program are often good, as in repressible machine checks (such as timer damage). In system damage, however, the instruction address is always marked invalid.

<u>Bit 27</u>. This floating point register validity bit indicates that the floating point register save area correctly reflects the state of the floating point registers at the time of interruption.

<u>Bit</u> <u>28</u>. This general registers valid bit indicates that the contents of the general registers were correctly saved at the time of interruption.

<u>Bit 29</u>. This control registers valid bit indicates the validity of the control-register save area.

<u>Bit 31</u>. When the storage logical valid bit is set to 1, it indicates that all store operations prior to the point of interruption have been completed and all store operations beyond the point of interruption have been suppressed. The operating system should always inspect bit 31 because continuation is often promising as in the case of timer damage. Bit $\frac{46}{46}$. This CPU timer valid bit indicates that the CPU timer is not in error and the contents stored in the save area are correct for the point of interruption.

<u>Bit 47</u>. This clock comparator valid bit indicates that the clock comparator is not in error and its contents have been saved with the value correct at the time of interruption.

Machine Check Recording

The 4331 Processor does not request recording on behalf of the operating system of anything but unit check records. Machine checks usually cause a reference code to be generated to indicate repair action to the service representation.

Storage

Reference and Change Recording

Reference and change recording is, without exception, as described in the principles of operation manuals. References to storage for display on the operator console are included in the recording. Excluded are explicit changes and page operand references.

Chapter 9. Compatibility Features

Standard capabilities and optional features are available for users who wish to process on the 4331 Processors:

- System/360 or System/370 programs and data sets
- 1401/1440/1460-Series programs
- System/3 data sets

Further details of compatibility features are given in a separate publication, <u>IBM</u> <u>4331</u> <u>Processor</u>, <u>Compatibility</u> <u>Features</u>, GA33-1528. System/3 Data Import, a standard capability of the 3340 direct attachment, is briefly described at the end of this chapter.

Direct Access Storage Compatibility Feature

The following types of direct access storage compatibility, one of which can be activated at IPL, are available on the 4331:

A.

- 2311/2314/2319-3310 Direct Access Storage compatibility
- 2311/2314/2319-3370 Direct Access Storage compatibility
- 3330-3370 Direct Access Storage compabitility
- 3340-3370 Direct Access Storage compatibility

The feature consists of microcode. Channel programs originally written for count-key-data disk files (2311/2314/2319, 3330, or 3340) can be run on the 4331 using 3310 or 3370 direct access storage. The capacity of the 3310 or 3370 can thus be exploited by users transferring from System/360 and System/370. Current programs, data sets, files and access methods need not be changed.

Note: Running this feature places additional demands on the processor and the channel. System performance may be affected, particularly in batch environments when the emulated DASD is heavily loaded. Compared to the performance on physically attached 2311/2314s, the time taken on batch jobs by emulated devices is slightly longer. In the case of 3330/3340s, increases in time of 20 to 50 per cent have been observed. The microcode is loaded during IML into a reserved area in processor storage without reducing the storage available to the user. The processor storage space required for buffers and tables is not accessible to user programs.

Transfer of Files

Files are transferred by unloading the count-key-data volumes on to magnetic tape attached to the System/360 or System/370, then loading the files from this tape onto suitably initialized 3310 or 3370 volumes attached to the 4331 Processor. The transferred data sets in 2311/2314/3330/3340 format can coexist with native 3310 or 3370 data sets on the same volumes. The operating system must be able to support the transferred data sets.

DOS, DOS/VS, and OS/VS1 Compatibility

Existing DOS, DOS/VS, and OS/VS1 releases (which do not support the 3310 and 3370) can be used with the compatibility feature. In these environments, however, stand-alone programs such as the initialize disk, FBA, format emulator extent, and initialize disk CKD utilities are needed (Program Number 5747-SA2 and Device Support Facilities 5747-DS1).

Operation of Feature

The compatibility feature accepts the commands from the existing channel program and produces logically the same results on the host 3310 or 3370 as would have been produced on the count-key-data files. The commands for the original System /360 or System /370 disk files are passed to the microcode of the compatibility feature for execution. The feature fetches complete tracks from the emulated volumes into a pre-allocated buffer in processor storage and processes the tracks there with the CKD commands instead of on the 3310 or 3370.

1401/1440/1460 Compatibility Feature

Programs originally written for the 1400-series can be run on the 4311 Processor with the aid of the 1401/1440/1460 compatibility feature. The feature consists of two parts, (1) the microcode, which is automatically loaded into processor storage during IML and (2) an emulator program product, which can be loaded at any time into any user partition as part of the regular job stream.

The microcode of the compatibility feature executes the simpler but high-speed 1400-type operations except 'edit' and 'halt', and communicates with the supervisor program. More complex tasks such as I/O operations are handled by the emulator program product.

System/3 Data Import

This capability of the optional 3340 direct attachment consists of microcode and a buffer in processor storage. It allows 3340 disk files generated on a System/3 to be read into a 4331 Processor. The disk files on the 3348 data modules from the System/3 are read into the 4331 by the VSE/IBM S/3-3340 Data Import utility (5746-AM3).

For the job of importing data from the 3348 in the System/3 format, the 3340 direct attachment has a set of microroutines which read the 3340 tracks into the microcode buffer in processor storage. The tracks are then transferred to a utility buffer in processor storage and converted by the utility program to the fixed-block format usable by DOS/VSE.

Once the converted 3340 files have been written onto the direct access storage attached to the 4331 Processor, they are used as normal fixed-block files. These files can be processed, without further assistance from the System/3 Data Import microcode routines, by new programs written for DOS/VSE.

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Figure 20. 4331-1 Configuration

10-1

Notes on Figure 20:

- One 3278-2A and up to fifteen other devices (3278-2s, 3287-1s, -2s, 3262-1s, -11s, and/or 3289-4s) can be connected to the display/printer adapter. Any combination is allowed, provided no more than two line printers (3289 and/or 3262) are attached.
- 2. The DASD adapter controls up to four A-boxes.
- 3. A maximum of two A-boxes with eight spindles per string can be attached.
- 4. A maximum of four spindles per string can be attached. Each spindle has one actuator (3310) or two actuators (3370).n
- 5. A maximum of six drives (each drive has its own controller) can be attached.
- 6. A maximum of 128 nonshared subchannels, plus 16 shared subchannels with a total of 128 addresses, is available.
- 7. A maximum of 31 subchannels, four of which are sharable, is available.
- A combination of up to eight binary synchronous, start/stop, and/or synchronous data link control lines can be attached. No more than two line control procedures can be installed together.
- 9. Up to two directly attached loops and up to two data links can be connected. The directly attached loops can consist of one or two lobes. The maximum number of terminals supported is 62 per loop, but no more than 80 per 4331.



Figure 21. 4331-2 Configuration 'A'

Notes on Figure 21:

- One 3278-2A and up to fifteen other devices (3278-2s, 3287-1s, -2s, 3262-1s, and/or 3289-4s) can be connected to the display/printer adapter. Any combination is allowed, provided no more than two line printers (3289 and/or 3262) are attached.
- 2. Two DASD adapters, each controlling up to four A-boxes, are available.
- 3. A maximum of two A-boxes with eight spindles per string can be attached.
- 4. A maximum of four spindles per string can be attached. Each spindle has one actuator (3310) or two actuators (3370).
- 5. Two block multiplexer channels, each with a maximum of 128 nonshared subchannels, plus 16 shared subchannels (with a total of 128 addresses), are available.
- 6. A maximum of 36 subchannels, four of which are sharable, is available.
- 7. A combination of up to eight binary synchronous, start/stop, and/or synchronous data link control lines can be attached. No more than two line control procedures can be installed together.
- 8. Up to two directly attached loops and up to two data links can be connected. The directly attached loops can consist of one or two lobes. The maximum number of terminals supported is 62 per loop, but no more than 80 per 4331.



Figure 22. 4331-2 Configuration 'B'

Notes on Figure 22:

- One 3278-2A and up to fifteen other devices (3278-2s, 3287-1s, -2s, 3262-1s, -11s, and/or 3289-4s) can be connected to the display/printer adapter. Any combination is allowed, provided no more than two line printers (3298 and/or 3262) are attached.
- 2. Two DASD adapters, each controlling up to four A-boxes, are available.
- 3. A maximum of two A-boxes with eight spindles per string can be attached.
- 4. A maximum of four spindles per string can be attached. Each spindle has one actuator (3310) or two actuators (3370).
- 5. A maximum of six drives (each drive has its own controller) can be attached.
- 6. A maximum of 128 nonshared subchannels, plus 16 shared subchannels (with a total of 128 addresses), is available.
- 7. A maximum of 36 subchannels, four of which are sharable, is available.
- A combination of up to eight binary synchronous, start/stop, and/or synchronous data link control lines can be attached. No more than two line control procedures can be installed together.
- 9. Up to two directly attached loops and up to two data links can be connected. The directly attached loops can consist of one or two lobes. The maximum number of terminals supported is 62 per loop, but no more than 80 per 4331.



Figure 23. 4331-2 Configuration 'C'

Notes on Figure 23:

- One 3278-2A and up to fifteen other devices (3278-2s, 3287-1s, -2s, 3262-1s, -11s, and/or 3289-4s) can be connected to the display/printer adapter. Any combination is allowed, provided no more than two line printers (3289 and/or 3262) are attached.
- 2. The DASD attachment controls up to four A-boxes.
- 3. A maximum of two A-boxes with eight spindles per string can be attached.
- 4. A maximum of four spindles per string can be attached. Each spindle has one actuator (3310) or two actuators (3370).
- 5. A maximum of 128 nonshared subchannels, plus 16 shared subchannels (with a total of 128 addresses), is available.
- 6. A maximum of 36 subchannels, four of which are sharable, is available.
- 7. A combination of up to eight binary synchronous, start/stop, and/or synchronous data link control lines can be attached. No more than two line control procedures can be installed together.
- Up to two directly attached loops and up to two data links can be connected. The directly attached loops can consist of one or two lobes. The maximum number of terminals supported is 62 per loop, but no more than 80 per 4331.
- 9. A maximum of 32 nonshared subchannels plus eight shared subchannels is available.

Standard Functions

Virtual storage Dynamic address translation Channel indirect data addressing in System /370 mode Channel virtual addressing in ECPS:VSE mode System /370 universal instruction set Move inverse Clear 1/0 Byte-oriented operands Extended precision floating point arithmetic Extended control program support: VSE mode System /370 mode EC and BC mode Clock comparator CPU timer Interval timer Time-of-day clock Control registers Monitoring Program event recording PSW key handling Storage protection (store and fetch) Error checking and correction in processor storage Machine check handling Processor identification Channel identification Channel command retry on block multiplexer channel Display/printer adapter Reloadable control storage System diskette facility Maintenance subsystem / Remote support facilities

Optional Features

Byte multiplexer channel Block multiplexer channel DASD adapter for 3340/3344*, 3310, 3370 String switch capability on DASD adapter for 3340, 3370 8809 Magnetic Tape Unit adapter 5424 attachment Display-printer adapter expansion Diskette drive Control storage expansion External signal Power interface Loop adapter Communications adapter Autocall unit interface EIA/CCIT interface High-speed modem adapter Line attachment base for clocked modems Line attachment base for nonclocked modems Local attachment interface 1200 bps integrated modem: Nonswitched Nonswitched with switched network backup and auto answer

Nonswitched with switched network backup and manual answer

Switched with auto answer 1401/1440/1460 compatibility feature Direct Access Storage compatibility ECPS: VM/370 Printer-keyboard mode

*DASD adapter for 3340/3344 includes capability for System/3 data import

Prerequisite

IBM 3278 Model 2A Display Console.

Note:

Further details of 4331 configurations are given in <u>IBM 4300 Processors</u> Summary and <u>Input/Output & Data Communicati</u> <u>Configurator</u>, GA33-1523.

Exclusivities

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Feature	Allowable with	On 4331-1	On 4331-
14XX Compatibility	ECPS: VM/370	No	No
	8809 on MTU adapter	No	No
231X on BMPX	Any magnetic tape on MPX	No	Yes
	3370 on DASD adapter	No	Yes
	3340 on DASD adapter	No	Yes
	8809 on MTU adapter	No	Yes
	CA line over 9,600 bps	No	Yes*
	High-speed BMPX	Not applicable	e No
High-speed BMPX	CA line over 9,600 bps	Not applicable	e Yes*
Loop adapter	5424 MFCU adapter	No	No
String switch (3340/3370)	Direct access storage compatibility	No	No

* No exclusivity but performance may be limited (see <u>IBM</u> <u>4331</u> <u>Processor</u> <u>Channel</u> <u>Characteristics</u>, <u>GA33-1527</u>).

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Appendix A. Calculation of Available Processor Storage

To determine the amount of processor storage available to the user, proceed as follows:

- 1. Consult Table AA, determine the module numbers required to support the features, 1/0 attachments, and/or channels to be installed.
- 2. On the Table AA1, place a checkmark in the appropriate rows. Note that each module is required only once, even if it supports multiple functions of the 4331 Processor (for the exception in Module 2, see the Notes, Table AA1).
- 3. Find the sum of each of the three columns for the required microcode modules.
- 4. The total from column A must pass three tests. When the total from column A:
 - Exceeds 65,536 bytes, the control store expansion is required (Model Group 1 only).
 - Exceeds 131,072 bytes on Model Group 1 or 143,360 bytes on a Model Group 2, an invalid configuration has been selected.
 - Exceeds 262,144 bytes when added to the total from column B, an invalid configuration has been selected.
- 5. For Model Group 1 subtract the total of Column A from either 65,536 or 131,072, depending on the size of the control storage. For Model Group 2 subtract the total of Column A from 143,360.
- 6. Subtract the result of step 5 from the total of Column B
- 7. Add the result of step 6 to the total from Column C and round up to the nearest multiple of 4096.

The result of step 7 shows the amount of processor storage occupied by microcode. This amount should be subtracted from the storage size ordered to determine the amount available for the user.

TABLE AA

Function/Feature Installed	Module(s) Required
• 4331 Processor	1
 Processor Storage 	2
• 3310 attached	3, 4, 5, 6
 3370 attached to DASD adapter 	3, 4, 6, 17
• String Switch for 3370	3, 4, 6, 17, 19
 8809 tape unit attached (exclusive with 1400/1440/1460 Compatibility) 	3, 4, 6, 7
• 3340 Direct Attachment with 3344	3, 6, 8, 15
• 3340 with 3344	3, 6, 8, 15, 20
• String Switch for 3340	3, 6, 8, 15, 18
• Direct Access Storage Compatibility	3, 4, 5, 6, 9, 15
 Communications Adapter Base BSC lines installed S/S lines installed SDLC lines installed 	6, 10, 6, 10, 11 6, 10, 12 6, 10, 13
 1401/1440/1460 Compatibility (exclusive with ECPS:VM/370 and exclusive with 8809 tape unit) 	14
 ECPS:VM/370 (exclusive with 1400/1440/1460 compatibility) 	16
• High-speed block MPX (4331-2 only)	21

TABLE AA1

- A - - B - - C -

	- A -	- D -	- L -		
Module Number	Name	Control Storage (only)	Control Storage - or - Processor Storage	Processor Storage (only)	Notes
1	Basic	33792	66816	12764	
2	MSD		2007 - 100 100 - 100 100 100 - 100 100 100 - 100 100 100 100 100 100 100 100 100 100	2048	ECPS: VSE mode: one for each megabyte of virtual storage. System/370 mode: one for each megabyte of processor storage.
					ECPS: VM/370 or high-speed block MPX (4331-2 only):
					sixteen.
2	Disk/Type	6144	24320	3150	STALCOIT.
3 4 5 6 7 8	FBS	5120	12288	-	
5	3310	-	4608	11250	
6	Inline		-	10250	
7	8809	6144	9728	3060	Excl. with Module 14
8	3340	9216	13312	11600	plus
U I		JEIO		8800	per 3340 buffer
				1800	for second 3340 string
9	Disk Emu	_	27648	1300	plus
	DISK LINU		27040	4096	per 2311 buffer
				7680	per 2314 buffer
				8704	per 3340 buffer
				13312	per 3330 buffer
10	CA	8192	9216	2150	
11*	BSC	6144	9210	2150	
	0.50	TFIO			* Only two of three may
12*	S/S	5120	-	-	be selected
13*	SDLC	12288	_	1024	
14	14XX	14336	_	1800	Excl. with 7 and 16
15	3340 Emu	-	5760	200	
16	VM Assist	6656	-	-	Excl. with 14
17	3370	-	9316	10000	(2x8 devices)
18	3340 STR	2048	4096	-	(1/0 40710037
19	3370 STR	2048	4096	-	
20	3344	2010	2048	_	
21	HSC	8448	2880	400	
6 - 1					

TOTAL:

Appendix B. Instruction Timings

Processor Performance

The average processing time for each instruction is specified in microseconds in this appendix. For the complex instructions, algorithms are given to reflect the influence or variables. The formulas include only parameters directly associated with the instructions and their operands. Interference from the system is not considered. The instructions are assumed to be issued in an environment which allows immediate start of execution.

In system operation, however, three major and one minor source of interference have to be considered. These sources are (1) DLAT miss, (2) instruction buffer miss, (3) high-speed buffer miss (4331-2 only), (4) input/output interference, and (5) storage refresh. The five terms are defined in the accompanying text.

To include these factors in a calculation of instruction timings the following formula should be used.

T = A + D + B + R + H

where:

T = Total time

A = Average basic instruction time (shown in Appendix B)

D = DLAT degradation

B = Instruction buffer or high speed buffer degradation

R = Refresh interference

| = 1/0 interference

These interfering factors rareley coincide to affect the same instruction. Over a longer period, however, degradation occurs, the amount depending on the job and on the configuration.

DLAT Degradation (D)

DLAT degradation is caused by the occasional absence of the desired address from the directory look-aside table (address buffer). The 4331 models use a 32-entry, two-way associative (32x2) buffer which is operated in the 4331-1 in a split fashion with two entries of sixteen each. The same buffer is used in the 4331-2 but without splitting.

Actual work load traces showed the following number of misses per instruction depending on the system mode:

DLAT-misses per instruction

Mode	4331-1 Split by: DAT off/on	Split by:	
E-Mode or /370-BC Mode	 - 	0.0072	0.0051
/370-EC Mode	0.0122	 	0.0066

Legend: DAT = Dynamic Address Translation SV/PP = Supervisor/Problem Program State

Every miss requires address resolution, the time needed for this depending mainly on the system mode. The resolution times and the time penalties per instruction are given in the following two tables:

Mode	Time for DLAT Miss Resolution	(<u>microsec</u>)
E-Mode	6	
/370-BC	10	
/370-EC	29	

Additional Time per Instruction (microsec) Mode 4331-1 4331-2

Mode		4331-1	4331-2
E-Mode /370-BC		0.043 0.072	0.031
/370-EC ((DAT)	0.354	0.191

Instruction Buffer Misses (B)

The 4331 has a 16-byte instruction buffer which is accessed at a rate of 200 ns per halfword and thus speeds up instruction decoding and execution.

The instruction buffer size of 16 bytes is a balance between a favourable hit ratio and quick buffer reloading. The buffer is replenished in two instances : when an instruction is not or not fully contained in the buffer, or when a successful branch occurs (regardless of the branch address). The miss ratio is 0.4 and reloading requires 2.3 usec. Thus the average time of a branch instruction in the 4331-1 (3.27 usec) is increased by 0.4 x 2.3 = 0.92 usec to about 4.2 usec.

High Speed Buffer Misses (B) (4331-2 only)

The 4331 Model Group 2 has a high speed storage buffer of eight kilobytes. This buffer is accessed for instructions and data at a rate of 200 ns per halfword or fullword (depending on the format required). A buffer storage miss can produce degradation of two kinds, (1) the normal time required to load 64 bytes, and (2) the additional time required for the data saving operation which precedes the fetch operation when data has been changed.

Thus, a high speed buffer miss may cause a varying degree of degradation depending on the change activity and its distribution. Traces reveal the following "hit ratio":

Hit Ratio per buffer access: 95.52 %

The relationship between the "normal" misses versus those where "castout" (data saving) precedes the fetch operation is as follows (average in percent per instruction):

Misses per instruction 0.1237 Castouts per instruction 0.0278

The data is saved by returning it from the high speed buffer to processor storage. Saving is required when the buffer data to be replaced is flagged by the change bit. Such a store-back operation causes additional degradation. Based on a buffer-miss and castout resolution time of 2.8 usec, the average buffer degradation adds about 0.424 micro sec to the execution time of each instruction.

Refresh Degradation (R)

A small amount of interference is caused by the bit cell refresh cycles that occur in processor storage and control storage. This interference is about 1.3 % in 4331-1 and 0.5~% in the 4331-2 which corresponds to an average time penalty of 0.065~ micro sec or 0.010~ micro sec per instruction respectively.

1/0 Interference (1)

1/0 interference is caused by the processor's participation in the initiation and termination of data transfer and chaining. The 4331-1 also updates the data address and count for every 4-byte transfer, the processor is furthermore involved in the tag control for the byte multiplexer channel and the byte format data transfer of the integrated communication adapter. In the 4331-2, most of these operations are performed by the IC hardware, and therefore cause less processor interference. Since the 1/0interference depends largely on the application and configuration, it must be calculated on a 'per workload' basis. The calculation method is described in IBM 4331-1 Processor Channel Characteristics, GA33-1527, and (when available) IBM 4331-2 Processor Channel Characteristics, GA33-1535.

4331 Model Group 1

The following tables show average instruction timings in microseconds for arithmetical, logical, and input/output operations. The timings of all instructions that refer to processor storage include any time needed for adding the contents of base registers to form an address.

The instruction timings depend on a number of factors such as the timing capabilities of storage units, circuit timings, and the optimization of logic. Changes in these factors can affect the instruction timings listed in this Appendix.

Mnem	Instruction	<u> 0p</u>	Timing in Micro sec
 A	Add	 5A	2.1+0.4X+1.3W2
AD	•		14.5+2.622
ADR	.	-	11.6
AE			7.2+1.3Z2
AER	Add normalized (short)	3A	5.3
AH	Add halfword	4A	2.2+0.4X+1.4W2
AL			2.1+0.4X+1.3W2
ALR	5		0.9
AP			8.4+3.6N1 (average)
AR	· · · · ·		0.9
AU			7.2+1.3Z2
AUR			5.5
AW AWR			14.3+2.6Z2 11.6
AWR			50 (25 oprd value dependent)
BAL	Branch and link	45	1.4+0.4X
BALR			1.4 See Note
BC		-	0.8+0.4X on branching
BCR			0.8 for all branch
		-	1.4+0.4X instructions
			1.4
			2.5
BXLE	Branch on index low/equal	87 	2.5
С	Compare	1	2.1+0.4X+1.3W2
CD			13.2+2.6Z2
CDR		29	11
CDS	Compare double and swap	BB	9.9(cc=0),7.9(cc=1)
CE	Compare (short)	79	6.0+1.3Z2
CER			1 4.1 ¹
СН	•	-	2.2+0.4X+1.4W2
CL			2.1+0.4X+1.3W2
CLC			1.6+2.9 (C/4 up)+ 1.3 (Z1W1+Z2W2)
CLCL	Compare logical (long)		25(10)+(0.75+(0.33 if oprds no t on)
<u>.</u>			same byte in fullword))C1+0.35C2
CLI			
CLM	Compare logical under mask		12.0 (average)
			0.9
			100-500 (device dependent)
CP		B215 F9	
LF	Compare decimal	-	2.6+3.4((Max(N1,N2))/4 up) +1.4(Z1W1+Z2W2)
CR	Compare		0.9
CS	•		5.5(CC=0), 4.5(cc=1)
CTP	Connect page		for $cc=0: 62(+9, -4)$
	1		for $cc=1: 45(+9, -4)$
CVB	Convert to binary		22.9+0.4X+2.6Z2 if converting
	1	'	less than 7 digits, else
	1		64.2+0.4X+2.6Z2
	1		

Mnem	Instruction	10p	Timing in Micro sec
CVD	Convert to decimal	 4E	24.1+4.4Z2 (average)
			34.1+0.4X+1.3W2
-			23(cc=1), 84(cc=0)
			+ UCW scan time
DD			150(100 oprd value dependent)
			150(100 oprd value dependent)
			39+1.3Z2
	5 . 5		34 + UCW scan time
	-	3D	
		-	23.1+21.2(N1-N2)+3.6Z1W1+1.4Z2W2
	Divide	1D	32.5
ED	Edit	DE	6+3.5N1+12D+7F
			6+3.5N1+12D+7F
			33+t(Subject instruction)
			15
	·		100-600(device dependent)
			13.5
HIO	Halt /O	9E	100-600(device dependent)
10	Insert character	1	2.1+0.4X
			8.6+1.7M3(+0.4 if M3=0)
	mask		
IPB			9.5
		B20B	
ISK	linsert storage key	09	4.9 if disconnected, else 8.2
		158	 2.1+0.4X+1.3W2
			0.8+0.4X
		23	
		33	
		113	
LD	$\{1, \dots, 1, \ell, 1, \dots, N\}$		15+1.3W2
	Load (long)		4.3+0.4X+2.6Z2
LDR	lLoad (long)	68 28	4.3+0.4X+2.6Z2 1.4
LDR LE	Load (long) Load (short)	68 28 78	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2
LDR LE LER	Load (long) Load (short) Load (short)	68 28 78 38	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1
LDR LE LER LF I	Load (long) Load (short) Load (short) Load frame index	68 28 78 38 B8	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max.
LDR LE LER LF I LH	Load (long) Load (short) Load (short) Load frame index Load halfword	68 28 78 38 88 48	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2
LDR LE LER LFI LH LM	Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple	68 28 78 38 88 48 98	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R
LDR LE LER LF I LH LM LNDR	Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long)	68 28 78 38 88 48 98 21	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5
LDR LE LFI LFI LM LNDR LNER	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative (short)</pre>	68 28 78 38 88 48 98 21 31	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3
LDR LE LF! LH LM LNDR LNER LNR	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative</pre>	68 28 78 38 88 48 98 21 31 11	4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1
LDR LE LFI LH LM LNDR LNER LNR LPDR	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative Load negative Load positive (long)</pre>	68 28 78 38 88 48 98 21 31 11 20	<pre>4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1 2.8</pre>
LDR LE LFI LH LM LNDR LNER LPDR LPER	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative Load positive (long) Load positive (short)</pre>	68 28 78 38 88 48 98 21 31 11 20 30	<pre>4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1 2.8 2.5</pre>
LDR LE LFI LH LM LNDR LNER LPDR LPER LPR	<pre> Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative Load positive (long) Load positive (short) Load positive (short) Load positive</pre>	68 28 78 38 88 48 98 21 31 11 20 30 10	<pre>4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1 2.8 2.5 1.1</pre>
LDR LE LFI LH LM LNDR LNER LPDR LPER LPR	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative (short) Load negative (long) Load positive (long) Load positive (short) Load positive (short) Load positive (short)</pre>	68 28 78 38 88 48 98 21 31 11 20 30 10 82	<pre>4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1 2.8 2.5</pre>
LDR LE LFI LH LM LNDR LNER LPR LPR LPSW	<pre>Load (long) Load (short) Load (short) Load frame index Load halfword Load multiple Load negative (long) Load negative (short) Load positive (long) Load positive (short) Load positive (short) Load positive Load PSW Load</pre>	68 28 78 38 88 48 98 21 31 11 20 30 10 82 18	<pre> 4.3+0.4X+2.6Z2 1.4 2.5+0.4X+1.3Z2 1.1 14.7 min., 19.6 max. 2.2+0.4X+1.4W2 1.5+1.3(1+Z2)R 2.5 2.3 1.4 if R2 positive, else 1.1 2.8 2.5 1.1 33.4</pre>

Mnem	Instruction	<u> 0p</u>	Timing in Micro sec
	Load rounded (extended	25	6.2
LRER	operand, long result) Load rounded (long ope- rand, short result)	35	4.0
	Load and test (long)	22	1.4
	Load and test (short)	32	1.1
LTR	Load and test	12	0.8
м	Multiply		29.2+0.4X+1.3W2
MAD	Make addressable		for cc=0: 24(4)
			for cc=1: 22(4)
MC	Monitor call 		9.4 (w/o interrupt processing), 4.1 if NOP
MD	Multiply (long)		125+2.6Z2
	Multiply (long)		120
ME			33.5+1.3Z2
			31.5
MH			17.8+0.4X+1.3W2
MP			32.5+5.5n
			27.6
MUN	Make unaddressable		for cc=0: 31(4); for cc=1: 23(4)
MVC	 Move (characters)		2.2+2.9(N/4 up)+1.3Z2W2+1.9Z1W1 (average)
	Move Inverse		4.7 + 3.2N
	Move (long)		25(10)+(0.75+(0.33 if oprds not on
	l		same byte in fullword))C1+0.35C2
MV I	Move (immediate)		1.7
	Move numerics		1.2+3.7N
MVO	Move with offset		1.5+3.9N1
MVZ			1.2+3.7N
			125(30 oprd value dependent)
MXDR		27	120(30 oprd value dependent)
	lextended result)		
MXR	Multiply (extended) 	26	440(60 op value dependent)
· N	AND	154	2.1+0.4X+1.3W2
NC	AND	ID4	1.2+3.5N
NI	AND	194	2.2
NR	AND	14	0.9
	 OR	156	 2.1+0.4X+1.3W2
0 0C	OR	150 106	1.2+3.5N
01	OR	196	2.2
OR	IOR	16	0.9
PACK	Pack	F2	1.8+3.3N1+1.4W2Q2
PTLB	Purge TLB	B20D	48

RRBReset Reference bitB213 17.0RSPRetrieve status and page1830Subtract582.1+0.4+1.3W2SCKSet clockB204 36.2SCKC is clock comparatorB206 31.6SDSubtract normalized (long) [28111.6SESubtract normalized (short) [7817.2+1.3Z2SRSubtract normalized(short) [787.2+1.3Z2SERSubtract normalized(short) [385.3SHSubtract normalized(short) [385.3SHSubtract normalized(short) [3717.2+1.3W2SIOFStart 1/019000 270SLSubtract logical5F2.1+0.4X+1.3W2SLASubtract logical15F2.1+0.4X+1.3W2SLASubtract logical15F1.9 (average)SLLShift left double18F1.9 (average)SLLShift left double logical 18D3.9 (if SA32, else 3.2)SLLSubtract decimal1FB8.4+3.6N1 (average)SPKASet Psw key from addressB200A 18.6SPMSet Program Mask1043.2SPTSet CPU timerB208 35.9SRSubtract1801.3.9 if SA32, else 3.2)SRLShift right single logical 1802.7 (+0.4 if SA ≥ 32)SRDShift right double logical 1802.7 (+0.4 if SA ≥ 32)SRAShift right single 1631.8.1 (average)SRAShift right single 1631.8.1 (average)SRAShift right single 1631.9.9 if SA32, else 3.2)<	Mnem	Instruction	<u> 0p</u>	Timing in Micro sec
RSP Retrieve status and page 108 1830 	RRB	Reset Reference bit	B213	17.0
S Subtract $ 5B 2.1+0.4+1.3W2$ SCK Set clock B204 36.2 SCKC Set clock comparator B206 33.6 SD Subtract normalized (long) 6B 14.5+2.6Z2 SDR Subtract normalized(short) 7B 7.2+1.3Z2 SER Subtract normalized(short) 7B 7.2+1.3Z2 SER Subtract normalized(short) 7B 7.2+1.3Z2 SER Subtract normalized(short) 7B 7.2+1.3W2 SIG Start /0 9C00 270 SIG Start /0 fast release 9C01 270 SL Subtract logical 5F 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double 8F 7.9 (average) SLDA Shift left double 0gical 89 2.7 (+0.4 \tilde from SA2, else 3.2) SLL Shift left single logical 89 2.7 (+0.4 \tilde from SA2, else 3.2) SLL Shift left single logical 85 13.1 f disconnected, else 4.9 SPKA Set PSW key from address B20A 8.6 SPM Set page bits B5 13.1 f disconnected, else 4.9 SPKA Set PSW key from address B20A 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SRA Shift right single logical 86 2.7 (+0.4 \tilde from SA2, else 3.2) SRA Shift right single 8A 3.1 (average) SRA Shift right single 8A 3.1 (average) SRA Shift right single 8A 3.1 (average) SRA Shift right single 8A 3.1 (average) SRDA Shift right double 8E 4.3 (average) SRDA Shift right single logical 86 2.7 (+0.4 \tilde from SA2, else 3.2) SRL Shift right single logical 86 3.9 if SA<32, else 3.2) SRL Shift right single logical 86 2.7 (+0.4 \tilde from SA2) SRDA Shift right single logical 86 3.9 if SA<32, else 3.2) SRL Shift right single logical 86 1.7+0.4X+1.6W2 STCAP Store capacity counts B21F 21.5 STCAP Store clock comparator B20F 13.1 STCAP Store clock comparator B20F 13.1 STCAP Store clock comparator B207 13.1 STCAP Store clock comparator B203 50-100(channel dependent)		-		
SKK Set clock B204 36.2 SKKC Set clock comparator B206 33.6 SUB Subtract normalized (long) 2B 11.6 SE Subtract normalized(short) 7B 7.2+1.3Z2 SR Subtract normalized(short) 7B 7.2+1.3Z2 SK Subtract logical SF 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double 8F 7.9 (average) SLDA Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 2.7 (+0.4 if SA ≥ 32) SLR Subtract logical IF 0.9 F Subtract decimal FB 8.4+3.6N1 (average) SPB Set page bits B5 13.1 if disconnected, else 14.9 SPK Set PSW key from address B20A 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SR Shift right double 8E 4.3 (average) SRDA Shift right 8E SDA SA		•		
SCKC iset clock comparator = 1206 i] 3.6 SD Subtract normalized (long) 16B = 14.5+2.622 SDR Subtract normalized (short) 17B = 7.2+1.3Z2 SER Subtract normalized(short) 17B = 7.2+0.4x+1.3W2 SIO = Start 1/0 fast release = 9C01 = 270 SIOF = Start 1/0 fast release = 9C01 = 270 SL Subtract logical = 5F = 2.1+0.4x+1.3W2 SLA = Shift left single = 8B = 4.9 (average) SLDA = Shift left double = 8F = 7.9 (average) SLDL = Shift left double = 8F = 7.9 (average) SLDL = Shift left single logical = 8D = 3.9 (if SA<32, else 3.2) SLL = Shift left single logical = 1F = 0.9 SP = Subtract logical = 1F = 8.4+3.6N1 (average) SPB = Set page bits = 15 = 3.1 if disconnected, else 14.9 SPKA = Set PSW key from address = 120A = 8.6 SPM = Set Program Mask = 0.9 SRA = Shift right single = 8A = 3.1 (average) SRA = Shift right double = 8E = 4.3 (average) SRDA = Shift right double = 8E = 4.3 (average) SRDA = Shift right double = 8E = 4.3 (average) SRDA = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.3 (average) SRDL = Shift right double = 8E = 4.7 (= 4.8 + 3.2) SRD = Store denacter = 15 = 1.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.6 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 1.7 + 0.4 + 0.5 + 1.7 + 0.4 + 1.7 + 0.5 + 0.5 + 0.7 + 0.5 + 0.6 + 0.7 + 0.5 + 0.6 + 0.6 + 0.3 + 5.0 + 0.4 + 4.2 = 0.5 + 0.4 + 4.2 = 0.5 + 0.6 + 0.4 +		-		
SD Subtract normalized (long) 68 14.5+2.6Z2 SDR Subtract normalized (long) 28 11.6 SE Subtract normalized(short) 78 7.2+1.3Z2 SER Subtract normalized(short) 78 7.2+1.3Z2 SER Subtract normalized(short) 78 7.2+1.3Z2 SER Subtract normalized(short) 78 7.2+1.3Z2 SER Subtract normalized(short) 78 7.2+1.3Z2 SIO Start 1/0 9C00 270 SIOF Start 1/0 fast release 9C01 270 SL Subtract logical SF 2.1+0.4X+1.3W2 SLA Shift left single 88 4.9 (average) SLDA Shift left double logical 80 3.9 (if SA<32, else 3.2) SLL Shift left double logical 80 3.9 (if SA<32, else 3.2) SLL Shift left single logical 80 3.9 (if SA<32, else 3.2) SLL Shift left double logical 1F 0.9 SP Subtract decimal FB 8.4+3.6N1 (average) SPKA Set PSW key from address B20A 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SRA Shift right single 8A 3.1 (average) SRA Shift right double logical 80 1.7 (+0.4 if SA ≥32) SRL Shift right double logical 86 1.4 (average) SRA Shift right double logical 86 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 86 4.3 (average) SRDL Shift right double logical 86 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 86 4.3 (average) SRL Shift right double logical 86 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 87 7.7 (+0.4 if SA ≥32) SRL Shift right double logical 86 11.6 if disconnected, else 4.7 SSK Set storage key 08 11.6 if disconnected, else 4.7 SSK Set storage key 08 11.6 if disconnected, else 4.7 STCAP Store capacity counts B21F 21.5 STCK Store clock comparator B207 13.1 STCM Store character under mask BE 11.1 (average) STCTL Store (long) 60 3.5+0.4x+422 STH Store halfword 40 1.7+0.4x+1.6W2 STIDC Store channel 1D B202 3.0 STM Store multiple 90 0.9-0.6Z2+(1.3+2.2Z2)R STNSM Store then AND system mask AD 17.6		-		
SDR Subtract normalized (long) 2B 11.6 SE Subtract normalized(short) 7B 7.2+1.3Z2 SER Subtract normalized(short) 3B 5.3 SH Subtract halfword 4B 2.2+0.4X+1.3W2 SIO Start 1/0 fast release 9C01 270 SL Subtract logical 5F 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double 8F 7.9 (average) SLDA Shift left double logical 8D 3.9 (if SA ³ 2, else 3.2) SLL Shift left single logical 8D 3.9 (if SA ³ 2, else 3.2) SLL Shift left single logical 8D 3.9 (if SA ³ 2, else 3.2) SLL Shift left single logical 1F 0.9 				
SE Subtract normalized(short) 7B 7.2+1.3Z2 SER Subtract normalized(short) 3B 5.3 SH Subtract halfword 4B 2.2+0.4X+1.3W2 SIO Start 1/0 fast release 9C01 270 SIOF Start 1/0 fast release 9C01 270 SLA Shift left single 8B 4.9 (average) SLA Shift left double 0SF 2.1+0.4X+1.3W2 SLA Shift left double 0SF 7.9 (average) SLDL Shift left double 0SF 7.9 (average) SLDL Shift left double 0SF 7.9 (average) SLL Shift left double 0SF 7.9 (average) SLL Shift left single logical 89 2.7 (+0.4 if SA ≥32) SLL Shift left single logical 1F 0.9 SP Subtract logical 1F 0.9 SP Subtract decimal FB 8.4+3.6N1 (average) SPKA Set PSW key from address B20A 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SRA Shift right single 8A 3.1 (average) SRA Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right single logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right single logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right single logical 88 11.6 if disconnected, else 4.7 SSM Set system mask 80 118.2 ST Store character 42 1.7+0.4X+1.6W2 STCAP Store capacity counts B21F 21.5 STCK Store clock B205 19.4 STCM Store character under mask BE 11.1 (average) STCTL Store Control B6 4.0+1.3W STD Store (long) 60 3.5+0.4X+4Z2 STH Store character under mask BE 11.1 (average) STCTL Store (long) 60 3.5+0.4X+4Z2 STH Store halfword 40 1.7+0.4X+1.6W2 STIDE Store channel D B203 50-100(channel dependent) STIDP Store CPU D B202 3.0 STM Store then AND system mask AD 17.6				
SER Subtract normalized(short) 3B 5.3 SH Subtract halfword 4B 2.2+0.4X+1.3W2 Sl0 Start 1/0 9C00 270 Sl0 Start 1/0 fast release 9C01 270 SL Subtract logical 5F 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double 0gical 8D 3.9 (if SA<32, else 3.2) SLL Shift left double logical 8D 2.7 (+0.4 if SA \geq 32) SLL Shift left single logical 8D 2.7 (+0.4 if SA \geq 32) SLR Subtract logical 1F 0.9 SP Subtract decimal FB 8.4+3.6N1 (average) SPKA Set PSW key from address B20A 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SR Subtract 1B 0.9 SRA Shift right single 8A 3.1 (average) SRDA Shift right double logical 8C 3.9 if SA<32, else 3.2) SLL Shift right double 8E 4.3 (average) SRDA Shift right double 8E 4.3 (average) SRDA Shift right double 8E 4.3 (average) SRDA Shift right double 88 2.7 (+0.4 if SA \geq 32) SRL Shift right double 88 2.7 (+0.4 if SA \geq 32) SRL Shift right double 88 2.7 (+0.4 if SA \geq 32) SRD Shift right double 88 2.7 (+0.4 if SA \geq 32) SRD Shift right double 88 11.6 if disconnected, else 4.7 SSM Set storage key 08 11.6 if disconnected, else 4.7 SSM Set system mask 80 18.2 ST Store character 42 1.7+0.4X STCAP Store capacity counts B21F 21.5 STCK Store clock B205 19.4 STCK Store clock B205 19.4 STCM Store character under mask BE 11.1 (average) STCT Store (short) 70 2.1+0.4X+4.22 STE Store (short) 70 2.2+0.222.18 STDSM Store then AND system mask AD 17.6				
SH Subtract halfword 4B 2.2+0.4X+1.3W2 SIO Start 1/0 9C00 270 SIOF Start 1/0 fast release 9C01 270 SL Subtract logical SF 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 3.1 (if disconnected, else 14.9 SP Subtract decimal FB 8.4+3.6N1 (average) SPKA Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SR Subtract 1B 0.9 SRA Shift right single 8A 3.1 (average) SRDA Shift right double 8E 4.3 (average) SRDA Shift right double 160 18(3.9 if SA<32, else 3.2) SRL Shift right single 03 11.6 if disconnected, else 14.7 SSK Set storage key 08 11.6 if disconnected, else 14.7 SSK Set storage key 08 11.6 if disconnected, else 14.7 STCAP Store clock comparator 8207 13.1 STCK Store clock comparator 8207 13.1 STCK Store clock comparator 8207 13.1 STCK Store clock comparator 8207 13.1 STCM Store chancel 10 8203 50-100(channel dependent) STIDP Store CPU D 8202 13.0 STM Store multiple 90 0.9-0.622+(1.3+2.222)R STNSM Store then AND system mask AD 17.6				
Si0 Start 1/0 9C00 270 Si0F Start 1/0 fast release 9C01 270 SL Subtract logical 5F 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double 8F 7.9 (average) SLDL Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 2.7 (+0.4 if SA ≥32) SLR Subtract logical 1F 0.9 				
SIOF Start I/O fast release 9C01 270 SL Subtract logical 5F 2.1+0.4X+1.3W2 SLA Shift left single 8B 4.9 (average) SLDA Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left double logical 8D 3.9 (if SA<32, else 3.2) SLL Shift left single logical 8D 3.9 (if SA<32, else 3.2) SLR Subtract logical 1F 0.9 SP Subtract decimal FB 8.4+3.6N1 (average) SPB Set page bits B5 13.1 if disconnected, else 14.9 SPKA Set PSW key from address B2OA 8.6 SPM Set Program Mask 04 3.2 SPT Set CPU timer B208 35.9 SR Subtract 1B 0.9 SRA Shift right single 8A 3.1 (average) SRDA Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right single 8A 3.1 (average) SRDA Shift right double logical 88 2.7 (+0.4 if SA ≥32) SRL Shift right single logical 88 2.7 (+0.4 if SA ≥32) SRP Shift and round decimal F0 18+0.8M1+(SA/7 up)(2.4+0.9N1) SSK Set storage key 08 11.6 if disconnected, else 14.7 SSM Set system mask 80 18.2 ST Store character 42 1.7+0.4X+1.6W2 STCA Store clock 8205 19.4 STCK Store clock 8205 19.4 STCKC Store clock 8205 19.4 STCKC Store clock 8205 19.4 STCKC Store clock 8205 19.4 STCK Store clock 86 4.0+1.3W STD Store (long) 60 3.5+0.4X+422 STH Store halfword 40 1.7+0.4X+1.6W2 STID Store chanel D 8203 50-100(channel dependent) STIDP Store CPU D 8202 13.0 STM Store multiple 90 0.9-0.622+(1.3+2.2Z2)R STNSM Store then AND system mask AD 17.6				
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STOSM Store then OR system mask AD 17.6				
STPT Store CPU timer B209 21.2	STOSM	Store then OR system mask	AD	17.6
	STPT	Store CPU timer	B209	21.2

Mnem	Instruction	<u> 0p</u>	Timing in Micro sec
	 Subtract unnormalized (short)	 7F 	7.2+1.3Z2
SUR	· • ·	3F 	5.5
SVC	Supervisor call	0A	148.0
SW		6F 	14.3+2.6Z2
SWR	Subtract unnormalized	2F 	11.6
	Subtract normalized (extended)	37 	50(20 oprd value dependent)
тсн	Test channel		 100-200 (chan. dependent)
			100-200 (chan. dependent)
		91	2.2
			7.9+4.5N+1.3Z1
			2.9+3.2T
			2.5
UNPK	 Unpack 	 F3 	4.8+3.3((N1-1)/2 up)+1.6W1Q1)
X	LExclusive OR	57	2.1+0.4X+1.3W2
• •		D7	4.7+1.3(N1/4 up), average
		97	2.2
		17	0.9
ZAP	Zero and add	F8	3.6+3.3N1 (average)

Legend:

(average)=	average timing or rough formula (weighted on instruction mix basis) but exact formula is supplied following this legend.
C =	number of bytes compared until unequal found
	condition code
	number of operand characters compared or moved
	number of pad characters compared or moved
	common length (of both operands)
	number of digits to be edited
	number of message characters
-	number of 1-bits in the mask
n =	number of digits in either multiplier or
	multiplicand, whichever contains the smaller value.
N =	number of characters (used or moved)
	number of characters in operand 1
	number of characters in operand 2
N/4 =	number of characters divided by 4 (fullwords)
Q1 =	0 if the operand 1 ending byte is located on an
-	odd address, else Q1 is 1.
	number of registers stored or loaded
	contents of register 1 (or 2)
	shift amount, number of bit positions (or digits) shifted
	number of translated bytes
UCW scan =	a time range from 60 to 300 us depending on the
	in-use or not in-use state of affected UCW's.
up =	up or rounded up means to round up the fraction
	to the next fullword integer.
W1 =	number of word boundary crossings in the first operand field (length N1)
W2 =	number of word boundary crossings in the second
X =	operand field (length N2) 1 if X-field in the instruction is not zero,
^ -	else $X = 0$.
Z1 =	0 if operand 1 starts on word boundary, else 1.
	0 if operand 2 starts on word boundary, else 1.
	is a tolerance figure which shows how much the
	basic time can vary depending on the numeric
	value of the operands (e.g. Multiply, Divide,
	etc) or on operand alignment.
50-600 =	the execution time range for an $1/0$ instruction.
	The time depends on the 1/0 device (or channel
	type) and on the current status.
	/1

Note on Branching: Successful branches require an additional time of 2.3 us for instruction buffer reloading.

If a delay is to be programmed with a Branch on Count
instruction, a 1-second wait, for example, can be achieved by entering Hex 00041FBE in the counter, and branching back to the Branch on Count.

Special Instructions

The 4331 Processor provides as a standard feature a MOVE INVERSE instruction which is especially useful for Middle East countries where the writing sequence is right-to-left. The instruction is defined as follows:

Move Inverse (MVCIN)

MVCIN D1(L,B1), D2(B2)

I	E8	1	L	B	1	D 1	B2	D2	ł
									-

Bytes from the second operand are fetched right to left and placed left to right in the first-operand location.

The location and length of the first operand are specified in the same way as the location and length of the first operand of any SS-format instruction. The second operand has the same length as the first operand, but the second-operand address specifies the right-most byte of the second operand. When the operands overlap, the result is obtained as if the operands were processed one byte at a time and each result byte were stored immediately after the necessary operand byte is fetched.

Condition Code: The code remains unchanged.

Program Exceptions:

Access (fetch, operand 2; store, operand 1)

<u>Note</u>: The mnemonic MVCIN is not supported by conventional assemblers.

Resolution of Average Values

Where the instruction execution time depends directly on the number of bit positions shifted or the value of a mask, an average is formed from all possible cases. In other cases where operand alignment or the numeric value of an operand has a significant influence on the execution time, a handy rough formula is supplied to allow a quick assessment. The individual values are given below in microseconds:

CLM-Timing

<u>M2</u>	time
0	6.0
1	10.1
2	8.9
2 3 4	12.0
4	7.7
5	12.0
6	10.8
7	13.9
8	6.8
9	12.3
A	11.1
B	14.2
C	9.9
D	14.2
E	13.0
F	16.1

STCM Timing

SLA-Timing

> shift amount ≥ 32, then: 4.3 (+0.7 if binary ovérflow)

If R1 negative, shift amount < 32, then: 6.7 (+0.7 if binary overflow)

> shift amount \geq 32, then: 5.8 (binary overflow assumed)

SRA-Timing

R1 positive: 3.1 (+0.4 if shift amount \ge 32) R1 negative: 4.1 (-1.0 if shift amount \ge 32)

SRDA-Timing

R1 positive, shift amount < 32 then 4.3
≥ 32 then 3.6
R1 negative, shift amount < 32 then 5.7
≥ 32 then 5.0</pre>

SLDA-Timing

AP, SP-Timing

- 8.4+3.6N1 plus case-dependent portion:
- a. If N2<N1 and effective addition, then: + 0.4+2 (((N2-N1)/4)up)+1.4Z4W4
- b. If N1<N2 and effective subtraction, then: + 2.7(((N2-N1)/4)up)-0.9+1.4Z4W4
- c. If result is "minus zero", then: + 2.5
- d. If result is recomplemented, then: + 1.6+4.2N1+3.6((((N2-N1)/4)up), positive values only)

Legend:

- Z4 = ((((Addr 0p2)+N2-N1) modulo 4)/4)up
- W4 = number of word boundary crossings in the field defined by Addr Op2...(Addr Op2)+N2-N1-1)

CVD Timing

- a. If decimal result consists of more than 8 significant (non-zero) decimal digits (R1>99,614,720), then: 65.9+4.4Z2+0.4X
- b. If R1>18 significant bits, then: 31.3+3.3Z2+0.4X
- c. If R1 contains more than 9, but less than 18 significant bits, then: 24.1+4.4Z2+0.4X
- d. If R1≤ 9 significant bits then: 16.3+4.4Z2+0.4X

MVC Timing

- a. In case of 4-byte overlap of both operands (which is likely when Op1 start address minus Op2 start address <4), then:
 2.4+3.2N
- b. If Op1 start addr minus Op2 start addr 4, then: 2.2+2.9(N/4up)+1.3Z2W2+1.9Z1W1

Note: If N>16, then: 3.5+2.9((N addr modulo 4)/4up)+1.3(Z2W6+Z8W8)+1.6Z1

Legend:

- Z8 = ((ADR2-ADR1)modulo 4)/4 up
- W8 = number of word boundary crossings in the field starting at ADR2+8-(ADR1 mod 4) with length N-8+(ADR1 mod4)
- W6 = number of word boundary crossings in the field starting at ADR2 with length 8-(ADR1 mod 4)
- ADR1= Operand 1 address
- ADR2= Operand 2 address

XC Timing

a.	If $ADR1 = ADR2$ th	en:
	N=14B (bytes):	3.8+1.6Z1
	N=58B:	5.9+3.2Z1
	N>8B :	5.9+3.2Z1 4.7+1.3(N+ADR1 mod 4)/4 up
b.	N<6B: 5.2+3.5N N≥6B:	ADR2 but no overlap within 4 bytes: R+1)mod4)/4 up+1.3Z8W2
c		DR2 but overlapping within 4 bytes
	(1≤ADR1-ADR2≤3), 3.4+3.5N	

Legend:

Z8 = see legend of MVC Timing

ZAP Timing

3.6+3.3N1 + 2.7 if "minus zero" result + 0.7+(2.3+1.4Z4)((N2-N1)/4 up)if N2 N1

Legend

Z4 = see legend of AP, SP Timing

4331 Model Group 2

Mnem	Instruction	0p	Timing in Micro sec
AD ADR AE AER AH AL ALR AP AR AU AUR AW AWR	<pre>Add normalized (long) Add normalized (long) Add normalized (short) Add normalized (short) Add halfword Add logical Add logical Add decimal Add decimal Add (register) Add unnormalized (short) Add unnormalized (short) Add unnormalized (long) Add unnormalized (long)</pre>	7A 3A 5E 1E 1A 7E 3E 6E 2E	<pre> 1.1+0.3X+0.4(W2+2K2+P2) 8.4+0.2Z2(W2+2K2+P2) 8.4 4.6+0.2Z2(W2+2K2+P2) 4.05 1.1+0.3X+0.4(W2+2K2+P2) 1.1+0.3X+0.4(W2+2K2+P2) 0.7 4.7+0.7N1(average) 0.7 4.7+0.7Z2(W2+2K2+P2) 4.25 9.0+0.2Z2(W2+2K2+P2) 4.25 9.0+0.2Z2(W2+2K2+P2) 8.9 38 (11, oprd value dependent) </pre>
BALR BC BCR BCT BCTR BXH	Branch and link Branch on Condition Branch on Condition Branch on count Branch on count Branch on index high	45 40 47	1.0+0.3X 0.8 0.7(no branch);0.7+0.3X(branch) 0.5 1.2+0.3X 1.0 2.0 2.0
CD CDR CDS CE CER CH CL CLC CLCL CLCL CLCL CLR CLR IO	<pre> Compare (long) Compare (long) Compare double and swap Compare (short) Compare (short) Compare halfword Compare logical Compare logical Compare logical (long) Compare logical under mask Compare logical under mask Compare logical under mask</pre>	BB 79 39 49 55 05 0F 95 8D 15 9D01 8215	<pre>1 1.1+0.3X+0.4(W2+2K2+P2) 6.5+0.2Z2(W2+2K2+P2) 6.1 5.0(cc=0);4.1(cc=1) 3.6+0.2Z2(W2+2K2+P2) 3.15 1.1+0.3X+0.4(W2+2K2+P2) 1.1+0.3X+0.4(W2+2K2+P2) 1.5+0.6(C/4 up)+0.2 Z1(W1+2K1+P1) +0.4Z2(W2+2K2+P2) 20+0.21C1+0.2C2 1.1 7.92 (average) 0.7 100-500 (device dependent) 138.5 2.2+0.9((MAX(N1,N2))/4 up)+ 0.3Y1(W1+2K1+P1)+0.5Y2(W2+2K2+P2)</pre>

Mnem |Instruction

mne	em		1	l
CR		[19	0.7
CS				3.2(cc=0);2.9(cc=1)
CTI		Connect page		22.4(cc=0),15.8(cc=1),
UII	r-	l l	•	8.9(cc=2)
CVI	D	' Convert to binary		17.8+0.3X+0.3Z2(2+2K2+P2)if converting
CVI	D			less than 7 non-zero decim. digits,
				else 51.4+0.3X+0.3Z2(2+2K2+P2)
CVI	n	Convert to decimal		14.0+0.3X+0.2Z2(2+2K2+P2) if
CVI			-	result has less than 8 signif.
				(non-zero) digits (R1<99,614,720),
				else 28.7+0.3X+
				10.2Z2(2+2K2+P2)
D		Divide	5D	, 14.7+0.3X+0.2(W2+2K2+P2)
-				17(cc=0), 11(c=1)
DD				60.15+0.2Z2(2+2K2+P2)+0.3X (average)
DDI				59.65 (average)
DE				15.7+0.2(W2+2K2+P2)+0.3X (average)
DE				27.3 + UCW scan time
DE		5 . 5		15.2 (average)
DP				15.95+7(N1-N2)+
				10.5Y1(W1+2K1+P1)+
				0.3Y2(W2+2K2+P2)+14.1
DR		Divide	1D	
ED		Edit	DE	6+2.5N1+8D+3F
				6+2.5N1+8D+3F
EX			-	13.6+t(Subject instruction)
HD	R	Halve (long)	24	7.8
HD	V	Halt device	19E	100-600 (device dependent)
HEF	R	Halve (short)	34	4.8
HIC	0	Halt /O	19E	100-600 (device dependent)
10			43	0.9+0.3X
101	M	Insert characters under	BF	7.25 (average)
		lmask		
IPI				9.4
IP		•	B20B	
I SI	K	linsert storage key	•	6.5 if disconnected, else 7.9
L		Load		0.9+0.3X+0.2(W2+2K2+P2)
LA		Load address		0.7+0.3X
			-	
		· ·		
LCF			-	
				15.5+0.2R
LD				1.3+0.2Z2(W2+2K2+P2)+0.3X
LDI	ĸ	Load (long)	28	0.9

Mnem	Instruction	0p	Timing in Micro sec
	Load (short)	78	1.3+0.2Z2(W2+2K2+P2)+0.3X
LER	Load (short)		0.7
	Load frame index		10.1(cc=0,1), 6.9(cc=2,3)
	Load halfword		1.0+0.3X+0.3(W2+2K2+P2)
	Load multiple		0.7+0.2R+0.2Z2(R+2K2+P2)
	Load negative (long)		1 1.8
	Load negative (short)		1 1.4
	Load negative		1.1 if R2 positive, else 0.8
	Load positive (long)		1.8
	Load positive (short)		
	Load positive		1 0.9
	Load		
	Load real address		24+0.3X
	Load rounded (extended	25	6.7
	operand, long result)	1	
	Load rounded (long ope-	35	3.5
	rand, short result)		 1 1
	Load and test (long)	22	1.1 0.8
	Load and test (short)		0.6
LIK			
M	Multiply	150	13.5+0.3X+0.2(W2+2K2+P2)
MAD	Make addressable	B21D	9.7(cc=1),10.6(cc=0)
MC	Monitor call	AF	1 5.8(without interrupt),4.3 if NOP
MD	Multiply (long)	16C	43.76+0.2Z2(2+2K2+P2)+0.3X (average)
MDR	Multiply (long)	20	143.36 (average)
ME	Multiply (short)	170	12.36+0.2(W2+2K2+P2)+0.3X (average)
MER	Multiply (short)	130	111.96 (average)
MH	Multiply halfword		8.5+0.3X+0.2(W2+2K2+P2)
MP	Multiply decimal		20.8+4.3n+0.5Y1(W1+2K1+P1)+0.3Y2
	l		(W2+2K2+P2) average
MR	Multiply		12.9
MUN	Make unaddressable		9.7(cc=1),11.2(cc=0)
MVC	Move (characters)	D2	2.2+0.4(N/4 up)+
			0.2Z1(W1+2K1+P1)+0.2Z2(W2+2K2+P2)
	Move (long)	-	20+0.11C1+0.1C2
MVI	Move (immediate)		0.9
	Move Inverse	IE8	1.6 + 0.4N
	Move numerics	D1	1.7+0.7N
	Move with offset		2.1+1.3N1
	Move zones	-	1.7+0.7N
	Multiply (long operand)	-	163.5
MXDR	Multiply (long operand,	27	62.5
	extended result)		
MXR	Multiply (extended)	26	211
N		154	1.1+0.3X+0.4(W2+2K2+P2)
NC	AND	D4	1.7+0.6N
NI	AND	194	1.1

Mnem		-	Timing in Micro sec
 NR	 AND 	•	l de la constante de
0 0C 01 0B	OR OR OR	56 D6 96 	1.1+0.3X+0.4(W2+2K2+P2) 1.7+0.6N 1.1
PACK PTLB	Pack Purge TLB 	F2 B20D	2.5+0.5N1+0.3QP(WP+2KP+PP)(average) 11.7
RRB RSP SCK SD SCK SD SCK SD SCK SD SCK SD SD SE SE SE SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLD SLA SLA SLD SLA SLA SLD SLA SLA SLA SLA SLA SLA SLA SLA SLA SLA	<pre> Reset Reference bit Retrieve status and page Subtract Set clock Set clock comparator Subtract normalized (long) Subtract normalized (long) Subtract normalized (short) Subtract normalized(short) Subtract normalized(short) Subtract halfword Start 1/0 Start 1/0 Start 1/0 Start lof fast release Subtract logical Shift left single Shift left double Shift left double Shift left single logical Subtract logical Subtract decimal Set page bits Set PSW key from address Set Program Mask Set CPU timer Subtract Shift right single Shift right double Shift right double Shift right double Shift right single logical Shift right single logical Shift right single logical Shift right and round decimal</pre>	B213 5B B204 B206 6B 2B 7B 3B 4B 9C00 9C01 5F 8B 85 85 85 85 85 820A 15 820A 18 820A 18 820A 18 820A 18 820A 18 820A 18 18 18 18 18 18 18 18	<pre>9.7 657(cc=0),14(cc=3) 1.1+0.3X+0.4(W2+2K2+P2) 36.2 33.6 8.4+0.2Z2(W2+2K2+P2)+0.3X 8.4 4.6+0.2Z2(W2+2K2+P2)+0.3X 4.05 1.1+0.3X+0.4(W2+2K2+P2) 280 280 1.1+0.3X+0.4(W2+2K2+P2) 5.0 (average) 7.15 (average) 3.2 if SA < 32, else 2.6 2.3 0.7 4.7+0.7N1 (average) 12. 7.2 3.4</pre>
SSM ST STC	Set system mask Store Store characters	80 50	12.8 0.9+0.3X+0.2(W2+2K2+P2) 0.9+0.3X
STCK STCKC STCM STCTL STD	Store clock Store clock comparator Store character under mask Store Control Store (long)	B240 B207 BE B6 60	19.4 13.1 5.83 (average) 1.6+0.2R 1.5+0.2Z2(W2+2K2+P2)
STE	Store (short)	70	1.1+0.2Z2(W2+2K2+P2)

Mnem	Instruction	0p	Timing in Micro sec
STIDC STIDP STM STNSM STOSM STPT	Store channel ID Store CPU ID	B203 B202 90 AC AD	0.7+0.2R+0.2Z2(R+2K2+P2) 13
SUR	(short)	 3F 	4.25
SVC Sw	Supervisor call	0A 6F	29.2 9.0+0.2Z2(W2+2K2+P2)
SWR		2F 	8.9
SXR	Subtract normalized (extended)		38(11, oprd value dependent)
TIO TM TR TRT TS	Test /O Test under mask Translate Translate and test	9D00 91 DC	100-200 (chann. dependent) 100-500 (chann. dependent) 0.9 2.3+2.2N 1.5+1.3T+1. 1.4
		F3	2.6+0.5((N1-1)/2 up) +0.2QU(WU+2KU+PU)
XC X I	Exclusive OR (character) Exclusive OR (immediate)	57 D7 97 17	1.1+0.3X+0.4(W2+2K2+P2) 5.6+0.2(N1/4 up),average 1.1 0.7
ZAP	Zero and add		4.5+0.6N1 plus: +0.9 if negative zero operand processed +0.4+(0.8ZR)ceil((N2-N1)/4) if N2>N1

Legend

(average)=	means average timing or rough formula (weighted on instruction mix basis) but exact formula is
C =	supplied following this legend. number of bytes compared in CLC (left to right) until mismatch is found ($C \leq N$).
= DD	condition code
	number of operand characters compared or moved
	number of pad characters compared or moved
	common length (of both operands)
	number of digits to be edited
	number of message characters
	number of 1-bits in the mask
	number of digits in either multiplier or
••	multiplicand, whichever contains the smaller
	value.
N =	number of characters
	number of characters in operand 1
	number of characters in operand 2
	number of characters divided by 4 (fullwords)
	is 0 if the operand 1 ending byte is located on
Y.	an odd address, else Q1 is 1.
Q2 =	is 0 if operand 2 ending byte is located on an
~	odd address, else Q2 is 1.
R =	number of registers stored or loaded
	contents of register 1 (or 2)
	shift amount number of bit positions (or digits)
	shifted
T =	number of translated bytes
UCW scan =	is a time range from 60 to 300 us depending on
	the in-use or not in-use state of affected
	UCW's.
up =	up or rounded up means to round up the fraction
	to the next fullword integer.
	ceil((Addr(0P1)mod4)/4)
=	1 if operand 1 not starting at a word boundary,
70 -	else_0 ceil((Addr(0P2)mod4)/4)
_	1 if operand 2 not starting at a word boundary, else 0
ZR =	ceil((Addr(0P2)+N2-N1)mod4)/4)
211	
Y1 =	ceil(((Addr(OP1) + N1)mod4)/4
	1 if operand 1 not ending at a word boundary,
	else 0
Y2 =	ceil(((Addr(0P2) + N2)mod4)/4)
	1 if operand 2 not ending at a word boundary,
	else 0
QP =	(Addr(0P2) + N2 - 1)mod2
QU =	(Addr(OP1) + N1 - 1)mod2
	Number of word-boundary cross-overs in the 1st
	operand field (length N1 or N where applicable);
	in CLC number of word-boundary cross-overs in

,

the 1st operand fie	ld with the length
min(4ceil(C/4),N),	starting left.

W2

WP

WU

WR

K1

K2

KP

KU

KR

P1

P2

PP

PU

PR

= Number of word-boundary cross-overs in the 2nd operand field (length N2 or N where applicable); in CLC number of word-boundary cross-overs in the 2nd operand field with the length min(4ceil(C/4),N), starting left. = Number of word-boundary cross-overs in the 2nd operand field for the data length PACKed into the 1st operand field, discarding the rightmost byte of the 2nd operand. = Number of word-boundary cross-overs in the 1st operand field, discarding the rightmost byte of the 1st operand. = Number of word-boundary cross-overs in the field from Addr(OP2) to Addr(OP2)+N2-N1-1. = Number of line-boundary (64B) cross-overs in the 1st operand field (length N1 or N where applicable); in CLC number of line crossings in the 1st operand field with the length min(4ceil(C/4),N), starting left. = Number of line-boundary (64B) cross-overs in the 2nd operand field (length N2 or N where applicable); in CLC number of line crossings in the 2nd operand field with the length min(4ceil(C/4),N), starting left. = Number of line-boundary (64B) cross-overs in the 2nd operand field for the data length PACKed into the 1st operand field, discarding the rightmost byte of the 2nd operand. = Number of line-boundary (64B) cross-overs in the 1st operand field, discarding the rightmost byte of the 1st operand. = Number of line-boundary (64B) cross-overs in the field from Addr(OP2) to Addr(OP2)+N2-N1-1. = 1 if page boundary (2kB) cross-over occurs in the 1st operand field (length N1 or N where applicable), else 0; in CLC regard the 1st operand field with the length min(4ceil(C/4),N), starting left. = 1 if page boundary (2kB) cross-over occurs in the 2nd operand field (length N2 or N where applicable), else 0; in CLC regard the 2nd operand field with the length min(4ceil(C/4),N), starting left. = 1 if page boundary (2kB) cross-over occurs in the 2nd operand field for the data length PACKed into the 1st operand field, discarding the rightmost byte of the 2nd operand, else 0. = 1 if page boundary (2kB) cross-over occurs in the 1st operand field, discarding the rightmost byte of the 1st operand, else 0. = 1 if page boundary (2kB) cross-over occurs in

= 1 if page boundary (2kB) cross-over occurs in the field from Addr(0P2) to Addr(0P2)+N2-N1-1,

	else 0.
F	= 0 if nonzero function byte found, else 1.
т	= Number of bytes translated.
X	= 1 if the X-field in the instruction is nonzero, else 0.
ceil	= Ceiling function, rounds up to next integer
up	<pre>= round up to next integer (same as ceiling)</pre>
modx	= Modulo base x function
50-600	= the execution time range for an I/O instruction.
	The time depends on the I/O device (or channel type) and on the current status.

Average Values

Where the instruction execution time depends on a variety of data distribution patterns, such as the number of bit positions shifted or the value of a mask, an average is formed from all possible cases. The individual values are given below in microseconds:

CLM	Timing	ICM	Timing
<u>M2</u>	time	<u>M3</u>	time
0	3.9	0	6.8
1	4.7	1	6.8
	6.4	2	6.8
3	8.3		7.3
Ĩ4	5.4	3 4	6.8
5	8.3	5	7.3
2 3 4 5 6	7.3	6	7.3
	9.2	7	7.8
7 8	4.6	8	6.7
9	8.5	9	7.2
Α	7.5	A.	7.2
	9.4	B	7.7
B C	6.5	C	7.2
D	9.4	D	7.7
E	8.4	· · · E	7.7
F	10.3	F	8.2

STCM 1	iming
<u>M3</u>	time
0 1 2 3 4 5 6 7 8 9 A 8 0 2 5 6 7 8 9 A 8 5 6 7 8 9 A 8 5 6 7 8 9 A 8 5 6 7 8 9 8 5 6 7 8 9 8 5 6 7 8 9 8 5 6 7 8 9 8 7 8 9 8 9 8 7 8 9 8 9 8 9 8 9 8	$1.1 \\ 6.1 \\ 5.4 \\ 4.1 \\ 6.4 \\ 5.7 \\ 3.6 \\ 5.9 \\ 6.9 \\ 6.9 \\ 5.9 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 \\ 7.2 $

```
SLA Timing
```

If R1 positive, shift amount < 32, then: 4.5(+0.3 if binary overflow) shift amount ≥ 32, then: 4.0 (+0.3 if binary overflow) If R1 negative, shift amount < 32, then: 5.5 (+0.3 if binary overflow) shift amount ≥ 32, then: 3.1 (binary overflow assumed)

SRA Timing

R1 positive: 2.7 R1 negative: 3.7 if SA < 32, else 2.7

SRDA Timing

R1 positive, shift amount < 32 then 3.6 ≥ 32 then 3.0
R1 negative, shift amount < 32 then 4.5 ≥ 32 then 3.9

SDLA Timing

R1 positive, shift amount < 32 then 6.5 (+0.3 if cc3) ≥ 32 then 5.3 (+0.3 if cc3)
R1 negative, shift amount < 32 then 7.8 (+0.3 if cc3) ≥ 32 then 6.6 (+0.3 if cc3)

AS, SP Timing

4.7+0.7 N1 plus case dependent portion:

- a) If N1<N2 and effective addition, then: +0.9+0.8((N2-N1)/4)up)+0.4ZR(WR+2KR+PR)
- b) If N1<N2 and effective subtraction, then: +1.0+0.8((N2-N1)/4)up)+0.4ZR(Wr+2KR+PR)
- c) If intermediate result isminus zerothen: +1.5
- d) If intermediate result is recomplemented, then: +3.4+0.8N1+1.1(((((N2-N1)/4)up),positive values only)

MVC Timing

- a) In case of 4-byte overlap of both operands (which is likely when op1 start address minus op2 start address is <4), then:
 2.6 + 0.4N
- b) else 2.2+0.4(N/4 up)+0.2Z1(W1+2K1+P1)+0.2Z2(W2+2K2+P2)

PACK Timing

```
If N1 \leq 8, then:
2.5+0.5N1+0.3QP(WP+2KP+PP)
```

If N1 >8, then: 3.0+0.7((N2-N1/2up)+0.3QP(WP+2KP+PP) + a if N1-1((N2-1)/up) where a =0.4+0.2(1+Z1)(N1-1-((N2-1)/2up))/4 up

ZAP Timing

4.3 + 0.7N1 plus case dependent portion: +0.9 ifminus zeroresult +0.4+(0.9+0.3ZR)((N2-N1)/4up) if N2>N1

XC Timing

a) If ADR1 = ADR2 then: N = 1...4B (bytes): 3.5+0.2Z1(1+2K1+P1) N = 5...8B : 4.5+0.2Z1(2+2K1+P1) N > 8B : 5.6+0.2(N+(ADR1)mod4)/4 up)

b) If ADR1 not equal ADR2 and no overlap within 4 bytes:

 $N \le 5B: 6.3 + 0.6N$ N > 5B: 9.4 + 0.6 ceil (N-1+(Addr(0p1)+1)mod 4)/4)+0.2ceil ((Addr(0p2)-Addr(0p1))mod 4)/4

c) If ADR1 unequal ADR2 but overlapping within 4 bytes
 (0 < ADR1-ADR2 <4), then:
 5.4 + 0.6N</pre>

MP Timing

MP and DP instructions.

```
a) If more than 8 significant multiplier
   digits (n)<sup>1</sup>), then:
   18.7+6.32n+0.5Y1(W1+2K1+P1)+0.3Y2(W2+2K2+P2)
b) If N1+N2 > 12, then:
   19.42+6.32n+.5Y1(W1+2K1+P1)+0.3Y2(W2+2K2+P2)
c) If 8 < N1+N2 \le 12, then:
   20.8+4.29n+0.5Y1(W1+2K1+P1)+0.3Y2(W2+2K2+P2)
d) If N1+N2 \leq 8, then:
   21.2+3.24n+0.5Y1(W1+2K1+P1)+0.3Y2(W2+2K2+P2)
1) 'number of significant multiplier
      digits' = minimum number of
      significant digits in OP1 or OP2, e.g.:
      0P\bar{1} = X'000001\bar{2}C'
      OP2 = X'980D'
      --> n = 2
Note: An even distribution of digits 0...9 is assumed for
```

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Appendix C : Definitions

Glossary of Terms and Abbreviations

This glossary contains technical terms associated with the subject of this publication. A wider and more general range of terms is contained in <u>IBM</u> <u>Data</u> <u>Processing</u> <u>Glossary</u>, GC20-1699.

IBM is grateful to the American National Standards Institute (ANSI) for permission to reprint its definitions from the American National Standard Vocabulary for Information Processing (Copyright c 1970 by American National Standard Institute, Incorporated), which was prepared by Subcommittee X3. 5 on Terminology and Glossary of American National Standards Committee X3. These definitions are indicated by an asterisk.

ABM = Asynchronous balanced mode ACF = Advance communications function ACK = Positive acknowledgement ACR = Abandon call and retry ACU=Automatic call unit

<u>address</u> <u>translation</u>: The process of changing the address of an item of data or an instruction from its virtual address to its processor storage address. See also dynamic address translation.

ADM = Asynchronous disconnect mode ARM = Asynchronous response mode ASCII = American National Standard Code for Information Interchange

basic control (BC) mode: A mode in which the features of a System/360 computing system and additional System/370 features, such as new machine instructions, are operational on a System/370 computing system. See also extended control (EC) mode.

BCC=Block check character

BCD=Binary coded decimal

bps=Bits per second

BSC=Binary synchronous communication

BSM=Basic storage module

CA=Communications adapter

CC=Condition code

CCITT=International Telephone and Telegraph Consultative Committee

CCW=Channel command word

CDSTL=Connect data set to line

CE=Channel end

CMDR=Command reject

<u>control registers</u>: A set of registers used for operating system control of relocation, priority interruption, program event recording, error recovery, and masking operations.

<u>control</u> <u>storage</u>: An area in a processor where the microcode is stored.

CPU=Central processing unit

CRC=Cyclic redundancy check

CRQ=Call request

CSW=Channel status word

CTLI=Control Interface

CTS=Clear to send

<u>cursor</u>: A movable marker on the video display used to indicate the position of the next character to be entered or deleted.

DE=Device end

DISC=Disconnect

DLE=Data link escape

DLO=Data line occupied

DM=Disconnected mode

DPR=Digit present

DSC=Distant station connected

DSR=Data set ready

DTE=Data terminal equipment

DTR=Data terminal ready

<u>*dump</u>: To copy the contents of all or part of a storage, usually from an internal storage into an external storage.

<u>dynamic</u> <u>address</u> <u>translation</u>: (1) The change of a virtual storage address to a processor storage address during execution of an instruction. See also address translation. (2) A hardware feature that performs the translation.

EBCDIC=Extended binary-coded decimal interchange code

ECPS=Extended control program support

ElA=Electronic Industries Association

ElB=Error index byte

EMU=Emulator

ENQ=Inquiry

<u>enter</u>: In this manual refers to the placing of information into the system by specifying commands, data or addresses at the keyboard, and then pressing the ENTER key. See also key in.

EON=End of number

EOT=End of transmission

ERP=Error recovery procedure

ETB=End of transmission block

ETX=End of text

<u>extended</u> <u>control</u> (<u>EC</u>) <u>mode</u>: A mode in which all the features of a System/370 computing system, including dynamic address translation, are operational. See also basic control (BC) mode.

FBS=Fixed block storage

FCS=Frame check sequence

HDV=Halt device

Hex=Hexadecimal

<u>hexadecimal</u>: A number system that uses the equivalent of the decimal number 16 as a base.

l=Information

IC=Integrated channel

ID=Identifier

IDA=Indirect data addressing

IDAL=Indirect data address list

IDAW=Indirect data address word

IML=Initial microcode loading

<u>initial microcode load</u>: The procedure that causes the microcode to be loaded into control storage. Abbreviated to IML.

<u>*initial progam load</u>: The procedure that causes the initial part of an operating system or other program to be loaded such that the program can then proceed under its own control. Abbreviated to IPL.

<u>*initialize</u>: To set counters, switches and addresses to zero or other starting values at the beginning of, or at the prescribed points in, a computer routine.

integrated adapter (or attachment): A device which allows 1/0 devices to be attached to the system without a standard control unit.

*interrupt: To stop a process in such a way that it can be resumed.

1/0=Input/output

IPL=Initial program loading

fSO=International Organization for Standardization

ITB=Intermediate text block

kbps=Kilobytes per second

<u>key in</u>: In this manual refers to the typing in or keying in of characters by means of the alphameric keys at the keyboard. It does not include pressing the ENTER key. See also Enter.

LRC=Longitudinal redundancy check

<u>microcode</u>: A sequence of microsteps, also termed a microroutine.

<u>*modem</u>: (MOdulator-DEModulator.) A device that modulates and demodulates signals transmitted over communication facilities.

MSD=Main storage directory

<u>multipoint</u> <u>network</u>: A line or circuit that interconnects several stations in a data communications system.

NAK=Negative acknowledgement

Nr=Number received

NRM=Normal response mode

NRZI=Nonreturn to zero inverted

Ns=Number sent

NSA=Nonsequenced acknowledge

NSP=Nonsequenced poll

<u>*online</u>: Pertaining to equipment or devices under control of the processor.

*operating system: Software which controls the execution of computer programs and which may provide scheduling, debugging, input/output control, accounting, compilation, storage assignment, data management, and related services.

PABX=Private automatic branch exchange

PCI=Program controlled interruption

P/F=Poll/Final

PIO=programmed input/output

PIU=Path information unit

PND=Present next digit

processor storage: All program addressable storage from which instructions can be executed and from which data can be loaded directly into registers.

program status word: A doubleword in the processor storage used to control the order in which instructions are executed, and to hold and indicate the status of the computing system in relation to a particular program.

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Abbreviated to PSW.

PSW=Program status word

PTTC=Paper tape transmission code

RNR=Receive not ready

RR=Receive ready

RTS=Request to send

RVI=Reverse interruption

SCA=Standard channel adapter

SCB=Station control block

SDLC=Synchronous data link control

SEP=Separator

SIO=Start input/output

SIOF=Start input/output fast

SLI=Suppress length indication

SNRM=Set normal response mode

SOH=Start of heading

SP=Space

S/S=Start/Stop

<u>stand-alone</u> program: An independent program that does not require an operating system.

STR=String switch

STX=Start of text

support processor: An independent control processor of the 4331 with its own clocking device.

SYN=Synchronization

<u>teleprocessing</u>: The processing of data that is received from or sent to remote locations by way of telecommunication lines. TIC=Transfer in channel

TLB=Translation look-aside buffer

<u>trap</u>: (ISO) An unprogrammed conditional jump to a specified address that is automatically activated by hardware, a recording being made of the location from which the jump occurred.

<u>tributary station</u>: In a centralized multipoint data communications system, this is a station, other than the control station, that can communicate only with the control station when polled or selected by the control stations.

<u>typamatic</u> <u>key</u>: A key that causes a single character entry when briefly depressed, and repetitive character entry as long as the key is held down.

UA=Unsequenced acknowledgement

UC=Unit check

UCW=Unit control word

virtual address: An address which refers to virtual storage and must, therefore, be translated into a processor storage address when it is used.

<u>virtual storage</u>: Addressable space that appears to the user as processor storage, from which instructions and data are mapped into processor storage locations. The size of virtual storage is limited by the addressing scheme of the computing system and by the amount of auxiliary storage available, rather than by the actual number of processor storage locations.

VRC-Vertical redundancy check

VTAME=Virtual telecommunications access method entry

WACK=Wait before transmit

XID-Exchange station identification

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Appendix D. CA Code Tables

					Lowe	r Case			Upper Case								
		ŕ				Mai	n Stora	ge Byte	e Positio	ons 0, 1	, 2, 3,	(S, B, A	, 8)				
Byte Posit	ions	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7	8	9	Α	В	с	D	E	F
0000	0		8	@		<u>®</u>			h		*	¢		<u>®</u>			н
0001	1	Space			v		q	&		Space			Y		٥	+	
0010	2	1			z		r	а		=			z		R	A	
0011	3		9	1		j			i		(?		J			1
0100	4	2					Minus Zero (MZ)	b		<						в	
0101	5		0	S		k			Plus Zero (PZ))	s		к			
0110	6		0 EOA #	t		I			\odot		 "ЕОА	т		L			\odot
0111	7	3					\$	с					1		!	с	
1000	8	4			Bypass		Re- store	d					Bypass		Re- store	D	
1001	9		Punch On (PN)	u		m			Punch Off (PF)		Punch On (PN)	υ		м			Punch Off (PF)
1010	A		Reader Stop (RS)	v		n			Horiz Tab		Reader Stop (RS)	v		N			Horiz Tab
1011	в	5			LF		CR LF	е		%			LF		CR LF	E	
1100	с		Up- shift	w		0		-	Down- shift		Up- shift	w		0			Down shift
1101	D	6			В ЕОВ		Back - space	f		-			B EOB		Back- space	F	
1110	E	7			Prefix		ldle	g		>			Prefix		Idle	G	
1111	F		© EOT	x		р			Delete		© eot	x		Р			Delete

0	1	2	3	4	5	6	7	4300 Byte			
	В	А	8	4	2	1	С	Terminal Code Structure			
Start	В	А	8	4	2	1	С	Stop Transmitted and Received Character			
	These codes perform no function in the 1050 Data Communication System but are valid data codes. They are not printable.										
\square	= Duplicate Assignment										

Notes:

1. Equivalent Functions CR/LF = NL

LF = Index

- 2. *S-bit* position (0 for lower case, set for upper case) inserted on receive operations or deleted on transmit operations. Insertion/deletion performed by hardware.
- 3. Start and stop bits are deleted at the CA during receive operations; added at the CA during transmit operations.

Figure 24. Code Structure for 1050 Data Communication System in IBM Terminal Control - Type 1 Operations

		Mai	n Stora	nge Byt	e Positi	ons O,	1, 2, 3,	(O, B, A	A, 8)
Byte Posit	ions	0000	0001	0010	0011	0100	0101	0110	0111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7
0000	0		8	Add		® -			н
0001	1	Space			Y		۵	+	
0010	2	1			z		R	A	
0011	3		9	1		J			I
0100	4	2					Mes- sage	в	
0101	5		0	S		к			Re- store
0110	6		0 EOA #	т		L			\otimes
0111	7	3					\$	с	
1000	8	4					*	D	
1001	9			U		M			Sub - tract
1010	A			V		N			Tab
1011	в	5			LF		CR	E	
1100	с			w		0			
1101	D	6			B EOB			F	
1110	E	7					ldie	G	
1111	F		© EOT	×		Р			Delete



Note: Start and stop bits are deleted at the CA during receive operations; added at the CA during transmit operations.

Figure 25. Code Structure for 1060 Data Communication System in IBM Terminal Control - Type 1 Operations

					Lowe	r Case							Upper	Case			
		ŕ				Mair	Storag	ge Byte	Positio	ns 0, 1,	2, 3, (S, B, A	, 8)				
Byte Positi	ons	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 2, 1, C)	Hex	0	1	2	3	4	5	6	7	8	9	A	В	с	D	E	F
0000	0		8	@		-			h		*	¢					н
0001	1	Space			У		q	&		Space			Y		۵	+	
0010	2	1			z		r	а		=			z		R	A	
0011	3		9	/		j			i		(?		J			1
0100	4	2						b		<						В	
0101	5		0	s		k)	s		к			
0110	6		0 EOA #	t		I			(V) •		± 0	т		L			Š
0111	7	3			, (S)		\$	с		;					i	с	
1000	8	4						d		:						D	
1001	9			u		m						U		м			
1010	А			v		n			Horiz Tab			v		N			Horiz Tab
1011	в	5			LF (Notes 3 & 5)		NL	е		%			LF (Notes 3 & 5)		NL	E	
1100	с		Up- shift	w		0			Down- shift		Up- shift	w		0			Down shift
1101	D	6			B EOB		Back- space	f		,			B EOB		Back- space	F	
1110	E	7					IDLE	g		>	•				IDLE	G	
1111	F		© eot	×		р						x		Р			

0	1	2	3	4	5	6	7	4300 Byte			
	В	А	8	4	2	1	С	Terminal Code Structure			
Start	В	А	8	4	2	1	с	Stop Transmitted and Received Character			
E	PTTC/EBCDIC characters are shown above dashed line. PTTC/BCD characters are shown below dashed line.										
			in unda EBCDI		oxes ar	e comr	non to	PTTC/BCD			

Notes:

- 1. Start and stop bits are deleted at the CA during receive operations; added at the CA during transmit operations.
- 2. S bit position (0 for lower case, 1 for upper case) is inserted during receive operations; deleted during transmit operations. Insertion / deletion is performed by hardware.
- 3. LF (line feed) performs indexing,

Figure 26. Code Structure for 2740 Communication Terminal or 2741 Communication Terminal in IBM Terminal Control – Type 1 Operations

- 4. NL (new line) performs a carrier return and line feed.
- The following characters (not used by 2740 or 2741 Communication Terminals) are provided for PTTC/ BCD and PTTC/EBCDIC programming considera-

tions with the 1050 Data Communication System: Punch ON (PN) '09' and '99'

- Bypass (BY) '38' and 'B8'
- Restore (RES) '58' and 'D8'
- Punch OFF (PF) '79' and 'F9'
- Delete (DEL) '7F' and 'FF' Prefix (PRE) '3E' and 'BE'.
- In the 2741, the index key is replaced by an attention key: no indexing can be performed during transmission. Indexing is performed when the terminal receives an index character from the line.

				<u></u>		Mair	n Stora	ge Byte	Positio	ns 0, 1	, 2, 3 (0), 1, 2,	3)				
Byte Positi	ions	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 5, 6, 7)	Hex	0	1	2	3	4	5	6	7	8	9	A	в	С	D	E	F
0000	0	NUL	DLE	DS		SP	&	-									0
0001	1	soн	DC1	sos						а	j			A	J		1
0010	2	sтх	DC2	FS	SYN					b	k	s		в	к	S	2
0011	3	ЕТХ	DC3							с	I	t		с	L	т	3
0100	4	PF	RES	вүр	PN					d	m	u		D	М	U	4
0101	5	нт	NL	LF	RS					e	n	v		E	N	v	5
0110	6	LC	BS	ЕОВ ЕТВ	υς					f	ο	w		F	0	w	6
0111	7	DEL	IL	PRE	ΕΟΤ					g	p	x		G	Ρ	x	7
1000	8		CAN							h	q	Ŷ		н	۵	Y .	8
1001	9		EM							i	r	z		-	R	z	9
1010	A	SMM	сс	SM		¢	ļ										
1011	в	VT					\$		=								
1100	с	FF	IFS		DC4	<	*	%	@///								
1101	D	CR	IGS	ENQ	NAK	()										
1110	E	so	IRS	АСК		+	;		-								
1111	F	SI	IUS	BEL	SUB	I	٦	?									

0	1	2	3	4	5	6	7	4300 Byte
0	1	2	3	4	5	6	7	EBCDIC Structure
0	1	2	3	4	5	6	7	Transmitted and Received Character

= Duplicate Assignment

Notes:

- During receive operations in non-text mode, the DLE character, followed by any of the bit configurations in columns 6 or 7, will cause the command to be ended. However, only those bit configurations indicated by are valid.
- 2. The following DLE sequences are defined:

'70' = ACK0

- '61' = ACK1
- '7F'= WABT

Figure 27. EBCDIC, as Used for Binary Synchronous Communication Control

			Main Storage Byte Positions 0, 1, 2, 3 (0, 7, 6, 5)														
Byte Posit	ions	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4, 5, 6, 7 (4, 3, 2, 1)	Hex	0	1	2	3	4	5	6	7	8	9	A	в	с	D	E	F
0000	0	NUL	DLE	SP	0	@	Р		p								
0001	1	зон	DC1	!	1	A	۵	а	q								
0010	2	sтх	DC2		2	В	R	b	r								
0011	3	ЕТХ	DC3	#	3	с	s	c	s								
0100	4	EOT	DC4	\$	4	D	т	d	t								
0101	5	ENQ	ΝΑΚ	%	5	E	υ	e	u								
0110	6	АСК	SYN	&	6	F	v	f	v								
0111	7	BEL	ЕТВ		7	G	w	g	w								
1000	8	BS	CAN	(8	н	x	h	x								
1001	9	нт	ЕМ)	9	I	Y	i	y								
1010	A	LF	SUB	*	:	J	z	j	z								
1011	в	VТ	ESC	+	;	к	[k	{								
1100	с	FF	FS	,	<	L		I	ł	а 1 — а							
1101	D	CR	GS		=	м]	m	}								
1110	E	so	RS		>	N	^	n	~								
1111	F	SI	US	1	?	0		0	DEL								

0 1

0

7

1



1

7



4

3

5

3

2

6

2





Notes:

 During receive operations in non-text mode, the DLE character, followed by any character appearing in column 3, causes the command to be ended.

2. There are three DLE sequences:

```
'30' = ACK0
```

- '31' = ACK1
- '3F' = WABT

Figure 28. ASCII, as Used for Binary Synchronous Communication Control

se a substantia de la constante de la constant La constante de la constante de

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