IBM

Field Engineering Education
Student Self-Study Course

SYSTEM/360

Introductory Programming
Book 5 – Input/Output Operations

Preface

This is Book 5 of the System/360 Introductory Programming Student Self-Study Course.

Course Contents

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Prerequisites

- Systems experience (1400 series with tapes, 7000 series with tapes) or a basic computer concepts course.
- Books 1 through 4 of this Introductory Programming course.

Instructions to the student and advisor

- This course is to be used by the student in accordance with the procedure in the Instructions to the Student section in Book 1 of this course.
- The course is to be administered in accordance with the procedure in the System/360 Introductory Programming Administrator Guide, Form #R23-2972.

This edition, R23-2959-1 is a minor revision of the preceding edition, but does not obsolete R23-2959-0. Numerous changes of a minor nature have been made throughout the manual.

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How to use this book

There are seven sections to this text. At the beginning of each section, is a list of Learning Objectives which you will be expected to learn as a result of studying that particular section. The book has a program exercise and review questions so that you can evaluate your progress.

This book also contains some tear-out pages. At an appropriate point in the text, you will be directed to remove one of the tear-out pages from the back of the book and use it as reference material. The use of tear-out pages eliminates the necessity of flipping back and forth in the book.

You will go through this book in a serial fashion. That is, you will not be expected to skip or branch around. The answer to each frame is in the next frame. You may find it helpful to use a standard IBM card to cover the answers as you read the frames.

Periodically, as you go through this book, you will be directed to study areas of the System/360 Principles of Operation manual. This will help you to become familiar with the manual so that it may be used as reference material at a later date.

THE CONTENTS OF THIS BOOK

System/360 Input/Output Operations

SECTION I LEARNING OBJECTIVES

At the end of this section, you should be able to do the following when given a format illustration of an I/O instruction, CAW, CCW and CSW:

1. State the function of the fields of a:
   "start I/O" instruction
   CAW
   CCW
   CSW

2. State how the "start I/O" instruction addresses a channel and a I/O device.

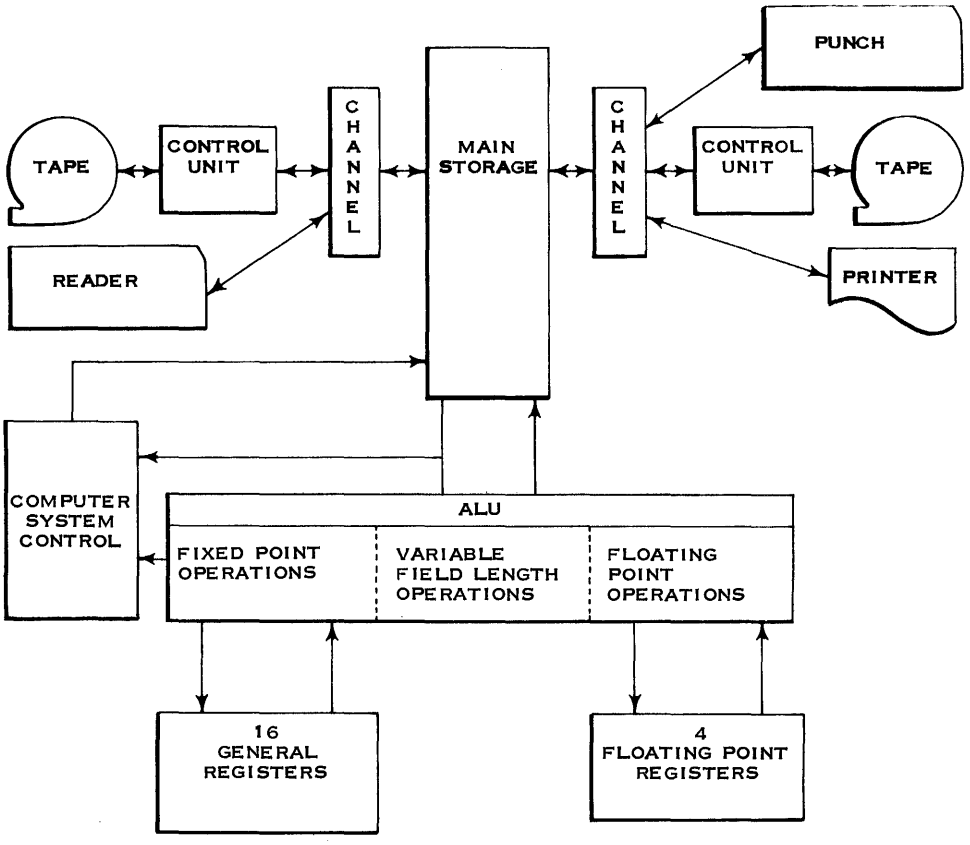
3. State the relationship between the "start I/O" instruction, CAW, CCW and CSW.

4. State the program, problem or supervisor in which I/O instructions must be executed.

Introduction to I/O Operation

In the self-study book titled "System/360 Introduction," you were introduced to the logical structure of the System/360. You found that in addition to processing, the ability to read data into main storage from an input device and to write data from main storage with an output device was also necessary. The intention of this book is to help you learn the input and output operations of the System/360. First let us review some of the material covered in the "System/360 Introduction."

CHANNEL CONCEPTS



Take a moment to review the data flow diagram above. Note the input-output data flow.

The preceding illustration shows that the section of a System/360 which is used to control the transmission of data between an input-output device and main storage is called a _____.

---

channel

Because the channel (abbreviated CH) is controlling the input-output (I/O) operation, the central processing unit (CPU) is free to continue processing. The simultaneous operation of a channel (CH) with an I/O data transmission and the CPU with processing is known as _____.

---

overlap

During an overlap operation, the channel (CH) and CPU are time-sharing the main storage unit. When the channel needs a main storage cycle, it requests one from the CPU. This is known as _____.

---

break-in

The channel controls the transmission of data bytes between the main storage and the I/O device. To take care of synchronizing the I/O device with the channel, a _____ _____ is needed.

---

control unit or
I/O adapter

Some I/O devices physically contain their associated control units. Other I/O devices, such as tape units, have _____ (internal/separate) control units.

---

separate

Write the names for the following abbreviations.

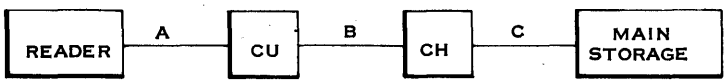
CPU = _____
I/O = _____
ALU = _____
CH = _____
CU = _____

CPU = Central Processing Unit
I/O = Input-Output
ALU = Arithmetic and Logic Unit (part of CPU)
CH = Channel
CU = Control Unit

As many as eight control units may be connected to a channel via a _____ _____ cable.

---

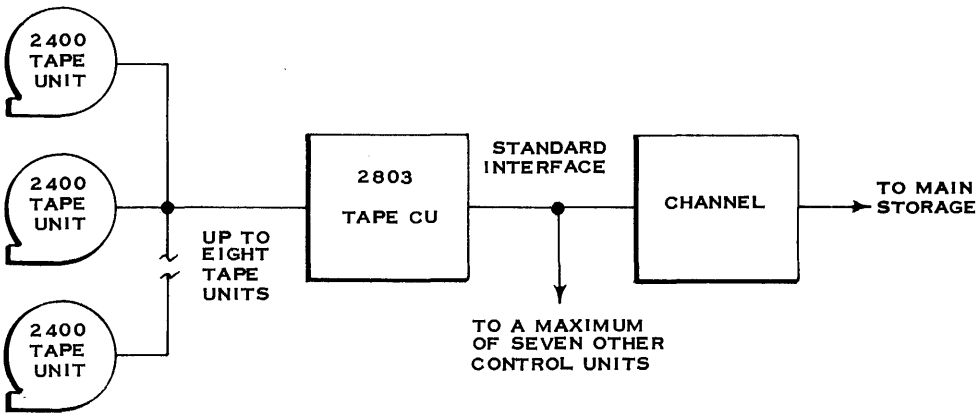
standard interface



Circle the line (A, B or C) that represents the standard interface cable.

B

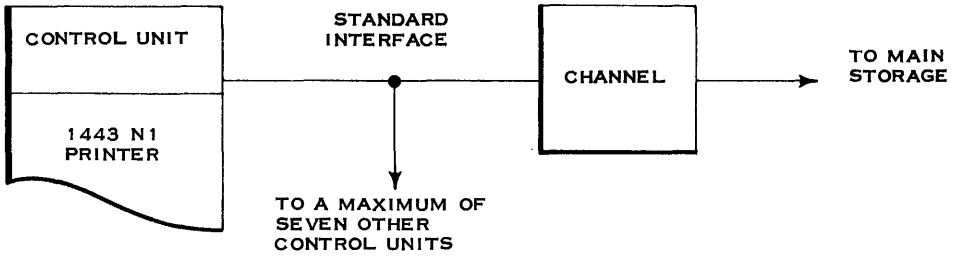
Some control units can control more than one I/O device. The 2803 Tape CU is such an example. It can control up to eight tape units of the 2400 series.



Controls units can be housed external to or built into the I/O devices. The 2803 Tape CU is _____ (internal/external) and can control up to eight tape units.

---

external



The 1443 N1 printer has an _____ (internal/external) control unit which can control only one printer.

---

internal

Two main types of channels are in use with System/360. They are: _____ _____

---

multiplexor selector

On a selector channel, one I/O device transmits an entire record over the standard interface. This is done a byte at a time, and no other I/O device can be transmitting data over the same channel during this time. This type of operation is known as _____ mode.

---

burst

Selector channels, which operate only in burst mode, are designed to operate with high speed I/O devices such as tape units or buffered I/O devices. By a buffered I/O device, we mean one whose control unit contains storage space for an entire record. The buffer allows a high speed data transfer over the channel while the data transfer between the buffer and I/O device may be comparatively slow. During the transfer between the CU buffer and the I/O device, the channel would be free to operate with another I/O device.

Another note concerning selector channels is this: Although a selector channel can sustain only one I/O operation at a time, simultaneous operations can be had with two or more selector channels. Buffered I/O devices are also used with a multiplexor channel since they can operate in multiplex mode.

A multiplexor channel usually operates in _____ mode. However, a multiplexor channel can also operate in burst mode. That is, if a read operation has been initiated for an I/O device, another I/O operation cannot be started until the first one is completed.

---

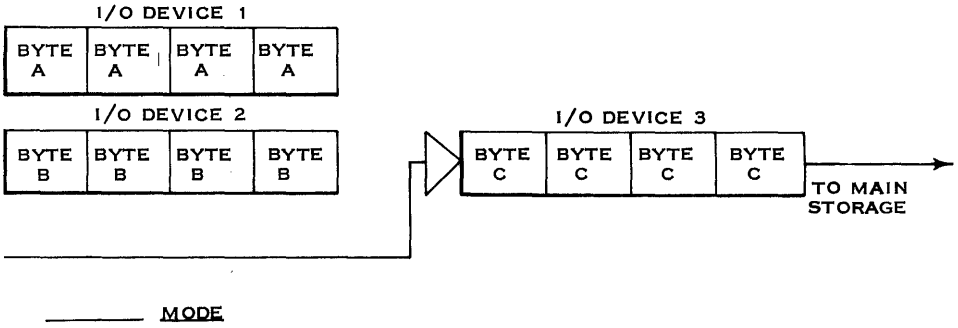
multiplex

When a multiplexor channel is operating in multiplex mode, a second I/O operation _____ (can/cannot) be initiated before the first one is completed.

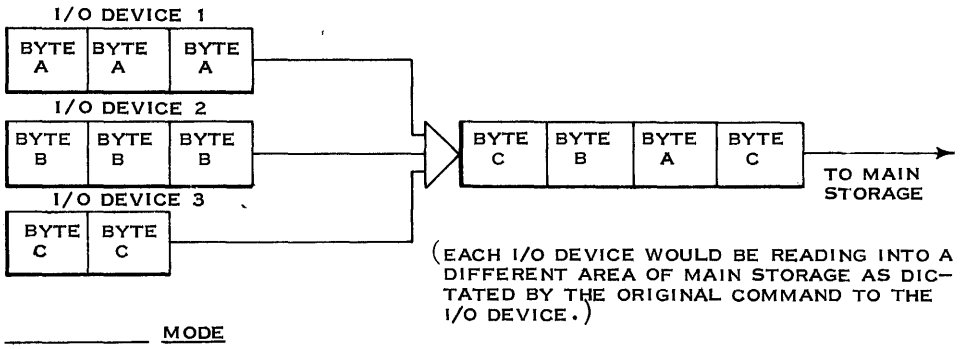
---

can

The two different channel modes can be seen below. Write in the correct title (multiplex or burst) for each illustration.



_____ MODE



_____ MODE

Upper illustration is burst mode.
Lower illustration is multiplex mode.

Go to page 119 and remove the page from the book. The page is a tear-out page and will be used as reference material for the rest of the book.

Let's take a minute to get some idea of the over-all I/O operation and how programming controls it.

Use the simplified program on tear-out page 119 for the following frames.

The problem program, supervisor program and I/O c_____ are written by the programmer.

---

commands

The problem program and supervisor program are composed of i_____

The I/O commands are called channel command words and are abbreviated __ __ __.

---

instructions
CCW

The computer system is controlled by instructions. The I/O devices are controlled by __ __ __s.

CCW

When the problem program reaches a point where an I/O operation is necessary, a "_____ _____" instruction is executed.

"supervisor call"

Control of the system passes (via an interrupt) to a portion of the _____ program, where an I/O handling routine is executed.

One of the instructions in this program is the "_____ ____" instruction.

---

supervisor
"start I/O"

Execution of the "start I/O" instruction causes the proper c_____ (CCW) to be sent to the channel and eventually to the I/O device.

---

command

As you go through the following frames, refer to the illustration on the tear-out page. It will help you maintain an over-all view of the I/O operation.

As was stated earlier, the function of the channel is to process or control input-output operations. This leaves the CPU free to process the data in main storage. To allow the overlapping of I/O operations with processing of stored data, the channel logically must have the necessary registers and control circuitry to do the following:

1. Fetch and execute the I/O commands from main storage.
2. Detect error conditions that occur during channel operations.
3. Send and receive signals from the I/O devices over the standard interface.
4. Store and access data from the proper locations in main storage.

In some models of System/360, the channels do not contain all of the circuitry necessary to be completely independent of CPU. The channel instead has to "borrow" CPU circuitry when needed. Of course, this means that the CPU would have to stop processing momentarily until the channel "returns" the circuitry. The amount of "borrowing" will vary from model to model of System/360. In no way should this alter our concept of a channel. To allow overlapping of I/O and processing, the channel logically consists of the registers and circuitry necessary to control an I/O operation. The lesser the amount of "borrowing" from CPU, the greater will be the effective overlapping.

Logically, then, we can consider a channel as:

1. A set of circuitry to support input-output operations.
2. The control information to sustain one operation on a specific I/O unit.

The control information to sustain one I/O operation is called a Unit Control Word. Much of the information in the unit control word comes from the original I/O command. Refer to the illustration on tear-out page 119.

A selector channel can sustain only one I/O operation at a time, it consists of a set of circuitry (including channel registers) and one u_____ c_____ w_____.

A multiplexor channel can sustain many I/O operations simultaneously. A multiplexor channel would then consist of a set of circuitry (including channel registers) and many _____ _____ _____.

---

unit control word
unit control words

The control information to sustain one I/O operation on a channel is called a _____ _____ _____.

---

unit control word

A channel consists of a set of circuitry to support input-output operations and at least one _____ _____ _____.

---

unit control word

A unit control word is considered a sub-channel. A multiplexor channel can be thought of then as a set of circuitry to support input-output operations and many UCWs or s____ - c_____.

---

sub-channels

A selector channel would contain only one _____.

---

sub-channel or unit control word. These two terms are used synonymously.

Since a selector channel operates in burst mode, its sub-channel (UCW) may be stored in its circuitry for the entire operation.

A multiplexor channel normally operates in multiplex mode. However, only one I/O device is transmitting data through the channel at any one point in time. As a result, the multiplexor channel needs only one UCW at a time. Refer to the illustration on tear-out page 119.

The UCWs (sub-channels) that make up the multiplexor channel are kept in a physical area of the main storage unit known as b_____ storage.

---

bump

A multiplexor channel with 128 sub-channels would need enough bump storage to hold _____ _____.

---

128 UCWs

The number of sub-channels available to the multiplexor channel may vary from model to model of System/360. To a large extent, it depends on the amount of bump storage available to hold the UCWs. Bump storage availability in turn depends on the size of the main storage unit.

During the remainder of this text, we will consider the multiplexor channel as having 128 UCWs or sub-channels. We have been using the terms UCW and sub-channel interchangeably. Actually, the UCW is the control information while the sub-channel is the area where the UCW is kept.

The following is a description of multiplexor channel operation. Refer to the illustration on tear-out page 119 as you go through the operation.

1. The multiplexor channel circuitry is used on a time-sharing basis by the concurrent I/O operations.

2. For each I/O operation that is started on a multiplexor channel, a UCW is formed, most of which comes from the I/O command. This UCW is then placed in the area of bump storage that corresponds to the address of the I/O unit. (Addressing of I/O units will be covered later.)

3. When an I/O unit wants to use the channel to transmit or receive a data byte, it signals the multiplexor channel via the standard interface.

4. The multiplexor uses the address of the I/O unit to obtain the correct UCW or sub-channel from bump storage.

5. The UCW is placed in the channel registers and used to service the I/O unit.

6. After the I/O unit is serviced, the UCW is placed back in bump storage. The multiplexor channel is now ready to service another (or possibly the same) I/O unit.

At this point you should understand what we mean by the following:

1. Channel
2. Sub-channel (UCW)
3. Multiplexor Channel
4. Selector Channel
5. Burst Mode
6. Multiplex Mode

Notice that the tear-out page 120 shows the format of the controlling words used in I/O operations. The formats are also shown in the Principles of Operation manual.

I/O INSTRUCTIONS

The next concept we would like to get across is that of INSTRUCTIONS versus COMMANDS. By this time, you should understand thoroughly what a System/360 instruction is. System/360 instructions come in five different formats. They are fetched and executed by the Central Processing Unit (CPU). Commands, on the other hand, are concerned solely with I/O operations. As such, they are fetched and executed by the channel.

The CPU executes instructions and the channel executes _____.

commands

An I/O command basically contains the following information:

1. The type of operation such as read or write.
2. The main storage address of the data.
3. The number or count of data bytes to be read or written.

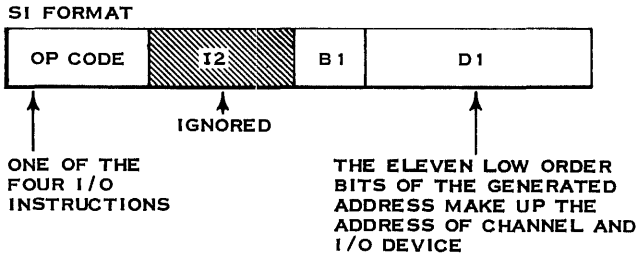
There is other information in an I/O command as well. We will examine an I/O command more thoroughly later on in this text. The main thought right now is to have a general idea of its contents and the fact that I/O commands are executed in the channels. Notice that the I/O command does not tell the channel which I/O to operate.

It is fine to say that the channel executes commands. But the channel still has to be told when to start an I/O operation and with which I/O device to operate. This is still handled by a CPU instruction. There are four I/O instructions:

1. Start I/O
2. Halt I/O
3. Test I/O
4. Test Channel

These four instructions are privileged operations and may be executed only when the system is in supervisor state (PSW bit 15 is set to 0). These instructions are in the regular sequence of instructions in a supervisor program and use the SI format. The CPU would fetch an I/O instruction and notify the proper channel that an operation is desired on a particular I/O device. The CPU would then continue processing more instructions while the channel fetches and executes a command on that I/O unit.

Let's examine the makeup of these privileged I/O instructions and see how they address the desired channel and I/O device.



As can be seen above, the I2 field of an I/O instruction is _____.

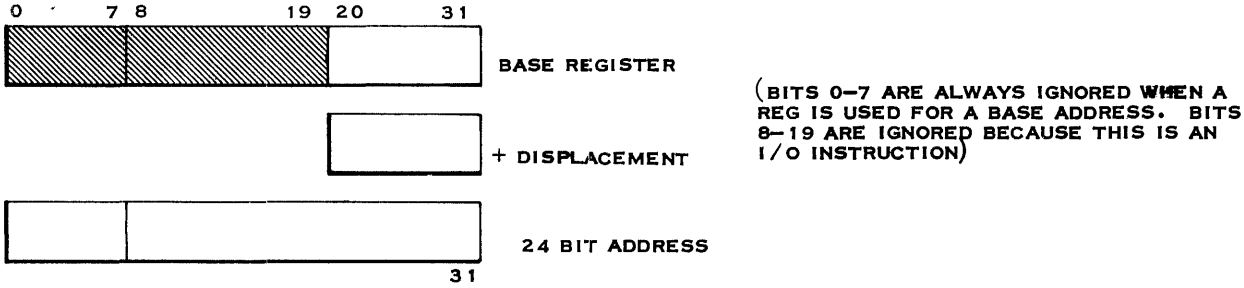
---

ignored

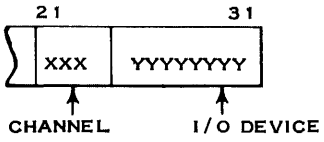
The B1 and D1 fields of an I/O instruction are used to generate an address as usual. However, instead of using it to address main storage, the eleven low-order bits become the address of the _____ and _____ _____.

---

channel,
I/O device (as seen below)



Bits 21-31 of the generated address are used to select channel and I/O device as follows:



As can be seen, three bits are used to select a channel. The channel addresses are as follows:

000	Multiplexor Channel
001	Selector Channel 1
010	Selector Channel 2
011	Selector Channel 3
100	Selector Channel 4
101	Selector Channel 5
110	Selector Channel 6
111	Invalid Channel Address

START I/O

9C	00	0	800	IN HEX

Given the above "start I/O" instruction, which channel is being addressed? _____

Multiplexor channel as shown below:

The generated "hex" address is 000800

Binary → 1000 0000 0000

Channel Address — Address of I/O unit

START I / O

9C	00	0	5FF

Given the above "start I/O" instruction, which channel is being addressed? _____

Selector channel 5

START I/O

9C	00	1	000	REGISTER 1	FFFFFC0F

Given the above "start I/O" instruction, which channel is being addressed? _____

Selector channel 4 as seen below:

C O F

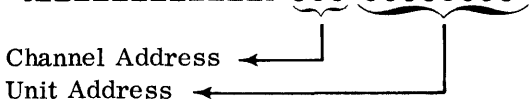
1100 0000 1111

Channel Address — UA (Unit Address)

As can be seen from the channel addressing scheme, seven different channels can be addressed: the multiplexor channel and selector channels 1-6. Refer to the illustration on tear-out page 119. A System/360 does not necessarily have all these channels. This will vary from model to model. The main point is to be able to address the available channels.

---

24 bit generated address - XXXXXXXXXXXXXX CCC UUUUUUUU



Of the eleven bits used for I/O addressing, the three high-order bits are the _____ address. The remaining eight bits are called the _____ address (abbreviated UA).

---

channel
unit

The low-order eight bits of the generated address are used to select the particular I/O unit on the addressed channel. These bits are referred to as the _____ _____. The address has eight bits. Theoretically, then, how many I/O units may be addressed on one channel? _____

---

unit address
256

The actual number of I/O devices on a channel will vary depending on such conditions as the number of I/O units that use the same control unit. The final limiting factor would be the physical restriction of how many control units can be attached to the standard interface.

For those devices that do not share a control unit (such as a 1443 N1 printer), any 8-bit unit address can be used, such as 00001000. An I/O device that must share a control unit with other devices presents a need for a further break-down of the 8-bit unit address. A typical example is a 2401 tape unit that must share its 2803 tape control unit with seven other tape units. For I/O devices that share a control unit the unit address may be divided this way:

Control unit address

Address of one of seven I/O devices

The unit address of the eight devices that share a common control unit would have _____ (the same/different) 5 high-order bits.

---

the same

If 00001000 is the unit address of tape unit 0, what is the unit address of tape unit 7 on the same control unit? _____

00001111

If 00001000 is the unit address (UA) of a tape unit, can 00001110 be the UA of a 1443 N1 Printer on the same channel? _____

No; because the 5 high-order bits of 00001 would be selecting the tape control unit. The low-order bits would then select tape unit 6.

If 00001000 is the unit address of a 1443 N1 Printer, can 00001001 be the unit address of a magnetic tape unit on a different channel? _____

Yes, as long as they are on different channels.

One other point you can derive from the preceding frames is that an I/O device can have any unit address as long as it doesn't conflict with other devices on the same channel. This differs from systems other than System/360. On other systems a particular number was usually reserved for a particular type of I/O device, such as card reader.

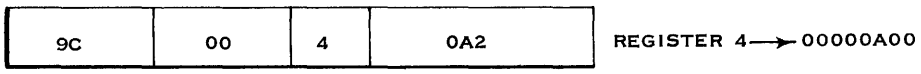
On System/360, these unit addresses are wired into a control unit's and/or I/O device's circuitry at installation time. As such, they cannot be changed except by re-wiring (or re-cabling) the machine.

Can an operator change the number of a tape unit from 0 to 7? _____

No

You previously saw that for I/O devices that share a control unit, the unit address is broken down into two groups of bits. The control unit uses 5 bits and the I/O device uses 3 bits. This is not a hard-and-fast rule. It will depend on the number of devices that share a control unit. If sixteen devices share one control unit, the breakdown will be 4 and 4: 4 bits for the control unit and 4 bits for devices 0-15.

Given the following "start I/O" instruction:



a. What is the second byte of the "start I/O" instruction used for? _____

b. On what channel will an operation be started? _____

c. What is the unit address of the I/O device that will be operated? _____

---

a. The 2nd byte of the "start I/O" instruction is the I2 field which is ignored.
b. Selector channel 2; The generated address is a "hex" 000AA2.
c. The unit address is A2 or 10100010.

You have just seen how the "start I/O" instruction furnishes the addresses of the desired channel and I/O unit. You have not yet seen how the sub-channel (UCWs) on a multiplexor channel are addressed. In this text, we will consider the multiplexor channel as having 128 sub-channels. Refer to the illustration on tear-out page 119.

A multiplexor channel with 128 sub-channels will have ____ _____ in bump storage.

---

128 UCWs

The 128 UCWs in bump storage are numbered 0-127. The UCW number corresponds directly with the unit address of the I/O unit. An I/O unit with a UA of 00001000 will use sub-channel # ____.

8; The number of the I/O unit was 8 and it will use UCW #8.

An I/O unit with a unit address of 01111111 will use UCW or sub-channel # _____.

127

Since the multiplexor channel uses the unit address of an I/O unit to address bump storage, it is assured of obtaining the correct UCW. However, there are situations in which each I/O unit does not need its own UCW.

Such a situation is that of a tape control unit with eight magnetic tape units. Only one of the eight tape units can be reading or writing at the same time. So why tie up 8 UCWs (sub-channels) when only one is needed? Why not have the 8 tape units share the same UCW?

The multiplexor channel has a way out of this situation. If the high-order bit of the unit address is a 1, this will indicate to the multiplexor channel that the I/O unit is using a shared UCW (sub-channel).

Which of the following unit addresses indicate I/O units which do <u>not</u> share a sub-channel (UCW) with other units? (Circle one or more)

a. 10001111
b. 01101101
c. 10011011
d. 01111111

---

b., d.; Since the high-order bit of the UA is a zero, the multiplexor channel knows that the I/O units (b, d) have their own UCWs which correspond directly with their unit addresses.

The I/O unit with a UA of 01101101 uses UCW #109.

The I/O unit with a UA of 01111111 uses UCW #127.

Which of the following unit addresses use a shared sub-channel? (Circle one)

a. 01110001
b. 01010101
c. 11111111
d. 00000000

---

c; This was the only UA with a high-order 1 bit.

When the unit address has a high-order 1 bit, its address does not directly relate to a UCW. Instead bits 1-3 of the UA indicate the UCW number.

Unit Address 10010111

Uses UCW #1 00000001

Given a unit address of 11111111, which UCW (sub-channel) will be used by the multiplexor channel? _____

UCW #7 as seen below.

Unit Address 11111111

Uses UCW #7 00000111

Given a unit address of 11111000, which sub-channel will be used?

_____

UCW #7

Unit addresses 11111111 and 11111000 both use the same UCW or sub-channel. This makes sense if we again look at the addressing of I/O devices on the same control unit.

For instance, if the following is a tape unit address.

11111 111

Address of tape control unit — Tape unit #7

The address of tape unit #0 on the same tape control unit would be _____.

11111000

Since only one tape unit can be reading or writing with the same control unit, only one sub-channel is needed. After all the purpose of multiple sub-channels on a multiplexor channel is to sustain simultaneous I/O operations. By assigning unit addresses beginning with 1XXXXXXX to I/O devices that share the same control unit, only one UCW is used up rather than the total number of I/O devices sharing the same control unit.

It is not absolutely necessary that magnetic tape units (or other such shared devices) be assigned unit addresses beginning with 1 when they are attached to the multiplexor channel. It is just a matter of being economical with UCWs or sub-channels. Why use up eight when one will do?

Can a magnetic tape unit attached to a multiplexor channel be assigned a unit address of 01000000? _____

Yes; It would then use sub-channel or UCW #64. The other seven tape units (1-7) on the same control unit would use up UCWs #65-71. This would be a waste of sub-channels.

The first eight UCWs (#0-7) can be shared sub-channels. For instance:

A unit address of 10000111 would use UCW #0.
A unit address of 10000001 would also use UCW #0.

A unit address of 11110000 would use UCW #7.
A unit address of 11110111 would also use UCW #7.

Unit addresses of 11100000 and 11100001 would both use UCW# _____.

6

If a magnetic tape unit on the multiplexor channel has a unit address of 10010111, can a 1443 N1 Printer on the multiplexor channel be assigned a unit address of 00000001? ____

Yes; It can be. However, if this were done, both units would be using UCW #1. Simultaneous operations with these two devices could not be attempted. So the answer is yes, they can be but no, they shouldn't be assigned these conflicting unit addresses.

If the 1st eight UCWs are used for shared sub-channels, the unit addresses assigned to I/O devices which do not share UCWs should begin with the following UA _____.

00001000

If only the 1st four UCWs are used for shared sub-channels, the unit addresses of I/O devices which do not share UCWs may begin at _____ without any conflict.

00000100

At this point you should know that:

1. There are 4 I/O instructions.
2. The I/O instructions are privileged operations and use the SI format.
3. The generated effective storage address (B1 and D1) supplies the address of the channel and the I/O unit.

You should also have a thorough understanding of how to address:

1. Channels
2. Sub-channels (UCWs)
3. I/O units

You should know that the channel will execute a command. The I/O command is used to put information in the UCW such as:

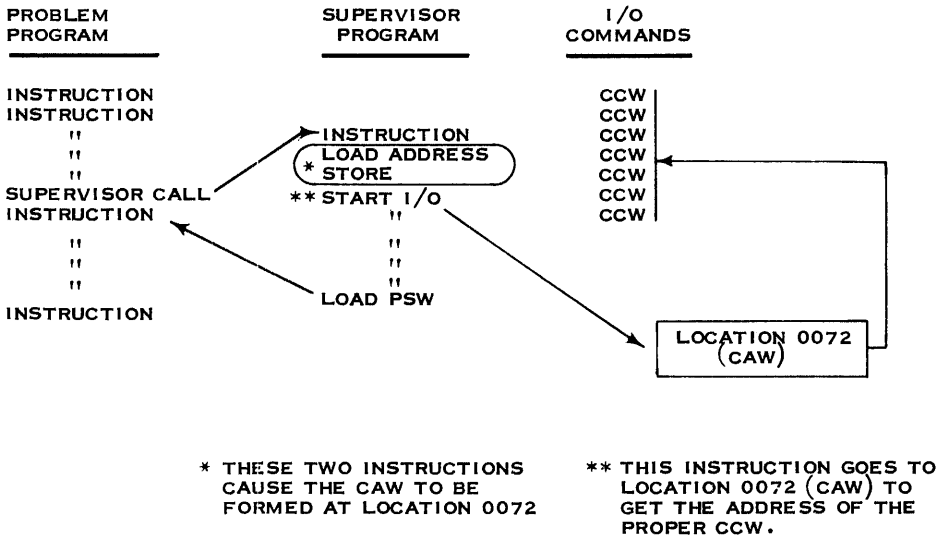
1. Type of operation, such as read or write.
2. Main storage address of the I/O data.
3. Count or number of data bytes.

CHANNEL ADDRESS WORD - CAW

You know that the "start I/O" instruction is used to tell a channel to start an I/O operation on a specific I/O unit. You know that as a result of the "start I/O" instruction, the channel will get an I/O command from main storage and execute it. A UCW is formed using information in the I/O command and the UCW is used to sustain an I/O operation on the addressed I/O unit. Refer to the illustration on tear-out page 119.

What you don't know is how the channel knows where the I/O command is located in main storage. This is done by use of a word in locations 0072-0075 of main storage. This word is called the Channel Address Word (CAW) and must be prepared by the person who writes the program. The instructions that form the CAW precede the I/O instruction.

Each I/O device that is used in a program will be given a list of one or more commands. When the programmer desires an operation on a particular I/O device, he will place the address of the first I/O command for that unit in the CAW at location 0072.



* THESE TWO INSTRUCTIONS CAUSE THE CAW TO BE FORMED AT LOCATION 0072

** THIS INSTRUCTION GOES TO LOCATION 0072 (CAW) TO GET THE ADDRESS OF THE PROPER CCW.

Prior to writing a "start I/O" instruction, the programmer should write instructions that will place the address of the 1st I/O command in the _____ at location 0072.

CAW

CAW is short for _____ _____ _____.

Channel Address Word

When a channel is started by use of a "start I/O" instruction, the address in the _____ at location 0072 is used to get the first _____.

CAW
I/O command

Before executing a "start I/O" instruction, the programmer must set up the address of the particular CCW that is to be used, in the _____.

CAW

Look at the CAW in the illustration on tear-out page 119.

The storage protection feature on a System/360 is designed to protect main storage area against I/O operation as well as CPU operation.

During a CPU operation, a store cycle will be allowed if the PSW protection key is zero. It will also be allowed if the protection key and _____ key match.

---

storage

A storage key of 0-15 is given to each block of _____ bytes.

2048

If the two keys do not match and the PSW key is not zero, a _____ exception will result in a _____ interrupt.

---

protection
program

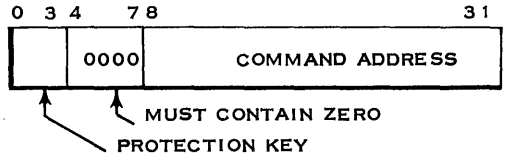
Channel operations are sustained by the Unit Control Word. The UCW must have a field similar to the protection key in the PSW. The information for this UCW field will come from the CAW.

Besides supplying the address of the first I/O command, the channel address word will also supply a _____ _____ for the UCW.

---

protection key

The following shows the CAW:



As can be seen above, bits 0-3 of the CAW contain the _____ ____ while bits 8-31 contain the _____ of the first I/O command.

---

protection key
address

The channel address word is a _____ (halfword/word/doubleword and occupies ___ bytes of main storage.

---

word
4

The command address from the CAW will be placed in the UCW and used in a manner similar to the instruction address portion of the PSW. All I/O commands are a doubleword in length. As a result the address in the CAW must contain three low-order zero bits. That is, the address must be divisible by eight.

Indicate the source (CAW or "start I/O" instruction) of the following:

a. Unit Address _____
b. 1st Command Address _____
c. Channel Address _____
d. Protection Key _____

---

a. "start I/O"
b. CAW
c. "start I/O"
d. CAW

The following information is placed in the Unit Control Word used to sustain the particular information. The remainder of the UCW will contain information from the I/O command.

Unit Address
Command Address
Protection Key

In review:

1. CPU will fetch a "start I/O" instruction. It will tell the addressed channel that an I/O operation is desired and will furnish the channel with the unit address of the I/O device.

2. The word at location 0072, called the CAW, is then sent to the addressed channel. The CAW contains the protection key to be used by the channel as well as the address of the 1st I/O command.

3. After the channel gets the I/O command and initiates the operation, it disconnects from CPU. CPU is then free to go on to the next instruction (the one after "start I/O").

Before examining the contents of the I/O command, let's see if you can answer the following:

Move Characters ——→ MVC 0072 (4, 0), 2048 (0)
Start I/O ——→ SIO 17 (1), 0

Locations 2048-2051 ——→ A0000F00
Register 1 ——→ 00000100

a. What channel is being used? _____
b. What is the Unit Address? (in binary) _____
c. What is the address (in hex) of the 1st I/O command? _____
d. What protection key will be used for this operation? Show binary bit structure. _____

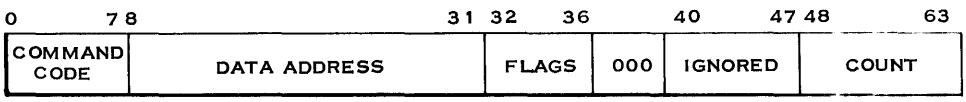
CHANNEL COMMAND WORD-CCW

a. Selector Channel 1
b. 00010001 (binary)
c. 000F00 (hex)
d. 1010 (binary)

Let's now examine the composition of an I/O command. An I/O command is a doubleword in length and is called a Channel Command Word. Refer to the tear-out illustration on page 119.

The address of the 1st CCW is contained in the _____.

CAW



THE CHANNEL COMMAND WORD

The command code tells the channel what the specific operation is (such as read or write). It is located in bits ___ through ___ of the doubleword called _____ _____ _____.

The command code is ___ (1/2) byte(s) long and is also referred to as the command byte.

0, 7
channel command word
1

The channel can execute six commands:

1. Read
2. Read Backward
3. Write
4. Control
5. Sense
6. Transfer in Channel

The bit structure of the command code specifies which of the commands the channel will execute. The bit structure depends to some extent on the I/O device being used. Later in this text, we will be discussing some of the I/O devices. So we will hold off for now any further discussion of the command code. For now, it is sufficient to say that the command code specifies the operation such as read or write. Just like the Op Code of an instruction, the _____ code is the first byte of a CCW.

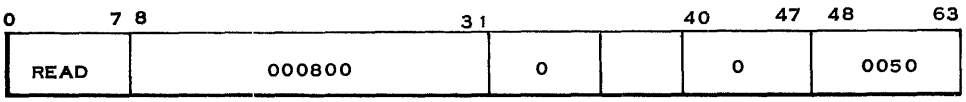
command

Bits 8-31 of the CCW are the _____ _____. This is the starting address in main storage for the I/O data. If the command byte specified a read operation, the 1st byte read would go into this location.

data address

The length of the I/O data area is given in bits 48-63 of the CCW. This area is called the c_____ field. The count field gives the total number of data bytes, including the first one.

count



CCW IN HEX

Assume the command code specifies a read operation.

Given the above CCW, a total of ___ bytes will be read into locations _____ through _____.

80
2048
2127

Bits 40-47 of the CCW are _____ while bits 37-39 must contain _____. Bits 32-36 contain ____ bits. The flag bits are used to further specify the channel operation. We will be discussing the flag bits in more detail later.

---

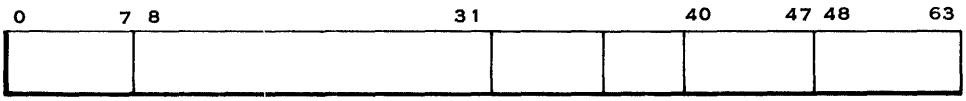
ignored
zeroes
flag

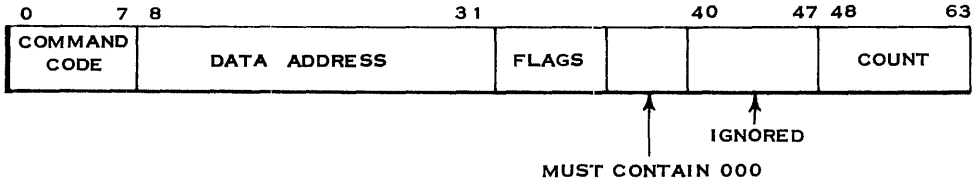
The flag bits are used to:

1. Indicate that more CCWs are to be used to either:
   a. Do consecutive I/O operations on the same I/O unit. This is known as "command chaining."
   b. Read or write data into or from non-adjacent areas of main storage. This is known as "chaining data."
2. Skip over an area of a data record.
3. Suppress recognition of incorrect length records.
4. Cause an I/O interrupt as soon as the next CCW is fetched.

NOTE: If more than one CCW is to be used, the CCWs are in consecutive locations of main storage.

Label the fields of the following CCW:





Where are the CCWs located? _____

In main storage

Who generates the CCWs? The machine or the programmer?

_____

The programmer

How many CCWs are needed? _____

A CCW is needed for each I/O unit used in the program. When "command chaining" or "data chaining", two or more CCWs are needed for an I/O unit.

When an I/O operation is started, how does the channel know where the programmer's CCWs are located? _____

The programmer must place the address of the 1st CCW to be used in the operation in the CAW at location 0072. He must do this prior to the "start I/O" instruction. The channel then uses the CAW to get its first CCW.

When do CPU and the channel disconnect on a "start I/O" instruction?

After the channel has the first CCW and has initiated the operation. The condition code is then set to indicate the operation was started with the I/O unit.

CHANNEL STATUS WORD - CSW - BASIC FUNCTION

The information in the CCW (as well as that in the CAW and the unit address from the "start I/O instruction) is placed in the UCW. The unit control word is then used to control the I/O operation. As a result, the CCW (and CAW) only have to be accessed once and are left unchanged in main storage.

The UCW would be modified in the course of the I/O operation. The modification of the UCW would consist mainly of updating the data and command addresses and reducing the count field by one for each data byte.

At the end of the I/O operation on the channel, CPU would be signaled via an I/O interrupt, assuming that the system mask field in the PSW allows the interrupt. At this time much of the information in the unit control word is then used to form a Channel Status Word which is placed in location 0064 of main storage. The channel status word can then be examined by the I/O interrupt program. Refer to the tear-out illustration on page 119.

How does CPU know when the I/O operation on the channel is finished?

_____

_____

_____

There will be an I/O interrupt (systems mask set to allow). In addition to the usual switching of PSWs, the channel will form a channel status word and put it in location 0064 of main storage.

You should be familiar with the following abbreviations. What do they mean?

a. CPU _____
b. ALU _____
c. UA _____
d. CAW _____
e. CCW _____
f. CSW _____
g. UCW _____
h. PSW _____

---

a. Central Processing Unit
b. Arithmetic and Logic Unit
c. Unit Address
d. Channel Address Word
e. Channel Command Word
f. Channel Status Word
g. Unit Control Word
h. Program Status Word

You have covered much ground so far in your study of I/O operations. To summarize what you have learned, briefly study the following areas in your Principles of Operation manual.

Do not read any other areas at this time! Most of the material in the specified areas should be familiar to you. Do not be alarmed if you read something that you do not understand. As we continue on with this text, these points should clear up.

Study:

Input/Output Operations
Attachment of Input/Output Devices
Input/Output Devices
Control Units
Channels
Modes of Operation
Types of Channels
System Operation
Compatibility of Operation
Control of Input/Output Devices
Input/Output Device Addressing
Instruction Formats
Instructions
Start I/O
Execution of Input/Output Operations
Blocking of Data
Channel Address Words
Channel Command Word
Command Code

Given the following information: (use tear-out page 120 as reference)

Locations 2048 - 2051 ⟶ E0000F00
Locations 3840-3847 ⟶ 02000F0800000064 } In hex

Instruction 1 MVC 0072 (4, 0), 2048 (0)
Instruction 2 SIO 128 (0), 0

a. What channel is being used? _____
b. What is the unit address (in binary)? _____
c. What is the six digit "hex" CCW address? _____
d. Assuming a read command, how many bytes will be read in main storage? _____
e. These bytes will be read into locations _____ through _____.
f. What protection key will be used by the channel? _____
g. What should the storage key of the I/O data area be? _____
h. Show the binary bit structure of the command code. _____

---

a. Multiplexor, b. 10000000 } B1 = 0 D1 = 128 or 10000000

c. 000F00; This was placed in locations 0073-0075 by the "move character" instruction.

d. 100 bytes; The count field of the CCW shows a "hex" 64.

e. 3848-3947; The beginning "hex" address was 000F08, which is location 3848.

f. E or 14; This was placed in the high order of location 0072 by the "move characters" instruction.

g. E or 14; If it isn't, a protection violation will be recognized.

h. 00000010

Arrange the following according to the sequence in which they are used.

CSW, CAW, UCW, "start I/O", CCW

1. _____
2. _____
3. _____
4. _____
5. _____

---

1. "start I/O"
2. *CAW
3. CCW
4. UCW
5. CSW

* This is the time when the CAW is used by the channel. However, you should note that the CAW in location 0072 must be set up prior to executing the "start I/O" instruction.

Complete the numbering of the following events according to the sequence in which they happen.

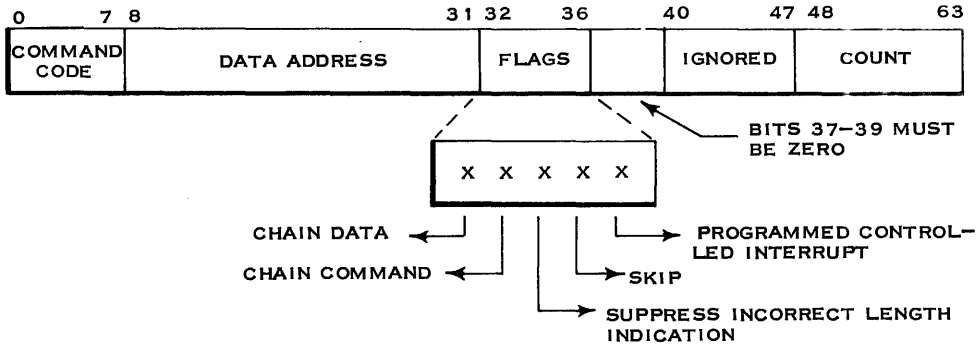
2nd	CPU fetches "start I/O" instruction
_____	Channel gets CCW
_____	Channel forms UCW
1st	CAW is placed in location 0072
_____	CSW is formed
_____	CAW is sent to the channel
_____	I/O Interrupt
_____	CPU fetches instruction following "start I/O"
_____	Data transmission between I/O device and main storage.

2
4
5
1
8*
3
9
6
7

* The CSW may be formed and stored in location 0064 prior to terminating the "start I/O" instruction. If this is done, the I/O operation wasn't started for some particular reason and the condition code will be set accordingly. This will be covered later.

FLAG BITS - CCW

Let's now examine the meaning of the flag bits in the channel command word (CCW).



The first flag bit we will examine is CCW bit 32. This is the _____ _____ flag. CDA is the abbreviation usually used for "chain data".

If the CDA flag bit is set to 1, the data address and count in the next sequential CCW is also to be used in storing a data record. Both CCWs will pertain to the same I/O record.

Data chaining permits the reading or writing of an I/O record from different areas of main storage. This is often referred to as Scatter Read-Write.

---

chain data

Suppose it were desired to read columns 1-30 of an IBM card into locations 2048-2077 and columns 31-80 into locations 3840-3889. This can be done with two CCWs. The first CCW would have its CDA flag bit set to 1 as shown below:

1ST CCW	8	31	IN HEX	
02	000800	80	00	001E

2ND CCW	IN HEX			
00	000F00	00	00	0032

As can be seen above, the 1st CCW will cause ____ bytes to read into storage starting at location _____.

30
2048

Since bit position 32 of the 1st CCW is set to 1, the channel knows that it is "chaining _____".

---

data

The 1st CCW was used to read thirty bytes into main storage. Because its CDA flag bit was set to 1, the 2nd CCW was then fetched. It was used to read _____ bytes into main storage starting at location _____.

50
3840

When "chaining data", the command bytes of successive CCWs are ignored. Only the 1st CCWs command byte is used. It is important to note that "chaining data" pertains to only one I/O operation or data record. This could be one IBM card or one tape record or one line of print and so forth.

If the CDA flag bit is 0, the CCW is the last one used for the operation. In our previous example, the CDA flag bit of the 2nd CCW was set to ___.

0

Suppose you desired to read a 200 character tape record into 4 different areas of main storage. How many CCWs would be needed? ____

4

Of these 4 CCWs, which one(s) would have the CDA flag bit set?

_____

---

all but the last one

Would the command bytes of all 4 CCWs have to specify a read operation?

_____

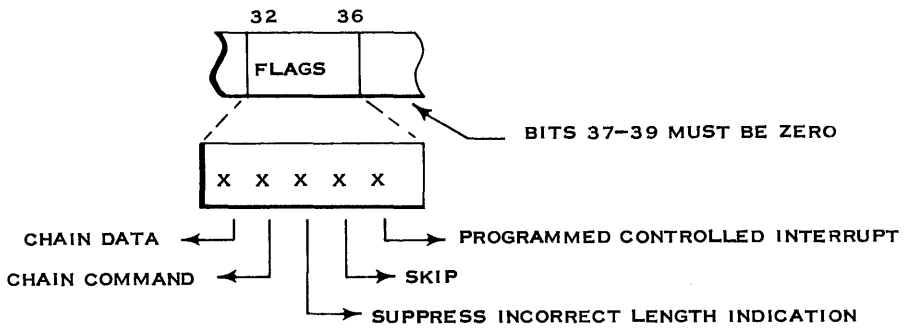
No; Only the 1st CCW has to specify a read operation. The remaining command bytes are ignored.

Assume that the 1st fifty characters of the record are to be read into main storage starting at location 2048, the next fifty at 2304, the next fifty at 2560, and the last fifty starting at 2816. Using a command byte of "hex" 02, write the list of necessary CCWs.

0200080080000032
00090080000032 in
000A0080000032 hex
000B0000000032

The ability to "chain data" is a very flexible feature of the I/O channels. It can be used to scatter read or write to or from different locations in main storage.

Where two or more data records are blocked together and written as one tape record, they can be de-blocked by "chaining data" and using a different CCW for each data record. When one of the records is to be processed, its data address (from the CCW) could be loaded into a base register and used to address the data fields. When the next data record (from the same tape record) is to be processed, the data address from its CCW can then be placed into a base register.



The data chaining feature can also be used to read selected portions of an I/O record into main storage. Notice that we said "into main storage". The I/O device always reads an entire record. That is, for one read command, a card reader will read an entire card or a tape unit will read from one inter-record gap to the next. However, the data chaining feature could be used to put only a portion of the record into main storage. To do this, the CDA flag is used along with bit 35 of the CCW which is called the _____ flag.

---

skip

Columns 51-80 of an IBM card are to be read into locations 2048-2077. The card reader will read all 80 columns of information and attempt to put 80 bytes of data into main storage. The channel will need to have 2 CCWs.

1ST CCW

02	000800	90	00	0032

2ND CCW

02	000800	00	00	001E

The 1st CCW has both the _____ and the _____ flags set to 1.

CDA
skip

Because the skip flag is set, the 1st CCW is not used to put data in main storage. The count field will cause ____ bytes to be ignored.

50

Because the CDA flag is set, the second CCW will be fetched after the first fifty bytes have been skipped.

The 2nd CCW will be the last one used for this operation because its _____ flag is zero.

CDA

The 2nd CCW will be used to put data into main storage because its _____ flag is zero.

---

skip — The 2nd CCW will be used to put columns ____ through ____ of the card into storage locations _____ through _____.

51
80
2048
2087

Given the following:

Location 2048 ⟶ 0200090080000010
0000090080000010
0000090090000010
00000A0080000010
00000A0010000010

Location 3840 ⟶ 10000800

Instruction 1	MVC	0072 (4, 0), 3840 (0)
Instruction 2	SIO	7 (0), 0

a. What channel is being used? _____
b. Assuming a card reader is being used, what is its unit address (in binary)? _____
c. Assuming a read command byte, how many CCWs will be used? _____
d. What protection key will be used by the channel for this operation? _____
e. What is the purpose of the MVC instruction? _____
f. How many bytes will be put into main storage by this operation? _____
g. Which card columns will be skipped? _____
h. What is the location of the last CCW used? _____
i. After the operation is finished, which card columns will be in locations 2304-2319? _____
j. After the operation is finished, which card columns will be in locations 2560-2575? _____

---

a. Multiplexor
b. 00000111
c. Five (all but the last one has its CDA flag set)
d. 0001
e. To set up the CAW
f. 48 bytes (32 bytes are skipped)
g. Columns 33-48 and 65-80
h. Location 2080 (the last CCW occupies 2080-2087)
i. Columns 17-32 (columns 1-16 were originally read into these locations)
j. Column 49-64

How does the CPU Program initiate an I/O operation? _____

_____

With a "start I/O" instruction

How does the CPU program know when the channel has finished the I/O operation? _____

By an I/O interrupt

Besides switching PSWs, what else happens on an I/O interrupt?

_____

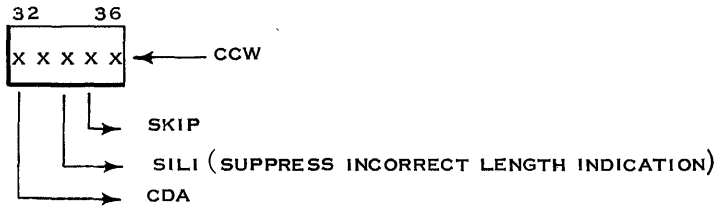
_____

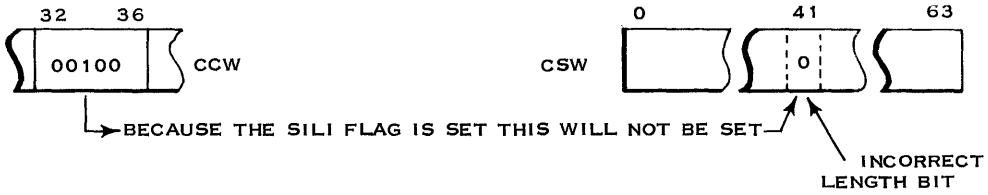
The channel forms a channel status word (CSW) which is stored in location 0064.

One of the bits in the CSW is used to indicate that the number of bytes read did not agree with the count in the CCW. This would be an indication of an incorrect record length.

For example, if a CCW with a count field of 50 were used to read a card, columns 1-50 would be read to main storage and the incorrect length bit in the CSW would be set. Columns 51-80 of the card would be read but would not be put into main storage.

The setting of the incorrect length bit in the CSW can be prevented with the SILI (pronounced Silly) flag in the CCW.

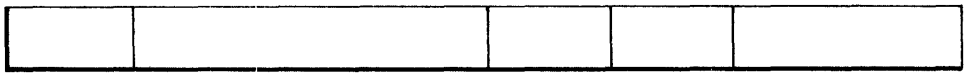


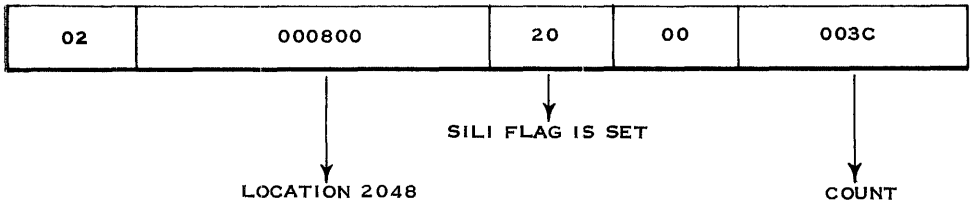


If the SILI flag of the last CCW is set, the incorrect length bit _____ (will/won't) be set when the CSW is stored.

won't

Suppose we wish to read columns 1-60 of a card into locations 2048-2107. We do not want an incorrect length indication. Write (in hex) the necessary CCW (use a command of 02).





Suppose we want to read columns 41-60 into main storage starting at location 2048. Write the necessary two CCWs and suppress the incorrect length indication. Use a command byte of 02.

CCW1 _____
CCW2 _____

CCW1 0200000090000028
CCW2 0000080020000014

In the previous answer, any valid data address could be in the 1st CCW and any command byte could be in the 2nd CCW.

CPU normally receives an I/O interrupt at the end of the I/O operation. However, bit position 36 of the CCW can be used to signal an I/O interrupt prior to the end of the operation. Refer to the CCW format on the back of tear-out page 120. This flag bit is called the PCI or _____ _____ _____.

When a CCW is fetched that has its PCI bit set, CPU will receive an I/O interrupt as soon as it can accept it. This is one way CPU could be notified of the progress of an I/O operation. We will be covering I/O interrupts more thoroughly later on.

---

program controlled interrupt

I/O interrupts normally occur at the end of the operation. An I/O interrupt may occur earlier if the _____ flag bit is set.

PCI (Program controlled interrupt)

Bit position 33 of the CCW is the _____ _____ flag. This bit (called the CC flag), when set to one will cause the next sequential CCW to be used to initiate another operation on the same I/O device.

For example, it is possible to read two cards into main storage as a result of one "start I/O" instruction. To do this requires two CCWs with the CC flag set in the first CCW. This is shown below.

CCW1

02	000F10	40	00	0050

LOCATION 3840

CCW2

02	000F60	00	00	0050

```
MVC   0072 (4,0), 2048 (0) <------ Set up CAW
SIO   0023 (0), 0 <------------- Initiate I/O operation on device
                                 #23 on the Multiplexor Channel
```

Location ⟶ 2048 70 000F00

70 → Key

000F00 → Address of 1st CCW

---

chain command

In the preceding example, the first CCW will initiate a read command. Assuming that device #23 on the multiplexor channel is a card reader, one card will be read into storage locations _____ through _____.

3856
3935

Because the CC flag in the first CCW is set to one, the second CCW will be used to initiate another card read operation. The next card will be read in storage locations _____ through _____.

3936
4015

Note that when chaining data, only one I/O operation occurs, such as reading one card. The data from the one I/O record is then placed in main storage under control of two or more CCWs.

When chaining commands, each CCW is used to control a different I/O operation. The commands that are chained need not be the same. For instance, it is possible to do a write-backspace-read combination with a magnetic tape unit by chaining commands with three CCWs.

When command chaining, an I/O interrupt does not occur at the end of each operation. When the last command has been executed, an I/O interrupt can occur.

2048 ⟶ 02000F0080000032
02000F324000001E
02000F5000000050

Load Address ⟶ LA 7,2048 (0) } ⟶ Set up CAW
Store ⟶ ST 7,0072 (0) }
SIO 260(0), 0 ⟶ Start I/O on device #4 Selector Channel #1

a. Assuming the addressed device is a card reader, how many cards will be read? _____
b. Will an I/O interrupt occur as a result of reading the 1st card? _____
c. What protection key will be used by selector channel #1 for these operations? _____ (You may have to refer to the description of the "load address" instruction in your Principles of Operation manual.)

---

a. Two; The first two CCWs were used to read one card and the data was chained. The third CCW was used to read a second card.
b. No; When command chaining, an I/O interrupt does not usually occur until the last command has been executed.
c. Zero; The "load address" instruction placed 2048 in bits 8-31 of the register and bits 0-7 were made zero.

TRANSFER IN COMMAND

At this time we have not examined the command bytes. This is because the actual makeup of the command byte will depend on the I/O device being used. One of the six commands can be examined at this time because it does not involve an I/O device. This is the transfer in command operation.

If bits 4-7 of the command byte are 1000, a transfer in command is specified. Bits 0-3 and 32-63 of the CCW are ignored.

The transfer in command does for the channel program (list of commands) what the "branch" instruction does for the CPU program (list of instructions). In other words, the TIC (transfer in command) causes a new CCW to be fetched from a non-sequential location in main storage. The data address in the CCW gives the location of the next CCW.

Given the following list of CCWs:

CCW1 0200080080000032 ⟵ Read
CCW2 000008324000001E
CCW3 0800080000000000 ⟵ TIC

a. What is the location of the fourth CCW? _____
b. Was this CCW in main storage at the beginning of the operation? _____

---

a. 2048; In hex this would be 000800.
b. No; The first eight bytes read in under control of CCW1 will be the fourth CCW.

There are two restrictions placed on the use of the TIC:

1. The data address must be divisible by eight since a CCW is a doubleword.
2. The next CCW (the one to which the channel is transferring) must not be another TIC.

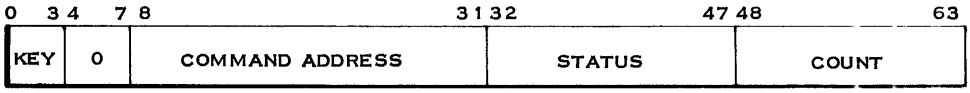
If either of these are violated, the channel operation is terminated. The channel status word stored during the I/O interrupt will indicate that one of these channel errors was detected.

CHANNEL STATUS WORD - CSW

You should now know the contents and functions of the following:

1. Channel Address Word (CAW)
2. Start I/O Instruction (SIO)
3. Channel Command Word (CCW)

You do not yet know the contents of the Channel Status Word (CSW). You should know that it is stored in location 0064 on any I/O interrupt. It's basic function is to let the CPU program know what happened as a result of the I/O operation. Refer to the illustration on tear-out page 119.



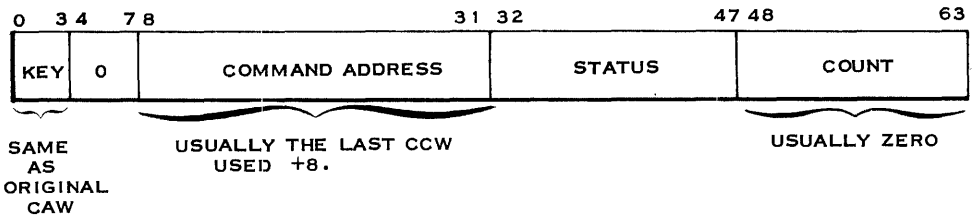
By looking at the first half of the CSW, you can tell that it is basically the same as the CAW that was used at the beginning of the operation. The only difference is that the command address portion will be changed.

In the event of chaining commands or data, this address will be continually updated. When the CSW is stored at I/O interrupt time, this portion of the CSW usually contains the address of the last CCW used + 8. That is, if only one CCW had been used and its location were 2048, the CSW would contain 2056 for the command address portion.

2048 ⟶ 02000F0080000032
02000F324000001E
02000F5000000050

Given the above list of CCWs, what would be in the command address portion of the CSW? Assume normal error free completion of the operation. _____

Location 2072; In hex it would be 000818.



Bits 48-63 of the channel status word (CSW) contain the residual _____ from the last CCW used. Unless the number of bytes read or written did not agree with the count field in the CCW, these bits are usually zero.

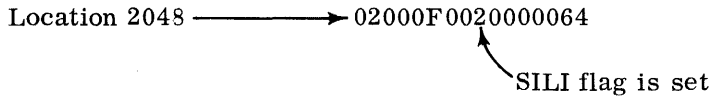
When the number of bytes read or written is less than the number in the count field of the CCW, the count in the CSW will indicate the amount of shortage. This is useful when reading variable length records.

Supposing the records on tape are variable in length but the maximum length will not exceed 100 bytes. A CCW with a count field of 64 (hex) can be used to read these tape records. The count field in the CSW can be subtracted from the count field in the CCW to determine the actual number of bytes in the record.

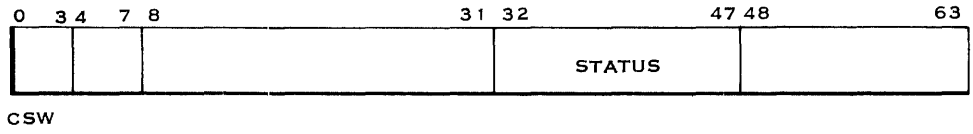
---

count

Given the following, show (in hex) the contents of the CSW which will be placed in location 0064 at the time of the I/O interrupt. Assume that a 96 character tape record is being read. Ignore the status portion of the CSW for now.

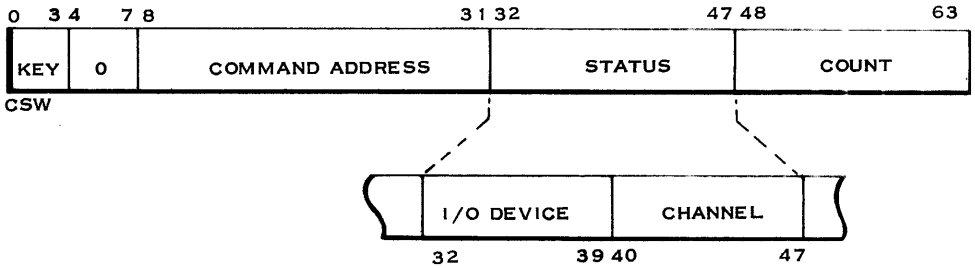



```
LA   7,2048(0)
ST   7,0072(0)
SIO  260(0), 0
```



0	0	000808	STATUS	0004

The hex 64 in the count portion of the CCW indicated that 100 characters should be read. The tape record contained only 96 characters.



Bits 32-47 are the status portion of the CSW. These two bytes include status information from the _____ _____ and the _____.

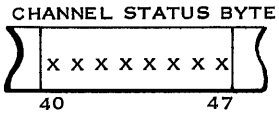
Bits 32-39 contain the status byte from the I/O device. This byte is sent by the I/O device to the channel at the end of the operation. It is transmitted to the channel over the standard interface. Bits 40-47 contain the channel's status byte. Any errors detected by the channel would be indicated in this byte.

I/O device
channel

Let's examine the status portion of the CSW. Refer to the preceding illustration or the CSW format on tear-out page 120. As indicated earlier, the status portion of the CSW has two bytes (bits 32-47). One byte (bits 32-39) indicates the _____ of the _____ _____. The other byte indicates the _____ of the _____.

status
I/O device
status
channel

The channel status byte is supplied by the channel and is used to indicate the following:



Bit 40	Programmed controlled interruption
Bit 41	Incorrect Length
Bits 42-47	Channel detected errors (both program errors and machine errors)

If an I/O interrupt is caused by the PCI flag in a CCW, bit position 40 of the CSW will contain _____ (1/0).

1

If bit position 41 of the CSW contains a 1, this means that _____ _____ _____.

---

the number of bytes read or written did not match the count in the last used CCW.

Bit position 41 (incorrect length) can be prevented from setting by use of the _____ flag in the CCW.

SILI

If bit positions 42-47 of the CSW contain any ones, this would indicate that _____.

---

an error was detected by the channel. Error conditions will be covered in detail in a separate section of this manual.

Assuming normal completion of an I/O operation, the channel status byte in the CSW should contain _____.

I/O DEVICE STATUS BYTE - CSW

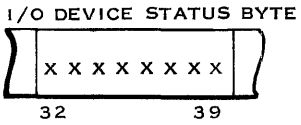
---

all zeros; This assumes (1) no PCI flags, (2) count field matches record length, and (3) error-free operation.

Bits 32-39 of the CSW represents the I/O device's _____ byte. This byte is supplied by the I/O device and is transmitted to the channel via the _____ _____.

---

status
standard interface



The I/O device's status byte represents the following:

Bit 32	-	Attention
Bit 33	-	Status Modifier
Bit 34	-	Control Unit End
Bit 35	-	Busy
Bit 36	-	Channel End
Bit 37	-	Device End
Bit 38	-	Unit Check
Bit 39	-	Unit Exception

Notice that three of the bits represent an end condition:

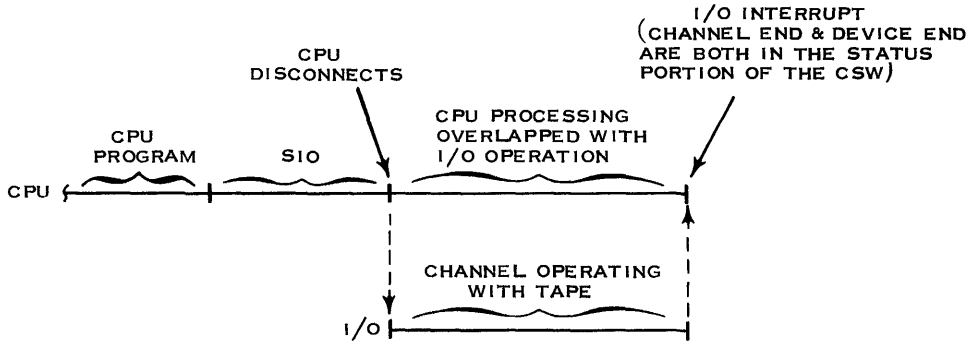
Bit 34	-	Control Unit End
Bit 36	-	Channel End
Bit 37	-	Device End

These bits indicate the unit named has "ended" its portion of the operation.

Channel end would indicate that the data transmission of a record over the standard interface has ended.

Device end would indicate that the mechanical operation of the I/O device has ended.

Both channel end and device end may occur together as they would at the end of a tape read or write operation.



After the I/O interrupt has occurred, the CPU program can interrogate the CSW in location 0064. If both the channel end and device end bits are present, the CPU program knows that both the I/O device and the channel are available for another operation.

If the channel end bit is present in the CSW, what does this signify to the CPU program? _____

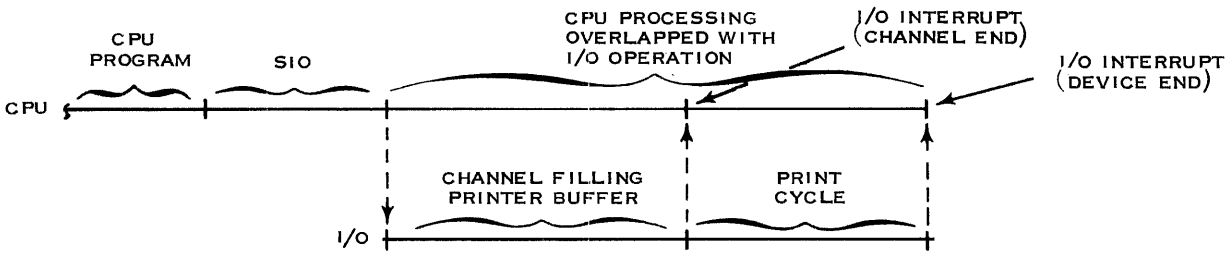
The channel has ended its portion of the I/O operation and is now available for another operation. It does <u>not</u> indicate that the addressed I/O device is available.

If the device end bit is present in the CSW, what does this signify to the CPU program? _____

The I/O device (such as a printer) has finished its portion of the operation. This usually consists of a mechanical operation. In the case of a printer, it would mean that the printing cycle has ended.

Can the channel end and device end bits be present together in the CSW?

Yes; This would indicate that both the channel and I/O device are finished with the operation. In the case of a unbuffered I/O device such as a magnetic tape unit, the channel end and device end would usually appear together. In a buffered device such as a 1443 N1 printer, the channel end would appear in the CSW after the buffer has been filled. After the print cycle, there would be another I/O interrupt and the CSW would contain the device end bit.

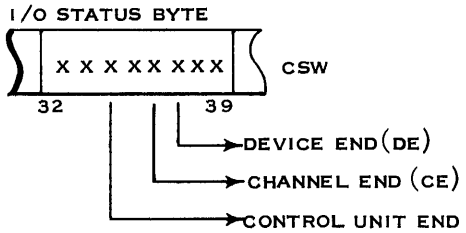


In the preceding example, the channel end and device end conditions occurred at two different times. It is entirely possible that the first interrupt will not occur immediately due to such conditions as the systems mask in the PSW. In fact, this interrupt might be delayed to the point where the printer has finished its print cycle. In this case, only one I/O interrupt would occur and the CSW would have both the channel end and device end bits. I/O interrupts will be covered more thoroughly later on. Right now, the main thing is to have a concept of what the channel end and the device end bits in the CSW mean.

What does the channel end bit in the CSW mean? The channel has finished its portion of the I/O operation and is available for another operation.

What does the device end bit in the CSW mean?

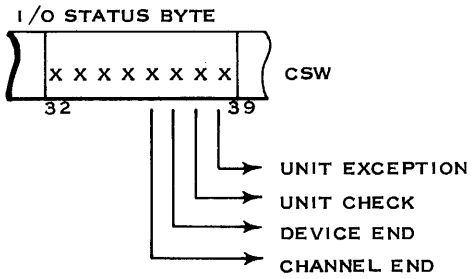
It signifies that the I/O device has finished its portion of the operation. Another operation can now be initiated on this device.



Bit 34 of the CSW represents the c_____ u_____ end bit. This bit is only used for those devices that share a control unit (such as tape units). Even for shared devices, the control unit end does not normally appear in the status byte. Later on when you take a look at some programming examples, you will see the use for control unit end.

---

control unit



Bits 38 and 39 represent u_____ c_____ and u_____ e_____ respectively.

The unit check bit is used to indicate that an error (such as wrong parity) has been detected by the control unit or I/O device. Channel detected errors would be indicated in the channel's status byte, not in the device's status byte!

The unit exception bit is used to indicate an unusual condition, not an error. Recognizing the end of reel marker during a tape write operation would be an example of a unit exception.

---

unit check
unit exception

Would the unit check or unit exception bits normally be set in the CSW?

____

No; These bits are used to indicate that the I/O device or its control unit has detected an error (unit check) or some unusual condition (unit exception).

Sensing the end of reel marker during a tape write operation is an example of an unusual condition. This condition would be indicated by the _____ _____ bit in the CSW.

---

unit exception

Reading a tape character with incorrect parity is an example of an error that would be detected by the control unit. This error would be indicated by the _____ _____ bit in the CSW.

---

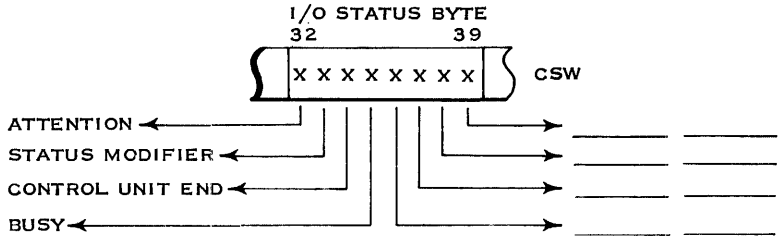
unit check

Sensing the 12 hole in a printer's carriage tape is another example of an unusual condition that is not an error. This would probably be indicated by the _____ _____ in the CSW.

---

unit exception

Fill in the labels on the illustration below. Use tear-out page 120 for reference if necessary.



As can be seen above, bit 35 of the channel status word is the b_____ bit. This bit is used to indicate that the control unit and/or the I/O device is busy and cannot initiate an I/O operation at the present time. The busy bit is used along with the status modifier bit (CSW bit 33) to indicate the busy states of control unit and I/O device.

---

busy

Neither of these bits are usually present in the CSW associated with an I/O interrupt. The CSW can also be stored on certain conditions when a "start I/O" instruction is issued. More on this later!

Bit 32 of the CSW is the a_____ bit. This bit has nothing to do with an I/O operation. It is normally the result of operator action at an I/O device. Not all I/O devices have the ability to generate an attention signal.

---

attention

Assume that a tape write operation has been completed. The operation was trouble-free with nothing out of the ordinary. What is the make-up (in hex) of the status byte that could be expected from the tape control unit?

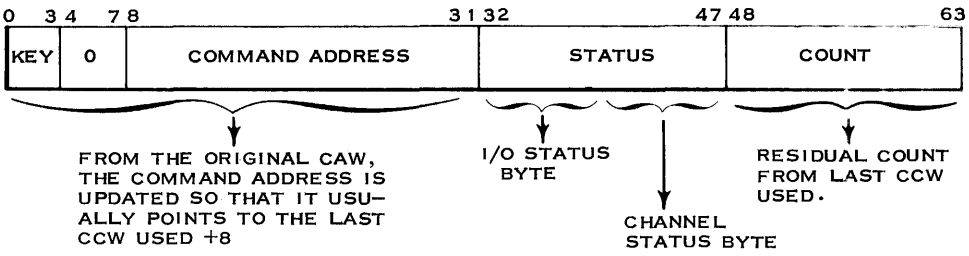
_____

0C (in hex); Note that only the channel end and device end bits are present.

Assume that the channel has just finished sending a data record to a printer's buffer. The print cycle has just started. What is the make-up (in hex) of the device status byte in the CSW? ____

08; Note that only the channel end bit is present.

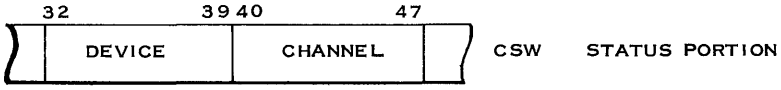
The following is a summary of the channel status word.



On an I/O interrupt the CSW is placed in location 0064 where it can be examined by the ___ ___ ___ program. The CSW can also be stored during a "start I/O" instruction. This occurs under certain conditions when the I/O operation can't be started.

CPU

The following is a summary of the status portion of the CSW.



Bit	Device	Bit	Channel
32	Attention	40	PCI
33	Status Modifier	41	Incorrect Length
34	Control Unit End	42-47	Channel Detected
35	Busy		Errors
36	Channel End		
37	Device End		
38	Unit Check		
39	Unit Exception		

At the conclusion of a typical I/O operation, it would be expected that the channel status byte would be all _____ and that the device status byte might contain _____ _____ and/or _____ _____.

---

zeroes
channel end
device end

You have now concluded your introduction to I/O operations. Read the following areas in the Input/Output Section of the Principles of Operation manual.

Execution of Input/Output Operations	Unit Status Conditions
Definition of Storage Areas	Attention
Chaining	Status Modifier
Data Chaining	Control Unit End
Command Chaining	Busy
Program Controlled Interruption	Channel End
Commands	Device End
Transfer In Channel	Unit Check
Channel Status Word	Unit Exception

REVIEW QUESTIONS ON INTRODUCTION TO I/O OPERATIONS

- Try to answer the questions without referring to the material. However, if you do require aid, refer to this book and/or the Principles of Operations manual and consider reviewing the area where aid is required.

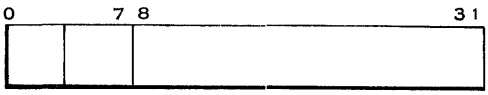
1. Write the names for the following abbreviations:

   a. I/O _____
   b. CH _____
   c. CU _____
   d. CAW _____
   e. SIO _____
   f. UCW _____
   g. UA _____
   h. CCW _____
   i. CSW _____
   j. CDA _____
   k. CC _____
   l. SILI _____
   m. PCI _____

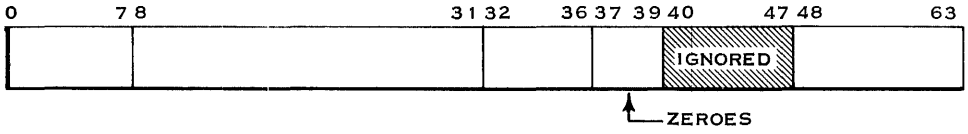
2. Number the following according to the sequence in which they are used on an I/O operation:

   a. CCW _____ c. CSW _____
   b. SIO _____ d. CAW _____

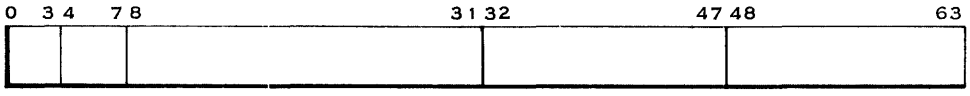
3. Label the fields of the CAW.



4. Label the fields of the CCW.



5. Label the fields of the CSW.



6. The control information to sustain one I/O operation is usually called a _____ _____ _____.

7. What is the difference between a channel and a sub-channel? Explain with reference to a multiplexor channel. _____
   _____
   _____
   _____

8. Given the following unit address of a device on a multiplexor channel, what UCW # will be used? 01111000 _____

9. Given the following unit address of a device on a multiplexor channel, what UCW # will be used? 11110000 _____

10. What is the name for the set of communication lines between a channel and the I/O control units? _____ _____

11. Given the following:

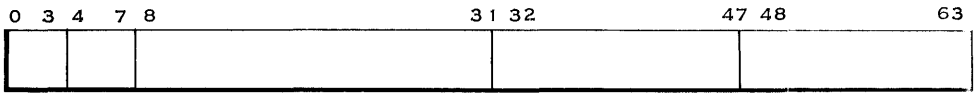
```
LA      6, 2048 (0)          2048 ⟶ 02000F0080000014
ST      6, 0072 (0)                 02000F1490000028
LA      12, 260 (0)                 02000F3C00000014
SIO     0 (12), 0
```

NOTE: You are not expected to remember the individual flag bits. Here is a list for your reference.

CDA - bit 32
CC - bit 33
SILI - bit 34
SKIP - bit 35
PCI - bit 36

a. What channel is being used? _____
b. Assuming that a magnetic tape unit is being addressed, how many tape records will be read? _____
c. The 80 character tape record will be read into what locations of main storage? _____
d. Show (in hex) the contents of the CAW used for this operation.

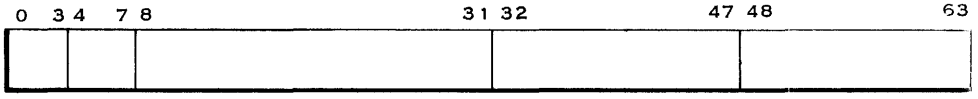
e. Assuming normal error-free completion of the operation, show the contents of the CSW that will be placed in location 0064 at the time of the I/O interrupt.



12. Given the following:

```
LA      7, 2048 (0)          2048 ⟶ 02000F0040000050
ST      7, 0072 (0)                 02000F5000000055
LA      12, 129 (0)
SIO     0 (12), 0
```

a. What channel is being used? _____
b. How many cards will be read? Assuming that we are addressing a card reader. _____
c. Will an incorrect length indication be placed in the status field of the CSW? _____
d. What will be the resulting contents of the CSW? Assume trouble-free operation.

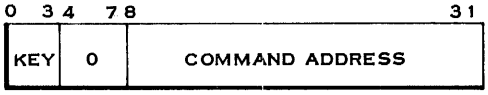


ANSWERS TO REVIEW QUESTIONS

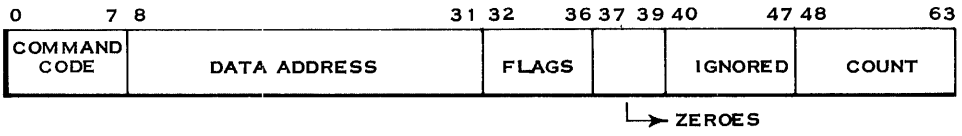
1. a. Input-Output
   b. Channel
   c. Control Unit
   d. Channel Address Word
   e. Start I/O
   f. Unit Control Word
   g. Unit Address
   h. Channel Command Word
   i. Channel Status Word
   j. Chaining Data
   k. Chaining Commands
   l. Suppress Incorrect Length Indication
   m. Programmed Controlled Interrupt

2. a. CCW 3
   b. SIO 1
   c. CSW 4
   d. CAW 2

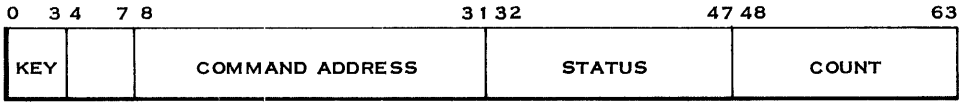
3.



4.



5.



6. Unit Control Word

7. A sub-channel refers to the area needed to hold the control information (UCW) for one I/O operation. A channel refers to the circuitry and registers to handle I/O operations for any device. A multiplexor channel contains circuitry that will service one of its sub-channels at a time. The sub-channels are located in bump storage.

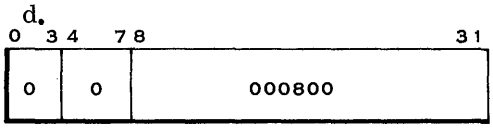
8. UCW #120

9. UCW #7

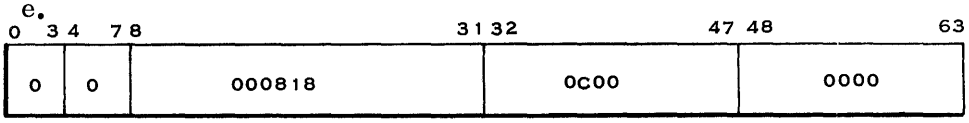
10. Standard Interface

11. a. Selector Channel 1
    b. One
    c. Columns 1-20 into locations 3840-3859
       Columns 21-60 are skipped
       Columns 61-80 into locations 3900-3919

d.

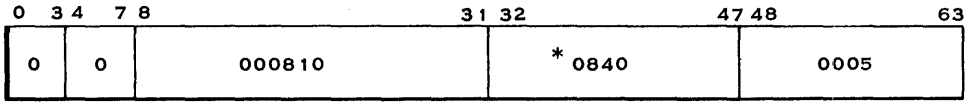


e.



12. a. Multiplexor Channel
    b. Two
    c. Yes; The number of characters (80) in the record does not agree with the count. Since the SILI flag isn't set, an indication of incorrect length will be placed in the CSW.

d.



* THE DEVICE STATUS MAY DIFFER, DEPENDING UPON THE PARTICULAR TYPE OF CARD READER USED. IT MAY CONTAIN THE CHANNEL END BIT ONLY, AS SHOWN ABOVE OR IT MAY CONTAIN BOTH CHANNEL END AND DEVICE END (0C).

System/360 Input/Output Operations

	Section I:	Introduction to I/O Operation
●	Section II:	I/O Devices
	Section III:	Standard Interface
	Section IV:	I/O Instructions
	Section V:	Channel Error Conditions
	Section VI:	Initial Program Load Procedure
	Section VII:	Analyzing I/O Programs

SECTION II LEARNING OBJECTIVES

At the end of this section, you should be able to do the following:

1. State the meaning of the following I/O commands;
   Read
   Read Backward
   Write
   Sense
   Control
   Transfer in Channel (TIC)

2. When given a list of the CSWs I/O device status byte bits, explain the function of each bit.

3. State the relationship between device end and channel end.

4. State the maximum number of lines that can be printed from one CCW on a 1443 N1.

5. State the maximum number of columns that can be read or punched from one CCW on a 1442 N1.

6. State the direction of tape movement on a 2400 series tape unit.

I/O Devices

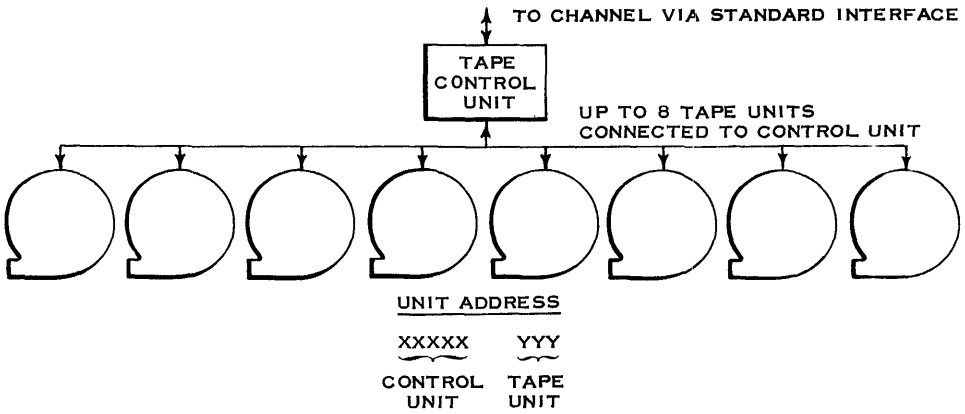
This section is intended to familiarize you with some of the I/O devices which can be used with System/360. The I/O devices which you will take a look at are:

2400 Series Magnetic Tape Unit
1442 N1 Card Read-Punch
1443 N1 Printer

You are not expected to know everything concerning these devices. They are being presented here only to make the explanations of channel operations and I/O programming more meaningful. You will become familiar with only the following information concerning these devices.

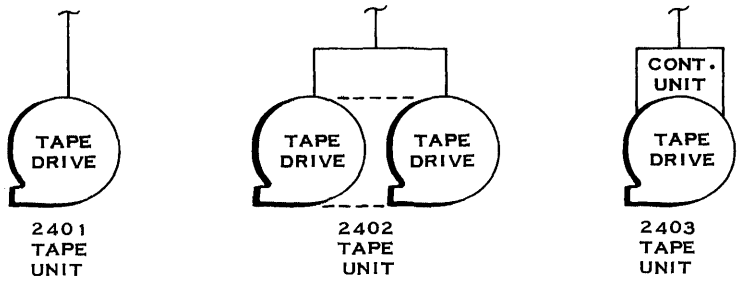
1. What operations (command byte) can these devices perform?
2. Are the channel end and device end signals presented to the channel together or separately for these operations?
3. What is the mechanical movement of the record media (card or tape) for each command?
4. What is the record format?

2400 SERIES MAGNETIC TAPE UNITS



A tape system using 2400 tape units consists of one tape control unit with from one to eight tape units attached to it. The unit addresses of the eight (maximum) tape units are consecutive. The five high-order bits represent the control unit while the three low-order bits represent the device.

The physical makeup of the tape system can vary depending on the tape units used. There are three standard magnetic tape units:



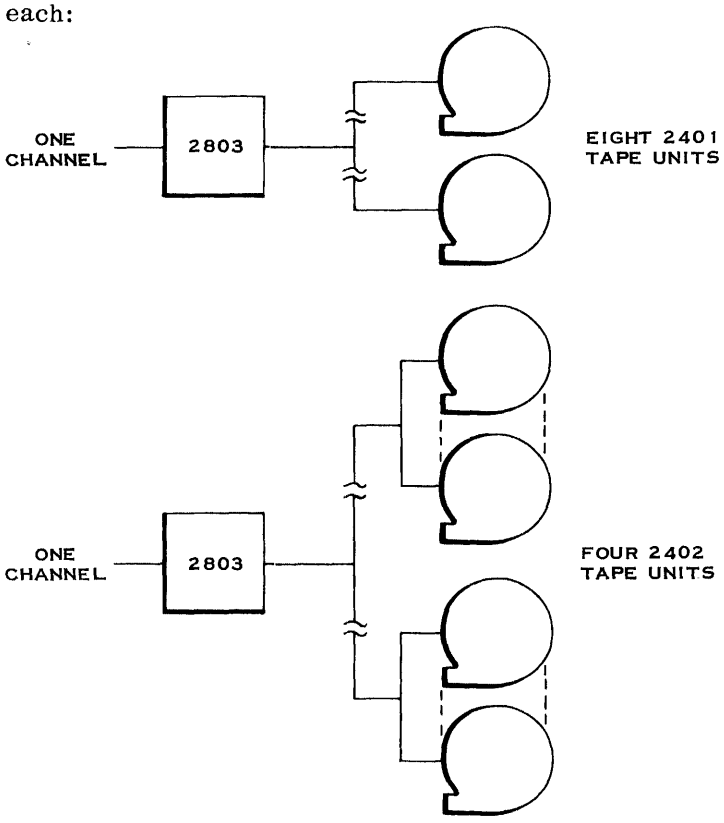
A tape unit with one tape drive in the cabinet is called the _____ tape unit.

A tape unit with two tape drives in the same cabinet is called the _____ tape unit.

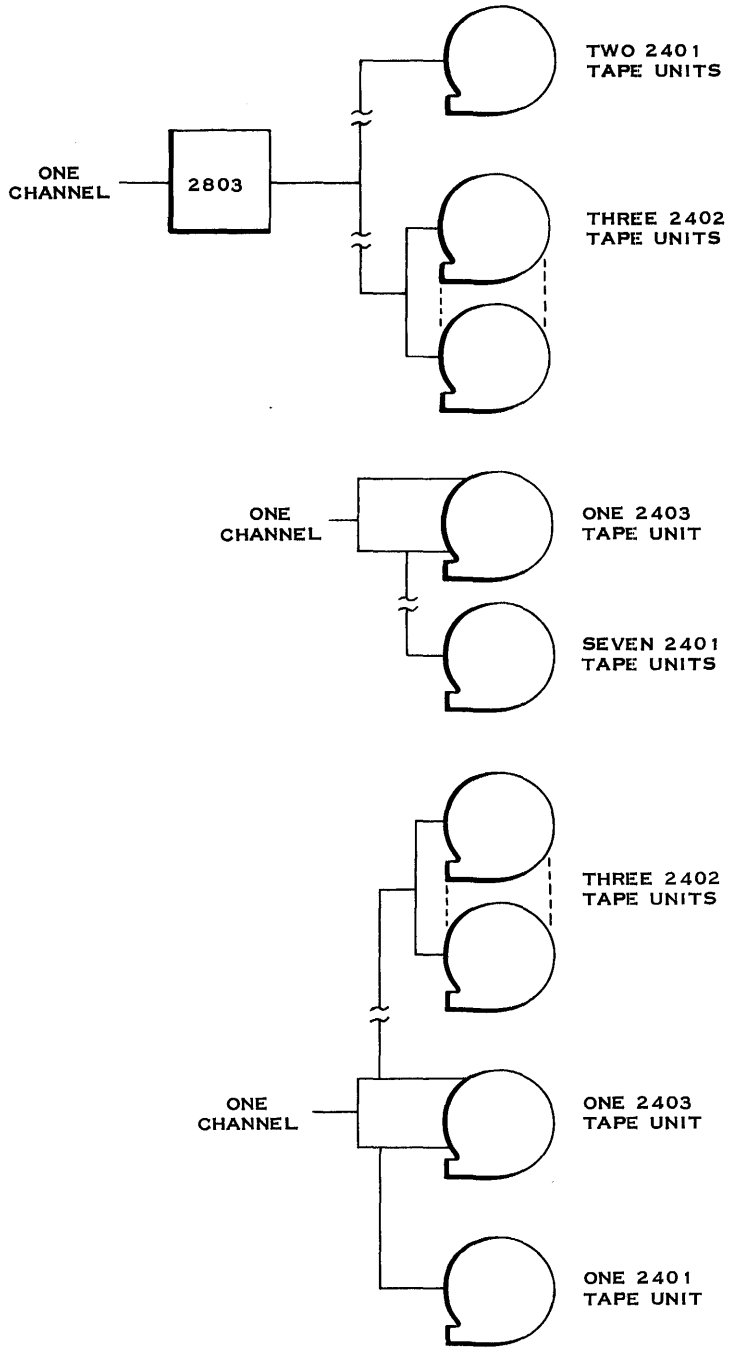
A tape unit with one tape drive and a control unit in the same cabinet is called the _____ tape unit.

2401
2402
2403

If a 2403 is not used, the tape system must have a 2803 tape control unit. The following are some of the possible tape systems with eight tape units each:



(Frame continued on next page)


TWO 2401
TAPE UNITS
ONE
CHANNEL
2803
THREE 2402
TAPE UNITS
ONE
CHANNEL
ONE 2403
TAPE UNIT
SEVEN 2401
TAPE UNITS
THREE 2402
TAPE UNITS
ONE
CHANNEL
ONE 2403
TAPE UNIT
ONE 2401
TAPE UNIT

The number of a magnetic tape unit (such as 2402) gives which of the following information about the unit: (circle one)

Tape speed
Physical packaging
Character rate

Physical packaging

The number of the tape unit specifies the packaging of units within the physical frame (cabinet). All standard 2400 tape units operate at only one density; 800 characters per inch. The inter-record gap is .6 inch. Special units can be had to operate at different densities and gap size to provide compatibility with systems other than System/360. We are concerned here with standard units.

Three different tape speeds are available with the 2400 series tape units. The tape speed is identified with a model number:

		Approximate Speed
24XX	Model 1	37.5 inches/second
24XX	Model 2	75 inches/second
24XX	Model 3	112.5 inches/second

Which of the following consists of two tape units packaged together and capable of moving tape at a rate of 75 inches per second?

a. 2402 Model 1
b. 2401 Model 2
c. 2403 Model 2
d. 2402 Model 2

---

d; 2402 Model 2

Two units per package → 75 inches per second

All standard 2400 series tape units read or write tape at ____ characters per inch.

The inter-record gap size for standard 2400 tape units is _____ inch.

800
.6

A tape character consists of 9 bits. Eight of these are data bits and one is a parity bit. Each tape character read or written is equivalent to one _____ in main storage.

---

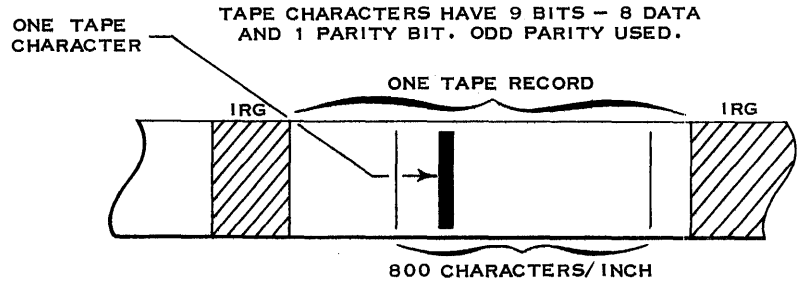
byte

Standard tape units are code insensitive. That is, the bits sent from main storage are written on tape without change. Therefore, the tape units use _____ (odd/even) parity.

---

odd; A tape character with an even number of bits set would cause an error. This would result in a unit check indication in the CSW.

The following summarizes the makeup of a tape record.

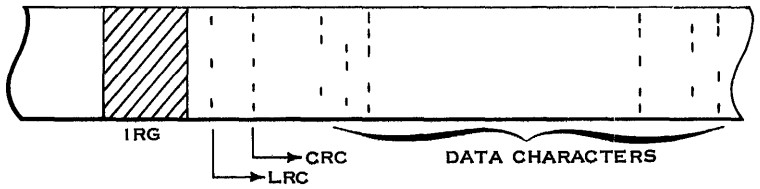


As with previous IBM tape units, an LRC (Longitudinal Redundancy Check) character is written at the end of the tape record. This character is used to make a horizontal redundancy check of the tape record. Either a LRC or a VRC error will result in a _____ _____ indication.

---

unit check

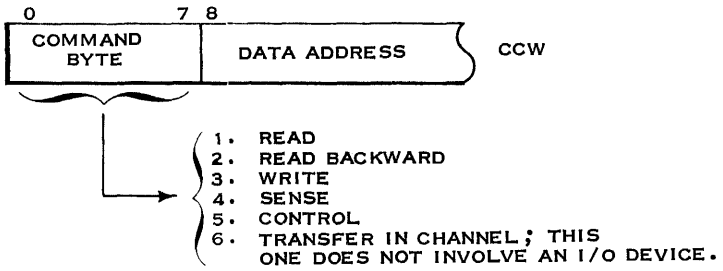
Between the last data character and the LRC character, another special character is written. It is called the Cyclic Redundancy Check (CRC) character. Its main function is to permit programmed correction of single track tape errors.



Both the LRC and CRC characters are strictly for checking purposes. They do not enter main storage and are not included in the count field of the channel command word (CCW).

A tape record then consists of the series of tape characters from one inter-record gap to the next inter-record gap. An I/O operation involving a tape record(such as read or write) will cause tape to move past the read/write head from one gap to the next gap. The next question is: "What operations can be performed on a standard 2400 series tape unit?"

There are six I/O commands but only five of these actually involve an I/O device.



If a read, read backward, or a write operation is called for, tape will move from one IRG to the next. Data will be transferred over the channel under control of the data address and count fields in the CCW.

Data chaining involves chaining the data of one tape record.

Command chaining involves two or more tape records.

These three operations are indicated by the command byte in the CCW as shown below:

Command Byte	Operation
X X X X X X 1 0	Read
X X X X 1 1 0 0	Read Backward
X X X X X X 0 1	Write

The bit positions marked X are ignored.

If a "hex" command byte of 7E is sent to a tape control unit, a _____ operation will be performed.

---

read; As long as the two low order bits are 10, a read operation will be performed.

A "hex" command of 01 will initiate a _____ operation.

---

write

CCW

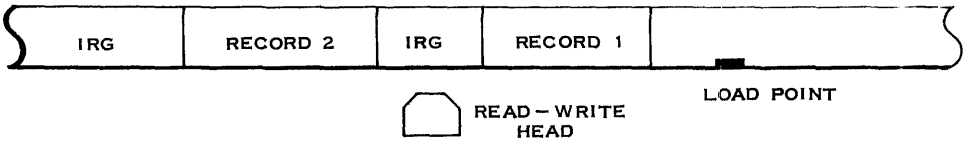
02	000800	00	00	0050

Given the above CCW, an eighty character tape record will be read into byte locations _____ through _____.

2048, 2127

Both the read and the write operations involve moving tape in a forward direction from one gap to the next. That is, tape will move from left to right and the LRC character will be the last one read or written.

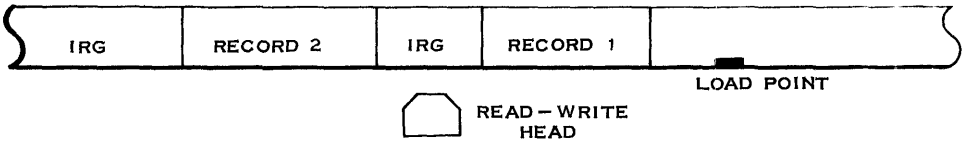
The read backward operation causes tape to move in a backward direction from one gap to the next. The LRC character will be the first character read. However, neither it nor the CRC character is placed in main storage.



Circle the record (in the illustration) that will be read into main storage if a read command is given.

---

record 2



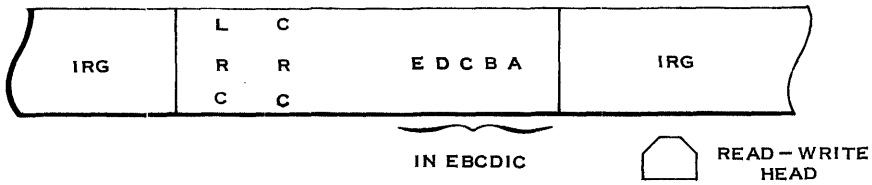
Circle the record (in the illustration) that will be read into main storage if a read backward command is given.

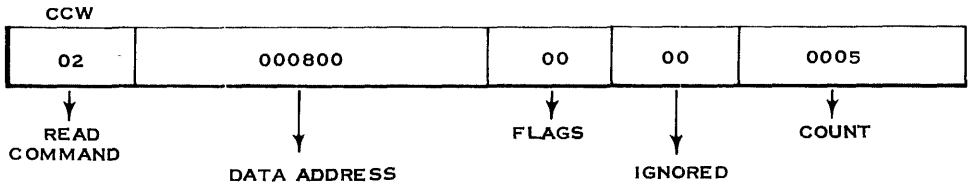
---

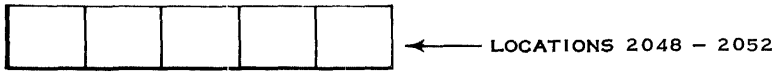
record 1

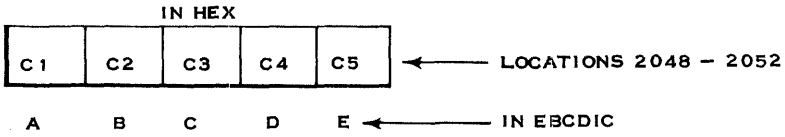
In a read or write operation, the storage addresses are used in ascending order starting with the data address in the CCW. In a read backward direction, the storage addresses are used in descending order starting with the data address in the CCW.

Given the following tape record and CCW, show (in hex) the resulting contents of main storage location 2048-2052.

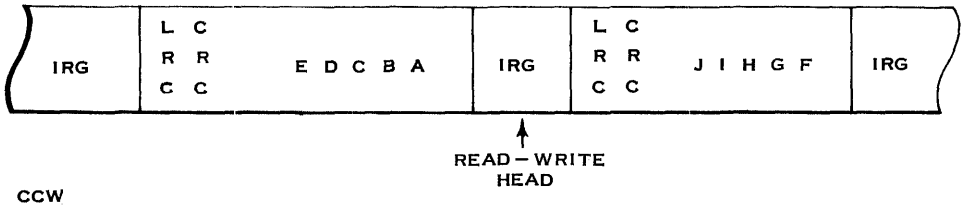


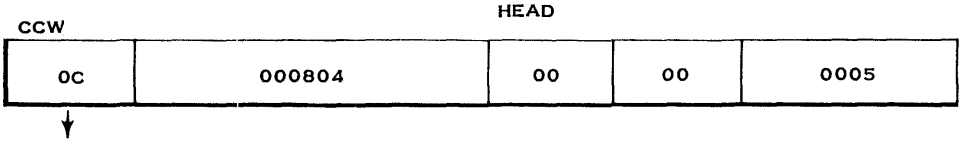


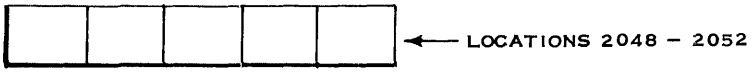




Given the following tape record and CCW, show (in hex) the resulting contents of main storage locations 2048-2052.



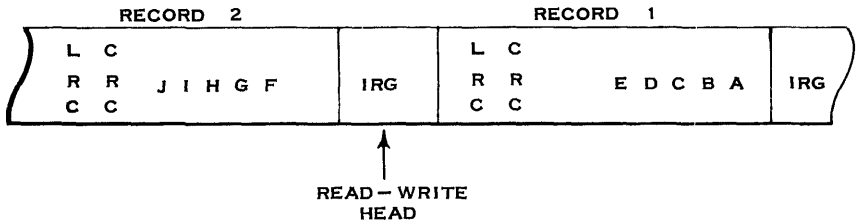




C6	C7	C8	C9	D1	LOCATIONS 2048 – 2052

Notice that the 1st character read in the read backward operation was a "J." This character was placed in location 2052 which was the starting address in the CCW. The next character was an "I" and this was placed in the next lower storage location (2051).

Given the following tape record show the locations used for both a read operation and a read backward operation.



CCW

X X	000800	00	00	0005

a. If the command byte calls for a read operation, Record # ____ will be read into locations _____ through _____.
b. If the command byte calls for a read backward operation, Record # ___ will be read into locations _____ through _____.

a. #2, 2048, 2052
b. #1, 2048, 2044

Besides the read, read backward, and write commands, the 2400 series tape units can also execute the sense and control commands. The control command is used to initiate a number of tape operations which do not involve a data transmission through the channel. The command code for a control operation is as follows:

If bits 6-7 of the command code sent to the tape control unit are 11, a control command is called for. The tape control unit will then examine bits 2-5 to see which control order to execute. Bits 2-5 are decoded as follows:

0001 Rewind; Tape moves backward to load point.

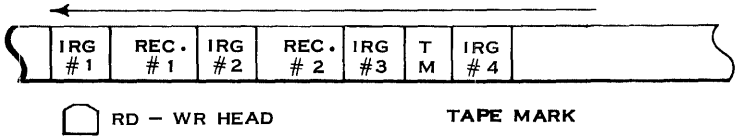
0011 Rewind and Unload; Tape moves backward to load point and then unloads.

0101 Erase Gap; Tape moves forward and erases tape for about 3-1/2 inches. This operation is to be used on a tape write error routine to get past a bad spot on tape.

0111 Write Tape Mark; A one character record consisting of a tape mark is written. Normal inter-record gaps are generated. The tape control unit will generate the bit configuration for the tape mark.

1001 Backspace Record; Tape is moved backward from one gap to another. This operation is useful in re-reading or re-writing a tape record.

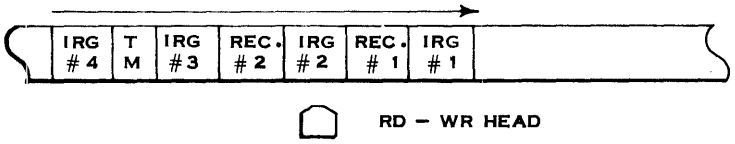
1011 Backspace File; Tape is moved backward to either (1) load point or (2) past the next tape mark. For instance:



Tape would stop with IRG #4 over the read-write head.

1101 Forward Space Record; Tape moves in a forward direction from one gap to the next. This differs from a read operation in that the channel isn't used and no data is transmitted.

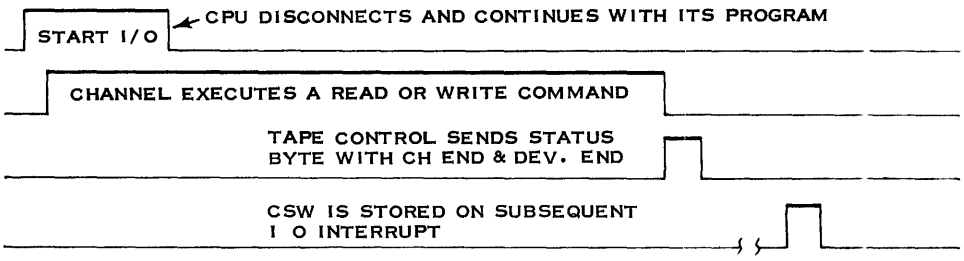
1111 Forward Space File; Tape moves in a forward direction to the gap just past the next tape mark. For instance:



Tape would move in a forward direction and stop with gap #4 over the read-write head.

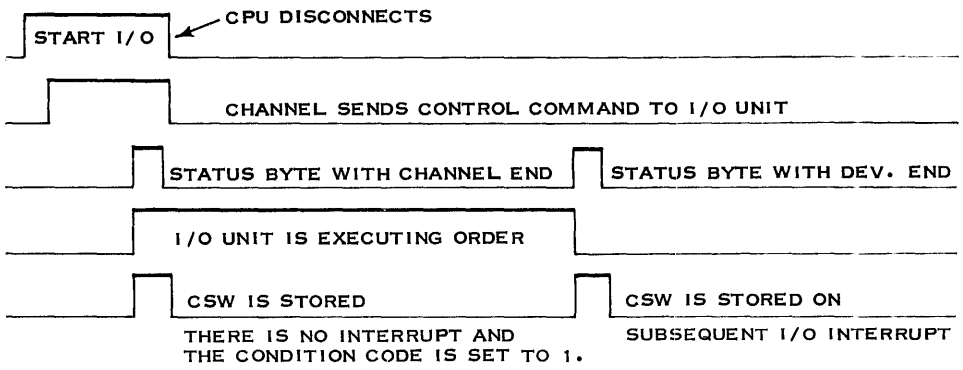
The preceeding was a brief description of the control orders that can be executed by a standard 2400 series tape unit. They are called control orders, because they are executed by the control unit and not by the channel. The channel simply supplies the command bytes. Once it is accepted, the channel has finished executing the control command. The control unit will then go off on its own and execute the control order, while the channel is free to operate with some other I/O device.

As you know, the tape control unit will send a status byte to the channel at the end of a read, read backward, or write operation. This status byte will be placed in the CSW and will contain both a channel end and a device end indication. These bits will indicate to the CPU program that the channel as well as the device is free. This is shown below.



READ – WRITE COMMAND

Since the channel is not used to execute a control order the tape control unit will send a status byte containing channel end to the channel after it receives the command byte. This status byte will be stored in the CSW before CPU is allowed to disconnect and end its execution of the "start I/O" instruction. Some time later, the control unit and I/O device will have finished executing the order. At this time, another status byte will be sent to the channel indicating device end. When the I/O interrupt happens, the CSW will then contain the device end bit. This is shown below.



CONTROL COMMAND

We will be referring to the status byte again later on when we discuss the standard interface.

The sense command (XXXXX100) is an operation which is used to send additional status information to main storage. For instance, at the end of a tape read operation, one byte of status information concerning the tape unit is placed in the channel status word. One of the bits in the device's status byte is the unit check bit. This bit when present will indicate to the CPU program that an error of some type occurred while reading tape. The sense command can now be used to request additional information such as what type of error it was. Up to six bytes of sense data can be placed in main storage depending on the count field in the CCW. Since you are not expected to be an expert on tape units, we will not discuss the bit by bit make-up of the sense bytes.

THE 1442 N1 CARD READ-PUNCH

The 1442 N1 is a card-read punch with a built-in control unit. Both the reading and the punching facilities of the 1442 share the one control unit. There is only one card feed path for both reading and punching. If separate punching and reading capabilities are desired, additional 1442s may be placed on the channel.

The 1442 N1 does not have a buffer storage and cards are read and punched column by column. Because of this, its character rate is relatively slow. You would expect, then, that a 1442 N1 would usually be placed on a multiplexor channel. However, it can be placed on a selector channel if desired.

A 1442 N1 is a card read punch in which reading and punching is done a _____ (column/row) at a time.

---

column

The 1442 N1 has _____ (one/separate) feed path(s) for reading and punching.

---

one

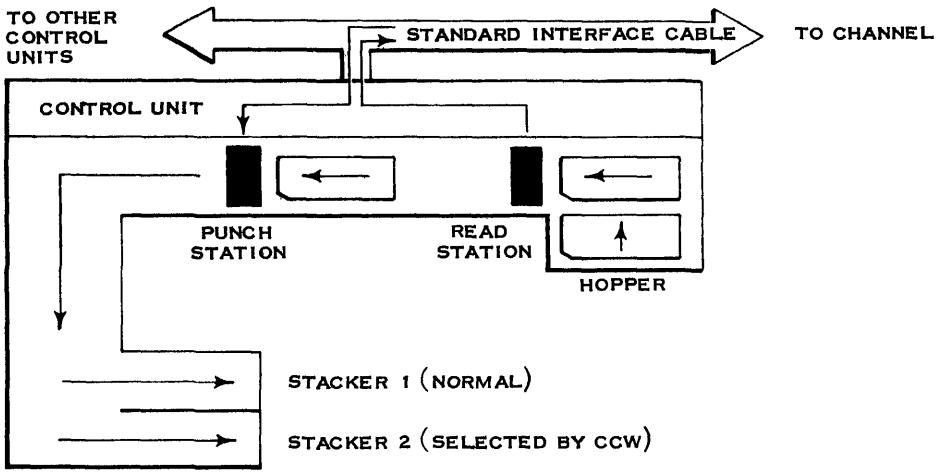
The information read from a card by the 1442 N1 is: (Circle one)
a. Placed in a buffer storage for fast transmission over the channel.
b. Sent directly to the channel a column at a time.

---

b.

The 1442 N1 has a maximum reading speed of 400 cards per minute. The actual reading speed is dependent on the programming involved. Each feed cycle requires a command from the channel.

The punching speed depends on both the programming and the number of columns punched in each card. When punching 80 columns, the maximum punching speed is approximately 90 cards per minute. Because of the single card path for punching and reading, it is possible to read data from a card, process it, and punch the results in the same card. Of course, this would require two separate operations; a read command followed some time later by a write command.



1442 N1 TOP VIEW

As can be seen above the read station is _____ (before/after) the punch station.

---

before

After a run-in cycle the first card is at the read station. A read command would cause the card to take a feed cycle. As the card passes the read station, the information is transmitted column by column to the channel.

At the end of the feed cycle, the first card would then be sitting at the _____ station and the second card would be at the _____ station.

---

punch
read

After the data from the first card has been processed by CPU, a write command can be given to punch the results in the same card. During the punching operation, a feed cycle does not occur. The number of columns that are punched depends on the _____ field in the CCW.

---

count

It should be noted at this time that the data bytes received by the 1442 N1 must be in EBCDIC. The data bytes read by the 1442 N1 and sent to main storage are also coded in EBCDIC.

After the punching operation is completed, a feed cycle may or may not occur depending on the bits in the command bytes. When reading and punching in the same card is being done, punching would usually be programmed without a feed cycle. This is to prevent losing the information from the card passing the read station. If card #1 were programmed to punch with a feed cycle, the information from card #2 would be lost.

Card feeding does not take place during the card punching. Whether a feed cycle follows the punching operation depends on the _____ byte.

---

command

CCW IN HEX

01	000800	00	00	0032

When the 1442 N1 takes a punch cycle without feeding a card, the punched card will remain under the punch station with the next blank column ready to be punched. The CCW shown above specifies a write command without feeding. Which card column will be under the punches at the end of the operation? _____

---

column 51

1442 N1 can accept four of the five I/O device commands. These are shown below:

Read	XM0XXX10
Write	MM0XXX01
Control	MMXXXX11
Sense	XX000100

Bit positions 0 and 1 are used as modifier bits for the read, write and control commands.

Bit position 0 when set to 1 will cause a feed cycle. (Read commands always cause a feed cycle).

Bit position 1 when set to 1 will cause the card in the punch station to be stacked in stacker #2. Otherwise, the card will go into stacker #1.

Given the following CCW and assuming a run-in cycle has been completed, answer the following. (Card #1 is registered at the read station.)

CCW

C2	000800	00	00	003C

a. Which columns of card #1 will be read into main storage?

_____

b. Where will cards #1 and #2 be at the end of the operation?

_____

c. Bits 0 and 1 of the command byte are set to 1. Did this have any effect on the operation? _____

---

a. Columns 1-60; columns 61-80 are read but not sent to main storage. The incorrect length indication bit in the CSW will be set to 1.

b. Card #1 will be just before the punch station; Card #2 will be registered at the read station.

c. No; bit 0 is ignored on a read operation since a feed cycle will be taken anyway. Bit 1 would have caused a card at the punch station to go into stacker #2. However, there wasn't a card there at this time.

Given a list of chained CCW's, answer the following questions. Assume that a run-in cycle has been completed and that card #1 is registered at the read station.

			Flags
CCW1	02	00080090000028	CDA, SKIP
CCW2	02	00080040000028	CC
CCW3	C1	00080060000028	CC, SILI
CCW4	83	00080000000050	None

a. Where are cards #1, 2, 3, and 4 at the end of the operation? _____

b. What information was punched into card #1, if any? _____

c. The data from which columns of which card is in main storage at the end of the operation? _____

---

a. Card #1 is in stacker #2.
   Card #2 is in stacker #1.
   Card #3 is at the punch station.
   Card #4 is at the read station.
b. The information from columns 41-80 of card #1 was punched into columns 1-40 of card #1.
c. Columns 41-80 of card #1; Card #2 passed the read station during the feed cycle resulting from the write command byte. Card #3 passed the read station because the control command specified a feed cycle only.

You should now know that the 1442 N1 can do the following operations:

1. Read data and transmit each column of a card to main storage as one EBCDIC byte. The card at the punch station can be directed to feed into either stacker #1 or stacker #2.

2. Punch data from main storage into the card at the punch station. After the data has been punched, the card can either be directed to feed into one of two stackers or it can be kept at the punch station. If the card is left at the punch station and another write command follows, punching will resume in the same card with the next available column.

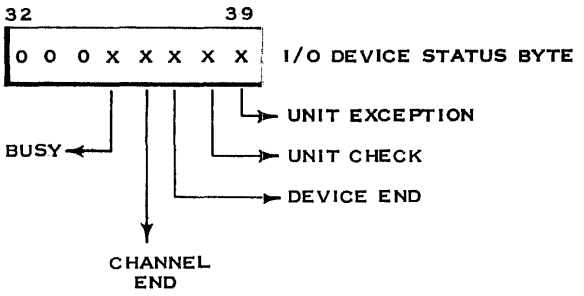
   NOTE: If a write command is given after the run-in cycle, a feed cycle will occur and bring card #1 up to the punch station and punching will begin.

3. With a control command, the 1442 N1 can be directed to take a feed cycle and stack in either stacker #1 or #2. With the absence of both bits 0 and 1, the control command does nothing.

4. With a sense command, the 1442 N1 can send one byte of sense data to main storage. If the count field in the CCW calls for more than one byte, the incorrect length indication bit in the CSW will be set.

Let's now examine the status byte that is placed in the CSW by a 1442 N1.

Bits 32-34, which represent attention, status modifier, and control unit end, are not used by the 1442 N1 and will always be zero.



Bit 35 - the busy bit is used during the execution of a "start I/O" instruction to indicate that the 1442 N1 is either busy executing a previous command or although it has finished, its status byte hasn't been accepted by the channel yet.

Bit 36 - channel end is placed in the CSW to indicate that the channel transmission has ended. For a read or write command, channel end is placed in the status byte as a result of the CCW's count field being reduced to zero. Otherwise, it will come at the end of the feed cycle along with device end.

Bit 37 - device end is normally sent at the end of a feed cycle. However, during a punch operation (no feed cycle), device end is sent with channel end at the end of data transmission.

Bit 38 - unit check is used to indicate that either an error occurred during the last operation or that operator intervention is required to put the 1442 N1 into a ready status (no cards in hopper, etc.)

Bit 39 - unit exception is used to indicate the end of a card file (it is not used to indicate an empty hopper). There is an end of file button on the 1442 N1. Normally, when the hopper is empty, the unit check bit is used to indicate that more cards are needed. When the last handful of cards from a card file is placed in the hopper, the end of file button is depressed. This time the 1442 will continue to read cards until the last card has been read and is at the punch station. With the next read command, the unit exception bit is set and the last card is stacked.

Under what conditions would channel end and device end be presented at the same time after a read command? _____

When the total count in the CCW(s) is greater than 80 bytes. In this case the channel would be expecting more bytes. When the 1442 N1 completes its feed cycle, it will send channel end along with device end.

If a punch operation is specified without a feed cycle, when will device end be sent? _____

It will be sent along with channel end at the end of the data transmission.

If a punch operation is specified with a feed cycle, when will device end be sent? _____

At the end of the feed cycle.

If a control command is used to feed a card, when will device end be sent? _____

At the end of the feed cycle.

On a control command, one data byte is sent to the 1442. This byte is not needed for the feed cycle, but is used during subsequent diagnostic operations. The channel end is sent after this data byte has been received.

At this point you should be familiar with the following items concerning a 1442 N1.

1. What operations the standard 1442 N1 can execute.
2. When the channel end and device end signals are sent.
3. The movement of cards through the feed for each command.
4. Record format (EBCDIC).

THE 1443 N1 PRINTER

The standard 1443 N1 printer has a set of 52 characters with a 120 position printing line. The maximum printing rate is 240 lines per minute. Like the 1442 N1 card punch, the 1443 N1 printer has a built-in control unit and is usually attached to a multiplexor channel.

Unlike the 1442 N1, the 1443 N1 printer has a buffer storage. The buffer storage is large enough to store 120 characters of EBCDIC data. However, only bits 2-7 of the EBCDIC byte are stored. This is okay for alphameric data since bits 0-1 are all the same anyway. The numeric bits of special characters do not use any numbers in the range of 0-9. So if the four numeric bits of a byte are in the range of 10-15, a special character will be printed.

What is the maximum length record that can be printed on a standard 1443 N1 with one write command? _____

120; Each write command will cause one line to print.

Records longer than 120 characters can be printed on successive lines by use of the _____ _____ flag in the CCW.

---

chain command

Data sent to the 1443 N1 printer must be in the _____ format.

EBCDIC

Is the channel tied up for the entire printing operation? _____

No; Because the printer contains a buffer storage.

When will the channel be free on print operation? _____

Once the data record has been stored in the 1443 N1 buffer.

What is the name of the signal that says the channel is free? _____

Channel End

What is the name of the signal that will indicate when the print cycle has ended? _____

Device End; If carriage movement is involved, device end won't be sent until the carriage stops.

The standard 1443 N1 can accept the following commands:

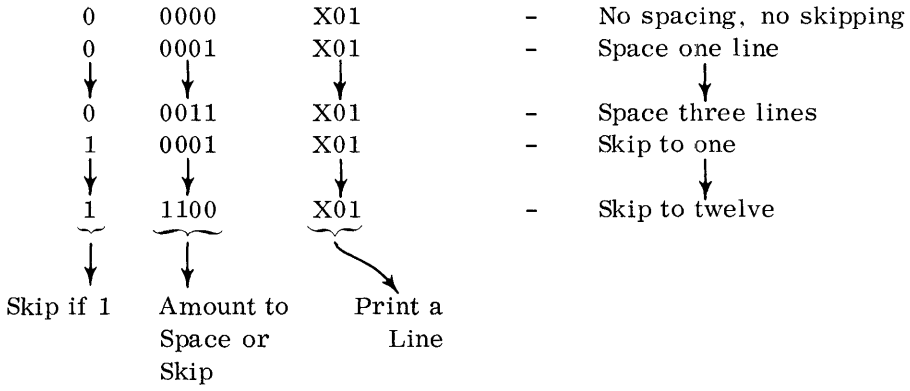
1. Write - A line is printed
2. Control - For carriage operations
3. Sense - A sense byte is read into main storage

NOTE: A 1443 N1 can also accept a read command. This is only used for diagnostic purposes, however.

If bits 6, 7 of the command byte are 01, a write command is specified. If no other bits are set, the 1443 N1 will print one line and there will be no movement of the printer carriage. There is no automatic spacing. Depending on bits 0-4 of the write command byte, the 1443 N1 can be directed to print and do one of the following:

1. No spacing or skipping.
2. Space 1, 2, 3 lines after printing.
3. Skip to carriage channel 1-12 after printing.

The write command is broken down as follows:



Given a 1443 N1 printer and the following CCW:

09	000800	00	00	0078

a. How many characters will print? _____
b. What carriage movement will occur if any? _____
c. When will the channel end signal be sent to the channel? _____
d. When will the device end signal be sent to the channel? _____

---

a. 120 characters (hex 78)
b. A single space will occur after the print cycle.
c. After the printer buffer has been loaded with 120 characters.
d. After the carriage has completed its single space.

Given a 1443 N1 printer and the following:

CAW

4	0	000F00

CCW 1

0 9	000800	80	00	003C

CCW 2

1 1	00083C	40	00	003C

CCW 3

1 9	000878	00	00	0078

a. How many lines will be printed? _____

b. State what carriage movements will occur as a result of the CCW's.

_____

_____

_____

c. How many I/O interrupts might occur as a result of the above CCW's?

_____

d. Show the resulting CSW for the first I/O interrupt, assuming trouble-free operation.

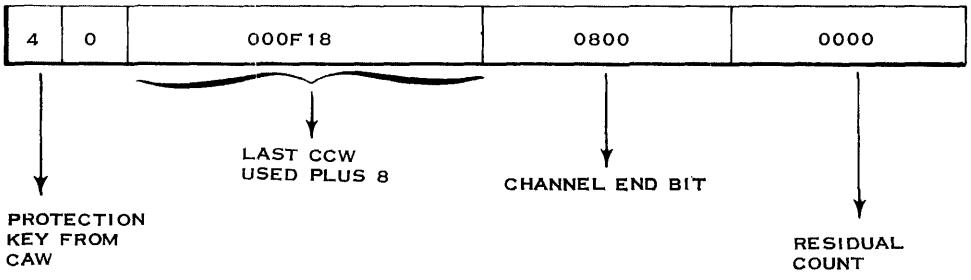
---

a. Two (CCW1 and CCW2 are chaining data)

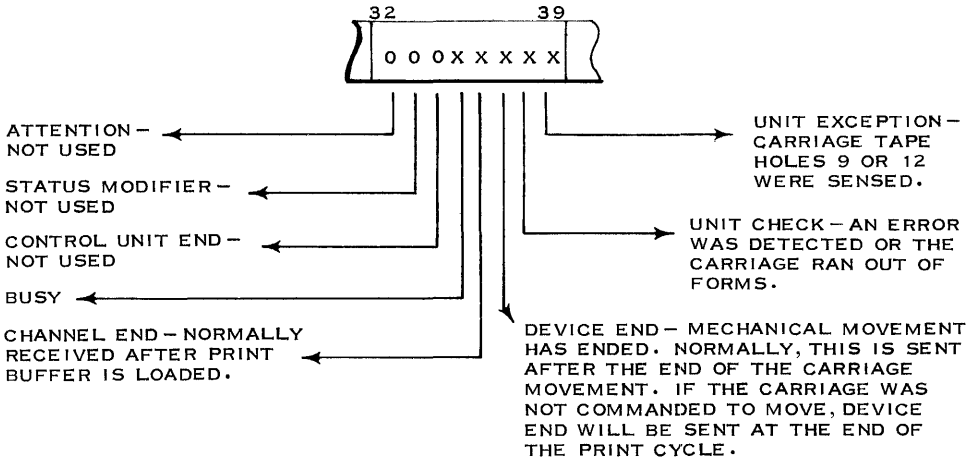
b. A single space will occur after the first line of print.
A triple space will occur after the second line of print.
The command byte in CCW2 is ignored because of data chaining.

c. Two; One might occur after the buffer has been loaded by CCW3 for the second line of print. When the triple space has finished, another I/O interrupt might occur. The I/O interrupts depend on the system mask in CPU's PSW.

d. Assuming that the first interrupt (channel end) is allowed, the CSW would look like this:



The status byte of a 1443 N1 is broken down as follows:



Besides the write command, the 1443 N1 can also do the control and sense commands. The control command is used to obtain carriage operation without printing. This is shown as follows:

0	0001	X11	-	Single space
0	0010	X11	-	Double space
0	0011	X11	-	Triple space
1	0001	X11	-	Skip to 1
↓	↓	↓		↓
1	1100	X11	-	Skip to 12
Skip if 1	Amount of space or skip	Control Command		

Once the control command has been accepted, channel end will be sent to the channel and carriage movement will begin. When the carriage movement has finished, device end will be sent.

Given the following CCW's and a 1443 N1:

CCW1	1100080040000078
CCW2	1B00000040000001
CCW3	0100080000000078

a. How many lines will print? _____
b. How many spaces are after line #1? _____
c. How many spaces are after line #2? _____
d. When will channel end be sent? _____
_____
_____
e. When will device end be sent? _____
_____
_____

---

a. Two
b. Five; Two after the print cycle and three more because of the control command.
c. None
d. After the printer buffer has been filled as a result of CCW3.
e. After the print cycle resulting from CCW3.

The sense command is usually given to a 1443 N1 as a result of detecting either unit check or unit exception in the CSW. The sense command is used to read into main storage from the 1443 N1 one byte of sense data. This byte will give further information as to what caused the unit check or unit exception. The sense command byte is XXXX0100. The byte of sense data placed in main storage by the sense command would have this meaning:

Bit 0	Command reject (the 1443 N1 received a command byte that it couldn't accept such as read backward).
Bit 1	Not ready because of such things as (1) out of forms, or (2) cover interlock not made.
Bit2	Bus Out Check - parity error on the standard interface.
Bit 3	Equipment Check - error detected within the printer.
Bit 4 & 5	Typebar selection (either 52, 13, 39 or 63 character set)
Bit 6	Nine hole sensed in carriage tape during last write or control command.
Bit 7	Twelve hole sensed in carriage tape during last write or control command.

By inspecting the sense data byte, the CPU program can determine what caused the unit check or unit exception in the CSW. The CPU program can then take appropriate action.

For example:

After the I/O interrupt, the CPU program inspects the CSW and finds the unit exception bit is set. It would then issue a "start I/O" instruction for a sense command. The sense command would bring a sense byte into storage. If bit 7 of the sense byte is set to 1, it would mean that the 12 hole in the carriage tape had been sensed. CPU could then issue a "start I/O" instruction to cause an overflow (skip to 1) with a control command.

You should now be familiar with the operations of the 2400 series magnetic tape units, the 1442 N1 read-punch and the 1443 N1 printer. Let's now take a look at the standard interface.

System/360 Input/Output Operations

SECTION III LEARNING OBJECTIVES

At the end of this section you should be able to do the following:

1. Explain the meaning of the following terms:

   Initial selection
   Data handling sequence
   Channel ending sequence

2. State the difference between the bus in lines and the bus out lines.

3. State the function of the tag lines.

4. State how I/O device priority is established.

Standard Interface

The set of communication lines between the channel and the control units has been referred to as the Standard Interface. The standard interface is also known as the System/360 I/O Interface. Each channel in a System/360 has its own I/O interface lines.

The I/O interface from a channel can accommodate a maximum of eight control units. This is due to the electrical considerations of the cabling involved. Through the eight control units, a maximum of 256 I/O devices can be addressed. This is the limit of the 8 bit address for an I/O device. Of course, the actual number of I/O devices on a channel may be quite less depending on the control units and I/O devices involved. For instance, if eight tape control units are on a channel, a maximum of 64 tape units can be accommodated. This is because each tape control unit can only accommodate eight magnetic tape units.

The I/O interface provides a uniform method of connecting I/O control units to the System/360 channels. The I/O interface consists of 34 lines which provide for:

1. Transfer of a byte from the control unit to the channel (9 lines).

2. Transfer of a byte from the channel to the control unit (9 lines).

3. Signals to and from the channel to identify whether the byte on the interface is an I/O unit address or a command, data, or status byte. (6 lines)

4. Controls for selecting a specific control unit and interlocking to the channel. (7 lines)

5. Special controls such as metering lines. (3 lines)

The following is a list of the I/O interface lines:

	NAME OF LINE	ABBREVIATIONS
BUS OUT (Channel to I/O)	Bus Out Position P	Bus Out P
	Bus Out Position 0	Bus Out 0
	Bus Out Position 1	Bus Out 1
	Bus Out Position 2	Bus Out 2
	Bus Out Position 3	Bus Out 3
	Bus Out Position 4	Bus Out 4
	Bus Out Position 5	Bus Out 5
	Bus Out Position 6	Bus Out 6
	Bus Out Position 7	Bus Out 7
BUS IN (I/O to channel)	Bus In Position P	Bus In P
	Bus In Position 0	Bus In 0
	Bus In Position 1	Bus In 1
	Bus In Position 2	Bus In 2
	Bus In Position 3	Bus In 3
	Bus In Position 4	Bus In 4
	Bus In Position 5	Bus In 5
	Bus In Position 6	Bus In 6
	Bus In Position 7	Bus In 7
TAGS (For identifying the byte on the bus)	Address Out	Adr-Out
	Address In	Adr-In
	Command Out	Cmd-Out
	Status In	Sta-In
	Service In	Srv-In
	Service Out	Srv-Out
SELECTION CONTROLS	Operational Out	Op-Out
	Operational In	Op-In
	Hold Out	Hld-Out
	Select Out	Sel-Out
	Select In	Sel-In
	Suppress Out	Sup-Out
	Request In	Req-In
METERING CONTROLS	Metering Out	Mtr-Out
	Metering In	Mtr-In
	Clock Out	Clk-Out

All I/O interface lines are identified as either in or out lines. This is with reference to the channel.

Lines going to the channel from the I/O control units are identified as _____ (in/out) lines.

---

in

Lines going from the channel to the control units are identified as _____ (in/out) lines.

---

out

Page 121 is a tear-out page. Remove it from this book and use it as reference material for the rest of the book.

When the channel wishes to send a byte to one of the control units, it would put it on the _____ (bus in/bus out) lines (refer to the illustration on tear-out page 121).

---

bus out

The purpose of the six lines known as tags is to identify the byte on the bus. When the channel places the address of an I/O unit on the bus out, it would identify it by raising (activate) the tag line known as _____ _____.

---

address out

Whenever the channel wishes to send a command to an I/O unit, it would put the command byte on the _____ _____ lines.

---

bus out

With the command on the bus out lines, the channel would then raise the _____ _____ tag line.

---

command out

Whenever the channel is servicing an I/O unit by putting a data byte on the bus out, it would raise the _____ _____ tag line.

---

service out

The channel can place any one of the following bytes on the bus out lines. Indicate the name of the line that the channel would bring up to identify each particular byte on the bus out lines.

	Byte	Tag
1.	Address of I/O Unit	_____
2.	Command Byte	_____
3.	Data Byte	_____

---

1. Address Out
2. Command Out
3. Service Out

The I/O control unit can also put three types of bytes on its bus (the bus in lines). They are:

1. Its address
2. Its status byte
3. Data bytes

The 1442 N1 read-punch has read a column and wishes to send a character to the channel. The 1442 N1 would put the byte on the _____ _____ lines.

---

bus in

When the data byte is on the bus in lines, the 1442 N1 would raise the _____ _____ line.

---

service in

At the end of channel transmission, a 1442 N1 would send a status byte to the channel. To do this, the 1442 N1 would put the status byte on the _____ _____ lines and raise _____ _____.

---

bus in
status in

Occasionally an I/O device needs to identify itself to the channel. The I/O device would put its address on the _____ _____ lines and raise _____ ____.

---

bus in
address in

Indicate the name of the line, an I/O control unit would bring up to identify each of the following on the bus in lines.

	Byte	Tag
1.	Address of I/O unit	_____
2.	Data Byte	_____
3.	Status Byte	_____

---

1. Address In
2. Service In
3. Status In

Whenever a byte is taken off a bus by the channel or control unit, the receiving unit will then respond with an appropriate signal. For instance, during a read operation, the control unit will place the data byte on the bus in lines and signal service in. When the channel has taken the data byte and put it in one of its registers, it will signal back with service out.

There is a common meaning to all signals or signal sequences on the I/O interface. For this reason, any I/O device that is designed to generate and receive these signals may be connected to the System/360 I/O interface. With the exception of the select out and select in lines, the I/O interface lines feed all control units in parallel. However, only one control unit will respond to the channel signals. This is because of a selection sequence which we will be describing.

Refer to the illustration on tear-out page 121. The illustration shows that the select signal originates at the channel. It progresses serially through all control units and returns to the channel. A control unit may either send the signal directly to the next control unit or it may take it through some logic before passing it on.

The select signal may be stopped by a control unit's logic so that it isn't propagated to the next unit. As a result, each control unit has a definite priority on the interface. The illustration shows that the control unit 2 has the lowest priority because the select signal goes through its logic last. Whether a control unit initially passes on the select signal or takes it through its logic depends on how its interface cabling is initially installed. As a result, the priority of a control unit on the interface is not dependent on its physical proximity to the channel.

Priority on the interface isn't too important on a selector channel. However, it is important on a multiplexor channel because of the time sharing I/O operations. It is customary to assign the highest priority to those I/O units with the faster character rates. The units with the slower character rates can wait longer to be serviced.

For any complete channel operation, there are at least three sequences of interface operation. They are:

1. Initial Selection Sequence (as a result of a "start I/O" instruction).

2. Data Handling Sequence (to transmit data bytes over the interface).

3. Channel Ending Sequence (to send status bytes containing channel end).

If device end wasn't sent during the channel ending sequence, there will be a fourth sequence later on for the status byte with device end.

There are many variations of these sequences depending on conditions within the channel and control units. There are also a number of "what if's" that could be covered but won't be. On the next few pages, we will briefly describe these sequences as they usually occur. We will assume that we are operating with a 2400 series magnetic tape unit on a selector channel. No other I/O units are in operation and all earlier I/O interrupts have been taken care of. Here is the program:

```
LA      1, 2048(0,0)
ST      1, 72(0,0)
SIO     384(0), 0
```

2048 ⟶ 02000F0000000005
3840 ⟶ F1F2F3F4F5

What channel is being used? _____

selector channel #1

What is the unit address of the magnetic tape unit being used? _____

10000000 (or if you wish to express the UA in hex, it would be 80).

What protection key will be used by selector channel #1 for this operation? _____

zero

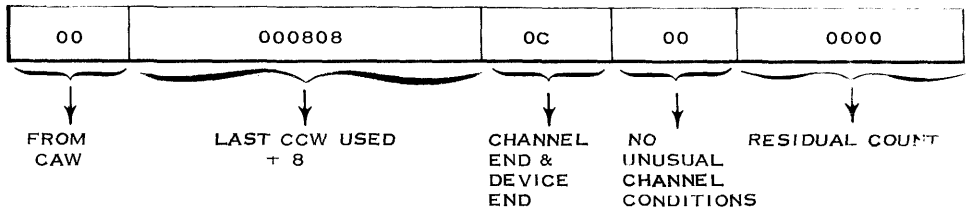
Are we going to do a read, write, sense or control command? Choose one. _____

read

There will be an incorrect length indication in the CSW unless the tape record is exactly _____ data characters long.

five

Assuming normal trouble-free completion of the operation, write the CSW that will be stored in location 0064 on the I/O interrupt.



For this tape read operation, there will be three general sequences of operation on the I/O interface of selector channel 1. The selector channel of course will be operating in burst mode only. That is, once selected the magnetic tape unit will remain interlocked with selector channel 1 until the end of the read operation. Let's take a look at the three sequences of operation, starting with initial selection.

The initial selection sequence will occur during the execution of the "start I/O" instruction. CPU will not disconnect and go on to the next instruction until this sequence is over. Basically, two things happen on the I/O interface during the initial selection sequence:

1. The channel sends the command byte to the I/O control unit.

2. The I/O control unit sends back a status byte to the channel.

The reason for sending the status byte is to see if the command can be initiated. If the status byte contains all zeroes, the command is initiated and the condition code in CPU's PSW is set to zero. If the command cannot be initiated, the condition code is set to one, two or three depending on the bits in the status byte. In either case, CPU disconnects after the condition code is set and continues on to the next instruction.

The instruction following a "start I/O" should usually be a "b_____ o_____ c_____".

"branch on condition"

Before looking at the I/O interface's initial selection sequence, let's examine a flow chart of the "start I/O" instruction and see where the initial selection sequence fits in the overall picture. Fill in the blanks and study the flowchart on tear-out page 122. (Answers are in the following frame.)

main storage
unit, channel
channel
channel
command, status
condition code

The following "branch on condition" instruction is executed after a "start I/O" instruction. What would it mean if the branch were successful? Refer to your Principles of Operation manual, if necessary. _____

BCR 7, 6

The I/O operation has not been started for some reason.

The following shows the significance of the condition code after a "start I/O" instruction.

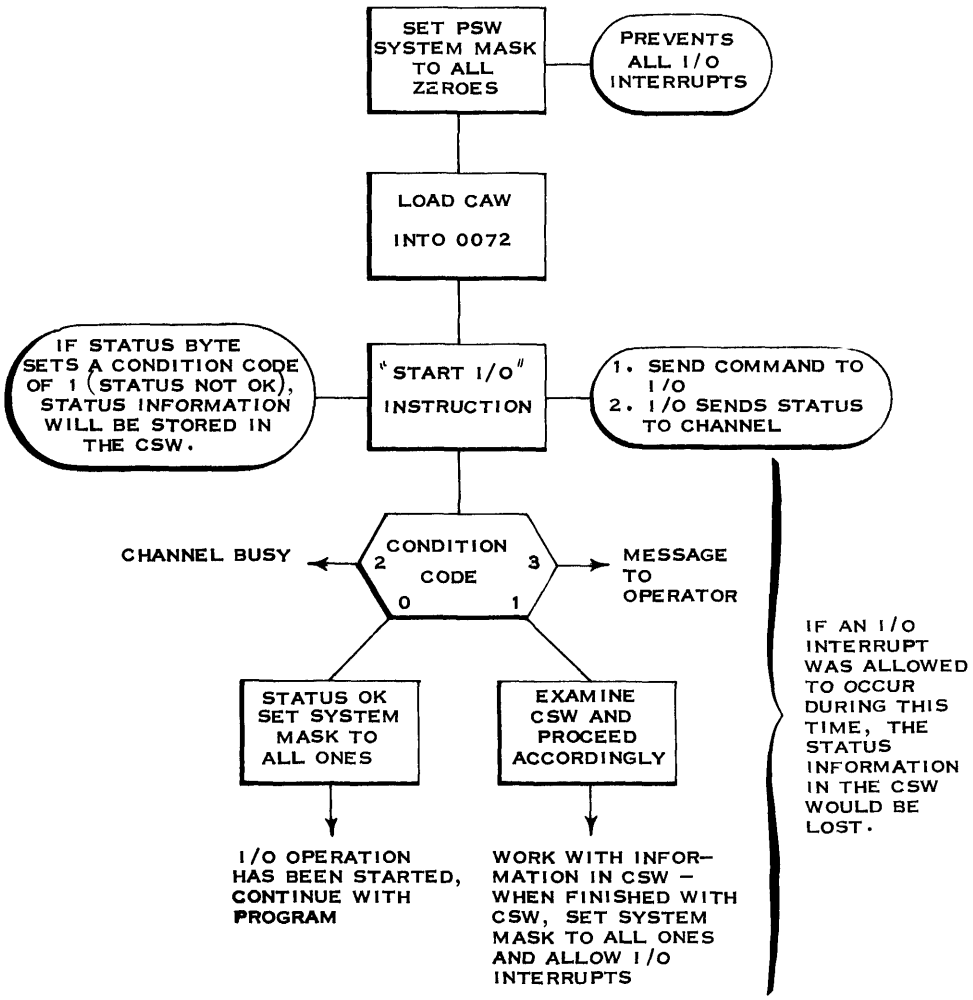
Condition Code

0	-	Operation started; everything okay.
1	-	A CSW will be stored containing the device status byte from the initial selection sequence as well as a channel status byte.
2	-	Operation not started because the channel or sub-channel was busy. That is, the channel is executing an operation initiated by a previous "start I/O" instruction or has a pending interrupt condition.
3	-	Operation not started because the addressed I/O unit either (1) is not in the system configuration, or (2) is in CE test mode (off line).

It is possible for an I/O interrupt to occur during the fetching of any instruction. Suppose for instance, that an I/O operation on selector channel 2 is completed during the execution of a "start I/O" instruction with selector channel 1.

If the "start I/O" instruction had resulted in setting condition code 1, information would have been stored in the CSW at location 0064. Instructions will be used to examine the CSW and prepare to handle the "other than OK" status of the I/O device.

During this examination and handling of the CSW it is possible that an I/O interrupt might occur due to the completion of the I/O operation on selector channel 2. A new CSW would then be stored and destroy the previous information concerning the "start I/O" instruction. This is undesirable. To avoid this, it is always best to mask off I/O interrupts prior to executing a "start I/O" instruction. The program flow chart would probably look like the following chart.



We will now examine the general flow of signals on the I/O interface for an initial selection sequence. You may refer to the flow chart of the initial selection on tear-out page 122 and the cable on page 121 to see where this sequence fits in.

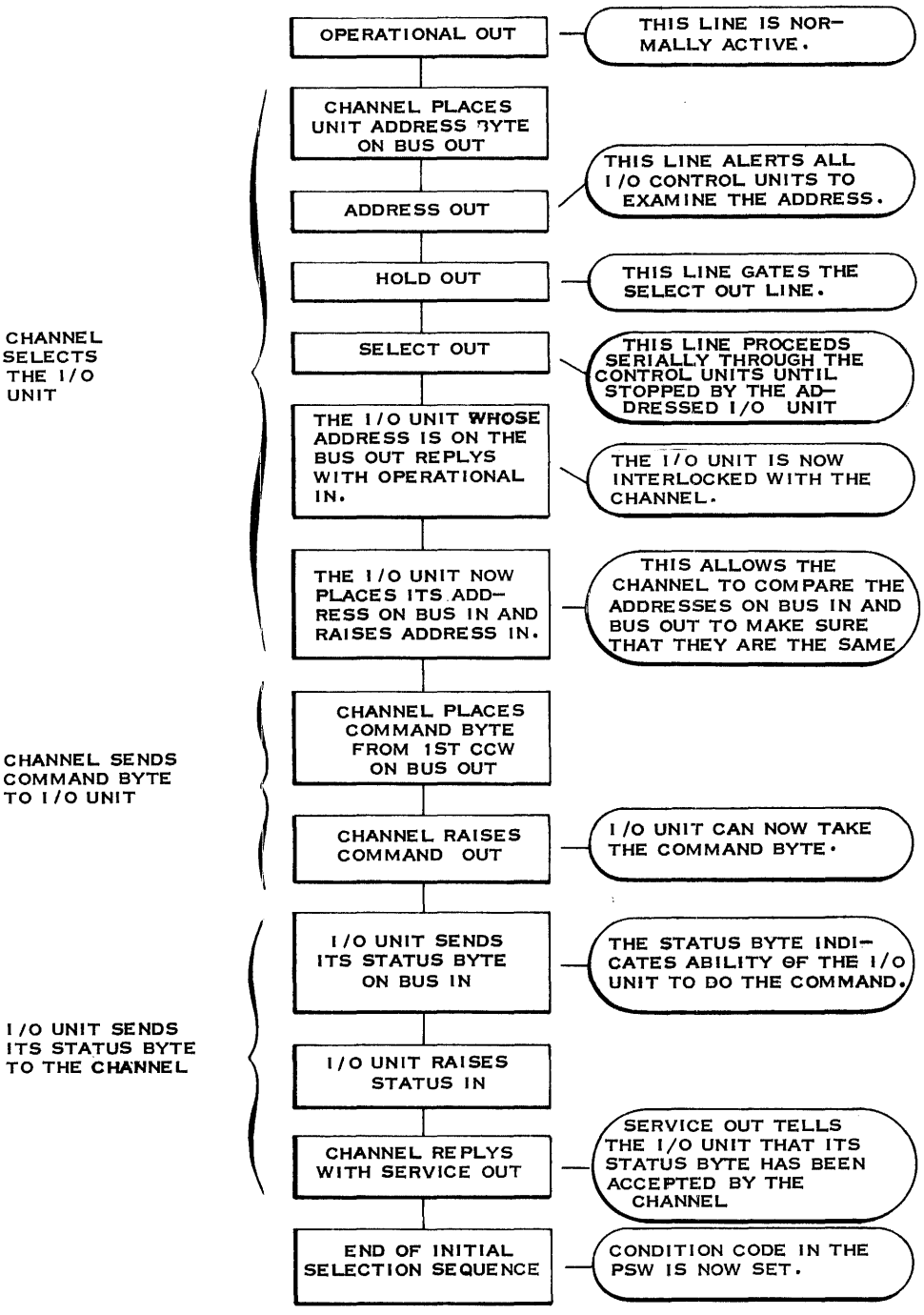
Name two functions accomplished by the initial selection sequence:

1. _____
2. _____

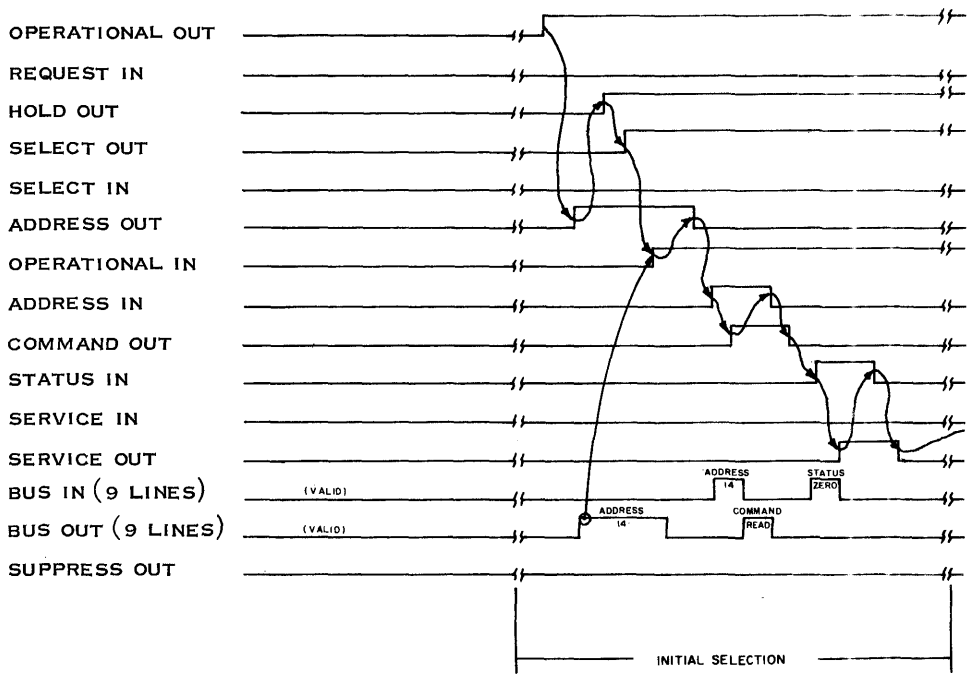
---

1. Channel sends command byte to I/O control unit.
2. I/O control unit sends its status byte to the channel.

The following is a generalized flow chart of the initial selection sequence:



The following sequence chart will show the cause and effect of the signals that are generated during the initial selection sequence.



Notice the line and arrows show the cause and effect sequence of the signal. Note also that the select out, hold out, and operational in lines remain up after this sequence. This is because we are using a selector channel which can only operate in burst mode. These lines remaining up keep the channel and I/O unit interlocked.

How does the channel select an I/O device? _____

By placing its unit address byte on the bus out and signaling address out to all the control units.

How does a selected I/O device reply to its selection? _____

By placing its unit address byte on the bus in and replying with address in. Note: The address that is placed on bus in is not the same physical address as on bus out. Instead, it comes from the address that is wired into the I/O unit. Of course, the two addresses should be equal.

How does the channel tell the I/O device what operation to do? _____

It places the command byte on bus out and signals command out.

What does the I/O device do after it receives the command byte? _____

The I/O device puts its status byte on bus in and signals status in.

What does the channel do with the status byte? _____

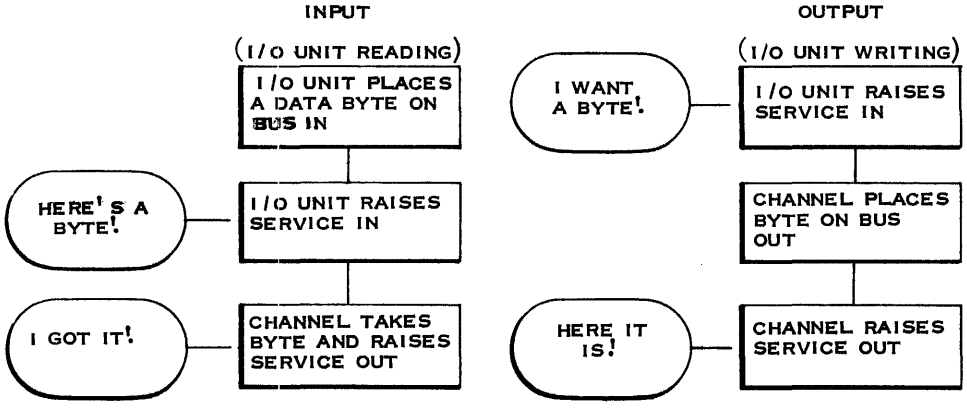
DATA HANDLING SEQUENCE

It uses it to set the condition code. Also, it will put in the CSW at location 0064 if the condition code is set to 1.

Since we are using a selector channel which operates in burst mode, the channel and I/O units remain tied together after the initial selection sequence. Which interface lines are used to interlock the channel and I/O unit? (Refer to preceding illustration.) _____

Select out, and hold out from the channel and operational in from the I/O unit.

The data handling sequence during burst mode consists of placing a byte on either bus in (read) or bus out (write). The I/O unit commences a data handling sequence by signalling service in. The sequence is terminated when the channel signals service out. The following flow charts will show the data handling sequence for both input and output operations on a channel that is operating in burst mode.



NOTE: For channels operating in multiplex mode, the I/O device would have to be re-selected for each data handling sequence.

On an input operation, how does an I/O device notify the channel that it has a data byte to be stored? _____

By placing the byte on bus in and signalling service in.

How long would the previous data byte remain on bus in? _____

Until the channel says it has the byte by signalling service out.

On an output operation how does the channel know that it should place a data byte on bus out? _____

The I/O unit will signal service in.

How many times will the data handling sequence be repeated during an operation? _____

CHANNEL ENDING SEQUENCE

Once for each data byte.

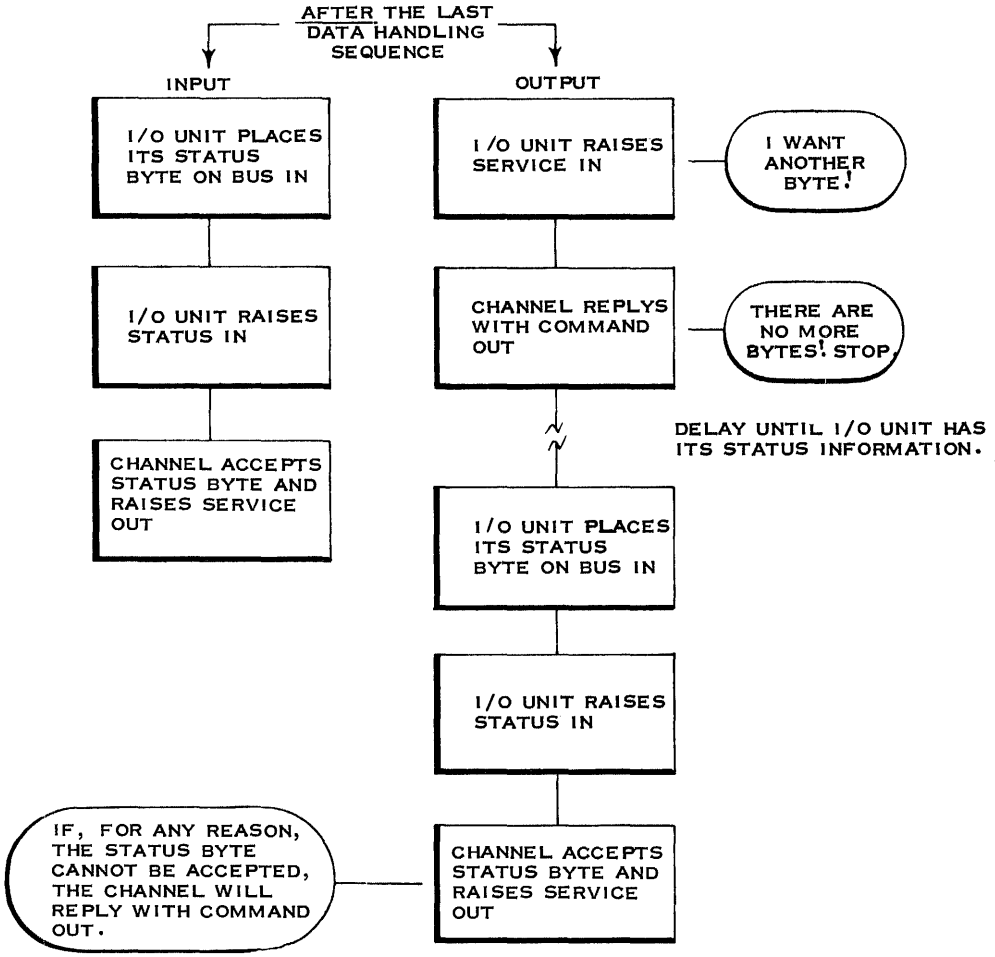
The next I/O interface sequence is the one in which the channel operation is terminated. The prime function of the channel ending sequence is to supply the I/O device's status byte to the channel.

On an output operation, the channel ending sequence is initiated because the count from the CCW was reduced to zero.

On an input operation, there are three possible ending situations:

1. Count field is equal to the number of data bytes in the input record.
2. Count field is greater than the number of data bytes.
3. Count field is less than the number of data bytes.

For our purposes we will take the case of the data bytes being equal to the count field. The following flow charts will show the channel ending sequence for both input and output operations.



On an output operation, how does the channel tell the I/O unit to stop? _____

After the last data byte has been transferred, the count from the CCW is reduced to zero. The next time the I/O unit says service in, the channel will tell it to stop by replying with command out.

On an input operation, how does the I/O unit notify the channel that it has finished transmitting data bytes? (That is, the number of data bytes equals the CCWs count field.) _____

The I/O unit comes in with its status byte and signals status in.

What is the purpose of sending a **status** byte during the channel ending sequence? _____

This status byte will be placed in the CSW on the pending I/O interrupt.

What bit would you always expect to see in the status byte received during this sequence? _____

Channel end; Other bits may also be present such as device end.

If device end is not in the channel ending status byte, the I/O unit will send another status byte later on that will contain device end.

The interlock between the channel and the I/O unit is dropped after the channel ending sequence. To submit device end at a later time, the I/O unit will have to initiate a selection sequence. It does this by putting its address on bus in and raising address in.

System/360 Input/Output Operations

	Section I:	Introduction to I/O Operation
	Section II:	I/O Devices
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	Section V:	Channel Error Conditions
	Section VI:	Initial Program Load Procedure
	Section VII:	Analyzing I/O Programs

SECTION IV LEARNING OBJECTIVES

At the end of this section, you should be able to do the following:

1. State the names of the four I/O instructions.

2. State the functions of the "start I/O" and "test I/O" instructions.

I/O Instructions

The "start I/O" instruction is used to initiate a channel command for an input or output operation. There are also three other instructions for I/O operations. They are:

Test I/O
Test Channel
Halt I/O

Like the "start I/O" instruction, these other I/O instructions are privileged operations. That is, the four I/O instructions will be executed only when the system is in the _____ (supervisor/problem) state.

---

supervisor

If an I/O instruction is fetched while the system is in the problem state, a _____ _____ will result.

---

program interrupt

The CPU initiates a channel operation by use of a "_____ _____" instruction.

"start I/O"

The CPU knows whether or not the channel operation was initiated by interrogating the _____ _____ in the PSW.

---

condition code

Normally the channel operation is overlapped with CPU processing. How then does CPU know when the channel operation has been completed?

_____

By an I/O interrupt.

Describe briefly what happens on an I/O interrupt? _____

_____

_____

_____

The channel's CSW is stored in location 0064 and the PSWs are switched. That is, the current PSW is stored as the I/O "old" PSW. The I/O "new" PSW is then brought out and becomes the "current" PSW. All of this is done automatically by the system and does not require any instructions.

How many I/O "new" PSWs are there? _____

---

one

How many channels can cause an I/O interrupt? _____

---

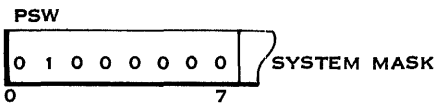
seven; There is one multiplexor channel and six selector channels that are possible.

How can CPU prevent an I/O interrupt? _____

By setting the system mask in the PSW to all zeroes. This will mask I/O interrupts from any of the channels.

How can CPU allow I/O interrupts selectively by channel? _____

By setting the appropriate bit(s) in the system mask.



The above system mask will only allow I/O interrupts from _____ _____.

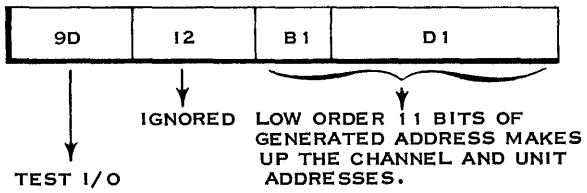
---

selector channel 1

I/O operations can be occurring simultaneously on all of the channels of a given System/360. As a result, it is possible that more than one operation may end at the same time and want to interrupt CPU. Since there is only one I/O interrupt, the hardware must have an assigned priority in the case of simultaneous requests for an interrupt. The assignment of priority among channel requests is based on the type of channel. The priority of selector channels is based on their addresses, with selector channel 1 having the highest priority. The priority of the multiplexor channel will depend on which model of System/360 is involved.

As was shown earlier, this assigned priority can be changed by the CPU program. This is done by selectively setting the PSWs system mask to allow an interrupt by the desired channel.

To allow the program to select which I/O device on a channel has top priority, the "test I/O" instruction can be used. This instruction uses the SI format and is shown below.



The "test I/O" instruction does not use a CAW or CCW. Its function is to test the status of an I/O device and set the condition code accordingly. The resulting condition code is as follows:

0 Available
1 CSW was stored and contains status information concerning the I/O device.
2 The channel or sub-channel is busy.
3 The addressed I/O unit is not operational.

Simple processing applications may have only one program state. That is, the CPU would always be in the supervisor state and no instructions would be executed in the problem state. There would not be a supervisor program. The entire program would be a problem program but would operate in a supervisor state.

When the System/360 is programmed in this manner (CPU always in supervisor state) the following occurs;

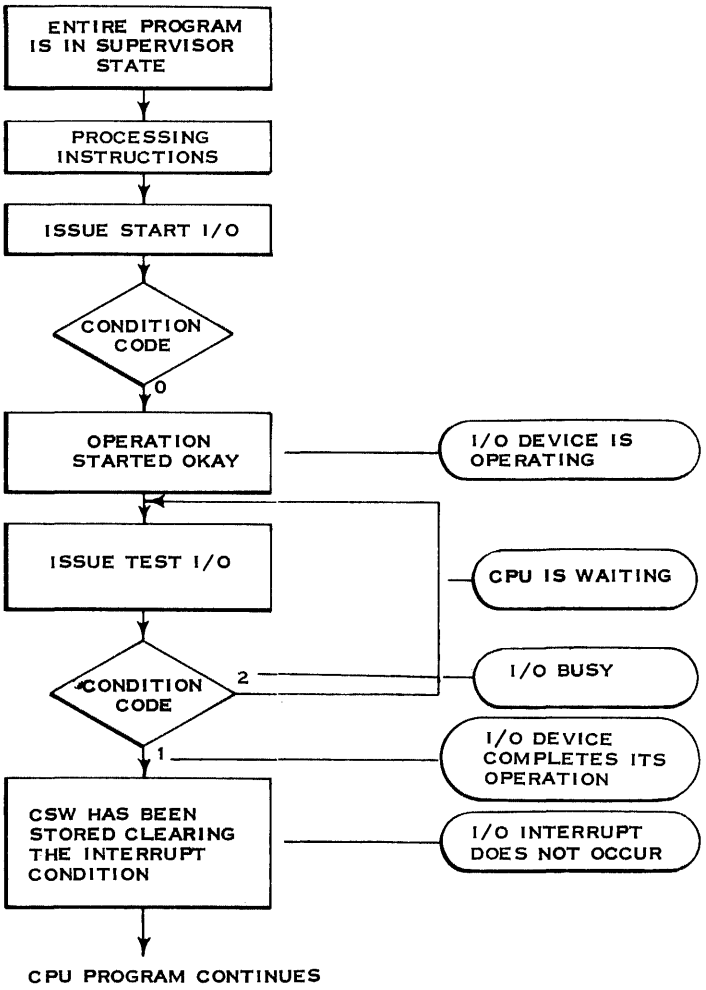
1. No I/O interrupts occur. They are prevented by setting the system mask in the PSW to all zeros.

2. I/O operations and processing are not overlapped.

   a. The CPU will have to wait until the I/O operation is completed.
   b. The "test I/O" instruction is used to cause the CPU to wait for the completion of the I/O operation.

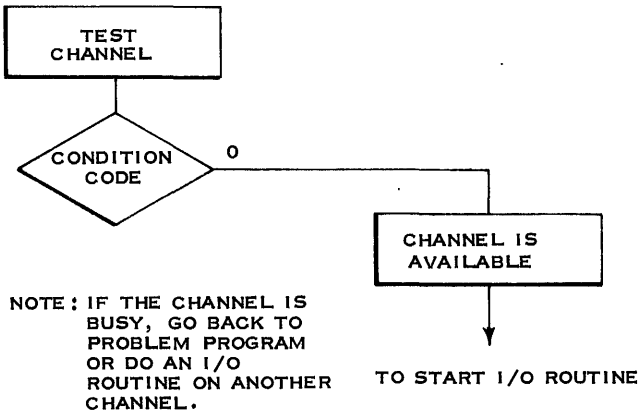
The following frames and flowchart illustrate one of the uses of the "test I/O" instruction.

The "test I/O" instruction is to be used to store the CSW rather than allowing the I/O interrupt to do it. The following flow chart will show how the "test I/O" instruction could be used to hold up processing until the I/O operation is finished. Upon completion of the I/O operation, the CSW is then stored without an interrupt. The CSW can then be examined by the CPU program to see if the operation was completed without any unusual conditions.



Read the description of the "test I/O" instruction in the Input/Output Operations section of your Principles of Operation manual.

Another I/O instruction is "test channel". This instruction is used to test only the condition of the channel. It does not clear any pending interrupts. It can be used along with the "branch on condition" instruction to operate as a "branch on channel busy" instruction. The following flow chart will illustrate one use of this instruction.



Read the description of the "test channel" instruction in the Input/Output Operations section of your Principles of Operation manual.

The fourth and final I/O instruction is "halt I/O." This instruction is used to terminate an I/O operation earlier than normal. This would then allow an operation of higher priority to get started. Read the following areas of your Principle of Operation manual.

Halt I/O
Termination of Input/Output Operations
(approximately 5 pages)

System/360 Input/Output Operations

	Section I:	Introduction to I/O Operation
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	Section IV:	I/O Instructions
●	Section V:	Channel Error Conditions
	Section VI:	Initial Program Load Procedure
	Section VII:	Analyzing I/O Programs

SECTION V LEARNING OBJECTIVES

At the end of this section, when given a list of the CSWs channel status bytes bits, you should be able to state the function of each bit.

Channel Error Conditions

We concluded our discussion of the channel status word earlier in this manual without touching on the subject of channel detected errors. As you know, two of the bytes in the CSW are status bytes. One status byte is for the I/O device and one is for the channel. (Refer to tearout page 120. We covered the bits of the I/O device's status byte. They are as follows:

Bit 32	Attention
Bit 33	Status Modifier
Bit 34	Control Unit End
Bit 35	Busy
Bit 36	Channel End
Bit 37	Device End
Bit 38	Unit Check
Bit 39	Unit Exception

Bits 40-47 of the CSW make up the status byte for the channel. The channel's status byte is used mostly for depicting types of channel errors as shown below.

Bit 40	Programmed Control Interrupt (PCI)
Bit 41	Incorrect Length
Bit 42	Program Check
Bit 43	Protection Check
Bit 44	Channel Data Check
Bit 45	Channel Control Check
Bit 46	Interface Control Check
Bit 47	Chaining Check

PROGRAMMED CONTROLLED INTERRUPT (PCI)

You should already be familiar with the function of bit 40 and 41. Bit 40 is the PCI bit. It will be set in the CSW when an I/O interrupt is taken because of the PCI _____ _____ in a CCW.

flag bit (Bit 36 of the CCW)

You may want to review the programmed controlled interrupt at this time, by reading its description in the Input/Output Operations section of your Principles of Operation manual.

INCORRECT LENGTH

Bit 41 of the CSW is used to indicate incorrect length. This bit will usually be set if the number of bytes read does not agree with the _____ field in the CCW.

count

If a CCW with a count field of 90 is used to read an IBM card, the incorrect length bit in the CSW _____ (will/will not) be set.

will

The setting of the incorrect length bit in the CSW can be prevented if the _____ flag in the CCW is set.

SILI

If a CCW with a count field of 24 and a SILI flag is used to read an IBM card, incorrect length bit in the CSW _____ (will/will not) be set.

will not

If on an output operation, the I/O device asks for another byte after the count has been reduced to zero, the incorrect length bit will be set. When you were introduced to the channel ending sequence earlier in this manual, you saw that this was the usual sequence for an output operation. That is, an I/O device such as a tape unit would ask the channel for another byte. The channel would then tell it to stop.

It would be _____ (normal/not normal) for the incorrect length bit to set in the CSW after a tape write operation.

normal

Although it would be normal for the incorrect length bit to be set after a tape write operation, it would not be desirable. Therefore, the CCW for a tape write operation would usually have the _____ flag bit set.

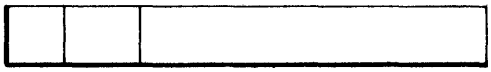
SILI

The remaining bits of the channel's status byte are used to indicate errors detected by the channel. Errors detected by the I/O device set the _____ _____ bit in the device's status byte.

unit check

Bit 42 of the CSW is used to indicate a program check that is detected by the channel. Most of the program checks have to do with incorrect setting up of the CAWs and CCWs.

Label the fields of the CAW.



Bits 0-3 of the CAW become the protection key for the channel operation. This key can be any number from 0 to 15. However, if the storage protection feature is not installed, this key must be zero. If not, the program check bit in the _____ will be set.

CSW (or the channel's status byte in the CSW)

Whenever the CAW has been shown in this book, bits 4-7 have been zero. If these bits are anything but zero, the _____ will be set.

program check bit in the CSW

Name two items that can set the program check bit in the channel's status byte.

1. _____
2. _____

1. The CAW has a non-zero protection key and the system does not have the storage protection feature.
2. Bits 4-7 of the CAW are not zero.

Bits 8-31 of the CAW are the address of the first CCW to be used for a channel operation. Since the CCW is a doubleword, this address must be divisible by _____.

eight	If the command address in the CAW is not divisible by eight, the _____ will be set.
program check bit in the channel's status byte	Besides being divisible by eight, the command address must be a valid one for the particular system. If the command address in the CAW is 16000 and the system has an 8K main storage, the _____ will be set.
program check bit (bit 42) in the channel's status byte	Name four items in the CAW that can cause the program check bit in the CSW to be set to 1. 1. _____ 2. _____ 3. _____ 4. _____

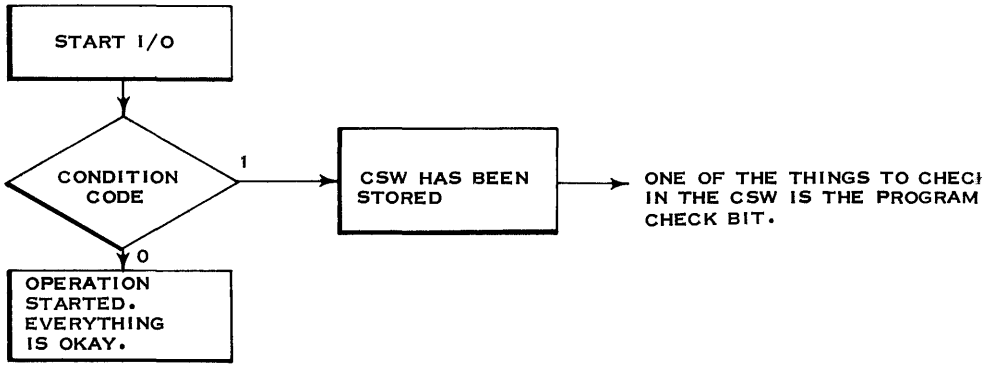
1. A non-zero protection key on a system without the storage protection feature. Note: This feature is standard equipment on models 50-70.

2. Bits 4-7 of the CAW are non-zero. There is no outstanding reason why these bits must be zero. However, this now allows these bits to be used at a later date for expansion without having to rewrite programs.

3. The command address in the CAW must be divisible by 8.

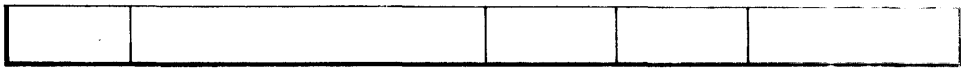
4. The command address in the CAW must be an available address.

If any of the program checks are detected in the CAW, the I/O operation is not started. Instead, the CSW is stored (with the program check bit set to 1) and the condition code is set to 01.



PROGRAM CHECK - CCW

The CCW must also be correctly set up or channel program checks will be detected. The CCW is a doubleword. Label its fields.



The program check bit in the CSW can be set as a result of an invalid command byte. If bits 4-7 of the command byte are set to zero, the command is invalid. The six I/O commands all have at least one of these bits set to 1. Which of the following hexadecimal command bytes are invalid. (Circle one or more.)

41
78
90
02
53

90

If the command byte of the 1st CCW specifies a transfer in channel (TIC), it is considered a channel program check. A program check is also detected when two successive transfer in channels are encountered during chaining operations.

Name three checks that are made on the command byte.

1. _____

2. _____

3. _____

---

1. Invalid Command; Bits 4-7 are zero.

2. 1st CCW specifies a TIC.

3. Two successive TICs during chaining operations.

Bits 8-31 of the CCW are the data address. If this address is not available on the system, a channel program check is detected.

If the data address in a CCW is 10,000 and the system has an 8K main storage unit, the _____ _____ bit in the CSW will be set.

---

program check

The data address in the CCW for a TIC command is the address of the next CCW. As such, this address must be divisible by _____.

---

eight

Name two checks made on the data address in a CCW:

1. _____

2. _____

---

1. The data address must be an available main storage address.

2. The data address in a TIC command must be divisible by eight.

Bits 32-39 of the CCW make up the flag byte. At the present time, only bits 32-36 are used for flag bits. However, to allow for future expansion, bits 37-39 must be zero or the program check bit in the channel's _____ byte will be set.

status

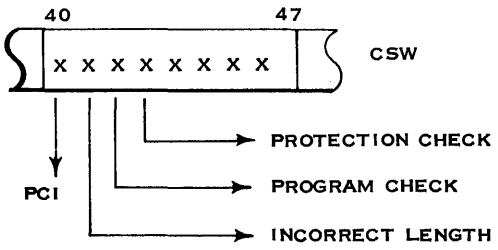
Bits 40-47 of the CCW are ignored and no check is made on them. Bits 48-63 make up the count field. The count field contains the number of bytes in the data area. As such, this field must not be _____.

zero

If the count field in a CCW is zero, a channel program check is detected. This will result in setting the program check bit in the CSW. However, if the command is a transfer in channel (TIC), no check is made on the flag or count fields.

PROTECTION CHECK

So far we have examined three bits of the channel's status byte. The next bit to examine is bit 43, which is used to indicate protection violations by the channel.



Anytime data is stored in main storage, the storage key for that block of 2048 bytes must match the protection key. The protection key for CPU operation is contained in the ___ ___ ___.

PSW

The protection key for channel operation is part of the information in the UCW. This protection key comes from bits 0-3 of the orignial _____.

CAW

If the protection key is zero, it does not have to match the storage key. A protection key of zero can be considered a "master key". If the channel's protection key is not zero, it must match the storage key or the _____ _____ bit in the CSW will be set.

CHANNEL DATA CHECK - CHANNEL CONTROL CHECK

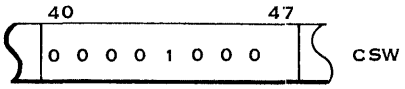
---

protection check

Parity errors during channel operation are handled in one of two ways depending on the model of System/360. In those models in which common circuitry is shared, a parity error may result in a normal machine check interruption just like any other CPU parity error. If the channel parity error does not result in a machine check interruption, it will then be indicated in the channel's status byte.

Bit 44 of the CSW is used to indicate parity errors on data bytes.

If the parity error occurs on a CCW, a data address, or a command address, bit 45 is set.

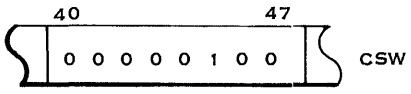


What would the above channel status byte indicate? _____

_____

_____

A parity error was detected in one of the data bytes. This includes parity errors detected on data bytes in main storage and I/O interface.



What would the above channel status byte indicate? _____

_____

_____

INTERFACE CONTROL CHECK

A parity error on a CCW or an address.

Bit 46 of the CSW is used to indicate an interface control check. It is usually a result of some malfunction on the part of the I/O device.

One of the possible interface control checks is detected during the initial selection sequence. If the address of the I/O unit that responds to the channel is not the right one, the channel will detect it as an interface control check and set bit 46 in the CSW.

CHAINING CHECK

Bit 47 is used for a chaining check indication. This bit is set when the input data rate is too fast and the channel cannot keep up with it.

Read the description of Channel Status Conditions in the Input/Output Operations section of your Principles of Operation manual.

System/360 Input/Output Operations

SECTION VI LEARNING OBJECTIVES

At the end of this section, you should be able to do the following:

1. State why the IPL is necessary.

2. State the function of the Load-Unit switches and the Load Key.

Initial Program Load Procedure

You have come a long way so far in studying Input/Output operations. You have studied the I/O instructions, CAWs, CCWs, and CSWs. You have learned about status bytes and channel errors. You have been introduced to the operations of some I/O devices and the I/O interface. In earlier books, you learned all about the PSW and CPU programming. There is, however, one last step to take. That step is getting the entire program to start. In other words, how do you get the initial instructions of any program whether it is a supervisor or a problem program into main storage.

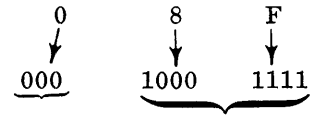
There is a common procedure in all models of System/360 for initially loading in a program. It is known as the initial program load procedure or IPL for short.

The basic function of the IPL is to read in 24 bytes of data from an I/O device.

On the system control panel there will be three rotary switches known as Load-Unit. These switches are used to set up the unit address of the I/O device to be used for the initial program load. The rotary switches are hexadecimal switches.

If the switches are set up to read 08F, what channel is being used for the IPL procedure? _____

The multiplexor channel



Multiplexor — Unit Address Channel

Because the high-order bit of the preceding unit address is set to 1, this indicates a shared sub-channel is being used for the unit control word (UCW).

UCW #_____ will be used. (If necessary, refer back to the Introduction to I/O Operations section for the answer.)

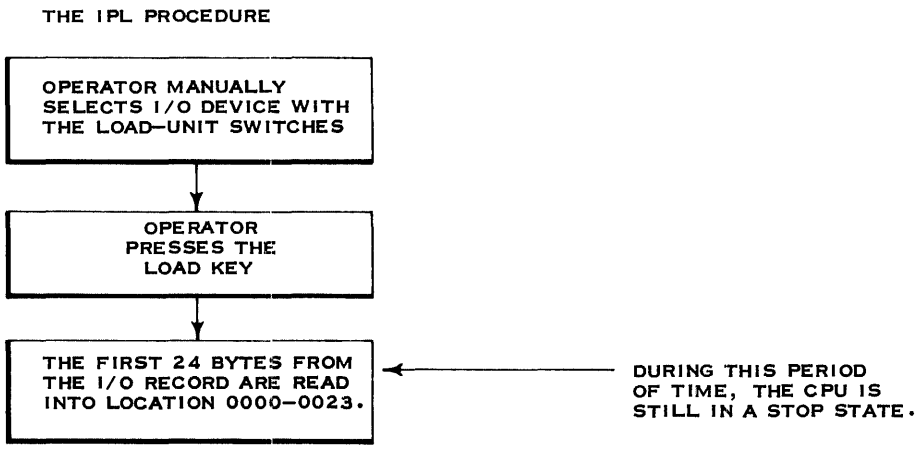
UCW #0

The next step in the IPL procedure after selecting the I/O device in the Load-Unit switches is to press the load key. This will cause the first 24 bytes of a record from the input device to be read into main storage starting at location 0000. No "start I/O" instruction, CAW, or CCW is needed for this phase of the IPL procedure.

In effect, however, the setting of the Load-Unit switches "simulates" the eleven low-order bits of the storage address generated during a "start I/O" instruction.

The pressing of the load key "simulates" the following:

1. A CAW with a protection key of 0.
2. A CCW with a read command, a data address at 0000, a count field of 24, and flag bits for commanding chaining and suppressing incorrect length indication. The following flow chart will illustrate what happens automatically (without additional programming) as a result of the IPL procedures.



If a card reader is being used for the IPL procedure, what happens to the information in columns 25-80? _____

It is not placed in main storage and of course, is ignored.

Since the IPL procedure simulates command chaining, we obviously need a CCW for the second I/O operation. The eight bytes that were read into locations 0008-0015 are used for the 2nd CCW. If the 2nd CCW also specifies chaining (either command or data), the bytes read into locations 0016-0023 are used for the third CCW.

The I/O operation that occurs after the first 24 bytes have been read into main storage will, of course, depend on the contents of the IPL bytes. They would probably be part of a common load program which can read in a supervisor program or any program desired.

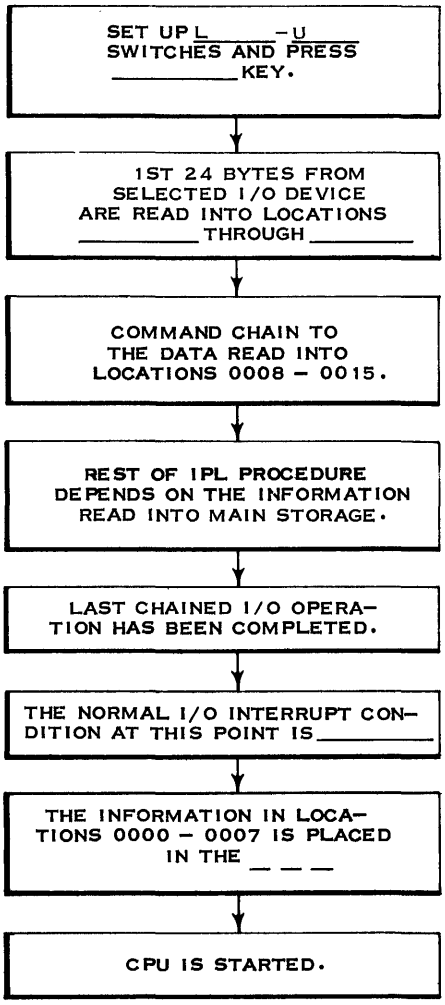
The total number of I/O operations that are performed before the IPL procedure is ended, may vary. This will depend on the common load program that is used and the format of incoming programs. However, since the initial read operation simulates command chaining, at least _____ I/O operations will be performed.

---

two

Of the 24 bytes initially read into locations 0000-0023, we used locations 0008-0015 (and possibly 0016-0023) as CCWs for chained operations. Wha do we use locations 0000-0007 for? They are used as the PSW to be used after the IPL procedure is ended. Also, there is no I/O interrupt as a result of the IPL procedure.

The following flow chart illustrates the complete IPL procedure. Fill in the blanks.



Load-Unit, Load
0000,0023
ignored, PSW

Read the description of Initial Program Load in the System Control Panel section of your Principles of Operation manual.

System/360 Input/Output Operations

	Section I:	Introduction to I/O Operation
	Section II:	I/O Devices
	Section III:	Standard Interface
	Section IV:	I/O Instructions
	Section V:	Channel Error Conditions
	Section VI:	Initial Program Load Procedure
●	Section VII:	Analyzing I/O Programs

SECTION VII LEARNING OBJECTIVES

At the end of this section, when given a simple I/O program which contains an input, output and wait state routine and is written in the supervisor state, you should be able to draw a flow chart of the program and explain how each instruction applies to the program.

Analyzing I/O Programs

Notice: This section of the input/output operations is very important. Your ability to learn the System/360 and ultimately, to service the system, will depend on your understanding of the following material. The material will require a good deal of effort and concentration. Dont' expect it to be easy. Use the Principles of Operation manual for reference and/or review whenever you are not sure of the details of an input/output operation.

Remember, now is the time and here is the place to learn.

PROGRAM #1

Given the following program and associated PSW and CSWs punched into one IBM card as follows: (Do not attempt to analyze the program at this time.)

COLUMNS		
1-2	BALR	1,0
3-6	LA	0,3840(0,0)
7-10	ST	0,0072(0,0)
11-14	SIO	64 (0),0
15-18	BC	7,50 (0,1)
19-22	TIO	128(0),0
23-26	BC	2,16 (0,1)
27-30	LA	0,3840 (0,0)
31-34	ST	0,0072 (0,0)
35-38	SIO	519(0),0
39-42	BC	7,50 (0,1)
43-46	TIO	519(0),0
47-50	BC	2,40 (0,1)
51-52	BCR	15,1
53-56	MVI	1,2
57-60	LPSW	0,0
61-68	CCW ⟶	02000F1000000050
69-76	CCW ⟶	01000F1000000050

Program #1 is punched into a standard IBM card. The IPL procedure wil be used to read this program into the system. The PSW to be used by this program is as follows:

In hex ⟶ 00 00 00 00 00 00 08 00

To use the IPL procedure, we need two IBM cards. Program #1 will be in the second card.

The first card will contain the PSW to be used by Program #1 (columns 1-8) as well as two CCWs to bring in the program card (columns 9-24).

Columns 1-60 of the Program #1 card are to be read into location 2048; columns 61-76 into location 3840.

Write in hex the data that must be punched into columns 1-24 of the 1st card used in our IPL procedure.

Columns 1-8 _____
Columns 9-16 _____
Columns 17-24 _____

Columns 1-8 0000000000000800
Columns 9-16 020008008000003C
Columns 17-24 00000F0000000010

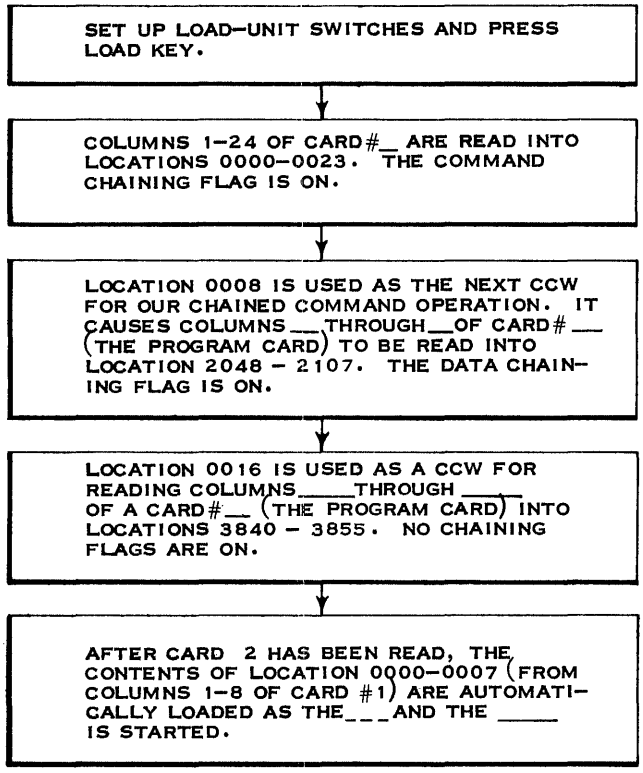
Columns 1-8 of the first IPL card contain the PSW that will be used at the end of the IPL procedure. Of course this should be the PSW for our program.

Columns 9-16 contain the command to read columns 1-60 of our program card (the second IPL card) into locations 2048-2107. The data chain flag bit is set. As a result, columns 17-24 are used for another CCW.

Columns 17-24 contain the data address and count to read columns 61-76 of our program card (the second IPL card) into locations 3840-3855.

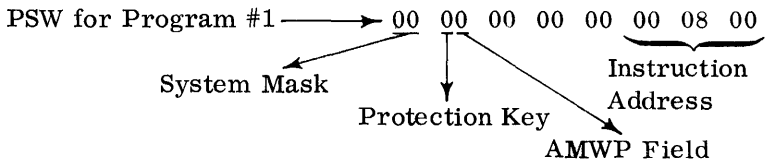
The following flow chart will illustrate the IPL action. Fill in the blanks.

IPL PROCEDURE FOR PROGRAM #1



1
1, 60
2
61, 76
2
PSW
CPU

Now that we have been able to read our program into the system, we are in a position to analyze it. First, let's analyze the PSW.



Will any I/O interrupts be allowed? _____

No

Will the program operate in supervisor state or in problem state?

_____

Supervisor State

Will any areas of main storage be protected from our program? ____

No

Will the program be able to handle any program check or machine check interrupts? _____

No; The program is written to operate without a seperate control or supervise type program. For sake of simplicity, the program is very limited, and is in the supervisor state.

Program #1 is listed on tear-out page 123. Tear out the page and use Program #1 for the following frames.

Take a few minutes to analyze Program #1. You may find it helpful to flow chart the program. Assume that a 1442 N1 read-punch unit is being used for input and a tape unit for output.

When you feel that you are ready, after analyzing Program #1, answer the following question:

Program #1 will do which of the following: (Circle one.)

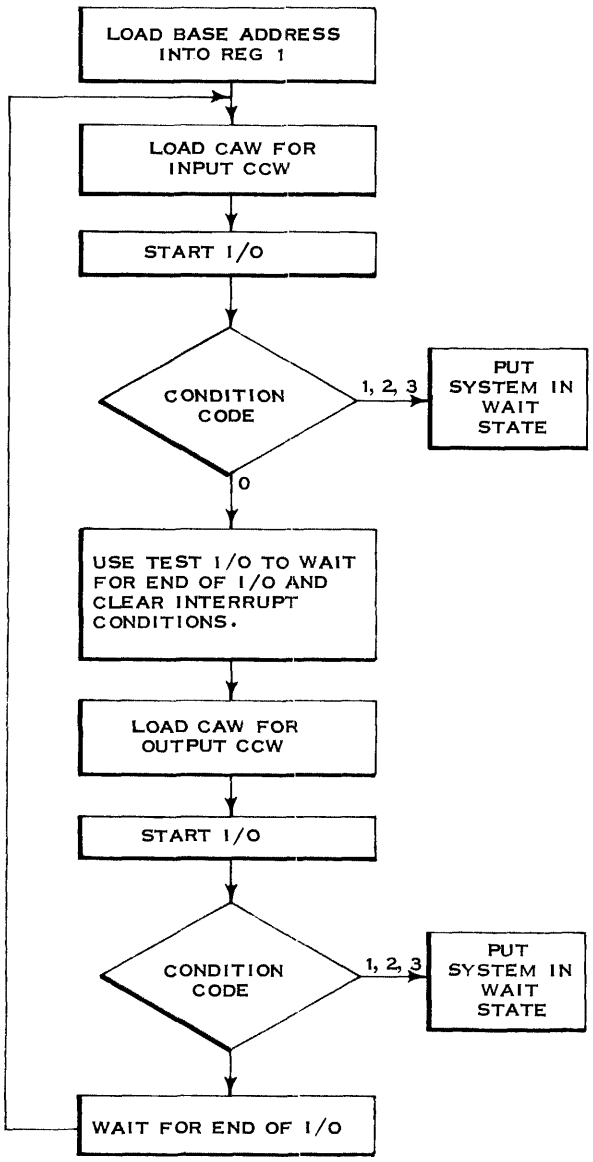
a. 80 character card records will be duplicated on tape. Data errors will be ignored.
b. 80 character card records will be duplicated on tape. Data errors will put the system in wait state.
c. One 80 character card record will be read and duplicated on tape. The system will then go into wait state.
d. One 80 character card record will be read. No tape record will be written and the system will go into wait state.
e. I am "snowed."

---

a. If you chose "a.", go to Program #2. If you chose answers b., c., or d., take a look at the following flow chart. Then see if you can arrive at the correct answer. If you still can't see the right answer, continue on below.

If you chose answer "e.", continue on with the following step by step analysis.

FLOW CHART OF PROGRAM # 1



What is placed in general register 1 as a result of the first instruction?

Bits 32-63 of the PSW.

Why doesn't a branch occur on the first instruction? _____

Because the R2 field is zero.

Show (in hex) the contents of general register #0 as a result of the second instruction. _____

00000F00

What is the purpose of the second and third instructions? _____

To place the address of the 1st CCW in the CAW location. A protection key of zero is also placed in the CAW.

After the "start I/O" instruction, a "branch on condition" is given. When will the branch not be taken? _____

Whenever the operation is started okay and the condition code is set to zero.

What is the purpose of the "test I/O" followed by "branch on condition"?

As long as the input operation is being executed, the program will branch back to the "test I/O". This allows us to wait until the input operation has finished.

The output routine is similar to the input routine. The output tape unit is on what channel? _____

Selector channel #2.

What channel was the input card reader on? _____

The multiplexor channel.

The BCR instruction at the end of the output routine is an unconditional branch. How does the system know where to branch to? _____

The "branch to" address is in general register 1. This will cause the program to branch back to the beginning of the input routine.

After the IPL procedure and the program is started, what is the contents of locations 0000-0007? _____

0000000000000800

What will be the contents (in binary) of location 0001 after the "move immediate" instruction is executed? _____

00000010

What happens after the "load PSW" instruction is executed? _____

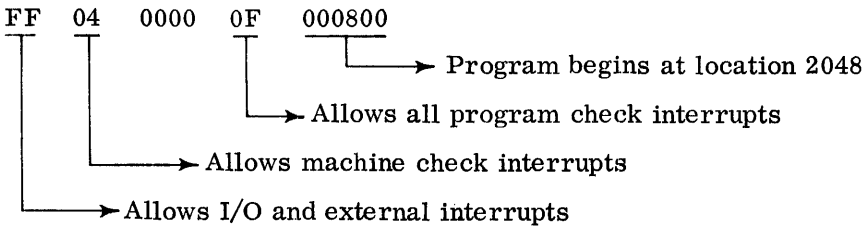
The new PSW will put the system in the wait state. As a result, the system will stop fetching instructions.

Normally, an I/O or external interrupt will take the system out of the wait state. In our case however, these interrupts are masked off. The IPL procedure can be used, however, to bring in another PSW and get the CPU started again.

PROGRAM #2

You are going to be asked to flow chart a program. The program will run in the supervisor state and allow all interrupts. Assuming that the program will begin at location 2048, write (in hex) the PSW that should be used at the end of an IPL procedure. The protection key will be zero.

_____



The program should do the following:

1. Read in one card from a 1442 N1 on the multiplexor channel. The hexadecimal unit address is 08. Use location 3840-3847 as the input CCW and locations 3848-3927 as the input area.

2. Put the system in wait state and depend on the I/O interrupt to get started again.

3. Check the channel status word. Mask off I/O interrupts and put the system in wait state if any of the following bits are set.
   a. Unit Check
   b. Unit Exception
   c. Any Channel Status Bit

4. The input record is in binary data format. Add positions 1-4 (Field A) of the input record and positions 11-14 (Field B). Change the result to EBCDIC ("convert to decimal" and "unpack").

5. Print only the results on a 1443 N1 printer on selector channel 1. The unit address is 0A (in hex). Use location 4096 for the output CCW and locations 4120-4127 as the output area. Print the result without spacing. By command chaining, use a control command to double space and then print the results a second time. Use locations 4096-4119 for the output CCWs.

6. Put the system in wait state and depend on the I/O interrupt to get started again.

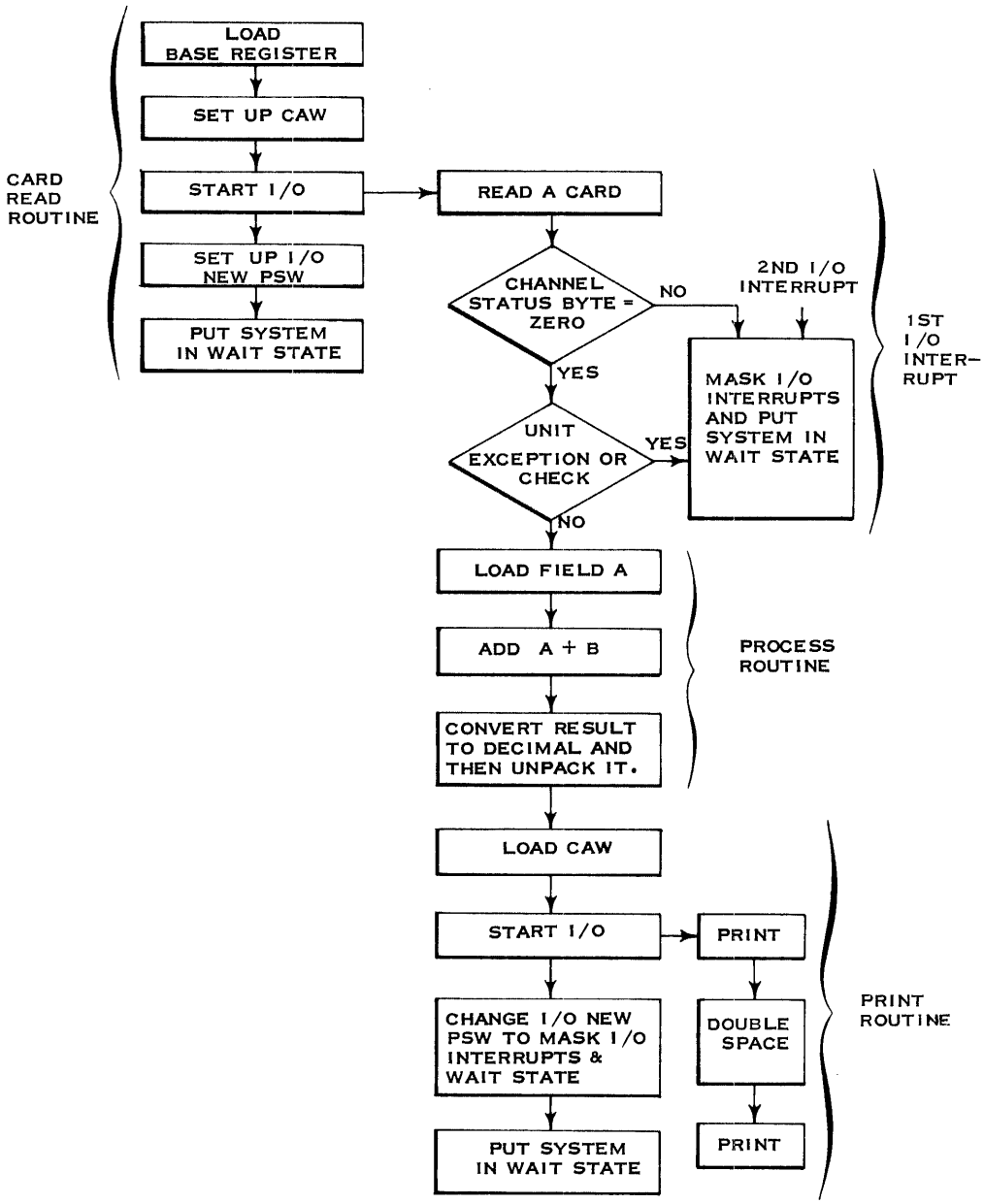
   The I/O interrupt should come after the printer buffer has been filled for the second time. Mask off the I/O interrupts and put the system in wait state. This is the end of the program.

Write (in hex) the input CCW at location 3840 and output CCWs at location 4096. Refer back to the description of the I/O devices if necessary to show the command bytes.

3840 _____
4096 _____
4104 _____
4112 _____

3840 02000F0800000050
4096 0100101840000008
4104 1300000040000001
4112 0100101800000008

Use the lower part of tear-out page 123 to draw a flow chart for the program. Then check it against the answer on the following flow chart.


LOAD BASE REGISTER
SET UP CAW
START I/O
SET UP I/O NEW PSW
PUT SYSTEM IN WAIT STATE
CARD READ ROUTINE
READ A CARD
CHANNEL STATUS BYTE = ZERO
NO
2ND I/O INTERRUPT
YES
UNIT EXCEPTION OR CHECK
YES
MASK I/O INTERRUPTS AND PUT SYSTEM IN WAIT STATE
1ST I/O INTER-RUPT
NO
LOAD FIELD A
ADD A + B
CONVERT RESULT TO DECIMAL AND THEN UNPACK IT.
PROCESS ROUTINE
LOAD CAW
START I/O
PRINT
CHANGE I/O NEW PSW TO MASK I/O INTERRUPTS & WAIT STATE
DOUBLE SPACE
PRINT
PUT SYSTEM IN WAIT STATE
PRINT ROUTINE

Your flow chart should be similar to the one shown on the previous page. Once you have resolved any differences, analyze the symbolic program on tear-out page 124. It should match the flow chart. You will probably have to use your Principles of Operation manual for reference on some of the instructions used in the program.

Assume that the IPL procedure is used to bring in the program. As a result, the initial PSW will also be in locations 0000-0007.

I hope you did not have too much difficulty in analyzing the preceding program. If you did, you should consider contacting someone who is familiar with the material and can help you overcome any obstacle.

This concludes your study of System/360 Input/Output operations.

Do you need a review? If you think that you may require a review of areas of this book, do the following:

Read the learning objectives at the beginning of each section.

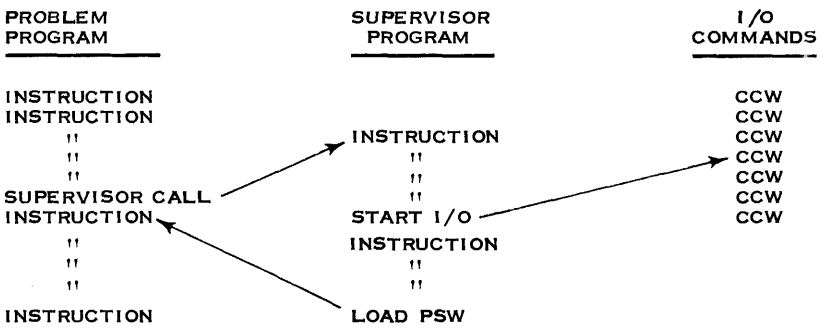
You should review only those areas where you think that you cannot do what the objective indicates.

After doing the following items, you will be finished with the System/360 Introductory Programming Course.

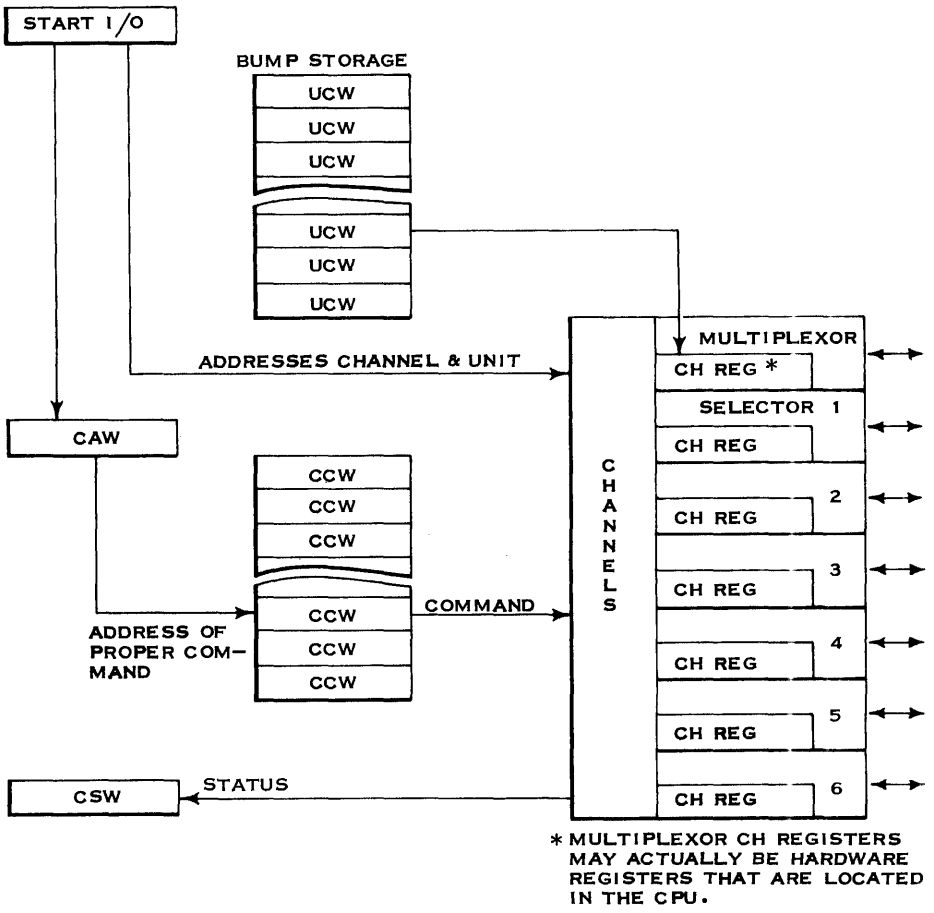
1. Fill out the Course Evaluation Sheet (located in the back of this book).

2. Ask the person that is administering this course for the Final Examination.

Alphabetical Index

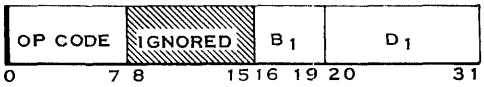


SIMPLIFIED PROGRAM OF AN I/O OPERATION



SIMPLIFIED DIAGRAM OF THE CONTROL OF AN I/O OPERATION

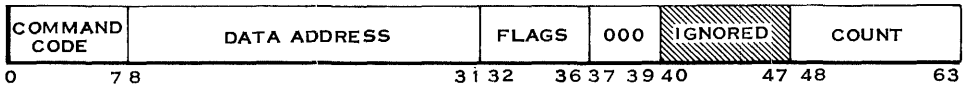
I/O INSTRUCTION



MNEMONIC = SIO XXX(X),X

CAW (CHANNEL ADDRESS WORD)

CCW (CHANNEL COMMAND WORD)

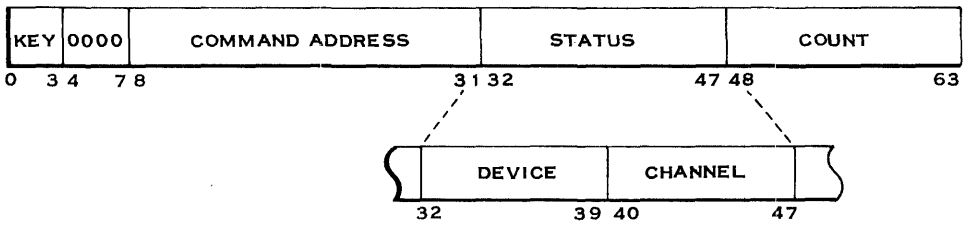


FLAG BIT DESIGNATION		FLAG BIT DESIGNATION	
32	CHAIN DATA	35	SKIP
33	CHAIN COMMAND	36	PROGRAMMED CONTROL INTERRUPT
34	SUPPRESS INCORRECT LENGTH INDICATION		

UCW (UNIT CONTROL WORD)

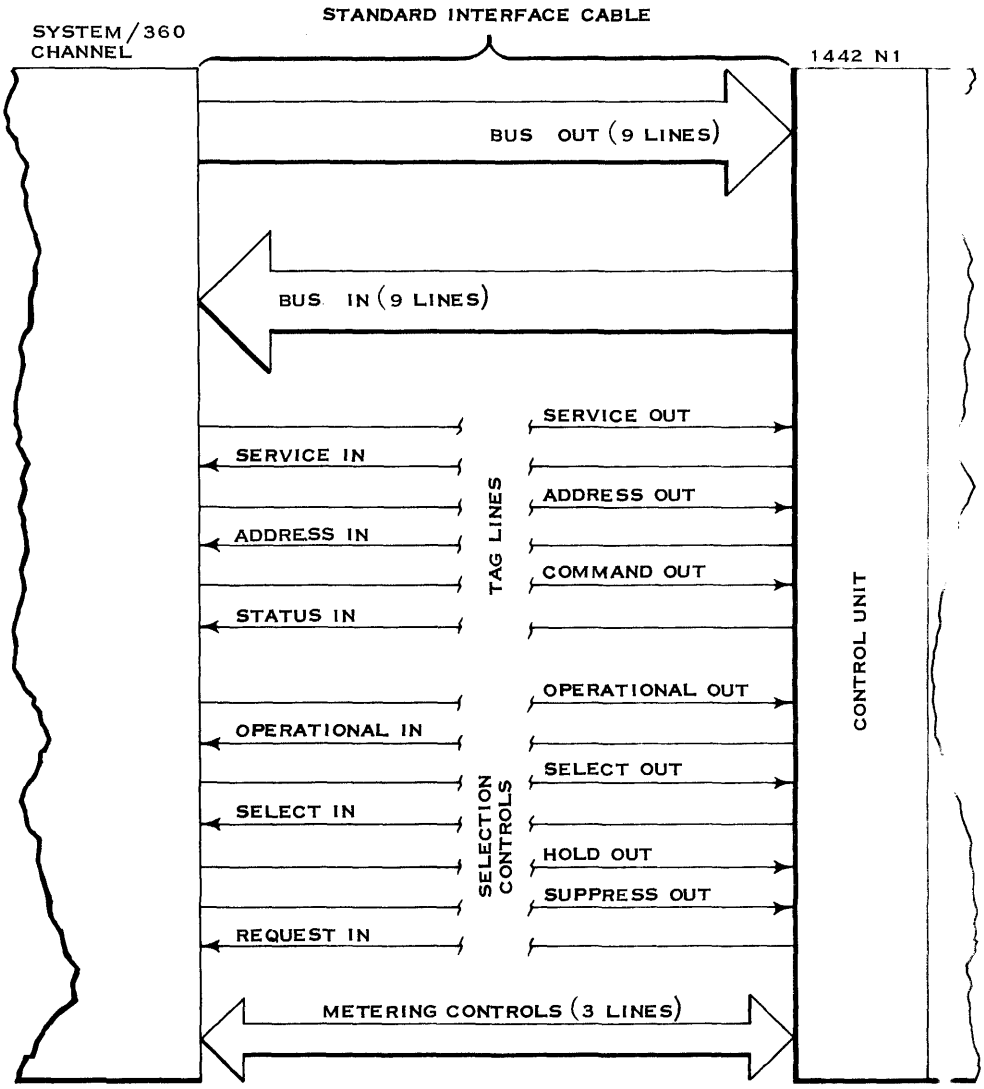
THE MAKE-UP OF THIS WORD VARIES WITH THE DIFFERENT MODELS OF THE SYSTEM/360

CSW (CHANNEL STATUS WORD)

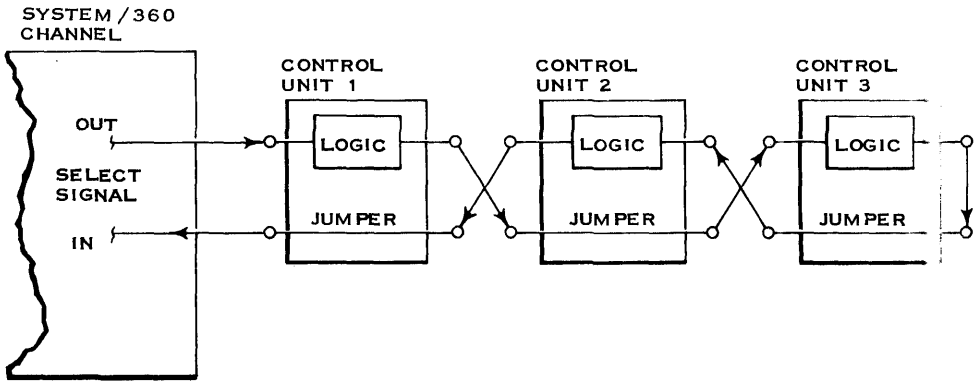


BIT	DESIGNATION	BIT	DESIGNATION
32	ATTENTION	40	PROGRAM-CONTROLLED INTERRUPTION
33	STATUS MODIFIER	41	INCORRECT LENGTH
34	CONTROL UNIT END	42	PROGRAM CHECK
35	BUSY	43	PROTECTION CHECK
36	CHANNEL END	44	CHANNEL DATA CHECK
37	DEVICE END	45	CHANNEL CONTROL CHECK
38	UNIT CHECK	46	INTERFACE CONTROL CHECK
39	UNIT EXCEPTION	47	CHAINING CHECK

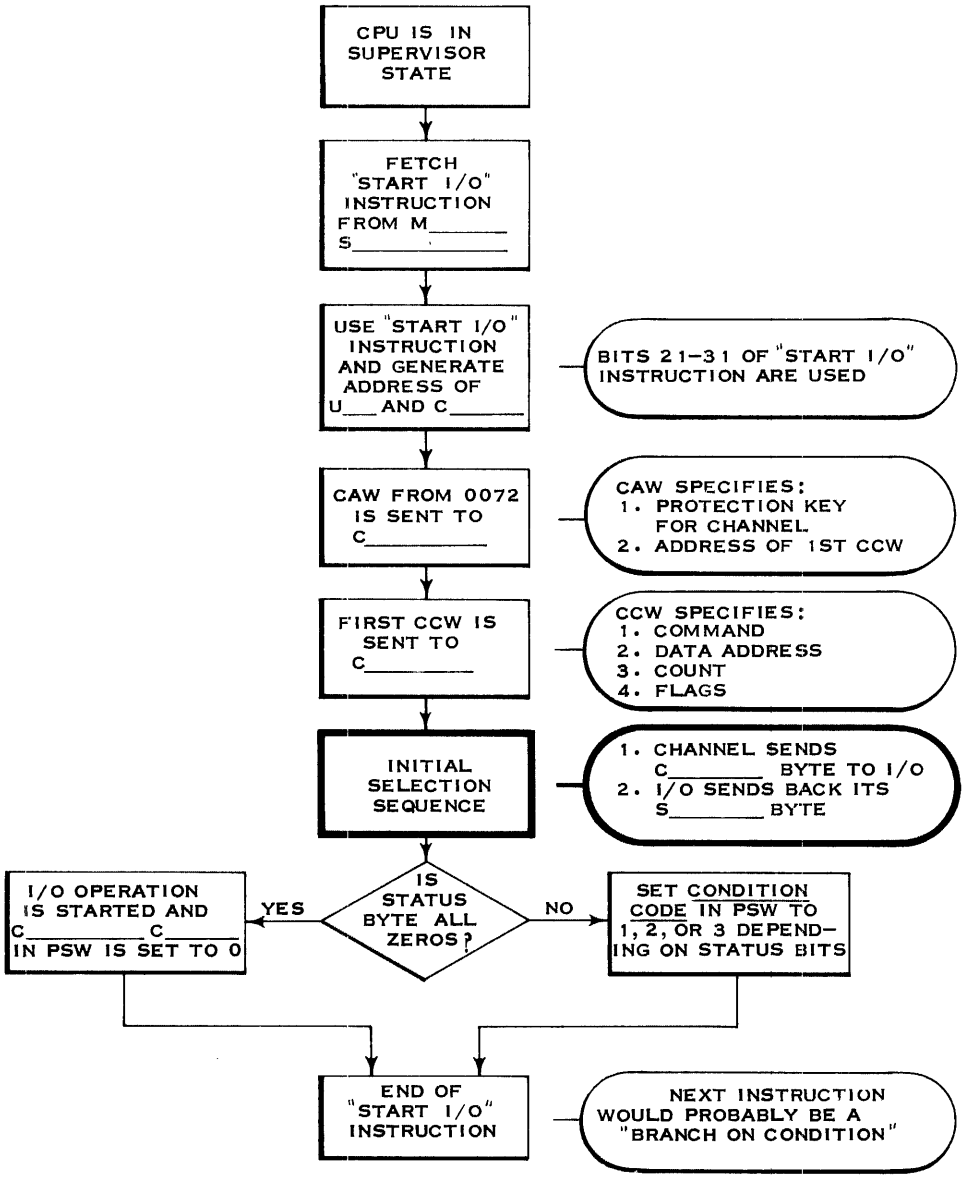
FORMATS OF I/O CONTROL WORDS



STANDARD INTERFACE LINES



CONTROL UNIT PRIORITY



INITIAL SELECTION

PROGRAM #1

Initial PSW		0000000000000800	
Location 2048	BALR	1,0	Load base address into Reg 1
	LA	0,3840(0,0)	
	ST	0,0072(0.0)	Load CAW
Input	SIO	128(0),0	Start Input Operation
Routine	BC	7,50(0,1)	Branch to Wait State
	TIO	128(0),0	Wait Loop Until End Of I/O Operation
	BC	2,16(0,1)	
	LA	0,3848(0,0)	
Output	ST	0,0072(0,0)	
Routine	SIO	519(0),0	
	BC	7,50(0,1)	
	TIO	519(0),0	
	BC	2,40(0,1)	
	BCR	15,1	Unconditional Branch to input routine
Wait State	MVI	1(0), 2	Turn to Wait State bit
Routine	LPSW	0,0	Put system in Wait State
Location 3840		02000F1000000050	Input CCW
		01000F1000000050	Output CCW

PROGRAM #2

Initial PSW	FF0400000F000800
0000-0007	FF0400000F000800
3840-3847	02000F0800000050
3848-3927	Input Area
4096-4103	0100101840000008
4104-4111	1300000040000001
4112-4119	0100101800000008
4120-4127	Output Area (8 bytes of EBCDIC)

```
2048    BALR    1,0                     Load Base Register
        LA      0,3840 (0, 0)           Set up Input CAW
        ST      0,0072 (0,0)
        SIO     8,0                     Unit #8 on Multiplexor
        MVC     0120(8), 0000 (0)
        LA      0,0034(1)
        ST      0,0124 (0, 0)           Set up I/O New PSW
        OI      0001,2                  Put System in Wait State
        LPSW    0000
        TM      0069,255                Check channel status byte
        BC      7,0050(1)               Not Zero?
        TM      0068,3                  Unit Exception or Check
        BC      8,0058(1)               No?
        NI      0000,0                  Mask I/O interrupts
        LPSW    0000                    And put system in Wait
                                          State
        L       2,1798(1)               Load Field A
        A       2,1808(1)               Add A + B
        CVD     2,2070(1)               Store and Convert re-
                                          sult to Packed Decimal
        UNPK    2070(8,1),2070(8,1)
        LA      0,2046(1)               Set up Output CAW
        ST      0,0072 (0, 0)
        SIO     266,0                   Unit #10 on Selector
                                          Channel 1
        NI      0120,0                  Set up I/O New PSW
                                          for Mask and Wait State
        OI      0121,2
        LPSW    0000                    Put System in Wait
                                          State
```

Book 5 System/360 Input/Output Operations Student Course Evaluation

You can make this course and all future courses more useful by answering the questions on both sides of this sheet and giving us your comments.

Do you feel that you have an adequate understanding of the learning objectives that are listed at the beginning of the following sections?

Section I:	Introduction to I/O Operation	Yes ☐ No ☐
Section II:	I/O Devices	Yes ☐ No ☐
Section III:	Standard Interface	Yes ☐ No ☐
Section IV:	I/O Instructions	Yes ☐ No ☐
Section V:	Channel Error Conditions	Yes ☐ No ☐
Section VI:	Initial Program Load Procedure	Yes ☐ No ☐
Section VII:	Analyzing I/O Programs	Yes ☐ No ☐

List any technical errors you found in this book.

Comments

Please complete the information block on the opposite side. Thank you for your cooperation.
For form R23-2959-1

Field Engineering Education - Student Course Evaluation

IBM

Student Name	Man Number	B/O Number	Area Number

Student: Please review this evaluation with the person administering the course; then remove it from the book and send to the FE Education Center via IBM mail.

- Were you given a copy of this text to write in and keep? . . . . . Yes ☐ No ☐
- How many hours per day were scheduled for this course? _____
- Were you interrupted during this time? . . . . . Yes ☐ No ☐
- How many hours were needed to complete this course? _____
- Did you require assistance during this course? . . . . . Yes ☐ No ☐
  (If your answer is yes, explain in the comments section)
- Indicate your understanding of the total course. Excellent ☐ Good ☐ Fair ☐ Poor ☐

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Reviewed by:	

To be completed by FE Education Planning	Date
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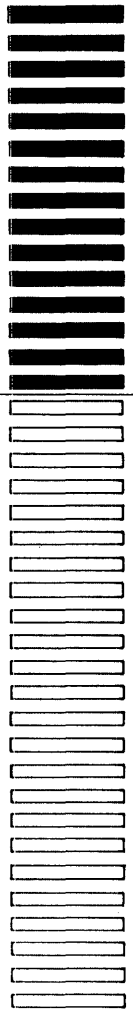
South Road
Poughkeepsie, N. Y. 12602



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International Business Machines Corporation
Field Engineering Division
112 East Post Road, White Plains, N.Y. 10601