IBM Field Engineering

Theory of Operation

(Manual of Instruction)

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System/360 Model 44

Single Disk Storage Drive

IBM®

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System/360 Model 44

Single Disk Storage Drive

PREFACE

This volume describes the Single Disk Storage Drive Control Unit of the IBM 2044 Processing Unit, the processor for the IBM System/360 Model 44. Chapter 1 provides an introduction to the unit, its connection to the processor, the disk format and the data flow. Chapter 2 describes the functional parts of the unit. Chapter 3 describes in detail the valid commands and their execution.

The manual assumes knowledge of the System/360 as described in IBM System/360 Principles of Operation, Form A22-6821.

The volumes that constitute the IBM Field Engineering Theory of Operation manual for the IBM System/360 Model 44, and their form numbers, are:

System/360 Model 44, Introduction and Functional Units, Form Y33-0001: Gives a general introduction to digital computers and computing techniques, defines the relationship of the IBM 2044 to the System/360 and describes the various parts which form the processing unit.

System/360 Model 44, Principles of Operation - Processing Unit, Form Y33-0002: Describes the operation of the instructions for the accelerator and basic machine (other than floating-point instructions), and program and machine interrupts.

System/360 Model 44, Principles of Operation - Channels, Form Y33-0003: Describes the Common Channel area, the Multiplexor Channel 0 and the High Speed Multiplexor Channel.

These volumes are referenced in other volumes by the main element of their titles.

Reference is also made in these volumes to the following associated manuals:

Field Engineering Theory of Operation (FETO) IBM System/360 Model 44, Floating Point Feature, Form Y33-0005: Gives an introduction to floating-point arithmetic, describes the functional implementation of floating-point arithmetic in the 2044 and details the operation of floating-point instructions.

Field Engineering Maintenance Manual (FEMM), IBM System/360 Model 44, Form Y33-0007: Contains information for servicing the 2044 Processing Unit.

Field Engineering Maintenance Diagrams (FEMD), IBM System/360 Model 44, Forms Y33-0008 and Y33-0009: Contain maintenance information in the following categories: Data Flow Charts, Flow Charts, Timing Charts, MAP's.

Other related manuals that describe units used in the System/360 Model 44 are:

Field Engineering Manual of Instruction (FEMI), 1052 Adapter, Form 223-2808.

Field Engineering Maintenance Manual (FEMM) Single Disk Storage/Direct Access, Form Y26-3663.

First Edition

This manual makes obsolete Field Engineering Theory of Operation, System/360 Model 44, Form Z33-0007-0.

This manual is written basically to Engineering Change Level 390049 and is some cases anticipates Engineering Change Level 390063. Significant changes or additions to the information in the manual will be covered in subsequent revisions or FE supplements.

This publication was prepared by IBM European Laboratories, Product Publications. A form is provided at the back of this manual for reader's comments. If the form has been removed, comments may be addressed to: IBM Corporation, FE Manuals, Dept. B96, BO Box 390, Poughkeepsie, N. Y. 12602

CONTENTS

ILLUSTRATIONS

ABBREVIATIONS

The following abbreviations are used in this manual.

BC Register	Burst Check Register
CCW	Channel Command Word
CLT	Circuit Level Test
CPU	Central Processing Unit
EXOR	Exclusive OR
I/O	Input/Output
SDSD	Single Disk Storage Drive

- The SDSD control unit ensures that the signals and information received from the channel over the standard interface (and vice versa) are presented to the SDSD in a recognizable and usable form.
- The control unit converts parallel data from the standard interface into serial bits of data to be written onto the disk.
- Serial data read from the disk is assembled by the control unit into parallel bytes of data for presentation to the standard interface.
- The control unit has two interfaces: the standard interface and the SDSD interface.
- A disk surface contains a maximum of 203 tracks where data can be recorded.
- Each track is subdivided into eight sectors (0 to 7)
- A sector has a capacity of 366 bytes of data.
- When recording, a fixed track format is used in each sector.
- The SDSD used the double frequency recording method.
- Valid commands to the SDSD are: seek, write, read, test I/O and sense.

One Single Disk Storage Drive (SDSD) is standard on the IBM System/360 Model 44. A second SDSD is an optional feature. The SDSD is a storage component sub-assembly that is designed to be housed within the covers of a host system. It can store approximately 600,000 bytes of data on each surface of a single magnetic-coated disk which is permanently enclosed in a removable cartridge. All communication between the Central Processing Unit (CPU) and the SDSD is made via the channel, the standard interface, the SDSD control unit and the SDSD interface (Figure 1-1).

The control unit ensures that the signals and information received over the standard interface are presented to the SDSD (and vice versa) in a recognizable and usable form. When writing onto disk, the main function is to convert the parallel data bits from the standard interface to serial data bits. Similarly, when reading from disk, the main function is to convert serial data bits from the SDSD to parallel data bits, for presentation to the standard interface.

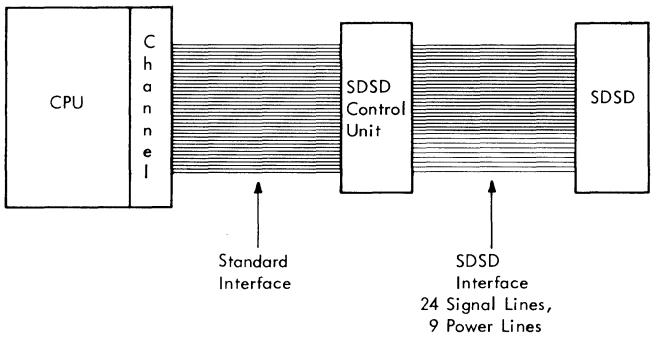


Figure 1-1. CPU to SDSD Connection

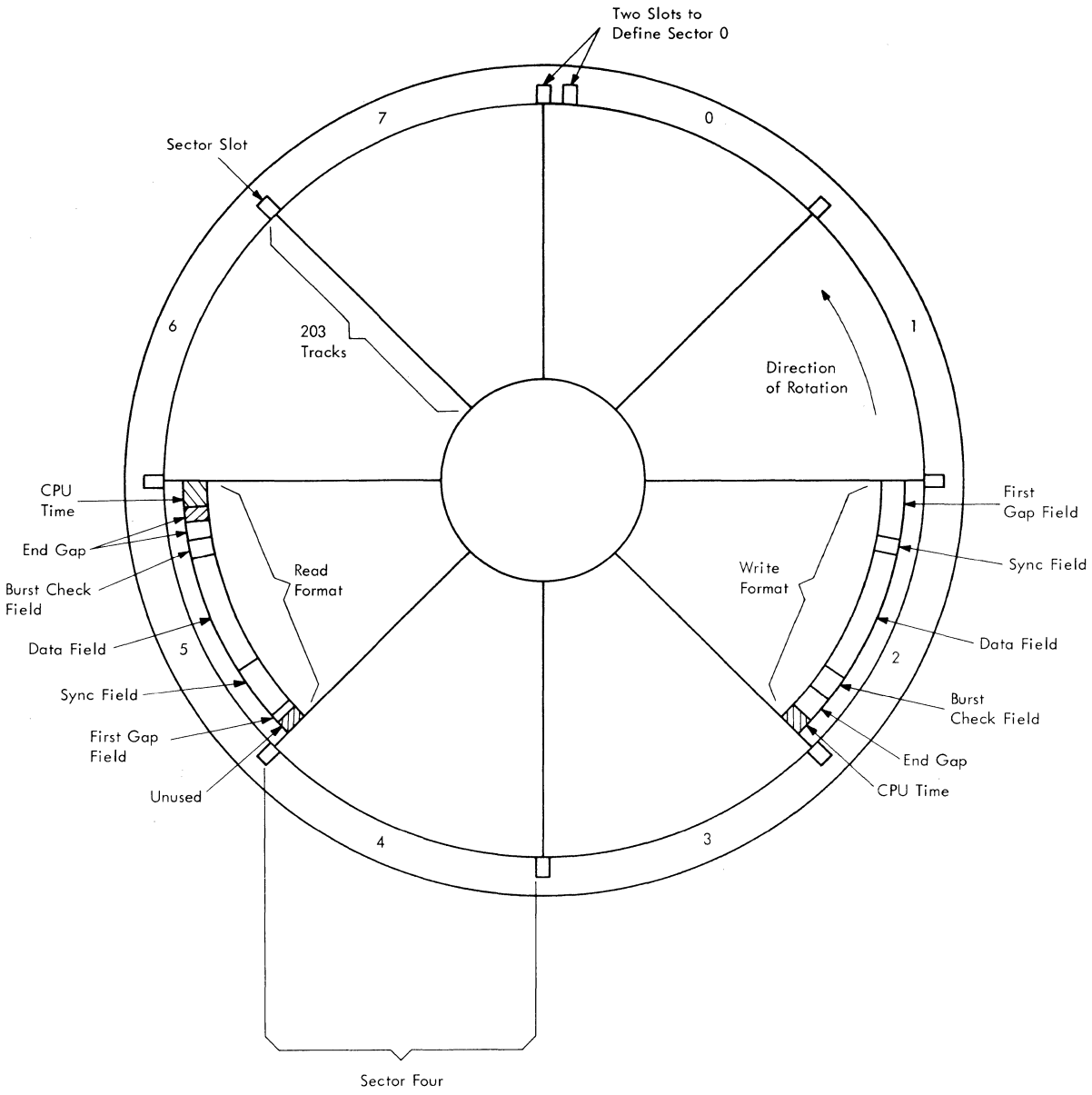


Figure 1-2. Disk Format

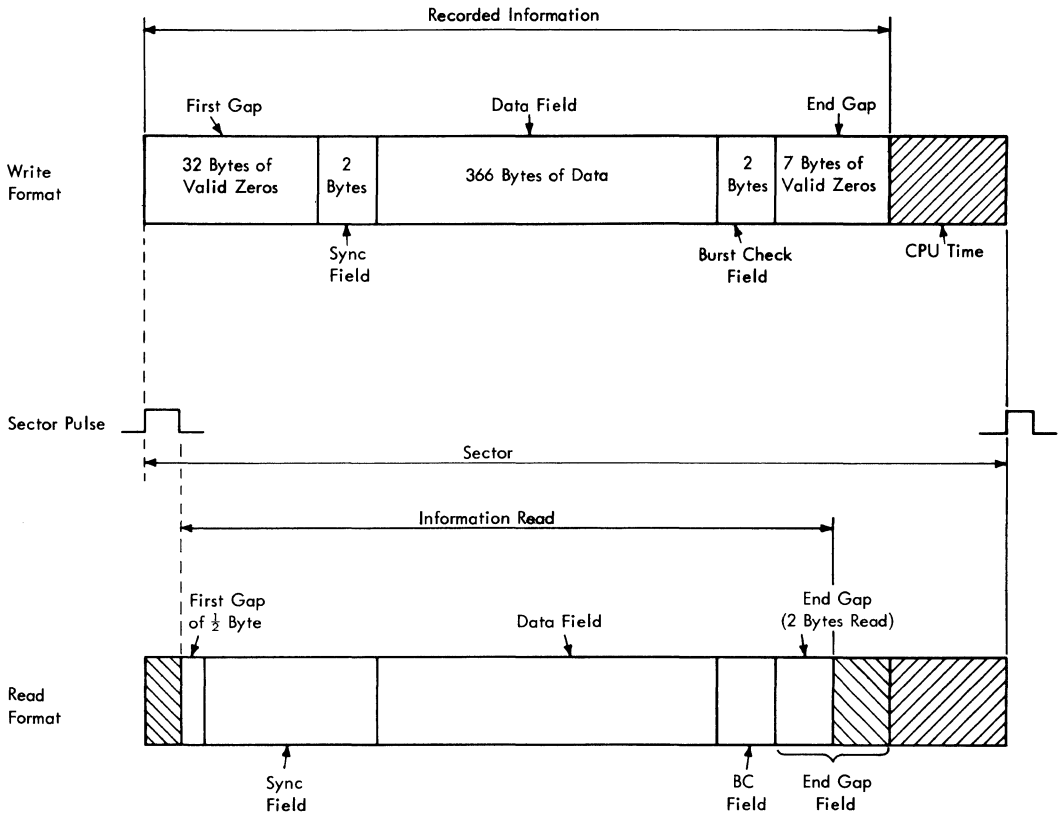


Figure 1-3. Write and Read Track Formats

FORMAT

Data is recorded on the disk according to a fixed track format (Figure 1-2). Each surface of the disk is divided into 203 tracks, each track into eight sectors (0 to 7) and each sector has a capacity of 366 bytes of data.

To define the position of the eight sectors, nine slots are cut into a sector ring mounted on the disk; two slots, close to one another, define sector 0.

Each sector is divided into fields, the function and duration of which differs for write and read operations. The write and read track formats (Figure 1-3) are controlled by the format control ring.

Data is recorded using the double frequency recording method, whereby data pulses are interleaved with clock pulses.

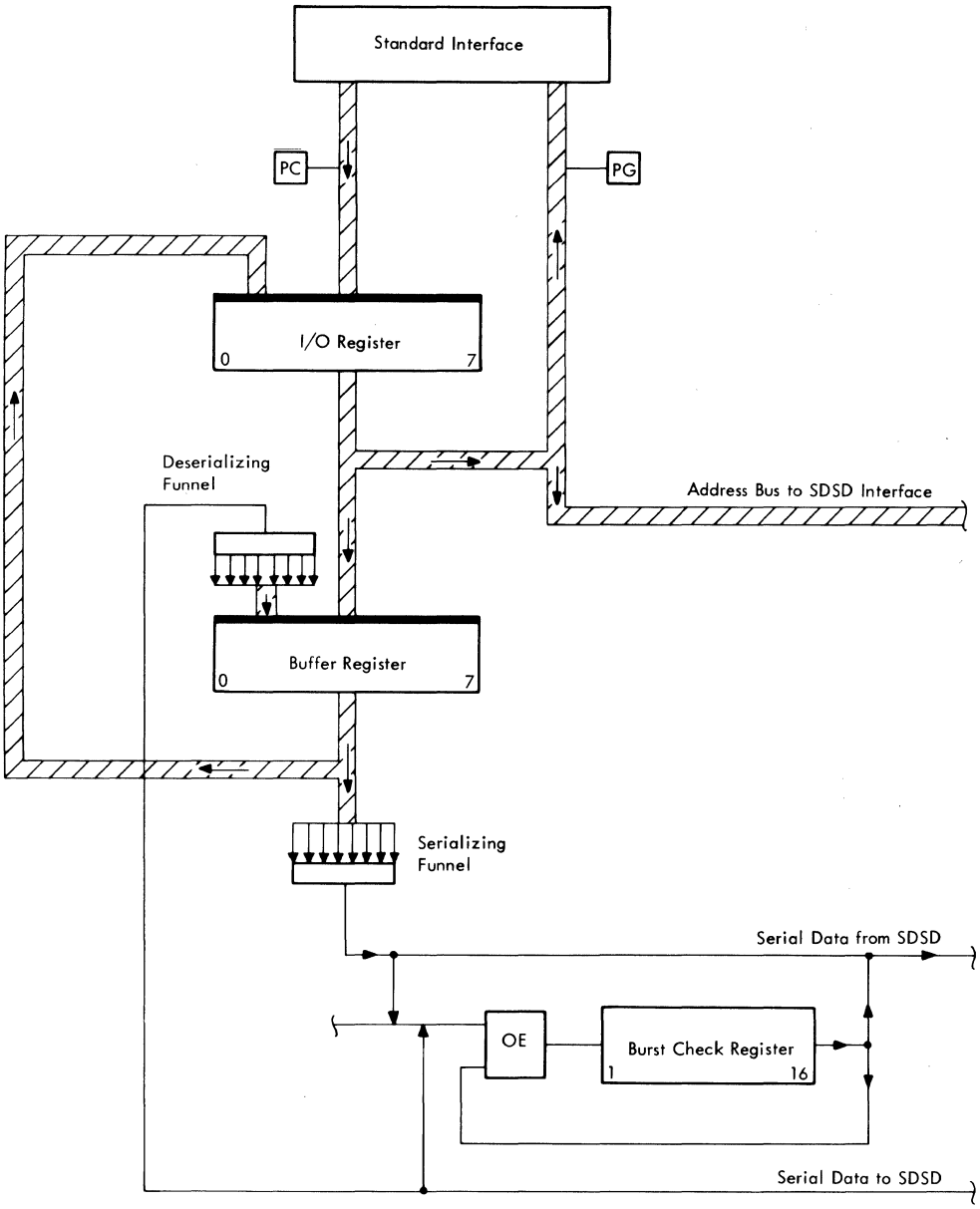


Figure 1-4. SDSD Control Unit Data Flow

SERIALIZING -- DESERIALIZING

- Data to disk from buffer register is serialized.
- Data from disk to buffer register is deserialized.
- Both serializing and deserializing are accomplished by the bit ring which runs in synchronism with the disk.

When writing, the bit ring works in conjunction with the serializing funnel. When reading, the bit ring gates successive bits of serial data to appropriate buffer register positions, via the deserializing funnel. The locations of these funnels and the buffer register, within the data flow of the control unit, are shown in Figure 1-4.

PARITY

- Data from the standard interface has parity checked then dropped.
- Data to the standard interface has parity generated.

Parity is not carried by the SDSD or the control unit, but data is checked by the burst check operation. When writing, a bit count is made in a 16-position, binary-coupled register. After all serial data has been written, the contents of the burst check register are written onto the disk. When reading, the data bits are counted once more and, if no error has occurred, this count must agree with the burst check field that was originally written onto the disk.

REGISTERS

As shown in Figure 1-4, the control unit uses two eight-bit registers in the main data flow path.

The I/O register input is from bus out during write operations and from the buffer register during read operations. Its output is to bus in during read operations, to the buffer register during write operations and to the address bus of the SDSD interface during seek operations.

The buffer register is a temporary storage device for data, prior to moving the data to the channel or to the disk.

SDSD CLOCKS

- Write clock is generated from a 1.44 megacycle oscillator which triggers a flip-flop.
- Read clock is generated from the clock pulses read from the disk.

To safeguard against synchronism problems, caused by disk speed variation, the read clock is generated from the clock pulses read from the disk.

COMMANDS AND ADDRESSING

- For the SDSD there are five valid commands.
- Each SDSD may be connected, via the standard interface, to multiplexor channel 0 or to either of the high-speed multiplexor channels.

The five valid commands for the SDSD are: control, read, write, test I/O and sense.

The control command has two different formats:

Control seek	0000	1011
Control no-op	0000	0011

The read command also has two formats:

Read data	HSSS	1010
Read IPL	0000	0010

The write, test I/O and sense commands each have one format:

Write data	HSSS	1001
Test I/O	0000	0000
Sense	0000	0100

A description of the operation of each command is given under "Principles of Operation."

Each SDSD is programmed as a control unit attached to any one channel. The addresses of the SDSD's are in the form:

Subchannel	Device
AAA	0000 Standard drive (file 0)
AAA	0001 Optional drive (file 1)

CHANNEL WRAP CIRCUITS

Channel wrap is a diagnostic aid for use on channel and interface maintenance. The uses of the wrap facility with special channel Circuit Level Tests (CTL's) or diagnostic programs are described further in Section 1.9 of the FEMM, IBM System/360 Model 44, Form Y33-0007.

SDSD INTERFACE

The SDSD interface is formed by 24 signal lines (Figure 2-1) that connect the control unit and logic elements with the SDSD.

Address Lines

The binary values of each position on the eight address lines are 1, 2, 4, 8, 16, 32, 64 and 128 and they represent the absolute address. An up level represents a selection for that line. The address must be time-coincident with the access-drive pulse.

Access Drive

The access-drive line supplies a positive pulse which has a minimum duration of 0.8 microseconds and a maximum duration of 100 microseconds. This pulse gates in the new address and initiates the access cycle.

Access Ready

The access-ready line is a logic level transmitted from the SDSD to the control unit upon completion of the access motion, including detenting and head settling time. The access-ready line drops from +3 volts to ground within 0.75 microseconds of the leading edge of the access-drive pulse. This interval constitutes the reset time for the address register. The down level represents the not ready state. The line rises to the ready state (+3 volts level) approximately 26 milliseconds after the arrival signal. The access-ready signal signifies to the control unit that the SDSD is ready for data processing.

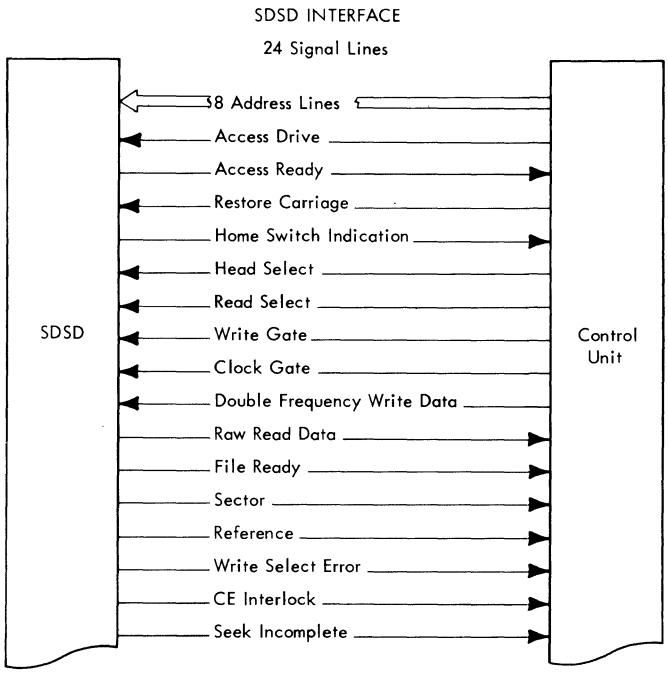


Figure 2-1. SDSD Interface

Restore Carriage

The restore carriage line, when activated, gives a negative pulse (dropping from +3 volts to ground) of any duration from 1 microsecond to 1 millisecond. It sets a restore-carriage latch which supplies a small dc voltage directly to the servo-summing amplifier, bypassing the addressing and position-error producing electronics. This permits the file to retract the carriage to track 000, independent of the address electronics. The restore-carriage latch is reset by the microswitch which is engaged when the carriage detents at track 000.

In a restore-carriage operation, the access-ready line will be in a not ready state until 26 milliseconds after the arrival state is reached.

Home Switch Indication

A switch is actuated whenever the carriage is in the home or track 000 position. The home switch indication line is at +3 volts when the carriage is detented in any of the track positions 001 to 203, and is grounded when the carriage is detented in the home position. This line provides a reference point to locate the carriage, and the line is formed directly from the output of a microswitch.

Head Select

The head select line state indicates which head is selected. When the level is +3 volts, head zero is selected and when the line is at ground level (activated), head one is selected.

Read Select

The read select line enables or disables the read amplifier output. Whenever this line is down (active) and the write gate is up (inactive), raw read data is available to the control unit.

When the read select line is up (inactive) there will be no output in the raw read data line. A minimum delay of 60 microseconds must be allowed before selecting a read operation after the machine has been in a write operation.

Write Gate

The write gate line controls the flow of write current to the recording heads. For proper file operation, this line must be operated in close co-ordination with the clock gate line. When the write gate line is up, the write and erase circuits are completely disabled, and the machine will not accept information on the 'double frequency write data' line. When the write gate line is down (active) and no write select error condition exists, the write and erase circuits are turned on.

Clock Gate

The clock gate line works in conjunction with the write gate to ensure proper write circuit operation. This line must be held at ground (active level) whenever the write gate is on.

Double Frequency Write Data

The write-data line drives the write trigger in the SDSD write circuits. Each negative going transition of the write-data line causes a magnetic flux reversal to be recorded on the disk surface.

Raw Read Data

The raw read data line contains both data and clock information interleaved in time. Each positive going pulse, of 200 nanoseconds nominal duration, corresponds to a detected magnetic flux reversal on the disk.

File Ready

The file ready line is at ground level when the file is in a ready state. The conditions required to achieve this state are:

Disk is at full rotational speed.
Heads are loaded against the disk.
No write-select error condition exists.
The 1.5 minute delay has elapsed after turning on the drive motor.

If these four conditions are not satisfied, the ready line has a +3 volt level (inactive).

Sector

The sector pulses assist in formatting data on the disk. There are eight negative going sector pulses, equally spaced 5 milliseconds apart, of 160 microseconds duration.

Reference

One reference pulse of 160 microseconds duration is generated for each revolution of the disk. This pulse follows one of the sector pulses (sector 0) by approximately 600 microseconds.

Write-Select Error

This line is available to the control unit as an indication of a write circuit failure. Because it is a latched line, an error indication will persist if the failure is intermittent. The write-select error line is set and latched to ground level when either the write gate is at ground (active) and the clock gate is at +3 volts (inactive), or when both heads are selected for writing simultaneously.

CE Interlock

This line supplies +3 volts from the control unit to the machine so that a read only mode is selected when the read/write CPU signal cable is disconnected from the electronic gate. At the same time, the write-gate signal is opened, inhibiting the write function.

Seek Incomplete

This line indicates an access malfunction to the control unit. The seek-incomplete line is set, and latched to ground, if the access mechanism has not come to a stop within 200 milliseconds from the time an access-drive pulse is received by the file. The seek-incomplete line must be unlatched by another access-drive pulse from the control unit. When the access mechanism functions normally, the seek-incomplete line is at +3 volts (inactive).

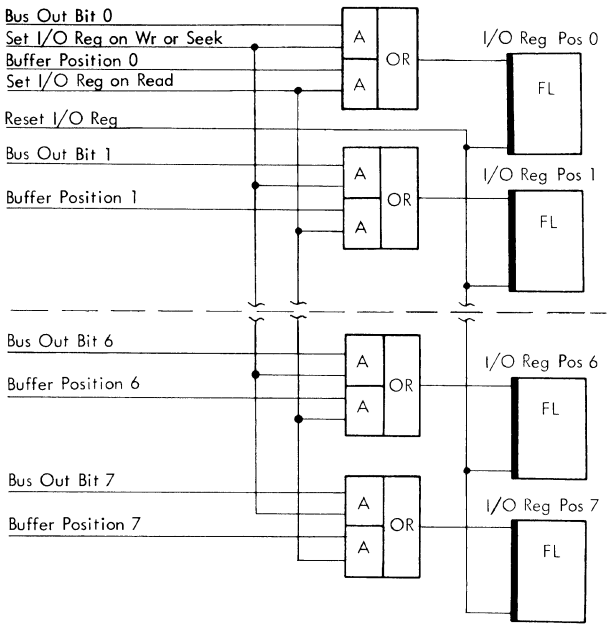
REGISTERS

I/O Register

- An eight-position register used in both write and read data paths.
- Input and output of I/O register is always serial by byte, parallel by bit.
- Input from standard interface bus out (write) or the buffer register (read).
- Output to either buffer register (write), or bus in (read), or address bus of SDSD interface (seek).
- Does not carry parity.

The input to the eight-position I/O register (Figure 2-2) comes either from the standard interface when writing, or from the buffer register when reading. (See Figure 1-4). The destination of the I/O register output is controlled by the type of command being executed. A valid seek command and address, causes the I/O register output to appear on the address bus lines of the SDSD interface. This is then the track address of the seek command. When writing, the I/O register output is transferred to the buffer register prior to serialization.

During read operations, the I/O register output is gated to the standard interface, good parity being generated before each byte is presented to the standard interface.



NOTE: Positions 2-5 of the I/O Register are similar to the positions shown.

Figure 2-2. I/O Register

Buffer Register and Serializing Funnel

- Buffer register is an eight-position register used in both write and read data paths.
- Buffer register input is from disk (read) or I/O register (write).
- Output of buffer register feeds serializing funnel (write and read) and I/O register (read).
- Serializing funnel provides single data bits from the data byte in the buffer register.
- Serial data bits read from the disk are assembled, in the buffer register, into complete bytes of data.
- Does not carry parity.

The eight-position buffer register is used as temporary storage for data, prior to moving the data on to the disk (write) or the channel (read). Figure 2-3 shows two positions of the buffer register, positions 4 through 7 being similar to position 0, and positions 2 and 3 being similar to position 1. This figure also shows the serializing funnel on the output of the buffer register. The serializing funnel, driven by the bit ring, gates successive positions of the buffer register to the file (during write operations) and to the Burst Check (BC) register (during read and write operations).

The bit ring and the buffer register are used as a deserializing circuit during a read operation. The serial data to buffer line sets each buffer register position at the appropriate bit ring time. As the serial data is read off the disk, each bit is set into the correct buffer register position by the bit ring.

Positions 1, 2 and 3 of the buffer register can be set from bus out bits 1, 2 and 3 of the standard interface. This logic allows the sector address to enter the buffer register (by-passing the I/O register) during the command initiation.

Burst Check Register

- A 16-position binary coupled, shift right, register.
- Used for checking data validity in the control unit.
- Sole input is into position 1 from serial data to or from the disk.
- Output is from position 16 to the disk or from all positions to the check circuit.
- A burst check error can be detected only on a read operation.
- A burst check error can occur at the end of any sector being read.
- A burst check error is a non zero content of the BC register at end gap.

The SDSD and its control unit do not carry parity but data is validated by a burst check using the BC register.

The BC register is a 16-position, binary coupled, shift right, register, so that one advance pulse moves the whole register one position to the right. Figures 2-4 and 2-5 show the BC register and its controls.

At bit ring 6 of the sync field of a read or write operation, the BC register is reset to all ones. Serial data is then Exclusive ORed (EXORed) with BC register position 16 output to form the input to position 1. Successive clock pulses produce the

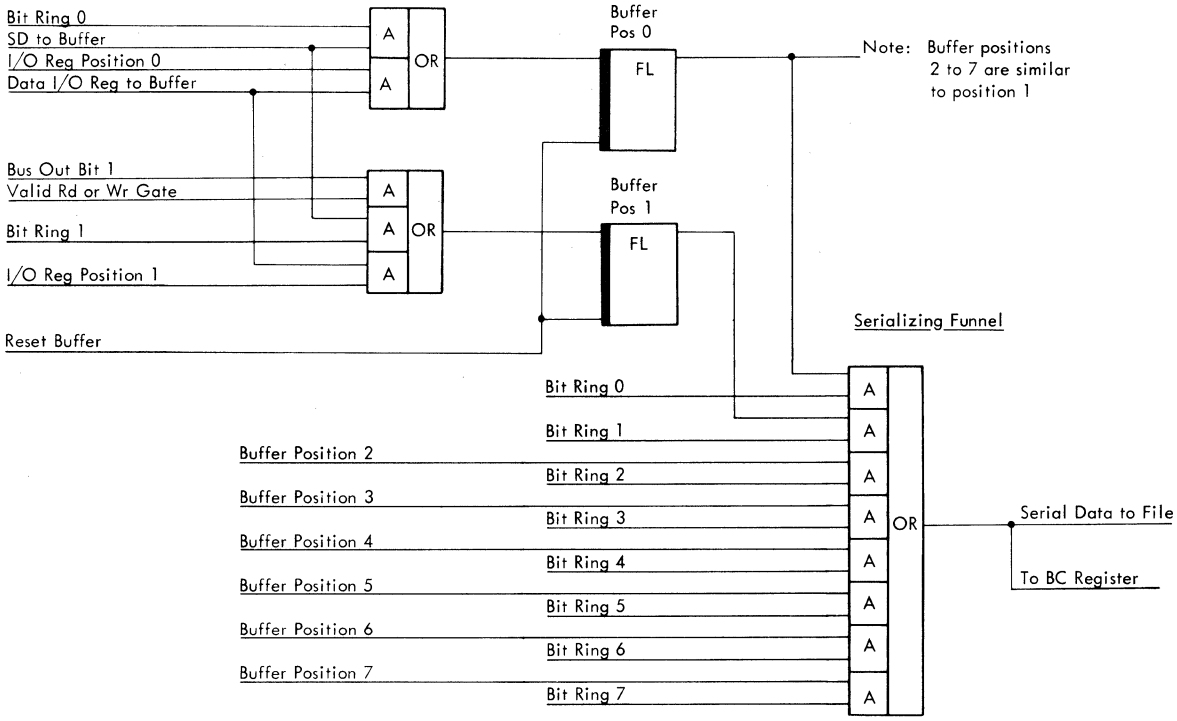


Figure 2-3. Buffer Register and Serializing Funnel

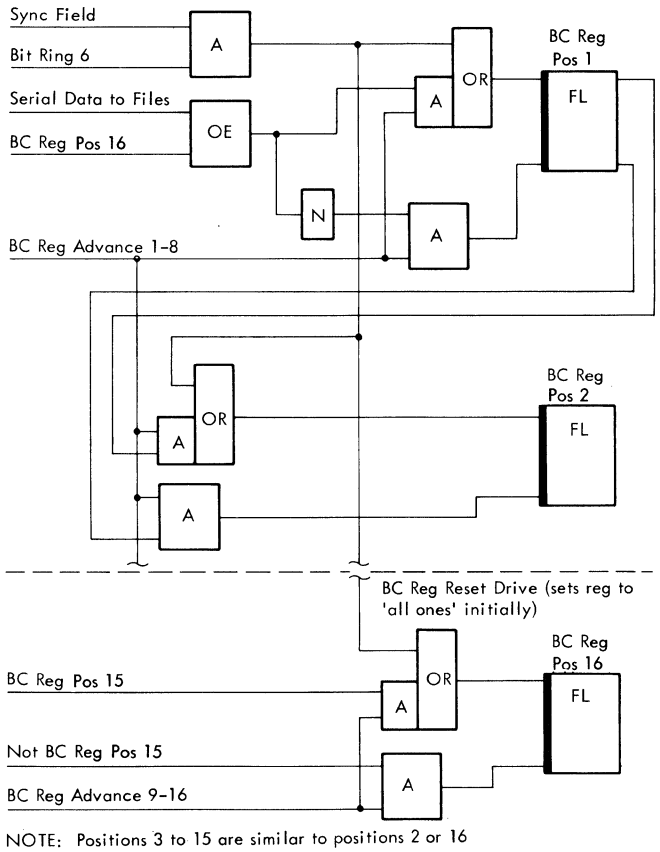


Figure 2-4. Burst Check Register

pulses BC register advance 1-8 and BC register advance 9-16, which shift right the register one position per pulse. This process continues until the end of the data field, developing a burst check pattern in the register.

During write operations, when the end of the data field is reached, the shift right process continues and the output of position 16 is sent as serial data to the disk to be recorded, as a two-byte burst check field.

During read operations, when the end of the data field is reached, the burst check field from the disk is read into the register in the same manner as the data field. Therefore, at the end of the burst check field, the BC register should be all zeros. Any position (or positions) remaining on causes a data check.

NOTE: If, during a write operation, the byte count is less than 366, the data field is zero filled and the burst check pattern continues to be developed until the end of the data field.

An example of the burst check operation is shown in Figure 2-6. This example uses an eight-bit data field and a five-position burst check register.

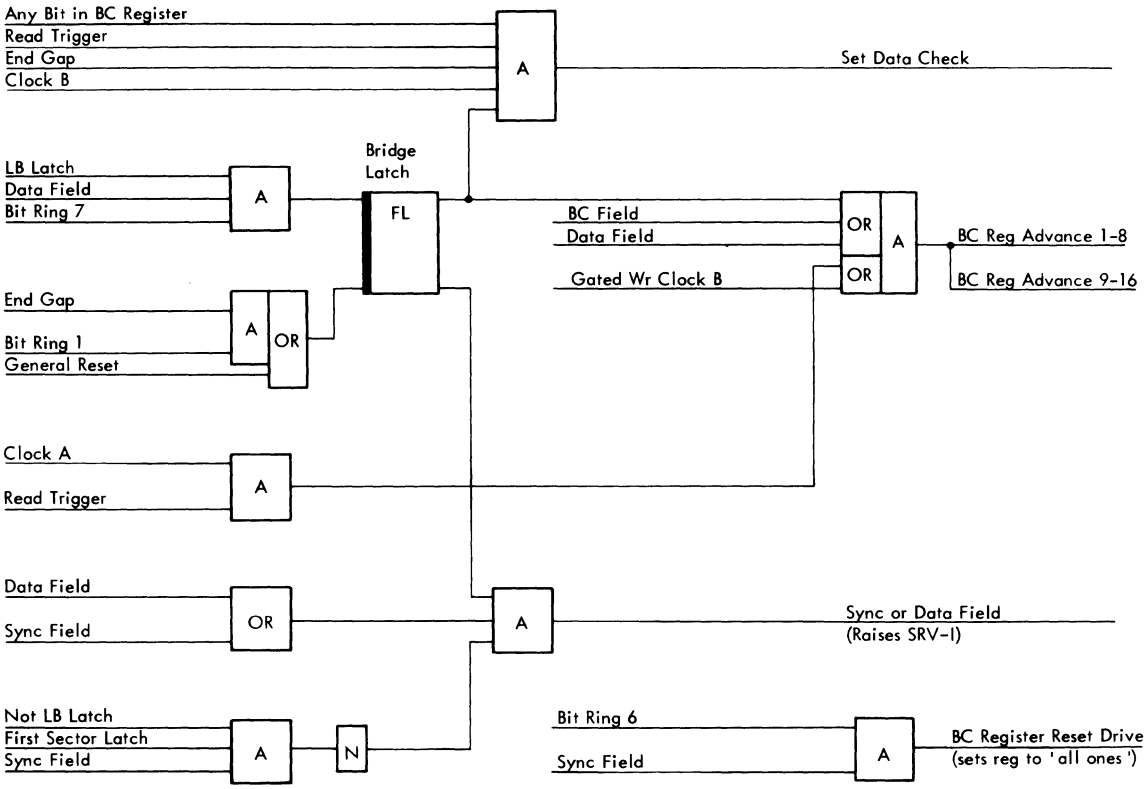


Figure 2-5. Burst Check Register Controls

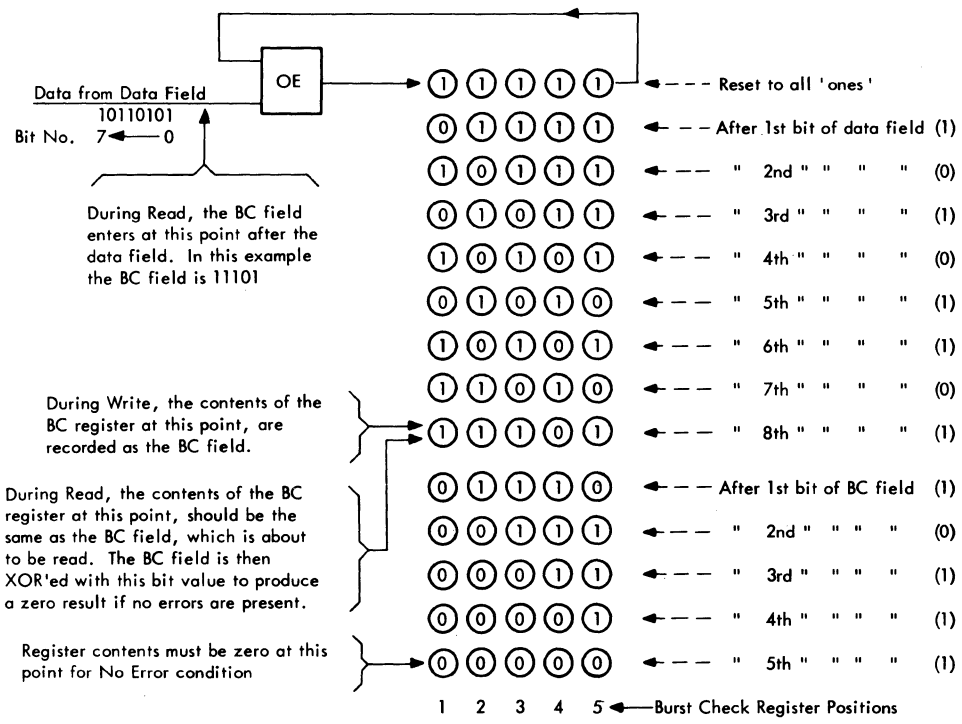


Figure 2-6. Burst Check Operation

SDSD CLOCKS

Oscillator and Write Clock

- Oscillator of 1.44 megacycles used only when writing.
- Oscillator output triggers a flip-flop to produce the basic timing pulses.
- The basic timing pulses have a cycle time of approximately 1.4 microseconds and are in antiphase.
- Six other clock pulses are produced from the basic timing pulses.
- Clock C and clock D pulses are used only on write.

A 1.44 megacycle oscillator, which is allowed to function only when the write trigger in the control unit is on, is used to switch a flip-flop. Thus, the flip-flop output is at half the frequency of the oscillator, giving a 1.4 microsecond cycle. These outputs, called clock phase A and clock phase B (the antiphase), form the basic timing pulses on write operations. Figure 2-7 shows the write clock circuit and the associated timing chart.

Further clock pulses are produced: clocks A and C are of 125 nanosecond duration, clock B is 225 nanoseconds, and the basic clock pulses (A and B) are delayed by 125 and 350 nanoseconds respectively. Clock pulses C and D are used only when writing and have no equivalent in the read clock circuit. However, the majority of the logic elements used in the write clock are the same as those used in the read clock.

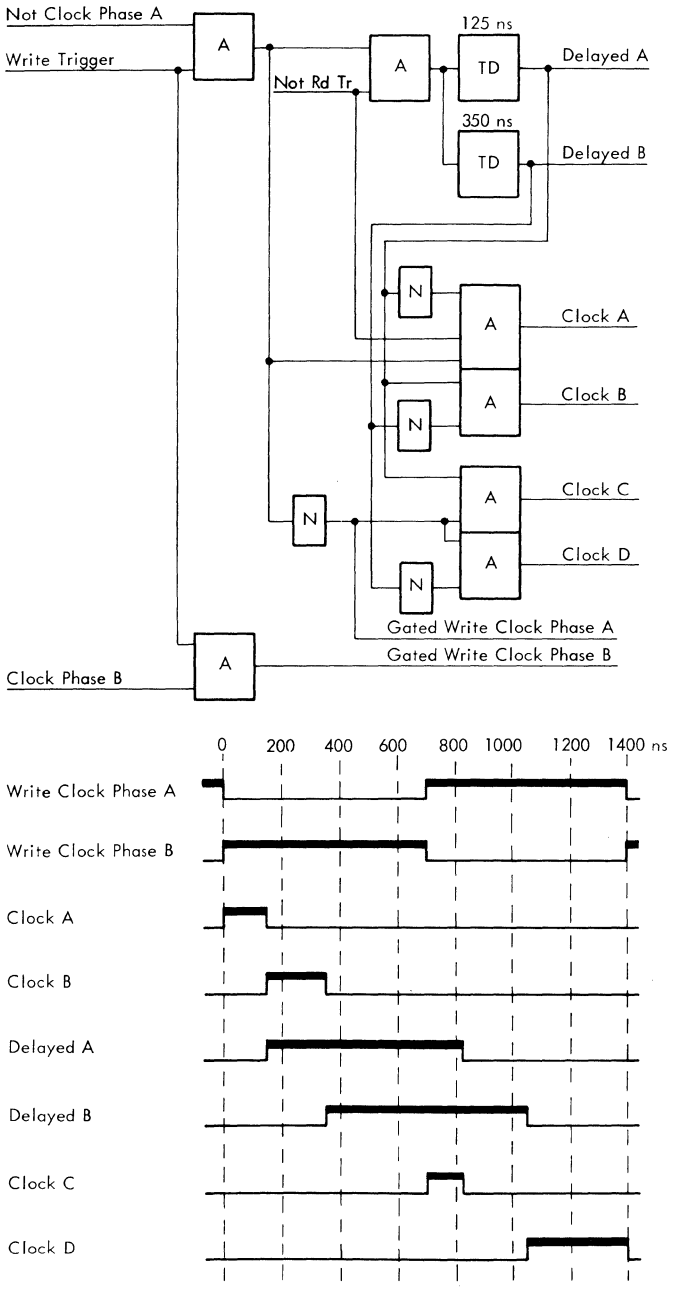


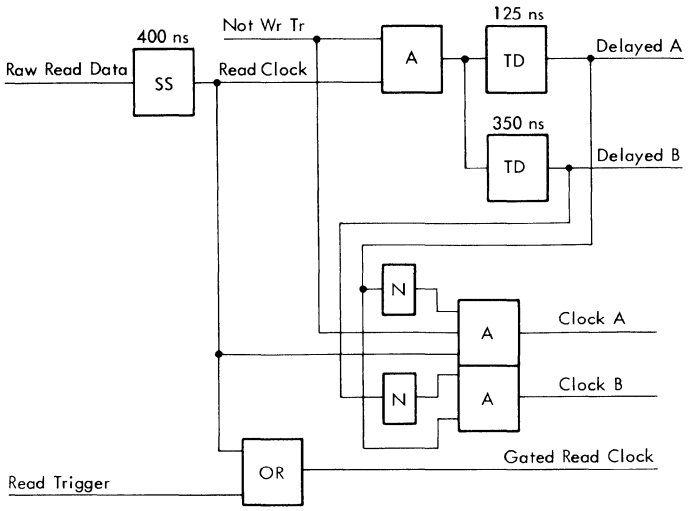
Figure 2-7. Write Clock

Read Clock

- Clock pulses recorded on the disk produce the basic timing pulse (read clock).
- The read clock is a 400 nanosecond pulse occurring every 1.4 microseconds.
- The read clock produces four other timing pulses using the same logic elements as in the write clock circuits.

The read clock is the output of a 400 nanosecond singleshot which is triggered from the recorded clock pulses read off the disk. An oscillator is not used in the read clock circuit because of the difficulty in synchronization with pulses read from the disk which are subject to variations. Thus, the read clock relies on the clock pulses recorded on the disk during a write operation. For this reason it is essential that the first gap, when recorded, consists of valid zeros (clock pulses only) to enable the read clock to be triggered by a clock pulse and not by a data pulse.

The 400 nanosecond read clock pulse, occurring every 1.4 microseconds, is used to produce four other timing pulses (Figure 2-8). They are: clock A, clock B, delayed A and delayed B. Clock A is 125 nanoseconds in duration, clock B is 225 nanoseconds, and delayed A and B are 400 nanoseconds in duration.



NOTE: Both TD blocks are the same delays as used in the Write Clock.

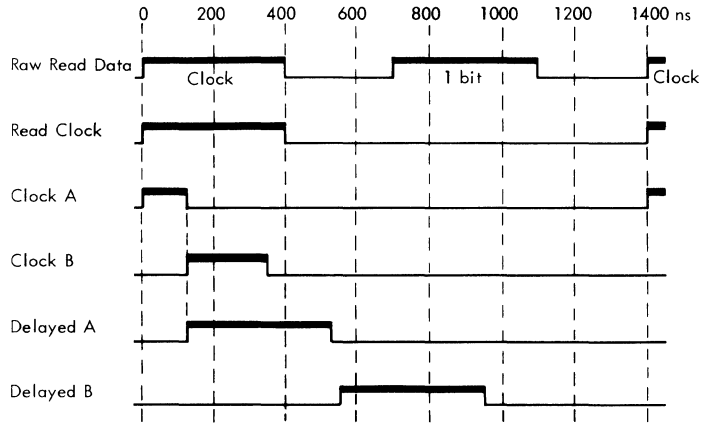


Figure 2-8. Read Clock

FORMAT CONTROL RING

- The track format within a sector consists of five fields.
- The state of the three triggers of the format control ring are decoded to define the fields within a sector.
- The format control ring runs once for each sector and may continue unless forced to reset.
- The ring is forced to reset after the end gap field, unless writing or reading across sector boundaries.
- The format control ring is always reset after the end gap of sector 7 (end of track).

The track format for both write and read is shown in Figure 1-3. Each of the five fields of the track format is defined by the state of triggers TR-1, TR-2 and TR-3 (Figure 2-9).

Initially all triggers are off and they are decoded to activate the FC ring off line. When a write or read command is sent to the SDSD and the addressed sector is found, the write or read trigger comes on and fires the first gap singleshot, and a 500 nanosecond pulse is available as the format control ring drive. If the write trigger is on, the first gap singleshot provides the dc set pulse for byte counter position 32, defining the first gap as 32 bytes long.

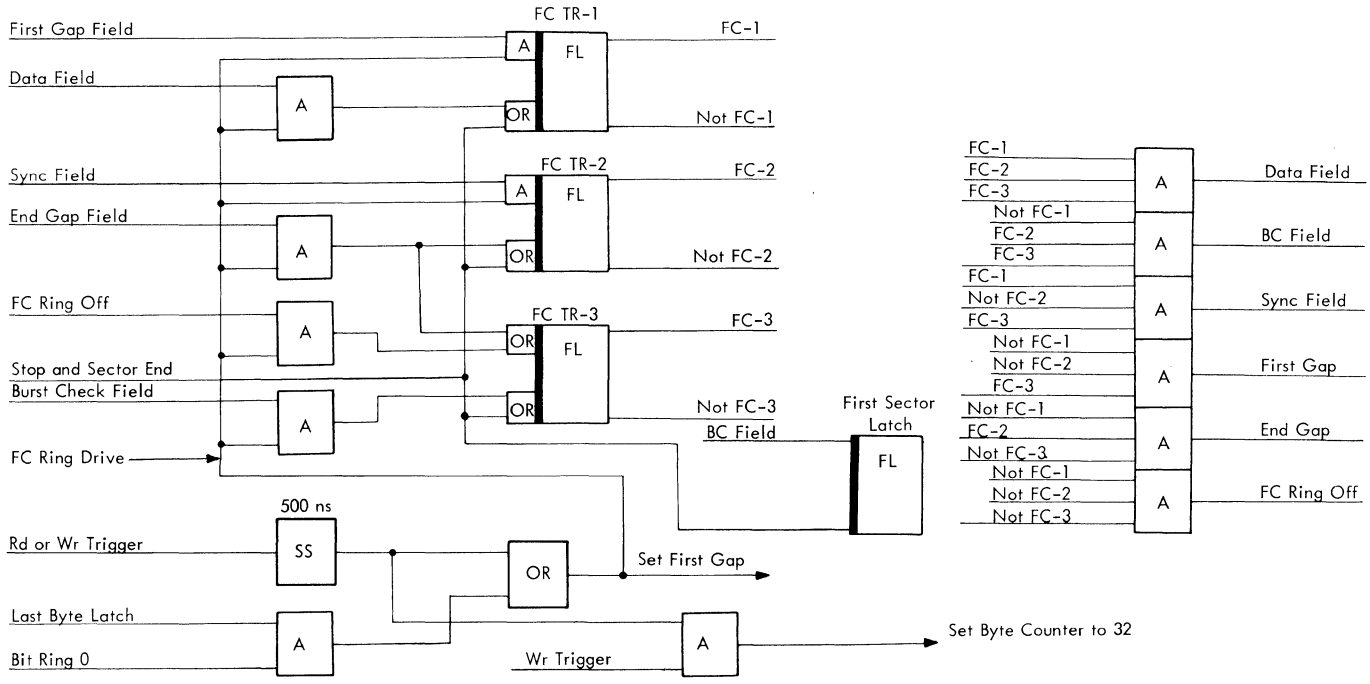


Figure 2-9. Format Control Ring and Decoder

If the read trigger is on, the first gap is defined as being a half-byte by ANDing read trigger and set first gap to provide a set for the last byte latch.

With the format control ring drive, TR-3 is turned on and this decodes as first gap field. The format control ring remains in this state until the next format control ring drive pulse occurs. Further format control ring drive pulses, for the remainder of the sector, can only occur at bit ring zero time when the last byte latch is on.

At the end of the first gap field, the format control ring advances to define the sync field as trigger TR-1 turns on, and the appropriate byte count is set into the byte counter. The format control ring is similarly advanced at the end of each field and the decoding of the triggers defines the following field.

If the write or read command is completed in one sector, the format control ring is then reset off by the stop and sector end pulse. However, if the Channel Command Word (CCW) byte count is greater than 366, writing or reading must be continued in the following sector. In this case, after the end gap, everything (including the write or read trigger) is reset with the exception of the format control ring. Therefore, TR-2 of the format control ring stays on over the sector boundary and when the write or read trigger comes on again (because end gap is on) in the following sector, the format control ring drive pulse is generated. This causes TR-2 to switch off and TR-3 to switch on, thus, the format control ring advances from end gap to first gap without going off.

The format control ring timing chart (Figure 2-10) shows the ring operation when writing and reading over a sector boundary.

BIT RING

- A three-position trigger ring, decoded to define each bit of a byte.
- When all triggers are off, bit ring 3 is decoded.
- Bit ring drive is supplied by gated write clock or read clock pulses.
- Stepping the bit ring causes only one trigger to change state at one time.
- Bit ring decoded output is used on write to convert a parallel data byte into serial data for disk recording.
- When reading, the bit ring decoded output gates the serial data from the disk into the correct buffer positions.
- Bit ring decoded output is used extensively as timing pulses.
- Bit ring is always reset at the end of each sector, during end gap.

The bit ring output has many functions in the control unit, but is basically used to define each bit of each byte. The bit ring (Figure 2-11) is a three position trigger circuit, the drive to which is controlled by the bit ring control latch. The drive pulses to the bit ring are provided by either the write clock or the read clock.

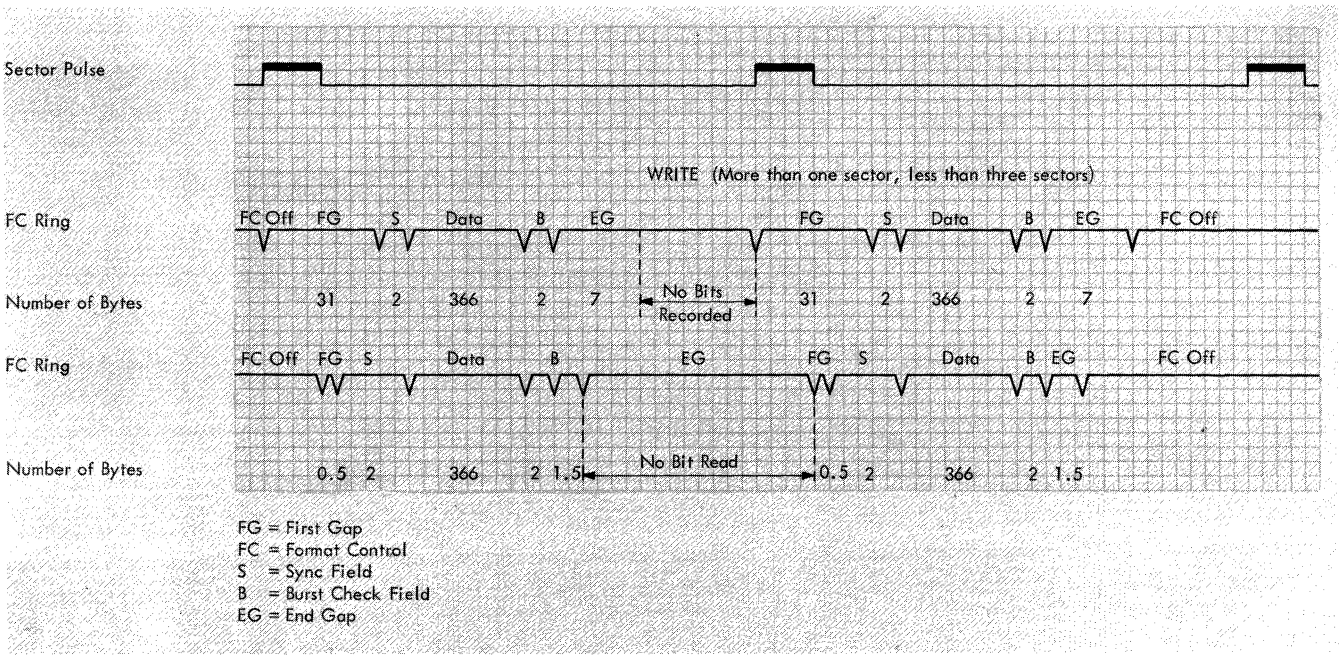


Figure 2-10. Format Control Timing

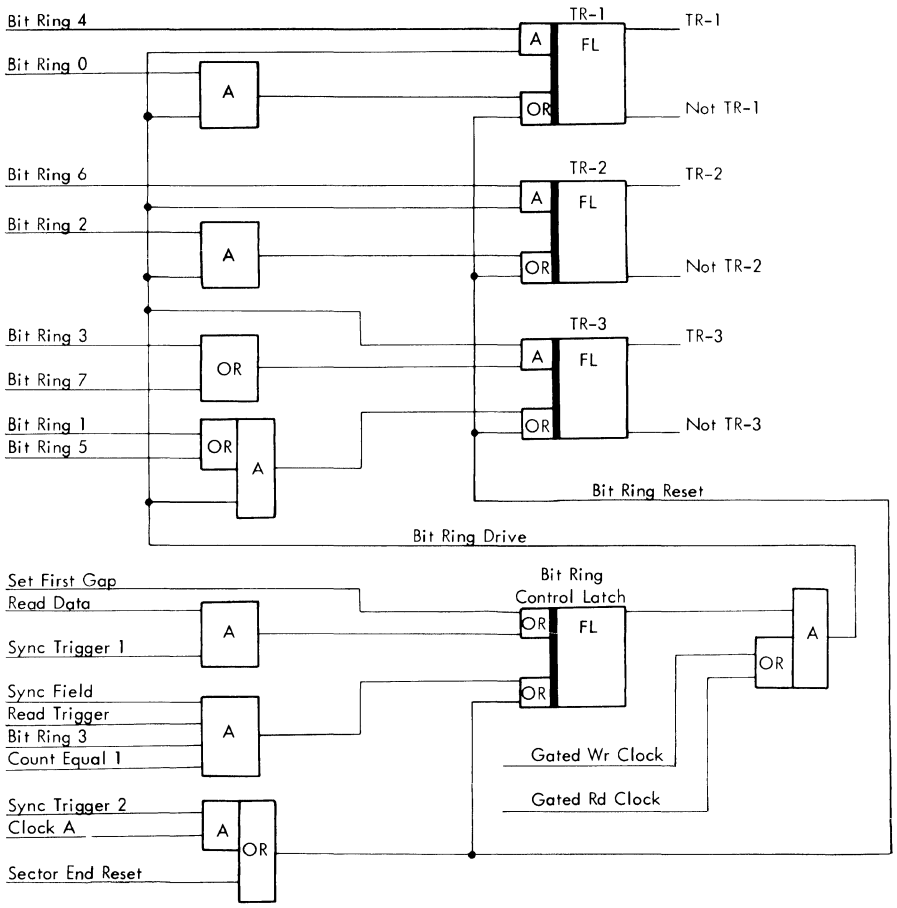


Figure 2-11. Bit Ring

The outputs of the three triggers are decoded (Figure 2-12) to define each bit ring time. Bit ring 3 time occurs when the bit ring is reset; stepping the bit ring from this position causes TR-3 to switch on, defining bit ring 4. The decoding of the trigger outputs decides which trigger switches on or off with the next drive pulse. Note, that the drive pulse causes only one trigger to change state at one time, and that the bit ring advances (as tabulated in Figure 2-11).

The bit ring is allowed to function by set first gap, which is coincident with the write or read trigger switching on. When writing, the bit ring runs continuously from the start of the sector pulse until reset by sector end reset, at completion of the end gap. Initially, in a read operation, the bit ring drive is provided by the read trigger switching on at the fall of the sector pulse. However, the bit ring stays on for only 20 microseconds before the bit ring control latch is reset at bit ring 3 time. When the first 1 bit of the sync field is read the control latch is turned on, gating the drive pulses to the bit ring. The bit ring runs continuously from this point until reset (to bit ring 3) at sector end.

On a write operation, the bit ring output is used to convert a byte of data, received from the channel, into serial data to be recorded on the disk. On a read operation, the bit ring output is used to convert serial data into eight-bit bytes. Serial data bits from the disk are set into the correct buffer positions by the decoded outputs of the bit ring occurring as timing pulses. (See Figure 2-2.)

Individual bit ring decoder outputs are used throughout the control unit logic as timing pulses. The bit ring is always reset at the end of a sector and is never allowed to continue running over the sector boundaries, even when write or read over sector boundaries is specified.

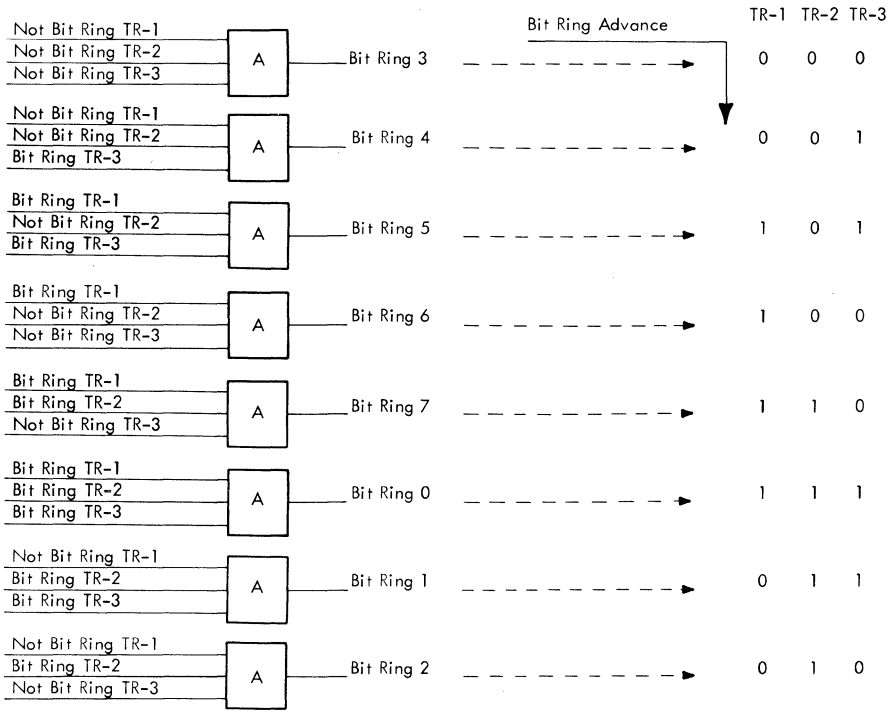


Figure 2-12. Bit Ring Decoder

SECTOR COUNTER AND CHECK COUNTER

- Sector counter and check counter are identical circuits.
- Contents of both counters are constantly compared to provide a reliability check.
- Sector counter is a three-position binary counter.
- Counters are always reset in sector 0 by the reference pulse.
- Counters are advanced, in every sector, 2 milliseconds after sector pulse.
- The contents of both counters and the specified sector address must agree before either write or read trigger is allowed to turn on.

Because the logic for the sector counter and the check counter is the same, only the sector counter is described. The counter is a three-position binary counter (Figure 2-13) which is reset on every revolution of the disk by the reference pulse in sector 0. When the sector pulse for sector 0 occurs, the contents of the counters are zero and, if the sector address is zero, the write or read trigger is allowed to turn on. The rise of the sector pulse fires a 2 millisecond singleshot (SS-1). When SS-1 times out, SS-2 is fired (2 millisecond duration) and is used to

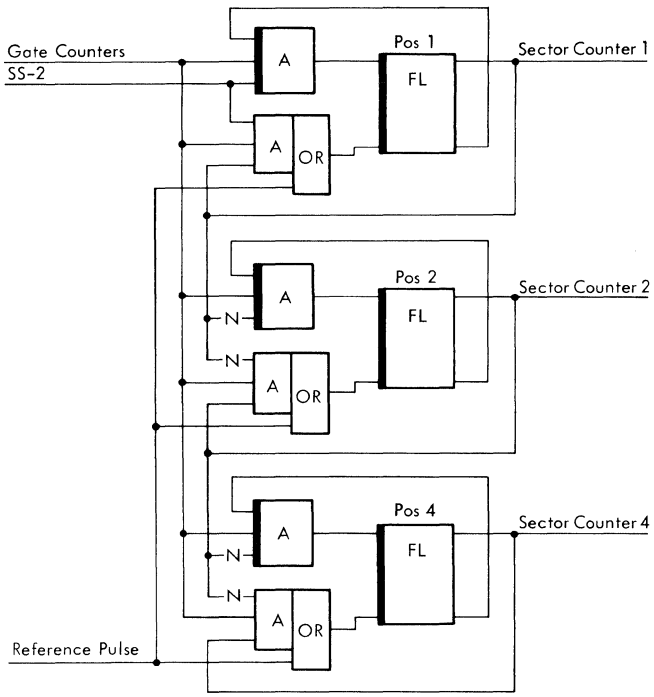


Figure 2-13. Sector Counter

increment the sector counter; its content is then one, in readiness for address matching when the sector pulse for sector 1 rises. Address matching ensures that no erroneous erasure of data occurs by writing in the wrong sector.

The contents of the sector counter and the check counter are continuously compared to check that the sector counter is functioning correctly.

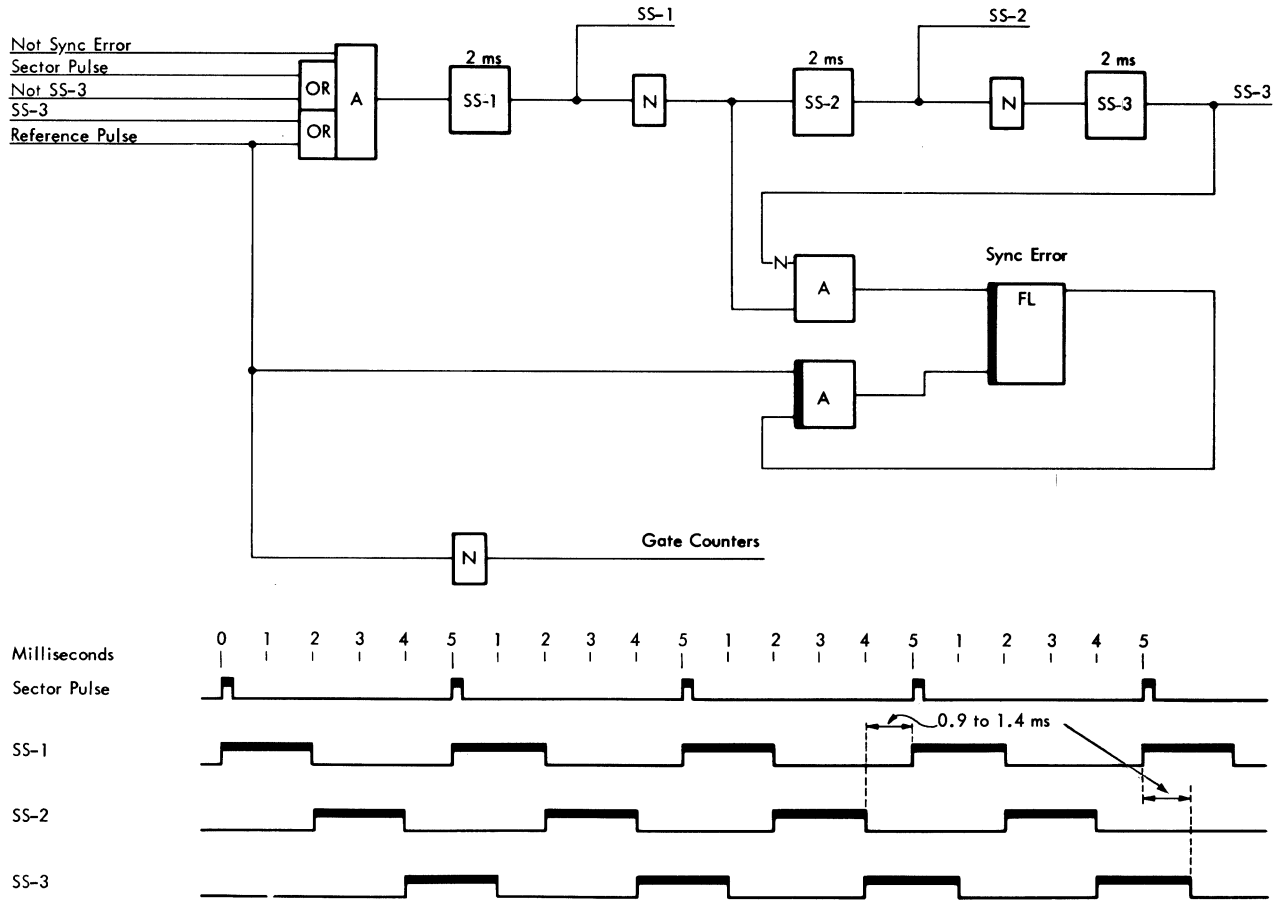


Figure 2-14. Sector Sync Check

SECTOR SYNC CHECK

The purpose of the sector sync check circuit is to ensure that the sector pulses occur within specified time limits. The three 2 millisecond singleshots and the sync error trigger that constitute the sector sync check logic are shown in Figure 2-14, together with the appropriate timing chart. The three singleshots are fired consecutively. SS-1 is fired initially by the reference pulse, SS-2 fires on the fall of SS-1, and SS-3 fires on the fall of SS-2. Thereafter, because SS-3 is on, SS-1 is fired at the beginning of each sector by the sector pulse. As the duration of each singleshot is 2 milliseconds, the sector pulse, occuring 5 milliseconds later, fires SS-1 when SS-3 is on. If SS-1 has not fired when SS-3 times out (after 2 milliseconds) the sync error trigger sets. This sync error signifies that the sector pulse did not occur within the specified limits. A sync error prevents the setting of the read or write trigger. The sync error trigger, once set, remains on until reset by the next reference pulse in sector 0. This reference pulse also fires SS-1 and the preceding process is repeated.

It is possible, due to an error condition, to have a hang-up situation where no sector can be found. That is, the contents of the sector and check counters agree but the sector address does not match. This situation is detected by use of the first reference found trigger (Figure 2-15). This trigger is set at the fall of the reference pulse and is normally reset by the stop and sector end pulse which is present only when ending the writing or reading of a sector. If, because of an error condition, no sector can be found, then the write or read trigger cannot be turned on and the stop and sector end pulse cannot occur to reset the first reference found trigger. Thus, after one revolution of the disk, the next reference pulse occurs when the first reference trigger is still on. This is an error condition and the sync error latch is set. The 'stop and sector end pulse' is forced and resets the first reference found trigger.

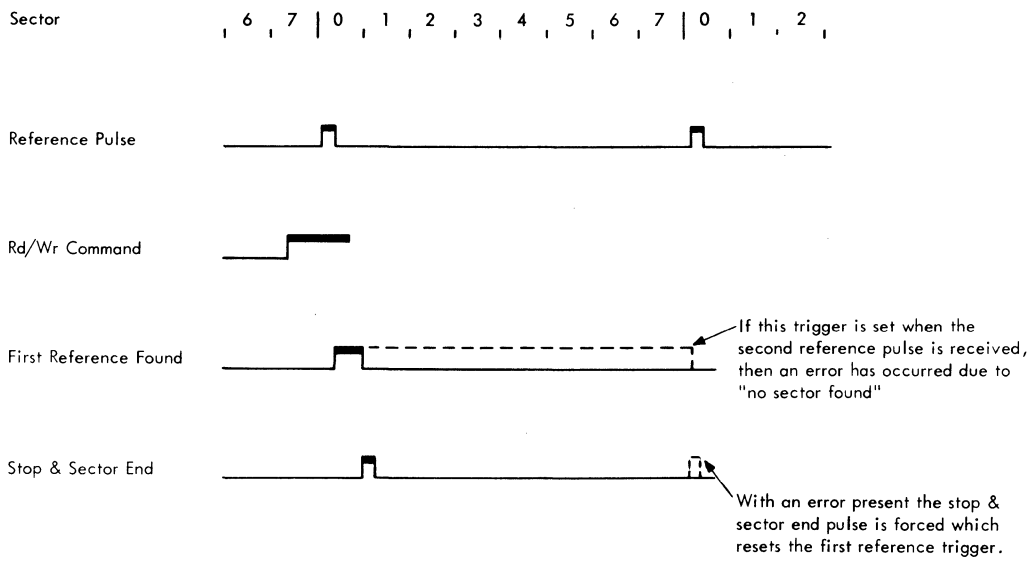
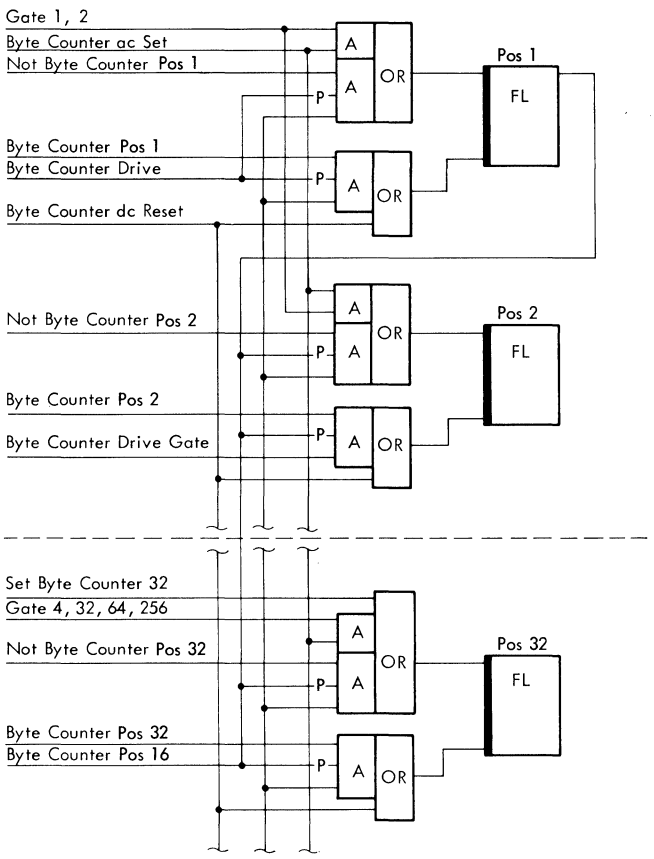


Figure 2-15. First Reference Found Operation



NOTE: 1. Byte counter positions 4,8,16 and 64,128,256 are similar to position 2 shown, with the appropriate gate.
2. Position 32 has a special dc set used on write for first gap.

Figure 2-16. Byte Counter

BYTE COUNTER

- Defines number of bytes in each field as in the track format.
- Nine-position binary counter.
- Reduced by one at every bit ring 0.
- Drive pulse to byte counter changes the state of position 1 trigger only.
- Remaining counter positions change only when previous position goes on.

The byte counter (Figure 2-16) is a nine-position binary counter; each position being named with its binary equivalent value. The counter is used to specify the number of bytes of each field as detailed in the fixed-track format. The byte counter drive and drive gate are provided during bit ring 0 time. The drive pulse is fed to position 1 only, setting or resetting that position, and the counter contents are reduced by one. In normal operation of the counter, the remaining eight positions will only switch when the previous position goes on.

The setting of the byte counter contents for each field is shown in Figure 2-17 and a simplified timing chart of the byte counter operation when crossing field boundaries is shown in Figure 2-18. The appropriate gate is activated to the required byte counter positions for setting the correct count in the counter. However, the counter is not set with the byte count of the following field until bit ring 7 time of the last byte of the present field. Note, that the

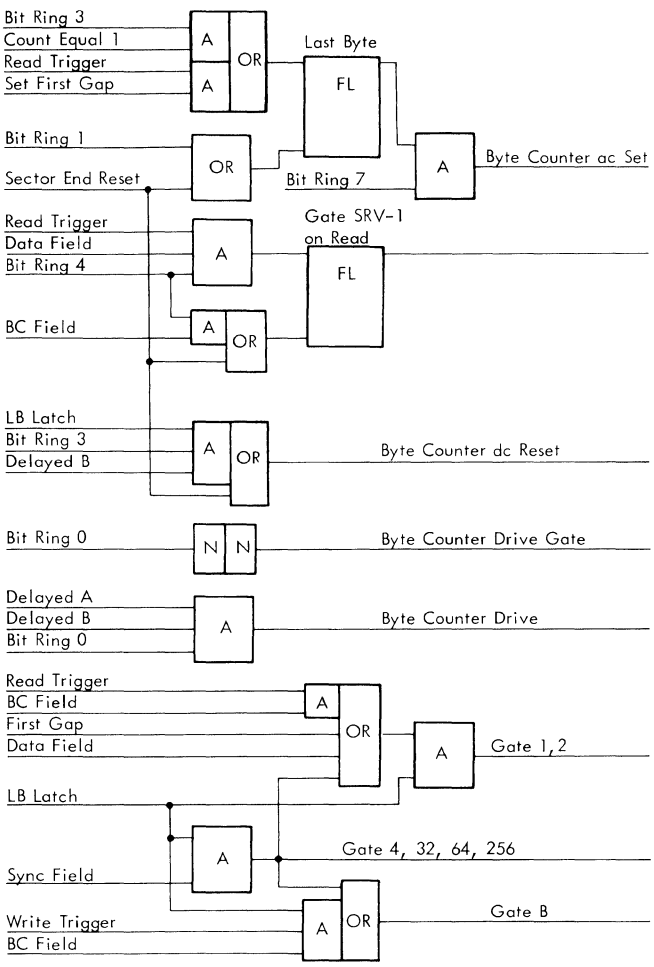


Figure 2-17. Byte Counter Controls

byte counter was previously dc reset at bit ring 3 of this last byte.

The count initially set into the counter is always one more than that required for the following field. This is done because the byte counter drive is at bit ring 0 time and the counter is reduced immediately on crossing field boundaries. Because the byte counter ac set pulse relies on the last byte latch being on, the first gap field, when writing, uses another method of setting the byte counter.

This method is a dc set to byte counter position 32 and is used solely to set a byte count of 32 for the first gap on write. On read, the first gap forces the last byte latch on and the byte counter is set to 3.

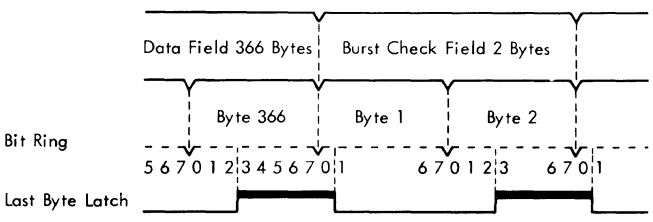


Figure 2-18. Byte Counter Operation

SYNC FIELD RECOGNITION

- Sync field ensures that the bit ring starts at the correct time to read the following data field.
- Two triggers are used to detect the presence of four consecutive ones in the sync field.
- If sync field bits are not consecutive, the bit ring is reset.

Recognition of the sync field is relevant only when reading, because the bit ring must 'get in step' with the recorded clock pulses. The two-byte sync field is recorded as 0000 0000 0001 1110 binary (00 1E hex). The read trigger is turned on at the fall of the sector pulse, and clock pulses only are read from the disk (data zero bits) until the first of the four consecutive 1 bits is encountered.

The rise of the first read data bit (Figure 2-19) turns bit ring control latch on, allowing the bit ring to advance to bit ring 4, and sets sync trigger 1. Clock B pulse, following the first bit, resets sync trigger 1, and sets sync trigger 2.

The rise of the second read data bit sets sync trigger 1, and the fall of the second read data bit resets sync trigger 2 before the next clock A pulse.

NOTE: Failure to reset sync trigger 2 before clock A, results in the reset of the bit ring to bit ring 3.

Clock B pulse, following the second bit, resets sync trigger 1, and sets sync trigger 2.

The rise of the third read data bit sets sync trigger 1, and the fall of the third read data bit resets sync trigger 2.

NOTE: Failure to reset sync trigger 2 before clock A, results in the reset of the bit ring.

Clock B pulse, following the third bit, resets sync trigger 1, and sets sync trigger 2.

The rise of the fourth read data bit has no effect, as sync trigger 1 cannot be set at bit ring 6. The fall of the fourth read data bit resets sync trigger 2.

Both triggers now remain off and the bit ring is allowed to run.

DATA SEPARATOR

- Raw data from disk consists of interleaved clock and data pulses.
- Three singleshots used to separate read clock and read data pulses.

A read operation is a self-clocking operation, because the read clock relies upon the clock pulses read from the disk. The clock pulses read from the disk are intermingled with data pulses and the two

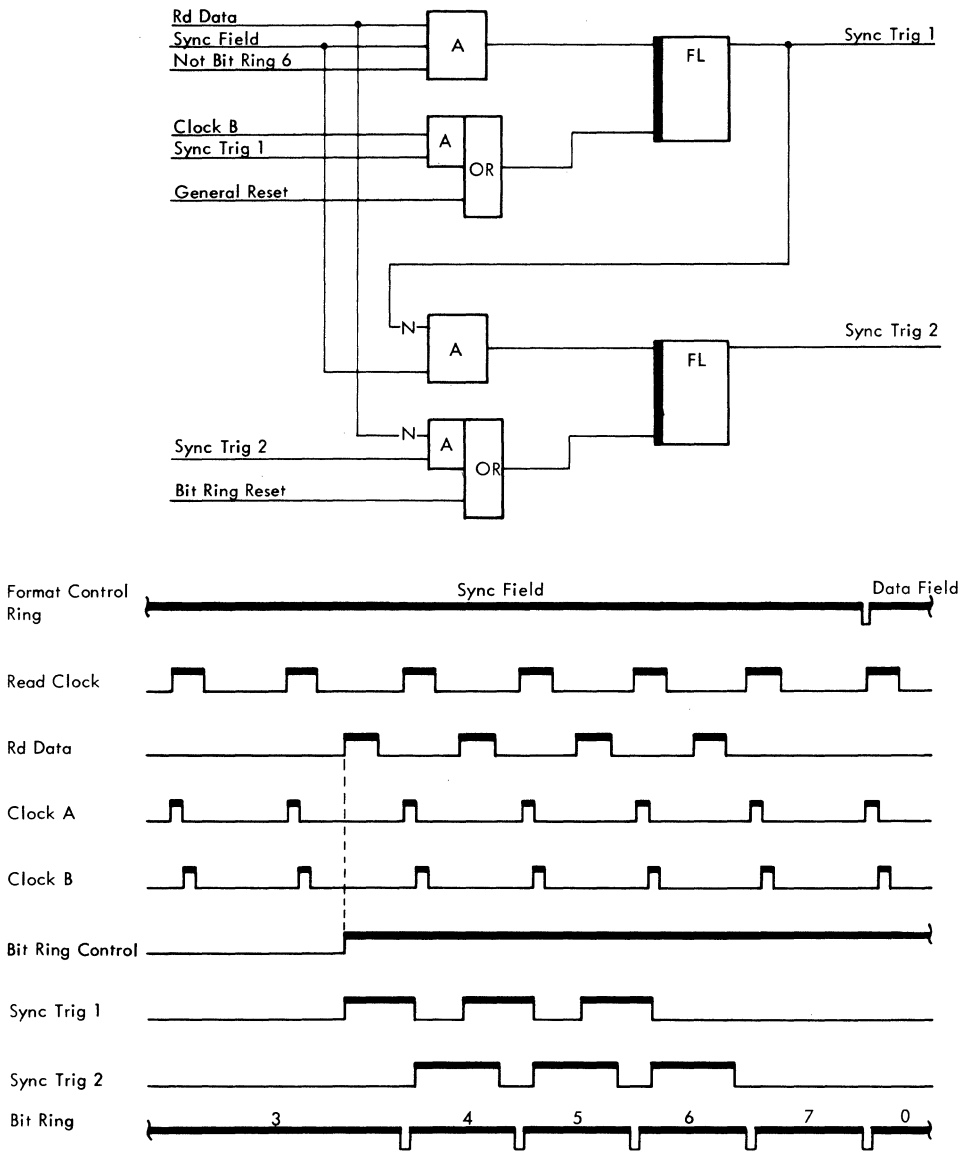


Figure 2-19. Sync Field Recognition

types of pulses must be separated. This is the function of the data separator circuit (Figure 2-20).

The three singleshots are arranged in cascade and, initially, because only clock pulses are being read during first gap, the raw read data line fires SS-1 every 1,400 nanoseconds. When SS-1 turns off, after 400 nanoseconds, SS-2 fires. SS-2 is an adjustable singleshot and it is adjusted to cover the time coincidence of the data pulse. As only clock pulses are being read prior to the sync field ones, SS-3 cannot switch on because it requires the coincidence of a data pulse with SS-2.

When a data pulse does occur, SS-3 fires during the time of SS-2. SS-3 is a 400 nanosecond singleshot the output of which is the read data line. The data pulse cannot fire SS-1 again because SS-2 is on at this time. Thus, SS-1 fires on clock pulses and SS-3 fires on data pulses, both singleshots giving a 400 nanosecond output.

BUS-IN FUNNEL

The bus-in funnel allows one byte of information to pass to bus in of the standard interface when the appropriate tag line is active. The table in Figure 2-21 shows the content of the bus in lines in all cases. For example, when service in is active, the I/O register is gated to bus in; when status in is active, a status byte is gated to bus in, and when address in is active, the control unit address is gated to bus in. In reply to a sense command, the sense byte is gated to bus in. Note, that the operational-in line must be active before the bus in lines are valid.

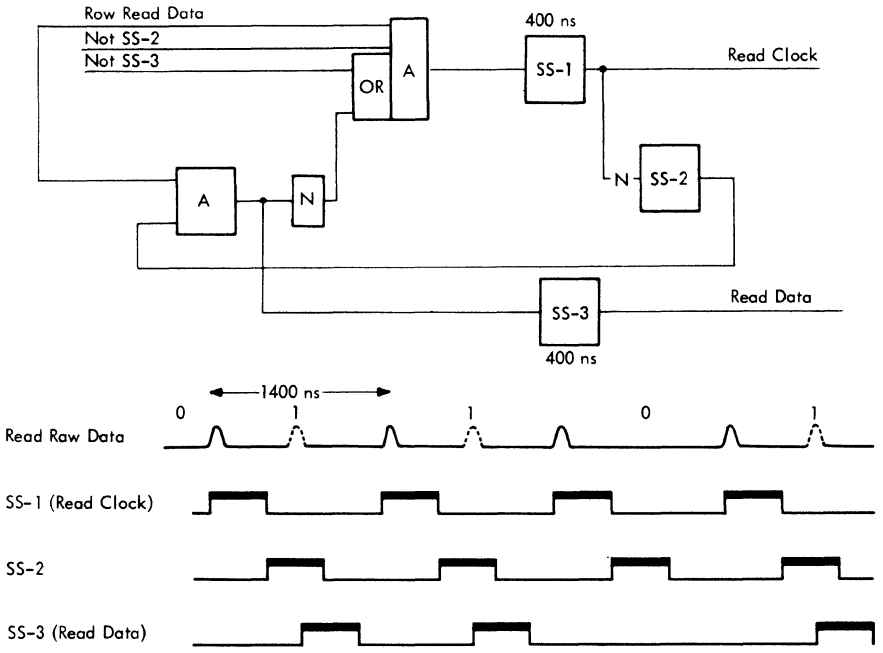
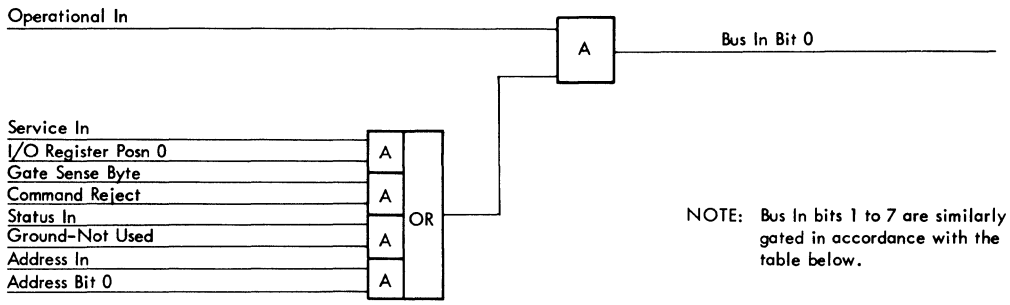


Figure 2-20. Data Seperator



Bit Position	Service In	Sense Byte	Status In	Address In
0	I/O Reg Posn 0	Cmnd Reject	Not Used	Address Bit 0
1	" " " " 1	Not Ready	" "	" " 1
2	" " " " 2	Bus Out Check	" "	" " 2
3	" " " " 3	Wr Sel Error	Device Busy	" " 3
4	" " " " 4	Data Check	Chan End	" " 4
5	" " " " 5	Overrun	Device End	" " 5
6	" " " " 6	Sector Check	Unit Check	" " 6
7	" " " " 7	Seek Icplt	Not Used	File 1

Figure 2-21. Bus In Funnel

CHANNEL WRAP

- Simulates the operation of an extremely fast I/O device on the standard interface.
- Allows the channel to work at its maximum data rate.
- All commands are valid in wrap mode.

Provided that either the system reset button or the control unit reset switch on the console has been set, setting the channel test switch on at the console sets a channel test latch in the SDSD control unit, and the file ready light goes off. This is the only effect of activating the channel test switch; there is no further action until a start I/O instruction is issued. This instruction is generally issued during the associated diagnostic program (CLT) or it can be part of a pro-

gram entered manually via the console keys. In either case, to the channel, the start I/O instruction appears to be executed normally with correct responses from an extremely fast I/O device. In fact, no data is either recorded or read from the disk when the appropriate command is generated. The I/O register performs as for normal read and write operations, but the read or write command to the file is suppressed, as is the seek command. This suppression is part of the function of the channel test latch.

With the channel test latch on, the following conditions and functions can occur.

1. File ready light is set off.
2. Read backward is a valid command.
3. IPL latch cannot be set.
4. Unit check cannot be set by a file malfunction.
5. Read and write command to files cannot be set.
6. Seek command latch cannot be set.
7. A control command causes channel end and device end to be generated together (equivalent to control no-op command).
8. Channel end and device end are generated only by a channel initiated stop or halt I/O.
9. The I/O register reset is prevented, on command out from the channel.

A description of the effect of the above conditions on the operation of each of the five commands follows.

Operation

Write

A data byte is transferred from the channel to the control unit I/O register. Nothing is recorded on the disk because the write command to file line is degated, preventing the turn on of the write trigger. Transfer of the data byte from channel to the I/O register continues until the channel commands stop, by sending a command out tag in reply to service in. The last byte transferred remains in the I/O register, because the I/O register reset is prevented. A channel end and device end status is presented to the channel, but a unit check status is not possible.

Read

This command causes the byte contents of the control unit I/O register to be transferred to channel via the standard interface. The content of the I/O register is constant (the read out is non-destructive), so that same byte is repeatedly transferred to the channel. The byte in the I/O register will be zero unless this read command is issued after a write command, in which case, the byte left in the I/O register at the end of the write operation becomes the byte transferred on the read operation. No data is read from the disk because the degating of read command to file prevents the read trigger turning on. Data transfer of the same byte continues until the operation is stopped by the channel, and channel end and device end status are presented to the channel.

Read Backward

This is a valid command to the SDSD control unit when the wrap facility is in use. The action in the control unit is identical to that of the read command described previously.

Control

All control commands are treated as control no-op commands and cause an immediate status response of channel end and device end. As the seek command latch is degated, the access arm does not move in response to a control seek command.

Sense

A valid sense byte, gated to channel in response to a sense command, can contain either or both bit 0 (command reject) and bit 2 (bus out check).

CHAPTER 3. PRINCIPLES OF OPERATION

This chapter describes the operation of the control unit when performing the seek, write, read, sense and test I/O operations. Each of these operations are commands specified by the first byte of a channel command word.

The issue of a start I/O instruction by the CPU first determines if the disk and channel are available to accept a new command. If available, a CCW is set into the channel and the command is sent to the disk control unit over the standard interface with the command out tag raised. If the command is accepted by the control unit, the status byte sent to channel will be zero, but if the command is rejected, the unit check bit will be in the status byte.

Each command is now dealt with in more detail.

SEEK COMMAND

- A control command specified by 0B hex in the first byte of a CCW.
- CCW data address specifies one byte containing the track address.
- CCW count must not be zero.
- One data byte (containing track address) is sent to the control unit.
- Track address is validity checked and, if good, channel end status is sent to the channel.
- Device end status is sent to the channel upon completion of the seek operation.
- A track address greater than 202 causes a unit check status, together with channel end and device end, to be presented.

The CCW containing the seek command also contains a data address which specifies the address of one byte of data. This data byte is the required track address which is sent to the control unit over the standard interface with the service out tag active. The track address enters the I/O register in the control unit and is checked for validity. A track address of 203 or greater is invalid and initiates a status in reply to the channel with the status byte containing channel end, device end and unit check.

A valid track address causes channel end only to be sent to the channel in a status byte, and the track address is transferred to the SDSD via the eight address lines of the SDSD interface. The access drive pulse to the disk mechanism is also initiated, firing a 200 millisecond singleshot in the device. This time-out singleshot represents the maximum allowable time for a complete seek operation through all tracks. Should the singleshot time out, a device end status with unit check is sent to channel, and the seek incomplete bit is set in the sense byte. The seek incomplete condition can only be reset by the issue of another seek command.

A seek command which follows another seek command by less than 200 milliseconds causes the time-out singleshot to reset and start again. When the head is correctly positioned over the addressed track, the SDSD sends access ready to the control unit, and the control unit sends device end status to the channel. This completes a seek operation and the control unit awaits a new command from the channel.

Another form of control command is control no-op and its format in the first byte of a CCW is 03 hex. This control no-op command causes the control unit to send a status byte to the channel containing the channel end and device end bits.

WRITE COMMAND

- A write command to the SDSD contains the head and sector address in the first four bits.
- The head is already positioned over the required track by a previous seek command.
- A complete record of 2,928 bytes, occupying one track, can be recorded.
- Write trigger is reset, and set again in the next sector, when writing across sector boundaries.
- All writing terminates at the end of sector 7 (end of track).
- Track address is recorded on every track in the first four bytes of the data field in sector 0.
- Channel end and device end are always generated together, at the end of a sector in which a write operation terminates.

Command Initiation

The format of the command code in the first byte of the CCW is HSSS 1001, where H specifies head 0 or 1, and SSS determines the sector (0 to 7) where writing is to begin. The binary 1001 is decoded by the SDSD control unit to be a write command. Thus,

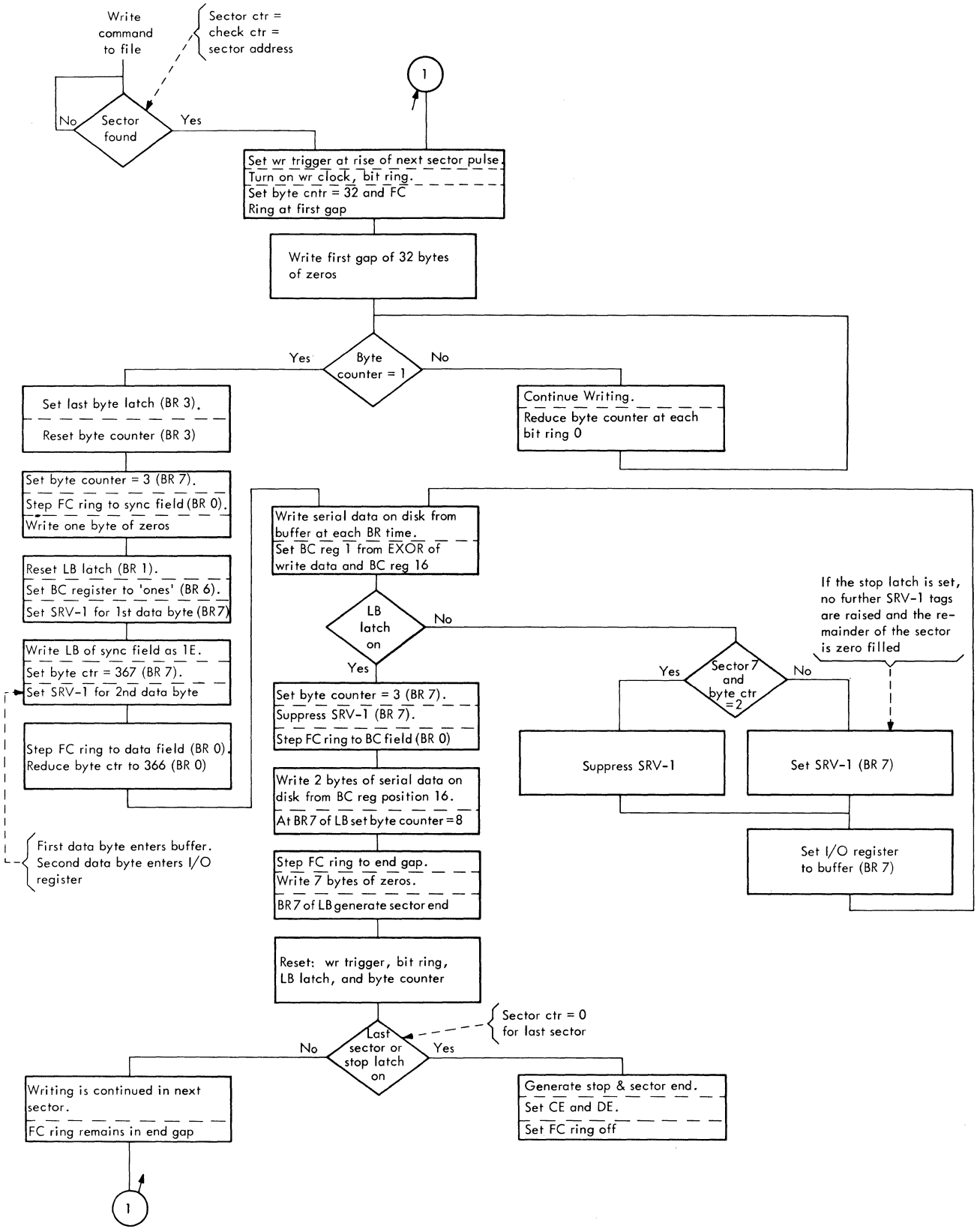


Figure 3-1. Write Operation

writing can commence on the track over which the head (H) is positioned as soon as sector SSS is found.

When command out is raised and the command is sent on bus out to the control unit, bits 1, 2 and 3 of bus out are gated directly into the buffer register. This is the three-bit sector address which is compared with the contents of the sector counter to generate sector found when a match occurs (Figure 3-1). Because the sector counter contents are predicting the next sector, the sector found line becomes active before the sector pulse of the required sector. However, as the write trigger cannot turn on until the rise of the next sector pulse, the recording of spurious bits in the middle of a sector is avoided.

First Gap Field

With the rise of the sector pulse the write trigger in the control unit turns on, allowing other circuits to function. A first gap singleshot (500 nanoseconds) is fired which advances the format control ring to define the first gap field. The singleshot also dc set sets the byte counter to 32 and sets the bit ring control latch, allowing the bit ring to run. The bit ring now runs continuously until the end gap, and at each clock phase A a clock pulse is written on the disk surface.

During the 32 bytes of the first gap, only clock pulses are recorded because data pulses can be recorded only during the sync, data or burst check fields.

The contents of the buffer register are significant only for the recording of data pulses during the data field. The byte counter is reduced at each bit ring 0 time and thus 32 bytes of zeros are recorded as the first gap field. The last byte latch comes on at bit ring 3 (Figure 3-2) and resets the byte counter. At the following bit ring 7 time the byte counter contents are set to 3 in preparation for the next field. (See Figure 2-16.) At bit ring 0, with the last byte latch on, the format control ring advances to define the sync field, and the byte counter is reduced to 2. (See Figure 2-8.)

Sync Field

Zeros are recorded in the sync field until bit ring 3 of the second byte. At this time, the last-byte latch comes on and ones are recorded in bit positions 3, 4, 5 and 6. Thus, the 2-byte sync field is recorded as 00 1E hex. During the sync field, at each bit ring 7 time, a service in request for data is sent to channel. The first data byte from channel is shunted through the I/O register to the buffer register before the first bit of the data field is recorded. The second data byte enters the I/O register before the first data bit is recorded. Thus, at the end of the sync field, the first and second data bytes are in the buffer register and I/O register respectively. At bit ring 7, the byte counter contents are set to 367 before the format control ring advances to define the data field at bit ring 0.

Data Field

The contents of the buffer register are now serialized by the bit ring and recorded on the disk bit by bit. (See Figure 2-2.) The serial data is also EXORed into the BC register to form the burst check pattern. The control unit raises service in at clock D every bit ring 7 time during both the sync and data fields. During the sync field, two bytes were set into the buffer and I/O registers. When the first byte from the buffer register is recorded on the disk, a service in request at clock D and bit ring 7 causes the I/O register contents to enter the buffer register, and the third data byte from channel enters the I/O register. The byte counter is reduced at bit ring 0 and the second byte is serially recorded at the SDSD.

The recording of the data field from the buffer register continues until terminated by either of the following:

1. The channel sends a stop command because the CCW count is zero.
2. The end of record is recognized at the end of sector 7.

When writing a record with a CCW count less than 366, the remainder of the data field in the sector is zero filled. The buffer register contents are recorded normally, but as the buffer register is reset, zeros are recorded. In this case, the burst check pattern is developed normally and the burst check is for all 366 bytes, even though data may have been recorded only in one byte. The channel stops the transfer of data when the count is zero by sending command out in reply to service in. The stop latch in the control unit is set, suppressing further data requests, and zeros are recorded in the remainder of the data field. Note, that one more service in was raised than the number of bytes required (count). This allows the channel to recognize the end of the operation and stop further data transmissions. Channel end and device end are not generated until the end of the sector during end gap.

When a CCW count is 366, a complete sector is written (Figure 3-3). As there are two data bytes available before the data field is recorded, the requests to the channel for data must stop when the byte counter contents are two. Thus, when the 367th (366 + 1) service in request is raised the CCW count is zero and the channel replies with command out (stop). The stop latch in the control unit is set, preventing further service in requests, and the final

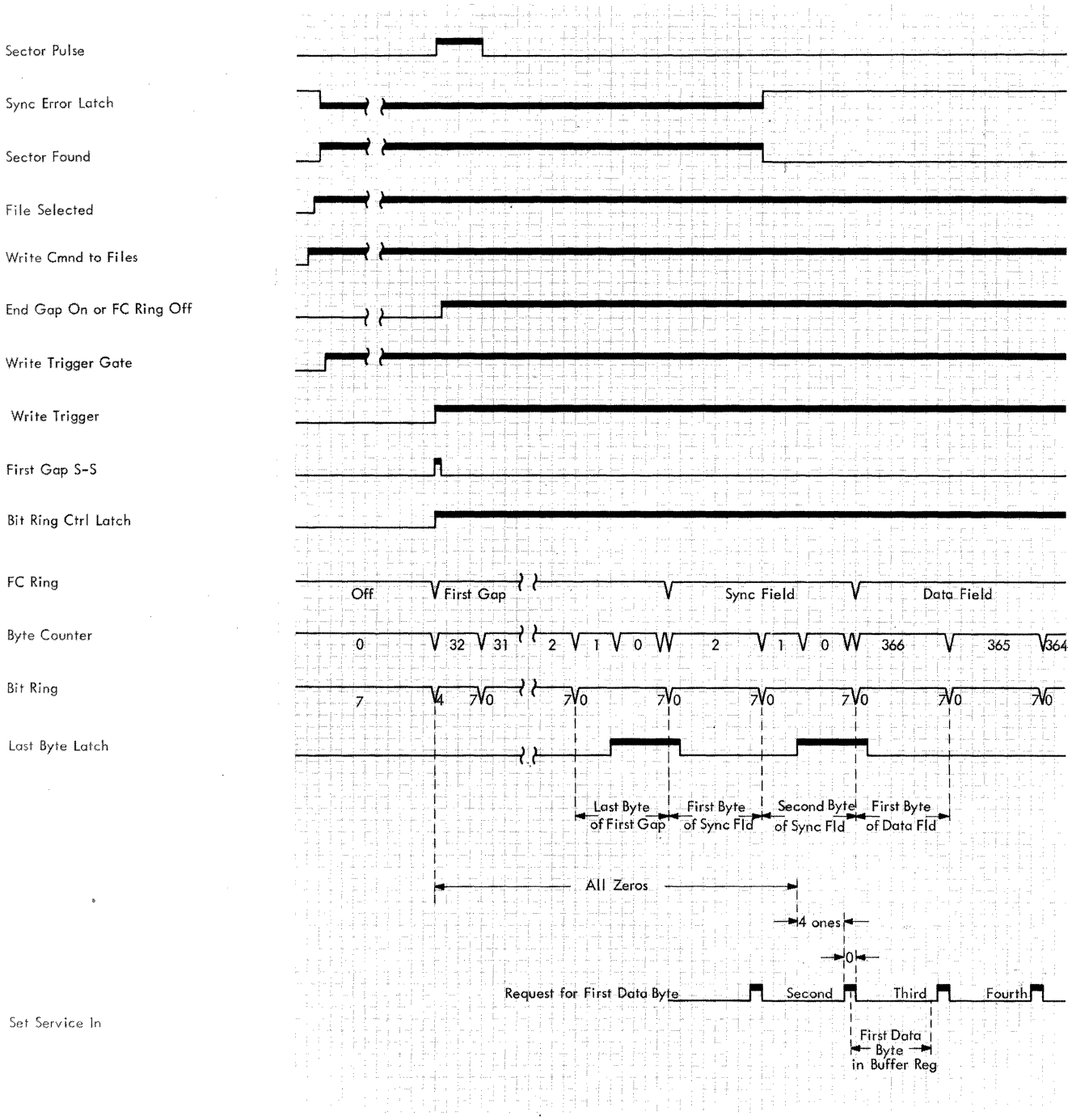
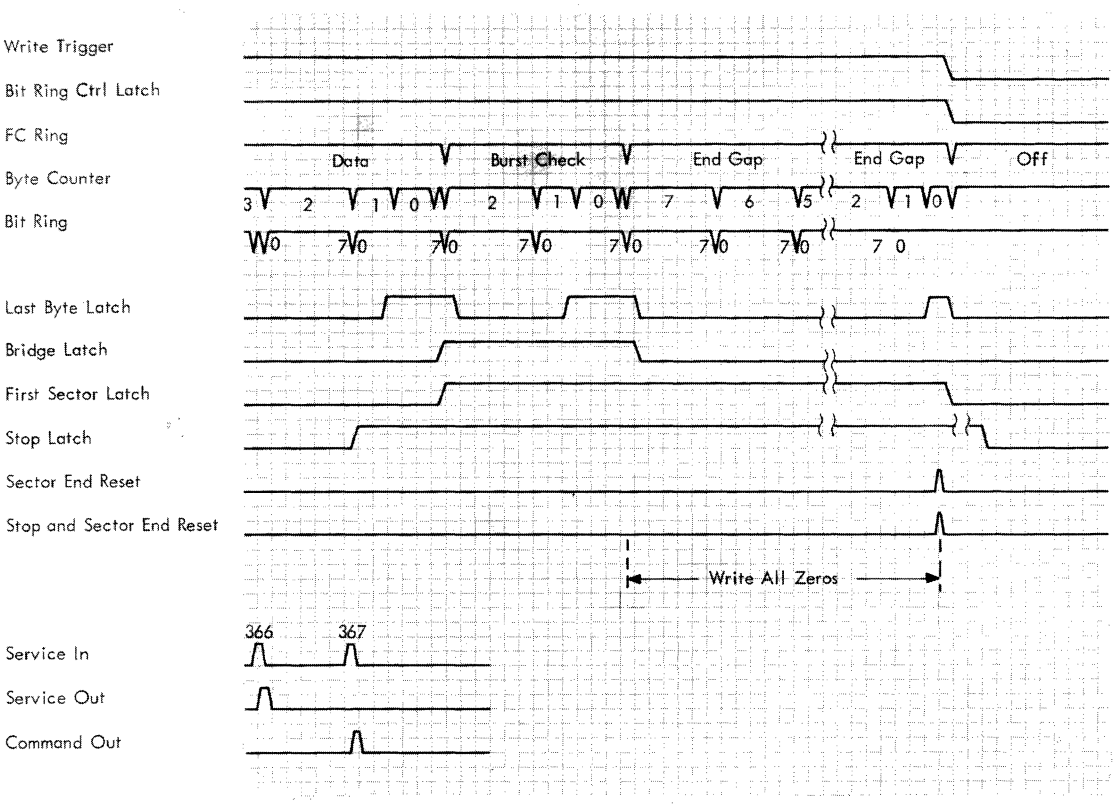


Figure 3-2. Write First Gap and Sync Field

byte of the data field is recorded from the buffer register. Note, that the last service in raised allows the channel to stop the recording. Channel end and device end are generated together during the end gap of this sector.

When a count greater than 366 is specified, writing over sector boundaries occurs, unless writing starts in sector 7. Because sector 7 is the end of record, writing from sector 7 to 0 is not allowed. The last service in possible, during the last byte of the data field, is always suppressed by the bridge latch. Thus, at the end of the first sector of a write command, the 367th service in is raised and this byte enters the I/O register. Writing of the data field has ceased in this sector, however, and this byte thus remains in the I/O register until the sync field of the next sector. The service in of the first byte of the sync field at bit ring 7 is suppressed



Notes: 1) Last service in of data field is always suppressed by bridge latch
2) When writing in sector 7 the last but one service in is also suppressed

Figure 3-3. Write Burst Check Field and End Gap

because there is already a data byte in the I/O register. The second byte of the sync field raises service in, the I/O register contents transfer to the buffer register, and the I/O register receives another data byte from bus out. Thus, when writing over sector boundaries, at the start of the data field there is a data byte in the buffer register and in the I/O register.

When writing over sector boundaries, the write trigger is reset after writing the end gap and is turned on again at the rise of the next sector pulse. The sector-found line does not have to be present to turn on the write trigger in the second and subsequent sectors, because the format control ring does not switch off but stays in end gap. The end gap condition allows the write trigger to turn on at the next sector pulse without the sector-found line present. When writing in sector 7, the last but one service in is suppressed as well as the last service in, because this is the end of record. Thus, when writing a complete record from sector 0, the first sector raises 367 service in data requests, the second and subsequent sectors raise 366 service in data requests, and sector 7 raises 365 service in data requests.

Note, that the first four bytes of the data field of sector 0 in every track contain the track address, and it is a programming function to rewrite this track address data in front of the record when writing in sector 0.

Burst Check Field

At the end of the data field, the byte counter contents are set to three and at bit ring 0 they are reduced to two. At this time, the format control ring is advanced to define the burst check field. The 16-bit checking pattern developed in the BC register is now gated out of BC register position 16, bit by bit, to be recorded on the disk as the burst check field.

End Gap Field

At bit ring 0 time, the format control ring advances to define the end gap, and the byte counter is reduced from eight to seven. Clock pulses only are recorded during the seven bytes of end gap, and when the last byte latch comes on at bit ring 5 the sector end reset pulse is generated. The sector end reset pulse resets the last byte latch, the bit ring (to bit ring 3)

and bit ring control, the byte counter, and the write trigger, so that no further recording can take place in this sector.

As shown in the timing chart in Figure 3-2, if the stop latch is on when the sector end pulse is generated, then a 'stop and sector end pulse' is also generated. This causes the first sector latch and format control ring to reset off, denoting the end of this recording. When the recording is to be continued into the next sector, the 'stop and sector end pulse' is not generated and the format control ring remains in end gap until the next sector pulse advances the ring to first gap. The format control ring remaining in end gap over sector boundaries, denotes that the command is to be continued in the next sector.

Channel end and device end are generated together, normally by the stop and sector end reset pulse when all writing has ceased.

READ COMMAND

- A read command to the SDSD contains the head and sector address in the first four bits.
- The head is already positioned over the required track by a previous seek command.
- Reading begins at the fall of the sector pulse in the specified sector.
- A complete track containing 2,928 bytes can be read.
- All reading terminates at the end of sector 7 (end of record).
- A burst check error is possible during end gap of each sector read.
- Burst check error sets data check and unit check, and prevents further data transmission.
- Channel end and device end are always generated together at the end of a sector in which a read operation is completed or terminated.

A read data command has the coding HSSS 1010 where H specifies head 0 or 1 and SSS determines the sector (0 to 7). The SDSD head is already positioned over the required track by a previous seek command. Reading commences at sector SSS and continues until either the CCW count reaches zero or the end of sector 7 is encountered, whichever is first. By starting to read at sector 0, the maximum record of 2,928 bytes can be read covering all eight sectors of one track.

In common with the write operation previously described, the sector-found condition must be active before the read trigger is allowed to switch on. Provided that there are no errors, the sector-found condition is activated halfway through the sector before the one specified by SSS in the read command. Thus, at the fall of the next 160 microsecond sector pulse the read trigger turns on. The read trigger fires the first gap singleshot (500 nanoseconds duration) which allows the bit ring, byte counter and FC ring to function (Figure 3-4). The format control ring is started and the first gap field is defined. Figure 3-5 is a flow chart of the read operation.

First Gap Field

The first gap singleshot also sets the last-byte latch, and, when the bit ring advances the first bit ring 0 time, the drive for the format control ring is provided. (See Figure 2-8.) Thus, the first gap on read lasts for four bit ring pulses (approximately 5.6 microseconds). At bit ring 7, the byte counter is set to 3 and then reduced to 2 at bit ring 0. The first gap, as recorded, consists of 32 bytes of zeros, starting from the leading edge of the 160 microsecond sector pulse and lasting for approximately 360 microseconds. Thus, starting the read operation in the middle of a valid zero field ensures that clock pulses only are provided by the read head to successfully initiate the data separator circuits.

Sync Field

The duration of the sync field is indeterminate, but should be in the order of 194 microseconds. When the format control ring advances to define the sync field, the bit ring is running and the byte counter contents are 2. After reading one more byte the byte counter contents are 1 and at bit ring 3 the bit ring control latch is reset, eliminating further bit ring drive pulses. (See Figure 2-10.) The last byte latch also comes on at this time providing a dc reset to the byte counter. This state remains until the first of the four consecutive bits of the sync field is detected.

The detection of the first bit in the sync field causes the bit ring control latch to set and the bit ring can again function. The recognition of the sync field by the detection of the four consecutive one bits is described earlier in this manual under "Sync Field Recognition" and a timing chart of the operation is shown in Figure 2-18. The BC register is set to all ones at bit ring 6 time. After the successful recognition of the sync field, the format control ring advances to define the data field.

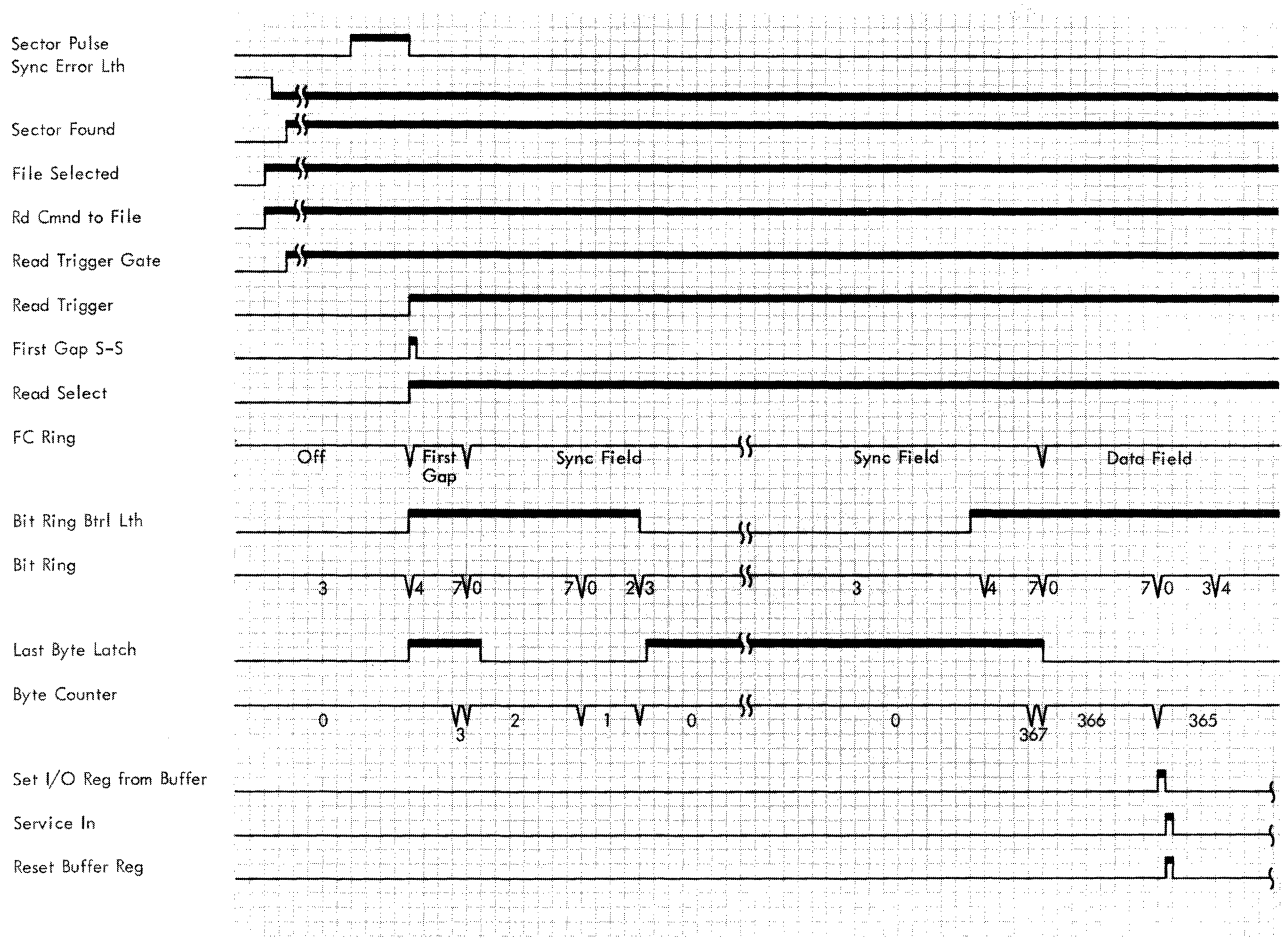


Figure 3-4. Read First Gap and Sync Field

Data Field

At the start of the data field, the byte counter is reduced from 367 to 366. The first data bit of the data field (0 or 1) appears on the read data line and is gated by bit ring 0 into buffer register position 0. At the following bit time, the read data line is gated by bit ring 1 and set into buffer register position 1. This process continues until buffer register position 7 is filled and the complete byte is in the buffer register.

During the next bit ring 0 time, the byte in the buffer register transfers to the I/O register, the service in tag is raised, and the byte is transferred to bus in. The buffer register is reset before data bit 0 of the second byte is set into buffer register position 0. The transfer of data to the channel continues and, assuming a CCW count of 366 or greater, the 366th service in data request (to transfer the last data byte of the sector) occurs during the first bit time of the burst check field. Because each bit is serially read from the disk and set into the buffer register, the output of the serializing funnel corresponds to the serial data. This serial data is set into the BC register, in the same manner as in a write operation, to form the burst check pattern. The CCW count determines the number of bytes sent to channel and this may be greater, the same as, or less, than the sector count (366).

When the initial CCW count is less than 366, the reading of the remaining bytes in a sector is still carried out, but service in is not raised and so data transfer to channel is inhibited. The burst check is performed on all 366 bytes of the data field regardless of count. The channel stops the data transfer after the count has reached zero by sending a command out reply to service in. This sets the stop latch in the control unit, preventing further service in data requests and, at bit ring 5 during the last byte of the end gap, channel end and device end are generated. The status in tag is raised and the status byte on bus in contains both channel end and device end bits. Data bytes not transferred to the channel are still assembled into the buffer register and transferred to the I/O register, but they are gated to bus in. The serial data also sets the BC register as

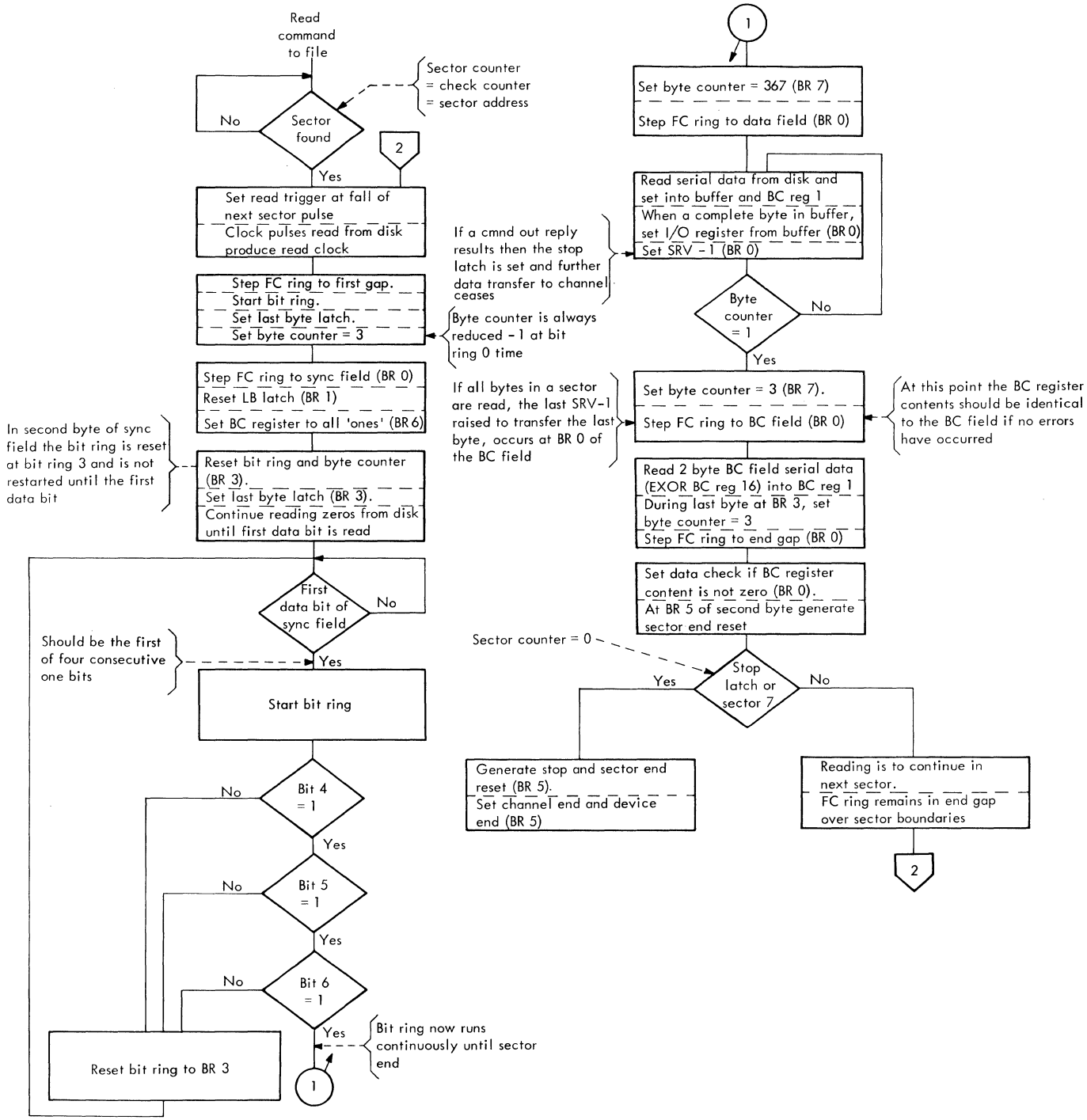


Figure 3-5. Read Operation

normal, so that data not transferred to the channel can cause a burst check error at the end of the sector.

If the count goes to zero at the 366th byte of the data field in sector 0 to 6, the first byte of the following sector is also read and a service in data request is raised. This byte is not sent to the channel because the count is zero, and the channel sends a stop command by replying with command out. The burst check in this sector is suppressed, because no data is transferred to the channel, but channel end and device end are generated at the end of the sector.

When the CCW count is greater than 366, reading across sector boundaries occurs unless the read command starts in sector 7. All reading is terminated at the end of sector 7, as this is the end of record. When reading is to be continued in the next sector, the format control ring stays in end gap over the sector boundary. With the end gap on, the read trigger can turn on at the fall of the next sector pulse without the sector-found gate present.

When the complete data field of a sector has been read, the contents of the BC register should be identical to the contents of the burst check field on the disk which is about to be read.

Burst Check Field

The two-byte burst check field follows the data field, and each bit as it is read from the disk, is EXORed with BC register position 16 to set BC register position 1. The burst check register is shifted right one position and the operation continues until the end of the burst check field, when the contents of the BC register should be zero for a no-error condition. The BC register is checked for zero contents at bit ring 0 of the first byte of end gap, and if not zero, the data check sense bit is set which also sets unit check in the status byte. Unit check sets the stop latch, terminating the read operation.

End Gap Field

Of the seven bytes of zeros recorded as the end gap, only two bytes are read before the read trigger switches off. At bit ring 0 of the first byte, the BC register contents are checked for zero, as described previously in "Burst Check Field." At bit ring 5 of the second byte (last byte), the format control ring is reset off; the bit ring and bit ring control latch, the last byte latch and the read trigger are all reset by the sector end reset pulse. If the read command is completed or terminated in this sector, channel end and device end are generated at this time, and will appear together in the status byte that is sent to the channel.

READ IPL COMMAND

- A command contained in the first byte of a CCW with the format 02 hex.
- The first four bits define the head and sector address as in a normal read command.
- A special type of command which consists of a carriage return operation followed by a read command.
- Read trigger turn on is prevented until the head is positioned over track 0, sector 0.
- Device end is generated when track 0 is reached, but is not sent to the channel until channel end time at sector end.

The read IPL command defines head 0, sector 0; the absence of bit 4 in the command byte signifies an IPL operation. Decoding the command sets the IPL latch, and the access pulse line is activated setting 'file go home'. This is a restore carriage operation causing the access mechanism to return to track 0. When the head is positioned over track 0 an access ready line is sent to the control unit, setting the device end latch. Device end to channel is suppressed by the IPL latch, but the device end condition allows the read trigger to turn on when the sector-found condition is available. Thus, reading commences at the fall of the sector 0 pulse, and channel end and device end are generated together at the end of the sector. Pressing the console load button forces a 02 read IPL command with a byte count of 24.

SENSE COMMAND

- A command contained in the first byte of a CCW having the format 04 hex.
- The presence of the unit check bit, in a status byte presented to channel, indicates that a sense byte is available at the control unit.
- The sense byte defines the cause of the unit check in the status.
- In reply to the sense command, the control unit sends the sense byte to channel on bus in with service in raised.
- Only one sense byte is available from the SDSD control unit.

When the status presented to channel during the initiation of termination of a command contains a

unit check bit, a sense command may be issued to determine the cause of the unit check. A sense command to SDSD control unit causes one byte of sense information to be sent to the channel over the standard interface with the service in tag active. No reading of information on the disk is involved because all the information is available in latches in the control unit. The appropriate latch or latches are set when the error condition occurs, and are gated to bus in when the service in tag is active in response to a sense command.

Sense Byte Format

The significance of each bit of the sense byte follows.

Bit 0; Command Reject: Indicates one of the following.

1. An invalid command has been issued, such as read backward.
2. An invalid track address has been used. The track address is transferred to the control unit after the initial selection sequence of the seek command, and the status will contain unit check, and channel end and device end bits.
3. A write command has been given to a disk with an uncleared seek incomplete condition.

Bit 1; Intervention Required: Indicates that the addressed disk is not on-line or not available because it is in a not-ready state.

Bit 2; Bus Out Check: Indicates that a parity error has been detected in data transferred from the channel to control unit on bus out. Bad parity in the command byte is a bus out check and not a command reject. If an invalid track address has bad parity, both bus out check and command reject are set.

Bit 3; Equipment Check: Indicates a write select error (a failure of the write circuit which can only be cleared by performing a stop-start sequence on the disks). This causes the disk to go not-ready and thus bit 1 is presented with bit 3.

Bit 4; Data Check: Indicates a burst check error detected during a read operation. When this bit occurs with bit 6, a sector overrun is indicated.

Bit 5; Overrun: Indicates that the channel was unable to accept or offer a byte of data to the control unit within the acceptable period (from 10 to 20 microseconds).

Bit 6; Sector Check: Indicates a sector sync check; that is, the disk is out of synchronism and preventing the writing or reading of the addressed sector. Bit 6 with bit 4 indicates a sector overrun; that is, the next sector is detected before the writing or reading of the present sector is completed.

Bit 7; Seek Incomplete: Indicates that a seek command has taken longer than the maximum access time allowed (200 milliseconds). If the disk file does not generate an access ready signal within 200 milliseconds from command initiation, the seek incomplete signal is sent to the control unit.

Bit 1 (intervention required), bit 3 (equipment check) and bit 7 (seek incomplete) signify a device malfunction and are not reset by issuing a new command. When only bit 1 is present, it is cleared by manually making the disk ready. Bits 1 and 3 occurring together is a write select error and can be cleared only by stopping the disk, waiting until the cartridge unlocked light glows, and then restarting. Another seek command to the SDSD is the only method of clearing bit 7. All other sense bits refer to the last operation that was terminated by channel end and device end. These bits are reset by the issue of a new command other than test I/O, no-op or sense.

TEST I/O

- A test I/O command is zero byte on bus out of the standard interface when the command out tag is active.
- The SDSD control unit replies to the test I/O command with a status byte on bus in.
- A test I/O command does not involve writing or reading at the disk because the status information is available at the control unit.
- Four bits only are used in the status byte provided by the SDSD control unit.

When the zero command byte of test I/O is received by the SDSD control unit, a status in reply is initiated and the state of the status latches is gated to the bus in funnel. Figure 2-20 shows the significance of the bus in lines when a status byte is gated to the interface.

Status Byte Format

Bits 0, 1, 2 and 7 are not used in the SDSD control unit and the remaining four bits in the status byte format are described as follows.

Bit 3; Busy: Sent in response to any command (except test I/O) when the control unit holds an out-

standing status. When presented on its own, this bit indicates that the addressed SDSD is between channel end and device end during a seek operation.

Bit 4; Channel End: Occurs, on its own, after the transfer of the track address byte during a seek operation. Occurs with device end during initial selection of the control command no-op and on completion of the read, write and sense commands.

Bit 5; Device End: Presented on its own at the completion of a seek command and also when the SDSD goes from the not ready state to the ready state. Presented with channel end during the initial selection of the control command no-op and on completion of the read, write and sense commands.

Bit 6; Unit Check: Presented on its own when the command byte has bad parity, is invalid, or cannot be implemented, during initial selection. When a write command addresses the SDSD with an uncleared seek incomplete condition, unit check is presented alone, and the sense byte contains the command reject bit and the seek incomplete bit. Bit 6 is presented with device end when a seek incomplete error occurs. For all other error conditions bit 6 is presented with channel end and device end.

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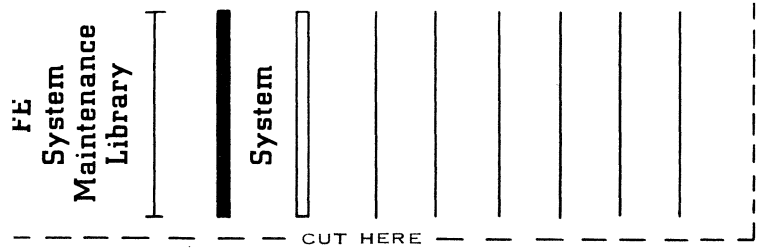

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