IBM Field Engineering

Maintenance Manual

System/360 Model 50
2050 Processing Unit

SY22-2832-4

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PREFACE

To obtain the most benefit from this manual, the reader should have a basic knowledge of System/360 concepts and general programming, and a working knowledge of the logical and physical operation of the 2050 Processing Unit. The manual includes diagnostic aids, maintenance features, and maintenance procedures along with reference material that will aid in troubleshooting and maintaining the System/360 Model 50.

Other Field Engineering Manuals written for the System/360 Model 50 include:

Comprehensive Introduction, FETOM	SY22-2821
Functional Units, FETOM	SY22-2822
Capacitor Read-Only Storage, FETOM	SY22-2823
RR, RX Instructions, FETOM	SY22-2824
RS, SI, SS Instructions, FETOM	SY22-2825
Selector Channel, Common Channel, FETOM	SY22-2826
Multiplexor Channel, FETOM	SY22-2827
Main Storage, Local Storage, Storage Protection, FETOM	SY22-2828
Power Distribution and Control, FETOM	SY22-2829
Features, FETOM	SY22-2830
2050 Processing Unit, FEMDM	SY22-2833
2050 Processing Unit, FEIM	SY22-9501

Fifth Edition (March 1971)

This is a major revision of, and obsoletes, SY22-2832-3. Maintenance strategy diagrams have been revised, expanded, and placed in the 2050 FEMDM. All CPU timing information has been removed from this manual and placed in the ALD's, Volume 1, Page AA000. Other changes or additions to text and illustrations are indicated by a vertical line to the left of the change.

Changes are periodically made to the specifications herein; any such changes will be reported in subsequent revisions or FE Supplements.

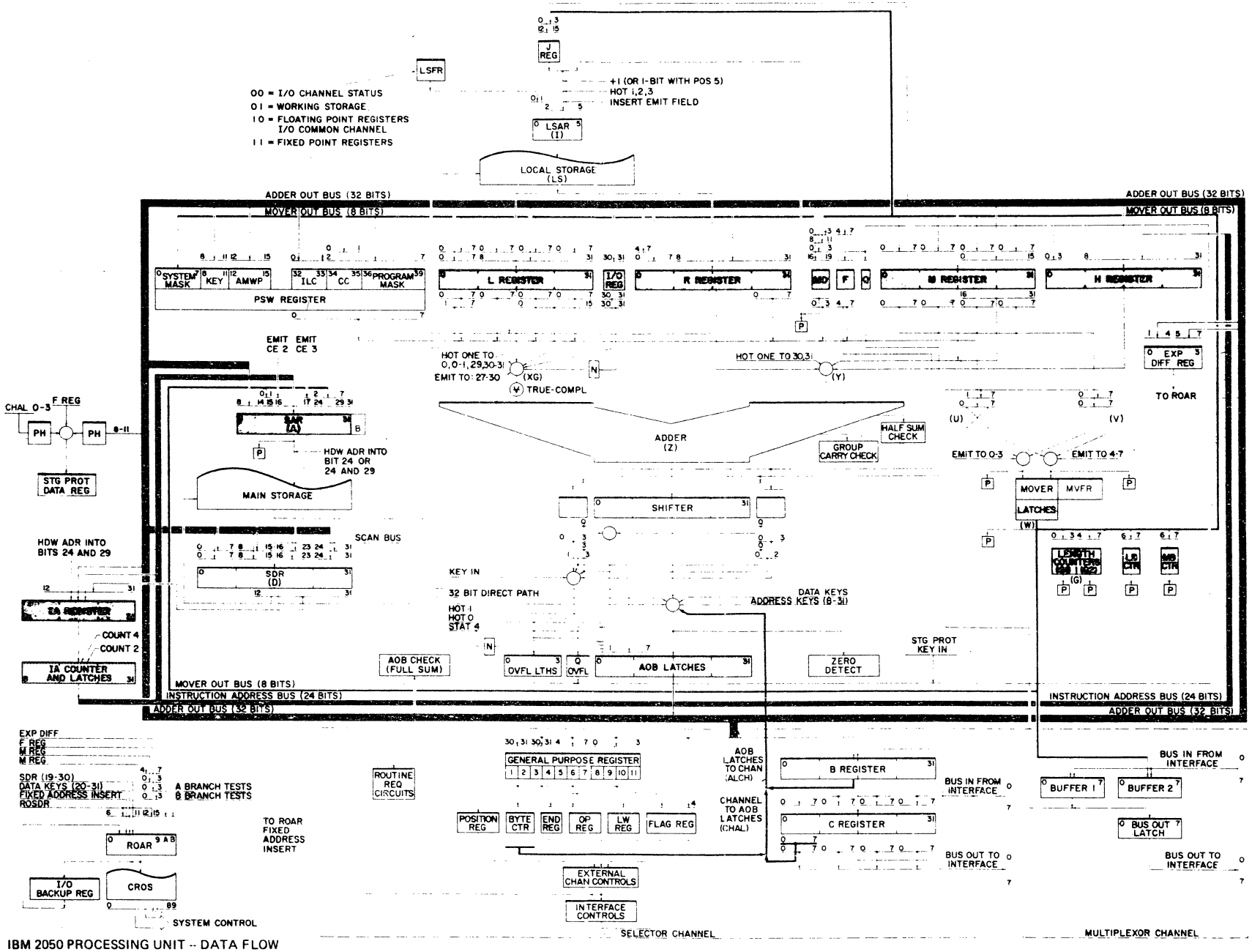
This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B96, PO Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for reader's comments. If the form has been removed, comments may be sent to the above address.

CONTENTS

ILLUSTRATIONS

ABBREVIATIONS

Adr	Address
ALCH	Adder Latches to Channel
ALD	Automated Logic Diagram
Blk	Block
BT	Binary Tgr
CC	Command Chain
CFC	Control Field Chart
Ch	Channel
CHAL	Channel to Adder Latches
Chk	Check
CLF	Condensed Logic Flowchart
Clk	Clock
Cnt	Count
Com	Common
Ctr	Counter
Ctrl	Control
Cyl	Cylinder
DTC	Data Transfer and Control
ECAD	Error Check Analysis Diagram
FLT	Fault Locating Test
G/F	Good/Fail
GP	General Purpose (Stats 0-7)
Gr	Group
Gt	Gate
HA	Hardware Address
Hdw	Hardware
IAR	Instruction Address Register
IF	Interface Register
IIC	Inhibit IAR Count
ILI	Incorrect Length Indication
Inh	Inhibit
Insn	Instruction
I/O	Input/Output
IPL	Initial Program Load
Irpt	Interrupt
LCS	Large Capacity Storage
LCW	Linkage Control Word
Loc	Location
LS	Local Storage
MC	Maintenance Console
Mpx	Multiplexor
MS	Main Storage
Op	Operation
P	Parity
PB	Pushbutton
PCI	Program Controlled Interrupt
P/F	Pass/Fail
PL	Program Load
Pri	Priority
PSS	Progressive Scan Stat
PSW	Program Status Word
Rd	Read
Reg	Register
Req	Request
ROAR	Read Only Storage Address Register
ROS	Read Only Storage
ROSDR	Read Only Storage Data Register
Rst	Reset
Rtne	Routine
R/W	Read/Write
S	Stat
SAR	Storage Address Register
SCR	Silicon-Controlled Rectifier
SDR	Storage Data Register
Seg	Segment
Sel	Selector
Seq	Sequence
SESS	Supervisory Enable Storage Stat
SILI	Suppress Incorrect Length Indication
SIM	Simulated Check
SP	Storage Protect
SS	Supervisory Stat
Sto	Storage
Sw	Switch
TD	Time Delay
Term	Termination
Tgr	Trigger
TIM	Timing Chart
UA	Unit Address
UCW	Unit Control Word
Wr	Write



IBM 2050 PROCESSING UNIT -- DATA FLOW

Safety cannot be overemphasized. To insure personal safety and the safety of co-workers, each CE should make it an everyday practice to observe safety precautions at all times. All CE's should be familiar with the general safety practices and procedures for performing artificial respiration that are outlined in CE Safety Procedures, S229-1264. For convenience, this form is duplicated below.

Always use a reliable voltmeter to verify that power is actually off after using power off switches. Although all power supplies are provided with bleeder resistors to drain off capacitor charges when power is dropped, it is wise to check all capacitors with a meter before attempting maintenance. A defective bleeder resistor could create an unexpected hazard.

CAUTION

Before changing SLT cards in main storage, storage protect, and local storage, drop power to the unit. Dropping power is the only sure way to prevent card damage from voltage surges during card replacement.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE YOUR EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles — this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS

S229-1264-1

12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

Thumb and finger positions

MAINTENANCE PHILOSOPHY

The system provides facilities that assist the CE in:

- Failure Detection
- Fault Location
- Deferred Maintenance
- Rapid Repair

Failure Detection

Error detection is accomplished by hardware parity checking, fault locating tests (FLT's), and functional diagnostic programs. Not all failures can be detected however.

Failure Detection By Hardware

The central processing unit (CPU) is parity checked. All data transfers between registers and main storage are checked by byte. Good parity is always written into main storage by design (except FLT's).

Parity checking is also used on the read-only storage (ROS) at the output.

Any multiplexor and selector channel circuitry not used by the CPU has its own parity checking circuitry.

Each error check is individually indicated on the CE-operator's console. To provide a high diagnostic resolution, the individual checks are OR'ed in groups by timing and function and are also indicated on the console.

Fault Locating Tests (FLT's)

FLT's are semi-automatic diagnostic procedures used in the Model 50 CPU. The procedure involves a battery of diagnostic tests, each performed by forcing the CPU to a predetermined state (scan-in), running the CPU for a specified number of machine cycles (clock advance), logging the resulting state into storage (scan-out), and then comparing the resulting state of the selected machine area under test (compare) with a pre-computed result.

Functional Diagnostics

The functional diagnostic programs are the highest level of testing a system. They are system programs that check for correct system operation. Functional diagnostics have been written for all areas of the Model 50.

Deferred Maintenance

The logout facility allows maintenance activity to be deferred. Certain intermittent failures will be such that long time periods elapse between interruptions. Troubleshooting this type of fault is time-consuming. The failure environment is difficult to reproduce. The customer will often prefer to continue system operation and postpone maintenance activity under these circumstances. The logout feature allows the customer to continue system operation while providing the CE with information on the system state at the time of the error.

TROUBLESHOOTING FLOWCHART

Flowcharts for troubleshooting the 2050 Processing Unit are now in the Maintenance Diagrams Manual for the 2050.

Figure 1 shows the status of indicators after system reset.

Roller		Indicators
Common Chan	2	SBCR unpredictable
Common Chan	3	BUFFER 1 and BUFFER 3 reset BUFFER 2 set to previous contents of BUFFER 1
Mpx Chan	4	BUFFER 1 and BUFFER 2 unpredictable
Mpx Chan	5	BUS OUT unpredictable
Mpx Chan	6	POLL on, MPX I/O STATS unpredictable
Selector Chan	1	B-REGISTER P-bits on
Selector Chan	2	C-REGISTER P-bits on
Selector Chan	3	BYTE COUNTER P-bits on
Selector Chan	4	CYCLE COUNTER stepping
Selector Chan	5	POS REG TRF, SP-D2, and INSN SCAN on; A-CLOCK stepping
Selector Chan	6	FIN on
CPU 1	1	L-REGISTER = PSW Backup
CPU 1	2	R-REGISTER P-bits on
CPU 1	3	M-REGISTER P-bits on
CPU 1	4	H-REGISTER P-bits on
CPU 1	5	SAR bit 17 on, BYTE STATS unchanged, BYTE STORE STATS set to 1
CPU 1	6	ROSDR = Halt Loop
CPU 2	1	ROSDR = Halt Loop
CPU 2	2	ROSDR = Halt Loop, MOVER FUNCTION unpredictable
CPU 2	3	ONE SYL OP on, REFETCH unpredictable. NEXT ROS ADDRESS = Halt Loop, ILC unpredictable
CPU 2	4	I/O REGISTER P-bit, L BYTE CNTR, and M BYTE CNTR on; F-REG, EDIT STATS, and CARRY unchanged
CPU 2	5	LSAR = Hex 17, LSFN = 1, J-REG = 7, MD = 3, G1 and G2 have S- and P-bits on
CPU 2	7	CURRENT ROS ADDRESS = Halt Loop
CPU 2	8	PREVIOUS ROS ADDRESS = Halt Loop

Most other indicators are off, but for definite status refer to machine logic.

FIGURE 1. STATUS OF INDICATORS AFTER SYSTEM RESET

Power Faults

See the section, Power System Service Checks, in this manual.

Loading Faults

See the section on FLTs in this manual. Remember that none of the central processing unit and very little of the channel circuitry is used to load FLTs.

Programming Faults and Error Stops

Programming faults and error stop approaches to troubleshooting are shown. Note that:

1. The machine status is logged out before beginning a troubleshooting sequence.
2. FLT's are run before functional tests.

OTHER MAINTENANCE DOCUMENTATION

Error Check Analysis Diagrams

Error check analysis diagrams (ECAD's) are computer-drawn, engineering controlled, schematic representations of the error register and the circuitry behind each possible error indication.

ECAD's are in Volume 1 Reference of Systems Diagrams. To use ECAD's, turn to page UCA101 and find your particular error in the error register block diagram. The numbers to the left of the error register lead you to an ECAD specifically tailored for that error. Further to the left is the ALD page number of the parity checker for that error.

Each ECAD contains a block diagram simplified to show the basic logic of the error checking circuit and a list of ROS functions that pertain to the circuit. In addition, basic timings, scope points, pertinent notes, and the complete logic for at least one bit position of the error circuit are shown wherever necessary.

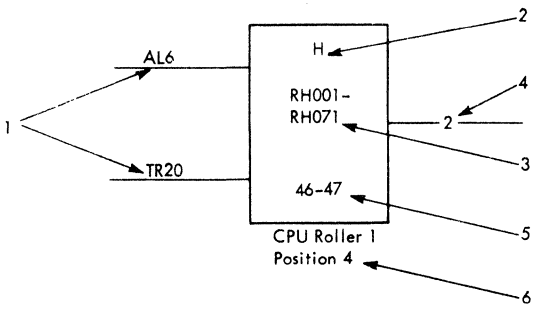
Figure 2 shows how to read an ECAD block.

SERVICE AIDS

This section is for Customer Engineering Memorandums (CEM's) and other aids helpful in servicing the Model 50. CEM's are generated and distributed by Field Engineering Technical Operations as the need for them arises.

ALD Page Key

Figure 3 is a key to the Model 50 ALD pages showing the basic content of each section of the ALD's.



1. ROS Functions: Specifies the gating into the register. Enough of the control field specifications are reproduced to permit interpretation of the function. In this example, AL6 would be shown as IAR H(8-31), and TR 20 would be shown as Latch H(0-31). Thus the two sources of input to the H register are the latch and IAR. By examining the ROS word in control during the error cycle, the source of the data in the H register can be pinpointed.

2. Name of Register: Self explanatory.

3. ALD Pages: Self explanatory.

4. Scoping Point: Refers to an entry in a testpoint table, from which scoping information can be obtained.

5. Logout Location: Refers to the storage word(s) into which the register is logged on an error log out. This is a decimal word address.

6. Indication: Specifies where in the switchable indicators the register is displayed.

FIGURE 2. ECAD BLOCK KEY

AM---	Half Adder
AN---	Adder Carry and Mover Parity
AP---	Adder Parity
AQ---	Sum Checking and Correction
AV---	Right Mover Position and Carry
AW---	Generation
BA---	SDR
BB---	A Lth to Chan
BC---	Chan to A Lth
BH---	Scan Out
BU---	Outgates to Left Mover
BV---	Outgates to Right Mover
BW---	Mpx to Mover, Mover to Chan
BX---	Outgates to Left Adder
BY---	Outgates to Right Adder
CA---	Instruction Register
CD---	M/D, Byte Counter
CG---	Length Counter
CL---	L Byte Counter
CM---	M Byte Counter
DR---	ROSDR
DS---	Mover Counter Controls
ED---	C-13
EE---	C-13
EF---	Multiplexor Chan
FA---	Multiplexor Chan
GA---	Extemal Chan Controls
GG---	Extemal Chan Controls
GH---	Extemal Data Flow
GQ---	Interface Controls
GV---	Interface Controls
JC---	Direct Data
JV---	Direct Data
KC---	Clocking
KE---	Common Channel
KE---	I/O Adder Lth Tests
KH---	Scan
KK---	ROS Address Controls
KL---	LSAR Controls
KP---	Mover Controls
KQ---	Mover Functions
KS---	Stat Setting Controls
KT---	Scan
KU---	I/O Computer Mode
LS---	Local Store
MA---	M-9 32K BOM
MB---	M-9 32K BOM
MC---	Main Storage Tailgate Logic
PA---	Console Controls
PS---	Console Controls
PG---	1052 Adapter
QA---	CAS I
QK---	CAS II
QT---	CAS III
RA---	SAR
RE---	Exponent Reg
RF---	F Reg
RH---	H Reg
RJ---	J Reg
RK---	ROSDR Bits
RL---	L Reg
RM---	M Reg
RP---	Protect Register
RR---	R Reg
RZ---	Direct Data Out
XA---	Hi Speed Adaptor, Shared Storage, LCS
XX---	Chan to Chan
ZH---	Maint Aids

FIGURE 3. ALD PAGE KEY

CAS Logic Diagram Page Key

Figure 4 is a key to the Model 50 CAS logic diagram pages.

Optional Feature Version Codes

The following version codes are used for optional features on the Model 50:

Version	B/M	Description
003	5366797	LCS (2361 Attachment)
004	5378078	Extended ROS
005	5364640	1410/7010 Emulator
006	5364641	7070/7074 Emulator
007	5363895	512K Storage (Mod I)
008	5365430	FLT Disk Load
050	5378451	High-resolution Timer (60 hz)
051	5378076	Fetch Protect
052	5378472	Monitor IF
053	5378528	Mpx Ch IF Extension
054	5378617	High-resolution Timer (300 hz)
101	5365230	50 hz Power Supply
102	5363828	Direct Control
105		CAS for Version 005
106		CAS for Version 006
110		CAS for Version 004
A03	5378000	Versions 007 and 050 combined
A04	5378527	Versions 003 and 004 combined
A05	5378667	Versions 050 and 051 combined
A06	5378455	Versions 003, 004, 050, and 052
C05		CAS for Version A05

Diagnostic Mode Codes

The following are diagnostic mode codes on machine histories:

Code Number	Item
1	9-track tape
2	7-track tape
3	Cards
4	1,600 bpi
5	Disc
6	Paper tape
7	Phase encoding
P	Scopex listing (bond paper)
M	Scopex listing (microfiche)

Add Subtract RR + RX A AR S SR	QB730
Branch and Link RR + RX	QA500
Branch on Condition BC + BCR	QA700
Branch On Count BCT + BCTR	QA700
Branch On Index BXH BXLE	QJ600
Branch Entry to I-Fetch	QT120
Bring Up Aids	QW111
Bring Up Aids Two Words of One Bits	QW222
Bump Store Kernel	QY140
CCW1 Routine Selector Channel	QV102
CCW2 Routine Selector Channel	QV103
Common Mask Trap Sense	QB730
Compares - Algebraic Logical RR + RX CR C CLR CL	QB500
Compare Decimal CP Comparison of 1st Wd Opnd 1 DL	QS200
Compare Decimal CP Comparison of 1st Wd Opnd 1	QS202
Compare Logical SS	QP100
Compare Routine Selector Channel	QV111
Command Chain Unit Address Compare D2-Mpx	QV330
Convert to Binary CVB from Decimal	QE900
Convert to Decimal from Binary CVD	QS112
Decimal Add AP Subtract SP First Work Assembly	QS110
Decimal Add AP Aubtract SP Add Subtract Inner Loop	QS114
Decimal Add AP Subtract SP G2 Counter Less than Four	QS116
Decimal Add AP Subtract SP G1 Counter Latch Zero Check Overflow	QS118
Decimal Add AP Subtract SP Recomplement and End Routine	QS120
Decimal Arithmetic Second Level I-Fetch	QS010
Diagnose Instruction	QY110
Direct Data Wrd RDD	QJ400
Divide Decimal Op Dividend Assembly	QS300
Divide Decimal - Loop for Single Word DVR Sign Insertion	QS302
Divide Decimal - Loop for Double Word Divisor	QS304
Divide Decimal Quotient Store Dividend Fetch	QS306
Divide Decimal Remainder Assembly	QS308
Edit Edit and Mark ED EDMK Initial Left Digit S Off	QP200
Edit Edit and Mark ED EDMK Left Source Digit S On	QP202
Edit Edit and Mark ED EDMK Right Source Digit S Off	QP203
Edit Edit and Mark ED EDMK Right Source Digit S On	QP204
Edit Edit and Mark ED EDMK Store Fetch Pattern Source	QP205
Edit Edit and Mark ED EDMK Set Condition Reg and General Reg 1	QP206
End Update Routine Selector Channel	QV106
Execute Instruction	QE400
Fixed Point Multiply Half Word RR and RX Format	QB800
Fixed Point RR Loads LPR LNR LTR LCR LR	QB100
Fixed Point Multiply Post Loop Routine	QB801
Fixed Point Divide DR + D Divide Loop	QB901
Fixed Point Divide DR +,D Post Loop Complementing	QB902
Fixed Point TX Load Store	QF100
Floating Point Halve RR Long and Short	QG200
Floating Point Load/Store RR/RX Format Long/Short	QG300
Floating Point Operations Second Level Decode	QG310
Floating Point Add Subtract Compare RR RX Format Long Short	QG400
Floating Point Add Subtract Compare Determine the Exponent Difference	QG401
Floating Point Add Subtract Compare Calculate the Exponent Diff - RR Long	QG402
Floating Point Add Subtract Compare Pre-Shift 0 through 5	QG403
Floating Point Add Subtract Compare Pre-Shift 6 through 8	QG404
Floating Point Add Subtract Compare Pre-Shift 9 through 16	QG405
Floating Point Add Subtract Compare Short Add Normal Complement of FR	QG406
Floating Point Add Subtract Zero Test Check Mask	QG409
Floating Point Add Subtract Compare Recomplement Guard Digit	QG416
Floating Point Divide Short RR RS Pre-Normalize	QG500
Floating Point DVD N DER NDE Exponent Subtraction	QG501
Floating Point DVD N DER NDE Divide Loop for FR	QG502
Floating Point DVD N DER Post-Normalize	QG503
Floating Point Multiply RR RX Format Long Short	QG700
Floating Point Multiply Mply Loop	QG701
Floating Point Multiply Post-Normalize Zero Test	QG702
FLT Compare and Branch	QY510
FLT Load Call Kernel	QY140
FP Long Multiply Divide MDR MD DDR DD - Prenorm	QG800
FP Long Multiply Divide MIER DVD Prenorm Exp Arith	QG801
FP Long Multiply MDR MD MCD Multiplies Mult Loop	QG802
FP Long Multiply MDR MD Multiply Loop	QG803
FP Long Multiply MDR MD End Routine - Post-Normalize	QG804
FP	QG900
Free Entry CY2	QT100
Half-Word Store STH	QE555
Half-Word Ops - Common Setup LH CH AH SH MH	QE580
Halt Loop and EXC Sensing	QT200
Instruction Fetch First Cycle	QT100
Instruction Fetch Second Page	QT110
Interrupt Routine Selector Channel	QV107
Invalid Ops	QM111
Invalid Op Groups	QN111
Invert SAR Kernel	QY140
I/O Op Countdown Loop and Responses	QK701
IPL	QK800
IPL Status Analysis	QK801

Long and Short Floating Point Loads that Refer to Sign	QG100
Long Floating Point Add of Fraction with Tests for Complement Normal	QG407
Long Floating Point Add Subt Compare Cmpl Normalizing Zero Test	QG408
Load PSW LPSW Set System Mask SSM	QJ200
Load Store Multiple LM STM	QK666
Load 64 - CPU Mode	QK705
Local Store Diagnostics	QY130
Local Store Write Routine Selector Channel	QV108
Local Store Read Routine Selector Channel	QV109
Logical Add Subtract RR RX AL SL ALR SLR	QB750
Logical and Move Instructions SS Adr Tests Initialization	QP800
Logical and Move Instruction SS Main Loop	QP810
Logical and Move Instruction SS Overlap Routine	QP820
Logical and Move Instruction SS End Routine	QP830
Log Out Scan Out	QY410
Mpx Chan Interrupt Handling	QK703
Mpx Chan Count Equals Zero Analysis	QV270
Mpx Chan Count and Fetch and Update	QV210
Mpx Chan Data Address Fetch and Update	QV220
Mpx Chan Data Handling Input	QV231
Mpx Chan Data Handling Output	QV230
Mpx Chan Data Handling Read Backward	QV243
Mpx Chan Data Handling Read Forward	QV241
Mpx Chan Data Handling Stop or Skip	QV242
Mpx Chan End Status Analysis	QV250
Mpx Chan Command Chain End Status Analysis	QV350
Mpx Chan Interrupt Preparation	QV820
Mpx Chan Sequence Control Fetch	QV410
Mpx Chan Start I/O Unit Select	QV420
Mpx Chan Start I/O Unit Address Compare	QV430
Mpx Chan Start I/O Status Analysis	QV440
Mpx Chan Count Store	QV460
Mpx Chan Data Store	QV470
Mpx Chan Check Handling	QV840
Mpx Chan PCI	QV260
Mpx Chan Test I/O Unit Select	QV520
Mpx Chan Test I/O Unit Address Compare	QV540
Mpx Chan Test I/O Accept Status	QV550
Mpx Chan Control Check Handling	QV850
Mpx Chan Control Unit Busy	QV810
MPX Chan Halt I/O Unit Select	QV620
Mpx Chan Test I/O Unit Select	QV530
Mpx Chan Count Address Fetch - Store	QV360
Mpx Chan Control Word I Fetch	QV310
Mpx Chan Command Chain Initial Status Analysis	QV340
Mpx Chan Fetch Second Half of Chan Control Word	QV320
Mpx Chan Control Word 2 Fetch	QV321
Mpx Chan Load 64 Prep	QV830
Mpx Chan Data Chaining	QV370
Multiply Decimal MP Final Product Assembly	QS406
Multiply Decimal - Single and Double Word Mpy Loops Product Store	QS404
Multiply Divide Decimal MP DP Opnd 2 Assembly MPCN/DVR	QS400
Multiply Divide Decimal MPCN Dbling Set Quotient Sign Sel Mplr Digit	QS402
Pack Move with Offset	QS500
Read Store Routine Selector Channel	QV105
Reset Error Register Kernel	QY140
Restore CPU Mode Sel Mpx Chan	QV112
ROS Forced Addressed for Prog Traps - Address Data Spec Prot	QT300
RR + RX Fixed Point Second Level I-Fetch	QA111
RR + RX AND OR Exclusive OR	QB400
RS + SI Second Level I-Fetch 8 + 9	QJ011
RX Control - Load Address Insert Store Character	QE100
Scan-In I/O Interrupt	QY310
Second Level I-Fetch for VFL Character Ops	QP010
Shift Left Logical SLL	QJ090
Shift Right Logical SRL	QJ080
Shift Left Algebraic SLA	QJ110
Shift Right Algebraic SRA	QJ100
Shift Left Double Logical SLDL	QJ130
Shift Right Double Logical SRDL	QJ120
Shift Left Double Algebraic SLDA	QJ150
Shift Right Double Algebraic SRDA	QJ140
SI Compare CLI Test under Mask TUM	QK555
SI Move and Logical Ops MVI NI OI XI	QK222
Start I/O, Halt I/O, Test I/O, Test Chan, Proc with Interrupt	QK700
Start I/O Routine Selector Channel	QV100
Store Display	QT220
Storage Protect Instructions STG + ITG Store Tag + Insert Tag	QA800
SVC and SAM - RR Control Ops	QA400
System Reset IPL PSW Restart	QU100
Time Out Check Loop IB Test On Start I/O	QK702
Timer Update and External Interrupt	QT210
Translate Translate and Test TR TRT	QP900
Trap Sequence - Store PSW	QT310
Trans In Chan Routine Selector Channel	QV101
Unpack Non-overlapped Fields	QS600
Unpack - Op 1 Storage Op 2 Fetch Zero Insertion	QS601
Unpack Overlapped Fields	QS602
Unit Address Fetch Routine Selector Channel	QV110
Write Fetch Routine Selector Channel	QV104
Zero and Add	QS700

FIGURE 4. CAS LOGIC DIAGRAM PAGE KEY

SELECTOR CHANNEL ERROR HANDLING

Interface Control Check

The following conditions can cause an interface control check:

1. Parity check on 'bus in' during 'address-in' or 'status-in' tag.
2. Address compare not equal during unit selection.
3. 'Operational in' falling while 'select out' is still active.
4. 'Select in' received by the channel in response to 'address out' during a command chain unit selection or a hardware test I/O selection on a device-end interrupt.
5. More than one in tag active while 'operational in' is active.
6. In response to 'address out', during initial selection on a start I/O or test I/O instruction, if the channel has not received 'operational in', 'select in', or 'status in', and the CPU countdown loop has timed out. The time-out indicator in the common channel will turn off before the system is stopped or logged.
7. In response to the halt disconnect sequence during a halt I/O instruction, if 'operational in' has not fallen and the CPU countdown loop has timed out. The time-out indicator in the common channel will turn off before the system is stopped or logged.

Mode Switch Settings

Stop Mode: Results in a master check and a log request (CPU roller 2, position 6).

Channel Stop Mode: Results in a master check and a log request (CPU roller 2, position 6). All channel-out tag responses to an in tag from a control unit are delayed to allow time to stop the channel response on the interface. This prevents the in tag from dropping, thereby freezing the error condition on the interface to facilitate error analysis.

Process Mode: Results in a logout of only the selector channel in error (when the channel is not masked) and in an I/O interrupt. If the error occurred during an initial selection, logout takes place and a channel status word (CSW) is stored.

Disable Mode: Results in a selective reset of the interface and I/O interrupt when the channel is not masked.

Channel Control Check--Channel Detected

The following conditions can cause a channel-detected channel control check:

1. Interface parity check on data going to bus out lines during address out and command out.
2. Byte counter parity check.
3. Log word 4 error.
4. Zero test portion of log word 5 test in the end update routine.

Mode Switch Settings

Results are the same as for interface control check mode switch settings.

Channel Control Check--CPU Detected

The following conditions can cause a CPU-detected channel control check:

1. Time-out check.
2. First-cycle check.
3. ROS parity check.
4. Full-sum check.
5. Mover output or input check.
6. Half-sum check.
7. Storage-protect parity check.
8. Parity test portion of the log word 5 test in the end update routine.

Mode Switch Settings

Stop or Channel Stop Mode: Results in a log request, the CPU error displayed on the check register, and a master check. The channel control check is set and displayed in the channel, and the channel indicators remain unchanged.

Process Mode: Results in a logout of the CPU and the channel in error when PSW bit 13 is on. This is followed by a machine check interrupt.

Disable Mode: Results in the error being set into the check register, but the channel control check is not sent to the channel.

Program, Storage-Protect, and Chaining Check

The following conditions will cause a program check:

1. Invalid command in the channel command word (CCW) (positions 4-7 are zero).
2. Invalid flags in the CCW (positions 5-7 of the flag byte are not zero.

3. Count specified in the CCW is zero.

4. Data address specified by the CCW exceeds the storage size.

5. Command address specified by the CCW exceeds the storage size.

6. CCW sequence in which the first CCW specified by the command address word is a transfer in channel.

7. CCW sequence in which two successive CCW's specify transfer in channel.

8. Command address specified in the CCW is not on a doubleword boundary.

9. Command address word in which positions 4-7 are not zero.

The following condition will cause a protection check:

1. The storage-protect tag specified in the command address word does not agree with the key of the addressed area of storage during a data store.

The following conditions will cause a chaining check:

1. The channel accepts more than one byte of read data assembling on word boundaries when the CCW specifies byte boundaries on data chaining. This is detected in the CCW 1 routine.

2. The channel accepts more bytes than CCW specifies while data chaining. This is detected in the CCW 2 routine.

Note: Both of the foregoing conditions are caused by attempting to read data chain with a control unit whose data rate is faster than the maximum specified in the Field Engineering Theory of Operation Manual, Model 50 Functional Units, SY22-2822.

Mode Switch Settings

Stop Mode: The system is not stopped and a master check does not occur. If the system is not masked, an I/O interrupt occurs. If error occurred during an initiation of a new I/O instruction, logout takes place and a CSW is stored.

Channel Stop Mode: The system is stopped by a log request in the check register and a master check. The channel indicators remain unchanged.

Process or Disable Mode: Same as for stop mode.

Data Check

The following conditions will cause a data check:

1. A parity check on 'bus in' while reading data into the channel. The parity is corrected before the data is set into the C-register.

2. A parity check is detected on write data going to 'bus out'. The parity is not corrected.

Mode Switch Settings

Process or Disable Mode: Channel proceeds to end of record; when channel is not masked an I/O interrupt occurs.

Stop or Channel Stop Mode: The channel stops. A master check and log request (CPU roller 2, position 6) are displayed.

SIM Check

This check indicator informs the channel to terminate an operation. It indicates that control unit status is not available for the CSW. SIM check occurs only inside the channel and never appears in the CSW.

The following conditions set SIM check:

1. Channel detects an error before the control unit can be selected to perform an operation.

2. A halt I/O instruction terminates the current operation.

3. An interface selective reset caused by an interface control check occurring in disable mode.

Incorrect Length Indication (ILI)

This indication appears in the CSW and will suppress command chaining unless the suppress incorrect length indication (SILI) flag is present in the current CSW. If the current CCW has a data chain and a SILI flag, the indication is not suppressed and will appear in the CSW.

The indication cannot occur on a command immediate. When the channel prefetches an invalid CCW (storage-protect or program check) on a write data chain operation and the control unit sends status in before the count in the current CCW is exhausted. the ILI indication will suppress the storage-protect or program check condition. This is also true if the channel prefetches data with an invalid data address. The ILI indication cannot appear in the CSW as a result of a program controlled interrupt (PCI) flag. ILI is turned on by the following conditions:

1. A control unit sends service in one or more times after the count in the CCW has been exhausted. On a read operation the extra bytes are not placed in main storage. An extra service in almost always occurs on a write or control operation, the only exception being on a formatted type device with a fixed record length. The residual count in the CSW is zero.

2. Service in is sent by a control unit less times than specified by the CCW. The residual count in the CSW is not zero.

Error Priority

Error priority is as follows (highest priority is 1):

1. Channel control check.
2. Interface control check.
3. Storage-protect or program check.
4. Chain check.
5. Incorrect length indication (ILI).
6. Data check.

If any of these errors occur simultaneously, the higher priority error will reset the lower priority error. There is one exception to this rule. On a write operation when the channel prefetches either an invalid CCW on data chaining or data with an invalid data address (storage-protect or program check), an incorrect length indication will reset the storage-protect or program check.

Data-check error is blocked from setting if a higher priority error occurs at the same time but is not reset if it is already on.

MAINTENANCE FEATURES

Two basic types of operation in the Model 50 are maintenance operations and normal operations. This section concerns itself with maintenance operations only. Figure 5 is a listing of various controls, latches, and triggers used in maintenance operations. These operations are used to:

1. Execute special kernels (maintenance routines) in ROS, entering these kernels via the diagnose instruction and using linkage control words (LCW's) set up by the individual currently using the kernels.
2. Initiate and run predetermined CPU tests (FLT's) that locate errors and the components causing those errors.
3. Initiate and run predetermined channel tests (Progressive Scan) under control of the diagnose instruction.
4. Document the status of registers, counters, and stats, etc. (logout or scan-out).
5. Execute the ROS ripple test program, or run a MS ripple test from the storage test panel on the console.

All other operations will be considered as normal System/360 operations.

CPU CONTROL MODES

Maintenance operations make use of three different CPU control modes: sequence counter, main store, and ROS. Figure 6 describes the two basic types of Model 50 operation and their possible CPU control modes. Figure 7 lists the entries, objectives, and controls for the three CPU control modes used in maintenance operations.

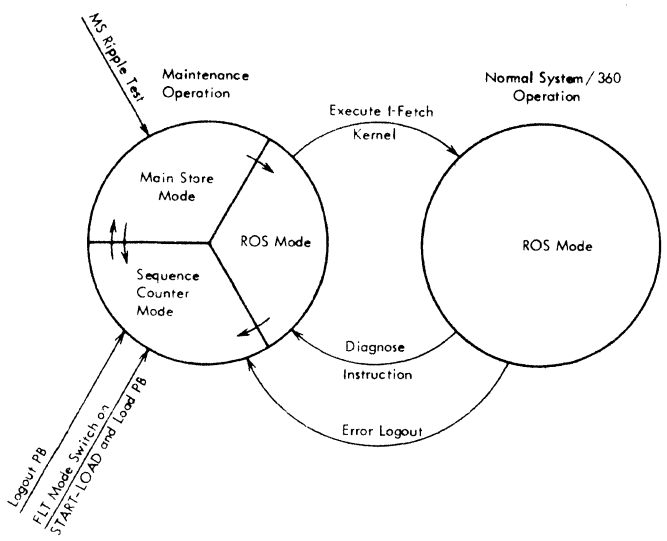
Sequence Counter Mode

When the sequence counter mode trigger (KT151) is on, the system is under control of the sequence counter and the sequence stats. This mode is used

	ALD Page
Backspace Tgr	KH555
Binary Tgr	KH211
Command Chain (CC) Tgr	GC161
CCW1, CCW2, Read Store, or Write Fetch Request Tgr	KH511
Channel Log Controls	KE661
Clock Stop Tgrs	KT211
CPU Control Modes	KT151-161
Cylinder Counter	KH553-554
DTC Tgr	KH531
End Update or Start I/O Reg Tgr	KH511
Error Interrupt Tgr	KT071
Error Pending Tgr	KT081
Error Reg	KT011-031
Fail Tgr	KH321
First/Second Word Tgr	KH541
FLT Load Controls	KH511-541
FLT Load Request Tgr	KT301
FLT Op Reg	KH111
FLT Op Reg Instructions	KH121-151
FLT Program Load Tgr	KT111
FLT Retry Tgr	KH555
GP Stats (0-7)	KS101-171
Hard Stop Tgr	KT161
Hardware Address to ROAR	KH321
Ignore Error I/O Tgr	KT161
Inhibit IAR Count Tgr	KH511
Inhibit IAR Count Control Tgr	KH511
Interrupt Request Tgr	KH521
I/O Mode Stat	KC531
IPL Accept Tgr	KH521
Log Decoder	KH371
Log Request Tgr	KT101
Log Tgr	KT151
Main Store Mode	KT151

	ALD Page
Maintenance Console Controls/Indicators/Etc.	PK001-PS121
Manual Controls	KE781
Manual Tgr	KS721
Normal Interrupt Tgr	KT111
Op to ALCH Tgr	KH511
Pass Tgr	KH321
Progressive Scan Control	KE701
Progressive Scan Stat	KH321
Read Store, CCW1, CCW2, or Write Fetch Request Tgr	KH511
Reset/Restart Controls	KK701
Retry Tgr	KH555
ROAR Backup Regs (Current and Previous)	KK312-313
ROS Mode	KT151
Scan IPL Tgr	KH521
Scan/Log Decoder	KH121-151
Scan Test Counter	KH311
SDR to ROAR Logic	KK081
Seek Control Tgr	KH555
Seek Tgr	KH555
Sequence Counter	KH341
Sequence Counter Mode	KT151
Sequence Stats	KH345
Suppress Incorrect Length Indication (SILI) Tgr	GC161
Start I/O to I/O Tgr	KH511
Stop Request Tgr	KT101
Stop Tgr	KS721
Storage Holdoff Clock Stop Tgr	KT215
Storage Holdoff Controls	KC511-531
Storage Ripple Logic	KT501-531
Storage Test Controls	PK071
Supervisory Enable Storage Stat	KH331
Supervisory Stat	KH321
System Reset Tgr	KT311
Timed Single Cycle Mode Tgr	KT271
Unit Address to ALCH Tgr	KH511
Write Fetch, CCW1, CCW2, or Read Store Request Tgr	KH511

FIGURE 5. CONTROLS, LATCHES, ETC. USED IN MAINTENANCE OPERATIONS



Maintenance Operation	Normal System/360 Operation
Sequence Counter Mode	
1. FLT Load 2. Logout: a. Error b. Logout Pushbutton	
Main Store Mode	
1. Main Store Mode FLT's 2. Logout 3. Main Store Ripple Test	
ROS Mode	
1. ROS Kernels (Maintenance Routines): a. ROS Mode FLT's b. All Logouts or Scan-Outs c. Execution of Diagnose Instruction 2. Diagnostics	1. All System/360 Instructions 2. I-Fetch of Diagnose Instruction

FIGURE 6. BASIC OPERATIONS AND CPU CONTROL MODES

	Entered via:	Objectives	Control or Instruction Source
Sequence Counter Mode	1. FLT mode sw on "Start-Load" and Load PB 2. Call for FLT load: a. MS mode -- op code A b. ROS mode -- scan*E, 00 and Emit 1010 3. Logout PB 4. Initiation of error log	1 or 2. Read FLT mode tapes or disks into storage: "OR's" each pair (odd/even) of consecutive words on tape or disk including parity bit generation, into each storage location used. 3 or 4. Logout into storage: a. SDR to location 80 b. SAR and byte stats to location 84 c. IAR to location 88	Controlled directly by sequence stats and sequence counter.
	Entered via:	**Objectives**	**Control or Instruction Source**
Main Store Mode	1. Call for MS mode while in Seq Ctr mode: a. During FLT load b. Logout 2. Main store ripple test: Storage test sw off Process, and Start PB. NOTE: The MS ripple test must run correctly before trying FLT's.	1a. MS hardcore tests and ROS bit tests or ROS ripple test. 1b. Logout into storage: (a) ROSDR (groups 1-4). This is one ROS word (0-89) which is sent to storage locations 8C, 90, 94, and 98. (b) ROAR to location 9C. 2. Test main storage via ripple (1's, 0's, worst, and reverse worst)	1. FLT op register: Decodes parity bits of word in SDR. 2. Storage test switch: Setting determines test.
	Entered via:	**Objectives**	**Control or Instruction Source**
ROS Mode	1. Call for ROS mode while in MS mode: a. Performing FLT's b. Logout 2. Start PB, then system reset PB.	1a. ROS hardcore tests and zero and one cycle tests. 1b. Logout into storage: CPU and/or channel status. 2. Progressive scan of channels, Special maintenance routines (kernels) in ROS.	1. FLT Op register: Decodes emit field bits (under microprogram control). 2. Microprogram control and linkage control words (LCW's).

FIGURE 7. CPU CONTROL MODES FOR MAINTENANCE OPERATIONS

for the FLT load operation and for the first portion of a logout operation.

Main Store Mode

When the main store mode trigger (KT151) is on, the system is under control of words read out of main storage. Main store mode operation provides continued main storage read-outs from addresses specified by the instruction address register (IAR). The IAR is usually incremented by four immediately before each address is requested. Data read out of main storage go into the storage data register (SDR).

Main Store Mode Timing

Main store mode timing consists of four half-microsecond periods (W2, R1, R2, W1). In the first period (W2), a new address is gated into SAR from the instruction address register (IAR), and a main storage cycle is initiated. Instructions requiring gating action to be performed, and which were read out in the previous main storage cycle, are also executed at this time.

In the second period (R1), the SDR is reset.

During the third half-microsecond period (R2), main storage completes the read portion of its cycle and a word is read into the SDR.

At the beginning of the fourth half-microsecond period (W1), the four SDR parity bits, which constitute the new microorder, are gated into the FLT op reg. If the decoded operation calls for the gating of the SDR into read only address register (ROAR), this is performed toward the end of the period.

During the next first half-microsecond period (W2), a new ROS cycle is taken if an address has just been gated into ROAR; otherwise this is a dead cycle.

Main Store Mode Instructions and Data Paths

With the CPU in MS mode and the storage test switch in the process position, the four parity-bit positions of SDR are gated into the FLT op register. There are 16 instructions (including no-ops) that may be decoded in the FLT op reg. Figure 8 shows the instructions and data paths available in main store mode.

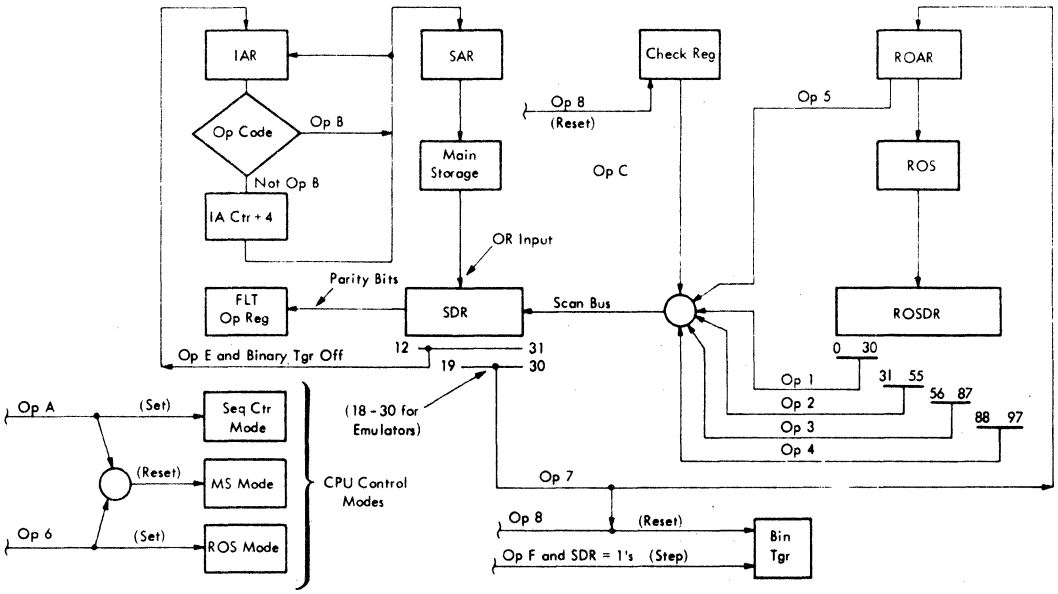
Main Store Mode Ripple

If the storage test switch is not in the process position, the data written into storage are controlled by a set of patterns forced into SDR and selected by means of positions on the storage test switch.

The available patterns are all zeros, ones, worst, and reverse worst. The worst and reverse worst patterns consist of two words of all zeros and then two words of all ones or vice versa. The switching from ones to zeros to ones is controlled by IAR bits 17 and 28 which are exclusive OR'ed.

ROS Mode

When the ROS mode trigger (KT151) is on, the system is under control of read-only storage (ROS). The system is always in ROS mode during normal System/360 operations, and may or may not be in ROS mode during maintenance operations.



NOTE: Op codes 0, 9, and D are no ops.

FIGURE 8. MS MODE INSTRUCTIONS AND DATA PATHS

FUNCTIONAL UNITS

Sequence Counter

The sequence counter, in combination with the sequence stats, controls the operations performed in sequence counter mode (FLT load and logout operations). In MS mode, the sequence counter controls the logout of ROSDR and ROAR. In ROS mode, if the supervisory stat is on, the sequence counter determines how many ROS words (microinstructions) are executed under control of the current linkage control word.

The counter equals all zeros when reset off. Microorder E → SCANCTL, in combination with EMIT 1000 (QY110-C5), sets the 2's complement of SDR(0-2) into the sequence counter indicators (4, 2, 1). See Figure 9, Sequence Counter Logic Chart. The sequence counter is stepped (incremented) by the same control line that sets it (clocked sequence counter select -- KH351).

Sequence Stats

The sequence stats, in combination with the sequence counter, control the operations performed in sequence counter mode.

FLT Op Reg

The FLT op reg controls most main store mode operations by decoding the SDR parity bits. It also controls many ROS mode operations after being set by the microorder SCAN * E, 00 (or 10) in combination with the emit field bits. Instructions decoded by the FLT op reg are shown on Figure 10. This register, used with general purpose stats 0-3, forms the scan/log decoder (Figure 11).

Scan/Log Decoder

The scan/log decoder is composed of the FLT op reg and general purpose stats 0-3 (Figure 11). This decoder controls the operations performed during a scan-out or logout. Figure 12 shows the data and storage locations used during a log or scan-out operation. Figure 13 is a log/scan-out logic diagram.

ROS Kernels

ROS kernels are special maintenance routines (consisting of one or many microinstructions in ROS) that are used by FLT's, progressive scan, error logouts, and the diagnose instruction, etc. Figure 14 is a listing of the ROS kernels. Figure 15 is the ROS kernels flowchart.

Scan-In

The scan-in kernel (maintenance routine) takes up to 11 words from storage, putting them into various CPU counters, registers, and stats. These words, in consecutive storage locations, may be started from any desired address. The scan-in kernel is used by FLT's and progressive scan, and may also

Input Value SDR (0,1,2)	First *PH (1's Compl of Input)	Second *PH (Input Value Minus 1)	Seq Ctr Indicators (4,2,1) (2's Compl of Input)	Seq Ctr Bit (Line Names on KH341)	Seq Ctr
2 = 0 1 = 0 0 = 0	On On On	On On On	1 Off 2 Off 4 Off	$\overline{1}$ $\overline{2}$ $\overline{4}$	0
2 = 1 1 = 0 0 = 0	Off On On	Off Off Off	1 On 2 On 4 On	1 2 4	7
2 = 0 1 = 1 0 = 0	On Off On	On Off Off	1 Off 2 On 4 On	$\overline{1}$ 2 4	6
2 = 1 1 = 1 0 = 0	Off Off On	Off On Off	1 On 2 Off 4 On	$\frac{1}{2}$ 4	5
2 = 0 1 = 0 0 = 1	On On Off	On On Off	1 Off 2 Off 4 On	$\overline{1}$ $\overline{2}$ 4	4
2 = 1 1 = 0 0 = 1	Off On Off	Off Off On	1 On 2 On 4 Off	1 $\frac{2}{4}$	3
2 = 0 1 = 1 0 = 1	On Off Off	On Off On	1 Off 2 On 4 Off	$\overline{1}$ $\frac{2}{4}$	2
2 = 1 1 = 1 0 = 1	Off Off Off	Off On On	1 On 2 Off 4 Off	$\frac{1}{2}$ $\frac{4}{4}$	1

FIGURE 9. SEQUENCE COUNTER LOGIC CHART

FLT Op Reg	Hex Op Code	Mode Usage	Operation
000000	00	MS	No op.
000001	01*	MS	ROSDR group 1 (0-30) to SDR and OR with next word from storage.
000010	02*	MS/ROS	ROSDR group 2 (31-55) to SDR and OR with next word from storage.
000011	03*	MS	ROSDR group 3 (56-87) to SDR and OR with next word from storage.
000100	04*	MS	ROSDR group 4 (88-97) to SDR and OR with next word from storage.
000101	05*	MS/ROS	ROAR to SDR (6-17) and OR with next word (mask) from storage.
000110	06	MS	Request for ROS mode.
000111	07	MS	SDR (19-30) to ROAR, reset binary tgr.
001000	08	MS	Reset error reg and binary tgr.
001001	09	MS	No op.
001010	0A	MS/ROS	Call for FLT load.
001011	0B	MS	Inhibit SAR clock (to stop--loops on same word in SDR). To continue operation, press start pushbutton.
001100	0C*	MS/ROS	Error reg to SDR (0-31).
001101	0D	MS/ROS	No op or LCS information to SDR (0-8).
001110	0E	MS	SDR (12-31) to IAR if binary tgr is off (causes branch to specified address +4).
001111	0F	MS	Step binary tgr if SDR is all 1's.
010000	10*	ROS	SAR and byte stats to SDR (0-31).
010001	11*	ROS	L (0-27) plus parity bits to SDR (0-31).
110001	31*	ROS	L (28-31) to SDR (24-27) "L reg fold."
010010	12*	ROS	Selector channel status to SDR (0-31). GP stats (0-3) are used with these codes to further specify what status is used.
010011	13*	ROS	
010100	14*	ROS	Stats, byte counters, etc. to SDR (0-31).
010101	15*	ROS	H (0-27) plus parity bits to SDR (0-31).
110101	35*	ROS	H (28-31) to SDR (24-27) "H reg fold."
010110	16*	ROS	M (0-27) plus parity bits to SDR (0-31).
110110	36*	ROS	M (28-31) to SDR (24-27) "M reg fold."
010111	17*	ROS	R (0-27) plus parity bits to SDR (0-31).
110111	37*	ROS	R (28-31) to SDR (24-27) "R reg fold."
011000	18*	ROS	LSAR, LSFR, counters, etc. to SDR (0-31).
011001	19*	ROS	Mpx channel (group 1) to SDR (0-31).
011010	1A*	ROS	Mpx channel (group 2) to SDR (0-31).
011011	1B*	ROS	Mpx channel (group 3) to SDR (0-31).
011100	1C*	ROS	Common channel (group 1) to SDR (0-31).
011101	1D*	ROS	Common channel (group 2) to SDR (0-31).
011110	1E*	ROS	Common channel (group 3) to SDR (0-31).
011111	1F	ROS	No op.

NOTES: The FLT op reg is a part of the scan/log decoder (Figure 11). More detailed information on the functions of these op codes is shown on Figure 12.
*All these op codes send data to the SDR via the scan bus. See Figure 13.

FIGURE 10. FLT OP REG INSTRUCTIONS

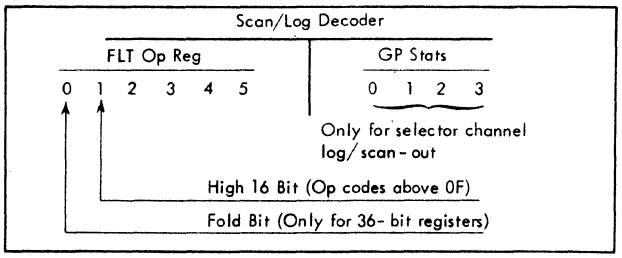


FIGURE 11. SCAN/LOG DECODER

be entered by any program or individual using the diagnose instruction.

Scan-Out

The scan-out kernel (maintenance routine) puts the contents of CPU and channel counters, registers, and stats, etc. into consecutive locations in storage. The scan-out kernel is used by FLT's, logout, and progressive scan, and may also be entered by any program or individual using the diagnose instruction. Storage locations used are predetermined for FLT's and logout. Progressive scan uses the diagnose instruction to enter the scan-out kernel; thus the first storage location used is the fullword address immediately following the diagnose instruction. See Figures 12 and 13.

Microorder HA → A: The HA → A microorder is used to select main storage. This microorder, in combination with the emit field bits, may give an OR select, write select, or a read select. At the same time the storage select is given, a hardware address (hex addresses 80 or 84) is forced to SAR (Figure 16). This microorder is used in the scan-out kernel and the FLT compare and branch kernel. It is also used by the diagnose instruction to store the assembled LCW in hex address 80.

Parity Bit Propagation/Generation: Normally the parity bit positions from tape or in a register are sent to storage along with the data bytes. These parity bits go into storage bit positions 32-35.

During a logout or scan-out, the parity bit positions are sent to storage along with their data bytes, and in addition, correct parity is generated for each byte of information (data and parity bit) sent to storage. Thus a register with 32 data bit positions plus 4 parity bit positions (total 36 positions) uses two storage locations for log or scan-out. See Figure 17 and the Fold Operation text.

One exception to the two preceding statements is during a log or scan-out into storage location 80. Here the entire SDR (data positions 0-31 plus the 4

CPU Mode	Seq Ctr Value	Data Stored**	Storage Locations		
			Full Logout	Channel Only Logout	FLT Scan - Out
Sequence Counter	0	SDR (data and parity)	80		
	4	Storage Address Register	84		
	6	Instruction Address Register	88		
Main Store	0	Read Only Storage Data Register (0 - 30)	8C		
	1	Read Only Storage Data Register (31 - 55)	90		
	2	Read Only Storage Data Register (56 - 87)	94		
	3	Read Only Storage Data Register (88 89)	98		
	4	Read Only Storage Address Register	9C		
ROS	Scan/ Log Decoder*				
	—	Test Word 13 (actual response adr)	—		80
	—	Test Word 14 (mask adr)	—		84
	0C	Error Register	A0		88
	02	Mover Function Register	A4		8C
	05	Current ROS Address (PSW 32 - 39)	A8		90
	14	Byte Counters, General Purpose Stats	AC		94
	18	Local Store, Address Register, Length Ctrs	B0		98
	0D	LCS Status	B4		9C
	15	H Register (0 - 27, parity)	B8		A0
	35	H Register (28 - 31)	BC		A4
	16	M Register (0 - 27, parity)	C0		A8
	36	M Register (28 - 31)	C4		AC
	17	R Register (0 - 27, parity)	C8		B0
	37	R Register (28 - 31)	CC		B4
	11	L Register (0 - 27, parity)	D0		B8
	31	L Register (28 - 31)	D4		BC
	11	Storage Data Register (0 - 27, parity)	D8		—
	31	Storage Data Register (28 - 31)	DC		—
	1C	Common Channel Group #1	E0		C0
	1D	Common Channel Group #2	E4		C4
	1E	Common Channel Group #3	E8		C8
	19	Multiplex Channel Group #1	EC		CC
	1A	Multiplex Channel Group #2	F0		D0
	1B	Multiplex Channel Group #3	F4		D4
	12-0	Selector Channel Group #1 (0-31)	F8	88	D8
	13-0	Selector Channel Group #1 (parity)	FC	8C	DC
	13-1	Selector Channel Group #2 (parity)	100	90	E0
	12-1	Selector Channel Group #2 (0-31)	104	94	E4
	12-2	Selector Channel Group #3 (0-31)	108	98	E8
	13-2	Selector Channel Group #3 (parity)	10C	9C	EC
	13-3	Selector Channel Group #4 (parity)	110	A0	F0
	12-3	Selector Channel Group #4 (0-31)	114	A4	F4
	12-5	Selector Channel Group #6 (0-31)	118	A8	F8
	12-4	Selector Channel Group #5 (0-31)	11C	AC	FC
	13-4	Selector Channel Group #5 (parity)	120	B0	100

* Hex values
** Sheets 2 - 4 show details

FIGURE 12. SCAN - OUT/LOGOUT: LOCATIONS AND DATA (PART 1 OF 4)

Storage Location	Bits	Data
0084	0	SAR P (8-15)
	1-8	SAR 8-15
	9	SAR P (16-23)
	10-17	SAR 16-23
	18	SAR P (24-31)
	19-26	SAR 24-31
	27	Unused
	28-31	Byte Stats
0088	0	IAR P (8-15)
	1-8	IAR 8-15
	9	IAR P (16-23)
	10-17	IAR 16-23
	18	IAR P (24-31)
	19-26	IAR 24-31
008C	0	ROSDR P (0-30)
	1-3	ROSDR 1-3 Mover Input Left
	4-5	ROSDR 4-5 Mover Input Right
	6-11	ROSDR 6-11 Q and P Address Field
	12-15	ROSDR 12-15 Address Extension Field
	16-18	ROSDR 16-18 Address Control Field
	19	Unused
	20-24	ROSDR 19-25 Adder Latch to Ingate
	25	Emulator Feature
	26-28	ROSDR 25-27 LS Addressing
	29-31	ROSDR 28-30
0090	0	ROSDR P (31-55)
	1-3	ROSDR 32-34 Invalid Digit Test and IC Control
	4-8	ROSDR 35-39 Gating Into Adder Latch
	9-12	ROSDR 40-43 Mover Destination
	13-14	ROSDR 44-45 Byte Ctr Function Control
	15-17	ROSDR 46-48 Counter Controls, MD, L Byte, M Byte
	18-20	ROSDR 49-51 Carry Insert Control
	21-22	ROSDR 52-53 Mover Output Left
	23-24	ROSDR 54-55 Mover Output Right
	25	Unused
	26-28	Mover Function (CPU)
	29-31	Mover Function (I/O)
0094	0	ROSDR P (56-88)
	1-4	ROSDR 57-60 Emit Field
	5-7	ROSDR 61-63 Outgates to Left Adder Input Gate
	8	ROSDR 64 TC Gating to Left
	9-11	ROSDR 65-67 Outgates to Right Adder Input Gate
	12-15	ROSDR 68-71 Adder Function CPU
	16-21	ROSDR 72-77 Condition Branch Grp A
	22-26	ROSDR 78-82 Condition Branch Grp B
	27	ROSDR 83 Emulator Feature
	28-31	ROSDR 84-87 Stat Setting Function
0098	0-4	Unused
	5	Emulator Feature
	6-17	Previous ROS Address
	18-23	Unused
	24-25	ROSDR 88-89 Stat Setting Function
	26-31	ROSDR 90-95 Emulator Feature
009C	0	One Syllable Op Stat
	1	Refetch Stat
	2-4	Unused
	5	Emulator Feature
	6-17	Current ROS Address
	18-23	Interrupt Register
	24-31	PSW 32-39
00A0	0-3	Half-Sum Cks
	4-7	Sum Cks
	8	Carry Cks
	9-11	L, M, MD Ctr Cks
	12-13	G1 and G2 Ck
	14-16	Mover Cks, U, V, W
	17	Unused
	18-20	SAR Cks
	21-23	ROS Cks
	24	Protect Tag
	25	LCS Feature
	26	Log Request
	27-31	Unused
00A4	0-31	Unused
00A8	0-31	Same as Location 009C
00AC	0	I/O Mode
	1-3	I/O Register (P, 30, 31)
	4-5	Interrupt Stats (Timer, Console)
	6-8	L Byte Ctr
	9-11	M Byte Ctr
	12-16	F Register
	17	Q Register
	18-19	Edit Stat
	20-27	General Purpose Stats
	28	L Sign
	29	R Sign
	30	Carry
	31	RTL
00B0	0-6	LSAR
	7-8	LS Function Register
	9-13	J Register
	14-18	MD Counter
	19	Unused
	20-25	Length Counter 1 (S, P, 0-3)
	26-31	Length Counter 2 (S, P, 0-3)
00B4	0-3	LCS Feature
	4	Unused
	5-8	LCS Feature
	9-31	Unused
00B8	0-31	H Register
00BC	0-23	Unused
	24-27	H Register Fold (28-31)
	28-31	Unused
00C0	0-31	M Register
00C4	0-23	Unused
	24-27	M Register Fold (28-31)
	28-31	Unused
00C8	0-31	R Register
00CC	0-23	Unused
	24-27	R Register Fold (28-31)
	28-31	Unused
00D0	0-31	L Register
00D4	0-23	Unused
	24-27	L Register Fold (28-31)
	28-31	Unused
00D8	0-31	SDR
00DC	0-23	Unused
	24-27	SDR Fold (28-31)
	28-31	Unused
00E0	0-3	I/O Inst (Start, Test, Halt, Test)
	4-6	Channel Number
	7-10	Inst Reply
	11	Reply
	12	Branch on Channel Interrupt
	13	Proceed on Interrupt
	14	Time Out
	15	Time Out Ck
	16	Foul
	17-31	Unused
00E4	0	Routine Received
	1	PCI Enable
	2	Break-In
	3	I/O Routine
	4	Early First Cycle
	5	First Cycle
	6	Chain First Cycle

FIGURE 12. SCAN-OUT/LOGOUT: LOCATIONS AND DATA (PART 2 OF 4)

Channel Only Logout	Full Logout	Bits	Data
	00E4	7	LS Read
		8	LS Write
		9	Channel to Adder Latches Data Transfer and Control
		10	Adder Latches to Channel Data Transfer and Control
		11	Chain
		12	Last Cycle
		13	Break-Out
		14-17	Storage Byte Control Register
		18	Unused
		19-22	ROSDR Bits 33, 34, 47, 48
		23	First Cycle Check
		24-31	Unused
	00E8	0-3	Buffer 1
		4-7	Buffer 2
		8-11	Buffer 3
		12-16	I/O Stats
		17	Unused
		18	I/O Check Mode
		19-21	Logs (1, 2, 3)
		22	Gate Status
		23	Log Reset
		24-31	Unused
	00EC	0-8	Buffer 1 (P, 0-7)
		9-17	Buffer 2 (P, 0-7)
		18-31	Request Log-Out
	00F0	0	Select Out
		1	Select In
		2	Op In
		3	Suppress Out
		4	Request In
		5	Service Out
		6	Address Out
		7	Command Out
		8	Service In
		9	Address In
		10	Status In
		11-19	Bus Out (P, 0-7)
		20	Program Check
		21	Storage Protect Check
		22-31	Unused
	00F4	0-3	Controlled Emit
		4-8	Routine Request Triggers (A, E1-E4)
		9-11	Priority (2, 3, PCI)
		12-17	Control Triggers (CC, DTC, UCW, IB Full, Poll, Burst Mode)
		18-21	Mpx I/O Stats
		22	Data Transfer Control
		23	CC Reset Control
		24-31	Unused
88	00F8	0-31	Selector Channel B Register (0-31)
8C	00FC	0-27	Unused
		28-31	Selector Channel B Register Parity
90	0100	0-27	Unused
		28-31	Selector Channel C Register Parity
94	0104	0-31	Selector Channel C Register (0-31)
98	0108	0-1	Byte Counter A (2, 1)
		2-4	Byte Counter B (P, 2, 1)
		5-6	End Register (2, 1)
		7-8	Last Words (3, 1)
		9	EOR Count Interlock
		10	EOR 1 Latch
		11	EOR 2 Latch
		12	EOR Read Interlock
		13	B Almost Changed
		14	Local Store Enable
		15	Local Store Register Full
		16	C Register Full

Channel Only Logout	Full Logout	Bits	Data
98	0108	17-20	Read (Bkwd, Op, Rdy, Interface)
		21-23	Write (Op, Rdy, Interface)
		24-31	Channel Checks (Sim, ILI, Prog, Stor Prot, Chan Data, Chan Ctrl, IF Ctrl, Chain 1)
9C	010C	0-27	Unused
		28-31	Group 3 Parity (Byte Ctr, Last Word 2, Reg Full B, CD = PC Type)
A0	0110	0-27	Unused
		28-31	Group 4 parity (UA Fetch, Cycle Ctr Step 0, Priority 1, Stat 0)
A4	0114	0-7	Position Register (CCW-1 Type, CCW-2 Type, Unit Sel, Rd Store, Wr Fetch, End Up, Compare, Interrupt)
		8-10	Cycle Ctr Phase A Step (1, 2, 3)
		11-13	Clock (A0, A1, Step)
		14	Local Store Request
		15	PCI Request
		16-17	Priority (2, 3)
		18-23	Request Register (0-5)
		24-26	Stats 1-3
		28-31	Common Channel Detect (LS, PRI 1, PRI 2-3, PCI, Inhibit Routine)
A8	0118	0-6	General Purpose Register (1-7)
		7-8	Unused
		9-13	Flag Register (CDA, CC, SILI, Skip, PCI)
		14	Finish
		15	First Word
		16	First Byte
		17	Total Record Fetch
		18	Write Chain Proceed
		19	Stop Release
		20-22	Unused
		23	Status Next Latch
		24-27	Multi-Purpose (C1-C4)
		28	Suppress Out
		29	Request In
		30	Service Out Hold
		31	Block Status In
AC	011C	0	Inhibit Read Store
		1-4	A Clock (A, B, C, D)
		5 6	Special Purpose (D1, D2)
		7	Instruction Scan
		8	Poll
		9	Poll Interrupt End
		10	Instruction Inhibit
		11	BC Ready
		12	UA to Bus Out
		13	Select Address Out
		14-15	Compare (= or ≠)
		16	Interface Chain Data Address First Byte
		17	Chain Data
		18	Byte Ctr Mod Enable
		19	Write Chain Ready
		20	Record End
		21	Op In Test
		22	Channel Stop
		23	Select Out
		24	Sel In
		25	Op In
		26-28	Service Out, Address Out, Command Out
		29-31	Service In, Address In, Status In
B0	0120	0-27	Unused
		28	Position Register Transfer
		29	Channel In Use
		30	Stop
		31	Stop Routine
	0124	0-15	Reserved for Selector Channel and Misc Features
		16-31	Reserved for Mpx Channel

FIGURE 12. SCAN-OUT/LOGOUT: LOCATIONS AND DATA (PART 3 OF 4)

Storage Location	Bits	Data
0088	0-3	Half-Sum Checks
	4-7	Sum Checks
	8	Carry Check
	9-11	Counters(L Byte, M Byte, MD) Checks
	12-13	Length Counters (G1, G2) Checks
	14-16	Mover Checks (U, V, and W)
	17	Unused
	18-20	SAR Checks
	21-23	ROS Checks
	24	Protect Tag
	25	LCS Feature
	26	Log Request
	27-31	Unused
008C	0-25	Unused
	26-28	Mover Function (CPU)
	29-31	Mover Function (I/O)
0090	0	One Syllable Op Stat
	1	Refetch Stat
	2-4	Unused
	5	Emulator Feature
	6-17	Current ROS Address
	18-23	Interrupt Register
	24-31	PSW 32-39 (ILC, CC, PM)
0094	0	I/O Mode
	1-3	I/O Register (P, 30, 31)
	4-5	Interrupt Stats (Timer, Status)
	6-8	L Byte Counter
	9-11	M Byte Counter
	12-16	F Register
	17	Q Register
	18-19	Edit Stats
	20-27	General Purpose Stats
	28-29	L Sign, R Sign
	30	Carry
	31	RTL
0098	0	Unused
	1-6	Local Storage Address Register
	7-8	Local Storage Function Register
	9-13	J Register
	14-18	MD Counter
	19	Unused
	20-25	Length Counter 1 (S, P, 0-3)
	26-31	Length Counter 2 (S, P, 0-3)
009C	0-3	LCS Feature (Mark, Key, Adr, Data)
	4	Unused
	5-8	LCS Feature (Unit Identity)
	9-31	Unused
00A0	0-31	H Register
00A4	0-23	Unused
	24-27	H Register Fold (28-31)
	28-31	Unused
00A8	0-31	M Register
00AC	0-23	Unused
	24-27	M Register Fold (28-31)
	28-31	Unused
00B0	0-31	R Register
00B4	0-23	Unused
	24-27	R Register Fold (28-31)
	28-31	Unused
00B8	0-31	L Register
00BC	0-23	Unused
	24-27	L Register Fold (28-31)
	28-31	Unused
00C0	0-3	I/O Instruction (Start, Test, Halt, Test)
	4-6	Channel Number (4, 2, 1)
	7-10	Instruction Reply (0-3)
	11	Reply
	12	Branch on Channel Interrupt
	13	Proceed on Interrupt
	14-16	Time Out, Time Out Check, Foul
	15-31	Unused
00C4	0	Routine Received
	1	PCI Enable
	2	Break In
	3	I/O Routine
	4-6	Early First Cycle, First Cycle, Chain First Cycle
	7-8	Local Store (Read, Write)
	9	Channel to Adder Latch Data Transfer and Control
	10	Adder Latch to Channel Data Transfer and Control
	11-13	Chain, Last Cycle, Break Out
	14-17	Storage Byte Control Register
	18	Unused
	19-22	ROSDR Bits 33, 34, 47, 48
	23	First Cycle Check
	24-31	Unused
00C8	0-11	Buffer 1, Buffer 2, Buffer 3
	12-16	I/O Stats
	17	Unused
	18	I/O Check Mode
	19-23	Logs (1, 2, 3, Gate Status, Reset)
	24-31	Unused
00CC	0-8	Buffer 1
	9-17	Buffer 2
	18-22	Unused
	23	Request Logout
	24-31	Unused
00D0	0-2	Select Out, Select In, Op In
	3-4	Suppress Out, Request In
	5-7	Service Out, Address Out, Command Out
	8-10	Service In, Address In, Status In
	11-19	Bus Out
	20-21	Program Check, Storage Protect Check
	22-31	Unused
00D4	0-3	Controlled Emit
	4-8	Routine Request Tgrs (A, E1-E4)
	9-11	Priority (2, 3, PCI)
	12-17	Control Tgrs (CC, DTC, UCW, IB Full, Poll, Burst Mode)
	18-21	Mpx I/O Stats
	22	Data Transfer Control
	23	CC Reset Control
	24-31	Unused
00D8	0-31	Selector Channel B Register
00DC	0-27	Unused
	28-31	Selector Channel B Register Parity
00E0	0-27	Unused
	28-31	Selector Channel C Register Parity
00E4	0-31	Selector Channel C Register
00E8	0-1	Byte Counter A (2,1)
	2-4	Byte Counter B (P, 2, 1)
	5-6	End Register (2, 1)
	7-8	Last Words (3, 1)
	9-12	End of Record (Count Interlock, 1, 2, Read Interlock)
	13	B Almost Changed
	14	Local Store Enable
	15-16	Register Full (LS, C)
	17-20	Read (Backward, Op, Ready, Interface)
	21-23	Write (Op, Ready, Interface)
	24-31	Channel Checks (Sim, ILI, Prog, Stor Prot, Chan Data, Chan Ctrl, IF Ctrl, Chain 1)
00EC	0-27	Unused
	28-31	Group 3 Parity (Byte Ctr P, Last Word 2, Register Full B, CD PC Type)
00F0	0-27	Unused
	28-31	Group 4 Parity (UA Fetch, Cycle Ctr Phase A Step 0, Priority 1, Stat 0)
00F4	0-7	Position Register (CCW-1 Type, CCW-2 Type, Unit Sel, Read Store, Write Fetch, End Up, Compare, Interrupt)
	8-10	Cycle Counter Phase A Step (1, 2, 3)
	11-13	Clock (A0, A1, Step)
	14-15	Local Store Request, PCI Request
	16-17	Request Register (Priority 2, 3)
	18-23	Request Register (0-5)
	24-26	Request Register Stats (1-3)
	27-31	Common Channel Detect (LS, PRI-1, PRI-2-3, PCI, Inh Rtne)
00F8	0-6	General Purpose Register (1-7)
	7-8	Unused
	9-13	Flag Register (CDA, CC, SILI, Skip, PCI)
	14	Finish
	15-16	First Word, First Byte
	17-19	Total Record Fetch, Write Chain Proceed, Stop Release
	20-22	Unused
	23	Status Next Latch
	24-27	Multi-Purpose (C1-C4)
	28-31	Suppress Out, Request In, Service Out Hold, Block Status In
00FC	0	Inhibit Read Store
	1-4	A Clock (A, B, C, D)
	5-6	Special Purpose (D1, D2)
	7	Instruction Scan
	8-9	Poll, Poll Interrupt End
	10	Instruction Inhibit
	11	BC Ready
	12	UA to Bus Out
	13	Select Address Out
	14-15	Compare (=, ≠)
	16-17	Interface Chain Data Address First Byte, Chain Data
	18-19	Byte Ctr Bad Enable, Write Chain Ready
	20-22	Record End, Op In Test, Channel Stop
	23-25	Select Out, Select In , Op In
	26-28	Service Out, Address Out, Command Out
	29-31	Service In, Address In, Status In
0100	0-27	Unused
	28	Position Register Transfer
	29	Channel In Use
	30-31	Stop, Stop Routine
0104	0-15	Reserved for Selector Channel and Miscellaneous Features
	16-31	Reserved for Multiplex Channel

FIGURE 12. SCAN-OUT/LOGOUT: LOCATIONS AND DATA (PART 4 OF 4)

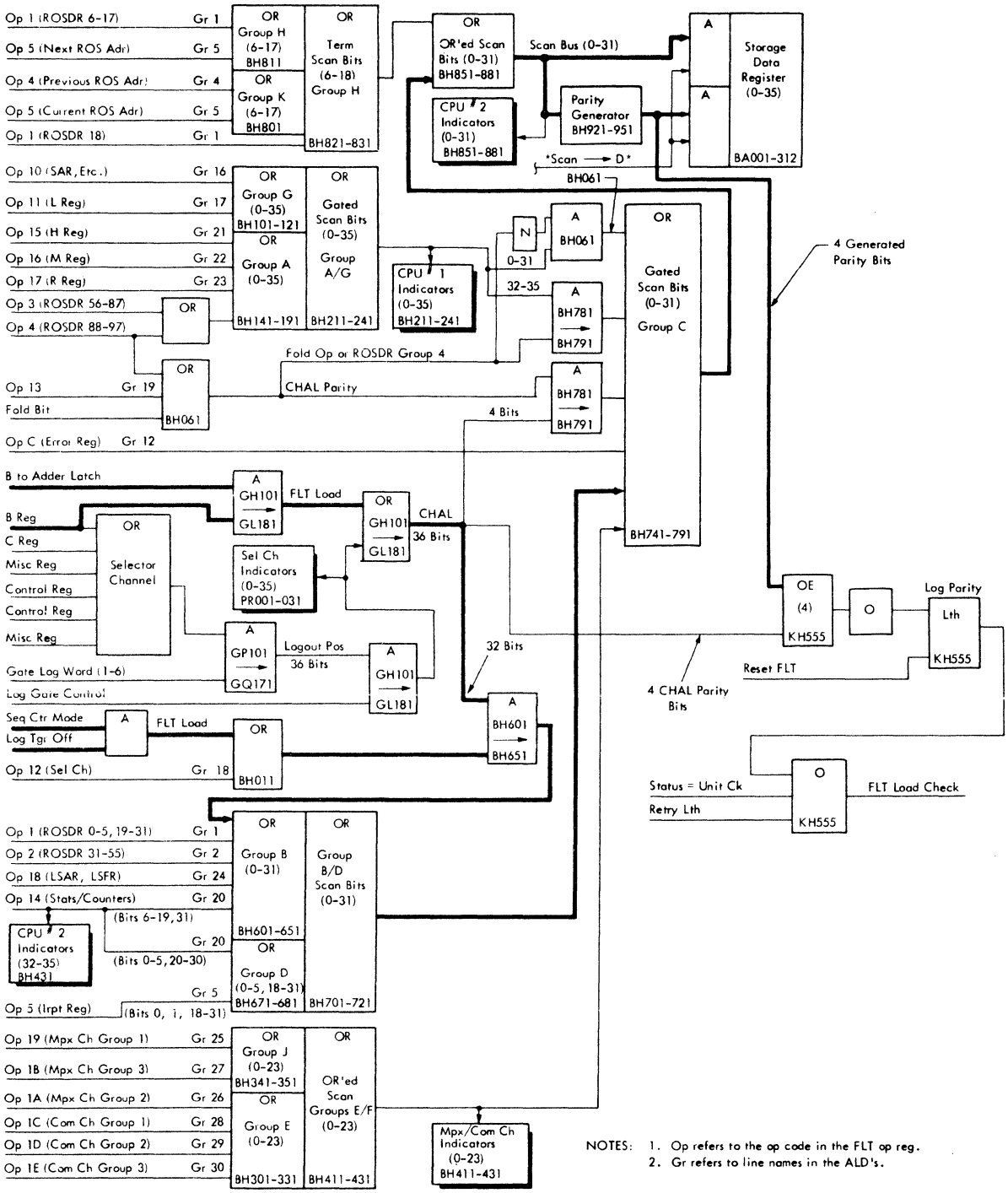


FIGURE 13. SCAN-OUT/LOGOUT: LOGIC AND INDICATORS

Kernel Name	CAS Page	ROS Address (From LCW 19-30)	Equivalent Hex Address in LCW 16-31	Function
Fetch LCW	QY110	F4E	1E9C	Read in next LCW from main storage.
Execute LCW	QY110	F8B	1F16	Set controls and ROAR from LCW.
I-Fetch Entry	QY110	FB9	1F72	Go back to normal I-fetch.
FLT Load Call	QY140	FBC	1F78	Initiates FLT load and puts CPU in sequence counter mode.
Scan-In:	----	----	----	Sets registers, stats, etc. from main storage (up to 11 words).
Scan entry	QY310	F48	1E90	
Diagnose entry	QY310	F31	1E62	
Scan-Out:	----	----	----	Puts contents of registers, stats, etc. into main storage (up to 34 words).
Hardware entry	QY410	2C0	(0580)	
Full Scan Entry	QY410	F26	1E4C	
Partial Scan Entry	QY410	F23	1E46	
Com, Mpx, and Sel Ch Entry	QY410	F09	1E12	
Sel Ch Entry	QY420	F1B	1E36	
FLT Compare and Branch	QY510	F45	1E8A	Compares actual response with expected response of FLT zero and one cycle tests, sets pass/fail triggers, and branches on results.
Reset Error and FLT Op Registers	QY140	FB7	1F6E	Resets both CPU error and FLT op regs and then goes to I-fetch.
Set Ignore Error-I/O Tgr	QY150	F3A	1E74	Prevents error recognition and I/O break-in.
Reset Ignore Error-I/O Tgr	QY150	FD3-7	1FA6,8,A,C,E	Allows error recognition and I/O break-in.
Log Local Storage:	----	----	----	Puts contents of local storage into main storage.
Sector 0 Entry	QY450	F51	1EA2	
Sector 1 Entry	QY450	F11	1E22	
Sector 2 Entry	QY450	FD0	1FA0	
Sector 3 Entry	QY450	F90	1F20	
Beat Local Storage	QY130	224	0448	Continuous scan-in and check of a specified local storage address.
Ripple Local Storage	QY130	FB8	1F70	Scan-in and check of all local storage addresses.
Fetch/Alter Bump:	----	----	----	Permits any location in bump storage to be fetched or altered (group specified by L reg).
Word 0	QY140	FB5	1F6A	
Word 1	QY140	F35	1E6A	
Word 2	QY140	FB4	1F68	
Word 3	QY140	F34	1E68	
Reset Mpx UCW	QY440	F07	1E0E	Resets mpx unit control word to stop I/O device (while logging mpx channel).
Invert SAR Bit 16 Tgr:	----	----	----	----
Turn On	QY140	FB6	1F6C	Inverts SAR 16, causing 8K (word) relocation of main storage, then goes to I-fetch.
Turn Off	QY140	F36	1E6C	Restores normal storage addressing, then goes to I-fetch.
Large Capacity Storage (LCS) Controls	----	----	----	----
	QY140	FB3	1F66	Turn on LCS parity control tgr.
	QY140	F33	1E66	Turn on LCS byte parity mode tgr.
	QY140	FB2	1F64	Resets both LCS parity control and LCS byte parity mode triggers.

FIGURE 14. ROS KERNELS (MAINTENANCE ROUTINES)

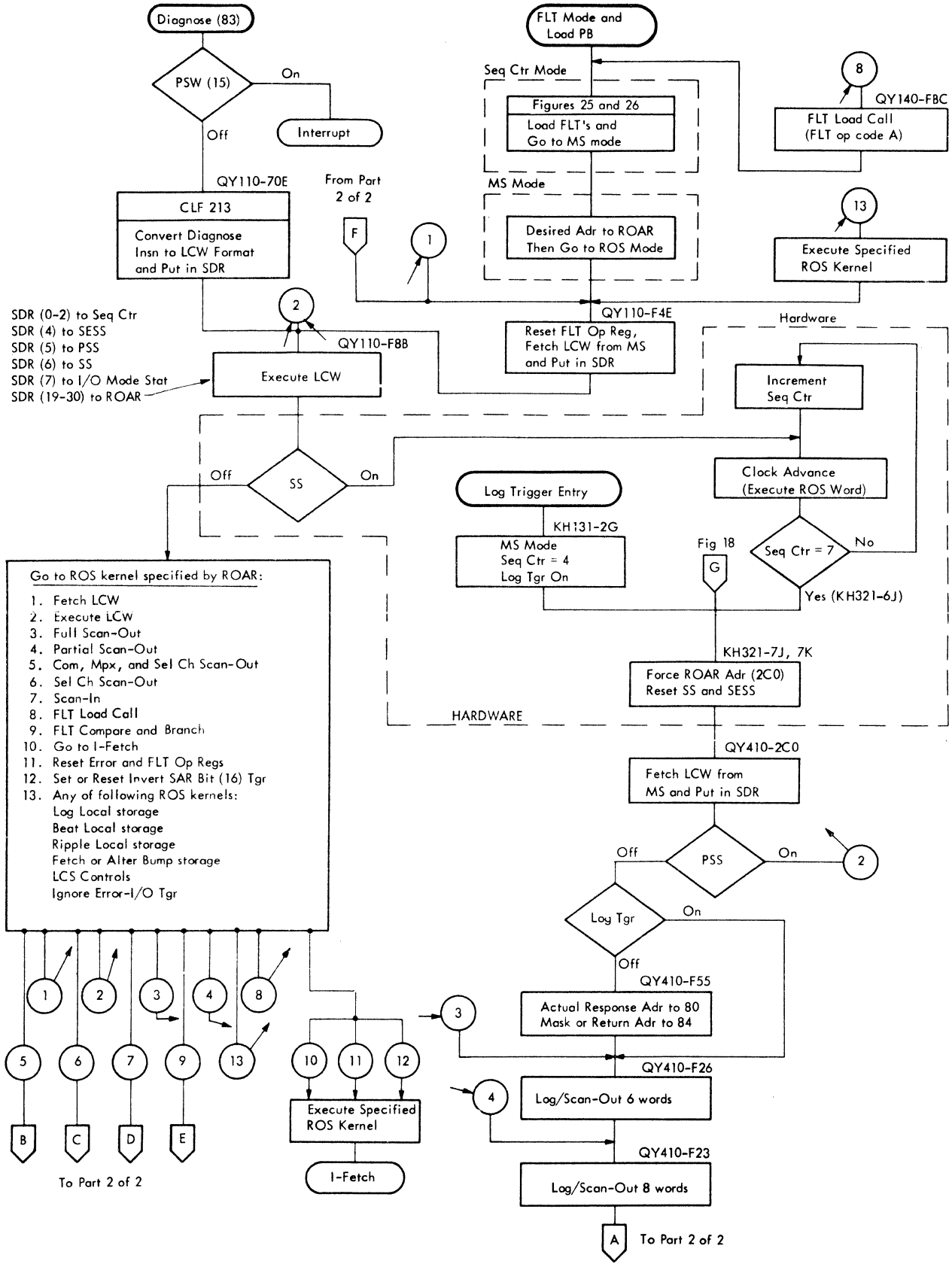


FIGURE 15. ROS KERNELS FLOWCHART: DIAGNOSE/FLT/LOG TRIGGER ENTRIES (PART 1 OF 2)

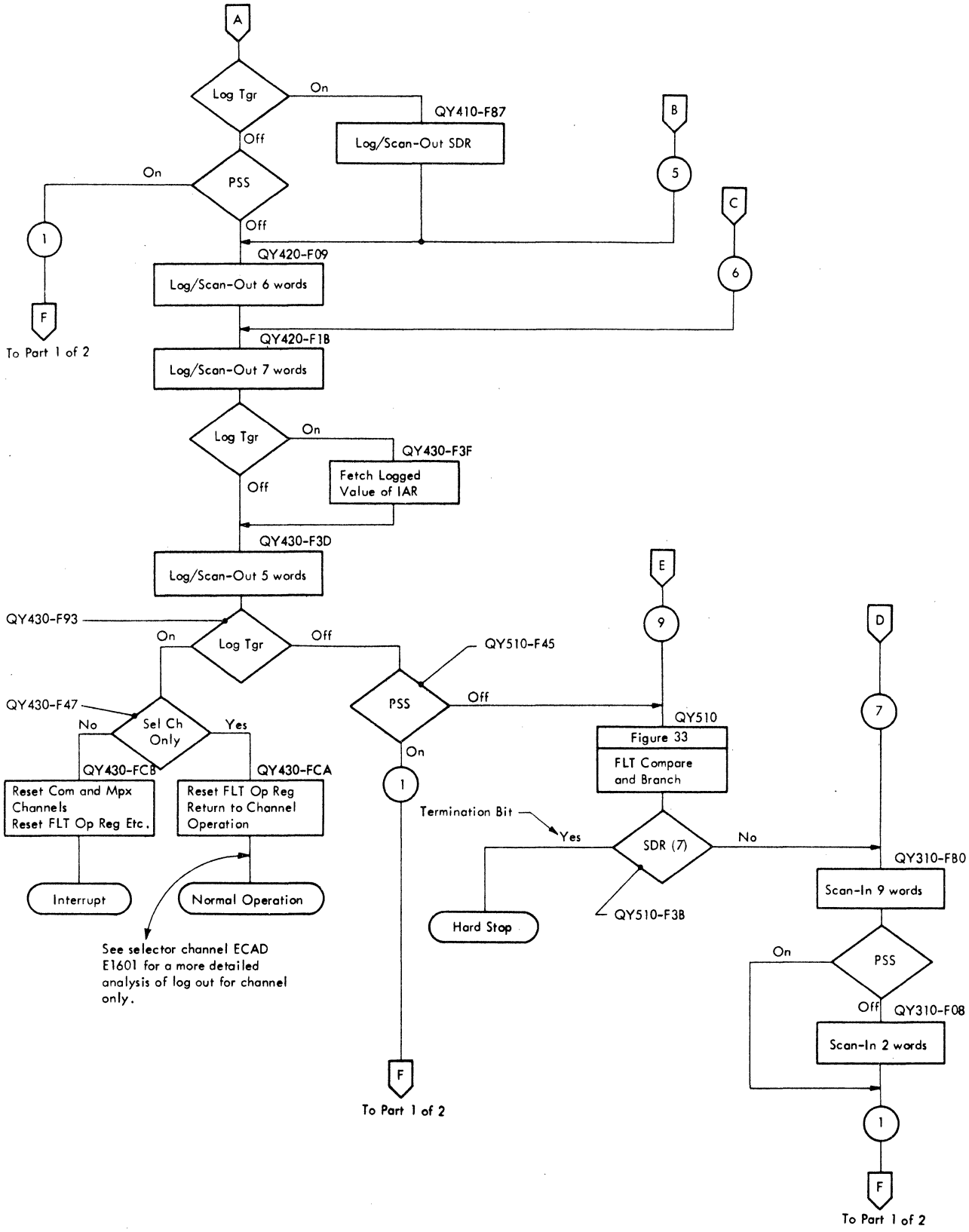


FIGURE 15. ROS KERNELS FLOWCHART: DIAGNOSE/FLT/LOG TRIGGER ENTRIES (PART 2 OF 2)

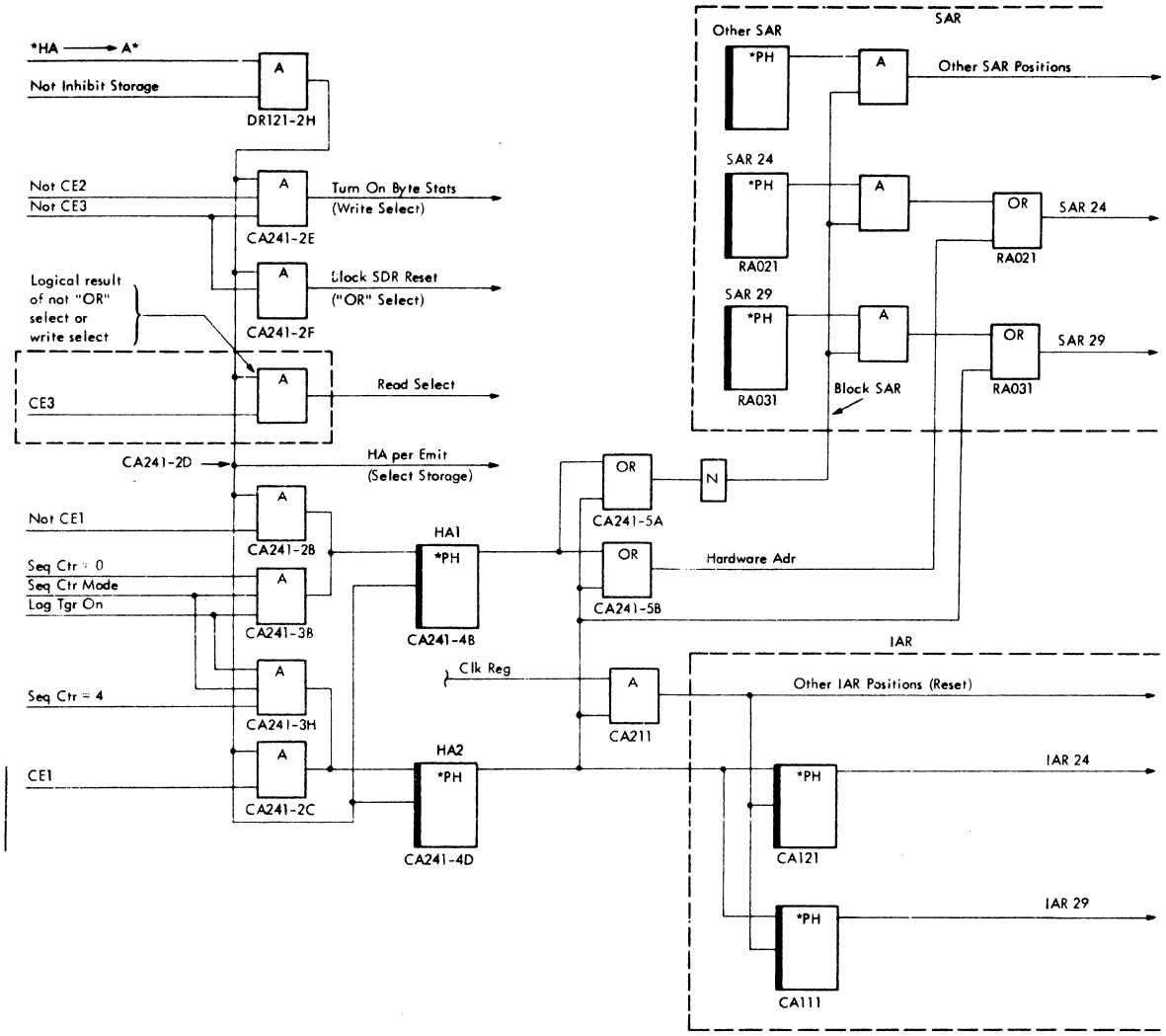


FIGURE 16. HARDWARE ADDRESSES NO. 1 AND NO. 2

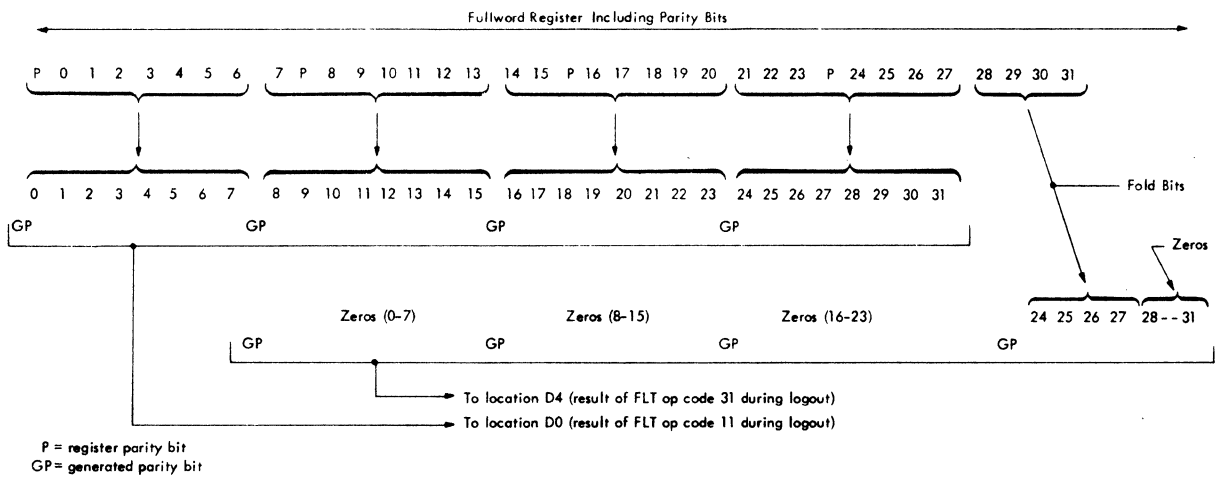


FIGURE 17. STORAGE LOCATIONS AND BITS FOR L REGISTER LOGOUT

parity positions) is sent directly to storage location 80 (positions 0-35) and no parity is generated.

Fold Operation: FLT op reg position 0 specifies the fold operation. This operation is necessary to completely log or scan-out a 32-bit register as discussed in Parity Bit Propagation. The fold operation sends bits 28-31 of the specified register into SDR (24-27) via the scan bus. This operation occurs on FLT op reg codes 31, 35, 36, and 37.

Logout Operation: Initiated by the logout pushbutton or a system error check. Either condition turns on the log trigger (KT151) and the log trigger indicator located on the system control panel. The logout operation uses all three CPU control modes: sequence counter, main store, and ROS. The ROS mode portion of a logout operation is performed by the ROS scan-out kernel. Up to 42 storage locations may be used for the storing of machine status. See Figure 12.

Figure 18 shows the initial logout sequence under sequence counter control mode and main store (MS) mode before logout is completed under ROS mode.

Log Trigger

The log trigger is set on if the log-request trigger (KT101-5F) is on and an error condition occurs. It may also be set on by depressing the logout PB on the system control panel. Either of the two preceding conditions initiates a logout which is indicated by the log trigger indicator on the system control panel. The log trigger is checked in one of the ROS maintenance routines (scan-out kernel) where its status determines the path to be followed in ROS.

Supervisory Stat

When on, the supervisory stat (SS) puts the number of microinstructions (ROS words) to be executed under control of the sequence counter. The SS also inhibits storage access unless the supervisory enable storage stat (SESS) is on. The SS is set to the value of SDR(6) by the microorder E → SCANCTL combined with EMIT 1000 (QY110-C5). When the sequence counter reaches seven, the SS is reset off (KH321-6J).

Progressive Scan Stat

The progressive scan stat (PSS) is set on by bit 14 of the diagnose instruction, via SDR(5), or by bit 5 of a linkage control word (LCW). The PSS is also set on by depressing the start PB when the FLT mode switch is on the force pass position. The PSS is checked in various ROS kernels where its status determines the path to be followed within ROS. Testing the PSS resets it off unless an inhibit storage condition (SS on and SESS off) exists. When the PSS is tested and found to be on, it usually initiates the fetching of a new LCW from main storage. The PSS is off when reset, normally off for FLT execution, and always off during an error logout.

Supervisory Enable Storage Stat

The supervisory enable storage stat (SESS) allows access to main storage even though the supervisory stat (SS) is on. This is accomplished by deconditioning the inhibit storage line activated by the supervisory stat (KH331-2E). The SESS is set to the value of SDR(4) by the microorder E → SCANCTL combined with EMIT 1000 (QY110-C5). The SESS is reset off when the sequence counter equals seven and the supervisory stat is on (KH321-6J).

Binary Trigger

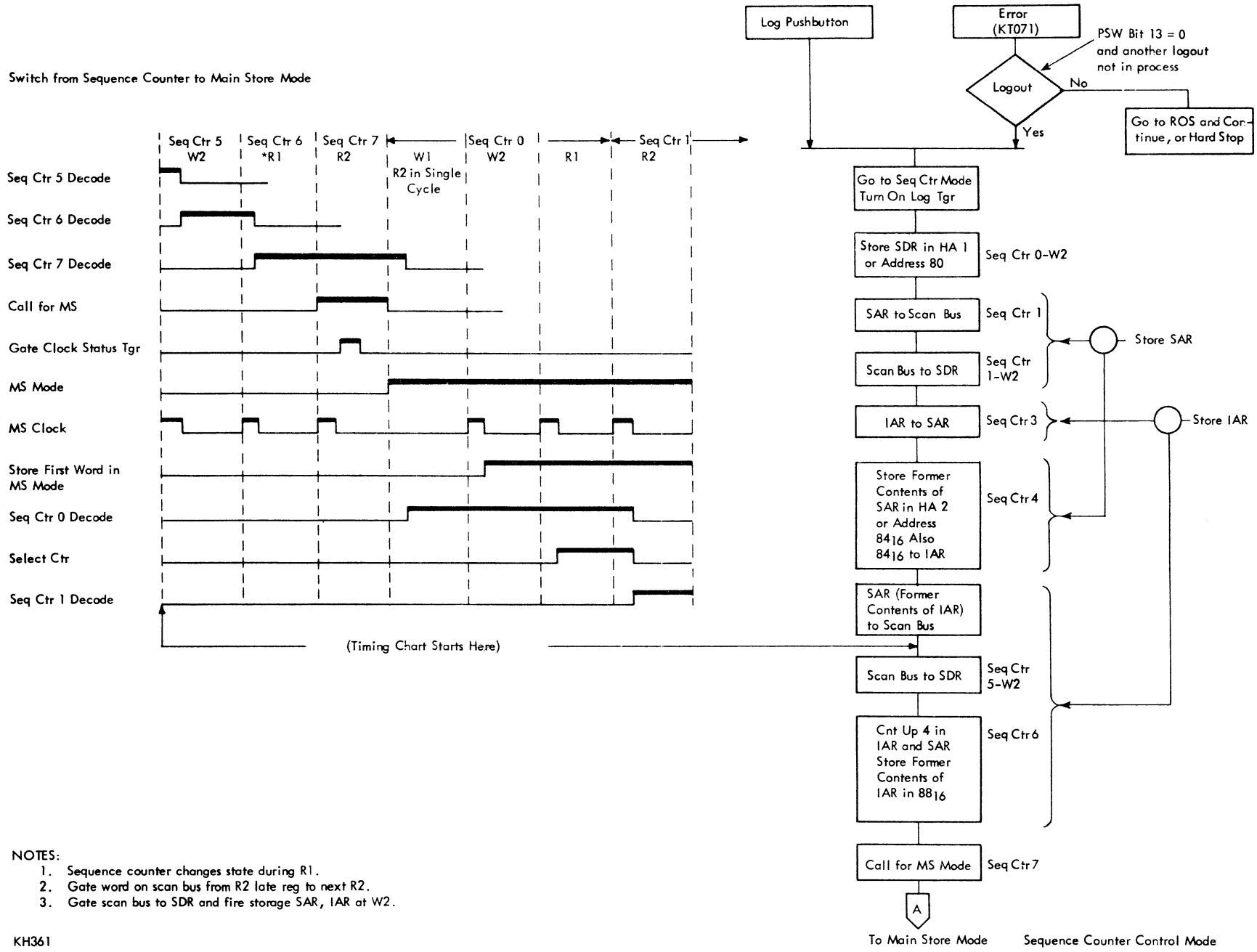
The binary trigger is used when running FLT's. In main store mode, FLT op reg instructions are used to reset off (op codes 07 or 08), or step (op code 0F), or test (op code 0E) this trigger. In ROS mode, the microorder E → SCANCTL (combined with the emit field bits) is used to test and/or set or reset the binary trigger in the FLT compare and branch kernel (QY510).

Scan Test Counter

The scan test counter controls the number of times (16) each individual test is executed during the FLT zero and one-cycle tests. The microorder, STC = 0, branches on and increments the counter (QY510-G5) on each pass through the FLT compare and branch kernel. The counter equals one when in the reset position.

Pass/Fail Triggers

The pass and fail triggers are used in the FLT compare and branch kernel in ROS (QY510). They are set, according to the status of the binary trigger, by the microorder E → SCANCTL in combination with EMIT 0001. That is, if the binary trigger is on, the fail trigger is set; if the binary trigger is off, the pass trigger is set. They are both unconditionally reset off by the same microorder (E → SCANCTL) in combination with EMIT 0101. The pass trigger is tested, and branched on, by the microorder SCPS. The fail trigger is tested, and branched on, by the microorder SCFS.

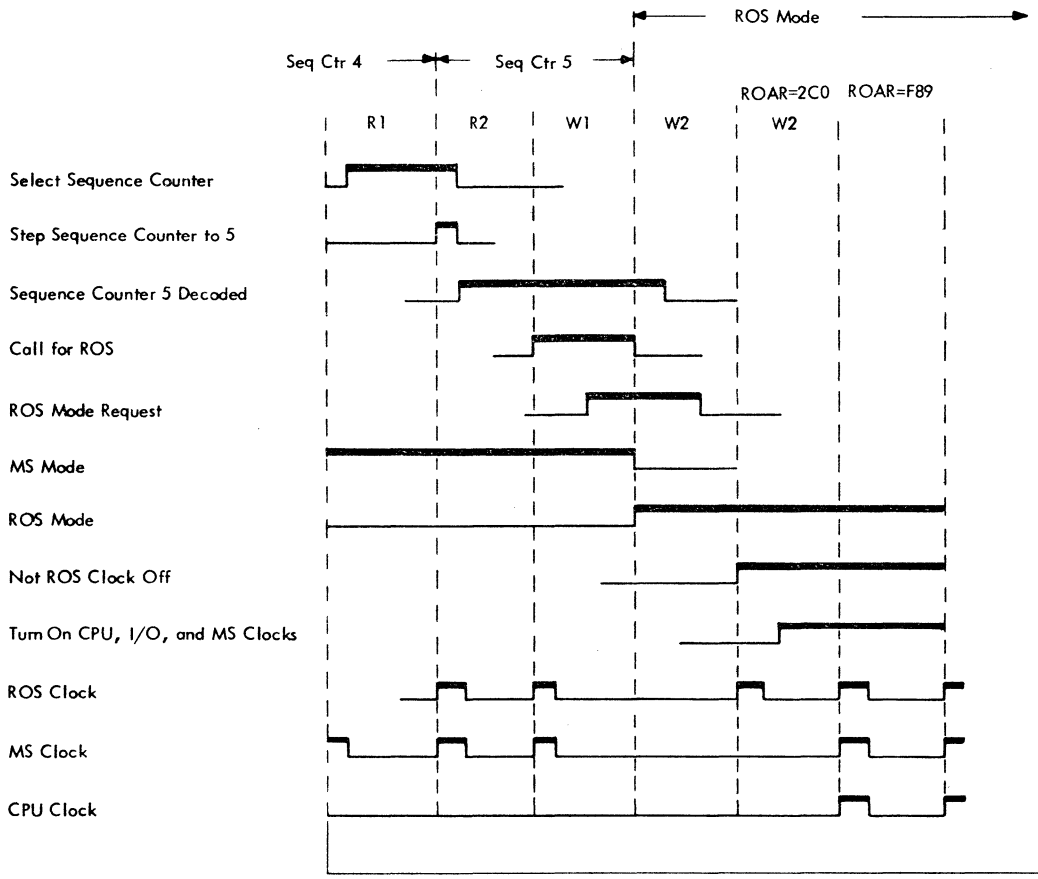


NOTES:

1. Sequence counter changes state during R1.
2. Gate word on scan bus from R2 late reg to next R2.
3. Gate scan bus to SDR and fire storage SAR, IAR at W2.

KH361

FIGURE 18. LOGOUT UNDER SEQUENCE COUNTER AND MAIN STORE MODES (PART 1 OF 2)



NOTES:
1. Sequence counter changes state during R1.
2. Gate word on scan bus from R2 late reg to next R2.
3. Gate scan bus to SDR and fire storage SDR, IAR at W2.

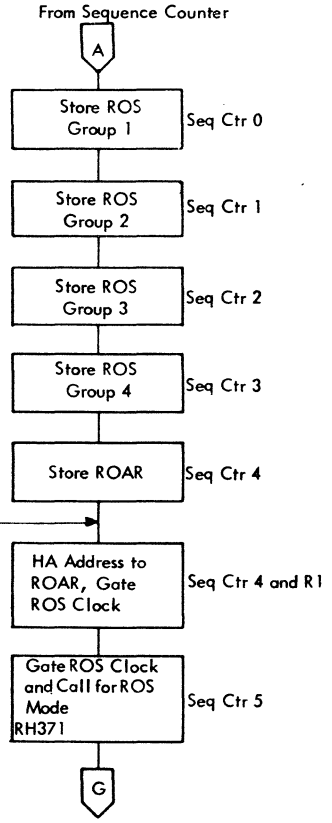


Figure 15 (1 of 2)
ROS Mode

FIGURE 18. LOGOUT UNDER SEQUENCE COUNTER AND MAIN STORE MODES (PART 2 OF 2)

SUPERVISORY CONTROLS

The supervisory controls are the hardware circuits that determine the CPU control status and the gating (or blocking) of certain clock pulses within the system (Figure 19). These circuits can be divided into two logical groups.

1. Clock gating control circuits:
   a. Circuits to recognize conditions that require the stopping of one or more logic clocks.
   b. Four clock stop triggers that block or gate the basic reg and late reg pulses within the system.
2. CPU control status circuits:
   a. Circuits that recognize the need for, and request a change in CPU control status.
   b. A log trigger and three CPU control mode triggers that determine the CPU control status.

Clock Gating Control Circuits

There are two main types of clocks in the CPU: free-running, and non free-running (Figure 20). The free-running clocks are latch, error, basic reg, and basic late reg. The non free-running clocks are CPU-I/O, ROS, and main storage.

The non free-running clocks are controlled by four clock stop triggers. These clock stop triggers are set/reset latches. Any condition that requires the blocking of a clock pulse(s) will turn on one or more of the following clock stop triggers:

1. CPU-I/O clock stop trigger -- When on, this trigger blocks the reg and late reg pulses to CPU circuits (regs and counters) and the common channel circuits.

2. ROS clock stop trigger -- When on, this trigger blocks the reg and late reg pulses that set and reset ROSDR and ROAR. (This effectively stops ROS.)

3. Main storage clock stop trigger -- When on, this trigger blocks the reg and late reg pulses that are used to generate a storage select from CPU, set IAR, and set SAR.

4. Storage holdoff clock stop trigger -- When on, this trigger serves the same function as the CPU-I/O clock stop trigger within CPU but does not block clock pulses to the common channel.

One way (of many) to stop the non free-running clocks is as follows:

1. The FLT load request trigger on, not start, and not sequence counter mode; brings up the normal interrupt line.

2. Normal interrupt turns on the main store, ROS, and CPU-I/O clock stop triggers.

3. The clock stop triggers, in turn, prevent the indicated clock pulses from occurring.

When all conditions needed to restart a clock are present, a reset to the clock stop trigger is generated.

CPU Control Status Circuits

The supervisory controls determine and set the CPU control status triggers. These are sequence counter mode, main store mode, and ROS mode triggers, and also the log trigger. These triggers disable controls that should not be in command and enable other controls to manipulate identical data paths. Note that this is not a priority function in the sense that one set of controls is caused to wait while another set performs a function.

Changing CPU Control Status

Changing the CPU control status generally involves a three-step sequence.

1. A supervisory interrupt condition turns on the clock stop triggers.

2. One dead cycle is then taken. During this dead cycle, a line labled "gate status" is used to set or reset the CPU control status triggers.

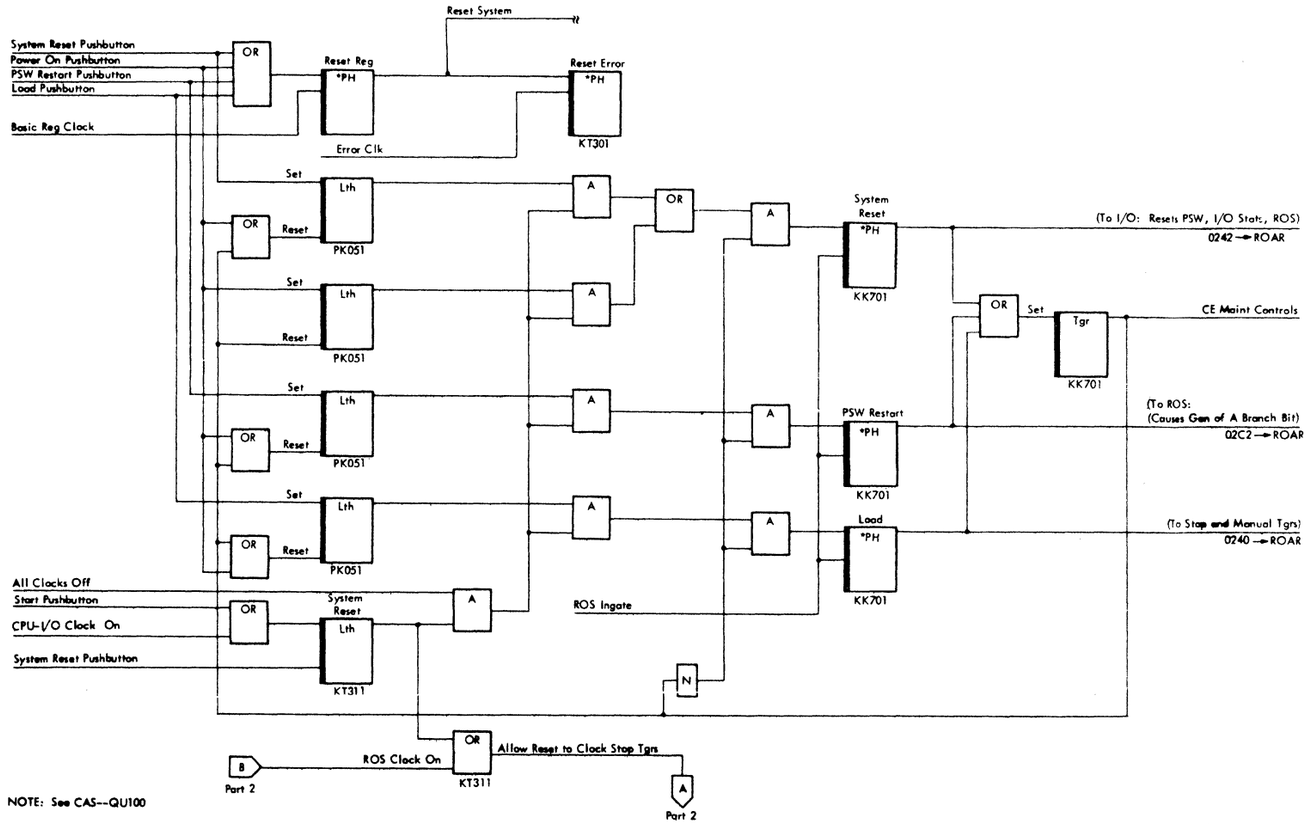
3. The logic clocks needed for the newly selected CPU mode have their clock stop triggers turned off.

A typical example, showing how the CPU control status is changed, is shown in the following logout sequence. Refer to TIM 209 (Sheet 1) and Figure 21. When a logout operation is initiated, the error interrupt line turns on the CPU-I/O, ROS, and MS clock stop triggers, thus freezing all registers. The next machine cycle has its non free-running reg and late reg pulses blocked, and is thus called a dead cycle. During this dead cycle, the log and sequence counter mode triggers are set on with a basic reg pulse. During the same dead cycle, the MS clock stop trigger is reset off at error reg time. Starting with the next machine cycle, the contents of SDR, SAR, and IAR are stored in locations 80, 84, and 88. Next, a call for MS mode is initiated. This resets the sequence counter mode trigger off and sets the MS mode trigger on. After the storing of ROSDR (groups 1-4) and ROAR, the ROS clock stop trigger is reset off, thus allowing the ROS clock to run.

During the next two cycles a call for ROS mode is initiated. This turns the MS mode trigger off, sets the ROS mode trigger on, and then resets all clock stop triggers off.

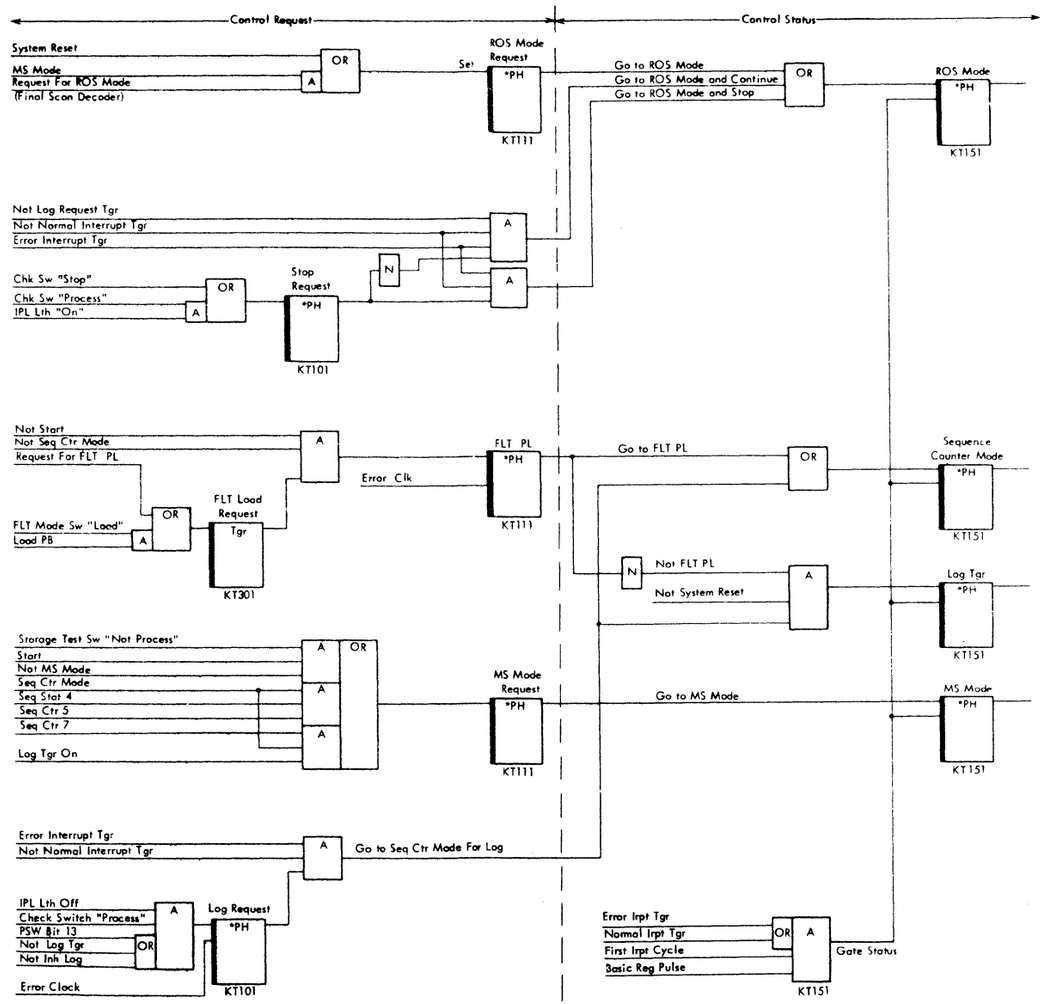
Supervisory Interrupts

The clock stop triggers and the CPU control status triggers make up the output interface of the supervisory controls (Figure 19). This interface is normally in a steady state. The output interface changes



NOTE: See CAS--QU100

FIGURE 19. SUPERVISORY CONTROLS (PART 1 OF 2)



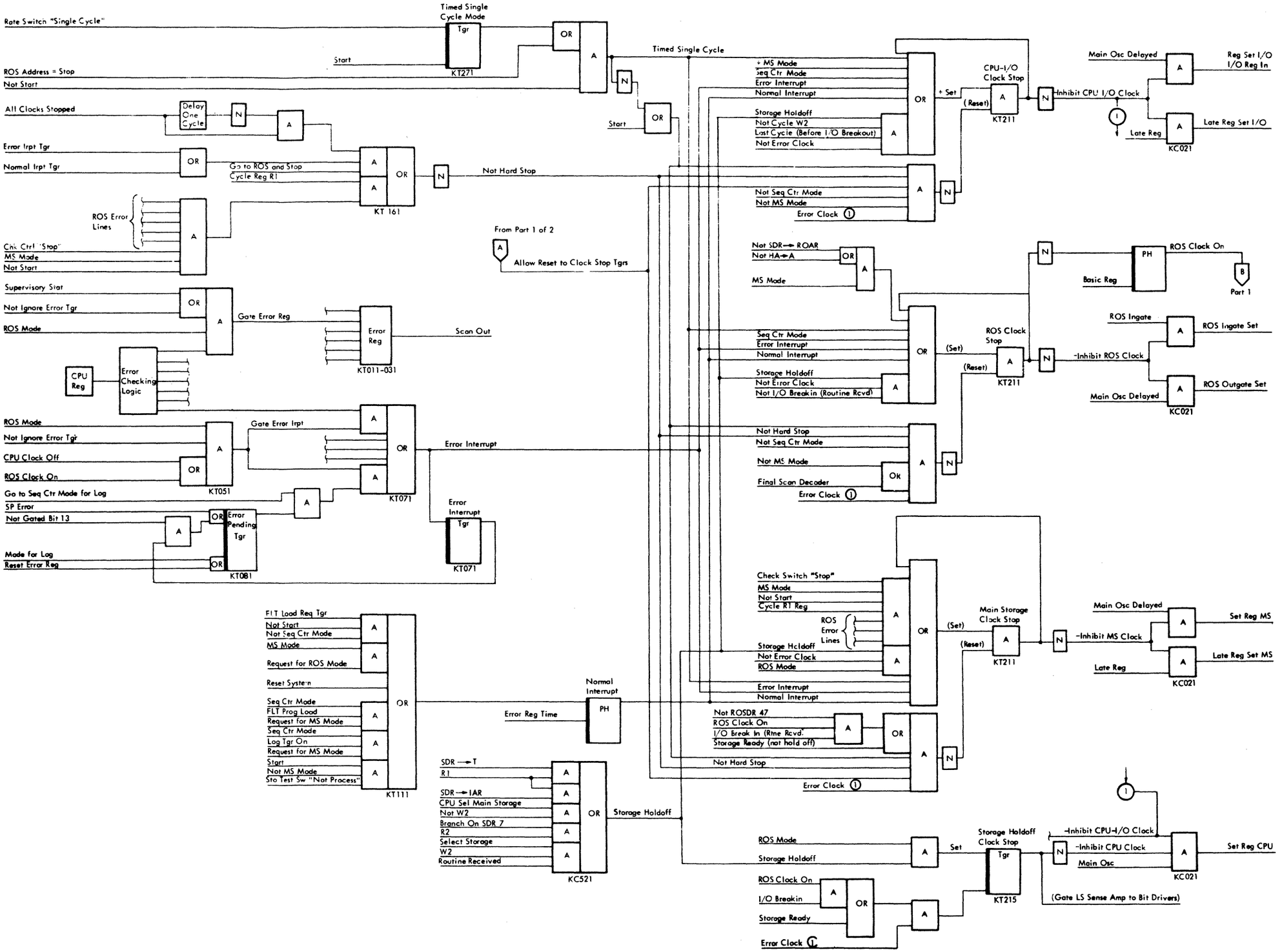
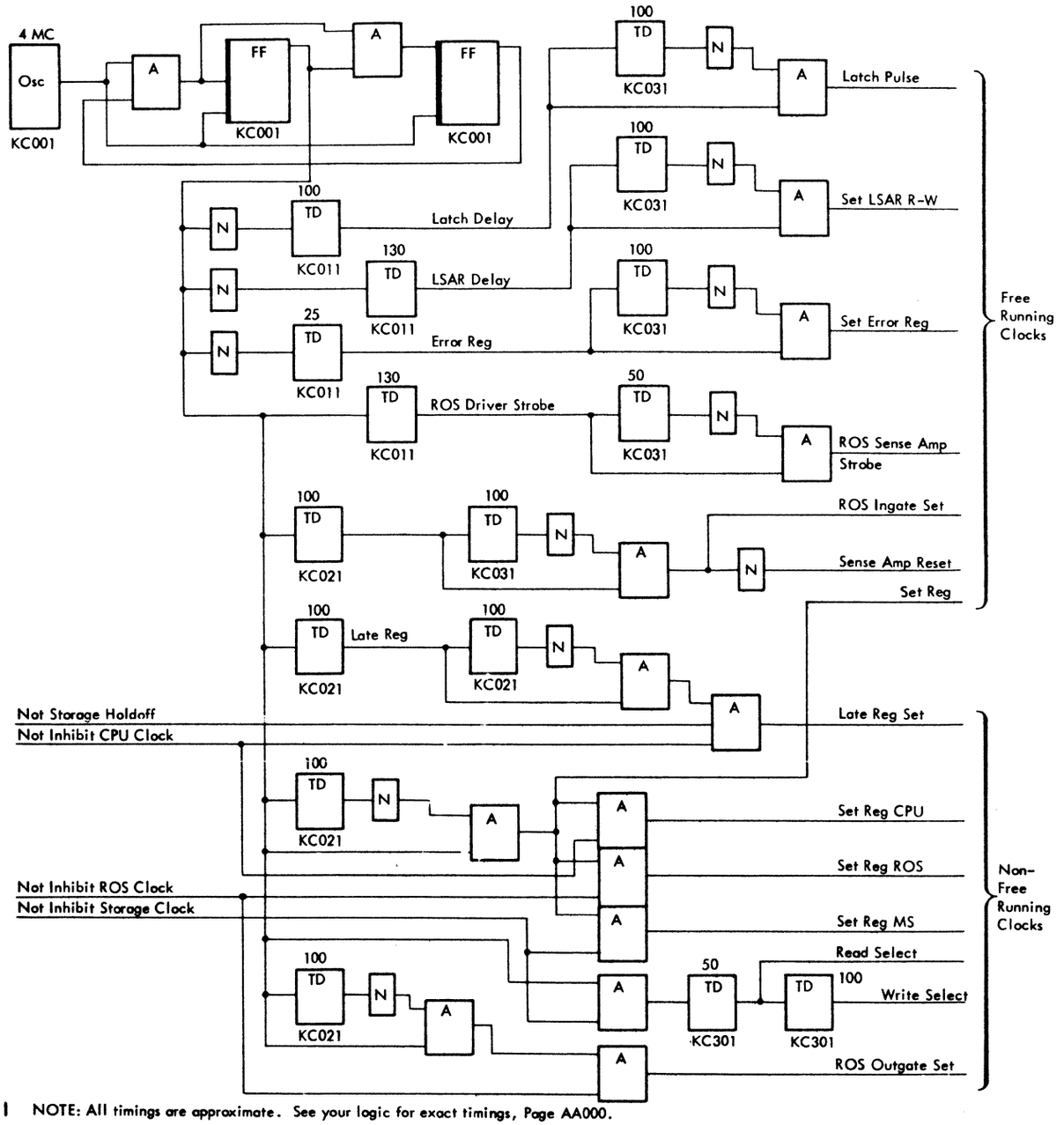


FIGURE 19. SUPERVISORY CONTROLS (PART 2 OF 2)



NOTE: All timings are approximate. See your logic for exact timings, Page AA000.

FIGURE 20. CLOCK DISTRIBUTION

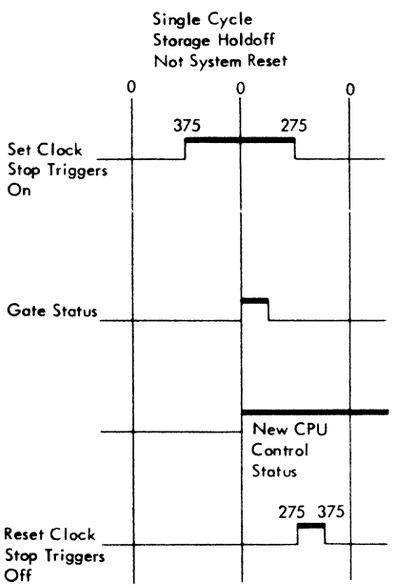


FIGURE 21. CHANGING CPU CONTROL STATUS

only as a result of an interrupt on the input interface of the supervisory controls. The three types of supervisory control interrupts and their causes are:

1. Error interrupt -- Parity check with PSW(13) on.
2. Normal interrupt -- System reset, FLT load request, storage test switches, FLT's request CPU mode change, or logout operation request CPU mode change.
3. Clock interrupt -- Storage holdoff or single-cycle operation.

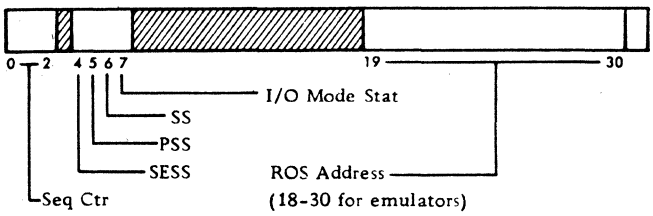
Error Interrupt: An error interrupt is the result of a parity check. The parity check causes all three clock stop triggers to be set on, thus stopping all gated (non free-running) clocks. The parity check also turns on the error interrupt trigger. In parallel with the interrupts, the status of various manual switches, CPU controls, and the type of error are used to set the CPU mode request triggers (Figure 19). At the end of the error detection cycle, the error interrupt trigger signifies that an error has occurred, and the CPU mode request triggers indicate the action to be taken. At the beginning of the next cycle (the first cycle that the clocks are stopped), the CPU mode request triggers are gated to the CPU mode triggers, thus producing a new CPU control mode on the output interface.

Normal Interrupt: A normal interrupt is the result of a manual control operation or a request for a change of CPU control modes. These requests show themselves at the input interface of the supervisory controls where they cause all three clock stop triggers and the normal interrupt trigger to be set on. The CPU mode request triggers are also set on at this time. As in an error interrupt, the CPU mode triggers are gated at the start of the next cycle.

Clock Interrupt: A clock interrupt is the result of a storage holdoff or a single-cycle operation. Clock interrupts cause all three clock stop triggers to be turned on. The error or normal interrupt triggers are not turned on and the CPU control mode triggers are not gated as in error or normal interrupt. This allows the clocks to be controlled without changing the control mode of the CPU.

Pushbuttons That Force ROAR: Figure 19 shows the CE panel pushbuttons that can force a hardware address into ROAR. The address forced is determined by the individual pushbutton whose function is then executed. Many other pushbuttons on the console cause ROS to cycle but do not directly force an address into ROAR.

LINKAGE CONTROL WORD



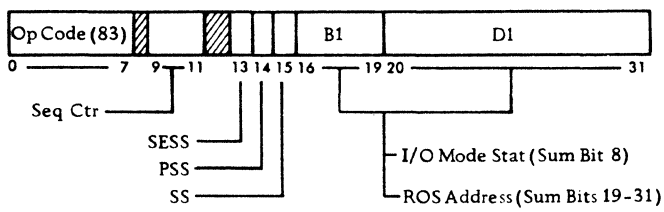
The linkage control word (LCW) contains information used in setting certain controls and ROAR for maintenance operations in ROS mode. The LCW must be put in the storage data register (SDR) before it can be used. This is accomplished by one of two methods; it is assembled in SDR by the diagnose instruction, or read into the SDR from main storage. With the linkage control word in the SDR, the following items can be set:

1. SDR(0-2) to sequence counter (Seq Ctr)
2. SDR(4) to supervisory enable storage stat (SESS)
3. SDR(5) to progressive scan stat (PSS)
4. SDR(6) to supervisory stat (SS)
5. SDR(7) to I/O mode stat
6. SDR(19-30) to read only storage address register (ROAR)

Items 1-4 (Seq Ctr, SESS, PSS, and SS) are set by microorder E → SCANCTL in combination with EMIT 1000. Item 6 (ROAR) is set by the microorder D → ROAR, SCAN.

Item 5 (I/O mode stat) is set by the microorder 1 → IOMODE. This is all accomplished by the execute LCW kernel in ROS (QY110) -- two microinstructions immediately following diagnose instruction, or the fetch LCW kernel.

DIAGNOSE INSTRUCTION



The diagnose instruction provides an exit from a normal operation (System/360 instructions) to a maintenance operation. This is accomplished by assembling a linkage control word (LCW) in the SDR,

storing it (LCW) in hex address 80, and then entering the execute LCW kernel in ROS (Figure 15).

Maintenance operations initiated by the diagnose instruction may be divided into two main catagories as follows:

1. Execution of special kernels (maintenance routines) in ROS (Figure 14). ROS mode FLT's and Progressive Scan make extensive use of some of these kernels.

2. Execution of any microinstruction, or subset of microinstructions, in any desired order. This procedure may be used to examine any specific area in ROS. See Figure 22 for examples.

The diagnose instruction must be located on a fullword boundary in main storage if additional LCW's are to be used. When other LCW's (in addition to the one built by diagnose) are desired, they must be located in main storage starting at the fullword address immediately following the diagnose instruction. Because IAR is used to count up and scan-out subsequent LCW's, any control logic function or malfunction that affects IAR content affects the sequence of the stream of LCW's.

Diagnose is initiated and decoded in I-fetch like all other System/360 instructions. When a controlling LCW contains the address of the entry to I-fetch kernel (FB9), normal operations (System/360 instructions) will be resumed.

FAULT LOCATING TESTS (FLT's)

Fault locating tests (FLT's) are a series of semi-automatic diagnostic tests that contain fault locating abilities. The fault location ability of FLT's is an additional step beyond the fault detection ability of most diagnostic programs. After detecting a failure, FLT's point to the probable cause(s) of the failure through the use of a scoping index called Scopex. FLT's and their supporting documentation are produced by computer programs that operate on data extracted from the design automation logic master tape.

Main Storage Location	Program Words	Function
WWW	83020F2A	Load L and R Regs (via scan-in kernel)
	YYYYYYYY	Bump Address Each Byte
	ZZZZZZZZ	Specified Data
	0400XXXX	Store Data in Bump
	0000XXXX	Read Data from Bump
	00001F72	Exit to I-Fetch
	47F00WWW	Branch On Condition Back to Beginning
XXXX	Bump Word 00 Use 1F6A	
	Bump Word 01 Use 1E6A	
	Bump Word 10 Use 1F68	
	Bump Word 11 Use 1E68	

LCW's

FIGURE 22. DIAGNOSE USAGE (SCOPE BUMP WORD)

The actual FLT's for the Model 50 are the ROS mode zero and one-cycle tests. Various areas (controls, registers, and circuits, etc.) must be operating correctly before these cycle tests can be run. Most of these areas (defined as hardcore) are checked out first in the hardcore tests. In addition, all of read only storage (ROS) is tested for addressing and content by the ROS bit tests. All tests for the preceding items are contained on the Model 50 FLT tapes (Figure 23). These tests (hardcore, ROS bit, and FLT's) are also available on disk packs. See Figure 24.

Main Store Mode Tape

A) MS Mode Hardcore Tests:

1. Binary trigger: reset off.
2. Address first 4096 words of MS.
3. Binary trigger: step on and off.
4. All ROAR bits.
5. ROS group readout.
6. ROS parity check circuits.

B) MS Mode ROS Bit Tests:

1. All ROS words for addressing and content.

ROS Mode Tape

A) ROS Mode Hardcore Tests:

1. Switch from MS mode to ROS mode.
2. Test the following:
   Progressive scan stat (via ROS scan-in kernel),
   supervisory stat, sequence counter,
   supervisory enable storage stat,
   log trigger, pass trigger, fail trigger, scan test counter, microorder HA→A, ROS scan-out kernel, zero-cycle pass test, and zero-cycle fail test.
3. Reset I/O interface register.

B) ROS Mode Cycle Tests (FLT's):

1. Zero-cycle tests; all storage elements for which scan-in (via adder out bus or emit field) and scan-out paths exist.
2. One-cycle tests as follows:
   Seg 1: L, F, Q, I/O, carry stat, PSW (32-39), and MVFR.
   Seg 2: R, H, GP stats, and half sum.
   Seg 3: M, G1, G2, J, L sign, R Sign, 1 syllable op, refetch, and error (U, V).
   Seg 4: Full sum, carry, and mover-out errors (2 cycle tests).
   Seg 5: LSAR and LSFR.
   Seg 6: ROAR (2 cycle tests).
   Seg 7: LB, MB, MD, G1, G2, error checks, and LB-MB parity check.

FIGURE 23. FLT TAPES: MODEL 50

Disk Pack 1
MS Mode Hardcore Tests
MS Mode ROS Bit Tests
(ROS Planes 0-5)

Disk Pack 2
MS Mode ROS Bit Tests
(ROS Planes 6-B)

Disk Pack 3
MS Mode ROS Bit Tests
(ROS Planes C-F)

Disk Pack 4
ROS Mode Hardcore Tests
ROS Mode Cycle Tests (FLT's)

FIGURE 24. FLT DISK PACKS: MODEL 50

The FLT technique involves the use of test patterns. These (FLT) test patterns are designed to prove that each trigger can be turned on and off and that each transistor in the combinatorial logic connecting triggers can be controlled by each of its inputs.

Each diagnostic test forces the system to the state specified by a particular test pattern. This process, called scan-in, sets the selected triggers to the predetermined values of the test pattern in core storage. The system is then forced to respond to the scan-in values by allowing its clock to operate a specified number of cycles. This process, called clock advance, exercises the combinatorial logic between triggers and places the system in a new internal state. This new internal state is called the actual response. The actual response is then made available for analysis through a process known as scan-out, which stores the actual response pattern into core storage. Next, the actual response is read from storage into the SDR, OR'ed there with a mask word from storage, and then the OR'ed result is tested. Following this, a second test is made with an expected response. The result of these two tests indicates whether the individual circuit under test functioned properly or not. This logical comparison, and a branch on the result, is called FLT compare and branch.

To run FLT's, additional paths to the storage data register (SDR) are used. These new (scan) paths allow the internal status of the CPU and channels to be logged (or scanned-out) to storage. FLT op codes initiating scan-out operations are denoted by an asterisk (*) on Figure 10. A simplified diagram of the scan-out logic is shown on Figure 13.

FLT LOAD

An alternate method of loading FLT's into main storage is required because the normal IPL sequencing is under ROS control and uses CPU and common channel hardware. To achieve an alternate method, additional hardcore controls and a new data path direct to main storage have been provided. A sequence counter and four sequence stats execute the load operation by controlling a selector channel clock, the same selector channel (B register) gating to SDR, the instruction address register (IAR), and the storage data register (SDR).

The main purpose of this alternate (FLT) load method is to store FLT programs in main storage even though the common channel or ROS may not be working correctly. Another reason is to allow either good or bad parity to be loaded into storage. Arbitrary bit patterns, without regard to parity, can be loaded in this way.

An FLT load can be accomplished from tapes or disk packs on a selector channel. See Figures 25 and 26. Data enter storage via the B register of the selector channel, the scan-out/logout logic, and thence over the scan bus into the SDR (Figure 13). Checking is performed in the channel and again in CPU before the data enter storage. Every two consecutive words on tape (or disk) are OR'ed together to produce one word in storage. All 36 positions of this word are the result of the OR'ing mechanism; that is, the 32 data positions are the OR'ed result of the data positions of two words on tape (or disk), and the four parity-bit positions are the OR'ed result of the parity generator output for each of those two words. This OR'ing mechanism allows bad parity to be loaded into storage. The FLT record in storage starts at location zero. There is no check for record length; however, the controls will hang up if the channel does not receive an even number of words.

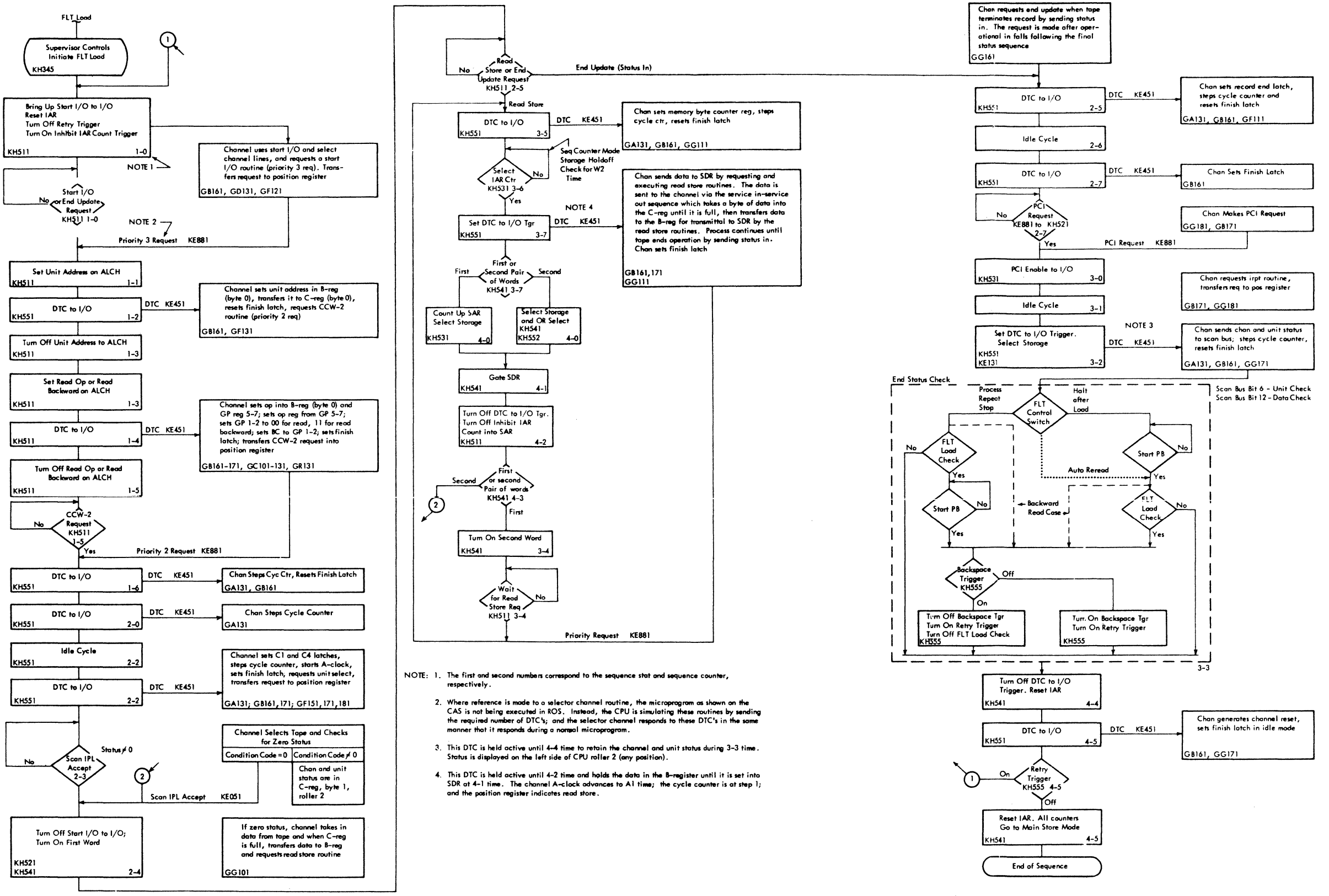
To convert two words on tape or disk into a single word in storage, the channel sends a read store request which causes a write storage cycle using the current IAR address. If reading an odd word (the first of each pair) from tape or disk, the IAR counter is incremented by four (IAR + 4 = full-word step), storage is selected, and the word from the B register is stored at that address. When the next (even) word is to be stored, the IAR counter is not incremented, the previously stored word (first of the pair) is read out, OR'ed in the SDR with the even word from the B register, and is then written back into main storage.

An FLT load can be initiated from the system control panel but not from a remote operator control panel. It can also be initiated by the diagnose instruction via the execute LCW kernel and the FLT load call kernel in ROS, or while performing a maintenance operation, in either main store or ROS mode, by inserting op code A in the FLT op register.

When loading FLT's from the system control panel, the unit to be started is specified by the channel and unit rotary switches (load unit switches) on the system control panel. If a channel other than a selector channel, or a device other than a tape drive or disk is specified, the FLT load will not perform, and the FLT controls will hang up.

Load From Tape

To initiate a FLT load from tape via the system control panel, the FLT mode switch is placed in the load position, the system reset PB is depressed, and then the load PB is depressed. (System reset does not occur automatically as in normal IPL and must be performed manually.) The FLT load from tape resets the IAR to zero, sets the sequence counter mode trigger on, and simulates a start I/O operation with a read data command.



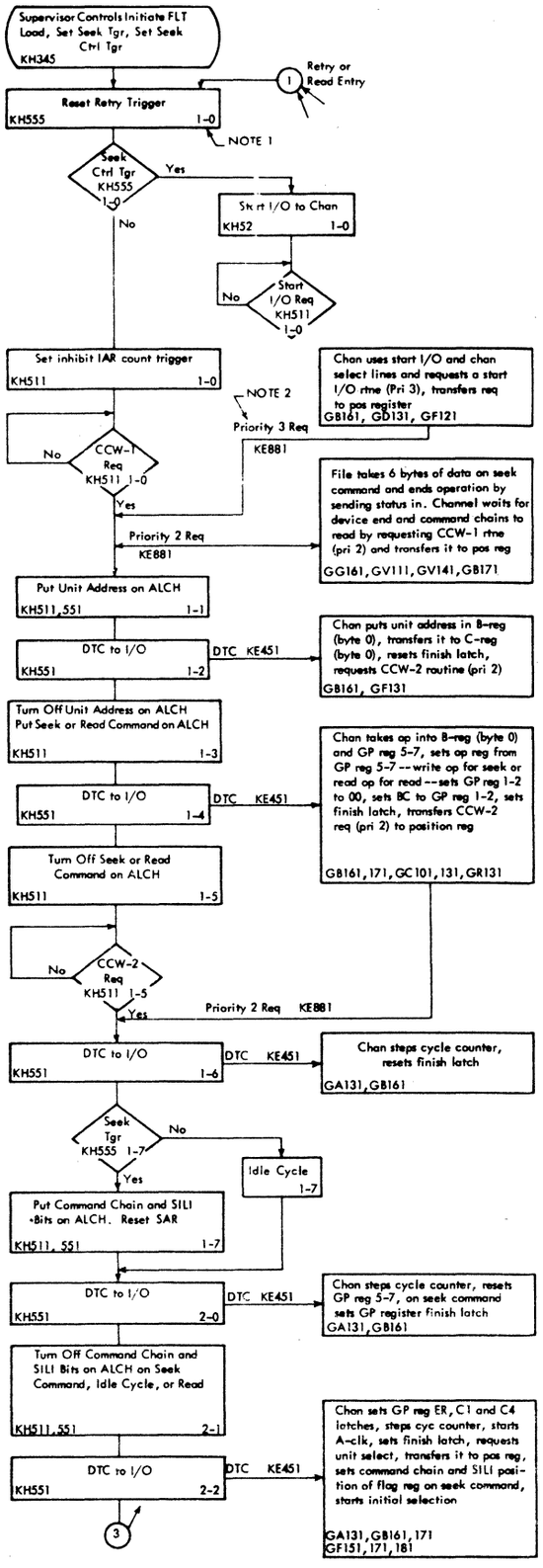
NOTE: 1. The first and second numbers correspond to the sequence stat and sequence counter, respectively.

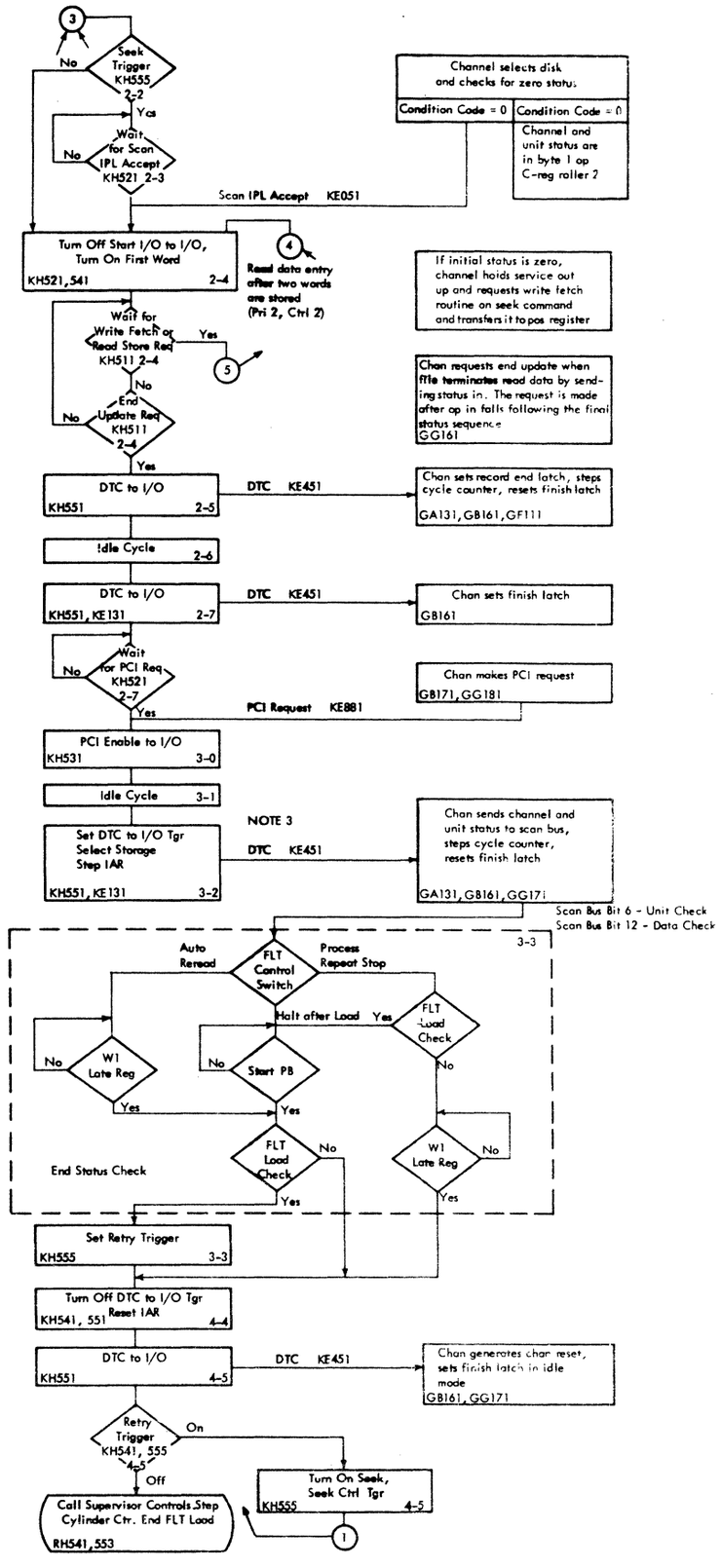
2. Where reference is made to a selector channel routine, the microprogram as shown on the CAS is not being executed in ROS. Instead, the CPU is simulating these routines by sending the required number of DTC's; and the selector channel responds to these DTC's in the same manner that it responds during a normal microprogram.

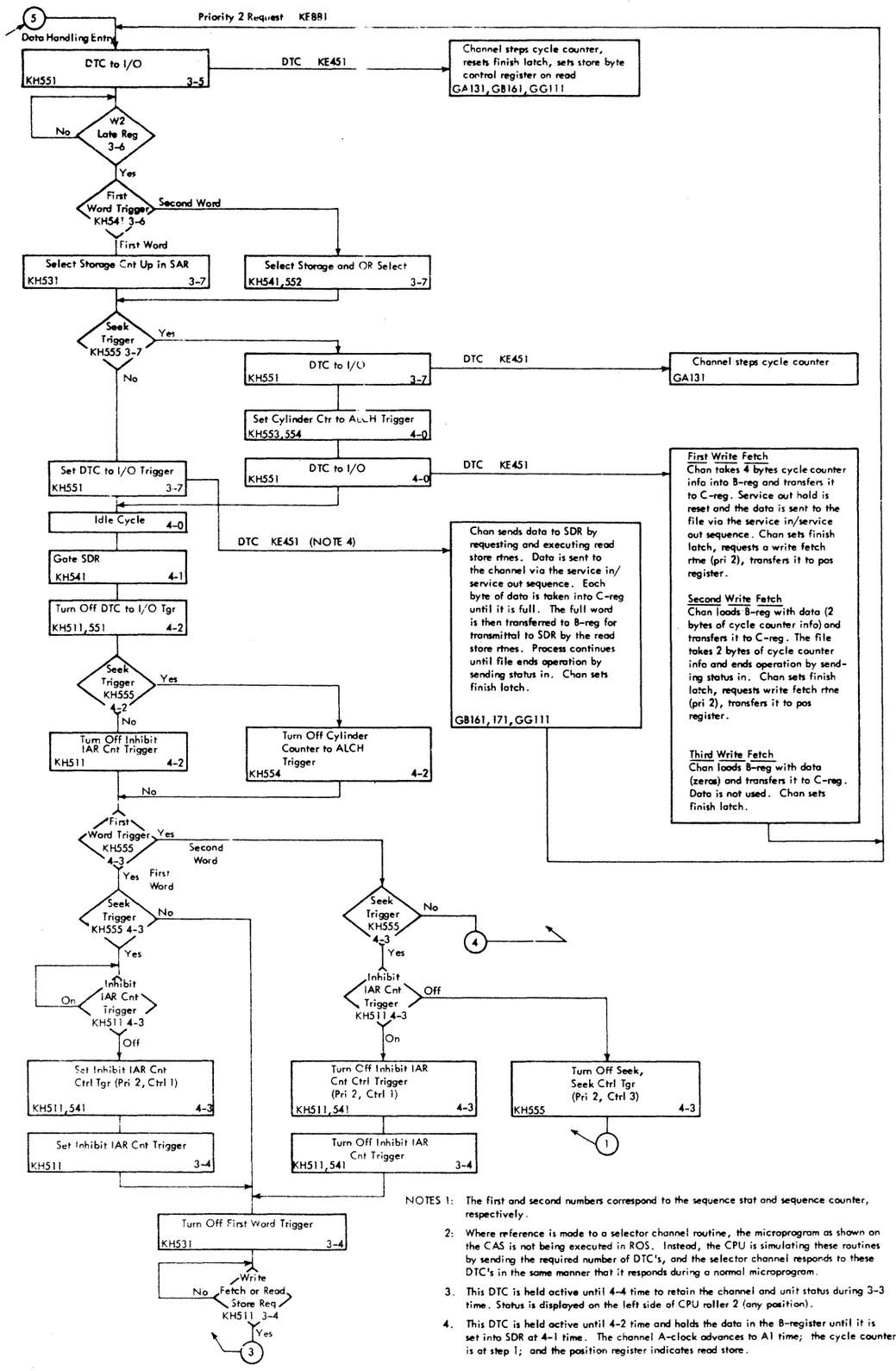
3. This DTC is held active until 4-4 time to retain the channel and unit status during 3-3 time. Status is displayed on the left side of CPU roller 2 (any position).

4. This DTC is held active until 4-2 time and holds the data in the B-register until it is set into SDR at 4-1 time. The channel A-clock advances to A1 time; the cycle counter is at step 1; and the position register indicates read store.

FIGURE 25. FLT LOAD VIA TAPE







NOTES 1: The first and second numbers correspond to the sequence stat and sequence counter, respectively.

2: Where reference is made to a selector channel routine, the microprogram as shown on the CAS is not being executed in ROS. Instead, the CPU is simulating these routines by sending the required number of DTC's, and the selector channel responds to these DTC's in the same manner that it responds during a normal microprogram.

3. This DTC is held active until 4-4 time to retain the channel and unit status during 3-3 time. Status is displayed on the left side of CPU roller 2 (any position).

4. This DTC is held active until 4-2 time and holds the data in the B-register until it is set into SDR at 4-1 time. The channel A-clock advances to A1 time; the cycle counter is at step 1; and the position register indicates read store.

FIGURE 26. FLT LOAD VIA DISK

Load From Disk

When loading FLT's from disk, the procedure is slightly different. First the FLT mode switch is set to the off position and the system reset PB is depressed, thus setting the cylinder counter (KH553-554) to zero. The FLT mode switch is then set in the load position and the load PB is depressed. The FLT load from disk resets the IAR to zero, sets the sequence counter mode trigger on, and simulates a start I/O operation with a control seek command. The control seek command initiates a series of three write fetch priority 2 requests (priority 2, control 1-3). The disk unit terminates the operation after accepting six bytes of seek data. As a read data command is command-chained to the control seek command, the FLT controls wait for a fourth priority 2 request (CCW1). When this CCW1 arrives, the read data command takes over control and the system proceeds to read in data. If a unit check or a channel data check is sensed at the end of the control seek operation, command chaining is suppressed and the FLT controls hang up.

Unsuccessful Load

When loading FLT's from either tape or disk, and a parity check, unit check, or channel data check occurs during the read data operation, the FLT load check indicator turns on and loading continues to the end of the record. (A unit check or channel data check is shown on CPU roller 2, positions 6 and 12, respectively.) Next the CPU stops or attempts to reread the record, depending on the FLT control switch setting. The retry and backspace triggers in conjunction with the FLT control switch are used to control the rereading of a bad record received from tape.

A FLT load hangs up prior to completion if either the selector channel or the FLT load controls fail to operate correctly. Failures of this type are diagnosable from the sequence stat and sequence counter indicators using Figure 25 or 26.

Completion of Successful Load

At the completion of a successful FLT load, the supervisory controls are set to main store mode, and execution starts at location four. (Locations zero through three are used for record identification.) Main store mode hardcore tests and the ROS bit tests are executed in this (main store) mode. When the ROS mode hardcore or cycle tests are to be executed, op code 06 (in the FLT op reg) will put the CPU in ROS mode.

The following sequence of words at the beginning of each FLT record in storage is used to initiate the ROS mode cycle tests.

Word	Location	Operation	Format
1	0-3	Identification	0-3 Machine type (Mod 50 = A) 4-7 Type of test 5 = Zero-cycle test 6 = One-cycle test 8-11 Zeros 12-15 Segment number 16-27 EC Level 28-31 Undefined
2	4-7	SDR to ROAR and reset binary trigger	F0B (hex) in bits 19-30 0111 in parity bits (MS mode)
3	8-11	Call for ROS mode	0110 in parity bits (MS mode)
4	12-15	Turn on ignore error trigger	F3A (hex) in bits 19-30; ones in bits 2, 5, and 6; zeros elsewhere
5	16-19	Reset pass/fail triggers	F44 (hex) in bits 19-30; zeros elsewhere
6	20-23	Reset binary trigger and error register, branch to first test	Address of first test in bits 8-31

The first word in this sequence is not used. (Location zero is never accessed.) The second word, which is executed from storage locations 4-7, forces the entry address of the fetch LCW kernel into ROAR. Thus when the third word causes ROS mode control, the fetch LCW kernel is executed. Words 4-6 are then executed in sequence under ROS control. Word 6 allows branching to any starting address and contains the location of the first word of scan-in data. Normal FLT execution is now in effect.

MAIN STORE MODE FLT's

Main store mode FLT's consist of hardcore tests and tests for checking out ROS. These tests are on a tape separate from ROS mode FLT's and are normally run first. They are the first step in a "bootstrap" checkout procedure aimed at exercising hardware and validating its operation before using it to control the checkout of other hardware. These tests are loaded via an FLT load operation. Main store mode tests may be terminated by:

1. A system reset
2. A call for FLT load (op code 0A)
3. A request for ROS mode (op code 06)

MS Mode Hardcore Tests

The main store mode hardcore tests consist of the following:

1. A test to reset the binary trigger.
2. A test of the first 4,096 words in main storage. This tests the ability to read into and out of main storage through use of a series of branches.
3. A test of the binary trigger. This tests the ability of the binary trigger to be stepped on and off.
4. A test of the read only address register (ROAR). This tests the ability of the ROAR bits to be turned on and off, one by one.
5. A test of the ROS group-readout op codes. This tests the ability to read a word from ROS and select the proper group.
6. A test of ROS parity check circuits.

Testing is resumed following a halt by pressing the start key. If all tests pass, the following halt occurs:

P	P	P	P
1FF	0FF	1FF	1FF

The tests comprise three FLT records; the first resets the binary trigger, the second is the main storage test, and the third contains the rest of the tests. Records two and three are automatically called by using the "request for FLT load" (op code 0A).

FLT Load Checking Program

The following program can be used to generate a tape of 30-byte (hex) records (48 decimal) used to check the FLT load circuits. Loading the 30-byte (hex) records (48 decimal) with FLT load is a good check of the FLT load circuits.

Tape Generate Program

This program will write a series of 30-byte (hex) records (48 decimal) on 9-track tape or on 7-track tape with data convert.

Location	Data	
0000	*0 00 00 00	*Enable channel to be used
0004	00 00 03 00	
0048	00 00 04 00	CAW
0078	*0 00 00 00	*Enable channel to be used
007C	00 00 03 00	
0300	9C 00 0* 80	SIO *channel used
0304	47 F0 03 04	branch
0400	01 00 06 00	CCW
0404	20 00 00 30	30-byte (hex) count (48 decimal)

Location	Data	
0600	80 80 80 80	This 12-word record is written on tape and is read in as the 6-word record in step 4, when the FLT load ORs a pair of tape words into one word to load into storage.
0604	80 80 80 80	
0608	00 00 00 00	
060C	00 00 00 00	
0610	AA AA AA AA	
0614	55 55 55 55	
0618	FF 00 FF 00	
061C	00 FF 00 FF	
0620	F0 80 F0 80	
0624	0F 80 0F 80	
0628	80 80 80 80	
062C	80 80 80 80	

Loading the Test Program

1. Mount the tape of continuous records that you generated.
2. Set FLT mode switch to LOAD.
3. Set FLT control switch to HALT AFTER LOAD LOAD.
4. Set load unit controls and depress LOAD button.

The first and second words on tape are OR'ed and loaded into the first word location in main storage; the third and fourth words on tape are OR'ed and loaded into the second word location in main storage, and so on, until the first six word locations of main storage are loaded with the twelve words of the record on tape. The six main storage locations should be:

Location	Data	Parity Bits	Operation
0000	80 80 80 80	0	No Op
0004	00 00 00 00	F	Test SDR Bin Tgr Off
0008	FF FF FF FF	F	Test SDR Bin Tgr On
000C	FF FF FF FF	F	Test SDR Bin Tgr Off
0010	FF 80 FF 80	A	Request FLT Load
0014	80 80 80 80	0	No Op

Test Methods (Mask and Expected Response)

The use of a mask and expected response is best explained using examples. Refer to Figure 27 in connection with the following description. In main store mode, FLT words are sent from storage locations into the SDR. The parity bits of these FLT words are then gated into FLT op reg (2-5). Note that there is absolutely no correlation between the parity bits and the data bytes of these FLT words. Note also that these parity bits may be OR'ed with parity bits already in the SDR (due to preceding op

Storage Location	SDR Data	FLT Op Reg (2-5)	Operation	SDR Byte 0	Comments
038	80001000	0111	SDR (19-30) to ROAR; reset bin trigger.	10000000	Set ROAR to 800; word from 038 in SDR.
03C	80008000	0101	ROAR to SDR (6-17) and OR with next word (mask) from storage.	10000000	Word from 03C in SDR.
					From ROAR (0).
----	02000000	----	----	00000010	Actual response in SDR.
040	FDFFFFFF	1111	Step bin trigger if SDR (OR'ed result) is all 1's.	11111101	Next storage word (mask) in SDR.
----	FFFFFFFF	----	----	11111111	OR'ed result in SDR.
044 Example 1	FFFFFFFF	1111	Step bin trigger if SDR (expected response) is all 1's.	11111111	Expected response in SDR.
054	80000000	0111	SDR (19-30) to ROAR; reset bin trigger.	10000000	Set ROAR to 000; word from 054 in SDR.
058	80008000	0101	ROAR to SDR (6-17) and OR with next word (mask) from storage.	10000000	Word from 058 in SDR.
					From ROAR (0).
----	00000000	----	----	00000000	Actual response in SDR.
05C	FDFFFFFF	1111	Step bin trigger if SDR (OR'ed result) is all 1's.	11111101	Next storage word (mask) in SDR.
----	FDFFFFFF	----	----	11111101	OR'ed result in SDR.
060 Example 2	FDFFFFFF	1111	Step bin trigger if SDR (expected response) is all 1's.	11111101	Expected response in SDR.

FIGURE 27. MASK AND EXPECTED RESPONSE EXAMPLES

code 01-05) before they are sent to the FLT op reg. When this OR'ing occurs, the entire word (data and parity bits) is OR'ed with the SDR contents. This OR'ed result remains in the SDR until replaced with new information. The FLT op reg contents determine what operation is to be performed.

Consider a main store mode hardcore test which sets ROAR(0) to a 1. The actual response, ROAR (0-11), is gated to SDR(6-17) and OR'ed with the mask word (0-31) which is all 1's except for bit position six. If ROAR(0) is actually set to a 1, the OR'ed result will be all 1's (Figure 27, Example 1).

If the test is for a reset of ROAR(0), the actual response will not have bit position six on (if successful). This actual response will be OR'ed with a mask of all 1's except for bit position six. If this OR'ed result is not all 1's when tested, the binary trigger will not be turned on. The second test, using the expected response, will not step the binary trigger as the expected response will not be all 1's (Figure 27, Example 2).

A successful test is achieved when the binary trigger is off after the testing of the expected result. Thus for a successful test, the binary trigger is stepped twice (Example 1) or not at all (Example 2).

MS Mode ROS Bit Tests

The main store mode ROS bit tests consist of a string of fault-detecting tests with one test for every ROS bit. Each test consists of a sequence of words in main storage. Test format is:

Word	Op	Function
1	07	SDR (19-30) to ROAR and reset binary trigger (18-30 for emulators).
2	01, 2, 3, 4	Selected ROSDR group to SDR and OR with next word (mask) from storage.
3	0F	Step binary trigger if SDR is all 1's. Mask in data field.
4	0F	Step binary trigger if SDR is all 1's. Expected response in data field.
5	0E	SDR (12-31) to IAR if binary trigger is off (causes branch to specified address + 4).
6	00	No-op (necessary to execute branch).
7	0B	Inhibit SAR clock (to loop on same word in SDR). Word address, expected response, and bit number in data field.
8	0A	Call for FLT load (last word of record).

Words 1-7 are repeated for every bit in the ROS word. Word 8 is the last word of the test record.

Word 2 causes a portion of the ROS data register (ROSDR) to be placed in SDR. Word 3 is a mask word and is OR'ed into SDR by inhibiting the normal SDR reset. This mask consists of 1's in all positions except for the bit position to be tested. The op portion of this word causes an all 1's test to be performed on the SDR. If the test is met, indicating that the bit being tested is a 1, the binary trigger is stepped.

Word 4, the expected response, is placed in SDR and the all 1's test is repeated. If this test is met, indicating that the expected bit is also a 1, the binary trigger is stepped again. If both the actual response bit and expected response bit are 1's, the trigger will have stepped twice and will be off. Similarly, if both bits are 0's, the trigger will be off. The trigger is on only if the actual response bit and expected response bit differ; therefore, it serves as the basis for a pass/fail decision.

Word 5 tests the binary trigger; if it is off, the program branches to the next test. If this conditional branch is not taken, indicating that the bit under test has not been read out correctly, word 7 is executed continuously by inhibiting the SAR clock. The effect is that of a diagnostic stop; the data portion of this word contains the address of the ROS word under test, and the bit in error. This information is displayed in the SDR. Figure 28 is a typical example of a ROS bit test.

Testing may be continued after a diagnostic stop by pressing the start pushbutton. When a fault exists, it normally causes many tests to fail. For example, a faulty sense amplifier indicates the same bit is incorrect in many unconnected words. By examining the addresses (both word and bit position) of every diagnostic stop, some measure of fault-localization is possible.

Running time for the test tape containing the ROS bit tests, and the hardcore tests preceding them, is approximately 3-4 minutes (on a good machine with no failures).

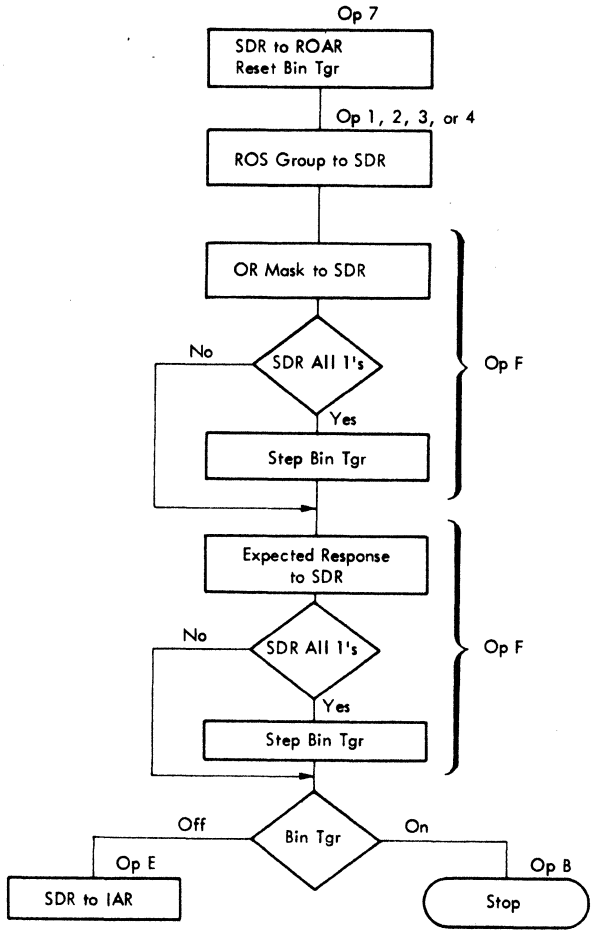


FIGURE 28. MS MODE ROS BIT TEST

ROS MODE FLT's

ROS mode FLT's are the second step in the "bootstrap" sequence begun with the main store mode FLT's. They are on the FLT ROS mode tape (or FLT disk pack 4) and are loaded with an FLT load. ROS mode FLT's are executed under microprogram control and assume a properly functioning ROS.

The ROS mode FLT's consist of hardcore tests, zero-cycle tests, and one-cycle tests.

ROS Mode Hardcore Tests

The ROS mode hardcore tests (Figure 23) check out the pass/fail triggers, control stats and counters, and the scan-in and scan-out kernels in ROS. The tests are executed via a series of linkage control words (LCW's) which exercise specific microprogram steps used by the FLT controls. Failures cause a halt or loop, and a listing must be consulted. These tests are placed first on the ROS mode FLT tape. See Figure 29 for a hardcore test sample.

NOTE: This is an actual ROS mode hardcore test, EC level 255452, for the progressive scan stat (PSS). This flowchart is for instructional purposes only, as future engineering changes may alter the method of testing.

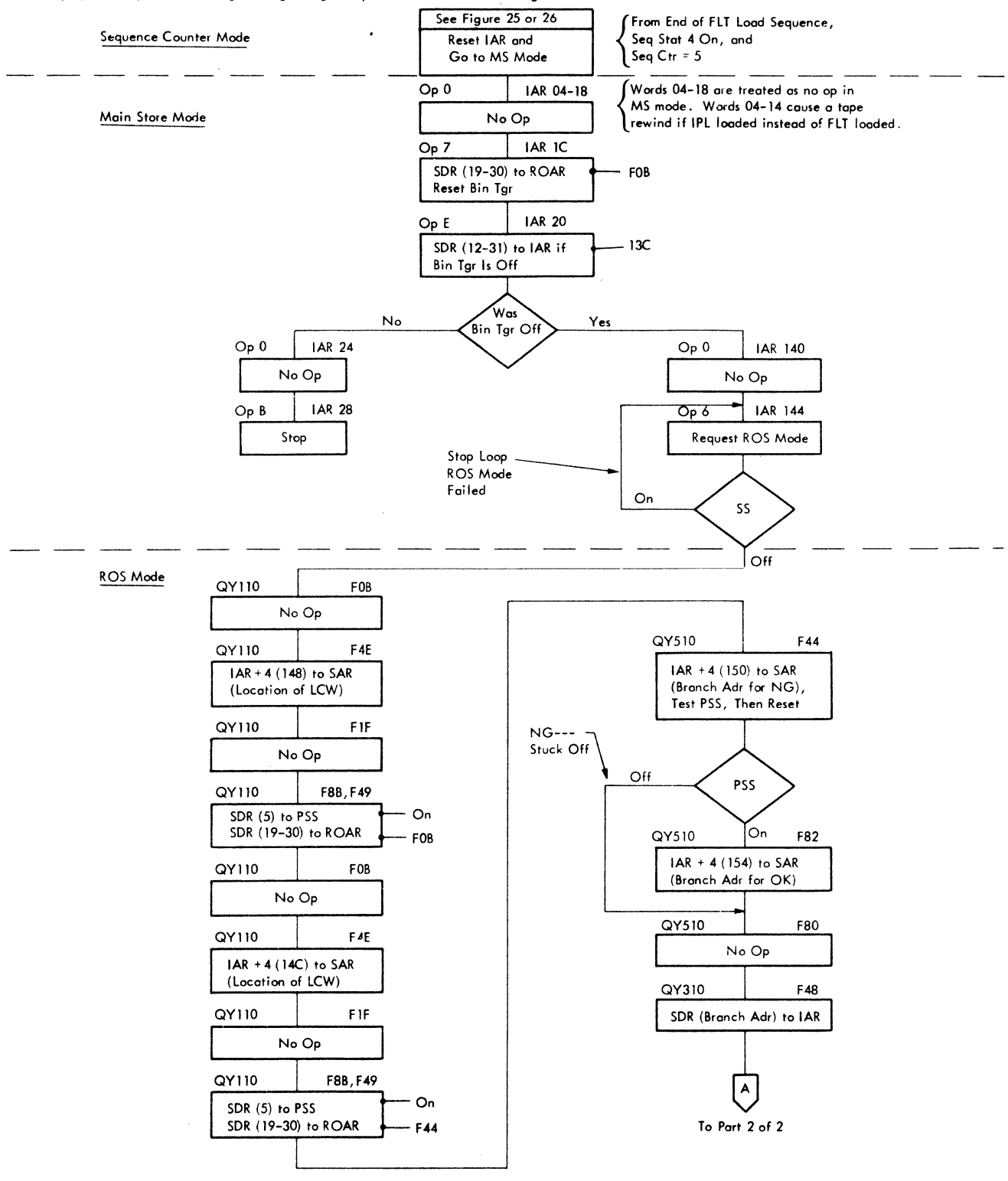


FIGURE 29. HARDCORE TEST SAMPLE: ROS MODE (PART 1 OF 2)

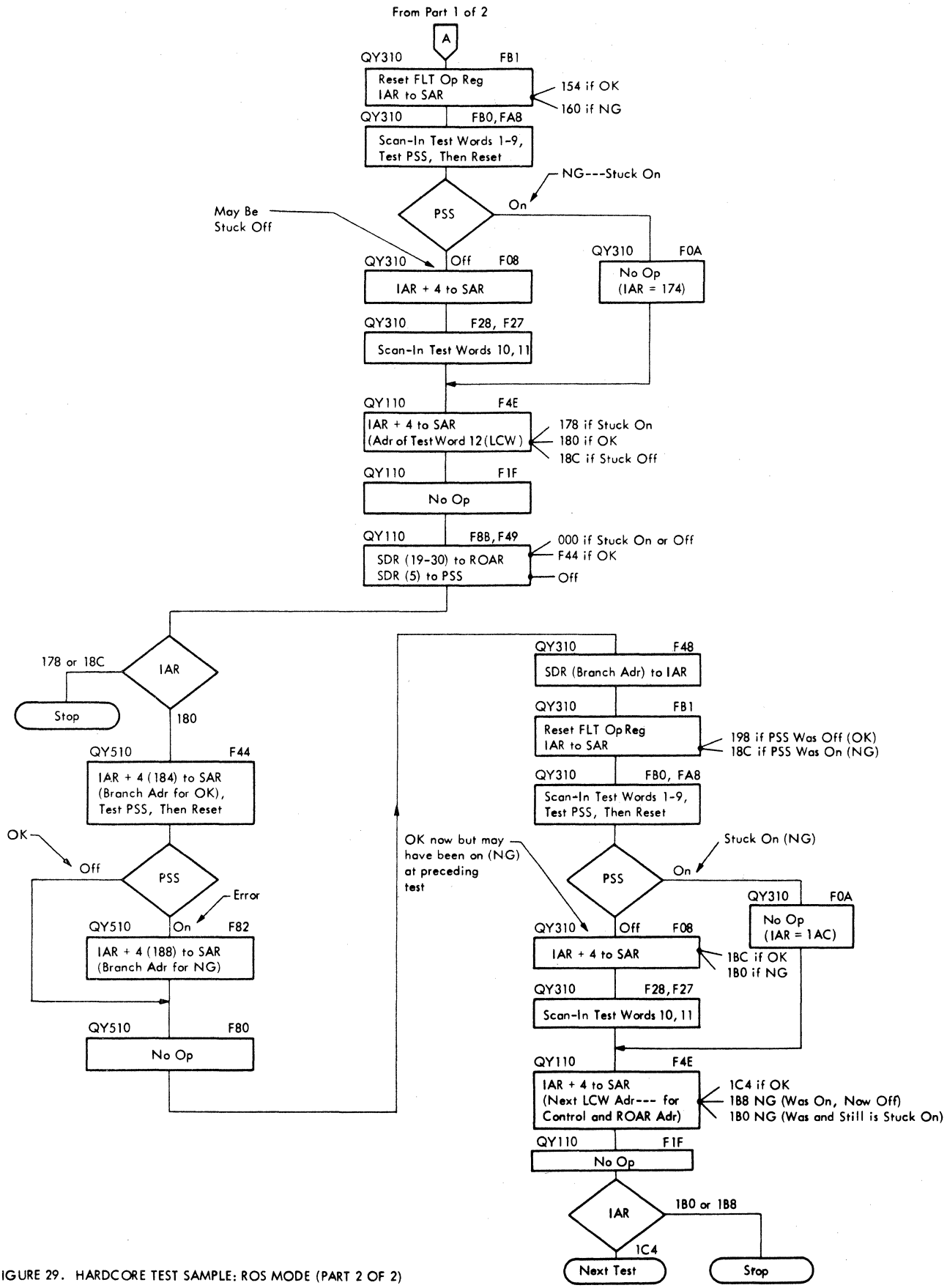


FIGURE 29. HARDCORE TEST SAMPLE: ROS MODE (PART 2 OF 2)

ROS Mode Zero/One-Cycle Tests

The zero-cycle tests are between the ROS mode hardcore and one-cycle tests. Zero-cycle tests insure that all triggers, for which scan-in paths (via adder out bus or emit field) and scan-out paths (via scan bus to SDR) are provided, can be set and reset.

The format and mode of execution is similar for both zero-cycle and one-cycle tests, however, documentation for these tests is different. A diagnostic index, containing a suspect card list, is provided for the zero-cycle tests. Only the index number displayed on termination and the function that the test was trying to perform are given.

One-cycle tests check the combinational logic between triggers. These tests follow the zero-cycle tests and are the last series of FLT's run. The successful running of all previous tests (on FLT tapes or FLT disk packs) assures that the controls and areas needed to run the one-cycle tests are functioning correctly. If a failure which should have been caught by hardcore or zero-cycle tests appears now, a wrong conclusion may be reached.

A scoping index (Scopex) is provided for the one-cycle tests. This index shows the logic that is sensitive for each individual test.

The one-cycle tests are divided into a series of segments. These segments test different areas of logic independently. Checking for intermittent failures is achieved by repeating each test 16 times before reaching a conclusion as to whether the test passed or failed. If the test both passes and fails, an intermittent failure has occurred.

Figure 30 shows the method used (via FLT load) to enter the ROS mode zero/one-cycle tests.

Zero/One-Cycle Test Methods

Each FLT cycle test uses its own individual test program consisting of 22 consecutive test words in storage. These cycle test programs are read into storage (via FLT load) from the FLT ROS mode tape or disk pack. There are approximately 181 cycle test programs on each tape record except for the last record of each segment which is variable. Figure 31 shows the word format of the cycle test programs. Figure 32 is a simplified flowchart of the FLT zero/one-cycle tests. ROS mode zero/one-cycle tests are performed as follows:

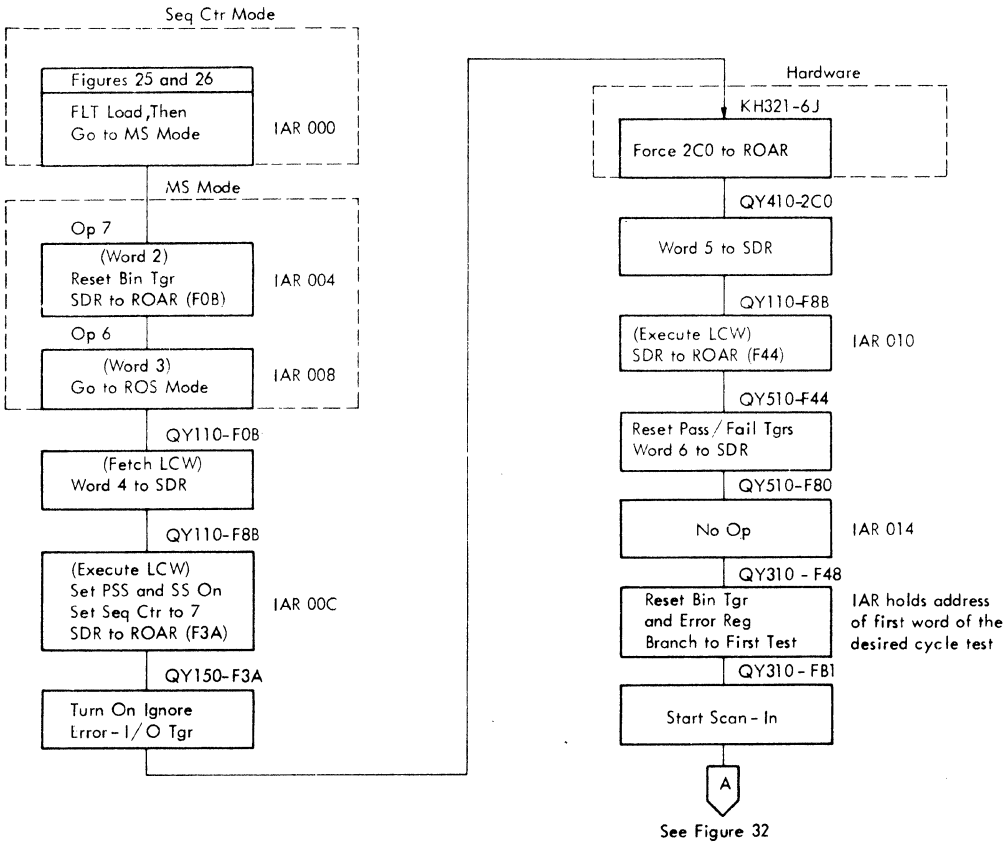


FIGURE 30. FLT LOAD TO CYCLE TESTS

ROS Kernel Using	Test Word	Bits	Function
Scan - In	1	0,1	PSW 32,33
		3,4	M byte ctr
		5 - 8	Length ctr # 2 (G2)
		12 - 15	J Reg
		16 - 19	MD ctr
		21 - 24	F Reg
		26 - 31	PSW 34 - 39
		P0 - P3	Byte Stats
	2	0,1	Sets carry stat if either bit is on
		8 - 11	Storage protect key (PSW 8 - 11)
		15 - 16	Syllable in op buffer stat is set to one if both bits equal zero
		23 - 30	PSW 0 - 7
		P0 - P3	General purpose stats 4 - 7
	3	0	L sign stat
		24 - 27	Length ctr # 1 (G1)
		31	Q Reg
		P1 - P3	CPU mover function reg
	4	0	R sign stat
		12 - 15	PSW 12 - 15
		P0 - P3	General purpose stats 0 - 3
	5	30 - 31	L byte ctr
		P2 - P3	Local store function reg
	6	30 - 31	I/O reg
		P3,P2,P1	I/O mover function reg
	7		M reg
	8		L reg
	9		R reg
	10		I/O interface reg
	11		H reg

ROS Kernel Using	Test Word	Bits	Function
Fetch/ Execute LCW	12	0 - 2	Sequence counter
		4	Supervisory enable storage stat
		5	Progressive scan stat
		6	Supervisory stat
		7	I/O mode stat
		19 - 30	ROAR (18 - 30 for emulators)
Scan - Out	13		Actual response address
	14		Mask address
FLT Compare and Branch	15		Mask
	16		Expected response (word to be tested)
	17		(X) Starting address this test (used 15 times)
	18		(X+1) Starting address next test (good test or start after checking failure)
	19		(X+2) Termination bit (7) and Scopex information
	20		(X+3) Starting address this test (restart after termination)
	21		(X+4) Starting address next test (forced pass after termination)
	22		Test number and segment number

FIGURE 31. FLT CYCLE TESTS: WORD FORMAT

Scan-In

The first 11 test words are used to place known values in various registers via the scan-in kernel. This kernel takes 11 consecutive words, addressed by the IAR, to perform the operation. It does nothing else to IAR except advance the address prior to reading the next word from storage.

Fetch/Execute LCW

At the completion of the scan-in sequence, test word 12 is read from storage into the SDR via the fetch LCW kernel. Word 12 is a linkage control word (LCW) whose contents are set into ROAR, the sequence counter, the supervisory stat (set on), the progressive scan and supervisory enable storage stats (set off), and the I/O mode stat (set according to SDR (7) of the 12th word). The LCW contents are set into the preceding items via the execute LCW kernel.

Clock Advance

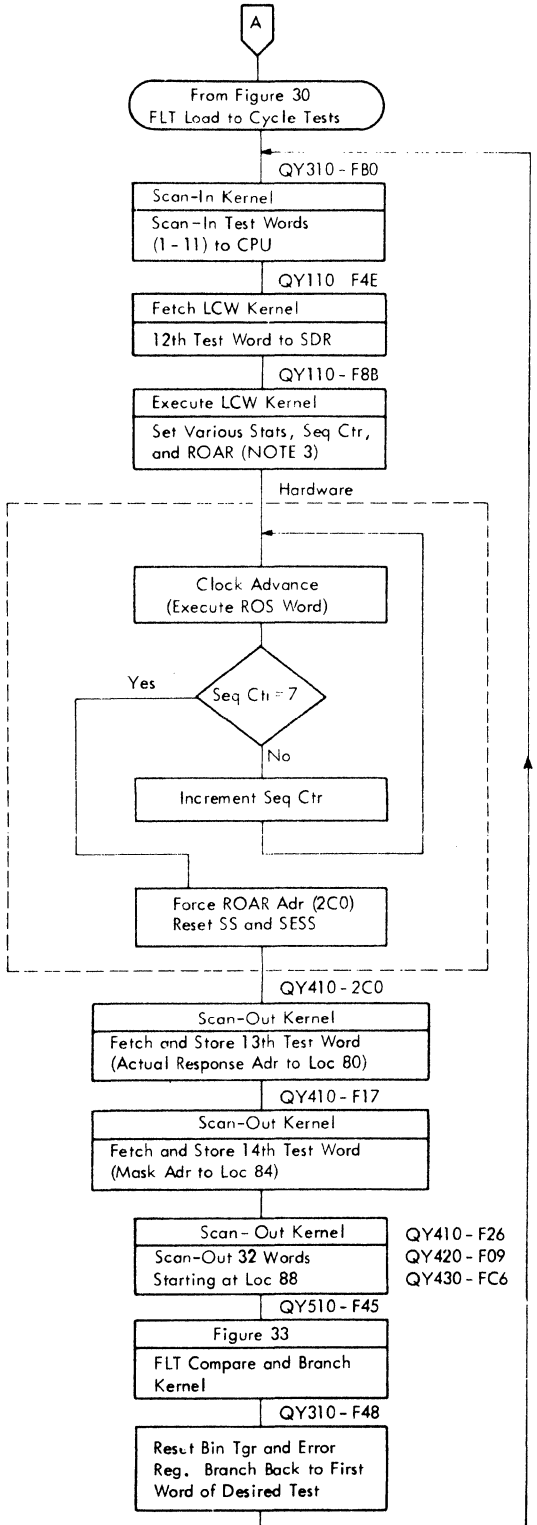
At this point ROS executes the ROS word specified by ROAR, and the sequence counter is stepped up by one. This operation is repeated until the sequence counter equals seven, which occurs after one or two cycles for the tests being described. When the sequence counter steps to seven, a hardware address (2C0) is forced into ROAR. This address is the beginning of the scan-out kernel.

Zero-Cycle: If the ROS word used during clock advance is 000, we have a zero-cycle test. When a trigger is being tested, three patterns are applied; the first and third reset the trigger, and the second sets it. A random pattern is applied to all other triggers while any particular trigger is being tested to help in the detection of noise and interference problems.

One-Cycle: The ROS word used in one-cycle tests allows a data transfer within CPU. This is normally accomplished in a single cycle except for two areas in which two cycles are needed (segments 4 and 6).

Scan-Out

The scan-out kernel stores test words 13 and 14 in hex address locations 80 and 84 for future use in the compare and branch kernel. Next, scan-out of the various registers and stats is begun. Contents of CPU registers and triggers (14 words) are stored



NOTES:
1. See Figure 15 for details on all kernels except the FLT compare and branch kernel (Figure 33).
2. See Figure 31 for word format of FLT cycle tests.
3. FLT's to date(EC level 255452)always set the SS--on, PSS--off, and the SESS--off.

FIGURE 32. FLT ZERO/ONE-CYCLE TESTS

in storage hex address 088-0BC. Channel status (17 words) is stored in hex addresses 0C0-104. See Figure 12 for details. When scan-out is complete, the compare and branch kernel is entered.

FLT Compare and Branch

The FLT compare and branch kernel compares the actual response with the expected response and sets the pass/fail triggers on the results. At the same time, the scan test counter is stepped up by one and a return to the beginning of the current test (scan-in) is made. This occurs 16 times except for the 16th pass which goes to the branch section of the kernel instead of returning to the beginning of the current test. See Figure 33, FLT Compare and Branch Kernel.

In the branch section of the kernel, both the pass and fail triggers are tested. The fail trigger will be on if the OR'ed result of the mask and actual response was different than the expected response for any of the 16 passes. The pass trigger will be on if the OR'ed result of the mask and actual response was the same as the expected response for any of the 16 passes. If a test both passes and fails during execution, the machine stops after the 16th pass with both the pass and fail triggers on, thus indicating an intermittent failure has occurred.

If both the pass and fail triggers are off at the end of the 16 passes, the machine stops. This condition indicates a failure in the checking circuits with a return to the ROS mode hardcore tests advisable. Pressing the start PB on this stop will force a pass to the next test even though the FLT mode switch is not on the force pass position.

FLT OPERATING/REPAIR PROCEDURES

This section contains the operating and repair procedures for running FLT's from tape or disk. Note that the main storage ripple test is always performed before attempting to run FLT's. For convenience, the operating procedures for tape and disk are separated. As repair procedures are the same for both tape-and disk-originating FLT's, no distinction is made between the two.

Figure 34 shows the FLT run and repair procedures for main store mode and ROS mode tests. Figure 35 is a cycle test repair procedure.

FLT's are run in the following sequence only after the main storage ripple test has been run successfully:

1. Main store mode hardcore tests
2. Main store mode ROS bit tests
3. ROS mode hardcore tests
4. ROS mode cycle tests

Note: Disable ROS retry by jumpering 01C-E3C4D11 to a D08 pin before running or biasing FLT's, diagnostics, or progressive scan.

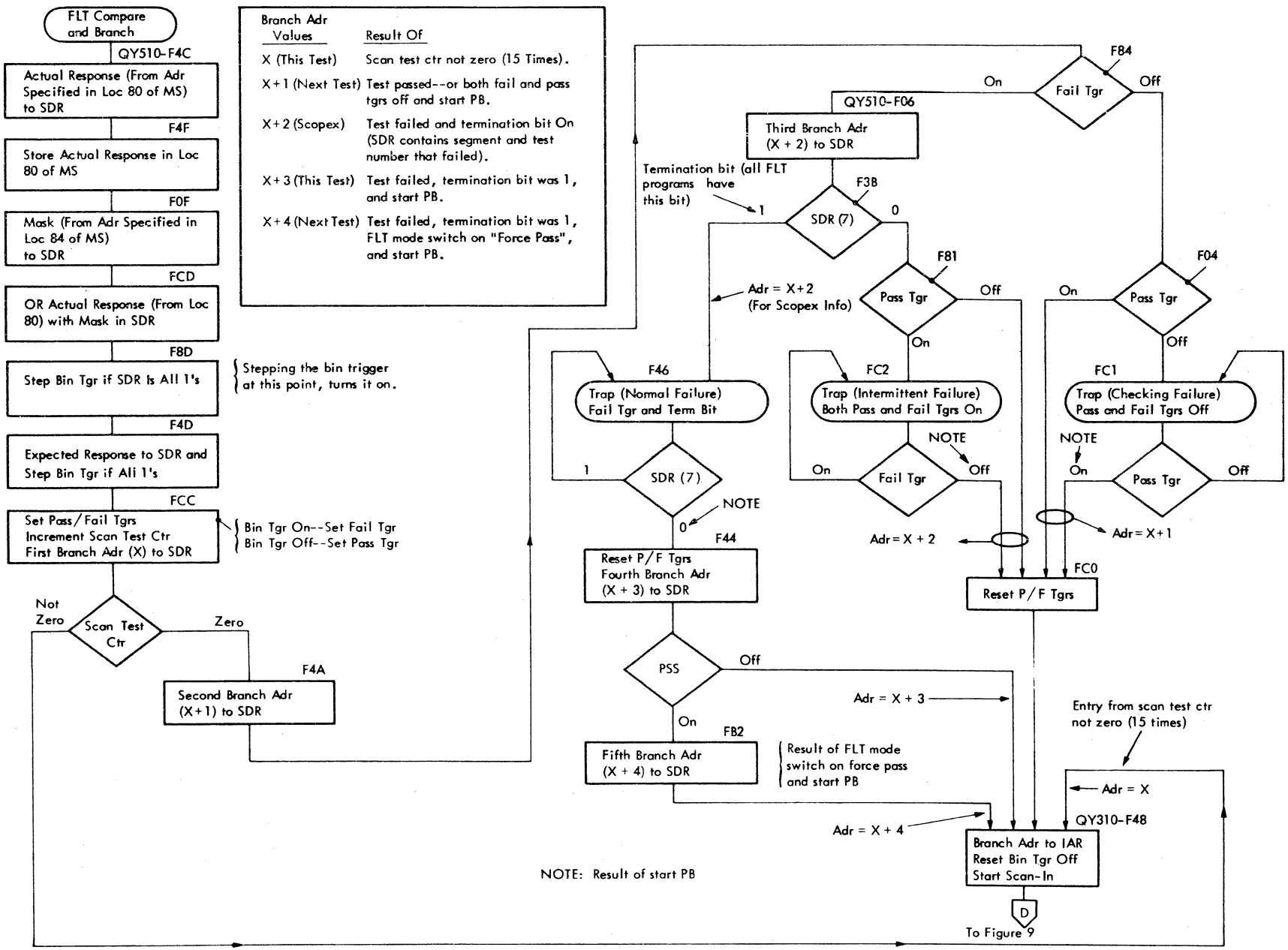
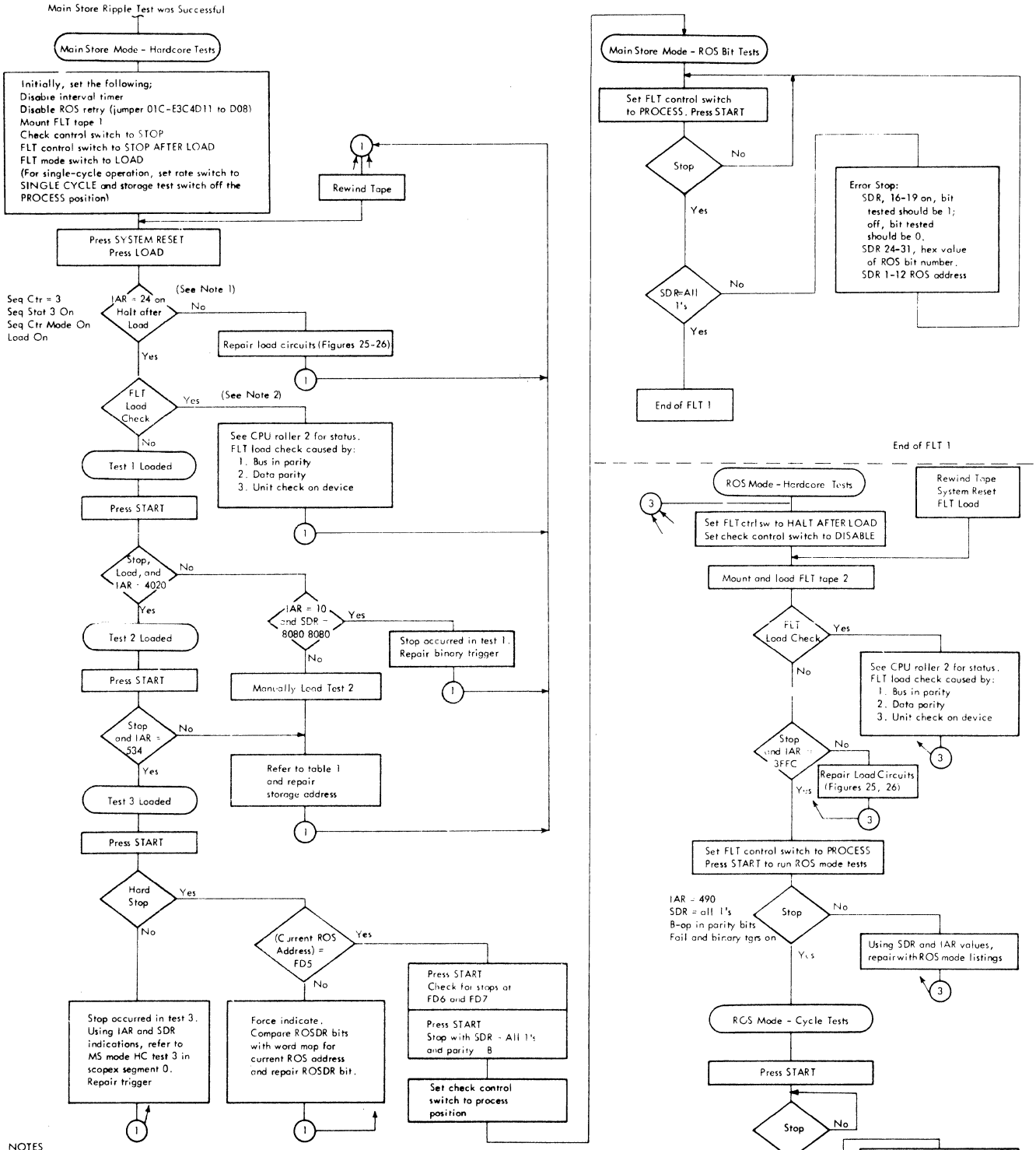


FIGURE 33. FLT COMPARE AND BRANCH KERNEL



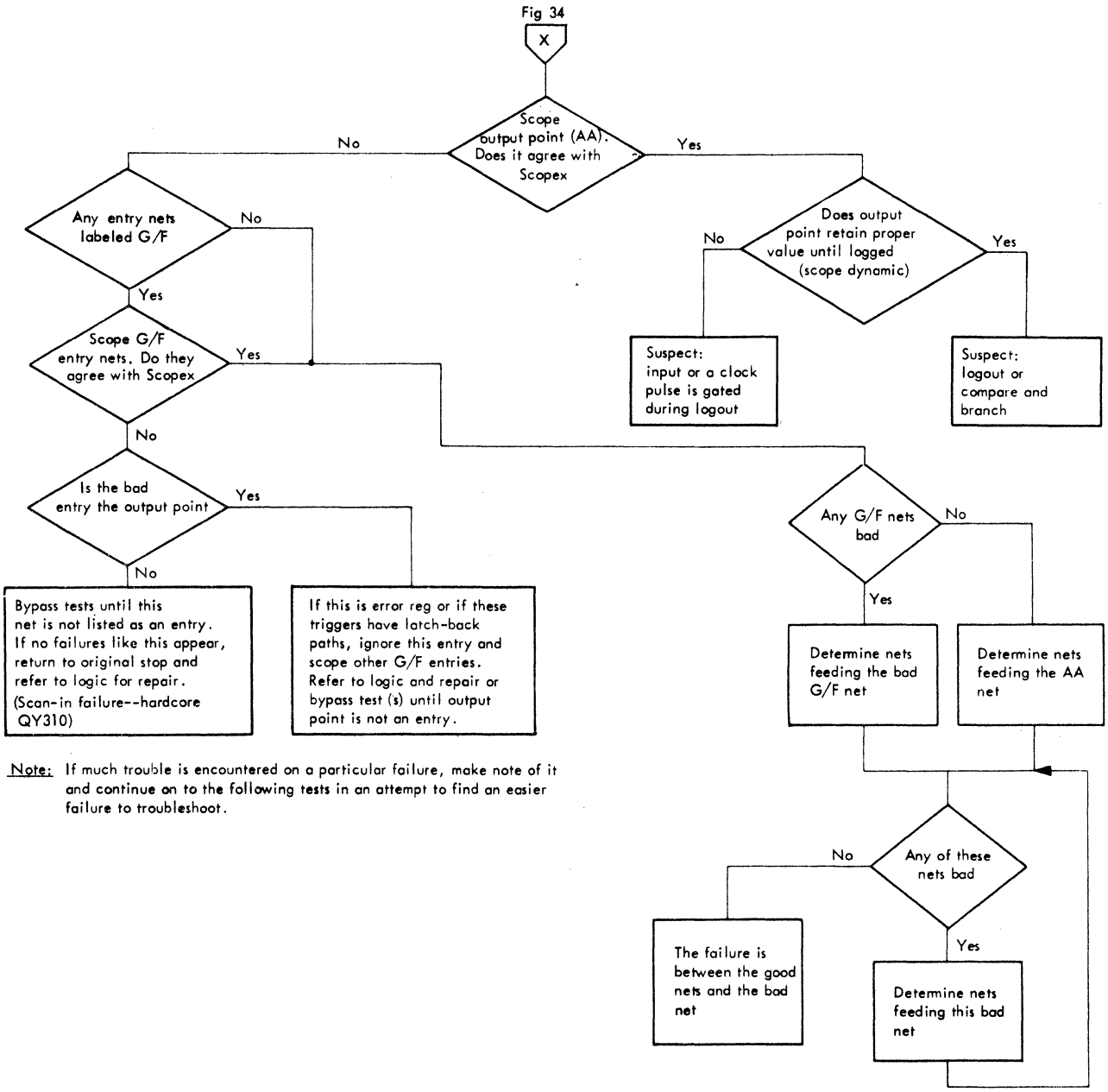
NOTES

1. On extended ROS, initial halt after load is IAR = 408C.
2. If FLT load operation results in load checks, perform the following operation to check out the FLT load data path from the selector channel B register to the SDR on an FLT load from tape:
   a. Using the off-line CE controls on the TAU, write a long, continuous record of all ones on a scratch tape (mounted on an available tape unit).
   b. Rewind the tape, put the TAU back on-line, and perform a normal FLT load.
   c. Set the selector channel roller to the B register (position 1) and visually compare the bits appearing in the B register with those appearing in SDR. If any bit position is not functioning, it is apparent in the indicators. An FLT load check also occurs but the loading of data continues until the end of the tape record is reached (the full record written in step 1).
   d. The procedure can be repeated to check for correct zero states by writing all zeros (except parity bit) on tape and repeating steps 2 and 3.
   e. The parity bit positions can be checked for their zero state by writing all zeros in bit positions P and 0-6 and one in position 7 and repeating steps 2 and 3.

Table 1

Failing SAR Bit	IAR Indicator	SDR Indicator Byte
29	101	C
28	4	C
27	4	14
26	4	24
25	4	44
24	4	84
23	209	308
22	4	204
21	4	404
20	4	804
19	4	1004
18	4	2004

FIGURE 34. FLT RUN AND REPAIR PROCEDURE



Note: If much trouble is encountered on a particular failure, make note of it and continue on to the following tests in an attempt to find an easier failure to troubleshoot.

FIGURE 35. CYCLE TEST REPAIR PROCEDURE

Main Storage Ripple Test

Following is the procedure for running the main storage ripple test:

1. Set the storage test rotary switch to the zeros position.
2. Press the write lever switch.
3. Press the start key. IAR and SAR indicators 15* through 29 should blink and SDR should contain ones.
4. Return the write lever switch to the neutral position.
5. Press stop on check. IAR and SAR indicators 15* through 29 should blink and SDR should contain zeros. Return stop on check switch to normal.
6. Repeat steps 2-5 with the rotary switch set to the ones position. Indications should be the same except SDR should contain all ones at step 5.

Note: While running the ones test, set the storage test switch to the process position. This gates the storage parity bits to the FLT op reg (2-5) thus turning the binary trigger on and off.

7. Repair any failures before continuing.
8. Return the main storage test controls to normal.

* Depends on storage size; 15 equals 128K.

Skipping Bad FLT Records

If a record on tape or disk cannot be read in correctly, and it is desired to skip that record and read in the next record, the following procedure must be followed:

For Tape: With the FLT control switch not on auto reread, depress the system reset PB and then depress the load PB.

For Disk: With the FLT control switch not on auto reread, set the FLT mode switch to the force pass position and depress the system reset PB. (This steps the cylinder counter up by one.) Next, set the FLT mode switch back to the load position and then depress the load PB.

Disk (FLT) Operating Procedures

The following procedures are for disk-originating FLT's and are not to be confused with the tape-originating FLT procedures which precede this section.

MS Mode Hardcore (Disk): For stops and loops not identified in this section, refer to the main store hardcore listing (FLT01) and check the stop codes to identify the failure.

1. Mount disk pack No. 1 containing the MS hardcore tests on a disk drive attached to a selector channel, start motor, and wait until unit is ready.
2. Select the channel and disk drive address with the load unit switches (switch labeled 0-7 selects the channel).
3. Press system reset with the FLT mode switch in neutral.
4. Place the FLT mode switch in the load position.
5. Place the FLT control switch in the halt-after-load position.
6. Place the check control switch in the stop position.
7. Press the load key. The first record of MS hardcore is read into storage and the following indicators should now be on:
   a. Sequence counter indicators 1 and 2 (equal 3).
   b. Sequence stat 3.
   c. Sequence counter mode.
   d. Load light.

   IAR should equal 024 (1st pack only).
   IAR should equal 408C (2nd and 3rd packs).
8. Return the FLT control switch to process if the load was successful; otherwise, repair the load circuitry and reload (Figure 26).
9. Press start.
   a. Record 1 is executed. If successful, record 1 calls in record 2 which, if successful, calls in record 3.
   b. Record 3 will stop three times for ROS words FD5, FD6, and FD7. These words have bad parity to test ROS parity check circuits.
10. At the first stop, the hard stop indicator should be on.
11. Turn CPU roller 2 to display current ROS address (row 7).
12. Depress the force indicator lever switch; the ROS address shown should be FD5.
13. Press start. The ROS address should be FD6 and the hard stop indicator should be on.
14. Press start. The ROS address should be FD7 and the hard stop indicator should be on.
15. Press start. SDR indicates a successful stop as follows:

```
P    P    P    P
1FF  0FF  1FF  1FF
```

MS Mode ROS Bit Tests (Disk): The SDR is used for error analysis and error indications. See the main store mode ROS bit test listing (FLT04) for stops and loops not identified.

1. Press start (following a successful halt of MS hardcore tests).
2. ROS bit test record 1 loads, executes, and calls for the next record.
3. ROS bit test records continue to be executed until the termination record is sensed at the end of the disk pack. If no stops occurred, disk pack No. 1 successfully checked out ROS bits for planes 0-5.

```
IAR = 004
SDR = P    P    P    P
      1FF  0FF  1FF  1F1
```

4. Remove disk pack No. 1 and mount disk pack No. 2, start disk drive motor and wait for the unit to become ready.
5. Repeat steps 2-8 as described under "MS Mode Hardcore (Disk)."
6. Press the start key.
7. ROS bit records continue to be executed until the termination record is sensed at the end of the disk pack. If no stops occurred, disk pack No. 2 successfully checked out ROS bits for planes 6-B.

```
IAR = 004
SDR = P    P    P    P
      1FF  0FF  1FF  1F2
```

8. Remove disk pack No. 2 and mount disk pack No. 3. Start disk drive motor and wait for the unit to become ready.

9. Repeat steps 2-8 as described under "MS Mode Hardcore (Disk)."

10. Press start.

11. ROS bit test records continue to be executed until the first good stop at location FD5. This word has bad parity in group 1 and tests the ROS parity check circuits. The hard stop indicator should be on.

12. Press the force indicator switch. The current ROS address should be FD5. At this stop, set the check control switch to disable and press start.

13. SDR indicates a successful stop as follows:

P	P	P	P
1FF	0FF	1FF	1FF

The IAR should equal 1581 (hex).

ROS Mode Hardcore (Disk): For error stops and loops, refer to the ROS hardcore listing (FLT02).

1. Mount disk pack No. 4 containing ROS hardcore, zero-cycle, and one-cycle tests on a disk drive attached to a selector channel, start file motor, and wait until the unit becomes ready.

2. Select the unit with the load unit rotary switches.

3. Make sure the check control switch is set to disable.

4. Set the FLT control switch to halt after load.

5. Press system reset with the FLT mode lever switch in neutral.

6. Place the FLT mode lever switch in the load position.

7. Press the load pushbutton. IAR should equal 3FFC.

8. Place the FLT control switch in the process position.

9. Press the start PB. The IAR should equal 490 (hex), and the fail and binary triggers should be on. The SDR should contain the following:

P	P	P	P
1FF	0FF	1FF	1FF

10. Place the FLT control switch in the process position.

ROS Mode Cycle Tests (Disk): For stops not identified in this section, refer to the repair procedures.

1. The ROS mode hardcore tests should have run successfully.

2. Press the start PB.

3. The zero-cycle tests are loaded into storage and executed.

4. Completion of the zero-cycle tests automatically calls in the one-cycle tests.

5. Completion of the one-cycle tests results in a successful stop with the SDR equal to the following:

P	P	P	P
1FF	0FF	1FF	1FF

6. Neutralize all the FLT controls (FLT mode switch off, FLT control switch on process, and check control switch on process).

7. Using the storage test switches, write all ones in storage to restore good parity to storage.

Cycle Test Repair Procedures (Tape/Disk)

Note: The FLT compare and branch microprogram (QY510) cannot be single-cycled correctly unless the FLT mode switch is in the neutral (off) position.

If a great deal of trouble is encountered on a particular test failure, make a note of it and then continue on to the following tests to attempt to find an easier failure to troubleshoot.

The following procedure may be used to locate problems that cause FLT's to stop before completing all tests.

1. Check the pass/fail triggers; either fail, or both pass and fail should be on.

2. Check SDR. Byte zero contains hex 01 (bit 7 is the termination bit). Bits 20-31 contain the hex value to use when referring to Scopex. If bits 16-19 are other than zero, stop is in a one-cycle test. Go to item 17. If bits 16-19 are zero, go to item 4.

3. If items 1 and 2 are not true, check IAR. If IAR is less than 148 (hex), the first six words of the record were not executed properly. Refer to the record format section. If IAR is more than 148 (hex), storage location 84 will contain the mask address for the current test.

Note: As an aid in finding the error, bypass this test to see if there are multiple errors in the zero-cycle tests. If no multiple errors, turn back to first error.

4. Get Scopex for the zero-cycle tests.

5. Find the hex value in Scopex that agrees with SDR 20-31. The column following the test number indicates what the test was trying to do with the trigger. R or 0 equals reset; S or 1 equals set. The next column contains the location of the card that the failing trigger is on. Change the card.

6. Press start.

7. If the card was bad, testing continues. Otherwise, SDR will contain the same hex value as in item 5.

8. If the card was not at fault, turn CPU roller 2 to position 7 and check that the current ROS address is 000.

9. Place the FLT control switch in repeat.

10. Set the ROS address compare switch to stop.

11. Place F49 in data keys 20-31 (checks scan-in, QY110).

12. Turn CPU roller 1 or 2 (depending on the trigger being tested) to the position containing the failing trigger.

13. Press start.

14. If the block indicators light is on, use the force indicator switch to check the value. The trigger should be in the state that is being tested for. If not, refer to the logic and the scan-in paths. The logic involves a maximum of four cards on scan-in.

15. If scan-in is correct, place F4F in data keys 20-31 (QY510).

16. Press start. SDR contains the actual response. To find the tested bit, refer to Figure 36 and the logic.

17. For one-cycle tests, the segment number and test number are displayed in SDR (16-31). Find this number in the appropriate Scopex volume.

18. Rotate CPU roller 2 to position 7 (current ROS address) for one-cycle tests, or position 8 (previous ROS address) for two-cycle tests (segments four and six).

19. Place the value of the current ROS address for one-cycle tests, or the value of the previous ROS address for two-cycle tests (segments 4 and 6) in data keys (20-31). This is the stop address for static scoping. (Emulators use data keys 19-31.)

20. Place the FLT control switch in the repeat position.

21. Press start. The output point (first line) of the failing test may be scoped dynamically. All other points may be scoped either dynamically or statically.

22. To scope the output of the failing test dynamically:

a. Attach the sync lead to the sync box (positive sync).
b. Rotate the switch on the sync box to FLT cycle sync. If sync box is not available, sync minus on B-D1C3D10 (KH331).
c. Set the scope time base to 0.1 microseconds/centimeter. (This displays two cycles.)
d. For two-cycle tests sync on first sync pulse.

23. The area of the scope face to check depends on the circuitry being scoped.

a. For group A, look during and after output trigger clock time (the group is indicated in Scopex next to test number. See Figure 9).
b. For group B, look during clock time.
c. For group C, look before and during clock time.
d. For group D, look before clock time.

Figure 34 is a simplified description of the following steps (24-29):

24. Place the scope probe on the output point. If the output level agrees with Scopex and holds that value until logged (see logout chart), check the test number and segment number (step 17) with FLT control switch in process. If step 17 is correct, check the logout circuitry. If the output level agrees with Scopex and does not hold its value until logged (a clock pulse is gated to the trigger before it is logged, or an input has changed during scan-out) or if it does not agree with Scopex, go to step 25 (static) or to step 26 (dynamic).

25. Statically scope as follows:

a. Set the ROS address compare switch to stop. Machine will stop unless the wrong ROS address is set up. (See step 18.)
b. If the check register gated indicator is on, go to step 26; otherwise, continue pressing start until the indicator comes on.

26. Scope the G/F entries. If the G/F entries do not agree with Scopex, continue; otherwise, go to step 29.

27. Check to see if the output point is listed as an entry.

a. If the output point is also an entry and this is the error register (KT011-031), ignore this entry and scope other G/F entries. If the output point is also an entry and this is logic (KS101-171, KS201-231, or RP011-021), these triggers have latch-back paths. Refer to logic and repair or bypass the test(s) (step 28) till the output point is not an entry.
b. If the output point is not an entry, bypass the test(s) (step 28) until this net (G/F entry, step 26) is not listed as an entry. If there are no similar failures, return to the original stop, refer to the logic and repair (scan-in, dead entry, or ROSDR failure).

28. To bypass tests, place the FLT mode switch in the force pass position, press start, return the FLT mode switch to the load position, and press start again.

29. Scope the G/F points in order after the output point.

a. If there are no G/F points, change the cards listed at the end of the test.
b. If a G/F point agrees with the Scopex:
   1. Go to the previous bad G/F point and scope its inputs (FED BY).
   2. If the inputs agree with Scopex, the card or some other point in the failing net is bad.

Scan-In To		From Test Word		Scan-Out To		Via Scan		Scan-Out Micro-Insn	Approx Time ** (usec)	Comments
Reg	Bits*	Word	Bits	Loc	Bits	Gr	Logic			
J	P-3	1	12-15	98	9-13	B	BH611-621	F24	15.5	Parity of J generated from AOB 8-15 and Parity of 8-15
MD	P-3	1	16-19	98	14-18	B	BH611-631	F24	15.5	Parity of MD generated from AOB 16-23 and parity of 16-23
Byte Stats		1	P0-P3	Not Logged						
PSW 32-33	32,33	1	0-1	9C	24,25	D	BH681	FA3	17.5	Bits 0 and 1 decoded to set ILC 0,1 = 00 ILC = 01 0,1 = 01 or 10 ILC = 10 0,1 = 11 ILC = 11
MB	P-1	1	3-4	94	9-11	B	BH611	FA4	13.5	Parity generated by and of mover 6-7
G2	S-3	1	5-8	98	26-31	B	BH641-651	F24	15.5	Parity generated by parity of mover 4-7
F	P-3	1	21-24	94	12-16	B	BH621	FA4	13.5	Parity generated by mover 4-7
PSW 34-39	34-39	1	26-31	9C	26-31	D	BH681	FA3	17.5	
Carry Stat		2	0,1	94	30	D	BH681	FA4	13.5	
Store Prot		2	8-11	Not Logged						
1 Syl Op		2	15,16	9C	0	D	BH671	FA3	17.5	
PSW 0-7		2	23-30	Not Logged						
Stats 4-7	4-7	2	P0-P3	94	24-27	D	BH681	FA4	13.5	
L Sgn Stat		3	0	94	28	D	BH681	FA4	13.5	
Mpx		3	1-13	D4	4-14	J	BH341			
G1	S-3	3	24-27	98	20-25	B				Parity generated by parity of mover 0-3
Q Reg	0	3	31	94	17	B	BH631	FA4	13.5	
CPU WFN	2	3	P1-P3	8C	26-28	B	BH641	FA5	10.0	
R Sgn Stat		4	0	94	29	D	BH681	FA4	13.5	
Stats 0-3	0-3	4	P0-P3	94	20-23	D	BH681	FA4	13.5	
Bfr 1		5	0-7	CC	0-8	J	BH341			
Bfr Mpx Stats		5 5	8-15 16-19	CC D4	9-17 18-21	J E	BH341-351 BH321			
LB	P-1	5	30-31	94	6-8	B	BH611	FA4	13.5	Parity generated by and of mover 6-7
LSFN	0-1	5	P2-P3	98	7-8	B	BH611	F24	15.5	
I/O Reg	P-1	6	30-31	94	1-3	D	BH671	FA4	13.5	Parity generated by exclusive OR of bits 30-31
I/O WFN	0-2	6	P3-P1	8C	29-31	B	BH651	FA5	10.0	
M	P0-27	7	P0-27	A8	0-31	A	BH141-191	F22	28.0	
	28-31		28-31	AC	24-27			FA1	25.0	
L	P0-27	8	P0-27	B8	0-31	G	BH101-131	F20	32.0	
	28-31		28-31	BC	24-27			FBD	33.5	
R	P0-27	9	P0-27	B0	0-31	A	BH141-191	F21	27.0	
	28-31		28-31	B4	24-27			FA0	29.0	
I/O IF		10	P0-31							
H	P0-27	11	P0-27	A0	0-31	A	BH141-191	F23	19.0	
	28-31		28-31	A4	24-27			FA2	21.0	
LSAR	P-5			98	0-6	B	BH601-611	FA4	13.5	Scanned in value is same as J Reg
Refetch				9C	1	D	BH671	FA3	17.5	Set If Bits 18-28 of AOBand IAR Match
Error Reg				88	0-26	C	BH741-781	F26	8.0	0-3 Eq. Half Sum 4-7 Eq. Full Sum 8 Eq. Car. 9-11 Eq. LB, MB, MD 12, 13 Eq. G1, G2, 14-16 Eq. U, V Mvr Out 21-23 Eq. ROS
ROAR				90	6-17	H	BH811	F25	11.5	

NOTES:

1. To check if trigger maintains value for scan-out:
   a. Rotate T/CM switch to 5 or 10 usec.
   b. Trigger should hold value for at least time specified in approximate time column.
   c. If not proper, check points feeding trigger from Scopex and make sure of all levels.
   d. If OK check 2.

*This column indicates number of bits logged out. Microinstruction is the actual ROS address that causes associated group to be placed on scan bus.

**Approximate time is the amount of time the output point on Scopex must maintain the indicated value to be gated into the SDR successfully (reference time is FLT cycle sync pulse).

2. To check the value of a trigger before scan-out and the actual scan-out before the compare and branch:
   a. Place address 2C0 into data keys 20-31.
   b. Place FLT control switch to repeat.
   c. Depress start.
   d. Place ROS address compare switch to stop.
   e. Rotate appropriate CPU roller to position that displays failing trigger.
   f. If block indicator light is on, depress force indicator switch.
   g. The value indicated now is what should be placed in memory.
   h. Place F4F in data keys 20-31.
   i. Depress start.
   j. If block indicator light is on, depress force indicator switch.
   k. SDR now contains the actual response (obtained from the scan-out location).

FIGURE 36. FLT SCAN-IN, PARITY GENERATION, AND SCAN-OUT

3. If any input is bad, follow its inputs until a point is found with all inputs good. This point is in the failing net, and the card or some other point in the net is bad.

c. If there are no G/F points listed and no cards listed, or if none of the G/F points agree with Scopex, refer to the logic and scope the dead entries.

Checkout After Repair

After effecting an FLT repair, rerun all FLT's to be sure of the fix. Use storage ripple (all ones) to put all good parity in storage (FLT's use both good and bad parity), and neutralize all FLT controls.

FLT DOCUMENTATION

This section describes documentation presently available for the Model 50 fault locating tests.

MS Mode Hardcore: Documentation consists of a program listing (FLT01) of the tests as they are in storage. This includes the op code, data, function, and IAR value. There is also a table provided for SAR and/or IAR failures.

MS Mode ROS Bit Tests: Documentation consists of a listing (FLT04) providing samples of the first two tests of record 1 and an explanation of how to determine the starting address of a failing test. This includes op code, data, function, and IAR and SDR values.

ROS Mode Hardcore: Documentation consists of a program listing (FLT02) of the tests as they are in storage. This includes data, function, and IAR values.

ROS Mode Zero-Cycle Tests: The zero-cycle test documentation is shown in Figure 37. The first column is the test number in hex. This is the number displayed in SDR bits 20-31 on a termination.

The second column contains two characters which show the condition the trigger should attain for the test. The first character indicates whether the trigger should be set (S) or reset (R) by the test, and the second character tells whether the scope point given should be an up (1) or a down (0) level. The only combinations that appear are R0 and S1.

The third column gives the pin at which the value (0 or 1) should be observed; the fourth column provides a logic page reference to the trigger being tested, and the fifth column gives the name of the trigger.

Test No.	Desired Result	Test Point	Logic Page	Trigger Name
012D	R0	01A-C4M4D12	RR071 AA4	R Reg 28
012E	S1			
012F	R0			
0130	R0	01A-C4M4B12	RR071 AB4	R Reg 29
0131	S1			
0132	R0			
0133	R0	01A-C4M4J10	RR071 AC4	R Reg 30
0134	S1			
0135	R0			
0136	R0	01A-C4M4G08	RR071 AD4	R Reg 31
0137	S1			
0138	R0			
0139	R0	01A-C3H2D06	RR001 AB4	M Reg 0
013A	S1			
013B	R0			
013C	R0	01A-C3H2D05	RM001 AC4	M Reg 1
013D	S1			
013E	R0			

Example: Stop at 133 indicates R register (30) does not reset off.
Stop at 134 indicates R register (30) does not set on.
Stop at 135 indicates R register (30) does not reset off after setting on.

FIGURE 37. ZERO-CYCLE TEST DOCUMENTATION

ROS Mode One-Cycle Tests (Scopex): The one-cycle test documentation (Scopex) is an automatically produced FLT document that allows conversion from the pattern displayed on the console lights to the suspect cards or nets. Scopex consists of a series of lists, each referring to one particular test. Lists are separated from the identification number of the test by asterisks. Each list consists of several lines of information, each line referring to a particular pin or net in the machine. A typical list is shown in Figure 38. When a test sequence stops, the hex number displayed in bytes two and three is the segment number and test number within the segment.

The term "tree" includes all nets encountered when tracing back from a trigger and continuing until each path reaches either another trigger or another entry to the combinational logic; e.g., I/O lines, console switches, etc. Entries to the trees are identified by the word "entry", if they are triggers which can be set to either state by the scan-in logic. If entry points are always at the same state at the conclusion of scan-in, they are "dead" entries.

Each line of the list refers to a net in the machines which, if it does not assume the value which the input pattern is trying to force it to, will cause the test to fail. These nets are given in the fourth column (net) of the list. The first line (Ref-AA) in each list corresponds to the output point, the next lines to the nets feeding this output point, and so on back through the logic to the entries. The pin at which each net can be observed is shown in the third column (Pin). Generally, only the nets having pins are printed on the list because the failure of a net internal to the card will nearly always propagate and give the wrong value on a pin. The second column

(V) of each list contains the values which should exist on these pins if the test passes. The time relative to the clock at which these points should be observed depends on the position of the block within the logic. The four classes defined, together with their observation times, follow. (The clock referred to is the clock controlling the output trigger, and the logic page for this trigger is always given in line AA. See Figure 39.)

1. Group A scoping values must be measured during and after clock time for the output trigger.
2. Group B must be measured during clock time.
3. Group C must be measured before and during clock time.
4. Group D must be measured before clock time.

The group to which a given line belongs is given next to the value which should be found.

Column 5 of Figure 38 (Ref) contains a reference list for all lines in the list starting from AA (the exit point) and going through AZ, B, and BA, as far as necessary.

Column 6 (Fed By) contains the references of all sensitive nets feeding the block to which the line refers. This enables the sensitive tree to be built up. Because this is only the sensitive tree and not the complete tree, several points should be noted. The fact that the output of a block is sensitive can still allow either all or some of the inputs to be insensitive. Figure 40 shows that if net BA, a 1, is sensitive, then neither of its inputs is sensitive because either can change without affecting the output. (The FLT concept assumes only a single failure.) In the case of net CA, a 1, net BA is sensitive but net AB is insensitive.

Figure 40 shows that if net EA is sensitive, then neither net BA nor net DA is sensitive because either could change without affecting the output. However, going back to net AA we see that if this changes, then both inputs to E will change and the output will be affected. Therefore, net AA and both of the inputs to block A are sensitive. In the case

Columns

1 G/F	2 V	3 Pin	4 Net	5 Ref	6 Fed By
		********** 1	1C		**********
	A0	01A-C4L4G08	RL071AD4	AA	AB AF
	C1	01A-C4L4J06	RL071AT4	AB	A1 AC
	C0	01A-C2L5D13	BA311AC4	AC	AD
	C0	01A-C2G4D04	BA311BH4	AD	AE A1 AT AU BH
	D1	01A-C2F6G13	BA311AE4	AE	AG
	C1	01A-C4L6B03	RL071BD4	AG	
	D0	01A-B3K5B08	AM071AT4	RG	AH AK BA
	D1	01A-B3K5D06	AM071AS4	AH	AJ
	D1	01A-C2K4D04	KC411AC4	AI	AL AO
	D0	01A-B3K5B02	AM071RR4	AJ	AW BB AS BC
	D1	01A-B2E3B02	AN081AZ4	AK	AV AM AN
	D1	01A-C2L4B07	KC401BH4	AL	
G/F	D0	01A-D2F2B07	DS301DC4	AM	AR
	D0	01A-D2F2B10	DS301GB4	AN	AP AQ BE
	D1	01A-C2K6D06	KC401BJ4	AO	
	D1	01A-D2G3B10	DS301DA4	AP	A2
	D1	01A-D2G3B07	DS301CB4	AQ	A3
G/F	D1	01A-D2G3B09	DS301CA4	AR	A4
	D1	01A-B4L5D06	BX031AJ4	AS	AX
	D1	01A-C2G7D06	BA311BV4	AT	
	D1	01A-C2D2B07	BA311BT4	AU	
	D0	01A-D1J3B02	DR032BR4	AV	AY AZ
	D1	01A-B4D4D11	BY031AM4	AW	
	D0	01A-B4J5B13	DR011BJ4	AX	BF
	D1	01A-D1J6B02	DR032CB4	AY	
	D1	01A-D1L6D09	DR032AT4	AZ	
	D1	01A-D1H5B02	DR032AS4	B	A5
	D1	01A-D1D6B08	DR031CL4	BA	BD
	D1	01A-B4E3D05	BY031AN4	BB	
	D0	01A-B4C5D12	DR021AD2	BC	BG
	D0	01A-D1M6D06	DR031AL4	BD	
	D1	01A-D2F2D18	DS301GA4	BE	
	D1	01A-B4H6D07	DR011AL4	BF	
	D0	01A-B4D6D02	RK311CD4	BG	A6
	D1	01A-C2G4J02	BA311AX4	BH	A7 A8 A9 B0
	0	DEAD ENTRY	RL071AM4	A1	ENTRY
	0	01A-D2D3B04	RK231AD4	A2	ENTRY
	0	01A-D2D3D06	RK231AE4	A3	ENTRY
G/F	0	01A-D2D3B03	RK231AF4	A4	ENTRY
	0	01A-D1K7D06	RK321BF4	A5	ENTRY
	1	01A-B4D6B04	RK311BD4	A6	ENTRY
	0	DEAD ENTRY	BA311AV4	A7	ENTRY
	0	DEAD ENTRY	BA311AU4	A8	ENTRY
	0	DEAD ENTRY	BA311AT4	A9	ENTRY
	0	DEAD ENTRY	BA311AS4	B0	ENTRY
G/F		01A-B2E3	CARDS		

FIGURE 38. ONE-CYCLE TEST DOCUMENTATION (SCOPEX)

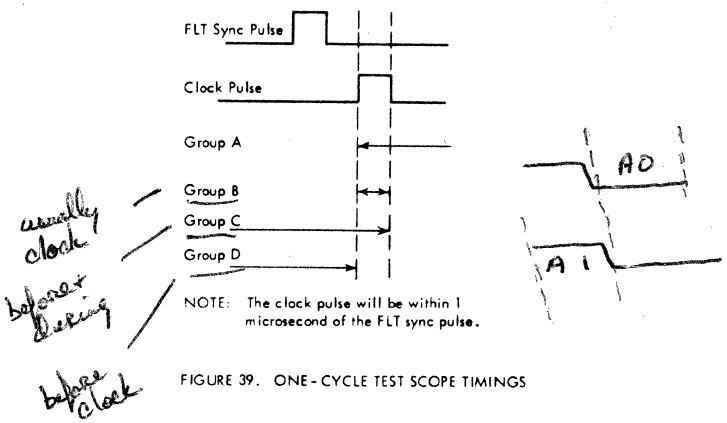


FIGURE 39. ONE-CYCLE TEST SCOPE TIMINGS

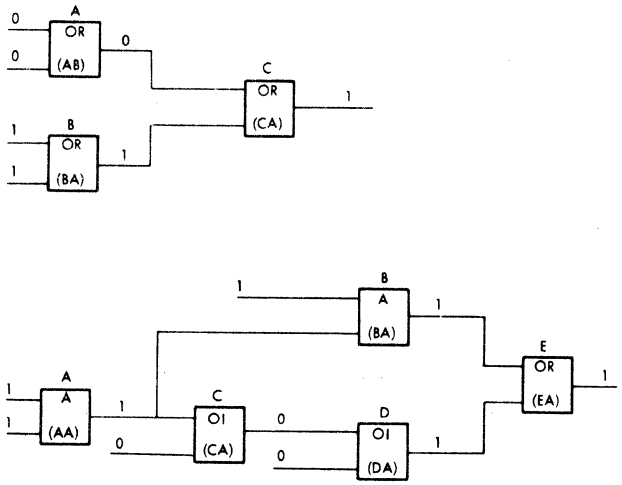


FIGURE 40. SENSITIVE NET EXAMPLES

of the blocks that are set by the scan-in circuitry and which are sensitive, no "fed by" information can be given and the word "entry" is printed in this space. To make it easy to identify these points in the main list, they are referenced differently. They are labeled A1-A9, B0-B9, etc. In the cases where a block is fed by several nets having sequential references, whether entries or in the main part of the list, the references are given as AD-AG, instead of AD, AE, AF, AG.

The only other information on Scopex concerns those cases where a net internal to a card is sensitive but does not propagate its sensitivity to a pin. In these cases, separate lines give the index number followed by the word "card" and then a list of the cards that are suspect.

PROGRESSIVE SCAN

Progressive scan is a method of testing the common channel, the multiplexor channel, and the selector channel, using no additional hardware to scan directly into each loggable storage element. Storage elements are set by controlling the action of the channel clocks and by applying patterns via the diagnose instruction.

Two tapes or disks are created in FLT format, one for testing the common channel and the selector channel, and the other for testing the common channel and the multiplexor channel.

The tests are written in a functional manner using the diagnose instruction as a vehicle for controlling clocks and the action of the I/O interface. Each group of tests making up a complete function is termed a series, and each series may be divided into routines.

Each test begins from a reset condition. A pattern is applied by diagnosing to ROS in a functional manner or after having set the interface (IF) register. Figure 41 shows details of the IF register. Each succeeding test includes all the preceding testing plus the testing required for the next stopping point prior to logout.

Figures 42 and 43 show multiplexor channel and selector channel progressive scan run and repair procedures, respectively.

Note: Disable ROS retry by jumpering 01C-E3C4D11 to a D08 pin before running or biasing FLT's, diagnostics, or progressive scan. (It is normal for the master check indicator to be on during the running of progressive scan tests.)

Test Descriptions

Progressive scan tests are identified by a series number and a test number along with the name of the test. A typical selector channel series is composed of many individual tests. Each test performs all the operations of the previous test plus additional operations. An example of this appears in Figures 44 and 45. Figure 46 shows how to determine the length of a progressive scan test when using the repeat instruction with the diagnose address.

Selector Channel Clock -- 100-001-006

The selector channel clock is stepped to each point in its instruction scan sequence, logged out, and compared to a known good pattern. If there is a mismatch between logout and good pattern, the pertinent information is printed on the printer.

Start I/O Write -- 110-101

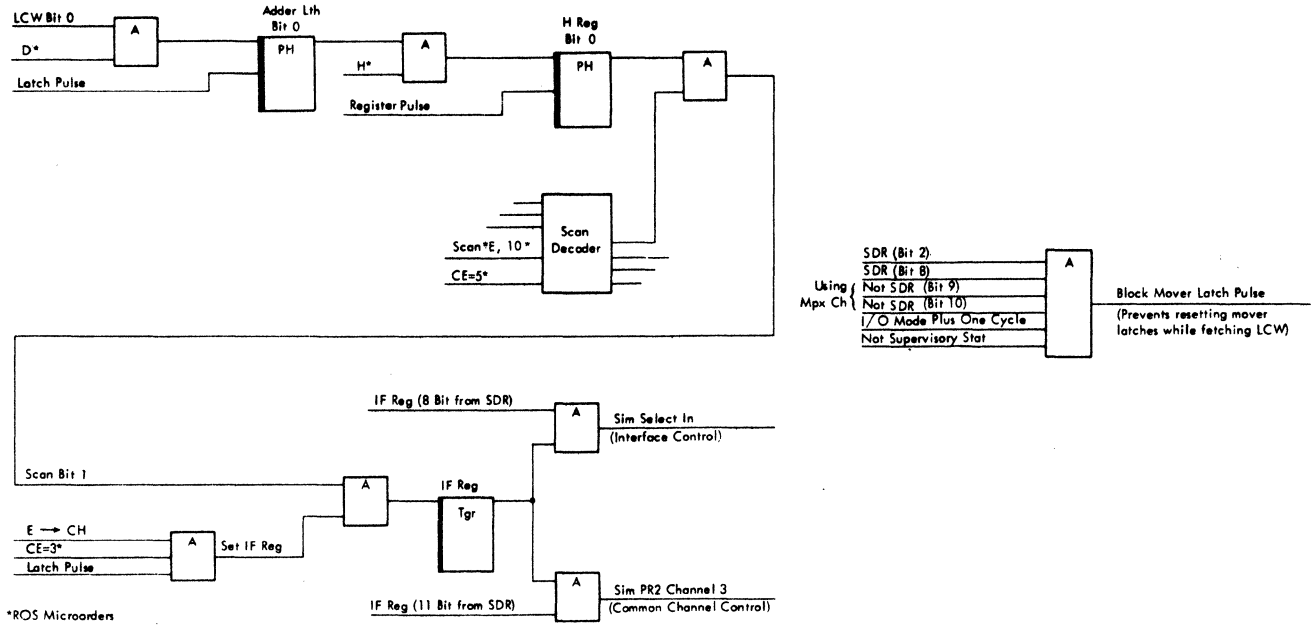
These tests are the start of true progressive scan. All other tests are modeled after this series. There are 12 stopping points between issuing a start I/O up to and including the second DTC of a start I/O ROS routine.

The selector channel and common channel are logged out when the start I/O microinstruction is given, at break-in for the first selector channel routine, and for each clock of each of two DTC's issued in start I/O routine.

The diagnose instruction is also used to functionally test the start I/O instruction. A description of some of this test follows. Figure 47 shows timing.

SIO Clock A1 -- 110-101: Common and selector channel are first reset. Diagnose instruction is used to scan into L register (unit address and channel), R register (command address), and M register (command code and data address). Next the IF register is set with the scan bit (stops the common channel clock) and the selector channel clock is allowed to advance to A1. The common channel clock will not run unless the diagnose instruction is counting ROS cycles. The diagnose instruction is now used with a count field of two to turn on the start I/O trigger in the common channel (ROS Addr 9BE). At this point the selector channel has acknowledged the start I/O, but it will not request a break-in until its clock reaches clock step. A log is initiated with the selector channel clock at A1 and with the common channel start I/O trigger on.

Reg SIO Routine -- 110-102: The common and selector channels are again reset. The L, R, and M registers are scanned. The IF register is set to control the common channel clock and to set the selector channel clock at A1. ROS Addr 9BE is again addressed by diagnose instruction to turn on start I/O in the common channel. At this point, test 02 is at the same place as the end point of test 01. To advance to the next logout point, the IF register is set to advance the selector channel clock to clock step. A logout is taken. Normally at this point the selector channel requests the start



SDR and Scan Bit	Interface Control(SDR 8)	Common Channel Control(SDR 11)	**If SDR bits 9 and 10 are zero, common channel control will be:
0	Select In	Priority 2 - Channel 3	
1	Operational In	Priority 3 - Channel 3	
2	NOTE 3	NOTE 3	
3	NOTE 3	Priority 3 - Channel 1	
4	NOTE 3	NOTE 3	
8	Scan (Must be one)	(Must be zero)	
9-10	Channel Address	----------	
11	(Must be zero)	Priority (Must be one)	
12	Reset	Reset	
16	Bus In - 0	PCI Request - Channel 1	
17	Bus In - 1	LS Request - Channel 1	
18	Bus In - 2	**PCI Request - Channel 2	Mpx Priority 2 (NOTE 1)
19	Bus In - 3	LS Request - Channel 2	
20	Bus In - 4	**PCI Request - Channel 3	Mpx Priority 3
21	Bus In - 5	LS Request - Channel 3	
22	Bus In - 6	**LS Write	Mpx PCI Request (NOTE 2)
23	Bus In - 7	Priority 1 - Channel 1	
P(24-31)	Bus In - P	Priority 2 - Channel 1	
24	Request In	Priority 1 - Channel 2	
25	Address In	Priority 2 - Channel 2	
26	Status In	Priority 3 - Channel 2	
27	Service In	Priority 1 - Channel 3	

With bit 8 on, bits 0-1, 16-23, P(24-31), 24-27 represent the 15 interface lines needed to simulate an I/O adapter. Bits 9-10 determine which channel is to be used (Mpx = 00, Sel 1 = 01, etc.). When bit 8 is one, the adapter connected to the addressed channel is logically disconnected and connected instead to the interface positions of the register.

With bit 11 on, the register positions are re-interrupted and used to set up common channel routine request controls and priority circuits, as indicated in the second column under format. Bits 8 and 11 must not be on at the same time.

Bits 9-10 cause a scan stat to be set in the addressed selector channel. This allows specification of a particular selector channel for log-out purposes. Bit 8 may be zero in this connection.

Bit 12 causes 8-11, which remain on once set, to be reset. When bit 12 is on in the scan-in word, bits 8-11 must be zero.

NOTE 1: PCI Request - channel 2 still comes on but is not used.

NOTE 2: LS write still comes on but does nothing.

NOTE 3: Bits 9-11 permit stopping of the selector channel clock at different points in a sequence. These bits are set into the SDR address keys and are decoded as follows:

9	10	11	
0	0	1	Stop on Clock A0
0	1	0	Stop on Clock Step Control
0	1	1	Stop on Clock A1
1	0	1	Stop on In-Tag Delay -- 1 and Not 2
1	1	0	Stop on In-Tag Delay -- 3 and Not In Tag
1	1	1	Stop on In-Tag Delay -- 2 and Not 3

All notes refer to LCW bit positions.

FIGURE 41. INTERFACE REGISTER AND FUNCTIONS

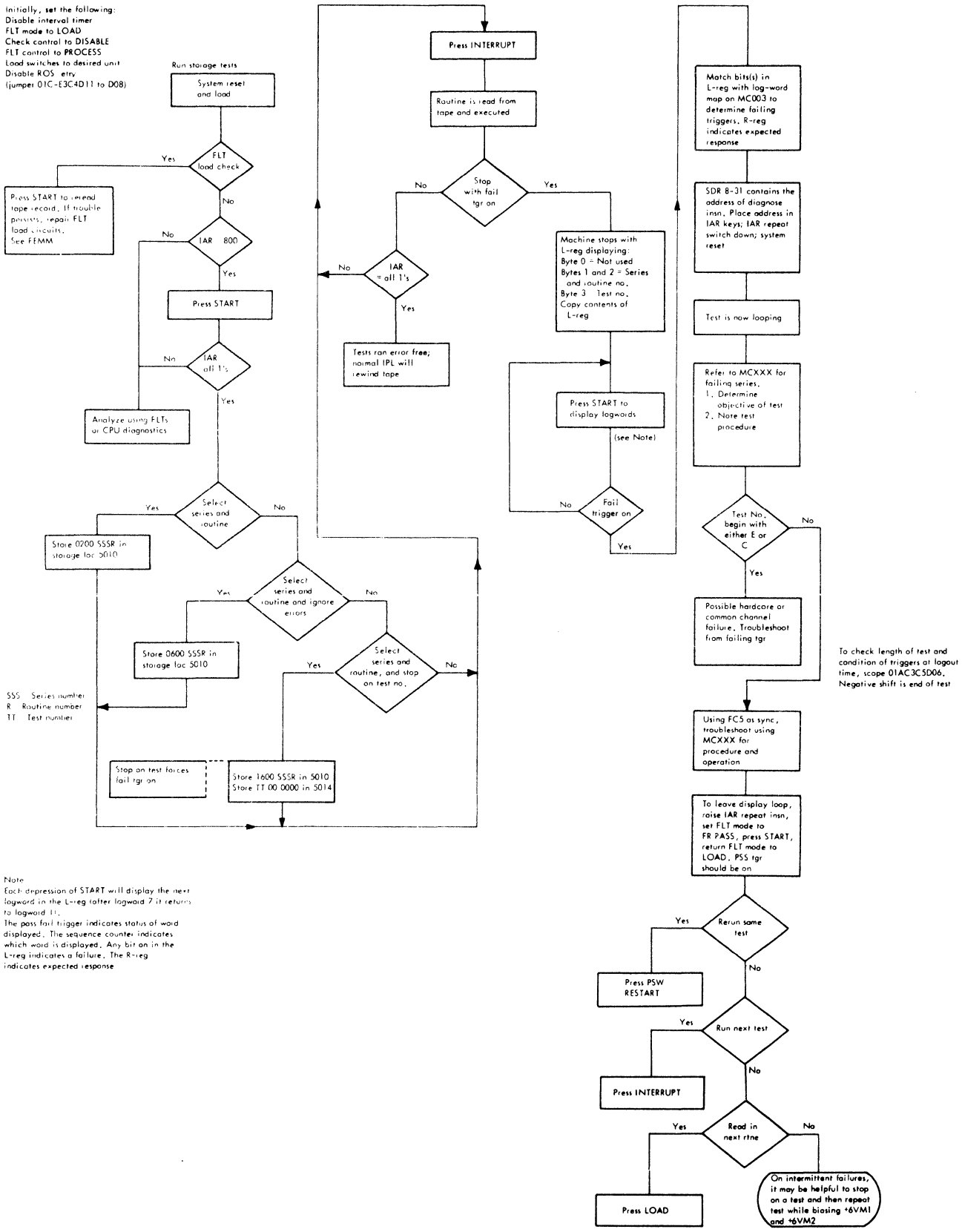


FIGURE 42. MULTIPLEXOR CHANNEL PROGRESSIVE SCAN RUN AND REPAIR PROCEDURE

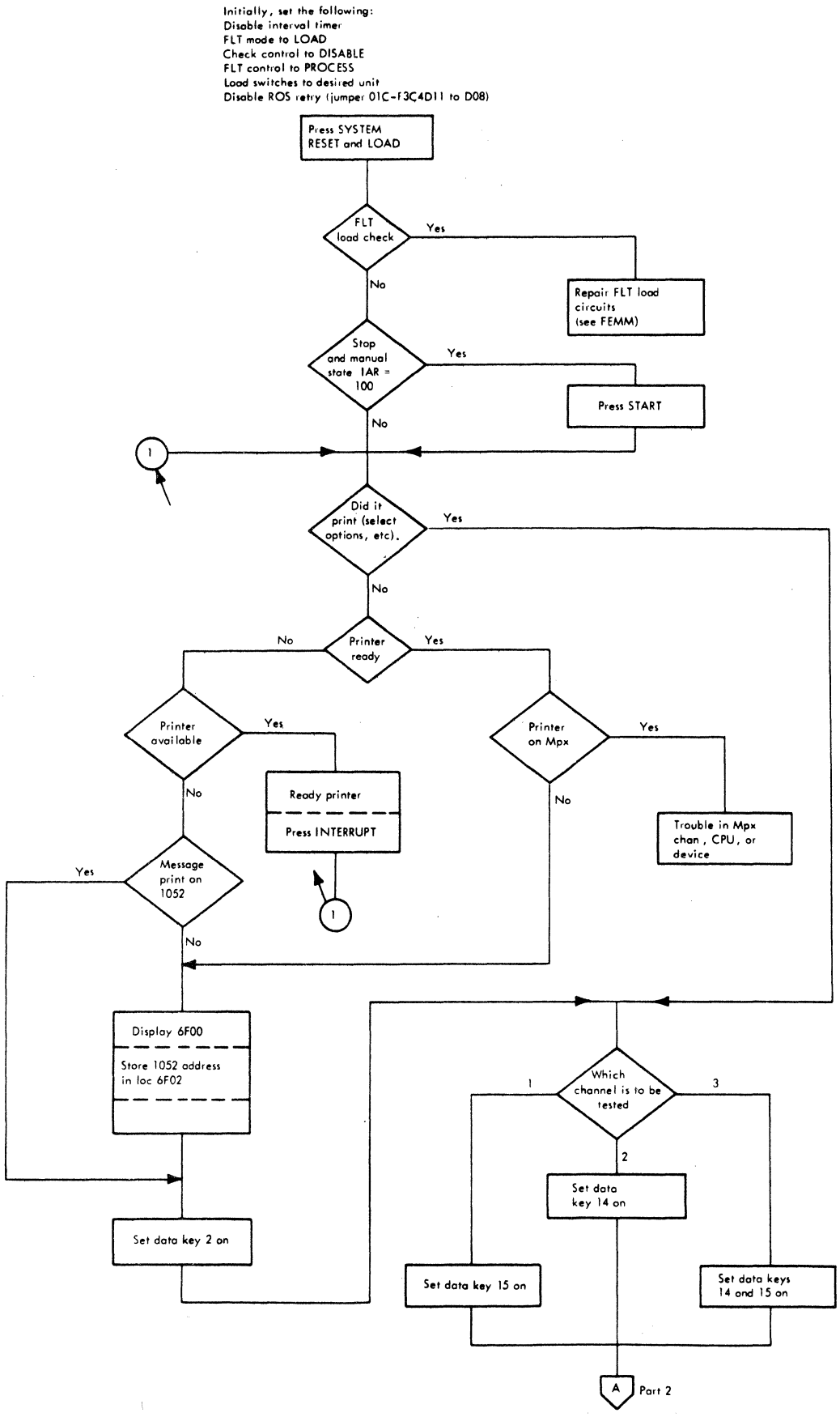


FIGURE 43. SELECTOR CHANNEL PROGRESSIVE SCAN RUN AND REPAIR PROCEDURE (PART 1 OF 3)

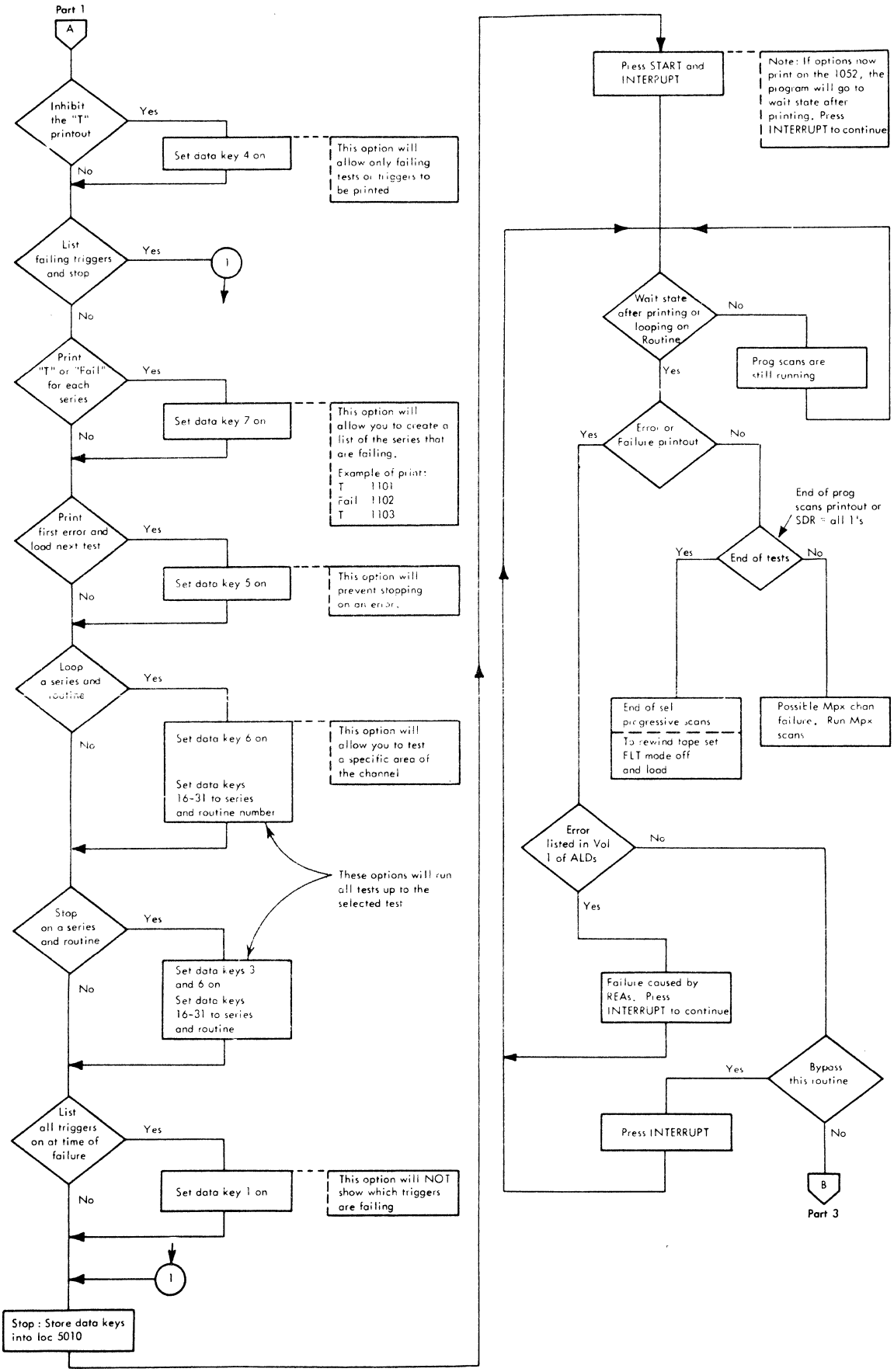
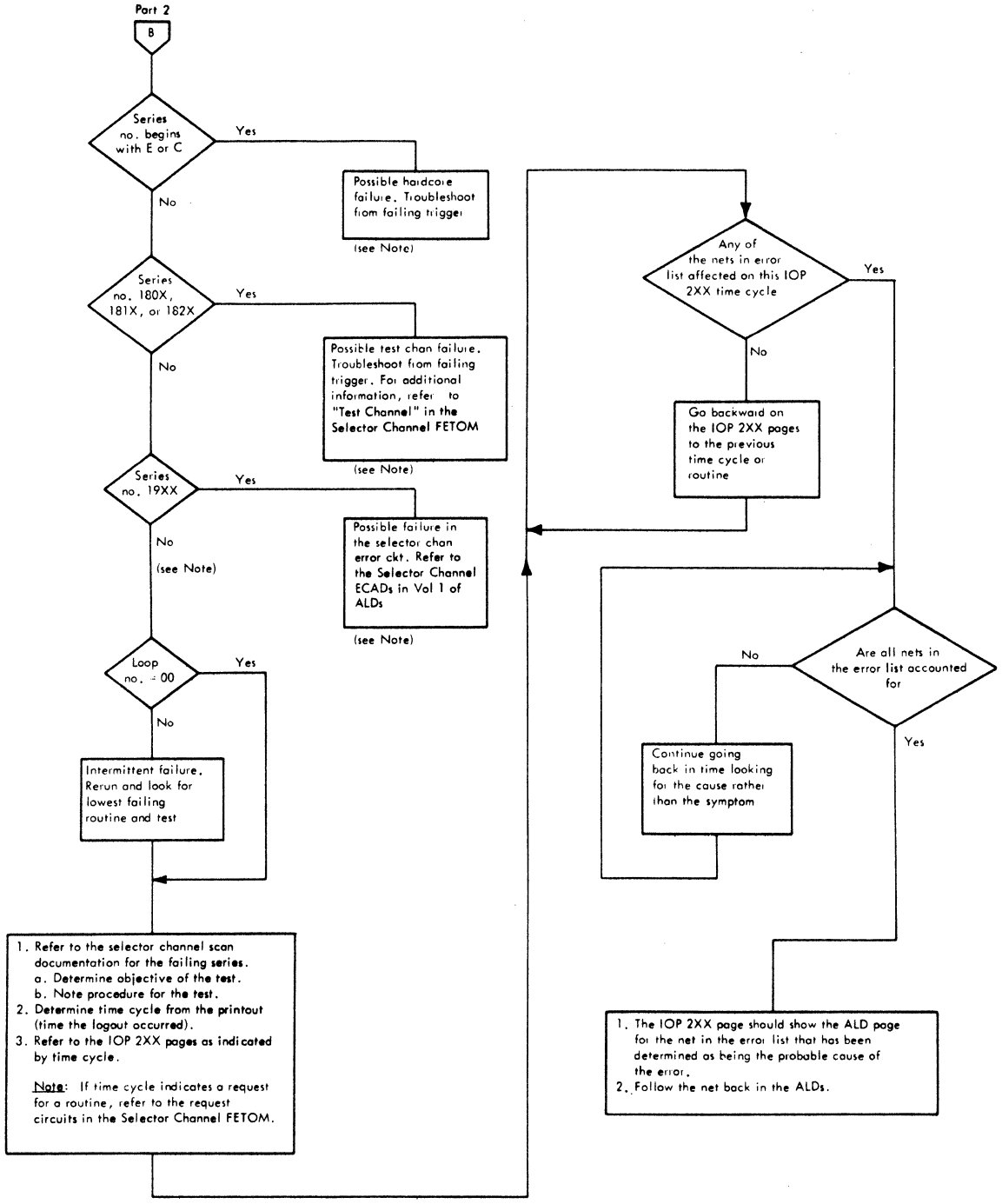


FIGURE 43. SELECTOR CHANNEL PROGRESSIVE SCAN RUN AND REPAIR PROCEDURE (PART 2 OF 3)



Note: Scoping Loop:
Do IAR repeat on the diagnose address for the failing test. Use FC5 ROS address for sync.
To check length of test, scope 01A C3C5D06.
Negative shift is the end of test.
To see the indicators as they are at the end of test lift IAR repeat switch.

FIGURE 43. SELECTOR CHANNEL PROGRESSIVE SCAN RUN AND REPAIR PROCEDURE (PART 3 OF 3)

LOCATION	CONTENTS	TEST 01	PROGRAMMING SOURCE LANGUAGE		COMMENTS
001000			ORG	AA+4096	X'1000'
001000			DS	OD	
			DC	X'8300'	
			DC	AL2(YSL13)	
			DC	X'00080001'	
		1	DC	F'0'	
001000	8300		DC	X'8300'	
001004	0F08		DC	AL2(YSL13)	SCAN-IN IF + H REG
001008	08A00001		DC	X'08A00001'	SET IF A0, SCAN, CH1 BITS 4, 8, 10, 31=1
00100C	00000000		DC	F'0'	ZERO H REG
001010	6600		DC	X'6600'	PSS=SS=1 C=3
001014	133E	2	DC	AL2(KC50FL)	RESET EXT CHAN--CECC1
001018	6600		DC	X'6600'	PSS=SS=1 C=3
00101C	1F96		DC	AL2(KC480L)	RESET COM + MPX CHANS--CECC6
001020	0400		DC	X'0400'	
001024	1E58		DC	AL2(YSG1FL)	SCAN-IN I/O, M,L,R REGS--4 WORDS
001028	00000000		DC	F'0'	ZERO I/O REG
00102C	01000290	3,4,&5	DC	X'01000290'	M REG = OP, DA(1,290)
001030	00000100		DC	X'00000100'	L REG = UA, CH(0,1)
001034	00000300		DC	X'00000300'	R REG + SP, CA(0,300)
001038	0000		DC	X'0000'	
00103C	1E10	6	DC	AL2(YSL13L)	SCAN-IN IF + H REG
001040	18A00001		DC	X'18A00001'	SET IF A1,SCAN,CH1,BITS 3,4,8,10,31=1
001044	00000000		DC	F'0'	ZERO H REG
001048	4600	7	DC	X'4600'	PSS=SS=1 C=2
00104C	120A		DC	AL2(KC051L)	START I/O
001050	0400		DC	X'0400'	
001054	1E12	8	DC	AL2(ULC73L)	LOGOUT COM, MPX, SEL CHANS--17 WORDS
001055			DS	17F	LOGOUT AREA

Refers to steps of test 01 shown on Figure 45.

FIGURE 44. TEST SERIES 110.1 TEST 01 (DIAGNOSE SECTION--START I/O WRITE SERIES)

TEST 01	TEST 02	TEST 03	TEST 04
1. Stop on A0	1. Repeat Test 001 steps 1-7	1. Repeat Test 001 steps 1-7	1. Repeat Test 001 steps 1-7
2. CECC 1,6	2. Stop on Clock Step	2. No clock Stop	2. No clock stop
3. Scan into L (UA and Ch)	3. Link to Logout	3. Link to Logout	3. Link to NOP 919 C=3 (break in will occur)
4. Scan into M (Op code and DA)			4. Link to Logout
5. Scan into R (SP tag and CA)			
6. Stop on A1			
7. Link to St I/O (905 - QK 700) C=2			
8. Link to Logout			
St I/O C1 A1	Req St I/O Rtne	Req St I/O Rtne	Break In St I/O Rtne

FIGURE 45. TYPICAL TEST SERIES (SERIES 110)

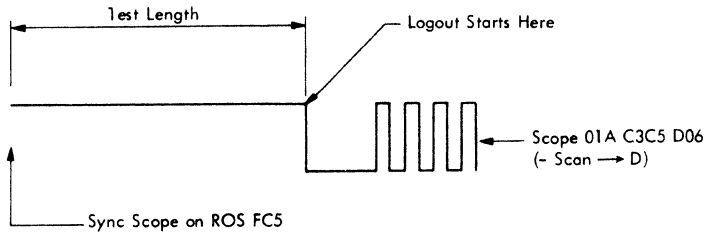


FIGURE 46. SCAN TEST TIMING PROCEDURE

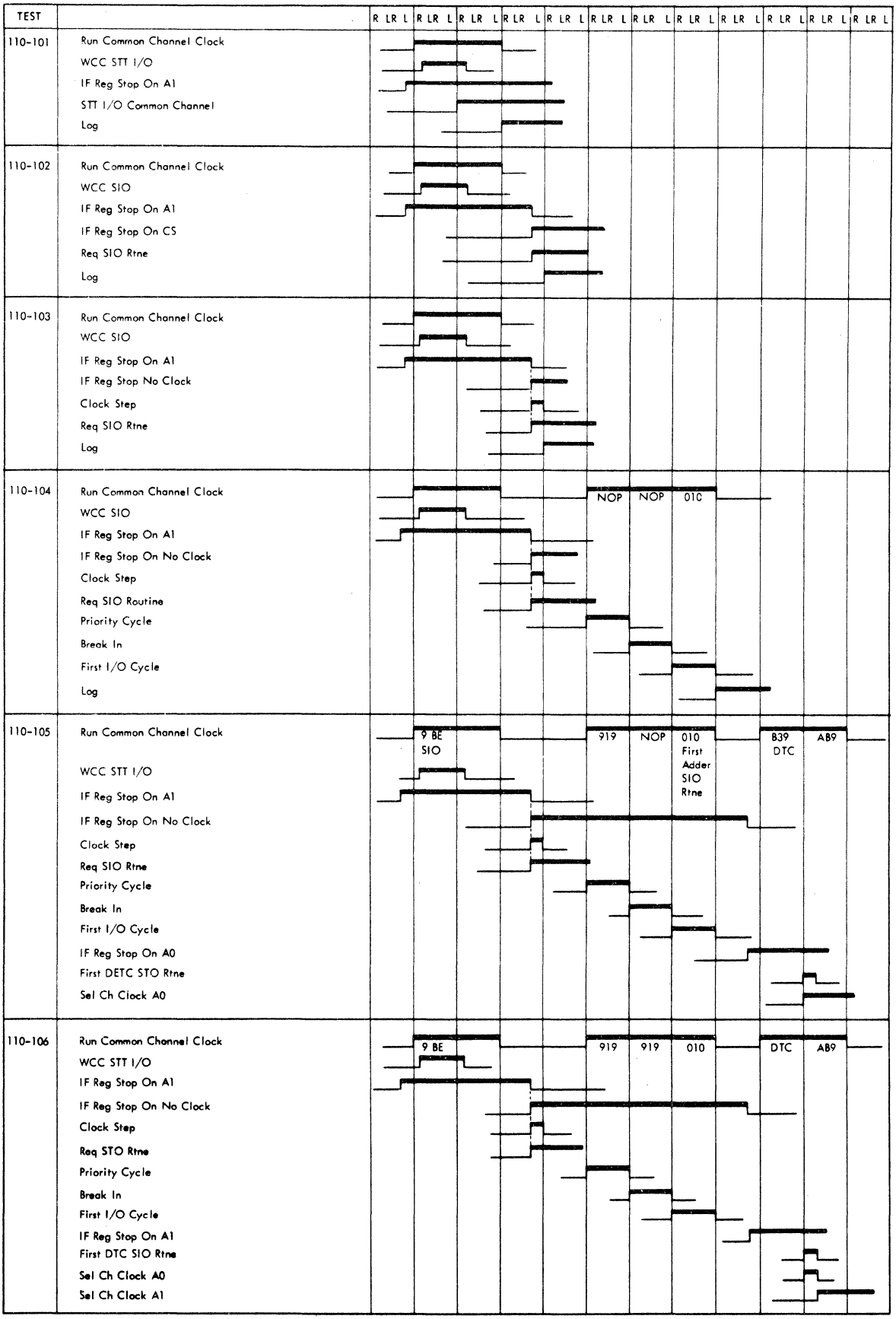


FIGURE 47. START I/O WRITE TIMING

I/O routine and the common channel breaks in. However, since the common channel clock is stopped, the detect registers will not turn on even though the selector channel has provided a priority request.

Reg SIO Routine -- 110-103: This test is the same as the previous test, except that the clock pulse is allowed to run at normal machine speed (100 ns) rather than be at a dc level at logout. After the start I/O trigger is turned on, the IF register is set to allow the selector channel clock to advance from A1 through clock step. A logout is taken at this time.

Break-In SIO Routine -- 110-104: The channel is reset and the L, R, and M registers are set prior to diagnosing to start I/O. The IF register allows the selector channel clock to advance past clock step as in test 03. Because the selector channel has a priority request pending, the only requirement of the common channel is that it turn on a detect register and break in to the CPU. Because the common channel clock is stopped, it is necessary to get it running to break in. This is done by diagnosing to a ROS NOP (919) for a count of three. A count of three allows for a break-in and execution of the first microinstruction of the I/O routine. An exit can be made from the routine to a linkage control word at this time in order to prepare the IF register (selector channel clock) for any DTC's in the I/O routine. A logout is taken at break-in time.

First DTC A0 SIO -- 110-105: The channel is exercised to exactly the same place as in the previous test at logout time. It has executed the first microinstruction of the start I/O routine. An exit is now made from the I/O routine, and the IF register is set to stop the selector channel clock on A0. Next the linkage control word goes to the next ROS address in the routine for a count of two in order to issue the DTC to the channel. When the DTC is issued, the selector channel clock steps to A0. A logout is taken here.

First DTC A1 SIO -- 110-106: Everything is the same as the previous test except when an exit is made from the I/O routine after break-in, the IF register is set to stop the selector channel clock on A1. The diagnose instruction calls on the second microinstruction of the SIO routine for a count of two, and the selector channel stops on A1. A logout is taken.

Remaining tests are applied in the same fashion. The selector channel is forced to a known state (not necessarily a reset state). Then the common channel is run to break in and issue DTC's. However, it is necessary to set the IF register in order to control the selector channel clock.

Test Patterns

The method used to obtain the good patterns is to apply the tests, logout the common and selector channels, and record the logout data as "good machine" patterns. Tests identical to those used for pattern generation are run, and the logout is compared to the pattern residing in storage. If a mismatch is sensed, the same type of information as provided in the selector channel clock test is given.

Selector Channel Tape or Disk

The tests on tape and disk appear in the following sequence:

1. Hardcore -- These tests check the hardware needed for running the progressive scan tests.
2. Common Channel -- These tests check the common channel for channel 0 operations (or channels 1, 2, or 3, depending on the system configuration).
3. Selector Channel -- These tests exercise the external selector channel.

The tests are arranged so that the greatest coverage occurs in the first few series.

The first two records contain the progressive scan selector channel control program which is used to compare the logout of the machine to a known good logout. The print section of this control program prints or types a heading and a list of the failing triggers. The heading contains the test number and name, the time of failure (log point), the sync point, the loop number (used for detecting intermittents) and the diagnose address (for looping).

Selector Channel Clock Control

Progressive scan tests the common channel and selector channel together. Both the common and the selector channel clocks are controlled by the diagnose instruction. Tests can therefore be run so that selector channel A clock can be stopped on any clock pulse for each data transfer control (DTC) signal issued by the common channel.

Either a DTC signal or a pulse from the IF register will start the A clock, causing the clock to advance through one cycle. DTC must fall to allow the clock step control signal to rise (Figure 48). Clock outputs then initiate a series of predetermined channel actions. The particular routine performed determines the number of DTC signals sent to the selector channel.

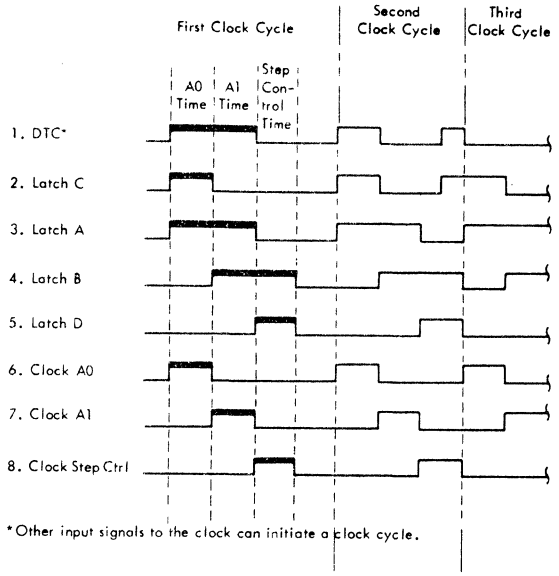


FIGURE 48. SELECTOR CHANNEL A CLOCK: SIGNAL SEQUENCES

The common channel clock (I/O clock) is inhibited by the diagnose word placing a bit in the IF register. The supervisory stat allows the clock to run for a given number of cycles.

The diagnose instruction begins from a normal I fetch and is executed in the following fashion:

1. The quantities (B) + D and the immediate data field are assembled in the storage data register (SDR) and stored into main storage (hex address 80). From the SDR, bit 8 of (B) + D is put into the I/O mode stat. Bits 20-31 of (B) + D are put into ROAR. Simultaneously immediate data bits 1-3 are put into the sequence counter, bit 5 is put into the supervisory enable storage stat, and bits 6 and 7 are put into the progressive scan stat and the supervisory stat respectively.

2. ROS now begins executing microinstructions starting from the address put into its address register.

3. If the supervisory stat is on, the CPU clock is advanced synchronously with the sequence counter. When the counter reaches zero, the progressive scan stat is tested.

4. If the progressive scan stat is on, the word following the diagnose instruction is fetched from main storage and used as a linkage control word. Bits 19-30 of this word are put into ROAR. At the same time, bits 0-2 are put into the sequence counter, bit 4 is put into the supervisory enable storage stat, bits 5 and 6 are put into the progressive scan stat and the supervisory stat, and bit 7 is put into the I/O mode stat. ROS begins executing microinstructions starting at the address put into ROAR, and step 3 is repeated. This sequence can be extended any number of storage words, allowing the programmer to execute any number of ROS words in any desired order. This is the case in progressive scan.

Selector Channel Operating Procedure Example

The selector channel operating procedure can be summarized as follows:

1. Run all tests, printing either T(for terminate) or fail.

2. Run all tests again and print out the results of the error logout for each routine and load the next routine. When this is finished, by looking at the failing tests you can determine which test to loop on and then

3. Loop on the selected failing routine, bypassing error printouts to allow scoping.

Note: The complete progressive scan operating procedure for the selector channel is on page MC000-01, in Volume 1 Reference of Systems Diagrams.

Selector Channel Test Documentation

Figure 49 shows the type of printout supplied by the selector channel progressive scan tests. A test failure in either or both the common channel and selector channel is printed out. From this printout, the following information may be obtained:

1. Test number - Example: 1921-14.

2. Test name - Indicates what operation is being performed; for example, IF Control Ck-Op In Test.

3. Test cycle - Defines the point in operation at which the failure occurred; for example, Unit Select Drop Op In.

4. Sync point - ROS address for syncing; for example, ROS FC5.

5. Loop number - Tells the number of times the test was run before a failure occurred; for example, 00.

6. Diagnose address - Address to use to loop on the failing test for scoping. This is accomplished by setting IC to the diagnose address and using the repeat IAR switch; for example, 1FD8.

```
SELECT OPTIONS IN 5010 AND INTERRUPT.

01  0Y ----          PRINT T OR FAIL FOR EACH RTNE.
06  0Y XXXX          PRINT FIRST ERROR OF EACH RTNE.
                     LOOP ON RTNE XXXX.
07  0Y XXXX          PRINT T OR FAIL FOR EACH RTNE.
                     LOOP ON RTNE XXXX.
08  0Y ----          SUPPRESS T PRINTING.
0A  0Y XXXX          SUPPRESS T PRINTING.
                     LOOP ON RTNE XXXX.
0D  0Y----           LIST FAILING RTNES.
12  0Y XXXX          LOOP ON TEST TT OF ROUTINE XXXX.
TT                   SDR CONTAINS ADDRESS OF DIAGNOSE
 T  E001             INSTRUCTION FOR LOOPING.
 T  E011             <- E indicates hardcore
 T  E021
 T  C001
 T  C101             <- C indicates common channel
 T  C111
 T  C011
 T  C121
 T  1000
 T  1011
 T  1021
 T  1022             <- Series
 T  1031
 T  1032
 T  1101             <- Routine
 T  1102
 T  1903
```

Storage location 5010 = WW0YXXXX

WW refers to MCxxx pages in Volume 1 of ALD Maintenance Diagrams
Y denotes channel number:
- 01 = channel 1
- 10 = channel 2
- 11 = channel 3

XXXX denotes series and routine

Storage location 5014 = TT (if EC 255458 or above)

TT denotes test number

```
                    (XXXX)  (TT)
TEST NUMBER         1921 - 14      TEST NAME      IF CONTROL CK-OP IN TEST
TIME CYCLE          Unit-Select-Drop-OP IN
SYNC POINT          ROS FC5        (Number of successful times through the test loop.)
LOOP NUMBER         00   Diagnose Adr   1FD8  <- (Address to be placed in address keys to loop on this test.
                                                  IAR repeat key must be used to loop.
                                                  Caution: This test must be in core.)
1ST CHARACTER INDICATES GOOD PATTERN  <- (What the result should have been)
CHANNEL 1 IS SELECTED IN 5011
1  GG131AC4  24  CH CHK SIM
1  GE101AM4  30  CH CK IF CL  <- (Example 1)
1  GA131AP4  29  CC PH A SP0
0  GB181AG4  02  PREG UNIT SEL
1  GB181AT4  05  PREG END UP
0  GA131AT2  09  CC PHASA ST2
1  GB151AG4  17  REQ R PR13  <- (Bit description)
1  GB101AC4  21  REQ REG 3
1  GV111AJ4  19  STOP REL
0  GS111AJ4  31  ENBL STAT IN
0  GR101AQ4  21  OP IN TEST
0  GR101AD4  23  SEL OUT
1  GB171 AV4 28  POS REG TRF  <- (Example 2)
Fail 1921
                                Bit position (see NOTE)
                             Net (block AV line 4)
                          ALD page number
```

NOTE- Refers to a position in one of the selector channel indicator rows (1-6). Note that positions 28-31 indicate one of two possible bit positions.

Example 1 (position 30) indicates the actual bit position (30) on roller row 3.

Example 2 (position 28) indicates the parity bit position for 0-7 on roller row 5.

To find the indicated bit you must compare the description with the selector channel roller charts. The parity positions that are now shown as 28-31 will soon be shown as positions 32-35 to eliminate this condition.

The error printout portion (1921-14) indicates an interface control check failure. Using the selector channel IF control check page (E1411-01), or the analysis page (E1321-01) in Volume 1 of ALD Maintenance Diagrams, the failure can be quickly diagnosed.

To see if an indicator is on while looping IAR on the diagnose address, raise the repeat IAR switch and look at roller position. Lower switch to resume looping.

FIGURE 49. PROGRESSIVE SCAN PRINTOUT (SEL CH)

Selector Scan Monitor

Locations of information within the selector scan monitor are as follows:

EC Level 255458 and Above

Main Storage Location	
5F00	Diagnose address of current instruction.
5F04	Current test number.
5F08	Diagnose address of previous instruction.
5F0C	Previous test number.
6F00-0E	Output printer addresses. If none on your
6F01-0B	system, store proper address in 6F03.
6F02-09	That is, 6F03-xx (active device).

EC Levels Below 255458

Local Storage GP Register	
00	Bits 22 and 23 determine which selector channel is in operation
09	Add one to contents of this reg to get number of times test was executed (including failure).
10	May be diagnose address (current) if between 1000 and 4000. Anything outside of this range is useless.
11	Contains the main storage address of the last test number executed.

Main Storage Location	
66D3	Address of output device. Normally 00E and must be changed if this is not your printer address.
66D7	Typewriter address. Normally 009.

To call next record from tape or disk, press reset PB and then load PB (if then in manual state, press start PB).

Multiplexor Channel Tape or Disk

The tests for the multiplexor channel appear in the following sequence:

1. Hardcore -- These tests check the hardware needed for running progressive scan tests on the multiplexor channel.
2. Common Channel -- These tests check out the hardware in the common channel needed for multiplexor channel operations.
3. Hardcore Check of I/O Stats, Buffer 1, and Buffer 2.
4. Multiplexor Channel Tests -- These tests exercise the external multiplexor channel.

The tests are arranged so that the greatest coverage occurs in the first few series.

The first record on tape contains the multiplexor channel progressive scan control and display program. This program compares the logout with a known good logout pattern for each test and displays in indicators the information needed for trouble-shooting when a failure is detected.

Multiplexor Channel Operating Procedure

The complete progressive scan operating procedure for the multiplexor channel is on page MC000-02 in Volume 1 of the ALD Maintenance Diagrams.

Multiplexor Channel Test Documentation

Hardcore and functional test documentation will take the form of flow charts and timing charts describing the series and the log points. These documents are in Volume 1 of the ALD Maintenance Diagrams.

DIAGNOSTIC PROGRAMS

Figure 50 is a list of Model 50 diagnostics. Each diagnostic is described in the documentation generated for it. Standard documentation for diagnostic programs consists of five major sections.

1. Purpose
2. Prerequisites
3. Use procedure
4. Printouts
5. Comments

Note: Disable ROS retry by jumpering 01C-E3C4D11 to a D08 pin before running or biasing FLT's, diagnostics, or progressive scan.

MIDAS replaces diagnostic programs F101X through F1F6X.

MIDAS Sense Switches

Number	Usage	Number	Usage
0	Inhibit isolation	12	Test loader device
1	Lock CPU high	13	Unassigned
2	Lock CPU low	14	End report period
3-4	Unassigned	15	Extend report period
5-7	Isolation No. 0-7	16-17	Device control
8	Isolate	18	Alter output device address
9	Unassigned		
10	Loop isolation No. in 5-7	19	Unassigned
		20-31	Unit address
11	Terminate		

MIDAS Display Codes

Wait Codes

IAR Display	Cause
AAAAAA	Program interrupt
FFFFFF	Program interrupt
CCCCCC	SVC interrupt
999999	Machine check
000A9A	Machine check
000C14	External interrupt
000000	Input device failure on initial load

Program Section Number	Program Description	Normal Voltage	Marginal Voltages							
			Ch	CPU	Local Storage		Main Storage		Storage Protect	
			6M1	6M2	6TC	6VAR	56 XY	60Z	Vsl	Vref
			+6.0v +0.5v -0.5v	+6.0v +0.5v -0.5v	Opt ±5%	Opt ±5%	Opt ±4.5%	Opt ±4.5%	Opt ±6%	1.4v ±10%
MIDAS	CPU Tests	1 Pass		1 Pass						
5340X 5341X 5342X	Diagnose and Error Circuits	1 Pass		1 Pass						
E381X	60 Cycle Int Timing	1 Pass		1 Pass						
E383X	50 Cycle Int Timing	1 Pass		1 Pass						
F38FX	Meter Timing	1 Pass		1 Pass						
5391X thru 5397X 5066	Main Storage Tests	1 Pass			1 Pass	1 Pass				
53C1X	Local Storage	2 Min			2 Min	2 Min				
53C4X	Bump Storage	2 Min					2 Min	2 Min		
E3C9X	Storage Protect	2 Min		2 Min					2 Min	2 Min
E421X thru E426X	Mpx Channel Using 1442	1 Pass	1 Pass							
E428X thru E42BX	Mpx Channel Using 2540	1 Pass	1 Pass							
E441X thru E446X	Sel Channel Using 2400 Each Channel	1 Pass	1 Pass							
F4D0X F4D1X	Channel-to Channel Feature	1 Pass	1 Pass							
F4E1X F4E2X	Direct Control	1 Pass		1 Pass						
5F01X 5F02X	1410 Emulator Instructions	1 Pass		1 Pass						
5F03X 5F04X	1410 Emulator Ch Translators	1 Pass	1 Pass							
5F21X 5F23X thru 5F2AX	7074 Emulator Instructions	1 Pass		1 Pass						
5350	ROS Ripple	1 Pass	1 Pass at limits of -12 ROS voltage							

FIGURE 50. MODEL 50 DIAGNOSTICS

Flashing Lights

AAAAAA and 555555 in IAR alternating every four seconds indicates output device not ready.

FF0000 and 00FFFF in IAR alternating every second indicates crisis.

MARGINAL CHECKING

Marginal checking is a technique used to detect the marginal operation of the most voltage-sensitive circuits in the system. These circuits have nominal levels of voltage and current at which they are designed to function. Each circuit operates within certain margins (regulator output voltage limits above and below the nominal rating). However, aging and other factors cause a gradual deterioration in the operating characteristics of the circuits. By raising and lowering the regulator output voltage within the design margins, it is possible to inspect all the circuits powered by that voltage. On the basis of this inspection, any circuit approaching a failure condition may be replaced. This type of check is made periodically as a preventive-maintenance technique. Marginal checking is useful also as an aid in locating operator-reported failures. Costly down time and many trouble calls can be avoided by using marginal checking to make failures less intermittent and more recognizable.

Nominal Voltages

The following regulators and their nominal outputs can be marginally checked:

Regulator	Nominal Output
1	+6 TC
1	+6 VAR
12	-12 ROS
3	+6 M1
4	+6 M2
14	+56 XY1
15	+60 Z1
16	+56 XY2
17	+60 Z2

Marginal Voltage Limits

The system control panel meter is color banded to show the marginal voltage limits. The actual marginal voltage limits are dependent on the results obtained by running shmoo-curves. The following are the specified operating limits.

Regulator	Voltage Limits for Testing
1 (+6 TC)	±5% of the optimum local storage setting
1 (+6 VAR)	±5% of the optimum local storage setting
12 (-12 ROS)	±2 volts of the optimum ROS setting
3 (+6 M1), 4 (+6 M2)	±.5 volt
14 (+56 XY1), 15 (+60 Z1), 16 (+56 XY2), 17 (+60 Z2)	±4 1/2% of the optimum main storage setting

Note: Storage drivers may be damaged if these voltages exceed +68 volts.

Marginal Checking Procedure

All marginal checking controls and indicators are mounted on the system control panel. Each control has an indicator which is activated whenever the margin control is adjusted from its nominal level. Each control varies the output of one regulator. The independent control of each regulator allows several inputs to the same circuit to change at any one time. The marginal voltage select switch determines which voltage is monitored by the meter.

ERROR CHECKING

Identification

All units of the Model 50 are identified, grouped, and provided with a hardware-checking scheme that detects errors at the unit, indicates them at the system control panel, and identifies them as to unit (for instance, power and overload sensing, cooling, data flow, address checking, channel errors, etc.). I/O errors occurring in a device or a control unit are not included except for their effects on the channels. Each CPU failure detection device has a unique indication in the error register.

Failure Detection Facilities

The data flow of the CPU is checked in eight-bit bytes. Control information is checked in bytes of varying length.

Power and Cooling Failure Detection

Power and overload failures are indicated by lights on the maintenance console. The specific unit at fault is indicated by a tripped circuit breaker or light in the power distribution unit (PDU).

Thermal failures (cooling) are indicated on the maintenance console by lights, one for each frame (CPU, storage, PDU).

CPU Parity Checking

The adder is parity checked and three levels of failure detection are provided: half-sum check, carry check, and full-sum check (adder output latch check).

A half-sum check indicates either incorrect parity on data entering the adder or a failure in the adder half-sum generation circuitry. The carry check indicates a failure in the carry lookahead circuitry. Full-sum checking, which is performed on the adder output latches, checks that correct parity has been generated for the developed sum, or that data entering the adder output latches from an external source (data keys, address keys, selector channel, etc.) has correct parity.

Because the adder is located in the data path between any two registers, it is used as the primary failure detection device for all register-to-register transfers. The adder output latch check also provides the checking for all transfers to and from main storage.

The mover is parity checked at both inputs as well as its output.

The three main groups of bits emerging from ROS are parity checked. Length counters G1 and G2, the L and M byte counters, and the MD counter are also parity checked. Control failures which are not covered by error detection circuitry, in general, cause data errors. For instance, a failure of the adder ingates would result in an invalid no-bit sum in the adder output latches.

SAR is also parity checked.

Timing Considerations

With the exception of the carry, mover output, and full-sum checks, all CPU failures cause the machine status to be frozen the cycle in which the error is detected. This is done by stopping the clock in time to prevent the set register pulse of the next cycle, thereby blocking the register ingating and preserving the contents of all registers.

The carry, mover output, and full-sum checks, however, are detected too late in the CPU cycle to block the next set register pulse. As a result, the clock is stopped one cycle later than the cycle in which the error is detected. In this case, the address of the microinstruction that was controlling the machine during the actual error cycle (previous ROS address) is available in a ROS address backup register. With this address available it is possible to "backup" to the previous cycle for error analysis.

Check Register

Each parity check circuit sets a unique bit in the check register. The table below shows the bit assignment for each position of the check register.

Bit 0	Half-Sum 0-7
Bit 1	Half-Sum 8-15
Bit 2	Half-Sum 16-23
Bit 3	Half-Sum 24-31
Bit 4	Sum 0-7
Bit 5	Sum 8-15
Bit 6	Sum 16-23
Bit 7	Sum 24-31
Bit 8	Carry
Bit 9	L Byte Counter
Bit 10	M Byte Counter
Bit 11	MD Counter
Bit 12	Length Counter (G1)
Bit 13	Length Counter (G2)
Bit 14	Mover Left Input
Bit 15	Mover Right Input
Bit 16	Mover Output
Bit 17	Unused
Bit 18	Storage Address Register 8-15
Bit 19	Storage Address Register 16-23
Bit 20	Storage Address Register 24-31
Bit 21	ROS 1-30
Bit 22	ROS 32-55
Bit 23	ROS 57-89
Bit 24	Storage Protect
Bit 25	Reserved for LCS Summary Check
Bit 26	Log Request
Bit 27-31	Reserved for Expansion

Bit 26 is turned on by the logout key or by the channel requesting an error logout. It may not represent an actual CPU error.

The error register is displayed on the system control panel and is included in the logout information. It can be reset by the check reset or system reset pushbuttons or by the diagnose instruction. It is automatically reset at the conclusion of an error logout immediately prior to the machine check interrupt.

Multiplexor and Selector Channel Parity Checking

The multiplexor and selector channel data flow and addressing are parity checked on the following data paths and registers:

Control Checks	Interface Checks
Byte Counter Parity	Multiple Tags
Address Out Parity	Address In Parity
Operation Parity	Address Compare
Routine Response	Status Parity
Routine Positional	Time-out
End Control Validity	

In addition, the following CPU failure detection circuits are active: SAR, mover, adder, and ROS.

Data entering or leaving the interface is parity checked as is all data transferred between the channel and CPU (adder full-sum check). Detected data errors are not propagated into storage on read operations; data is cycled through the adder to correct the parity before it is stored (disable mode), or an error logout and machine check interrupt occur (process mode).

I/O Errors

I/O errors are handled by IOCS. No I/O error indicators are displayed on the maintenance console.

Main Storage Parity Checking

All main storage checking is performed in CPU. The adder output latches provide parity checking for all transfers to and from storage, because they are located in the data path between the storage data register (SDR) and the CPU working registers. The storage address register (SAR) is also parity checked.

The following data error handling rules apply during Model 50 storage operations:

1. On a fetch operation, data set into SDR and regenerated without being transferred into CPU is not checked. Checking occurs only when the word is transferred through the adder output latches into one of the CPU working registers. An error detected in this word sets the error register whether it is in an addressed byte or not.
2. During a store operation, data from CPU is checked on a full word basis even though only a portion of the word may be set into SDR. An error detected in this word sets the error register

whether it is in the addressed byte or not. Depending upon when the error is detected, three different actions occur with respect to SDR:

a. If the error is detected as SDR is being set (latch check), the data is stored uncorrected.
b. If the error is detected as the data to be stored is passing through the adder (half-sum check), SDR does not set to the data and zeros are stored instead. The bytes of SDR which were to be replaced with data from CPU will have been reset.
c. If the error is detected after storage selection but in the cycle prior to the cycle in which SDR is set, the store operation is converted to a fetch and the data is regenerated without checking.

3. No checking is performed on data read from the cores during a store operation.

A preventive maintenance schedule for the Model 50 is shown on Figure 51. The asterisked items indicate the frequency that should be used for the first six months of system operation. Because component failures are more frequent during the first six months of operation, frequent preventive maintenance will minimize unscheduled maintenance during that period.

Preventive maintenance should be performed at a critical time, such as the first thing Monday morning or immediately after power has been down for an extended period.

Lamp Test

Use the lamp test switch on the maintenance panel to test and replace all defective lamps. Marginal voltage, frame thermal, open CB, and power check lamps are not tested by the test switch, but should be checked by substitution or by duplicating the situation that would cause the lamp to indicate. The lamps are pluggable and can be replaced from the front of the pannel. Use CE tool #461420 for removing lamp assemblies.

Diagnostics

Run all diagnostics (CPU and channel multiprograms using all multiplexor and selector channels available in order to get a maximum configuration in overlapped operation).

For biasing, vary the marginal check voltages per the marginal check specifications before running the diagnostics. Test for both upper and lower marginal check limits while running the diagnostics. Figure 50 is a listing of Model 50 diagnostics.

Unit	Item	Installation	Frequency (Weeks) 1	2	4	8	13	26	52
CPU	Lamp Test (Page 79)	X	*	X					
	Run Diagnostics and FLT's (Page 74)	X	*			X			
	Bias Diagnostics and FLT's (Page 74)	X				X			
CPU and Channel	Run CPU and Channel Control Multiprogram	X	*			X			
	Bias CPU and Channel Control Multiprogram	X				*		X	
Channel	Run Diagnostics (Page 74)	X	*			X			
	Bias Progressive Scan (Page 74)	X			*	X			
Main Storage (Includes Bump and Storage Protect)	Run Diagnostics (Page 74)	X	*			X			
	Bias Diagnostics** (Page 84)	X			*	X			
Local Storage	Run Diagnostics (Page 74)	X	*			X			
	Bias Diagnostics** (Page 76)	X			*	X			
	Check Array Temperature (Page 92)	X						X	
ROS - Retry	Check Timing (Page 95)	X						X	
Power System	Make Visual Checks	X						X	
Miscellaneous	Check Filters/Screens	X			X				
	Check Fans/Blowers	X						X	
	Check Usage Meter	X					X		

*Denotes frequency during first six months of operation. (A diagnostic listing is shown on Figure 50.)

**Biasing in these cases means checking operation at the four corners of the shmoo plot limits; that is, the corners of the rectangle in local storage and the corners of the rectangle in main storage whose sides are at least 4.5% (of the operating point voltages) away from the operating point.

FIGURE 51. MODEL 50 PREVENTIVE MAINTENANCE SCHEDULE

CPU AND CHANNEL SERVICE CHECKS

Waveform Measurements

All waveform measurements for the 2050 Processing Unit are made to the following specifications (Figure 52):

1. The rise time of a pulse is the time required for the transition from 0.3 volts to 1.8 volts as the pulse is going in a positive direction.
2. The fall time of a pulse is the time required for the transition from 1.8 volts to 0.3 volts as the pulse is going in a negative direction.
3. The width of a pulse is measured from the 1.0 volt point at the beginning of the transition on the leading edge to the 1.0 volt point at the beginning of the transition of the trailing edge.
4. The delay between pulses is measured from the 1.0 volt point at the beginning of the transition of the leading edge of the first pulse to the same point on the next pulse.

2050 Clock

The 2050 clock consists of a 4-megacycle oscillator, which is frequency divided to 2 megacycles, and a number of circuit delays which can be adjusted. Oscillator pulses are shaped, delayed, and powered to meet all system requirements.

All 2050 clock timings are on ALD AA000 in Volume 1 of the ALD's.

MAIN STORAGE (MS) SERVICE CHECKS

Storage Test

A rotary switch on the panel selects one of four test patterns to be applied to main storage. When the rotary switch is in the fifth position (process), the test light is off (in the operator control section). The four test positions are:

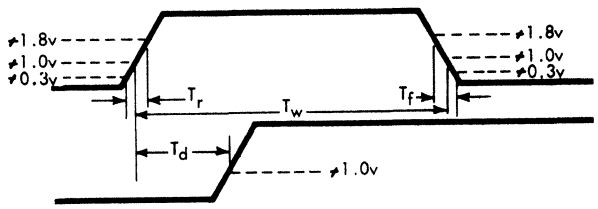
1. All ones
2. All zeros
3. Worst pattern
4. Reverse worst pattern

To operate the storage test:

1. Set the rotary switch to one of the four desired positions.
2. Press the start pushbutton.
3. Set the write lever switch down to write the desired pattern into storage. When the write lever is down, SDR contains all ones regardless of the position of the rotary switch.
4. Return the write lever switch to its normal position to read/regen storage.
5. With the stop on check lever down, IAR contains the address of the error word. Each depression of the start pushbutton resumes storage scanning until the next error word is detected.

Main Storage Test Points

Figure 53 shows important test points for the main storage unit.



T_r = Rise Time
T_f = Fall Time
T_w = Pulse Width
T_d = Delay

FIGURE 52. WAVEFORM MEASUREMENTS

Bit	A Segment	B Segment	C Segment	D Segment	Gate Pin M9A Strobe Pin M9	Sense-Amp Output	Final Amp In	Final Amp Out
0	B1L2 B3/B4	B1K2 B3/B4	B1L4 B3/B4	B1K4 B3/B4	B12	B7	B1J4 G10	B1J4 G12
1	B1L2 D5/D6	B1K2 D5/D6	B1L4 D5/D6	B1K4 D5/D6	B13	D7	B1J4 G9	B1J4 J12
2	B1L2 B8/B9	B1K2 B8/B9	B1L4 B8/B9	B1K4 B8/B9	D12	G2	B1J4 G3	B1J4 D2
3	B1L2 B10/D10	B1K2 B10/D10	B1L4 B10/D10	B1K4 B10/D10	G4	D13	B1J4 G2	B1J4 J05
4	B1J2 B3/B4	B1H2 B3/B4	B1H4 B3/B4	B1G4 B3/B4	B12	B7	B1J4 J2	B1J4 J4
5	B1J2 D5/D6	B1H2 D5/D6	B1H4 D5/D6	B1G4 D5/D6	B13	D7	B1J4 D13	B1J4 B9
6	B1J2 B8/B9	B1H2 B8/B9	B1H4 B8/B9	B1G4 B8/B9	D12	G2	B1J4 B5	B1J4 B2
7	B1J2 B10/D10	B1H2 B10/D10	B1H4 B10/D10	B1G4 B10/D10	G4	D13	B1J4 D7	B1J4 D11
8	B1G2 B3/B4	B1F2 B3/B4	B1F4 B3/B4	B1E4 B3/B4	B12	B7	B1J4 J9	B1J4 G13
9	B1G2 D5/D6	B1F2 D5/D6	B1F4 D5/D6	B1E4 D5/D6	B13	D7	B1C2 G10	B1C2 G12
10	B1G2 B8/B9	B1F2 B8/B9	B1F4 B8/B9	B1E4 B8/B9	D12	G2	B1C2 G9	B1C2 J12
11	B1G2 B10/D10	B1F2 B10/D10	B1F4 B10/D10	B1E4 B10/D10	G4	D13	B1C2 G3	B1C2 D2
12	B1E2 B3/B4	B1D2 B3/B4	B1D4 B3/B4	B1C4 B3/B4	B12	B7	B1C2 G2	B1C2 J5
13	B1E2 D5/D6	B1D2 D5/D6	B1D4 D5/D6	B1C4 D5/D6	B13	D7	B1C2 J2	B1C2 J4
14	B1E2 B8/B9	B1D2 B8/B9	B1D4 B8/B9	B1C4 B8/B9	D12	G2	B1C2 D13	B1C2 B9
15	B1E2 B10/D10	B1D2 B10/D10	B1D4 B10/D10	B1C4 B10/D10	G4	D13	B1C2 B5	B1C2 B2
16	B1B2 B3/B4	A1M2 B3/B4	B1B4 B3/B4	A1M4 B3/B4	D12	B7	B1C2 D7	B1C2 D11
17	B1B2 D5/D6	A1M2 D5/D6	B1B4 D5/D6	A1M4 D5/D6	B13	D7	B1C2 J9	B1C2 G13
18	B1B2 B8/B9	A1M2 B8/B9	B1B4 B8/B9	A1M4 B8/B9	D12	G2	A1J2 G10	A1J2 G12
19	B1B2 B10/D10	A1M2 B10/D10	B1B4 B10/D10	A1M4 B10/D10	G4	D13	A1J2 G9	A1J2 J12
20	A1L2 B3/B4	A1K2 B3/B4	A1L4 B3/B4	A1K4 B3/B4	B12	B7	A1J2 G3	A1J2 D2
21	A1L2 D5/D6	A1K2 D5/D6	A1L4 D5/D6	A1K4 D5/D6	B13	D7	A1J2 G2	A1J2 J05
22	A1L2 B8/B9	A1K2 B8/B9	A1L4 B8/B9	A1K4 B8/B9	D12	G2	A1J2 J2	A1J2 J4
23	A1L2 B10/D10	A1K2 B10/D10	A1L4 B10/D10	A1K4 B10/D10	G4	D13	A1J2 D13	A1J2 B9
24	A1H2 B3/B4	A1G2 B3/B4	A1J4 B3/B4	A1H4 B3/B4	B12	B7	A1J2 B5	A1J2 B2
25	A1H2 D5/D6	A1G2 D5/D6	A1J4 D5/D6	A1H4 D5/D6	B13	D7	A1J2 D7	A1J2 D11
26	A1H2 B8/B9	A1G2 B8/B9	A1J4 B8/B9	A1H4 B8/B9	D12	G2	A1J2 J9	A1J2 G13
27	A1H2 B10/D10	A1G2 B10/D10	A1J4 B10/D10	A1H4 B10/D10	G4	D13	A1E4 G10	A1E4 G12
28	A1F2 B3/B4	A1E2 B3/B4	A1G4 B3/B4	A1F4 B3/B4	B12	B7	A1E4 G9	A1E4 J12
29	A1F2 D5/D6	A1E2 D5/D6	A1G4 D5/D6	A1F4 D5/D6	B13	D7	A1E4 G3	A1E4 D2
30	A1F2 B8/B9	A1E2 B8/B9	A1G4 B8/B9	A1F4 B8/B9	D12	G2	A1E4 G2	A1E4 J5
31	A1F2 B10/D10	A1E2 B10/D10	A1G4 B10/D10	A1F4 B10/D10	G4	D13	A1E4 J2	A1E4 J4
P 0-7	A1D2 B3/B4	A1C2 B3/B4	A1D4 B3/B4	A1C4 B3/B4	B12	B7	A1E4 D13	A1E4 B9
P 8-15	A1D2 D5/D6	A1C2 D5/D6	A1D4 D5/D6	A1C4 D5/D6	B13	D7	A1E4 B5	A1E4 B2
P 16-23	A1D2 B8/B9	A1C2 B8/B9	A1D4 B8/B9	A1C4 B8/B9	D12	G2	A1E4 D7	A1E4 D11
P 24-31	A1D2 B10/D10	A1C2 B10/D10	A1D4 B10/D10	A1C4 B10/D10	G4	D13	A1E4 J9	A1E4 G13

FIGURE 53. MAIN STORAGE TEST POINTS

Main Storage Addressing

Figure 54 shows the inputs and functions of SAR for both main and bump storage addressing.

Main Storage Temperature and Humidity

The operating temperature for the main storage unit must be between 60° and 90°F, and the relative humidity must be between 20% and 80% with a maximum wet bulb temperature of 78°F. There can be only a two-degree maximum difference in the temperature between two arrays of one main storage unit.

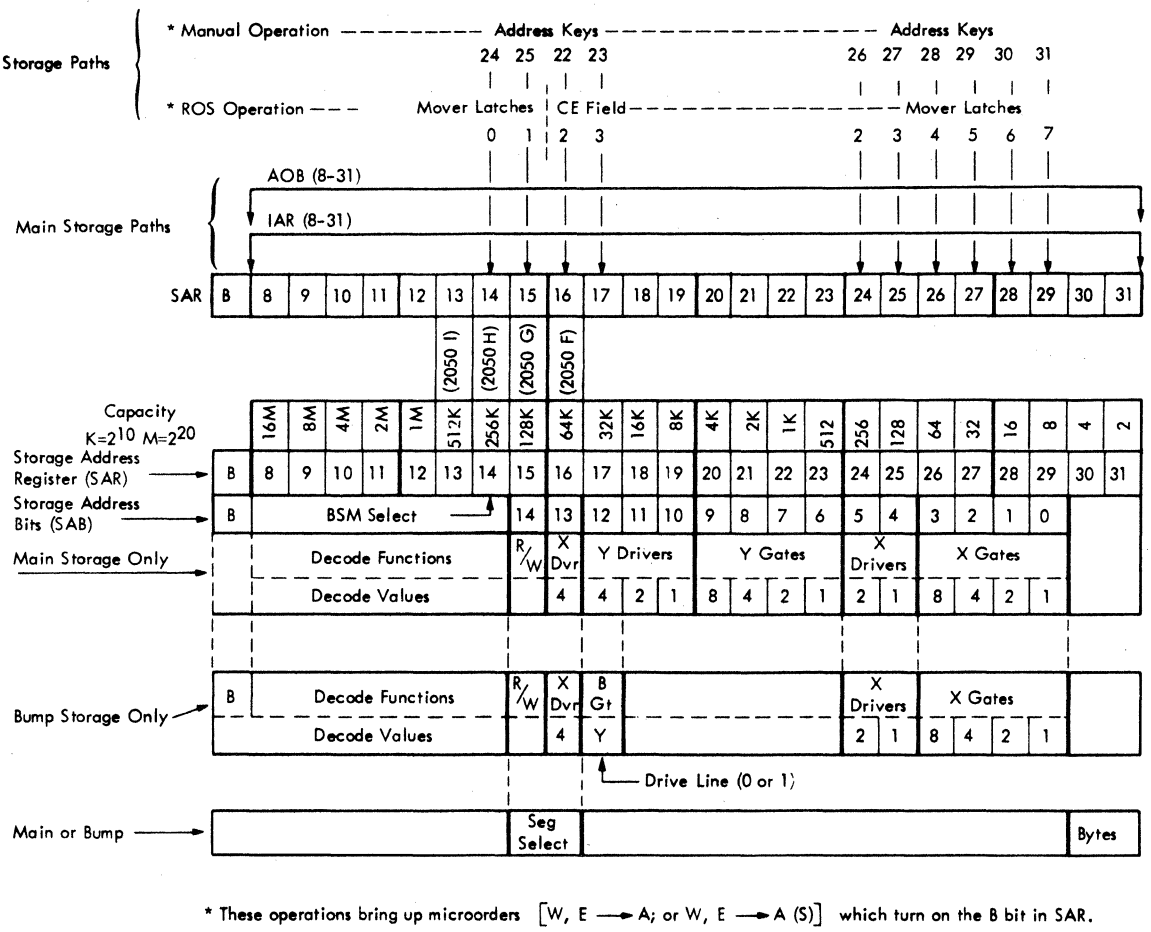
Main Storage Power Information

The +60 volt XY and Z supplies are manually variable between 48 and 68 volts and are temperature-compensated.

Measure dc voltages at the logic cards under dynamic conditions. All voltages have a ±2% tolerance.

Voltage	Amps	Over-voltage Setting	Under-voltage Setting	TB-1 Pins	Wire Color	Type
-3.0	12.0	-4.5	---	1, 15	Yellow	Logic
+3.0	5.0	+4.5	---	2, 13	Grey	Logic
+6.0	12.0	+9.0	5.2	3, 11	Orange	Logic
+18.0	4.5	+22.0	---	9	White	Special
+60.0XY	2.0	+68.0	---	5	Red	Tracked
+60.0Z	8.0	+68.0	---	7	Blue	Tracked

Upon sensing an under voltage on the +6.0 volt supply, the unit should stop cycling within 20 milliseconds and drop power.



* These operations bring up microorders [W, E → A; or W, E → A (S)] which turn on the B bit in SAR.

FIGURE 54. MAIN AND BUMP STORAGE ADDRESSING

Exercise Bump Storage

To exercise the bump storage portion of main storage, tie 01A-B1H7B12 (SAR B Bit) to ground before running any main storage diagnostic.

Continually Address One MS Location

To address a single main storage location continually, the following ROS routine 202 (QW111) may be used:

1. Set IC to the selected address.
2. Place ROS repeat switch in down position.
3. Set data keys to ROS routine 202, and press start pushbutton.

Scan MS for Bad Parity

A simple program for a full storage scan, checking for bad parity, follows:

Location 0 - 00000000
Location 4 - 00000008
Location 8 - 41101004
Location C - D2041000
Location 10 - 100047F0
Location 14 - 00080000
GP-1 should contain hex 18

This program will scan storage to the error. With the check switch in the stop position, the machine will stop and the failing address will be indicated in SAR, SDR will contain the bad data, but the storage location will have been changed by the program.

Bit Arrangement of MS Word

A full word in main storage is arranged as follows:

Bits 0-7	Byte 0
Bits 8-15	Byte 1
Bits 16-23	Byte 2
Bits 24-31	Byte 3
Bit 32	Parity for byte 0
Bit 33	Parity for byte 1
Bit 34	Parity for byte 2
Bit 35	Parity for byte 3

Check Strobe of Main Storage

To check the main storage strobe, use the following procedure:

1. Use pin B1J4J09 (ALD MC051) in the main storage frame as the test point for strobe A. This is the bit eight (segment A or C) pre-amp output.

2. Run the "all ones" test and adjust your scope to the same scale as Figure 55.

3. Make sure the strobe falls 120 ± 10 nanoseconds prior to the peak of the output signal and then run a shmoo curve.

4. If the shmoo curve picks or drops bits before it makes the established limits, re-adjust the 5-nanosecond delay tap to obtain the best shmoo for both "all ones" and "all zeros."

5. Realize that if the strobe is set near point b (Figure 55) the tendency is to pick bits and if the strobe is set near point c, the tendency is to drop bits.

6. For strobe B use pin B1C2J09 (ALD MC081) as a test point and repeat steps 2-5.

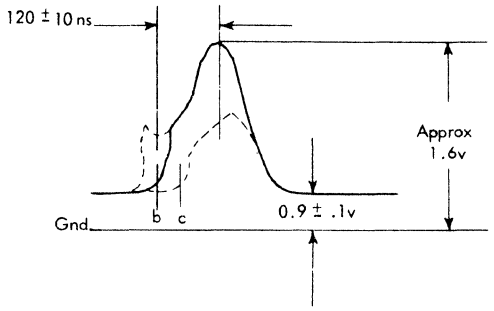


FIGURE 55. MAIN STORAGE STROBE

Checking MS Drivers and Terminating Diodes

Much time is lost in machine storage areas in observing waveforms with a voltage probe. Remember that a line with little or no current on it will appear the same as a good line if you use a voltage probe. If you suspect blown drivers or terminating diodes, use a current probe.

1. Drop dc power on the machine.

2. Locate the card whose outputs you want to scope and extend it with a card extender.

3. On the extender, locate the line you want to scope, remove the short jumper wire (Figure 56), and replace it with a longer wire. This will give you a sufficient loop with which to hang the current probe.

4. Bring up power and observe the pulse.

5. Always drop dc power when changing or removing driver, or the jumper wire on extended drivers.

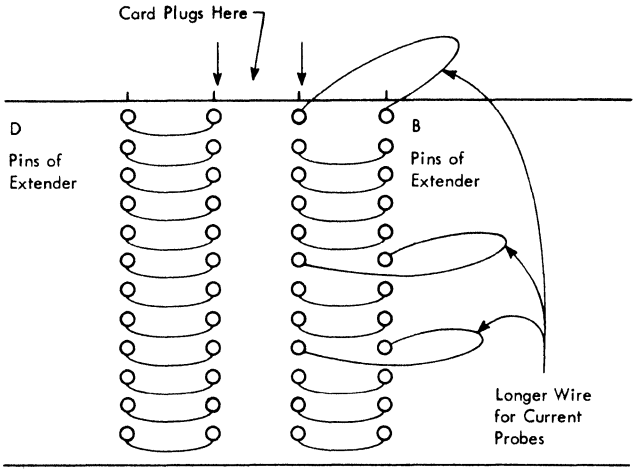


FIGURE 56. CARD EXTENDER JUMPER WIRE

Delay Line Clock

Timings taken from the A1C6 delay line (Figure 57) are used to set timing latches. Timings from the A1F6 delay line are used to reset timing latches. Changing the set master reset timing on the A1C6 card also changes all timings taken from the A1F6 card. Timings from the A1B6 delay line are used to set the strobe turn-ons.

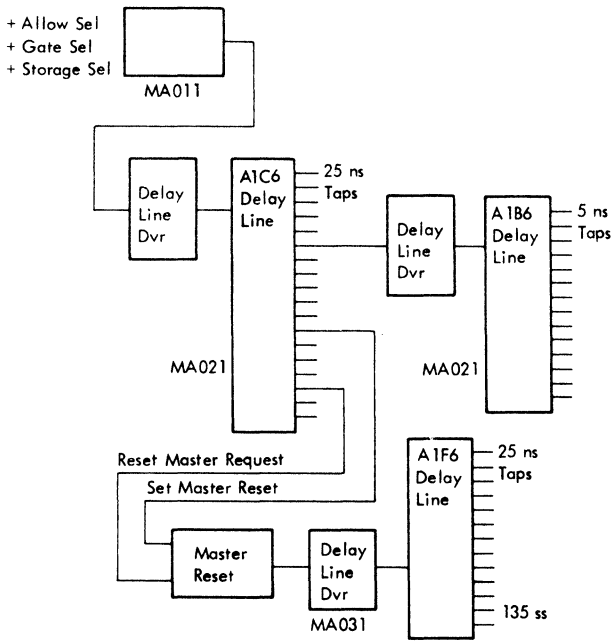


FIGURE 57. DELAY LINE CLOCK

Two singleshots (135 ns and 450 ns) in the clock section of the M9/M9A should be checked and adjusted. The 450-ns singleshot (A1H6D09) prevents any read reset pulse during the first part of a read cycle. If the 450-ns singleshot does not fire, check the +18-volt power supply.

When scoping main storage, especially the clock section, the best place to sync the scope is write control at A1H6J07. All timing is with respect to plus store select as it appears at A1H6G05.

X read/write driver timing (A1H6B07) and Y read/write driver timing (A1H6J05) should be a 2.5- to 3.0-volt signal. A pulse of less than 2.5V decreases driver current and causes random failures. The read-write latch is a 6.0-volt pulse. If zeros cannot be read, check to see that strobes A and B at A1J6G12 and A1J6J04 are present.

Delay Line Driver

In checking the delay line card (4906), be sure that the input to the delay line driver 02A-A1C6D11 is a positive pulse (Figure 58). The output of the delay line driver (02A-A1C6J11) should be the same as the input.

If the output of the delay line driver (02A-A1C6J11) has ghost pulses between the normal pulses, the delay line is open and the card should be changed. If there is no pulse at 02A-A1C6J11 on delay line card (4906), the delay line driver may be bad. If changing the card does not correct the pulse, there is probably something shorting out the delay line (for example, a cold flow on one of the yellow timing wires). Check the yellow timing wires associated with the delay line card to see if any of them are pulled tight around a pin and shorting out. The timing chart on ALD Page AA001 should be used if any storage timings are changed.

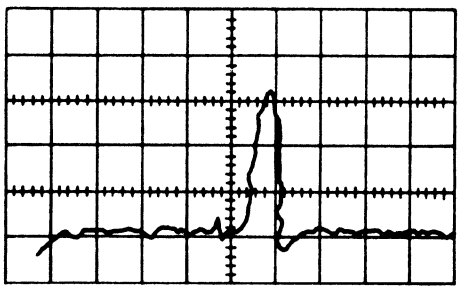


FIGURE 58. INPUT TO DELAY LINE DRIVER

Layout of M9/M9A Plane

Figure 59 is a block diagram of the M9/M9A read-write drive system. Layout of the planes is in Figure 60.

X drive lines in Figure 60 on pins 6 through 69 go through all 18 planes to the D2 board on the back of the array, jumper down, and come back through all 18 planes on pins 228 through 291. X drive lines on pins 80 through 143 go through the array to the D2 board, jumper down, and come back through the array on pins 154 through 217.

Use a current probe when checking the drive circuits. Currents should be checked on the gray wires to card locations B1M2 and B1G6 on the BSM. The X current will be on the gray wires to pins G03 and J04. The Y current will be on the gray wires to pins D12 and B12.

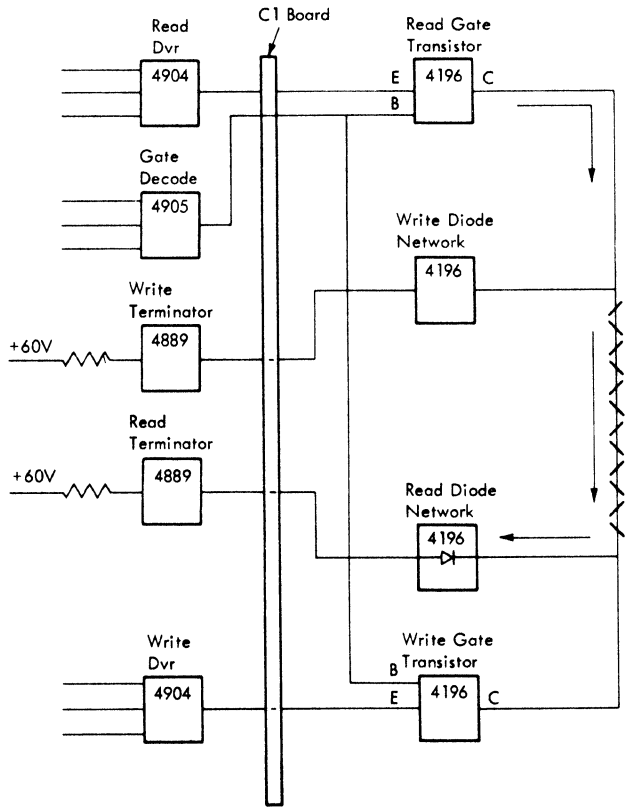


FIGURE 59. M9/M9A DRIVE SYSTEM

X Drive Current

An example of good X current is shown in Figure 61. The read pulse is longer than the write.

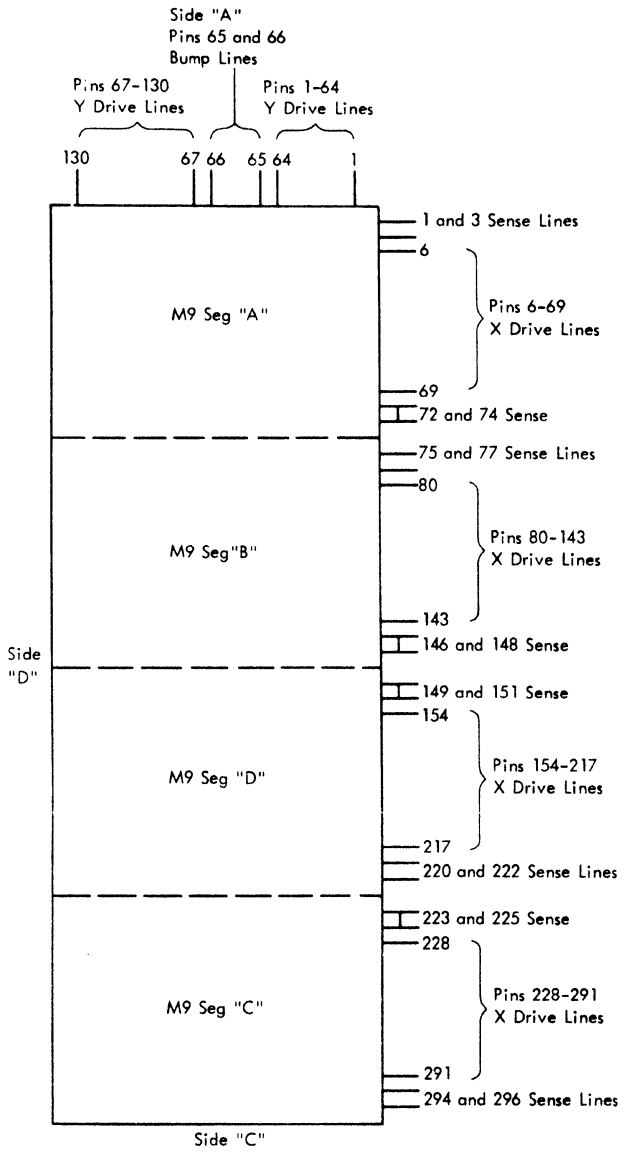


FIGURE 60. PHYSICAL LAYOUT OF M9/M9A PLANES

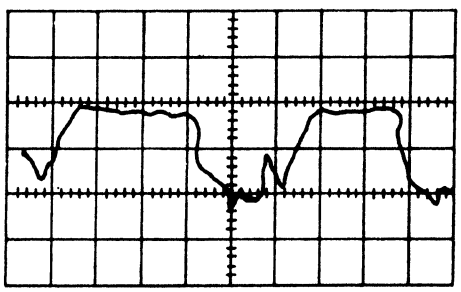


FIGURE 61. X DRIVE CURRENT

Y Drive Current

An example of good Y current is shown in Figure 62. The read and write pulses have about the same duration. Read will have a larger stagger between the terminator gate turn-on and current turn-on.

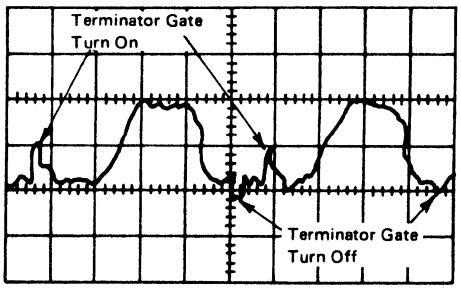


FIGURE 62. Y DRIVE CURRENT

Shorted X Drive Line

Figure 63 is a current indication of two drive lines shorted together. In Figures 63 and 64, where all of storage is cycled, the trace will be very light. These traces were taken while cycling 1/4 of storage.

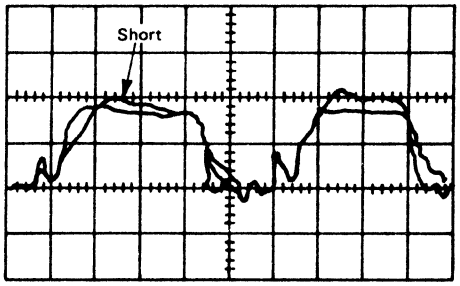


FIGURE 63. SHORTED X DRIVE LINE

Open X Drive Line

Figure 64 is a current indication of an open drive line. To locate a shorted or open drive line on the array, loop on the failing address. Using a voltage probe, lightly run the tip down the drive lines on the array. Approximately a +60-volt level will show on all the unselected drive lines. When the selected drive line is reached, a voltage drop indication occurs. With a short, the voltage indication looks

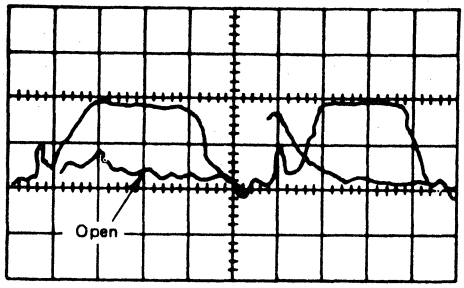


FIGURE 64. OPEN X DRIVE LINE

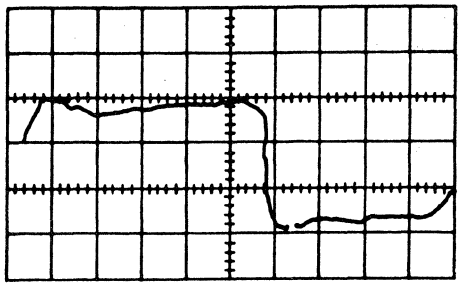


FIGURE 66. POSSIBLE OPEN DRIVE LINE

like that in Figure 65. With an open, the voltage indication resembles that in Figure 66.

With a short, the indication in Figure 65 appears on the line selected and also on the line shorted to it. The shorted lines should be adjacent drive lines. Once the shorted lines have been isolated, take an ohmmeter and walk across the array on the shorted lines until the least resistance is reached. When a resistance of nearly zero is reached, examine the area for the cause of the short. Look for drive line pins bent and touching or a metal chip between the pins. A chip may wedge under the rubber seal between planes. If the shorted lines are not adjacent, replace the gate cards (4196) associated with the shorted lines (see MD030).

An example of an open drive line is shown in Figure 66. To locate an open in the array, use a voltage probe and step across the planes of the array on the open line. When the open is passed, the indication in Figure 66 reverses--positive becomes negative, and negative becomes positive. In the area of the open, check the drive line welds for secure bonding. Remember that the drive lines zigzag across the array, and the weld may be on either side of the array. If the welds appear to be good, use an ohmmeter to isolate the open.

Drive Line Shorted to Ground

A current indication such as that in Figure 67 usually indicates that a drive line is shorted to ground. If the X current is bad, check the inhibit resistor assembly on the B-side of the array to make sure it is not shorted against the X drive lines. Three standoffs are located on the B and D side of the array and one standoff on the A and C side between the D1 board and the front frame casting. If one or more of the yellow and black wires that go to the pins on the array are pinched between the standoffs, the indication is like that in Figure 67. A shorted limiter on the gate card (4196) can cause the same indication. If a gate card might be the cause of the trouble, watch the defective current and pull the gate cards one at a time. When the defective gate card is pulled, the current is similar to normal current with an open line.

If one of the orange drive lines from the driver card (4904) on the B1 board to the array interface is shorted to ground, or if a transistor in the driver card (4904) is shorted, the indication resembles that in Figure 67. A defective gate clamp card (3583) gives a similar indication.

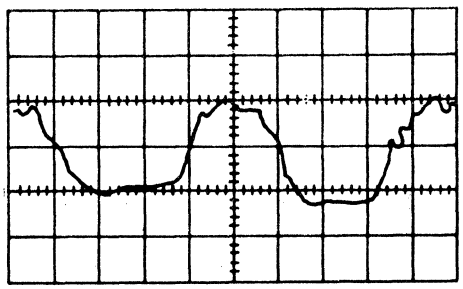


FIGURE 65. POSSIBLE SHORTED DRIVE LINE

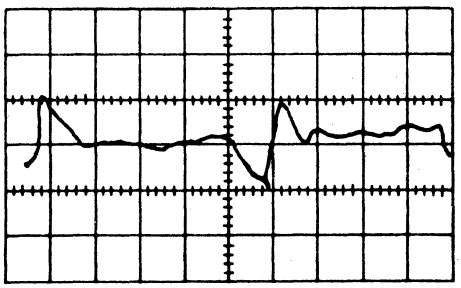


FIGURE 67. DRIVE LINE SHORTED TO GROUND

The turn-off of the driver currents should be before the terminator gate turn-off. If the current is being turned off by the terminator gate, unwanted noise in the array and bit failure may result (Figure 68). To correct this condition, replace the gate cards (4196) or drivers (4904) that have the late turn-offs. If the currents have different amplitudes (read is twice the amplitude of write, or vice versa) a bad gate terminator card (4889) is indicated.

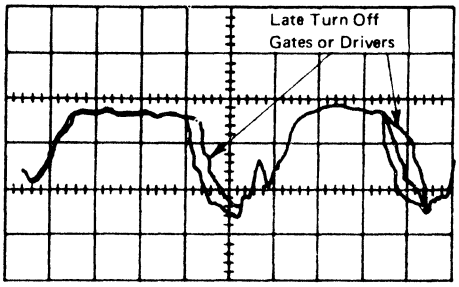


FIGURE 68. CURRENT TURNED OFF BY TERMINATOR GATE

Sense Inhibit

The sense and inhibit circuits use the same blue and white lines (Figure 69) from the logic boards, A1 and B1, to the array. The resistance of each leg of the sense-inhibit line to ground should be about 7.5 ohms. The resistance between the blue and white wires at the output of the sense-inhibit card is about 15 ohms. A normal inhibit pulse at the output of the inhibit driver card is like that in Figure 70. This pulse is the same on either the blue or the white wire.

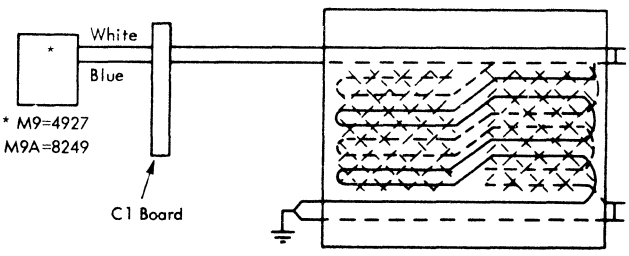


FIGURE 69. BLUE-WHITE SENSE LINES, SENSE INHIBIT

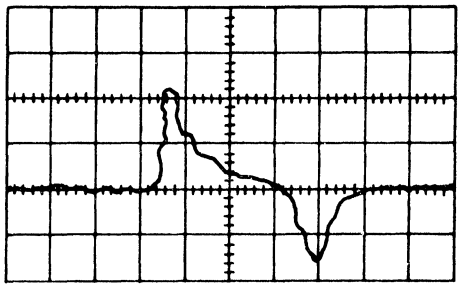


FIGURE 70. INHIBIT PULSE

When an open occurs in either leg of the sense-inhibit lines, the output of the inhibit driver is like that in Figure 71. Check continuity of the blue or white wire from the sense-inhibit card on the A1 or B1 board to where the wire welds onto the B side of the array. If continuity to the array is good, check the small jumpers on the D side of the array for the plane and segment that is bad, to see if the weld has opened up. If the welds on the jumpers are good, check the welds on the inhibit bus on the B side of the array.

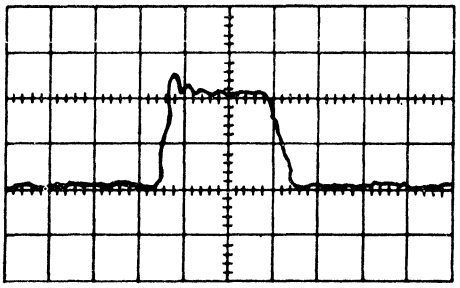


FIGURE 71. INHIBIT PULSE WITH OPEN LEG

If a short to ground in either leg of the sense-inhibit line occurs, or if the inhibit driver transistor is shorted, the output of the inhibit driver is as shown in Figure 72. If a sense-inhibit card has a shorted inhibit transistor, that segment may run and the other three segments may not run. Replacement of the sense-inhibit card for the segment that is running usually corrects the problem. If the output of the inhibit driver card still resembles Figure 72, use an ohmmeter to check the resistance of the blue and white lines. If a short to ground exists on the blue or white wire, pull the paddle card for that bit and segment (see MD020) on the C1 board to isolate it to the BSM or array.

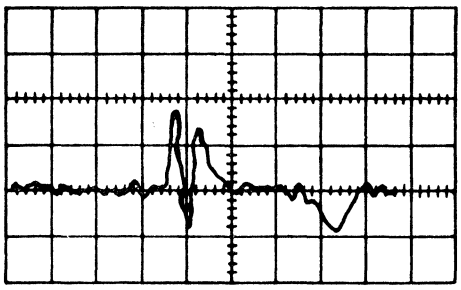


FIGURE 72. INHIBIT PULSE WITH GROUNDED SENSE INHIBIT LINE OR SHORTED INHIBIT DRIVER

The placement of the strobe turn-on is a controlling factor in the operation of the M9/M9A. To get the strobes in the approximate area of best operation look at the output of the sense amplifier card and set the strobes so that there is a small porch on the leading edge of the pulse (Figure 73). See AA000 for strobe timings of the M9 and M9A.

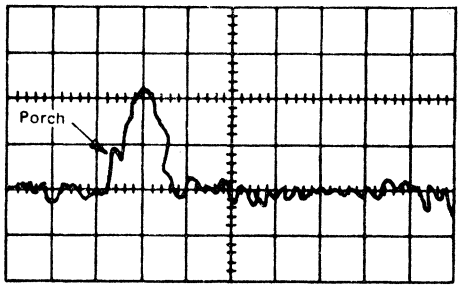
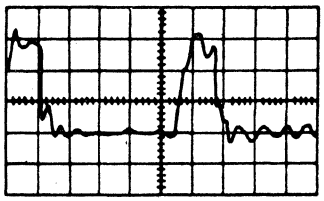


FIGURE 73. OUTPUT OF GOOD SENSE AMPLIFIER (M9 ONLY)

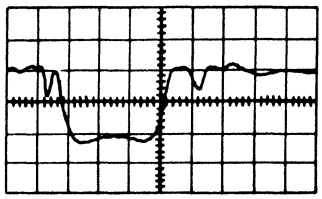
Storage Waveforms (Voltage Probe)

Figures 74-76 are waveforms for storage select, terminator gate, and X and Y gate decode and X write/read drivers. The sync point for these figures is plus read A1H6G12 (MA011). Figures 74-75 were taken while rippling storage from the storage test switch. Figure 76 was taken while continuously addressing one location. Because of phase reversal, the figures of Y drive lines have a double trace. A good scoping procedure is to scope the yellow wire on the X and Y read and write terminators (Figure 75). Scoping this point detects open, shorted, or weak drivers (see Figure 77).

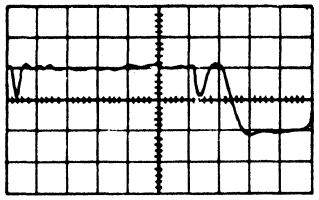


Storage Select
A1H6G05 (MA011)
0.2 us/cm; 1v/cm

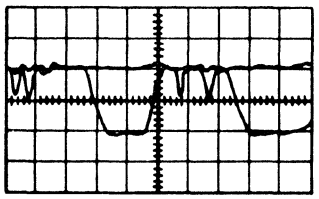
FIGURE 74. MAIN STORAGE SELECT—WAVEFORM



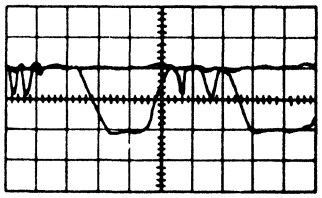
X-Read Terminator Gate
B1M2G02 (yellow wire) MB091
0.2 us/cm; 20v/cm



X-Write Terminator Gate
B1M2J02 (yellow wire) MB091
0.2 us/cm; 20v/cm



Y-Read Terminator Gate
B1M2D13 (yellow wire) MB091
0.2 us/cm; 20v/cm

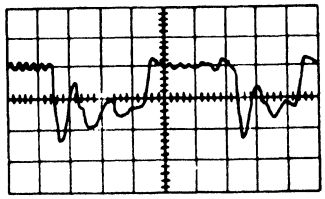


Y-Write Terminator Gate
B1M2B13 (yellow wire) MB091
0.2 us/cm; 20v/cm

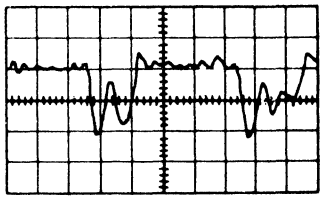
FIGURE 75. MAIN STORAGE TERMINATOR—WAVE FORMS

Sense Amplifier Output (M9)

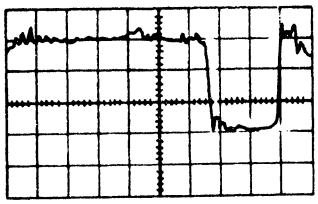
If no porch is on the leading edge of the pulse (Figure 73), the strobe turn-on is too late and should be moved earlier. If the porch on the leading edge of the pulse is too long (over 60 ns), the strobe turn-on is too early. Setting the strobes using the porch



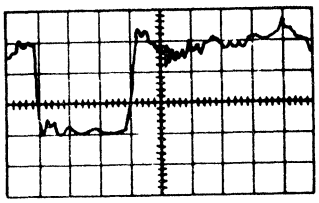
X-Gate Decode-02 Active
B1M4J07 (MB071)
0.2 us/cm; 2v/cm



Y-Gate Decode-02 Active
B1M6J07 (MB051)
0.2 us/cm; 2v/cm

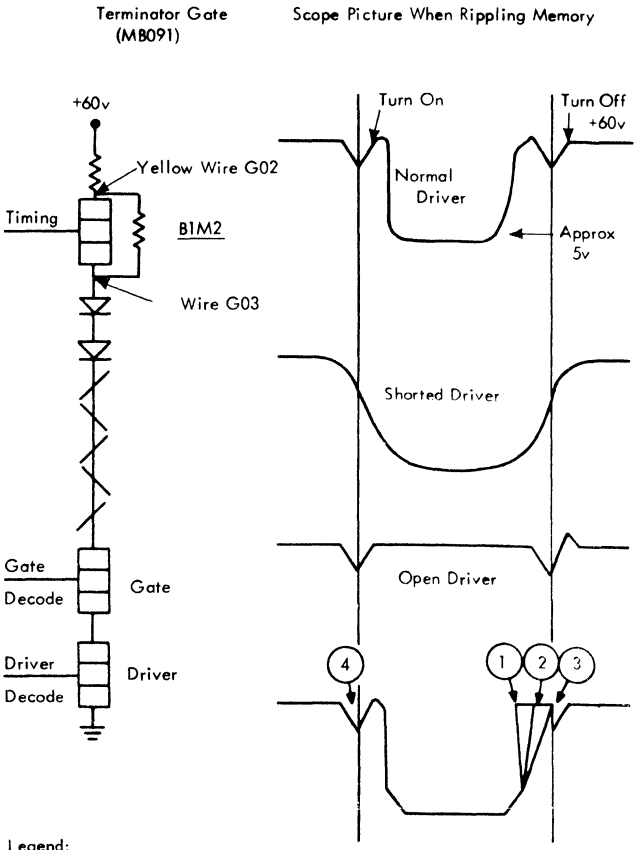


X-Write Driver-03 Active
B1N4J05 (MB101)
0.2 us/cm; 2v/cm



X-Read Driver-02 Active
B1N4G02 (MB141)
0.2 us/cm; 2v/cm

FIGURE 76. MAIN STORAGE GATE AND DRIVER PATTERNS—WAVEFORMS



Legend:
① Normal drive turn-off.
②&③ Weak drivers turn off.
④ Distorted pulse shapes can cause intermittent problems that are difficult to analyze.

FIGURE 77. MAIN STORAGE DRIVER FAILURES - WAVEFORMS

method gives an approximate area of best operation, but the final setting should be done by running a shmoo and moving the strobes to improve operation. The chart in Figure 78 shows the strobe for each segment and bit. With the aid of the chart, adjust the strobes for best operation.

M-9

Seg	Strobe A	Strobe B
A-B	Bits 9-17 Bits 27-35	Bits 0-8 Bits 18-26
C-D	Bits 0-8 Bits 18-26	Bits 9-17 Bits 27-35

FIGURE 78. STROBE FOR EACH SEGMENT AND BIT

If a bit is dropping when the XY voltage is lowered, try moving the strobe associated with that bit and segment earlier. This usually helps the operation of that bit. If a bit is picking when the XY voltage is raised, move the strobe associated with that bit and segment later. The strobe turn-off placement has little effect unless moved a great distance (75-100 ns).

M9A Differences

Drive currents are to be measured on the wires to the C1 board from pins listed in the following table.

	Bits 0 thru 17	Bits 18 thru 35
X Read	B1M2G03	B1G6G03
X Write	B1M2J04	B1G6J04
Y Read	B1M2B12	B1G6B12
Y Write	B1M2D12	B1G6D12

Figure 79 represents the sense scheme for the M9A, which is the only significant difference between the M9 and M9A. Note that the following cards are not interchangeable.

Function	M9	M9A
Sense Amp	5804927	5808249
Final Amp	5804920	5808250
Strobe	5804910	5808254
Timing	5804815	5808253

The array part number is 2511311 for both the M9 and M9A.

Figure 80 shows waveforms for the M9A BSM. The sync point is storage select A1H6G5 for all waveforms.

LOCAL STORAGE (LS) SERVICE CHECKS

Local Storage Timings

Local storage timing information is in ALD Volume 1, Page AA000.

Local storage zero time is defined as CPU 255 time.

LS Read Operation

The gate drivers and read drivers supply the current to reset the core and induce an output on the sense winding.

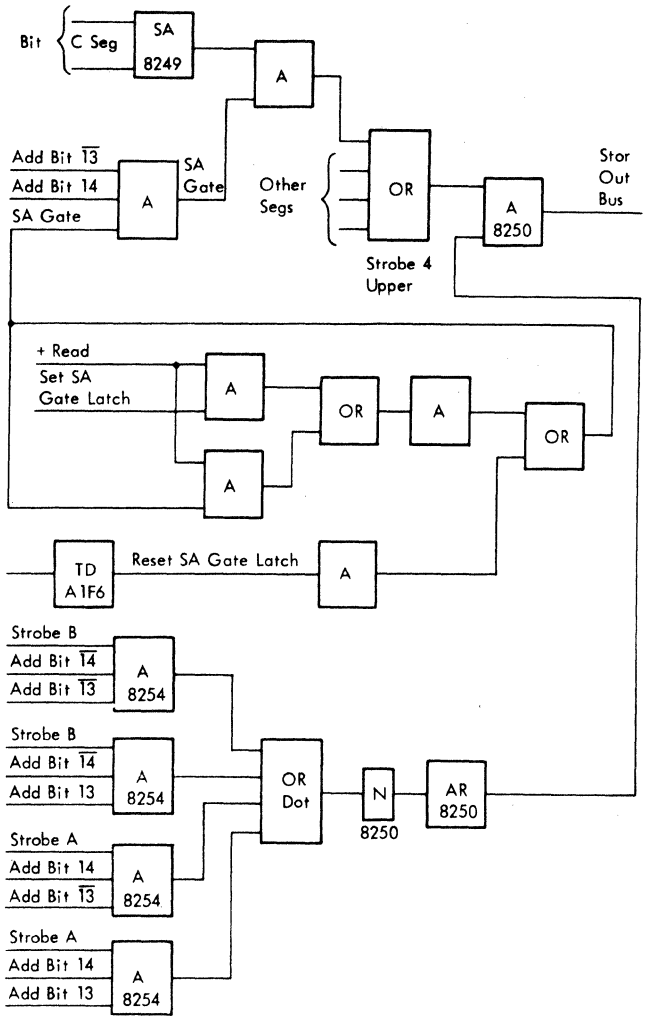
LS Write Operation

The gate drivers and write drivers select the word, and the bit drivers supply the additional current necessary to set the core. A bit driver must be on for each position to be set.

LS Functional Packaging

Local storage drivers and sense amplifiers are functionally packaged as follows:

1. The eight gate drivers are packaged four per card with one fuse per card.
2. The eight read drivers are packaged four per card.
3. The eight write drivers are packaged four per card.



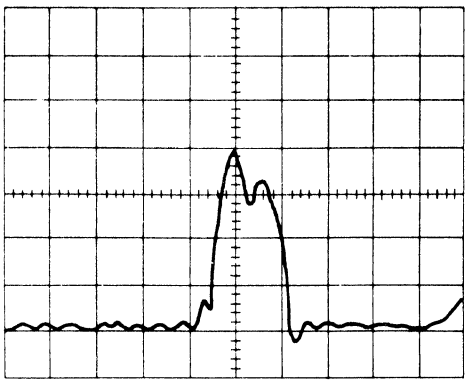
Strobe		Bits
1 Lower	=	0, 1, 2
2 Lower	=	3, 4, 5
3 Lower	=	6, 7, 8
4 Lower	=	9, 10, 11
5 Lower	=	12, 13, 14
6 Lower	=	15, 16, 17
1 Upper	=	18, 19, 20
2 Upper	=	21, 22, 23
3 Upper	=	24, 25, 26
4 Upper	=	27, 28, 29
5 Upper	=	30, 31, 32*
6 Upper	=	33, 34, 35*

Bits
32 = P 0-7
33 = P 8-15
34 = P 16-23
35 = P 24-31

FIGURE 79. M9A STROBE AND SENSE CIRCUITS

4. The 36 bit drivers are packaged four per card with four fuses per card.
5. The 36 sense amplifiers are packaged four per card.

(A)

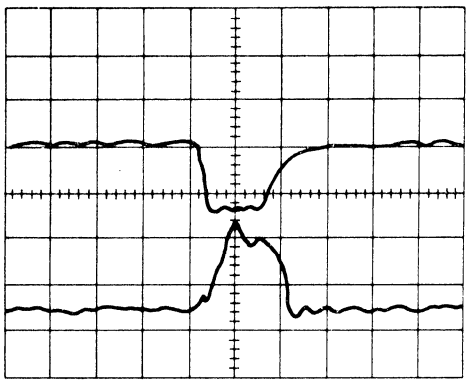


Preamp output for a 1 Bit
scope setting V/cm = .5
Time/cm = 100 ns

"A" trace = -SA strobe B1C2G04
Logic MC007

"B" trace - Preamp output = 1 Bit

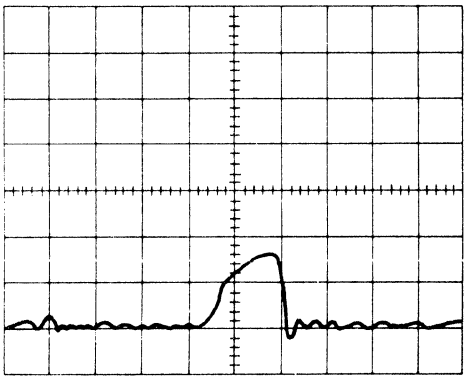
(B)



scope setting

Trace A	Trace B
V/cm = 2	1
Time/cm = 100 ns	100 ns

(C)

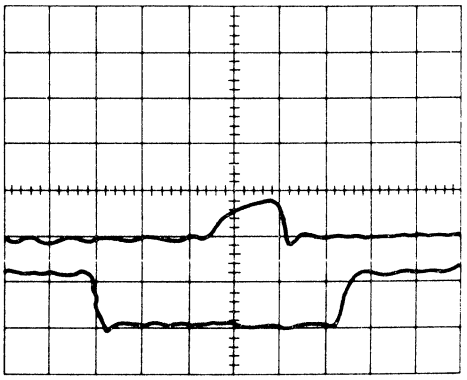


Preamp output = 0 Bit
scope setting V/cm = .5
Time/cm = 100ns

"A" trace Preamp output = 0 Bits

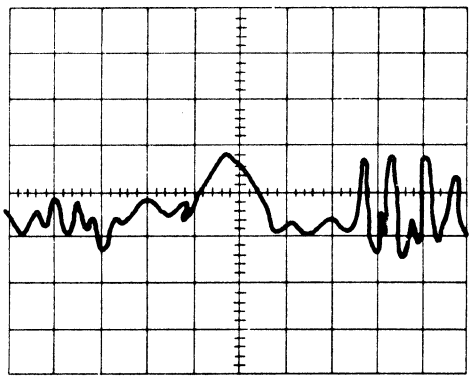
"B" trace Sense amp gate

(D)



scope setting V/cm = 1
Time/cm = 100 ns

(E)



Input to S/A = 1 Bit
(Actual core output)
scope setting V/cm = 50 mv
Time/cm = 100 ns

Note: All scope settings were made with sync point storage select A1H6G5

FIGURE 80. M9A PREAMPLIFIER OUTPUTS -- WAVEFORMS

Local Storage Word Selection

Figure 81 shows how the local storage word is selected from the six-bit address.

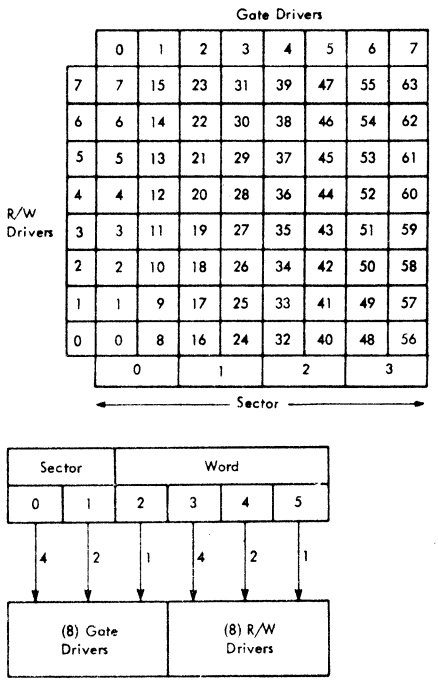


FIGURE 81. LOCAL STORAGE ADDRESS BIT FUNCTIONS

LS Temperature Control Unit Check

Following is the procedure for calibrating the local storage temperature control unit (TCU) using resistor assembly P/N 461614 and a standard 6-pac card extender P/N 452554. Proper use of this procedure results in the correct TCU setting for controlling the local storage array at a temperature of 104°F, ±1°. Resistor assembly P/N 461614 is a 1%, 8250-ohm resistor with two SLT pluggable terminals.

Initial Setup

1. Turn off all power to the local storage unit and TCU. The TCU is located in the power supply section.

Caution

The TCU has a single phase, 60 cycle, 208-230 vac input on terminals L1 and L2.

2. Remove the cover from the TCU and insure that the ac input power terminals L1 and L2 are properly insulated or enclosed. Correct any safety violation before continuing.

3. Connect the standard 6-pac extender jumpers and resistor assembly P/N 461614. Refer to Figure 82 for card plugging.

4. Remove the dust protector around the array board and unplug the SLT connector cable at the M2 location of the local storage array board.

5. Plug the SLT cable connector just removed from the M2 into the SLT pin connectors on the 6-pac extender (side opposite the jumper and resistor). Make sure that the B and D sides of the cable connector correspond to that of the 6-pac extender.

6. Plug the shroud end of the 6-pac extender into the M2 position at the local storage array board.

7. Remove the two thermistor wires connected to terminals T1 and T2, located adjacent to the input power terminals of the TCU. Using an ohmmeter calibrated against the 8250-ohm resistor, measure the resistance between these two disconnected thermistor wires. The meter should read 8250 ohms ±1%. If there is a higher resistance, check for a bad crimp or broken wire and repair before continuing.

8. Replace the two thermistor wires to TCU terminals T1 and T2.

TCU Calibration Procedure

1. With an insulated screwdriver, turn the potentiometer dial of the TCU to the extreme counter-clockwise position.

2. Turn power on the local storage and the TCU.

3. With an oscilloscope, monitor the +30 volt array heater voltage TCU return line located at D4M2D07 on the local storage array board.

4. With an insulated screwdriver, turn the TCU potentiometer dial clockwise until the heater just barely turns on. The heater is on when the oscilloscope trace at D4M2D07 is at ground; the heater is off when the oscilloscope trace is at +30 volts.

5. Turn power off. Remove the 6-pac extender and replug the connector cable into the M2 position at the array board.

6. Mark the position of the dial setting for future reference. This setting should be at the 9 to 12 o'clock position. If not, the TCU may be defective. Recheck the procedure, especially step 7 in the initial setup.

7. Correct operation is indicated by the heater being turned on and off periodically.

Local Storage Waveforms

Typical waveforms for normal storage operation are illustrated in Figures 83 through 87. These waveforms are not to be used as specifications for levels, rise times, fall times, or pulse widths, but rather as general indications of the wave shapes to be expected.

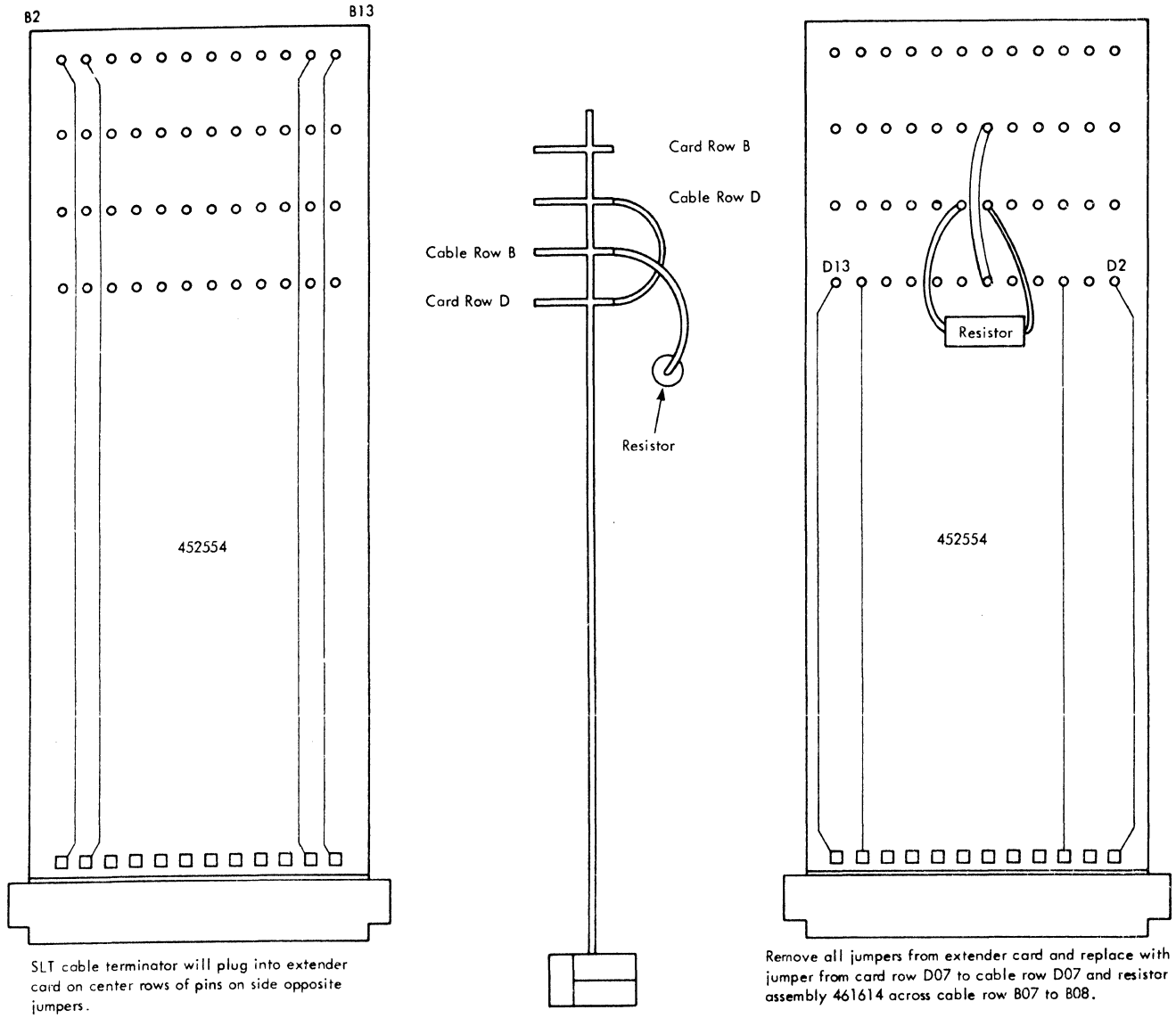


FIGURE 82. EXTENDER CARD WIRING: LS TEMPERATURE CHECK

Optimize LS Drive Currents (Shmoo)

For a triple-six supply, execute sequence A. For a single +6-volt supply, execute sequence B.

Sequence A: To optimize the +6 TC and +6 VAR voltage, plot the +6 VAR versus the +6 TC while running the worst case test program as follows:

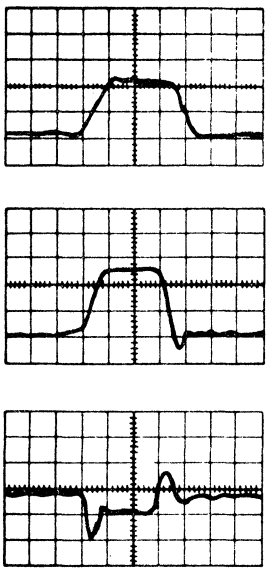
1. With all logic voltages at nominal and the +6 TC at approximately 4.5V, vary the +6 VAR to the low and high voltage failure points and record these points on the plot.

2. Increase the +6 TC by 0.5V and repeat step 1. Continue to perform steps 1 and 2 until the +6 TC can no longer be increased without a failure occurring.

3. The optimum setting of the +6 VAR and +6 TC voltage is the center of the longest rectangle that can be drawn inside the plotted curve. (The sides of the rectangle should be parallel to the X and Y axes of the plot.) The minimum rectangle must be equal to or greater than ±5% of the nominal setting. The four corners of the rectangle are checked during preventive maintenance.

Sequence B: To optimize the +6 VAR, plot the +6 VAR versus the +6 TC while running the worst case test program as follows:

1. Determine the upper and lower error-free running limits for the +6 VAR. The midpoint of these limits is the operating point.

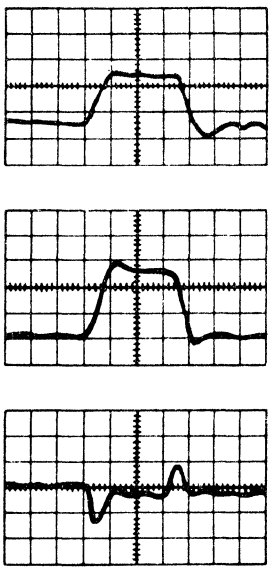


Input
40 ns/cm
5 v/cm

Test Point
40 ns/cm
2 v/cm

Output
40 ns/cm
5 v/cm

FIGURE 83. LS WRITE DRIVER

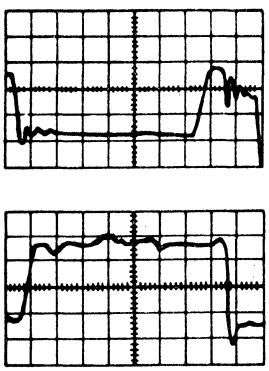


Input
40 ns/cm
5 v/cm

Test Point
40 ns/cm
2 v/cm

Output
40 ns/cm
5 v/cm

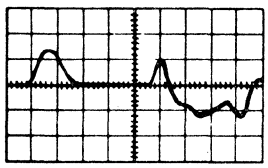
FIGURE 84. LS BIT DRIVER



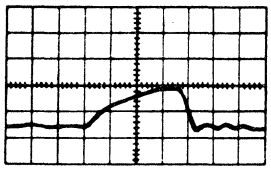
Input
50 ns/cm
2 v/cm

Output
50 ns/cm
10 v/cm

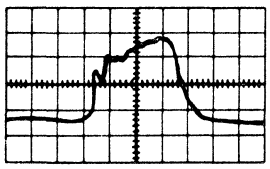
FIGURE 85. LS GATE DRIVER



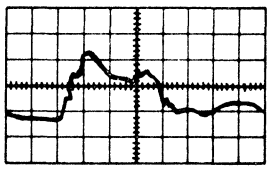
Input
40 ns/cm
100 mv/cm
TC = 5.35
K = 5.35



Strobe
20 ns/cm
1 v/cm

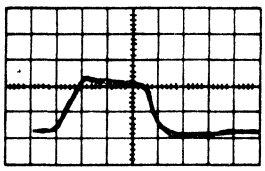


Test Point
40 ns/cm
1 v/cm

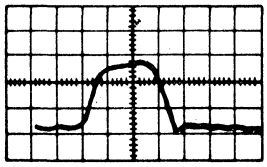


Output
100 ns/cm
1 v/cm

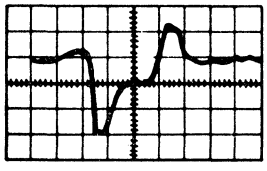
FIGURE 86. LS SENSE AMPLIFIER



Input
40 ns/cm
5 v/cm



Test Point
40 ns/cm
2 v/cm



Output
40 ns/cm
5 v/cm

FIGURE 87. LS READ DRIVER

2. Plot the three points on the S9 driver operating voltage determination graph.

3. Assure that one minute of error-free operation is possible at ±7% from the operating point.

4. After the run, set +6 VAR to the operating point.

LS Strobe Driver Identification

There are 18 separate strobe drivers. If bits are being dropped, consider the possibility of a missing strobe. The strobe distribution, on ALD page LS721, is arranged as follows:

Strobe bits 00 and 01	Strobe bits 17 and 21
Strobe bits 02 and 03	Strobe bits 18 and 22
Strobe bits 04 and 05	Strobe bits 20 and Parity 8-15
Strobe bits 06 and 07	Strobe bits 23 and Parity 16-23
Strobe bits 08 and 09	Strobe bits 24 and Parity 0-7
Strobe bits 10 and 11	Strobe bits 25 and 26
Strobe bits 12 and 15	Strobe bits 27 and 28
Strobe bits 13 and 14	Strobe bits 29 and 30
Strobe bits 16 and 19	Strobe bits 31 and Parity 24-31

Note: These circuits are all located on the card at 01A-D4M6.

ROS 201--Cycle One Sector of Local Storage

1. System reset; set check control switch to STOP.
2. Display sector to be cycled.
3. Set rate switch to SINGLE CYCLE.
4. Set data keys 22 and 31 on.
5. Set ROS REPEAT INSN down.
6. Press START.
7. Restore ROS REPEAT INSN.
8. Set data to be stored into local storage in data switches.
9. Set rate switch to PROCESS.
10. Press START.

The following should occur:

Data keys to L-register.
L-register to local storage.
Local storage to R-register.
R-register to adder for half-sum error check.

Note: If error occurs, LSAR will have advanced one address.

Array Temperature

If intermittent troubles are experienced on local store, check the array temperature. It should be $104^{o}F, \pm 1^{o}$.

Local Storage Heater

At time of installation, scope cycle time. Record cycle time and the temperature at entrance to gate near local store on shmoo page S9. The approximate cycle time should be 6 seconds on, 20 seconds off.

Checking Drivers and Terminating Diodes

See the section entitled "Checking MS Drivers and Terminating Diodes" under "Main Storage (MS) Service Checks."

READ ONLY STORAGE (ROS) SERVICE CHECKS

ROS Retry Adjustment

This procedure is based on voltage and timings being within specified tolerances. Refer to ALD AA000 for timings. Check -3 volts at 01C-E1B2D06 to be within ± 4%. Required equipment is an ohmmeter and a Tektronix 453 oscilloscope.

1. Remove the 5801515 card from 01C-E2L4; disable ROS retry by grounding pin 01C-E3C4D11.
2. With the ohmmeter, set up the following resistances on the two pots on the 1515 card:
   a. Measure between pins 1 and 2 (Figure 88) on the top pot and rotate the pot counterclockwise until a minimum reading of about 0 ohms is obtained.
   b. Measure between pins 1 and 2 (Figure 88) on the bottom pot and rotate the pot clockwise until a maximum reading of about 1000 ohms is obtained.
3. Re-insert 5801515 card in 01C-E2L4.

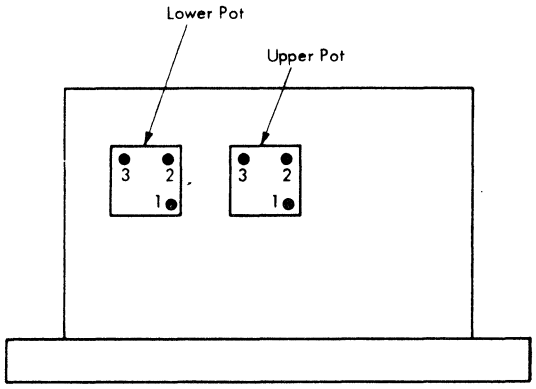


FIGURE 88. MODULE SIDE OF 5801515 CARD

4. Enable ROS retry by removing ground from 01C-E3C4D11.

5. Using a 10 x 1 probe (with ground probe) on the "CH 1 input," scope either:

   a. 01C-E2L4G05 if 5801515 card has five modules.

   b. 01C-E2L4G07 if 5801515 card has six modules (EC 259398 or later).

6. Set up the scope to single sweep on a 0.5-volt negative shift. See following section for procedure.

7. Load and run ROS ripple; see "ROS Ripple Test." Machines with EC 259860 or later must ground 01C-E3C2B10 for this procedure only.

8. Ready the single sweep on the scope.

9. For a one-minute period after step 8 was executed, determine whether or not the scope triggered.

   a. If the scope was not triggered, skip to step 13.

   b. If the scope was triggered, go to step 10.

10. Rotate the lower pot counterclockwise four turns.

11. Ready the single sweep.

12. While running ROS ripple, determine whether or not the scope still triggers during a one-minute period after step 11.

   a. If it does not, go to step 13.

   b. If it does, repeat steps 10-12 until it no longer does, then go to step 13.

13. Ready the single sweep.

14. Rotate the top pot clockwise until the scope triggers occasionally during a one-minute interval on a half-volt negative shift.

15. Set up the scope to single sweep on a 1.0-volt negative shift.

16. Ready the single sweep.

17. If the scope does not trigger for a one-minute period at this setting, the ROS retry adjustment is complete. If the scope triggers, rotate the top pot 1/4 turn counterclockwise. Repeat this step until the following conditions are met:

   a. The scope triggers occasionally on a 0.5-volt negative shift.

   b. The scope does not trigger when set for a one-volt negative shift.

Setting Up Single Sweep

1. Set the A and B time/div and delay time knob to 0.1 second scale.

2. Set the mode knob on CH 1 and the trigger knob on CH 1 only.

3. Set A TRIGGERING as follows:

   a. Source -- Internal

   b. Coupling -- DC

   c. Slope - Minus

   d. Set LEVEL CONTROL to 0 position and HF STAB all the way clockwise.

4. Set A SWEEP MODE to SINGLE SWEEP.

5. Set HORIZ DISPLAY to A and MAG to OFF.

6. Set the volts/div CH 1 knob to 50 MV and the three-way switch below it to the ground position.

7. Rotate the position knob fully clockwise.

8. Press the reset pushbutton and make sure the light comes on.

9. Rotate the position knob slowly counterclockwise until the reset light goes off.

10. The light is to be set to go off either 1 cm below the top horizontal graticule (0.5-volt setting) or 2 cm below the top horizontal graticule (1.0-volt setting).

   a. If the light went off above this point, rotate the level control slightly counterclockwise and repeat steps 7-10 until the scope fires at the right point. Go to step 11.

   b. If the light went off below the reference point, rotate the level control slightly clockwise and repeat steps 7-10 until the scope fires at the right point.

11. Move the three-way switch below the volts/div CH 1 knob from the ground position to the DC position.

12. Set the A sweep mode switch to the auto trigger position.

13. Position the trace on the top horizontal graticule.

14. Move the A sweep mode switch back to the single sweep position.

15. Press the reset pushbutton and make sure the light comes on.

ROS Waveforms

Figure 89 shows typical waveforms for normal ROS operation. These waveforms are not to be used as reference for levels, transition times, or pulse widths, but rather as a general indication of a normally functioning ROS unit.

ROS Parity Errors

To check ROS parity error circuits, ROS repeat on one of three ROS words.

ROS Repeat	Error
FD5	0-30
FD6	31-55
FD7	56-89

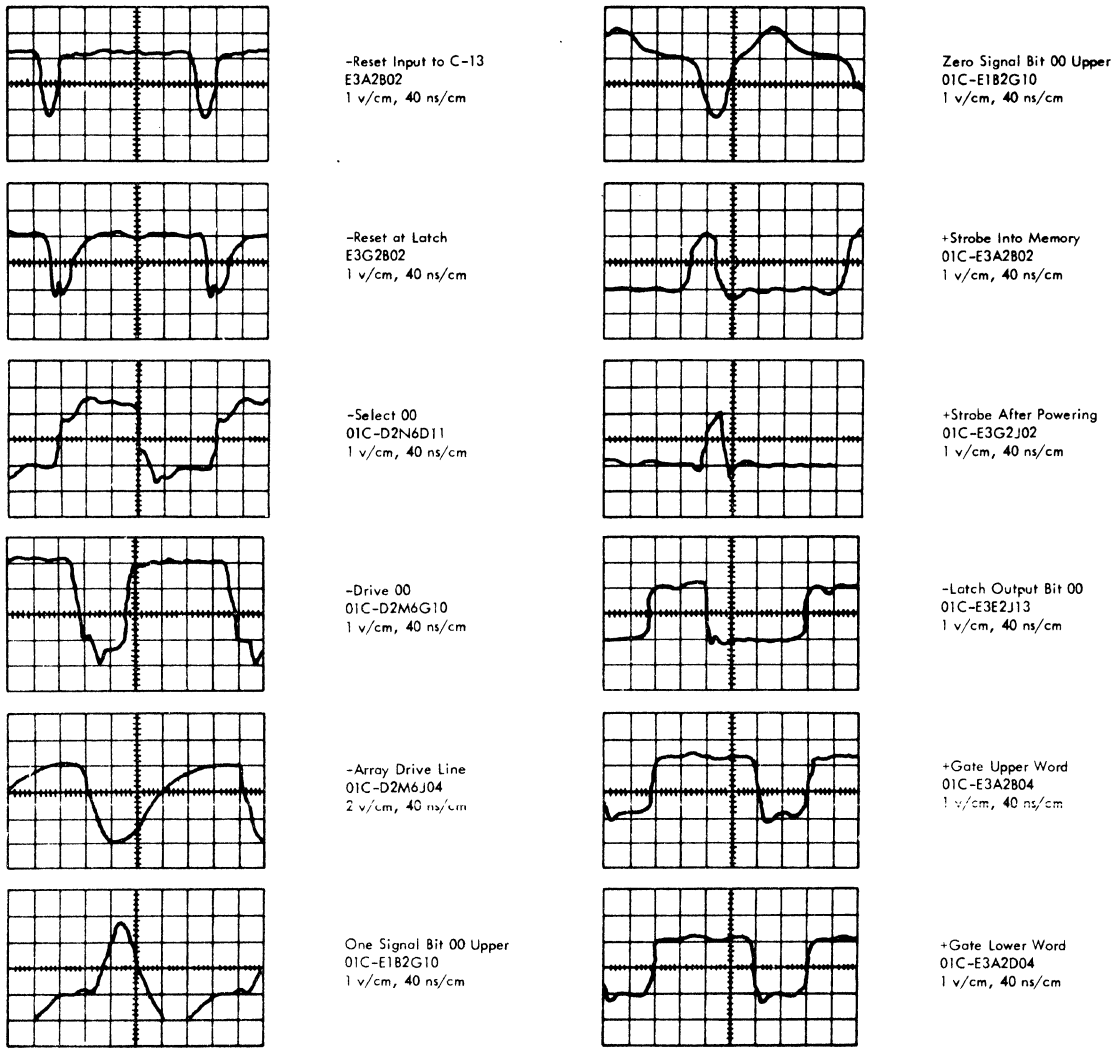


FIGURE 89. ROS WAVEFORMS

ROS F00-F03--ROSDR Test All Ones

1. System reset.
2. Set data keys 20-23 (F00).
3. Set ROS REPEAT INSN down.
4. Check CPU roller 1, position 6 and CPU roller 2, positions 1 and 2 for all bits on except 16, 24, and 83.
5. Set data keys 30 and 31 on, in addition to 20-23 (F03).
6. Check for the conditions described in step 4.
7. Restore ROS REPEAT INSN.
8. System reset.

ROS F01-F02--ROSDR Test All Zeros

1. System reset.
2. Set data keys 20-23 and 31 (F01).
3. Set ROS REPEAT INSN down.
4. Check CPU roller 1, position 6 and CPU roller 2, positions 1 and 2 for all bits off except the parity positions.
5. Set data key 30 on and 31 off (F02) in addition to 20-23.
6. Check for the conditions described in step 4.
7. Restore ROS REPEAT INSN.
8. System reset.

ROS Address 000

ROS Addr 000 has only bits 16, 35, 37, 38, 39, 50, 56 (ZN4) (AL23) (DG2).

Extra or Missing Bits

Usually, the picking or dropping of a great number of bits is due to an extra or missing drive line or select line.

To check for a missing or extra drive line, use the ROS addresses in Figure 90. These ROS addresses all use select line one so each drive line may be checked at the console until the faulty line is located. Remember, if two lines are driving at once, the line that gives no error is the failing line.

To check for a missing or extra select line use the ROS addresses in Figure 91. These addresses all use drive line zero so each select line may be checked at the console until the faulty line is located.

Sense Latch and Strobe

If a strobe is lost, the sense latch will not set and the corresponding bits will be set into ROSDR.

If a sense latch reset is lost, the sense latch will not reset and the corresponding bits will not set into ROSDR.

Figure 92 is a list of test points for the ROS strobe pulse and the sense latch reset. These test points can be used to determine which strobe or reset is failing.

Figure 93 shows ROS sense amplifier and sense latch card locations.

ROS Ripple Test

The ROS ripple test tape can be generated with diagnostic program 5350. For systems using disks only, use program 5FE5 to generate a ROS ripple pack. Since the ROS ripple test checks only the parity of the ROS words, no test tape update is necessary when EC activity affects the ROS bit planes.

The first record on the ROS ripple test tape pack checks all planes. If it is desired to ripple only one given plane, depress system reset pushbutton, and FLT load the next record. The second record ripples plane zero; the third record ripples plane one; etc.

Basic ROS Ripple

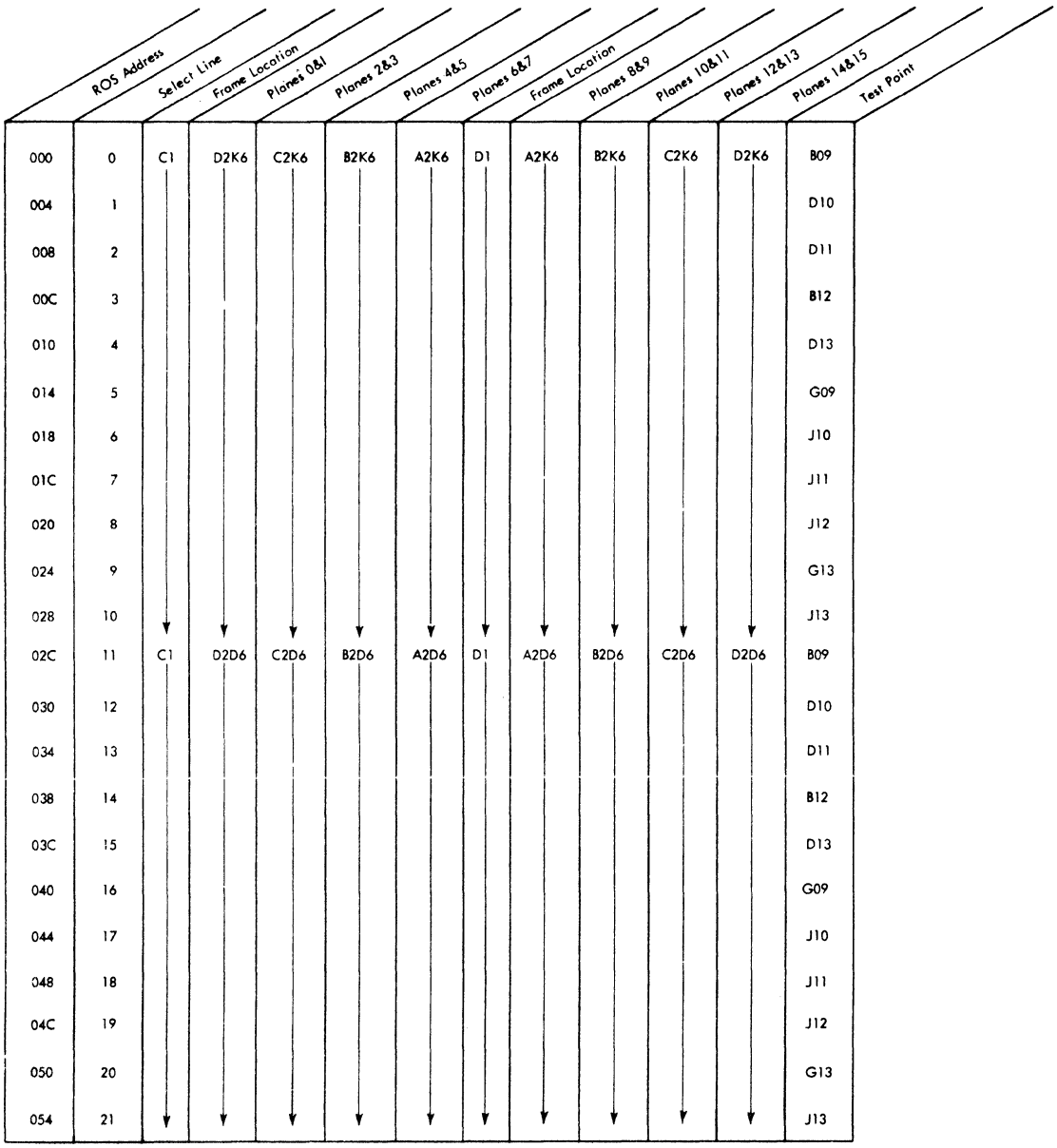
1. Set the check control switch to stop position.
2. Place the ROS ripple test tape or pack on an available unit; set the address of the unit in the load unit switches; press the load pushbutton.
3. The first section loads and ripples all planes. If an error occurs, the program stops and the hard

ROS Addr	Card Location	Drive Line
004	C1D2M6	0
006	C1D2J6	1
084	C1D2F6	2
086	C1D2C6	3
104	C1D2L6	4
106	C1D2H6	5
184	C1D2E6	6
186	C1D2B6	7
204	C1C2M6	8
206	C1C2J6	9
284	C1C2F6	10
286	C1C2C6	11
304	C1C2L6	12
306	C1C2H6	13
384	C1C2E6	14
386	C1C2B6	15
404	C1B2M6	16
406	C1B2J6	17
484	C1B2F6	18
486	C1B2C6	19
504	C1B2L6	20
506	C1B2H6	21
584	C1B2E6	22
586	C1B2B6	23
604	C1A2M6	24
606	C1A2J6	25
684	C1A2F6	26
686	C1A2C6	27
704	C1A2L6	28
706	C1A2H6	29
784	C1A2E6	30
786	C1A2B6	31

ROS Addr	Card Location	Drive Line
804	D1A2L6	32
806	D1A2H6	33
884	D1A2E6	34
886	D1A2B6	35
904	D1A2M6	36
906	D1A2J6	37
984	D1A2F6	38
986	D1A2C6	39
A04	D1B2L6	40
A06	D1B2H6	41
A84	D1B2E6	42
A86	D1B2B6	43
B04	D1B2M6	44
B06	D1B2J6	45
B84	D1B2F6	46
B86	D1B2C6	47
C04	D1C2L6	48
C06	D1C2H6	49
C84	D1C2E6	50
C86	D1C2B6	51
D04	D1C2M6	52
D06	D1C2J6	53
D84	D1C2F6	54
D86	D1C2C6	55
E04	D1D2L6	56
E06	D1D2H6	57
E84	D1D2E6	58
E86	D1D2B6	59
F04	D1D2M6	60
F06	D1D2J6	61
F84	D1D2F6	62
F86	D1D2C6	63

Note: All of the cards indicated above use output pin B13 for scoping. When a line is addressed, it should pulse. If not conducting, the line should be at +2v. If this level is down only 3/4(0.75)v, trouble is indicated.

FIGURE 90. ROS DRIVE LINE TESTS



Note: Test point pins are the same for each of the eight card locations of a given select line.

FIGURE 91. ROS SELECT LINE TESTS

Strobe Upper Word	Strobe Lower Word	Sense Latch Reset	Bits
E3G3B03	E3G3D07	E3G3B02	0-9
E3G3D06	E3G3D05	E3G3B02	10-19
E3G5B13	E3G5B10	E3G5B07	20-29
E3G3B10	E3G3D10	E3G3D11	30-39
E3G6B09	E3G6D11	E3G6B10	40-49
E3G6D06	E3G6D10	E3G6D07	50-59
E2G7D02	E2G7D06	E2G7D11	60-64 and 75-79
E3G6B02	E3G6D02	E3G6B03	65-74
E2G7B02	E2G7D07	E2G7B09	80-90

Note: All test points are on gate 01C.

FIGURE 92. ROS STROBE AND SENSE LATCH TEST POINTS

Sense Amplifiers

Bit	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X
0,1	E1B2	E1G2	E1B4	E1G4	E1B6	E1G6	E2B2	E2G2	E2B4	E2G4
2,3	E1C2	E1H2	E1C4	E1H4	E1C6	E1H6	E2C2	E2H2	E2C4	E2H4
4,5	E1D2	E1J2	E1D4	E1J4	E1D6	E1J6	E2D2	E2J2	E2D4	E2J4
6,7	E1E2	E1K2	E1E4	E1K4	E1E6	E1K6	E2E2	E2K2	E2E4	E2K4
8,9	E1F2	E1L2	E1F4	E1L4	E1F6	E1L6	E2F2	E2L2	E2F4	

Sense Latch

Bit	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X
0-4	E3E2	E3H2	E3D4	E3H4	E3E6	E3J6	E2B6	E3H6	E2C6	E2H6
5-9	E3F2	E3J2	E3E4	E3J4	E3F6	E3K6	E3F4	E2L6	E2E6	E2K6

Note: All cards are in frame 01, gate C.

FIGURE 93. ROS SENSE AMPLIFIER AND LATCH CARD LOCATIONS

stop indicator comes on. The master check indicator is not set. To determine the failing address, subtract one from the ROS address indicated in SDR (19-30) The force indicator switch must be used to get the proper indication from the switchable indicators.

ROS BIT PLANE REMOVALS AND ADJUSTMENTS

ROS Bit Plane Adjustments

The pressure screws in the spider assemblies must be checked for minimum torque of 4.5 inch-pounds every 90 days. Use the torque screwdriver (P/N 461450) to carry out the adjustment procedure that follows:

1. Following the sequence shown in Figure 94 check the torque on setscrews 1 through 8, 11, and 12 for 4.5 inch-pounds. Use torque wrench listed above.

Note: Make sure the torque wrench has been recently calibrated. This wrench must be calibrated periodically.

2. Check the torque on setscrews 9 and 10 for 3.5 inch-pounds (Figure 94).

3. After completing steps 1 and 2, check the torque in the same sequence indicated in Figure 94 to see that torques for positions 1-8, 11 and 12 are within 4.0 to 5.0 inch-pounds and that torques for positions 9 and 10 are within 3.0 to 4.0 inch-pounds. If the torques are not within specifications, re-torque as described above.

4. Repeat steps 1-3 until the specifications are met.

11	12
1	2
3	4
5	6
7	8
9	10

FIGURE 94. SETSCREWS TORQUE SEQUENCE (ROS BIT PLANES)

ROS Bit Plane Removal

Caution
Use extreme caution when handling bit plates; they are easily damaged.

1. Release pressure on the 12 pressure pads by loosening the setscrews bearing on the center of each pad. Use a standard bristol wrench or a torque wrench (P/N 461450). Do not loosen slotted-head screws that are located toward the center of the casting assembly.

2. Release pressure from upper and lower drive connectors by loosening the four spring-loading screws in each connector. Do not disengage screws completely.

3. Remove the four corner hex-head screws and two center knurled nuts and remove spider assembly from two center studs. (The knurled nuts may be removed by hand.)

4. Remove rubber pressure pad from center studs.

5. Remove upper and lower drive connectors by removing two screws at the end of each connector.

Note: Plastic or lint-free gloves must be worn when handling bit planes.

6. Carefully remove the bit plane from alignment pins and studs by holding at center of each of the horizontal edges. The plane must be held and gently lifted out without being allowed to bow.

Caution
Exercise extreme care in handling the bit plane to avoid creasing, folding, or scratching.

7. Cleanliness of the sense and bit planes is very important. Perform the following cleaning procedure before installing the bit plane.

Note: Elapsed time between cleaning the sense lines and bit planes and installing the bit planes, rubber pressure pad, and spider assembly must be kept to a minimum.

ROS Bit Plane Cleaning

New bit planes are stored in an IBM-approved polyethylene bag. The bag must not be opened until just before the bit plane is to be installed. If the bag is opened or damaged prior to installation the bit plane

must be recleaned. If a new bit plane is to be installed, begin installation procedure; however, do not remove the bit plane from the polyethylene bag until all preparations have been made for immediate installation on the equipment.

Cleaning of the bit plane is necessary when a bit plane is removed and replaced or when the polyethylene bag is accidentally broken.

Caution

IBM-approved nylon or lint-free gloves must be worn during all phases of bit-plane handling.

To clean the bit plane, proceed as follows:

1. Clean a flat surface, as large as or larger than the bit plane with a lint-free cloth well saturated with cleaning fluid (P/N 450608). The surface must be lint-free.
2. Clean all array hardware associated with the bit plane to be installed.
3. Place the bit plane, with the Mylar* side up, on the lint-free surface.
4. Clean upper and lower connector tabs with lint-free cloth that is thoroughly moistened with circuit cleaner.
5. Fold clean, lint-free cloth into a pad about 3 or 4 inches square and saturate thoroughly with circuit cleaner.

Caution

Do not apply circuit cleaner directly to the bit plane.

6. Briskly rub the Mylar side of the bit plane.

Note: Best results are obtained by starting at one edge and rubbing back and forth over the entire length of the bit plane. If the cloth becomes dry, reapply the circuit cleaner to the pad only.

7. Allow bit plane to dry.
8. Immediately after cleaning, install bit plane in its proper location, using the following ROS bit plane installation procedure.

Note: Carrying the bit plane in a vertical position reduces the possibility of further contamination.

ROS Bit Plane Installation

Note: Extreme care must be taken throughout the following procedure to avoid damage to the bit planes, sense planes, or connector tabs. Plastic or lint-free gloves must be worn when handling bit planes.

1. Turn all setscrews counterclockwise until pressure plates are just flat to the casting. Do not back screws out past this point.
2. Clean the bit plane, if this has not been done, in accordance with cleaning procedure. If a new bit plane is being installed, perform steps 2 and 5 of the cleaning procedure.
3. Carefully place the bit plane over the two center mounting studs with Mylar dielectric side toward sense plane. Gently slip the bit plane over the upper and then the lower alignment pins and press flat on the small copper lands around upper hole and lower slot. The upper alignment hole has a slight press fit and the lower alignment slot prevents any side motion but allows lengthwise motion so that the bit plane can lie flat on the sense plane.
4. Install the upper and lower drive connectors with the mounting screws. Do not tighten spring-loading screws at this time. This procedure ensures correct location of the bit plane while the spider assembly is being installed and loaded.
5. Install the large-rubber pressure pad by placing it gently over the two center studs.
6. Holding the rubber pressure pad in position, place spider assembly over center studs. The holes in the spider casting are large clearance holes for the studs.
7. Exerting light upward pressure on the casting, align upper corner holes with the mating tapped holes in the vertical bars. Insert and fasten the four corner hex-head mounting screws. Do not over-tighten these screws but make sure they are bottomed. Fasten the two knurled nuts to the center studs. The knurled nuts are to be bottomed but must be only finger-tight when this is done.

Caution:

If the knurled nuts are too tight, bending and fracture of the casting may result when the spider is loaded.

8. Using the torque wrench, tighten all setscrews (1 through 12) to 2 inch-pounds in the sequence shown in Figure 94. Repeating the sequence, tighten setscrews in positions 1 through 8 and 11-12 to 4.5 inch-pounds; tighten setscrews in positions 9 and 10 to 3.5 inch-pounds.
9. After completing step 8, check torque in sequence indicated in Figure 94 to see that all torques for positions 1 through 8 and 11-12 are within 4.0 to 5.0 inch-pounds and that torques for positions 9 and 10 are within 3.0 to 4.0 inch-pounds. If torques are not within specifications, re-torque as described above.
10. Repeat steps 8 and 9 until set torque specifications are met.

* Trademark of E.I. duPont deNemours & Co. (Inc.)

Connector Installation

1. Remove upper and lower drive connectors by removing the mounting screws. Check alignment of bit plane connector tabs with tabs on terminating resistor card at top and the drive card on bottom. Resistor card and lower drive card may be shifted for horizontal alignment by loosening the two hold-down screws in each resistor card.
2. Reinstall connectors and tighten the mounting screws.
3. Load upper and lower drive connectors by turning spring-loading screws clockwise until they bottom. Do not over-tighten.

STORAGE PROTECT (SP) SERVICE CHECKS

Storage protect timing information is located in Volume 1 of the ALD's, Page AA000.

Reference Voltage and Sense Level Adjustments

Two potentiometers set the storage protect reference and sense level voltages. The card at 02B-A3J4 has a 1000-ohm potentiometer (bottom) for the reference voltage and a 2000-ohm potentiometer (top) for the sense level voltage adjustments.

Reference Voltage

Reference voltage should be set as follows:

1. Connect an accurate dc meter between 02B-A3J4D11 (+ lead) and any B06 pin (- lead at -3 volt reference).
2. Using the bottom potentiometer at 02B-A3J4, adjust for a potential difference of +4.8 volts. This setting should be made at room temperature of approximately 68°F. If the system must operate under other temperature conditions, use the graph of Figure 95 to determine the range of allowable reference voltage settings.

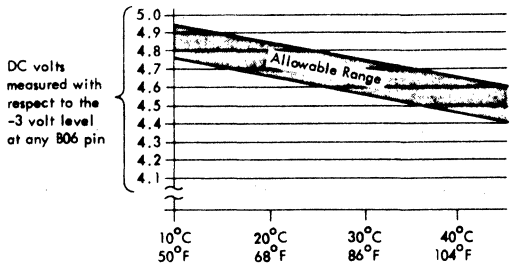


FIGURE 95. SP REFERENCE VOLTAGE TRACKING

With the room temperature between 68°-86°F, the storage protect storage should operate with the reference voltage varied ±0.4 volts from its nominal point. Before checking this variance, however, be sure that all logic voltages and the sense level voltage are at the nominal points.

Sense Level Voltage

The sense-level voltage is used by the final amplifier to yield the best discrimination between a maximum zero and a minimum one. As an initial setting, adjust the sense-level voltage to 3.1 volts (measured between 02B-A3J4B02 and ground).

To find the optimum setting, run the storage protect diagnostic (E3C9) with all the logic voltages and the reference voltage at their nominal values.

Lower the sense-level voltage (top potentiometer at 02B-A3J4) until the first error occurs. Return to the nominal value, restart the program, and raise the sense level until another error occurs. Set the sense-level voltage at the mid-point of the high and low values.

With nominal logic voltages and nominal room temperature, the storage protect storage should operate with the sense-level voltage varied ±0.2 volts from its nominal value.

Checking SP Drivers and Terminating Diodes

See the section entitled "Checking MS Drivers and Terminating Diodes" under "Main Storage (MS) Service Checks."

Inhibit Drivers and Sense Amplifiers

Figure 96 shows the location of the inhibit drivers and sense amplifiers for the storage protect storage

Bit	Location	Out (Inhibit)	Return	Sense Pin	Line Name
1	B-A3L4	B08	B07	B02	Parity
2	B-A3L3	B03	B10	B04	0
3	B-A3J3	B08	B07	B02	1
4	B-A3L4	B03	B10	B04	2
5	B-A3L3	B08	B07	B02	3

FIGURE 96. SP INHIBIT DRIVER AND SENSE AMP LOCATIONS

SP Sense Windings

Figure 97 shows the location of the storage protect storage sense windings. The sense windings may be scoped using a one-to-one probe and the differential amplifier feature of the scope to cancel noise.

Bit	Location	Pin	Pin
1	B-A3K4	D05	D06
2	B-A3K3	D11	B10
3	B-A3K3	B03	B04
4	B-A3K4	D04	B05
5	B-A3K3	B13	D13

FIGURE 97. SP SENSE WINDING TEST POINTS

Termination Diodes

The termination diodes (steering diodes) for the storage protect storage are located on the array boards. They are not shown on the logic pages. Remember that there are diodes in the driver lines.

Two types of diodes exist: 03E1 (part number 2414884), and 03E2 (part number 2414885). There are 16 of each type.

X and Y Drivers

Figure 98 shows the location and test points of the storage protect X and Y drivers.

Write Pin	Location	Read Pin	Line Name
D10	A3J2	B05	Y0,2,4,6
B08	A3J2	B04	Y8,10,12,14
D05	A3J2	D12	Y line in 1N,3N,5N,7N
D06	A3J2	B13	Y line in 9N,11N,13N,15N Y Rd on Read Y WG on Write
B05	A3L2	D10	0N,1,8N,9
B04	A3L2	B08	2N,3,10N,11
D12	A3L2	B08	4N,5,12,13
B13	A3L2	D06	6N,7,14N,15

Y Drivers

Write Pin	Location	Read Pin	Line Name
D10	A3J5	B05	X0,2,4,6
B08	A3J5	B04	X8,10,12,14
D05	A3J5	D12	1N,3N,5N,7N
D06	A3J5	B13	9N,11N,13N,15N Y Rd on Read X WG on Write
B05	A3L5	D10	0N,1,8B,9
B04	A3L5	B08	2N,3,10N,11
D12	A3L5	D05	4N,5,12N,13
B13	A3L5	D06	6N,7,14N,15

X Drivers

FIGURE 98. STORAGE PROTECT DRIVER LOCATIONS

Storage Protect Test Points

Following are some common test points for the storage protect storage.

Sense Gate	B-A3J4B04
Inhibit Timing	B-A3J7D05
Strobe	B-A3K6B12
Read Gate	B-A3K6B13
Write Gate	B-A3K6D02

CHANNEL SERVICE CHECKS

The material in this section can be used to adjust delays and singleshot timings and to check for proper circuit operation of the selector channel and the 1052.

SELECTOR CHANNEL

Figure 99 outlines the maintenance approach for servicing the selector channel when a malfunction is suspected. Procedures are outlined for progressive scan and non-progressive scan diagnostic techniques.

When trouble is suspected in a specific area of the selector channel, the following checks can be used to pinpoint or correct the malfunction.

C Reg Set and IF Service Out Delays

1. Set check switch to disable position. Manually store the following program; press PSW restart push-button. The program should be looping.

Location	Data	Symbolic
0000	*0 00 00 00	PSW
0004	00 00 01 00	PSW
0048	00 00 02 00	CAW
0078	*0 00 00 00	PSW
007C	00 00 01 00	PSW
0100	9C 00 0‡ XX	SIO
0104	47 F0 01 04	Branch to itself
0200	04 00 03 00	CCW
0204	00 00 00 06	CCW

* Enable
‡ Channel Tested
XX Available Tape or Disk

2. Sync scope plus on rise of IF service in line at 01X-N4K7D04 (0 time).

3. Observe C reg set line (01X-N4G6D12) falls at 340ns. Adjust delay at 01X-L4H2 bottom.

4. Observe that IF service out line (01X-N4L7D05) falls at 215ns. Adjust delay at 01X-N3E2 bottom.

Channel Reset

1. Set check switch to disable position and rate switch to process position.

2. Sync scope on L3E7B08 plus external.

3. Press system reset to time pulses; check all points on Figure 100.

4. If clocks are running, use Figure 101 for reference.

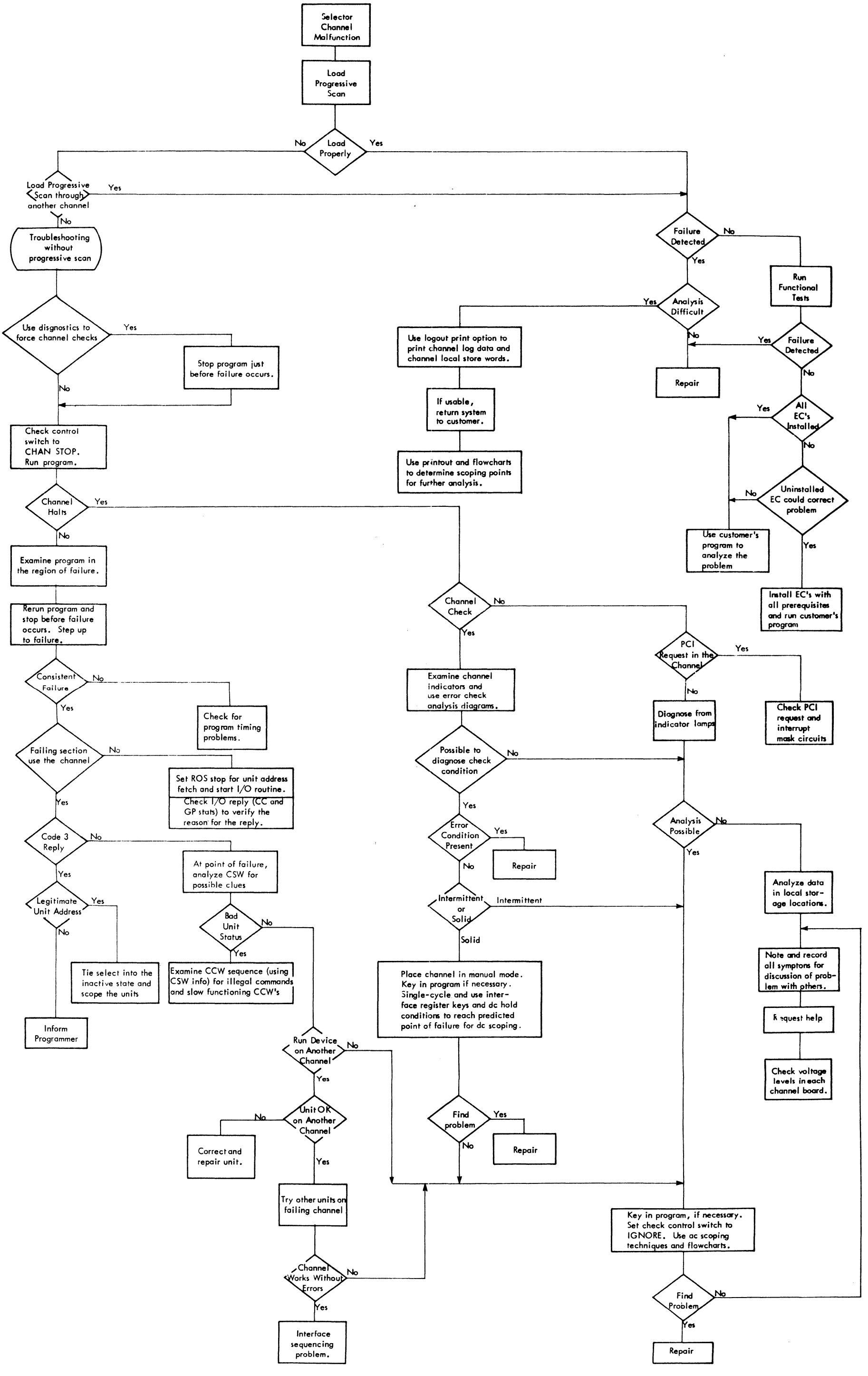


FIGURE 99. SELECTOR CHANNEL MAINTENANCE APPROACH

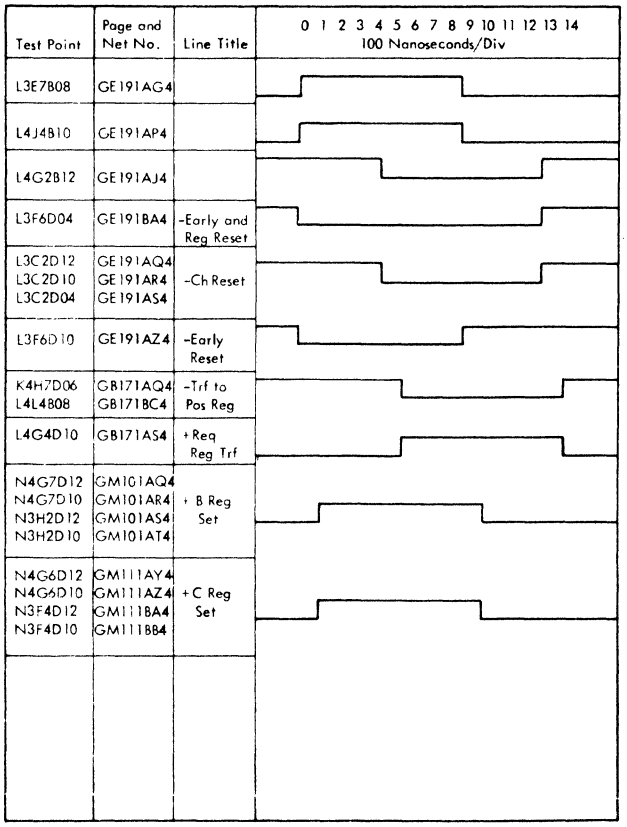


FIGURE 100. RESET PULSES (CLOCK NOT RUNNING)

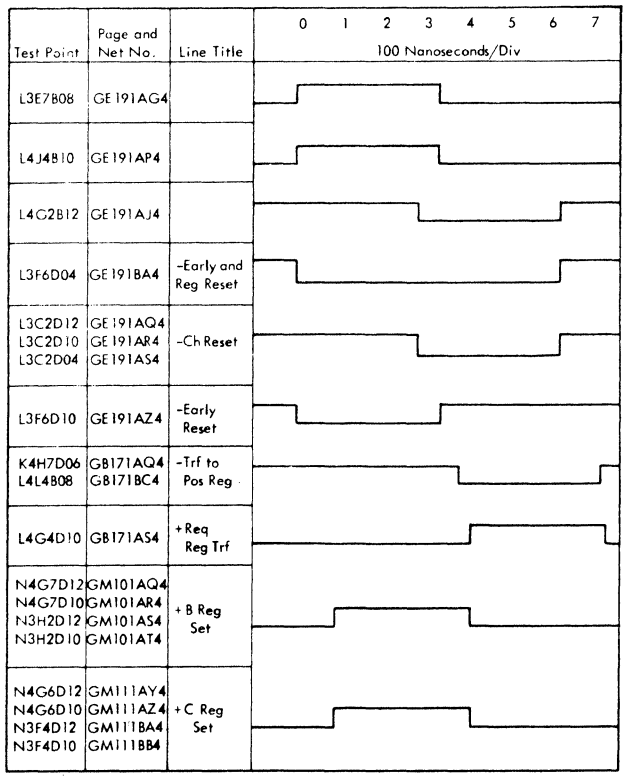


FIGURE 101. RESET PULSES (CLOCK RUNNING)

A-Clock Check

Add jumper from XM4H7D04 to ground.

1. Set check switch to disable position and rate switch to process position.
2. Sync scope on L3E7B08 minus external; set first pulse on Figure 102 to zero time.
3. Press system reset to time pulses; check all points in Figure 102; ensure that clock is running.

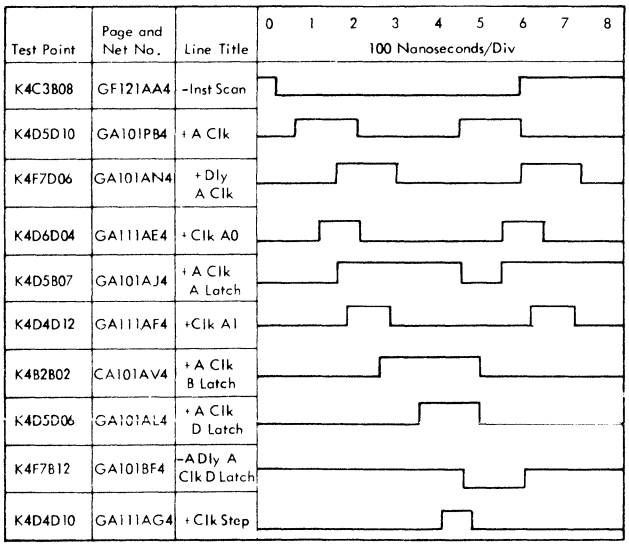


FIGURE 102. A CLOCK

Cycle Counter Check

1. Set check switch to disable position and rate switch to process position.
2. Sync scope on L3E7B08 plus external; set first pulse on Figure 103 at zero time.
3. Check all points in Figure 103.

B-Clock Check

1. Set check switch to disable position and rate switch to process position.
2. Sync scope on L3E7B08 plus external; set first pulse on Figure 104 at zero time.
3. Add a temporary jumper between K4M4D07 and K4H7D10.
4. Check all points in Figure 104.
5. Remove jumper installed in step 3.

Tag Generator and Manual Stop Controls

1. Repeat steps 1 and 2 of preceding "B Clock Check."

2. Add the following temporary jumpers:
   M4K6B10 (GS111BN4) to M4K6B02 (GS111AK4)
   M4K7D04 (GS111BP4) to L3F6D04 (GE191BA4)
3. Check all points in Figure 105.
4. Set channel control switch to selector channel position; set channel selector to correct channel.
5. Set address key 9 down (if STOP SEL).
6. Scope test point *1 in Figure 105.
7. Set address key 10 down, address key 11 up (10 code ITD1 and IT); press enter pushbutton. Pulse should change from solid to solid plus dotted line.
8. Press system reset pushbutton.
9. Repeat step 7 and 8 scoping test points *2 (code 01 = 10 up, 11 down) and *3 (code 11 = 10 down, 11 down) (Figure 105).
10. Remove jumpers installed in step 2 and reset channel control switch to normal position.

Test Point	Page and Net No.	Line Title	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 100 Nanoseconds/Div
K4H7D06	GB171AQ4	-Trf to Pos Reg	
K4B5D12	GA131AP4	+CC Step 0 Ph A	
K4C7B10	GA131AQ4	+CC Step 0 Ph B	
K4B5D10	GA131AR4	+CC Step 1 Ph A	
K4C7B09	GA131AS4	+CC Step 1 Ph B	
K4B6D04	GA131BL4	+CC Step 2 Ph A	
K4G2B10	GF121AG4	-No Poll Reset Reg	
L3C2D12	GE191AQ4	-Ch Reset L2	
K4C3D06	GF121AA4	-Inst Scan Start	

FIGURE 103. CYCLE COUNTER

Test Point	Page and Net No.	Line Title	0 1 2 3 4 5 6 7 8 9 10 Nanoseconds/Div
L3F6D10	GE191A24	-Early Reset	
K4E2B08	GA121AA4	+B Clk	
K4H7B12	GA121AN4	-B Clk	
K4F6B10	GA121AG	-GP to BC Set B	
K4E4B10	GA121AY4	-GP to BC Set A	
K4C4D05	GA121AH4	-CLk B2	
K4J6D05	GA121AP4	-B Clk	

FIGURE 104. B CLOCK

Test Point	Page and Net No.	Line Title	0 1 2 3 4 5 6 7 8 9 10 11 100 Nanoseconds/Div
M4K7D09	GS111AL4		
N3F2D10	GR111AM4	+ITD 1	*1
N3E4D10	GR111AL4	+ITD 2	
N3F6D10	GR111BE4	+ITD 3	
N3E4D12	GR111AW4	+ITD 1 Not 2	*2
N3E4D04	GR111BW4	+ITD 2 Not 3	*3
N3E5D11	GR111BM4	+Svc In Dly	
M4J2D06	GS111BQ4	+IF Svc Lth	
N3D2D10	GR111AC4	+Not ITD 1	

FIGURE 105. TAG GENERATOR

Indicator Check

1. Check that the following indicators are on or rippling:

Roller Position	Indicators	State
3	Byte Counter: A and B parity bits only	On
4	CC Phase: 0, 1, 2; Clock: A0, A1, step	Rippling
5	Pos Reg Trf; A Clock: A, B, C, D, SP: D2	Rippling
5	Instruction Scan	On
5	Byte Counter Mod Enable	May be on dimly or not visibly lighted
6	FIN (Flag Reg Unpredictable)	On

A-Clock Manual Controls

1. Set channel control switch to selector channel position; set channel selector for correct channel.
2. Using address keys 10 and 11 as follows, press enter pushbutton and check for correct results:

Code	Address Keys	Position
01	10 up and 11 down	Stop A0
11	10 and 11 down	Stop A1
10	10 down and 11 up	Stop CS

3. Set channel control switch to normal position.
4. Return address keys to normal position.

Operation Control Check

1. Set channel control switch to selector channel position, channel selector for correct channel, and rate switch to single-cycle position.
2. Set the following IAR keys down and check for correct results; press the enter key for each and then reset each key off.

IAR Key	Result
30	Select In
29	Service In
27	Address In
26	Poll and Select Out (Do not reset)
31	Operational In (Do not reset) and Operational In Test
28	Status In and Command Out

3. Reset Channel Control to normal position.

DTC Hold Check

1. Add the following jumpers:
   B-B2G4D04 (KE311AB4 tie I/O routine on) to ground
   B-B2K5B09 to ground if channel 1 under test
   B-B2C7D07 to ground if channel 2 under test
   B-B2C7B03 to ground if channel 3 under test
2. ROS repeat on address 0B0.
3. Set rate switch to single-cycle position.
4. Scope the following points on the channel under tests:
   Channel 1 B-B2K7D04 (KE451)
   Channel 2 E-C3L2D06 (KE451)
   Channel 3 E-C3L2B12 (KE451)
5. Press system start pushbutton; observe a -350ns pulse.
6. Set address key 8 down (Hold DTC); press enter and start pushbuttons; point should go down until address key 8 is reset.

Singleshot Adjustment

Adjust singleshots as shown in Figure 106; sync scope on internal.

Selector Channel Clock-Stepping Procedure

The following will allow clock stepping through the start I/O CCW1, CCW2, unit select, end update, and interrupt routines. This procedure is to be used in conjunction with IOP201, 202, 211, 209, and 210, respectively. A mixture of channel clock stops and ROS single cycle is used to step the routines and allow scoping at each stop. The channel stops at the end of the indicated clock cycle; therefore, all conditions on the IOP pages, following a clock cycle and up to the next clock cycle, have been completed. Figure 107 shows a block diagram of the routines that can be stepped by this procedure.

To prepare for selector channel clock stepping, proceed as follows:

1. Mount a scratch tape on a tape drive. Make sure it is not file protected.
2. Key in the following program:

Address	Data	Comments
0000	FF040000	Restart PSW
0004	00000300	
0048	00000400	CAW

Name	Page	Location	Timing	Procedure
IF Line Check	GR101	N3D5B02	150* (-)	a. Set sel chan switch to desired channel and set manual op switch to sel. b. Set keys 27, 29, and 31 down (addr in, svc in, op in). c. Jumper K4J6D06 to M4E7B02. d. Press ENTER; the single shot should be firing continuously; observe scope and adjust top potentiometer.
Select In Gate	GR101	N3D5D02	150* (-)	a. Set sel chan switch to desired channel and manual op switch to sel position. b. Jumper N3D5B02 to N3D05B07. Jumper K4J6D06 to M4E7B02. c. Set keys 27, 29, 30, 31 down (addr in, svc in, sel in, OP IN) and depress ENTER. d. Observe pulse on scope and adjust bottom potentiometer.
Start IF POLL	GR121	M4H7D02	150* (-)	a. Set manual op switch to off position; set rate switch to process position; press reset and start pushbuttons. (Ensure that channel clocks are running) b. Jumper K4J6D06 to M4H7B08 and M4F6B08 to ground. c. Observe pulse on scope and adjust bottom potentiometer.
IF RESET	GS151	M4H7B02	8 usec (-)	a. Press RESET repeatedly and observe pulse on scope; adjust top potentiometer. (Place check control switch in any position other than disable.)

FIGURE 106. SINGLESHOT TIMING PROCEDURE

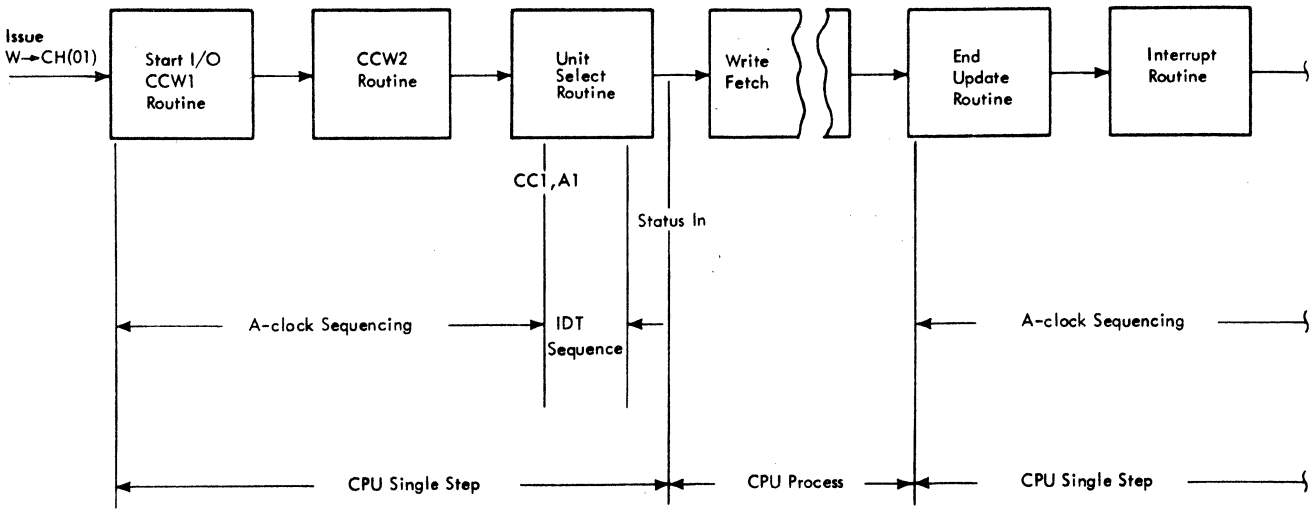


FIGURE 107. SELECTOR CHANNEL CLOCK-STEPPING BLOCK DIAGRAM

Address	Data	Comments
0078	FF040000	I/O new PSW
007C	00000300	
0300	9C000CUU	SIO--CUU = channel and unit address of scratch tape
0304	47F00304	Unconditional branch to 304
0400	01000501	CCW
0404	20000100	

3. Set selector channel display switch to channel number of scratch tape.

4. Press PSW RESTART and observe that the scratch tape moves.

Any or all of the five following routines may now be stepped through. (Make sure the tape is moving as each routine is started.)

Start I/O (CCW1) Routine IOP201

Action	ROS Address	Channel Time
1. Set ROS address 010 in the storage data keys.		
2. Set ROS address compare switch to STOP.		
3. Press SYSTEM RESET and PSW RESTART.	010	CCW1, CC0
4. Set rate switch to SINGLE CYCLE.		
5. Set address key 11 on, 9 and 10 off; press ENTER.		
6. Press START.	AAB	
7. Press START.	AAA	CCW1, CC0, A0
8. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW1, CC0, A1
9. Set address key 10 on, 9 and 11 off; press ENTER.		CCW1, CC1, CS
10. Set address key 11 on, 9 and 10 off; press ENTER.		CCW1, CC1
11. Press START.	ABB	
12. Press START.	A80	CCW1, CC1, A0
13. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW1, CC1, A1
14. Set address key 10 on, 9 and 11 off; press ENTER.		CCW1, CC2, CS
15. Set all address keys off; press ENTER.		
16. Set rate switch to PROCESS.		

CCW2 Routine IOP202

Action	ROS Address	Channel Time
1. Set ROS address 030 in the storage data keys.		
2. Set ROS address compare switch to STOP.	030	CCW2, CC0
3. Set rate switch to SINGLE CYCLE.		
4. Set address key 11 on, 9 and 10 off; press ENTER.		
5. Press START.	A51	
6. Press START.	AD0	
7. Press START.	AB5	CCW2, CC0, A0
8. Set address keys 10 a. i 11 on, 9 off; press ENTER.		CCW2, CC0, A1
9. Set address key 10 on, 9 and 11 off; press ENTER.		CCW2, CC1, CS
10. Set address key 11 on, 9 and 10 off; press ENTER.		CCW2, CC1

Action	ROS Address	Channel Time
11. Press START.	A24	CCW2, CC1, A0
12. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW2, CC1, A1
13. Set address key 10 on, 9 and 11 off; press ENTER.		CCW2, CC2, CS
14. Set address key 11 on, 9 and 10 off; press ENTER.		CCW2, CC2
15. Press START.	BA2	
16. Press START.	03C	CCW2, CC2, A0
17. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW2, CC2, A1
18. Set address key 10 on, 9 and 11 off; press ENTER.		CCW2, CC3, CS
19. Set address key 11 on, 9 and 10 off; press ENTER.		CCW2, CC3, A0
20. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW2, CC3, A1
21. Set address key 10 on, 9 and 11 off; press ENTER.		CS
22. Set all address keys off; press ENTER.		
23. Press START.	940	
24. Set rate switch to PROCESS.		

Unit Select Routine IOP211

Note: Since the unit select routine does not have an associated ROS routine, it is impossible to ROS stop at the beginning of unit select. The following procedure will stop near the end of the CCW2 routine, step through to the end, and go to the beginning of the unit select routine.

Action	ROS Address	Channel Time
1. Set ROS address BA2 in the storage data keys.		
2. Set ROS address compare switch to STOP.	BA2	CCW2, CC2
3. Set rate switch to SINGLE CYCLE.		
4. Set address key 11 on, 9 and 10 off; press ENTER.		
5. Press START.	03C	CCW2, CC2, A0
6. Set address keys 10 and 11 on, 9 off; press ENTER.		CCW2, CC2, A1
7. Set address key 11 on, 9 and 10 off; press ENTER.		CCW2, CC3, A0
8. Set address key 10 on, 9 and 11 off; press ENTER.		CS
9. Press START.	940	
10. Set address key 11 on, 9 and 10 off; press ENTER.		Unit Sel, CC0, A0
11. Set address keys 10 and 11 on, 9 off; press ENTER.		Unit Sel, CC0, A1
12. Set address key 10 on, 9 and 11 off; press ENTER.		Unit Sel, CC1, CS
13. Set address key 11 on, 9 and 10 off; press ENTER.		Unit Sel, CC1, A0
14. Set address keys 10 and 11 on, 9 off; press ENTER.		Unit Sel, CC1, A1
15. Set address key 10 on, 9 and 11 off; press ENTER.		Unit Sel, CC2, CS
16. Set address keys 9 and 11 on, 10 off; press ENTER.		Unit Sel, ITD1 and not ITD2
17. Set address keys 9, 10, and 11 on; press ENTER.		Unit Sel, ITD2 and not ITD3
18. Set address keys 9 and 10 on, 11 off; press ENTER.		Write fetch ITD1 and not In Tag
19. Set all address keys off; press ENTER.		
20. Set rate switch to PROCESS.		

End Update Routine IOP209

Action	ROS Address	Channel Time
1. Set ROS address 00C in the storage data keys.		
2. Set ROS address compare switch to STOP.	00C	
3. Set rate switch to SINGLE CYCLE.		
4. Set address key 11 on, 9 and 10 off; press ENTER.		End Up, CC0
5. Press START.	B4E	
6. Press START.	BB5	End Up, CC0, A0
7. Set address keys 10 and 11 on, 9 off; press ENTER.		End Up, CC0, A1
8. Set address key 10 on, 9 and 11 off; press ENTER.		End Up, CC1, CS
9. Set address key 11 on, 9 and 10 off; press ENTER.		End Up, CC1
10. Press START.	BC4	
11. Press START.	B35	End Up, CC1, A0
12. Set address keys 10 and 11 on, 9 off; press ENTER.		End Up, CC1, A1
13. Set address key 10 on, 9 and 11 off; press ENTER.		End Up, CC2, CS
14. Set address key 11 on, 9 and 10 off; press ENTER.		End Up, CC2
15. Press START.	03C	
16. Set rate switch to PROCESS.		

Interrupt Routine IOP210

Action	ROS Address	Channel Time
1. Set ROS address 004 in the storage data keys.		
2. Set ROS address compare switch to STOP.	004	Irpt, CC0
3. Set rate switch to SINGLE CYCLE.		
4. Set address key 11 on, 9 and 10 off; press ENTER.		Irpt, CC0
5. Press START.	A00	
6. Press START.	A99	Irpt, CC0, A0
7. Set address keys 10 and 11 on, 9 off; press ENTER.		Irpt, CC0, A1

Action	ROS Address	Channel Time
8. Set address key 10 on, 9 and 11 off; press ENTER.		Irpt, CC1, CS
9. Set address key 11 on, 9 and 10 off; press ENTER.		Irpt, CC1
10. Press START.	AA7	
11. Press START.	AC2	Irpt, CC1, A0
12. Set address keys 10 and 11 on, 9 off; press ENTER.		Irpt, CC1, A1
13. Set address key 10 on, 9 and 11 off; press ENTER.		Irpt, CC2, CS
14. Set all address keys off; press ENTER.		Instruction Scan
15. Press START.	AB4	
16. Press START.	03C	

The interface portion of the interrupt routine is now complete. Continue single cycle to observe CSW store, exchange of PSW, and return to I-fetch.

1052 ADAPTER/PRINTER-KEYBOARD

Singleshot Adjustment

1. Turn off motor switch (located under typewriter); press not ready key on typewriter console.
2. Enter ROS address 200 in the data keys; set ROS repeat switch on; press start pushbutton. The IAR should be rippling.
3. Adjust singleshots in Figure 108 (all test points are on C1E4 panel). Connect a long jumper from 1A-B1G4D06 to input point called out in the procedure (RA011 SAR 15). Measure all timings at the 1.5 volt level. See Figure 109 for 1052 read flow chart.

Switch and Indicator Check

1. Set motor switch on (located under typewriter).
2. Set the following typewriter switches on: CE mode and Cont Write; continuous printing of O A O A etc. should occur. While the 1052 is printing recheck and re-adjust (if necessary) all singleshots.
3. The following indicators should be on: Write, Printer, Busy, and Upper Case.
4. Set switch to read position; read indicator and read proceed indicator should come on.
5. Type all characters on keyboard and check printout. Check carriage return key and the fact that the right-hand margin forces a carriage return. Ensure that last character typed on extreme right-hand side does not type over character next to it.
6. Put 1052 on line. Ensure that 1052 is in upper case. Press power off pushbutton; press power on pushbutton and ensure that intervention required indicator is on. (Power on reset turns off equipment check on the 1052.) Press ready pushbutton on the 1052 and ensure that the ball on the 1052 rotates 180° and that the intervention required indicator goes off.

Tiedown to ground	Page	SS Designation	Test Point	Duration	Tolerance	Adjust	Input Point
G7B03	PG 601	SS 1	F6D04	+ 700ns	± 35ns	CPG7	G7B07
G7B03	PG 601	SS 2	F6D05	+ 200ns	± 10ns	LPG7	G7B07
E7B03	PG 601	SS 4	F6B03	+ 200ns	+0 to -10ns	CPE7	E7B07
*	PG 601	SS 5	D5B03	+ 28ms	-0 +1.4ms	CPD7	D7D10
*	PG 601	SS 6	F6B08	+ 500ns	± 25ns	LPE7	D7D10
*	PG 601	SS 7	F6D11	+ 200ns	± 10ns	UPE7	D7D10
**	PG 621	Alarm	D7D06	- 30ms	± 1.5ms	LPD7	D4M5B12
Pull G5	PG 621	Ready	G7D12	- 200ns	± 10ns	UPG7	D5D06

*Pull M3 (PG631)

F6D09 to ground (PG 641 Ch 4)
F6B12 to ground (PG 631 BU4)
1052 in CE mode read condition.

These pulses may be difficult to see. Proper scope adjustment is important.

**Panel change this point only.

FIGURE 108. 1052 SINGLESHOT TIMING PROCEDURE

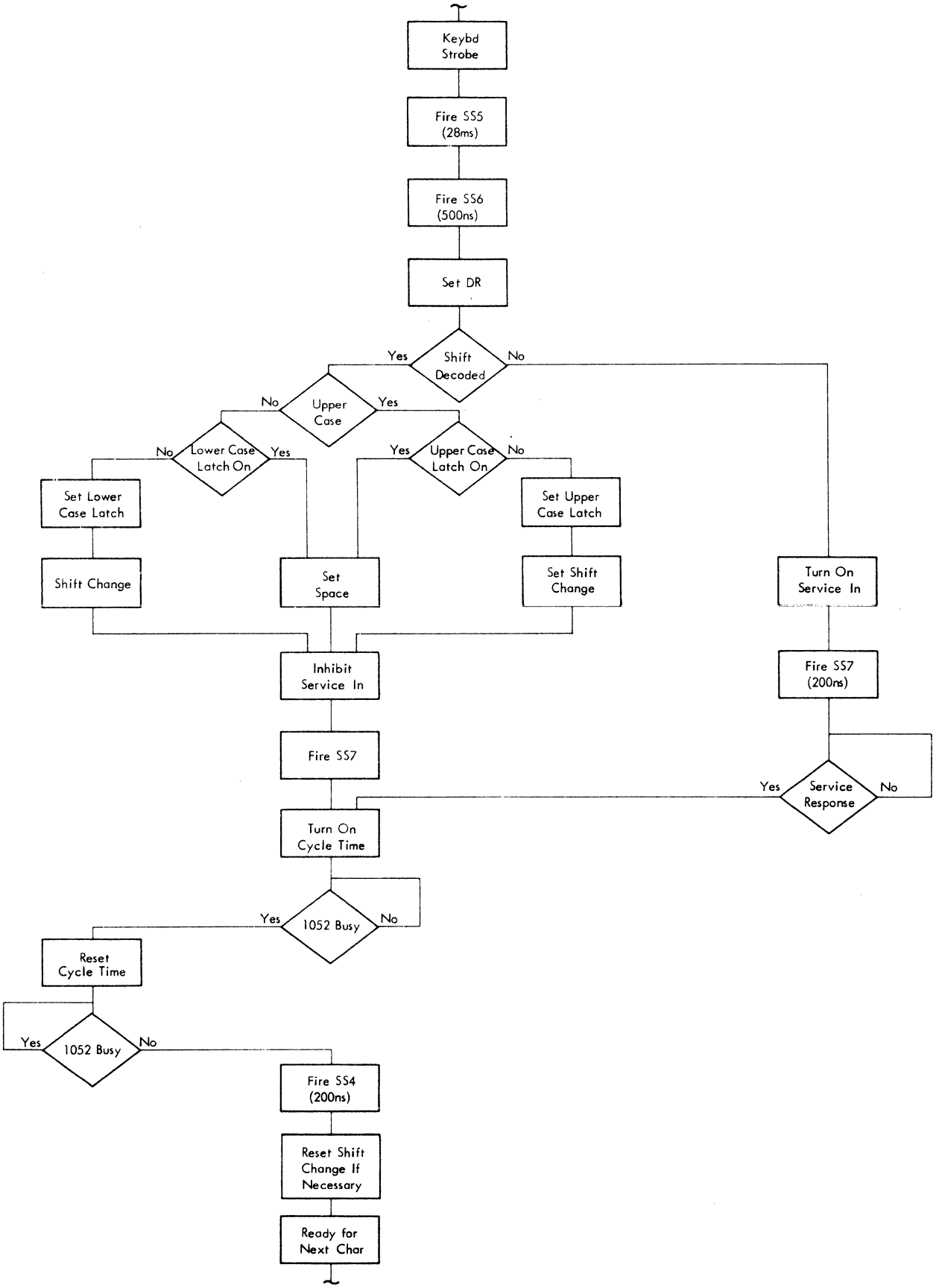


FIGURE 109. 1052 READ SEQUENCE

EMULATOR SERVICE AIDS

1410/7010 EMULATOR DELAYS

Figure 110 shows the selector channel delays and adjustments for the 1410/7010 Compatibility Feature.

1410/7010 DISK CONVERSION

2302 Disk Storage Map

The following map of the 2302 Disk Storage shows the track allocation used by the 1410/7010 Emulator:

From Cylinder/ Head	Through Cylinder/ Head	Function
0-0	0-39	Contains standard information (initial program loader, volume label, etc.)
0-40	218-11	1301 emulation area
218-13	245-45	Unused by the emulator
246-0	249-45	Alternate track area

2302 Track Correspondence

The 1410/7010 Emulator uses sequential tracks on the 2302 Disk Storage. The location of a 2302 track corresponding to a particular 1301/2302 track may be determined by using the following algorithm:

(1301/2302 track address + 40) ÷ 46
- Quotient = 2302 cylinder number
- Remainder = 2302 head number

Example:
1410/7010 1301/2302 track address = 1000
(1000 + 40) ÷ 46 = 22, remainder = 28
Therefore: 2302 address is cylinder 22, head 28.

2314 Disk Storage Map

The following map of the 2314 Disk Storage shows the track allocation used by the 1410/7010 Emulator:

From Cylinder/ Head	Through Cylinder/ Head	Function
0-0	0-19	Contains standard information (initial program loader, volume label, etc.)
1-0	198-19	1301/2302 emulation area
199-0	199-19	Unused by the emulator
200-0	202-19	Alternate track area

Note: Four 2314 drives are required for each 1410/7010 access; however, only three drives are physically used by the emulator. Drive 1 contains 1410/7010 tracks 0000-3959, drive 2 contains tracks 3960-7919, and drive 3 contains tracks 7920-9999. Drive 4 is available for any function the user desires.

2314 Track Correspondence

The 1410/7010 Emulator uses sequential tracks spread across three 2314 drives, omitting the first and last cylinders on each drive. The location of a 2314 track corresponding to a particular 1301/2302 track may be determined by using the following algorithm:

(1301/2302 track address)÷ 3960
- Quotient = Relative device number
- Remainder = Relative track number within the 2314 device

Add 20 to the remainder (to bypass cylinder 0).
Divide this sum by 20 (number of tracks per cylinder within a 2314 device).
- Quotient = 2314 cylinder number
- Remainder = 2314 head number.

Example:
1410/7010 1301/2302 track address = 1000
1000 ÷ 3960 = 0, remainder = 1000
(1000 + 20) ÷ 20 = 51, remainder = 0
Therefore: 1410/7010 track address 1000 is located on the first 2314 drive, cylinder 51, head 0.

	Type of Delay	Page	Location	Setting	Test Point
Channel 1	Svc Out	XE621	02C-E4G3A1	125	Fixed Setting
	Svc Out	XE621	02C-F4G3B1	100	Fixed Setting
	Svc In	XE631	02C-E4H3A1	125	Fixed Setting
	Svc In	XE631	02C-E4H3B1	100	Fixed Setting
	In Tag	XE641	02C-E4E3A1	50	Fixed Setting
	Out Tag	XE651	02C-E4E3B1	50	Fixed Setting
	Select Out	XE661	02C-E4L6B1	60	Fixed Setting
	Late Reg Delayed	XE521	02C-E4L6A1	70	02C-E4K6D12 (XE521 TR4)
Channels 2 and 3	Svc Out	XE801	01Y-P4G3A1	125	Fixed Setting
	Svc Out	XE801	01Y-P4G3B1	100	Fixed Setting
	Svc In	XE811	01Y-P4H3A1	125	Fixed Setting
	Svc In	XE811	01Y-P4H3B1	100	Fixed Setting
	In Tag	XE821	01Y-P4E3A1	50	Fixed Setting
	Out Tag	XE831	01Y-P4E3B1	50	Fixed Setting
	Select Out	XE841	01Y-P4L6B1	60	Fixed Setting

FIGURE 110. 1410/7010 EMULATOR DELAYS

1410/7010 DIAGNOSE INSTRUCTION ADDRESSES

Instruction	ROS Address	CAS Page
Link Back	AB1	QR181
Special Scan	A36	QR900
Start I/O	AB8	QR920
Device Table Search	AD5	QR930
CCW Create	AB5	QR910

START I/O DIAGNOSE INSTRUCTION

Under normal System/360 operation, when a start I/O instruction is given, bit positions 4 through 7 of the channel address word (CAW) must contain zeros, and bit positions 38 and 39 of every channel command word (CCW) except one specifying transfer in channel must contain zeros. If either of these restrictions is violated, program check is stored in the channel status word.

The start I/O diagnose instruction inhibits normal validity checks of bits 4 through 7 of the CAW and bit 38 and 39 of CCW. Instead, these bits are used for translator control. CAW bit 5 must be on if the start I/O diagnose instruction is used; otherwise, a program check indication is stored in the channel status word (CSW).

CAW Bits 4-7	Meaning
0100	Tape move mode
0101	Disk move mode
0110	Tape load mode
0111	Disk load mode
1100	Tape move mode, odd parity
1101	Illegal
1110	Tape load mode, odd parity
1111	Illegal

CCW Bits 38-39	Meaning
00	No translation
01	Meaningless results
10	Tape or disk load mode, read
11 (read op)	Tape or disk move mode and wordmark preservation
11 (write op)	Write translation

There is one parameter for the start I/O diagnose instruction. The "x" in the general diagnose instruction format specifies a GPR that contains the channel and unit address (in the low-order 11 bits) of the I/O device to be used.

7070/7074 OPERATION CODES

Figure 111 is a list of emulated operation codes for 7070/7074 systems.

S,0,1	Abbreviation	Name	Digit 4 - Digit 5		Digits 6,7,8,9	Comments
+00	HB	Halt and Branch	Not used		Branch address	Next instruction from PR 6-9.
-00	HP	Halt and Proceed	Not used		Not used	Next instruction from IC.
+01	B	Branch	Not used		Branch address	Unconditional branch without halt; next instruction from PR 6-9.
-01	NOP	No Operation	Not used		Not used	Next instruction from IC.
+02	BLX	Branch and Load Location in Index Word	Index Word for storing IC		Branch address	Contents of IC are stored in index word, positions 2-5.
+03	CD	Compare Storage to Digit	Value compared	Position to be compared	Address of data	Turns on high, low, or equal indicator.
-03		Sign Control	Sign value	Operation:		Compare operations turn on high, low, or equal indicator:
	CSA	Compare Sign to Alpha	3,6, or 9	0. Compare	Address of data for operations	
	CSM	Compare Sign to Minus		1. Make	0-1	
	CSP	Compare Sign to Plus		2. Sign change sense	Not used for operations 2 and 3	Highest +9999999999
	MSA	Make Sign Alpha		3. Sign change stop		+0000000000
	MSM	Make Sign Minus		4. Sign change test	Branch address for operation 4	-0000000000
	MSP	Make Sign Plus				-9999999999
	SMSC	Operation 2				@9999999999
	HMSC	Operation 3				Lowest @0000000000
	BSC	Operation 4				
+08						
-08	Unemulated					
+09	Operations					
-09						
+10	BZ1	Branch if Zero in Accumulator 1	Not used		Branch address	Sign is ignored.
-10	BM1	Branch if Minus in Accumulator 1	Not used		Branch address	Contents are ignored.
+11	BV1	Branch if Overflow in Accumulator 1	Not used		Branch address	If overflow indicator is on, branch and turn it off.
-11	ZST1	Zero Storage and Store Accumulator 1	Field definition		Address of data	
+12	ST1	Store Accumulator 1	Field definition		Address of data	
-12	STD1	Store Digits from Accumulator 1 and Ignore Sign	Field definition		Address of data	
+13	ZA1	Zero Accumulator 1 and Add	Field definition		Address of data	
-13	ZS1	Zero Accumulator 1 and Subtract	Field definition		Address of data	
+14	A1	Add to Accumulator 1	Field definition		Address of data	
-14	S1	Subtract from Accumulator 1	Field definition		Address of data	
+15	C1	Compare Accumulator 1 to Storage	Field definition		Address of data	Sets high, low, or equal indicator.
-15	CA	Compare Absolute in Accumulator 1 to Absolute in Storage	Field definition		Address of data	Sets high, low, or equal indicator.
+16	ZAA	Zero Accumulator 1 and Add Absolute	Field definition		Address of data	
-16	ZSA	Zero Accumulator 1 and Subtract Absolute	Field definition		Address of data	
+17	AA	Add Absolute to Accumulator 1	Field definition		Address of data	
-17	SA	Subtract Absolute from Accumulator 1	Field definition		Address of data	
+18	AS1	Add to Storage from Accumulator 1	Field definition		Address of data	
-18	SS1	Subtract Accumulator 1 from Storage	Field definition		Address of data	
+19	AAS1	Add to Absolute Storage from Accumulator 1	Field definition		Address of data	
+20	BZ2	Branch if Zero in Accumulator 2	Not used		Branch address	Sign is ignored.
-20	BM2	Branch if Minus in Accumulator 2	Not used		Branch address	Contents are ignored.
+21	BV2	Branch if Overflow in Accumulator 2	Not used		Branch address	If overflow indicator is on, branch and turn if off.
-21	ZST2	Zero Storage and Store Accumulator 2	Field definition		Address of data	
+22	ST2	Store Accumulator 2	Field definition		Address of data	
+23	ZA2	Zero Accumulator 2 and Add	Field definition		Address of data	
-23	ZS2	Zero Accumulator 2 and Subtract	Field definition		Address of data	
+24	A2	Add to Accumulator 2	Field definition		Address of data	
-24	S2	Subtract from Accumulator 2	Field definition		Address of data	
+25	C2	Compare Accumulator 2 to Storage	Field definition		Address of data	Sets high, low, or equal indicator.
+28	AS2	Add to Storage from Accumulator 2	Field definition		Address of data	
-28	SS2	Subtract Accumulator 2 from Storage	Field definition		Address of data	
+29	AAS2	Add to Absolute Storage	Field definition		Address of data	
+30	BZ3	Branch if Zero in Accumulator 3	Not used		Branch address	Sign is ignored.
-30	BM3	Branch if Minus in Accumulator 3	Not used		Branch address	Contents are ignored.
+31	BV3	Branch if Overflow in Accumulator 3	Not used		Branch address	If overflow indicator is on, branch and turn it off.
-31	ZST3	Zero Storage and Store Accumulator 3	Field definition		Address of data	
+32	ST3	Store Accumulator 3	Field definition		Address of data	
-32	STD3	Store Digits from Accumulator 3 and Ignore Sign	Field definition		Address of data	

FIGURE 111. EMULATED 7070/74 OPERATION CODES (PART 1 OF 4)

S,0,1	Abbreviation	Name	Digit 4 - Digit 5	Digits 6, 7, 8, 9	Comments
+33	ZA3	Zero Accumulator 3 and Add	Field definition	Address of data	
-33	ZS3	Zero Accumulator 3 and Subtract	Field definition	Address of data	
+34	A3	Add to Accumulator 3	Field definition	Address of data	
-34	S3	Subtract from Accumulator 3	Field definition	Address of data	
+35	C3	Compare Accumulator 3 to Storage	Field definition	Address of data	Sets high, low, or equal indicator.
+38	AS3	Add to Storage from Accumulator 3	Field definition	Address of data	
-38	SS3	Subtract Accumulator 3 from Storage	Field definition	Address of data	
+39	AAS3	Add to Absolute Storage from Accumulator 3	Field definition	Address of data	
+40	BL	Branch if Low	Not used	Branch address	Tests the low indicator.
-40	BH	Branch if High	Not used	Branch address	Tests the high indicator.
+41	BFV SMFV HMFV	Field Overflow Control	Not used Operation: 0. Test 1. Sense 2. Stop	Branch address in operation 0; not used for operations 1-2 operations 1-2	Test operation tests field overflow indicator.
-41	BE	Branch if Equal	Not used	Branch address	Tests the equal indicator.
-43	BCX	Branch Compared Index Word	Operand index word	Branch address	
+44	BXN	Branch if Index Word Indexing Portion is Non-Zero	Operand index word	Branch address	Sign and the other six digit positions are ignored.
-44	BXM	Branch if Index Word is Minus	Operand index word	Branch address	Contents are ignored.
+45	XL	Index Word Load	Operand index word	Address of data	
-45	XU	Index Word Unload	Operand index word	Address of data	
+46	XZA	Index Word Zero and Add to Indexing Portion	Operand index word	Four-digit factor	Sign is set to plus and the other six digits are unchanged.
-46	XZS	Index Word Zero and Subtract from Indexing Portion	Operand index word	Four-digit factor	Sign is set to minus and the other six digits are unchanged.
+47	XA	Index Word Add to Indexing Portion	Operand index word	Four-digit factor	Sign may change; other positions are unchanged.
-47	ZS	Index Word Subtract from Indexing Portion	Operand index word	Four-digit factor	Sign may change, other positions are unchanged.
+48	XSN	Index Word Set Non-indexing	Operand index word	Four-digit factor	Sign and the other six digits are unchanged
-48	XLIN	Index Word Load with Interchange	Operand index word	Address of data	Positions 2-5 and 6-9 are interchanged.
+49	BIX	Branch Incremented Index Word	Operand index word	Branch address	Branch if indexing portion (incremented by 1) is not greater than non-indexing portion.
-49	BDX	Branch Decremented Index Word	Operand index word	Branch address	Branch if decremented indexing portion is not brought to zero or beyond non-indexing value.
+50	SR# SRR# SL# SLC#	Shift Control	Index word for shift and count	Acc. (1-3) Opn. * Length of shift (00-10)	*Operation: 0. Shift right 1. Shift right and round 2. Shift left 3. Shift left and count
-50	SR SRR SL SLC SRS SLS SRS SLS	Coupled Shift Control	Index word for shift	Digit position for split; 0 for normal Opn. * Length of shift (00-20)	*Operation, normal: 0. Shift right 1. Shift right and round 2. Shift left 3. Shift left and count *Operation, split: 4. Shift right from point Acc 1. 5. Shift left from point Acc 1 6. Shift right from point Acc 2 7. Shift left from point Acc 2
+51		Branch on Alteration Switch or Channel Busy	Operation: Switch 1-4 Sync or Chan 1-4 0. Alteration switch 1. Sync busy 2. Channel busy	Branch address	
+53	M	Multiply	Field definition of multiplier	Address of multiplier	Beginning: Multiplicand in Accumulator 3. End : Product in Accumulators 1 and 2; multiplicand in Accumulator 3.
-53	D	Divide	Field definition of divisor	Address of divisor	Beginning: Dividend in Accumulators 1 and 2. End : Quotient in Accumulator 2, remainder in Accumulator 1; divisor in Accumulator 3.
+54		Inquiry Control	Unemulated operation		
+55	PC	Priority Control	4: Not used 5: Mask register 0 or 1	Address of priority mask	0 - Allow; 1 - Mask

FIGURE 111. EMULATED 7070/74 OPERATION CODES (PART 2 OF 4)

S,0,1	Abbreviation	Name	Digit 4 - Digit 5	Digits 6,7,8,9	Comments
+56	ENA	Edit Numeric to Alphameric		Address of first record definition word	RDW defines alpha area.
-56	ENS	Edit Numeric to Alphameric with Sign Control	Index word, in which 2-5 locates first numeric word	Address of first record definition word	RDW defines alpha area.
+57	ENB	Edit Numeric to Alphameric with Blank Insertion		Address of first record definition word	RDW defines alpha area.
-57	EAN	Edit Alphameric to Numeric		Address of first record definition word	RDW defines alpha area.
+60		Stacking Latch Test	Stacking latch:	Branch address	
	BAL		00 Any stacking latch		
	BUL		01 Unit record A		
	BUL		02 Unit record B		
	BTL		10-19 Tape units 0-9 sync 1		
	BTL		20-29 Tape units 0-9 sync 2		
	BTL		30-39 Tape units 0-9 sync 3		
	BTL		40-49 Tape units 0-9 sync 4		
+61		Electronic Switch Control	Operation: Switch Number	Branch address	Controls the ten switches in word 0101.
	BES		0. Test		
	ESN		1. Turn on (0-9)		
	ESF		2. Turn off		
	BSN		3. Test and turn on		
	BSF		4. Test and turn off		
-61		Stacking Latch Set	Stacking latch:	Not used	
	ULN		01 Unit record A		
	ULN		02 Unit record B		
	TLN		10-19 Tape units 0-9 sync 1		
	TLN		20-29 Tape units 0-9 sync 2		
	TLN		30-39 Tape units 0-9 sync 3		
	TLN		40-49 Tape units 0-9 sync 4		
+62		Electronic Switch Control	See +61		Controls the ten switches in word 0102.
-62		Stacking Latch Reset	Stacking latch	Not used	
	ULF		Same as -61		
	TLF				
+63		Electronic Switch Control	See +61		Controls the ten switches in word 0103.
+64	PR	Priority Release	Not used	Branch address	Branch address is usually 0097.
+65	RS	Record Scatter	Index word, in which 2-5 locates first transmitting word	Address of first record definition word	RDW defines receiving area.
-65	RG	Record Gather	Index word, in which 2-5 locates first receiving word	Address of first record definition word	RDW defines transmitting area.
+66	LL	Lookup Lowest	Field definition	Address of first RDW	Entire table is always searched.
+67	LE	Lookup Equal Only	Field definition	Address of first RDW	Index word 98: Positions 2-5, found address
+68	LEH	Lookup Equal or High	Field definition	Address of first RDW	Positions 6-9, increment
+69		Unit Record Control	Sync Operation:	Address of first RDW	IC + 1 Error IC + 2 EOF (not punch) IC + 3 Normal
	US		(1-3) 0. Set PES		
	UR		(1-3) 1. Read (7500)		
			(4) 1. Read (7501)		
	UW/UP		(1-3) 2. Write or Punch		
	UWIV/UPIV		(1-3) 3. Write or Punch invalid		IC + 1
	TYP		(0) 4. Type		IC + 1 Error IC + 2 Normal
+70	FBV	Floating Branch Overflow	Not used	Branch address	Tests the floating decimal overflow indicator.
-70	FBU	Floating Branch Underflow	Not used	Branch address	Tests the floating decimal underflow indicator.
+71	FR	Floating Round	Not used	Not used	
+73	FM	Floating Multiply	Not used	Address of multiplicand	
-73	FD	Floating Divide	Not used	Address of divisor	
+74	FA	Floating Add	Not used	Address of data	Accumulator 2 cleared at start.
-74	FS	Floating Subtract	Not used	Address of data	Accumulator 2 cleared at start.
+75	FZA	Floating Zero and Add	Not used	Address of data	
-75	FDD	Floating Divide Double Precision	Not used	Address of divisor	
+76	FAD	Floating Add Double Precision	Not used	Address of data	Accumulator 2 not cleared at start.
-76	FADS	Floating Add Double Precision Suppress Normalization	Not used	Address of data	
+77	FAA	Floating Add Absolute	Not used	Address of data	
-77	FSA	Floating Subtract Absolute	Not used	Address of data	

FIGURE 111. EMULATED 7070/74 OPERATION CODES (PART 3 OF 4)

S,0,1	Abbreviation	Name	Digit 4 - Digit 5		Digits 6,7,8,9	Comments
+81		Tape Control 1	Tape unit	Operation:	If position 5 is not 0, address of	
-81	TR*		(0-9)	1. Read	first RDW.	
	TRR*			2. Read per RM		
	TW*			3. Write		
	TWR*			4. Write per RM		
	TWZ*			5. Write with zero elimination		
	TWC*			6. Write per RM and zero elimination		
	TSF*			7. Segment forwardspace per count		
	TSB*			8. Segment backspace per count		
	TRA*, **			9. Read all alpha		
				0. Operation in position 9		
	TSEL	+ Priority			0. No-op select	
	TM*	-No Priority			1. Write tape mark	
	TRW				2. Rewind	
	TRU				3. Rewind/unload	
	TRB				4. Backspace	
	TSM*				5. Write tape segment mark	
	TSK				6. Skip	
	TEF				7. Turn off EOF	
	TSLD				8. Set low density	
	TSHD				9. Set high density	
		*May set a stacking latch				
		**May be treated as a Read				
+82	Same as ± 81					
-82	except other					
+83	sync is used					
+84						
-84						

Note: All other 7070/74 operation codes are unemulated.

FIGURE 111. EMULATED 7070/74 OPERATION CODES (PART 4 OF 4)

POWER SYSTEM SERVICE CHECKS

- Figure 112 shows the power-on sequence.
- Figure 113 shows the power-off sequence.
- YB401 shows how to adjust the overvoltage reference potentiometers.

Converter-Inverter

When the converter-inverter fails, the circuitry can be checked rapidly with an oscilloscope and an ohmmeter. The oscilloscope is used to check the silicon-controlled rectifier (SCR) gate signals and the ohmmeter is used to check the other rectifiers.

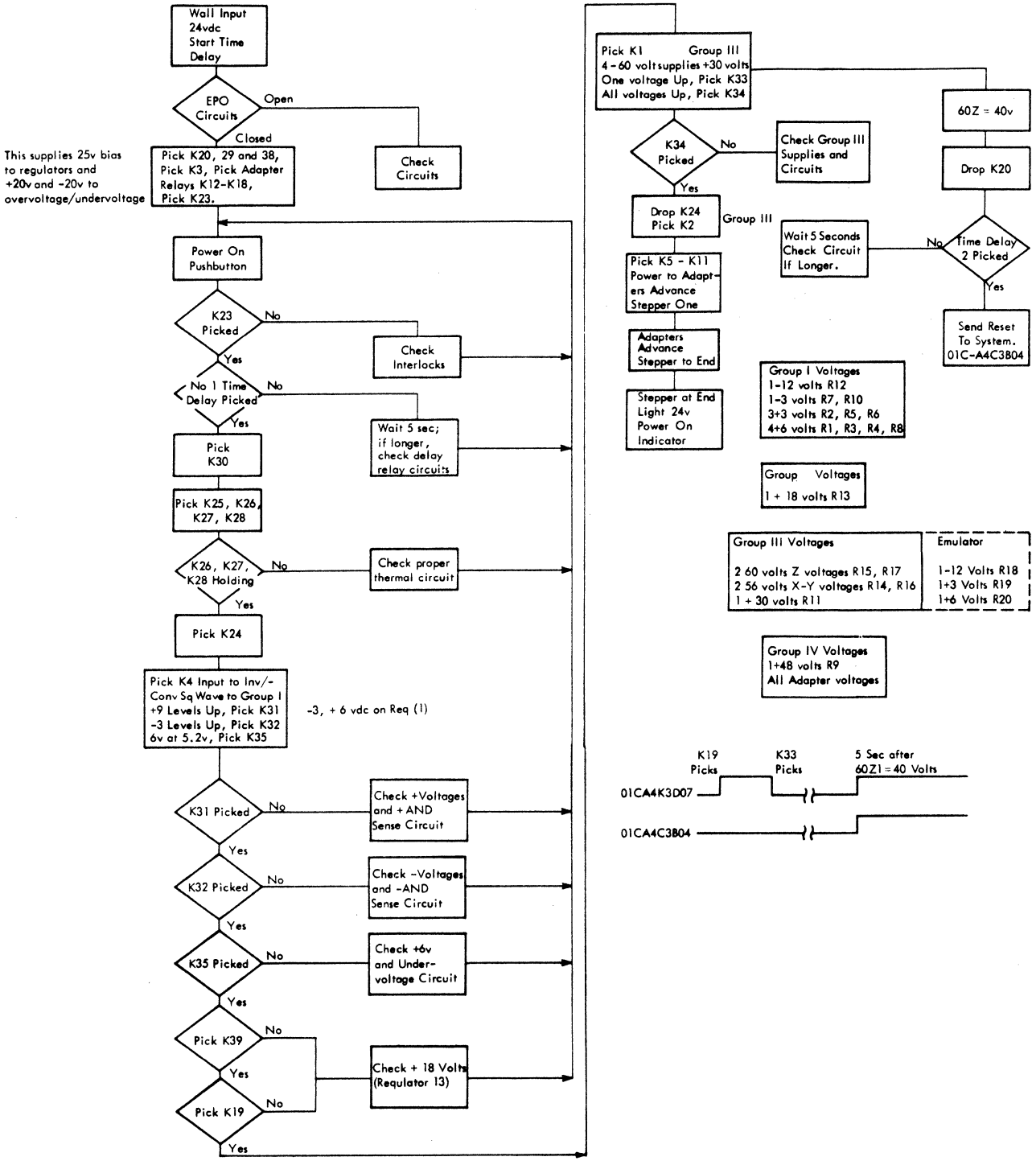


FIGURE 112. POWER ON SEQUENCE

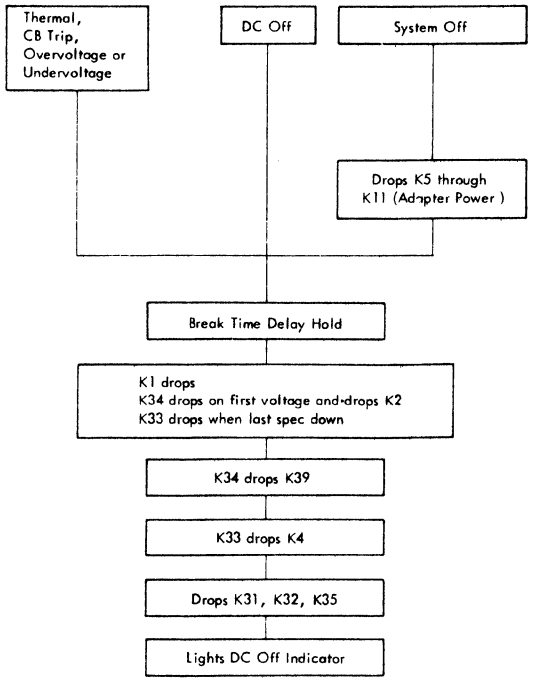


FIGURE 113. POWER/DC OFF SEQUENCE

SCR Gate Signals

Always check the SCR gate signals when a failure occurs. The gate signals are the most critical operating requirement of the inverter. Any abnormal variation from the general voltage wave shapes shown in Figure 114 will cause the inverter to fail. The SCR gate signals are measured when the three-phase input power is off. The large allowable percentage variations on the gate signal voltages are mainly attributable to the correspondingly large variations of SCR gate impedance. If all of the timing measurements are out of the specified tolerances, a potentiometer located on the oscillator card may be adjusted to give the correct 2.5-kc operating frequency.

If the SCR gate signals are normal, critical components may be checked at the converter-inverter terminal boards (Figures 115 and 116) with an ohmmeter. Remember that a good rectifier has a high resistance in only one direction but a good SCR has a high resistance in both directions.

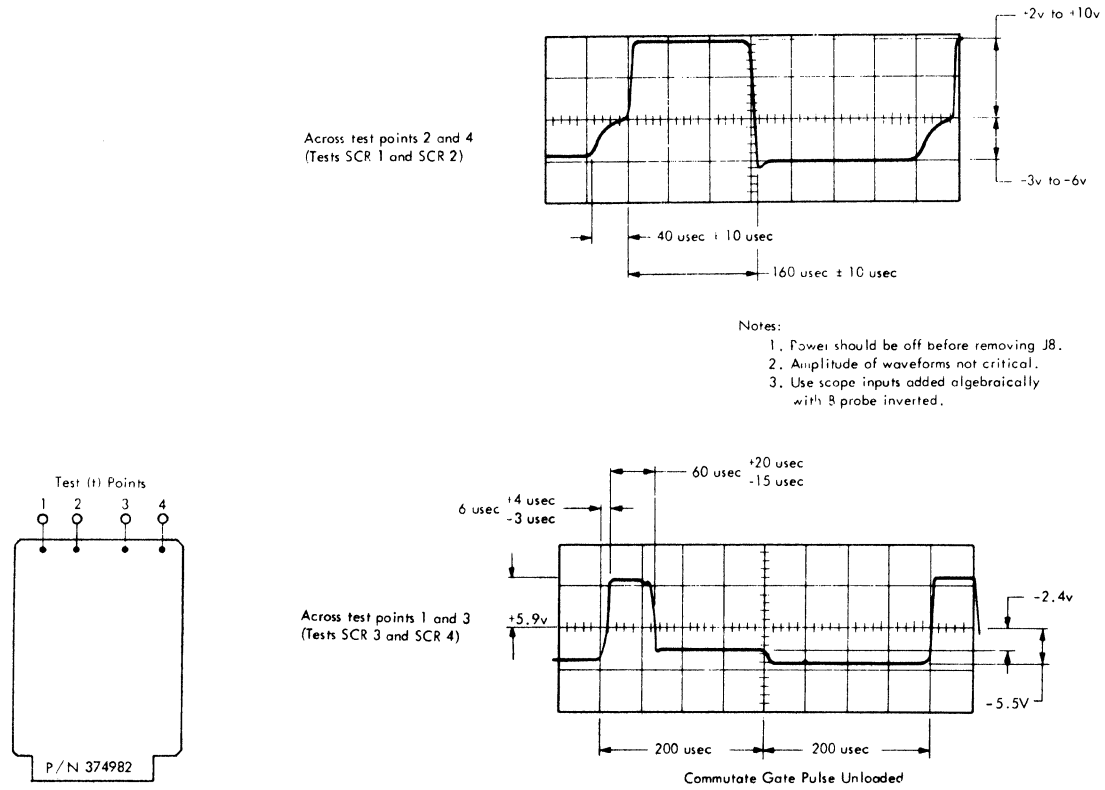
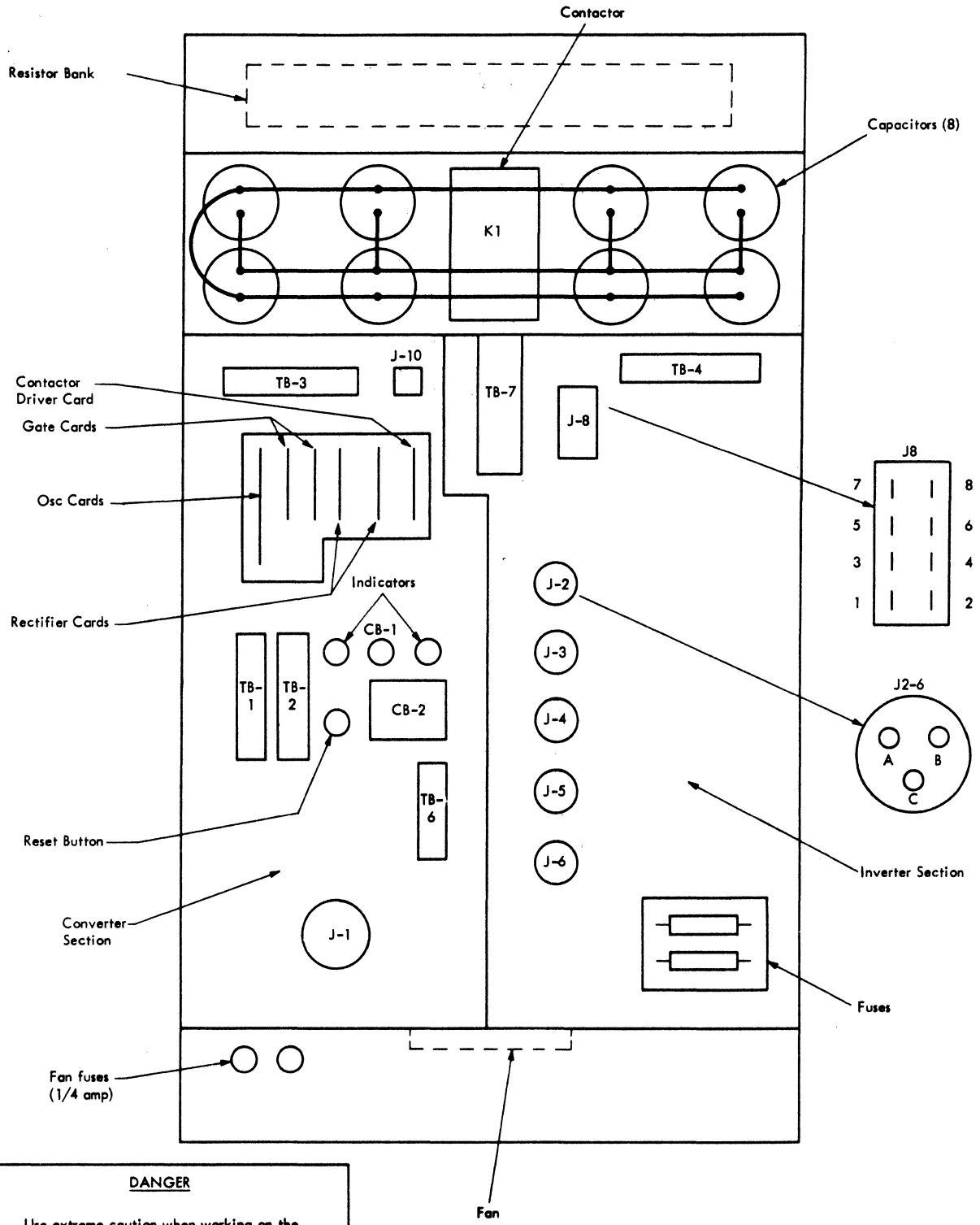


FIGURE 114. CONVERTER-INVERTER TESTPOINTS AND WAVEFORMS



DANGER

Use extreme caution when working on the converter-inverter. High voltages are present throughout the converter-inverter tub assembly, including the heat sinks that are floating and the SMS cards.

FIGURE 115. CONVERTER-INVERTER (COVER OFF)

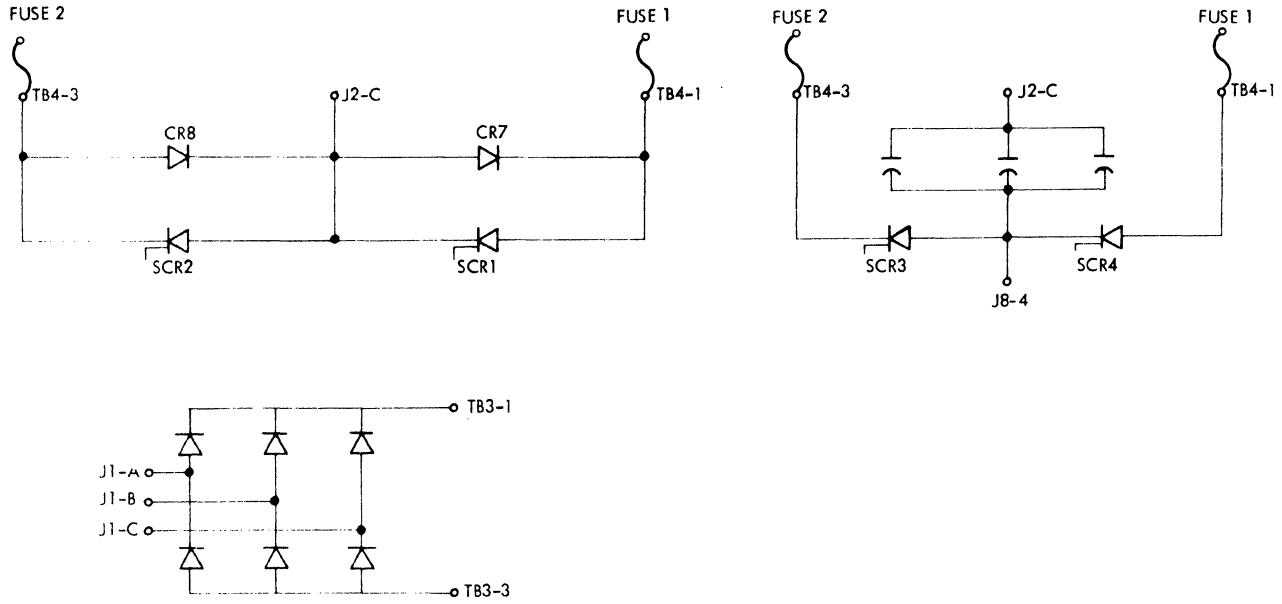


FIGURE 116. CONVERTER-INVERTER TEST POINTS

Types of Failures

Following are the four general classifications of failures on the converter-inverter.

1. Inverter blows fuses on start.
2. Inverter blows fuses when load is applied.
3. Inverter blows fuses after running for a short time.
4. Input circuit breaker trips on start.

Inverter Fuses Blow on Start: If the SCR gate signals are normal, use the following procedure to locate the fault.

1. Remove the converter-inverter cover (Figure 115).
2. Replace the blown inverter fuses.
3. With all power removed from the machine, use an ohmmeter to test the components attached to the terminal board terminals in Figure 116 and locate the faulty component. Remove the inverter chassis if necessary.

Inverter Fuses Blow When Load is Applied: If the SCR gate signals are normal, scope the SCR gate signals for noise while the unit is running with no load. Also, the turn-off time of a newly replaced SCR may not meet the specification.

Inverter Fuses Blow After Running a Short Time: If the SCR gate signals are normal, watch for a change with temperature rise that comes with the application of a load. Check the inverter components per Figure 116. Remove the inverter chassis if necessary.

Inverter Circuit Breaker Trips on Start: This symptom indicates either a short-circuited load or a faulty inverter component. Remove the normal load to prove whether the load is shorted or not before testing for faulty components with an ohmmeter (Figure 116).

Converter-Inverter Fuse Replacement

The converter-inverter fuses may be reached for replacement by removing main power plug P1 from its socket on the back of the PDU and opening the access door.

Converter-Inverter Troubleshooting

Converter-inverter troubles can be worked on without any load. For instance, remove P2-P6 and no dc voltages will be generated.

Voltage Regulator Test Points

Figure 117 shows the meter test points and the ripple test points of all the voltage regulators in the 2050 Processing Unit. The ripple, including noise and voltage variation, should not exceed ±4%.

Changing Voltage Regulators

Remember that with a normal power-off, the 28 volt bias voltage is still present on all voltage regulators. To remove this bias voltage in order to change a regulator, manually trip circuit breaker 9.

Regulator	Voltage	Ripple Test Point	Meter Point
1A	+6 VAR	01AD4G4B09	Gate A-TB-2-4
1B	+6 TC	01AD4G2D04	Gate A-TB-2-5
1C	+6 ROS	01CA2B6B11	Gate C-UOBD-12
2	+3	01AE4M2D03	Gate A-TB-2-12
3	+6	01BB4M2B11	Gate B-TB-2-12
4	+6	01BA1B2B11	Gate B-TB-1-12
5	+3	01BB4M2D03	Gate B-TB-2-8
6	+3	02BA3M2D03	02B-TB1-8
7	-3	01AE1B1B06	Gate A-TB-1-10
8	+6	Gate C-UOBD-8	Gate C-UOBD-8
9	+48	Feed Thru Capacitor C-57 in PDU	Feed Thru Capacitor C-57 in PDU
10	-3	02BA3M2B06	Gate 02B-TB-1-10
11	+30	01AD4G2B02	Gate A-TB-2-1
12	-18	Gate C-UOBD-6	Gate C-UOBD-6
13	+18	M9-BSM 1 TB1-6	M9-BSM 1 TB1-6
14	+56	M9-BSM 1 TB1-2	M9-BSM 1 TB1-2
15	+60	M9-BSM 1 TB1-4	M9-BSM 1 TB1-4
16	+56	M9-BSM 2 TB1-2	M9-BSM 2 TB1-2
17	+60	M9-BSM 2 TB1-4	M9-BSM 2 TB1-4

Reg 384K	Reg 512K	Voltage	Meter and Ripple Test Point	
1	1	+60	M9-BSM 3 TB1-4	For 384K or 512K Storage Feature, Located in Power Frame 04
-	2	+60	M9-BSM 4 TB1-4	
2	3	+56	M9-BSM 3 TB1-2	
-	4	+56	M9-BSM 4 TB1-2	
3	5	+18	M9-BSM 3 TB1-9	
4	6	+3	M9-BSM 3 TB1-13	
5	7	-3	M9-BSM 3 TB1-15	
6	8	+6	M9-BSM 3 TB1-11	

Note: Maximum allowable ripple is $\pm$4% of the nominal voltage. Ripple includes voltage variation, ripple and noise.

FIGURE 117. VOLTAGE REGULATOR TEST POINTS

Voltage Sequence Problems

To assist in servicing sequence problems, the voltage sequencing can be stopped in various points of its cycle by selectively removing the P2-P6 plugs from the converter-inverter. For instance, all power except for the 60 volt XY, the 60 volt Z, and the -12 ROS voltage can be brought up and examined if P5 and P6 are removed. An examination of the YB logic pages shows which regulators are fed from each plug. This allows you to inspect certain voltages in their proper sequence without possible damage to drivers, etc., if one of the logic voltages is not functioning properly.

Plus 18 Volt Sequence Down

The +18v should remain up for at least one second after the loss of the 56XY or 60Z voltages. Adjusting the RC-time constant around the K39 contactor core (YB221) controls K39 dropout. The following sequence can be used to adjust the resistor:

1. With power down, preset resistor R23 (in lower right-hand ac compartment) to half its value.
2. With the A probe, monitor the 60Z (regulator 15) at the plus bus.
3. Sync on the fall of 60Z and set the scope sweep for 1 sec/cm.
4. Set the scope mode switch to see both A and B probes simultaneously (chopped).
5. With the B probe, monitor the output of the 18-volt regulator.
6. Drop power; note the time difference between the fall of 60Z and 18-volt supplies.
7. Set R23 to approximately one-third resistance so that the time is at least one second; no harm will result if the time is more than one second. To lengthen dropout time, increase the resistance of R23 (however, if a very high resistance is used, the dropout time will be greatly reduced instead of lengthened).

Once the resistor is set, the difference should be checked between all 60- and 56-volt supplies (A probe) and the 18-volt supply; there should be a delay of at least one second with any one of the 60 or 56 supplies.

Overcurrent Problems

Overcurrent problems usually cannot be found by resistance checking, due to the very low load resistance. However, the load can be selectively uncoupled by removing laminar bus connections or, when the trouble is isolated to a board, by removing the bus to jumper plugs one at a time to find the row at fault. (Use logic pages YB411 and YB421 to assist in finding the proper bus terminals.)

Note: Use care in removing voltage regulator loads in storage areas. If -3 volts are removed and the storage driver voltages are still present, the drivers could be ruined. If a -3 voltage regulator overloads on a storage board, remove the driver voltages before removing the -3 volt loads.

Voltage Regulator Problems

Following is a suggested sequence to use when a voltage regulator is causing a problem:

1. Replace the overcurrent and regulator cards.
2. Make sure the reed relay on the overcurrent card is properly seated.
3. Check for proper bias on the voltage regulator.
4. Check for proper connections of local or remote sensing (or both, if used).
5. Check remote potentiometer connections if used.
6. Check for 150 vac input.
7. Make sure that all terminal screws, screws on capacitor bus, and screws on feed-through capacitors are tight.
8. Replace the voltage regulator.

Overvoltage Unit Adjustment

To adjust an overvoltage unit when no external adjusting device is available:

1. Make sure dc voltage is down.
2. Remove the overvoltage feed wire from the regulator being tested (to prevent feeding dc back to the load).
3. Check that the overvoltage potentiometers on the overvoltage unit are adjusted to their proper firing level (center arm to dc zero). (See logic page YB401.)
4. Connect an external dc supply (or batteries) and a 5000-ohm potentiometer as shown in Figure 118 to provide a variable input to the overvoltage unit under test.
5. Meter the output pin of the overvoltage unit with a voltmeter. (This is the wire that goes to the firing gate on the overvoltage unit SCR.)
6. Gradually raise the test input voltage with the 5000-ohm potentiometer until a dip in voltage is noticed at the output. At this point the input can be read to tell at what level the overvoltage unit fired the SCR.
7. If the SCR does not fire, check the components on the overvoltage unit or readjust the dividers on any supply being tested that has an output of over 6 volts. (See logic page YB291.)

Overvoltage occurs when the supplies are at the following levels. The voltage sensitivity of the overvoltage card is also shown.

Supply	Upper-limit	Overvoltage Card
60Z	67	When divider output is 8.5 volts, the card senses the overvoltage condition.
56XY	67	
48	57	
30	36	
18	22	
-12	-22	
6	8.5	8.5
3	4.5	4.5

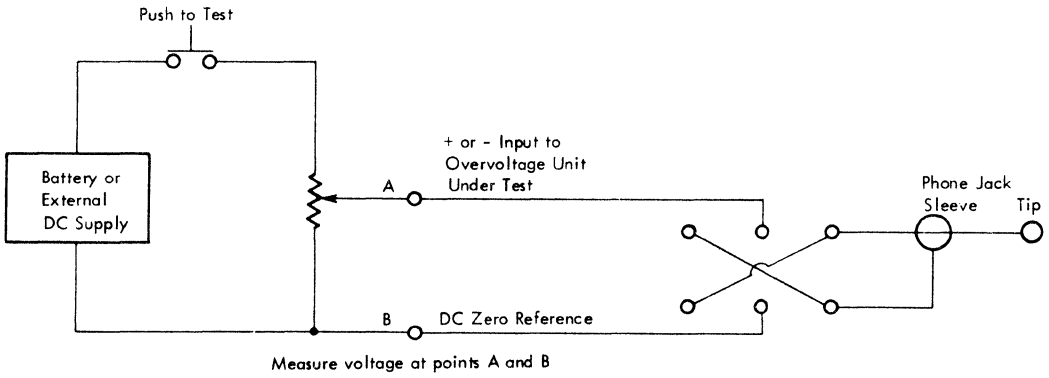


FIGURE 118. OVERVOLTAGE ADJUSTMENT

Low Voltage AC Supplies

With a normal power off, 40 vac and 12.6 vac are present in CPU. If these voltages are to be removed without actuating the emergency power off circuit, CB-1 should be opened.

Power Sequencing Relays

When working with sequencing relays, remember not to mix the 18v, 24v, and 48v coils. They all fit in each other's socket. For instance, a 6 point 18v relay coil will fit in a 6 point 24v socket.

Dual or Multi System Emergency Power Off (EPO)

The EPO bypass switch is used to isolate the multi system EPO capability. The EPO bypass switch should only be activated when a shared control unit, channel, storage device, or CPU must be powered down and removed from the system configuration while the rest of the system is being used.

In a dual or multi system configuration, if any 'emergency pull' EPO switch is activated, power is removed from all units. A complete description of the EPO network for dual or multi systems is available in the Original Equipment Manufacturer's Information manual, IBM System/360 Power Control Interface, GA22-6906.

Dual System Control

The EPO circuits of two systems (sharing a control unit, channel, or storage device) are interlocked with the cable connecting the J47 sockets of each system. To remove any unit from the system configuration:

1. Remove power from both systems.
2. Remove the EPO cables connecting shared units and the PDU which is being isolated (at the units) and replace them with dummy plugs.
3. Remove the EPO cable from socket J47 of the PDU which is not being isolated and replace it with a dummy plug.
4. Power can now be brought up on the remaining system.
5. When repairs are completed, reestablish a common EPO network by removing power from all units, removing the dummy plugs, and reconnecting the EPO cables.

Multi System Control

The EPO circuits of three or more interconnected CPUs are interlocked by connecting the J47 cables from each CPU to the multi-system EPO control box (IBM Part No. 5271793). To drop power and remove any unit from the system configuration:

1. Drop power on the CPU to be isolated.
2. Disconnect all isolated CPU to shared-unit EPO cables. This allows any EPO switch except the one on the isolated CPU to control the EPO interface of the remaining units.
3. Activate the bypass switch on the multi-system EPO control box.
4. Disconnect the EPO cable between the isolated CPU and the multi-systems EPO control box; and insert a dummy plug to bypass the isolated CPU.
5. Deactivate the bypass switch immediately, to restore the interlocked EPO capability to the remainder of the multi-system units.
6. When the isolated CPU is returned to the EPO network, a similar procedure should be used to minimize the time that the bypass switch is active.

This section of the manual concerns itself with the packaging of the 2050 Processing Unit and the location of components and subassemblies within the processing unit. For basic packaging concepts that are common to all models of the System/360, see SLT Packaging, SY23-2800.

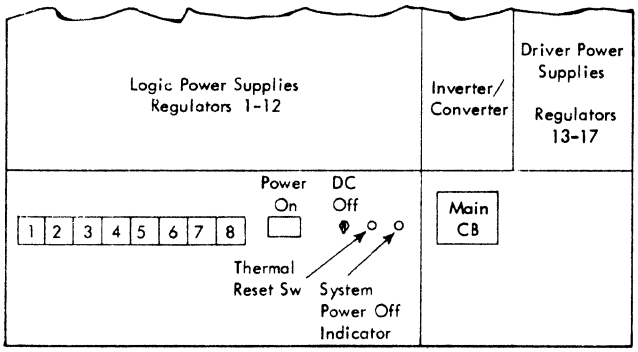
Power Distribution Frame Locations

Figure 119 shows the locations of the circuit breakers and switches in the bottom part of frame 03.

Figure 121 (Part 1) shows the location of all major components in the standard power distribution frame (03). Figure 121 (Part 2) shows the location of major components in power distribution frame 05 which is used for the 512K storage feature only.

Frame and Gate Locations

The frame and gate locations of the 2050 are shown in Figure 120 as are the swing angles of each gate in the processing unit for access to the various areas of the system.



Bottom Section of Power Frame 03

FIGURE 119. PDU CB AND SWITCH LAYOUT

Relay and Contactor Locations

Figure 122 shows the location of all relays and contactors in the processing unit. Note that all of the relays and contactors are accessible from the rear of the power frame. For access to K1-K4, hinged covers must be opened. The remaining relays are mounted in a relay gate in the lower right corner of the power frame.

Circuit Breaker Locations

Figure 123 shows the location of the primary ac circuit breakers in the processing unit. Primary ac circuit breakers 1-8 are mounted on a hinged cover located in the lower center of the drawing on Figure 110. The circuit breakers for each individual service voltage are located with the voltage regulator for that service voltage.

Fuse Locations

Figure 124 shows the location of the fuses in the processing unit. Fuses 1-6 are mounted on a hinged cover located in the right lower center of the drawing in Figure 124.

Voltage Regulator Locations

The voltage regulators that provide the various service voltages for the processing unit are all located in the power frame. Figure 125 shows the location of each voltage regulator, its systems page location, part number, and description.

Figure 126 shows layout and jumpering of the voltage divider assembly.

Overvoltage Assembly Locations

Figure 127 shows locations and adjustments of the overvoltage assembly.

I/O Tailgate Locations

Figure 128 shows locations of the I/O gate terminators; Figure 129 shows locations of the interface connections.

I/O Address Cards

Figures 130-133 show the plugging for address cards for the 1442, 1443, 2841, and 2400 TAU, respectively.

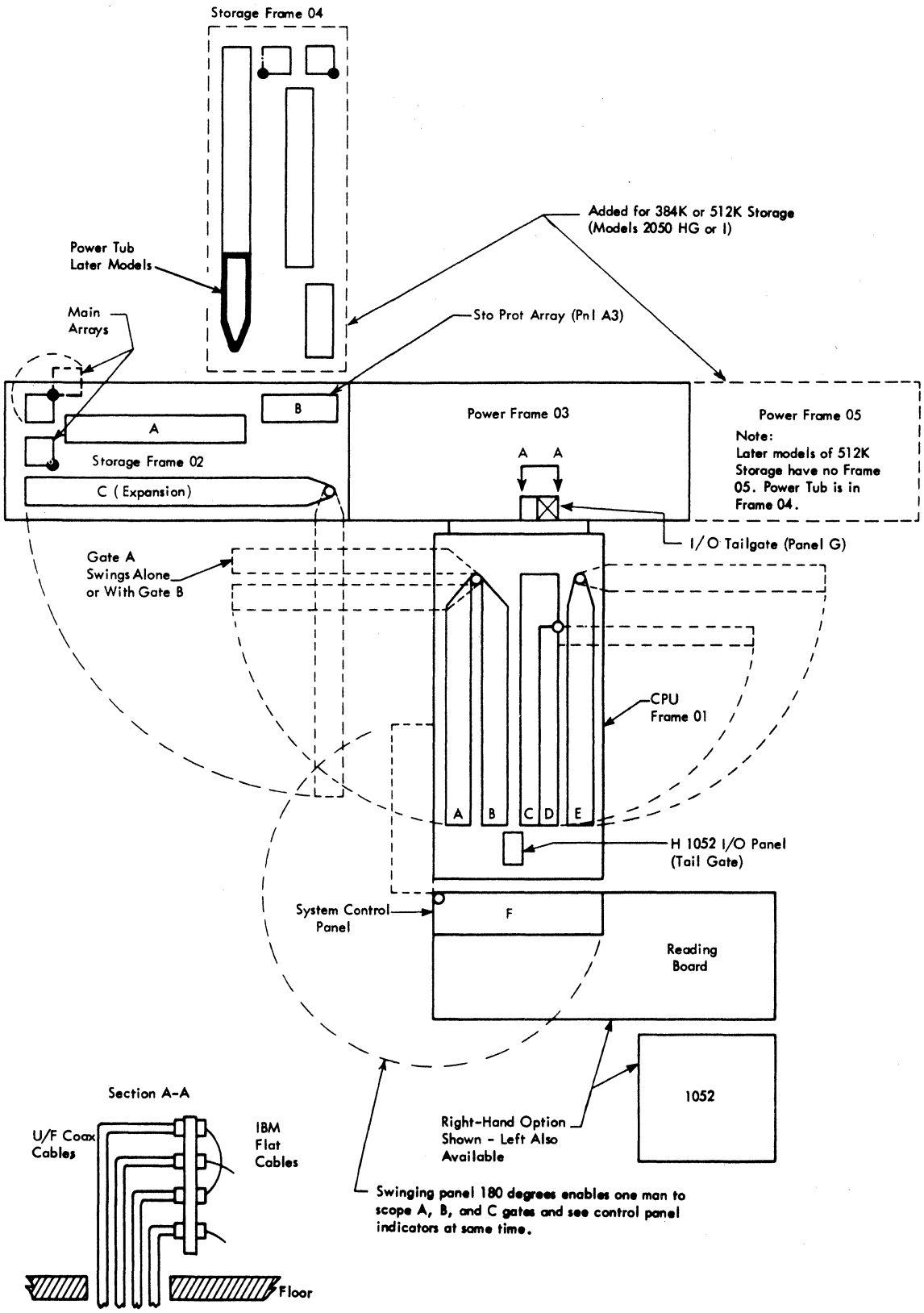


FIGURE 120. MODEL 50 FRAME AND GATE LOCATIONS

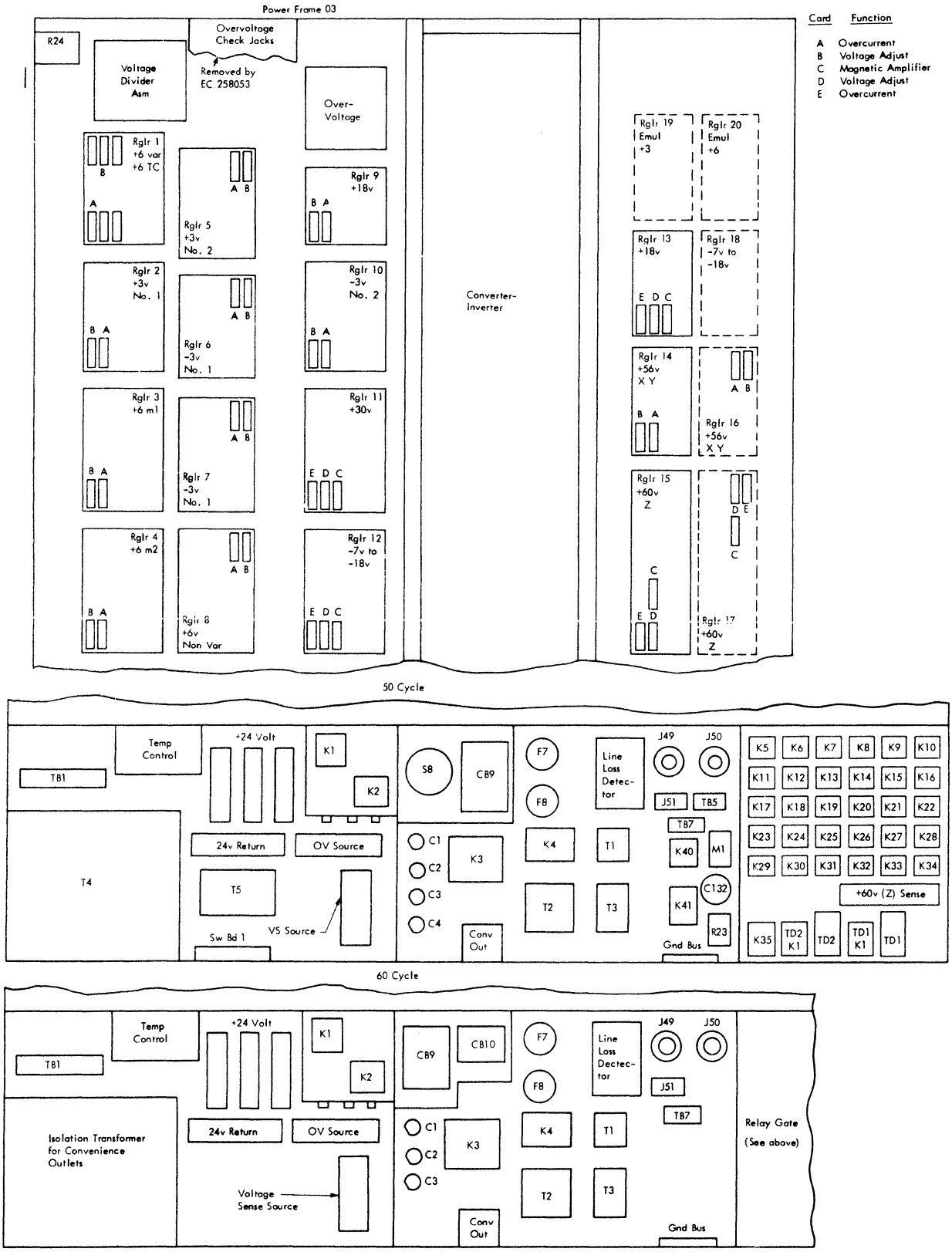


FIGURE 121. POWER DISTRIBUTION FRAMES (PART 1 OF 2)

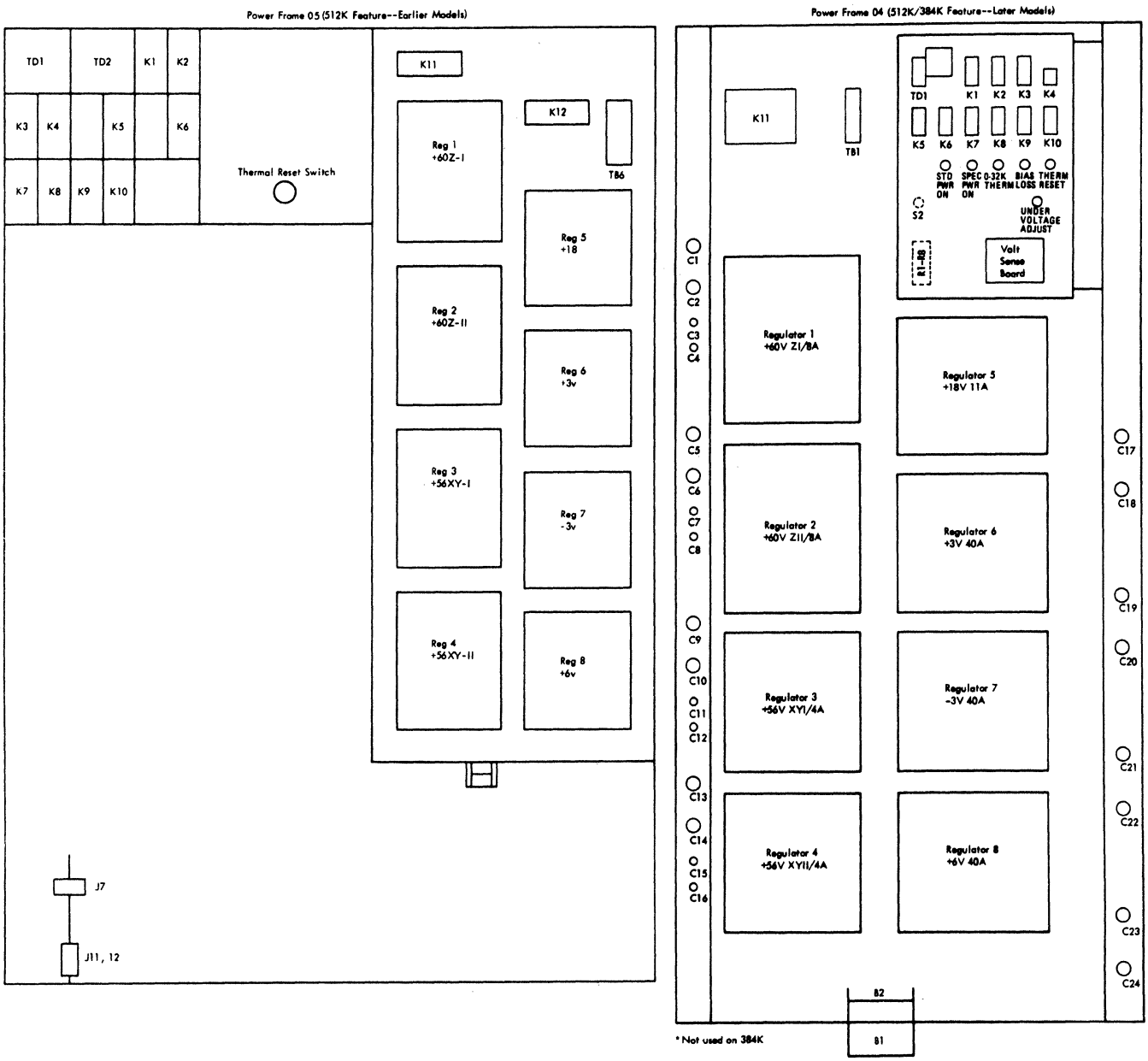


FIGURE 121. POWER DISTRIBUTION FRAMES (PART 2 OF 2)

Contactor No.	System Sheet Number						Part No.	Function
	Coil	Contact Points						
		L1 & T1	L2 & T2	L3 & T3	L4 & T4			
K1	YB221	YB351	YB351	YB341	YB341		5351162	Special Voltages

Relay No.	System Sheet Numbers						Part No.	Function
	Coil	Contact Points						
		1	2	3	4			
K2	YB221	Spare	YB341	YB341	Spare		2128689	Typewriter

Contactor No.	System Sheet Numbers						Part No.	Function
	Coil	Contact Points						
		1A & 1B	2A & 2B	3A & 3B	4A & 4B			
K3	YB221	YB221	YB201	YB201	YB201		5270586	EPO
K4	YB221	YB201 YB221	YB201	YB201	YB201		5364165	STD Voltages

Relay No.	System Sheet Numbers							Part No.	Function
	Coil	Contact Points							
		5 - 6 - 7	8 - 9 - 10	11 - 12 - 13	14 - 15 - 16	17 - 18 - 19	20 - 21 - 22		
K5	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	Power On Adapter
K6	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	Power On Adapter
K7	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	Power On Adapter
K8	YB231	YB271	YB281	YB281	YB281	YB281	YB281	5351156	Power On Adapter
K9	YB231	YB281	YB281	YB281	YB281	YB281	YB281	5351156	Power On Adapter
K10	YB231	YB281	YB281	YB281	YB281	YB281	YB281	5351156	Power On Adapter
K11	YB231	YB281	YB281	YB291	YB291	YB291	YB231	5351156	Power On Adapter
K12	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	EPO Adapter
K13	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	EPO Adapter
K14	YB231	YB271	YB271	YB271	YB271	YB271	YB271	5351156	EPO Adapter
K15	YB231	YB271	YB281	YB281	YB281	YB281	YB281	5351156	EPO Adapter
K16	YB231	YB281	YB281	YB281	YB281	YB281	YB281	5351156	EPO Adapter
K17	YB231	YB281	YB281	YB281	YB281	YB281	YB281	5351156	EPO Adapter
K18	YB231	YB281	YB281	YB291	YB291	YB291	Spare	5351156	EPO Adapter
K19	YB351	YB221	YB221	Spare	Spare			5364161	+18V Sense
K20	YB341	Spare	YB221	Spare	Spare			5213415	-3V Sense
K22	YB261	YB241	YB231	YB331	YB261	YB251	Spare	5364163	Voltage Sense (48V)
K23	YB221	YB221	YB221	Spare	Spare			5318968	Power Check
K24	YB221	YB221	YB221	YB231	Spare			5318968	Sequence
K25	YB231	YB231	YB231	YB231	Spare			5318968	Thermal Reset
K26	YB231	YB221	YB231	Spare	Spare			5318968	Thermal Reset
K27	YB231	YB221	YB231	Spare	Spare			5318968	Thermal Reset
K28	YB231	YB221	YB231	Spare	Spare			5318968	Thermal Reset
K29	YB221	YB221	YB291	YB291	YB351			5318968	EPO
K30	YB221	YB221	YB231	Spare	Spare			5318968	Power On
K31	YB301	YB221	YB231	YB331	Spare			5364161	Logic Sense (+)
K32	YB301	YB221	Spare	Spare	Spare			5364161	Logic Sense (-)
K33	YB301	YB221	Spare	Spare	Spare			5364161	Special Sense
K34	YB301	YB221	YB221	YB221	YB221			5364161	Special Sense
K35	YB301	YB221	YB221					5364164	Undervoltage
K38	YB351	YB291	YB291	YB291	YB291	Spare	Spare	5351156	Bias Sense

Relay No.	System Sheet Numbers						Part No.	Function
	Coil	Contact Points						
		1	2	3	4			
K39	YB221	Spare	YB351	YB351	Spare		2128689	+18V Sequence
K40 *	YB221	YB221	YB211	Spare	Spare		2128689	Blower Seq
K41 *	YB221	YB211	YB211	YB211	YB211		5351162	Blower Seq

* 50 Cycle Only

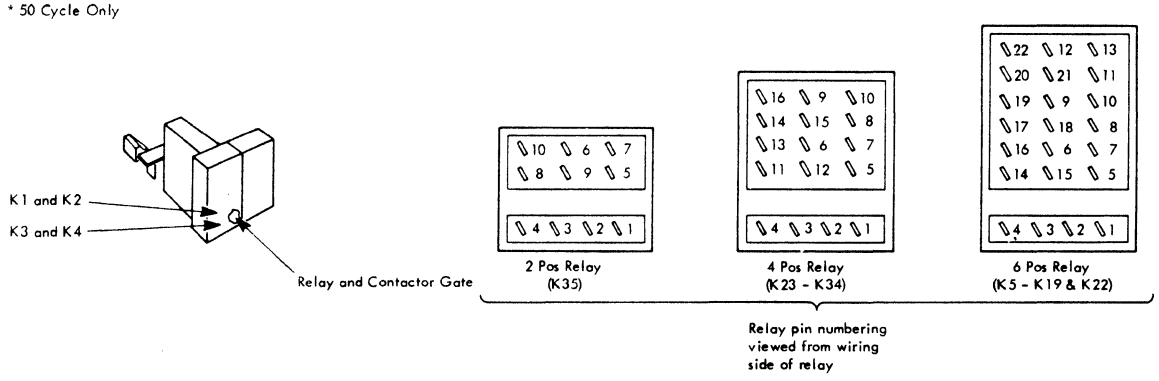


FIGURE 122. RELAY AND CONTACTOR LOCATION CHART

50 Cycle			
SYMBOL	SYSTEM SHEET NO.	PART NO.	DESCRIPTION
CB1	YB201, YB221	5270651	Circuit breaker, 2 pole, 0.4A, 250 vac
CB2	YB201, YB221	5270559	Circuit breaker, 2 pole, 0.65A, 250 vac
CB3, 16	YB211, YB221	725002	Circuit breaker, 2 pole, 5A, 250 vac
CB4,5,6,7,8, 10,14,15	YB211, YB221	5213816	Circuit breaker, 1 pole, 0.9A, 250 vac
CB9	YB201	8026896	Circuit breaker, 3 pole, 25/40A, 440 vac
CB11	YB211, YB221	529016	Circuit breaker, 2 pole, 20A, 240 vac
CB12,13	YB211, YB221	5213818	Circuit breaker, 1 pole, 0.45A, 250 vac

60 Cycle			
SYMBOL	SYSTEM SHEET NO.	PART NO.	DESCRIPTION
CB1	YB 201, YB 211	5270651	Circuit breaker, 2 pole, 0.4A, 250 vac
CB2	YB 201, YB 211	5270559	Circuit breaker, 2 pole, 0.65A, 250 vac
CB3	YB 211	5270566	Circuit breaker, 2 pole, 0.85A, 250 vac
CB4	YB 201, YB 211	5270559	Circuit breaker, 2 pole, 0.65A, 250 vac
CB5	YB 201, YB 211	5270559	Circuit breaker, 2 pole, 0.65A, 250 vac
CB6	YB 201, YB 211	5270559	Circuit breaker, 2 pole, 0.65A, 250 vac
CB7	YB 211	5364273	Circuit breaker, 2 pole, 15A, 250 vac
CB8	YB 201, YB 211	5270651	Circuit breaker, 2 pole, 0.4A, 250 vac

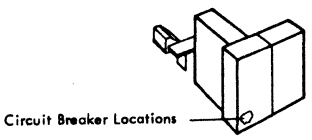


FIGURE 123. CIRCUIT BREAKER LOCATION CHART

SYMBOL	SYSTEM SHEET NO.	PART NO.	DESCRIPTION
F1 and F2	YB201	107669	Fuse, 10A, 250 vac
F3 and F4	YB201	78999	Fuse, 0.5A, 250 vac
F5 and F6	YB201	511063	Fuse, 10A, 250 vac
F7 and F8	YB201	335010	Fuse, 1A, 110 vac (60 Cycle)
F7 and F8	YB201	78999	Fuse, 0.5A, 250 vac (50 Cycle)

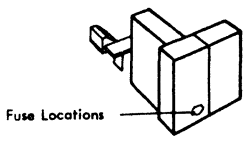
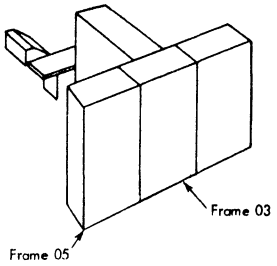


FIGURE 124. FUSE LOCATION CHART

Power Frome 03.			
SYMBOL	SYSTEM SHEET NO.	PART NO.	DESCRIPTION
Reg 1	YB 311	5709310	Regulator, +6v @ 0.5A,1.5A,2.5A
Reg 1	YB 311	5712120	Regulator, +6v @ 2.5A*
Reg 2	YB 321	5261220	Regulator,+3v @ 40A
Reg 3	YB 321,	5261240	Regulator,+6v @ 40A
Reg 4	YB 321,	5261240	Regulator,+6v @ 40A
Reg 5	YB 331	5261220	Regulator,+3v @ 40A
Reg 6	YB 331	5261220	Regulator,+3v @ 40A
Reg 7	YB 331	5261220	Regulator,-3v @ 40A
Reg 8	YB 331	5709300	Regulator,+6v @ 40A (Non-Variable)
Reg 9	YB 341	5261280	Regulator,+48v @ 2A
Reg 10	YB 341	5261220	Regulator,-3v @ 40A
Reg 11	YB 341	5253790	Regulator,+30v @ 5A
Reg 12	YB 341,	5244090	Regulator,-12v @ 11A
Reg 13	YB 351	5253800	Regulator,+18v @ 11A
Reg 14	YB 351,	5261480	Regulator,+56v @ 4A
Reg 15	YB 351,	5253780	Regulator,+60v @ 8A
Reg 16	YB 361	5261480	Regulator,+56v @ 4A
Reg 17	YB 361	5253780	Regulator,+60v @ 8A
Reg 18	YB342 added when an emulator feature is used.	5712160	Regulator,-12v @ 3A
Reg 19		5712010	Regulator,+3v @ 20A
Reg 20		5712030	Regulator,+6v @ 25A
Divider Assembly	———	5364140	(See Figure 126)

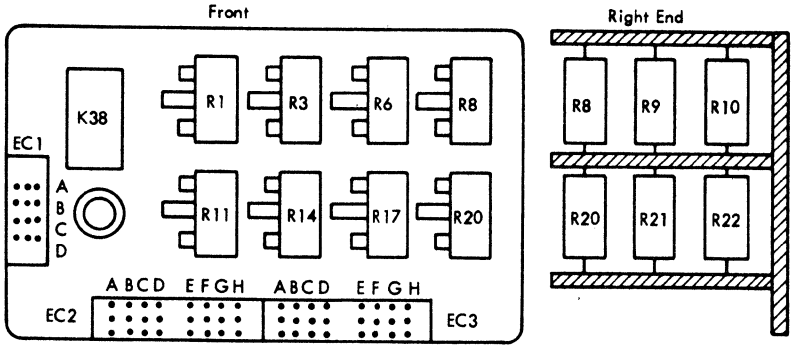


Power Frame 05 (512K Feature)			
Symbol	System Sheet No.	Part No.	Description
Reg 1	YE141	5712180	Regulator, +60v @ 8A**
Reg 2	YE141	5712180	Regulator, +60v @ 8A
Reg 3	YE141	5712480	Regulator, +56v @ 4A**
Reg 4	YE151	5712480	Regulator, +56v @ 4A
Reg 5	YE151	5712100	Regulator, +18v @ 11A
Reg 6	YE161	5712020	Regulator, +3v @ 40A
Reg 7	YE161	5712020	Regulator, -3v @ 40A
Reg 8	YE161	5712140	Regulator, +6v @ 40A

*Used on later machines. Not interchangeable.

**Not used on 384K.

FIGURE 125. VOLTAGE REGULATOR LOCATION CHART



JUMPER CHART

From	To	From	To	From	To	From	To
R1-1	R4-1	R12-2	R11-3	R14-2	K38-10	EC2-g	R8-2
R3-1	R6-1	R11-1	R13-1	R19-2	K38-11	EC2-h	R10-2
R6-1	R8-1	R15-2	R14-3	R17-2	K38-13	EC3-a	K38-6
R8-1	R12-1	R14-1	R16-1	R22-2	K38-14	EC3-b	R13-2
R12-1	R15-1	R18-2	R17-3	R20-2	K38-16	EC3-c	K38-9
R15-1	R18-1	R17-1	R19-1	R13-2	K38-5	EC3-d	R16-2
R18-1	R21-1	R21-2	R20-3	EC2-2	R1-2	EC3-e	K38-12
R1-3	R2-2	R20-1	R22-1	EC2-b	R2-1	EC3-f	R19-2
R4-2	R3-3	R11-2	K38-7	EC2-c	R3-2	EC3-g	K38-15
R6-3	R7-2	R16-2	K38-8	EC2-d	R5-2	EC3-h	R22-2
R8-3	R9-2	K38-1	EC1-6	EC2-e	R6-2	EC1-c	R12-1
R9-1	R10-1	K38-4	EC1-d	EC2-f	R7-1	R3-1	R5-1

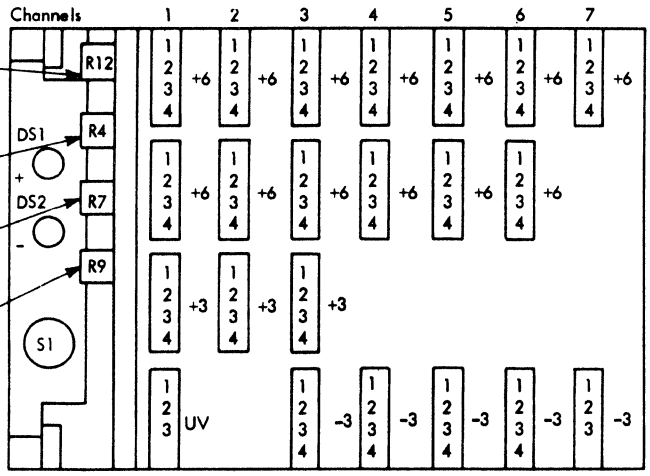
FIGURE 126. VOLTAGE DIVIDER ASSEMBLY

+6 undervoltage setting should be adjusted so that relay is de-energized when the +6 volt supply is at 5.2vdc. R12 center arm should be set for approximately 5.3vdc from center arm of potentiometer to common as measured with a 3 percent 20K voltmeter.

For +3 volt overvoltage setting, adjust R4 for overvoltage trip setting on +3 volt supplies. R4 center arm should be set for +4.5vdc from center arm of potentiometer to common as measured with a 3 percent 20K voltmeter.

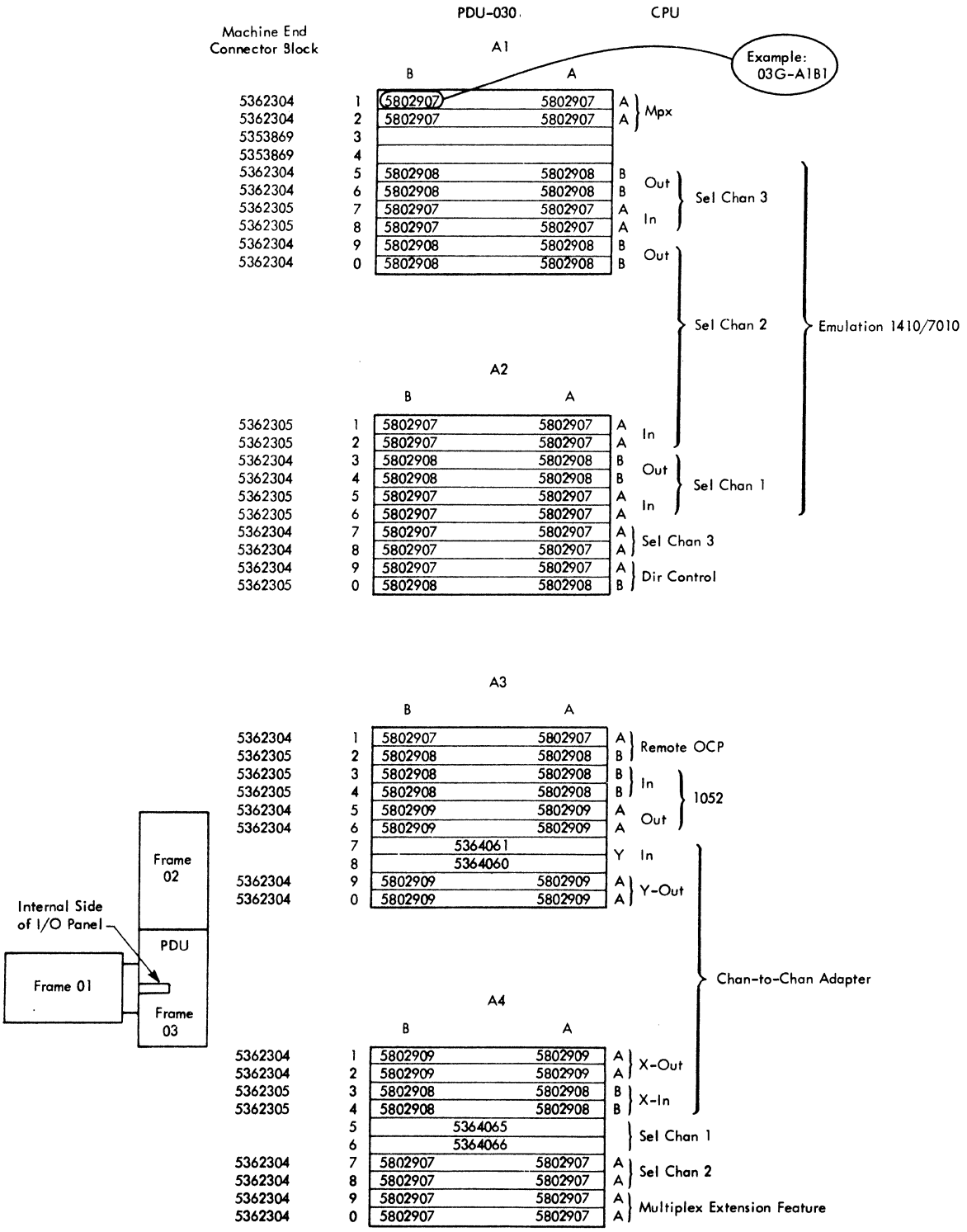
For -3 volt overvoltage setting, adjust R7 for overvoltage trip setting on -3 volt supplies. R7 center arm should be set for -4.5vdc from center arm of potentiometer to common as measured with a 3 percent 20K voltmeter.

For +6 volt overvoltage setting, adjust R9 for overvoltage trip setting on +6 volt supplies. R9 center arm should be set for +9.5vdc from center arm of potentiometer to common as measured with a 3 percent 20K voltmeter.



Note: DS1 and DS2 removed by EC 259862

FIGURE 127. OVERVOLTAGE ASSEMBLY



NOTES:

1. In places where the use of a feature results in unused lower cable connector positions, use 5353869 as required to fill out column.
2. 5362304 is style A (light gray) out
   5362305 is style B (dark gray) in

FIGURE 128. I/O GATE TERMINATORS

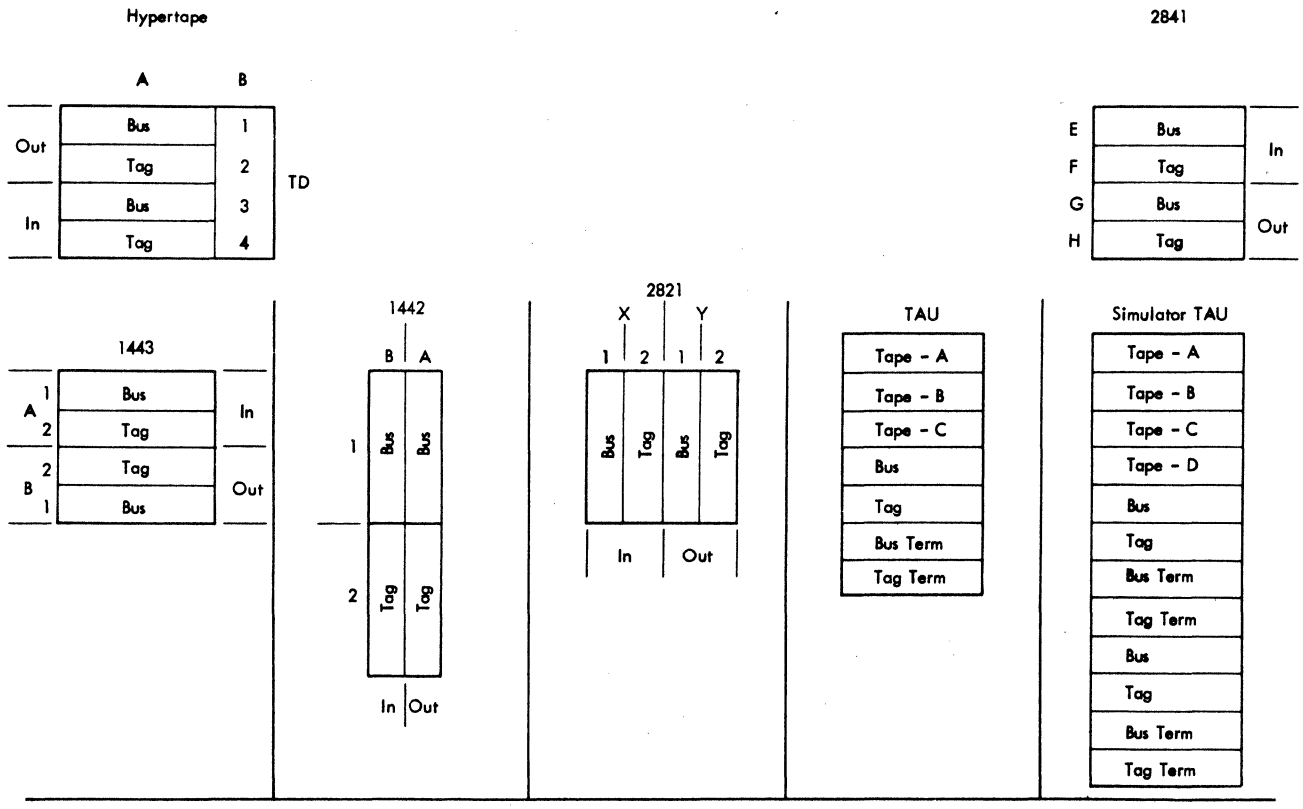


FIGURE 129. I/O INTERFACE CONNECTIONS

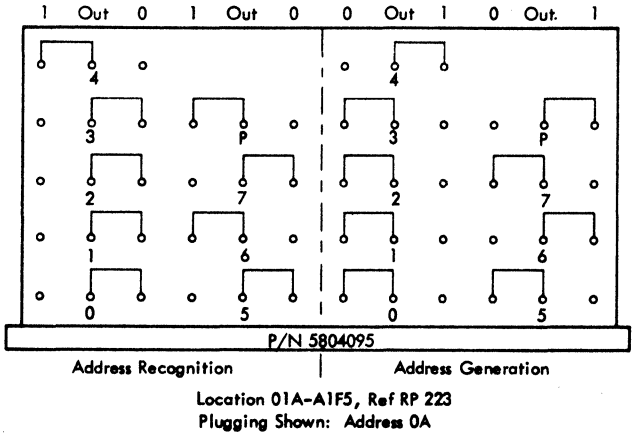


FIGURE 130. 1442 ADDRESS CARD LOCATIONS AND PLUGGING

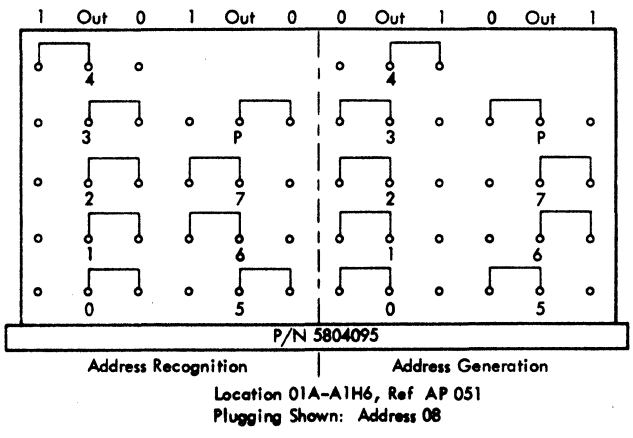


FIGURE 131. 1443 ADDRESS CARD LOCATIONS AND PLUGGING

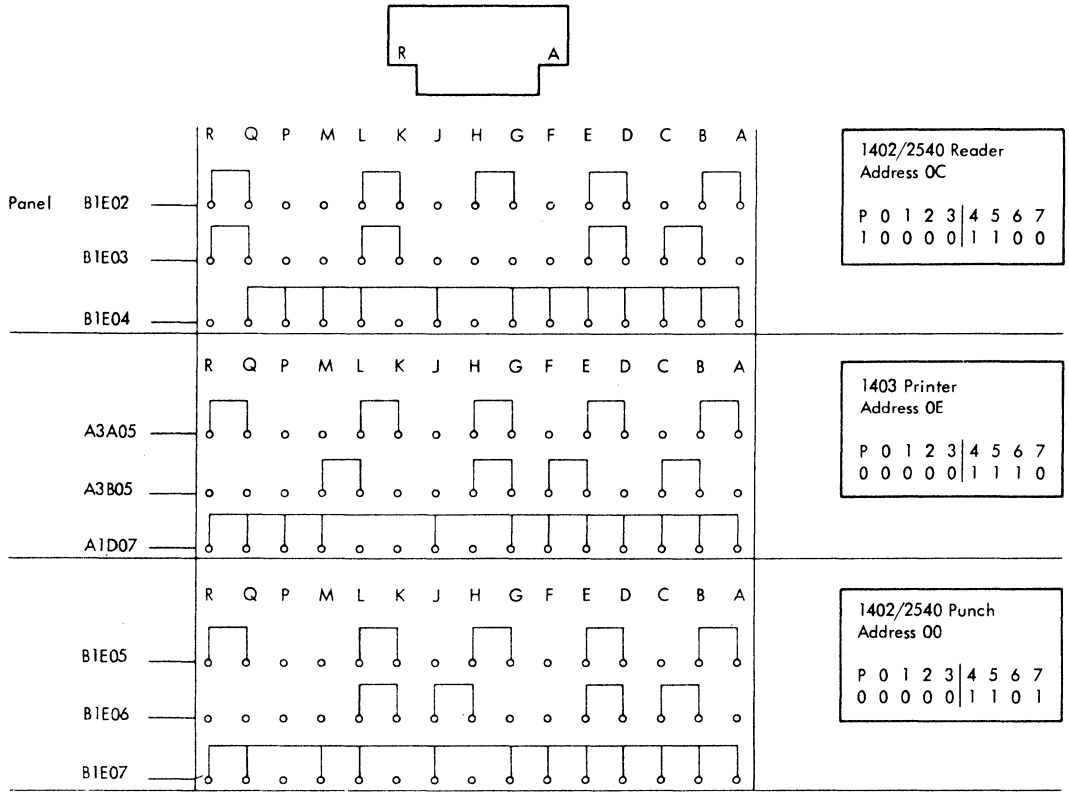


FIGURE 132. 2821 ADDRESS CARD LOCATIONS AND PLUGGING

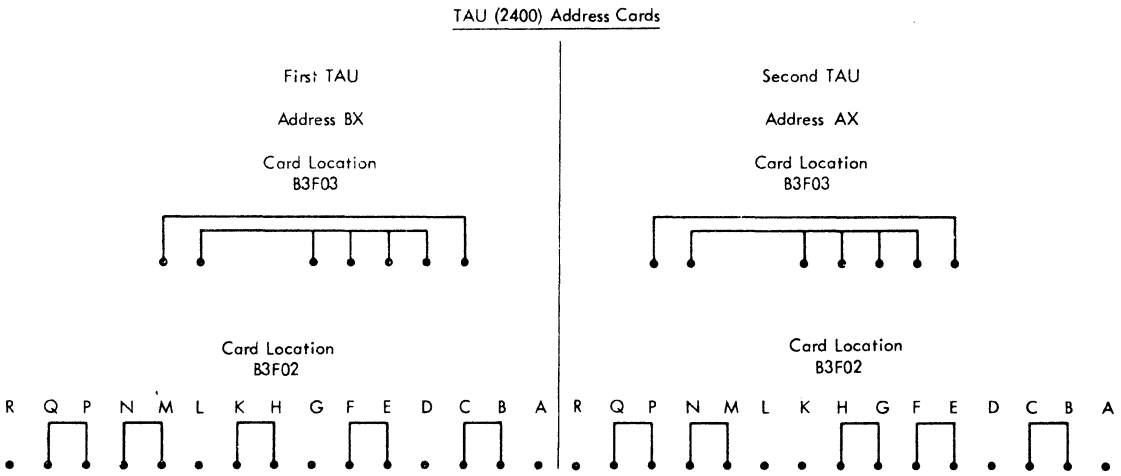


FIGURE 133. TAU (2400) ADDRESS CARDS LOCATIONS AND PLUGGING

APPENDIX A - SYSTEM CHARACTERISTICS

PHYSICAL DATA

- 2050 Processing Unit has three frames: CPU, Main Storage, and Power.
- Power frame connects the CPU and Main Storage frames.
- System control panel is mounted on the CPU frame.

The 2050 Processing Unit (Figure 134) consists of the CPU frame, the main storage frame, and the power frame.

The CPU frame contains the CPU logic, the channels, the capacitor read only storage, and the local storage. The system control panel is mounted on one end of this frame. Within the CPU frame are three hinged gates (A, B, and E on Figure 135). Each hinged gate holds twenty printed circuit boards. One fixed gate (C) with a hinged section (D) contains the capacitor read only storage (ROS) and twelve printed circuit boards.

The main storage frame houses the main storage modules, their associated logic, and large capacity

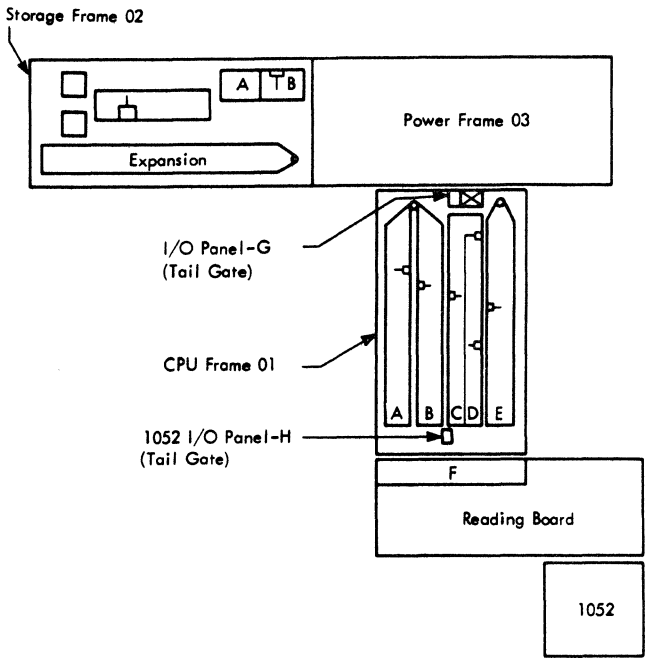


FIGURE 135. IBM 2050 FRAME AND GATE LAYOUT

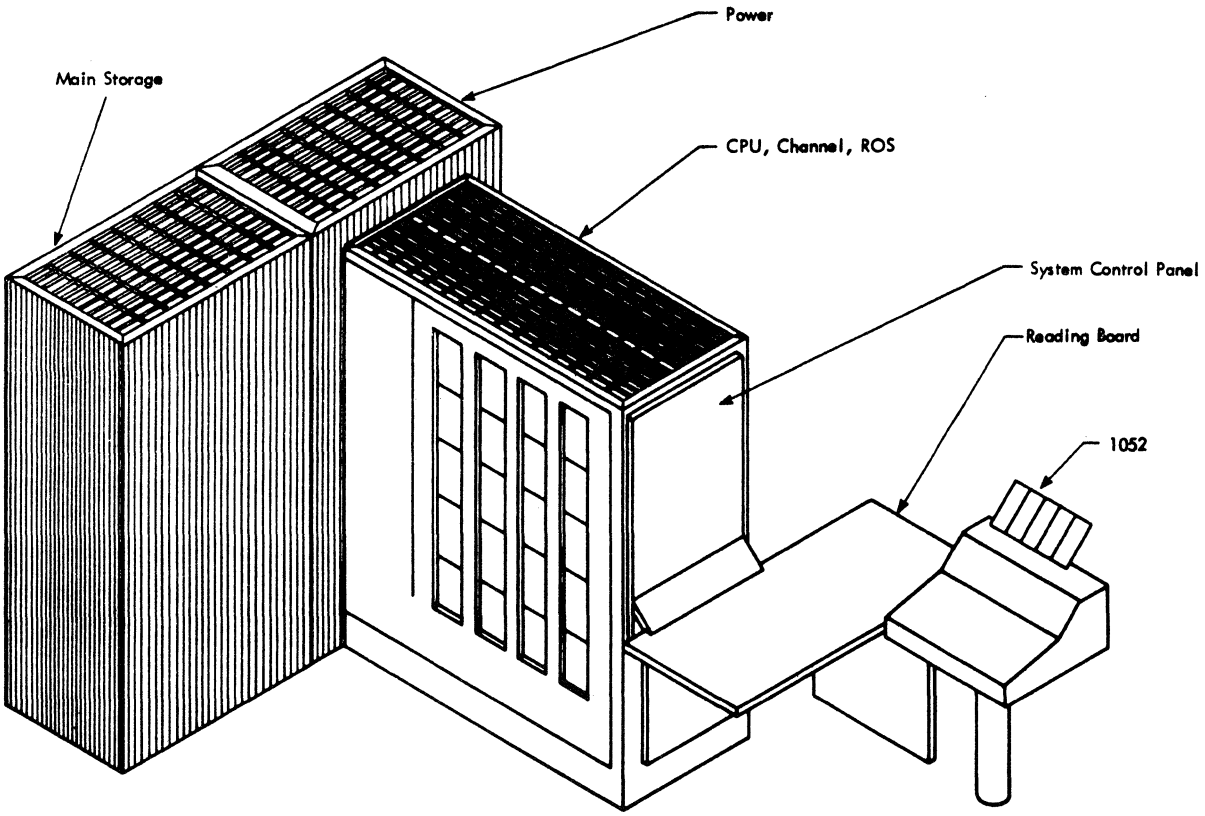


FIGURE 134. IBM 2050 PROCESSING UNIT

storage connections. The storage protection buffer is also located in this frame. One main storage module is used for all standard storage sizes up to and including 128K bytes. Storage sizes greater than 128K bytes use two main storage modules. The frame capacity is two main storage modules, eight printed circuit boards, and a hinged gate for expansion.

The power frame contains the power converter-inverter, the power sequencing and control circuitry, and all regulators. The power frame also serves as a cable path between the CPU and storage frames and contains the Input/Output (I/O) panel for external cables.

Frame Specifications

The following chart gives the physical specifications for the three frames that make up the 2050 Processing Unit.

	CPU	Main Storage	Power
Dimensions (inches)			
Length	62.5	60.0	60.0
Width	29.5	24.0	24.0
Height	70.0	72.5	72.5
Floor Area (sq ft)	12.8	10.0	10.0
Weight (pounds)	2000	1100	1500

Cabling

The external cable connectors for the 2050 are located in the power and main storage frames. A raised floor facilitates the routing of external cables but is not an absolute necessity. Cables connecting the channels to external devices pass through the bottom of the power frame to reach the I/O connector panel. Cables connecting the 2050 to shared or large capacity storage pass through the bottom of the main storage frame to reach the connector panel.

A maximum of twelve external cables may be attached to the I/O panel in the power frame: two for each of five channels (one multiplexor, three selector, one high speed) and two for an external operator's control panel.

POWER REQUIREMENTS

- Three input voltage options.
- Current requirements depend on storage size.

The 2050 Processing Unit is manufactured for one of the following input voltage options:

Option 1	Option 2	Option 3
60 cps ± 1 cps 3 phase-4 wire delta 208/230 vac RMS ± 10%	50 cps ± 1 cps 3 phase-4 wire delta 195/220/235 vac RMS ± 10%	50 cps ± 1 cps 3 phase-5 wire "Y" 380/425 vac RMS ± 10%

Current requirements and heat dissipation are dependent on storage size:

	64K	128K	256K
Power Input (kva)	9.0	9.0	10.6
Service Rating (amperes)	30	30	30
Heat Dissipation (BTU/hr)	14,900	14,900	18,700

APPENDIX B - SYSTEM CONTROL PANEL

- System control panel provides operator, intervention, and maintenance controls.

The system control panel (Figure 136) contains the switches and indicators required for system operation. Twelve panel sections contain operator, intervention, and maintenance controls.

Panel sections C and N provide basic operational control. Panel sections G, L, and M provide intervention and maintenance controls. The remaining panels provide maintenance controls.

CONTROLS AND INDICATORS

- Five types of control switches.
- Switchable indicators on panel section G.
- Functional grouping of switches and indicators.

Each panel section contains switches and/or indicators grouped by function.
Five types of switches are used:

1. Rotary Select--Position defines function.
2. Roller Select--Position selects status indicator data.
3. Data Key--Lever switch active in the down position.
4. Control Key--Lever switch selects indicated function.
5. Pushbutton--Active when pressed.

Panel sections A, G, L, and M have vertically-placed letters and/or horizontally-placed numbers to aid in locating a particular switch or indicator.

Section A - Power Display

The power display panel section contains power check indicators, marginal check controls, a dc off switch and a voltmeter.

DC Off Switch

This keylever switch removes dc power from the CPU, storage, and channels. Attached adapters are not affected except for the 1052 adapter which is packaged in the CPU.

DC Off Indicator

This indicator is on when dc power has been removed from the CPU, storage, and channels.

Frame Thermal

Three indicators monitor frame temperatures in the system. The opening of any thermal switch in the CPU, storage, or power frame causes the removal of dc power from the CPU, storage, and channels. The frame in fault is indicated by a light (CPU, STOR, or PDU) which remains on when power drops.

Open CB

This indicator is turned on if any circuit breaker in the power frame opens.

Power Check

The detection of an overcurrent condition in any dc regulator turns on the power check indicator. The detection circuitry is interlocked with the power sequence controls to remove the voltages or prevent their application. This indicator remains on when power drops.

Meter

The panel meter allows direct monitoring of any system voltage under control of the marginal voltage select and monitor voltage select rotary switches. Two scales are provided: the upper is numbered 2 through 10, with 6 at center scale; the lower is numbered 1 through 5, with 3 at center scale. Scale reading is either times 1 or times 10. Electrical accuracy at center scale is ± 0.3 percent of full-scale deflection and at end scale it is ± 0.6 percent of full-scale deflection.

Marginal Voltage Select

This rotary switch selects the marginal voltage to be monitored on the meter. The following voltages may be selected:

+6 TC (Temperature Compensated - Local Storage)
+6 VAR (Variable - Local Storage)
+6 M1 (Variable - Channel)
+6 M2 (Variable - CPU)
-12 ROS #1
-12 ROS #2
+56 XY 1 (Main Storage XY Drivers)
+60 Z 1 (Main Storage Z Drivers)
+56 XY 2 (Main Storage XY Drivers)
+60 Z 2 (Main Storage Z Drivers)

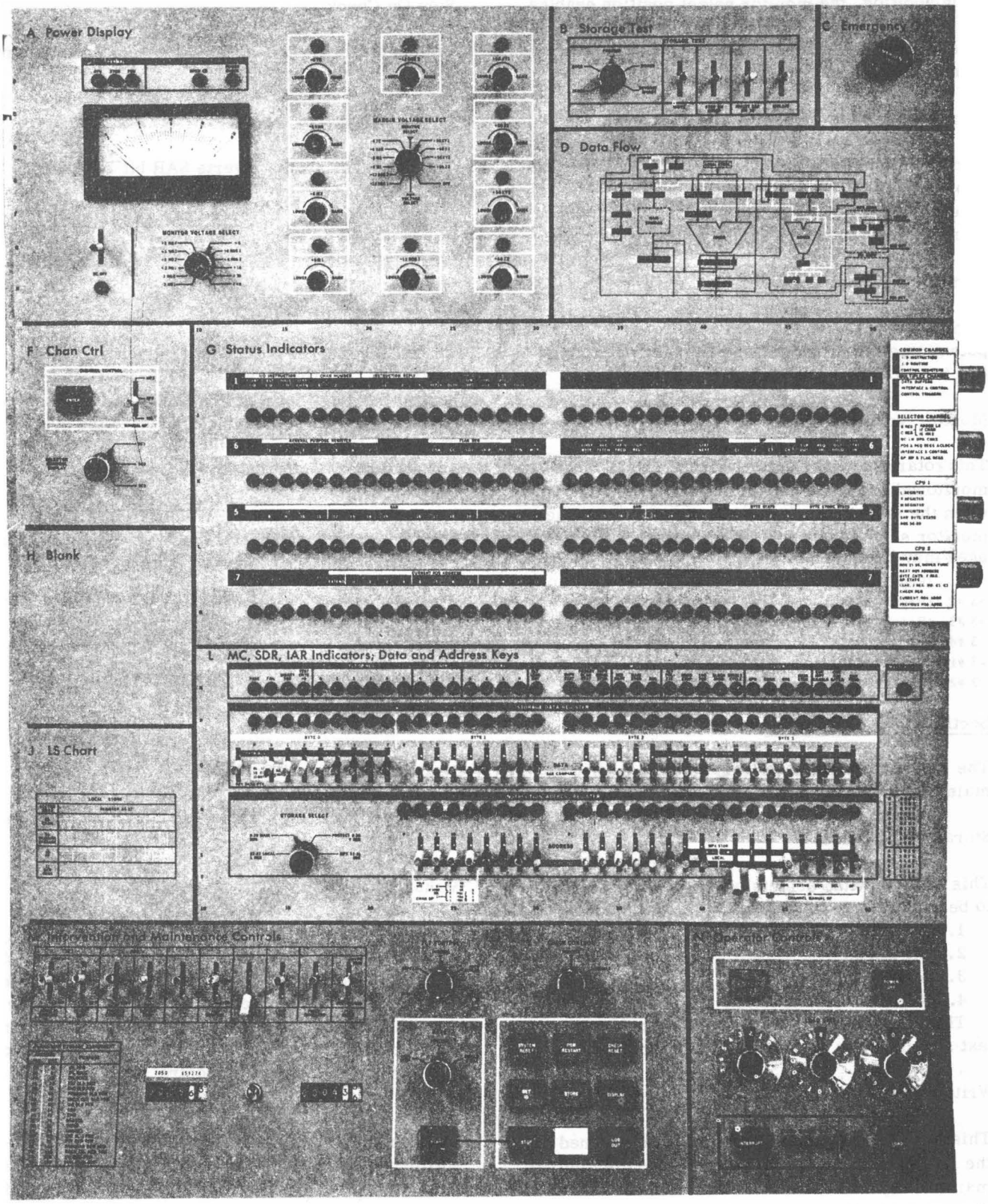


FIGURE 136. SYSTEM CONTROL PANEL

In addition, the monitor select position enables the monitor voltage select switch and the aux voltage select position enables the aux storage select switch when 384K or 512K storage is installed.

Marginal Voltage Control

Ten potentiometers (one for each marginal voltage) provide marginal voltage control, allowing the voltage to be varied around its nominal value. More than one voltage can be varied at the same time.

Marginal Voltage Indicators

Ten indicators, one for each of the above-mentioned potentiometers, indicate when a marginal voltage has been varied from its nominal value.

Monitor Voltage Select

This rotary switch selects a non-marginal voltage to be monitored by the meter. The switch is active only when the marginal voltage select switch is in the monitor select position. The following system voltages may be selected:

+3 #1 (Regulator 6)	+6 (Regulator 8)
+3 #2 (Regulator 5)	+6 ROS 1 (Regulator 1C)
+3 #3 (Regulator 2)	+6 ROS 2 (Emulator)
+3 #4	+18 (Regulator 13)
-3 #1 (Regulator 10)	+30 (Regulator 11)
-3 #2 (Regulator 7)	+48 (Regulator 9)

Section B - Storage Test

The storage test panel section permits testing the main storage array.

Storage Test Select

This rotary switch selects one of the four test patterns to be applied to main storage. The four patterns are:

1. All Ones
2. All Zeros
3. Worst Pattern
4. Reverse Worst Pattern

The test light (Section N) is on when the storage test select switch is off the Process position.

Write

This keylever switch causes the pattern defined by the storage test select switch to be written into all main storage locations when start is pressed. Storage protection is ignored. The test is terminated by a stop on check condition or by a system reset.

Stop On Check

This keylever switch causes a detected storage error to terminate the storage test.

Invert SAR Bit 16

This keylever switch inverts SAR bit 16, thereby interchanging the two 32K halves of a 64K section of main storage. With storage reversed in this manner, words 0-8K are referenced as 8-16K and vice versa. Words 16-24K are referenced as 24-32K, and so on.

Section C - Emergency Off

The emergency off pull switch is located on panel section C. Pulling this switch turns off all power beyond the entry terminal on every unit which is part of the system or can be switched on to the system. This switch therefore controls the system proper and all control units and I/O devices that are switched offline.

The emergency off switch latches in the "out" position. Mechanical intervention by the customer engineer is required to restore the switch to the "in" position.

Section D

Panel section D shows major data paths in CPU, channels, and storage elements.

Section F - Channel Control

This panel section provides three channel maintenance controls.

Manual Operation

This keylever switch provides a means of manually disconnecting the channels from the CPU and attached adapters, and coupling them to the data and address keys for control purposes. In manual channel operation, the address keys are used to control the channel interfaces (CPU and I/O), and the data keys provide data for use in the various control sequences. The manual sequencing of any channel operation is possible.

When this switch is in the MPX position the multiplexor channel is selected for manual testing; when it is in the SEL position, the selector channels respond.

Address and Data Key Assignments

Address Key	Function
8	Hold DTC Switch: This switch is not controlled by either the manual switch or the enter pushbutton; it is active when the rate switch is in single cycle. The hold DTC switch causes the DTC line to channel to be held active after it has once been issued by ROS. To reset the hold on the DTC, raise the switch.
9-11	IF stop, and Stop Select Switch: The 'IF stop' switch (key 9) determines which clock is to be controlled. The stop select switches (keys 10-11) control the sequencing of the A-clock to the tag gate generator. These switches are gated to the interface register (making them active to stop the clock at a certain position) by the enter pushbutton. The manual switch is not a gating condition. The stop select keys affect all selector channels.

Keys	Stop on A-Clock
000	(No stop)
001	During clock A0
011	During clock A1
010	During clock step

Keys	Stop on Tag gate generator
100	(No stop)
101	During ITD1 and not ITD2
111	During ITD2 and not ITD3
110	During ITD1 and not 'In' tag

26	Request In
27	Address In
28	Status In
29	Service In
30	Select In
31	Operational In

Data Key	Data
0-7, Parity	Byte
0-31, Parity	Word

To visually examine the contents of the adder latch, (the B or C register of an idle selector channel) the A-clock should not be stopped with the keys.

Stopping the sequence at any point or advancing the sequence from one stop to another stop is permissible.

A-Clock Stop: For proper single-step operation, the A-clock sequence should be completed before the start pushbutton is pressed for the next cycle. To examine unit selection, stop the clock before the third DTC in CCW2 routine is issued to the channel, and sequence the A-clock with the keys from that point through CC step 1 (clock A1 of unit select). If operating with a real unit, use tag gate sequencing from that point to the end of unit select.

Tag Gate Generator Stop: When working with a real I/O unit (manual op off) the check control switch should be in the channel stop position to delay transmission of the out tag. Stopping the sequences in the data handling portions of the record may cause overrun conditions in an unbuffered unit.

Enter

This pushbutton switch causes address and data key information to be gated into the channels for manual operation. The switch is active only in the manual mode.

Selector Channel Display

This rotary switch selects one of the selector channels for display in the status indicators. The particular status word displayed is determined by the position of the selector channel status roller select switch.

Section G and K - Status Indicators

The status indicators on panel section G provide a display of CPU and channel status. The 144 indicators are arranged in four rows, 36 to a row. Each row is separated in the center, with positions 0-17 in the left half and positions 18-35 in the right half.

Eight status words can be displayed in each row of indicators. The desired word is selected with an eight-position roller select switch. The switch also positions a roller format to identify the information displayed.

Panel section K is mounted to the right of the status indicators to identify each row and the general content of each word position.

The roller positions are explained in:

Figure*	Roller Position	Content
		Common Channel
137	1/1	I/O instructions
138	1/2	I/O routines
139	1/3	Control register
		Multiplex Channel
140	1/4	Data buffers
141	1/5	Interface and control
142	1/6	Control triggers
143	1/7	(Special features)
144	1/8	(Special features)
		Selector Channel
145	2/1	B-register
146	2/2	C-register
147	2/3	BC LW operations or checks
148	2/4	Position and request registers A-Clock
149	2/5	Interface and control
150	2/6	GP MP and flag registers
151	2/7	(Special features)
152	2/8	(Special features)

* Located at end of this Appendix

Figure *	Roller Position	Content
		CPU1
153	3/1	L-register
154	3/2	M-register
155	3/3	M-register
156	3/4	H-register
157	3/5	SAR byte stats
158	3/6	ROS 56-89
159	3/7	(Special feature)
160	3/8	(Special feature)
		CPU2
161	4/1	ROS 0-30
162	4/2	ROS 31-55 mover function
163	4/3	Next ROS address
164	4/4	Byte ctr F-register GP stats
165	4/5	LSAR J-register MD G1 G2
166	4/6	Check register
167	4/7	Current ROS address
168	4/8	Previous ROS address

Selector Channel Roller Analysis

The following information will aid in interpreting the indicators on the selector channel roller and logout.

Word 3

Bits 0-5 Byte Counter: Phases A and B should have correct parity. Phase A normally equals Phase B; if unequal:

1. On write, 'svc in' is still active.
2. The stop lines to the tag gate generator are active from the IF register.
3. Overrun condition was detected in CCW2, in which case BC(B) equals ER. Chain check is active.
4. During end update, ER transferred to BC(B).
5. CDA chaining occurs before the first 'svc in' of the new record arrives and before the arrival of new BC information. BC(B) equals ER, BC(A) equals 00 and 'if CDA first byte LA' is active.
6. The stop channel line is active, BC(A) is 1 less than BC(B).

The byte counter incrementing is not changed in a read backward operation; however, its output gating is inverted.

Bits 6-7 End Register: The end register should contain the count modification information obtained in the CCW2 routine, except in the case where it is reset to 00 on detection of a program-type check in a write operation. The end register should have no effect on the channel, unless both EOR1 and L1W latches are active. At the end of an operation if there are no channel check indications, BC(A, B) equals ER.

Bits 8-10 Last Word Register:

1. Conditions: Read op and read ready are active, CL step is not active.
   a. If EOR1 is active, the lowest active LW latch (L3W is high, L1W is low) indicates the additional number of buffers needed for collection of data from the interface to complete the block of data
   b. If EOR2 is active, the lowest active LW latch indicates the additional number of read store routines needed to completely store the block of data.
2. Conditions: Write op and finish (fin) latches are active, A clock is not active.
   a. If EOR1 is active, the lowest active LW latch indicates the number of buffers that contain the old record.

For EOR2 with read op or EOR1 with write op, if the number of full latches (C, B, LS) exceeds the lowest active LW latch, CDA chaining is implied, with part of the new record block resting in the channel buffers.

At the end of a write operation, L2W and L3W should never be active.

For any operation, if L1W is not active, the record has not reached the end of count as specified by the CCW.

Bits 11-14 End of Record:

1. EOR Cnt Intlk: Interface controls are about to be informed that the end of the block of data approaches. Routine request circuits wait for a reaction from the interface controls in a read op only.
2. EOR1: The interface clocks the LW registers.
3. EOR2: Routine request circuits clock the LW register in read op.
4. Read Intlk La: To inform the routine controls that the interface controls have completed their use of the LW register.

This table shows the invalid combinations of the end of record latches:

Bit Position				Other Conditions
11	12	13	14	
Count Intlk	EOR 1	EOR 2	Read Intlk	
1	-	-	1	Not Svc In
1	-	1	-	
-	1	1	-	
-	-	1	-	Write Op
-	-	-	1	Write Op
-	-	1	-	L3W

If EOR1 and 'cnt intlk' are both active when 'svc in' is not active, a write op, is in progress and a complete short record has just been fetched.

* Located at end of this Appendix

Bit 15 BAC Latch: If the B almost changed latch is active:

1. For read operations, the preceding or present transfer is from the B register.
2. For write operations; the present storage data transfer is to the B register and the channel has not finished with the data transfer.

'BAC' and 'LS full' should never be active at the same time.

Bit 16 LS Enable: A priority 1 request should not be present if LS enable is active. LS enable, LS full, and B full should not be active concurrently.

1. For read operations, if LS enable latch is active, the contents of the B register will be or are being transferred to the buffer in LS. If LS full is also active, the LS DTC is active.
2. For write operations, if the LS enable latch is active, the buffer in LS is available for new data from main storage. If LS full is also active, the data has not been transfered from LS to the B register.

Bits 17-19 Register Full:

Operation	BAC Bit 15	ENA Bit 16	Full Bit 17	Full Bit 18	Description
---	0	0	0	1	Data in B register.
---	0	0	1	-	Data in LS.
Read	0	1	0	0	Illegal.
"	0	1	0	1	LS routine in progress; LS DTC has not arrived;
"	0	1	1	0	LS DTC present.
"	0	1	1	1	Illegal.
"	1	0	0	0	Previous routine: B to main storage.
"	1	0	0	1	B being or just transferred to main storage.
"	1	1	0	0	Illegal.
"	1	1	0	1	B to main storage. C full active, one cycle to end read store routine.
---	1	-	1	-	Illegal.
Write	0	1	0	0	Last fetch transferred to B via LS.
"	0	1	0	1	Data in B after transfer via LS.
"	0	1	1	0	LS routine in progress, LS DTC has not arrived.
"	0	1	1	1	Illegal.
"	1	0	0	0	Write fetch routine in progress, data destined for B register.
"	1	0	0	1	Write fetch step 2, clock A0 or A1.
"	1	1	0	0	Illegal.

Bits 20-26 Read, Write Latches: Any active indications in both the read and write groups at any one time are signs of malfunction.

Op	Rdy	IF	Description
Read Bits 21	Read Bits 22	Read Bits 23	
Write Bits 24	Write Bits 25	Write Bits 26	
0	0	0	Not performing that operation.
0	0	1	Illegal.
0	1	0	Illegal.
0	1	1	Illegal.
1	0	0	Channel in CCW1 or CCW2 routine not CDA chaining.
1	0	1	Channel working in routines other than above.
1	1	0	Channel performing unit selection.
1	1	1	Channel waiting to perform any of the above.

Bits 27-35 Channel Checks: 'Sim check' signals the channel to terminate the operation. Unit status will not be available for the CSW. Three conditions set sim check:

1. Channel discovered a check condition before the unit could be selected to perform the operation.
2. A halt I/O terminated the current operation.
3. An IF control check occured to disconnect the unit by a selective reset.

Word 4

Bits 0-8 Position Register: Only one position in this field should be active at any one time. If none of the positions is active, the channel is in one of two states:

1. Idle (instruction scan latch is active).
2. Unit selection routine is finishing or has just finished; rd rdy or wr rdy latch is active.

The CCW1 type position is used for:

1. Start I/O routine.
2. CCW1 routine.
3. TIC routine.

If the end up position is active and the PCI req is active, the CPU may be masking interrupts for this channel.

Bits 9-12 Cycle Counter Phase A: Only one position in this field may be active at any one time. If no bits are active, the channel has either:

1. Completed unit selection (MP C2, C3, C4 latches are all active).
2. Completed CCW2 routine previously.

If the A-clock A and B latches are not active, the number associated with the active light indicates the number of clock sequences (A0, A1, CL STEP equal one sequence) that have occurred and are associated with the routine in the position register.

Clock step pulses advance the cycle counter if clock step is active; the channel gating is associated with the cycle counter step previous to the one that is active at the time.

Pos 4 Bit 9	Pos 5 Bits 4-5	Pos 5 Bit 0	Pos 6 Bit 16	Remarks
Cycle Counter Step 0	A-clock C, D latch	Position Register Transfer	Finish Latch	
1	0	1	1	Request register equals position register; first clock sequence in routine has not occurred.
-	0	0	1	Last clock sequence in routine has occurred (unit select and CCW2 are exceptions). New request register can transfer to position register.
-	-	0	0	The routine in the position register is being processed and is not associated with the routine in the request register.
-	0	1	0	Illegal.

Bits 13-15 Clock A0, A1, Clock Step: Only one light should be active at any one time. If one position is active the clock is:

1. Stopped by the setting of the interface register.
2. Stopped because of an error detection outside of the clock circuitry.
3. Stopped because of a clock malfunction.

For analysis of the A clock see word 5 bits 2-5.

Bit 16 LS request: Channel wishes to perform LS-B transfer. No LS request should exist if:

1. On read, LS full is active.
2. On write, LS full is not active

If LS enable is also active, the LS routine is being serviced, but the LS DTC is still to come.

Bit 17 PCI Request: Channel wishes to present status information to CPU.

1. If 'PCI req,' 'end up (position register), and 'rec end' are all active, the channel has stopped record transmission to the unit. C register bits 8-15 contain the unit status.
2. If 'PCI req' and 'poll' latches are both active, the unit presented status while the channel was idle. C register 0-7 contains unit address; C register 8-15 contains unit status.
3. If 'PCI req' is active with either 'IF read' or 'IF write' active and 'rec end' is not active, the request is due to the PCI flag.

Bits 18-30 Request Register: Positions 21-26 should have only one position active at any time, except for unit select routine where bits 2 and 4 are active. There should be at least one active priority bit if one position in 21-26 is active.

If the 'fin' latch is active when the request register contains a request, the request should be in the position register and the common channel has not yet sent a DTC associated with the routine (the 'inh rtne' indication should not be active). If the 'fin' latch is not on, the channel has not transfered the request into the position register.

Bits 31-35 Common Channel Detect:

1. PCI: If PCI's is active, the CPU has issued a proceed with interrupt signal, the interrupt mask is not active and the common channel is in the break-in cycle.
2. Inh Rtne: If the inhibit routine is active, the selector channel has not responded to the first DTC associated with the routine serviced by CPU. Further requests from the channel will not be considered in the priority matrix until the channel passes through step 0 clock A1 time.

LS Request (pos 16)	LS Detect (pos 31)	Remarks
Priority 1, 2 or 3 request in Sel Ch (18-20)	Pri 1 detect (32) Pri 2-3 detect (33)	
1	0	Either LS detect inhibit latch (for a local store request) (not indicated) inhibit routine latch (for a priority 1, 2, or 3 request) (pos 35), or the routine received latch is active.
0	1	The routine received latch is active and the channel is selected for a routine break-in cycle.
1	1	The channel has responded to a previous routine and the request is not being serviced.

Word 5

Bit 0 Position Register Transfer: If bit 0 is active together with cycle counter step 0 and the 'fin' latch; the request register equals the position register and the first clock sequence in the routine has not occurred.

Bit 1 Inh Rd Store: If bit 1 is active, the last word of data has been stored in CPU even though some of the register full indications are active. Too many bytes were accepted by the channel before the record count information was available in the CCW2 routine when CDA chaining.

Bits 2-5 A-clock Latches: Latches A and B verify proper clock sequencing and outputs. Latches C and D are used with delay lines to generate the clock timings. If improper operation exists, latches A and B stop the sequence.

A and B Latches

A Clock		Clock State
A latch	B latch	
0	0	Clock A0 pulse has not occurred.
1	0	Clock A0 occurred. Clock A1 did not occur.
1	1	Clock A0 and A1 occurred. Clock step did not occur. DTC may be active.
0	1	Clock step is active

C and D Latches

A Clock		Clock State
C latch	D latch	
1	0	Clock A0 time
0	1	Clock step time
1	1	Clock step time and request was made to start another sequence.
0	0	Clock A1 time or DTC is active or clock sequence is complete.

Bits 6-7 SP Latches:

1. D1 active and:
   a. Rd rdy or wr rdy are not active. Tic op has been detected, second op was not yet examined.
   b. Rd rdy or wr rdy is active. PCI interrupt in progress due to the PCI flag.
2. D2 active and:
   a. Instruction scan latch is not active. Channel is performing compare routine for test I/O.
   b. Instruction scan latch is active. Channel is in idle mode.

Bit 8 Instruction Scan Latch: Channel is either:

1. Idle - clock is cycling.
2. Polling - poll latch is active.
3. Performing unit selection and has not yet replied to an initial instruction.

Bit 9 Channel in Use: Channel is in operation as a result of a start, halt or test I/O instruction.

Bit 10 Poll: The channel is attempting to accept interrupt status from an I/O device.

Pos 4 Bit 3	Pos 5 Bit 10	Pos 5 Bit 11	State Description
Unit Sel in Position Reg	Poll LA	Poll Int End LA	
0	1	0	Channel has not stacked poll status.
0	1	1	Channel has stacked status; PCI request is active, common channel has not honored request.
1	1	1	PCI enable received; channel attempts to select unit; unit sel, step 1, CL step not reached.
1	0	1	SEL out sent to unit; polling status taken; channel has not requested the interrupt routine.
0	0	1	Channel should have the interrupt routine in the position register.

Bit 11 Poll Interrupt End: The CPU has received the polling status, causing channel to reply to status in with command out.

Bit 12 Instruction Inhibit: This bit gates the instruction lines when performing a unit selection as the result of control word chaining. It should be reset before a read store or write fetch operation is performed.

Bit 13 BC ready: The new byte count information is available in the selector channel; the interface has not reached a state permitting modification of the byte counter. The fourth clock sequence in CCW2 will not occur until BC rdy is inactive.

Bit 14 UA to Bus Out: In unit selection, the unit address is being gated to bus out. C register byte 0 contains the UA.

Bit 15 Unit Select Adr Out: In unit selection, address out is being generated.

Bit 16 Compare equal: In unit selection, the unit address sent by the channel was the same as that returned by the I/O control unit.

Bit 17 Compare unequal: In unit selection, the unit address sent by the channel was different from that returned by the I/O control unit but each has correct parity.

Bit 18 Stop: The channel has detected conditions for terminating an operation on the interface.

Bit 19 IF CDA First Byte: The channel has accepted the last byte of a read CDA data block. If the latch remains set, the next data byte will be set into all positions of the C register.

Bit 20 CD: Channel is performing a CDA chain operation, collecting and preparing new control information for the handling of the next block of data. The new control information has not been completely transfered to the proper channel registers.

Bit 21 BC Mod Enable: A response to the BC mod request line stating that the interface is at a static state, 'In' tags are not serviced in this period.

Bit 22 Wr Chain Rdy:

Roller 5 Bit 20	Roller 5 Bit 22	Roller 6 Bit 21	Roller 6 Bit 20	Analysis
CD LA	Write Chain Ready	Write Chain Procd	Total Rec'd Fetch	
1	1	0	0	New control information ready in selector channel, old record not fully transmitted.
1	1	0	1	Same as above. Whole new record totally assembled in channel registers.
1	1	1	—	New control information ready, old record fully transmitted, first word of new record not yet sent by CPU.
1	0	1	0	Old record completely transmitted, new control information not ready or the first byte of previous block not transmitted on interface.
1	0	—	1	Channel after prefetching total record and transferring control to proper registers, has requested CCW1 routine and is waiting for DTC.
0	0	1	—	New control transferred to proper registers, new data in C register, first SVC in is not present. CCW1 step 1 CL step has not occurred.

Bit 23 Rec End: The channel is finished with an operation and wishes to store status in the CSW.

Bit 24 Op In Test: 'Op in' line is active in response to sel out, which remains active through the operation. If 'op in' drops while the 'op in test' latch is active, 'IF ctrl check' will be set.

Bit 25 Channel Stop: Channel has immediately stopped all operations. The reason for stopping depends on the check control switch on the CE panel.

1. Process--Stop and log on detection of:
   a. Channel control check
   b. Interface control check
2. Stop:--Stop on detection of:
   a. Channel control check
   b. Interface control check
   c. Data check
   d. Any CPU check (freeze channel line)
3. Channel Stop--Stop on detection of:
   a. Channel control check
   b. Interface control check
   c. Data check
   d. Storage protect or program check
   e. Chain check
   f. Any CPU check (freeze channel line)

Bit 26 Sel Out: Sel out line is active on the interface unless blocked by program scan or manual controls.

Bit 27 Stop Routine: Stop latch has been set and the 'in' tag associated with its setting has fallen.

Bit 28 Sel In: Sel in is active on the interface or it is being simulated by the interface register.

Bit 29 Op In: Op in is active on the interface or it is being simulated by the interface register.

Bits 30-32 IF Out Tags: Conditions have been generated for activating the out tag, but the actual IF line may be blocked by program scan, manual controls or channel stop condition.

Bits 33-35 IF In Tags: Either the in tag is active on the interface or it is being provided by the IF register. 'Svc in' can be blocked on read by 'C full active' and on write by 'C full not active.' Status in can be blocked by the reset of the enable status latch.

Word 6

Bits 1-7 GP Register: The GP register is set from the ALCH bus and is used to hold various types of data during a channel operation. Register contents are:

General Purpose Latches							Channel State
1	2	3	4	5	6	7	
0	0	0	0	0	0	0	Idle to CCW1, Step 1
BC Info		0	0	Rd Cp	Back-wards	WR Op	CCW1, Step 1 to CCW2, Step 1
BC Info		0	0	0	0	0	CCW2, Step 1 to CCW2, Step 2
BC Info		LR Info		L1W	L2W	L3W	CCW2, Step 2 to CCW2, Step 3, A1
BC Info		0	0	L1W	L2W	L3W	CCW2, Step 3A, to Rd Store or Wr Fetch
MB CR Info				L1W	L2W	L3W	Rd Store
BC Info Original		0	0	L1W	L2W	L3W	Wr Fetch
-	-	BC Final		L1W or Comp	L2W	L3W	End up (Rd) to Intrpt to Reset
BC Info Original		0	0	L1W or Comp	L2W	L3W	End up (WR) to Intrpt to Reset

Bits 11-15 Flag Register: This regiater stores the special conditions that the channel command word (CCW) designates for the operation. Flag register positions correspond to flag bits in the CCW. The positions are: chain data, chain command, suppress incorrect length indication (SILI), skip, and program controlled interruption (PCI). The set state of any flag register position causes the channel to deviate from normal procedures in executing the operation.

Except in write chain data operations, the channel sets the flag register while processing the second half of the channel command word (CCW2):

An active CDA flag resets the CC and SILI flags. The CC flag is reset also when control word chaining is suppressed because of checks detected by the interface controls.

Bit 16 Fin Latch: The last clock sequence in the routine has occurred; new request register information can transfer to the position register.

Bits 17-19 First Word, First Byte: On write, if both are active, control information is completely fetched and the first data word is not fetched. On read if both are active, first data byte not yet transmitted on interface.

Bits 20-21 Total Rec Fetch, Wr Chain PRCD: If these bits are active, with the CDA latch; the channel after prefetching total record and transfering control to proper register has requested a CCW1 routine and is waiting for DTC.

Bit 22 Stop Rel: Channel has terminated an operation on the interface. The setting of this latch normally results in dropping sel out and either interrupting or fetching a new CCW.

Bit 26 Stat Next: Channel has detected that the last valid byte has been transmitted on the interface.

Bits 28-31 MP latches:

Routine	MP Latch	Function
Idle	C1	Degates start clock signal when start, test, or halt I/O instruction is detected.
	C4	Unit wants service but instruction line appears. Used for reset of channel and handling the instruction.
CCW1	C1	TIC op is detected.
CCW2	C1	CDA chaining; used in the request of unit select.
	C2	Chain check detected in CCW2; used to end update.
	C3	A channel check is present.
	C4	Starts the clock for the fourth sequence except in Wr CDA.
Wr Fetch	C1	Data is sent from storage to B register.
	C2	L1W line was sent by common channel.
Unit Select	C2	Degates the A clock in the first sequence of two complete clock cycles.
	C3	Degates the A clock in the second sequence of two complete clock cycles.
	C4	Used in the gating of the command to bus out.

Bit 32 Sup Out: This is set:

1. If CC chaining conditions were present when channel end status was received. Reset in next unit selection.
2. When read CDA chaining to prevent chain checks when starting on byte boundaries and working with buffered units. Reset when byte counter is set with new information.
3. For suppressing data under the following conditions:
   a. On read, if common channel allows LS fetches with the LS buffer finish latch on; on write, if one register is full and the end of the record has not been reached.
   b. If the multiplexor channel is in use and is not resetting the interface and the selector channel is transmitting data.

Bit 33 Request In: The request in line is active.

Bit 34 Svc Out Hold: This bit is set in unit selection in response to status in (except on CU busy sequence). Used in write operation to prevent the active state of 'svc in' until data is fetched from storage.

Bit 35 Enable Stat: This bit allows the interface status in line to be gated to the IF controls when I/O status may be gated to the C register.

Section H - Blank

This panel is blank on the basic system.

Section J - Local Store Chart

The printed chart on this panel shows fixed assignments in the local storage area.

Section L - MC, SDR, IAR Indicators; Data and Address Keys

This panel section contains indicators and switches for system maintenance and operator intervention.

Master Check Indicator

The master check light is on when any trigger in the error register is on (KT081).

Maintenance Control (MC) Indicators

This row of 36 indicators is used with the Fault Locating Tests (FLT's). Figure 169 shows the ALD page, bit position, and a description of the 36 indicators.

Storage Data Register

The 36 indicators in this row display the Storage Data Register (SDR). Bit positions 0, 9, 18, and 27 display the parity of the associated byte. Figure 170 shows the ALD location of the indicators.

Data Keys

The 32 data keylever switches specify four data bytes to be stored in an addressed location. Correct parity is normally generated. Incorrect parity may be generated with the reverse data parity switch.

Data keys may be used to specify a selected ROS address for display or compare. A storage address is set into the data keys for SAR compare. The data keys are also used to simulate bytes of data when testing the channels. The keys can be changed without disrupting CPU operations.

Reverse Data Parity

This switch generates incorrect parity for data specified in the data keys. Parity is inverted for all bytes of the word. The test light is on when this switch is on.

Storage Select Switch

The storage select rotary switch selects the storage area that is to be addressed by the address keys. This switch can be moved without disrupting CPU operations. The four switch positions are: Local Storage, Main Storage, Protect Storage, and MPX Storage (Bump).

Instruction Address Register

This row of 27 indicators displays the Instruction Address Register (IAR). Bit positions 9, 18, and 27 indicate the parity of the associated byte. Figure 171 shows the ALD locations of the indicators.

Address Keys

The 24 address keylever switches address a location in a storage area. These keys, in conjunction with the storage select switch, permit store or display access to any location in local storage, main storage, protect storage, and bump storage. The keys can be changed without disrupting CPU operations.

The address keys are also used to simulate various conditions when manually testing the channels. (Refer to Panel Section F - Channel Control.)

Section M - Intervention and Maintenance Switches

This panel section contains pushbutton, rotary select, and keylever switches that are required for operator intervention and system maintenance. The customer and CE usage meters and a permanent storage assignment chart are also located on panel section M.

Rate Select Switch

The rate switch determines the manner in which instructions are to be performed. Three positions are provided: process, instruction step, and single cycle. When the rate switch is off the process position, the test light is on.

Process: The system operates at normal clock speed.

Instruction Step: One complete machine instruction is executed for each depression of the start switch, after which the CPU returns to the stopped state. The stop point is identical to that achieved by the stop switch. Any machine instruction can be executed in this mode. Input/output instructions are completed to the interruption point. The interval timer is not incremented while the rate switch is set to the instruction step position. Moving the rate switch from process to instruction step while the CPU is running has no effect.

Single Cycle: The CPU advances by its minimum clock amount for each depression of the start switch, returning to the stopped state each time. Input/output instructions can be single-cycled to the point where asynchronous operation begins. The asynchronous portion starts with the next depression of the start switch and runs to completion. If the start switch is

depressed during this time, the next cycle is taken. If an interruption results, the interruption sequence is not automatically executed but must be single-cycled. Moving the rate switch from process to single cycle while the CPU is running stops the CPU.

The stopped state for single cycle is one in which no CPU clocks are running. In the normal stopped state, ROS is running and executing the halt loop.

Start PB Switch

The start pushbutton switch starts system operation as defined by the rate switch. If it is pressed after a normal stop, it causes continuation of instruction processing as if no stop had occurred. If it is pressed after a system reset, the instruction designated by the instruction address register is the first one executed.

Stop PB Switch

The stop pushbutton switch causes the CPU to enter the stopped state. The stopped state is indicated by the manual light being on. The transition from operating state to stopped state occurs at the end of instruction execution. When the CPU is in the wait state, the transition takes place immediately. All interruptions which are pending and not masked off are taken, causing the old PSW to be stored and the new one fetched before entering the stopped state.

System Reset PB Switch

The system reset pushbutton switch resets the system to its initial state. The switch is active in all modes. The general status of the system after a system reset is:

1. CPU is in the stopped state.
2. All pending interruptions are eliminated.
3. Each channel in the system receives a reset. The channels, in turn, issue a general reset to the I/O interfaces. (Off-line control units and I/O devices are not reset.)
4. All error indicators are reset. Errors occurring during initialization will show.
5. All local store registers are set to good parity.
6. The bump area of main storage is set to good parity. The DA word is set to zero. The other three words associated with each subchannel are set to 07000000.
7. The instruction address register is set to zero.
8. The L, M, H, R, J, and MD registers are set to good partiy.
9. The FLT Op register, pass and fail triggers, ignore error I/O trigger, and progressive scan stat are reset.

PSW Restart PB Switch

The PSW restart pushbutton switch causes a system reset followed by a load PSW operation from storage location zero. At completion of the load PSW, the CPU changes from stopped to operating state. This switch is active in all modes.

Check Reset PB Switch

The check reset pushbutton switch resets all check triggers in the error register and turns off the master check light.

Set IC PB Switch

The set IC pushbutton switch enters an address into the instruction address register. The address is specified by the address keys. This switch is active only when the CPU is in the manual state.

Store PB Switch

The store pushbutton switch stores information in an addressed location. Data specified by the data keys is placed in the location specified by the address keys and the storage select switch. Storage protection is ignored. The store switch is active only while the CPU is in the manual state.

Display PB Switch

The display pushbutton switch causes information in an addressed location to be displayed. The switch is active only while the CPU is in the manual state.

The information at the storage location specified by the address keys and the storage select switch is displayed in the following indicators:

Storage	Indicators
Main	Storage Data Register
Local	L Register (CPU Roller #1, Roller Switch Position #1)
MPX (Bump)	Storage Data Register
Protect	F Register (CPU Roller #2, Roller Switch Position #4)

Log Out PB Switch

The log out pushbutton switch causes a complete log out of CPU and channel status. This log out is identical to that which occurs when an error is detected.

The log out switch is active when CPU is in one of the following states:

Manual
Single cycle
Hard stop
ROS address compare stop

Address Compare Key (IAR)

The address compare (IAR) keylever switch provides a means of stopping the CPU or generating an oscilloscope sync pulse on an instruction address comparison. Three switch positions are provided: process, stop, and sync. When this switch is set to stop or sync, the test light is on.

Process: No comparison is performed.

Stop: An equal comparison between the address keys and the instruction address register causes the CPU to enter the stopped state. The stop occurs at completion of the addressed instruction.

Sync: An equal comparison between the address keys and the instruction address register causes an oscilloscope sync pulse to be generated at the sync control box. (The sync control box is mounted on the end of C gate behind the control panel.)

Repeat Instruction Key (IAR)

The repeat instruction (IAR) keylever switch causes the instruction at the location specified by the address keys to be repeated, under control of the rate and start switches. The test light is on when this switch is not in its normal position.

Address Compare Key (ROS)

The address compare (ROS) keylever switch causes a comparison of the twelve low-order data keys (thirteen for extended ROS) and the ROS address. Two positions are provided; stop and sync. The test light is on when the switch is not in the sync position.

Stop: The CPU stops on an equal comparison. The stop occurs at completion of the addressed microinstruction.

Sync: An oscilloscope sync pulse is generated by an equal comparison. The sync pulse is available at the sync control box.

Repeat Instruction Key (ROS)

The repeat instruction (ROS) keylever switch causes the microinstruction at the location specified by the twelve (thirteen for extended ROS) low-order data keys to be repeated continuously. The test light is on when this switch is on.

Address Compare Key (SAR)

The address compare (SAR) keylever switch provides a means of stopping the CPU or generating an oscilloscope sync pulse on any address other than instruction addresses used for main storage. Two positions are provided: stop and sync.

Stop: An equal comparison between the SAR compare keys (data keys 8-31) and the AOB to SAR causes the CPU to enter the stopped state.

Sync: An equal comparison between the SAR compare keys and the AOB to SAR generates an oscilloscope sync pulse as the sync control box.

The above address comparisons are further gated to distinguish between I/O and CPU addresses by the SAR compare control keys (data keys 0 and 1). Both switches off (straight out) deconditions the SAR compare. The SAR Address Compare switch is ineffective in FLT modes.

Disable Interval Timer Key

This keylever switch prevents the interval timer from advancing. The test light is on when this switch is on.

Lamp Test Key

The lamp test keylever switch permits all indicators (except marginal voltage, frame thermal, open CB, and power check) to be tested simultaneously. The indicator driver is tested as well as the lamp.

Force Indicators Key

A special FLT op register is used to control scan-out during execution of FLT tests. At such times the information displayed in the status indicators is under control of this special op register rather than the status roller select switches.

The force indicators keylever switch provides a partial override of the FLT op register. Any indicator that was off will give a valid indication when the switch is pressed. The force indicators switch

allows certain registers and status information to be displayed regardless of the FLT op register and is primarily intended for use during single cycling of FLT's.

FLT Mode Key

The FLT mode keylever switch is used with the FLT tests. Two positions are provided: start/load and force pass.

Start/Load: This position redefines the start and load switches to provide for initial loading of FLT programs and starting up after a test termination. When the load switch is pressed, IPL is not executed. Instead, an FLT load occurs using hardcore controls, and data enters storage directly, bypassing common channel hardware. If the start switch is pressed following a stop condition, testing is resumed.

Force Pass: This position causes bypassing of a failing FLT when the start switch is pressed following a stop condition.

FLT Control Select Switch

The FLT control rotary select switch provides five modes of operation when performing FLT load or executing tests. The switch positions are: process, stop, repeat, auto re-read, and halt after load.

Process: Each FLT is executed 16 times before branching to the next test.

Stop: The CPU stops after repeating a test 16 times if the fail trigger has been set.

Repeat: The FLT being executed is repeated continuously. The pass/fail indicators are reset every 16 times.

In each of the first three positions (process, stop, and repeat) a data check during FLT load causes the CPU to hang up. The two additional positions of the switch are provided to control retry; both cause execution in the process mode once the FLT record is in main storage.

Auto Re-Read: Backspace and retry occur automatically without the need for manual intervention.

Halt After Load: CPU hangs up at the end of any FLT load sequence whether it was correct or not. If correct, the start switch causes execution. If incorrect, the start switch causes a backspace and then a hang up.

Check Control Select Switch (CPU or Channel Op)

The check control rotary select switch provides four modes of operation when an error is detected in either the CPU or channels.

CPU OPERATION:

Process: Unless PSW bit 13 is masked, this position causes an error log of the entire system followed by a machine-check interrupt. If PSW bit 13 is masked, the error register will be set but the error will remain pending. Error log and machine-check interrupt will occur upon unmasking of bit 13.

Disable: Any errors that occur are set into the error register but operation continues. No log out or interrupt occurs.

Stop: The first error that occurs stops the system with the error displayed in the error register.

Chan Stop: The first error that occurs stops the system with the error displayed in the error register.

CHANNEL OPERATION:

Process: If bit 13 is masked, operation proceeds (as in disable mode) except that system log out due to error detection takes place when bit 13 is unmasked. The selector channel stops and is logged upon detection of a channel control or interface control check. Two types of logouts may occur; (1) full log out, which includes the selector channel in error and CPU registers; or (2) partial log out, which includes only the selector channel.

Full log out occurs as a result of the following check conditions:

- Parity check of logword 5 test
- Parity check detected by CPU
- First cycle test
- Chain check
- Time out check

Partial log out occurs as a result of the following check conditions:

- Interface control checks
- Byte counter parity check
- Interface bus out parity check on non-data sent to the unit
- Logword 4 test
- Zero test of logword 5 test

Any other selector channel errors request an I/O Interrupt with the status in the CSW.

Disable: When a check condition is detected, the channel attempts to terminate the operation and have status formed in the CSW. If an interface control check exists, an interface reset sequence occurs immediately.

The time out signal associated with an I/O instruction is not sent to the selector channel; the time out check causes the common channel to initiate formation of the CSW and reset the selector channel.

Stop: The selector channel and CPU stop upon detection of a channel control check, interface control check, or any CPU check condition.

Channel Stop: The selector channel stops on detection of any channel check condition except ILI, program check, storage protect check, or channel data check. CPU check conditions also freeze channel operations.

In this mode, interface responses (out tags) are delayed until 'in tag delay 3' time so that a check condition detected by interface tests can stop the channel response on the interface. This mode should not be used with diagnostic programs that force check conditions.

Metering

Two time-recording meters and a key-operated switch are located on panel section M. One meter records customer usage time; the other records maintenance time. The key-operated switch selects which meter is to record the running time. The selected meter accumulates time when:

1. The manual light is off and there is no wait bit in the PSW.
2. A metering-in signal is received from any I/O device.
3. Any system control panel pushbutton switch is pressed.

Section N - Operator Controls

This section of the system control panel contains the controls required by the operator when the CPU is operating under full monitor control. A minimum of direct intervention is required of the operator because the control program performs routine operations such as store and display. The main functions provided on this panel section are the control and indication of power and initial program load controls.

Power On PB Switch

The power-on switch initiates the power-on sequence for the system. Power is applied to dc supplies in five groups. Power controls include sensing circuits to prevent application of the next group until all levels in the previous group are present. Power and cooling failures bring power down in reverse sequence.

A system reset occurs at the completion of the power-on sequence. The button is backlighted to indicate when power is on and the I/O Adapter relay has stepped to completion. Power-on switch is active only when emergency off switch is 'in'.

Power Off PB Switch

The power-off switch initiates the power-off sequence for the system.

Load PB Switch

The load switch causes a system reset and starts the Initial Program Load (IPL) routine.

Load Unit Select Switches

Three rotary select switches provide an 11-bit number to select the channel and I/O device for IPL. The left switch has eight positions labeled 0 through 7 to select the channel. The other two switches select the device and are labeled with the hexadecimal characters 0-9 and A-F.

Interrupt PB Switch

The interrupt switch causes an external interruption request. The interruption is taken when not masked off and when the CPU is not stopped. Otherwise the interruption request remains pending. When the interrupt is taken, bit 25 of the PSW is set to one to indicate that the interrupt switch is the source of the external interruption.

System Indicator

This indicator (PK101) is on whenever the customer usage meter or the maintenance meter on the system control panel is running.

Manual Indicator

This indicator (PK101) is on when the CPU is in the stopped state.

Wait Indicator

This indicator (PK101) is on when the CPU is in the wait state (bit 14 of the current PSW is one).

Note: Operations cannot be single-cycled while the CPU is in the wait state.

Test Indicator

This indicator (PK101) is on when a manual control is not in its normal position or when a maintenance function is being performed for CPU, storage, or channels. The following switches light the test indicator when not in their normal positions:

Check Control	Manual Operation
Reverse Data Parity	Rate
FLT Mode	Address Compare (ROS)
FLT Control	Repeat Instruction (ROS)
Address Compare (IAR)	Storage Test
Repeat Instruction (IAR)	Invert SAR Bit 16
Disable Interval Timer	CE Mode (Metering)
Address Compare (SAR) - Stop	

Load Indicator

This indicator (PL031) is on while the CPU is executing the IPL routine. The indicator is turned on

when the load switch is pressed and is turned off after the read operation and loading of the new Program Status Word (PSW) are successfully completed.

OPERATING INSTRUCTIONS

- Power, interrupt, and initial program load switches on panel section N provide basic system control.

- Switches and indicators on panel sections L and M permit program intervention by the operator.

The switches on panel section N permit the manual operations that are necessary when the system is to be operated under full supervisor control. Power switches apply or remove system power; initial program load switches reset the system and load the first program; and the interrupt switch allows an external interrupt request to be made. Five indicators on panel section N display overall system status to the operator. Start, stop, reset, display, store, and other intervention operations are performed with the switches and indicators located on panel sections L and M.

System Initialization

System initialization results from a system reset. A system reset occurs with the power-on sequence, the initial program load routine, or from the depression of either the system reset or the PSW restart switch.

Initial Program Load (IPL)

Initial program load is performed by selecting a properly-prepared input device with the load unit rotary select switches and pressing the load pushbutton switch. The three rotary switches provide the 11-bit address of the desired device. The leftmost switch, labeled 0-7, designates the channel number. The two remaining switches, labeled with the Hex characters 0-9 and A-F, designate the device. Pressing the load pushbutton switch causes a system reset, turns on the load indicator, turns off the manual indicator, and initiates a read operation from the selected input device.

IPL reads new information into the first six words of main storage. The remainder of the IPL program may be placed in any desired section of storage. Storage protection, program controlled interruption, and incorrect length indication are ignored.

Display and Store Operations

Intervention controls on panel sections L and M permit the operator to display or store data in main storage, in local storage, and in the working PSW. For these operations the system must be in the stopped state (manual indicator on). The stopped state is achieved at the end of the current instruction when the stop switch is pressed, when single instruction execution is specified, or when a preset stop address is reached.

Display Main Storage

1. Manual mode.
2. Set the desired address in address switches 8 through 29.
3. Turn the storage select switch to "Main."
4. Press the display switch.
5. The word at the desired address is displayed in the SDR indicators.

Store in Main Storage

1. Manual Mode.
2. Set the desired address in address switches 8 through 29.
3. Turn the storage select switch to "Main."
4. Set the desired data switches.
5. Press the store switch.

Display Local Storage

1. Manual mode.
2. Set the sector to be displayed in address switches 22 and 23.
3. Set the word to be displayed in address switches 24 through 27.
4. Turn the storage select switch to "Local."
5. Press the display switch.
6. The selected word is displayed in the L Register (CPU Roller #1, Switch Position #1).

Store in Local Storage

1. Manual mode.
2. Set the desired sector in address switches 22 and 23.
3. Set the desired word in address switches 24 through 27.
4. Set the desired data switches.
5. Set the storage select switch to "Local."
6. Press the store switch.

Display the Working PSW

1. Manual mode.
2. Set address 170 in the address switches.
3. Set the storage select switch to "Local."
4. Press the display switch.
5. The working PSW (first half) is displayed in the L Register (CPU Roller #1, Position #1).

Alter the Working PSW

1. Manual mode.
2. Set address 170 in the address switches.
3. Set the storage select switch to "Local."
4. Set the desired data switches.
5. Press the store switch.

Miscellaneous Operations

Set the Instruction Counter

1. Manual Mode.
2. Set the desired instruction address in the address switches.
3. Press the set IC switch.

Stop on an Instruction Address

The following steps should not be taken while executing a program but may be taken in any other mode.

1. Set the desired address in the address key-lever switches.
2. Place the IAR address compare switch in the stop position.
3. The address in the address switches will be executed and the next address in the program will be displayed in the IAR. If the instruction at the address in the address switches is a branch instruction and the branch is taken, the address displayed in the IAR is the address of the branch instruction.

Changing the address keys while in IAR stop or sync mode and a program is running, may cause a machine check condition to occur.

Reset An Error Indication

The check reset switch is normally used to reset all machine check indicators. Check reset only resets the error indicators and does not guarantee that the object program has not been altered by a machine failure. A system reset, however, resets the complete system, including all pending interruptions.

Bump Storage Display

To display bump storage:

1. Set the storage select switch to MPX 22-31.
2. Set the desired word in address switches 22 and 23.
3. If an unshared subchannel is being displayed, set the unit address in address switches 24-31.
4. If a shared subchannel is being displayed, set the modified unit address in address switches 24-31.
5. Press the display switch.

To display bump storage after a hard stop:

1. Set the ROS address switches (data switches) to 191 (Hex).
2. Set ROS REPEAT INSN down.
3. Press START.
4. Set check control switch to DISABLE.
5. Set manual channel control to MPX.
6. Restore ROS REPEAT INSN.
7. Set the rate switch to INSN STEP.
8. Press START.
9. Press STOP.
10. Follow the foregoing procedure to display desired location.

Clear Storage

1. System reset.
2. Set IAR keys to zero.
3. Set rate switch to SINGLE CYCLE.
4. Set data switch 22 down (all others straight out).
5. Set ROS REPEAT INSN down.
6. Press START.
7. Restore ROS REPEAT INSN.
8. Restore data switch 22.
9. Set rate switch to PROCESS.
10. Press START.
11. System reset.
12. Press STORE.

Alternate Method of Clearing Storage

1. Set data switch 22 down (all others up).
2. Set ROS REPEAT INSN down.
3. System reset.
4. Restore ROS REPEAT INSN.
5. Restore data switch 22.
6. Allow IAR to ripple through one time.
7. Set ROS REPEAT INSN down to terminate.
8. System reset.

ROS Function Check

Figure 172 shows the content of the closed loop starting at ROS 202 that can be used to display, change, and observe the content of the various CPU registers (QW111).

ROS 202 Loop Procedure:

1. System reset.
2. Set check control switch to DISABLE.
3. Set rate switch to SINGLE CYCLE.

4. Set data switches 22 and 30 down.
5. Set ROS REPEAT INSN down.
6. Press START.
7. Restore ROS REPEAT INSN.
8. Set desired data in data and address switches.
9. Set rate switch to PROCESS.
10. Press START.

The following results will occur:
Data keys to the L, R, M, and H registers, and SDR.
Data keys 12-15 to J-reg; 8-11 to MD; and 28-31 to F-reg.
Address keys to IAR and SAR (to initiate storage cycle for read out and regenerate).

Note: For ZCT failures, use this routine to load all registers.

Recycle Any Maintenance Console PB Operation

1. Tie C-A4H23 (manual control pulse SS) PK001 to A-A4E2D2 (60-cycle interval timer KS252).
2. Depress pushbutton to be tested, and hold it depressed as long as cycling is desired.

Note: The 60-cycle interval timer pulse will fire the manual control pulse SS, and, as long as any maintenance console pushbutton is depressed, the operation will be restarted by the pulse that updates the timer.

THEORY OF OPERATION

- System reset, power-on reset, PSW restart, and IPL use common reset routine.
- IPL routine loads the initial program and starts program execution.
- Stop switch sets stopped state and halt loop.
- ROS halt loop samples panel switches for display and store operations.

Power On, Power Off

The power-on switch initiates the power-on sequence. The pushbutton is backlighted to indicate when power is on. The power-off switch initiates the power-off sequence. For theory of operation of the power-on and power-off sequences refer to FE Theory of Operation, System/360 Model 50 Power Distribution and Control SY22-2829.

System Reset

The Model 50 is initialized with a system reset. A system reset occurs with the power-on sequence; the initial program load routine; or from depression of the system reset or the PSW restart switch. The general status of the system after a system reset is:

1. CPU is in the stopped state.
2. All pending interruptions are eliminated.
3. Each channel in the system receives a reset. The channels, in turn, issue a general reset to the I/O interfaces. (Off-line control units and I/O devices are not reset.)
4. All error indicators are reset. Errors occurring during initialization will show.
5. All local store registers are set to good parity.
6. The bump area of main storage is set to good parity. The DA word is set to zero. The other three words associated with each subchannel are set to 07000000.
7. The instruction address register is set to zero.
8. The L, M, H, R, J, and MD registers are set to good parity.
9. The FLT Op register, pass and fail triggers, ignore error I/O trigger, and progressive scan stat are reset.

System Reset Operation

The system reset timing sequence is shown on Timing Chart 203--System Reset Sequence, #T2031. Figure 173 in this manual is a flow diagram of microprogram system reset.

System reset or power-on reset forces address 242 on QU100. IPL routine and PSW restart enter the common reset routine at block 2B2. At this point, two parallel operations are started: correct local store parity, and load bump storage. Local store data is run through the adder for correct parity insertion. The DA word of bump storage is loaded with zeros; the other three words associated with each subchannel are loaded with 07000000.

Local store is addressed with bits 2 and 3 of the emit field and bits 24 through 27 of the R register. The R register must therefore be decremented 16 times to cause a change in bits 2-5 of LSAR. Because of this, each local store word is parity-corrected a number of times while bump is being loaded. When byte three of the R register is reduced to all zeros, the loop operation is finished and a branch exit results from S3 and MD settings. For system reset, S3 = 0 and MD = 3 cause a branch to block 204 to restore PSW 0-7 and 12-15. The routine then goes to the halt loop on QT200.

Microprogram Reset: The following procedure can be used to check the reset loop on QU100:

1. Set rate switch to PROCESS: enter address 242 in ROS address entry keys.
2. Set the stop on ROS address switch to ON.

3. Depress system reset pushbuttons; the system should stop at next ROS address 2BA. FLT 2 and block indicators should light (to check ROAR, depress force indicator lever). Each subsequent address will appear in the next ROS address field and represents the true next address.

4. Set rate switch to SINGLE CYCLE.

5. Single cycle through the microprogram and assure that the proper conditions are set.

6. Single-step through the bump storage loop and local storage loop.

7. Enter 243 in ROS address entry keys.

8. Set the stop on ROS address switch to ON.

9. Set rate switch to PROCESS.

10. Depress the system start pushbutton; this will loop through all of the bump storage loop. Current ROS will stop at 243.

Halt Loop: The following procedure can be used to check the halt loop on QT200:

1. Perform step (7) through (10) from previous operation (microprogram reset).

2. Set the rate switch to SINGLE CYCLE and continue single stepping through the microprogram until current ROAR 150.

3. Set the rate switch to PROCESS. Depress START.

Current ROS Address	Condition
243	Set allow error and error interrupt on
204	
150	Halt loop
191	Halt loop
18C	Halt loop
208	Halt loop

4. Enter 208 in ROS address entry keys, set the stop on ROS address switch to ON.

5. Depress the system reset pushbutton; CPU will stop with current ROAR at 208.

6. Return the stop on ROS address switch to normal; depress the system reset pushbutton.

When ROAR is at address 208, halt loop is operating correctly. Set the rate switch to PROCESS and depress the system start pushbutton; all four clock indicators should come on.

Initial Program Load

To load a program, the channel number and the desired device must be entered in the three load unit switches.

Pressing the load pushbutton causes a system reset and initiates a read operation from the selected input device.

The first 24 bytes read are placed in storage locations 0-23. The doubleword in location 0 is the IPL PSW. The doubleword read in location 8 is the channel command word (CCW). When chaining is specified in this CCW, the operation proceeds with the CCW at location 16 (CCW2).

After the input operation is performed, the I/O address is stored in bits 21-31 of the first word in storage. Bits 16-20 are set to zero; bits 0-15 remain unchanged. The CPU proceeds under control of the new PSW in location 0 and the load indicator is turned off. Interruptions that become pending during IPL are taken before instruction execution.

If the PSW in location 0 has bit 14 set to one, the CPU is in the wait state after IPL. If the I/O operation and PSW loading are not completed satisfactorily, the CPU idles and the load indicator remains on.

IPL Operation

IPL timing and clock controls are shown on Timing Chart 202--Load Sequence, #T2021. Microprogram logic flow is shown on Figure 174 in this manual.

The IPL load switch forces address 240 on QU100. The error and H registers are cleared; MD is set to 3; S3 is set to 1; and the common reset routine is initiated. At the completion of system reset, MD = 3 and S3 = 1 branches the microprogram to QK800.

On QK800: CCW2 is set up, the unit and channel addresses are set in the L register, and zeros are set in the R register for the command address. S3 is reset; S7 is set; and Start I/O is issued. The program then loops on block 988 waiting for the channel response.

With the channel response, S3 is set on to break out of the wait loop. Stats 0-3 are reset and a test is made for condition code (CC) = 0. CC = 1, 2, or 3 indicates that Start I/O is not accepted by the channel and the microprogram will loop in block 98C. CC = 0 indicates that Start I/O has been accepted and begun by the channel. S7 is reset, Test I/O is issued, and the wait loop is taken for channel response. S3 is turned on with channel response and a test is made for CC = 1 (channel end). The microprogram loops on CC = 2 (channel busy) until CC = 1 is received. After channel end sets CC = 1, channel status and unit status checks are made on logic QK801.

Channel status (40-47 of CSW) must be XX000000 or the program will loop on block 990. Unit status (33-39 of CSW) must be 0XX01X00 or the program will loop on block 919. If both status checks are good, the PSW is loaded from location zero and program execution is started.

Note: If IPL hangs up with the CPU idle and the load indicator on, the microprogram will most

likely be in one of the following loops:

Block 988 - No channel response
Block 98C - Start I/O not accepted by channel
Block 990 - Channel status bad
Block 919 - Unit status bad

Start, Stop

The start and stop switches on panel section M allow the operator to intervene in programmed system operation.

The start switch initiates system operation under control of the rate switch. After a system reset, the start switch begins program execution with the instruction designated by IAR. After a normal stop, the start switch causes processing to continue as if no stop had occurred.

The stop switch places the CPU in the stopped state. The manual trigger is turned on and the resultant exception branch causes ROS to enter the halt loop. Store, display, and other exception-type manual operations are dependent on the halt loop.

Figure 175 in this manual is a diagram of start, stop, and exception logic. For start and stop sequence timing refer to Timing Chart 210--Start, Stop, Check Reset, #T2101. Exception logic flow is shown on CLF 121, Basic Interruption Flow and CLF 122, Interruptions/Exceptions, in the Diagrams Manual.

Start

Pressing the start switch after a normal stop turns off the manual trigger to allow ROS to break out of the halt loop and branch to I-fetch. The start switch fires the 135 ns singleshot (any pushbutton) to bring up the MC Pulse Ungated line. This line develops MC Pulse Gated which AND's with the start PB switch to bring up Start Sw. With the rate switch set to process, Start Sw turns off both manual triggers and the stop trigger. Manual trigger off drops the Exception line allowing ROS to exit from the halt loop.

On QT200, Exception = 0 causes a branch out of the halt loop. PSW 0-15 is set in the L Register to restore the storage protect key; IAR is set in the H Register and through the adder to set SAR; and a branch is made to I-fetch. The Start PB line that is brought up along with Start Sw develops the Pulsed Start PB line (circled 5 on Figure 175). Pulsed Start PB drops Hard Stop and develops the clock controls on logic KT211 and KT221.

Stop

Pressing the stop switch turns on the manual trigger to place the CPU in the stopped state and ROS in the halt loop. The stop PB switch generates the same MC pulse as the start switch. MC Pulse Gated AND's with the stop PB switch to bring up Stop Sw which turns on manual triggers A and B. Manual trigger A sets Exception = 1 to cause ROS to branch to the halt loop after the current instruction has been executed. Manual trigger A also turns on the manual indicator and brings up Halt Trigger (KS141) to enable the setting of stats 4-7 for subsequent manual operations. Manual trigger B on inhibits the Timer Update Signal (Timer Tick).

The halt loop on QT200 consists of four microprogram instructions. The first instruction samples the control panel switches to set stats 4-7, turns off the stop trigger, and checks for external or channel interruptions. The second and third instructions decode stats 4-7 for manual operation requests. The fourth instruction indicates no manual requests have been made and therefore turns on the stop trigger and tests for exception. With exception held on by the manual trigger on, ROS will continue cycling in the halt loop waiting for operator intervention.

Halt loop manual operations (display, store, set IAR, etc.) set stats 4-7 for the correct branch from microinstruction two or three of the halt loop. All branch instructions, except one, will turn on the stop trigger to inhibit any external or channel interruptions. The one exception is the instruction step operation which allows one instruction to be executed and interrupts, if any, to be taken after execution. On return to the halt loop, the fourth instruction turns on the stop trigger to prevent any subsequent interruptions.

Halt Loop Operations

Halt loop operations are performed under control of the halt loop and GP stats 4 through 7. The Op Panel to S 4-7 microorder (step one of the halt loop) sets the stats indicated by the Cons Fcn lines that are brought up by the panel switches. The halt loop controlled operations are:

Instruction step
Set IC
Repeat instruction (IAR)
Address compare (IAR)
Display and store main storage
Display and store protection key
Display and store local storage
Display and store bump storage

All of the above operations, except address compare, require that the CPU be in the stopped state (ROS in the halt loop, QT200). Address compare will force ROS into a halt loop cycle after each instruction execution. Step one of the halt loop allows

the control panel switches to set stats 4-7. Steps two and three of the halt loop decode the stats and branch ROS to the desired routine. Logic flow for the operations is shown on CLF 122, Interruptions/ Exceptions, in the Diagrams Manual.

Stat Setting

Figure 176 shows the GP stats that are set by the panel switches and the logic involved. The Hex value of the four stat bits is used on the Interruption/ Exceptions CLF chart to denote the operation. The switch settings on the control panel bring up the proper Stat Cons Fcn lines which are gated by Set Sts 4-7 Per CE Cons and the halt trigger to set the general purpose stats.

Instruction Step

The rate switch set to instruction step turns on the manual trigger (if off) and brings up the exception line (Figure 175). Pressing the start switch (wait bit must be off) develops the Stat 7 Cons Fcn line allowing stat 7 to be turned on. Decode of stats 4-7 branches ROS to instruction 151. The stop trigger is left off to allow interrupts following instruction execution to be honored. Storage protect key is restored and a branch to I-fetch is made with the H register (instruction address) in SAR. (Refer to CLF Interruptions/Exceptions.)

After the single instruction has been executed and interrupts, if any, taken, the halt loop is reentered. Step four of the halt loop (150) turns on the stop trigger to prevent any subsequent interruptions.

Set IC

The set IC switch enters an address, specified by the address switches, into the IAR. Set IC develops Set IAR to set stat 6. Halt loop decode branches ROS to instruction 152. The stop trigger is turned on; the address keys are set in IAR; and ROS returns to the halt loop.

Repeat Instruction (IAR)

The repeat instruction switch causes the instruction at the location specified by the address keys to be repeated. Pressing the keylever switch down allows the setting of stats 6 and 7. Stat decode causes ROS to branch out of the halt loop to instruction 153. The stop trigger is turned on; storage protect key is restored; the address keys are set in SAR; and ROS branches to I-fetch. At the completion of instruction execution, the exception branch returns ROS to the halt loop and the same routine is repeated.

Address Compare (IAR)

With the address compare switch in the stop position, an equal compare between the address keys and the IAR causes the CPU to enter the stopped state after execution of the addressed instruction. In the sync position, the same comparison causes an oscilloscope sync pulse to be generated but processing continues.

The address compare switch set to stop or sync sets the exception branch (Figure 175) and causes the turn on of stat 5 (Figure 176). The exception branch takes ROS to the halt loop after each instruction execution. Stat decode branches ROS to instruction 209 to turn on the stop trigger and set the address keys in the L register. The L register is compared with IAR (R register) and the storage protect key is restored. An unequal compare allows ROS to branch directly to I-fetch with the next address.

An equal compare between the L and R registers causes generation of the sync pulse by instruction 107. If the address compare switch is set to the sync position, ROS branches to I-fetch with the next instruction address. If the address compare switch is set to the stop position, the sync pulse turns on the manual trigger (Figure 175) to place CPU in the stopped state.

Note: The address compare switch in the stop or sync position adds a minimum of 3 microseconds (time required to check IAR keys and IC for comparison) to each instruction.

Display and Store

Figure 176 shows the stats that are set for each unique display or store operation. Use the Hex value of the stat bits to follow the CLF Interruptions/ Exceptions diagram.

All display or store operations cause stat 4 to be set on. Store operations will also set stat 7 on. The setting of stats 5 and 6 is dependent on the storage area defined by the storage select switch: main, local, protect, or bump (MPX).

Halt loop decode of stats 4-7 causes all display and store operations to branch to logic QT220 (20A for main storage and storage protect; 20B for local storage and MPX bump storage). The display timing sequence is shown on Timing Chart 208, #T2081; the store timing sequence is shown on Timing Chart 207, #T2071.

Display: The display pushbutton switch causes the data at the address and the storage unit specified by the control panel switches to be displayed. The 135 ns (any pushbutton) singleshot generates the MC Pulse Gated line which AND's with the display PB

switch to develop Display Stor. The Display Stor line allows stat 4 to be set. The position of the storage select rotary switch determines the setting of stats 5 and 6 (Figure 176). Halt loop decode of stats 4-7 branches ROS to QT220 for the selected routine as follows:

Display Main Storage--20A, 20D, 235.
Address keys to R register to SAR.
SDR displays data at the location specified.

Display Storage Protect Key--20A, 20E, 2BB, 2BE.
Address keys to R register to SAR.
Storage Protect Key to F register.
F register indicators display Protect Key (CPU Roller #2, Position #4).

Display Local Storage--20B, 244, 2C1, 21-(branch on sector), 234.
Address keys 22-23 to LSFR, 24-27 to MD (LS sector, address).
Local Storage to L register.
L register indicators display local storage (CPU Roller #1, Position #1).

Display MPX Bump Storage--20B, 244, 2C3, 21-(branch on sector), 235.
Address keys 22-31 to SAR (22-23 = sector)
SDR indicators display bump area specified.

All display routines end by branching back to the halt loop.

Store: The store pushbutton switch causes the data specified by the data keylever switches to be stored in the selected area. The MC Pulse Gated line AND's with the store PB switch to develop the Write Stor line. Write Stor allows the setting of stats 4 and 7. The setting of stats 5 and 6 is dependent on the position of the storage select rotary switch. Halt loop decoding of stats 4-7 branches ROS to QT220 for the selected routine as follows:

Store in Main Storage--20A, 20D, 237.
Address keys to R register to SAR.
Data keys to SDR.

Store Storage Protect Key--20A, 20F, 2BF.
Address keys to R register to SAR.
Data keys to F register.
F register to storage protect.

Store in Local Storage--20B, 244, 2C1, 21-(branch on sector), 236.
Address keys 22-23 to LSFR, 24-27 to MD (LS sector, address).
Data keys to Local Storage.

Store in MPX Bump--20B, 244, 2C3, 21-(branch on sector), 237.
Address keys 22-31 to SAR (sector, address).
Data keys to SDR.

All store routines end with ROS branching back to the halt loop.

1	I/O INSTRUCTION				CHAN NUMBER			INSTRUCTION REPLY						PRCD ON IRPT	TIME OUT	[illegible]	FOUL	
	START I/O	TEST I/O	HALT I/O	TEST CHAN	4	2	1	0	1	2	3	REPLY	BCHI					

																			1

Indicator	ALD	Bit Position	Description
START I/O TEST I/O HALT I/O TEST CHAN	KE001 KE001 KE001 KE001	0-3	The CPU generated I/O instruction turns on the appropriate indicator - Start I/O, Test I/O, Halt I/O, or Test Chan. The indicator is on until the channel responds.
CHAN NUMBER 4	KE021	4-6	Selected channel number in binary.
CHAN NUMBER 2	KE021		
CHAN NUMBER 1	KE021		
INSTR REPLY 0	KE051	7-10	Indicates the condition code with which the channel responded to an I/O instruction.
INSTR REPLY 1	KE051		
INSTR REPLY 2	KE061		
INSTR REPLY 3	KE061		
REPLY	KE071	11	Reply is on when a reply to an instruction is received from a channel.
BCHI	KE141	12	Branch on channel interrupt is on whenever an unmasked channel wants to interrupt. The latch is checked by the microprogram during I - fetch
PRCD ON IRPT	KE101	13	Proceed on interrupt is turned on by a signal from CPU in reply to BCHI.
TIME OUT	KE091	14	Time out is on after an I/O instruction or proceed on interrupt is given to the channel and CPU has not received a reply for 74 usec.
TIME OUT CHK	KE091	15	Time out check is on if an answer is not received from the channel after time out.
FOUL	KE091	16	Foul is on if there is a program check on a start I/O instruction that is detected by CPU microprogram.
		17-35	Not used.

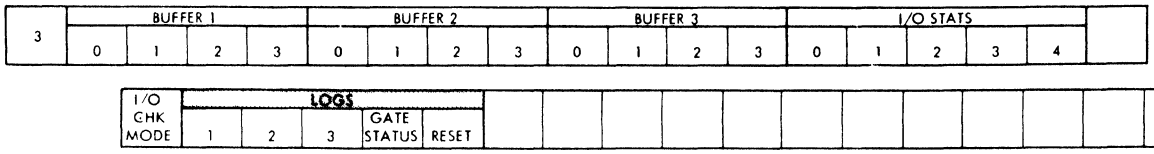
FIGURE 137. COMMON CHANNEL ROLLER - POSITION 1

2	RTNE RECD	PCI ENABL	BREAK IN	I/O RTNE	EARLY FIRST CYCLE	FIRST CYCLE	CHAIN FIRST CYCLE	LS RD	LS WR	CHAL DTC	ALCH DTC	CHAIN	LAST CYCLE	BREAK OUT	SBCR 0	SBCR 1	SBCR 2	SBCR 3

	ROS BITS 33	ROS BITS 34	ROS BITS 47	ROS BITS 48	FIRST CYCLE CHK													2

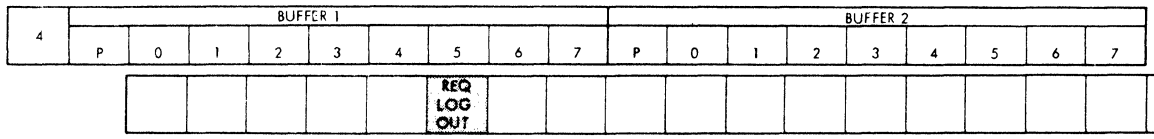
Indicator	ALD	Bit Position	Description
RTNE RCVD	KE301	0	Routine received is on when a request to break into CPU is granted.
PCI ENABL	KE131	1	PCI enable is on during a PCI routine.
BREAK IN	KE301	2	Break in is on after a routine received signal has been received and break in is occurring.
I/O RTNE	KE311	3	I/O routine is on whenever an I/O routine is being processed.
EARLY FIRST CYC	KE301	4	Early first cycle is on early in the first cycle of an I/O routine.
FIRST CYC	KE301	5	First cycle is on during the first cycle of an I/O routine.
CHAIN FIRST CYC	KE321	6	Chain first cycle is on during the first cycle of a chained routine. (One routine is finished and the next started without CPU breaking in.)
LS RD	KE471	7	Local store read is on during a local store read routine when data is transferred from the B register to the local store buffer.
LS WR	KE471	8	Local store write is on during a local store write routine when data is transferred from the local store buffer to the B register.
CHAL DTC	KE441	9	Channel to adder latch data transfer and control is on when the micro-order is given telling a selector channel to transfer information from the channel to the adder latch.
ALCH DTC	KE441	10	Adder latch to channel data transfer and control is on when the micro-order is given telling a selector channel to transfer information from the adder latch to the channel.
CHAIN	KE321	11	Chain is on during the last cycle of a routine and indicates that another routine is to be chained into.
LAST CYC	KE321	12	Last cycle is on during the last cycle of a routine and indicates that chaining to another routine will not occur.
BREAK OUT	KE321	13	Break out is on when a routine is completed and CPU and ROS are restored to the point they were at before break in.
SBCR 0	KE381	14-17	Storage byte control register is used by the selector channel to designate the bytes that are to be placed placed in storage during a read store.
SBCR 1	KE381		
SBCR 2	KE381		
SBCR 3	KE381		
		18	Not Used
ROS BITS 33	KE441	19-20	ROS bits 33 and 34 represent timing signals to the channel (I/O mode).
ROS BITS 34	KE441		
ROS BITS 47	KE321	21-22	ROS bits 47 and 48 represent control signals to the channel (I/O mode).
ROS BITS 48	KE321		
FIRST CYC CHK	KE531	23	First cycle check is made during the first cycle to make sure that ROS is really in the first cycle of an I/O routine.
		24-35	Not used.

FIGURE 138. COMMON CHANNEL ROLLER - POSITION 2



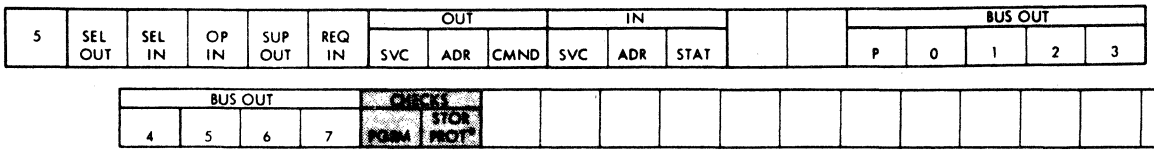
Indicator	ALD	Bit Position	Description
BUFFER 1 0	KE341	0-11	The buffer registers indicate the channels using the CPU. They are used to gate control information and errors to the channel.
BUFFER 1 1	KE341		
BUFFER 1 2	KE351		
BUFFER 1 3	KE351		
BUFFER 2 0	KE341		
BUFFER 2 1	KE341		
BUFFER 2 2	KE351		
BUFFER 2 3	KE351		
BUFFER 3 0	KE341		
BUFFER 3 1	KE341		
BUFFER 3 2	KE351		
BUFFER 3 3	KE351		
I/O STATS 0	KE151	12-16	I/O stats indicate the condition of the five I/O stats that set conditions for microprogram branching. They are set by the selector channel on break-in.
I/O STATS 1	KE161		
I/O STATS 2	KE171		
I/O STATS 3	KE181		
I/O STATS 4	KE191		
		17	Not used.
I/O CHK MODE	KE311	18	I/O check mode is on to indicate that the channel is using CPU and any errors detected in the CPU could be caused by the channel.
LOGS 1	KE661	19-21	Log 1, 2, or 3 indicates the number of the selector channel that is being logged.
LOGS 2	KE661		
LOGS 3	KE661		
GATE STATUS	KE671	22	Log gate status is on after a logout allowing the channel that was logged to gate its status to CPU.
RESET	KE671	23	Log reset is on after the gate stat has been turned off to provide a reset to the channel that was logged.
		24-35	Not used.

FIGURE 139. COMMON CHANNEL ROLLER--POSITION 3



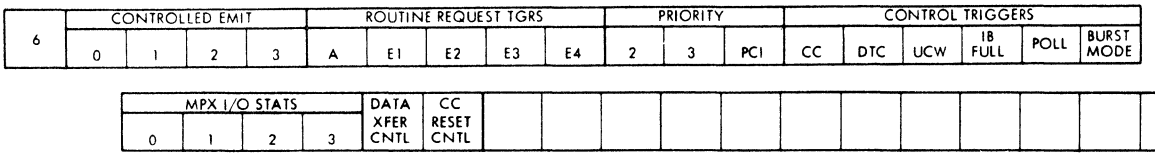
Indicator	ALD	Bit Position	Description
BUFFER 1 P	FA011	0-8	Contents of buffer 1 plus parity.
BUFFER 1 0	FA011		
BUFFER 1 1	FA011		
BUFFER 1 2	FA021		
BUFFER 1 3	FA021		
BUFFER 1 4	FA021		
BUFFER 1 5	FA031		
BUFFER 1 6	FA031		
BUFFER 1 7	FA031		
BUFFER 2 P	FA011	9-17	Contents of buffer 2 plus parity.
BUFFER 2 0	FA011		
BUFFER 2 1	FA011		
BUFFER 2 2	FA021		
BUFFER 2 3	FA021		
BUFFER 2 4	FA021		
BUFFER 2 5	FA031		
BUFFER 2 6	FA031		
BUFFER 2 7	FA031		
REQ LOG OUT	FA341	23	Request log out indicates an error in the multiplexor channel is conditioning a log out request.
		24-35	Not used.

FIGURE 140. MULTIPLEX CHANNEL ROLLER--POSITION 4



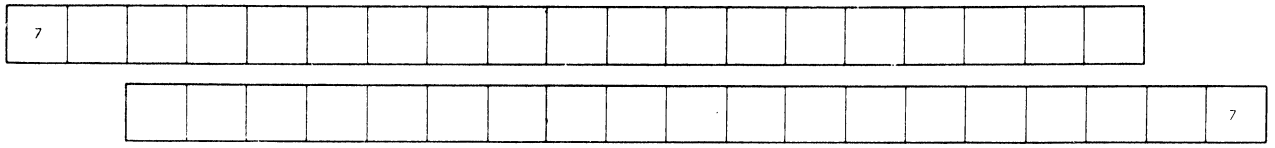
Indicator	ALD	Bit Position	Description
SEL OUT	FA141	0	Indicates when select out is up on the interface.
SEL IN	FA361	1	Indicates when select in is up on the interface.
OP IN	FA361	2	Indicates when op in is up on the interface.
SUP IN	FA151	3	Indicates when suppress out is up on the interface.
REQ IN	FA361	4	Indicates when request in is up on the interface.
SVC OUT	FA141	5	Indicates when service out is up on the interface.
ADR OUT	FA131	6	Indicates when address out is up on the interface.
CMND OUT	FA141	7	Indicates when command out is up on the interface.
SVC IN	FA351	8	Indicates when service in is up on the interface.
ADR IN	FA351	9	Indicates when address in is up on the interface.
STAT IN	FA351	10	Indicates when status in is up on the interface.
		11-12	Not used.
BUS OUT P	FA051	13-21	Displays the information that is on bus out plus parity.
BUS OUT 0	FA051		
BUS OUT 1	FA051		
BUS OUT 2	FA051		
BUS OUT 3	FA051		
BUS OUT 4	FA051		
BUS OUT 5	FA051		
BUS OUT 6	FA051		
BUS OUT 7	FA051		
PRGM CHK	FA371	22	Program check indicates a boundary violation in storage.
STOR PROT CHK	FA371	23	Storage protect check indicates that data is trying to be stored in a protected storage location and the keys do not match.
		24-35	Not used.

FIGURE 141. MULTIPLEX CHANNEL ROLLER - POSITION 5



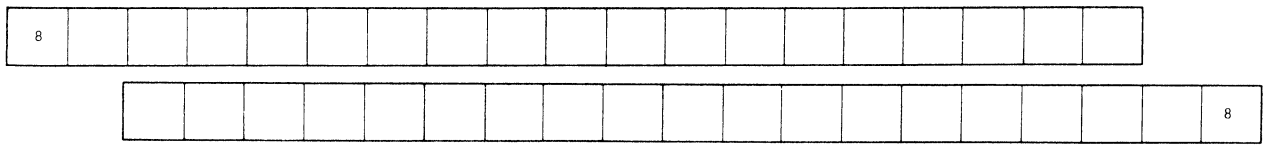
Indicator	ALD	Bit Position	Description
CONTROLLED EMIT 0	FA063	0-3	Controlled emit indicates the contents of the ROS emit field at the time a DTC is issued.
CONTROLLED EMIT 1	FA063		
CONTROLLED EMIT 2	FA063		
CONTROLLED EMIT 3	FA063		
RTNE REQ TGRS A	FA171	4-8	Indicates the address of the first microinstruction of the routine requested or of the routine presently being run.
RTNE REQ TGRS E1	FA171		
RTNE REQ TGRS E2	FA171		
RTNE REQ TGRS E3	FA171		
RTNE REQ TGRS E4	FA171		
PRIORITY 2	FA261	9-10	Indicates the priority of the routine requested.
PRIORITY 3	FA261		
PCI	FA261	11	Indicates a request for a PCI routine.
CTRL CC	FA251	12	Indicates that the UCW the channel is working with contains a CC flag.
CTRL DTC	FA261	13	Indicates when a micro-order DTC timing signal is given to request the next routine.
CTRL UCW	FA251	14	Indicates when a device disconnects from the interface that a new count word and data address word are to be stored in the UCW in bump.
CTRL IB FULL	FA331		
CTRL POLL	FA341	15	Indicates whenever there is an interrupt pending in the channel.
CTRL BURST MODE	FA311	16	Indicates whenever the channel is idle (poll state).
		17	Indicates the multiplexor channel interface is operating in the burst mode.
MPX I/O STATS 0	FA091	18-21	Indicates the condition of the multiplexor I/O stats used for microprogram branching.
MPX I/O STATS 1	FA101		
MPX I/O STATS 2	FA111		
MPX I/O STATS 3	FA121		
DATA XFR CTRL	FA071	22	Indicates a byte of data is being transferred in either direction over the interface.
CC RESET CTRL	FA252	23	Indicates the presence of a signal to reset the command chain flag because of an error condition.
		24-35	Not used.

FIGURE 142. MULTIPLEX CHANNEL ROLLER - POSITION 6



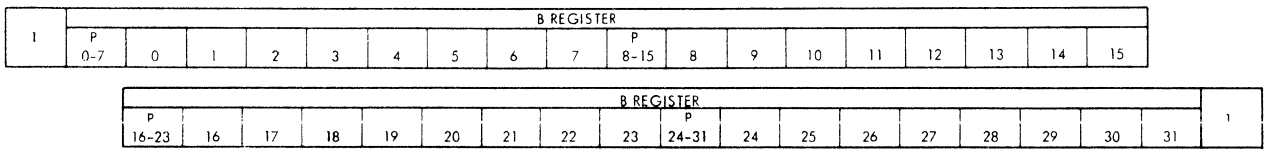
Indicator	ALD	Bit Position	Description
		0-35	Not used.

FIGURE 143. MULTIPLEX CHANNEL ROLLER - POSITION 7



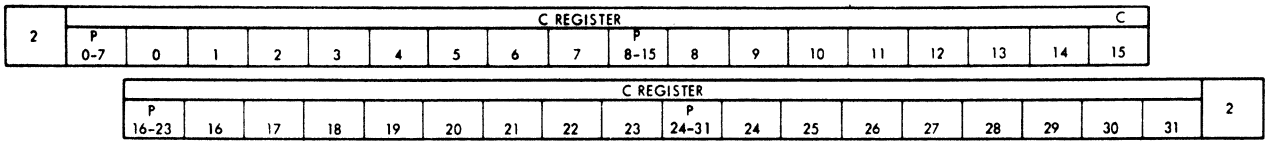
Indicator	ALD	Bit Position	Description
		0-35	Not used.

FIGURE 144. MULTIPLEX CHANNEL ROLLER - POSITION 8



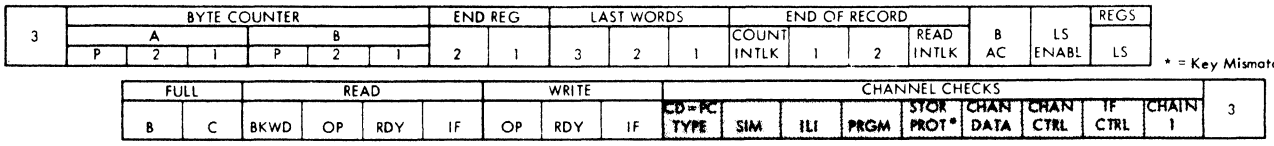
Indicator	ALD	Bit Position	Description
P 0- 7	GH101	0-35	Word 1 position of the selector channel roller select switch displays the contents of the B register. Bit positions 0, 9, 18, and 27 display the parity of the associated byte. The B register is connected on one side to the CPU adder latch and on the other to the C register.
0	GH111		
1	GH121		
2	GH131		
3	GH141		
4	GH151		
5	GH161		
6	GH171		
7	GH161		
P 8-15	GJ101		
8	GJ111		
9	GJ121		
10	GJ131		
11	GJ141		
12	GJ151		
13	GJ161		
14	GJ171		
15	GJ181		
P16-23	GK101		
16	GK111		
17	GK121		
18	GK131		
19	GK141		
20	GK151		
21	GK161		
22	GK171		
23	GK181		
P24-31	GL101		
24	GL111		
25	GL121		
26	GL131		
27	GL141		
28	GL151		
29	GL161		
30	GL171		
31	GL181		

FIGURE 145. SELECTOR CHANNEL ROLLER - POSITION 1



Indicator	ALD	Bit Position	Description
P 0- 7	GH101	0-35	Word 2 position of the selector channel roller select switch displays the contents of the C register. Bit positions 0, 9, 18, and 27 display the parity of the associated byte. The C register ties directly to the interface for byte assembly and disassembly.
0	GH111		
1	GH121		
2	GH131		
3	GH141		
4	GH151		
5	GH161		
6	GH171		
7	GH181		
P 8-15	GJ101		
8	GJ111		
9	GJ121		
10	GJ131		
11	GJ141		
12	GJ151		
13	GJ161		
14	GJ171		
15	GJ181		
P16-23	GK101		
16	GK111		
17	GK121		
18	GK131		
19	GK141		
20	GK151		
21	GK161		
22	GK171		
23	GK181		
P24-31	GL101		
24	GL111		
25	GL121		
26	GL131		
27	GL141		
28	GL151		
29	GL161		
30	GL171		
31	GL181		

FIGURE 146. SELECTOR CHANNEL ROLLER - POSITION 2



Indicator	ALD	Bit Position	Description
BYTE CTR A P	GR131	0-2	Byte counter phase A and parity.
BYTE CTR A 2	GR131		
BYTE CTR A 1	GR131		
BYTE CTR B P	GR131	3-5	Byte counter phase B and parity.
BYTE CTR B 2	GR131		
BYTE CTR B 1	GR131		
END REG 2	GC111	6-7	The end register points to the last byte plus one to be transferred.
END REG 1	GC111		
LAST WORDS 3	GC141	8-10	The last word latches control the last three words in a read or write routine.
LAST WORDS 2	GC141		
LAST WORDS 1	GC141		
EOR CNT INTLK	GC151	11	Count interlock indicates when the channel has stored the fourth from the last word in a read operation or has fetched the last word in a write operation.
EOR 1	GC151	12	End of record 1 indicates when the interface is using the last word latches.
EOR 2	GC151	13	End of record 2 indicates when the external channel controls are using the last word latches.
EOR RD INTLK	GC151	14	EOR read interlock indicates when the interface logic has finished using the last word latches and is requesting the external channel control to take over.
BAC	GG131	15	'B register almost changed' indicates that local store is being bypassed in the data transfer path.
LS ENABL	GG131	16	Local Store enable indicates that data will be transferred between local store and the B register.
REG FULL LS	GC171	17-19	Indicate when local store, the B register, or the C register contain data.
REG FULL B	GC171		
REG FULL C	GT141		
READ BKWD	GC131	20	Read backward indicates a read backward op has been decoded.
READ OP	GC131	21	Read op indicates a read type op has been decoded.
READ RDY	GF161	22	Read ready indicates that the channel is performing a read type op and is permitted to make data store requests.
READ IF	GT121	23	Read interface indicates that the interface is now ready to read.
WRITE OP	GC131	24	Write op indicates a write type op has been decoded.
WRITE RDY	GF161	25	Write ready indicates that the channel is performing a write type op and is permitted to make data fetch requests.
WRITE IF	GT121	26	Write interface indicates that the interface is now ready to write.
CHAN CHKS CD=PC TYPE	GE111	27	CD=PC type check indicates a program check during a write data chaining CCW fetch sequence.
CHAN CHKS SIM	GG131	28	Simulated check indicates that the channel will interrupt without the unit's status.
CHAN CHKS ILI	GE111	29	Incorrect length indicates that the number of bytes contained in the storage areas assigned is not equal to the number requested or offered.
CHAN CHKS PGRM	GE111		
CHAN CHKS STOR PROT	GE111	30	Program check indicates that the channel has detected a program error.
CHAN CHKS CHAN DATA	GE111	31	Storage protect check indicates that the associated protect keys do not match.
CHAN CHKS CHAN CTRL	GE101	32	Channel data check indicates when an error is detected on any data transfer to or from an I/O device.
CHAN CHKS IF CTRL	GE101	33	Channel control check indicates when there is any machine malfunction that affects channel controls.
CHAN CHKS CHAIN 1	GE111	34	Interface control check indicates when there was an invalid signal combination or sequence on the interface.
		35	Chaining check indicates when there is a channel overrun. (channel assumed a wrong starting address or count while waiting for the information - during input chaining operations only.)

FIGURE 147. SELECTOR CHANNEL ROLLER - POSITION 3

4	POSITION REGISTER									CYCLE COUNTER PHASE A STEP				CLOCK				
	UA FETCH	CCW1 TYPE	CCW2 TYPE	UNIT SEL	RD STORE	WR FETCH	END UP	COMP	IRPT	0	1	2	3	A0	A1	STEP	LS REQ	PCI REQ

REQUEST REGISTER														COMMON CHAN DETECT					
PRIORITY										STAT					PRI	PRI		INH	4
1	2	3	0	1	2	3	4	5		0	1	2	3	LS	1	2-3	PCI	RTNE	

Indicator	ALD	Bit Position	Description
UA FETCH	GB181	0-8	The position register indicates the routine the channel is processing or has done last. The nine indicators are: UA, Fetch, CCW 1 Type, CCW 2 Type, Unit Sel, Rd Store, Wr Fetch, End Up, Comp, and Irpt.
CCW1 TYPE	GB181		
CCW2 TYPE	GB181		
UNIT SEL	GB181		
RD STORE	GB181		
WR FETCH	GB181		
END UP	GB181		
COMPARE	GB181		
INTERRUPT	GB181		
CYCLE CTR PHASE A STEP 0	GA131	9-12	The cycle counter indicates the number of times the A clock has cycled through in a particular routine.
CYCLE CTR PHASE A STEP 1	GA131		
CYCLE CTR PHASE A STEP 2	GA131		
CYCLE CTR PHASE A STEP 3	GA131		
CLOCK A0	GA111	13-15	Indicates the position the A clock is presently in.
CLOCK A1	GA111		
CLOCK STEP	GA111		
LS REG	GG101	16	Local store request indicates when local store data is requested.
PCI REQ	GG181	17	Program controlled interrupt request indicates that a maskable type of interrupt is being requested.
PRIORITY 1	GB141	18-20	Indicates the priority of the routine requested.
PRIORITY 2	GB141		
PRIORITY 3	GB151		
REQUEST REG 0	GB101	21-26	The request register, in conjunction with the selected priority, identifies the routine being requested by the channel.
REQUEST REG 1	GB101		
REQUEST REG 2	GB101		
REQUEST REG 3	GB101		
REQUEST REG 4	GB111		
REQUEST REG 5	GB111		
STATS 0	GB131	27-30	Indicates the I/O stats used for microprogram branching in the requested routine.
STATS 1	GB121		
STATS 2	GB121		
STATS 3	GB131		
COM CHAN DETECT LS	GA030	31-34	Indicates that the common channel has detected a routine request from the channel.
COM CHAN DETECT PRI 1	GA030		
COM CHAN DETECT PRI 2-3	GA030		
COM CHAN DETECT PCI	GA030		
COM CHAN DETECT INH RTNE	GA030	35	Indicates that the detect registers (Pri 1, 2, 3, PCI) are inhibited from being set.

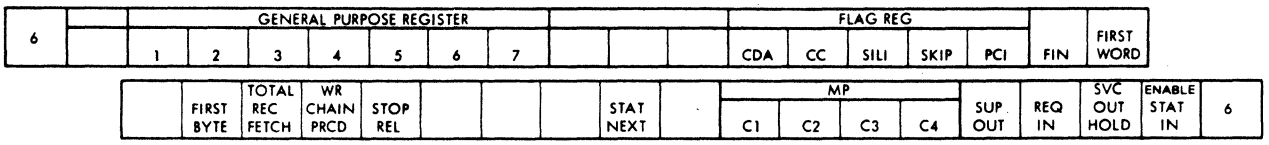
FIGURE 148. SELECTOR CHANNEL ROLLER - POSITION 4

5	POS REG TRF	INH RD STOR	A CLOCK				SP		INSN SCAN	CHAN IN USE	POLL	POLL IRPT END	INSN INH	BC RDY	UA TO BUS = 0	U SEL ADR OUT	COMPARE	
			A	B	C	D	D1	D2									=	≠

	STOP	IF CDA FIRST BYTE	CD	BC MOD ENABL	WR CHAIN RDY	REC END	OP IN TEST	CHAN STOP	SEL OUT	STOP RTNE	SEL IN	OP IN	OUT			IN			5
													SVC	ADR	CMND	SVC	ADR	STAT	

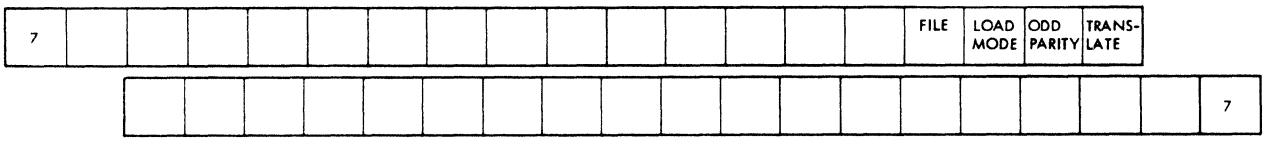
Indicator	ALD	Bit Position	Description
POS REG TRF	GB171	0	Position register transfer indicates that a routine was transferred from the request to the position register but has not yet been serviced.
INH RD STOR	GG131	1	Inhibit read store indicates that the channel will inhibit storing of extra data on an overrun when chaining.
A CLOCK A	GA101	2-5	Displays the A clock latches that control the A clock.
A CLOCK B	GA101		
A CLOCK C	GA101		
A CLOCK D	GA101		
SP D1	GA161	6	Selector channel D1 special purpose latch is used to set program check if a CCW specifying a TIC addresses another CCW that also specifies a TIC.
SP D2	GA161	7	Selector channel D2 special purpose latch is used for request compare routine in a test I/O operation.
INSN SCAN	GF111	8	Instruction scan indicates that the channel is idle and ready to perform an operation.
CHAN IN USE	GF111	9	Channel in use indicates the channel is performing an operation.
POLL	GR121	10	Poll indicates the channel is polling the interface due to a request in.
POLL IRPT END	GR121	11	Poll interrupt end indicates that every thing needed from the selected unit has been received and the CPU is now to be interrupted.
INSN INH	GD131	12	Instruction inhibit is on when the channel is fetching a CCW (other than initial) and is used to prevent any instruction line from affecting a unit selection.
BC RDY	GF141	13	Byte counter ready indicates that the new byte counter value has been obtained from a CCW.
UA TO BUS = 0	GV121	14	Unit address to bus out indicates when, in the unit select routine, bus out contains the unit address.
UNIT SEL ADR OUT	GV121	15	Unit select address out indicates when the address out line is active on the interface during the unit select routine.
COMPARE =	GR151	16-17	Compare equal or not equal indicates the compare result between the address sent out on the interface and the address received back during unit selection.
COMPARE ≠	GR151		
STOP	GV101	18	Stop indicates when the interface stop trigger is on.
IF CDA FIRST BYTE	GT161	19	Interface CDA first byte places the first byte of the new record into all bytes of the C register if it has been received before a new value for the byte counter has been obtained from the CCW.
CD	GF111	20	The chain data latch is used during data chaining to differentiate between a CCW requiring a unit selection and one that does not.
BC MOD ENABL	GR141	21	Byte counter mod enable indicates when the interface controls permit the channel to modify the byte counter.
WR CHAIN RDY	GF161	22	Write chain ready indicates when a new CCW is completely fetched during data chaining.
REC END	GF111	23	Record end indicates the end of any operation.
OP IN TEST	GR101	24	Operational in test indicates if op in falls during the period that select out is up.
CHAN STOP	GE121	25	Channel stop condition indicates the channel is unable to continue operation.
SEL OUT	GR101	26	Indicates when select out is up on the interface.
STOP RTNE	GV101	27	Stop routine indicates an interface stop sequence.
SEL IN	GS121	28	Indicates when select in is up on the interface.
OP IN	GS121	29	Indicates when operational in is up on the interface.
SVC OUT	GS131	30	Indicates when service out is up on the interface.
ADR OUT	GS131	31	Indicates when address out is up on the interface.
CMND OUT	GS131	32	Indicates when command out is up on the interface.
SVC IN	GS111	33	Indicates when service in is up on the interface.
ADR IN	GS111	34	Indicates when address in is up on the interface.
STAT IN	GS111	35	Indicates when status in is up on the interface.

FIGURE 149. SELECTOR CHANNEL ROLLER - POSITION 5



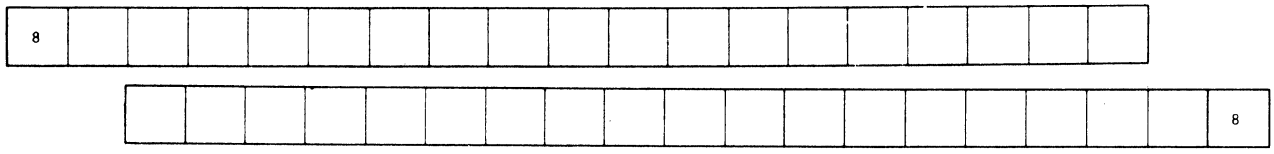
Indicator	ALD	Bit Position	Description
GENERAL PURPOSE REG 1	GC101	1-7	The general purpose register is used as a buffer for pre-fetched and control information and for byte control on input data.
GENERAL PURPOSE REG 2	GC101		
GENERAL PURPOSE REG 3	GC101		
GENERAL PURPOSE REG 4	GC101		
GENERAL PURPOSE REG 5	GC121		
GENERAL PURPOSE REG 6	GC121		
GENERAL PURPOSE REG 7	GC121		
		8-10	Not used.
FLAG REG CDA	GC161	11-15	The flag register indicates when the associated flag bit in the CSW is active.
FLAG REG CC	GC161		
FLAG REG SILI	GC161		
FLAG REG SKIP	GC161		
FLAG REG PCI	GC161		
FINISH	GB161	16	Finish indicates the end of each routine.
FIRST WORD	GF161	17	First word remains on until the first word in the record is stored or fetched.
		18	Not used.
FIRST BYTE	GF161	19	First byte remains on until the first byte is received on the interface.
TOTAL REC FETCH	GF111	20	Total record fetch indicates that a CCW and its data have been completely pre-fetched on a write data chain operation.
WR CHAIN PRCD	GT131	21	Write chain proceed indicates when the data under control of the previous CCW has been completely transmitted.
STOP REL	GV111	22	Stop release drops select out and ends an interface sequence.
		23-25	Not used.
STAT NEXT	GT161	26	The status next latch represents special program check conditions that should block the setting of incorrect length.
		27	Not used.
MP C1	GA141	28-31	The multipurpose latches (C1, C2, C3, C4) indicate specific conditions during execution of an I/O routine.
MP C2	GA141		
MP C3	GA151		
MP C4	GA151		
SUP OUT	GS131	32	Suppress out indicates the suppress out line is up on the interface.
REQ IN	GS141	33	Indicates request in is up on the interface.
SVC OUT HOLD	GV151	34	Service out hold indicates the channel is holding service out up until it has the first word ready to send over the interface.
ENABLE STAT IN	GS111	35	Enable status in indicates the channel may receive status in.

FIGURE 150. SELECTOR CHANNEL ROLLER - POSITION 6



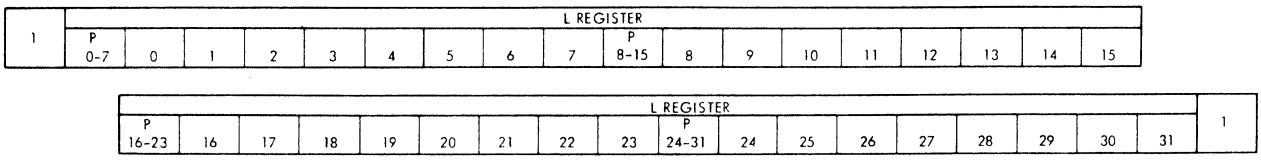
Indicator	ALD	Bit Position	Description
		0-13	Not used.
FILE	XE501	14	Set from CAW bit 7 for 1410 file to/from EBCDIC-II code translation during I/O data transfers.
LOAD MODE	XE501	15	Set from CAW bit 6 for 1410 I/O operations that involve changing the wordmark bit.
ODD PARITY	XE501	16	Set from CAW bit 4 for 1410 I/O operations with an odd parity tape code.
TRANSLATE	XE521	17	Set from CCW bit 38 to activate the selector channel translator control circuits during I/O data transfers in 1410 mode.
		18-35	Not used.

FIGURE 151. SELECTOR CHANNEL ROLLER - POSITION 7



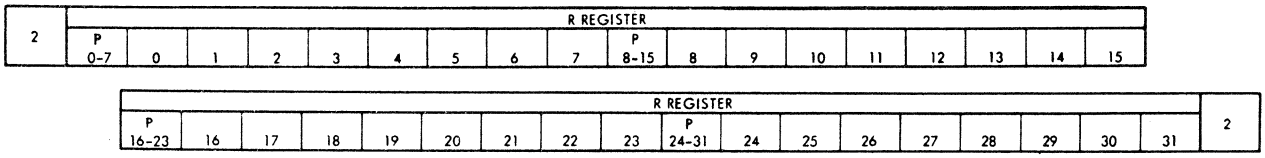
Indicator	ALD	Bit Position	Description
		0-35	Not used.

FIGURE 152. SELECTOR CHANNEL ROLLER - POSITION 8



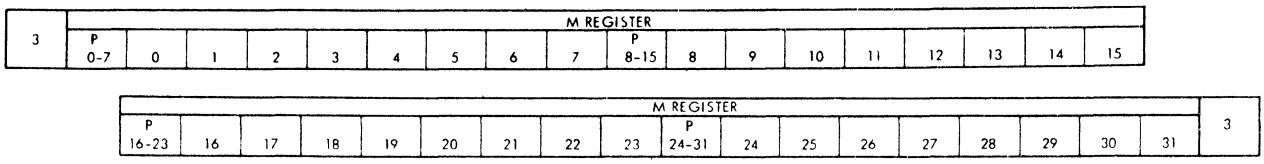
Indicator	ALD	Bit Position	Description
P 0- 7	RL001		
0	RL001		
1	RL001		
2	RL001		
3	RL001		
4	RL011		
5	RL011		
6	RL011		
7	RL011		
P 8-15	RL021		
8	RL021		
9	RL021		
10	RL021		
11	RL021		
12	RL031		
13	RL031		
14	RL031	0-35	Word 1 indicators display the contents of the L register. The L register is a primary source of data for adder XG input and buffer for local store. The L register can also gate a byte of data at a time to the mover. Bit positions 0, 9, 18, and 27 display the parity of the associated byte.
15	RL031		
P16-23	RL041		
16	RL041		
17	RL041		
18	RL041		
19	RL041		
20	RL051		
21	RL051		
22	RL051		
23	RL051		
P24-31	RL061		
24	RL061		
25	RL061		
26	RL061		
27	RL061		
28	RL071		
29	RL071		
30	RL071		
31	RL071		

FIGURE 153. CPU 1 ROLLER - POSITION 1



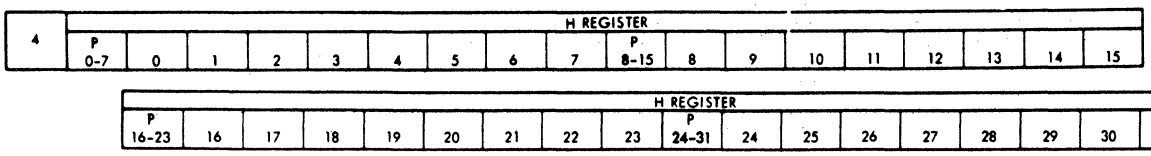
Indicator	ALD	Bit Position	Description
P 0- 7	RR001		
0	RR001		
1	RR001		
2	RR001		
3	RR001		
4	RR011		
5	RR011		
6	RR011		
7	RR011		
P 8-15	RR021		
8	RR021		
9	RR021		
10	RR021		
11	RR021		
12	RR031		
13	RR031	0-35	Word 2 indicators display the contents of the R register. The R register is a primary source of data for adder Y input and buffer for local store. The R register can also gate a byte of data to the mover. Parity is displayed in bit positions 0, 9, 18, and 27.
14	RR031		
15	RR031		
P16-23	RR041		
16	RR041		
17	RR041		
18	RR041		
19	RR041		
20	RR051		
21	RR051		
22	RR051		
23	RR051		
P24-31	RR061		
24	RR061		
25	RR061		
26	RR061		
27	RR061		
28	RR071		
29	RR071		
30	RR071		
31	RR071		

FIGURE 154. CPU 1 ROLLER - POSITION 2



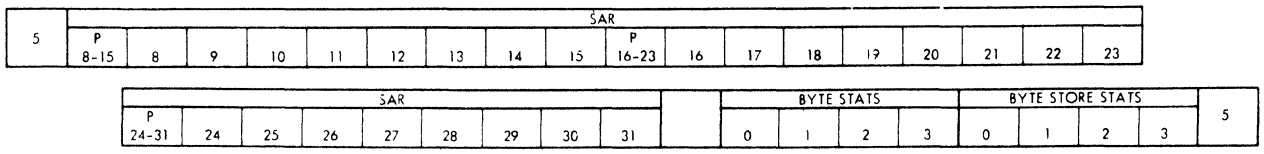
Indicator	ALD	Bit Position	Description
P 0- 7	RM001		
0	RM001		
1	RM001		
2	RM001		
3	RM001		
4	RM011		
5	RM011		
6	RM011		
7	RM011		
P 8-15	RM021		
8	RM021		
9	RM021		
10	RM021		
11	RM021		
12	RM031		
13	RM031	0-35	Word 3 indicators display the contents of the M register. The M register is an alternate source of data for adder Y input and can gate its four bytes to the mover V input. Parity is displayed in bit positions 0, 9, 18, and 27.
14	RM031		
15	RM031		
P16-23	RM041		
16	RM041		
17	RM041		
18	RM041		
19	RM041		
20	RM051		
21	RM051		
22	RM051		
23	RM051		
P24-31	RM061		
24	RM061		
25	RM061		
26	RM061		
27	RM061		
28	RM071		
29	RM071		
30	RM071		
31	RM071		

FIGURE 155. CPU 1 ROLLER - POSITION 3



Indicator	ALD	Bit Position	Description
P 0- 7	RH001		
0	RH001		
1	RH001		
2	RH001		
3	RH001		
4	RH011		
5	RH011		
6	RH011		
7	RH011		
P 8-15	RH021		
8	RH021		
9	RH021		
10	RH021		
11	RH021		
12	RH031		
13	RH031	0-35	Word 4 indicators display the contents of the H register. The H register is an alternate source of data for adder Y input. Parity is displayed in bit positions 0, 9, 18, and 27.
14	RH031		
15	RH031		
P16-23	RH041		
16	RH041		
17	RH041		
18	RH041		
19	RH041		
20	RH051		
21	RH051		
22	RH051		
23	RH051		
P24-31	RH061		
24	RH061		
25	RH061		
26	RH061		
27	RH061		
28	RH071		
29	RH071		
30	RH071		
31	RH071		

FIGURE 156. CPU 1 ROLLER - POSITION 4



Indicator	ALD	Bit Position	Description
P 8-15	RA061	0-26	The storage address register is used for addressing main and bump storage. Bit positions 0, 9, and 18 display the parity of the associated byte.
8	RA003		
9	RA003		
10	RA002		
11	RA002		
12	RA002		
13	RA002		
14	RA001		
15	RA011		
P16-23	RA061		
16	RA011		
17	RA011		
18	RA011		
19	RA011		
20	RA021		
21	RA021		
22	RA021		
23	RA021		
P24-31	RA061		
24	RA021		
25	RA031		
26	RA031		
27	RA031		
28	RA031		
29	RA031		
30	RA061		
31	RA061		
		27	Not used.
BYTE STATS 0	KS001	28-31	Indicates byte stats 0, 1, 2, and 3
BYTE STATS 1	KS001		
BYTE STATS 2	KS001		
BYTE STATS 3	KS011		
BYTE STORE STATS 0	KS021	32-35	Indicates byte store stats 0, 1, 2, and 3.
BYTE STORE STATS 1	KS021		
BYTE STORE STATS 2	KS031		
BYTE STORE STATS 3	KS031		

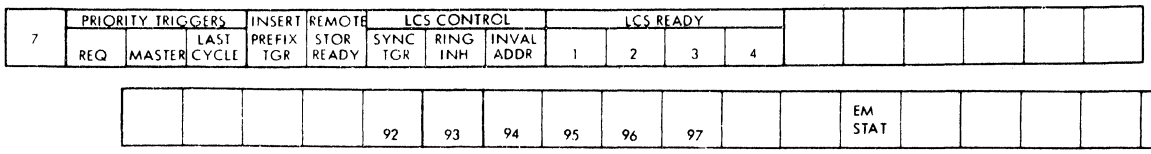
FIGURE 157. CPU 1 ROLLER - POSITION 5

6	ROS P	CE				LX			TC	RY			AD						
													CL						
	57-89	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	

	AB				BB					UX	SS								6
	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89			

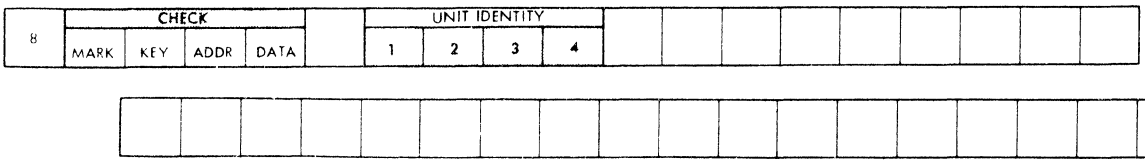
Indicator	ALD	Bit Position	Description
ROS P57-89	RK301	0	Parity of bits 57-89.
CE 57	RK301	1-4	Emit field.
CE 58	RK301		
CE 59	RK301		
CE 60	RK301		
LX 61	RK311	5-7	Left input to adder (XG).
LX 62	RK311		
LX 63	RK311		
TC 64	RK311	8	True or complement to left adder input (XG).
RY 65	RK311	9-11	Right input to adder (Y).
RY 66	RK311		
RY 67	RK311		
AD CL 68	BH061		
AD CL 69	BH061	12-15	Adder function (CPU mode).
AD CL 70	BH061	12-14	Selector channel adder latch tests (I/O mode).
AD CL 71	BH061	15	Spare position (I/O mode).
AB 72	RK331	16-21	Condition branch test A (furnishes bit 11 of next ROS address).
AB 73	RK331		
AB 74	RK331		
AB 75	RK331		
AB 76	RK331		
AB 77	RK331		
BB 78	RK341	22-26	Condition branch test B (furnishes bit 12 of next ROS address).
BB 79	RK341		
BB 80	RK341		
BB 81	RK341		
BB 82	RK341		
83	XG401	27	Used in 1410 compatibility feature to expand the UR field (54-55) for control of the decimal adder in the mover circuits.
SS 84	RK351	28-33	Stat setting and micellaneous control.
SS 85	RK351		
SS 86	RK351		
SS 87	RK351		
SS 88	RK351		
SS 89	RK351		
		34-35	Not used.

FIGURE 158. CPU 1 ROLLER - POSITION 6



Indicator	ALD	Bit Position	Description
PRIORITY { REG, MASTER, LAST CYCLE }		0-2	
INSERT PREFIX TGR		3	
REMOTE STORE READY		4	
LCS CONTROL { SYNC TGR / RING INH / INVAL ADDR }	KT272 / KT272 / BH131	5-7	
LCS READY { 1, 2, 3, 4 }	BH131	8-11	
		12-21	Not used.
ROSDR { 92, 93, 94, 95, 96, 97 }	XF001	22-27	CPU Mode: ROSDR 92-97 are the Y-input to the adder during 1410 compatibility feature address conversion. I/O Mode: ROSDR 92-94 are used to set selector channel translator controls for 1410 compatibility feature I/O operations.
		28-29	Not used.
EM STAT	XF501	30	
		31-35	Not used.

FIGURE 159. CPU 1 ROLLER - POSITION 7



Indicator	ALD	Bit Position	Description
CHECK { MARK, KEY, ADDR, DATA }	BH132	0-3	
		4	Not used.
UNIT IDENTITY { 1, 2, 3, 4 }	BH132	5-8	
		9-35	Not used.

FIGURE 160. CPU 1 ROLLER - POSITION 8

	ROS P 1-30	LU			MV		ZP						ZF				ZN	
1		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

ZN		TR					ZR	WS			SF						
18		19	20	21	22	23	24	CS 25	SA 26	27	28	29	30				1

Indicator	ALD	Bit Position	Description
ROS P1-30	BH091	0	Parity of bits 1-30.
LU 1	RK121	1-3	Left input to mover (U).
LU 2	RK121		
LU 3	RK121		
MV 4	RK121	4-5	Right input to mover (V).
MV 5	RK121		
ZP 6	KK301	6-11	Bits 1-6 of next ROS address.
ZP 7	KK301		
ZP 8	KK311		
ZP 9	KK311		
ZP 10	KK321		
ZP 11	KK301		
ZF 12	KK001	12-15	Source of bits 7-10 of next ROS address.
ZF 13	KK001		
ZF 14	KK001		
ZF 15	KK001		
ZN 16	KK003	16-18	ROS addressing mode.
ZN 17	KK003		
ZN 18	KK003		
		19	Not used
TR 19	RK101	20-24	Destination of adder latch contents.
TR 20	RK101		
TR 21	RK101		
TR 22	RK101		
TR 23	RK101		
		25	Not used.
WS CS- 25	RK111	26-28	Local store address control.
WS CS- 26	RK111	26	Local store address sector (I/O mode).
WS SA 27	RK111	27-28	Local store address (I/O mode).
SF 28	RK111	29-31	Local store function.
SF 29	RK111		
SF 30	RK111		
		32-35	Not used.

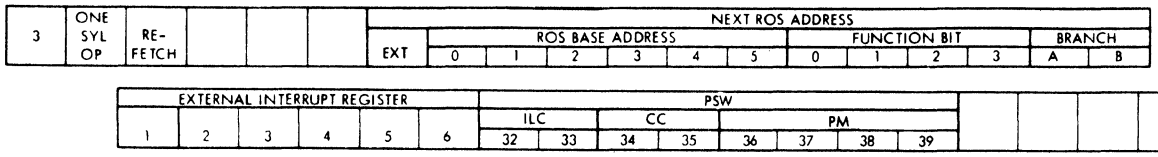
FIGURE 161. CPU 2 ROLLER - POSITION 1

	ROS P 32-55	IV CT			AL					WM W/L			HC	UP MS		MD	LB	MB CG
2		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48

DG MG			UL		UR			MOVER FUNCTION CPU			I/O						
49	50	51	52	53	54	55		0	1	2	0	1	2				2

Indicator	ALD	Bit Position	Description
ROS P30-55	RK211	0	Parity of bits 32-55.
IV-CT 32	RK201	1-3	Invalid digit and instruction address control (CPU mode).
IV-CT 33	RK201		
IV-CT 34	RK201	1-3	Timing signals to external channel (I/O mode).
AL 35	RK211	4-8	Shift control and gating into adder latch.
AL 36	RK211		
AL 37	RK211		
AL 38	RK211		
AL 39	RK211		
WM WL 40	RK221	9-12	Mover destination (CPU mode).
WM WL 41	RK221		
WM WL 42	RK221	9-11	Mover destination (I/O mode).
WM HC 43	RK221	12	Insert carry control (I/O mode).
MS UP 44	RK221	13-14	Byte counter function control (CPU mode).
MS UP 45	RK221	15	MD counter control (CPU mode).
MS MD 46	RK231	13-15	Multiplex stat setting (I/O mode).
CG LB 47	RK231	16	LB counter control (CPU mode).
CG MB 48	RK231	17	MB counter control (CPU mode).
		16-17	Control signal gating to channel (I/O mode).
DG-MG 49	RK231	18-20	Length counter and carry insertion control (CPU mode).
DG-MG 50	RK231		
DG-MG 51	RK231	18-20	Multiplex channel gate control (I/O mode).
UL 52	RK201	21-22	Mover function left digit.
UL 53	RK201		
UR 54	RK201	23-24	Mover function right digit.
UR 55	RK201		
		25	Not used.
MVR FUNCT CPU 0	KQ001	26-28	CPU mover function register.
MVR FUNCT CPU 1	KQ001		
MVR FUNCT CPU 2	KQ001		
MVR FUNCT I/O 0	KQ001	29-31	I/O mover function register.
MVR FUNCT I/O 1	KQ001		
MVR FUNCT I/O 2	KQ001		
		32-35	Not used.

FIGURE 162. CPU 2 ROLLER - POSITION 2



Indicator		ALD	Bit Position	Description
ONE SYL OP		KS221	0	One syl op trigger indicates a half word instruction.
RE-FETCH		KS211	1	Refetch stat indicates that the instruction buffer should not be used as the source of the next instruction.
			2-4	Not used.
EXT			5	Additional bit to address extended ROS.
NEXT ROS ADDR ROS BASE ADR	0	KK301	6-11	ROS base address (bits 0-5 of ROAR).
	1	KK301		
	2	KK311		
	3	KK311		
	4	KK321		
	5	KK301		
NEXT ROS ADDR FUNCT BIT	0	KK011	12-15	ROS address function field (bits 6-9 of ROAR).
	1	KK021		
	2	KK031		
	3	KK041		
NEXT ROS ADDR BRANCH	A	KK261	16	A branch (bit 10 of ROAR).
	B	KK271	17	B branch (bit 11 of ROAR).
EXT IRPT REG	1	KS271	18-23	External interrupt register.
	2	KS271		
	3	KS271		
	4	KS281		
	5	KS281		
	6	KS281		
PSW ILC	32	RP001	24-31	PSW 32-29.
	33	RP001		
PSW CC	34	RP011		
	35	RP021		
PSW PM	36	RP001		
	37	RP001		
	38	RP001		
	39	RP001		
			32-35	Not Used

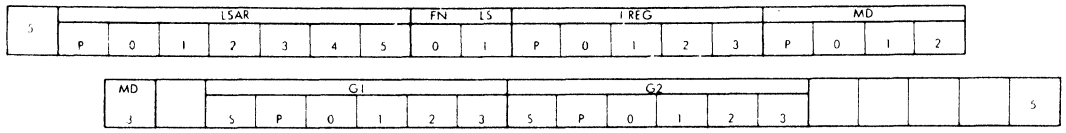
FIGURE 163. CPU 2 ROLLER - POSITION 3

4	I/O MODE	I/O REGISTER			TIMER IRPT	CONS IRPT	L BYTE CNTR			M BYTE CNTR			F REG					Q REG
		P	0	1			P	0	1	P	0	1	P	0	1	2	3	

EDIT STATS		GENERAL PURPOSE STATS												STORAGE RING				4
1	2	0	1	2	3	4	5	6	7	L SIGN	R SIGN	CARRY	RTL	R1	R2	R3	W1	

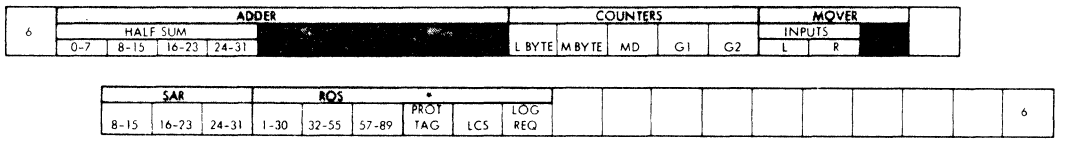
Indicator	ALD	Bit Position	Description
I/O MODE	KU111	0	I/O mode trigger is on during I/O routines.
I/O REG P	RL111	1-3	I/O register and parity (used for byte addressing in I/O mode).
I/O REG 0	RL111		
I/O REG 1	RL111		
TIMER IRPT	KS251	4	Timer interrupt stat (set by timer counting to zero).
CONS IRPT	KS251	5	Console interrupt stat (set by interrupt switch).
L BYTE CNTR P	CL001	6-8	L byte counter and parity (L register byte selection).
L BYTE CNTR 0	CL001		
L BYTE CNTR 1	CL001		
MB CNTR P	CM001	9-11	M byte counter and parity (M register byte selection).
MB CNTR 0	CM001		
MB CNTR 1	CM001		
F REG P	RF021	12-16	F register and parity (four bit shift spill and enter).
F REG 0	RF001		
F REG 1	RF001		
F REG 2	RF001		
F REG 3	RF011		
Q REG	RF031	17	Q register (one bit shift spill and enter).
EDIT STATS 1	KK581	18-19	Edit stats control operation during edit instruction.
EDIT STATS 2	KK581		
GP STATS 0	KS101	20-27	General purpose stats 0-7 (multipurpose stats).
GP STATS 1	KS111		
GP STATS 2	KS121		
GP STATS 3	KS131		
GP STATS 4	KS141		
GP STATS 5	KS151		
GP STATS 6	KS161		
GP STATS 7	KS171		
L SIGN	KS201	28	L register sign stat (on for positive).
R SIGN	KS201	29	R register sign stat (on for positive).
CARRY	KS231	30	Carry stat (on for carry insert).
RTL	KS631	31	Retry threshold latch indicates whether instruction retry is possible (tested by SERR program).
STORAGE RING R1	KC501	32-35	Storage ring positions R1, R2, R3, and W1.
STORAGE RING R2	KC501		
STORAGE RING R3	KC501		
STORAGE RING W1	KC501		

FIGURE 164. CPU 2 ROLLER - POSITION 4



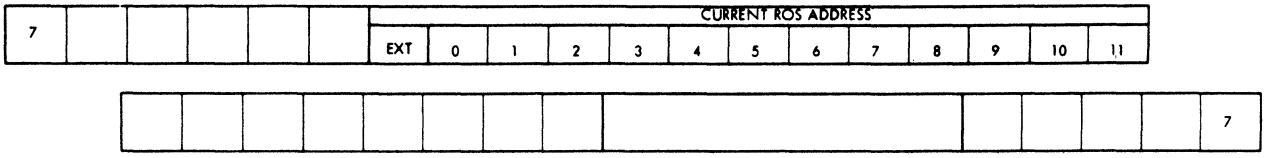
Indicator		ALD	Bit Position	Description
LSAR	0	LS111	0-6	Local store address register plus parity.
	1	LS111		
	2	LS111		
	3	LS121		
	4	LS121		
	5	LS121		
LSFN	0	KL001	7-8	Local store function register (local store addressing).
	1	KL001		
J REG	P	RJ011	9-13	J register plus parity (local store addressing).
	0	RJ001		
	1	RJ001		
	2	RJ001		
	3	RJ001		
MD CTR	P	CD021	14-18	MD counter plus parity (local store addressing and decimal multiplication and division).
	0	CD001		
	1	CD001		
	2	CD011		
	3	CD011		
			19	Not used.
G1	S	KP031	20-25	Length counter 1 plus sign and parity (G1 storage field length counter).
	P	CG101		
	0	CG101		
	1	CG101		
	2	CG101		
	3	CG101		
G2	S	KP031	26-31	Length counter 2 plus sign and parity (G2 storage field length counter).
	P	CG201		
	0	CG201		
	1	CG201		
	2	CG201		
	3	CG201		
			32-35	Not used.

FIGURE 165. CPU 2 ROLLER - POSITION 5



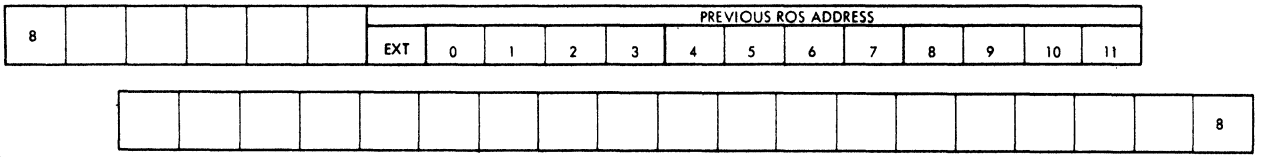
Indicator		ALD	Bit Position	Description
HALF SUM	0-7	KT011	0	Half sum 0-7.
	8-15	KT011	1	Half sum 8-15.
	16-23	KT011	2	Half sum 16-23.
	24-31	KT011	3	Half sum 24-31.
SUM	0-7	KT011	4	Sum 0-7.
	8-15	KT011	5	Sum 8-15.
	16-23	KT011	6	Sum 16-23.
	24-31	KT011	7	Sum 24-31.
CARRY		KT021	8	Carry.
CNTRS	L BYTE	KT021	9	L byte counter.
	M BYTE	KT021	10	M byte counter.
	MD	KT021	11	MD counter.
	G1	KT031	12	G1 length counter.
	G2	KT031	13	G2 length counter.
MVR IN L		KT021	14	Mover left input.
MVR IN R		KT021	15	Mover right input.
MVR OUT		KT021	16	Mover output.
			17	Not used.
SAR	8-15	KT031	18	Storage address register 8-15.
	16-23	KT031	19	Storage address register 16-23.
	24-31	KT031	20	Storage address register 24-31.
ROS	1-30	KT031	21	ROS 1-30.
	32-55	KT031	22	ROS 32-55.
	57-89	KT031	23	ROS 57-89.
PROT TAG		KT041	24	Storage protect.
LCS			25	LCS summary check.
LOG REQ		KT041	26	Log request (turned on by log out switch or common chan log out request).
			27-35	Not used.

FIGURE 166. CPU 2 ROLLER - POSITION 6



Indicator		ALD	Bit Position	Description
			0-4	Not used.
CURRENT ROS ADDRESS	EXT	KK302	5-17	Current ROS address.
	0	KK312		
	1	KK312		
	2	KK312		
	3	KK312		
	4	KK312		
	5	KK312		
	6	KK313		
	7	KK313		
	8	KK313		
	9	KK313		
	10	KK313		
	11	KK313		
			18-35	Not used.

FIGURE 167. CPU 2 ROLLER - POSITION 7



Indicator		ALD	Bit Position	Description
			0-4	Not used.
PREVIOUS ROS ADDRESS	EXT	KK302	5-17	Previous ROS address.
	0	KK312		
	1	KK312		
	2	KK312		
	3	KK312		
	4	KK312		
	5	KK312		
	6	KK313		
	7	KK313		
	8	KK313		
	9	KK313		
	10	KK313		
	11	KK313		
			18-35	Not used.

FIGURE 168. CPU 2 ROLLER - POSITION 8

ALD	Bit Position	Title	Description
KH321	0	PASS	Turned on by a successful FLT test execution.
KH321	1	FAIL	Turned on by a failing FLT.
KH211	2	BINARY TGR	Turned on or off for each good comparison. For a successful test, the light will return to its initial off state.
KH311	3	TEST CNTR = 0	Indicates a test has been executed 16 times (normal operation).
KH111	4-9	FLT OP REG	Six indicators display the FLT op register, which is used for decoding FLT operation routines.
KH341	10-12	SEQ CNTR	The three-position sequence counter is used for control during FLT load and for clock advance during FLT execution.
KH345	13-16	SEQ STAT	Indicates the four stats that are used in conjunction with the sequence counter during FLT load.
KH555	17	FLT LOAD CHK	Indicates a detected parity error in an unsuccessful FLT load.
KH321	18	SUPV STAT	Supervisory stat on allows the sequence counter to be decremented.
KH321	19	PROGSV SCAN STAT	Progressive scan stat on causes a return to main storage for control or scan information during execution of the diagnose instruction. (Normally off during FLT execution.)
KH321	20	SUPV ENABLE STOR	Supervisory enable store on disables the storage inhibit function of the supervisory stat during execution of the diagnose instruction. (Normally off during FLT execution.)
KT151	21	SEQ CNTR MODE	Indicates the CPU is under sequence counter control.
KT151	22	MAIN STOR MODE	Indicates the CPU is under main storage control.
KT151	23	ROS MODE	Indicates the CPU is under ROS control.
	24	ALT PREFIX	Indicates the state of the prefix trigger (this indicator is part of the multisystem feature).
KT161	25	HARD STOP	Indicates the four clocks are stopped due to an error.
KT151	26	LOG TGR	Indicates an error condition when a log out is to be initiated.
KH231	27	BLOCK INDIC	Block indicators is on when a bit in the FLT op register indicates that the information displayed in the status indicators is not being gated by the select switches. (At such times the force indicators keylever switch may be used.)
KT271	28	SINGLE CYCLE	Indicates when the CPU is in single cycle mode, or if the rate switch has been turned off single cycle but the start switch has not been pressed.
KT215	29	CPU CLOCK	On when the CPU clock is running.
KT211	30	CHAN CLOCK	On when the I/O clock is running.
KT211	31	ROS CLOCK	On when the ROS clock is running.
KT211	32	MAIN STOR CLOCK	On when the main storage clock is running.
KT161	33	CHK IRPT ENABLED	Check interrupt enabled is on whenever an error interrupt is possible.
KT161	34	CHK REG GATED	Check register gated is on whenever the error register is gated.
KT081	35	CHK PEND	The check pending trigger is set at the time the error register is set if PSW 13 is masked off. Upon unmasking, this trigger causes a log out and machine-check interrupt.

FIGURE 169. MAINTENANCE CONTROL INDICATORS

SDR	ALD	Bit Position
P0-7	BA 072	0
0	BA 001	1
1	BA 011	2
2	BA 021	3
3	BA 031	4
4	BA 041	5
5	BA 051	6
6	BA 061	7
7	BA 071	8
P8-15	BA 152	9
8	BA 081	10
9	BA 091	11
10	BA 101	12
11	BA 111	13
12	BA 121	14
13	BA 131	15
14	BA 141	16
15	BA 151	17
P16-23	BA 232	18
16	BA 161	19
17	BA 171	20
18	BA 181	21
19	BA 191	22
20	BA 201	23
21	BA 211	24
22	BA 221	25
23	BA 231	26
P24-31	BA 312	27
24	BA 241	28
25	BA 251	29
26	BA 261	30
27	BA 271	31
28	BA 281	32
29	BA 291	33
30	BA 301	34
31	BA 311	35

FIGURE 170. SDR INDICATORS

IAR	ALD	Bit Position
P8-15	CA 171	9
8	CA 161	10
9	CA 161	11
10	CA 161	12
11	CA 161	13
12	CA 151	14
13	CA 151	15
14	CA 151	16
15	CA 151	17
P16-23	CA 171	18
16	CA 141	19
17	CA 141	20
18	CA 141	21
19	CA 141	22
20	CA 131	23
21	CA 131	24
22	CA 131	25
23	CA 131	26
P24-31	CA 171	27
24	CA 121	28
25	CA 121	29
26	CA 121	30
27	CA 121	31
28	CA 111	32
29	CA 111	33
30	CA 111	34
31	CA 111	35

FIGURE 171. IAR INDICATORS

ROS Address		Function	Results Observed
202	* AK→T	Address keys to latches (8-31).	Display latches, change and observe address key settings.
	T→A	Latches (8-31) to SAR.	Display SAR, change and observe address key settings.
203	* AK→T	Address keys to latches (8-31).	
	T→IA	Latches (8-31) to IAR.	Display IAR, change and observe address key settings.
205	DK→T	Data keys to latches; bits 28-31 to F.	Display latches, change and observe data key settings.
	T→L	Latches to L register.	Display L register, change and observe data key settings.
20C	DK→T	Data keys to latches; bits 28-31 to F.	
	T→R	Latches to R register	Display R register, change and observe data key settings.
21F	DK→T	Data keys to latches; bits 28-31 to F.	
	T→H	Latches to H register	Display H register, change and observe data key settings
283	DK→T	Data keys to latches; bits 28-31 to F.	
	T→M	Latches to M register	Display M register, change and observe data key settings.
2AA	DK→T	Data keys to latches; bits 28-31 to F.	
	T→D	Latches to MDR.	Display MDR, change and observe data key settings
2AB	DK→T	Data keys to latches; bits 28-31 to F.	
	T→J	Latches 12-15 to J register.	Display J register, change and observe data key settings.
2AE	DK→T	Data keys to latches.	
	T→MD	Latches 8-11 to MD.	Display MD, change and observe data key settings.
202	AK→T	Back to first step in closed loop.	

* For AK→T machine check will come on when keys are changed; change keys and reset. Error should remain off

Channel Check Note: Display B and C registers for each channel. Set data keys to the following combinations: zeros, all ones, and alternate hex 5's and A's and check for correct data transfer.

FIGURE 172. ROS FUNCTION CHECK

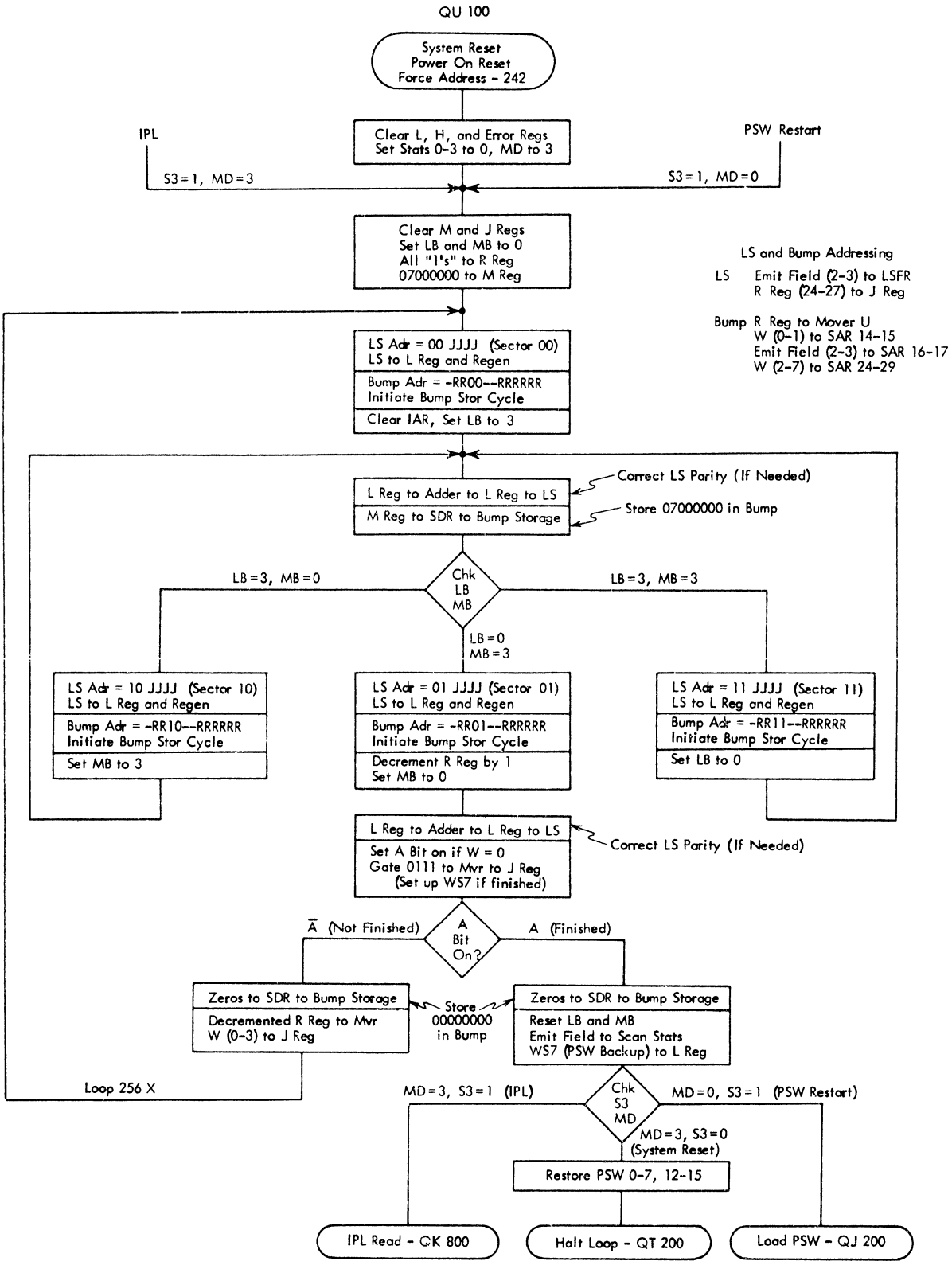


FIGURE 173. SYSTEM RESET

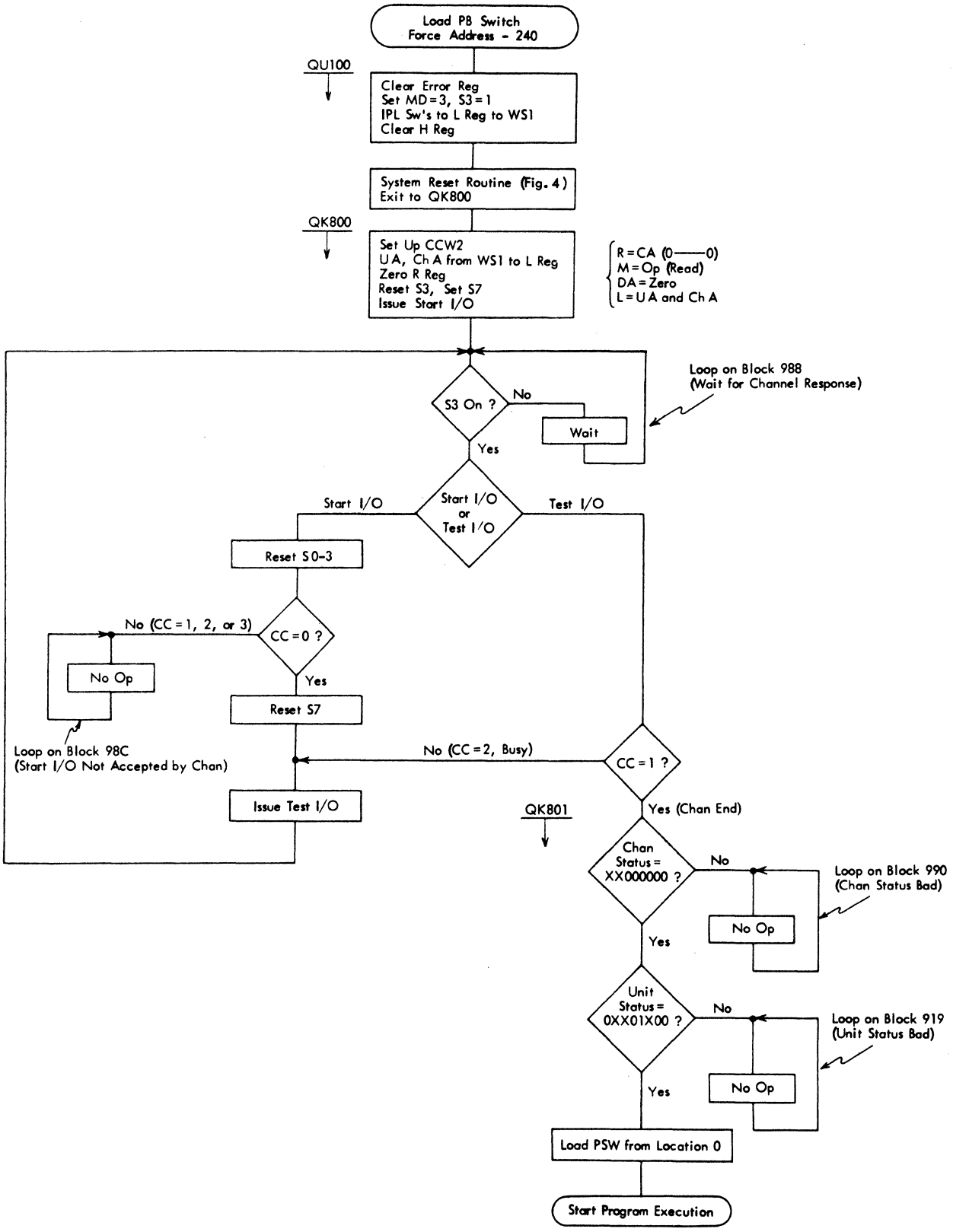


FIGURE 174. INITIAL PROGRAM LOAD

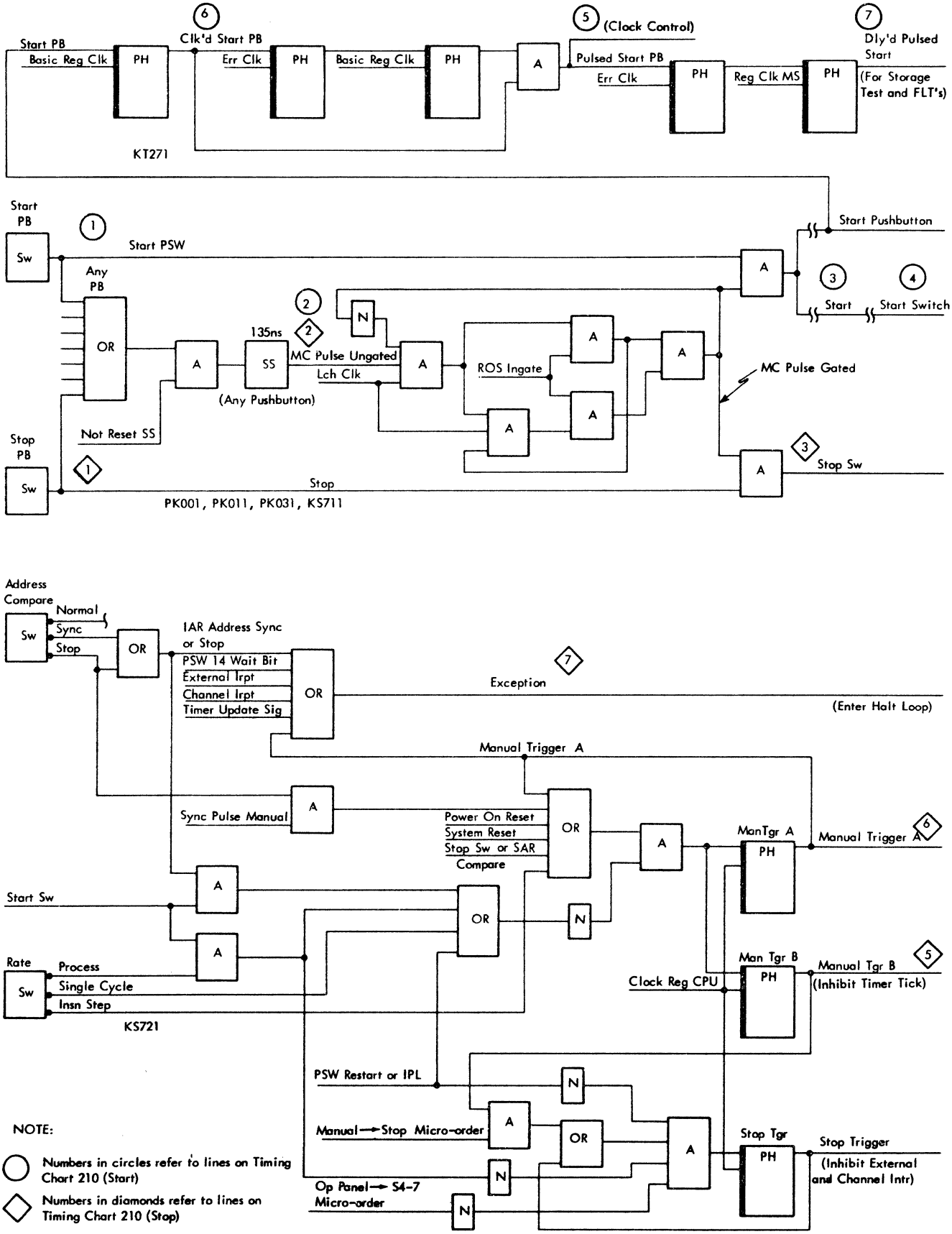


FIGURE 175. START, STOP, EXCEPTION LOGIC

Operation	Stats Set 4	5	6	7	Hex Value (Use with CLF 122)	Notes
Halt Loop	0	0	0	0	0	Stay in Halt Loop
Instruction Step	0	0	0	1	1	Wait Bit (PSW 14) must be off
Set IC	0	0	1	0	2	Set IAR
Repeat Instruction (IAR)	0	0	1	1	3	Instruction set by Address Switches
Address Compare (IAR)	0	1	0	0	4	Stop or Sync Position and Not Manual and Not Wait Bit
Display Main Storage	1	0	0	0	8	SDR Indicators
Store Main Storage	1	0	0	1	9	Data Switches to SDR
Display Storage Protect Key	1	0	1	0	A	F Register Indicators (CPU Roller #2, Position #4)
Store Storage Protect Key	1	0	1	1	B	Data Switches 28-31 to F Register
Display Local Storage	1	1	0	0	C	L Register Indicators (CPU Roller #1, Position #1)
Store Local Storage	1	1	0	1	D	Data Switches to L Register to Local Store
Display Bump Storage	1	1	1	0	E	SDR Indicators
Store Bump Storage	1	1	1	1	F	Data Switches to SDR

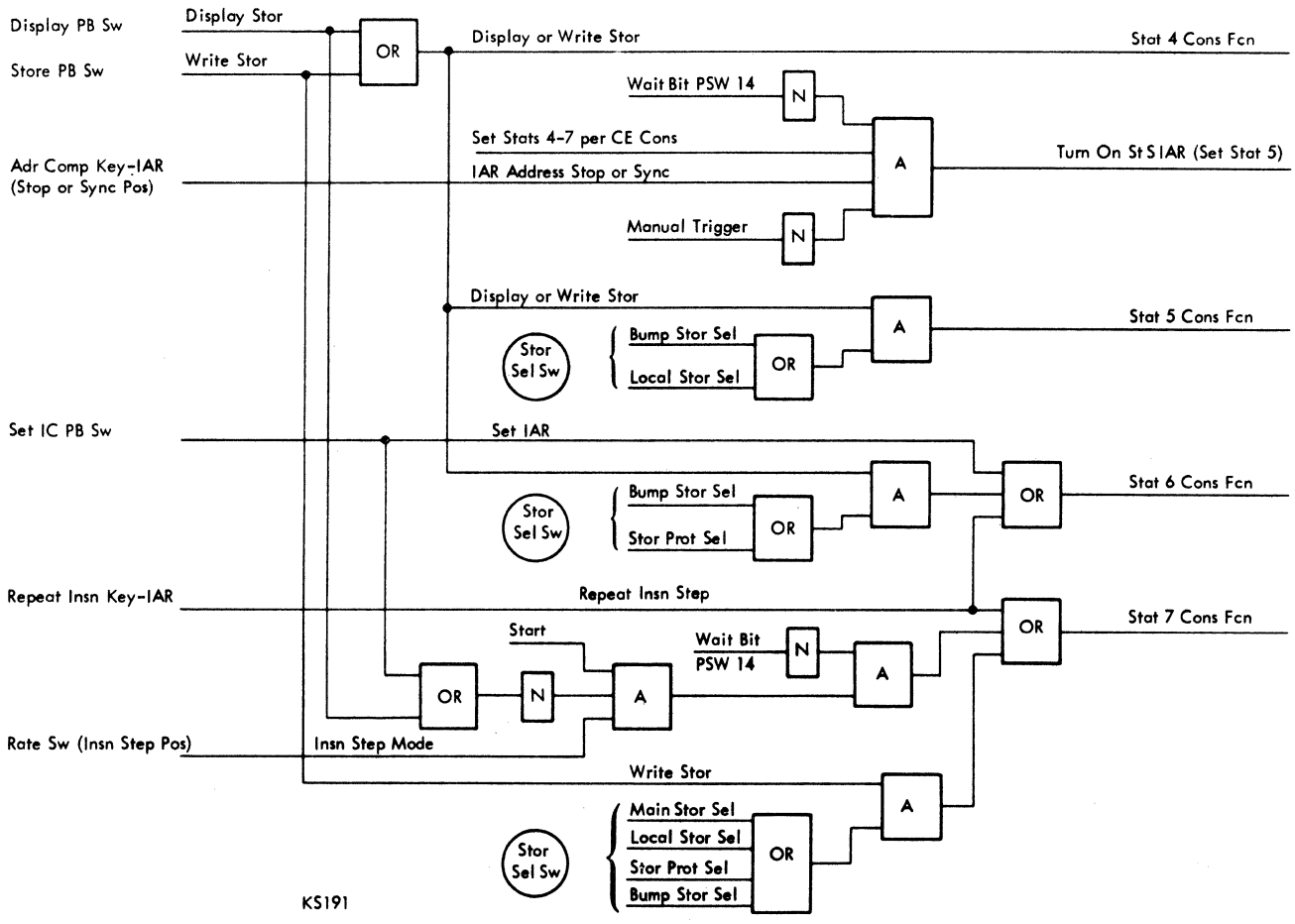


FIGURE 176. CONTROL PANEL SETTING

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