IBM Field Engineering

Theory of Operation

For Sale Through IBM Branch Offices

1800 Data Acquisition and Control System

Data-Processing Input/Output Features

SY26-3617-6

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PREFACE

This manual describes the 1800 system adapter features for the following IBM data processing input/output units:

1053 Printer
1816 Printer-Keyboard
1054 Paper Tape Reader
1055 Paper Tape Punch
1442 Card Read Punch
1443 Printer
1627 Plotter
2401/2402 Magnetic Tape Units

Chapter 4 (Features), normally found in the FETOM, does not apply to this manual.

Electromechanical and operational details of the DP I/O units are described in the manuals written for each unit. These unit manuals are referenced in the related chapters and listed, with form numbers, in the FE Bibliography - 1800 System, Order No. SY26-0560.

Information that is necessary to the understanding of this manual is in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller (See FE Bibliography -- 1800 System, Order No. SY26-0560.) It contains a comprehensive introduction to the 1800 system and specific descriptions of the 1801 and 1802 Processor-Controllers, including channel control.

The functional unit and operation descriptions in this manual refer to diagrams contained in the IBM Field Engineering Maintenance Diagrams Manual, 1800 Data Acquisition and Control System (see FE Bibliography -- 1800 System, Order No. SY26-0560). *

*Manuals referred to in this publication that have a form number with a four character prefix are identical in content to the same manual without the initial prefix character. (e.g., SY26-xxxx is the same in content as Y26-xxxx.)

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Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest FE Publications Systems Sequence Listing, Order No. SY20-0070, for revisions or contact the local IBM branch office.

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*Not applicable. Power supplied by Processor-Controller.

**Console and maintenance facilities for this feature are described in Chapter 6 of the Processor-Controller FETO manual.

ABBREVIATIONS

A Reg	Accumulator
ALD*	Automated logic diagram
B Reg	Storage buffer register
BCD	Binary coded decimal
BPI	Bytes per inch
CAB*	Channel address buffer
CAR*	Channel address register
CPU	Central processing unit
CRC*	Cyclic redundancy check
CRP*	Card read punch (IBM 1442)
CS*	Cycle steal
CWC*	Control word cycle
D Reg	Arithmetic factor register
DC*	Data channel
DPC*	Direct program control
DSW*	Device status word
DWC*	Data word cycle
EA*	Effective address
ECAD*	Error check analysis diagram
EOC*	End of conversion
EOT*	End of table
EPR*	Error pattern register
F Reg	Format register
FF*	Flip-flop
FL*	Flip-latch
I Reg	Instruction register
ILSW*	Interrupt level status word
IOCC*	Input/output control command
IPL	Initial program load
LC*	Lower case
LP	Load point
LRC	Longitudinal redundancy check
M Reg	Storage address register
MDM*	Maintenance diagram manual
Mod Reg	Modifier register
Op Reg	Operation code register
P-C*	Processor-controller
Q Reg	Accumulator extension register
RDD*	Read disconnect delay
R/W*	Read/write
SC*	Shift counter
SLD*	Simplified logic diagram
SLT*	Solid logic technology
SMS	Standard modular system
SRL*	Systems reference library
SS	Single-shot (multivibrator)
T Reg	Tag register
TCU*	Tape control unit
TU	Tape unit
U Reg	Temporary accumulator register
UC*	Upper case
UDCD*	Unit data and control diagram
VRC	Vertical redundancy check
WC*	Word counter
WDD*	Write disconnect delay
XR*	Index register
XIO*	Execute input/output

*Non-standard ALD abbreviation.

CHAPTER 1 INTRODUCTION

- The 1816 (Figure 1-1) provides a console keyboard and console printer for the IBM 1800 System.
- The 1053 (Figure 1-2) provides additional output typewriter printers for the IBM 1800 System.
- For a detailed description of the printer mechanics, see IBM Field Engineering Theory of Operation, I/O Printer (Modified IBM SELECTRIC®). (see FE Bibliography -- 1800 System, Form Y26-0560.)
- For a detailed description of the keyboard mechanics, see IBM Field Engineering Theory-Maintenance, 1052-1053. (see FE Bibliography -- 1800 System, Form Y26-0560.)

The 1816 is a combination of an IBM 1052 Keyboard and a 1053 Printer. The printer portion of the 1816 and the 1053 are therefore physically and functionally the same. The printer description presented here applies to both of these units.

A maximum of two 1816s and eight 1053s can be attached to the 1800 system; however, no more than a total of eight of these units in combination can be attached.

All printers operate in the overlapped mode; that is, each can print a different message at the same time. The 1816 can be installed up to 50 feet from the processor-controller (P-C). The 1053 can be installed up to 2000 feet from the P-C.

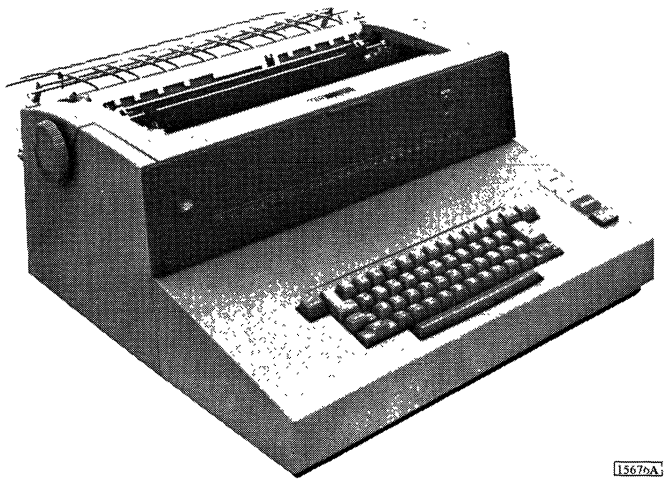


Figure 1-1. IBM 1816 Printer-Keyboard

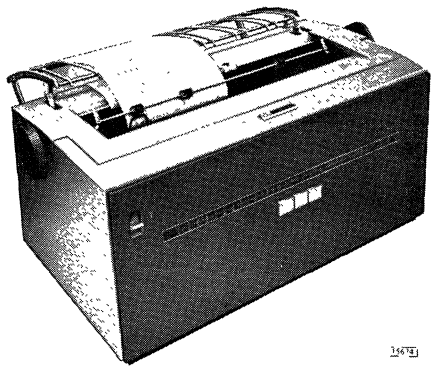


Figure 1-2. IBM 1053 Printer

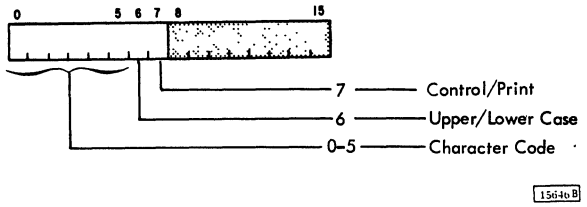
PRINTER FUNCTIONAL DESCRIPTION

- Maximum output rate of the printer is 14.8 characters per second.
- Data to be printed is transferred from core storage to the typewriter by direct program control.
- Data and control characters (space, tabulate, etc.) are sent to the typewriter by means of the write command.

Because control characters and data characters are sent in the same manner, the message to be printed contains a mixture of data characters and control characters in the sequence necessary to provide output in the desired format.

NOTE: The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is unrelated to the subject matter.

The character format within a core storage word to be transmitted to the typewriter printer is:



Each word transmitted to the typewriter printer contains one data character or one control character.

KEYBOARD FUNCTIONAL DESCRIPTION

- The keyboard of the 1816 printer-keyboard is similar to the keyboard of the IBM 1052.
- The keys are not connected to the printer; therefore, keyboard entries are not printed unless the P-C is programmed to do so.
- Maximum input speed of the keyboard is 20 characters per second but is usually limited by the speed of the operator.
- The keyboard operates under direct program control.
- The keyboard emits an IBM-card-coded character for each operation of a key.

The character coding emitted by the keyboard is shown in Figure 1-3. The character enters the P-C left justified. Thus, bit 0 corresponds to IBM card code 12, bit 1 to IBM card code 11, etc. Bits 12, 13, and 14 have special significance and indicate end of field, erase character, and erase field respectively. (See description of these three keys.) Odd-bit parity is generated to provide a data-transmission check on the input data at the processor-controller B-register.

Keys and Lights

Keys with special functions are:

KBD REQ (Keyboard Request Interrupt): This key initiates an interrupt in the P-C and turns off the proceed light.

END FLD (End of Field): When a read command is executed in response to this key, a word with only bit 12 = 1 is placed in core storage. Analysis of this word allows the program to determine that no further characters are to be sent in this message.

ER CHR (Erase Character): When a read command is executed in response to this key, a word with bit 13 = 1 is placed in core storage.

Analysis of this word allows the program to determine that the last character received is to be replaced by the next character to be entered.

ER FLD (Erase Field): When a read command is executed in response to this key, a word with bit 14 = 1 is placed in core storage. Analysis of this word allows the program to determine that the message being entered is to be deleted and replaced by a corrected message.

REST KB (Restore Keyboard): This key allows the operator to unlock the keyboard to release any key that is locked down.

The following lights appear on the keyboard:

Proceed: This light comes on when the P-C has performed the XIO (control) instruction. The keyboard is unlocked when proceed is on. This light goes off 25 milliseconds after the key is pressed or when the XIO (read) is executed.

Alpha: When on, this light indicates that keyboard characters on the lower half of the keybutton will be placed on the in bus for entry into the processor-controller.

Numeric: When on, this light indicates that keyboard characters on the upper half of the keybutton will be placed on the in bus for entry into the processor-controller.

ADAPTER FUNCTIONAL DESCRIPTION

- The 1816-1053 adapter provides a means of attaching keyboard input and typewriter-printer output to the 1800 system.
- The 1816-1053 adapter is contained on one SLT board located in the 1801 or 1802 at location A1 of gate C. A second adapter (expander) can be installed at B1 of gate D.
- Each 1816-1053 adapter accommodates four 1053s or one 1816 and three 1053s.

The adapter performs one or more of the following functions for each I/O command sent to it:

1. Selects the specified printer or printer-keyboard.
2. Decodes the function to be performed.

Key	IBM Card Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
*	11,8,4		1					1				1					
/	0,1			1	1												
0	0			1													
1	1				1												
2	2					1											
3	3						1										
4	4							1									
5	5								1								
6	6									1							
7	7										1						
8	8											1					
9	9												1				
$	11,8,3		1				1					1					
. (Period)	12,8,3	1					1					1					
, (Comma)	0,8,3			1			1					1					
EOF	None													1			
ER CHR	None														1		
ER FLD	None															1	
=	6,8									1		1					
' (Apostrophe)	5,8								1			1					
(	12,5,8	1							1			1					
)	11,5,8		1						1			1					
+	12,8,6	1								1		1					
- (Dash)	11		1														
A	12,1	1			1												
B	12,2	1				1											
C	12,3	1					1										
D	12,4	1						1									
E	12,5	1							1								
F	12,6	1								1							
G	12,7	1									1						
H	12,8	1										1					
I	12,9	1											1				

Key	IBM Card Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
J	11,1		1		1												
K	11,2		1			1											
L	11,3		1				1										
M	11,4		1					1									
N	11,5		1						1								
O	11,6		1							1							
P	11,7		1								1						
Q	11,8		1									1					
R	11,9		1										1				
S	0,2			1		1											
T	0,3			1			1										
U	0,4			1				1									
V	0,5			1					1								
W	0,6			1						1							
X	0,7			1							1						
Y	0,8			1								1					
Z	0,9			1									1				
Space	Blank	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
¢	12,8,2	1				1						1					
<	12,8,4	1					1					1					
|	12,8,7	1									1	1					
&	12	1															
!	11,8,2		1			1						1					
; (Semi-colon)	11,8,6		1							1		1					
¬	11,8,7		1								1	1					
%	0,8,4			1			1					1					
_ (Underscore)	0,8,5			1				1				1					
>	0,8,6			1					1			1					
?	0,8,7			1						1		1					
: (Colon)	8,2				1							1					
#	8,3					1						1					
@	8,4						1					1					
"	8,7										1	1					
0-8-2	0,8,2			1		1						1					

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Figure 1-3. Keyboard Character Code

3. Controls the mechanical motion of the printer or keyboard.
4. Transfers a data or control word to or from the processor-controller.
5. Indicates the status of the 1816, 1053, and the adapter to the P-C.
6. Initiates interrupts in the processor-controller program when the 1816 or 1053 requires service.

The adapter circuits include a buffer register to store the printer data word or printer control word for the printer operations. The keyboard data and control signals are stored in the keyboard contacts until the adapter gates them to the processor-controller.

Indicators are provided for keyboard, printer, and adapter status. Analysis of these indicators enables the program to determine the functions to be performed by the 1816 and 1053. A CE-mode circuit enables the adapter to be placed in an on-line-service mode.

I/O INTERFACE

- The 1816-1053 adapter connects to the 1801 or 1802 P-C channel control through the standard I/O channel interface.

- The 1816 printer-keyboard and 1053 printer connect to the adapter through a unique interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation (Manual of Instruction), 1800 Data Acquisition and Control System, Processor Controller. (see FE Bibliography – 1800 System, Form Y26-0560.)

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, and exits all 60 lines to the next adapter in sequence. If the 1816-1053 adapter is the last in the sequence, the channel interface lines must be jumpered through the remaining adapter positions (dummy boards). The lines are then terminated at the mixer panel (gate H).

The 1816-1053 adapter taps off and uses signals from these lines:

Out-bus bits 0 through 9 and 11 through 15 (not bit 10)
In-bus bits 0 through 15
Parity bit for bits 0 through 7
Parity bit for bits 8 through 15
Poll interrupt level 0-13
Poll interrupt level 14-23
Time pulse A
Time pulse B
Time pulse C
CAR check or parity error
Storage protect violation
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal and data lines that connect the 1816-1053 adapter to the keyboard and the printer.

The printer signals connect from the adapter board, through a flat cable and a serpent connector, to the P-C signal tailgate. The signals connect from the tailgate, through a serpent connector and signal cable to Amp connectors at the printer.

The keyboard signals connect from the adapter, through a flat cable, to the rear of the F gate. The front side of the F gate facilitates the connection of a special serpent connector that contains the integrator circuits for the key-contact signals. From this gate a flat cable connects the signals to the signal tailgate. The signals connect from the tailgate, through a serpent connector and signal cable to Amp connectors at the keyboard.

The 1816 keyboard interface lines and their functions are listed in Figure 1-4. The 1053 printer lines and functions are listed in Figure 1-5.

Line	Adapter In/Out	Function
dc Ground	Out	One line transmits dc ground to device.
Keyboard contact 0-9, 11, 12	In	These twelve lines transmit the condition of bail contacts in the keyboard. A unique combination of these contacts are closed for each key depressed on the keyboard. This combination of contacts closed is sent to core storage when the keyboard is read. Any contact closure causes a keyboard service request to be sent to the processor-controller.
Keyboard End Field	In	This line causes a keyboard service request and causes a 12 bit to be placed in core storage in response to the read command. Analysis of this word allows the program to determine that no further characters are to be sent in this message.
Kybd. Re-enter Char.	In	This line causes a keyboard service request and enters a 13 bit in core storage in response to a read command. Analysis of this word allows the program to determine that the last character received is to be replaced by the next character to be entered.
Kybd. Re-enter Field	In	This line causes a keyboard service request and enters a 14 bit in core storage in response to a read command. Analysis of this word allows the program to determine that the message being entered is to be deleted and replaced by the corrected message.
Kybd. Restore Key	In	This line turns on the keyboard-restore magnet driver in the adapter and causes the keyboard to be restored.
Keyboard Space	In	This line causes a keyboard service request and enters a zero data word in core storage in response to a read command.
Kybd. Interrupt Req. Key	In	This line causes a keyboard interrupt request to the P-C and turns on the manual-status flip-flop. This informs the program that the operator wishes to enter a message on the keyboard.
Keyboard Ready	In	Indicates presence of +12 vdc in keyboard.
Kybd. Proceed Lamp	Out	This line turns on the proceed lamp on the keyboard, indicating the adapter is ready to receive a keyboard service request.
Kybd. Restore Mag.	Out	This line energizes the keyboard restore magnet and resets the keyboard.

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Figure 1-4. 1816 Device Interface Lines

Line	Adapter In/Out	Function
Ready	In	Indicates presence of d-c power and paper in place at the printer.
Carrier Return Line Feed & Tab	In	Indicates when the printer is busy performing a line feed, tab , or carrier return. The rise of the line turns on the printer-response flip-flop and the fall resets the printer-response flip-flop.
Printer Cam	In	Indicates the printer is taking a cam cycle. Line is active when cam contact 2, 5, or 7 is open due to printer taking a cycle to perform an operation. Cam 2 is active on a print cycle. Cam 5 is active on a tab, space or backspace. Cam 7 is active on a shift. The printer-response flip-flop is turned on when this line becomes active and is turned off when the line becomes inactive.
Motor On	In	Indicates the motor is stopped. Forces shift required and starts a 35 millisecond single-shot if motor is stopped when the adapter receives a command.
End of Line	In	Indicates the carrier is at the right hand margin. When next print cycle occurs, turns on last-col flip-flop, causing a carrier return to take place.
Upper Case	Out	Picks a magnet in the printer, causing a shift to upper case and a shift cycle in the printer (Cam 7 cycles) if the printer is not already at upper case.
Lower Case	Out	Picks a magnet in the printer, causing a shift to lower case and a shift cycle in the printer (Cam 7 cycles) if the printer is not already at lower case.
Carrier Return	Out	Picks a magnet in the printer, causing the carrier to return to the left hand margin and a line feed.
Tab	Out	Picks a magnet in the printer, causing a tab cycle (Cam 5 cycles). The carrier advances to the right until it reaches the position of the next tab stop.
Space	Out	Picks a magnet in the printer, causing the carrier to advance one print position to the right, (Cam 5 cycles).
Drop Motor Relay	Out	Energizes motor-control time-delay relay. If energized continually for 2 minutes, the time delay relay picks and holds as long as energized. When time delay relay picks, TD1-1 N/C drops relay 6 which drops printer motor. TD1-2 N/O informs the adapter that the motor is stopped with the motor-on line.
48 v	Out	Four lines are used to transmit 48 volts to the printer for magnet and relay power.
+12 v	Out	12 volts to the printer to power ready, end of line, carrier-return, line-feed, and tab status contacts.
d-c Ground	Out	Two lines are used to transmit dc ground.
T2,T1, R1, R2A	Out	Picks magnets in the printer to control the positioning of the print ball and cause the printer to take a print cycle (Cam 2 cycles).
Backspace	Out	Picks a magnet in the printer, causing the carrier to advance one print position to the left (Cam 5 cycles).
R2	Out	Picks a magnet in the printer to control the positioning of the print ball and cause the printer to take a print cycle (Cam 2 cycles).
Red	Out	Picks a magnet in the printer, causing a shift of the ribbon mechanism so printing will take place on red portion of ribbon.
R5	Out	Picks a magnet in the printer to control the positioning of the print ball and cause the printer to take a print cycle (Cam 2 cycles).
Black	Out	Picks a magnet in the printer, causing a shift of the ribbon mechanism so printing will take place on black portion of ribbon.
Line Feed	Out	Picks a magnet in the printer to cause the platen to advance.
Aux.	Out	Picks a magnet in the printer to cause a print cycle to occur if the character to be printed is all zeros and does not pick any other print-positioning magnet. The ball prints its home position character. The printer takes a print cycle (Cam 2 cycles).

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Figure 1-5. 1053 Device Interface Lines

CHAPTER 2 FUNCTIONAL UNITS

- The interrelationship of the functional units described in this section is shown in the 1800 System Maintenance Diagram Manual (MDM) page EA 40160.

FUNCTION REGISTER

- One three-position register decodes the functions for both the keyboard and the printer.
- Loaded from out-bus bits 5, 6, and 7 during the XIO control cycle.

Bits 5, 6, and 7 of the IOCC control word, placed on the out bus during the XIO control cycle, are the gate inputs to the function register. The pulse that sets the register, called function set, is activated by the XIO-control-cycle line if the printer-keyboard area or interrupt level is on the out bus and if there is no parity error indicated by the processor-controller (P-C). The function register is reset at the end of the XIO data cycle. The decoded output of the function register provides the following functions:

001 Write: This command sends the P-C word at the core storage location specified by the IOCC address word to the typewriter-printer. The word sent to the typewriter-printer is either printed or it causes a control operation to be performed.

010 Read: This command enters a single input character from the keyboard into the P-C core storage location specified by the IOCC address word. This command turns off the proceed status. It also turns on the parity or storage-protect indicator if either error is detected during the read operation.

011 Sense Interrupt: This command directs the printer keyboard adapter to place its assigned interrupt-level-status-word (ILSW) bit on the in bus if any of its interrupt indicators are on. The ILSW is loaded into the P-C accumulator for program analysis.

100 Control: This command restores the keyboard and turns on the proceed lamp. The proceed lamp indicates to the operator that the P-C is ready to receive a keyboard character. The depression of a character key will then cause a service interrupt.

111 Sense Device: This command causes the selected printer or printer-keyboard to place its device status word (DSW) on the in bus. The DSW is loaded into the P-C accumulator for program analysis.

000 CE Mode: This special use command is not decoded by the function register. It is decoded by the CE mode circuit, to place the selected printer or printer-keyboard in, or take it out of, the CE mode.

CHARACTER SHIFT CIRCUITS

- Consists of a single flip-flop, named "shift required."
- Controls the upper- and lowercase magnets in the printer.
- Delays printing to allow time for shifting.
- Controlled by bit 6 of the data word.
- Refer to FEMDM page EA 60100 for explanation of write operation with shift.

BUFFER REGISTER

- Eight flip-flops, loaded from out-bus bits 0 through 7.
- Loaded at T7 time of the XIO data cycle.
- Six positions are dual purpose; their function is determined by out-bus bit 7.

  Reset by a single-shot after the print operation has commenced.

If out-bus bit 7 = 1, specifying a control operation, buffer-register position 7 is not turned on. The off condition of position 7 gates the output of positions 0 through 6 to the printer control magnets. If out-bus bit 7 = 0, specifying a print operation, buffer-register position 7 is turned on. The on condition of position-7 gates the output of positions 0 through 5 to the print magnets.

CHAPTER 3 PRINCIPLES OF OPERATION

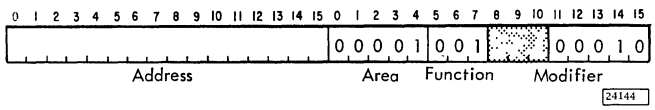
PRINTER OPERATIONS

- An execute I/O instruction places the control word of the addressed I/O control command (IOCC) on the out bus.
- Bits 5, 6, and 7 are loaded into and decoded by the printer-keyboard function register.
- The printer performs any of the following functions:
  1. Control (carrier return, tabulate, etc.)
  2. Shift and print
  3. Print without a shift
  4. Sense device
- The write function, modified by bit 7 of the data word, can initiate either a print or a control operation.
- The sense device function places the status of the printer indicators on the in bus.

Write

- Reads data word from core storage location specified by IOCC address word and places it on the out bus.
- Data word is either printed or it is decoded to cause a printer control operation.
- The I/O operation diagrams for the write function are on MDM page EA 40111 and EA 40112.
- The write operation objectives are shown for each type of operation on MDM page EA 60100.
- The timing diagrams for the write function are on MDM page EA 60105, and EA 70100.

IOCC – Write



Address: These 16 bits specify the core storage location of the data word. It is used during the XIO data cycle.

Area: Bits 0 through 4 decode as 00001 to specify the printer-keyboard adapter.

Function: Bits 5, 6, and 7 decode as 001 to specify a write function.

Modifier: Bits 11 through 14 select the printer. Bit 14 addresses the first printer, bit 13 addresses the second, bit 12 the third, and bit 11 the fourth. If two or more printers are addressed, all those addressed will print the same data simultaneously.

Data Word

Data to be printed by the typewriter-printer is coded by the program into the typewriter code. Figure 1-6 shows the characters which can be printed by the standard print element for IBM 1800 typewriter-printers.

Bit 6 of the data-character determines the upper-case (UC) shift or lower-case (LC) shift characters. The printer shifts automatically as required for each data character.

A typewriter-printer write command is effectively modified by bit 7 position of the output character word. If bit 7 = 1, the write command to the printer results in a control function. If bit 7 = 0, the write command results in a print function.

The codes for typewriter-printer control functions are shown in Figure 1-7.

Description

E-1 Cycle: This cycle is referred to as the XIO control cycle. The effective address (EA), loaded into the accumulator during the I cycle, must be an even address. This address, which is the location of the IOCC, is loaded into the M register. The on output line of the M register bit-15 flip-flop is activated. This causes EA +1, the location of the IOCC control word, to be addressed. The control word, which includes the area, function, and modifier bits, is placed on the out bus.

The channel function register is loaded at T5 time to perform I/O bus gating, etc. The function register in the printer-keyboard adapter is loaded if the printer

B0	B1	B2	B3	B4	B5	B6=0 LC	B6=1 UC	B7
0	0	1	1	1	1	A	A	0
0	0	0	1	1	0	B	B	0
0	0	0	1	1	1	C	C	0
0	0	1	1	0	0	D	D	0
0	0	1	1	0	1	E	E	0
0	0	0	1	0	0	F	F	0
0	0	0	1	0	1	G	G	0
0	0	1	0	0	1	H	H	0
0	0	1	0	0	0	I	I	0
0	1	1	1	1	1	J	J	0
0	1	0	1	1	0	K	K	0
0	1	0	1	1	1	L	L	0
0	1	1	1	0	0	M	M	0
0	1	1	1	0	1	N	N	0
0	1	0	1	0	0	O	O	0
0	1	0	1	0	1	P	P	0
0	1	1	0	0	1	Q	Q	0
0	1	1	0	0	0	R	R	0
1	0	0	1	1	0	S	S	0
1	0	0	1	1	1	T	T	0
1	0	1	1	0	0	U	U	0
1	0	1	1	0	1	V	V	0
1	0	0	1	0	0	W	W	0
1	0	0	1	0	1	X	X	0
1	0	1	0	0	1	Y	Y	0
1	0	1	0	0	0	Z	Z	0
1	1	1	1	1	1	1	(	0
1	1	0	1	1	0	2	+	0
1	1	0	1	1	1	3	<	0
1	1	1	1	0	0	4	¬	0
1	1	1	1	0	1	5	)	0
1	1	0	1	0	0	6	;	0
1	1	0	1	0	1	7	*	0
1	1	1	0	0	1	8	'	0
1	1	1	0	0	0	9	"	0
1	1	0	0	0	1	0	|	0
1	1	0	0	0	0	#	=	0
1	0	1	1	1	1	/	-	0
1	0	0	0	0	1	-	?	0
1	0	0	0	0	0	,	:	0
0	1	0	0	0	1	&	>	0
0	1	0	0	0	0	$	.	0
0	0	0	0	0	1	@	%	0
0	0	0	0	0	0	.	¢	0

15647

Figure 1-6. Data Character Coding (1816/1053)

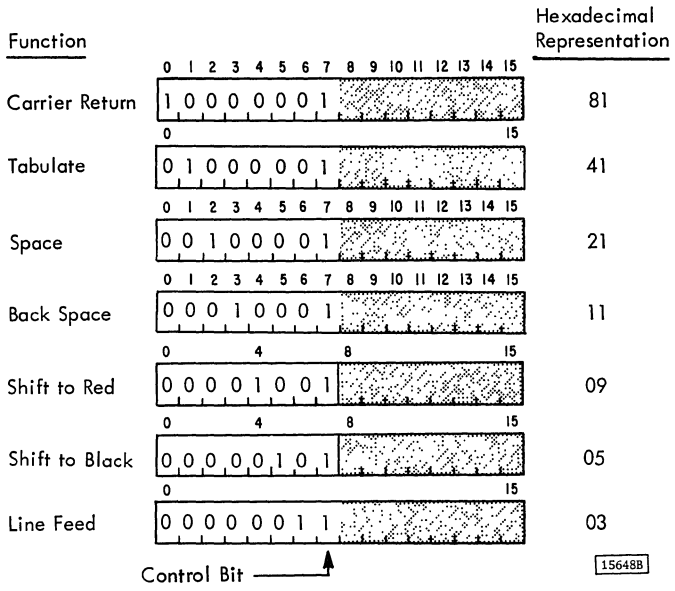


Figure 1-7. Control Characters (1816/1053)

area code is specified in the IOCC and if there is no parity error signal from the processor-controller. The decoded output of the function register is used during the E-3 data cycle to specify the write function (Code 001).

E-2 Cycle: The M_{15} bit output is no longer forced active so that EA, which is the location of the address word, is addressed. The address word is therefore read from core storage and loaded into the accumulator for use in the E-3 cycle.

E-3 Data Cycle: The address word of the IOCC, loaded into the accumulator during the E-2 cycle, addresses the data word which is placed on the out bus. The XIO instruction execution is terminated and the program continues with the next instruction.

Print and Control Execution: FEMDM pages EA 60100 through EA 60110 illustrate the following printer operations:

- Print character with motor on/off.
- Print with shift.
- Print last column (EOL).
- Control operation.
- Color shift.

KEYBOARD OPERATIONS

- Request key initiates an interrupt request and locks the keyboard. When the interrupt is serviced, an XIO instruction with an IOCC specifying a control function is executed.
- The control operation selects the keyboard, places it in the proceed status, unlocks the keyboard, and turns on the proceed lamp.
- Operation of a character key places the card code of that character into the keyboard contacts and initiates another interrupt request.
- When this interrupt is serviced, an XIO instruction with an IOCC specifying a read function is executed.
- The read operation transfers the data word (card-code character) from the keyboard contacts to the processor-controller (P-C) core storage.
- The I/O operation diagram for the keyboard control and read operations is on MDM page EA 40101.
- The timing diagram for the control and read operations is on MDM page EA 70101.

The keyboard operation, for the first character, requires these four steps:

1. Keyboard Request. The operator presses the request key to signal the P-C that a character is to be entered from the keyboard.
2. Control Command. The P-C signals the keyboard adapter that it is ready to accept the character.
3. Character Key Operation. The operator presses the character key and the keyboard adapter signals the P-C that the character is ready to be placed on the in bus.
4. Read Command. The P-C executes a read operation to take the character and store it.

The operation for subsequent characters requires steps 2 through 4.

Keyboard Request

- Initiated by operation of the keyboard request key.
- Generates an interrupt request to the P-C.
- Locks the keyboard.

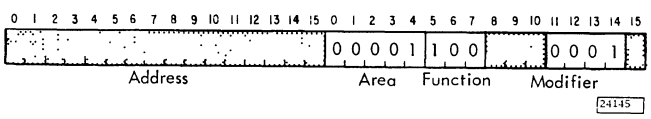
Operating the keyboard request key activates a 25-millisecond keyboard-service-request single-shot. The timing out of this single-shot turns on the manual-status flip-flop which activates a second single-shot, the output of which restores the keyboard. Manual-status also conditions the typewriter interrupt-request circuit that is activated when its assigned interrupt level is polled by the P-C.

Control Command

- Initiated by an XIO instruction as a result of an interrupt.
- Selects the keyboard, restores the keyboard, and turns on the proceed lamp.

When the P-C satisfies all conditions to service the interrupt initiated by the request key, a branch is forced to a subroutine containing an XIO instruction with an IOCC specifying the keyboard and a control function.

IOCC Control



Address: Not used.

Area: Bits 0 through 4 decode as 00001 to select the printer-keyboard area.

Function: Bits 5, 6, and 7 decode as 100 to cause the keyboard to perform a control operation.

Modifier: Bits 11 through 14 decode to select the specified printer or keyboard. Bit 14 must be a one to select the keyboard.

Description

E-1 Control Cycle: The keyboard area code and bit 14 of the IOCC turn on the select-keyboard flip-flop. The control function is decoded by the function register.

E-2 Data Cycle: At T6 of this cycle, the 25 millisecond restore single-shot is activated to energize the keyboard restore magnet. The restore single-shot also turns on the proceed flip-flop, the output of which turns on the proceed lamp on the keyboard. The proceed lamp signals the operator to press a character key. The fall of the XIO data cycle line activates the function reset line to reset the function register.

Character Key Operation

- Stores the character code in the keyboard contacts.
- Initiates an interrupt request after a 25-millisecond delay.

The operation of any keyboard contact activates the keyboard-service-request line. Keyboard-service-request activates a 25-millisecond single-shot. The timing out of the single-shot resets the proceed flip-flop and turns on the service-request flip-flop. The output of the service-request flip-flop conditions the typewriter interrupt-request circuit that is activated when its level is polled by the P-C.

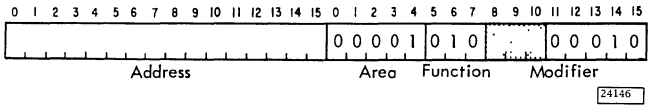
Read Command

- Initiated by an XIO instruction as a result of an interrupt.
- Gates the character from the keyboard to the in bus.
- Stores the character at the location specified by the address portion of the IOCC.

- Resets the proceed flip-flop.
- The I/O operation diagram for the read operation is on MDM page EA 40101.

When the P-C satisfies all conditions to service the keyboard interrupt, a branch is forced to a subroutine containing an XIO instruction with an IOCC specifying keyboard and a read function.

IOCC Read



Address: This 16-bit address word specifies the core storage location into which the keyboard character is stored.

Area: Bits 0 through 4 decode as 00001 to select the printer-keyboard area.

Function: Bits 5, 6, and 7 decode as 010 to cause the keyboard to perform the read operation.

Modifier: Bits 11 through 14 decode to select the specified printer or keyboard. Bit 14 must be a one to select the keyboard.

Example: Bit 14 = 1 selects 1816 number 1
Bit 13 = 1 selects 1053 number 2

Description

E-1 Control Cycle: The on output line of the M register bit-15 flip-flop is activated to address EA + 1 (odd). This address is the location of the control word of the IOCC. The control word is set into the B register and placed on the out bus.

The keyboard area code and bit 14 of the IOCC turn on the select-keyboard flip-flop. The area code also activates the function-set line to load the function register with bits 5, 6, and 7.

E-2 Cycle: The decoded output of the function register is used to specify the read function (Code 010). The P-C drops the forced M_{15}-bit line, reads the IOCC address word (at EA) and loads it into the accumulator to be used during the E-3 cycle to address core storage.

E-3 Data Cycle: The select-keyboard and read-function lines activate the keyboard-read-gate line which gates the character from the keyboard contacts to the in bus. The character is stored at the core storage location specified by the IOCC address word. The keyboard-read-gate also conditions parity or storage-protect flip-flops to be turned on at T7 if either error is detected.

The fall of XIO-data-cycle activates the function-reset line to reset the function register. The fall of keyboard-read-gate resets the proceed flip-flop.

If additional characters are to be entered, the program must execute another XIO control command to return the keyboard to the proceed condition. After the last character is entered, the end-of-message key is operated to indicate to the program that the subroutine need not be repeated.

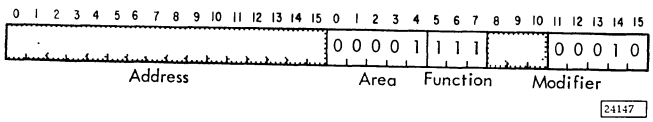
PRINTER-KEYBOARD SENSE AND CE MODE OPERATIONS

Sense Device

- Places the printer or printer-keyboard device status word (DSW) on the in bus.
- The DSW is loaded into the P-C accumulator to be analyzed by the program.
- If specified by bit 15 of the IOCC control word, the sensed indicators are reset.
- The I/O operation diagram for the sense device operation is on MDM page EA 40151.

The first printer and the keyboard are both selected by the same modifier code. Therefore, the first printer indicators and the keyboard indicators are all placed on the in bus as one DSW. If any printer other than the first printer is selected, the indicators for that printer only will be placed on the in bus as the DSW.

IOCC – Sense Device



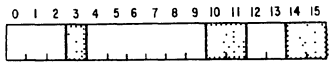
Address: Not used.

Area: Control-word bits 0 through 4 decode as 00001 to select the printer-keyboard area.

Function: Bits 5, 6, and 7 decode as 111 to cause the printer-keyboard to perform a sense device operation.

Modifier: Bits 11 through 14 decode to select the specified printer: bit 14 selects the first printer and the keyboard; bit 13 selects the second printer; bit 12, the third printer; and bit 11, the fourth printer. If more than one printer is selected, the DSW indicates a composite of all the selected printer conditions. Bit 15 = 1 specifies that the indicators will be reset after they are sensed.

Device Status Word



0 Printer Service Response
1 Keyboard Service Response
2 Keyboard Request
4 Printer Busy
5 Printer Not Ready
6 Keyboard Not Ready
7 Storage Protect Violation
8 Keyboard Parity Error
9 Printer Parity Error
12 CE Busy
13 CE Not Ready

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Bits associated with the keyboard are present only if IOCC modifier bit-14 is a one. The assigned bits of the DSW define the status of the following indicators:

Printer Service Response: This indicator indicates that the printer has completed printing the data or executing the control operation specified by the last data word transmitted by the XIO (write) instruction. This indicator is reset by the sense device operation if the IOCC bit-15 is a one.

Keyboard Service Response: This indicator indicates that one of the keyboard contacts has closed while the proceed light was on and that a character is ready to be transferred to the P-C. This indicator is reset by the keyboard-DSW-reset line.

Keyboard Request: This indicator indicates that the keyboard request key has been operated. This indicator is reset by the keyboard-DSW-reset line.

Printer Busy: When on, this indicator indicates that the printer is in the process of printing a character or executing a control and therefore should not be given a write command. The printer-busy line is active from the time data is sent to the printer until the printer completes the specified operation.

Printer Not Ready: When off, this indicates that the typewriter-printer is properly loaded with forms, has dc power, and is not busy. It is necessary that the program always determine that the not-ready indicator is off before a write command is given. If a write command is given while not-ready is on, loss of information will probably occur. No indication is given of this loss.

If not-ready is tested and found to be on, busy should then be tested. If busy is off, operator intervention is required. However, if not-ready is on and busy is on, it indicates that the typewriter-printer has not finished execution of the previous write command.

Keyboard Not Ready: This indicator, when on, indicates that the keyboard is not physically ready (dc power off, keyboard disconnected) or that the proceed flip-flop is on. The proceed flip-flop is on from the time that the XIO control command is decoded until the keyboard-service-request interrupt is activated (the interrupt is activated 25 milliseconds after the character key is operated), or until a read command is executed.

Storage Protect Violation: This indicator indicates that when the keyboard is being read, a storage protect violation is detected in the P-C. It is reset by the sense device operation if the IOCC bit-15 is a one.

Keyboard Parity Error: This indicator indicates that when the keyboard is being read, a parity error is detected in the P-C. It is reset by the sense device operation if the IOCC bit-15 is a one.

Printer Parity: This indicator is turned on if the P-C indicates that a parity error has been detected in the last character transferred from the P-C. It is reset by the sense device operation if the IOCC bit-15 is a one.

CE Busy: If the printer is in the CE mode (CE-mode flip-flop on), this indicator replaces the busy indicator (bit 4).

CE Not Ready: If the printer is in the CE mode, this indicator replaces the not-ready indicator (bit 5).

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area, function, and modifier bits are decoded to select the DSW to be placed on the in bus. The storage-use line (P-C line to core storage) is deactivated because the data (DSW)

to be transferred from the printer is not to be stored in core storage.

If bit 15 of the control word is a one, the DSW-reset flip-flop is turned on.

E-2 Data Cycle: A one is placed on the in bus in the bit positions associated with the status indicators that are on. The in bus is gated to the out bus during this cycle. If the DSW-reset flip-flop is on (bit-15 in E-1 cycle), the service-response and printer-parity flip-flops are reset by their corresponding out-bus bits.

The DSW is set into the B register, loaded into the accumulator, and the operation is terminated.

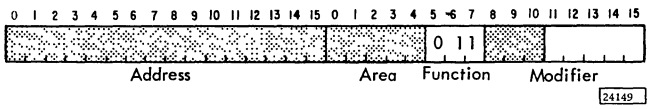
Sense Interrupt

- The interrupt level status word (ILSW), with one bit position representing the collective status of the printer-keyboard interrupts, is transferred to the processor-controller for program analysis.
- The I/O operation diagram for printer-keyboard sense interrupt is on MDM page EA 40151.

The sense-interrupt function causes the status of the three interrupt indicators to be ORed and placed on the in bus in the position assigned to the printer-keyboard. The three interrupt indicators are keyboard-request, keyboard-service-response, and printer-service-response.

The ILSW is loaded into the P-C accumulator to enable the program to determine which area or device is requesting an interrupt on the associated level.

IOCC Sense Interrupt



Address: Not used.

Area: Not used.

Function: Code 011 specifies the sense interrupt function.

Modifier: Bits 11 through 15, containing the ILSW address, are placed on the out bus automatically by the P-C during the XIO control cycle. These bits are decoded to identify the interrupt level to which the printer-keyboard is assigned.

Interrupt Level Status Word

The 16 bits of the ILSW indicate the interrupt status of each I/O device or area that is assigned to the interrupt level specified by the IOCC modifier.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. If modifier bits 11 through 15 decode as the interrupt level to which the printer-keyboard adapter is assigned, the function and modifier bits are decoded to condition the sense interrupt circuits.

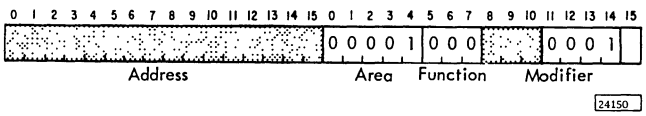
E-2 Data Cycle: The ORed outputs of the three interrupt indicators are gated to a single position on the in bus. This bit position, together with bit positions assigned to other I/O devices (areas) at this interrupt level, make up the ILSW that is transferred to the P-C.

CE Mode

- Turns on or off the CE-mode flip-flop.

When the CE-mode flip-flop is on, interrupt and device status indicators are modified to signal the program that the specified printer or printer-keyboard (one CE mode circuit) is in the CE mode. When in CE mode, all printer-keyboard interrupts are on the CE interrupt level rather than on the assigned interrupt level.

IOCC CE Mode



Address: Not used.

Area: Control word bits 0 through 4 decode as 00001 to select the printer-keyboard area.

Function: Bits 5, 6, and 7 decode as 000 to turn on, or off, the CE-mode flip-flop in the specified adapter.

Modifier: Bits 11 through 14 specify the printer-keyboard or printer for which the CE-mode flip-flop is to be turned on or off. Bit 15 = 1 conditions the CE-mode flip-flop to be turned on; bit 15 = 0 conditions it to be turned off.

Description

E-1 Control Cycle: The word at EA +1 (IOCC control word) is placed on the out bus. The area is decoded if there is no parity-error signal from the P-C. At time-pulse-B time, the function-set pulse is generated. Function-set, gated by bits 5, 6, and 7 = 000 and out-bus bit 15 = 1, turns on the CE-mode flip-flop. If out-bus bit-15 = 0, function-set and bits 5, 6, and 7 = 000 turn off the CE-mode flip-flop.

E-2 Data Cycle: A dummy cycle.

CHAPTER 1 INTRODUCTION

The 1054 Paper Tape Reader (Figure 2-1) and 1055 Paper Tape Punch (Figure 2-2) provide paper tape input/output for the IBM 1800 System.

One of each can be connected to the system.

READER-PUNCH FUNCTIONAL DESCRIPTION

- The 1054 and 1055 operate under direct program control.
- The 1054 Paper Tape Reader reads one-inch, eight-track, paper tape at a maximum rate of 14.8 columns per second (cps).
- The 1055 Paper Tape Punch punches one-inch, eight-track, paper tape at a maximum punching rate of 14.8 cps.
- For additional 1054 and 1055 information, see Field Engineering Theory of Operation, 1054 Paper Tape Reader, 1055 Paper Tape Punch (See FE Bibliography – 1800 System, Order No. SY26-0560.)

Data Coding

The 1054 Paper Tape Reader reads input data into the processor-controller core storage as an image of the holes in the tape. One paper-tape character is read into each addressed core storage location. Any code translation must be made by programming.

Figure 2-3 indicates the bits of the core storage word and the corresponding holes in the paper tape read by the 1054.

The 1055 Paper Tape Punch punches data as an image of the data contained in the core storage word on a character-to-character basis as shown in Figure 2-3.

Special data-character and control-character (feed code, etc.) coding and recognition must be handled by the stored program.

Initial Program Load

A special mode, called initial program load (IPL), provides a means of reading a group of instructions from an input unit, storing them beginning at the core storage location specified by the I register (normally reset to 0000), and automatically branching to 0000 to execute the program. In the 1800 system, the 1054 Paper Tape Reader and the 1442 Card Read Punch are both capable of initial program load. Only one unit in a system can be wired for initial program load. The first 1442, if attached, must be the IPL device. If there is no 1442 in the system, the paper tape reader is wired for IPL.

In initial-program-load mode, the 1054 reads four 4-bit characters into a 16 position buffer and sends the 16-bits to the processor-controller as one

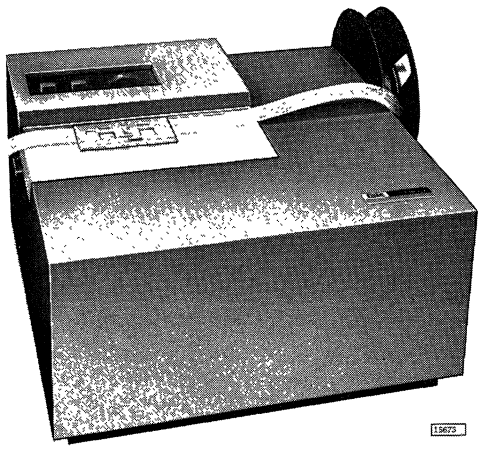


Figure 2-1. IBM 1054 Paper Tape Reader

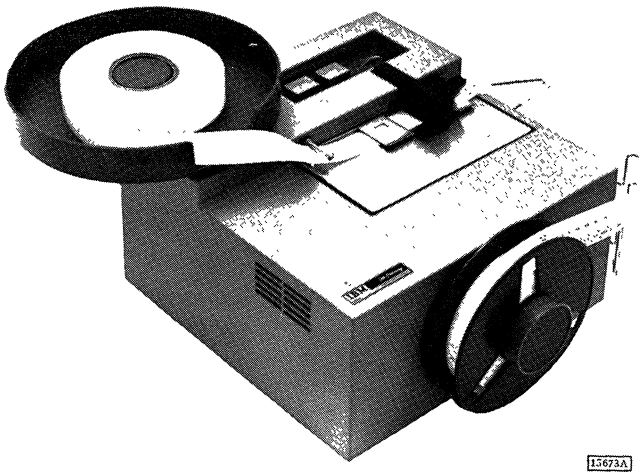


Figure 2-2. IBM 1055 Paper Tape Punch

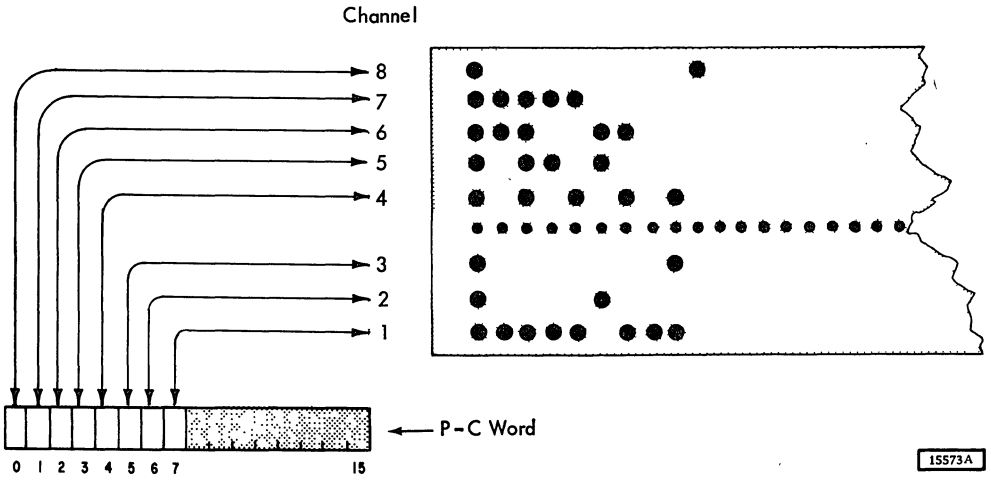


Figure 2-3. Word Format, Read Mode

word (Figure 2-4). The initial-program-load operation continues until a punch in tape-channel 5 is read.

ADAPTER FUNCTIONAL DESCRIPTION

- The 1054-1055 adapter provides a means of attaching paper-tape input and/or output to the 1800 system.
- The 1054-1055 adapter is contained on one SLT board located in the 1801 or 1802 at location A1 of gate D.
- The adapter accomodates one 1054 paper tape reader and one 1055 paper tape punch.

The adapter performs one or more of the following functions for each I/O command sent to it:

1. Decodes the function to be performed.
2. Controls the mechanical motion of the reader or punch.
3. Transfers data from the processor-controller to the 1054.
4. Transfers data from the 1055 to the processor-controller.
5. Indicates the status of the 1054, 1055, and the adapter to the P-C.
6. Initiates interrupts in the processor-controller program when the 1054 or 1055 requires service.

To implement these functions, the adapter circuits include a function register, a read buffer, and a punch buffer. The adapter contains interrupt and status indicators that the program can analyze to determine the functions to be performed on the reader or punch. The adapter also contains circuits that enable the initial loading of a program from paper

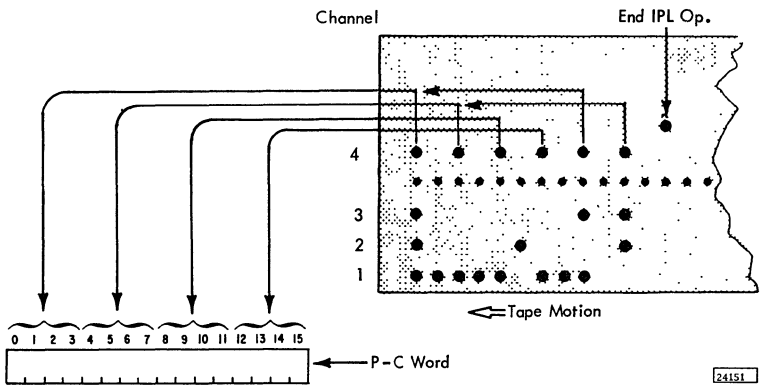


Figure 2-4. Word Format, IPL Mode

tape. A CE-mode circuit enables the adapter to be placed in an on-line-service mode.

I/O INTERFACE

- The 1054-1055 adapter connects to the 1801 or 1802 P-C channel control through the standard I/O channel interface.
- The 1054 Paper Tape Reader and 1055 Paper Tape Punch connect to the adapter through a unique interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation (Manual of Instruction), 1800 Data Acquisition and Control System, Processor-Controller (see FE Bibliography – 1800 System, Form Y26-0560).

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, and exits all 60 lines to the next adapter in sequence. If the 1054-1055 adapter is the last in the sequence, the channel interface lines must be jumpered through the remaining adapter positions (dummy boards). The lines are then terminated at the mixer panel (gate H).

The 1054-1055 adapter taps off and uses signals from these lines:

Out-bus bits 0 through 9 and 11 through 15 (not bit 10)
In-bus bits 0 through 15
Parity bit for bits 0 through 7
Parity bit for bits 8 through 15
Poll interrupt level 0-13
Poll interrupt level 14-23
IPL Mode
Time pulse A
Time pulse B
Time pulse C
CAR check or parity error
Storage protect violation
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal and power lines that connect the paper tape reader and paper tape punch to the 1054-1055 adapter and to the power supplies.

The 1054 and 1055 signals connect from the adapter board, through flat cable to edge connectors EC15 through EC20. At the edge connectors, the reader signals feed through resistors and the punch signals feed through diodes. From the edge connectors, the signals connect to twist connectors on the P-C power tailgate. The twist connectors and cables connect the signals and power to the 1054 and 1055.

The 1054 device interface lines and their functions are listed in Figure 2-5. The 1055 device interface lines and their functions are listed in Figure 2-6.

Line	Adapter In/Out	Function
Bit Rdr. A,B,C,8,4,2,1	In	These seven lines transmit the open or closed status of the read contacts, for paper tape channels 7 to 1, to the read buffer.
8th Ch. Sense Fwd.	In	This line transmits the open or closed status of the read contact, for paper tape channel 8, to the read buffer.
Reader Strobe	In	This timing signal defines the time in the reader cycle the pin sensors are reading the holes in the paper tape.
Reader Not Rdy.	In	This line transmits the presence of the tape at read station and tape tension status to the control adapter.
Reader Clutch	Out	This line energizes the reader feed clutch which, when tripped, permits the reader to take a mechanical cycle to sense the tape channels and advance the tape.
48 vdc	Out	48 volts dc to the reader for clutch power.
115 vdc	Out	Two lines are used to transmit a-c power for the reader motor.
12 vdc	Out	12 volts dc to power the reader ready status line, the pin sense contacts for the eight paper tape data channels, and the reader strobe pin sense contact.
Frame Ground	-	One line transmits frame ground to the reader.

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Figure 2-5. 1054 Device Interface Lines

Line	Adapter In/Out	Function
Punch Channel 1 - 8	Out	These eight lines, when active, trip punch magnets in the device to punch holes in their respective paper tape channels when the punch goes through its mechanical cycle.
Punch Ready	In	This line transmits the presence of paper tape at the punch station with punch head cover down and the status of the paper tape feed tension switch to the control adapter.
Punch Clutch	Out	This line energizes the punch feed clutch which causes the punch to go through its mechanical cycle of punching the paper tape channels and advancing the paper tape.
+48 vdc	Out	48 volts dc to power punch magnets and punch clutch magnet.
+12 vdc	Out	12 volts dc to power the punch ready status contacts.
115 vac	Out	Two lines are used to transmit 115 for the punch drive motor.
d-c Ground	-	Two lines transmit d-c ground to the punch.
Frame Ground	-	One line transmits frame ground to the punch.

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Figure 2-6. 1055 Device Interface Lines

CHAPTER 2 FUNCTIONAL UNITS

- The interrelationship of the functional units described in this section is shown in the 1800 Maintenance Diagram Manual (MDM) pages ES 40101, ES 40102, and ES 40111.

FUNCTION REGISTER

- One three-position register decodes the functions for both the paper tape reader and the paper tape punch.
- Loaded from out-bus bits 5, 6, and 7 during the XIO control cycle.

Bits 5, 6, and 7 of the IOCC control word, placed on the out bus during the XIO control cycle, are the gate inputs to the function register. The pulse that sets the register, control-word, is activated by the XIO-control-cycle line if the 1054/1055 area or interrupt level is on the out bus and if there is no parity error indicated by the processor-controller (P-C). The function register is reset at the end of the XIO data cycle. The decoded output of the function register provides the following functions:

001 Write: This command sends the P-C word at the core storage location specified by the IOCC address word to the paper tape punch.

010 Read: This command enters a single input character from the paper tape reader into the P-C core storage location specified by the IOCC address word.

011 Sense Interrupt: This command directs the 1054/1055 adapter to place its assigned interrupt-level-status-word (ILSW) bit on the in bus if any of its interrupt indicators are on. The ILSW is loaded into the P-C accumulator for program analysis.

100 Control: This command is not decoded by the function register. Bits 5, 6, 7, and 11 are decoded to cause the 1054 to read one character and signal the P-C that the character is ready to be transferred to the P-C.

111 Sense Device: This command transfers the 1054/1055 device status word (DSW) to the P-C for program analysis. The DSW indicates the status of the 1054/1055 indicators.

000 CE Mode: This special-use command is not decoded by the function register. It is decoded by the CE-mode circuit, to place the paper tape reader or punch in, or take it out of, the CE mode.

READ BUFFER

- Sixteen flip-flops, position 0 through 15 (Figure 2-7).
- For a read operation, positions 0 through 7 are loaded from the reader sense channels 1 through 8.
- Initial program load (IPL) loads positions 0 through 15 from sense-channels 1 through 4 in four intervals.
- Reset during the control operation that precedes each read operation.
- Output is gated to the in bus, the parity generator, and the I/O monitor connectors.

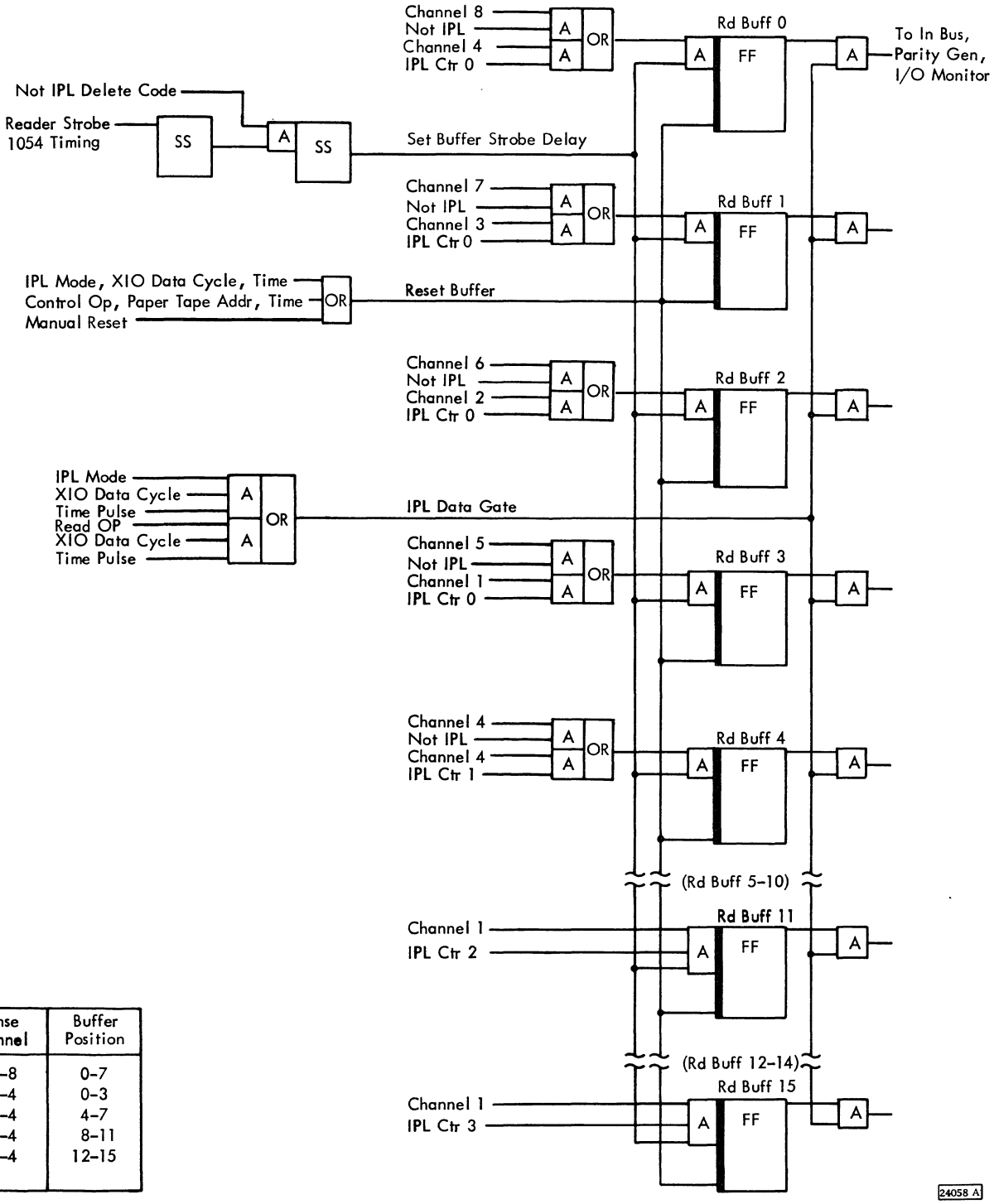
Control Operation: The read buffer is reset when the reader-clutch flip-flop is turned on during the control command E-1 cycle. The set-read-buffer pulse that loads the buffer is generated by the reader-strobe pulse. The reader-strobe pulse results from the reader clutch cycle initiated by the control command.

Initial Program Load Operation: Positions 0 through 15 are loaded from sense-channels 1 through 4 under control of the IPL counter. The buffer is reset at the beginning of the IPL operation by the reader strobe and IPL-counter-0. It is loaded by pulses generated from the reader strobe.

IPL COUNTER

- Two flip-flops, IPL 0-1 and IPL 2-3, and four AND circuits produce IPL counter-0 through -3 signals.
- Stepped by binary inputs from the set-read-buffer line.

The same pulse that sets the read buffer, activated by 1054 timing pulses, steps this two-position binary counter to provide gates for loading the read buffer.



Operation	Sense Channel	Buffer Position
Read	1-8	0-7
IPL-0	1-4	0-3
IPL-1	1-4	4-7
IPL-2	1-4	8-11
IPL-3	1-4	12-15

Figure 2-7. Read Buffer

PUNCH BUFFER

- Eight flip-flops, 0 through 7.
- Loaded from out-bus bits 0 through 7 during the XIO data cycle of a write operation.
- Reset by same pulse that sets it after a 30-millisecond delay.
- Output goes directly to the 1055 punch circuits.
- Figure 2-8 shows the input and output scheme.

Out Bus Bit	Punch Buffer Position
0	8 Channel
1	B
2	A
3	C
4	8
5	4
6	2
7	1

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Figure 2-8. Punch Buffer Loading

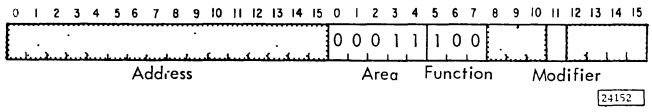
READER OPERATIONS

- Initiated by an XIO instruction with an IOCC function of control.
- Control command loads the read buffer and then moves paper tape one character position.
- When the read buffer is loaded (approximately 15 ms), an interrupt request is sent to the processor-controller (P-C).
- Branch is forced to an XIO with an IOCC function of read.
- Read command transfers a character from the read buffer to the core storage location specified by the IOCC address word.
- In initial-program-load mode, 16-bit words (composed of four 4-bit tape characters) are sent to the P-C to be used as instructions.

Control

- A control command must precede each read command to perform the following functions:
  1. Load tape image into read buffer.
  2. Initiate an interrupt request.
  3. Move tape one character position.
- The I/O operation diagram showing control functions is on MDM page ES 40101.
- The timing diagram for the control function is on MDM page ES 70141.

IOCC Control



Address: Not used.

Area: Bits 0 through 4 decode as 00011 to specify the paper tape reader-punch.

Function: Bits 5, 6, and 7 decode as 100 to specify a function of control.

Modifier: Bit 11 must be a one to specify a start-paper-tape-reader operation. No other modifier positions are used.

Description

E-1 Cycle: An XIO instruction effective address (EA) which has been loaded into the accumulator is an even address. This address is transferred to the M register and the on output line of the bit-15 flip-flop is forced on to address EA + 1. The word at EA + 1, which is the IOCC control word, is placed on the out bus to load the function register in the P-C channel-control circuits and in each I/O adapter.

If the area bits in the control word decode as 00011, no parity error is indicated by the P-C, bit 11 is a one, and the reader is ready, bits 5, 6, and 7 decode as 100 to turn on the reader-clutch flip-flop and reset the read buffer.

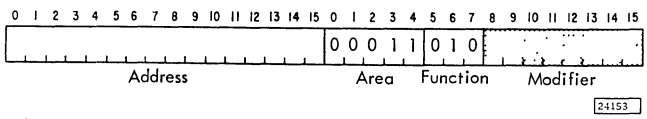
E-2 Cycle: This is a dummy cycle; all reader functions have been initiated.

Reader Functions: When the reader clutch is energized, the cycle contact on the reader sensing assembly emits the reader strobe. Reader strobe starts a 5 millisecond single-shot. When the single-shot times out, the read buffer is set with the image of the tape character, the clutch flip-flop is reset, and the reader-response flip-flop is turned on to send an interrupt request to the P-C. After the sensing pins are retracted from the tape, the reader advances the tape.

Read

- Transfers one character from the read buffer to the P-C core storage location specified by the IOCC address word.
- The I/O operation diagram is on MDM page ES 40101.

IOCC Read



Address: These 16 bits specify the core storage location into which the paper tape character is stored.

Area: Bits 0 through 4 decode as 00011 to specify the paper tape reader-punch area.

Function: Bits 5, 6, and 7 decode as 010 to specify the read function.

Modifier: Not used.

Description

E-1 Control Cycle: The IOCC control word at EA + 1 is placed on the out bus. If the area bits decode as 00011 and no parity-error is indicated by the P-C, out-bus bits 5, 6, and 7 are loaded into the function register. Function-register positions 5, 6, and 7 decode as 010 to specify a read function. No reader action takes place in this cycle.

E-2 Cycle: No reader action. The P-C reads the address word of the IOCC from core storage and loads it into the P-C accumulator for use in the E-3 Cycle.

E-3 Data Cycle: XIO data cycle and read-function gate the contents of the read buffer on the in bus. The data word is transferred to the processor-controller B register and stored in the core storage location specified by the address word of the IOCC.

The operation is terminated and the P-C continues with the program. To read subsequent characters from paper tape, another control command and read command must be executed.

Initial Program Load Operation

- Reads paper-tape channels 1 through 4 in four groups.
- Loads the read buffer with 4 four-bit groups (16 bits).
- Transfers the contents of the read buffer as one 16-bit word to the P-C.
- The timing diagram for IPL mode is on MDM page ES 70101.

The purpose of the initial-program-load mode is to read paper tape characters and send them to the P-C in a format that enables their use as instructions. The characters are read from tape channels 1 through 4 and loaded into read buffer positions 0 through 15 (Figure 2-5). The 16-bit word is gated onto the in bus and stored in one core storage location. The first 16-bit P-C word (four 4-bit tape characters) is stored at core storage location 0000, the second is stored at 0001, etc.

Reading in IPL mode continues until a punch in channel 5 is detected. The P-C then automatically branches to 0000 and begins executing the instructions.

Description

The IPL operation is initiated by the IPL-mode line from the processor-controller (P-C). IPL mode is activated by the program-load button on the programmer's console. The reader clutch is activated by IPL mode (from P-C) and the reader being ready. The reader-clutch flip-flop is not turned on.

The first reader strobe from the reader resets the read buffer because IPL-counter-0 is active. Reader strobe also activates a 5-millisecond single-shot. The timing out of the single-shot generates the set-read-buffer pulse. IPL-counter-0 gates the sense-channel-1 through -4 signals into read buffer positions 0 through 3. The same pulse that loads the buffer turns on the IPL-counter-0 -1 flip-flop, establishing the IPL-counter-1 condition.

The reader-clutch line remains active, causing the reader to feed tape, sense the characters, and generate the reader-strobe pulses. The second reader-strobe pulse generates a set-read-buffer pulse that, because IPL-counter-1 is active, gates sense-channel-1 through -4 into buffer positions 4 through 7. Set-read buffer also turns off the IPL-counter-0 -1 flip-flop. IPL-counter-0 -1 going off turns on IPL-counter-2 -3 flip-flop, establishing the IPL-counter-2 condition. The third reader-strobe pulse generates a set-read-buffer pulse that, because IPL-counter-2 is active, gates sense-channel-1 through -4 into buffer positions 8 through 11. The same set-read-buffer pulse also steps the IPL counter.

IPL-counter-0 -1 flip-flop is turned on. Both IPL-counter-0 -1 and IPL-counter-2 -3 being on establish the IPL-counter-3 condition. The fourth reader-strobe pulse generates a set-read-buffer pulse that, because IPL-counter-3 is active, gates sense-channel-1 through -4 into buffer positions 12 through 15.

The set-read-buffer and IPL-counter-3 combine to turn on the interrupt-request-15 flip flop. Interrupt-request-15 flip-flop activates in-bus bit 15 to signal the P-C that an IPL character is ready to be transferred. IPL-request in the P-C turns on the XIO-data-cycle flip-flop. XIO-data-cycle and IPL-mode combine to gate the output of the read buffer to the in bus. XIO-data-cycle resets the IPL-request-15 flip-flop.

The set-read-buffer pulse also steps the IPL counter to the IPL-counter-0 condition.

Delete Code: In IPL mode, a tape character with holes in channels 1 through 7 (delete code) inhibits the gating of the reader-strobe pulse; thus, no set-read-buffer pulse is generated. The delete character is not loaded into the buffer and the IPL counter is not stepped.

End of IPL Operation: The IPL read operation continues until a hole in tape-channel-5 is sensed. The sense-channel-5, IPL-mode, and not-delete-code signals combine to activate in-bus bit 14 to signal the P-C that all the IPL characters have been read. These same three lines also combine to reset the read buffer.

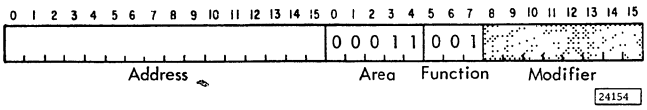
PUNCH OPERATIONS

- Each character to be punched requires an XIO instruction with an IOCC specifying a write function.
- Write command punches the character specified by the IOCC address word and advances the paper tape.
- After a delay to advance tape and reset circuits, an interrupt request is initiated.
- The I/O operation diagram for the write operation is on MDM page ES 40111.
- The timing diagram is on MDM page ES 70111.

Write

The addressing, punching, and tape advancing are all accomplished by the write command. An XIO instruction effective address (EA) is loaded into the processor-controller (P-C) accumulator during I cycles.

IOCC Write



Address: These 16 bits specify the core storage location of the data word. It is used during the XIO data cycle.

Area: Bits 0 through 4 decode as 00011 to specify the paper tape reader-punch area.

Function: Bits 5, 6, and 7 decode as 001 to specify a write function.

Modifier: Not used.

Description

E-1 Cycle: This cycle is referred to as the XIO control cycle. The effective address (EA), loaded into the accumulator during the I cycle, must be an even address. This address, which is the location of the IOCC, is loaded into the M register and the on output of bit-15 flip-flop is activated. This causes EA+1, the location of the control word, to be addressed. The control word, which includes the area, function and modifier bits, is placed on the out bus.

The channel function-register is loaded at T5 time to perform I/O bus gating, etc. The function register in the paper-tape adapter is loaded if area code 00011 is specified in the IOCC and if there is no parity-error signal from the P-C. The decoded output of the function register is used during the E-3 data cycle to specify the write function (Code 001).

E-2 Cycle: The bit-15 line is no longer forced active so that EA, which is the location of the address word, is addressed. The address word is therefore read from core storage and loaded into the accumulator for use in the E-3 Cycle.

E-3 Data Cycle: The address word of the IOCC, loaded into the accumulator during E-2 Cycle, addresses the data word which is placed on the out bus. Time pulse B (from P-C at T3 time), XIO data cycle, and write-function AND to generate the set-punch-buffer pulse. The set-punch-buffer pulse gates out-bus bits 0 through 7 into the punch buffer. The punch-buffer outputs connect to magnet drivers to control the punch magnets directly.

Set-punch-buffer also turns on the punch-busy flip-flop. Punch-busy gates the output of the oscillator flip-flop to the complement input of the punch-control-A flip-flop.

The operation of the clutch flip-flop, the reset of the punch buffer, and the reset of the punch-busy flip-flop are all controlled by a timing ring consisting of three binary-connected punch-control flip-flops. The punch-control flip-flops are operated by a free-running oscillator gated by the punch-busy flip-flop.

The second, punch-control-B, flip-flop going on turns off the clutch flip-flop to advance the paper tape. (The character just transferred has been punched.)

The third, punch-control-C, flip-flop gates the punch-buffer-reset pulse. It is generated the next time punch-control-B goes on. The punch-control-C flip-flop going off turns off the punch-busy flip-flop. All three positions of the ring are now off.

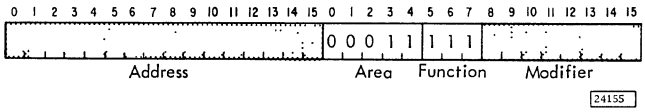
The punch-busy flip-flop going off turns on the punch-response flip-flop. When the processor-controller polls the assigned interrupt level, the assigned bit position of the in bus is activated. The punch-response flip-flop also conditions the DSW bit-3 position to indicate to the program, through the sense device command, that the character has been punched. Subsequent characters must be transferred to the punch by another write command.

READER-PUNCH SENSE OPERATIONS

Sense Device

- Places the paper tape reader-punch device status word (DSW) on the in bus.
- The DSW is loaded into the P-C accumulator to be analyzed by the program.
- If specified by bit 15 of the IOCC control word, the sensed indicators are reset.
- The paper tape reader-punch indicators are shown on MDM pages ES 40101 and 40111.

IOCC Sense Device



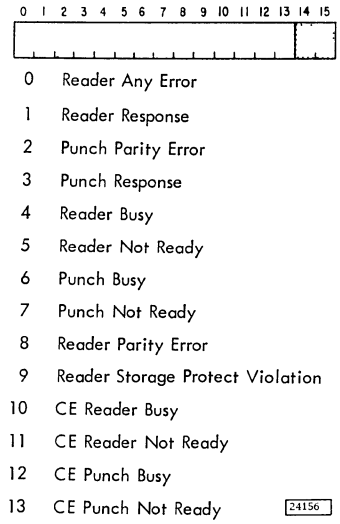
Address: Not used.

Area: Control-word bits 0 through 4 decode as 00011 to select the paper tape reader-punch area.

Function: Bits 5, 6, and 7 decode as 111 to cause the reader-punch adapter to perform a sense device operation.

Modifier: Bit 15=1 causes certain indicators to be reset when they are sensed.

Device Status Word



The assigned bits of the device status word define the status of the following indicators:

Reader Any Error: This indicator indicates that when the adapter is transferring a tape character to the P-C, either a parity error or a storage protect violation is detected in the P-C.

Reader Response: This interrupt indicator is activated when the reader has completed the execution of a control command. This indicator indicates to the P-C that a character is available to be entered into core storage. It is reset by the sense device command if the IOCC control word bit 15 is a one.

Punch Parity Error: This indicator indicates that when the punch buffer is being loaded, the P-C detects a parity error. It is reset by the sense device command if the IOCC control word bit 15 is a one.

Punch Response: This interrupt indicator is turned on when the punch has completed punching as directed by the execution of a write command, and indicates that the punch can accept the next command. It is reset by the sense device command if the IOCC control word bit 15 is a one.

Reader Busy. This indicator is active as a result of the reader-clutch flip-flop being on. It is on from the time a control command (start paper tape reader) is

given until data is available (approximately 15 ms). Availability of data is signaled through issuance of a reader-response interrupt.

Reader Not Ready: This indicator is on when the tape-tension switch is open. This condition exists when the paper tape is broken or not feeding freely. Manual intervention is required to clear these conditions. This indicator is also on if the reader is "busy." (See Reader Busy indicator.)

Punch Busy: This indicator is on for the total time the punch is mechanically engaged and punching a character (68 ms). During this time the punch is not able to accept another write command.

Punch Not Ready: This indicator is on when tape is not feeding freely from the tape spool, when the tape-pressure-roll holder is not down and holding the tape against the feed wheel, or when tape is not present. Manual intervention is required to clear these conditions. The indicator is also on if the punch is "busy." (See Punch Busy indicator.)

This indicator should always be tested by the program before a write command is given. If a write command is given while this indicator is on, loss of information will probably occur. No indication is given of this loss.

Reader Parity Error: This indicator indicates that when the adapter is transferring a character to the P-C, a parity error is detected in the P-C. This indicator is reset by the sense device command if the IOCC control word bit 15 is a one.

Reader Storage Protect Violation: This indicator indicates that when a tape character is being transferred to the P-C, a storage protect violation is detected in the P-C. It is reset by the sense device command if the IOCC control word bit 15 is a one.

CE Reader Busy: If the paper tape adapter is in the CE mode, this indicator replaces the busy indicator (bit 4).

C-E Reader Not Ready: If the paper tape adapter is in the CE mode, this indicator is activated along with the reader-not-ready indicator (bit 5).

CE Punch Busy: If the paper tape adapter is in the CE mode, this indicator replaces the punch-busy indicator (bit 6).

CE Punch Not Ready: If the paper tape adapter is in the CE mode, this indicator is activated along with the punch-not-ready indicator (bit 7).

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area, function and modifier bits are decoded to select the DSW to be placed on the in bus. The storage-use line (P-C line to core storage) is deactivated because the data (DSW) to be transferred from the adapter is not to be stored in core storage.

If bit 15 of the control word is a one, the DSW-reset flip-flop is turned on.

E-2 Data Cycle: A one is placed on the in bus in the bit positions associated with the status indicators that are on. The in bus is gated to the out bus during this cycle. If the DSW- reset flip-flop is on (bit 15 in E-1 cycle), the reader-response, punch-response, punch-parity, reader-parity, and reader-storage-protect flip-flops are reset by their corresponding out-bus bits.

The DSW is set into the B register, loaded into the accumulator, and the operation is terminated.

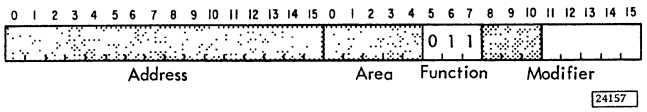
Sense Interrupt

- The interrupt level status word (ILSW), with one bit-position representing the collective status of the paper tape interrupts, is transferred to the processor-controller for program analysis.

The sense-interrupt function causes the status of the two interrupt indicators to be ORed and placed on the in bus in the position assigned to the paper tape adapter. The two interrupt indicators are reader-response and punch-response. The indicators are described in the device status word description.

The ILSW is loaded into the P-C accumulator to enable the program to determine which area or device is requesting an interrupt on the associated level.

IOCC Sense Interrupt



Address: Not used.

Area: Not used.

Function: Code 011 specifies the sense interrupt function.

Modifier: Bits 11 through 15, containing the ILSW address, are placed on the out bus automatically by the P-C during the XIO control cycle.

Interrupt Level Status Word

The 16 bits of the ILSW indicate the interrupt status of each I/O device or area that is assigned to the interrupt level specified by the IOCC modifier.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. If modifier bits 11 through 15 decode as the interrupt level to which the paper tape adapter is assigned, the function and modifier bits are decoded to condition the sense interrupt circuits.

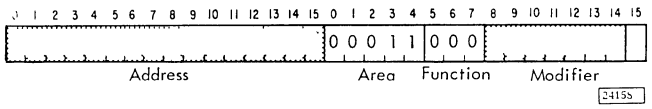
E-2 Data Cycle: The ORed outputs of the three interrupt indicators are gated to a single position on the in bus. This bit position, together with bit positions assigned to other I/O devices (areas) at this interrupt level, make up the ILSW that is transferred to the P-C and loaded into the accumulator for program analysis.

CE Mode

- Turns on, or off, the CE-mode flip-flop.

When the CE-mode flip-flop is on, interrupt and device status indicators are modified to signal the program that the paper tape adapter is in the CE mode. When in CE mode, the 1054 or 1055 interrupts on the CE interrupt level rather than on the assigned level.

IOCC CE Mode



Address: Not used.

Area: Control Word bits 0 through 4 decode as 00001 to select the paper tape area.

Function: Bits 5, 6, and 7 decode as 000 to turn on, or off, the CE-mode flip-flop in the adapter.

Modifier: Bit 15 = 1 conditions the CE-mode flip-flop to be turned on; bit 15 = 0 conditions it to be turned off.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area is decoded if there is no parity error signal from the P-C. At time-pulse-B time, the control word pulse is generated. The control-word pulse is gated by a decode of bits 5, 6, and 7 as 000 and out-bus bit 15 = 1 to turn on the CE-mode flip-flop. If out-bus bit 15 = 0 control-word and bits 5, 6, and 7 = 000 turn off the CE-mode flip-flop.

E-2 Data Cycle: A dummy cycle.

CHAPTER 1 INTRODUCTION

- The 1442 Model 6 or 7 (Figure 3-1) provides punched-card input and output for the 1800 system.
- One 1442 can be attached if a 1054/1055 is in the system. Otherwise, two 1442's can be attached.
- The 1442 connects to the processor-controller through the data channel.

READ-PUNCH FUNCTIONAL DESCRIPTION

- Processes cards serially, column-by-column, from a single hopper.
- All cards first pass the read station, then pass the punch station.
- Maximum machine speeds are:

Operation	Model	Speed
Read	6	300 cards per minute
	7	400 cards per minute
Punch	6	80 columns per second
	7	160 columns per second

- For a description of the 1442, see IBM Field Engineering Theory of Operation, 1442 Models 6 and 7. (See FE Bibliography – 1800 System, Form Y26-0560.)

Maximum reading rates are attained only when successive read-cycle commands arrive early enough to re-energize the read clutch before the clutch latch point is reached. To accomplish this, successive read-cycle commands must arrive within 35 milliseconds (25 ms for the model 7) after the operation-complete interrupt is activated by the card read punch. If a read-cycle command does not arrive within this time, the maximum reading rate becomes 285 cards per minute (cpm) for model 6 and 375 cpm for model 7.

Punching rates depend on the position of the card when the last column is punched. The punching speed ranges are

Model 6 -- 49 cpm to 255 cpm
Model 7 -- 90 cpm to 370 cpm

The approximate time required to process a single card is

Model 6 -- 12.5 ms + 12.5 ms per card-column spaced or punched
Model 7 -- 6.25 ms + 6.25 ms per card-column spaced or punched

The customer assigns the 1442 adapter to a data channel according to the priority he wishes the card read punch to have. Read and punch data is read from and stored into a data table in core storage by cycle steal cycles. For a description of data channel operations see the IBM Field Engineering, Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller. (See FE Bibliography – 1800 System, Order No. SY26-0560).

Data Coding

- The card read punch reads in either card image or packed mode and punches IBM card image only.
- Any code translation required must be done by the stored program.

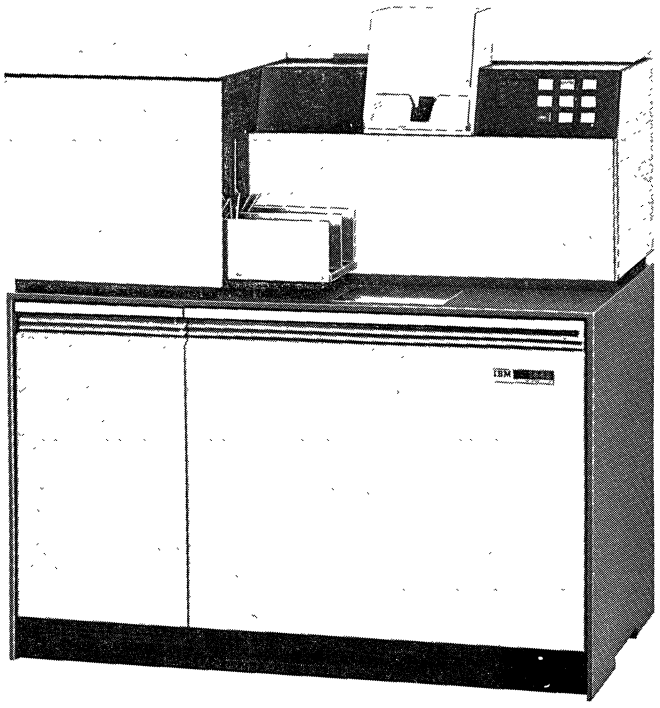


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Figure 3-1. IBM 1442 Card Read Punch

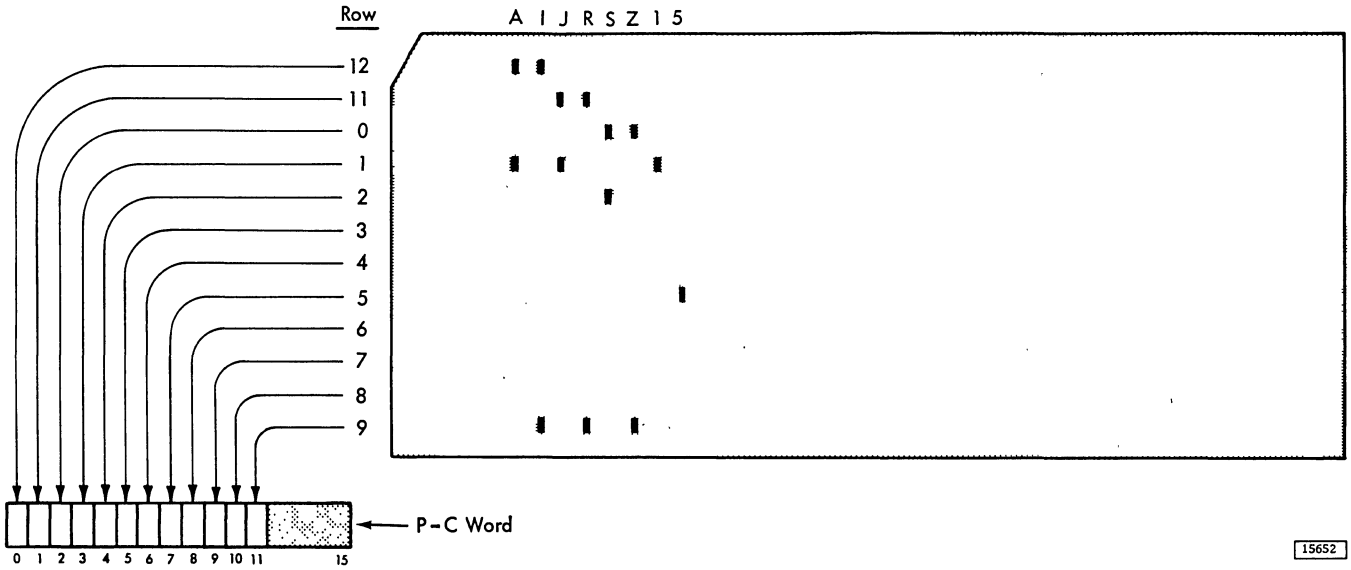

Figure 3-2. Card-Image-Mode Read

Card Image Mode: The twelve rows (12-9) in a card column correspond to the 0-11 bits respectively in core storage (Figure 3-2).

Packed Mode: Rows 12-5 of the odd-numbered columns are stored in core storage as bits 8-15. Rows 12-5 of the even-numbered columns are stored in core storage as bits 0-7 (Figure 3-3).

Initial Program Load Mode: This is a special mode, initiated by pressing the program-load key on the processor-controller console. In the load mode, data enters core storage as in the packed mode to form the load program.

Functional Keys

Start Key:

1. When initially loading the card read punch, pressing the start key causes the bottom card in the hopper to move to the read station (run in).
2. After manually stopping the card read punch, or when initiating a last card routine, the start key restores the ready status.

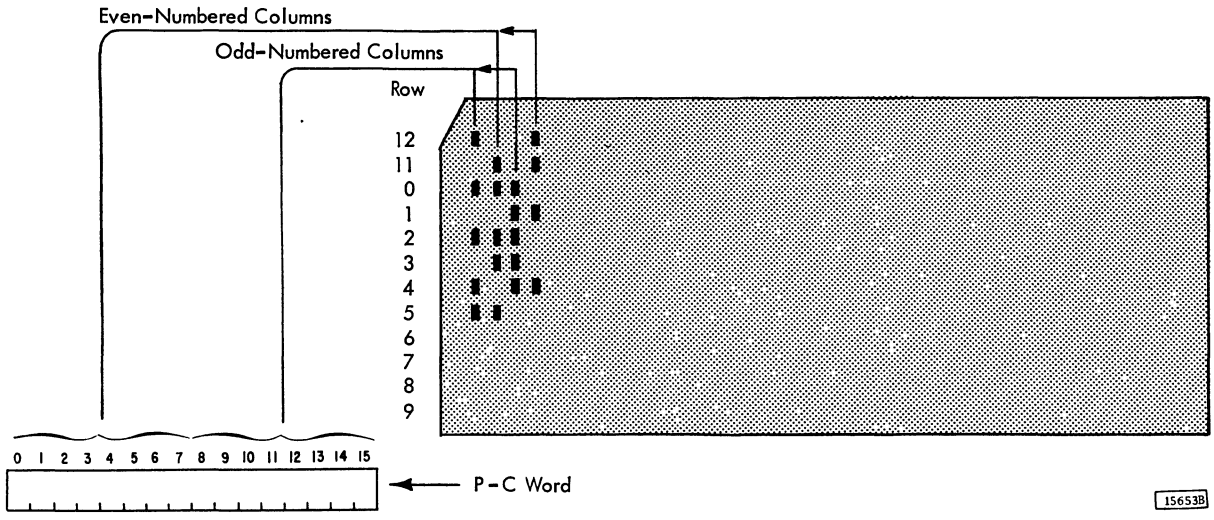

Figure 3-3. Packed-Mode Read

Stop Key: This key removes the card read punch from the ready status.

Non-Process Runout key: This key is used to eject cards from the serial path without processing them. It also resets the error latches. This key is effective only if the hopper is empty.

Indicator Light

Power on Light: This light indicates that power is supplied to the card read punch.

Check Light

Indicates that one of the eight error conditions exists. These are displayed on the back-lighted panel of the 1442 and are listed below.

Data Overrun: Indicates that data was lost because the channel failed to transfer the data to or from core storage within the time the 1442 required service.

Read Registration Check: Indicates that a read error has occurred due to incorrect registration of the card or failure of the first and second reading of a column to compare equally.

Punch Check: Indicates that a punching error has been detected.

Hopper: Indicates that a card failed to pass properly from the hopper to the read station.

Transport: Indicates a jam in the stacker.

Feed Check, Read Station: Indicates a card improperly positioned at the read station.

Feed Check, Punch Station: Indicates a card improperly positioned at the punch station.

Feed Clutch: Indicates that a feed cycle was taken that was not requested.

Chip Box Light: This light indicates that the punch chip box is either full or has been removed. This condition removes the 1442 from ready status.

Ready Light: This light indicates that the card read punch is prepared to accept instructions from the processor-controller. The following conditions are required.

1. Power on.
2. Card properly registered at the read station.
3. Either cards in the hopper or card read punch in the last-card routine.
4. Stacker not full.
5. Check light off.
6. Chip box light off.

ADAPTER FUNCTIONAL DESCRIPTION

- The 1442 adapter provides a means of attaching a card read punch unit to the 1800 system.
- The 1442 adapter is contained on one SLT board located in the 1801 or 1802 at location B2 of gate C.
- The adapter accommodates one 1442 model 6 or 7.

The 1442 adapter performs one or more of the following functions for each I/O command sent to it:

1. Decodes the function to be performed.
2. Controls the mechanical motion of the card read punch.
3. Transfers data from the P-C to the punch.
4. Transfers data from the reader to the P-C.
5. Indicates the status of the reader, punch, and adapter to the processor-controller.
6. Initiates interrupt or cycle steal cycles in the processor-controller program when the reader or punch requires service.

The adapter contains all the circuits necessary to perform these functions. For a read or punch operation, the basic data flow in the adapter is through the data register. For a read in pack mode and for IPL operations, the data flow is through the data register and the pack register. Indicators for adapter and reader-punch status, interrupt and cycle steal circuits, initial program loading, error checking, CE mode, and control circuits are also part of the adapter.

I/O INTERFACE

- The 1442 adapter connects to the 1801 or 1802 P-C channel control through the standard I/O channel interface.
- The 1442 card read punch connects to the adapter through a unique interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller. (See FE Bibliography – 1800 System, Form Y26-0560.)

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines and exits all 60 lines to the next adapter in sequence. If the 1442 adapter is the last in the sequence, the channel interface lines must be jumpered through the remaining adapter positions (dummy boards). The lines are then terminated at the mixer panel (gate H).

The 1442 adapter taps off and uses signals from these lines:

Out-bus bits 0 through 15
In-bus bits 0 through 15
Parity bit for bits 0 through 7
Parity bit for bits 8 through 15
IPL Mode
Poll Interrupt level 0-13
Poll Interrupt level 14-23
Use meter gate
Time pulse A
Time pulse B
Time pulse C
Cycle steal request F through K
Cycle steal acknowledge F through K
Cycle steal control 1
Cycle steal control 2
CAR check or Parity error
Storage protect violation
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal lines that connect the 1442 card read punch to the 1442 adapter.

The 1442 signals connect from the adapter board, through flat cable, to the processor-controller signal tailgate. Two serpent connectors and signal cables connect the interface lines to the 1442. These lines and their functions are listed in Figure 3-4.

Line	Adapter In/Out	Function
Card Feed CB 1-4 (4 lines)	In	Signals the position of the card feeding mechanism at four different points.
Punch CB 1 and 2 (2 lines)	In	Indicates to the adapter when to impulse the punch magnets and when to detect the punch echo pulses.
Read SCA 12, 11, and 0-9 (12 lines)	In	Read data to the adapter.
Read Emitter 1	In	This signal occurs near the middle of each column during a feed or read cycle.
Incremental Drive CB A and B (2 lines)	In	Signals the adapter when to impulse the incremental drive magnets
Punch Lamp Dark	In	Indicates a card is in between the read station and the punch station.
Punch Check Amp 12,11, and 0-9(12 Lines)	In	Punch echo pulses which indicate which rows were punched in the previous column.
Start Switch	In	Signals the adapter that the operator desires to place the 1442 in the ready status.
Stop Switch	In	Signals the adapter that the operator wants to stop the 1442 and remove it from the ready status.
NPRO Switch	In	When the NPRO key is depressed this line signals the adapter that the operator wants to remove the cards from the 1442 feed path without processing them.
Hopper Empty Switch	In	Indicates the hopper contains no cards.
Stacker Jam Switch	In	Indicates a card jam in the stacker transport area.
Idle Relay Contact	In	Indicates that the idle relay is activated.
Punch Magnet 12, 11, and 0-9 (12 lines)	Out	Punch data to the 1442
Ready Indicator	Out	Indicates the 1442 is ready to process cards.
Check Indicator	Out	Indicates an error condition exists that is further defined on the back-lighted panel.
Misfeed Indicator	Out	Indicates a card did not feed from the hopper during a card feed cycle.
Read Station Jam Indicator	Out	Indicates a card jam or faulty operation of the read station.
Punch Station Jam Indicator	Out	Indicates a card jam at the punch station.
Stacker Jam Indicator	Out	Indicates a card jam in the stacker transport area.
Feed Clutch Misfeed Indicator	Out	Indicates the card feed clutch made an unrequested cycle.
Read Error Indicator	Out	Indicates that data read from a card column during the first sample time was not equal to the data read at the second sample time.
Punch Error Indicator	Out	Indicates that the punch echo pulses were not equal to the data that was to be punched.
Data Overrun	Out	Indicates that data was lost because the channel failed to transfer data within the time the 1442 required service.
Process Meter	Out	Activates the process meter relay which activates the process meter.
Stacker Select Magnet	Out	Activates stacker select magnet which selects a alternate stacker.
Idle Relay	Out	Activates the idle-relay driver when the 1442 is not busy.
Motor Relay	Out	Activates the motor relay, causing the 1442 drive motor to be activated.
Feed Clutch Relay	Out	Activates the card feed clutch magnet which advances all the cards in 1442 one station.
Incremental Drive Magnet A and B (2 lines)	Out	Activates an incremental drive magnet which advances the card in the punch station one column.

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Figure 3-4. 1442 Device Interface Lines

- The interrelationship of the functional units described in this section is shown in the 1800 Maintenance Diagram Manual (MDM) page EN 20101.

FUNCTION REGISTER

- One three-position register decodes the functions for the card read punch.
- Loaded from out-bus bits 5, 6, and 7 during the XIO control cycle.

Bits 5, 6, and 7 of the IOCC control word, placed on the out bus during the XIO control cycle, are the gate inputs to the function register. The pulse that sets the register is activated by the XIO control cycle line if the card read punch area or interrupt level is on the out bus and if there is no CAR-check or parity-error indicated by the processor-controller. The function register is reset at the end of the XIO data cycle. The decoded output of the function register provides the following functions:

011 Sense Interrupt: This command directs the card read punch adapter to place its assigned interrupt-level-status-word (ILSW) bit on the in bus if any of its interrupt indicators are on. The ILSW is loaded into the P-C accumulator for program analysis.

100 Control: This command causes the card read punch to perform either a feed cycle or a stacker selection as specified by the IOCC control word modifier.

101 Initialize Write: This command causes the data in the core storage location specified by the IOCC address word to be transferred to the card read punch adapter and punched in the card.

110 Initialize Read: This command causes the 80-column card image to enter core storage, through cycle stealing, starting at the specified address.

111 Sense Device: This command causes the card read punch adapter to place its device status word (DSW) on the in bus. The DSW is loaded into the processor-controller accumulator for program analysis.

000 CE Mode: This special-use command is not decoded by the function register. It is decoded by the CE-mode circuit to place the card read punch adapter in, or take it out of, the CE mode.

DATA REGISTER

- Twelve flip-flops: position 12, 11, and 0 through 9.
- Loaded from one of three inputs for read, punch data, and punch check.
- Cleared for a read operation by the rise of each read-emitter pulse.
- Cleared for a punch operation by the TR-2 register-complement flip-flop.
- Output is gated to the punch magnets by the punch-data gate.
- Output is gated to the in bus by cycle steal acknowledge.
- Output is checked for a no-bit condition for both read and punch operations.
- Initial program load (IPL) loads and clears the data register via the read load-and-clear circuits.
- IPL mode gates the data-register and pack-register outputs to in-bus bits 0-15.

During a read or IPL operation, the data-register input is from the photo sense amplifiers. The input is gated by XIO-read or IPL-mode and set by the register-complement sample pulse. Output is to the in-bus positions shown in Figure 3-5.

During a punch-write operation, input to the data register is from out-bus bits 0 through 11. Bit 0 is

Data Reg.	In Bus Bit		
Position	Read	IPL Odd Col	IPL Even Col
12	0	8	0
11	1	9	1
0	2	10	2
1	3	11	3
2	4	12	4
3	5	13	5
4	6	14	6
5	7	15	7
6	8		
7	9		
8	10		
9	11		

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Figure 3-5. Data Register Output, Read and IPL Operation

loaded into data-register position 12; bit 1 into position 11; etc., through bit 11 which is loaded into position 9. This input is gated by a channel timing pulse. Output is gated to the punch magnets by the punch-data-gate flip-flop and turned on at T7 time of an XIO data cycle.

During a punch-check operation, input is from the punch-magnet-echo pulses, gated by the register-complement sample pulse.

Register Complement

- Two flip-flops, TR1 and TR2, shown in MDM EN 40121 and MDM EN 40131.
- During a read operation, TR1 is turned on by the read emitter.
- During a punch operation, TR1 is turned on by punch CB-1.
- TR1 is turned off by a four-megacycle oscillator.
- TR2 is turned on by TR1 going off and is turned off by the next pulse from the four-megacycle oscillator.
- The output provides data-register reset for a punch operation and gates the complementary input for punch and read operations.

Read Operation: The turning-off of TR2, while the read-SS1-gate single-shot is active, generates a register-complement sample pulse to load the data register. TR2 going off also turns on the cycle-steal-request flip-flop to initiate a data transfer. After the read-SS1-gate single-shot times out, the turning on of TR2 generates another register-complement pulse that, because the same read pulses are still active, leaves all the data register flip-flops off. When TR2 is turned off by the oscillator pulse (read-SS1-gate off), a set-read-error pulse is generated to test for a data-register-equal-zero condition.

Initial Program Load or Pack Mode Operation: With read-SS1-gate active, the turning off of TR2 gates every odd column (conditioned by odd/even flip-flop) to the pack register. TR2 going off also turns on the cycle-steal-request flip-flop after every even column.

Punch Operation: TR2 going on generates the register-complement pulse to gate the punch-echo pulses into the data register for checking. The turning-off of TR2 by the oscillator pulse generates a data-register-reset pulse, a set-cycle-steal-request pulse, and a punch-error sample pulse.

Punch Incremental Drive

- Two flip-flops, incremental-drive-A and -B.
- Shown in MDM EN 40131.
- Controlled by card-feed position and punch CB's.
- Provides punch card-feed pulses.
- Controls the data-register-complement circuit.

The incremental-drive mechanism for the punch card-feed requires two pulses for magnet energization. The drive pulses are provided by two flip-flops that are controlled by card-in-punch-station, XIO punch flip-flop, and punch CB pulses. The output also controls the turn-on of the TR1 flip-flop in the data-register-complement circuit.

CHAPTER 3 PRINCIPLES OF OPERATION

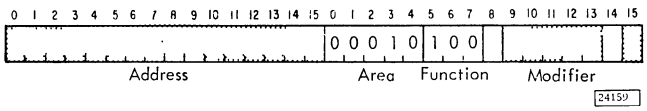
- The 1442 read and punch operations are under control of the 1800 data channel.

- Before a read or punch operation can begin, the 1442 must be placed in the ready condition (card at read station).

Control Command

- Causes the card read punch to perform either a feed cycle or a stacker select operation.

IOCC Control



Address: Not used.

Area: Control word bits 0 through 4 decode as 00010 to select the first 1442 card read punch adapter.

Function: Bits 5, 6, and 7 decode as 100 to specify a control command.

Modifier: Only bits 8 and 14 are used. Bit 8 = 1 causes a stacker select operation. Bit 14 = 1 causes a feed cycle operation

Description

E-1 Control Cycle: The IOCC control word is placed on the out bus. If bits 0 through 4 decode as 00010 and if no CAR-check-or-parity-error is indicated from the processor-controller, the set-function-register pulse is generated. Set-function-register loads out-bus bits 5, 6, and 7 into the function register. The function register activates the control-function line to the I/O monitor interface connector. This function register decode performs no other function in the adapter.

Out-bus bits 5, 6, and 7 also decode as 100 to condition the turn on of both the stacker-select and the XIO-feed flip-flops. If out-bus bit 8 = 1, the set-function-register pulse turns on the stacker-select flip-flop. If out-bus bit 14 = 1, the set-function-register pulse turns on the XIO-feed flip-flop.

E-2 Data Cycle: Dummy cycle.

Feed Cycle: The XIO-feed flip-flop activates the busy line which turns on the motor latch to start the drive motor. The busy line starts an 850-millisecond time delay to allow time for the motor to reach running speed. If the feed-interlock latch is off, the timing out of the time delay turns on the feed-clutch latch. If a card is at the punch station (Figure 3-6), the feed cycle moves it into the stacker. If a card is at the read station, the feed cycle moves it to the punch station with column-one under the punches. The feed cycle also moves a card from the hopper to the read station.

Stacker Select: During the E-1 control cycle, if out-bus bit 8 = 1, the set-function-register pulse turns on the stacker-select flip-flop. With stacker-select on, the feed CB1-2 pulse turns on the stacker-magnet flip-flop and at the same time turns stacker-select off. The stacker-magnet flip-flop activates a line to the 1442 to cause the card leaving the punch station to be selected into the second stacker.

Initialize Write Command

- A cycle steal request is sent to the processor-controller to request data transfer.

- The data at the core storage location specified by the IOCC address word is transferred to the 1442 adapter by a cycle steal cycle.

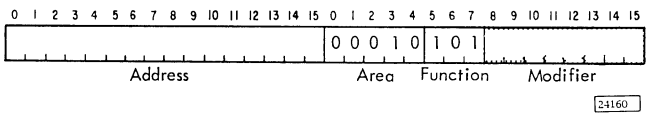
- As the data is punched, it is checked and another cycle steal request is initiated to get the data for the next column.

- At the end of the punch data, the operation-complete interrupt is initiated.

- The I/O operation diagram for the punch operation is on MDM page EN 40131.

- The timing diagram for the punch operation is on MDM page EN 70131.

IOCC Initialize Write Command



Address: These 16 bits specify the core storage location of the first word of the data table.

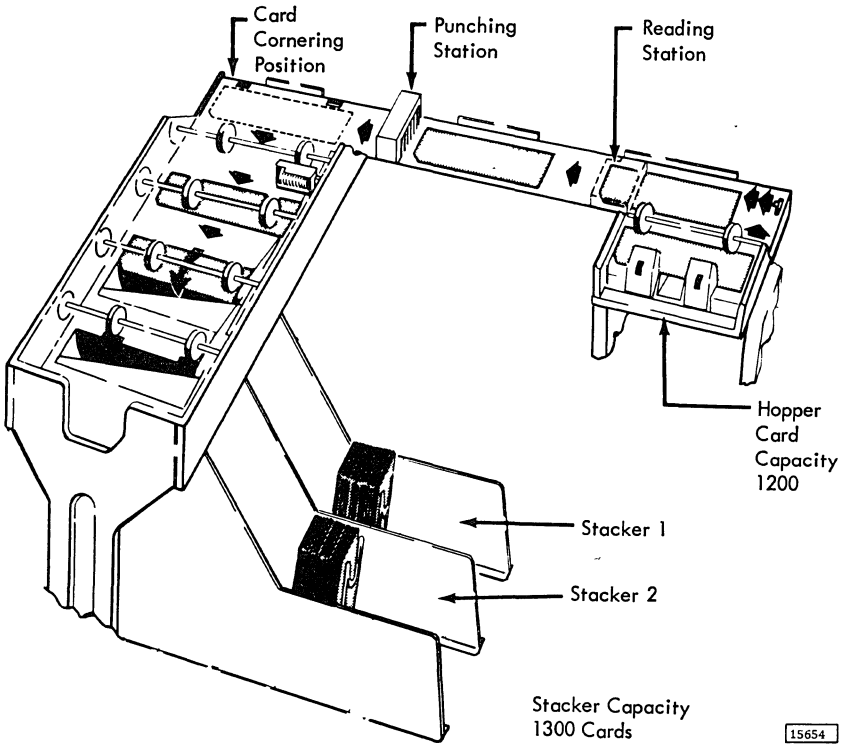


Figure 3-6. Card Path

Area: Bits 0 through 4 decode as 00010 to select the first 1442 adapter.

Function: Bits 5, 6, and 7 decode as 101 to specify the initialize write function.

Modifier: Not used.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If bits 0 through 4 decode as 00010 and there is no CAR-check-or-parity-error indicated by the processor-controller, the 1442 adapter loads its function register with out-bus bits 5, 6, and 7. The function register decodes as 101 to activate the initialize write function.

E-2 Data Cycle (Load CAR): The processor-controller places the IOCC address word on the out bus.

Initialize write and XIO data cycle AND to activate the set-address-register line. Set-address-register activates the cycle-steal-acknowledge line to the processor-controller and gates the address word into the channel address register. The channel address register addresses core storage for the cycle steal cycles that follow.

The initialize-write function conditions the XIO-punch flip-flop to be turned on at T7 time.

Punch Cycle: XIO-punch activates the busy line which starts the motor and initiates an 850-millisecond delay to allow the motor to reach operating speed. The feed clutch is then energized and a card is fed to the punch station. When the card is in the punch station, XIO-punch conditions the incremental-drive-A and -B flip-flops. The incremental-drive flip-flops are turned on by incremental-drive CB pulses to energize the incremental drive magnets.

Incremental-drive-A or -B, AND'ed with punch CB-1, activate a one-millisecond CB-1 gate. This gate turns on the register-complement-TR1 flip-flop. When TR1 is turned off by a four-megacycle oscillator, TR2 is turned on to generate the register-complement pulse. This pulse normally gates the punch-echo signals to the data register; however, during this first cycle there will be no signals because the data transfer has not taken place.

When TR2 is turned off by the four-megacycle oscillator, the set-cycle-steal-request sample pulse is generated to gate the data register output to the punch-error flip-flop and to turn on cycle steal request.

When the processor-controller services the cycle steal request, it sends a cycle steal acknowledge to the adapter. During the data cycle, the data to be punched is loaded into the data register. At the end of the cycle steal acknowledge, the data register output is gated to the punch magnets. As each column

is punched, punch echo signals are gated to the complement input of the data register. All positions should thereby be turned off.

The next time TR2 is turned off, the data register is sampled for any positions being on, the register is reset, and the cycle-steal-request flip-flop is turned on to request the transfer of the data for the next column.

Punching continues until a bit-12 is received on the out bus to turn on the last-punch flip-flop. Last-punch resets the XIO-punch flip-flop and the operation-complete flip-flop is turned on.

To eject a punched card to the stacker, the program must execute a control (feed card), an initialize read, or another initialize write command. These commands advance all the cards in the serial path.

Last Card Sequence

- When the hopper becomes empty during a feed cycle, the card-read-punch-ready status is deactivated.

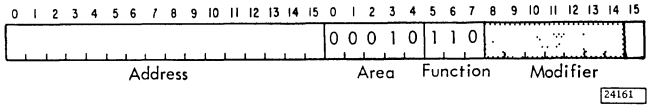
The operator may continue processing cards by loading more cards into the hopper and pressing the start key or he may initiate a last-card sequence by pressing the start key without loading more cards in the hopper. When the start key is pressed without cards in the hopper but with a card in the read station, the 1442 adapter activates the ready condition and allows two more feed cycles to be taken.

If the last-card sequence is to be entered, the program determines this through the last card indicator in the device status word. This indicator is turned on after the last card has passed the read station.

Initialize Read Command – Card Image Mode

- Initiated by an initialize read command with bit 15 equal zero.
- The 1442 reads columns 1 through 80 in one continuous motion of the card.
- Each column is read, placed in the data register, and checked.
- As soon as the data register is loaded (one column), the adapter sends a cycle steal request to the processor-controller to request a data transfer.
- The adapter sends an operation-complete interrupt to the processor-controller after all 80 columns have been read.
- The I/O operation diagram for the read operation is on MDM page EN 40121.
- The timing diagram is on MDM page EN 70121.

IOCC Initialize Read (Card Image Mode)



Address: These 16 bits specify the core storage location of the first word of the data table.

Area: Bits 0 through 4 decode as 00010 to select the first 1442 adapter.

Function: Bits 5, 6, and 7 decode as 110 to specify an initialize read command.

Modifier: Bit 15 must be a zero to specify the card-image mode of read operation. (Bit 15 = 1 would specify the pack mode.)

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If bits 0 through 4 decode as 00010 and there is no CAR-check-or-parity-error indicated by the processor-controller, the 1442 adapter loads its function register from out-bus bits 5, 6, and 7. The function register decodes as 110 to activate the initialize read function.

E-2 Data Cycle (Load CAR): The IOCC address word is placed on the out bus. Initialize read and XIO data cycle AND to activate the set-address-register line. Set-address-register activates the cycle-steal-acknowledge line to the processor-controller and gates the address word into the channel address register (CAR). The channel address register addresses core storage for the cycle steal cycles that follow.

The initialize-read-function line conditions the XIO-read flip-flop to be turned on at T7 time.

Card Read Cycle: XIO-read activates the busy line which starts the 1442 motor and initiates an 850-millisecond delay to allow time for the motor to reach operating speed. The feed clutch is then energized and a card is fed to the read station.

XIO-read and a read-emitter pulse condition the reset of the data register. This line also turns on TR1 of the register complement circuit. TR2, turned on when TR1 is turned off by a two-megacycle oscil-

lator, conditions the loading of the data register from the read photo-sense amplifiers. The I/O operation diagram for a control and read operation (MDM EN 40121) contains circuits and a timing chart that show that when XIO-read is on, read emitter pulses (one per column), through TR1 and TR2, initiate the following four functions:

1. Resets the data register
2. Loads the data register
3. Turns on the cycle-steal-request flip-flop
4. Checks the data register output

Note that there is one data-register reset, two complement-sample pulses, and two set read-sample pulses for each emitter pulse or card column. The first set-read-error pulse is not effective because the read-SS-1-gate is active. The data register is loaded with the card image by the first complement sample pulse. The same pulse that loads the data register, TR2 going off, turns on the cycle-steal-request flip-flop. During the next 100 microseconds, the data is gated onto the in bus by a cycle-steal-acknowledge signal from the processor-controller.

When the read-SS1-gate drops, TR1 turns on and is reset by the next oscillator pulse, turning on TR2. TR2 going on generates a second register-complement pulse. The same card column is being read; therefore, all positions of the data register should be complemented to the off condition.

When TR2 is turned off by the next oscillator pulse, the set-read-error pulse is generated. If any data register flip-flops are on at this time, the read-error flip-flop is turned on.

Cycle Steal Cycle: The cycle steal request, when its priority level can be serviced, initiates a cycle steal cycle. The processor-controller activates the assigned cycle-steal-acknowledge line to the 1442 adapter. The cycle-steal-acknowledge line gates the data register output onto in-bus positions 0 through 11.

The data word containing the card-column image is stored in the core storage location addressed by the channel address register. During this cycle steal cycle the channel address register is advanced one position to contain the core storage address of the next data table position for the next data word received from the 1442.

The data read from each card column is transferred to the processor-controller by cycle steal cycles until column 80 is read. After column 80 is read, the busy line is deactivated to turn on the operation-complete flip-flop. Operation-complete initiates an interrupt request to signal the program that the card has been read. To read another card, the program must execute another XIO instruction referencing an IOCC with an initialize read function specified.

Initialize Read Command - Pack Mode

- Initiated by an initialize read command with control word bit-15 = 1.
- Rows 12 through 5 of odd-numbered columns are read and loaded into the pack register for transfer and into the data register for checking.
- Even-numbered columns are read and loaded into the data register.
- Cycle steal request is sent to the processor-controller after every even-numbered column is read.
- Operation complete is turned on after column 80 is read.
- The pack mode circuits are shown on the I/O operation diagram, MDM page EN 40121.

The only difference between card-image mode and pack mode is that pack mode must read two card columns and load the data into registers to be gated to the in bus as one data word before generating a cycle steal request.

The pack-mode flip-flop, turned on by bit 15 of the initialize read command, gates the binary input of the odd/even flip-flop. Odd/even is turned on by the fall of the first-TR1 pulse and turned off by the fall of the TR1 pulse for the next column (read SS-1 gate on).

Odd/even is therefore on during the reading time of the odd-numbered columns. The on-output gates the load-pack-register SPD; it is turned on by the fall of the TR2 pulse, thereby loading the pack register (eight flip-flops) with bits 12 through 5 of the odd-numbered columns. The odd-numbered columns are read and loaded into the data register at the same time for checking purposes. Data register bits 6 through 9 are not gated to the in bus or the parity generator during pack mode operation.

The even-numbered column data is read and loaded into the data register only. The turn-on of cycle steal request is gated by the off output of the odd/even flip-flop and is turned on by the fall of the TR2 pulse. A cycle steal request is thus generated after every even-numbered column is read, resulting in 40 cycle steal requests per card.

Initial Program Load IPL)

- Reads, stores, and initiates a program.
- Reads each column as pack mode (Figure 3-3).
- After the load-card is stored, beginning at the core storage location specified by the I register (normally reset to 0000), the P-C begins execution of the instruction at 0000.
- IPL circuits that are in the 1442 adapter are shown on MDM page EN 40121.
- Processor-controller IPL circuits are shown on MDM page CC 50103.

The following procedure starts the initial program load operation.

1. Place the processor-controller mode switch in the run or the single-instruction-with-cycle-steal position.
2. Place the program deck in the 1442 hopper.
3. Press the processor-controller reset key.
4. Press the 1442 start key to cause a run-in cycle.
5. Press the processor-controller program-load key.

The program-load key turns on the IPL-mode flip-flop in the processor-controller, activating the IPL-mode line to the 1442 adapter. IPL-mode ORs with XIO-read and XIO-feed to perform the same functions that are performed by the initialize read, pack mode, command.

IPL-mode also conditions the data-register-output gating during the XIO data cycle. The output is gated to the in-bus positions as shown in Figure 3-4.

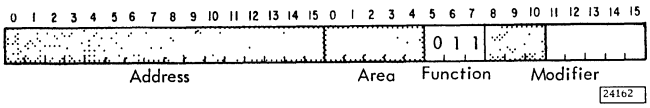
An IPL column interrupt (in bus bit 15) is activated when each even column of the card is read. This signals the P-C that the pack and read registers are loaded and starts the P-C clock. The clock runs for one cycle to transfer the pack and read register contents to core storage.

When column 80 is transferred by the IPL column interrupt, in-bus bit 14 is also activated. Bit 14 turns off the IPL-mode flip-flop to modify the IPL column interrupt sequence. This sequence causes the P-C to transfer the pack and read register contents, reset the I register to 0000, and run the clock to execute the instruction loaded at 0000.

Sense Interrupt

- Causes the operation-complete flip-flop, if on, to place its assigned bit on the in bus as part of the interrupt level status word (ILSW).
- ILSW is loaded into the processor-controller accumulator for program analysis.
- The sense-interrupt gating of the operation-complete indicator is shown on MDM pages EN 40121 and EN 40131.

IOCC Sense Interrupt



Address: Not used

Area: Not used (adapter is selected by the modifier bits).

Function: Code 011 specifies the sense interrupt command.

Modifier: Bits 11 through 15 are placed on the out bus automatically by the processor-controller during the XIO control cycle. These bits are decoded to identify the interrupt level to which the 1442 adapter is assigned.

Interrupt Level Status Word

The 16 bits of the ILSW define the interrupt status of all the I/O adapters assigned to the specified interrupt level. The 1442 adapter contains one interrupt indicator, operation-complete. The customer assigns the ILSW bit position that represents the 1442 operation-complete.

Description

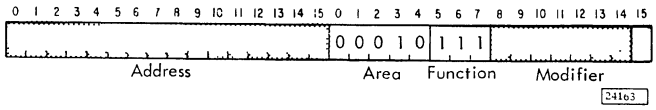
E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If the modifier bits represent the interrupt level to which the 1442 adapter is assigned, the adapter decodes the function code as 011 to specify the sense interrupt function.

E-2 Data Cycle: The sense interrupt function gates the output of the operation-complete flip-flop into the assigned in-bus position.

Sense Device

- Causes the adapter to place its device status word (DSW) on the in bus.
- The DSW is loaded into the processor-controller accumulator for program analysis.
- If specified by bit 15 of the IOCC control word, certain sensed indicators are reset.

IOCC Sense Device



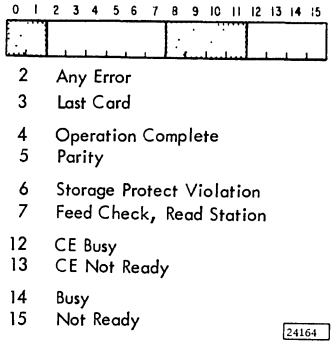
Address: Not used.

Area: Control-word bits 0 through 4 decode as 00010 to select the first 1442 adapter.

Function: Bits 5, 6, and 7 decode as 111 to cause the 1442 adapter to perform a sense device function.

Modifier: Bit 15 = 1 causes certain indicators to be reset when they are sensed.

Device Status Word



Any Error: Indicates that one or more of the following error conditions exist:

1. Parity Error.
2. Storage Protect Violation.
3. Feed Check, Read Station.
4. Data Overrun.
5. Read Registration Check.
6. Punch Check.
7. Hopper.
8. Transport.
9. Feed Check, Punch Station.
10. Feed Clutch.

Last Card: This indicator shows that column 80 has passed the read station and the hopper and read station are empty.

Operation Complete: The operation-complete interrupt occurs after a card has been read. It indicates that column 80 of the card has passed the read station. This interrupt occurs 20.6 ms after column 80 for the model 6 and 15.4 ms after column 80 for the model 7.

This interrupt also occurs after the last column to be punched has been punched and checked, and the punch drive stopped. This will occur 12.5 ms after the last terminating write function for the model 6 and 6.25 ms after the last terminating write function for the model 7.

The operation-complete interrupt also occurs if a new XIO command is given before clutch pick-up time (Feed CB-3) and one of the following feed errors is detected: mis-feed, feed check punch station, feed check read station, stacker jam.

Parity: Indicates that the processor-controller detects a CAR check or parity error during an XIO-read or XIO-punch data cycle, or, the 1442 parity-check circuits detect a parity error in the data register during a punch operation.

Storage Protect Violation: Indicates that an attempt was made to enter card column data into a protected (read only) core storage location.

Feed Check, Read Station: Indicates that a card is improperly positioned at the read station.

CE Busy: Indicates that the 1442 is busy and is in the CE mode.

CE Not Ready: Indicates that the 1442 is either not-ready or busy, and, is in the CE mode.

Busy: The busy indicator indicates that a command cannot be initiated because one is already in progress.

Not Ready: This indicator shows that the 1442 is not ready, is busy, or is in CE mode. If not busy, manual intervention is required to ensure that the following conditions are met.

1. Power On.
2. Card registered at read station (initially).
3. Cards are in hopper or last-card sequence is in progress.
4. Stacker not full.
5. Check light off.

6. If the stop key has been pressed, the start key must have been subsequently pressed.
7. Chip box not full or removed.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. The 1442 adapter decodes the area, function, and modifier bits. If bit 15 = 1, the bit-15 flip-flop is turned on.

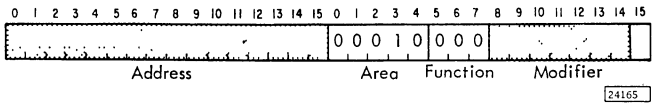
E-2 Data Cycle: The adapter places a one on the in bus in the bit positions associated with the status indicators that are on. The in bus is gated to the out bus during this cycle. If the bit-15 flip-flop is on, the operation-complete, parity-check and storage-protect-violation flip-flops are reset by their corresponding out-bus bits.

CE Mode

- Turns on, or off, the CE-mode flip-flop in the adapter.

When the CE-mode flip-flop is on, interrupt and device status indicators are modified to signal the program that the 1442 adapter is in the CE mode. When in CE mode, the 1442 interrupts on the CE interrupt level rather than on the assigned level.

IOCC CE Mode



Address: Not used.

Area: Control word bits 0 through 4 decode as 00010 to select the first 1442 adapter.

Function: Bits 5, 6, and 7 decode as 000 to turn on, or off, the CE-mode flip-flop in the adapter.

Modifier: Bit 15 = 1 conditions the CE-mode flip-flop to be turned on; bit 15 = 0 conditions it to be turned off.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area is decoded if there is no parity error signal from the P-C. At time-pulse-B time, the control-word pulse is generated. The control-word pulse, gated by bits 5, 6, and 7 = 000 and out-bus bit 15 = 1, turns on the CE-mode flip-flop. If out-bus bit 15 = 0, control-word and bits 5, 6, and 7 = 000 turn off the CE-mode flip-flop.

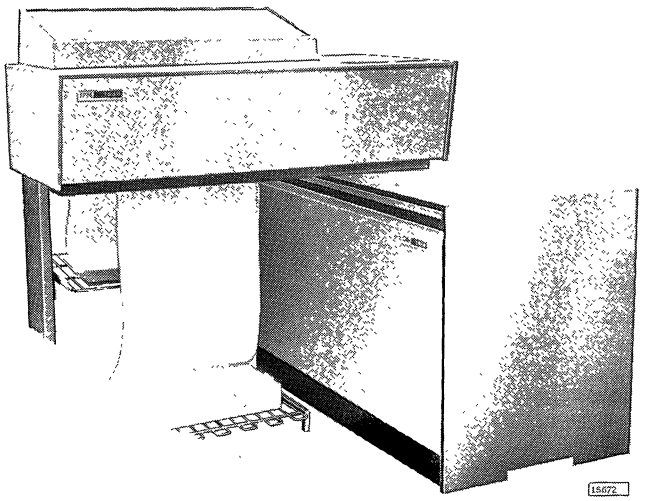
E-2 Data Cycle: A dummy cycle.

CHAPTER 1 INTRODUCTION

- The 1443 Printer (Figure 4-1) provides high-speed on-line printing capabilities for the 1800 system.
- One 1443 Printer can be attached to the system.
- Printer is buffered and operates on a data channel.
- Data to be printed must be edited and arranged in core storage in the form to be printed.
- Data format in core storage is two characters per word (Figure 4-2).

An initialize write command causes the data to be transferred from core storage to the print buffer, two characters at a time. The number of characters transferred is determined by the word count (N). (A word count of N will cause 2N characters to be transferred. The word count must not be greater than one half the number of print positions.) Once the data is transferred and the remaining positions of the print buffer have been filled automatically with blanks, the printer prints the line.

The total time demand from the processor-controller during the loading of the buffer via the data channel depends on the core storage cycle time. The time is approximately 4 (N+1) microseconds (μsec) for 4 μsec core storage, 2 (N+1) μsec for 2-μsec core storage.



Spacing and skipping of the carriage are under direct program control. Control commands are used to indicate the spacing or skipping desired before or after printing the line. The control command can be executed at any point in the program. All skip-immediate and space-immediate controls are executed by the printer when the control command has been completed. Skip-after-print and space-after-print controls are executed immediately after the printing of the next line.

PRINTER FUNCTIONAL DESCRIPTION

- For a description of the 1443 Printer, see IBM Field Engineering Theory of Operation, 1443 Printer. (See FE Bibliography – 1800 System, Order No. SY26-0560.)

Printing Speeds

The 1443 takes approximately 2 milliseconds (ms) to load its buffer. The actual line printing speed depends upon the character set in use (Figure 4-3).

Print Positions

The standard printer has 120 print positions horizontally spaced at 10 per inch. Vertical line spacing of 6 or 8 lines per inch is selected by a belt pulley adjustment on the printer carriage.

Word 1		Word 2		Word 3		Word 4		Word 5		Word 6		Word 7	
I	B	M		1	4	4	3		P	R	I	N	T

15564

Figure 4-2. Core Storage Word Format

Character Set	Lines per Minute	
	1443-1	1443-2
13	430	600
39	190	300
52	150	240
63	120	200

15565B

Figure 4-3. Printing Speeds

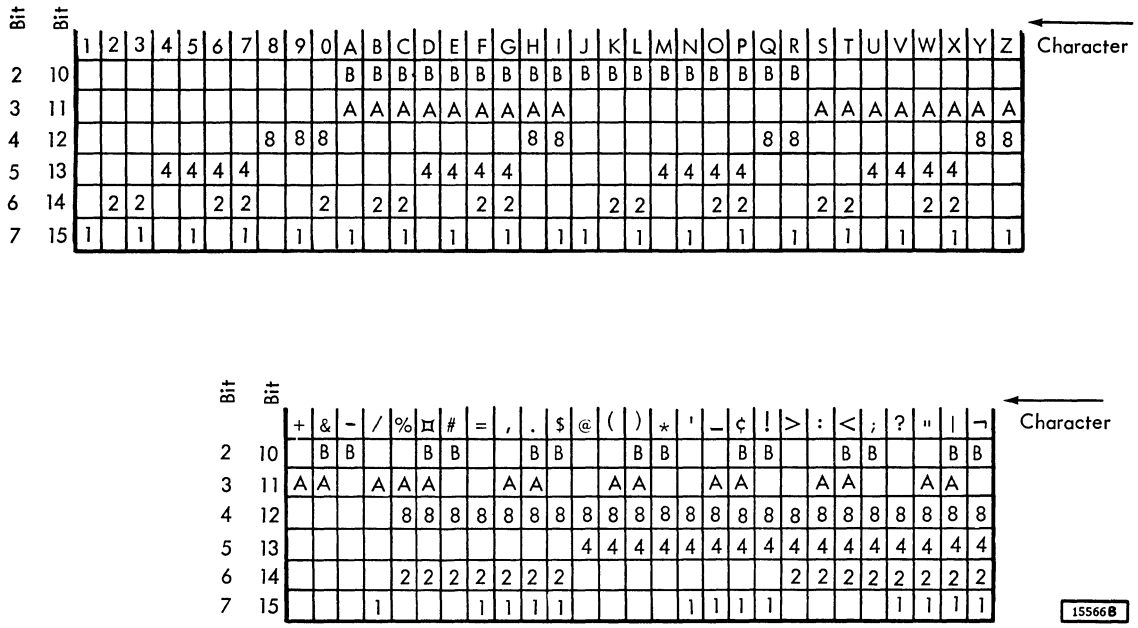


Figure 4-4. Character Coding

The 1443 option of 24 additional print positions is available.

Character Codes and Typebar Arrangements

- IBM 1800: Figure 4-4 shows the character coding required in the core storage for the corresponding printer character.

- IBM 1443: The 52-character bar is standard and is shipped with all machines; typebars with 13, 39, and 63 characters are available as additional typebars (Figure 4-5).

Forms

Continuous forms with marginal punching on both sides must be used. For more detail on forms specifications refer to IBM 1403 and 1443 Printers: Form Design Considerations (Order No. GA24-3041).

Carriage

The carriage is tape controlled and advances the form as directed by the program. The carriage control characters and their meanings are shown in Figure 4-6.

The carriage control command can be used to initiate an immediate or a delayed start for a line space or forms skip. An immediate skip or immediate space is executed at the time the control command is given. A delayed skip or delayed space is executed at the end of the next print cycle and supersedes the automatic single space after print that is given if there is no programmed carriage control.

The carriage can be single, double, or triple spaced on an immediate or delayed basis. An immediate skip or immediate space requires 45 ms for the first line and 10 ms for each additional line. A delayed space or delayed skip of one or two lines is executed as part of the 1443 print cycle. The third line adds approximately 1 ms to the print time and each additional line of a skip adds 10 ms. Sensing a punch in the 9 or 12 tape channel during spacing, sets indicators in the device status word that can be entered into the P-C accumulator by a sense device command.

The carriage is equipped with an adjustable paper brake that also functions as an end-of-forms contact. The distance between the platen and the typebar is adjustable to permit optimum printing impressions with forms of different thickness. The forms tractor on the 1443 can be positioned to approximate locations and locked to the guide. Final adjustment is accomplished with the lateral print vernier which is capable of moving each tractor a maximum of 1/2 inch.

Printer Keys and Lights

Power On: This light indicates that
to the printer control circuits

TB 63

&	-	1	/	A	J	2	S	B	K	3	T	C	L	4	U	D	M	5	V	E	N	6	W	F	O	7	X	G	P	8	Y	H	Q	9	Z	I	R	0	%	□	#	=	,	.	$	@	(	)	*	'	_	¢	!	>	:	<	;	?	"	¬			+
B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B					
A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A					A
																														8			8	8			8	8			8	8			8	8			8	8			8	8			8	8					
													4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4																4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4			
						2	2	2	2	2	2	2	2									2	2	2	2	2	2	2	2											2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2			
		1	1	1	1				1	1	1	1	1					1	1	1	1					1	1	1	1				1	1	1	1					1	1	1	1				1	1	1	1	1	1	1	1	1			

PCC Reset

TB 52

&	-	1	/	A	J	2	S	B	K	3	T	C	L	4	U	D	M	5	V	E	N	6	W	F	O	7	X	G	P	8	Y	H	Q	9	Z	I	R	0	%	□	#	=	,	.	$	@	(	)	*	'	+
B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	
A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A
																														8			8	8			8	8			8	8			8	8			8	8			8	8			
													4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4																4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	
						2	2	2	2	2	2	2	2									2	2	2	2	2	2	2	2											2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	
		1	1	1	1				1	1	1	1	1					1	1	1	1					1	1	1	1				1	1	1	1					1	1	1	1				1	1	1	1	1	1	1	1	1	1	1	1	

Sync Check

PCC Reset

TB 39

,	.	$	1	A	J	2	S	B	K	3	T	C	L	4	U	D	M	5	V	E	N	6	W	F	O	7	X	G	P	8	Y	H	Q	9	Z	I	R	0
	B	B		B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B
A	A	8		A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			A	A			8
8	8	8												4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	8	8	8	8	8	8	8	8	8
2	2	2				2	2	2	2	2	2	2	2									4	2	2	2	2	2	2	2									2
1	1	1	1	1	1				1	1	1	1	1					1	1	1	1					1	1	1	1				1	1	1	1		

Sync Check

PCC Reset

TB 13

1	2	3	4	5	6	7	8	9	0	.	*	-
										B	B	B
										A		
							8	8	8	8	8	
			4	4	4	4					4	
	2	2			2	2			2	2		
1		1		1		1		1		1		

Sync Check

PCC Reset

◡ Indicates change in PCC drive pattern

24114 B

Figure 4-5. Type Bars and Associated Bit Configurations

Immediate Skip to	Bit 2 3 4 5 6 7	Skip after Print to	Bit 2 3 4 5 6 7
Channel 1	0 0 0 0 0 1	Channel 1	1 1 0 0 0 1
Channel 2	0 0 0 0 1 0	Channel 2	1 1 0 0 1 0
Channel 3	0 0 0 0 1 1	Channel 3	1 1 0 0 1 1
Channel 4	0 0 0 1 0 0	Channel 4	1 1 0 1 0 0
Channel 5	0 0 0 1 0 1	Channel 5	1 1 0 1 0 1
Channel 6	0 0 0 1 1 0	Channel 6	1 1 0 1 1 0
Channel 7	0 0 0 1 1 1	Channel 7	1 1 0 1 1 1
Channel 8	0 0 1 0 0 0	Channel 8	1 1 1 0 0 0
Channel 9	0 0 1 0 0 1	Channel 9	1 1 1 0 0 1
Channel 10	0 0 1 0 1 0	Channel 10	1 1 1 0 1 0
Channel 11	0 0 1 0 1 1	Channel 11	1 1 1 0 1 1
Channel 12	0 0 1 1 0 0	Channel 12	1 1 1 1 0 0
Immediate Space		Space after Print	
1 Space	1 0 0 0 0 1	1 Space	0 1 0 0 0 1
2 Spaces	1 0 0 0 1 0	2 Spaces	0 1 0 0 1 0
3 Spaces	1 0 0 0 1 1	3 Spaces	0 1 0 0 1 1

15568C

Figure 4-6. Carriage Control Characters

Ready: This light indicates that the printer is ready to accept instructions from the processor-controller. The light is turned off by the stop key or carriage stop key being pressed, or the printer running out of forms.

Parity Check: This light is turned on by a parity error being detected in the printer check circuits. It is turned off by the processor-controller reset key being pressed or by the printer check indicator being program tested.

SYNC Check: This light is turned on by the type bar being improperly synchronized. This check removes the printer from the ready condition. Pressing the printer reset key turns the light off.

End of Form: This light is turned on by the last form passing the end-of-form switch lever. Printing continues until a hole is sensed in control tape channel 1. This signal turns off the ready light. Pressing the start key places the printer in the ready condition and causes the remaining lines to be printed until the next channel-1 hole is sensed.

Start: Pressing this key with power on, the type bar motor on, and paper forms in position places the printer in a ready condition.

Stop: Pressing this key removes the printer from the ready condition.

Reset: Pressing this key causes all printer check circuit indicators to be reset.

Ribbon Switch: When this switch is in the off position, the type bar motor is off; however, ribbon and typebar control circuits are still active. In the typebar-removal position, the typebar motor is off, the ribbon and typebar control circuits are de-energized, and the typebar can be removed. The switch is turned to the on position for normal printer operation.

Carriage Restore: Pressing this key positions the carriage at the next channel-1 punch of the control tape. If the carriage clutch is disengaged, the form does not move. When the clutch is engaged, the form moves in synchronization with the control tape.

Carriage Space: Pressing this key causes the form to advance one space.

Carriage Stop: Pressing this key stops carriage operation and removes the printer from the ready condition.

Carriage Clutch Knob: The carriage clutch is used to control the carriage tape drive and the form feed mechanism. When the carriage clutch knob is at the neutral position, automatic form feeding cannot take place.

ADAPTER FUNCTIONAL DESCRIPTION

- One adapter accommodates the attachment of the 1443 printer and/or the 1627 plotter to the 1800 system.
- The 1443-1627 adapter is contained on one SLT board located in the 1801 or 1802 at location B1 of gate C.
- The channel interface portion of the adapter is common to both the 1443 and 1627 control; all other circuits are unique.

The 1443 adapter circuits perform one or more of the following functions for each I/O command sent to it:

1. Decodes the function to be performed.
2. Controls the printer carriage.
3. Transfers data from the processor-controller to the 1443 print circuits.
4. Indicates the status of the printer and the adapter to the processor-controller.
5. Initiates interrupts or cycle steal cycles when the printer requires service.

Note: If the 1443 is busy or not ready, the XIO write or control command will be ignored (handled as a no-op).

The 1443 adapter contains two buffer registers, a word counter, a function register, and control circuits to implement the printer and carriage operations. Indicators for adapter and printer status, error checking circuits, and CE mode circuits are also part of the adapter.

I/O INTERFACE

- The 1443-1627 adapter board connects to the 1801 or 1802 P-C channel control through the standard I/O channel interface.

- The 1443 printer connects to the adapter through a unique interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller (See FE Bibliography – 1800 System, Form Y26-0560.)

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, and exits all 60 lines to the next adapter in sequence. If the 1443-1627 adapter is the last in the sequence, the channel interface lines must be jumpered through the remaining adapter positions (dummy boards). The lines are then terminated at the mixer panel (gate H).

The 1443 adapter taps off the signal lines that are used by both the 1443 and 1627 adapter circuits (System Diagram EJ pages). The 1443 adapter circuits use these lines:

Out-bus bits 0 through 7 and 9 through 15 (not bit 8)
In-bus bits 0 through 15 (depending on DSW and ILSW assignment)
Parity bit for bits 0 through 7
Parity bit for bits 8 through 15
Poll interrupt level 0-13
Poll interrupt level 14-23
Use meter gate
Time pulse A
Time pulse B
Time pulse C
Cycle steal request F through K
Cycle steal acknowledge F through K
Cycle steal control 0, 1, and 2
CAR check or parity error
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal and data lines that connect the 1443 adapter circuits to the 1443 printer. The printer signals connect from the adapter board, through flat cable and serpent connectors, to the P-C signal tailgate. The signals connect from the tailgate, through a serpent connector and signal cable to the printer.

The 1443 device interface lines and their functions are listed in Figure 4-7.

Line	Adapter In/Out	Function
Carriage or Printer Busy, or Skip Suppress	In	Indicates to the adapter that a line print cycle is in progress, or that the carriage is in motion. The end of the carriage or printer busy or skip suppress condition turns off the busy FF and turns on the print complete FF.
Print Ready	In	Indicates to the adapter that the printer is ready to accept a print operation start.
Print Clock Control	In	Indicates to the adapter (by initiating another cycle steal request) that the 1443 buffer has received the two output characters.
Print Check	In	Indicates to the adapter that a 1443 parity error or sync check has occurred. The parity check latch (1443) can be reset by the sense-device command or by operating either the 1443 or P-C manual reset keys. The sync check latch can be reset by the 1443 manual reset key only.
Process Release	In	Indicates to the adapter that the 1443 buffer is full.
Carriage Channel 9	In	Indicates to the adapter (by turning on the channel-9 flip-flop that the printer carriage has detected a punch in channel-9 of the carriage control tape. The adapter channel-9 flip-flop will be reset by detecting a punch in channel-12 of the control tape.
Carriage Channel 12	In	Indicates to the adapter (by turning on the channel-12 flip-flop that the printer carriage has detected a punch in channel 12 of the carriage control tape. The adapter channel 12 flip-flop will be reset by sensing a punch in channel 1 of the control tape.
Carriage Channel 1	In	This line is active only while the carriage is sensing a punch in channel 1 of the carriage control tape.
Process Bit CBA8421 (7 lines)	Out	Carries print data and carriage control bits.
Time 015-030	Out	Resets carriage latches during a carriage control operation.
Time 060-090	Out	Times the set of carriage latches during a carriage control operation. Times the turn-on of the clock control trigger which starts the 1443 clock during a print operation.
Time 090-000	Out	Times the reset of carriage latches to prevent a skip start when the carriage is already positioned at the location (channel) to which the instruction directs it.
Time 105-000	Out	Times the start of an immediate skip during a carriage control operation.
Carriage Control	Out	This gate allows timing pulses to reach carriage latches during a carriage control operation.
Print Instruction	Out	Gates time-060-090 pulse to turn on the clock control trigger which turns on the 1443 clock during a buffer load operation. Sets 1443 meter-control latch.
Print Check Reset	Out	Resets the parity-check latch.
Inhibit Print Clock Reset	Out	This line allows the printer clock to run two cycles to load the print buffer with the two print characters contained in each data word. This line also allows the printer to print blanks after the last print character is transferred.
Space Suppress	Out	Turns on the 1443 space-supp latch at the beginning of a line print operation to suppress the automatic line spacing that would normally follow the line print operation.
Meter On	Out	Indicates to the printer that the P-C process meter is running.
Reset SCM	Out	Turns on the inhibit-print-clock-reset flip-flop in the adapter, which shifts second print character of each data word from the seven-bit-serial buffer to the seven-bit-print buffer.
End of Form	Out	Active when the last form passes the end-of-form switch. Printing continues until a hole is sensed in carriage tape channel 1. This line activates the not-ready line in the adapter.

24201A

Figure 4-7. 1443 Device Interface Lines

CHAPTER 2 FUNCTIONAL UNITS

- The interrelationship of the functional units described in this section and those contained in the 1443 printer are shown on MDM page EL 201 01.

FUNCTION REGISTER

- Consists of three flip-flops and four decoding AND circuits.
- Loaded from out-bus bits 5, 6, and 7 during the XIO control cycle.

Bits 5, 6 and 7 of the IOCC control word, placed on the out bus during the XIO control cycle, are the gate inputs to the function register. The pulse that sets the register, function set, is activated by the XIO-control-cycle line if the 1443 printer area or interrupt level is on the out bus and if there is no parity error indicated by the processor-controller. The function register is reset at the end of the XIO data cycle. The decoded output of the function register provides the following functions:

011 Sense Interrupt: This command directs the 1443 adapter to place its assigned interrupt-level-status-word (ILSW) bit on the in bus if any of its interrupt indicators are on. The ILSW is loaded into the P-C accumulator for program analysis.

100 Control: This command causes the 1443 carriage to perform a space or skip operation. The carriage operation is specified by the IOCC address word.

101 Initialize Write: This command transfers data from the data table in core storage to the 1443 adapter for printing.

111 Sense Device: This command causes the 1443 printer adapter to place its device status word (DSW) on the in bus. The DSW is loaded into the P-C accumulator for program analysis.

000 CE Mode: This special use command is not decoded by the function register. It is decoded by the CE-mode circuit to place the selected printer in, or take it out of, the CE mode.

WORD COUNTER

- Consists of seven flip-flops arranged as a binary counter and a counter-zero flip-flop.
- Loaded from out-bus bits 9 through 15 during the first cycle steal cycle.
- Loaded in 1's complement form (Figure 4-8).
- Counter-1 flip-flop is complemented and the counter is advanced with each cycle steal acknowledge (each data transfer).
- Reset at the beginning of the XIO data cycle.

The word counter is loaded with the complement of the word count. Each data transfer (cycle steal acknowledge) complements the counter-1 flip-flop. Counter 1 going off turns on, or off, counter 2; counter 2 going off turns on, or off, counter 4; etc, until counter 64 going off turns on the counter-zero flip-flop. Counter-zero turns on the transfer-complete flip-flop to request a program interrupt.

Out Bus Positions	9	10	11	12	13	14	15
Word Count	0	0	0	0	1	0	0
Word Counter Positions	64	32	16	8	4	2	1
1's Complement Word Count	1	1	1	1	0	1	1

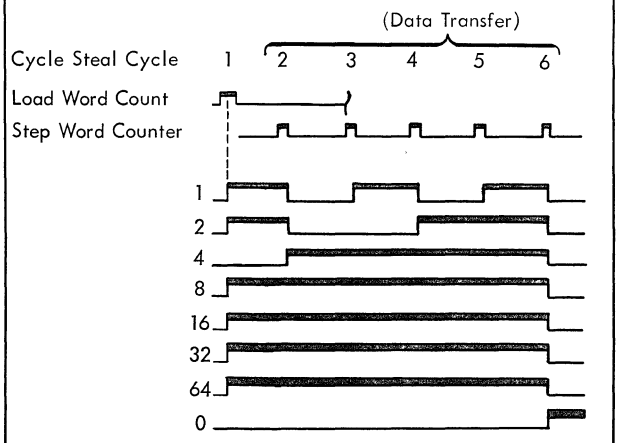


Figure 4-8. Word Count Register Load and Count

SEVEN BIT SERIAL BUFFER

- Loaded from out-bus bits 10 through 15 and the parity-bit for bits-8 through 15 during the second and subsequent cycle steal cycles.
- Contents are the second characters of each set of two characters to be printed.
- Output is gated to the seven-bit print buffer after the first of each set of two characters is sent to the 1443 print buffer.
- Reset by the 1443 cycle steal request.

SEVEN BIT PRINT BUFFER

- Loaded twice for each data transfer: once from out-bus bits 2 through 7 and the parity-bit for bits 0 through 7 (first character) and once from the seven-bit serial buffer (second character).
- Output goes to the 1443 print buffer.
- Reset by the 1443 cycle steal request.
- Position C is turned on and all others are turned off by the blank-buffer pulse when the word counter reaches zero.

TIMING PULSE GENERATOR

- Generates pulses for the 1443 printer control circuits.
- Consists of two flip-flops controlled by the 1443 control flip-flop and channel timing pulses.
- One AND circuit generates the time-060-090 pulse for the write operation.

The 1443 adapter must generate timing pulses to synchronize the printer operation with the adapter operations. These timing pulses are generated from the channel timing pulses A, B, and C, and from the various conditioning pulses in the adapter.

Figure 4-9 shows a simplified circuit and a timing diagram for the generator as it is used during a control operation. The write operation uses only one pulse, generated by cycle steal acknowledge, ANDed with channel timing pulses. The AND circuit is ORed with the time-060-090 line as shown. Note that the line names are those of the lines in the 1443 and do not indicate a time relationship.

The 015-030 pulse is issued to reset the 1443 carriage latches. The 060-090 pulse gates the output of the seven-bit print-buffer into the 1443 print buffer for a write operation and into the carriage latches for a control operation. The 090-000 pulse interlocks the carriage latch-reset circuits and the 105-000 pulse starts a carriage skip if a skip is specified.

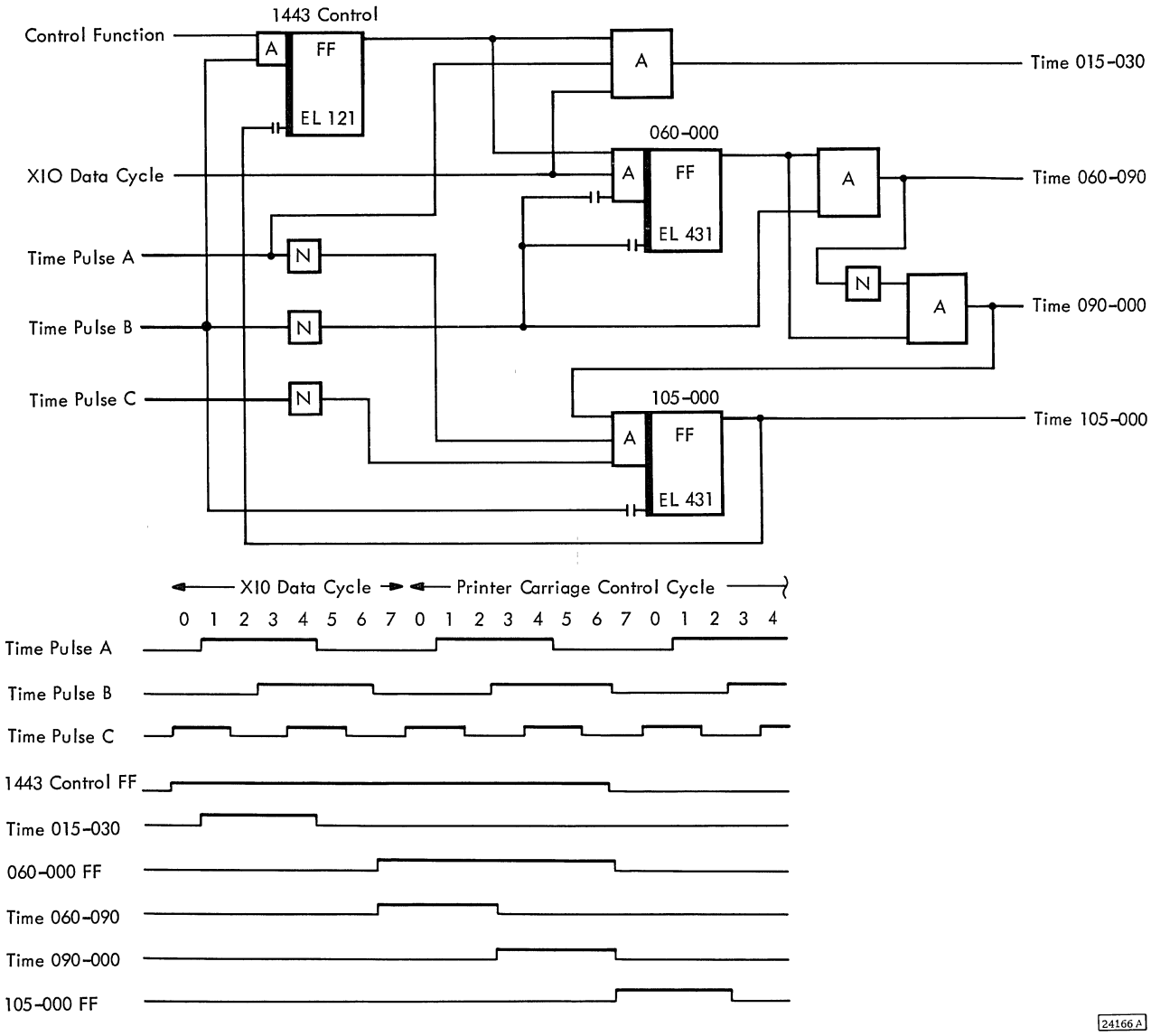


Figure 4-9. Timing Pulse Generator

- Initiated by an execute I/O (XIO) instruction that references an I/O control command (IOCC) specifying an initialize write function.

- Operation continues under data channel control.

Initialize Write

- Causes data in the table at the location specified by the address word of the IOCC to be transmitted to the 1443 buffer.

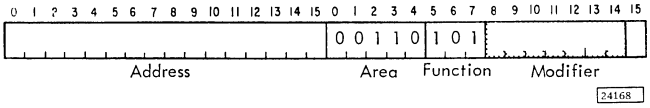
- The I/O operation diagram for the initialize write command is on MDM page EL 40131.

- The timing diagram is on MDM page EL 70101.

The word count (N) defines the number of words in the message (Figure 4-10). This results in 2N characters being sent to the buffer (two characters per word). After 2N characters have been sent to the buffer, the remainder of the buffer is filled with blanks and a 1443 print cycle is automatically taken.

The 1443 carriage will automatically take a line space after printing a line unless the space-suppress latch has been set by bit 15 of the control word.

IOCC Initialize Write



Note: If the printer is busy or not ready, the write instruction will be treated as a no-op.

Address: These 16 bits specify the core storage location of the first word of the data table shown as TA (table address) in Figure 4-10.

Area: Bits 0 through 4 decode as 00110 to select the 1443 printer adapter.

Function: Bits 5, 6, and 7 decode as 101 to condition the 1443 adapter circuits to perform one initialize-write operation.

Modifier: Bit 15 controls the space after print function.

Data Table

The first word of the data table (Figure 4-10), specified by the address word of the IOCC, contains the word count (N). The word count specifies the number of data words, each containing two print characters, that are transferred to the 1443 adapter. The word-count word and the data words are read from core storage and placed on the out bus by cycle steal cycles. The word count is loaded into the adapter word counter which is stepped once for each data word transfer. When the last data word is transferred, the word counter is advanced to a zero count to signal the program that all of the data table has been transferred.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If the area code is 00110 and there is no parity error indicated, the area, function, and modifier bits are decoded by the adapter. The initialize write function and XIO data cycle turn on the 1443-write flip-flop.

E-2 Data Cycle: The data to be printed by the 1443 is located in a data table in core storage. The IOCC address word contains the address of the first word of the data table. The processor-controller reads the IOCC address word from core storage (located at EA) and places it on the out bus.

The initialize-write function activates the reset-word-counter line that clears the word counter and forces a cycle-steal-acknowledge and cycle-steal-control signals to the data channel. The cycle-steal-acknowledge line is jumpered to the cycle steal level to which the 1443 adapter is assigned. The combined cycle steal acknowledge and control lines cause the IOCC address word to be loaded into the channel address register for this level. If a CAR check occurs during the loading of the channel address register, the 1443 adapter automatically discontinues the operation. The channel address register will address core storage for the cycle steal cycles that follow. Near the end of the data cycle, the load-word-count-cycle-steal-request flip-flop is turned on to define the next cycle. This flip-flop also turns on the attachment-cycle-steal-request flip-flop. The attachment-

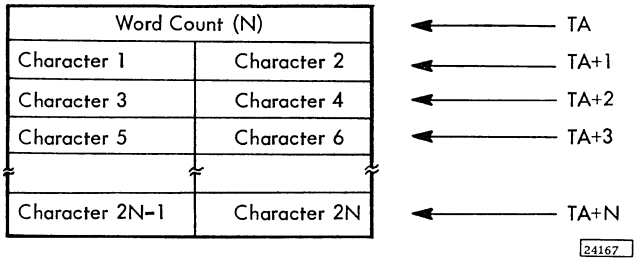


Figure 4-10. 1443 Data Table

cycle-steal-request line generates a cycle steal request to the data channel.

First Cycle Steal Cycle: When the processor-controller can service the cycle steal request, the channel address register that was loaded during the data cycle addresses the first word (word-count) of the data table. The processor-controller places this word-count word on the out bus and sends a cycle steal acknowledge to the adapter.

The fall of time-pulse-A, this time ANDed with cycle steal acknowledge, activates the set-word-counter line to gate the complement of the out-bus 9 through 15 bits into the word counter. If modifier bit 15 = 1, the space suppress flip-flop is turned on.

The attachment-cycle-steal-request line requests a second cycle steal cycle.

Second and Subsequent Cycle-Steal-Cycles: When the processor-controller can service the cycle-steal-request activated during the first cycle steal cycle, it sends a cycle-steal-acknowledge to the adapter. The channel address register was advanced one address during the previous cycle steal cycle so that it now addresses the second word of the data table (first data word). The processor-controller places this data word on the out bus.

The end of time-pulse-A turns off the attachment-cycle-steal-request flip-flop during the 2nd cycle-steal cycle. The attachment-cycle-steal-request flip-flop going off allows the printer clock to start. The printer clock is started when the adapter generates the 'CS Ack X5, 6' (060-090) pulse.

The 'CS Ack X5,6' pulse and time pulse C generate the set-print-buffer and step word counter pulses. Set-print-buffer loads data-word bits 2 through 7 and the parity-bit for bit 0-7 into the seven-bit-print buffer. The same pulse loads data-word bits 10 through 15 and the parity-bit for bits 8-15 into the seven-bit-serial buffer. The output of the seven-bit-print buffer is connected directly to the 1443.

Printer Clock Cycle: The seven-bit print word, consisting of bits C, B, A, 8, 4, 2, and 1 is gated into one position of the 1443 print buffer by a 1443 printer-clock pulse.

Four microseconds after the 1443 printer clock starts, it generates the reset-SCM pulse. Reset SCM turns on the inhibit-printer-clock-reset flip-flop to allow the printer clock to run for two cycles. The inhibit-printer-clock-reset flip-flop generates the storage register to buffer register pulse to gate the output of the seven-bit-storage register to the seven-bit-print buffer. This transfer places the second printer-word in the seven-bit print buffer and activates the data bit lines to the 1443 printer.

The inhibit-printer-clock-reset line enables the printer clock to run for another (second) cycle. The printer generates another reset-SCM to turn off the inhibit-printer-clock-reset flip-flop. The printer clock gates the second print-word into the 1443 print buffer. The printer-clock control trigger (1443) going off turns on the 1443-cycle-steal-request flip-flop in the adapter. The cycle steal request resets the seven-bit-serial buffer and seven-bit-print buffer and initiates a request for another data word transfer.

Last Data Word: On the next cycle-steal cycle after the last two characters (one data word) are transferred from core storage, the word-counter-zero flip-flop is turned on. The word-counter-zero flip-flop turns on the blank-buffer flip-flop and the transfer-complete flip-flop. Blank-buffer turns on the seven-bit-print-buffer C-bit flip-flop and turns off all other positions. The remainder of the 1443 print buffer is thereby loaded with blanks (C-bit only).

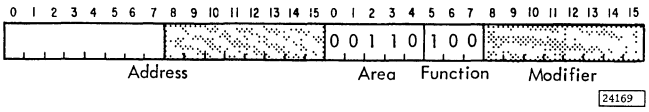
The transfer-complete flip-flop output, when conditioned by the poll-A or poll-B signal from the processor-controller, signals the program that all the data is transferred to the 1443 adapter.

Print Cycle: When the 1443 print buffer is completely loaded, the 1443 automatically takes a print cycle. If bit 15 of the IOCC control word is not a one, the space-suppress flip-flop will not be on, and, the 1443 automatically takes a line space after printing the line.

Control Command

- Initiates one of the following four carriage operations:
  - Space Immediate
  - Space After
  - Skip Immediate
  - Skip After
- Space operations can be specified as 1, 2, or 3 spaces.
- Skip operations can be specified to any carriage tape channel (1 through 12).
- The carriage operation is decoded from the IOCC address word bits 0 through 7.
- Must be given prior to the initialize write command associated with the same line of print and while the printer-not-ready indicator is off.

IOCC Control



Note: If the printer is busy or not ready the control instruction will be treated as a no-op.

Address: Bits 0 through 7 specify the carriage operation to be performed (Figure 4-6).

Area: Control word bits 0 through 4 decode as 00110 to select the 1443 adapter.

Function: Bits 5, 6, and 7 decode as 100 to specify a control command.

Modifier: Not used.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If bits 0 through 4 decode as 00110 and if no parity error is indicated from the processor-controller, the function-set line is activated. Function-set loads bits 5, 6, and 7 into the function register. The function register decoding circuits activate the control-function line.

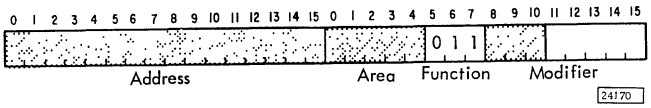
E-2 Data Cycle: The processor-controller places the IOCC address word on the out bus. At the rise of time-pulse-A, control-function generates a buffer-reset pulse to clear the seven-bit-print buffer and seven-bit-storage register. The fall of time-pulse-A generates a set-print-buffer pulse to gate out-bus bits 2 through 7 and the parity-bit for bits 0-7 into the seven bit print buffer. Set-print-buffer also gates out-bus bits 10 through 15 and the parity-bit for bits 8-15 into the seven-bit-storage register as a normal function; however, this information is not used for the control operation. Control-function and XIO data cycle turns on the 1443-control flip-flop.

Carriage Control Cycle: The 1443 timing pulse generator (Figure 4-8), described in Section 2, Functional Units, uses channel timing pulses from the processor-controller to generate timing pulses that the 1443 uses to control the carriage operation. The 015-030 pulse resets the 1443 carriage latches. Time 060-090 sets the carriage latches with the output of the seven-bit-print buffer. The 090-000 pulse is used by the printer to reset the carriage latches if a skip operation is called for and the carriage is at the specified line (punch in carriage tape channel). If print with space suppress has occurred then the skip occurs, and the reset to the carriage latches is blocked. Time 105-000 causes the carriage operation to start if the control bits sent to the carriage latches specify an immediate operation.

Sense Interrupt

- Causes the 1443 adapter to activate its assigned interrupt-level-status-word (ILSW) bit on the in bus if either the transfer-complete or printer-complete flip-flop is on.
- The ILSW is loaded into the processor-controller accumulator for program analysis.

IOCC Sense Interrupt



Address: Not used.

Area: Not used.

Function: Control-word bits, 5, 6, and 7 specify a sense-interrupt function in the adapter.

Modifier: Bits 11 through 15 are placed on the out bus automatically by the processor-controller during the XIO control cycle. These bits are decoded to identify the interrupt level to which the 1443 adapter is assigned.

Interrupt Level Status Word

The 16 bits of the ILSW define the interrupt status of all the I/O adapters assigned to the specified interrupt level. The 1443 adapter contains two indicators that can cause an interrupt. The status of these two indicators are ORed and placed in the one assigned position to indicate the interrupt status of the 1443 adapter.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If modifier bits 11 through 15 represent the interrupt level to which the 1443 adapter is assigned, the adapter decodes the function code as 011 to specify the sense-interrupt function.

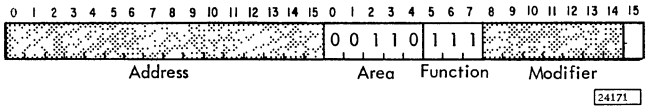
E-2 Data Cycle: The sense-interrupt function gates the output of the transfer-complete flip-flop ORed

with the output of the printer-complete flip-flop into the assigned in-bus position.

Sense Device

- Causes the adapter to place its device status word (DSW) onto the in bus.
- The DSW is loaded into the processor-controller accumulator for program analysis.
- If specified by bit 15 of the IOCC control word, certain sensed indicators are reset.

IOCC Sense Device



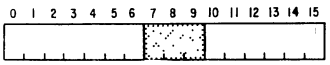
Address: Not used.

Area: Control-word bits 0 through 4 decode as 00110 to select the first 1443 printer adapter.

Function: Bits 5, 6, and 7 decode as 111 to cause the 1443 adapter to perform a sense-device function.

Modifier: Bit 15=1 causes certain indicators to be reset when they are sensed.

Device Status Word



0 Transfer Complete
1 Error
2 Printer Complete
3 Channel 9
4 Channel 12
5 Channel 1
6 Parity
10 CE Carriage Busy
11 CE Printer Busy
12 CE Printer Not Ready
13 Carriage Busy
14 Printer Busy
15 Printer Not Ready 24172

Transfer Complete: This interrupt occurs when the word count (N) has been reduced to zero by the channel controls. This indicates that 2N data characters have been transmitted to the printer buffer. Once this interrupt occurs, the P-C program can start storing the next line of print into the data table. This indicator is turned off by the sense device command if bit 15=1.

Error: This indicator is turned on by a parity check or sync check in the printer, or by a parity error detected in the processor-controller during a data-transfer cycle-steal-cycle. These errors can occur randomly during the program execution because the printer is buffered and data is transferred by cycle steal cycles.

The execution of a sense-device command, with IOCC control-word bit 15=1, resets the error indicator if a printer parity error turned it on. If a sync check turned it on, the sense-device operation does not reset it.

The processor-controller reset turns off the indicator if a printer parity check or a processor-controller parity check turned it on. The 1443 reset turns off the indicator if a 1443 parity error or sync check turned it on.

Printer Complete: This interrupt occurs when the printer has completed a print or control operation. It signals that the next line of data can be transmitted to the 1443 buffer. This indicator is turned off by the sense-device command if bit 15 = 1.

Channel 9: This indicator is turned on when a punched hole is detected in channel 9 of the carriage control tape. This indicator is turned off when a hole is detected in channel 12 of the carriage control tape.

Channel 12: This indicator is turned on when a punched hole is detected in channel 12 of the carriage control tape. This indicator is turned off when a hole is detected in channel 1 of the carriage control tape.

Channel 1: This indicator is on only while a punched hole in channel 1 of the carriage control tape is being sensed.

Parity: This indicator is turned on by a channel-address-register (CAR) check or parity check in the processor-controller during a cycle steal cycle. This indicator is turned off by the sense-device command if bit 15 = 1.

CE Carriage Busy: This indicator indicates that the 1443 attachment is in CE mode and the buffer is loading, printing is in progress, or the carriage is in motion. Sensing this indicator does not reset it.

CE Printer Busy: This indicator indicates that the 1443 attachment is in CE mode and the buffer is loading, printing is in progress, or the carriage is in motion. Sensing this indicator does not reset it.

CE Printer Not Ready: This indicator indicates one of the following conditions:

The 1443 attachment is in CE mode and CE printer busy is on as indicated above.
The 1443 is physically unable to accept an instruction.
The end-of-forms latch in the 1443 is on.

This indicator should be tested prior to execution of an XIO control or initialize write command to the 1443 if the 1443 attachment is in CE mode.

Sensing this indicator does not reset it.

Carriage Busy: This indicator indicates that the buffer is loading, printing is in process, or the carriage is in motion. Sensing this indicator does not reset it.

Printer Busy: This indicator indicates that the buffer is loading, printing is in process, or the carriage is in motion. Sensing this indicator does not reset it.

Printer Not Ready: This indicator indicates one of the following conditions:

The printer-busy indicator is on, as defined above.
The 1443 is physically unable to accept an instruction.
The end-of-form latch is on.
The 1443 attachment is in CE mode.

Sensing this indicator does not reset it.

This indicator should be tested prior to execution of an XIO control or initialize write command to the 1443.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. The 1443 adapter decodes the area, function, and modifier bits. If bit 15=1, the bit-15 flip-flop is turned on.

E-2 Data Cycle: The adapter activates the position of the in bus associated with the status indicators that are on. The in-bus is gated to the out-bus during this cycle. If the bit-15 flip-flop is on, any of the following indicators that place a bit on the in-bus will be reset by the corresponding position of the out-bus:

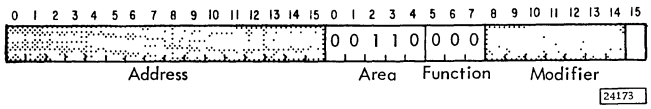
1. Transfer Complete
2. Error
3. Print Complete
4. Parity

CE Mode

- Turns on, or off, the CE-mode flip-flop in the adapter.

When the CE-mode flip-flop is on, interrupt and device status indicators are modified to signal the program that the 1443 adapter is in the CE mode. When in CE mode, the 1443 interrupts on the CE interrupt level rather than on the assigned level.

IOCC CE Mode



Address: Not used.

Area: Control-word bits 0 through 4 decodes as 00110 to select the 1443 adapter.

Function: Bit 15=1 conditions the CE-mode flip-flop to be turned on; bit 15=0 conditions it to be turned off.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area is decoded if there is no parity error signal from the P-C. At time-pulse-B time, the function-set pulse is generated. The function-set pulse, gated by bits 5, 6, and 7 = 000 and out-bus bit 15=1, turns on the CE-mode flip-flop. If out-bus bit 15 is a zero function-set and bits 5, 6, and 7 = 000 turn off the CE-mode flip-flop.

E-2 Data Cycle: A dummy cycle.

CHAPTER 1 INTRODUCTION

- Models 1 (Figure 5-1) and 2 provide incremental plotting capabilities for the 1800 system.
- One 1627 Plotter can be attached to the system.
- Produces output in the form of bar charts, flow charts, engineering drawings, etc.
- Operates under direct program control.

PLOTTER FUNCTIONAL DESCRIPTION

- Data from the processor-controller core storage is translated into 1627 actuating signals and converted to incremental plotter movements.
- X-Y increment speed for Model 1 is 300 steps per second; for Model 2, it is 200 steps per second.
- Pen-status-change speed is 600 operations per minute.
- Increment size is 1/100 inch.
- Plotting area for Model 1: 11 inches by 120 feet.
- Plotting area for Model 2: 29-1/2 inches by 120 feet.
- For a detailed description of the plotter, see IBM Field Engineering Theory-Maintenance, 1627 Plotter (see FE Bibliography – 1800 System, Form Y26-0560).

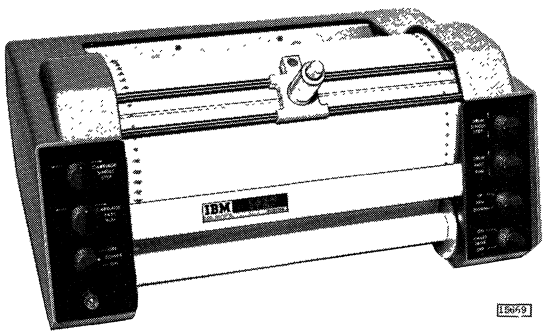


Figure 5-1. IBM 1627 Plotter

The actual recording is produced by incremental movement of the pen on the paper surface (y-axis) and/or the paper under the pen (x-axis). The pen is mounted in a carriage that travels horizontally across the paper as viewed from the front of the plotter. The vertical plotting motion is achieved by rotation of the pin feed drum, which also acts as a platen (Figure 5-2).

The drum and the pen carriage are bi-directional; that is, the paper moves up or down and the pen moves right or left. Control is also provided to raise or lower the pen from or to the paper surface. The pen remains in the raised or lowered position until directed to change to the opposite status.

The drum and pen-carriage movements and the pen status are controlled by digits transferred to the 1627. Each output word is decoded into a directional signal which causes a 1/100-inch incremental movement of the pen carriage (Figure 5-3) and/or paper, or a raise-pen or a lower-pen movement. The motion or action resulting from each word in the output record is shown in Figure 5-4.

As shown in Figure 5-4, a valid combination of bits 1 through 4 (1/4, 1/3, 2/4, 2/3) causes a diagonal line.

Opposing command-bit combinations (1/2 and 3/4) are invalid, and should not be used.

The time required for execution of raise-pen and lower-pen commands is 100 milliseconds (ms). The time to plot a point is approximately 5 ms

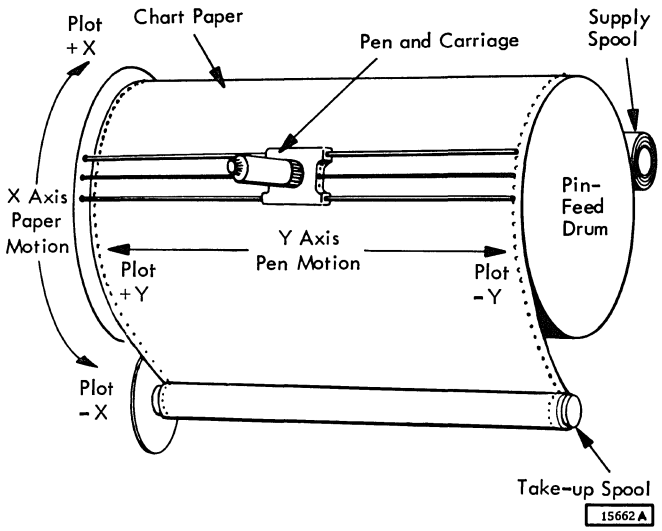


Figure 5-2. Paper and Pen Motions

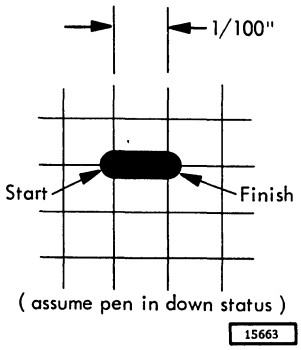
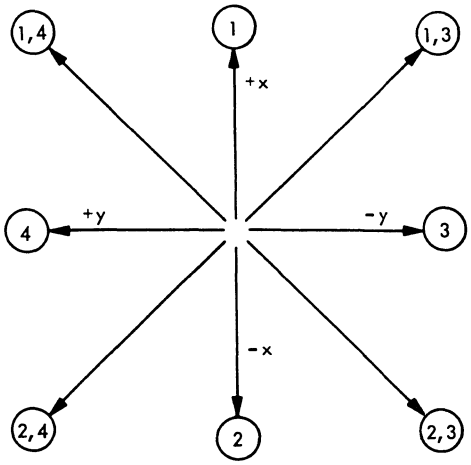


Figure 5-3. Plotter Result for One Horizontal (Y Axis) Movement



Pen
B5 - Raise Pen
B0 - Lower Pen

NOTE: The encircled numerical figures are the P-C word bit positions that correspond to the indicated direction of plotting movement as viewed from the front of the plotter. Normally, graphs are plotted so that their horizontal axes are, in reality, the X axis as shown above. 15661

Figure 5-4. Output Record Control

(3.3 ms for 300 steps/sec). In order to keep the plotter operating at full speed, the next control character must be sent to the plotter 0.5 ms after the service-complete interrupt.

The timing circuits in the plotter control can be adjusted by an IBM Customer Engineer to the correct speed for either plotter model at installation time or during service.

1627 Operating Controls

- Seven operating controls and one power-on light are mounted on the front panels of the 1627 (Figures 5-5, 5-6).
- A description of the function of each control follows:

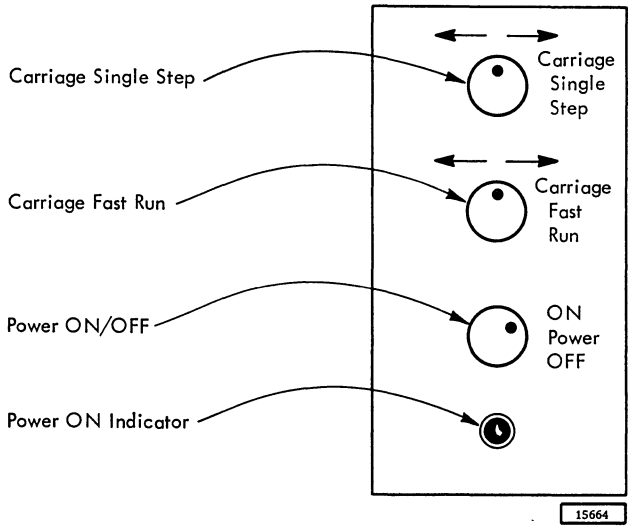


Figure 5-5. Left Console Controls

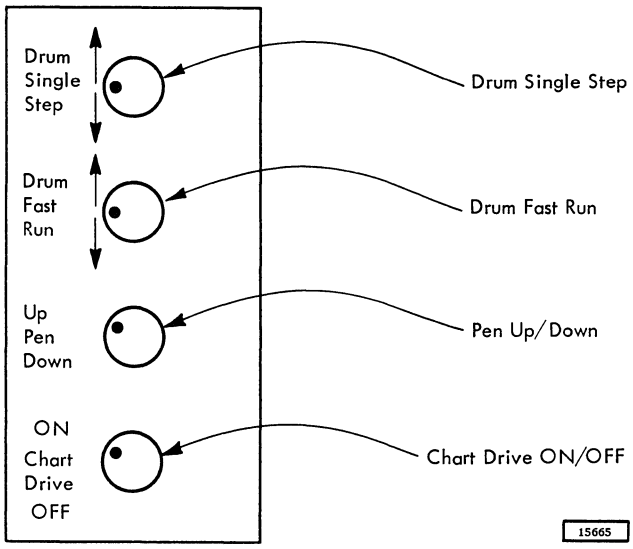


Figure 5-6. Right Console Controls

Power: This switch connects power from the 1800 to the 1627. There is no "power-on delay" involved with the 1627 power switch; that is, the plotter can operate as soon as the switch is turned on. A power-on light, associated with this switch, indicates when power is on.

Carriage Fast Run: This switch allows the pen carriage to be stepped rapidly to the left or right at the rate of 120 steps a second. The carriage-fast-run switch is used to move the carriage to any desired area of the graph.

Carriage Single Step: This switch allows the pen carriage to be moved in single-step increments (1/100-inch) either left or right. The carriage single step switch permits the operator to accurately align the carriage along the y-axis of the chart.

Drum Fast Run: This switch allows the drum to move the paper rapidly up or down at the rate of 120 steps a second. The drum-fast-run switch is used in conjunction with the carriage fast run switch to position the pen to any desired area of the graph.

Drum Single Step: This switch allows the drum to be rotated in single-step increments (1/100-inch) in either direction. The drum-single-step switch is used in conjunction with the carriage-single-step switch to permit the operator to accurately align the pen on a point or fixed coordinate on the graph.

Pen: This switch provides a means for manually raising the pen from the surface of the drum or lowering the pen to the drum.

Chart Drive: This switch allows the front and rear chart drives to be disabled. When recording on single sheets of graph paper, the chart drive switch should be in the off position. When recording on roll-paper this switch should be in the on position.

Vernier Control: Large size chart paper may vary in width due to high or low humidity; therefore a vernier control is provided on the 1627, Model 2, to vary the size of the pen carriage increments. In this way, the pen traverse is adjusted to match the printed scale of the chart paper. The vernier control knob is located at the left end of the drum above the switch panel. For work with non-scale paper, the control should be centered at the zero position.

ADAPTER FUNCTIONAL DESCRIPTION

- One adapter accommodates the attachment of the 1627 plotter and/or the 1443 printer to the 1800 system.
- The 1443-1627 adapter is contained on one SLT board located in the 1801 or 1802 at location B1 of gate C.
- The channel interface portion of the adapter is common to both the 1443 and 1627; all other circuits are unique.

The 1627 adapter circuits perform one or more of the following functions for each I/O command sent to it:

1. Decodes the function to be performed.
2. Controls the plotting according to the data words received from the processor-controller.
3. Indicates the status of the plotter and the adapter to the processor-controller.
4. Initiates interrupts in the processor-controller program when the plotter requires service.

The 1627 adapter contains a function register, a buffer register and control circuits to implement the plotting of data. Indicators for plotter and adapter status and CE mode circuits are also part of the 1627 adapter.

I/O INTERFACE

- The 1443-1627 adapter connects to the 1801 or 1802 P-C channel control through the standard I/O channel interface.
- The 1627 plotter connects to the adapter through a unique interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller. (See FE Bibliography – 1800 System, Form Y26-0560.)

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, and exits all 60 lines to the next adapter in sequence. If the 1443-1627 adapter is the last in the sequence, the channel interface lines must be jumpered through the remaining adapter positions (dummy boards). The lines are then terminated at the mixer panel (gate H).

The 1443-1627 adapter taps off the signal lines that are used by both the 1443 and 1627 circuits (Sys-

tem Diagram EJ pages). The 1627 adapter circuits use these lines:

Out-bus bits 0 through 7 and 11 through 15 (not bits 8, 9, 10)
In-bus bits 0 through 15 depending on DSW and ILSW assignment
Poll interrupt level 0-13
Poll interrupt level 14-23
Time pulse A
Time pulse B
Time pulse C
CAR check or parity error
Storage protect violation
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal and power lines that connect the 1627 plotter to the 1443-1627 adapter and to the power supplies. The plotter signals connect from the adapter board, through flat cable, to a twist connector at the P-C power tailgate. From the power tailgate, the signal and power supply lines connect to the 1627 plotter. These lines and their functions are listed in Figure 5-7.

Line	Adapter In/Out	Function
Drum Up	Out	Pen plots vertically, paper moves upward (+X).
Drum Down	Out	Pen plots vertically, paper moves downward (-X).
Carriage Left	Out	Pen plots horizontally to the left (+Y).
Carriage Right	Out	Pen plots horizontally to the right (-Y).
Pen Up	Out	Raise pen from paper.
Pen Down	Out	Pen contacts paper.
Plotter Ready	In	Power is on and plotter drive is on.
115 vac	Out	Two lines are used to provide power to plotter motor.
115 ac Common	-	Tied to frame ground on plotter.

24202

Figure 5-7. 1627 Device Interface Lines

- The interrelationship of the functional units described in this section is shown in the 1800 Maintenance Diagram Manual (MDM) page EK 40101.

FUNCTION REGISTER

- Consists of three flip-flops and three decoding AND circuits.
- Loaded from out-bus bits 5, 6, and 7 during the XIO control cycle.

Bits 5, 6, and 7 of the IOCC control word, placed on the out bus during the XIO control cycle are the gate inputs to the function register. The pulse that sets the register, control-word, is activated by the XIO-control-cycle line if the 1627 area or interrupt level is on the out bus and if there is no parity error indicated by the processor-controller (P-C). The function register is reset at the end of the XIO data cycle. The decoded output of the function register provides for the following functions:

001 Write: This command sends the P-C word at the core storage location specified by the IOCC address word to the 1627 plotter.

011 Sense Interrupt: This command directs the 1627 adapter to place its assigned interrupt-level-status word (ILSW) bit on the in bus if the service-response indicator is on. The ILSW is loaded into the P-C accumulator for program analysis.

111 Sense Device: This command transfers the 1627 device status word (DSW) to the P-C for program analysis. The DSW indicates the status of the 1627 indicators.

000 CE Mode: This special use command is not decoded by the function register. It is decoded by the CE-mode circuit to place the plotter in, or take it out of, the CE Mode.

PLOTTER CONTROL BUFFER

- Consists of six flip-flops: drum-up, drum-down, carriage-right, carriage-left, pen-up, and pen-down.
- Loaded from out-bus bits 0 through 5 at T6 time of the data cycle.
- Output goes to plotter control circuits.
- Single-shot circuits reset the buffer.

The out-bus bits turn on the buffer positions as follows:

Bit	Control
0	Pen Down
1	Drum Down
2	Drum Up
3	Carriage Right
4	Carriage Left
5	Pen Up

The output of each flip-flop goes directly to a magnet driver which connects to the 1627 control circuits.

When either the pen-up or pen-down flip-flop turns on, the shift of the on output starts two 50-millisecond single-shots in tandem. The busy line is active for the combined 100 milliseconds. The timing-out of the second single-shot resets the pen-up and pen-down flip-flops.

Any of the other four buffer flip-flops, drum and carriage controls, start two single-shots in tandem. These single-shots are 1.9 milliseconds for the 1627 Model 1 or 2.9 milliseconds for the 1627 Model 2. The timing-out of the second flip-flop resets these four buffer flip-flops.

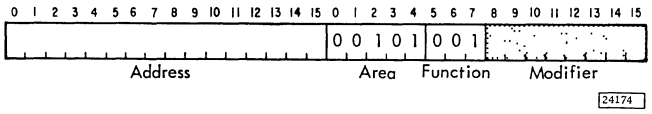
CHAPTER 3 PRINCIPLES OF OPERATION

- The 1627 plotter operates under direct-program-control of the 1800 system.
- Each incremental movement of the pen or drum requires an XIO instruction that references an IOCC with a write function.
- The write command sends a data word to the plotter adapter to control the plotter movements.
- The plotter adapter sends a service-response interrupt to the processor-controller when the plotter movement is complete.
- The I/O operation diagram for the plotter is on MDM page EK 40101.
- The timing diagram is on MDM page EK 70111.

Write

- Initiated by an execute I/O (XIO) instruction that references an I/O control command (IOCC) specifying a write function.
- Data word, at core storage location specified by IOCC address word, specifies the plotter operation.

IOCC Write



Address: These 16 bits specify the core storage location of the data. It is used during the XIO data cycle (E-3).

Area: Bits 0 through 4 decode as 00101 to select the 1627 plotter adapter.

Function: Bits 5, 6, and 7 are loaded into the adapter function register during the XIO control cycle (E-1). These bits decode as 001 to specify the write function.

Modifier: Not used.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. If the area (bit 0 through 4) decodes as 00101 and if there is no parity error indicated by the processor-controller, bits 5, 6, and 7 are loaded into the function register. The decoded output of the function register is used during the E-3 data cycle.

E-2 Cycle: The processor-controller loads the IOCC address word into the accumulator for use in the E-3 data cycle.

E-3 Data Cycle: The processor-controller uses the IOCC address word to address core storage. The data word is read from core storage and placed on the out bus.

At T6 time of this cycle, the set-buffer pulse is generated to gate the data word bits from the out bus (bits 0 through 5) into the buffer-register. The output of each buffer register flip-flop goes directly to a magnet driver that connects to the plotter control circuits.

The on output of any of the drum or carriage control flip-flops (drum-up, drum-down, carriage-right, carriage-left) start a single-shot that activates the busy line. The timing-out of this single-shot starts another single-shot that keeps the busy line active. Both of these single-shots are 1.9 milliseconds for the 1627 Model 1 and are 2.9 milliseconds for the 1627 Model 2.

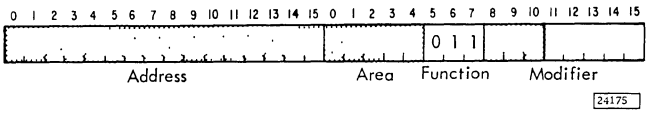
The timing-out of the second single-shot turns on the response flip-flop. When the interrupt polling pulse for the assigned interrupt level becomes active, a service-response interrupt request is sent to the processor-controller. This interrupt signals to the program that the plotter write operation is completed.

Similarly, when either the pen-up or pen-down flip-flop is turned on, the on output starts a 50-millisecond single-shot that activates the busy line. The timing-out of this single-shot starts another 50-millisecond single-shot that keeps the busy line active. The timing out of this second single shot turns on the response flip-flop.

Sense Interrupt

- Places a bit on the in bus, as part of the interrupt status word, if the response flip-flop is on. The in-bus position is assigned by the customer.
- The interrupt status word is loaded into the processor-controller for program analysis.

IOCC Interrupt



Address: Not used.

Area: Not used. The 1627 adapter is selected by the modifier bits.

Function: Code 011 specifies the sense-interrupt command.

Modifier: Bits 11 through 15 are placed on the out bus automatically by the processor-controller during the XIO control cycle. These bits are decoded to identify the interrupt level to which the 1627 adapter is assigned.

Interrupt Level Status Word (ILSW)

The 16 bits of the ILSW define the interrupt status of all the I/O adapters assigned to the interrupt level specified by the IOCC modifier. The 1627 adapter contains one interrupt indicator, service response. The customer assigns the ILSW bit position that represents the 1627 service response.

Description

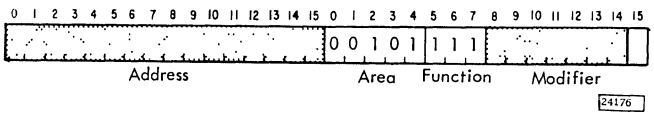
E-1 Data Cycle: The processor-controller places the IOCC control word on the out bus. If the modifier bits represent the interrupt level to which the 1627 adapter is assigned, the adapter decodes the function code. A function code of 011 specifies the sense-interrupt function.

E-2 Data Cycle: The sense-interrupt function gates the output of the service-response flip-flop onto the assigned in-bus position.

Sense Device

- Causes the 1627 adapter to place its device status word (DSW) onto the in bus.
- The processor-controller loads the DSW into the accumulator for program analysis.
- If specified by bit 15 of the IOCC control word, the service-response and parity indicators are reset.

IOCC Sense Device



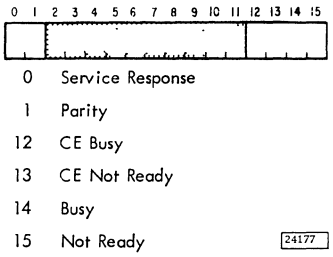
Address: Not used.

Area: Control word bits 0 through 4 decode as 00101 to select the 1627 adapter.

Function: Bits 5, 6, and 7 decode as 111 to cause the 1627 adapter to perform a sense-device function.

Modifier: Bit 15 = 1 causes the response and parity flip-flops to be reset when they are sensed.

Device Status Word



Service Response: This interrupt indicator is turned on when the 1627 has completed the operation specified by the last write command. This indicator is reset by the sense-device command if modifier bit 15 = 1.

Parity: Indicates that a parity error was detected by the processor-controller when the plotter buffer was being loaded. This indicator is reset by the sense-device command if modifier bit 15 = 1.

CE Busy: If the plotter adapter is in the CE mode, this indicator replaces the busy indicator (bit 14).

CE Not Ready: If the plotter adapter is in the CE mode, this indicator replaces the not-ready indicator (bit 15).

Busy: This indicator is on from the time the plotter buffer is loaded until enough time has elapsed to allow the specified operation to be completed.

Not Ready: This indicator, when on, indicates that the 1627 is not powered or otherwise ready, or the adapter is in the CE mode.

Description

E-1 Control Cycle: The processor-controller places the IOCC control word on the out bus. The 1442 adapter decodes the area, function, and modifier bits. If bit 15 = 1, the bit-15 flip-flop is turned on.

E-2 Data Cycle: The adapter places a one on the in bus in the bit positions associated with the status indicators that are on. The in bus is gated to the out bus during this cycle. If the bit-15 flip-flop is on, the service-response and parity flip-flops are reset by their corresponding out-bus bit.

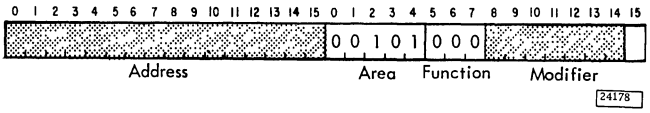
CE Mode

- Turns on,or off,the CE-mode flip-flop in the adapter.

The CE-mode flip-flop, when on, causes interrupt and device status indicators to be modified to signal the program that the 1627 adapter is in CE mode.

When in CE mode, the 1627 interrupts on the CE interrupt level rather than on the assigned level.

IOCC CE Mode



Address: Not used.

Area: Control-word bits 0 through 4 decode as 00101 to select the 1627 adapter.

Function: Bits 5, 6, and 7 decode as 000 to turn on, or off, the CE-mode flip-flop in the adapter.

Modifier: Bit 15 = 1 conditions the CE-mode flip-flop to be turned on; bit 15 = 0 conditions it to be turned off.

Description

E-1 Control Cycle: The word at EA + 1 (IOCC control word) is placed on the out bus. The area is decoded if there is no parity error signal from the P-C. At time-pulse-B time, the control-word pulse is generated. The control-word pulse, gated by bits 5, 6, and 7 = 000 and out-bus bit 15 = 1, turns on the CE-mode flip-flop. If output bit 15 = 0, control-word and bits 5, 6, and 7 = 000 turn off the CE-mode flip-flop.

E-2 Data Cycle: A dummy cycle.

The IBM 2310 Disk Storage enclosure houses the single disk storage drives and the attachment circuitry needed to provide disk storage for the 1800 System. The IBM 2310 and the Single Disk Storage Unit are described in separate Field Engineering manuals. (See FE Bibliography - 1800 System, Form Y26-0560.)

(Pages 6-2 through 6-19 deleted)

CHAPTER 1 INTRODUCTION

- The tape control unit (TCU) for the 1800 system is contained on four SLT boards in the 1802 Processor-Controller.

- The tape control unit provides for the connection of IBM 2401 or 2402 Magnetic Tape Units via a data channel.

FUNCTIONAL DESCRIPTION – TAPE UNITS

- These tape unit configurations are available:
  1. One or two 2401 Model 1, 2, or 3 (30, 60, or 90 kc single tape-unit).
  2. One 2402 Model 1, 2, or 3 (30, 60, or 90 kc double tape-unit).

- Both the 2401 and 2402 are 9-track tape units. A 7-track compatibility feature is available.

- IBM 2400 series tape units are described in IBM Field Engineering Theory of Operation, 2401, 2402, 2403, 2404 Magnetic Tape Units, Models 1, 2, and 3. (See FE Bibliography – 1800 System, Form Y26-0560.)

The 2400 tape units use a two-gap, nine-track (eight data tracks and one check track), read/write head. The two-gap head allows automatic error checking of the tape data while it is being written. The first gap is used for writing and the second for reading. As an optional feature, a seven-track head that allows the 2400 tape unit to read or write Binary Coded Decimal (BCD) tape characters at densities of 200, 556, or 800 bits per inch is available. The seven-track feature also enables odd or even parity and two or three byte format.

The 2400 tape units use the NonReturn to Zero IBM (NRZI) method of recording data on tape. In the NRZI system of recording information, tape is continuously saturated in either the positive or negative direction. A change in saturation polarity is called a one, and no change is called a zero.

The 2400 tape units read or write tape in true binary form. However, the 2400 tape units can read or write binary coded decimal (BCD) data if a 7-track feature is installed.

FUNCTIONAL DESCRIPTION – TAPE CONTROL UNIT

- The 1800 Tape Control Unit:
  1. Selects the specified tape unit.
  2. Decodes the function.
  3. Initiates and controls tape motion.
  4. Assembles data into the specified format.
  5. Writes or reads tape data.
  6. Initiates cycle steal cycles when needed.
  7. Performs checks on data and on tape control functions.
  8. Corrects read errors in nine-track mode.

As with all 1800 DP I/O adapters, the basic functions of the tape control unit are to decode the I/O control command, initiate motion in the selected I/O unit, provide a buffer for one data word, and gate that data word to the in bus or from the out bus.

Because of the relatively high speed of magnetic tape units, the 1800 data channels are used; therefore, data transfer is accomplished by cycle stealing. Figure 7-1 is a simplified data flow of the tape control unit. During a read operation, data is read from magnetic tape, amplified by the final amplifiers and accepted by the skew register hi-clip or lo-clip latches. The hi-clip output is checked and corrected, then loaded into the read-write (R/W) register. The data is gated from the R/W register to the data register

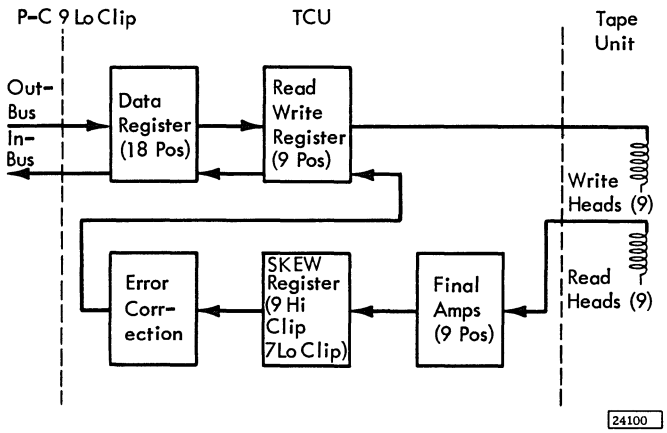


Figure 7-1. Tape Control Unit Basic Data Flow

in a byte format specified by the IOCC, then transferred to the P-C via the in bus.

During a write operation, data is transferred from the P-C via the out bus to the data register, gated to the R/W register in the specified byte format, and then gated to the tape unit to be written on magnetic tape. The tape control unit also controls these tape unit operations:

1. Backspace
2. Rewind
3. Rewind-unload
4. Write Tape Mark
5. Erase

All data flow and tape unit control is gated by the TCU clocks and delay counters.

Initializing the TCU

- All magnetic tape operations are initiated by the execute input/output (XIO) instruction in the processor-controller through a data channel (cycle stealing).

Descriptions of the XIO instruction, control words, and channel operations can be found in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller. See FE Bibliography – 1800 System, Form Y26-0560.) The XIO instruction causes two 16-bit control words to be transmitted to the channel control. The first word transmitted is the control word; it initializes the tape control unit. The second word transmitted is a data address word for the channel address register (CAR) used only in initialize read and initialize write operations. Figure 7-2 is a breakdown of the control words used by the tape control unit. Bit positions 0 through 4 (5 bits) in the first word transmitted refer to an area and designate one tape control unit. Bits 5 through 7 (3 bits) refer to a function code, where 011 indicates the sense ILSW function, 100 indicates the control function, 111 indicates the sense DSW function, 110 indicates the data-channel initialize read function (with a 1 in bit position 14 indicating a read-with-correction operation on 9-track formats), and 101 indicates the data channel initialize write function. The modifier bits 8 through 15 are defined in Figure 7-2. Note that in Figure 7-2 density, parity, and bytes per word are used only by 7-track tapes and are ignored by 9-track tapes.

Read-with-correction is used only by 9-track tapes. Read-while-correcting is ignored if the error occurs in more then one track or if the tape is 7-track. The read-with-correction operation corrects any number of errors in any one track (up to one per character) during reading. The normal read operation transmits such errors (uncorrected) into core storage, but correct parity is assigned to each byte in the P-C word.

- Sense device command selects a tape unit if bit 11 = 0 and the tape control unit is not busy.
- Select tape unit 0 if bit 10 = 0; select tape unit 1 if bit 10 = 1.

Selecting a Tape Unit

- A tape unit can be selected only by the sense device command.

A tape unit stays selected until a sense device command selects the other tape unit (bit 10, Figure 7-2). If an initialize read, initialize write, or control command specifies the unselected tape unit (modifier bit 10, a command-reject interrupt is initiated.

Data Formats

- Each P-C word consists of 16 data and 2 parity bits.
- The tape control unit translates data words into two 9-bit bytes, two 7-bit bytes, or three 7-bit bytes for tape for tape format.

Figure 7-3 shows the three data-word formats available for tape. Each word transmitted to or from the processor-controller consists of 16 bit positions (numbers 0 through 15) plus two parity bits labeled "P" and "V". When writing or reading 9-track tape format two bytes of 9 bits each go to or from each word.

When writing or reading packed 7-track tape format, three bytes go to or from each processor-controller word. Each byte on magnetic tape consists of six data bits (labeled B, A, 8, 4, 2, 1) and one parity bit (labeled C) which is generated and checked in the tape control unit.

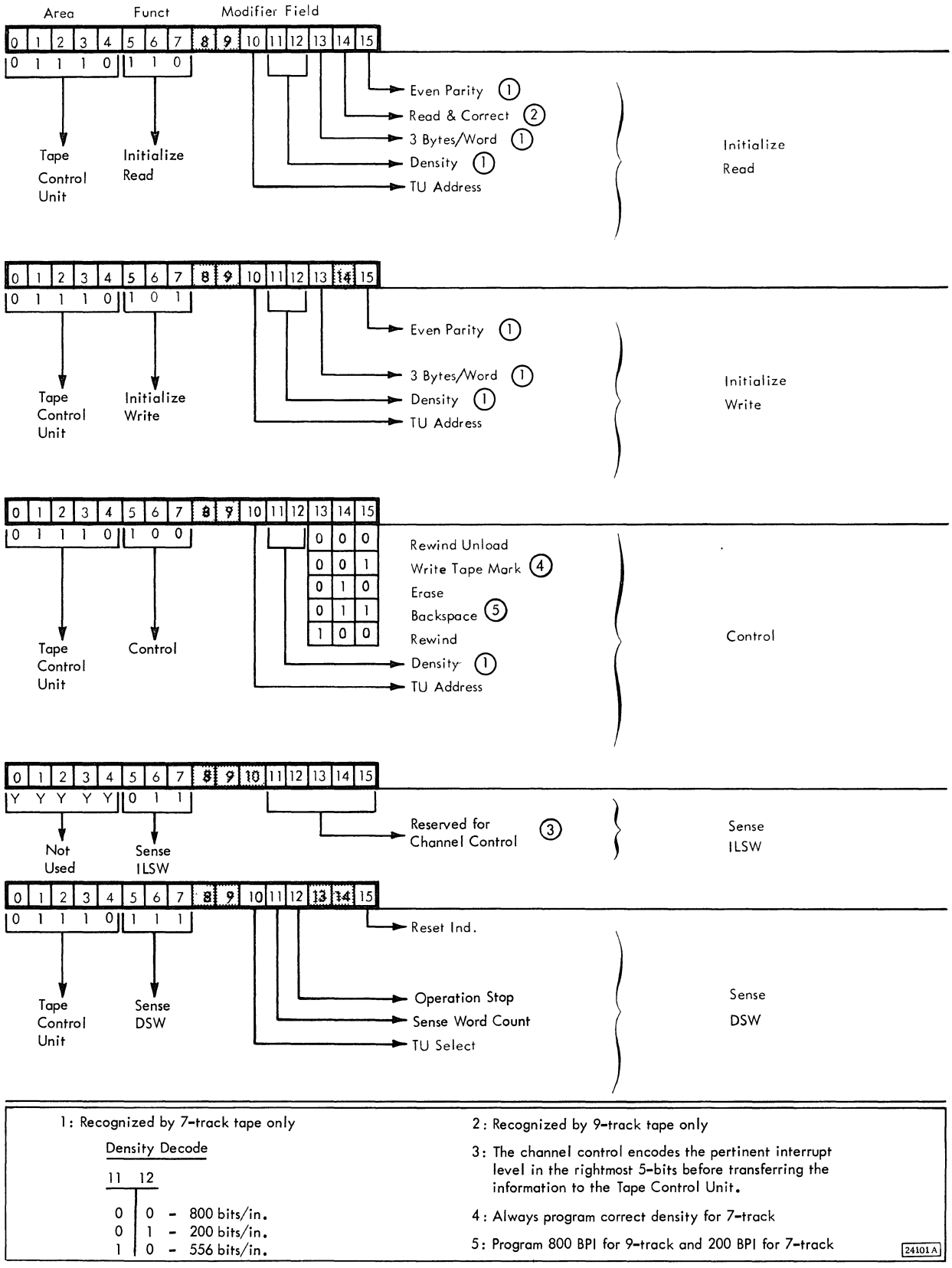
The P and V bits always reflect 2-bytes-per-word parity. The significance of P and V bits are always the same on both 7-track and 9-track operations, except that on 9-track and 7-track 2-bytes-per-word operations, P and V are the working parity bits on tape while on 7-track 3-bytes-per-word operations, P and V bits are carried as data on tape and an additional parity bit (C) is generated for each such byte.

Parity

Nine-track operations are performed in odd parity only. Seven-track mode may be written or read in odd or even parity as specified by bit 15 of the control word. A "one" bit selects even parity; a "zero" bit selects odd parity.

Tape Record Length

Minimum lengths are 12 bytes for a read operation and 16 bytes for a write operation. This minimum length is used by programs to aid in distinguishing



1: Recognized by 7-track tape only

Density Decode

11	12	
0	0	- 800 bits/in.
0	1	- 200 bits/in.
1	0	- 556 bits/in.

2: Recognized by 9-track tape only

3: The channel control encodes the pertinent interrupt level in the rightmost 5-bits before transferring the information to the Tape Control Unit.

4: Always program correct density for 7-track

5: Program 800 BPI for 9-track and 200 BPI for 7-track

24101A

Figure 7-2. Control Words - 1800 Tape Control Unit

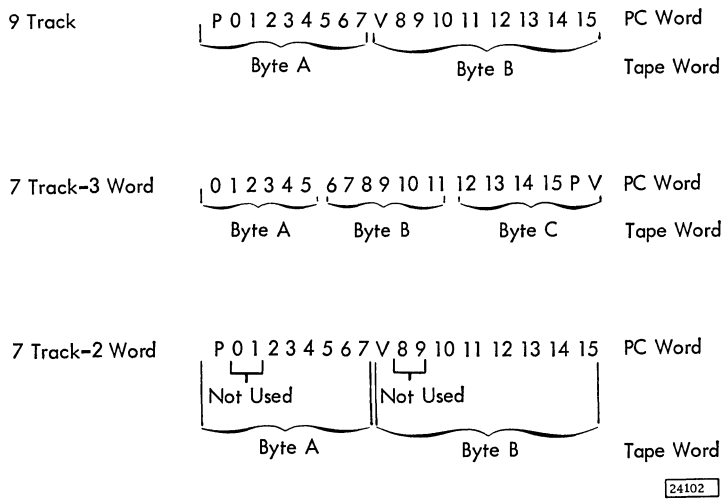


Figure 7-3. Data Word Format

noise records from data records. There is normally no check for noise unless there is a data check.

Device Status Word (DSW)

The sense device function selects a tape drive if the tape control unit is not busy. Otherwise the sense device function simply presents the device status word of a previously selected tape unit. If bit 11 = 0, the device status word enters the accumulator. Indicators in the DSW are reset after being loaded into the accumulator only if bit 15 of the sense DSW modifier is a one.

If bit 11 = 1 in a sense-device control word, the channel word count replaces the contents of the accumulator in the processor-controller. Word-counter bit positions 0 and 1 = 11, during a sense-word-count operation, indicate the count is in one's complement. Both bits being zero indicates a true binary number. Bit positions 2 through 15 contain the word count. When the tape record is longer than the programmed word count, the count of the extra P-C words is loaded into the word-count register in true form. When the tape record is shorter than the programmed word count, the word-count register is the one's complement of the number of P-C words not read.

For example, assume a tape record of 15 P-C words. If the programmed word count is +6, the word-count register is equal to +9 at the end of the operation. If the programmed word count is +18 the word count register is equal to -3 in one's complement (or -4 in two's complement) at the end of the operation.

If the programmed word count is +15, the word-count register shows all zeros at the end of the operation, providing 15 words, or 14 words plus one or two bytes, were read.

The bit positions of the device status word reflect indicators as follows:

Bit Position	Indicator
0	(Spare)
1	Tape Unit 1 Select
2	Command Reject
3	End of Table
4	Chain Stop
5	Storage Protect Violation Stop
6	Tape Data Error
7	Data Bus Out or P-C Parity Error
8	Data Overrun Error
9	Operation Complete
10	Tape CE Diagnostic Indicator
11	Wrong Length Record
12	At Load Point
13	Tape Indicator or Mark
14	Tape Busy or Rewind
15	Tape Busy or Not Ready

The absence of a command-reject indicator bit indicates that the last command has been accepted by the tape control unit.

Interrupts

- There is one interrupt level associated with the tape control operation.

The following three indicators are set by interrupting conditions. The indicator in turn raises the interrupt request to the P-C.

Operation Complete Indicator: This indicator is set at the completion of a write tape mark, initialize read,

initialize write, erase, or backspace operation. This indicator is also set immediately after the initiation of a rewind or rewind-unload when tape drive status lines indicate that free running operation is under way. This indicator is turned off by a sense DSW operation. The operation complete indicator is set upon recognition of an inter-record gap on an initialize read operation and therefore is set even if a wrong length record (inconsistent with data-channel word-count) is read. The operation complete indicator is also set on an initialize read or initialize write operation even if a chain stop, storage protect, tape data, data-bus-out or P-C parity, data overrun, or tape diagnostic error occurs. If a command is rejected, that rejected command does not set the operation complete indicator, although any previous operation still in progress does set this indicator.

End of Table Indicator: This indicator is set, if requested by the scan control bits, when the specified word count on a magnetic tape input/output operation becomes equal to zero. The indicator is turned off by a sense device command if bit 15 = 1.

Command Reject Indicator: This indicator comes on if any one of the following conditions occurs:

1. Rejection of initialize write, initialize read, or any control command issued to a busy or not ready tape unit.
2. Rejection of initialize write, initialize read, control, sense DSW, or sense ILSW command due to P-C or out-bus parity error in an initializing XIO control word cycle.
3. Rejection of an initialize write or initialize read command due to P-C or out-bus parity error when loading channel address register (CAR) or when loading the word counter in the TCU while initializing.
4. Rejection of initialize write, write tape mark, or erase command issued to a file-protected tape unit.
5. Rejection of backspace or rewind command at load point. (Includes trying to backspace from the beginning of first record into load point.)
6. Rejection of initialize read, initialize write, or any control command issued to an unselected tape unit. A tape unit can be selected only by the sense DSW operation and only if the TCU is not busy.

The indicator is reset by a sense DSW operation. If a command is rejected, that rejected command will not set the operation-complete indicator, although any previous operation still in progress will set the operation-complete indicator in the normal manner.

Indicators

- The following indicators are associated with 1800 tape control operation.

Tape Unit Select Indicator: Bit position 1 in the device status word indicates which of two tape drives is currently selected by the tape control unit.

Command Reject Indicator: This indicator is turned on by the command-reject interrupting conditions described in the preceding paragraphs on interrupts.

End of Table Indicator: This indicator is turned on by the end-of-table interrupting condition as described in the interrupt description.

Chain Stop Indicator: This indicator comes on if condition 3 of command-reject indicator takes place while chaining and not while initializing. The initialize write operation will terminate at this point and an operation-complete interrupt will occur. Any transfer of data for an initialize read operation will be terminated although the operation-complete interrupt will not occur until an inter-record gap is encountered. This indicator is reset by a sense device command if bit 15 = 1.

Storage Protect Violation (SPV) Stop Indicator: This indicator is set if an attempt is made to store data (tape read operation) into a storage-protected location. The transfer of data is terminated although the tape proceeds to the inter-record gap. This indicator is reset by a sense device command if bit 15 = 1.

Tape Data Error Indicator: This indicator is turned on if any one of the following read or write checks is detected:

1. R/W register vertical redundancy check (VRC) error.
2. Write high-clip VRC error.
3. Write-no-echo error or read-lost-character.
4. Write skew error.
5. R/W longitudinal redundancy check register (LRCR) error.
6. Read cyclic redundancy check register (CRCR) error.

This indicator is reset by a sense device command if bit 15 = 1.

Data Bus-out or P-C Parity Error Indicator: This indicator is turned on during cycle steal data transfer cycles if a P-C parity error is detected on the out bus or in bus, or if an out-bus parity error is detected in the TCU. This indicator is reset by a sense device command if bit 15 = 1.

Data Overrun Indicator: This indicator is turned on if a cycle steal acknowledge does not arrive in time for a valid data transfer: This indicator is reset by a sense DSW operation.

Operation Complete Indicator: This indicator is turned on by interrupting conditions as described in the interrupt description.

Tape CE Diagnostic Indicator: This indicator is turned on if any one of the following tape control checks is detected:

1. Read high-clip VRC error.
2. Read clock VRC error.
3. Write clock VRC error.
4. Delay counter VRC error.

Wrong Length Record Indicator: This indicator is turned on if the number of words of data upon magnetic tape in an initialize read operation is not identical to the word count in the processor-controller or if a tape mark is encountered during an initialize read operation. The indicator is turned on by attempts to read either long or short records (as compared to the processor-controller word count). This indicator is also turned on if a record does not contain byte multiples exactly matching the whole total of P-C words. In this case, extra byte(s) are added to fill up the last P-C word and this complete word is transferred to core storage with the word counter counting this last word. This indicator is reset by a sense DSW operation.

At Load Point Indicator: This indicator is turned on if the tape is physically at load point. The indicator is reset only by tape motion that results in the tape physically leaving load point. This indicator is not turned off by a sense DSW operation.

Tape Indicator or Mark Indicator: This indicator is turned on if a tape indicator is sensed during initialize read, initialize write, write tape mark, erase, or if a tape mark is read during an initialize read operation. This indicator is not turned on by tape marks encountered during any initialize write, write tape mark, erase, or backspace operations.

This indicator will be reset by a sense DSW operation only if a tape mark was sensed. To reset the indicator if a tape indicator is sensed, it is necessary to perform either a backspace rewind or rewind-unload operation.

Sensing a tape mark always causes the wrong length record indicator to be set. Sensing a tape indicator does not stop the transfer of data and therefore does not cause the wrong length record indicator to be set unless a short or long record condition also exists.

Tape Busy or Rewind Indicator: This indicator is on during initialize read, initialize write, write tape mark, erase, and backspace operations. The indicator will also be on during rewind and rewind-unload operations after initialization of these operations, provided the rewinding tape unit is selected and has not reached load point. This indicator is not reset by a sense DSW operation.

Tape Busy or Not Ready Indicator: During initialize read, initialize write, write tape mark, erase, and backspace operations, the tape unit is considered to be ready and busy. During rewind and rewind-unload operations, the tape unit is considered to be not ready and not busy. Accordingly, the tape-channel-busy-or-not-ready indicator will be on during all of the above listed operations. This indicator will also be on if the tape unit is not physically ready. This indicator is not reset by a sense DSW operation.

Error Correction

On every read operation in 9-track format, error correction circuitry constantly monitors high-clip VRC errors to determine the track in error. If the track is found and the program requests a backspace followed by a read-with-correct, all such errors in the found track are corrected. On the other hand, if the errors are in more than one track, the read-with-correct commands are transformed to the normal read operations.

The error correction circuitry automatically checks for the correct programming sequence of initialize read, backspace, read-with-correction, backspace, read-with-correction, etc., on the same tape record, and, if the program moves to a different tape record, the error correction circuitry is reset to start a new computation on the new record.

I/O INTERFACE

- The tape control unit connects to the 1802 P-C channel control through the standard I/O channel interface.

- The 2401 or 2402 Magnetic Tape Unit connects to the tape control unit through a unique device interface.

Channel Interface

- All I/O adapters in the 1800 system share a standard interface that is described in the IBM Field Engineering Theory of Operation, 1800 Data Acquisition and Control System, Processor-Controller. (See FE Bibliography – 1800 System, Form Y26-0560.)

The I/O channel interface consists of two sets of 60 signal and control lines. These lines connect to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, and exits all 60 lines to the next adapter in sequence. If the tape control unit is the last in the sequence, the channel interface lines must be terminated at the mixer panel (gate H). The tape control unit taps off and uses signals from these lines:

Out-bus bits 0 through 15
In-bus bits 0 through 15
Parity bit for bits 0 through 7
Parity bit for bits 8 through 15
Poll interrupt level 0-13
Poll interrupt level 14-23
Use meter gate
Time pulse A
Time pulse B
Time pulse C
Cycle steal request A through E
Cycle steal acknowledge A through E
Cycle steal control 0, 1, and 2
CAR check or Parity error
Storage protect violation
XIO data cycle
XIO control cycle
Reset

I/O Device Interface

- The I/O device interface includes the signal and data lines that connect the tape control unit in the 1802 to the 2401 Magnetic Tape Unit.

The tape control signals connect the tape control unit, through flat cable and serpent connectors, to the P-C signal tailgate. The signals connect from the tailgate, through a serpent connector and signal cable to a 200-position T/C connector at the 2401 or 2402.

The T/C connector, signal cables, and the purpose of each signal line are described in the IBM Field Engineering Theory of Operation, 2401, 2402, 2403, 2404 Magnetic Tape Units, Models 1, 2, and 3. (See FE Bibliography – 1800 System, Form Y26-0560.) Each signal line has a ground shield that connects to an adjacent pin in the serpent connector at the 1802 and in the T/C connector at the 2401 or 2402. The signal lines and their functions are listed in Figure 7-4.

Line	Adapter In/Out	Function
Read Select 0 and 1 (2 lines)	Out	Gates data and control lines into and out of a selected tape unit. Since select lines are rotated in the signal cable, each select line addresses a single tape unit.
Go	Out	Starts and stops tape movement in a selected tape unit.
Backward	Out	Determines direction of tape motion in a selected tape unit (forward = not backward), and turns off the tape indicate light.
Set Read	Out	Puts a selected tape unit in read status to prevent writing from taking place.
Set Write	Out	Puts a selected tape unit in write status and allows writing to take place.
Rewind	Out	Initiates a rewind sequence and turns off the tape indicate light in a selected tape unit.
Metering Out	Out	Runs the meter of a tape unit whose start relay is picked, if the tape unit is loaded and away from load point, or if the tape unit is unloaded and rewinding.
Write Pulse, Write LRCC Gate, and Write Bus P, 0-7 (11 lines)	Out	These lines determine the bit pattern written by selected tape unit.
Rewind Unload	Out	Initiates a rewind sequence that unloads the tape from the vacuum columns and raises the upper read-write head assembly upon reaching load point.
Read Bus P, 0-7 (9 lines)	In	Lines carry the amplified output of a selected tape unit's read buses to the tape control.
Model 1,2,or 3 (3 lines)	In	Indicates operating speed of the selected tape unit to the tape control. The model line brought up by any tape unit depends on its model number.
7 Track	In	Indicates that the selected tape unit has the 7-track feature installed.
Selected and Read Status	In	Indicates that the selected tape unit is in read status. Write status is indicated when Model 1/Model 2/ Model 3 is active and selected and read status is inactive
Selected and at Load Point	In	Indicates that tape on the selected tape unit is positioned at load point.
Write Echo	In	A write echo pulse is generated whenever one of the tape unit's write triggers flips to write a bit on tape.
Selected and Tape Indicate OFF	In	Indicates that the tape-indicate trigger in the selected tape unit has not been turned on. Tape indicate is turned on by sensing the end of tape marker. Tape indicate is turned off by any backward operation, or by unloading the tape unit.
Selected and NFP 1	In	Indicates that a write enable ring is installed in the file reel on a selected tape unit, so that writing can take place. Absence of the write enable ring prevents the tape unit from being set to write status.
Backward Status	In	Indicates that the selected tape unit previously has completed a backward operation, or is in the process of doing so.
Not Ready-0 and -1 (2 lines)	In	Indicates that a physically connected tape unit is not available for use (not mechanically ready) because its start relay is not picked, or the tape unit is busy rewinding.

24204

Figure 7-4. 2401/2402 Device Interface Lines

CHAPTER 2 FUNCTIONAL UNITS

Tape control functional units can be classed as data flow, control, and checking units as follows:

Data Flow	Control
final amplifiers	read clock
skew registers	write clock
read/write register	delay counter
data register	word counter
	byte generator
	function register

Checking

longitudinal redundancy check

cyclic redundancy check

error pattern register

MDM GB20101 shows the relationship of these units.

READ CLOCK

- Three flip-flops with decoding circuits and a single-shot provide the necessary outputs.
- Synchronized with incoming tape characters by the read clock drive circuits.
- Drive pulses change the state of only one flip-flop at a time, providing "cleaner" outputs.
- Runs for read operation, write operation (for checking), and for backspace operation.
- Completes one cycle per character.
- Output is checked for vertical redundancy.

The read clock provides pulses to gate data flow through the tape control unit (TCU). There is no way of knowing just when characters will start being read from tape; therefore, the clock is started by the first bit that is read.

The read clock runs through one complete cycle for each character of a record.

When not in operation, the clock flip-flops are held disabled by the not-start-RC line (Figure 7-5). After the start-RC line is activated, the drive pulses begin stepping the flip-flops in a cyclic pattern; that is, only one flip-flop changes state for each drive pulse. The cyclic pattern permits fast operation with clearly defined output pulses.

Read-clock (RC)-A flip-flop is turned on by the first clock-drive pulse. The next drive pulse turns off RC-A. When RC-A is on, the fall of the first drive pulse turns on RC-B; it is turned off by the fall of the clock-drive pulse during the next RC-A time. RC-C is turned on by the fall of the drive pulse when RC-A is off. The output of these three flip-flops decodes to produce RC 0 +1, RC 2, RC 4, and RC 6. A single-shot, turned on by the fall of RC 6, provides the RC 7 pulse.

Clock Reset: The read clock is reset after RC 7 time for a read operation. During a write operation, the reset at RC 7 is blocked by the skew gate and the clock continues to step until RC 2 is turned on. The clock is then reset by skew gate and RC 2.

Read Clock Drive

- Two oscillators, 1.0 mc and 1.4 mc, are gated by the first-bit latch (Figure 7-6).
- Two flip-flops, 400 bits per inch (BPI) and 200 BPI, are stepped in a binary fashion by the 1.4 mc oscillator.
- One of three outputs (two oscillators and the 200-BPI flip-flop) is gated, by bit-density selection, to the model 1, 2, and 3 flip-flops.
- One output of the three model flip-flops, is gated by model selection, to the read clock as drive pulses.

The read clock drive frequency is determined by two factors: the density, measured in bits per inch (BPI), and the tape unit model. The density for 9-track operation is fixed at 800 BPI. If the 7-track feature is being used, the density is specified by program means as 800, 556, or 200 BPI. If neither 556 BPI nor 200 BPI is specified, the 800 BPI line is activated to gate the output of the 1.4 mc oscillator as the basic frequency. The basic-frequency pulse turns on and off the four model flip-flops (model 1, model 2, model 3 Phase A, and model 3 phase B), one output of which is gated by the model 1, 2, or 3 line. The model 1, 2, or 3 line is activated by the selected tape unit.

For a specified density, the basic-frequency must be divided to provide a different frequency for each tape unit model. This frequency division is accomplished by the circuit shown in Figure 7-5. The model-3-phase-A flip-flop divides the basic frequency by two. The rise of the basic-frequency

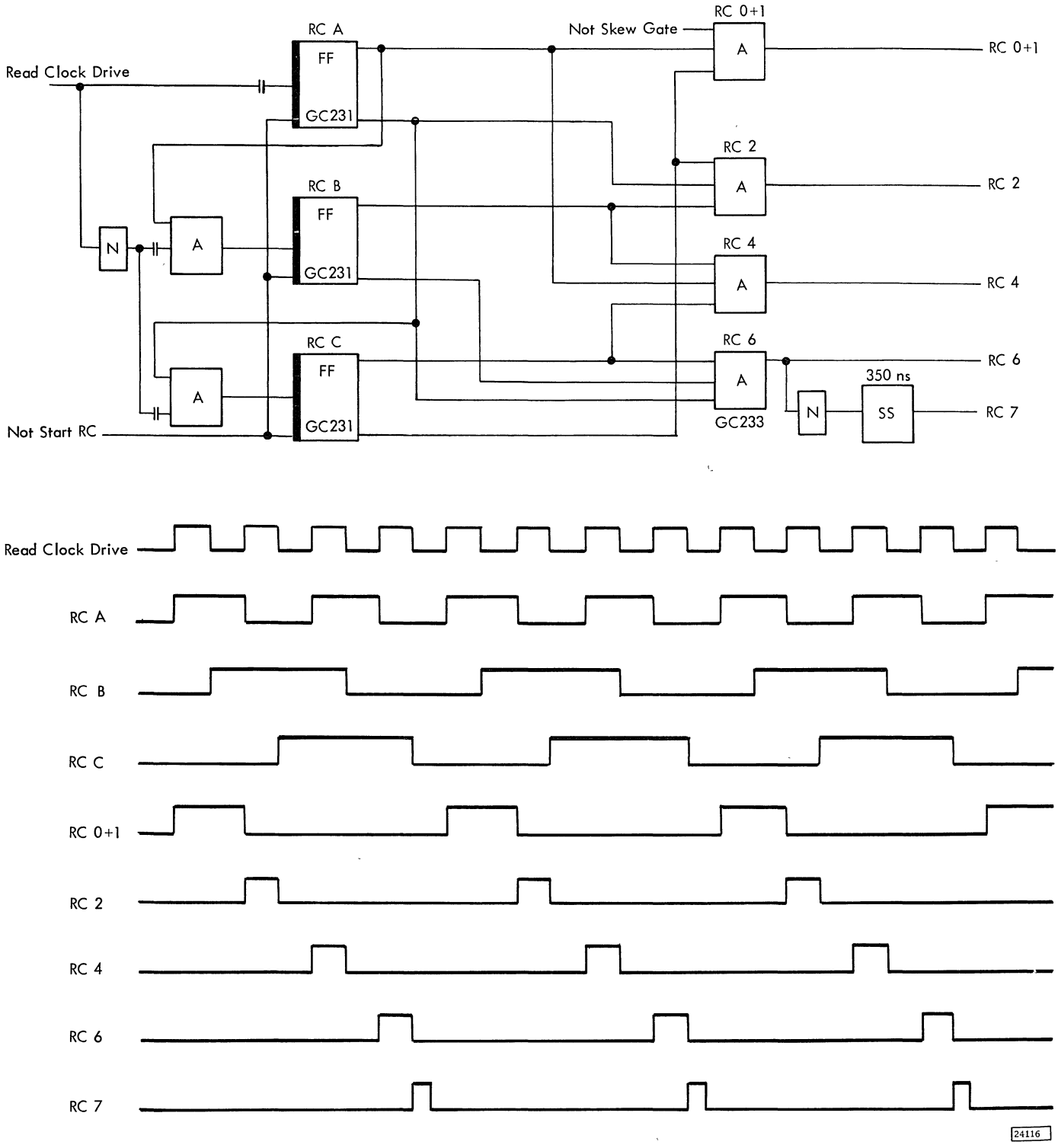
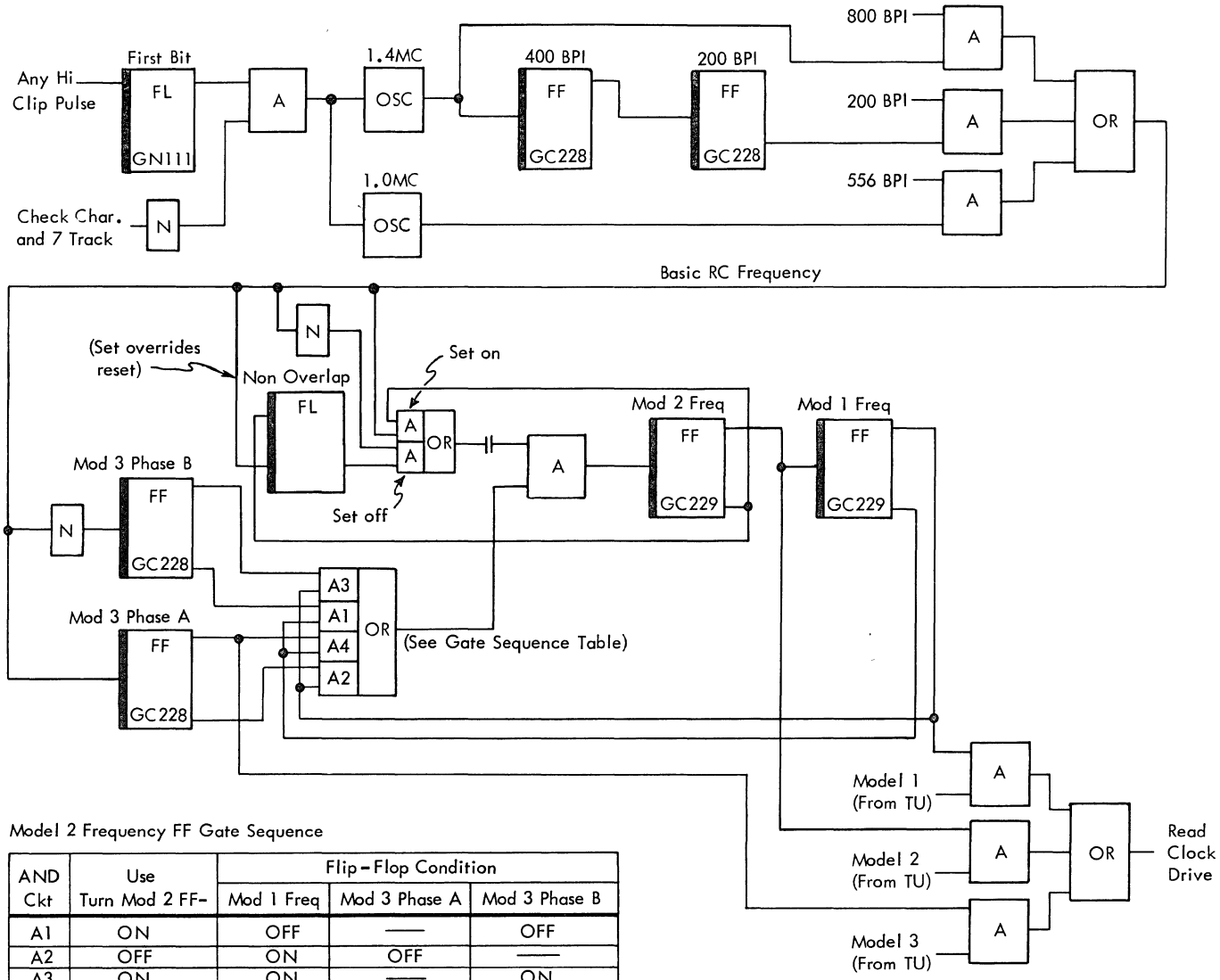


Figure 7-5. Read Clock



Model 2 Frequency FF Gate Sequence

AND Ckt	Use Turn Mod 2 FF-	Flip-Flop Condition		
		Mod 1 Freq	Mod 3 Phase A	Mod 3 Phase B
A1	ON	OFF	—	OFF
A2	OFF	ON	OFF	—
A3	ON	ON	—	ON
A4	OFF	OFF	ON	—

AND ckts A1 and A3 are also conditioned by Mod 2 freq OFF.
AND ckts A2 and A4 are also conditioned by Mod 2 freq ON.

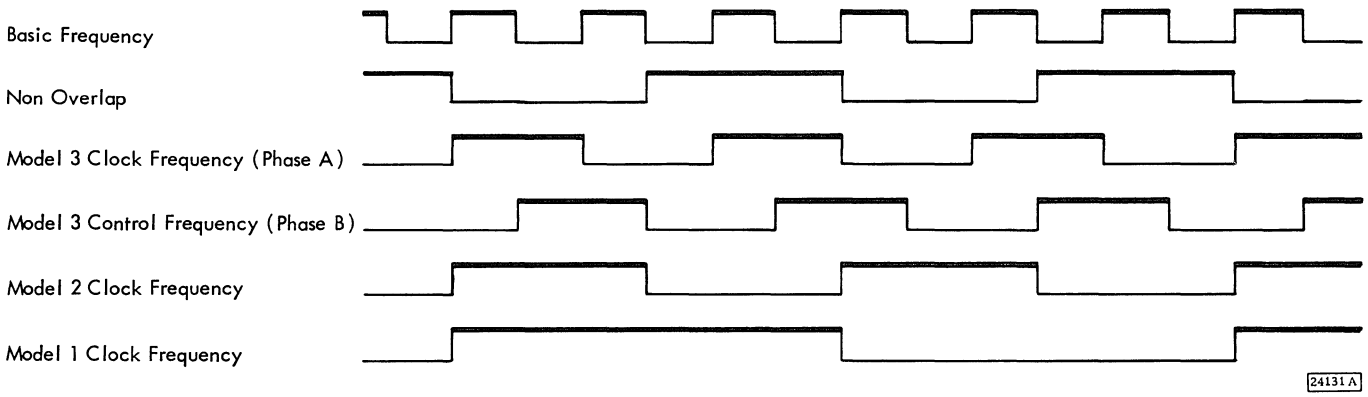


Figure 7-6. Read Clock Drive

pulse turns on, and off, this flip-flop.

Another flip-flop (model 3 phase B) is used for control only. It is turned on and off by the fall of the basic-frequency pulse. The outputs of these two model-3 flip-flops are out of phase with each other, enabling the control of the model-2-frequency flip-flop for a frequency one-third of the basic frequency. The model-2-frequency flip-flop turns on and off the model-1-frequency flip-flop producing a frequency that is one-sixth of the basic frequency.

WRITE CLOCK

- Four flip-flops with decoding circuits provide the following four clock-pulse outputs: write clock (WC) 2, WC5, WC8+9, and WC14+15.
- Only one flip-flop is turned on or off at one time.
- Runs when the write condition latch is on; completes the last cycle after write condition is turned off.
- Gates data to the various TCU circuits and to the tape units.
- Output is checked for vertical redundancy.

Write Clock Drive

- Two free-running oscillators, 1.0 mc and 1.44 mc, generate the basic frequency for the write-clock-drive circuits.

The bit-density and tape unit model determine the write clock drive frequency with the same circuit configuration used in the read-clock drive. The basic drive frequency, called "μsec pulse", is also used as the delay-counter drive when in μsec control.

The difference between the write-clock drive and read-clock drive is due to the fact that the read clock must be synchronized with the first bit received from tape, while the write clock determines the time at which writing takes place.

DELAY COUNTER (DC)

- Consists of nine binary-operated flip-flops, DC-A through DC-J, providing 512 combinations of outputs.
- Only one flip-flop is turned on or off at one time.
- Various outputs are gated to control the tape operations.
- Outputs are checked for vertical redundancy.

The outputs of this counter are gated with the various operations, tape unit models, and track formats to provide time-interval pulses for tape-control functions. During a read operation, read-delay (RD) and read-disconnect-delay (RDD) pulses are generated from the delay counter; during a write operation, write-delay (WD) and write-disconnect-delay (WDD) pulses are generated.

Delay Counter Drive

- Basic drive frequency is either millisecond or microsecond based as required by the current operation.
- Millisecond-mode basic-drive pulses are generated by a 5 kc free-running oscillator.
- Microsecond-mode basic drive pulses are the same pulses used by the write-clock-drive circuits.

When tape control requires millisecond-based timing pulses, the delay counter is driven by the msec-mode circuits. The msec-mode basic frequency is generated by a 5 kc free-running oscillator and two binary-operated flip-flops, 1.25 kc and 2.5 kc. If the selected tape unit specifies model 1, the output of the 1.25 kc flip-flop is gated as the DC drive. If the selected tape unit specifies model 2, the output of the 2.5 kc flip-flop is used. If the selected tape unit is a model 3, the 5 kc oscillator output is used as the basic drive pulse.

When tape control requires microsecond-based timing pulses, the delay counter is driven by μsec-pulse which is also used as the write clock drive. It is conditioned by bit-density and model-frequency by the same circuit configurations as described in the read clock drive description.

WORD COUNTER

- Fourteen flip-flops arranged as a binary counter.
- Loaded from out bus during first cycle steal cycle.
- Loaded in one's complement form.

- Word counter is advanced during each data transfer.

- End-of-data-table is indicated by word-count-zero when all positions are on.

The word counter is reset (all flip-flops off) during the E-1 cycle of the XIO instruction. It is loaded from the out bus during the first cycle steal cycle.

The word count of the data to be transferred, located in the first word of the data table, is loaded into the word counter in one's complement form.

The word counter is advanced one count at T2 time of every cycle steal cycle by cycle steal acknowledge. The on outputs of all positions are ANDed to indicate word-count-zero. Figure 7-7 shows a word count of three being loaded in complement form into the word counter and the counter being advanced with each cycle steal cycle until all positions are turned on.

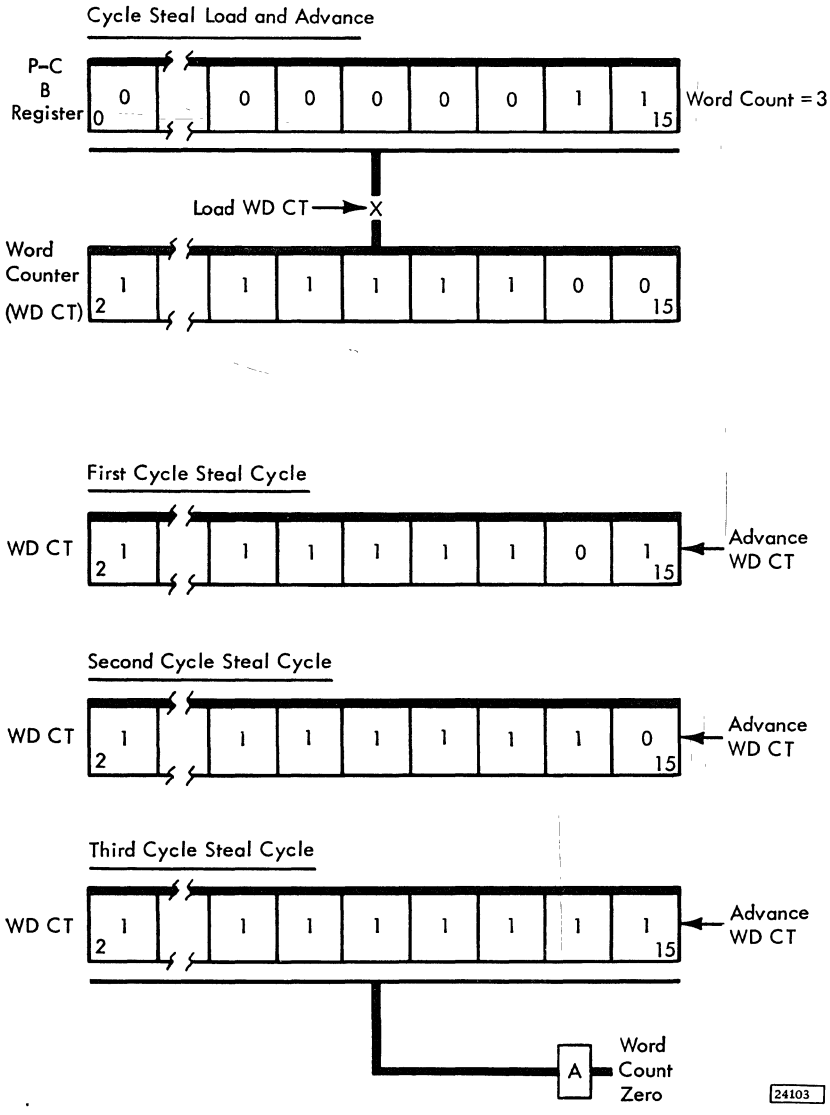


Figure 7-7. Word Counter Advance to Zero

BYTE GENERATOR

- Two binary operated flip-flops, BT0 and BT1 (Figure 7-8).
- Reset (both flip-flops off) at T5 of the XIO control cycle (E-1) or by the first-check-character and byte A.
- BT0 is operated for either 2-bytes-per-word or 3-bytes-per-word operations.
- BT1 is operated only for 3-bytes-per-word operations.

The byte generator is a two position binary counter that gates data bytes from the data register to the read/write register on a write operation and from the read/write register to the data register on a read operation. It is controlled by read command and write command timing and by 2-byte-per-word and 3-byte-per-word modes.

FUNCTION REGISTER

- Ten flip-latches and decode circuits for the following functions (Figure 7-9):

rewind	initialize write
rewind-unload	initialize read
write tape mark	sense DSW
backspace	sense word count
erase	sense ILSW

- Loaded during the control word cycle of an XIO instruction according to the function code (bits 5, 6, 7) and the modifier (bits 11, 13, 14, 15).

Four function codes condition the circuits of the function register. Initialize-write and initialize-read decodes turn on the corresponding flip-latch conditioned by R-W-C enable. Control decode conditions the five control-function flip-latches, one of which is turned on by a decode of modifier bits 13, 14, and 15.

The sense-DSW decode conditions the DSW-remember and the sense-word-count flip-latches. Sense-word-count is turned on if modifier bit 11 = 1. The ILSW-remember flip-latch is turned on at T6 time of an XIO control word cycle if the assigned interrupt level is decoded.

FINAL AMPLIFIERS

- Consist of nine identical circuits, for nine tracks, bit P and bit 0 through 7.

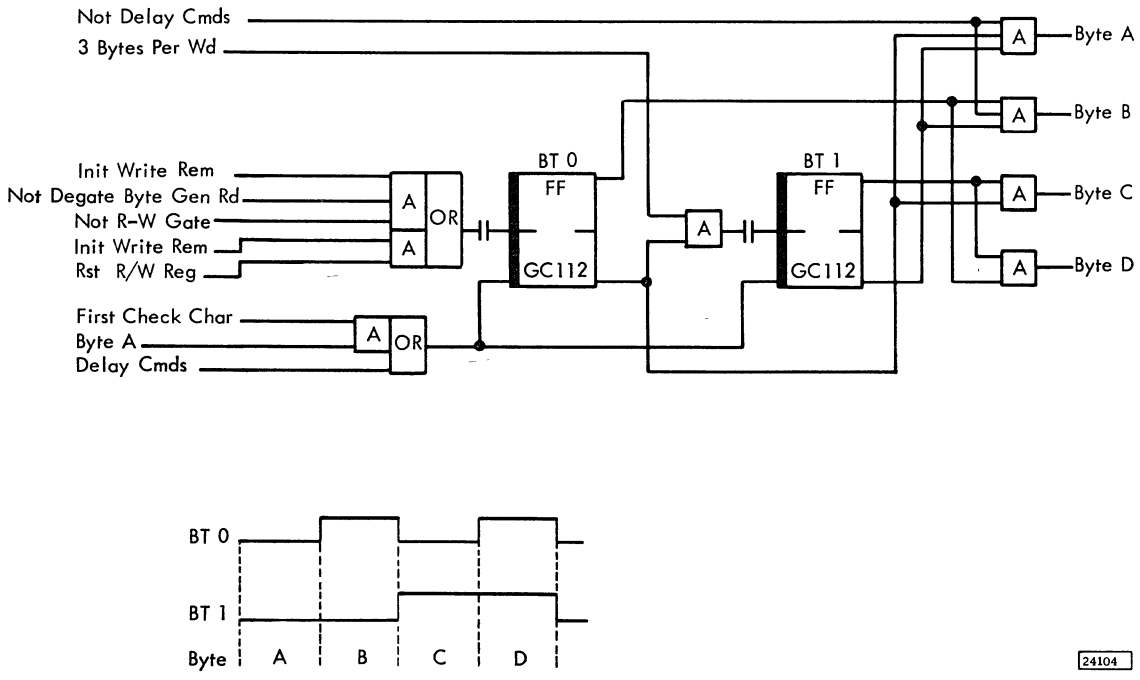


Figure 7-8. Byte Generator

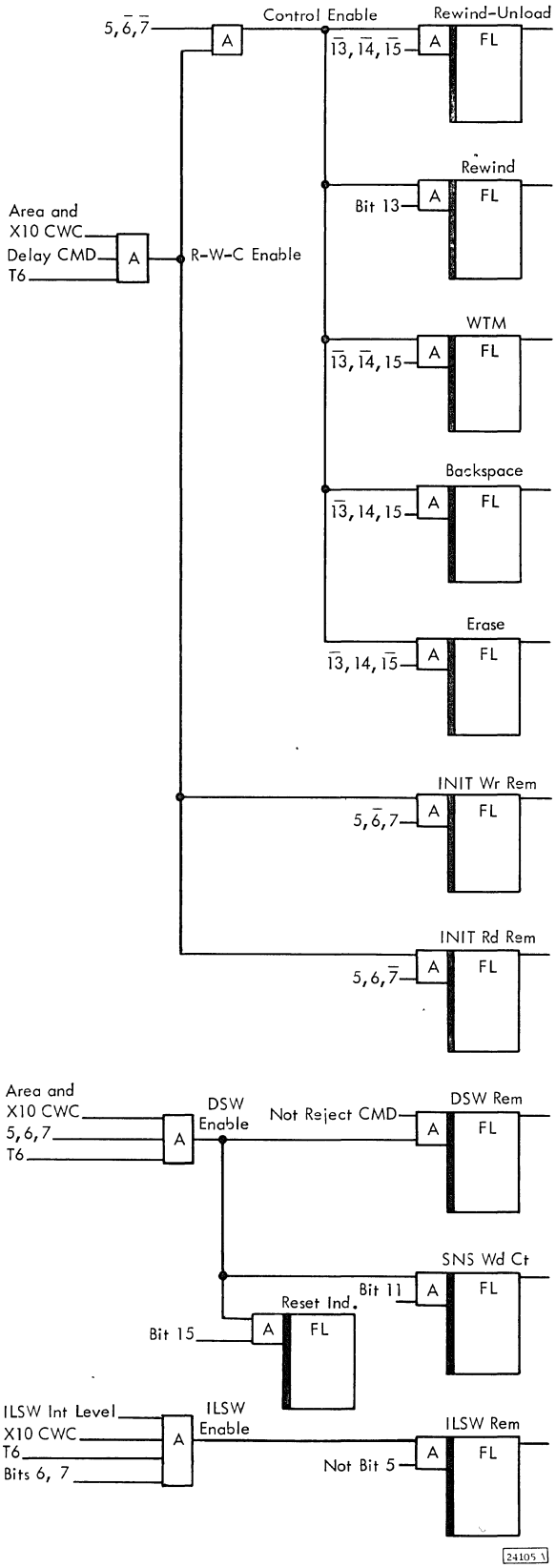


Figure 7-9. Function Register

- Each final amplifier consists of these four stages: a terminator, a rectifier and channel separator, the peak detector (2), and the pulse shaper and drivers (2 each), shown in Figure 7-10.
- Inputs are non-return to zero IBM (NRZI) signals from the tape unit pre-amplifiers.
- Two outputs, high-clip and low-clip, for each track provide positive pulses to the skew registers.
- Positions 0 and 1 are not gated out if in seven-track operation.

Final amplifiers accept pulses from the tape unit and convert the pulses to high- and low-clip data. The high- and low-clip outputs are used to set the high- and low-clip skew registers.

The term "clip" in this usage refers to a method of establishing amplitude requirements for the input pulses. To generate a high-clip output pulse the input must be above a certain level. An input signal below this level does not generate a high-clip output but may still cause a low-clip output. If the signal is lower than the requirement for low-clip output, no output is generated. A high amplitude signal generates both high- and low-clip outputs.

The low-clip outputs are used only for seven-track operation. Nine-track operation establishes more critical requirements so only high amplitude pulses are accepted from the tape unit.

Terminator: Input to the terminator is a positive and negative NRZI signal. The output is two out-of-phase signals from a center-tapped transformer. The center tap is connected to low clip to control the acceptance level of the circuit.

Rectifier and Channel Separator: This stage consists of a rectifier circuit, the output of which is connected to two emitter followers for output signal separation. Input to the rectifier circuit is the terminator output transformer, the center tap of which is connected to a potentiometer to provide input-signal balancing. The low-clip and high-clip emitter followers are both supplied by a -9v zener supply. The high-clip circuit is biased by high clip voltage to establish an acceptance level for signals to be used by the high-clip circuits that follow.

Peak Detector: The peak detector stage is the first of the two channels through which the separated signals are passed. The stage consists of a detector circuit and an amplifier.

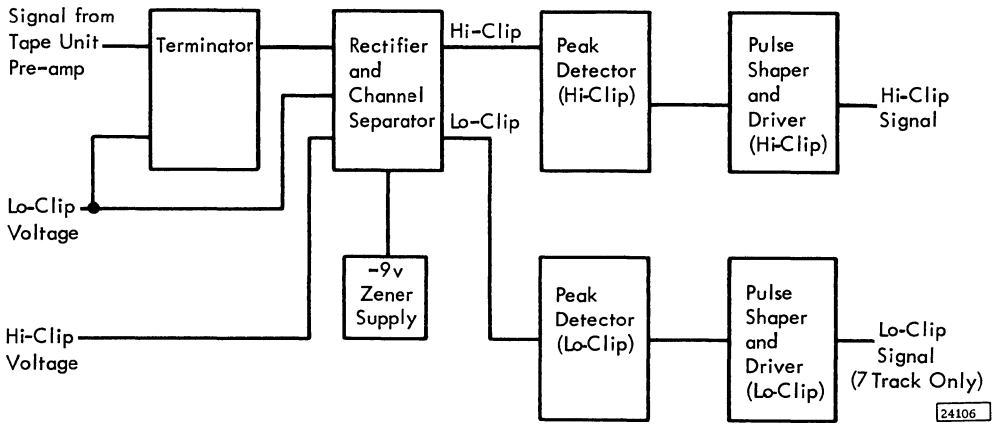


Figure 7-10. Final Amplifier

Pulse Shaper and Driver: This stage consists of identical circuits for both the low-clip and high-clip channels. The circuits, including an integrator, trigger, shaper, and driver, reject pulses below a specified width and accept all others. The outputs are positive pulses that are gated into the skew registers.

SKEW REGISTER

- Consists of 16 flip-latches that accept bits as they are read from tape, allowing for tape skew.
- Nine high-bit latches, P and 0 through 7, store the high-clip bits.
- Seven low-bit latches, P and 2 through 7, store the low-clip bits.
- Both the high-bit and low-bit latches are turned on unconditionally by the final-amplifier pulses.
- High-bit latches are also turned on by the outputs of the error-pattern register (EPR) for error correction.
- All skew register latches are reset (turned off) at the fall of read condition.
- The outputs of the high-bit latches go to the error-correcting circuits, a vertical-redundancy-check (VRC) circuit, the longitudinal-redundancy-check register (LRCR), and to the read/write register.
- The outputs of the low-bit latches are gated to the LRCR and R/W register if there is a high-clip VRC and the unit is in seven-track mode.

Due to the electrical or mechanical skew of tape, not all the bits of one character are necessarily read at the same instant. The first bit read starts the read clock; the character is not gated from the skew register into the read-write register until RC 7 time, allowing time for all bits of each character to be read.

During the end-read portion of an error correction cycle (nine-track only), the outputs of the EPR are gated to the high-clip latches for exclusive OR comparison with CRCR outputs to find the track in error.

During the read-with-correction operation, the error pattern register outputs indicate the track in error in reverse order, that is, error pattern register P indicates track 7, error pattern register 0 indicates track 6, etc.

The low-clip latches are not used in nine-track mode. If a tape signal is not at a level that is accepted by the high-clip circuits, a high-clip VRC error is detected. The same character, if at a level acceptable to low-clip circuits, will be in the low-clip skew latches. In this case, the outputs of the low-clip latches are gated to the read/write register.

READ/WRITE REGISTER (R/W)

- Consists of nine flip-latches; used for write and read operations.
- Write operation: input from data register (from P-C); output to write bus (to tape units).

- Read operation: input from skew register; output to the data register (to P-C).
- Input from the data register varies with nine-track and seven-track mode.
- Output parity is unconditionally determined; checking and generation of parity is determined by nine-track or seven-track mode and by odd or even parity call.

DATA REGISTER

- Consists of 18 flip-latches; used for write and read operations.
- Write operation: input is from the P-C via the out bus; output is gated to the R/W register in various formats depending on track mode and bytes-per-word format (Figure 7-11).
- Read operation: input is from the R/W register, gated in two or three bytes; output is to the P-C via the in bus.
- Data register is reset (all latches turned off) at T5 of each cycle in which it is used.

Data Reg.	From R-W Register (Read Op.)						From
	9 Track		7 Track				Out-Bus
	(2 Bytes/Wd. Only)		2 Bytes/Wd.		3 Bytes/Wd.		(Write Op)
Position	Position	Byte	Position	Byte	Position	Byte	Position
P	P	A	P	A	6	D	P
0	0		-		2	A	0
1	1		-		3		1
2	2		2		4		2
3	3		3		5		3
4	4		4		6		4
5	5		5		7		5
6	6		6		2	C	6
7	7		7		3		7
V	P	B	P	B	7	D	V
8	0		-		4	C	8
9	1		-		5		9
10	2		2		6		10
11	3		3		7		11
12	4		4		2	D	12
13	5		5		3		13
14	6		6		4		14
15	7		7		5		15

24108 A

Figure 7-11. Data Register Input

LONGITUDINAL REDUNDANCY CHECK REGISTER (LRCR)

- Consists of nine binary-operated flip-flops.
- Operated from high-bit or low-bit latches of the skew register.
- Each flip-flop maintains an odd-even count of the bits read from the corresponding tape unit track.
- Output is checked at the end of each read or write operation.
- LRCR is reset (all flip-flops turned off) during the XIO control word cycle (E-1 Cycle).

All nine positions of the register are turned off before each data read or write cycle. As characters are read from tape and loaded into the skew register high-bit latches, each LRCR flip-flop will be turned on with the first bit, off with the second, on again with the third, etc., throughout the tape record. The bit-count of each tape record, when written, is always made even by the check character (second check character in 9-track mode); therefore, all positions of the LRCR should be off (even count) after being set by each bit of the record including the check character(s).

All the outputs of the register are ORed together and at the end of the read operation (RDD 159-175) the OR circuit output is sampled. If any LRCR flip-flop is on, the tape data error flip-latch is turned on.

CYCLIC REDUNDANCY CHECK REGISTER (CRCR)

- Consists of nine flip-flops, each with a binary input circuit (Figure 7-12).
- Input to each CRCR position is from the corresponding R/W register position, conditioned by the other CRCR positions.
- During a nine-track write operation, the CRCR generates the first check character to be written four spaces after the last data character.
- During a nine-track read operation, the CRCR calculates a new cyclic redundancy check (CRC) character to be exclusively ORed with the original CRC character read from tape.

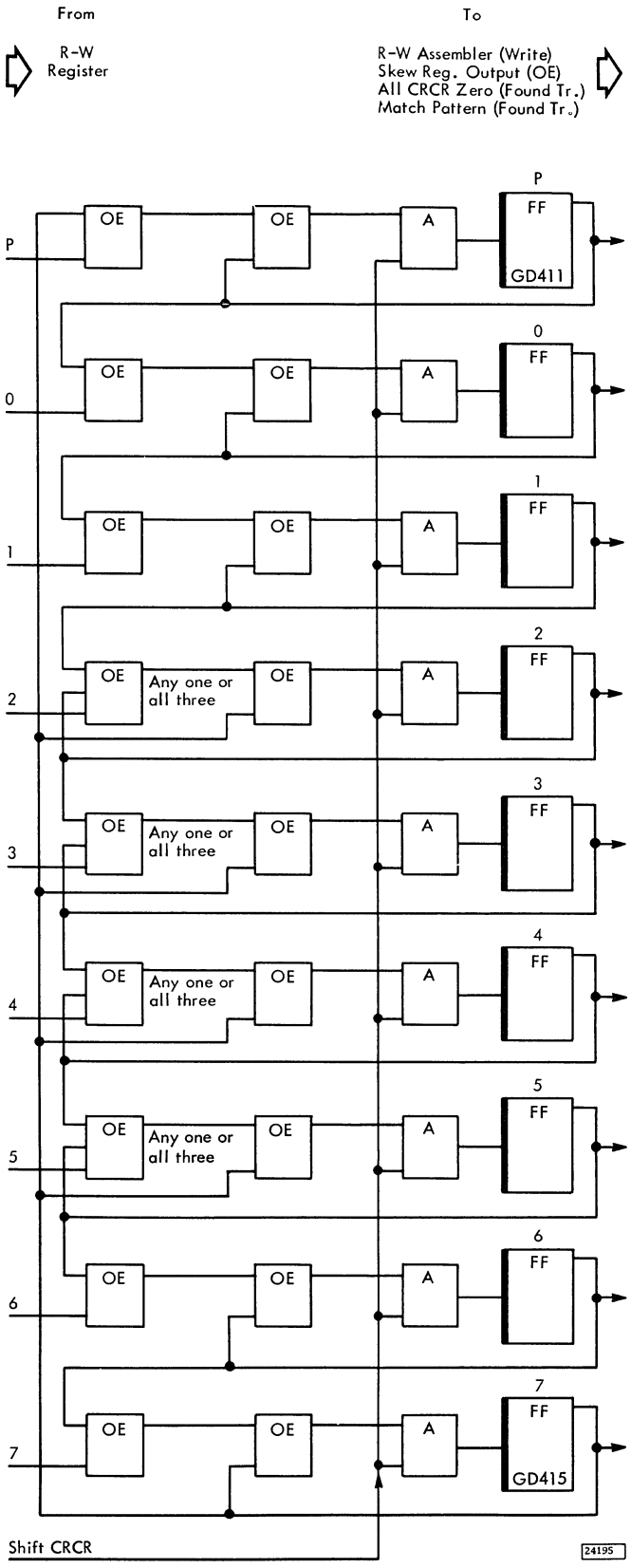


Figure 7-12. Cyclic Redundancy Check Register

As each character passes through the R/W register it is gated by a shift pulse, into the CRCR in a form determined by the previous CRCR combination. The character in CRCR after each shift is a combination of the R/W register character and the previous CRCR characters. If the CRCR is blank, the first character is loaded unchanged into the CRCR. When there are bits in CRCR, the character from the R/W register is modified as it is loaded into CRCR.

During write disconnect delay (WDD) 51-54 of a write operation the outputs of CRCR bit two and four are written on tape in true form; all other CRCR outputs are written in complement form.

During a read operation, another CRC character is generated, the true form of which is exclusively ORed with the original CRC character after it is read from tape. The result should be the match character (111010111); a CRCR error is indicated if the result is not the match character. Section 3 contains an error correction example.

ERROR PATTERN REGISTER (EPR)

- Consists of nine flip-flops with binary input circuits; similar to the cyclic redundancy check register (Figure 7-13).
- All positions have inputs from the preceding EPR position and positions 2, 3, 4, and 5 are exclusively ORed with the output of position 7 gated by the shift EPR pulse.
- EPR creates a high-clip VRC error pattern, which in comparison with CRCR specifies the track in error for error correction.
- Outputs are gated to the corresponding high-clip latches of the skew register.

As in the CRCR, the condition of position 7 determines how positions P, 2, 3, 4, and 5 are affected by the inputs. As a record is read, each vertically redundant character conditions the turn-on of EPR-7. If EPR 6 and 7 are off, position 7 is turned on by the shift pulse. If EPR 6 and 7 are both on, position 7 is turned off by the shift pulse.

The binary inputs to all EPR positions are gated by the shift EPR pulse (at RDD 167) during second-check-character time to set a one into position P for counting down to position 7. The position containing this count at the end of the operation indicates the track in error.

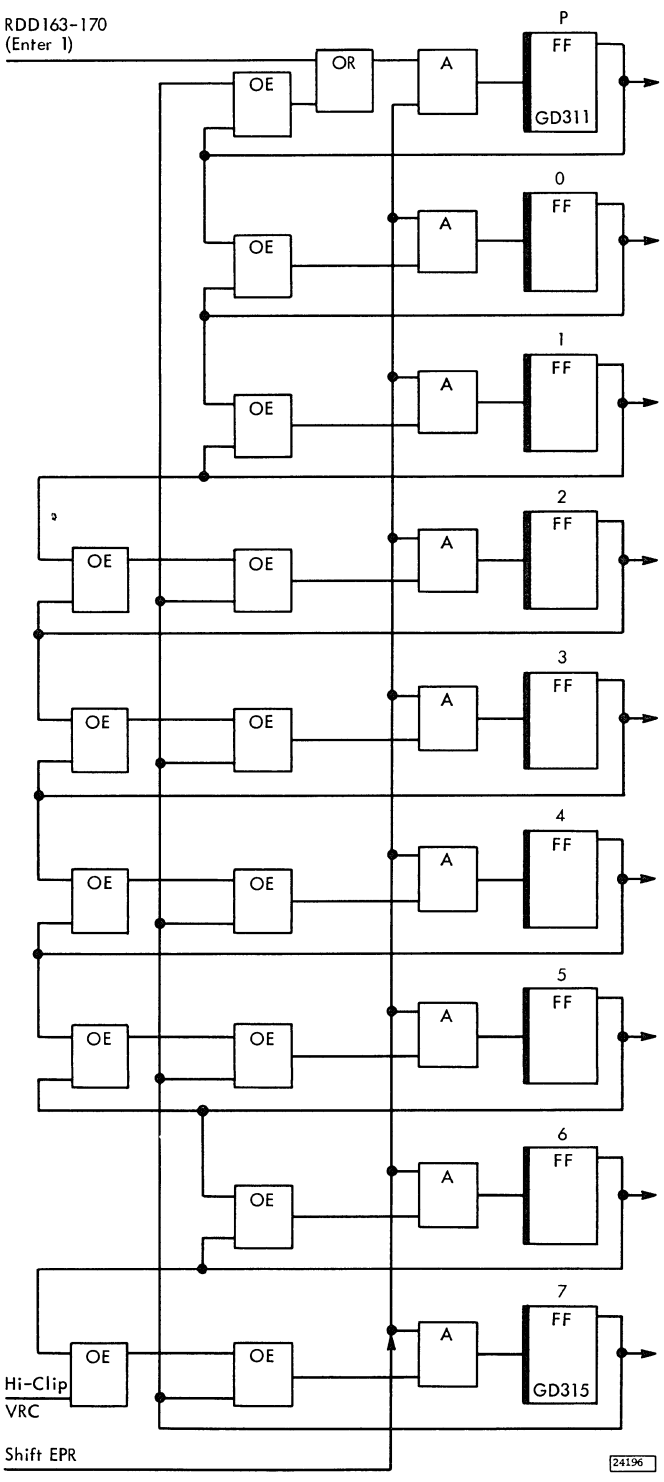


Figure 7-13. Error Pattern Register

CHAPTER 3 PRINCIPLES OF OPERATION

- The operation of the tape control unit is described in this section.
- The operation of the magnetic tape units is described in IBM Field Engineering Theory of Operation, 2401, 2402, 2403 Magnetic Tape Units Models 1, 2, and 3. (See FE Bibliography – 1800 System, Form Y26-0560.)
- The descriptions refer to diagrams found in the 1800 Maintenance Diagram Manual, provided as a system document.
- Figure 7-14 is a block diagram of the circuits used in the read and write operations.

READ OPERATION

- The tape control unit determines if the operation can be executed.
- The tape control unit is conditioned for read operation.
- If the previous operation left the tape unit in backward status execute a turnaround sequence.
- Start read delay and turn on the go flip-latch to start tape motion.
- At the end of read delay, turn on read condition to look for data from tape.
- Read and check the data. Gate data from the tape unit through:
  1. Final amplifiers
  2. Skew register (high or low)
  3. Read/write register
  4. Data register
- Read the check characters when the end of data is reached.
- Stop tape motion and reset the control unit.
- Objectives of the read operation are listed on MDM GB40122.
- The I/O operation diagram is on MDM GB40121.
- Flow charts of the read operation begin on MDM GB60121.
- Timing charts for the read operation begin on MDM GB70121.

Control Word Cycle

- E-1 cycle of the execute I/O (XIO) instruction.
- Transfers the control word of the I/O control command to the out bus.
- Area, function, and modifier bits are decoded by the tape control unit.
- If area is that assigned to tape control, turn on delay-commands to allow time for the tape control unit to receive all the control data from the P-C.
- Delay commands ANDed with initialize-read turn on the initialize-read-remember flip-latch at T6 time.
- Initialize-read-remember activates the busy line.

Data Word Cycle (DWC)

- E-2 cycle of XIO instruction.
- Delay commands, initialize read remember, and XIO-DWC activate the cycle-steal-acknowledge line.
- Cycle steal acknowledge conditions a line that gates the address of the first word in the data table to the specified channel address register (CAR).
- Send cycle steal request to the P-C.

First Cycle Steal Cycle

- Load word counter and set scan-control circuits.
- Word counter is loaded from bits 2 through 15.
- Scan-control bits are bits 0 and 1.
- The operation of the word counter is described in the Functional Units section of this chapter.
- Reset delay-commands.

The first word of the data table contains the word count and scan control bits. (If the data table has been chained, the word count and scan control bits are in the second word.) The word count word is placed on the out bus by the data channel. Positions 2 through 15 are gated into the word counter by cycle steal acknowledge (CSA) and the CSA control triggers (Figure 7-15).

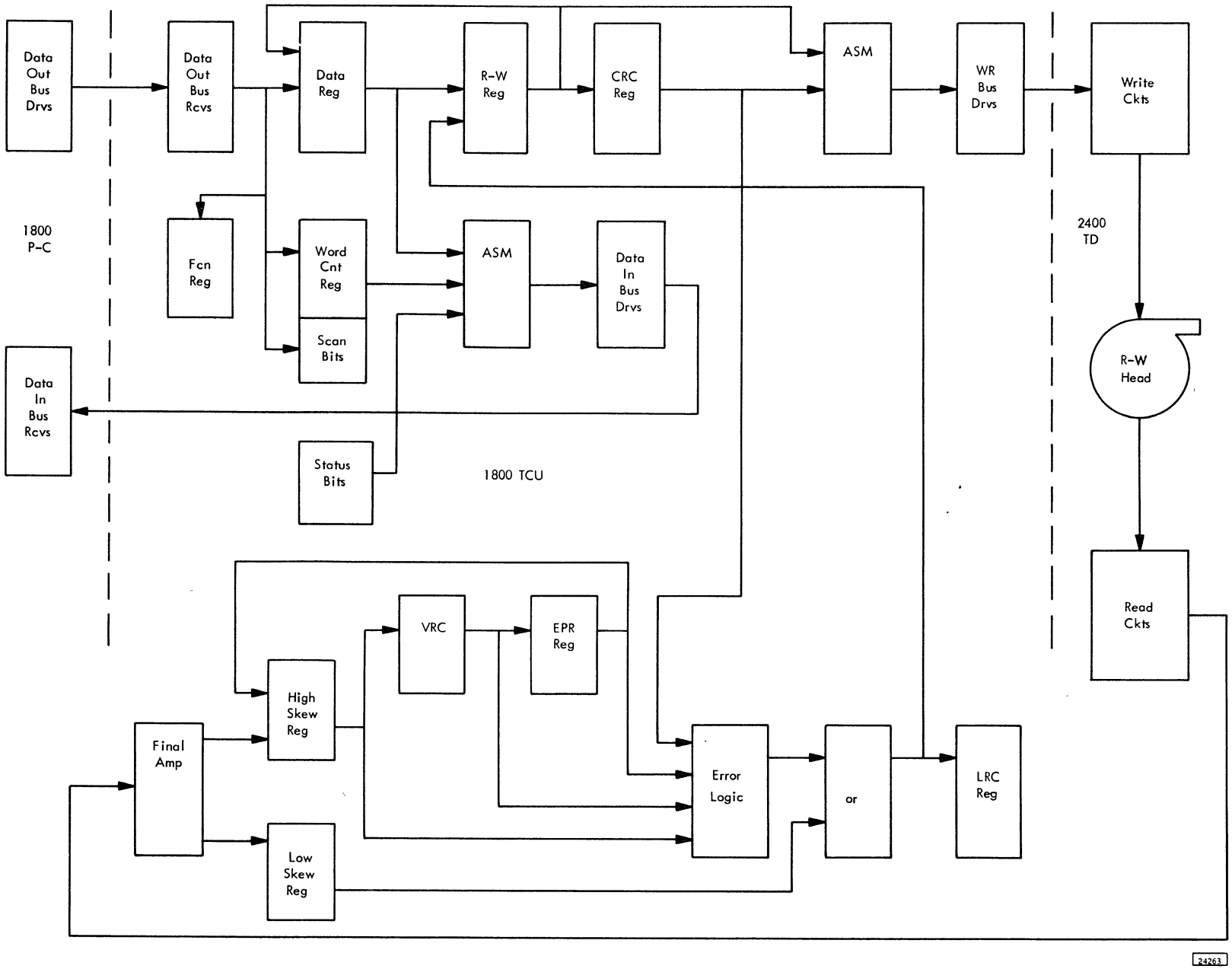
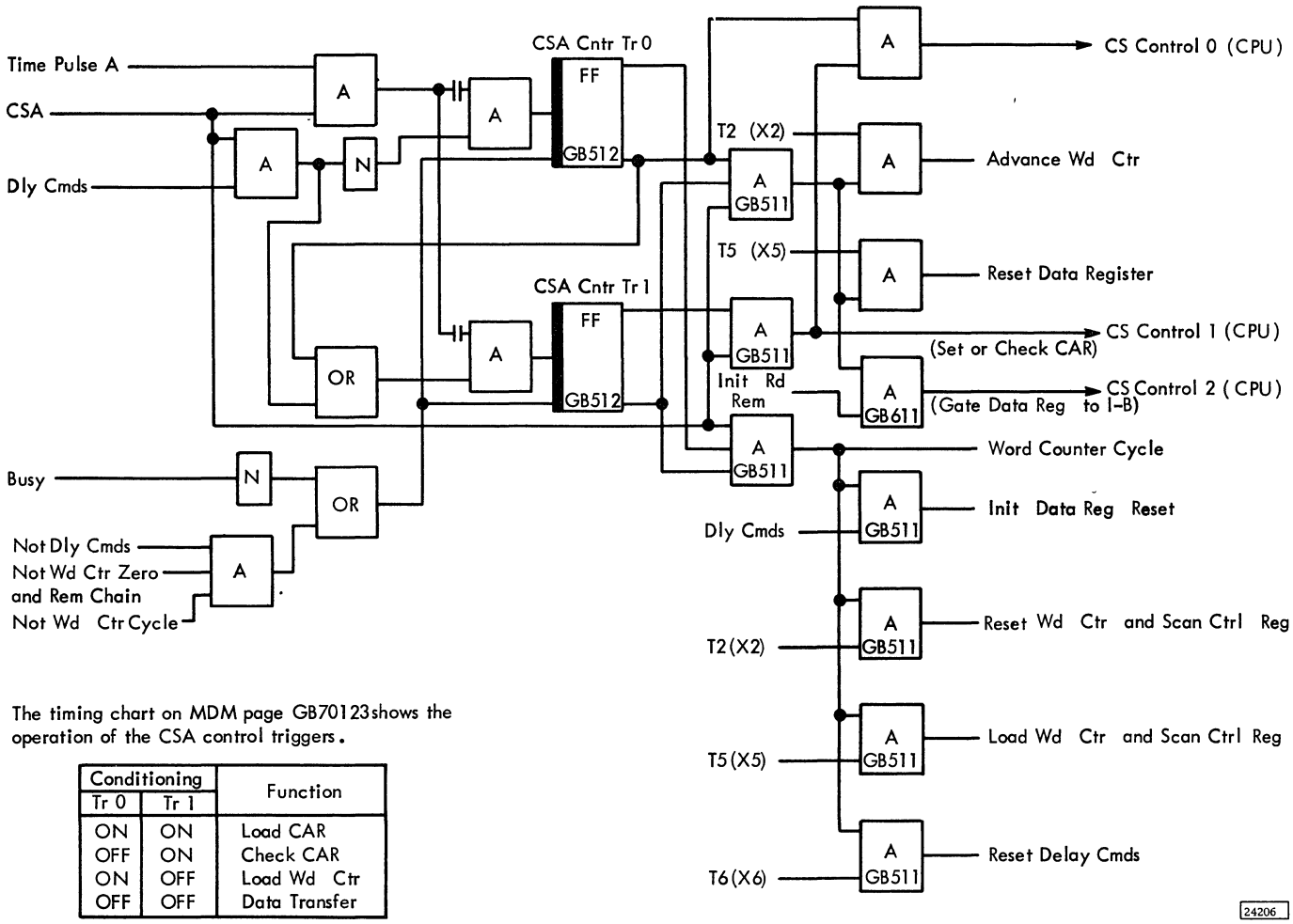


Figure 7-14. Tape Control Unit Block Diagram



The timing chart on MDM page GB70123shows the operation of the CSA control triggers.

Conditioning		Function
Tr 0	Tr 1	
ON	ON	Load CAR
OFF	ON	Check CAR
ON	OFF	Load Wd Ctr
OFF	OFF	Data Transfer

Figure 7-15. Cycle Steal Acknowledge Control Triggers

Scan control consists of two flip-latches, which are end-of-table (EOT)-interrupt-remember and chain-remember. A zero-bit in bit position one turns on the EOT-interrupt-remember flip-latch to cause an interrupt when the word count reaches zero.

A one-bit in position zero turns on the chain-remember flip-latch to re-initialize the tape control unit when the word count reaches zero. Re-initializing the tape control unit causes a new CAR address to be loaded, and a new word count and scan control setup for the next data table.

Cycle Steal Data Cycles

- Fall of delay-commands activates read.
- Check need for turnaround operation.
- If no turnaround operation is required, set read-status and start read-delay.
- After read-delay has allowed time for tape to reach speed, turn on read-condition.
- Tape character is set into the skew register.
- The first bit of each tape character read from tape turns on the first-bit latch.
- First-bit starts the read clock.
- At RC-7 time, start read-disconnect-delay (RDD) to test for check-character time.

Read activates read-delay at the end of delay commands. The read-delay line:

1. Sets the go flip-latch. The active go flip-latch output causes the selected tape unit to move tape forward.
2. Conditions millisecond-delay-counter drive circuts. The delay counter advances in millisecond mode at a rate determined by the tape unit designated to read the record. While read-delay

is active, tape on the selected tape unit accelerates to proper operating speed. Because the read head on the tape unit was positioned either in an interrecord gap, or, in the gap between load-point and the first tape record when the operation began, characters do not transfer to the tape control unit immediately after tape movement begins.

If tape on the selected tape unit was not at load-point when the read delay started, the read-condition flip-latch turns on when the delay counter advances:

1. To 28, if a model 3 tape unit equipped with the 7-track feature is selected.
2. To 15, if a model 3 tape unit not equipped with the 7-track feature is selected.
3. To 31, if a model 1 or 2, 7-track tape unit is selected.
4. To 17, if a model 1 or 2, 9-track tape unit is selected.

If tape on the selected tape unit is at load-point when the read delay begins, the load-point delay flip-latch is set, blocking the set path to the read-condition flip-latch until the delay counter advances to 160 for model 3 or to 103 for a model 1 or 2. Regardless of the original position of tape on the selected tape unit, read delays are shorter than corresponding write delays to ensure that read circuits are conditioned soon enough to read the first character in the tape record.

The read-condition flip-latch blocks read delay, which resets the delay counter. Read-condition also activates the first-bit and read-clock circuits to look for data from the tape unit. Between the times that tape control sets the go and read-condition flip-latches, tape accelerates to proper operating speed.

Accept Characters

Each input character from the tape unit enters tape control final amplifiers. Final amplifiers contain a separate track for each bit position. A final amplifier track has two outputs, a high- and low-clip output. Input bits to corresponding final-amplifier tracks must meet predetermined minimum amplitude requirements to produce high- and low-clip outputs. The high-clip output from each final-amplifier track sets the corresponding high-clip skew-register flip-latch; the low-clip output from each final-amplifier track sets the corresponding low-clip skew-register flip-latch. Theoretically, all bits in a character should arrive at the input to the final amplifiers simultaneously; however, all bits may not arrive at exactly the same time. The first high-clip output from any final-amplifier track sets the first-bit latch to start the read clock.

It is possible to have a character in the low-clip skew register and nothing in the high-clip skew register because of low amplitude pulses from the tape unit.

Read Clock Cycles

The output of the read clock at 7 time sets the read-disconnect-delay (RDD) flip-latch. RDD conditions microsecond-delay-counter drive circuits, and the delay counter steps in microsecond mode at the rate determined by the tape unit reading the record. If the next character from the tape unit is not a check character, the read clock output at RC 4 time resets the RDD flip-latch, stopping the delay counter. The next tape character must arrive at the tape control soon enough to start the read clock before the delay counter advances to 36 or tape control will turn on the first check character flip-latch and process the character as a check character.

In 9-track operation, the high-clip skew register is used for every character. The low-clip skew register can be gated out only during 7-track operation. After RC-7 time, the read clock generates RC Reset to:

1. Reset the first-character flip-latch (only at the end of the first read clock cycle).
2. Reset the first-bit flip-latch, blocking drive pulses to the read clock; the clock resets and cannot start again until the next character from the tape units sets the first-bit flip-latch.
3. Reset the high-and-low-clip skew registers.

Read Data Gating - Nine-Track, or Seven-Track Two-Bytes.

The byte generator, a two position binary counter, described in the Functional Units section, provides the pulses that gate data in the specified byte format from the R/W register to the data register. The byte generator and its associated circuits are shown on MDM GB40182; the timing chart is on MDM GB70124.

The following circuit objectives relate to these diagrams and assume an initial condition of both BT0 and BT1 off (byte A time). Figures 7-16 and 7-17 shows the data gating for nine-track and seven-track two-byte read operations.

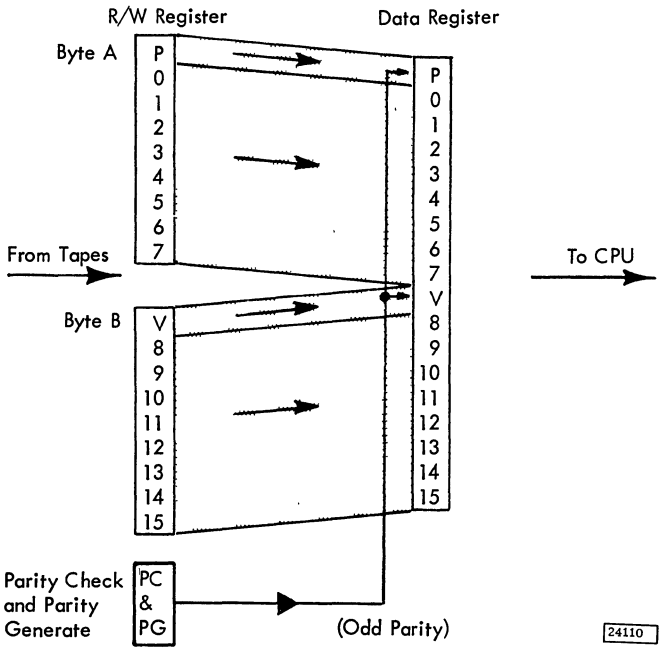


Figure 7-16. Read Data Gating - Nine-Track

Reset R/W Register. At RC-7 time, R/W strobe fires a 150-nsec single-shot, the output of which resets the R/W register.

Gate Data to R/W Register (Byte A). The timing-out of the 150-nsec single-shot pulse (reset R/W register) fires a 300-nsec single-shot that gates the tape character that is in the skew register into the R/W register. If 7-track tape is being read, positions 0 and 1 will be reset and a parity bit generated to produce bits C, B, A, 8, 4, 2, and 1.

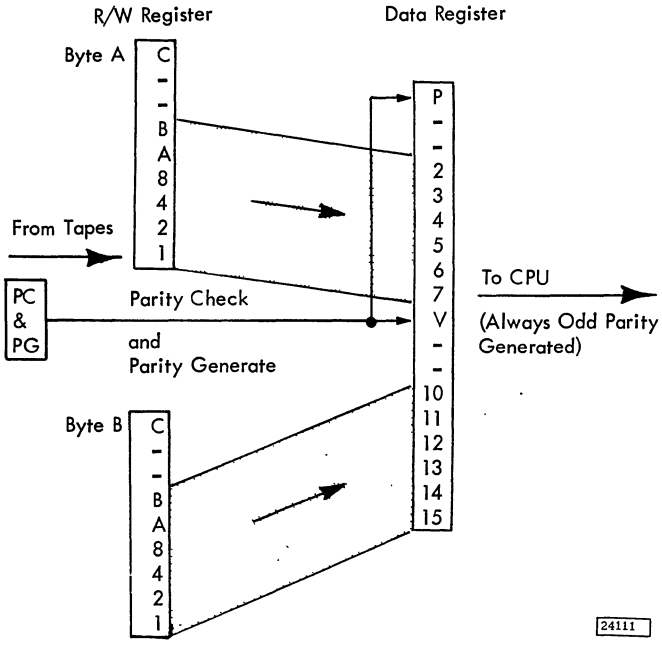


Figure 7-17. Read Data Gating - Seven-Track-Two-Byte

Step Byte Generator. The timing-out of the 300-nsec single-shot (R/W gate) turns on BT0 to establish the byte B condition.

Gate Byte A to Data Register. The rise of byte B, after any cycle steal acknowledge, fires a 350-nsec single-shot to condition a line that gates R/W register bits P through 7 to positions P through 7 of the data register.

Parity Check R/W Register (Byte A). The timing-out of the 350-nsec single-shot fires a 200-nsec single-shot. The output pulse of this 200-nsec single-shot (R/W check gate) conditions the R/W VRC error circuit. If the R/W register has even parity and 9-track or 7-track-odd-parity is specified or vice-versa for 7-track, a R/W VRC error is indicated.

Reset R/W Register. Same as for byte A.

Gate Data to R/W Register (Byte B). The timing-out of the 150-nsec single-shot fires the 300-nsec single-shot that activates a line (read gate). The read gate line, in turn, gates the tape character from the skew register into the R/W register. These nine, or seven, bits make-up byte B.

Gate Byte B to Data Register. The 300-nsec single-shot (R/W gate) pulse also activates a line that gates this second tape character from the R/W register to positions V and 8 through 15 of the data register. Notice on the timing chart (GB 70124) that byte A is gated to the data register at the beginning of byte B time (by gate byte A) and byte B is gated to the data register at the end of byte B time (by R/W gate).

Request Cycle Steal. During byte B time, if the word count register does not equal zero, the 300-nsec (R/W gate) pulse turns on the data cycle steal request (CSR) flip-latch.

Step Byte Generator. The timing-out of this same 300-nsec single-shot turns off the BT0 flip-flop. BT0 going off does not turn on BT1 because the 3 bytes per word line is not active. The byte generator is now at the byte-A condition for the next tape character.

Parity Check R/W Register (Byte B). The timing-out of the 300-nsec single-shot (R/W gate) also fires another 200-nsec single-shot (R/W check gate). The output pulse of this single-shot conditions the R/W VRC error circuits.

Gate Data to the P-C (18-bit word). Cycle steal acknowledge, from the P-C, gates the data register output onto the in bus. At this time, byte A of the next tape character may be in the R/W register.

Read Data Gating - Seven-Track, Three Bytes.

In seven-track, three-bytes-per-word format, the byte generator is stepped through bytes A, B, C and D. Byte B does not gate any data; therefore, only three bytes of data form the word in the data register. During the other three byte times - A, C, and D - data is gated as in the two-byte format except for the differences that are indicated in the following circuit objectives. The circuits described are on MDM GB40182 and the timing chart is on MDM GB70125. Figure 7-18 shows the format of the data gating for seven-track, three byte, read operation. Figure 7-19 shows the timing of the data gating for seven-track, three bytes read.

Reset R/W Register: Same as two-byte format.

Gate Data to R/W Register: Same as two-byte format.

Step Byte Generator to Byte B. The fall of the 300-nsec single-shot (R/W gate) turns on BT0 to establish the byte B condition. This is the same as for two-byte format because the degate-byte-generator-read line is inactive at this time.

Gate Byte A to the Data Register. The rise of byte B, after any cycle steal acknowledge, fires a 350-nsec single-shot. In three-byte format, this pulse conditions a line called gate-byte-A-read-3-bytes-per-word. This line does not gate R/W register outputs P through 7 directly into the data register as in two-byte format. As shown in Figure 7-9, data register positions P, 6, and 7 are not loaded; positions 0 through 5 are loaded from R/W register positions 2 through 7. This selective loading is accomplished by the gate-byte-A-read-3-bytes-per-word line.

Parity Check R/W Register (Byte A). Same as two-byte format.

Step Byte Generator to Byte C. Three-bytes-per-word enables the gate-byte-A pulse (350-nsec single-shot) to de-activate the BT0 input. The fall of gate-byte-A then turns off BT0. Three-bytes-per-word also enables the turn-on of BT1 and the byte generator is stepped to the byte C condition (BT0 off, BT1 on).

Reset R/W Register. Same as two-byte format.

Gate Data to R/W Register. Same as two-byte format.

Gate Byte C to Data Register. During byte C, the 300-nsec single-shot (R/W gate) pulse activates a line that gates R/W register positions 2 and 3 to data register positions 6 and 7. This line also gates positions 4, 5, 6, and 7 to data-register positions 8, 9, 10, and 11.

Step Byte Generator to Byte D. The timing-out of the 300-nsec single-shot (R/W gate) turns on BT0; BT1 remains on, establishing the byte D condition.

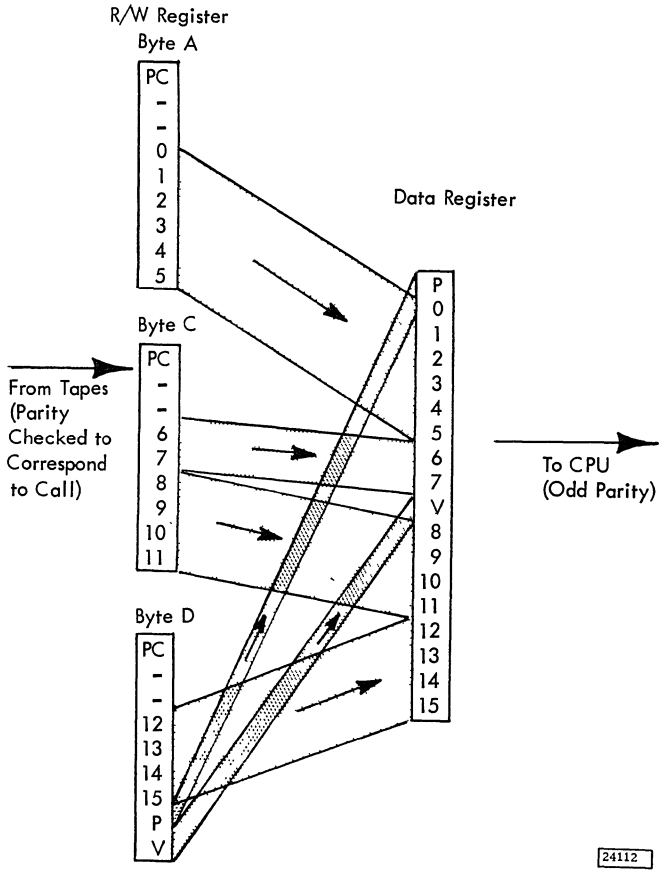


Figure 7-18. Read Data Gating - Seven-Track-Three-Byte

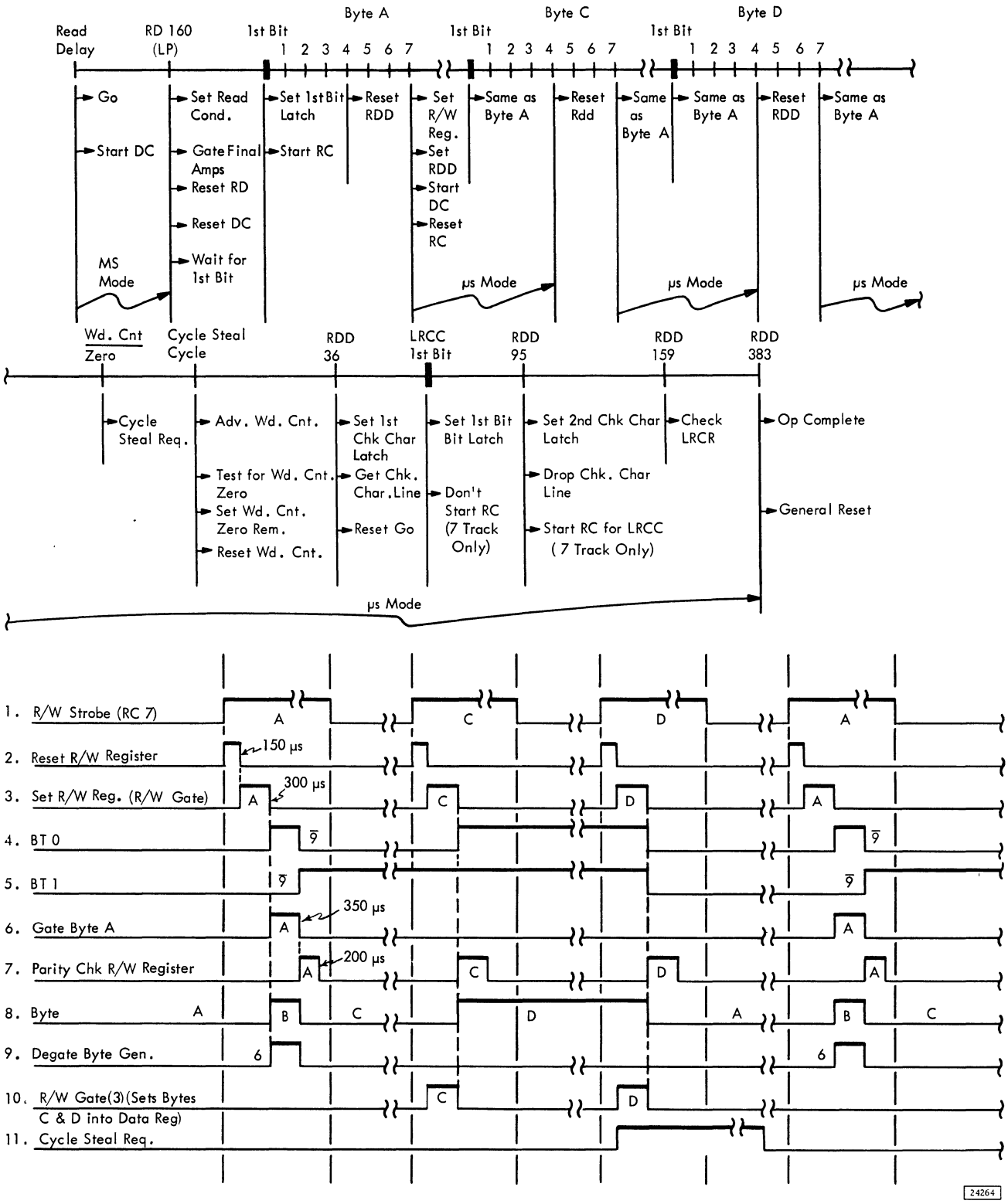


Figure 7-19. Timing: Read Data Gating, Seven-Track Three-Byte

Parity Check R/W Register (Byte C). Read-gate, a line activated by the 300-nsec single-shot, ANDs with byte-trigger-1 (BT1) to fire 200-nsec single-shot (R/W check gate) to condition the R/W vertical redundancy check (VRC) error circuits.

Reset R/W Register. Same as other bytes.

Gate Data to R/W Register. Same as other bytes.

Gate Byte D to Data Register. During byte D time, the 300-nsec R/W gate single-shot pulse activates a line that gates R/W register positions 6, 7, and 2 through 5 to Data register positions P, V, and 12 through 15, respectively.

Step Byte Generator to Byte A. The timing-out of the 300-nsec single-shot (R/W gate) turns off BT0 which turns off BT1, establishing the byte A condition for the next tape character.

Parity Check R/W Register (Byte D). Same as for byte C.

Request Cycle Steal. The R/W gate pulse and byte D turn on the data CSR flip-latch.

Gate Data to P-C. Cycle-steal-acknowledge, from the P-C, gates the data register outputs onto the in bus.

Cyclic Redundancy Check Character.

In 9-track operation, each data character is shifted into the cyclic redundancy check register (CRCR) from the R/W register. Because of the shift pattern within the CRCR, a cyclic check character is developed. At the end of a record in read operation, the cyclic redundancy check character (CRCC) should match the CRCC generated when the record was written. At the end of the record, the CRCC developed from the data characters is combined with the CRCC read from tape. The result should be the match pattern (111010111) in the CRCR.

If the record contains error characters, the CRCR is used in conjunction with the error pattern register (EPR) to analyze and, if possible, correct the errors. For detailed information about the actual error correction operation, see the description of the error correction operation.

The process of analyzing an error condition occurs between read disconnect delay (RDD)-159 and RDD-222. If the errors are in one track only, the tape control will turn on the found-track flip-latch.

Check Character Cycles

In a normal read clock cycle, tape control sets the RDD flip-latch at read clock (RC)-7 time, allowing the delay counter to advance in microsecond mode; at RC-4 time of the following normal read clock cycle, tape control resets the RDD flip-latch, stopping the delay counter. Normal character spacing in the tape record allows the tape unit to transfer at least one bit in a character to tape control to start the read clock and stop the delay counter before the counter advances to 36 to set the first-check-character flip-latch.

Because the check characters are spaced farther from the last data character in the tape record than normal character spacing, the delay counter advances to 36 after tape control processes the last data character. RDD-36 sets the first-check-character flip-latch, indicating the next character the tape unit transfers is the first-check-character. The tape record might have blank check-characters. If no bits are received between RDD-36 and RDD-95, the CRC character (9-track only) is assumed to be blank. In 7-track operation the longitudinal redundancy check (LRC) character should be received between RDD-36 and RDD-95.

At RDD-95 the second-check-character flip-latch is turned on. In 9-track operation the second check character is the LRC character. In 7-track operation there is no second check character.

The tape control unit examines check-character bits stored in the high-clip skew register for a parity error. If a check-character parity error is detected in the high-clip skew register during 7-track operation, the low-clip skew register is gated to the LRC register and the R/W register. For other conditions the high-clip skew register is gated out.

During second-check-character time, RDD-95 to RDD-383, the skew registers cannot enter the R/W register. The 9-track LRC character is gated to the LRC register but not to the R/W register.

At RC reset time, the tape control unit resets the first-bit flip-latch and the skew registers. Because the LRC character is the last character the tape unit transfers to tape control, the read clock does not run again in the read operation.

CRCC Parity: The parity of the CRCC depends upon the configuration of the record. If the character-count flip-flop is off (even count), the CRCC parity should be odd. Check character parity error is indicated by read-high-clip VRC (tape CE diagnostic indicator).

LRCC Parity: In nine track operation, the LRCC parity is always odd. In seven-track operation, LRCC parity depends upon the parity call and the character count as follows:

Even parity call – always even parity LRCC
Odd parity call
even character count – even parity LRCC
odd character count – odd parity LRCC

Check character parity error is indicated by read-high-clip VRC (tape CE diagnostic indicator).

End of Data Table

- If the scan-control latches so specify, end-of-table (EOT) interrupt is activated when the last data word is transferred.
- If chaining is specified by the scan control latches, transfer of data to the next data table is started without program control.

If the end-of-table-interrupt-remember latch is on, word-count-equal-zero and cycle-steal-acknowledge causes an interrupt request. Bit three of the device status word (DSW) will indicate end of table when the sense interrupt level command is executed.

If the chain-remember flip-latch is on, word-count-equal-zero sends three cycle steal requests to the P-C. The word that is placed on the out bus by the cycle steal is the word that follows the last data word in the data table and is the address of the first word in the next data table. If the cycle-steal-control-0 line is active and the cycle-steal-control-1 line is inactive (Figure 7-15), this address is loaded into the specified channel address register (CAR).

The next cycle steal cycle places the first word of the new table on the out bus. This first word contains its own address. The cycle-steal-control-0 and -1 lines are activated to condition the CAR check circuits. If the address on the out bus does not compare equally with the contents of the specified CAR, a CAR check is indicated. The CAR check logic is shown on MDM CC30101.

The next word in the new data table contains the word count and scan-control bits. If this is the last table to be chained, bit position zero contains a zero so that the chain-remember flip-latch is not turned on and bit position one contains a one to turn on, or a zero to turn off, the end-of-table-interrupt-remember flip-latch.

End Read Operation

- Read-disconnect-delay (RDD) flip-latch is turned on at RC7. This places the delay counter in μsec mode.
- Delay counter is reset at each RC4 time (first bit of next tape character starts read clock).
- After the last data character is read, the delay counter will continue to advance.
- At RDD36, the go flip-latch is turned off and first-check-character flip-latch is turned on.
- If 7-track, read LRC character and end operation at RDD383.
- If 9-track, read CRC character; at RDD96, 2nd check-character flip-latch is turned on and LRC character is read; gate CRCR and EPR to locate error track if any; end operation at RDD383.

First Character Tape Mark

The first character transferred to the tape control unit in a read operation causes final-amplifier tracks to produce high- and low-clip outputs that set corresponding high- and low-clip skew register positions. The first high-clip output from any final-amplifier track sets the first-bit flip-latch, causing the read clock to start.

The first-character flip-latch, set during the data word cycle, is on during the first read-clock cycle in the operation, allowing the read clock output at RC-6 time to check the character in the high-clip skew register for the tape mark bit configuration.

A tape mark in 9-track is composed of bits in positions 3, 6, and 7 and no bits in P, 0, 1, 2, 4, or 5. A tape mark in 7-track is composed of bits in positions 4, 5, 6, and 7, and no bits in P, 2, or 3. Tracks 0 and 1 are not used in 7-track operation.

A true tape-mark record contains only a tape mark followed by a check character with the same bit structure. The tape control unit holds the first character in the R/W register until the next character is received. The character spacing and bit configuration determine whether the record is a tape mark or data.

If the character in the high-clip skew register has the bit configuration of a tape mark, the tape control unit turns on the first-character-tape-mark flip-latch at read clock 6 time (Figure 7-20). The tape control must now wait for the next character to see if the record is a true tape mark. This check is made by the character-after-tape-mark flip-latch, turned on by the first-character-tape-mark and a read-clock-4 pulse (2nd character).

If a third character is read, the record is not a true tape mark record. This possibility is checked by a circuit that turns off both the first-character-tape-mark and the character-after-tape-mark flip-latches if a read-clock -0 +1 pulse is detected when the character-after-tape-mark flip-latch is on.

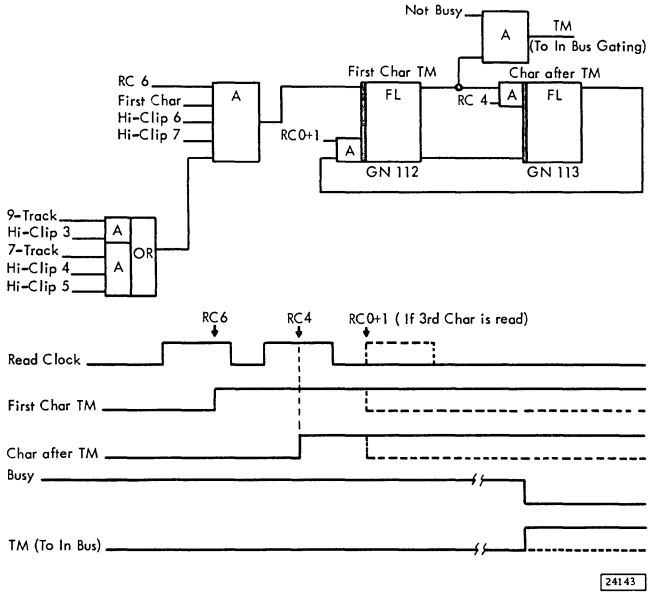


Figure 7-20. Tape Mark Recognition

In this case (third character read) the tape mark indication is not placed on the in bus because the first-character-tape-mark flip-latch is turned off before the busy line drops.

At RC-7 time in the first read-clock cycle:

1. The tape control unit turns on the read-disconnect-delay (RDD) flip-latch. RDD conditions microsecond delay-counter-drive circuits, and the delay counter steps in the microsecond mode at the rate determined by the model of the tape unit reading the record.
2. The tape control unit checks the character in the high-clip skew register for a parity error. The high-clip skew register possibly contains a character with the structure of a tape mark as the result of an error. A BCD tape mark is always an even parity character; an 8-bit code tape mark is always an odd parity character.

At RC reset time, the tape control unit:

1. Resets the first-character flip-latch.
2. Resets the first-bit flip-latch, causing the read clock to reset.
3. Resets the high- and low-clip skew registers.

If the delay counter advances to 36 before the next tape character produces a high-clip output from final amplifiers, the tape control unit sets the first-check-character flip-latch. The tape mark character stored in the R/W register on the previous read clock cycle has also been transferred to the data register.

WRITE COMMAND OPERATION

- Determine if command can be executed.
- Condition tape control for write operation.
- If previous command was a backward operation do a turnaround sequence.
- Start write delay and tape motion.
- Condition write and read circuits after write delay.
- Write and read-check the data record.
- Send end-of-table interrupt.
- Start disconnect delay and write check character(s).
- Stop tape motion and complete read-check of record.
- Objectives of the write operation are listed on MDM GB 401 22.
- The I/O operation diagram for the write operation is on MDM GB 401 31.
- Flow charts of the write operation begin on MDM GB 601 31.
- Timing charts for the write operation begin on MDM GB 701 31.

Control Word Cycle

- E-1 cycle of the XIO instruction transfers the control word of the I/O control command to the out bus.
- Area, function, and modifier bits are decoded by the tape control unit.
- If area is that assigned to the tape control unit, delay-commands is turned on to allow time for the tape control unit to receive all the control data from the P-C.
- Delay-commands and initialize-write decode turns on initialize-write-remember at T6.
- Initialize-write-remember activates the busy line.

Data Word Cycle (DWC)

- E-2 cycle of XIO instruction.
- Cycle steal acknowledge (CSA) is sent to the P-C.
- Cycle steal acknowledge and CSA-control-trigger-1 together gate the address word of the I/O control command into the specified channel address register.

- Two initial cycle steal requests are generated to obtain word count and scan control bits (first cycle steal cycle), and, the first data word from the data table (second cycle steal cycle).
- Turn on the first-character flip-latch; to be used in a later cycle.

First Cycle Steal Cycle

- Load the word counter and set the scan-control circuits at T5 time.
- Word counter is loaded from bits 2 through 15.
- Scan-control bits are bits 0 and 1.
- The operation of the word counter is described in the functional units section of this chapter.
- Reset delay commands.
- Activate write op.

The first word of the data table contains the word count and scan-control bits. (If the data table has been chained, the word count and scan-control bits are in the second word.) The word-count word is placed on the out bus by the data channel. Positions 2 through 15 are gated into the word counter by cycle steal acknowledge and the CSA control triggers.

Scan control consists of two flip-latches, end-of-table (EOT)-interrupt-remember and chain-remember. A zero-bit in bit position one turns on the EOT-interrupt-remember flip-latch to cause an interrupt when the word count reaches zero.

A one-bit in position zero turns on the chain-remember flip-latch to re-initialize the tape control unit when the word count reaches zero. Re-initializing the tape control unit causes a new CAR address to be loaded, this CAR address to be checked, a new word count and scan control setup for the next data table, and the first data word to be sent to the tape control unit.

Cycle Steal Data Cycles

- Load data register with the first data word (18 bits).
- Advance the word counter.

While cycle steal acknowledge is still active, T2 advances the word counter and resets the data-CSR (cycle steal request) flip-latch. The same circuits, cycle steal acknowledge and CSA control, gate the reset of the data register at T5 time. The out bus is gated to the data register at T6 of every cycle except the first cycle steal cycle (word count cycle). The first data word, placed on the out bus by the data channel circuits, is loaded into the data register at T6.

Write Delay and Tape Motion

- Check need for turnaround delay.
- Activate write status in tape unit.
- Initiate write delay.
- Turn on the go flip-latch.
- Turn on read-condition flip-latch for read checking while writing.
- Turn on write-condition flip-latch after write delay has reached the specified delay.

If backward-memory-status is not active, turnaround delay is not needed. A signal is sent to the tape unit to activate write-status, the go flip-latch is turned on to start tape motion, and a write delay is started.

Write-delay turns on the go flip-latch and activates millisecond (ms) mode. The delay counter advances in ms mode at a frequency determined by the tape unit model.

While write-delay is active, tape on the selected tape unit accelerates to proper operating speed, but the tape control unit does not transfer characters to the tape unit.

If tape on the selected tape unit is not at load point when the write-delay begins, the write-condition flip-latch turns on when the delay counter advances to 31 if a model 1 or 2 tape unit is selected, or to 53 if a model 3 tape unit is selected.

If tape on the selected tape unit is at load point when the write-delay begins, the load-point-delay flip-latch is turned on, blocking the set path to the write-condition flip-latch until the delay counter advances to 320. Because tape is not positioned at the same spot with respect to the write head after each load-rewind operation, the longer write delay (when the load-point-delay flip-latch is set) causes the tape unit to erase a section of tape approximately 3-3/4 inches long between load point and the first character in the tape record. This erasure ensures that all previously recorded data on tape are destroyed before the new record is begun.

Write and Read Condition

- Write-condition turns on after the specified delay.
- Conditions the tape unit to write the data.
- Starts the write clock to control the data flow through the tape control unit.
- Read-condition, turned on by write-condition, enables the checking of data as it is written on tapes.

The write-condition flip-latch drops write delay and stops the delay counter to permit actual writing of the tape record. However, between the time that the go flip-latch is turned on to start tape movement and the write-condition flip-latch is set, tape on the selected tape unit reached proper operating speed. In addition to ending the write delay, the write-condition flip-latch, when on, further prepares the tape control unit to perform the write operation by:

1. Setting the write-release flip-latch to allow write triggers in the selected tape unit to turn on and off as required to record characters on tape. The write-release flip-latch is reset after the tape control processes the last data character in the record to the tape unit, causing all tape unit write triggers in the on-state at that time to switch to their off-state. In returning to their reset conditions, write triggers write the longitudinal redundancy check (LRC) character at the end of the tape record. However, the resets to the off-states are gated by an all-one-bit (special) character that uses the same path as normal data. This allows deskewing of the LRC character the same as for a data character.
2. Directly setting the read-condition flip-latch if the load-point (LP)-delay flip-latch is on. If load-point is not on, read-condition is set when the delay counter advances to 17 or 32 during the write delay. The on-state of the read-condition flip-latch conditions output gates for the final amplifiers to allow the tape control to check each character that the tape unit writes.
3. Starting the write clock. Write-clock outputs establish timings that control data flow and processing in the tape control unit. The write clock cycles continuously as long as the write-condition flip-latch is on.

Write Gating - Nine-Track, or Seven-Track Two-Bytes

The byte generator, a two-position binary counter described in the Functional Units section of this chapter, provides the pulses that gate data in the specified byte format from the data register to the R/W register. The byte generator and its associated circuits are shown on MDM GB40182; the timing chart is on MDM GB70124.

The following circuit objectives relate to these diagrams and assume an initial condition of both BT0 and BT1 off (byte-A time). The data word (18 bits) is on the out bus because a cycle steal request was initiated. Figures 7-21 and 7-22 show the data gating for nine-track and seven-track two-byte write operations.

Load Data Register with P-C Data Word. At T6 time of the cycle during which the tape control unit services the cycle steal request, the out bus is gated to the data register.

Gate Byte A to the R/W Register. At T7 time, the fall of cycle steal acknowledge fires a 350-nsec single-shot. The output pulse of this single-shot

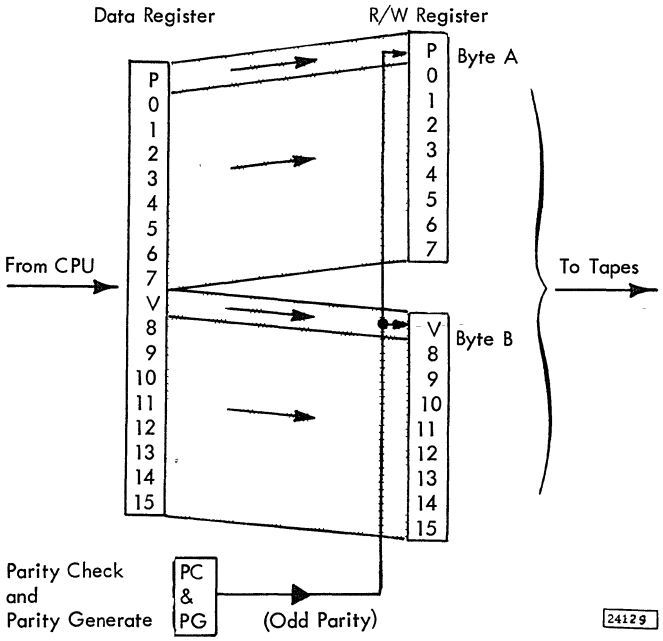


Figure 7-21. Write Data Gating, Nine-Track

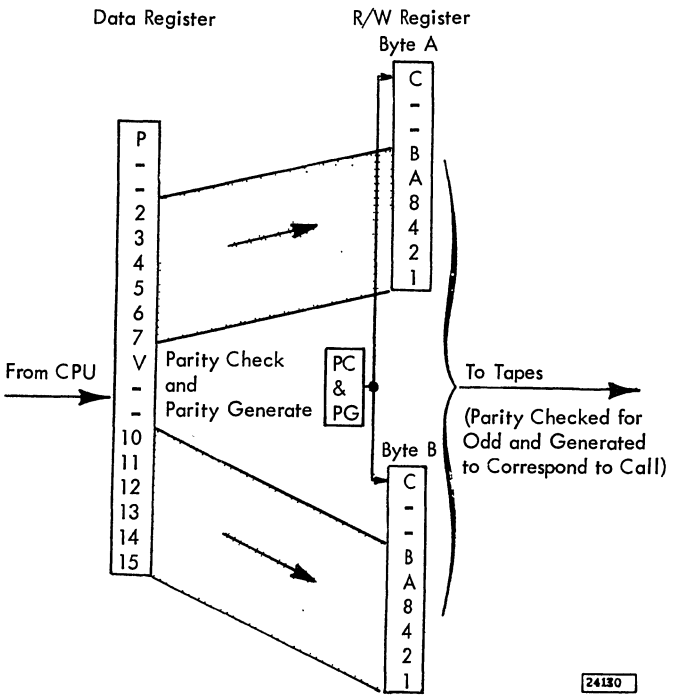


Figure 7-22. Write Data Gating, Seven-Track Two-Byte

conditions a line that gates the output of data register positions P and 0 through 7 (except for bits 0 and 1 which are lost in 7-track) into the R/W register. Write-clock pulses 6 through 10 cause the tape unit to write the R/W register output.

Parity Check R/W Register (Byte A). The timing out of the 350-nsec single-shot fires a 200-nsec single-shot. The output pulse of this single-shot activates R/W vertical redundancy check (VRC) error if the R/W register has even parity and 9-track or 7-track-odd-parity is specified or vice-versa for 7-track.

Reset R/W Register. (Prepare to gate byte B into R/W register.) At WC 14 time, byte A has been written on tape. R/W strobe fires the 150-nsec single-shot to reset the R/W register.

Step Byte Generator. The 150-nsec single-shot pulse (reset R/W register) turns on the BT0 flip-flop; BT1 is still off. This establishes byte-B time.

Gate Byte B to the R/W Register. When the 150-nsec single-shot times out, the 300-nsec single-shot (R/W gate) conditions a line that gates the output of data register positions V and 8 through 15 (except for bits 8 and 9 which are lost in 7-track) to the R/W register. Write clock pulses 6 through 10 cause the tape unit to write the R/W register output.

Initiate a Cycle Steal Request. The 300-nsec single-shot (R/W gate) turns on the data cycle steal request flip-latch. If the word count is not zero, the P-C places another data word on the out bus when it can next service the magnetic-tape cycle-steal priority.

Parity Check the R/W Register (Byte B). The timing out of the 300-nsec single-shot (R/W gate) during byte B time fires another 200-nsec single-shot (R/W check gate). The output pulse of this second single-shot activates R/W VRC Error if the R/W register parity is even and 9-track or 7-track-odd-parity is specified or vice-versa for 7-track.

Data Gating - Seven-Track, Three Bytes - Write

In seven-track, three-bytes-per-word format, the byte generator is stepped through bytes A, B, C, and D. Byte B gates data to the R/W register for parity checking only. During byte A, D, and D times, data is gated as in the two-byte write operation except for the differences indicated in the following circuit objectives. The circuits described are on MDM GB40182 and the timing chart is on MDM GB70125. Figure 7-23 shows the format of the data gating for seven-track three-byte, write operation. Figure 7-24 shows the timing of the seven-track, three-byte, write operation.

Load Data Register with P-C Data Word. Same as two-byte format.

Gate Byte A to the R/W Register. Circuits, similar to those that gate byte A in two-byte format, gate data register positions P and 0 through 7 into the R/W register in three-byte format. Bits P, 0, and 1 will be reset and a new parity bit generated before the output is gated to the tape unit.

Parity Check R/W Register (Byte A). Same as two-byte format.

Reset R/W Register Positions P, 0, and 1. When the 200-nsec single-shot (R/W check gate) times out, positions P, 0, and 1 of the R/W register are reset. A parity bit, called C-bit, is generated based on the 6 remaining bits, 2-7.

Write Byte A. The seven-bits now assembled at the R/W register output are called C, B, A, 8, 4, 2, and 1. These data bits are gated to the tape unit by write-clock pulses 6 through 10.

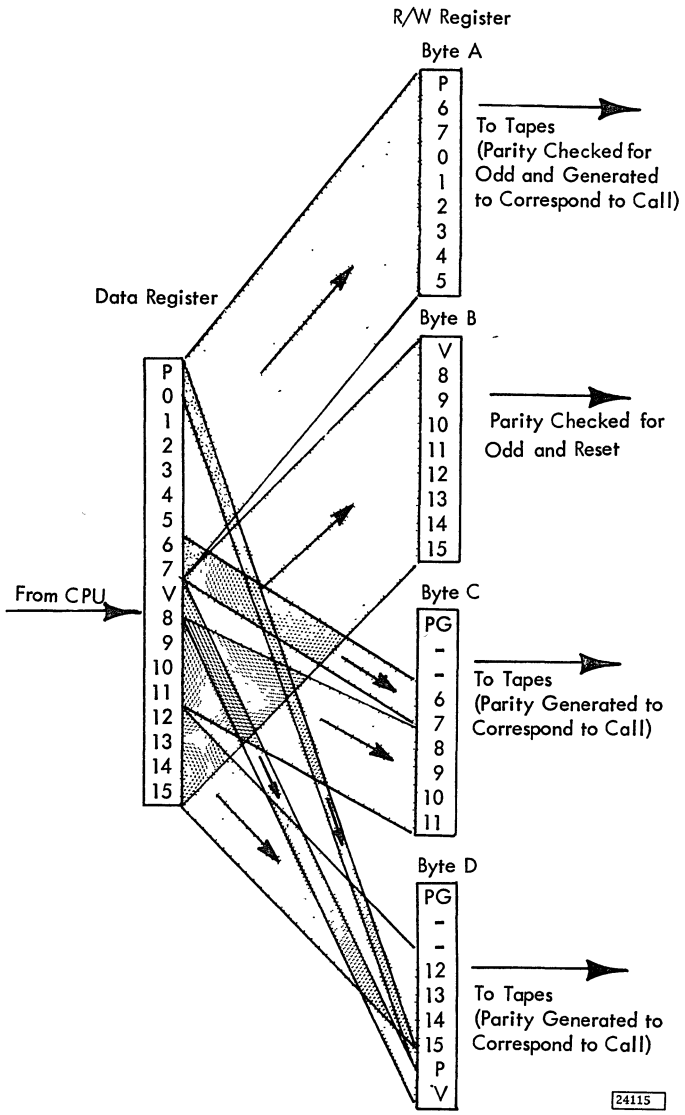


Figure 7-23. Write Data Gating, Seven-Track Three-Byte

Reset R/W Register. Same as two-byte format.

Step Byte Generator. Same as two-byte format.

Gate Byte B to the R/W Register. The same circuits that gate byte B in two-byte format gate data-register positions V and 8 through 15 into the R/W register. This data is parity checked but is not gated to the tape unit.

Parity Check R/W Register (Byte B). Same as two-byte format.

Reset R/W Register. The fall of the 200-nsec single-shot pulse that conditions the parity check (R/W check gate) during byte B time fires a 150-nsec single-shot that resets the R/W register.

Step Byte Generator. The 150-nsec single-shot that reset the R/W register also steps the byte generator. BT0 is turned off and the 3-bytes-per-word latch conditions BT1 so that it is turned on. This establishes the byte-C condition.

Gate Byte C to R/W Register. When the 150-nsec single-shot (reset R/W register) times out, a 300-nsec single-shot fires. The output pulse of this single-shot conditions a line that gates data-register positions 6 through 11 (not V) to R/W-register positions 2 through 7.

Write Byte C. Byte C is not parity checked in the R/W register because all of the data-register bits have been checked during byte-A and -B. A parity bit (C-bit) is generated according to the six bits in the R/W register and these seven bits, C, B, A, 8, 4, 2, and 1 are gated to the tape unit.

Reset R/W Register. At write clock (WC)-14 time, R/W strobe fires a 150-nsec single-shot to reset the R/W register. This reset is the same for two-byte format at byte-A time.

Step Byte Generator: The 150-nsec pulse (reset R/W register) turns on BT0 and BT1 remains on. This establishes the byte-D condition.

Gate Byte D to R/W Register: The timing-out of the 150-nsec single-shot (reset R/W register) fires a 300-nsec single-shot (R/W gate). This pulse conditions a line that gates data register positions 12 through 15 to R/W register positions 2 through 5 and data register positions P and V to R/W register positions 6 and 7.

Initiate a Cycle Steal Request: During byte-D time, the 300-nsec single-shot pulse (R/W gate) turns on the data cycle steal request (CSR) flip-latch. If the word count is not zero, the P-C places another data word on the out bus when it can next service the magnetic-tape cycle-steal priority.

Write Byte D. Same as byte C.

Reset R/W Register. Same as byte C.

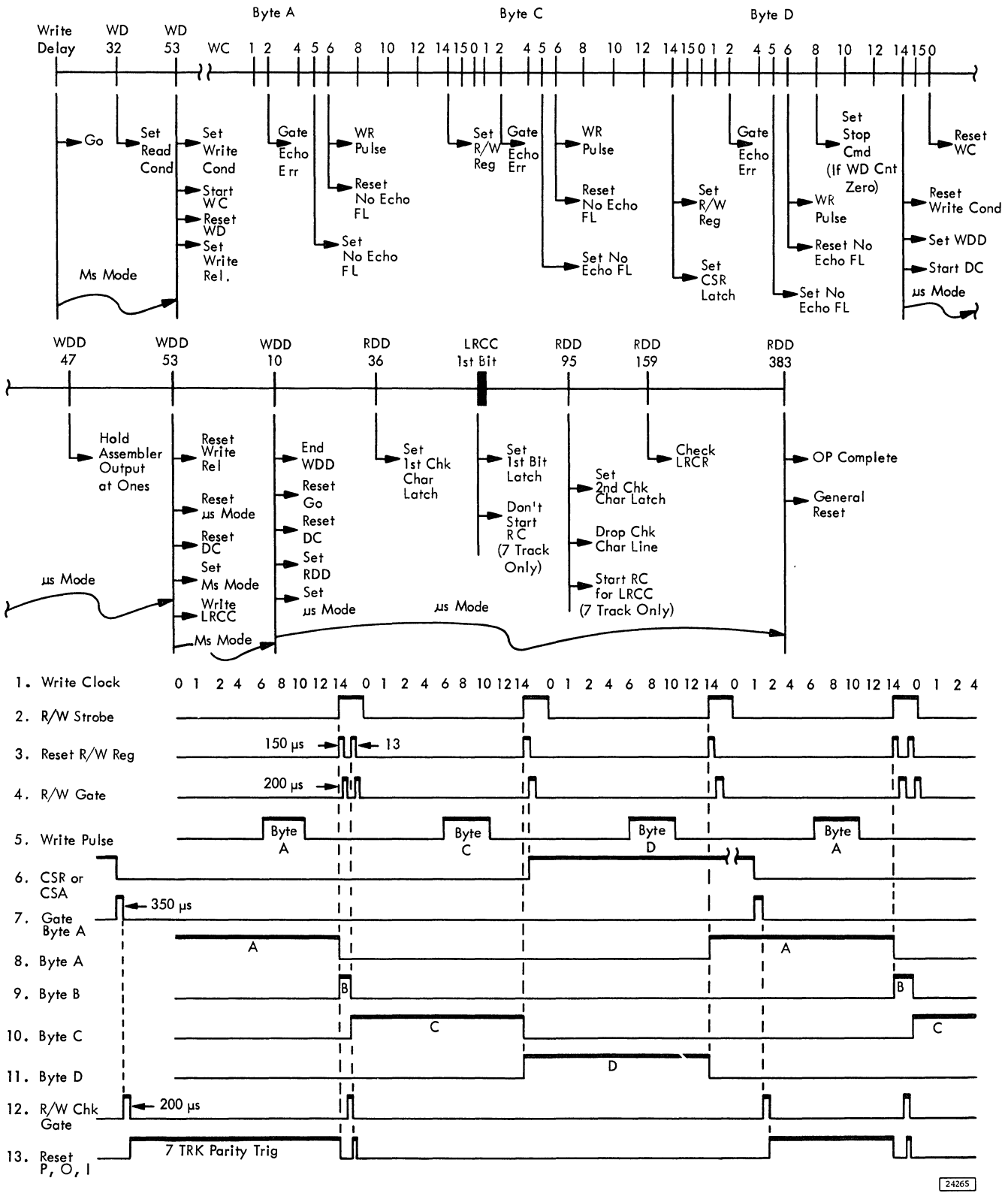


Figure 7-24. Timing: Write Data Gating, Seven Track Three Bytes

End of Data Table

- If the scan control latches so specify, and end-of-table (EOT) interrupt is activated when the last data word is transferred.
- If chaining is specified by the scan control latches, transfer of data to the next data table is started without program control.

If end-of-table-interrupt-remember latch is on, word-count-equal-zero and cycle-steal-acknowledge cause an interrupt request. Bit three of the device status word will indicate end of table when the sense-interrupt-level command is executed.

If the chain-remember latch is on, word-count-equal-zero sends three cycle steal requests to the P-C. The word that is placed on the out bus by the cycle steal is the word that follows the last data word in the data table and is the address of the first word in the next data table. Both cycle-steal-control triggers 0 and 1, when on, cause this address to be loaded into the specified channel address register.

The next cycle-steal-cycle places the first word of the new table on the out bus. This first word contains its own address. The cycle-steal-control-0 and -1 lines are activated to condition the channel address register (CAR) check circuits. If the address on the out bus does not compare equally with the contents of the specified CAR, a CAR check is indicated. The CAR check logic is shown on MDM CC30101.

The next word in the new data table contains the word count and scan-control bits. If this is the last data table to be chained, bit position zero contains a zero so that the chain-remember latch is not turned on. Bit position one contains a one to turn on, or a zero to turn off, the end-of-table-interrupt-remember latch.

Cyclic Redundancy Check Character

An additional error checking and correcting feature is employed for nine-track operation only. As each character is gated into the R/W register, the R/W register outputs condition the cyclic-redundancy-check-register (CRCR) inputs. The bits are gated into the CRCR in a pattern that creates a special check character. At the end of the record, all positions except 2 and 4 are complemented and the resulting cyclic redundancy check character (CRCC) is written on tape four character-spaces after the last data character and four character-spaces before the longitudinal redundancy check character (LRCC). The longitudinal-redundancy-check register (LRCR) considers the CRCC as a normal character when generating the LRCC. (See Error Correction, this section.)

CRCC Parity: The parity of the CRCC depends upon the configuration of the record. If the character-count flip-flop is off (even count), the CRCC parity should be odd. CRCC parity error is indicated by write-high-clip VRC (tape data error).

LRCC Parity: In nine track operation, the LRCC parity is always odd. In seven-track operation, LRCC parity depends upon the parity call and the character count as follows:

Even parity call – always even parity LRCC
Odd parity call
even character count – even parity LRCC
odd character count – odd parity LRCC

LRCC parity error is indicated by write-high-clip VRC (tape data error).

End Write Operation

- When the word count reaches zero, if chain-remember flip-latch is off and end-of-table-interrupt-remember flip-latch is on, request interrupt and turn on the stop-command flip-latch.
- Stop-command turns off the write-condition flip-latch at WC 14 time.
- Continue to read tape characters under control of read disconnect delay (RDD) as in read operation.
- If 9-track, gate CRCC, LRCC, and echo error, write CRCC and LRCC, all under control of write disconnect delay (WDD).
- If 7-track, write LRCC and gate echo error.
- Turn off the go flip-latch at one of the following times:
  1. If 7-track, model 3 – WDD10.
  2. If 9-track, model 3 – WDD403.
  3. If 7-or 9-track and not model 3 – RDD36.
- End of operation at RDD383.

TURNAROUND

- The turnaround flip-latch is turned on by read or write op if backward-memory-status (from the tape unit) is on, or by backspace if backward-memory-status is off.
- Delays the start of a read delay, write delay, or backward delay under millisecond control to allow time to reverse the direction of tape motion.

After initial selection is complete, the designated operation is begun by activating the operation line

such as read-op or write-op. Any tape operation requires conditioning of a beginning delay such as read-delay or write-delay. Before any tape operation can begin, the designated delay circuit must be conditioned by not-turnaround.

Turnaround means the tape unit just completed an operation moving tape in one direction and the operation just beginning designates that tape be moved in the opposite direction. Because the tape unit is largely mechanical, it requires some time to reverse its mechanical functions, such as the reel drives. The amount of turnaround delay varies with the tape unit model.

Backward Memory Status

The key line in the tape control unit that determines whether a turnaround delay is necessary is the backward-memory-status line brought up by backward status from the tape unit. If the tape-unit backward-trigger is on, indicating the preceeding operation moved tape backward, backward-memory-status is active in the tape control unit.

Any command that brings up read-op, designating forward tape movement, will set the turnaround flip-latch if backward-memory-status is active. Backspace turns on the turnaround flip-latch if backward-memory-status is not active.

Turnaround degates normal delay circuits and gates millisecond mode to the delay counter which advances to begin the delay sequence.

Erase Tape Forward

If the tape unit is in write status (not read status from tape unit) and backward-op is designated, the go flip-latch is turned on at delay-counter-3 time. Write-status indicates the last operation wrote a record, wrote a tape mark (TM), or erased tape. In the case of the record or tape mark, the erased area after the last check character is short because a new record was not written and a full, erased inter-record gap does not exist. During a subsequent read operation, old record information could be read during read-disconnect-delay (RDD) time and cause improper positioning of tape.

The condition just described is prevented by simply erasing tape forward for a few milliseconds to lengthen the "clean" area after the last written record or tape mark.

Tape Movement. With the go flip-latch on, go is sent to the tape unit and the prolays begin moving tape with the erase head energized. After the necessary tape movement, the delay-counter output resets the go flip-latch.

Tape Unit Status Lines

When the delay counter advances to 96, delay-96-turnaround (D 96 TA) sets the tape unit to the status designated by the op line. One of the following occurs:

1. Read-op gates set-read-status to the tape unit, to reset the R/W trigger and bring up read-status. Set-read also resets the tape-unit backward trigger to drop backward-memory-status to the tape control unit.
2. Write-op gates set-write-status to the tape unit to turn on the R/W trigger and activate write-status. Set-write also resets the tape unit backward trigger to drop backward-memory-status to the tape control unit.
3. Backspace, gated by D-96-turnaround or rewind, sets the backward flip-latch in the tape control unit. This flip-latch, when on, sends backward to the tape unit, to set the backward flip-latch which:

   a. Resets the R/W trigger to bring up read-status.
   b. Sends backward-memory-status back to the tape control unit.

End Turnaround

After D 96 the delay counter advances to D 160 TA to complete the turnaround-delay sequence by generating delay-counter-reset, which:

1. Resets the delay counter.
2. Resets the turnaround flip-latch to drop the delay-counter drive (ms mode).

Not-turnaround now conditions the delay circuit designated by the command and the new operation proceeds.

ERROR CORRECTION

- Error correction technique employs a modified cyclic code in conjunction with character parity to correct error bursts of unlimited length in any one of the nine tracks.
- Employed only on nine-track tape units.
- Errors involving more than one track within the same record are detected but not corrected.
- Error correction is performed in the tape control unit.

- As a result of error correction, the tape record contains a cyclic redundancy check character (CRCC).
- During a correction read, characters are corrected at the output of the high-clip skew register.
- The correction is checked by computing a new CRCC from the corrected data.
- The description of error correction for write and read operations is on MDM GB 401 22.
- The I/O operation diagram for cyclic redundancy check and error pattern register is on MDM GB 401 81.

Error correction is designed to correct almost any pattern of erroneous bits as long as they are in the same track within a record.

Error correction is based on the assumption that the record was written correctly, and that defects occurred after writing. No attempt is made to correct bits on the tape. Only the information sent to the data channel is corrected.

Cyclic Redundancy Check

To determine which track contains errors, two check characters are written at the end of the record (instead of only one as in former tape systems). The added check character is called a cyclic redundancy check (CRC) character; it is written after the data, but before the usual longitudinal redundancy check (LRC) character. The circuit that generates the CRC character is based on a complex equation that reduces the mathematical probability of an undetected error almost to zero. The mathematical formula used is involved and is of no use in troubleshooting.

The CRC character aids in error detection, but its primary function is determining which track contains the error. When a record is read, a new CRC character is computed and compared with the CRC character on the tape. If the record contains an error, the erroneous CRC value is used to determine the track in error.

Error Pattern

The CRC character by itself does not contain enough information to find which track contains the error. The error pattern register (EPR) supplies the missing information. During reading the EPR keeps a record of the R/W register redundancy errors in the form of an error pattern. If there are no errors, the EPR remains blank.

At the end of an error record, the error pattern (saved in the high-clip skew register) is compared with the CRCR. The error track is located by counting the number of shifts needed to reach a "match pattern." If all nine tracks have been tried unsuccessfully, shifting and comparing stop because no track in error can be found. Failure to find the track in error could be caused by read errors in more than one track or electronic error in the circuits.

Write Operation

Data in the R/W register is shifted into the CRCR once for each character written on tape. During each shift, bits are shifted and exclusively ORed into the next lower position, P to 0, 0 to 1 and etc. Bit-7 shifts to bit-P. No carries exist - just shifts. A bit-7 forces an additional input to bit positions 2, 3, 4 and 5. This means three inputs to these bit positions.

The CRCR bits are written on tape four characters after normal data and four characters before the LRC character. CRCR bits 2 and 4 are written on tape in true form at WDD 51-54 and gated to the write bus during WDD47-78 time. CRCR bits P, 0, 1, 3, 5, 6, and 7 are written at the same time, but in complement form.

The LRC character includes the CRC character. The error pattern register (EPR) is not used during write.

Read Operation

Data is transferred to the CRCR during a read operation just as during a write operation. High-clip VRC errors condition the EPR bit-7 to accept a bit on the next shift pulse. While reading data, the only input to the EPR is to bit 7. During the next character shift pulse, EPR-7, when on, forces additional inputs to EPR positions 2, 3, 4 and 5 just as in the CRCR. The tape-diagnostic-error flip-latch is also turned on by high-clip VRC error.

After all data is read, the CRCR character on tape is shifted into the CRC register. The CRC character from tape is in complement form except for bits 2 and 4. The CRCR now has all bits on except bits 2 and 4. This is "match pattern." If match pattern does not exist, the tape-data-error flip-latch is turned on.

Track in Error

The track in error is located as the tape is stopping, if match pattern was not obtained. The EPR character is gated to the high-clip skew register and the CRC character is gated to the comparing circuits at the output of the high-clip skew register. The CRCR is now shifted until all-data-zero indicates an equal

comparison between the CRC character and the EPR character (which remained in the high-clip skew register). The R/W register contains no bits because no read-gate is available at this time.

The EPR is used to count the number of shifts. This will indicate the track in error. The EPR is reset with bit-P on after its character is transferred to the skew register. Each shift (both CRCR and EPR) advances the bit to the next higher bit position. (P to 0, etc.) After all shifts, the EPR is not reset until a new record is read, or until this record is read with a read-with-correction operation.

Correction

When the P-C executes the sense-DSW instruction to check for errors, a one in bit position 6 of the DSW indicates a tape data error. The program should then branch to a backspace operation. After backspacing has been accomplished, a read-with-correction operation (bit-14 in the control word) causes corrected data to be transferred to the R/W register as follows:

1. EPR has not been reset; it therefore indicates the track in error.
2. High-clip-skew data is VRC checked. Any error is assumed to be in only one track, but any number of bits may be picked up or dropped in the error track. The VRC indicates which character is in error.
3. If no bits exist in the skew register for the error track and if there is a skew-register-VRC error, the selected output of the skew register sets a bit in the R/W register. If there is a bit in the skew register error track, it is prevented from reaching the R/W register when a VRC error exists.

Lost Character: If no bits exist in any one character, this character is defined as a lost character. This feature compensates for dropped single-bit characters if the character is not the first or last character of a tape record.

Detection of a lost character is accomplished by checking for RC-0 between RDD 19 and RDD 36. This condition indicates that a character is lost because the character spacing is too short for a check character and too long for normal character spacing.

When a lost character is detected, the following things are done to keep the data being transferred in the proper core storage word and to update the check circuits.

1. The byte generator is advanced.
2. The character-count flip-flop is complemented.
3. CRCR and EPR are shifted.
4. Tape data error is indicated.
5. I/O monitor line, echo-error-or-lost-character, is activated.
6. R-W strobe is generated.

The remainder of the operation is the same as for a normal character. The R-W register is blank because the high skew register is not gated out until RC-7.

The CRCR is effective during this read operation and indicates a tape data error in the normal manner. The EPR is not used because it contains the error track information.

If more than one track is in error (EPR 6 and 7 on), the read-correct flip-latch is reset during the read-delay time to change this operation to an ordinary read operation. This cancels the effect of bit 14 in the control word.

Error Correction Example

The example in Figures 7-25 through 7-28 shows the operation of the CRCR and EPR during write, read, and read-with-correction operations.

These four figures show each logical operation of the registers separately for easy instructional purposes. Figures 7-29 and 7-30 show the registers as they actually appear during a similar operation.

Figure 7-20 shows the shift pattern and the character by character generation of the CRC character as a five character data record is written on tape. Figure 7-12 is a simplified diagram of the CRCR. Note that after the last data character (character 5) is written, the CRCR is shifted one more time. The R/W register contains all zeros at this time. The resulting final CRCR character is written on tape following the last data character.

During the read operation for the same data characters, a new CRC character is generated in the CRCR. In the example in Figure 7-26, three read errors occur: (1) a bit is picked up in track four while reading character 3; (2) a bit is dropped in track four while reading character 5; (3) a bit is dropped in track four while reading the CRC character. These read errors result in a final CRCR character that is different from the one on tape.

During this same read operation, the EPR (Figure 7-13) is shifted for each data character and for the CRC character, as shown in Figure 7-27.

Because the CRC character generated during the read operation did not compare equally with the tape CRC character, the EPR is used to locate the error track. The ERP character is transferred to the skew register and is compared with the CRCR output. The CRCR is

Five Character Data Record	Bit	Char. 1				Char. 2				Char. 3				Char. 4				Char. 5				Reset			
	P	1				0				0				0				0				0			
	0	1				0				0				0				1				0			
	1	0				1				0				0				0				0			
	2	0				0				1				1				1				0			
	3	0				1				0				1				1				0			
	4	0				0				1				1				1				0			
	5	0				1				0				1				1				0			
Shift and Load Pattern	6	1				1				0				1				1				0			
	7	0				1				1				0				0				0			

CRCR Position	CRCR Pos. 7	CRCR Shifted	R-W Reg.	CRCR	R-W Reg. Ch. 1	CRCR Ch. 1	∀ Pos. 7	Shift CRCR	R-W Reg. Ch. 2	CRCR Ch. 2	∀ Pos. 7	Shift CRCR	R-W Reg. Ch. 3	CRCR Ch. 3	∀ Pos. 7	Shift CRCR	R-W Reg. Ch. 4	CRCR Ch. 4	∀ Pos. 7	Shift CRCR	R-W Reg. Ch. 5	CRCR Ch. 5	∀ Pos. 7	Shift CRCR	R-W Reg = 0	Final CRCR	CRCR on Tape
P	7∀P			0	1	1		0	0	0		0	0	0		1	0	1		0	0	0		1	0	1	0
0	P∀0			0	1	1		1	0	1		0	0	0		0	0	0		1	1	0		0	0	0	1
1	0∀1			0	0	0		1	1	0		1	1	0		0	0	0		0	0	0		0	0	0	1
2	7∀1∀2			0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	1
3	7∀2∀3			0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	1	0	0	1
4	7∀3∀4			0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0	1	1	1	0	0	1	1
5	7∀4∀5			0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1
6	5∀6			0	1	1		0	1	1		1	1	0		0	1	1		1	1	0		0	0	0	1
7	6∀7			0	0	0		1	1	0		1	0	1		0	0	0		1	0	1		0	0	0	1

Note: The exclusive OR (∀) of Pos. 7, shift, and load of CRCR are simultaneous and interacting; they are shown separately for ease of understanding.

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Figure 7-25. Generation of CRC Character During Write

Five Character Tape Record	Bit	Char. 1				Char. 2				Char. 3				Char. 4				Char. 5				Tape CRC Char.		
	P	1				0				0				0				0				0		
	0	1				0				0				0				1				1		
	1	0				1				0				0				0				1		
	2	0				0				1				1				1				1		
	3	0				1				0				1				1				1		
	4	0				0				1				1				1				1		
	5	0				1				0				1				1				1		
Shift and Load Pattern	6	1				1				0				1				1				1		
	7	0				1				1				0				0				1		

CRCR Position	CRCR Pos. 7	CRCR Shifted	R-W Reg. (Tape Char.)	CRCR	Tape Ch. 1	CRCR Ch. 1	∀ Pos. 7	Shift CRCR	Tape Ch. 2	CRCR Ch. 2	∀ Pos. 7	Shift CRCR	Tape Ch. 3	CRCR Ch. 3	∀ Pos. 7	Shift CRCR	Tape Ch. 4	CRCR Ch. 4	∀ Pos. 7	Shift CRCR	Tape Ch. 5	CRCR Ch. 5	∀ Pos. 7	Shift CRCR	Tape CRCC	Final CRCR	Compare CRCR
P	7∀P			0	1	1		0	0	0		0	0	0		1	0	1		0	0	0		1	0	1	0
0	P∀0			0	1	1		1	0	1		0	0	0		0	0	0		1	1	0		0	1	1	0
1	0∀1			0	0	0		1	1	0		1	1	0		0	0	0		0	0	0		0	1	1	0
2	7∀1∀2			0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	0	0
3	7∀2∀3			0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	1	1	1	0
4	7∀3∀4			0	0	0	0	0	0	0	0	1	[1]	0	1	1	1	1	0	0	[0]	0	1	0	[0]	1	1
5	7∀4∀5			0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	1
6	5∀6			0	1	1		0	1	1		1	1	0		0	1	1		0	1	1		0	1	1	0
7	6∀7			0	0	0		1	1	0		1	0	1		0	0	0		1	0	1		1	1	0	1

Note: The exclusive OR(∀) of Pos. 7, shift, and load of CRCR are simultaneous and interacting; they are shown separately for ease of understanding.

[1] Picked-up bit while reading. [0] Dropped bit while reading. 0 Result of error.

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Figure 7-26. Generation of CRC Character During Read

Shift Pattern	EPR	Shift Ch. 1	Shift Ch. 2	Shift Ch. 3	Shift Ch. 4	Shift Ch. 5	Shift CRC
7 → P	0	0	0	0	1	0	1
P → 0	0	0	0	0	0	1	0
0 → 1	0	0	0	0	0	0	1
7 ∀ 1 → 2	0	0	0	0	1	0	1
7 ∀ 2 → 3	0	0	0	0	1	1	1
7 ∀ 3 → 4	0	0	0	0	1	1	0
7 ∀ 4 → 5	0	0	0	0	1	1	0
5 → 6	0	0	0	0	0	1	1
VRC ∀ 6 → 7	0	0	0	1	0	1	0

VRC

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Figure 7-27. EPR During Read

Shift Pattern	Compare CRC	Shift Ch. 1	Shift Ch. 2	Shift Ch. 3
7 → P	0	1	0	1
P → 0	0	0	1	0
0 → 1	0	0	0	1
7 ∀ 1 → 2	0	1	0	1
7 ∀ 2 → 3	0	1	1	1
7 ∀ 3 → 4	1	1	1	0
7 ∀ 4 → 5	1	0	1	0
5 → 6	0	1	0	1
6 → 7	1	0	1	0

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Figure 7-28. CRCR Shifting for Error Track Detection

CRCR Pos.	CHAR 1	CHAR 2	CHAR 3	CHAR 4	CHAR 5	CRCC	Shift & Compare	Shift & Compare	Shift & Compare
P	1	0	0	1	0	1	0	1	0
0	1	1	0	0	0	1	1	0	1
1	0	0	0	0	0	1	1	1	0
2	0	0	0	0	1	0	1	0	1
3	0	1	1	0	0	1	0	0	0
4	0	0	0	1	0	1	1	1	0
5	0	1	0	0	0	0	1	0	1
6	1	1	0	1	1	1	0	1	0
7	0	0	1	0	1	0	1	0	1

Drop Drop Pick Up

Hi Clip VRC

Not "Match Pattern" Compare to High Skew Register. Look for "All Data Zero"

A. CRCR Operation with Read Errors in Track 4

EPR Pos.	CHAR 1	CHAR 2	CHAR 3	CHAR 4	CHAR 5	CRCC	EPR to Skew Reg.	Set "p" Trig	Shift	Shift	Shift	Track in Error
P	0	0	0	1	0	1	0	1				7
0	0	0	0	0	1	0	1		1			6
1	0	0	0	0	0	1	0			1		5
2	0	0	0	1	0	1	1				1	4
3	0	0	0	1	1	1	0					3
4	0	0	0	1	1	0	0					2
5	0	0	0	1	1	0	1					1
6	0	0	0	0	1	1	0					0
7	0	0	1	0	1	0	1					P

Hi Clip VRC

Exclusive "OR" with CRCR to find "All Data Zero"

B. EPR Operation with Read Errors in Track 4

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Figure 7-29. Error Correction Example

shifted, as shown in Figure 7-28, until its output compares with the EPR output. In the example, after three shifts (four compares) are made, the EPR character (in the skew register) and the CRC character are equal.

During this error-track-location operation, the EPR counts the number of shifts (not shown in the example) and thereby indicates the error track. The error track in this example is track four.

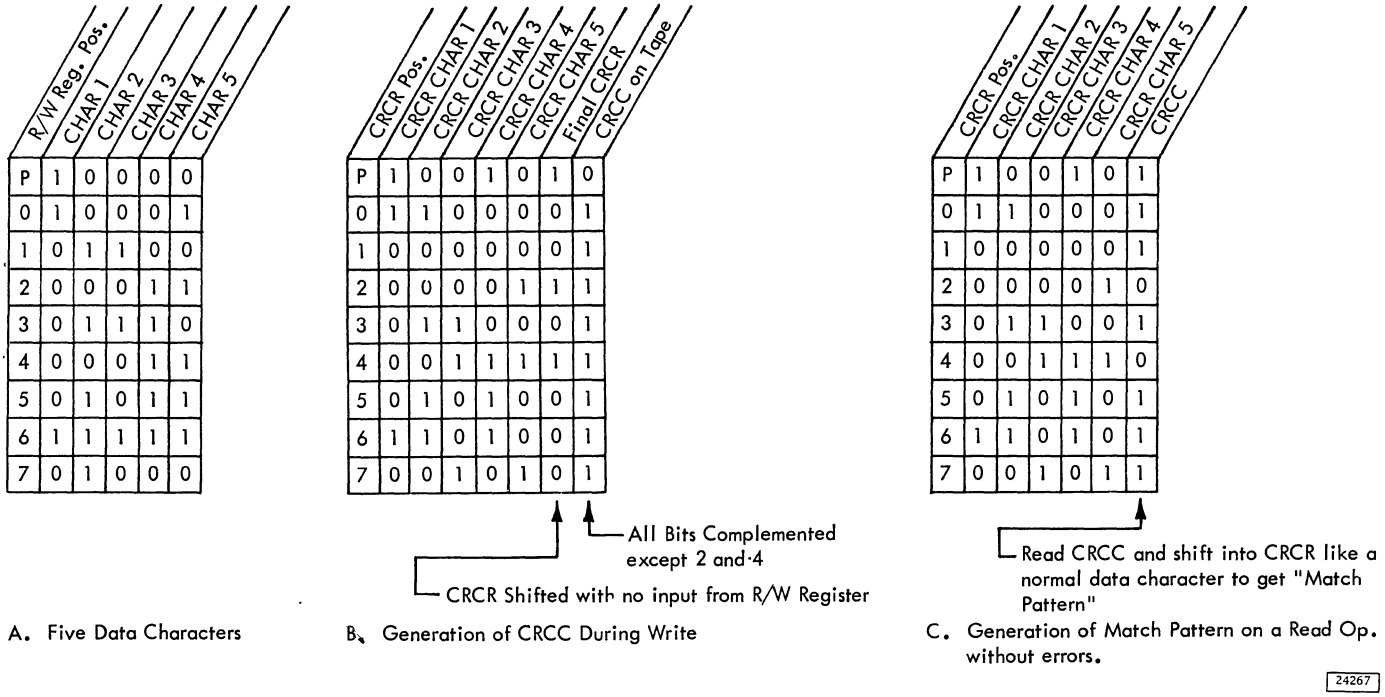


Figure 7-30. CRCR Operation With No Errors

CONTROL OPERATIONS

- The tape control unit can cause the tape unit to perform any of the following five control functions:

  Backspace
  Erase
  Rewind
  Rewind-unload
  Write tape mark

- The objectives of backspace, erase, rewind, and rewind-unload are on MDM GB 401 42.

- The I/O operation diagram for backspace, erase, rewind, and rewind-unload and some of the pertinent tape unit circuits are on MDM GB 401 41.

- The circuits that implement the write-tape-mark function are on the Write I/O-operation-diagram, MDM GB 401 31.

Control Word Cycle

The control word cycle (E-1 cycle) is similar for all control commands. If the area bits of the control word are those assigned to tape control (01110), the function and modifier bits are decoded. The control function (100) enables the turning-on of the specified control function flip-latch. The tape unit is selected according to bit-10. Delay-commands is turned on to allow time for all the control information to be received. Any one of the control function flip-flops activates the busy line.

Backspace

- Specified by IOCC control word bit positions 13, 14, and 15 being 011.

- Check for turnaround condition (backward memory off).

- Start tape motion in backward direction.

- Condition circuits to read tape characters.

- Stop tape at the inter-record gap.

- The timing chart for backspace is on MDM GB 701 41.

Tape normally stops with the read head positioned in the inter-record gap. The backspace operation moves the tape backward one record to the preceding inter-record gap. To accomplish this, backward, go, and the read circuits are activated. When the first character of the record (last one reading back-

ward) is reached, tape motion is stopped with tape positioned with the read head in the preceding inter-record gap.

Circuit Description

The backspace flip-latch is turned on by an 011 decode of bits 13, 14, and 15 at T6 time. If the backward-memory line is not active, the backward flip-latch is off and is not turned on until D 96 TA is activated. The tape control unit backward line turns on the tape unit backward flip-latch and resets the tape unit read/write flip-latch to the read condition.

If the tape unit is in the write status at the beginning of the operation (turnaround condition), the go flip-latch is turned on for a few milliseconds, moving the tape forward in write status (Timing Chart, MDM GB 701 41). This procedure erases the tape farther into the gap to ensure a clean gap following the check characters. When tape unit status changes from write to read, a noise splash is recorded on tape under the write heads. By moving the tape ahead, the weak noise splash is positioned farther from the last good record.

If the previous operation was a backspace, the go flip-latch is turned on by the backward-delay line which is activated by first-character. Other turn-on times and the turn-off times of the go flip-latch are determined by the tape unit model (see Timing Chart).

Backward-delay (backward read delay) is deactivated at one of three different times depending upon the tape unit model (see Timing Chart). The fall of backward-delay turns on the read-condition flip-latch.

The read clock is turned on by the first bit of each character. Read clock (RC)-7 turns on read-disconnect-delay (RDD) to run the delay counter under millisecond control. RC-4 of the next character turns off RDD. After the first data character of the record (last one reading backward) is read, RDD 383 is eventually reached. RDD 383 turns on the operation-complete-interrupt flip-latch to signal the program and to reset the backspace circuits.

Erase

- Specified by I/O control command (IOCC) control word bit positions 13, 14, and 15 = 010.
- Check for turnaround condition (backward-memory-status on).
- Condition write circuits.
- Start tape motion in forward direction.
- Stop tape after approximately 3.5 inches are erased.

The erase flip-latch, a function-register circuit, activates the write op line. If turnaround is not active, write-op activates write-delay to run the delay counter under millisecond control. Write-delay turns on the go flip-latch.

Not-backward-memory-status or D96 TA and write-op activates the set-write-status line to turn on the read-write flip-latch in the tape unit.

WD 320 turns off the first-character flip-latch to turn on RDD. RDD 36 turns on the first-check-character flip-latch which turns off the go flip-latch to stop tape motion. RDD 383 turns on the operation-complete-interrupt flip-latch to request a program interrupt and reset the erase circuits.

Rewind or Rewind-Unload

- Rewind operation is specified by IOCC control word bit positions 13, 14, and 15 = 100.
- Rewind-unload is specified by IOCC control word modifier bits 13, 14, and 15 = 000.
- Rewind or rewind-unload signal is sent to the tape unit.
- Tape control unit circuits are reset.
- Tape is moved backward to the load-point for either rewind or rewind-unload; it is also unloaded for the rewind-unload operation.
- The timing chart for rewind or rewind-unload is on MDM GB 701 42.

The rewind or rewind-unload flip-latch (function register circuits) activates a line that causes the tape unit to perform the specified function. Rewind also turns on the backward flip-latch which turns on the tape unit backward flip-latch.

The busy line, activated by rewind or rewind-unload, and a line from the tape unit indicating that it is rewinding, activate RDD 383. RDD 383 resets the rewind or rewind-unload circuits in the tape control unit and turns on the operation-complete-interrupt flip-latch to request a program interrupt.

Write Tape Mark

- Specified by IOCC control word bit positions 13, 14, and 15 = 001.
- Check for turnaround condition (backward-memory-status on).
- Start tape motion in forward direction.
- Condition write and read circuits.
- Write the tape mark in seven-track or nine-track code.
- Stop tape motion.
- Read-check the tape mark written on tape.

The write-tape-mark flip-latch activates the write op line.

If the backward-memory-status line is active from the tape unit, write-op turns on the turnaround flip-latch. Turnaround prevents write-op from activating write-delay and set-write-status until the delay counter reaches 96. The delay counter is activated in millisecond mode by the turnaround flip-latch. When D96 is reached, write-op activates the set-write-status line to set the read/write flip-latch in the tape unit; this deactivates backward-memory-status.

With backward-memory-status not active, write op conditions write-delay. Write-delay turns on the go flip-latch to start tape motion. At a delay time determined by the tape unit model, write-delay turns on the write-condition and read-condition flip-latches. Write-condition starts the write clock.

The nine-track tape-mark consists of one-bits in bit positions, 3, 6, and 7. The seven-track tape-mark consists of one-bits in bit positions 4, 5, 6, and 7 (BCD code 8, 4, 2, 1).

The write-tape-mark flip-latch output line activates R/W assembler bits 6 and 7. Write-tape-mark ANDs with nine-track (not 7-track) to activate R/W assembler bit 3. Write-tape-mark ANDs with seven-track to activate R/W assembler bits 4 and 5. The R/W assembler lines go directly to the write bus. The tape mark character is written on tape at write-clock-6 through -10 time.

At write-clock-8 time, write-tape-mark turns on the stop-command flip-latch, which, at write-clock 14 time, turns off the write-condition flip-latch. As write condition goes off, it activates write-disconnect-delay to write the LRC character and turn off the write-trigger-release flip-latch.

Read condition allows the first-bit of the tape mark, as it is read from tape, to start the read clock. The tape mark is checked for parity and is loaded into the longitudinal redundancy check register (LRCR). Read-clock-7 turns on read-disconnect-delay (RDD) after write-delay and write-release have been deactivated. RDD-36 turns on the first-check-character flip-latch which turns off the go flip-latch. The LRC character is read and loaded into the LRCR. At RDD 159 time, the LRCR is checked; if any bit position flip-flop is on, the tape-data-error is turned on.

RDD 383 turns on the operation-complete-interrupt flip-latch to request a program interrupt and to reset the write-tape-mark circuits.

SENSE INTERRUPT LEVEL STATUS WORD (ILSW)

- Gates bits (assigned by customer) onto the in bus to indicate to the program which, if any, of the three interrupt condition indicators in the tape control unit are active.

XIO Control Cycle (E-1)

- If interrupt level and function decode as specified, the ILSW-remember flip-latch is turned on.

If function 011 is decoded from out-bus bits 5-7 and the interrupt level assigned to the tape control unit is decoded from bits 11-15, the ILSW-enable line is activated at T6. If out-bus bit 15 is not active, indicating a sense ILSW function code, ILSW enable turns on the ILSW-remember flip-latch.

XIO Data Cycle (E-2)

- Gate the assigned ILSW bit 0-15 to the in bus for operation-complete-interrupt, end-of-table-interrupt, or command-reject if any of these are active.

SENSE DEVICE

- If IOCC control word bit 11 = 0, the tape control unit gates any of the previously described indicators and conditions, that are active, onto the in bus.
- If bit 11 = 0 and the tape control unit is not busy, bit 10 selects the tape unit. Bit 10 = 0 selects tape unit 0, bit 10 = 1 selects tape unit 1.
- If bit 11 = 1, the word count is gated onto the in bus.
- The DSW or word count (defined in Data Format description) is loaded into the processor-controller accumulator for program analysis.
- If IOCC control word bit 15 = 1 and bit 11 = 0, this command turns off the following indicators:

  Chain stop
  Storage protect violation stop

Data bus out or P-C parity error
Data overrun
Wrong length record
Tape indicator or mark
(If turned on by a tape mark only)
Command reject
End of Table
Operation complete
CE Diagnostic Indicator
Tape Data Error

- If out-bus bit 12 = 1, the word count is set to zero, causing an operation stop.

XIO Control Word Cycle (E-1)

- If out bus bits 0-4 decode as 01110, turn on the DSW-remember flip-latch.
- If out bus bit 11 = 1, turn on the sense-word-counter flip-latch.
- If out-bus bit 12 = 1, turn on the word-count-zero-remember flip-latch.
- If out bus bit 15 = 1, turn on the reset-indicator flip-latch.

XIO Data Cycle (E-2)

- If the sense-word-count flip-latch is not on, the DSW-remember flip-latch gates the specified indicator bits to the in bus.
- If both the sense-word-count flip-latch and the DSW-remember flip-latch are on, gate the contents of the word counter to the in bus.
- The reset-indicator flip-latch turns off the previously listed indicators at T5.

The 2310 Disk Storage machine characteristics are located in the Field Engineering Theory-Maintenance Manual, IBM 2310 Disk Storage Models A1, A2, A3, C1, C2, C3. All other DP I/O attachment features are located in the 1801 or 1802 Processor-Controller.

The Processor-Controller's machine characteristics are located in the Field Engineering Theory of Operation Manual, IBM 1800 Data Acquisition and Control System Processor-Controller. (See FE Bibliography - 1800 System, Form Y26-0560.)

APPENDIX B SPECIAL CIRCUITS

All circuits that may be considered special circuits are described in the Functional Units section for each feature.

The Area, Function, and Modifier codes listed below are required for 1800 I/O operations (x indicates an unused bit position):

	AREA	FUN	MODIFIER
Console Data Entry Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 0 x x x x x
Read - switch data to core.	0 0 0 0 0	0 1 0	0 1 0 x x x x x
Console Sense, Program Switches and CE Switches			
Sense Device - switch data to A-reg.	0 0 0 0 0	1 1 1	0 1 1 x x x x x
Read - switch data to core.	0 0 0 0 0	0 1 0	0 1 1 x x x x x
Console Interrupt			
Sense Device - console DSW to A-reg; indicators not reset	0 0 0 0 0	1 1 1	1 1 0 x x x x 0
- console DSW to A-reg; reset indicators	0 0 0 0 0	1 1 1	1 1 0 x x x x 1
Operations Monitor			
Control - timer not reset	0 0 0 0 0	1 0 0	1 1 1 x x x x 0
- reset timer	0 0 0 0 0	1 0 0	1 1 1 x x x x 1
Interval Timers			
Control - timers started or stopped according to bits 0-2 of IOCC Address word	0 0 0 0 0	1 0 0	0 0 1 x x x x x
Interrupt Mask Register			
Control - mask or unmask interrupt levels 0-13, depending on IOCC Address word bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 0 x x x x 0
- mask or unmask interrupt levels 14-23, depending on IOCC Address word bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 0 x x x x 1
Program Interrupt			
Control - turn on interrupt levels 0-13, depending on IOCC Address word bit positions 0-13.	0 0 0 0 0	1 0 0	1 0 1 x x x x 0
- turn on interrupt levels 14-23, depending on IOCC Address word bit positions 0-9.	0 0 0 0 0	1 0 0	1 0 1 x x x x 1
ILSW			
Sense	0 0 0 0 0	0 1 1	0 0 0 0 0 0 0 0

NOTE: For Process Interrupt see Digital Input.

	AREA	FUN	MODIFIER
1053 Printer:			
First four 1053's:			
Write - individual 1053 specified by IOCC modifier bits 11-14.	0 0 0 0 1	0 0 1	x x x y y y y x
Sense Device - 1816/1053 DSWs to A-reg. Individual 1053 specified by IOCC bits 11-14; bit 15 determines reset of indicators.	0 0 0 0 1	1 1 1	x x x y y y y y
Second four 1053's: Area code is 01111.			
1816 Printer - Keyboard			
Read - single character to core storage	0 0 0 0 1	0 1 0	x x x x 0 0 1 0
Sense Device - 1816/1053 DSWs to Accumulator. Individual 1053 specified by IOCC bits 11-14; bit 15 determines reset of indicators.	0 0 0 0 1	1 1 1	x x x y y y y R
Control - places keyboard in Ready status.	0 0 0 0 1	1 0 0	x x x x 0 0 1 0
1442 Card Read Punch			
First 1442:			
Initialize Read - card columns to core storage. Where P is Packed Mode.	0 0 0 1 0	1 1 0	x x x x x x x P
Initialize Write - core storage to card columns.	0 0 0 1 0	1 0 1	x x x x x x x x
Control - IOCC bits 8 and 14 specify function. Where Y is Stacker Select F is Feed Cycle	0 0 0 1 0	1 0 0	y x x x x x Fx
Sense Device - DSW to Accumulator; bit 15 determines reset of indicators.	0 0 0 1 0	1 1 1	x x x x x x x R
Second 1442: Area code is 10001.			
1054 and 1055 Paper Tape			
Read - one character from tape buffer to core storage.	0 0 0 1 1	0 1 0	x x x x x x x x
Write - core storage to tape.	0 0 0 1 1	0 0 1	x x x x x x x x
Control - One character from tape to tape buffer.	0 0 0 1 1	1 0 0	x x x 1 x x x x
Sense Device - DSW to Accumulator; bit 15 determines reset of indicator.	0 0 0 1 1	1 1 1	x x x x x x x R

	AREA	FUN	MODIFIER
2310 Disk Storage Drive			
First 2310:			
Initialize Read-into-memory: yyy specify disk sector.	0 0 1 0 0	1 1 0	0 x x x x y y y
Initialize Read-check	0 0 1 0 0	1 1 0	1 x x x x y y y
Initialize Write	0 0 1 0 0	1 0 1	x x x x x y y y
Control - seek as specified by IOCC address and modifier bit 13.	0 0 1 0 0	1 0 0	x x x x x x S x
Sense Device - DSW to A-reg; bit 15 determines reset of indicators.	0 0 1 0 0	1 1 1	x x x x x x x R
Second and Third 2310's require Area codes of 01000 and 01001, respectively.			
1627 Plotter			
Write - core storage to plotter.	0 0 1 0 1	0 0 1	x x x x x x x x
Sense Device - DSW to A-reg; bit 15 determines reset of indicators	0 0 1 0 1	1 1 1	x x x x x x x R
1443 Printer			
Initialize Write - bit 15 is used for space suppress.	0 0 1 1 0	1 0 1	x x x x x x x y
Control - carriage control	0 0 1 1 0	1 0 0	x x x x x x x x
Sense Device - DSW to A-reg; bit 15 determines reset of indicators.	0 0 1 1 0	1 1 1	x x x x x x x R
Analog Input			
Direct Program Control:			
Write - AI point to ADC; Address word of IOCC specifies the core-storage location of the multiplexer address; where E is External Sync. L is 8-bit resolution H is 14-bit resolution.	0 1 0 1 0	0 0 1	E x x L H x x x
Read - ADC to core storage; Address word of IOCC is core-storage location specifying where the ADC reading will be stored; where S is Sequential Program mode.	0 1 0 1 0	0 1 0	S x x x x x x x

	AREA	FUN	MODIFIER
Sense Device - DSW to A-reg; where C specifies Comparator or AI status word. R bit resets indicators.	0 1 0 1 0	1 1 1	C x x x x x x R
Control (Blast Instruction)	0 1 0 1 0	1 0 0	x x x x x x x x
Data Channel Control:			
Initialize Read - ADC readings to core storage; where T specifies a two DC operation.	0 1 0 1 0	1 1 0	E x T L H x x x
Initialize Write - Address from core storage to multiplexer.	0 1 0 1 0	1 0 1	x x x x x x x x

The AI Expander Area code is 10000.

Digital Input

Direct Program Control:			
Read - DI or PI group to core storage; Bits 9-15 are DI addresses 64_{10} through 127_{10} or PI addresses 2_{10} through 25_{10}.	0 1 0 1 1	0 1 0	x A A A A A A A
Sense Device - DSW, DI, or PISW to A-register; Bits 11-15 are DSW addresses 0 0 0 0 0 or 0 0 0 0 1 (reset indicators), PISW addresses 2_{10} through 25_{10} or DI addresses 64_{10} through 127_{10}.	0 1 0 1 1	1 1 1	x B B B B B B B
Control (Blast Instruction)	0 1 0 1 1	1 0 0	x x 1 x x x x x
Data Channel Control:			
Initialize Read - where bits 8-10 specify the read mode.	0 1 0 1 1	1 1 0	R R R x x x x x

Digital and Analog Output

Direct Program Control:			
Write - core storage to DAO device; where bits 9-15 are device addresses 0_{10} through 127_{10}.	0 1 1 0 0	0 0 1	x A A A A A A A
Control - where bit 9 initiates simultaneous transfer from buffer registers, bit 8 initiates timing pulse for Pulse Output, and bit 10 resets all DAO controls (Blast Instruction).	0 1 1 0 0	1 0 0	P B R x x x x x
Sense Device - DSW to A-reg; bit 15 determines reset of the indicators.	0 1 1 0 0	1 1 1	x x x x x x x R
Data Channel Control:			
Initialize Write - core storage to DAO registers. Bits 8-10 specify write mode.	0 1 1 0 0	1 0 1	R R R x x x x x

	AREA	FUN	MODIFIER
System/360 Adapter			
Initialize Write	0 1 1 0 1	1 0 1	x x x x x x x x
Initialize Read	0 1 1 0 1	1 1 0	x x x x x x x x
Sense Status	0 1 1 0 1	1 1 1	0 x x x x x x x
Sense Word Count	0 1 1 0 1	1 1 1	1 x x x x x x x
Control (Reset)	0 1 1 0 1	1 0 0	x x x x x x x x
2401 or 2402 Magnetic Tape			
Initialize Read - where bits 10-15 specify:	0 1 1 1 0	1 1 0	x x Y Y Y Y Y Y
10 Address Tape Unit 0 or 1	0 1 1 1 0	1 1 0	x x T Y Y Y Y Y
11,12 Bit density for 7-track (ignored for 9-track)			
Bits 11 and 12 equal 00 for 800 BPI	0 1 1 1 0	1 1 0	x x Y 0 0 Y Y Y
Bits 11 and 12 equal 01 for 200 BPI	0 1 1 1 0	1 1 0	x x Y 0 1 Y Y Y
Bits 11 and 12 equal 10 for 556 BPI	0 1 1 1 0	1 1 0	x x Y 1 0 Y Y Y
13 "Packed-format" for 7-track (ignored for 9-track)	0 1 1 1 0	1 1 0	x x Y Y Y F Y Y
14 Read-while-correcting (ignored for 7-track)	0 1 1 1 0	1 1 0	x x Y Y Y Y C Y
15 Even parity for 7-track (ignored for 9-track)	0 1 1 1 0	1 1 0	x x Y Y Y Y Y P
Initialize Write - where modifier bits specify:	0 1 1 1 0	1 0 1	x x Y Y Y Y X Y
10 Address Tape Unit 0 or 1	0 1 1 1 0	1 0 1	x x T Y Y Y X Y
11,12 Bit density for 7-track (ignored for 9-track)			
Bits 11 and 12 equal 00 for 800 BPI	0 1 1 1 0	1 0 1	x x Y 0 0 Y X Y
Bits 11 and 12 equal 01 for 200 BPI	0 1 1 1 0	1 0 1	x x Y 0 1 Y X Y
Bits 11 and 12 equal 10 for 556 BPI	0 1 1 1 0	1 0 1	x x Y 1 0 Y X Y
13 "Packed-format" for 7-track (ignored for 9-track)	0 1 1 1 0	1 0 1	x x Y Y Y F X Y
15 Even parity for 7-track (ignored for 9-track)	0 1 1 1 0	1 0 1	x x Y Y Y Y X P
Control - Bit 10 addresses the tape unit, bits 11-12 specify the bit density for 7-track (11-12 ignored for 9-track)			
Rewind and unload	0 1 1 1 0	1 0 0	x x T X X 0 0 0
Write Tape mark	0 1 1 1 0	1 0 0	x x T D D 0 0 1
Erase	0 1 1 1 0	1 0 0	x x T D D 0 1 0
Backspace	0 1 1 1 0	1 0 0	x x T 0 1 0 1 1
Rewind	0 1 1 1 0	1 0 0	x x T X X 1 0 0

	AREA	FUN	MODIFIER
Sense Device			
Select tape Unit "T" and Read DSW into A-register (1)	0 1 1 1 0	1 1 1	x x T 0 0 x x 0
Select tape unit "T", Read DSW into A-register, and reset indicators (2)	0 1 1 1 0	1 1 1	x x T 0 0 x x 1
Read Tape Channel word count into A-register (3)	0 1 1 1 0	1 1 1	x x x 1 0 x x x
Operation Stop (free tape channel) with bits T, Y, and R also performing functions 1, 2, and 3 above	0 1 1 1 0	1 1 1	x x T Y 1 x x R

Meaning of symbols in 2401/2402 IOCC modifiers above:

Symbol	Meaning
C	Read-while-correcting
D	Density
F	Packed Format
P	Even Parity
R	DSW Reset
T	Tape Unit
X	Not Used
Y	Variable

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	* Interrupt Request															
	Interval Timers	* Timer A	* Timer B	* Timer C													
	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Sense Switches	← Sense →				← Program →				← CE Sense →							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1 15**	1816 Printer-Keyboard	* Printer Service Response	* Keyboard Service Response	* Keyboard Request		Printer Busy	Printer Not Ready	Keyboard Not Ready	Storage Protect Violation	Keyboard Parity Error	Printer Parity Error			†CE Busy	†CE Not Ready		
	1053 Printer	* Printer Service Response				Printer Busy	Printer Not Ready				Printer Parity Error			†CE Busy	†CE Not Ready		
2 17**	1442 Card Read Punch			Error	Last Card	* Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					†CE Busy	†CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	* PT Reader Service Request	PT Punch Parity Error	* PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy		
4	2310 Disk Storage	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun		†CE Not Ready	†CE Busy		Sector Count High	Sector Count Low
5	1627 Plotter	* Service Response	Parity Error											†CE Busy	†CE Not Ready	Busy	Not Ready
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready
10 16**	Analog Input	* End of Table	* DPC SS Conv Complete	* DPC Rly Conv Complete	* Storage Protect Violation	* Parity Control Error	* Parity Data Error	* Overload	* Overlap Conflict	Cyc Steal, SS, AMAR Busy	DPC Relay Busy						Any Error
	Comparator	* High Out of Limit	* Low Out of Limit	* Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input	* Parity Error	* Storage Protect Violation	* DI Scan Complete	* Command Reject												DI Busy
	PISW	← Process Interrupt Points (Customer Assigned Groups) →															
12	Digital and Analog Output	* Parity Error	Pulse Output Timer	* D & A Out Scan Complete	* Command Reject	Data Channel Active											D/AO Busy
13	S/360 Adapter	* Command Reject	1800 Command Stored	* 360 Command Stored	* Halt	* Data Check	* Storage Protect Violation	* Transfer End	* End of Table	← 360 Command Byte →							
	Adapter Word Counter			← Word Count (1's Complement) →													
14	Tape Control Unit		Tape Unit 1 Select	* Command Reject	* End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	* Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
	TCU Word Counter	00 = True Count 11 = 1's Complement		← Word Count →													

* Interrupt Conditions

** Second Adapter Area Code

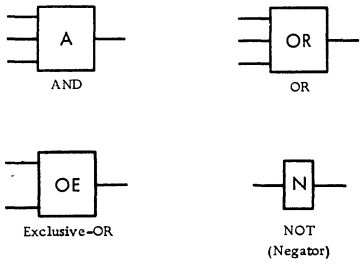
† Active Only in CE Mode

14092B

APPENDIX E MAINTENANCE DIAGRAM SYMBOLOGY (POSITIVE LOGIC)

In positive logic representation, signal levels are disregarded. The negator (N block symbol) is used to invert logic, not level. Passive elements (such as drivers and pulse shapers generally are not shown, since they contribute nothing to the logic.

LOGICAL ELEMENTS



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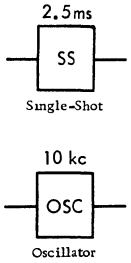
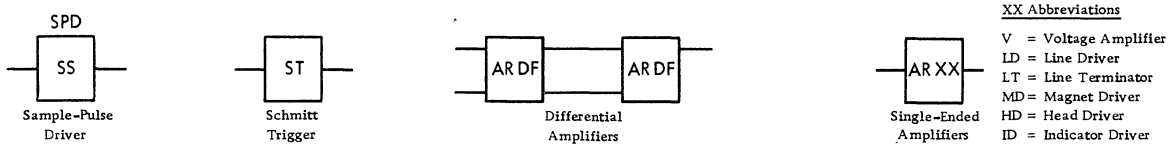
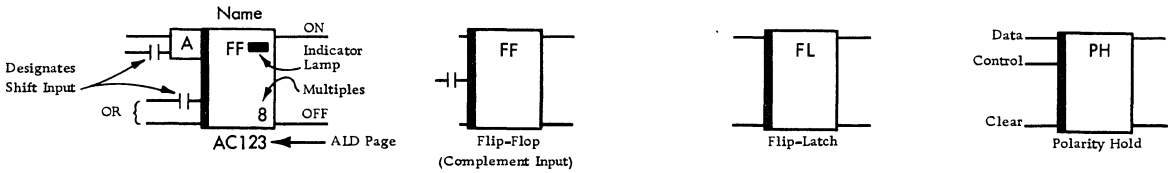


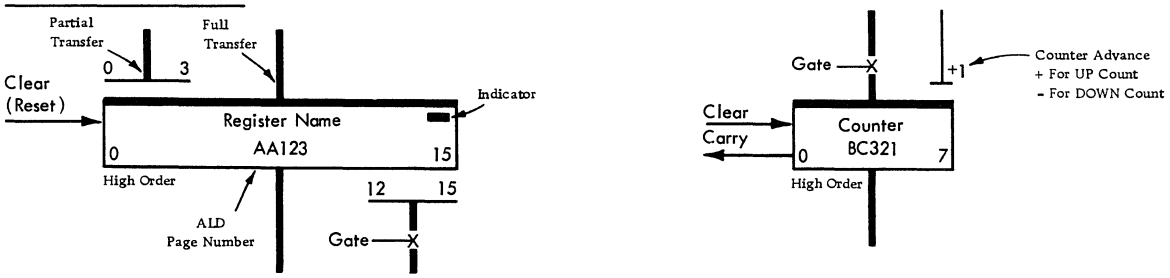
PASSIVE ELEMENTS



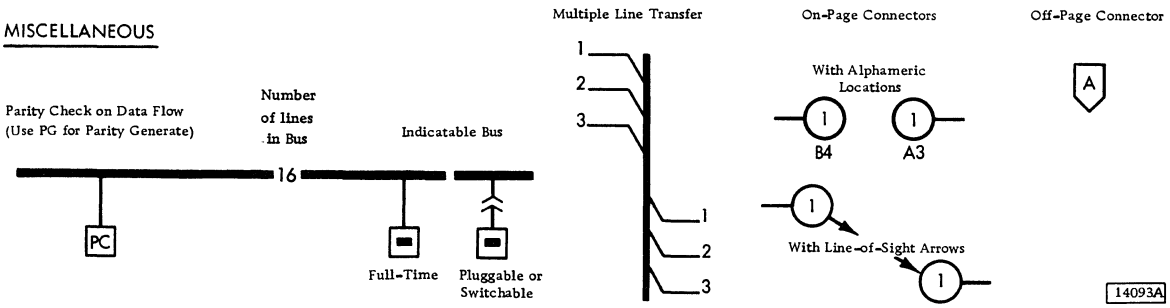
STORAGE ELEMENTS



REGISTERS AND COUNTERS



MISCELLANEOUS



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