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7631 File Control

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IBM Customer Engineering

Instruction-Maintenance

7631 File Control

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7631 File Control

Preface

This Customer Engineering Instruction-Maintenance Manual describes IBM 7631 File Control Model 3 operation with the IBM 1410, 7010, 7040-44, 7070-74, 7080, and 7090-94 Data Processing Systems. The manual contains seven parts:

1. "Introduction" shows the IBM 7631 File Control relationship to the IBM Data Processing Systems and the IBM 1301 Disk Storage. The magnetic disk recording, cylinder concept, data track, and format track information are also included.

2. "Operations" describes the five basic machine cycles, the prepare to verify, and the miscellaneous instruction sequences.

3. "Functional Units" presents the timing, register operation, parity circuit, format recognition, and compare circuit concepts.

4. "Interfaces" presents the 1410 I-O Interface and Standard Interface concepts.

5. "Operation Timing" presents the five basic machine cycles, the prepare to verify, and the miscellaneous instruction timings.

6. "7320 Drum Storage Adapter" presents the drum characteristics, functional units, and operation theory.

7. "Maintenance Information" contains the CE panel operating instructions, 1410 System status conditions, 7000 system error conditions, singleshot timing, flag operation, and power control sequence.

Programming information, power supply information, and 1301 Disk Storage Fundamentals are contained in the publications:

IBM 1301 Disk Storage with IBM 7000 Series Data Processing Systems, General Information Manual, Form D22-6576-3.

IBM 1301 Disk Storage with IBM 1410 and 7010 Systems, Systems Reference Library, Form A22-6670-2.

IBM 60-Cycle SMS Power Supply, Customer Engineering Manual of Instruction, Form 225-6478-1.

IBM 1301 Disk Storage, Customer Engineering Manual of Instruction, Form 227-5582-2.

IBM 1301 Disk Storage, Customer Engineering Maintenance Manual, Form 227-5581-4.

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This edition, Form 223-2766-1, is a relatively unchanged version of the preceding edition, Form 223-2766-0. There are no significant differences in content or terminology. Changes to text or illustrations are indicated by a bullet (●) in the table of contents or list of illustrations.

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Safety

All IBM Customer Engineers are thoroughly familiar with IBM safety procedures; however, here are some reminders of general safety practices:

1. Do not work alone on the machine when power is on.
2. Wear safety glasses.
3. Be sure a fire extinguisher of the CO_2 type recommended for electrical fires is located in the room.
4. Turn DC off to prevent shorting when replacing a fuse or removing and inspecting SMS cards.
5. Discharge capacitors before working on DC power supplies.
6. Remember that 208 volts is present in the machine with power off.

Introduction

- **7631 File Control controls data transfer between 1301 Disk Storage and 1410 and/or 7000 systems.**
- **7631 is available in five models.**
- **7631 controls up to five 1301's—10 modules.**

The IBM 7631 File Control unit is used to control data exchanged between the IBM 1301 Disk Storage and the IBM 1410, 7010, 7090-7094, 7080, 7070-7074, and 7040-7044 Systems (Figure 1). The 7631 File Control provides the data path, the registers, and the sequence controls necessary to exchange sense and to control data with the systems. Sense is used only for 7000 system operation. The 7631 also contains the registers necessary to position and select the 1301 read-write heads, the circuits to control magnetic reading and writing, and the timing flexibility to operate in six-bit or eight-bit mode.

The 1301 Disk Storage is available in two models:

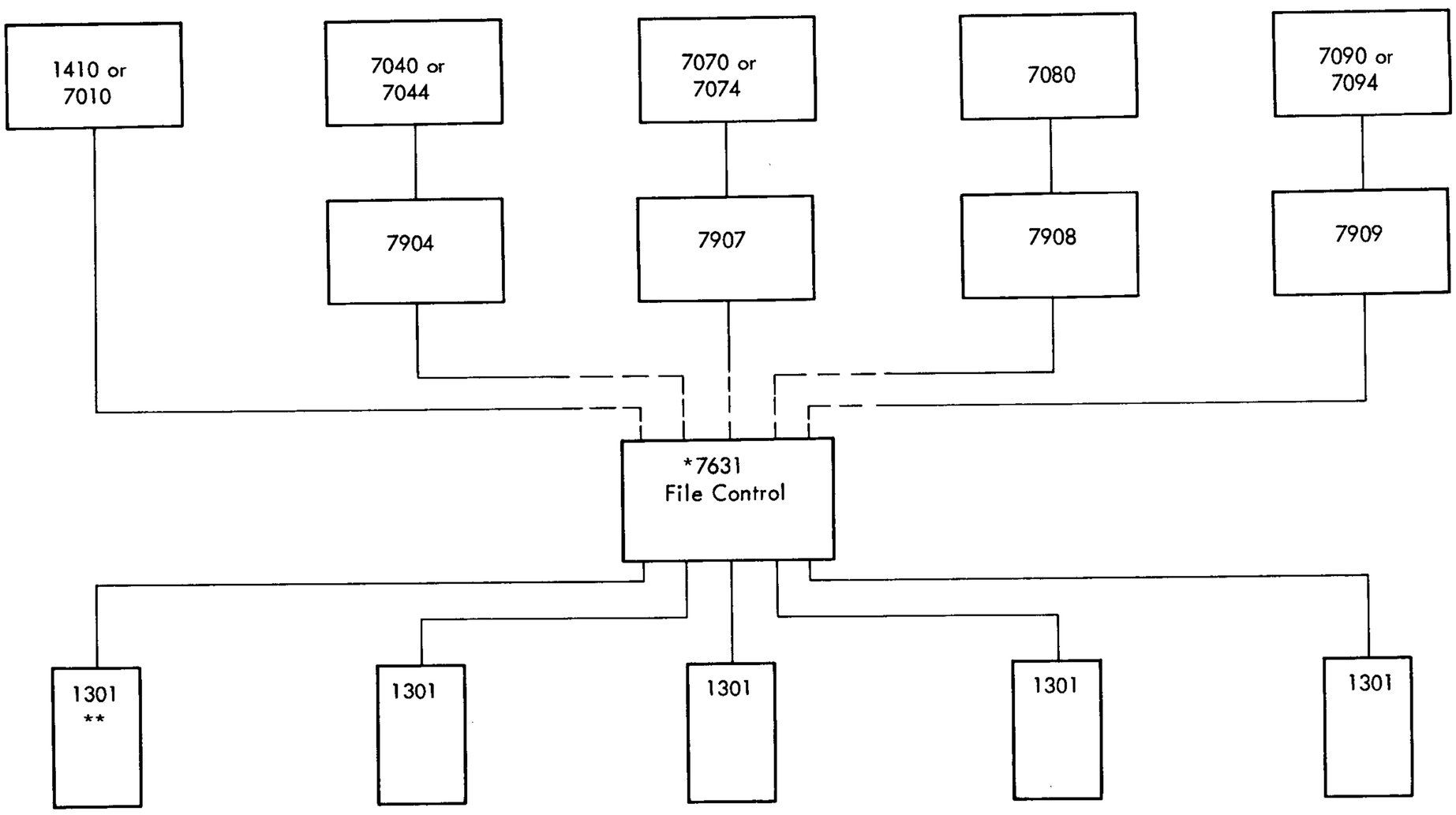
Model 1—single module, providing capacity for 28,000,000 six-bit mode (7080) characters or, using eight-bit mode, 43,300,000 digits.

Model 2—two modules, providing capacity for 56,000,000 six-bit mode (7080) characters or, using eight-bit mode, 86,600,000 digits.

7631 File Control is available in five models:

Model 1—for use with a 1410 system
Model 2—for use with a 7000 system
Model 3—for shared use with a 7000 system and a 1410 system
Model 4—for shared use with two 7000 systems
Model 5—for shared use with two 1410 systems

One 7631 controls up to five 1301 Disk Storage units; therefore, up to ten modules of disk storage and their access mechanisms can be controlled by one 7631. Each 1301 storage module contains 40 storage surfaces and



*Model 1 Connects to a 1410 System
2 Connects to a 7000 System
3 Connects to a 7000 System and a 1410 System
4 Connects to two 7000 Systems
5 Connects to two 1410 Systems

** 7631 Controls up to five 1301's

Figure 1. 7631 File Control Systems Relationships

one access mechanism to position the 40 read-write heads. Each storage disk surface contains 250 concentric data tracks, and since there are 40 storage surfaces, each module contains 10,000 data tracks. Data are read or written serially by bit in six-bit or eight-bit characters or bytes. The eight-bit mode permits the use of packed mode (packing two four-bit digits into one eight-bit character) on the 7070 and 7080 systems. Data characteristics of the 1301 Disk Storage are shown in Figure 2.

When the 1301 model 2 is used, a maximum of five disk storage units with a total of ten modules can be connected to one 7631 File Control. The modules are addressed 0 through 9 (Figure 3). For example, to select the upper module of 1301 number 3, it is necessary to specify access zero and module five.

When 1301 model 1's are used (a single module per file frame) the access unit is in the lower half of the 1301; the access units are the even-numbered units shown in Figure 3. For example, to select the access unit in 1301 model 1 number 3, you must specify 0 and module 4.

Operations Scheme

- **7631 designed to execute four commands.**
- **Control—set up type of file operation and specify file address where it will be done.**
- **Read—causes data flow from 1301 to system.**
- **Write—causes data flow from system to 1301.**
- **Sense (7000)—causes file control status data transfer to 7000 system.**

The 7631 can execute four operations: control, read, write, and sense. Sense is used only for 7000 system operation. All I-O instructions or commands issued cause the 7631 to execute one of the four operations. Each of

Characteristics *	Six-Bit Mode				Eight-Bit Mode					
					7070/4		7080		7040/4 7090/4	1410 7010
	7070/4	7080	7040/4 7090/4	1410 7010	Packed	Unpacked	Packed	Unpacked		
Maximum Characters per Track	2,780	2,800	2,796	2,800	4,310	2,150	4,330	2,165	2,160	2,165
Maximum Characters Per Cylinder	111,200	112,000	111,840	112,000	172,400	86,000	173,200	86,600	86,400	86,600
Maximum Characters Per File (2Modules)	55,600,000	56,000,000	55,920,000	56,000,000	86,200,000	43,000,000	86,600,000	43,300,000	43,200,000	43,300,000
Maximum Characters Per File Control (5-1301's)	278,000,000	280,000,000	279,600,000	280,000,000	430,000,000	215,000,000	433,000,000	216,500,000	216,000,000	216,500,000
Character Rate	90,100 Char/Sec				140,200 Digit/Sec	70,100 Char/Sec	140,200 Digit/Sec	70,100 Char/Sec	70,100 Char/Sec	70,100 Char/Sec

* Figures represent maximum utilization of space (each track written with a single record)

Figure 2. Data Characteristics of Disk Storage

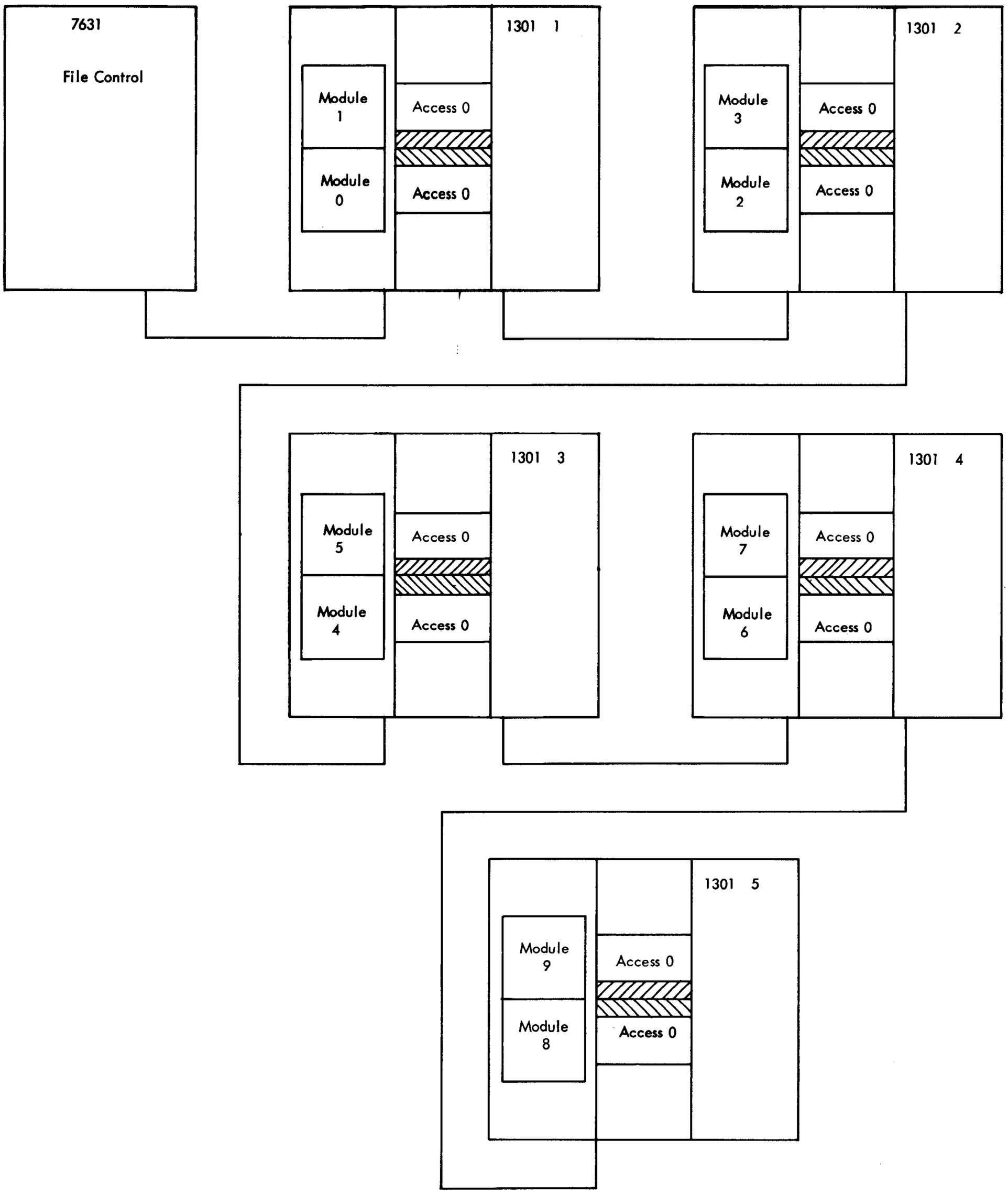


Figure 3. 1301 Addressing

the four operations causes the 7631 to operate in different sequence, and each different sequence can be divided into one or more machine cycles.

Control

The control operation allows the file control to read in and store control data used to specify the 1301, the track, and the type of operation. There are two types of instructions (orders): miscellaneous and prepare to verify. The miscellaneous orders are used to set the bit mode for 7000 Systems, position access mechanisms, set access mechanisms inoperative, set status indicators, prevent interrupts for 1410 Systems, and to release a shared file control. The prepare to verify orders are used to define the type of read or write operation and to specify the address to be verified. The prepare to verify order must be stored in the file control before starting a read or write operation (Figure 4).

Read

The read signal causes the file control to execute a read operation. During the read operation the file control uses the control word data (stored during the control cycle) to select the access, module, and read-write head. Then the file control reads and compares the disk address with its stored address; if the disk address and the stored address compare, the file control transfers the specified read data from the 1301 to the requesting system (Figure 4).

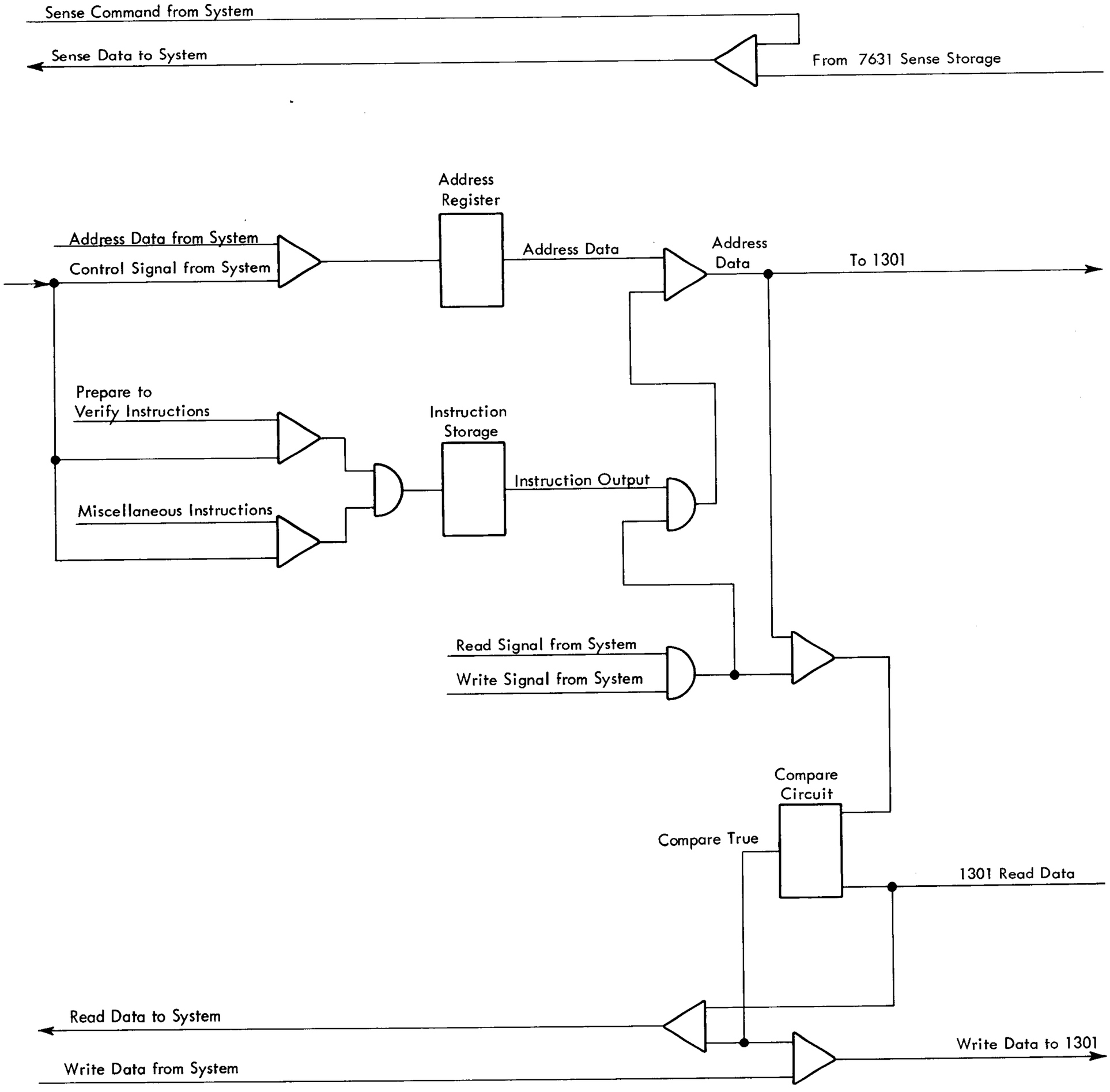


Figure 4. 7631 File Control Simplified Operations

Write

The write signal causes the file control to execute a write operation. During the write operation the file control uses the stored control word to select the access, module, and read-write head. Then, the file control reads and compares the disk address with its stored address. If the disk address and the stored address compare, the file control requests and writes data from the system on the specified 1301 track areas (Figure 4).

Sense (7000)

The sense command causes the file control to transmit status data to the requesting 7000 system to indicate attention conditions, errors, and unusual conditions (Figure 4).

Magnetic Disk Recording

- **Data is written serially by bit on 1301.**
- **6 or 8 bit mode configuration.**
- **Data tracks are program-addressable allowing random access.**
- **Format track allows convenient data track arrangement of data.**

The magnetic disk is a thin metal disk coated on both sides with magnetic recording material. Twenty-five disks are mounted on a vertical shaft slightly separated from each other to provide space for the movement of read-write heads. The shaft revolves, spinning the disks at a maximum of 1,790 revolutions per minute.

Data are stored as magnetized spots in concentric tracks on each disk surface (Figure 5). There are 250 customer tracks on each surface. The tracks are selected for reading and writing by positioning the read-write heads between the spinning disks. Data bits are written serially at a 1.6 μs-per-bit rate. A written character (byte) is preceded by a sync bit (bit S) generated by the file control. The sync bit enables the file control to separate disk characters in subsequent read operations. Each bit written on the disk has a fixed relationship to the data character bits of its particular system.

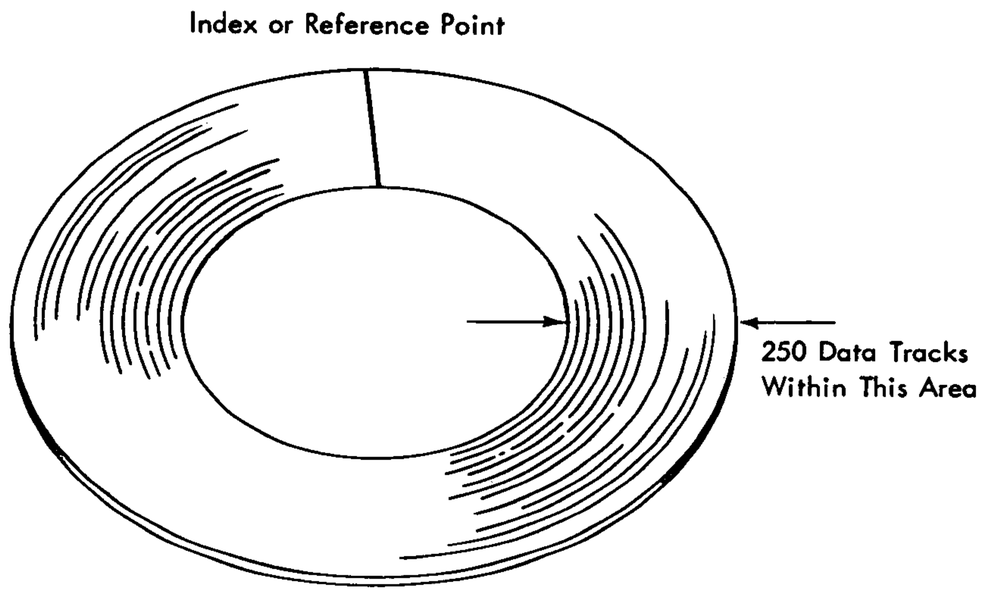


Figure 5. Magnetically Coated Disk

Nine bits (bit S (sync), bit 0, and bits one through seven) are used to write one eight-bit mode BCD character (Figure 6, line 1). The relative position of BCD bits to the disk data bits is shown on line 2. The eight-bit mode configuration of a BCD A is shown on line 3. The 1410 must use load mode to write word marks; the

Disk Data Bit Positions	S	0	1	2	3	4	5	6	7	Line 1
BCD Bit Positions (1410 Load Mode)		BI	WM	B	A	8	4	2	1	Line 2
BCD A in 8-Bit Mode	1	0	0	1	1	0	0	0	1	Line 3
7070/4 and 7080 Pack Mode Bit Pos		8	4	2	1	8	4	2	1	Line 4
Digits 5 and 3 in Pack Mode	1	0	1	0	1	0	0	1	1	Line 5

Figure 6. Disk Data Eight-Bit Mode

Disk Data Bit Positions	S	0	1	4	5	6	7	Line 1
BCD Bit Positions		B	A	8	4	2	1	Line 2
BCD A in 6-Bit Mode	1	1	1	0	0	0	1	Line 3
Digit 5 in 6-Bit Mode	1	0	0	0	1	0	1	Line 4

Figure 7. Disk Data Six-Bit Mode

word mark bit is recorded in the disk data bit 1 position. The 7070-7074 and 7080 systems can operate in packed mode so that the file control in eight-bit mode can record two non-zoned characters in the nine disk data bit recording positions (line 4). The eight-bit mode configuration of two non-zoned characters is shown on line 5.

Seven bits (bit S (sync), bit 0, bit 1 and bits 4 through 7) are used to write one six-bit mode BCD character (Figure 7, line 1). The file control circuits are designed to skip bit 2 and bit 3 time intervals in six-bit mode operation; therefore, character recording rate is increased over eight-bit mode unpacked recording, and the maximum characters per track are increased (Figure 2, "Maximum Characters Per Track" and "Character Rate"). The position of the BCD bits relative to the disk data bits is shown in Figure 7, line 2. The six-bit mode configuration of zoned and non-zoned characters is shown on lines 3 and 4.

The read-write heads are mounted on an access mechanism which has 24 arms, arranged like teeth on a comb, moving horizontally between the disks. No vertical motion is involved (Figure 8). Reading and writing are possible on both sides of a disk. Two read-write heads are mounted on each arm; one head services the bottom surface of the upper disk while the other head services the top surface of the lower disk.

The magnetic disk data surface can be used again and again. Each time new information is stored on a track, the previous record information is erased. The recorded data may be read as often as desired; data remain recorded in the tracks of a disk until written over.

Disk storage, like trays of cards or magnetic tape, provides external storage capacity to supplement computer core storage. Disk storage has a major advantage, however, in that all records contained in the 1301 are program-addressable, providing random access to any record or group of records (faster access to any record).

Although the total number of character positions of the track is fixed, the number of records and the number of characters per record can be arranged to suit the needs of a particular system. Addresses must be provided to identify the track and each record, and space must be provided in the form of gaps to separate address and record areas.

A format track provides a means of defining and monitoring the address, record, and gap areas for the data tracks. One format track monitors 40 associated data tracks, and can be changed to describe the data track format the user needs.

A disk storage module is a stack of 25 magnetic disks and an associated access mechanism. Forty surfaces of the 25 disks are used to store data. Of the other ten surfaces, six are used as alternate surfaces, one is a format surface, one is a clock surface (Figure 9) and the remaining two surfaces are not used. The data storage surfaces and the format surface each contain 250 concentric tracks that are accessible for reading and writing.

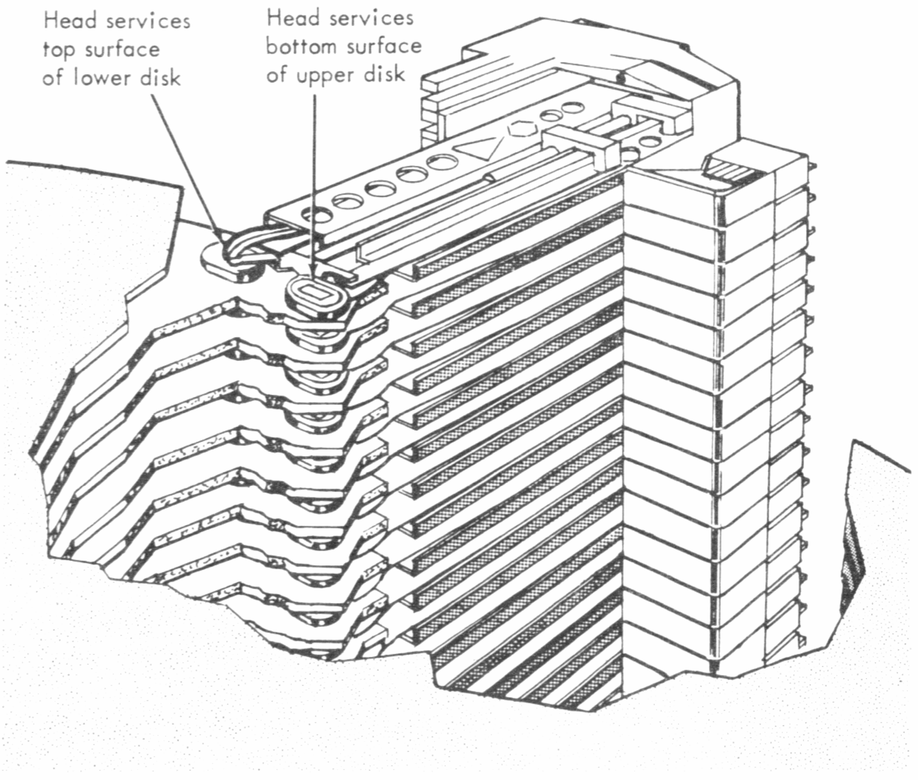


Figure 8. Read-Write Comb

DISK	SURFACE	MODULE 0	MODULE 1
24	40	Not Used	Not Used
	39		
23	38		
	37		
22	36		
	35		
21	34		
	33		
20	32		
	31		
10	30		
6-19	2-29	DATA SURFACES	
5	1		
4	0		
	1	Alternate	Alternate
3	2		
	3		
2	4		
	5		
1	6	Alternate	Alternate
	-	Format	Format
0	-	Spare	Spare
	-	Clock	Not Used

Figure 9. Disk Surfaces

Cylinder Concept

- **1301 data tracks are aligned one above the other.**
- **40 tracks for each access setting = one cylinder (plus format track and alternates).**
- **250 cylinders = 10,000 (plus CE) in one module.**
- **One module = 10,000 tracks × 2,800 characters/track = 28,000,000 characters.**
- **Two modules/file = 56,000,000 characters.**

Because the heads and disk tracks are mechanically aligned one above the other, the vertical alignment of the tracks can be described as a cylinder of tracks (Figure 10). When the access mechanism is placed in any one of the 250 cylinders, 40 tracks of data are available without any other access motion; only electronic head switching is necessary. For example, in one access mechanism setting as many as 112,000 characters (7080) are available.

The tracks are numbered sequentially from the bottom to the top of the cylinder (corresponding to the 40 heads, 00 to 39), starting at the outermost cylinder (000) to the innermost cylinder (249). Thus, with large storage areas for reference tables, the data can be conveniently stored in a cylinder of tracks or in a number of adjacent cylinders. This technique reduces access time to a minimum.

The cylinder arrangement of tracks also permits the optional feature, cylinder mode of operation, to read or write a cylinder (or part of a cylinder) of tracks in one operation.

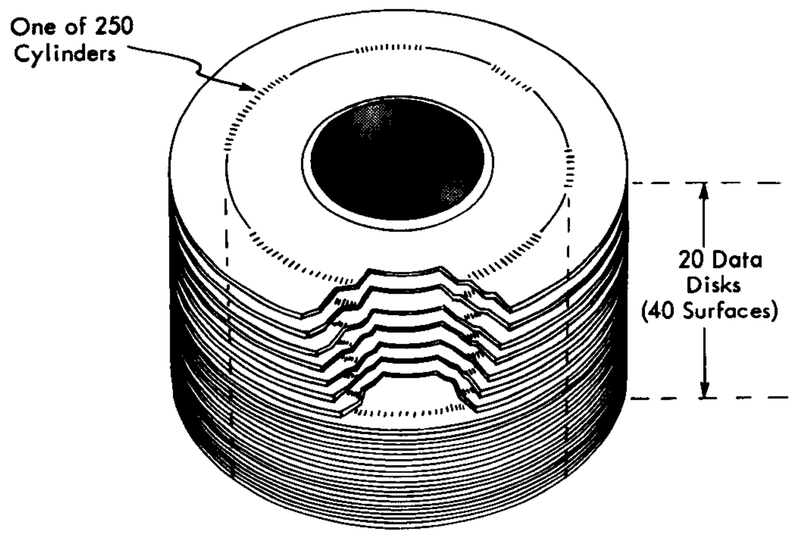


Figure 10. Cylinder Concept

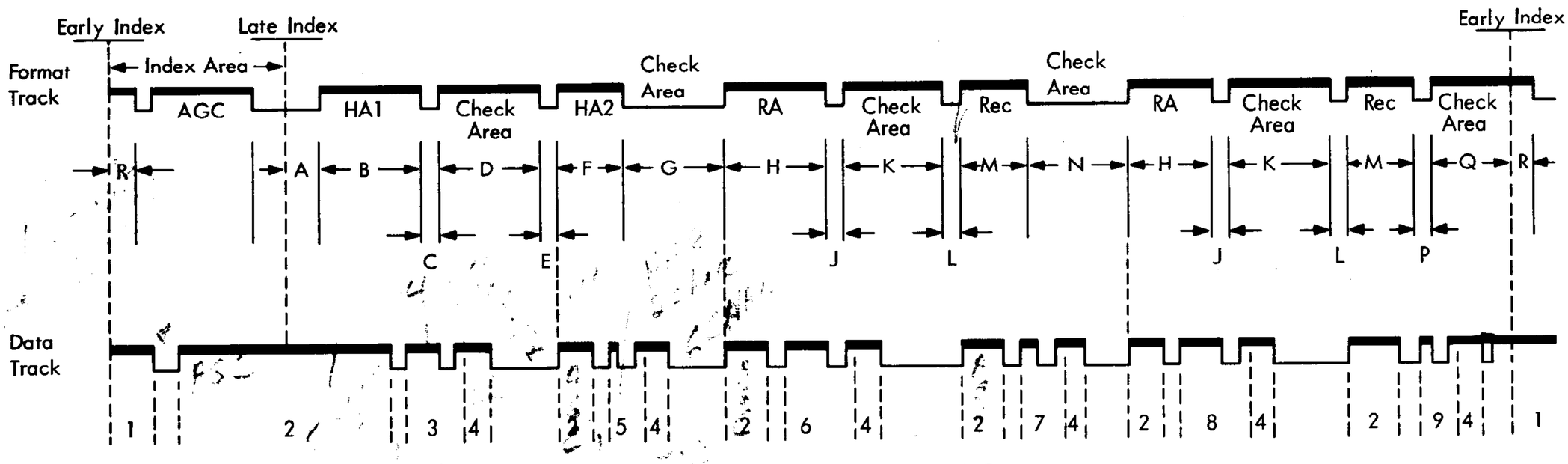
Data Tracks

- **Index timing defines beginning and end of track.**
- **Each track has distinct areas to record information.**
- **Each area consists of AGC, data and check characters.**
- **Each area is separated by gaps.**
- **The data track areas will always follow the sequence: HA1, HA2, RA, Rec, RA, Rec, etc.**

The basic fixed recording area of the 1301 is the data track. The physical make-up of the track limits it to a specific overall recording capacity. Although each track has equal overall recording capacity, this capacity depends on the number of records and number of characters per record, because track areas needed to separate and define recorded areas cannot be used for data recording (Figure 11).

Each data track has seven distinct areas:

1. Index area
2. Home address area
3. Record addresses
4. Records
5. AGC
6. Check character areas
7. Gaps



Format Track Chart

Format Areas	Characters	Bit Mode
A	3 absolute	8
B	9 abs	8
C	1 abs	8
D	10 abs	8
E	1 abs	8
F	6 minimum	6/8
G	12 abs	6/8
H	10 min	6/8
J	1 abs	6/8
K	10 abs	6/8
L	1 abs	6/8
M	6 min	6/8
N	12 abs	6/8
P	1 abs	6/8
Q	11 min	6/8
R	6 abs	6/8

Data Track Chart

Data Area	Name
1	Filler
2	AGC
3	Hal (home address one)
4	Check Characters
5	HA2 (home address two)
6	RA (record address)
7	Rec (record data)
8	RA (record address)
9	Rec (record data)

Figure 11. Format and Data Track

Index Area

The index point is the reference point of the track. Because the data track is circular, its beginning and end must be sensed. A magnetic slug is mounted on the outer edge of the format track disk for this purpose. Late and early index signals are generated as the slug rotates past two magnetic sensors. The magnetic sensors mounted through the array shield are physically displaced to create a 475-microsecond interval between the early and late index signals. Early index signals the end of a track and late index signals the beginning of a track to the 7631 (Figure 11, index area).

Home Address 1

This portion of the home address is the track number (Figure 11, area 3). HA1 consists of five numeric characters written by the customer engineer; it should not be written by the customer. The four high-order positions of HA1 contain a four-digit track number (0000-9999) that identifies the physical track location within the module. The low-order position (fifth character) is the track flag character. The flag character function is discussed in the section, "Verify Address Cycle." The flag character must be a blank or an eight to prevent a flag operation.

The last character of each address and record is separated from the preceding address or record characters by a one-character gap. This is written to provide greater format/data skew tolerance.

Tracks are numbered sequentially starting with the bottom track of the outermost cylinder, track number 0000, and continuing up through the cylinder to track number 0039. There are 40 data tracks in each cylinder. The track numbers continue with the lowest track of the adjacent cylinder, track 0040, up the cylinder to track number 0079. Continuing through each of the cylinders, the last track number, 9999, is the top track of the innermost cylinder; therefore, adjacent tracks on the same disk always differ by 40. This provides a formula to determine the track number for any track within any cylinder: given the head number and the cylinder number, the track number is the product of the cylinder number and 40 plus the head number. For example, for cylinder number 241 and head number 20 the track number is: $241 \times 40 = 9640 + 20 = 9660$. The cylinder number and head number can be determined by dividing the track number by 40: the quotient will

be the cylinder number, the remainder will be the head number. For example, if the track number 0590 ÷ 40 = 014 with a remainder of 30; the cylinder number is 014 and the head number is 30.

Home Address 2

The second portion of the home address (HA2) is called the home address identifier or random record area (Figure 11, area 5). This portion of the address further identifies the track to the using system. HA2 is written by the user and consists of two or more numeric, alphabetic, or special characters, depending upon the requirements of the using system. Two characters are required for HA2, and although only two characters are compared during address verification operations, additional characters may be used.

HA2 can be written to serve any convenient purpose. It can be used as a coded file protect device or it can be used to identify or tag a category of records, such as receipts, withdrawals, payments, or inventory.

On certain read or write operations the file control reads and compares the first four (high-order) positions of HA1 and the first two (high-order) positions of HA2 with address data stored in the file control. The address verification assures the correct track selection before data reading or writing.

Record Addresses

Each record on the data track must be preceded by a record address, which identifies individual records, allowing random access to any file record (Figure 11, area 6).

The record address must be six or more alphameric characters. Only the first six characters are compared during the verify address cycle. The numeric portion of the four high-order characters are compared, but all bits of the fifth and sixth characters are compared.

No relationship is necessary between the record address, used to identify an individual record on a track, and the home address recorded on the track. Record addresses are assigned and written by the user to fit any convenient addressing scheme.

Record Areas

The record areas contain the record data (Figure 11, area 7). There may be one or more records with a minimum of two characters and a maximum limited by the physical length of the track.

AGC Areas

Automatic gain control (AGC) compensates for signal variation at the selected read-write heads. A five-character burst of all bits is automatically recorded immediately before each address or record area. The five-character AGC burst is recorded before every address or record written. When reading, the AGC bits generate a bias voltage used to adjust the read amplifier gain before reading data bits (Figure 11, area 2).

Check Areas

When writing an address or record on disk, the file control develops a three-character check code for each address or record written and records the check character code on the disk (Figure 11, area 4). When an address or record is read, the file control uses the read data to generate the same check code and compares it against the previously written check code. If a true comparison is not made, an error condition results. The check characters appear on the file as the last three characters of a four-character field. The first character of the four-character field is the last character of the preceding address or record.

Gaps

A one-character gap is written automatically by the file control to separate each address and record from the preceding five characters of AGC (Figure 11). When reading, this gap is detected by the data gap singleshot. The absence of AGC bits causes the data gap singleshot to time out. Data gap singleshot output rises to indicate the next bits are either address or record data.

A second one-character gap is written automatically by the file control in the main body of each address or record (Figure 11). This one-character gap separates the last address or record data character from the preceding characters. This gap is different from the one-character gap that separates AGC from the address or record data because it is written without a sync bit. When reading this gap, the missing sync bit conditions three file control triggers (the three zeros triggers). These triggers enable the file control to read the character after the gap as the last address or record character, and to process the remaining three characters as check characters. Check characters are read, transferred to the file control, and used to verify the validity of the address or record data read; they are never transferred to the system.

Following the check characters, a third data gap (nominally six characters in length) is present for two reasons: (1) when writing does not involve a complete track, space is provided to prevent partial erasure of the next address or record area because the erase head precedes the read-write head; (2) to allow space (time) to switch the file system from read to write status if the operation requires it. The end of this third type of gap, the start of the next address or record area, is determined by the output of two format track singleshots. These two singleshots, the short and long gap singleshots, monitor format track data and are discussed with the following section, "Format Track."

Format Track

- **Written to define storage space (data areas) of data tracks.**
- **Format track written as all bits or no bits.**
- **No bit areas (gaps) recognized by format singleshots to define data areas.**

The format tracks are written to define how the storage space of the tracks is to be divided into records, identified, and used. This is similar to the field definition function performed by a keypunch program card.

Before data can be written on a data track, the format track must be written for the cylinder. Provision is made to allow reading any data track regardless of the presence or condition of the related format track. The 253 format tracks, one for each customer cylinder (250 total) plus three for CE operations, are located on one disk surface: the format disk.

Format tracks are written as areas of all bits or no bits. HA1, HA2, record address, record, and filler areas are written with all bits characters. The format track gap areas are written with no bits characters. The format track gaps are sensed with the short and long gap singleshots; the trailing edges of the gaps are sensed with the short and long gap holdover singleshots. Format gaps are either short gaps (three microseconds or greater) or long gaps (24 microseconds or greater). The sequence of format track areas must be: HA1, gap, check area, gap, HA2, gap, check area, etc.; therefore, any related data track area can be recognized with the short and long gap singleshot outputs (Figure 11, format track).

The short and long gap singleshot outputs are applied to the format recognition circuit inputs. The format recognition circuit converts the singleshot input signals to address, record, and check area outputs, which condition the file control to process the read or write data accordingly. For example, if the file system processes an address area (Figure 11, area H) and recognizes a format track short gap (Figure 11, area J), the format recognition circuit output signals check area, and check area signal conditions the file control to process the check characters because each address area is always followed by a check character area. Another example: if the file system processes a check area following an address area, and recognizes a format track short gap (Figure 11, area L), the format recognition circuit signals record area and record area signal conditions the file control to process record data because each address check area is always followed by a record area.

While the file control is processing the record area (Figure 11, area M) both the short and long gap singleshots time out in the format track long gap (Figure 11, area N). When the short gap singleshot times out, the record check area is defined because each record area must be followed by the record check area. The long gap singleshot times out and remains off until the first bit of the following address area (Figure 11, area H) is sensed. When long gap singleshot detects the trailing edge of the long gap (Figure 11, area N), the file control is conditioned to process an address area. Every time the long gap trailing edge is detected, the file control is conditioned to process an address area.

The format recognition sequence repeats. The short gap (Figure 11, area P) following the last record area is detected. The short gap signal following a record area signals the file control that the last record has been processed and all that remains to be processed are record check characters.

Operations

- **All 7631 operations involve one or more of the five basic cycles.**
- **Control cycle—sets type of operation and file address where it will be done.**
- **Prep read-write cycle—prepare 7631 and 1301 to read or write.**
- **Address verify cycle—prove correct track is selected in 1301.**
- **Read data cycle—transfer 1301 read data to system.**
- **Write data cycle—transfer system write data to 1301.**

All 7631 operations involve one or more of the five basic cycles:

1. Control
2. Prep rd-wr (prepare to read-write)
3. Verify address
4. Read data
5. Write data

All on-line 7631 operations (except a sense command from a 7000 system) started by a 7000 control command or a 1410 file operation issued to the 7631 cause the 7631 to execute a control cycle. During the control cycle the 7631 requests and receives an order word to store in the operation and address registers. At the completion of the control cycle the 7631 has stored operation data defining the operation to be performed and the address data that tells where to perform the operation.

The 7000 system order word transmitted from the data channel to the 7631 during a control cycle usually contains a two-character operation code and eight characters of address information (Figure 12). Since some operations do not require address information, only the two-character operation code is transmitted to the 7631.

Control data transmitted from the 1410 to the 7631 always contain an op code character and eight BCD address characters (Figure 13). The op code character is transferred directly from the 1410 units number register to the 7631 operation decoder. The operation decoder output sets a 7631 control op trigger; the 1410 address data is stored in the 7631 address register.

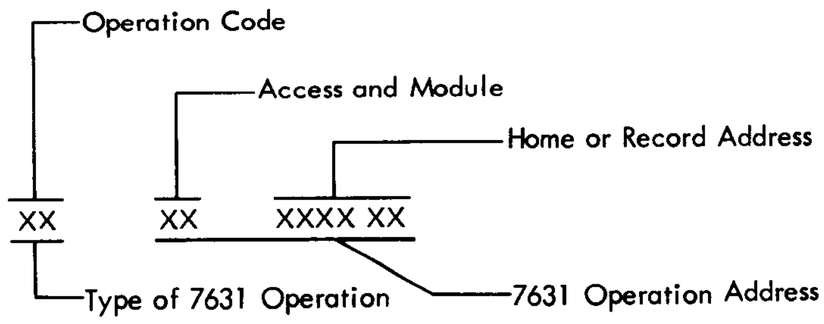


Figure 12. 7000 Systems Order Word Layout for 7631

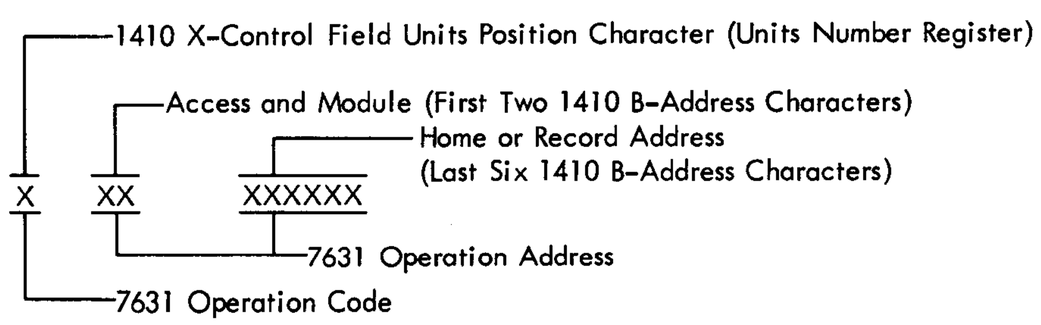


Figure 13. 1410 System Control Data for 7631

Control

- **Requests control data from the using system.**
- **Decodes the operation or order code.**
- **Stores the control data (address data).**
- **Issues signals to the selected 1301 file when required.**
- **Signals end of control to the using system.**

A control operation is a preparatory cycle for subsequent 7631 read or write operations. Essentially a control operation serves the same function in a 7631 as the instruction readout cycle serves in a computer; the main difference is that the 7631 must obtain its control data (instructions from 1410 systems, orders from 7000

systems) from an attached system. Any file operation started by the 1410 or any control command accepted by the 7631 results in a control cycle. Once a control operation is started, the 7631 performs as described.

Briefly, the 7631 control circuits are used to store instructions or orders transferred from the system before reading or writing (Figure 14).

Access unit positioning, bit mode, the address to be verified, and the type of reading or writing are determined by control data stored in the 7631 during control cycles. Consider the control cycles that must precede reading or writing:

1. *Control-seek:* A control cycle (executed by the 7631 in response to the using system's file operation) stores control data that is transferred to the selected 1301 access unit. The control data transferred from the 7631 to the 1301 causes the 1301 to position the read-write heads to the correct cylinder.

2. *Control—bit mode (7000 only):* The 7631 reads or writes in six- or eight-bit mode. Control data decoded

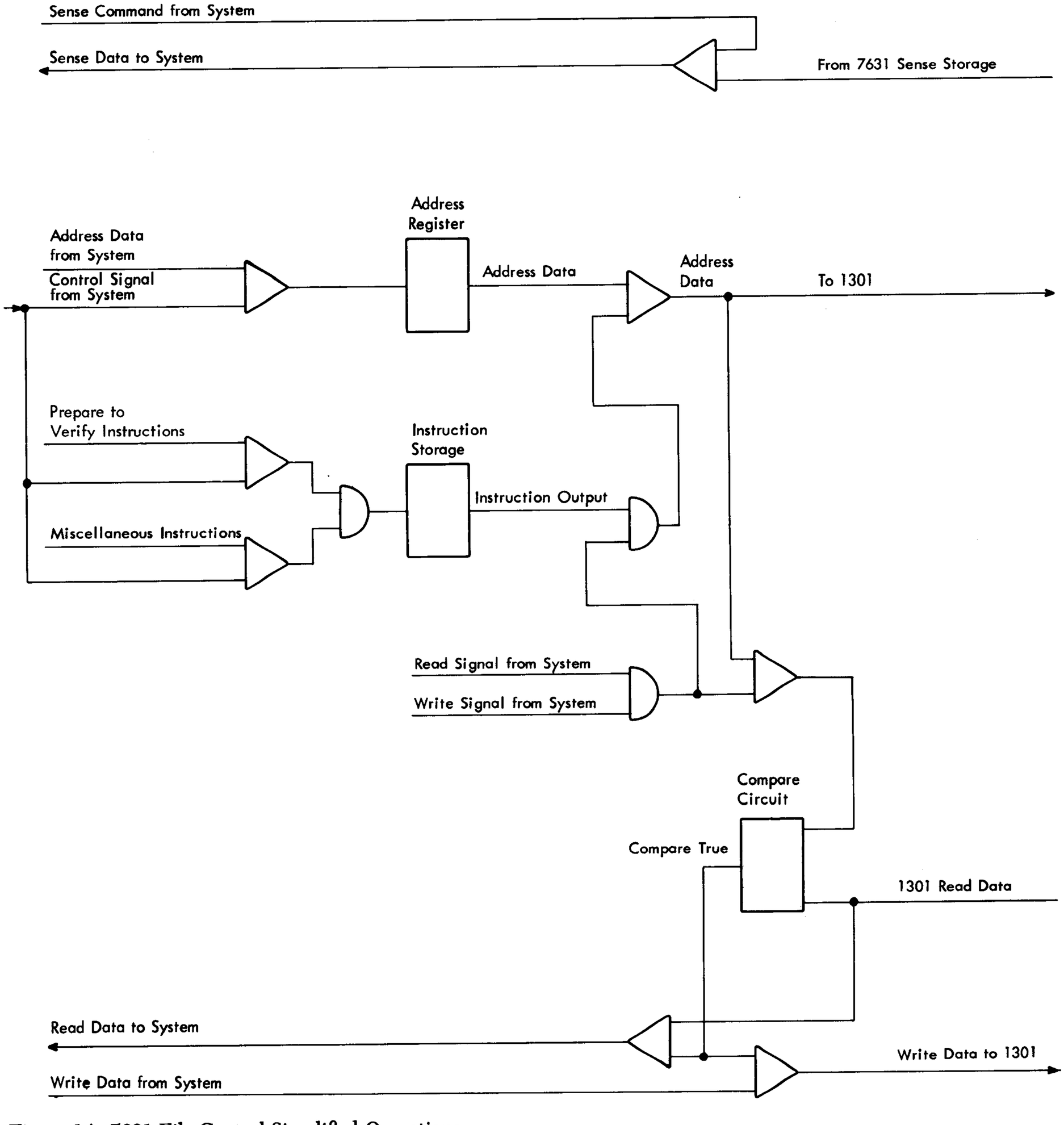


Figure 14. 7631 File Control Simplified Operations

during this control cycle determines the bit-mode of the next read or write operation.

3. *Control—prepare to verify:* The operation code stored during this third control cycle determines the type of read or write operation: single record operation (SRO), track without address (TWA), etc. The eight bytes of control address data stored are used to select the correct 1301 access and module and to provide the address of the track or record on the following verify address cycle.

Read-Write

Receipt of the read or write signal causes the 7631 to select the access mechanism and read-write head with the address data stored during the previous control-prepare to verify cycle. The 7631 then synchronizes with 1301 rotation, locates the correct read or write data area, and either requests and writes data from the system on the designated track areas, or reads the designated track areas and transfers the read data to the system (Figure 14). Each read or write sequence can be divided into cycles: prepare to read-write, verify address, and read or write data.

Cycles

Prepare to Read-Write Cycle

Receipt of a read or write signal causes the 7631 to start a prepare to read-write cycle. All read or write operations start with a prepare to read-write cycle, which prepares both the 7631 and the 1301 for reading or writing (Figure 15). If all the prepare to read-write cycle functions are not successfully completed, the 7631 indicates an error occurred and prevents continued read or write operation.

Verify Address Cycle

The verify address cycle is executed after a successful prepare to read-write cycle, except when the HAO-CE switch is active and the operation is either HAO read, HAO write, or format write. These three operations (special CE operations) executed with the HAO-CE switch active cause the 7631 to bypass the address compare cycle. During the verify address cycle the address stored in the 7631 address register (track-head and random record sections) is compared with either the home address or the record address read from the disk (Figure 15). (If the track contains more than one record, a number of address verify cycles can occur for single record operation because record addresses are compared until the comparing record address is found.)

The address data read from the disk is compared bit by bit with the stored address data and is also used as the input to the shift register to generate check characters. After the last bits of address data are compared, the 7631 reads the check characters and compares them bit by bit with the generated check characters to verify the validity of the address data read from the disk. If a compare failure occurs during the address data or check character comparisons, the no record found trigger is set to end the operation and prevent the read or write data cycles from occurring.

Read Data Cycle

Following a successful address compare cycle with the read trigger set, the 7631 locates the read data area, address or record area, depending on the type of prepare to verify operation stored, and reads each bit from the track into the 7631 serial register storage. The read bits are stored in the serial register until a complete character is assembled and the correct parity is assigned. The data character, with a parity bit, is transferred to the system and the next character is read. Each bit read from the disk is also entered into the shift register where the check characters are generated.

Check characters read from the disk after the address or record characters are compared with those generated by the shift register; the check characters are not transferred to the system but are used to determine the validity of the read data. If the check characters do not compare, the 7631 indicates a parity error after the read operation is complete. A parity error does not stop or alter the read operation except to indicate the error occurred. The read data cycle repeats for each additional address or record area if the prepare to verify operation requires additional track data transfers (Read Data Cycle, Figure 15). The read operation ends when either the 7631 reads and signals that the last of the data characters are transferred, or the system signals end after the required amount of data has been received.

Write Data Cycle

Following a successful address compare cycle with the write trigger set, the 7631 starts a write data cycle. During a write data cycle the 7631 must first locate the area to be written; this area can be an address or record area depending on the type of prepare to verify operation. When the correct area is found, the 7631 generates and writes the required five-character AGC burst and the one-character gap following. After the gap the first write data character is transferred into the serial register where it is checked for correct parity. If parity is incorrect, the 7631 indicates a parity error after the write operation is complete. A write parity error does not stop the write operation, but indicates an error after the write operation completes.

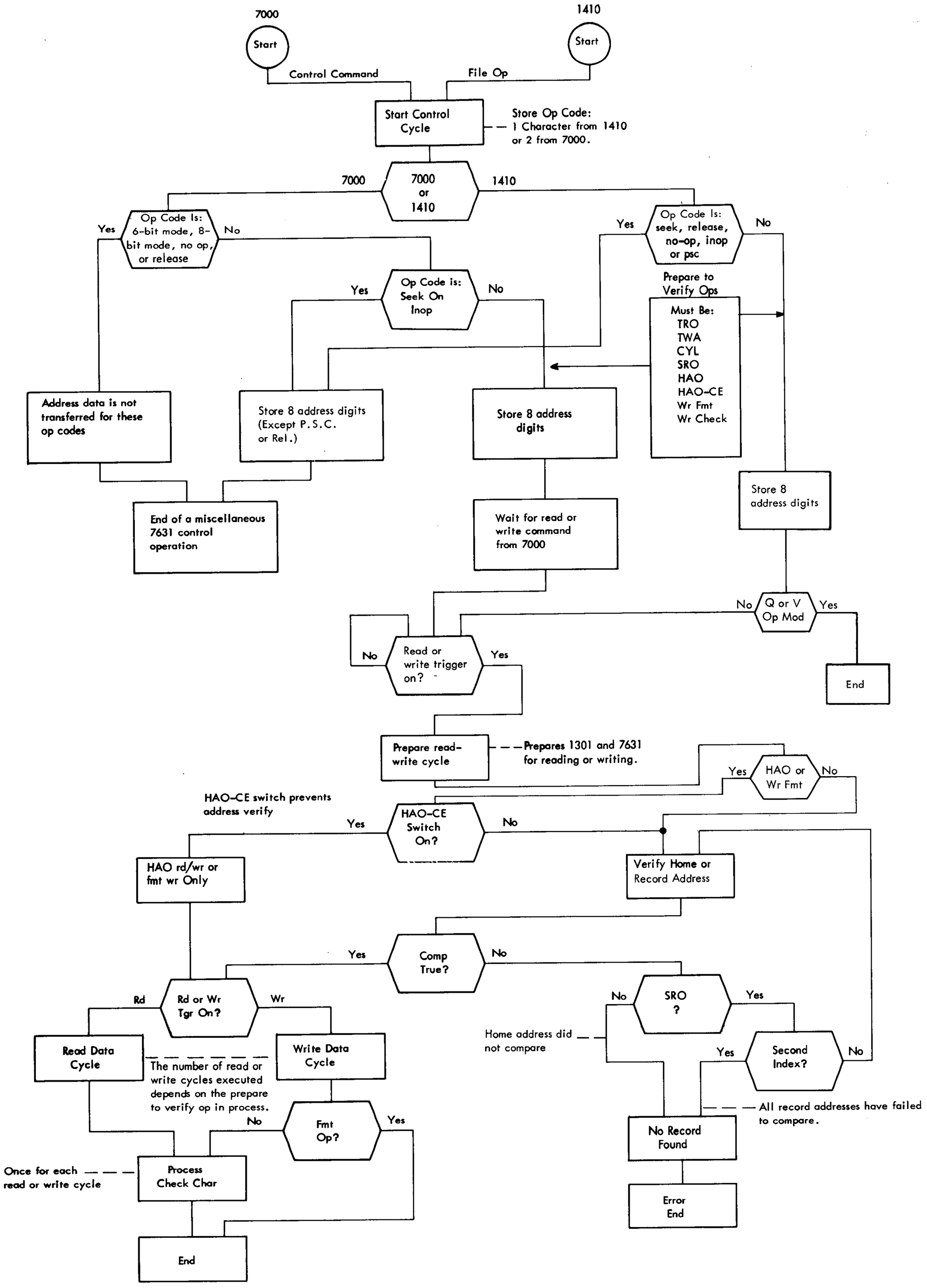


Figure 15. Operations Flow Chart

The character in the serial register is transferred bit by bit to the 1301, where it is written, and also enters the shift register where check characters are generated. The request, write data, and check character generation continue until the write data area is filled. The shift register contents (three check characters) are recorded immediately following the last character of write data to conclude the write data cycle. The write data cycle repeats for each additional address or record area if the prepare to verify operation requires additional track data transfers (Write Data Cycle, Figure 15). The write operation ends when the 7631 finds the track recording areas are filled with write data, or when the system signals end after the last write data is transferred to the 7631.

Sense Command (7000 Systems only)

The sense command is used by the 7000 systems to obtain status information from the 7631. Receipt of the sense command causes the 7631 to transfer the status word to the 7000 system (Figure 14). The status word is made of ten 4-bit bytes of error, status, and attention information. Ten sense data transfers are required to transfer a complete sense word.

Cycle Sequence

- **Two primary timing sources are used.**
- **625 KC oscillator in 7631 is used for control, prep R/W cycles and sense (7000).**
- **625 KC clock track on 1301 is used for address verify, read and write cycles.**

Machine Timing

The two primary sources of timing used by the file control are:

1. A prerecorded 625-KC clock track, written on the 1301, which provides the primary timing source for operations causing bits to be written on or read from the 1301 file (Figure 16).

2. A 625-KC oscillator in the file control unit which provides timing for operations that do not cause bits to be written on or read from the 1301 (control, sense and prepare to read-write) (Figure 16).

Data operations fall into one of two categories: read or write.

Read: The 1301 is a mechanical device, and the data heads and clock head are not rigid and immovable, so that the timing relationship between any given data head and the clock head does not remain constant. For proper clocking during a read operation, the timing relationship of the data track and the clock track is established at bit sync time of each character. The 1.6 microsecond sine wave read from the clock disk is divided into four 400-nanosecond segments called phases 1, 2, 3, and 4. The first bit (sync bit) of each character arrives during one of these phase timings and causes the phase selection circuitry to "lock on" (select) and gate the appropriate phase pulses to the delay line. The timing sequence for each character read is started in relation to its bit-sync, insuring correct data clocking.

Write: When writing, the hold phase line is made active. Hold phase causes the phase selector to select one of the four timing phases and write the entire data area with the same timing phase.

Non-data operations are control, sense and prepare to read-write. During non-data operations the phase selection circuitry is degated and the 625-KC oscillator is gated to the delay line pulse generator input.

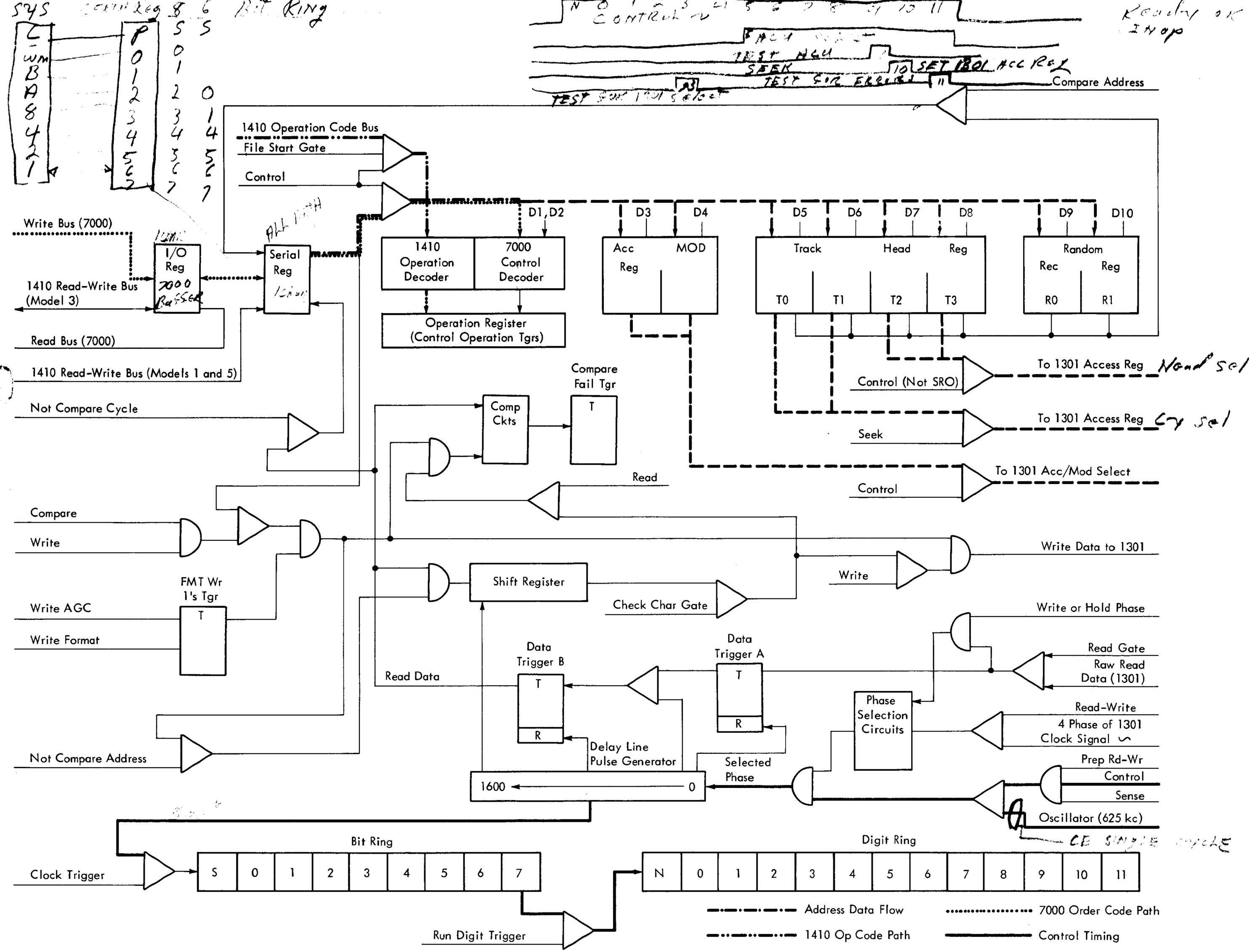


Figure 16. Control Data Flow Diagram

1410 Control Cycle

- **Initiated by file operation from 1410 unit select register.**
- **Sets type of file operation from 1410 units number register.**
- **Gate address data (control word) specified by B-address of 1410 instruction into address register.**
- **Address register consists of access, module, track and random record registers.**
- **Access and module register select a module.**
- **Track and RR register determine which track is used.**

When the 1410 processes a 1301 file instruction it issues file operation to prepare the 7631 for receipt of control information, an operation code, and eight address characters. Receipt of file operation from the 1410 causes the 7631 to start the control cycle (Figure 15). Receipt of the 1410 file start gate causes the 7631 to decode the 1410 operation code. (The units number register output, the operation code, is available on the 1410 operation code bus; when the operation code is decoded the corresponding 7631 control operation trigger is set.) Figure 17 shows the 1410 instruction layout and relates operation codes to 7631 control operation triggers. Figure 16 (upper left corner) shows the 1410 operation decoder and operation register.

The control signal gates the oscillator to start the 7631 timing circuits (Figure 16, lower right corner). Control cycle digit timing enables the 7631 to gate eight address characters from the 1410 B Address field into storage. The address data flow is: from the 1410 E2 register to the 1410 read-write bus, from the read-write bus into the 7631 I-O register (I-O register is not in 7631 models 1 and 5), from the I-O register to the serial register, and from the serial register into the address register via the storage bus (Figure 16, data paths to the

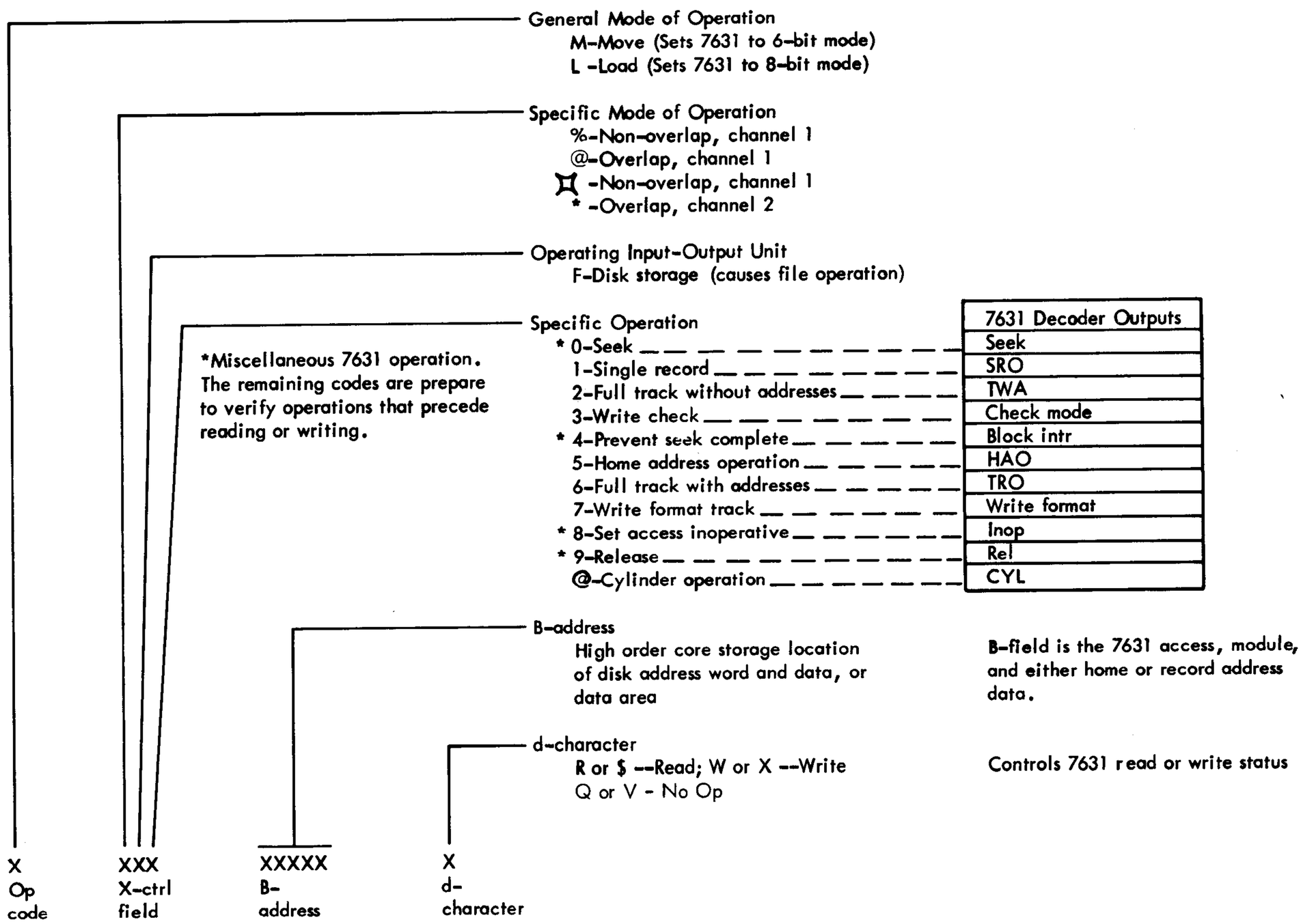


Figure 17. 1410 Instruction Layout

storage bus). One data strobe is issued by the 7631 for each character to maintain data transfer synchronization between the 7631 and the 1410. After the first data strobe is issued, the 1410 drops the file start gate because it is not needed to continue the address data transfers. With digit pulses D3 through D10, each address character is gated from the 7631 storage bus into a different segment of address register storage. After the last address character is stored, the 7631 issues end operation, for the miscellaneous instructions. The miscellaneous control instructions are: set-inop, no-op, release, seek, or prevent seek complete instructions. End operation causes the 1410 to stop file operation until the next file instruction is processed by the 1410. Figure 15 shows the miscellaneous instructions that end without causing a read or write operation.

After the last address character is stored and the instruction is a prepare to verify type (not set-inop, no-op release, seek, or prevent seek complete), the 7631 inhibits end operation and issues end of address transfer, 1410 address transfers stop and file operation continues. Because end operation is not issued for prepare to verify type instructions, the 1410 issues file start gate a second time. The second file start gate causes the 7631 to sample the CPU to file read and CPU to file write lines; the sample causes either the read or write trigger to set. CPU to file read and write lines are controlled by the 1410 instruction d-character. A read or write operation starts when the 7631 read or write trigger is set after a prepare to verify type instruction is stored and the control cycle is complete (Figure 15).

Figure 15 shows that the 7631 accepts two types of 1410 instructions: instructions that cause a 7631 control cycle and end file operation after completion of the 1410 second address transfer cycle, or instructions that cause a 7631 control cycle followed by a read or write cycle.

7000 Control Cycle

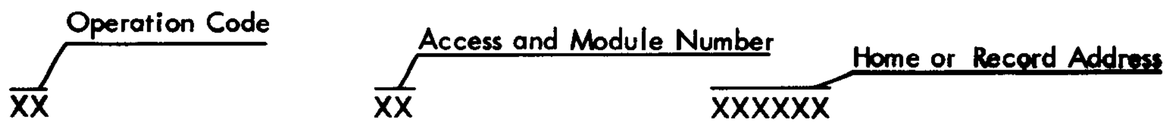
- **Initiated by control command.**
- **First two bytes of control data set type of file operation.**
- **Next eight bytes of control data set address register in 7631.**
- **Address register consists of access, module, track and random record registers.**
- **Access and module register select a module.**
- **Track and random record register determines which track is used.**

When a 7000 system issues a control command to a 7631, a command response is returned, indicating the 7631 is prepared to execute the control command. The control command causes the 7631 control cycle to start and gates the oscillator to the timing circuits (Figure 16, lower right corner). Two service requests are issued to gate in the first two bytes of control data, the order code. (See Figure 18 for 7000 order codes and names of the 7631 control operation triggers set with the 7000 order codes.) The first two bytes of control data, the operation code, are transferred from the write bus into the I-O register to the serial register and on to the storage bus, and from the storage bus to the control operation decoder (Figure 16, upper left corner).

One control operation trigger is set as a result of decoding the first two bytes of control data. If the first byte of control data decoded is zero (called decimal 00 in ALD's) the instruction is either no-operation, release, six-bit mode, or eight-bit mode; these instructions do not require addresses (Figure 15). The 7631 issues normal end to complete the control cycle immediately following decoding (decimal 00 decoding).

If the first byte of control data decoded is eight (referred to as decimal 80 in ALD's) the instruction requires eight address characters. The file control sequentially issues eight additional service requests to gate the required address data from the system into the address register. Each address character received is gated into a different segment of the address register with digit pulses D3 through D10. Following the last address data transfer cycle, the 7631 issues end. File operation does not continue until the attached 7000 system issues another command.

Figure 15 shows there are two types of control orders: decimal 00 type orders to transfer the operation code without address transfers, and decimal 80 orders to transfer the operation code and eight characters of address data.



Order	Mnemonic Code	Numeric Code	7631 Op Decoder Output
No Operation	DNOP	00	No-Op
Release	DREL	04	Rel
Eight-Bit Mode	DEBM	08	8-Bit Mode
Six-Bit Mode	DSBM	09	6-Bit Mode
Seek	DSEK	80	Seek
Prepare to Verify, Single Record	DVSR	82	SRO
Prepare to Write, Format	DWRF	83	Write Format
Prepare to Verify, Track with No Address	DVTN	84	TWA
Prepare to Verify, Cylinder Operation (Optional Feature)	DVCY	85	CYO
Prepare to Write Check	DWRC	86	Write Check
Set Access Inoperative	DSAI	87	Inop
Prepare to Verify, Track with Address	DVTA	88	TRO
Prepare to Verify, Home Address	DVHA	89	HAO

Figure 18. 7000 Order Layout

Prepare To Read-Write Cycle

- **Initiated from 7000 system by read or write command.**
- **Initiated from 1410 by read or write signal from channel input or output mode.**
- **Selects and conditions 1301 to read or write.**
- **Performs several circuit checks.**
- **Successful completion allows address verify cycle to occur.**
- **On CE operations will force a compare true.**

The prepare to read-write cycle, called prep rd-wr in ALD's, is needed to condition numerous circuits in the 7631 and the 1301 before every read or write data operation. Either a 1410 read or write signal controlled by the 1410 file instruction d-character or a 7000 system read or write command starts the prepare to read-write cycle. The prep rd-wr cycle functions are listed below. Each number corresponds to the circled numbers shown on the right side of Figure 19.

1. Gate the Timing Circuits: The timing circuits, oscillator, delay line pulse generator, bit and digit rings are started to sequence the prep rd-wr cycle.

2. Test the Validity of the Address: The test prevents the customer from writing on a CE track (cylinder 254 or rezero). An invalid address causes the prep rd-wr cycle to end immediately with an error indicated to prevent data loss.

3. End of Address Transfer Trigger Reset: Resets the end of address transfer trigger when reading or writing follows a control operation.

4. Test for an Invalid Sequence: Before issuing a read or write signal the attached system issued the operation code (1410) or order (7000) to the file control. The operation code or order sets a control operation trigger in the file control that defines the type of read or write operation; for example, SRO (single record operation), TRO (track operation) or some other valid operation must be defined. The absence of a prepare to verify op code followed by read or write, or an operation code used only for writing followed by read causes the prep rd-wr cycle to end immediately with an error indicated.

5. Select the 1301 Access and Module: Module selection, one of ten possible selections, is gated to the specified 1301. The module and previous transferred access selection remains unchanged until the reading or writing is completed.

6. Set the T2B2 Binary Trigger Position of the Cylinder Counter: The trigger, if set with head 39 selected, causes overflow to end a CYO operation (cylinder opera-

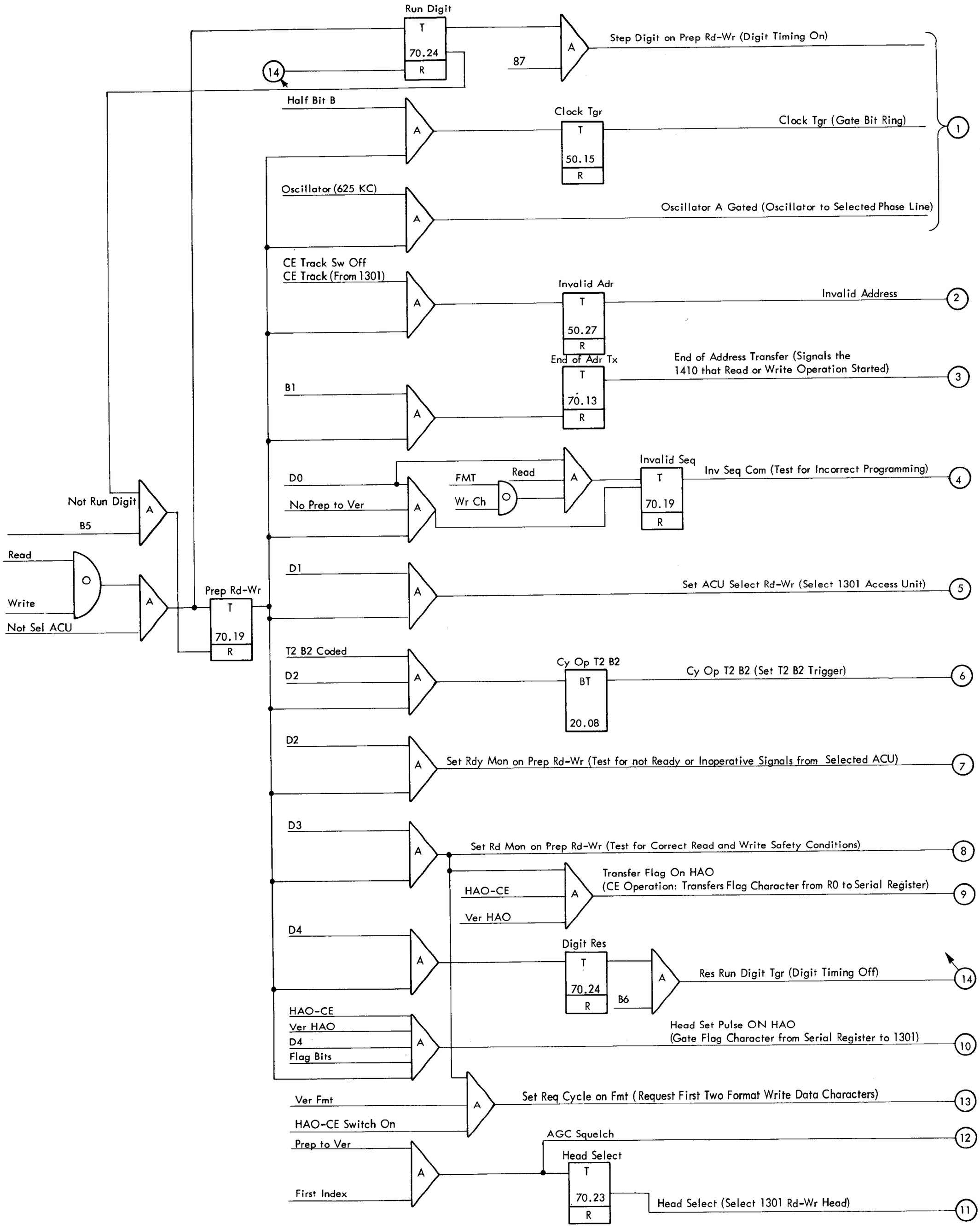


Figure 19. Prep Read-Write Cycle Simpilfied Logic

tion) after reading or writing the last track of the cylinder.

7. Test the Selected 1301 Access (ACU) Unit for Not Ready and Inoperative Conditions: The ready monitor trigger is set, for the duration of the read or write operation, to cause an immediate error stop if the selected access unit signals not ready or inoperative to the file control.

8. Test 1301 Read and Write Safety Conditions: The read monitor trigger is set to gate three possible safety error conditions. If the file frame (1301) read safety is off, write safety is on, or if the write monitor trigger is set and write safety is off, an immediate error stop occurs. The test assures the 1301 is in read status at the start of each read or write operation. The read status of the 1301 should not change until the file control is prepared to write data.

9. Transfer Flag on HAO: An alternate track address transfer occurs (the result of a CE-HAO operation) from random record register R0 to the serial register.

10. Set Head Pulse on HAO: The function permits a customer engineer to select an alternate data track to replace a damaged data track without physically removing the damaged disk. The set head pulse on HAO gates the serial register contents (9 in this listing) to the selected 1301.

11. Select the Read-Write Head: The pulse causes the 1301 to select the specified read-write head.

12. Generate AGC Squelch Conditions (SRO only): The single record operation (SRO) is not started with index signals. Index area filler cannot be used to adjust the 1301 read amplifier gain before reading data, so the file control generates AGC squelch, a 350 microsecond signal, plus a 200 microsecond delay to adjust the 1301 read amplifier prior to reading data.

13. HAO-CE Format Write Data Request: The HAO-CE format write operation bypasses the address compare cycle. A format write instruction with an address compare cycle (not HAO-CE type) requests and stores the first two format write data characters at the end of the address compare cycle; therefore, the HAO-CE format prep rd-wr cycle data is needed to insure that two format write data characters are transferred and available for writing before late index.

Verify Address Cycle

- **Compare 1301 address data with 7631 address register in 7631 compare circuit.**
- **1301 address data read from selected 1301.**
- **7631 address register contains address of file operation set up during control cycle.**
- **Fail to compare = no record found.**
- **Successful compare allows read or write data cycle to occur by indicating compare true.**

The verify address cycle, when required, occurs before read or write data transfers. The track or record address is verified (compared with the address stored in the 7631 address register) to insure reading or writing occurs with the correct track or record. Format write and home address operation (HAO) read or write operations executed with the HAO-CE switch on bypass the verify address cycle; all other read or write operations verify either home address or a record address before read or write data transfers. If the address stored in the 7631 address register fails to compare with the disk address, the 7631 indicates no record found and stops operation.

As an example of a verify address cycle, consider a track operation (TRO) read or write; a TRO requires home address one and two verify before read or write data transfers. (HA1 and HA2 are shown in Figure 20.) Completion of a successful prep read-write cycle is a prerequisite to the verify address cycle. The completed prep read-write cycle conditions the 7631 to accept the next early and late index signals, which gate format read data to the format recognition circuits. When the format recognition circuits signal address area (HA1), the address area signal causes the 7631 to generate hold phase. This forces the phase selection circuits to select one of the four 1301 clock phases signals for a timing

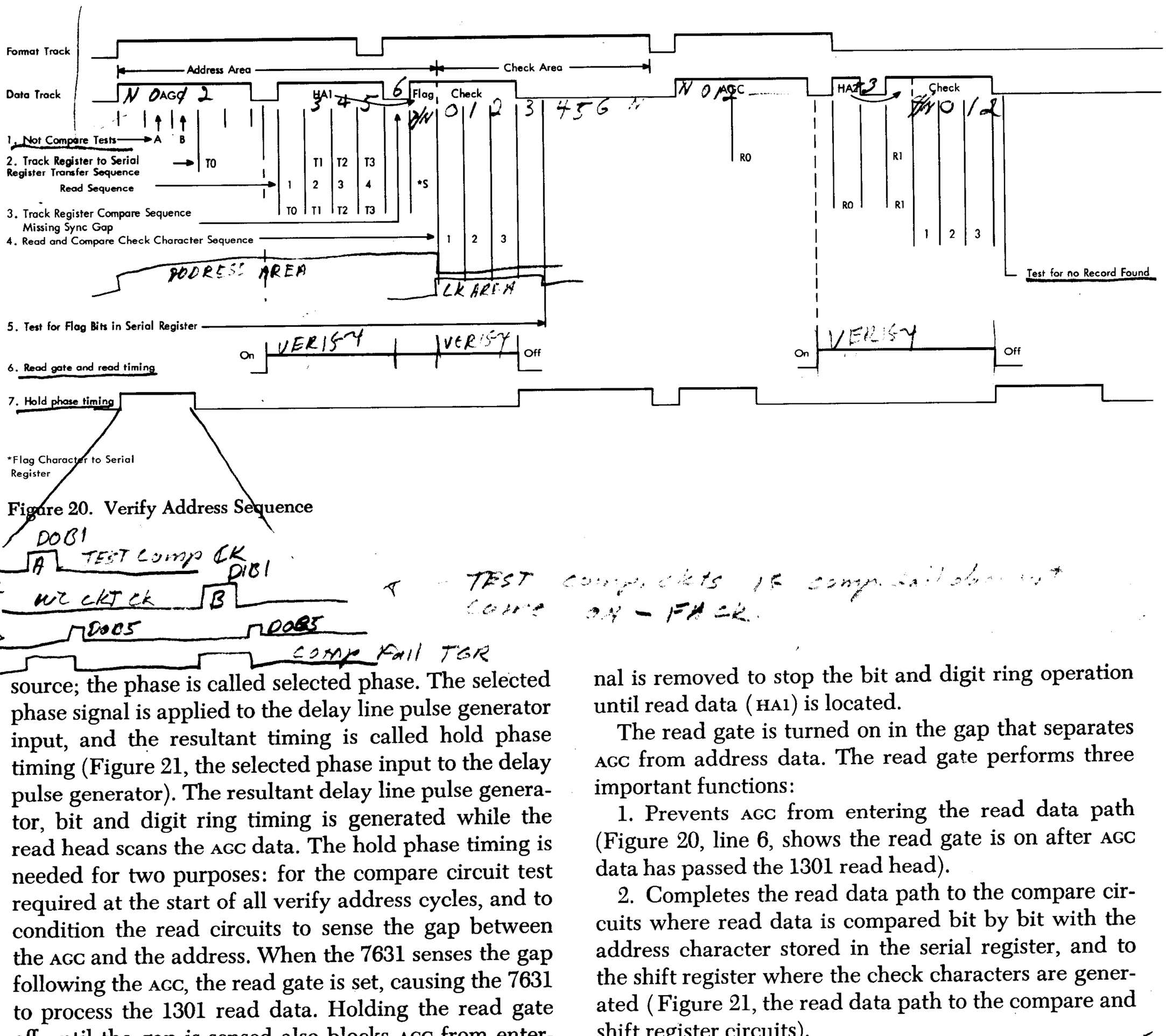
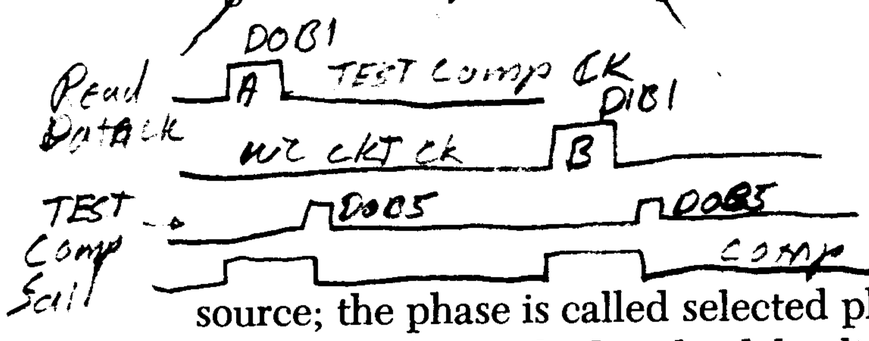


Figure 20. Verify Address Sequence



source; the phase is called selected phase. The selected phase signal is applied to the delay line pulse generator input, and the resultant timing is called hold phase timing (Figure 21, the selected phase input to the delay pulse generator). The resultant delay line pulse generator, bit and digit ring timing is generated while the read head scans the AGC data. The hold phase timing is needed for two purposes: for the compare circuit test required at the start of all verify address cycles, and to condition the read circuits to sense the gap between the AGC and the address. When the 7631 senses the gap following the AGC, the read gate is set, causing the 7631 to process the 1301 read data. Holding the read gate off until the gap is sensed also blocks AGC from entering the 7631 read data path and being processed as read data (Figure 20, line 6).

The 7631 tests the compare circuits while in the five-character AGC area (test not compare A and B). Test not compare A tests for no compare when a simulated read one bit is compared with a simulated write zero bit; test not compare B tests for no compare when a simulated write one bit is compared with a simulated read zero bit. (In Figure 20, the not compare tests are shown on line 1.) If the compare test is not successful, the 7631 compare circuits are defective and the file operation is stopped, indicating a file adapter circuit check.

Following a successful compare circuit test, the contents of track register position T0 are gated to the serial register, where they are temporarily stored until compared. (Figure 21, the compare address gate, shows the path to the serial register.) Figure 20 shows when T0 is transferred to the serial register. The hold phase signal is removed to stop the bit and digit ring operation until read data (HA1) is located.

The read gate is turned on in the gap that separates AGC from address data. The read gate performs three important functions:

1. Prevents AGC from entering the read data path (Figure 20, line 6, shows the read gate is on after AGC data has passed the 1301 read head).
2. Completes the read data path to the compare circuits where read data is compared bit by bit with the address character stored in the serial register, and to the shift register where the check characters are generated (Figure 21, the read data path to the compare and shift register circuits).
3. Gates read data to the timing circuits.

Because 1301 read data and timing signals are derived from two different heads, each mounted at the physical end of non-stable arms, a fixed timing relationship does not exist between the 1301 read data and clock track signal for long time intervals. A precise data sample and accurate compare timing is needed for reliable read operation. Because 7631 read timing is derived from the 1301 clock track signal, some means of synchronizing 7631 read timing with 1301 read data is required; the phase selection circuits are used for this purpose.

Phase Selection

The read gate allows read data to enter the 7631 phase selection circuits (Figure 21). Each character written on the 1301 is preceded by a bit sync; during read,

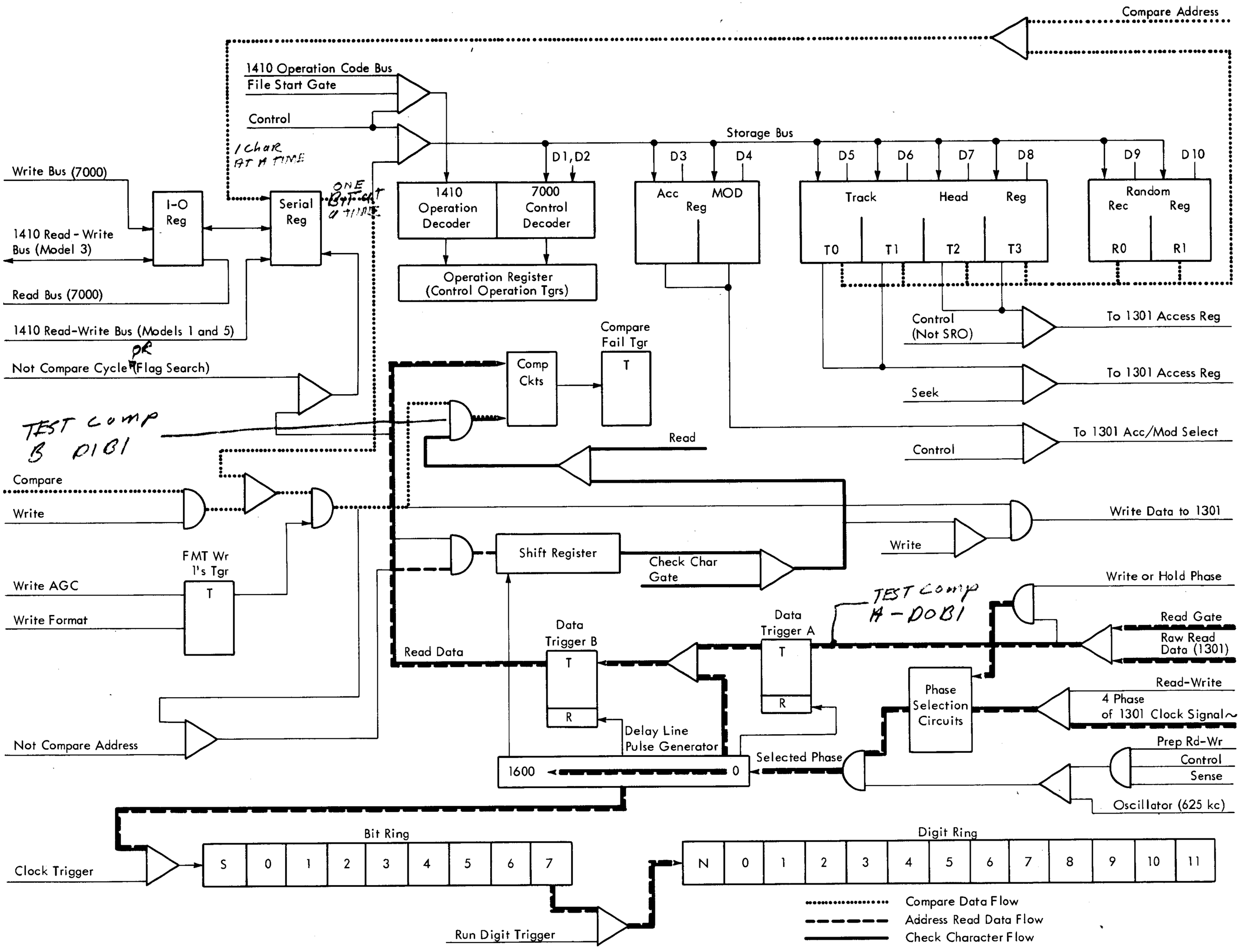


Figure 21. Verify Address Data Flow Diagram

each bit sync is used to determine the phase relationship between read data and clock track signals. Bit sync is used by the phase selection circuits to select the 1301 clock track signal phase, one of four phases, that compares with the read data bit-sync phase. The comparing phase is labeled selected phase. (In Figure 21, the selected phase signal is used as the input to the delay line pulse generator.) The delay line pulse generator divides the selected phase input into accurately timed pulses needed to sample data (read), operate the shift register, provide an address verify compare sample, and step the bit ring.

Bit ring timing is important because bit ring outputs must transfer the correct serial register bit to the compare circuit when the corresponding bit is read from the 1301 track. For example, the B4 bit ring output gates the B4 serial register trigger output to the compare circuit for comparison with bit-four read from data trigger B. Digit timing is advanced one step when required for each complete bit ring cycle. Digit timing is needed to transfer address characters T0, T1, T2, and T3 to the serial register in the correct sequence for the home address one comparison. Because relation between the read data and clock track signals relationship is continuously changing, the phase selection circuits use bit-sync to determine the selected phase for only one read data character. The phase selection circuit operation is repeated as often as data characters are read, or once for each bit-sync.

Receipt of the first home address read data bit causes read data timing to start and the corresponding serial register bit (the first bit of T0) to transfer to the compare circuit (Figure 21, read data and compare data flow). Each remaining address data bit is compared with the corresponding bit transferred from the serial register. After the first character is compared, the contents of track register position T1 are transferred to the serial register (Figure 20, line 3, shows the track register compare sequence). Bit by bit comparisons continue until track register position T2 and T3 contents are compared and the data gap following is detected with the four HA1 digits read from the disk. At the same time as the HA1 comparison, the read data bits are also applied to the check character register to generate HA1 check characters (Figure 21).

After the data gap, the flag character is read from the disk and stored in the serial register (Figure 20, the fifth character in Read Sequence). The format recognition circuits condition the 7631 to compare the check character register contents, HA1 check characters, with the HA1 check characters read from the disk. A single bit compare failure during the HA1 or HA1-check characters comparison causes the compare fail trigger to set.

After a HA1 comparison the file control tests for flag bits, serial register positions B4, B5, and B6 previously read from the disk (Figure 20, line 5). Flag bits present cause an alternate track selection where the verify address cycle is repeated; the absence of flag bits enables the 7631 to end the HA1 verify address cycle and to search the data track until the recognition circuits detect HA2.

When the format recognition circuits signal record area, following the HA1 check area, the HA2 verify address cycle starts (Figure 20, right half). Random record register R0 and R1 contents are compared with the first two HA2 characters read from the track. If HA2 is more than two characters, the additional HA2 characters cannot be compared, but read and gated into the shift register to insure that the check characters generated compare with those read from the HA2 check area. Since the compare circuits were tested before comparing HA1, the test (test not compare A and B) is not repeated in the HA2 AGC area. The HA2 verify address cycle following assumes HA2 to be two characters (Figure 20).

After the HA2 data gap, separating AGC from the read data, random record register R0 contents (alpha or numeric data) are compared with the serial register. Receipt of the first read data bit causes the corresponding serial register bit to read out to the compare circuit. The comparison continues for only one more character or, in this example of a two-character HA2, until the data gap preceding the last HA2 character is detected. Following the data gap, random record register R1 contents are transferred to the serial register.

If HA2 is two characters, the second HA2 character is compared and the format recognition circuits condition the 7631 to process HA2 check characters. The check characters read from the disk are compared bit by bit with the contents of the check character register. Immediately following the check character comparison, the compare fail trigger is tested; if the compare fail trigger is set, the TRO operation ends with no record found indicated. A successful comparison causes the compare true trigger to set. Compare true enables the file control to continue to search the data track for the read or write data area.

Read Data Cycle

- **Initiated after a compare true.**
- **Locate read data area on 1301.**
- **Gate serial read data to: serial register, assign parity and gate to system, to shift register to develop check character, to phase select circuits to control timing.**
- **Locate check area and compare shift register to check characters read from track.**
- **Fail to compare causes parity error.**

After a successful verify address cycle, or an address verify bypass, the 7631 locates the address or record read data area. The address or record area signal causes hold phase timing to start. The read data cycle hold phase timing circuit is needed to condition circuits that enable the 7631 to recognize the one-character gap that separates the AGC from the read data (Figure 22). This initial timing function prevents AGC from entering the 7631 read data path and being processed as read data.

When the gap is detected, the 7631 sets the read gate causing read data flow to the serial register, the shift register, and the timing circuits (Figure 23). Read data timing causes a selected phase input to the delay line pulse generator. The resultant delay line pulse generator outputs are used to sample data trigger A (read), operate the shift register, and drive the bit ring.

The read data cycle phase selection is the same operation required to read address data for the verify address cycle. Each read data bit transferred from data trigger A to data trigger B is entered into the shift register where check characters are generated. Data trigger B is also gated into the serial register. The selected phase signal, synchronous with read data, makes the bit ring step once for each read data bit to insure that each bit is stored in the correct serial register position. Before they are transferred to the system, the read data bits are assembled and assigned parity in the serial register to make up the same character written from the computer.

Each data character is read, stored in the serial register, and transferred until the last character is processed; then the 7631 processes the check characters. The 7631 reads and compares the check characters read with the shift register contents to verify the validity of the read operation.

If the check characters fail to compare, a parity error is indicated. A parity error does not stop or alter the read operation except to indicate that an error occurred. The read data cycle repeats for each additional address or record area if the prepare to verify operation requires additional track data transfers. The read operation ends when either the 7631 signals that all the required characters are transferred, or the system signals stop.

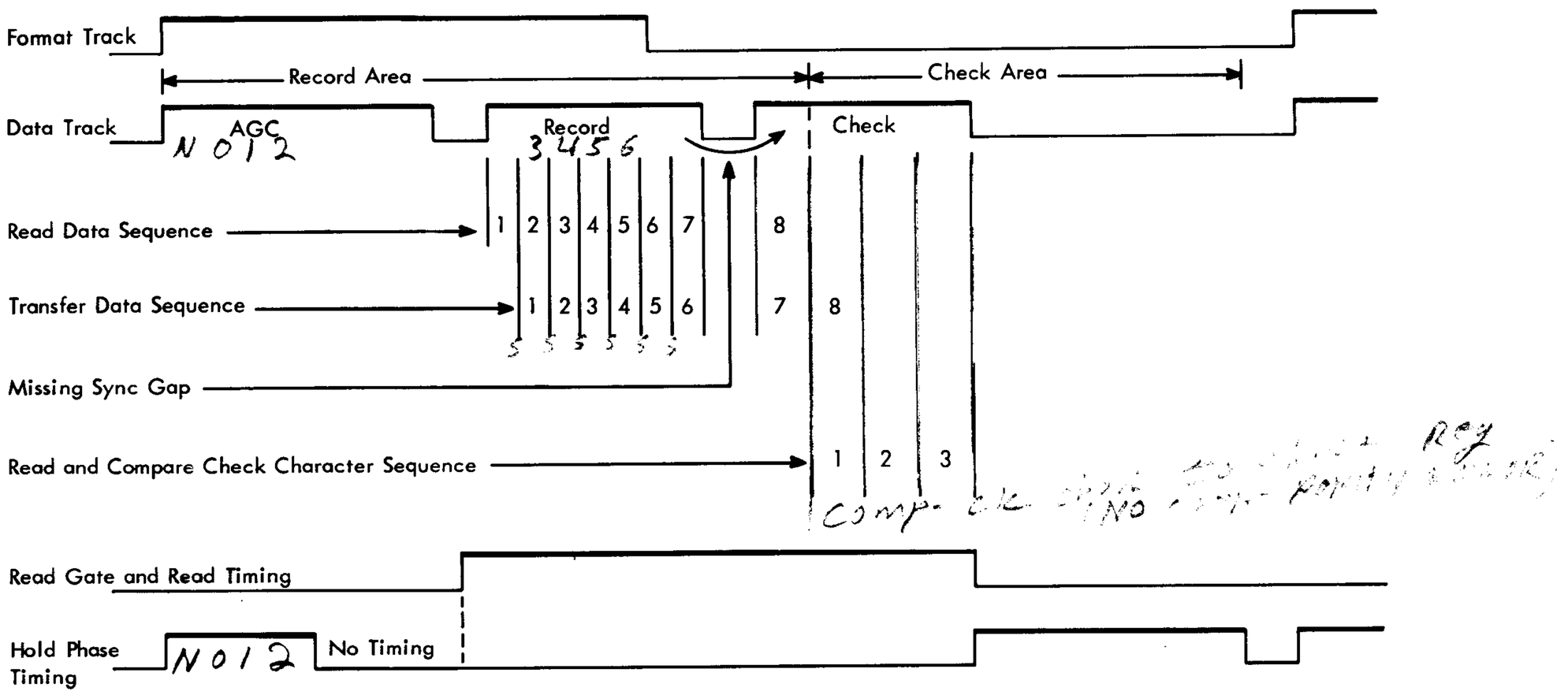


Figure 22. Read Data Sequence-Record

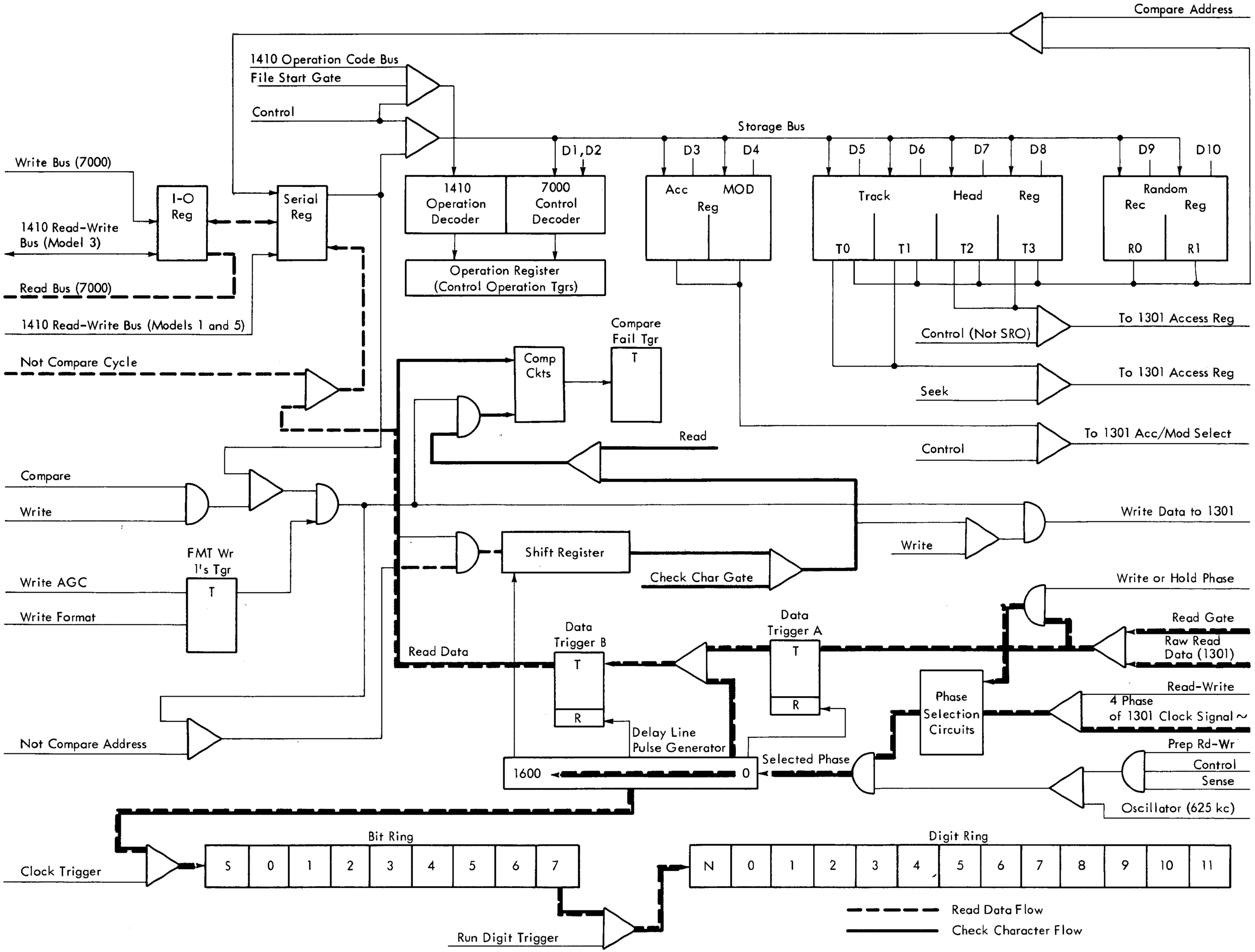


Figure 23. Read Data Flow Diagram

Write Data Cycle

- **Initiated after a compare true.**
- **Locate write data area on 1301.**
- **Write AGC for data area.**
- **Request and gate system data into serial register.**
- **Serial register is gated to: 1301 data track, to shift register to develop check character.**
- **Locate check area, readout shift register and write check character.**

The write data cycle is used to record address or record data in the correct track area. Briefly, the write data cycle causes the 7631 to locate and write five characters of AGC in the recording area. While writing AGC, the 7631 tests the shift register to insure its correct operation (Figure 24). After writing the AGC, the 7631 requests the first data character and writes the gap. Following the gap the first character is written and a second character is requested from the system. Check characters are generated from the write data as the write operation continues. When the format recognition circuits signal check area, a gap is written and the last address or record character is written. After writing the last data character the contents of the shift register (three check characters) are written to end the write data cycle.

The write data cycle occurs following a successful verify address cycle or a verify address bypass. The 7631 locates the address or record area; the address or record area signal causes hold phase timing to start. One of the four 1301 clock track phases is selected and used as the selected phase input to the delay line pulse generator for write timing. The hold phase signal holds one of the 1301 clock track phases selected from the start of the address or record area until after the check characters are written (Figure 24). The write gate and format write ones triggers are set to write the required five characters of AGC data, after which the timing circuits reset the format write ones trigger. (See Figure 25 for the AGC data path to the 1301 write bus.)

The last 28 AGC bits and the first two zeros of the gap written following the AGC are gated into the shift register for test purposes. The shift register should always generate the same pattern of check characters for the fixed input of 28 ones and two zeros. Gates are provided to test a few of the shift register trigger positions and determine if the shift register operation is correct. (Figure 24 shows where the shift register test occurs.) A test failure causes the write operation to end and indicates a file adapter FA circuit check. The five characters of AGC data are required to condition the 1301 read circuits for subsequent read operations; the following one-character gap separates AGC from the recorded address or record data.

If attached to a 7000 series system, the 7631 issues a data request while the one-character gap is written. The write data character is gated from the write bus to the I-O register (Figure 25). After the gap is written, the character is parallel-transferred from the I-O register to the serial register, where the parity check is made.

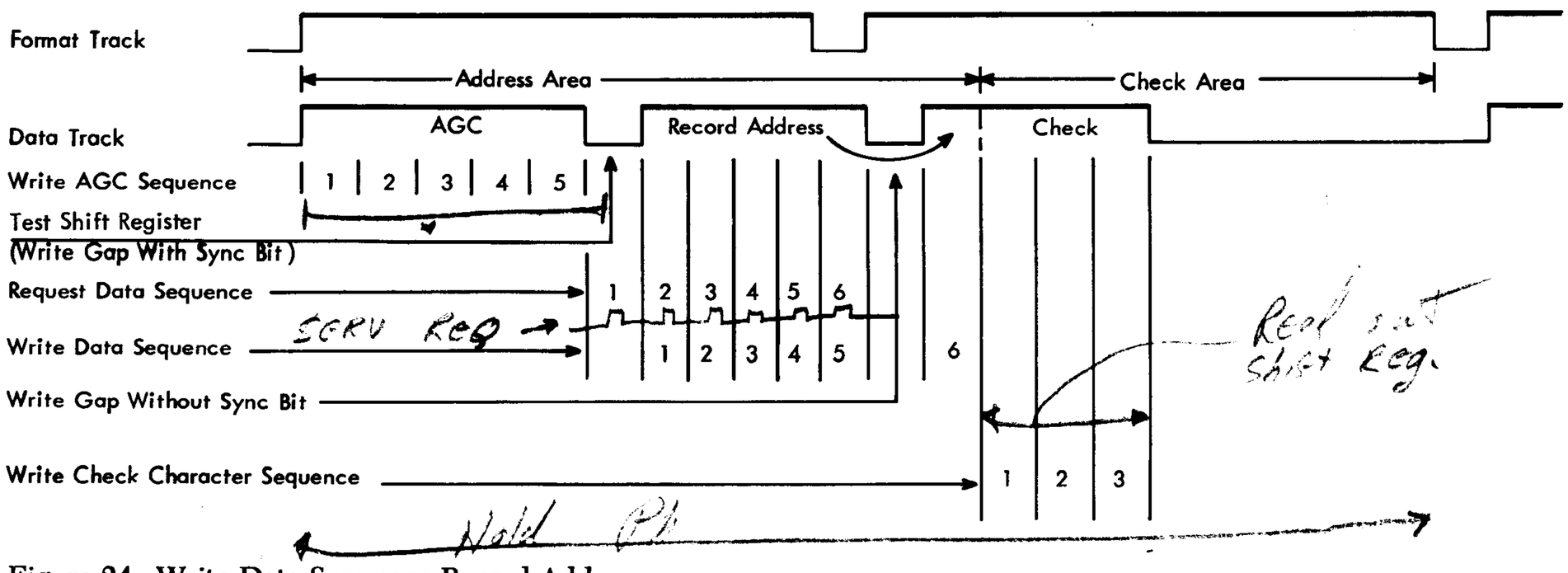


Figure 24. Write Data Sequence-Record Address

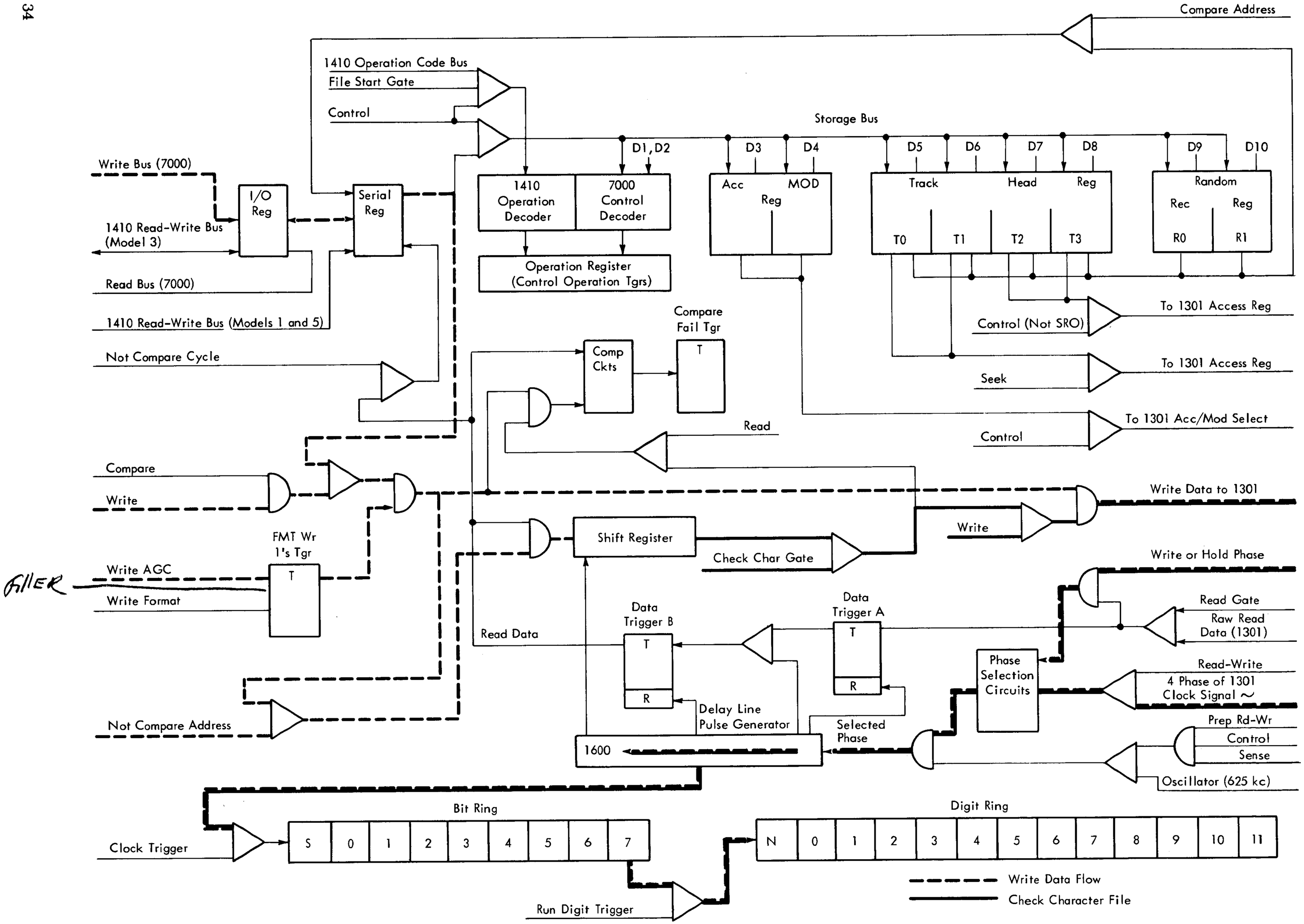


Figure 25. Write Data Flow Diagram

Although incorrect parity causes the parity error trigger to set, the error does not alter the write operation except to indicate that a parity error has occurred. Bit ring timing is used to gate each data bit from the serial register to the 1301 write bus and to the shift register. For example, bit ring output B0 gates the contents of serial register trigger B0 to the 1301 write bus and to the shift register. While the remaining bits of the first data character are being written, a second data request is issued to the system to fill the empty I-O register. After the first character is written, the second data character is transferred from the serial register to the I-O register to repeat the request-write sequence (Figure 24). Writing is repetitious and continues until the format read data shows that the end of the recording area is approaching.

If attached to a 1410 system, the data request operation is different from 7000 operation. After the gap following the AGC characters is written, the 7631 parallel transfers the first character available on the 1410 read-write bus into the serial register. Figure 25 shows that the 1410 read-write bus for the 7631 models 1 and 5 feeds directly into the serial register. The 1410 read-write bus shown feeding the I-O register is for 7631 model 3. A 7631 model 3 is used for 7000 and 1410 shared system operation. The I-O register is required for 7000 operation and used for 1410 operation also in this shared system operation.

The character parity is checked in the serial register. Incorrect parity causes the parity error trigger to set; the error does not stop the write operation except to indicate a parity error at the end of the operation. Bit ring timing is used to gate each data bit from the serial register to the 1301 write bus and to the shift register (Figure 25). For example, bit ring output B0 gates the contents of serial register trigger B0 to the 1301 write bus and to the shift register. While the remaining bits of the first data character are being written, a data strobe is issued to maintain data flow from the 1410 to the 7631.

Format signals are used to detect the end of the write data area causing the 7631 to write a one character gap, the last character of write data, and to gate the contents of the shift register to the 1301 write bus. The write data cycle repeats for each additional address or record area if the prepare to verify operation requires additional track area writing. The write operation ends either when the 7631 signals the write area, or when areas are filled, or when the system signals stop.

Prepare to Verify Instruction Operations

- **Determines manner in which the following read or write data cycle will occur.**
- **Must be set up on control cycle before prep R/W cycle is started.**
- **During control cycle on all prep to ver orders (except SRO), the head portion of the track register is gated to 1301.**

TRO (Track Operation)

- **Control cycle—set TRO op code and address register.**
- **Prep R/W cycle.**
- **Address verify cycle—compare HA1 with track register and HA2 with RR register.**
- **Read or write data cycle—transfer record address and record data between system and 1301.**
- **End TRO at end of track.**
- **If system sends stop—end TRO at end of the record address or record area.**

The operation codes for TRO are:

88 for 7000 systems

6 for 1410 systems

The basic cycles required to execute TRO are:

Control—prepare to verify TRO
Prep rd-wr
Verify address
Read or write data

After a successfully completed control cycle, receipt of the read or write signal starts the prep rd-wr cycle. The TRO operation occurs as outlined in Figure 26 after a successful prep rd-wr cycle. HA1, read from the data track, is compared with the four track-address digits stored in track position of the address register. The first two HA2 characters, read from the data track, are compared against the two address characters (alphabetic or numeric) stored in the random record register portion of the address register.

If HA1 and HA2 compare true, the read or write data cycles occur at the first record address and continue to process all records and record addresses until the computer signals stop or the physical end of the track is sensed. The basic cycles required to execute TRO read or write are shown in flow chart form on Figure 27.

	7000	Order	1410	Address Compare HA1	Address Compare HA2	Address Compare Record Address	Read or Write Data to System HA1	Read or Write Data to System HA2	Read or Write Data to System Record Address	Read or Write Data to System Record
Prepare to Verify Orders — Read or Write	88	TRO	6	yes	yes	no	no	no	yes	yes
	84	TWA	2	yes	yes	no	no	no	no	yes
	85	CYL	@	yes*	yes*	no	no	no	no	yes
	82	SRO	1	no	no	yes	no	no	no	yes
	89	HAO	5	yes	no	no	no	yes	yes	yes
	89	HAO-CE	5	no	no	no	yes	Read-Yes Write-see Note ✱	Read-Yes Write-see Note ✱	Read-Yes Write-see Note ✱
Prepare to Verify Orders — Write Only	83	Wr FMT	7	yes	no	no	Entire Format Track			
	86	Wr Ch	3	Same as operation being write checked						
Miscellaneous Orders	80	Seek	0	Position the access to a particular cylinder						
	04	Rel	9	On shared system the file control is released						
	09	6-Bit	M	Set 6-bit Mode						
	08	8-Bit	L	Set 8-bit Mode						
	00	No-Op	Q/V	No operation (1410 has special use)						
	87	In-Op	8	Sets selected access in-op						
	⊠	PSC	4	Used on models 3 or 5 in 1410 with priority feature						

* On first track only.

✱ Note: 7631 writes all bits if flagging the track; if not flagging, write data are written on remainder of track

Figure 26. 7631 Cycles Chart

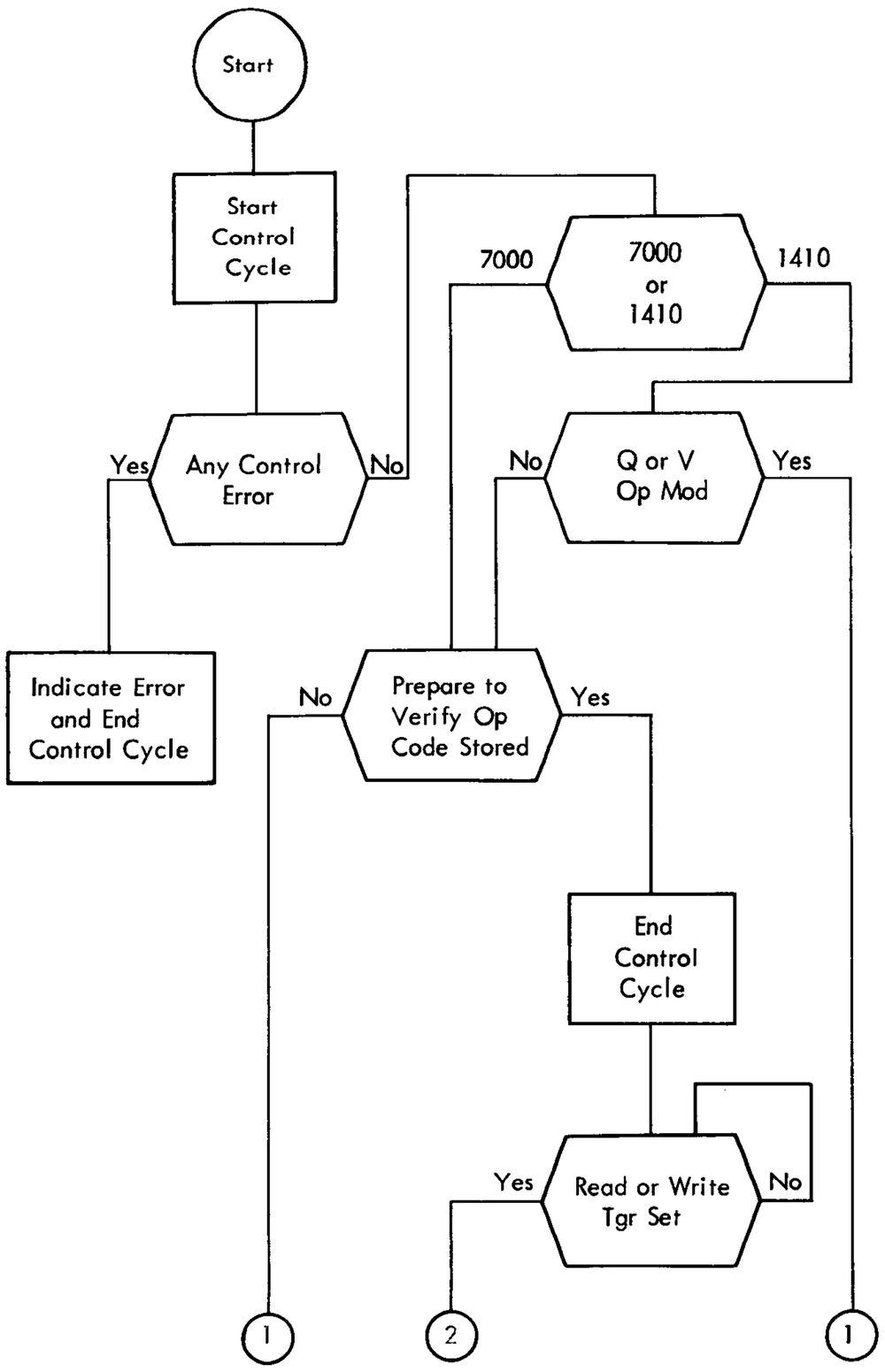


Figure 27. (Sheet 1 of 4). Instruction Flow Chart

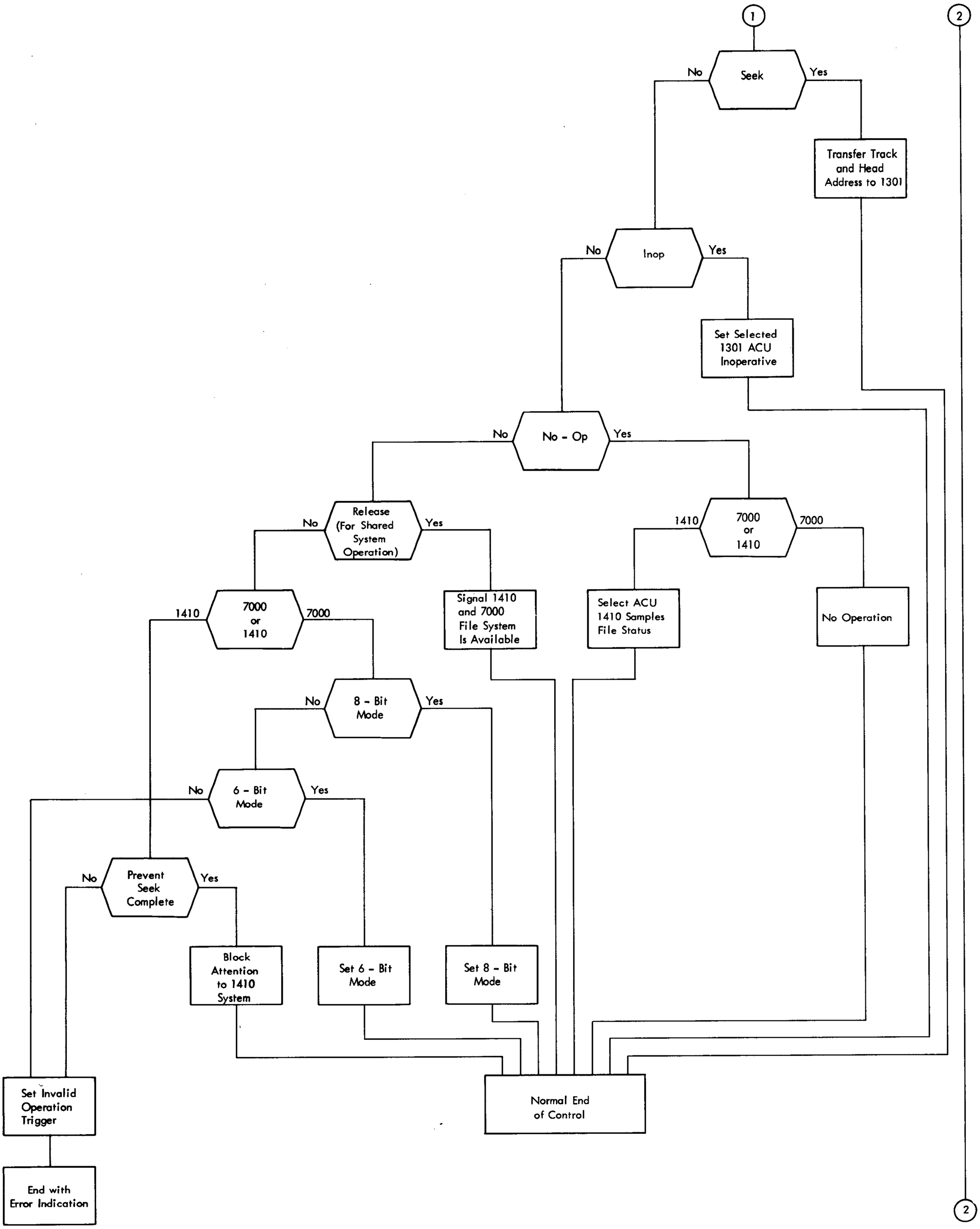


Figure 27. (Sheet 2 of 4). Instruction Flow Chart

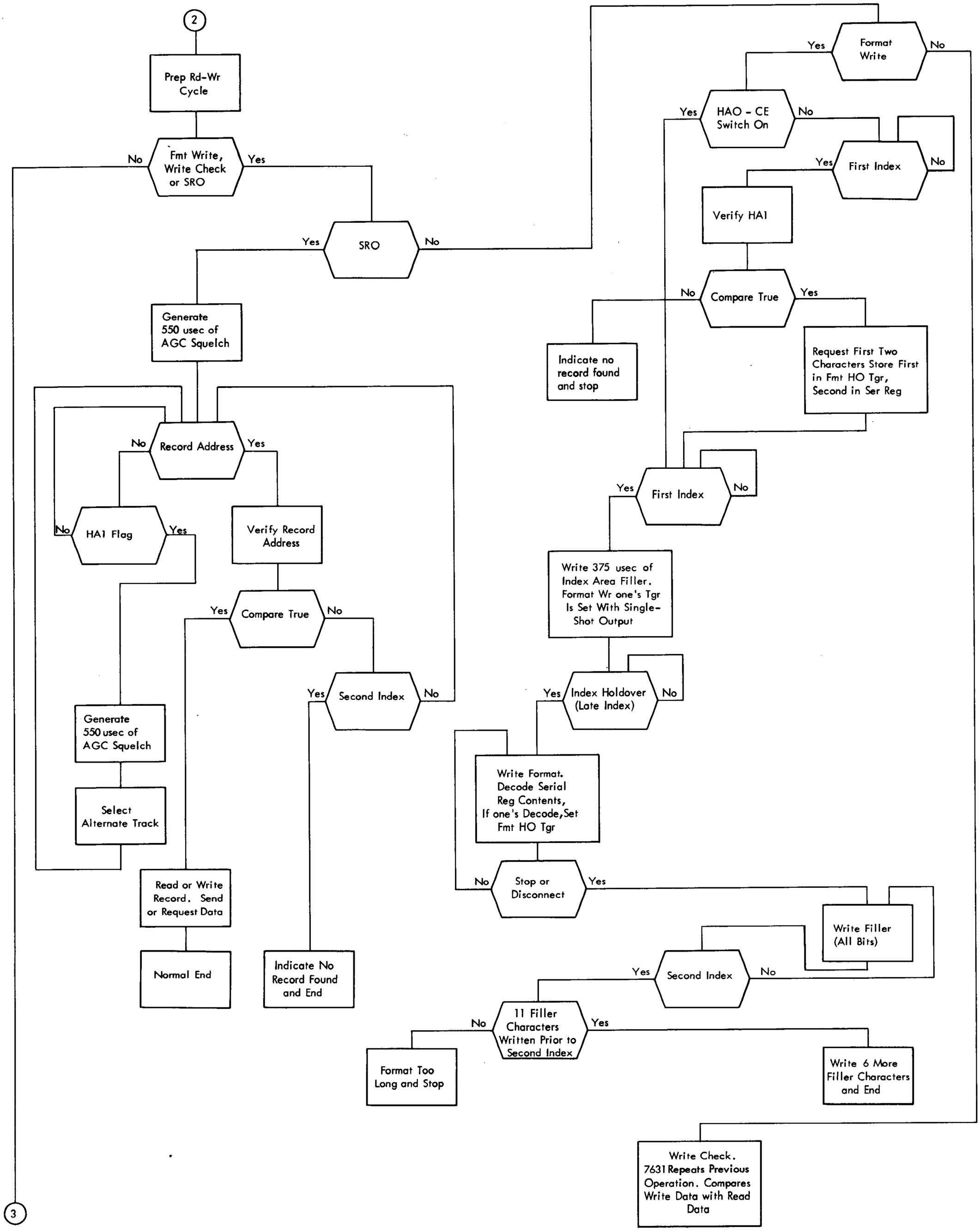


Figure 27. (Sheet 3 of 4). Instruction Flow Chart

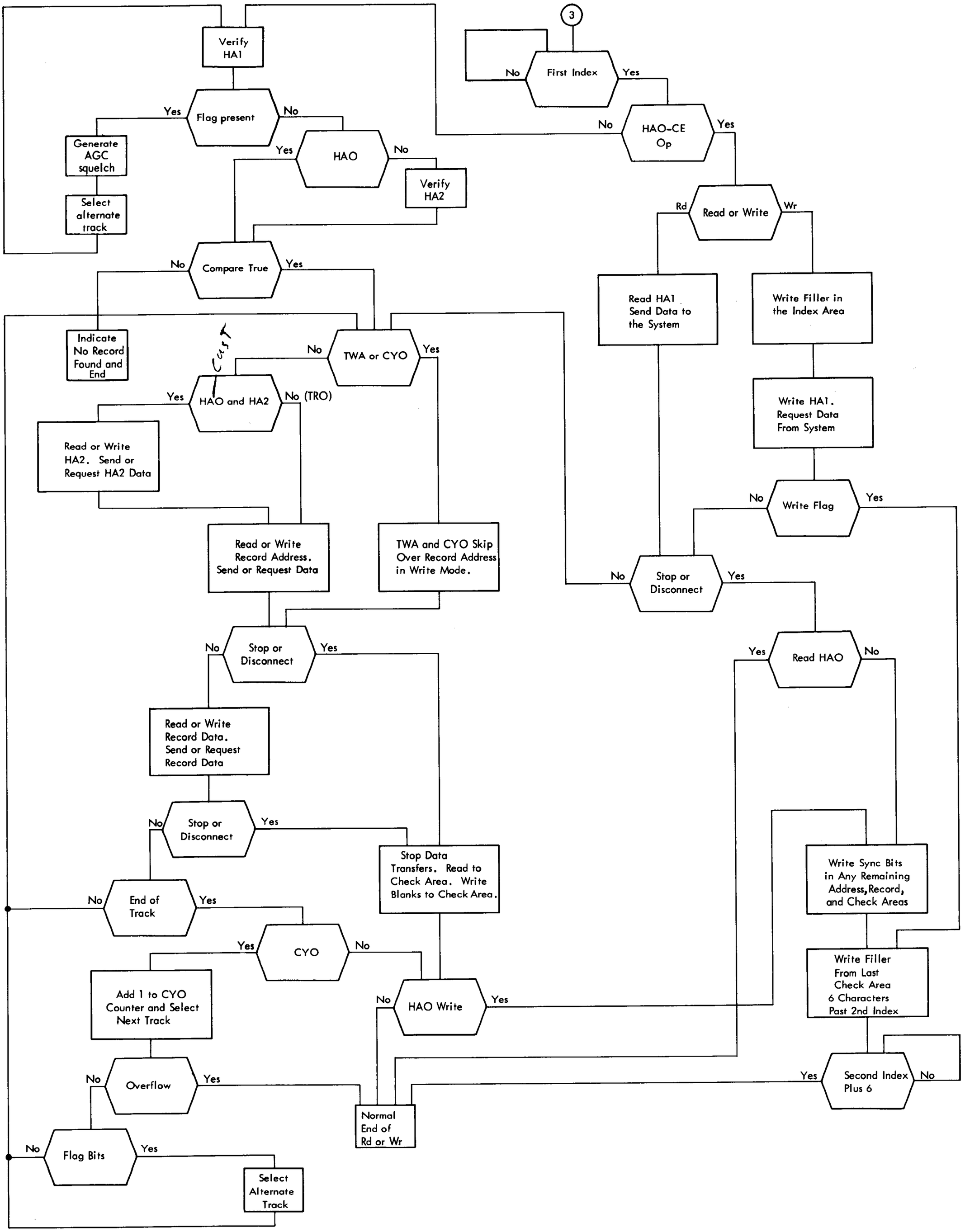


Figure 27. (Sheet 4 of 4). Instruction Flow Chart

TWA (Track Without Address)

- **Control cycle—set TWA op code and address register.**
- **Prep R/W cycle.**
- **Verify address cycle—compare HA1 with track register and HA2 with RR register.**
- **Read or write data cycle—transfer record data between system and 1301.**
- **End TWA at end of track.**
- **If system sends stop, end TWA at end of the record area.**

The operation codes for TWA are:
84 for 7000 systems
2 for 1410 systems

The basic cycles required to execute TWA are:
Control—prepare to verify TWA
Prep rd-wr
Verify address
Read or write data

After a successfully completed control cycle, receipt of the read or write signal starts the prep rd-wr cycle. The TWA operation occurs as outlined in Figure 26 after a successful prep rd-wr cycle. The TWA verify address cycle verifies HA1 and HA2; the TWA home address verify cycle is identical to TRO. If HA1 and HA2 compare true, the read or write operation begins with the first record area and continues to process the remaining records until the computer signals a stop or physical end of the track is sensed. Record address data is not processed during TWA write; record address data is not read or transferred from record address areas during TWA read. The basic cycles required to execute TWA read or write operations are shown in flow chart form in Figure 27.

CYO (Cylinder Operation)

- **Operation codes: 85 for 7000 systems, @ for 1410 systems.**
- **Control cycle—set CYO op code and address register.**
- **Prep R/W cycle—check for head 39.**
- **Verify address cycle—compare HA1 with track register and HA2 with RR register on addressed track only.**
- **Read or write data cycle—transfer record data from addressed track and following tracks in cylinder.**
- **End CYO at end of cylinder (end of track on head 39).**
- **If system sends stop—end CYO at end of record area.**

The operation codes for CYO are:
85 for 7000 systems
@ for 1410 systems
The basic cycles used to execute CYO are:
Control—prepare to verify CYO
Prep rd-wr
Verify address
Read or write data

Cylinder operation (optional feature) causes TWA type of operation to process a cylinder of 40 tracks in a sequential manner. The CYO read or write operation can be started on any track within the cylinder and continues to the end of the cylinder rather than the end of the track. The record areas of one or up to the full cylinder of 40 tracks are processed with the one CYO operation.

After the control and prep rd-wr cycles complete successfully, the 7631 executes the address compare cycle. (Figure 26 outlines the CYO sequence.) HA1 and HA2 are verified only on the addressed track; the re-

maining track addresses are not verified. The CYO verify address cycle is identical to TRO. If HA1 and HA2 for the addressed track compare true, the read or write operation starts with the first record area on the addressed track. All following record areas are processed until a stop is issued by the computer or end of cylinder is sensed by the 7631.

Each time end of track is sensed, the starting address stored in the track portion of the address register is incremented by one. The incremented address is transferred to the file to select the head of the next higher track in the cylinder. If the computer does not signal stop, the 7631 continues to process each record on the selected track and steps to the next higher numbered track until the cylinder end is recognized. End of track with head 39 selected causes overflow; overflow conditions the 7631 to end CYO operation. Data in HA1, HA2 and record address areas are not written during CYO write. HA1, HA2 and record address areas are not transferred to the system during CYO-read. The basic cycles required to execute CYO read or write are shown in flow chart form in Figure 27.

SRO (Single Record Operation)

- **Control cycle—set SRO op code and address register.**
- **Prep R/W cycle.**
- **Verify address cycle—compare record addresses with track and RR register.**
- **Read or write data cycle—transfer the record data associated with record address.**
- **End SRO at end of record data transfer after compare true.**

The operation codes for SRO are:

82 for 7000 systems
1 for 1410 systems

The basic cycles required to execute SRO are:

Control—prepare to verify SRO
Prep rd-wr
Verify address
Read or write data

SRO allows random access to a specified record located anywhere on the selected track. After a successfully completed control cycle the read or write signal causes the prep rd-wr cycle to start. Because SRO is not started with index, the 7631 generates a 350-microsecond AGC squelch signal plus a 200-microsecond delay. The 200-microsecond delay conditions the 1301 read amplifier before starting the verify address cycle. (Operations such as TRO, TWA, CYO, etc., started with index use AGC squelch between early and late index to condition the 1301 read amplifiers prior to the verify address cycle.)

Each record address on the track is compared with the contents of the track and random record portion of the 7631 address register. A total of six address characters are stored in the 7631; therefore, the track's record addresses must contain at least six characters, the minimum length record address. When compare true occurs, the 7631 processes only the following record area and ends the operation.

Because record addresses are not related to the home address, the 7631 track and random record registers contents (a record address stored during the control prepare to verify SRO cycle) cannot be used to select a head during SRO read or write. Head selection is inhibited for SRO operation so that the address transferred to 1301 track and head register during the previous operation remains unchanged by the control prepare to verify SRO operation. The contents of the 1301 track and head register, loaded during the previous control and since unchanged, determine the head number used for SRO read or write.

HA1 and HA2 are not verified during SRO read (Figure 26). Data is not written or read by the system in either HA1, HA2, or record address areas during SRO write.

Second index during SRO operation causes the 7631 to stop and indicate no record found. If second index occurs no record found is indicated, because all record addresses have been compared, enough time has elapsed to permit a normal SRO operation to complete and prevent no record found at second index. The basic cycles required to execute SRO read or write are shown in flow chart form in Figure 27.

HAO (Home Address Operation—Customer)

- **Control cycle—set HAO op code and address register (customer HAO switch on).**
- **Prep R/W cycle.**
- **Verify address cycle—compare HA1 with track register.**
- **Read or write data cycle—transfer HA2, record address and record data between system and 1301.**
- **Read HAO does not use format track to define data areas and ends at index.**
- **Write HAO will write entire track and if system sends stop, will write blanks for remainder of track.**

HAO (Home Address Operation—CE)

- **Control cycle—set HAO op code and address register (customer and CE HAO switches on).**
- **Prep R/W cycle—test RR0 register for flag bits and set 1301 flag latches if present.**
- **Read or write data cycle—transfer HA1, HA2, record address and record data between system and 1301.**
- **Read HAO does not use format track to define data areas and ends at index.**
- **Write HAO will write entire track and if system sends stop, will write blanks for remainder of track.**
- **Flag character (BCD 1, 2 or 4 bit) written causes filler to be written after HA1 for remainder of track.**

The operation codes for HAO are:

89 for 7000 systems

5 for 1410 systems

Two types of home address operation are possible with the use of two HAO switches. One HAO switch is mounted on the 7631 operator's panel and the other HAO switch is mounted on the 7631 CE panel. The two HAO operations are:

1. HAO customer operation, when the operator panel switch is on and the CE panel HAO switch is off.
2. HAO CE operation, when both HAO switches are on.

The basic cycles required to execute HAO customer are:

Control—prepare to verify HAO (with operator panel HAO switch on)

Prep rd-wr

Verify address

Read or write data

After a successfully completed control cycle, the read or write signal starts the prep rd-wr cycle. After a successful prep rd-wr cycle, the HAO customer operation occurs as outlined in Figure 26. The HAO customer operation verifies HA1 comparison, the 7631 is prepared to read or write HA2, record addresses, and records.

When reading, the HAO customer operation does not use the format track signals to identify the various data track areas. Because the end of the track cannot be identified with the format track signals, second index (index sensed a second time) is used to end the HAO customer read operation, if the computer does not send stop.

When writing, HA2, record addresses, and records are written; the write areas are identified with format track signals. If the system sends stop before the end of the track is sensed, write data transfers from the system are stopped. Following stop, the 7631 writes blank characters (a sync bit followed by no bits is a blank character) to fill the remaining formatted areas. Adjacent to the last formatted area, a record area, the 7631 writes filler (all one-bit characters) six characters past second index to complete the HAO customer write operation. (The basic cycles required to execute HAO cus-

tomer read or write are shown in flow chart form in Figure 27.)

The basic cycles required to execute HAO CE are:

Control—prepare to verify HAO (with both HAO switches on)

Prep rd-wr

Read or write data

After successfully completed control cycles, the read or write signal starts the prep rd-wr cycle; the HAO CE operation forces the compare true condition during the prep rd-wr cycle. (Figure 15 shows compare true is forced. Figure 26 outlines the HAO CE operation that follows a successful prep rd-wr cycle.) The verify address cycle is bypassed and the 7631 is conditioned to read or write HA1, HA2, record address, and record areas.

When reading, the HAO CE operation does not use the format track signals to identify the various data track areas, so that the end of the track cannot be sensed by identifying the format track not long gap signal. Second index (first index sensed a second time) is used to end the HAO CE operation if the system does not send a stop.

When writing, HA1, HA2, record address, and record areas are written, and the write areas are identified with format track signals. If the system sends a stop before the track end is sensed, system write data transfers are stopped. Following a stop, the 7631 writes blank characters (a bit sync followed by no bits is a blank character) to fill the remaining formatted areas. If the flag character (the fifth home address character) is other than a blank or a BCD eight, the track is flagged. Writing a flag causes the 7631 to write all one bits (filler), starting with the HA2 area up to six characters after second index; as a result, HA2, record address, and record data are destroyed. (The basic cycles required to execute HAO CE operation are shown in flow chart form in Figure 27.)

During an HAO CE read or write prepare to read-write cycle, the contents of random record register R0 are transferred to the serial register. If flag bits are present, the read or write data transfers following are switched to the selected alternate track.

Wr Format (Write Format)

- **Control cycle—set wr format op code and address register (1301 format switch to write).**
- **Prep R/W cycle—if HAO-CE switch is on, compare true is forced to bypass the verify address cycle.**
- **Address verify cycle—compare HA1 of addressed data track to track register.**
- **Write data cycle—decode system write data and write on format track.**
- **End wr format at index.**

The operation codes for write format are:

83 for 7000 systems

7 for 1410 systems

The basic cycles required to execute wr format are:

Control—prepare to write format (with the 1301 format switch in the write position)

Prep rd-wr

Verify address (if HAO CE switch is off)

Write data (read causes invalid sequence)

After successfully completed control cycles the write signal causes a prep rd-wr cycle to start. If the HAO CE switch is on (this causes the operation to bypass the verify address cycle), the prep rd-wr cycle timing gates the first two write characters from the system into storage. (See Figure 19, item 13.) If the HAO CE switch is off, the 7631 executes the prep rd-wr cycle without gating write data into storage.

If a verify address cycle is required (the HAO CE switch is off), HA1 is verified. The home address verified is selected by the address stored during the control-prepare to write format cycle. Any track within the cylinder can be selected to verify address, because the verify cycle is only needed to insure the correct cylinder selection. After HA1 check characters are processed, the 7631 gates the first two write characters into storage. Format write data from the system can only be a BCD one, two, three, or four; any other character causes an error stop. Write data is decoded in the 7631 to determine if a no-bit or all-bits character is to be written in either six-bit or eight-bit mode. The write character

transferred and its effects on 7631 writing are shown in the following table.

WRITE DATA FROM SYSTEM	7631 BIT-MODE	CHARACTER WRITTEN ON 1301
BCD 1	6	all bits
BCD 2	6	no bits
BCD 3	8	all bits
BCD 4	8	no bits

The BCD characters transferred from the system are decoded. (The control decoder circuits, Figure 16, normally used for 7000 order decoding are also used to decode format write data.) For example, if a BCD one is decoded, the control decoder output sets the 7631 to six-bit mode and sets the format holdover trigger. When the format write ones trigger is set, the 7631 writes an all-bits character. If a BCD four is decoded, the control decoder output sets the 7631 to eight-bit mode and resets the format holdover trigger; the 7631 writes no bits.

Receipt of early index causes the 7631 to generate and write 350 μs of filler (all-bits characters) between early and late index. With the 1301 format write switch in the write position, a write path is provided from the 7631 to the 1301 format write head regardless of the head selection specified. Starting with late index, the 7631 gates the format holdover trigger output (decoded write data from the system) to write the format track. Data is transferred from the system, decoded, and written until the complete format track data image stored in the computer is processed. The system must send stop at least 11 characters prior to second index. The 7631 error circuits are designed to detect format too long and indicate an error if the system stop is not received at least 11 characters prior to second index.

Following the last format character (always one no-bits character) written by the system, the 7631 writes filler (all-bits) six characters past second index to complete the format write operation. (The basic cycles required to write format are shown in flow chart form in Figure 27.)

When the user plans a format track certain invariable rules must be followed. (Use Figure 11 for a detailed reference.)

1. The area from late index to the end of the HA1 check area must be written in eight-bit mode. Beginning with HA2, the user can choose either six- or eight-bit mode for the remainder of the track; however, the mode chosen for HA2 must be maintained to the end of the format track.

2. All format check areas must be 12 characters long. For example, HA1 check area is composed of two one-character gaps and ten characters of filler for a total of 12. HA2 check area is also 12 characters long as are the record address and record check areas. These areas must be 12 characters long so that the gap following the check characters on the data track will be six characters long.

3. On the format track, the user must always write address and record areas, including HA1 and HA2, that are four characters longer than the address or record to be written on the data track. For example, HA1 is always five characters long on the data track, so the format for HA1 must always be nine (5 + 4) characters long. HA2 must be at least two characters long on the data track, so the format for HA2 must be at least six (2 + 4) characters long. Record addresses must be at least six characters long on the data track, so record address format must be at least ten (6 + 4) characters long. The four extra characters written in the format areas insure that the data track has a nominal length of six characters. This prevents partial erasure of data on write operations.

4. The area from late index to HA1 must always consist of three characters of eight-bit mode no-bits.

5. The user must end the format at least 11 characters before early index with a programmed short gap after the last record area. This allows space to process the check characters of the last data track record area before early index.

Write Check

- **Control cycle—sets wr check op code and address register but does not reset previous operation code.**
- **Write check executes the same basic cycles as the prepare to verify order as it is write-checked.**
- **Compare system write data to 1301 read data serially by bit in compare circuit.**
- **Indicate write check error if compare fail occurs.**

The operation codes for write check are:

86 for 7000 systems

3 for 1410 systems

The basic cycles required to write check are:
Control—prepare to write check
Prep rd-wr
Verify address (when required)
Write data

The write check operation is used to verify any 7631 write operation. For example, if control-prepare to write check and the write signal are issued to the 7631 following a TRO operation, the 7631 repeats the TRO operation. The first cycle executed after control is prep rd-wr; the next cycle executed is verify address.

Following a successful TRO verify address cycle, the 7631 requests write data from the system and compares the write data with read data from the selected track. The write data transferred from the system is not written on the 1301, but write data is processed in the 7631 as if a TRO write operation was in progress. While the 7631 is processing the write data from the system, the 7631 operates on the selected 1301 track in read mode. Read data from the 1301 and write data from the system are synchronized by the 7631 and compared bit by bit to verify the data stored on the track in the previous TRO-write operation. Any single bit compare failure causes the 7631 to indicate a data failure. Essentially the 7631 performs in write mode with respect to the system and in read mode with respect to the 1301.

Because format read cannot be executed, format read causes an invalid sequence. Write check and write issued to the 7631 following a format write operation is the only means of verifying the format data written on the 1301.

Miscellaneous Instruction Operations

- **Miscellaneous orders cannot be followed by a read or write operation.**
- **Misc orders always end the file operation during or at end of control cycle.**

Seek (1410 and 7000)

- **Control cycle—set seek op code and address register.**
- **Gate track register to selected 1301 access register.**
- **End seek at end of control cycle.**
- **1301 will indicate attention (seek complete) at completion of mechanical movement.**

The seek operation codes are (Figure 26):

80 for 7000 systems

0 for 1410 systems

The 7631 stores and executes seek during a control cycle. During control-seek, the 7631 stores the seek operation code and eight address digits in the 7631 address register. The first two stored address digits are used to select the 1301 access and module; the next four digits, track and head, are transferred from the 7631 track and head register to the selected 1301 access register. (See Figure 16.)

The set access register signal gates four digits, track and head, to the selected access and module causing the 1301 to seek. When the 1301 has positioned the access mechanism, an attention signal is issued to set the 7631 attention trigger. Attention is passed from the 7631 to the system indicating that the access mechanism is in position and prepared for operation. If a seek is issued to a 1301 access mechanism that is in motion (seeking because of a previous seek operation), the 1301 indicates not ready.

A 7000 system may issue sense and analyze the sense data received from the 7631 to determine the origin (access and module) of the attention signal.

Release (7631 Models 3, 4, and 5)

- **Control cycle—sets release op code but does not gate address data.**
- **Used on models III, IV or V which share a file control between two systems.**
- **A system gains and maintains control of the 7631 by initiating a file operation.**
- **The using system must then release the file control which allows both systems to be available again.**
- **End release at completion of control cycle.**

The release operation codes are (Figure 26):

04 for 7000 systems

9 for 1410 systems

The release operation code is transferred to the 7631 during a control operation (Figure 27). Address information is not needed to execute release. The 7000 systems do not transfer address data to the 7631 during the control-release operation. The 1410 B-address should address a ≢.

The 7631 file control models 3, 4, and 5 permit two different data processing systems to share a common disk storage system. These models have three-way switching circuits as shown in Figure 28.

When the switch is in the neutral position (as shown), the first system to issue an order (instruction, if a 1410, 7010, or 7080) to the file control takes control of the 7631 and the attached 1301's. Control is retained until the controlling system issues release, restoring the switch to neutral. Assume System A has control of the 7631.

1. If System B is a 1410 or 7010 and tries to issue a disk storage instruction, the 1410 or 7010 receives a busy indication.
2. If System B is a 7090 and tries to issue a disk storage order, a channel interrupt results.
3. If System B is a 7080 and tries to issue a disk storage order, but does not use a transfer ready instruction (TRS01) before issuing the order, the channel will wait until the 7631 is available.
4. If System B is a 7070 or 7074 and tries to issue a disk storage order, the 7907 data channel waits for System A to release the file control. The 7070 or 7074 computer does not have to wait for the data channel and can continue data processing.
5. If System B is a 7040 or 7044 and tries to issue a disk storage order, the 7904 data channel and the computer wait for System A to release the file control.

The release operation code is not effective on 7631 model 1 or 2, but circuits are included in 7631 models 1 and 2 to accept the release instruction; this permits a program written for shared system operation to be used on a 7631 model 1 or 2 without causing an invalid op code error.

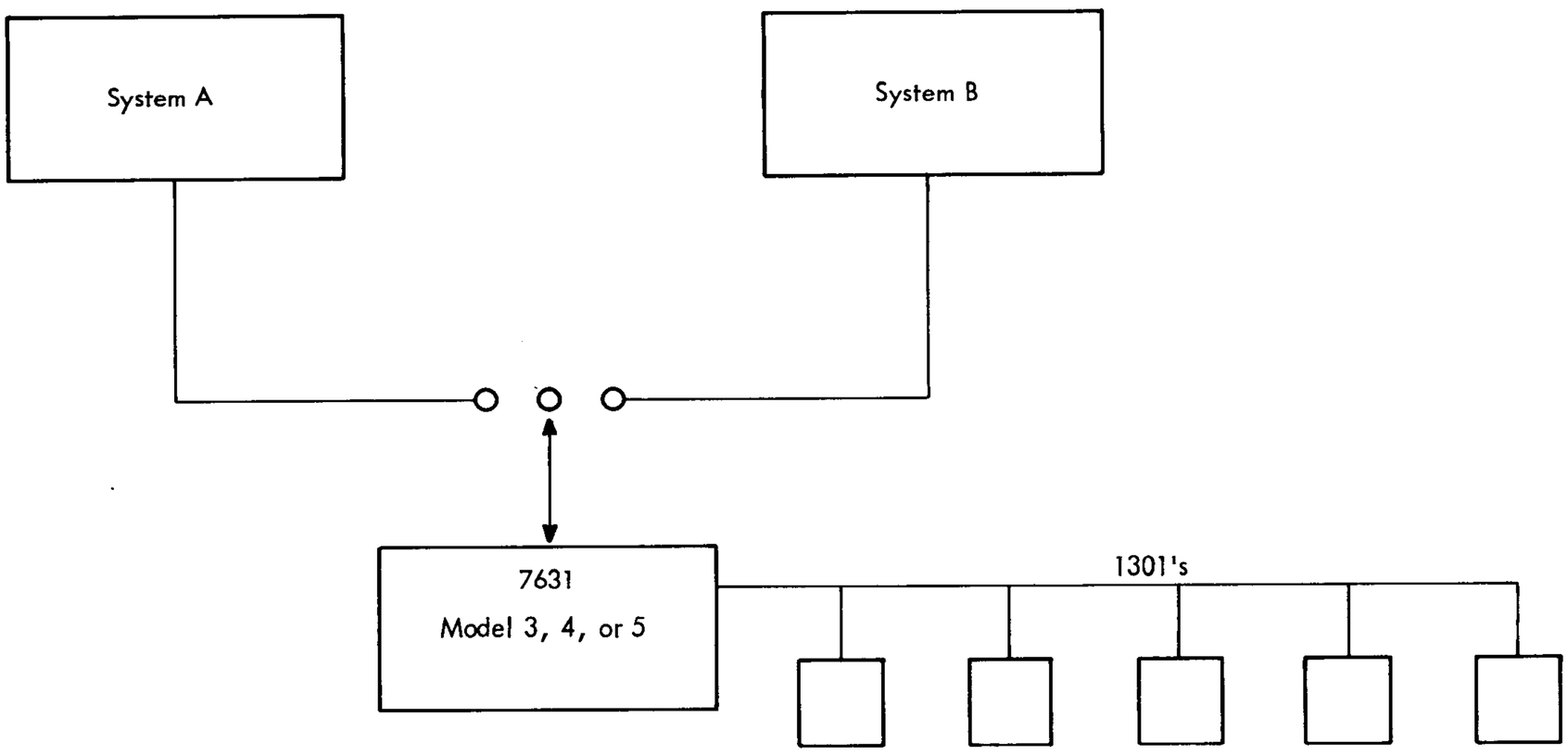


Figure 28. Shared System Three-way Switch

No-Op (1410 and 7000)

7000:
- **Control cycle—sets no-op code but does not gate address data.**
- **Programming convenience only, does not perform any function.**
- **End no-op at completion of control cycle.**

1410:
- **Control cycle—sets appropriate op code, gates address data and activates seek interface line.**
- **Does not perform a seek and cannot be followed by a read or write operation.**
- **Used to test status of files on 1410 with priority feature.**
- **End no-op at completion of control cycle.**

The operation codes for no-op are (Figure 26):
00 for 7000 systems
Any operation code with a Q or V op-modifier for 1410 systems

The 7631 stores and executes a 7000 no-op order during a control cycle (Figure 27). The operation requires that the 7000 system issues a two-digit operation code. (No address digits are required.) The order when issued by a 7000 system is accepted by the 7631 as a programming convenience only. No function is performed by the 7631 for this order.

In 1410 operation, a Q or V op-modifier causes the 7631 to end op following the control cycle. The first two characters, access and module, are needed to execute no-op; the remaining six characters can be any valid characters because they are not used by the 7631.

The primary use of this instruction for a 1410 with priority feature is to set the I-O channel status indicators for the selected I-O unit, so that the status of the unit can be tested by a branch if I-O channel status indicator instruction—R(I)d or X(I)d. For example, assume that seek instructions have been issued to several 1301 access mechanisms. The first access mechanism to reach its destination will cause an interrupt to the 1410 system. Once the program determines that the interrupt was caused by completion of a seek, the particular mechanism which caused the interrupt can be determined by:

1. Using the I-O NOP instruction to set the status indicators for each mechanism to which an order was issued.

2. Testing the I-O busy indicator for a busy condition by means of the R(I)d instruction. If the access mechanism is not in motion, a busy condition will not result (seek is complete) and it can be assumed that the access mechanism addressed is the one that caused the interrupt.

If the I-O NOP instruction is being used to set the I-O channel status indicators, the op code may be M or L, the units position of the X-control field can be any valid character, the HA1 and HA2 areas of the disk address word can be any valid characters, and the d-character can be either Q or V.

The I-O NOP instruction can also be used to set the mode of operation (single record, track, or cylinder) for a succeeding write check operation. In this case, the units position of the X-control field of the instruction must indicate the type of write check operation to be performed.

3. For seek orders, the cylinder portion of the 7631 access register is not gated to the 1301 if the op-modifier is Q or V.

Inop (1410 and 7000)

- **Control cycle—set in-op op code and address register.**
- **Set selected access off-line by picking 1301 in-op relay.**
- **End in-op at completion of control cycle.**

The operation codes for inop are (Figure 26):
87 for 7000 systems
8 for 1410 systems

The inop code is transferred to the 7631 during a control operation (Figure 27). Two address characters, access and module, are needed to execute inop. The re-

maining six address characters transferred can be any valid characters because they are not used. The file control issues set access inoperative to the selected 1301 access mechanism. The selected access is set inoperative until the 1301 is serviced. The next system to select the inoperative access detects the inoperative condition and the operation terminates with an access inop error indicated.

Prevent Seek Complete (1410)

- **Control cycle—sets PSC (prevent seek complete) op code but does not gate address data.**
- **Used to block interrupts from file seek complete signals to 1410 (if priority feature is used).**
- **Reset by next seek order.**
- **End PSC at completion of control cycle.**

The operation code for prevent seek complete is "4" (Figure 26). The prevent seek complete code is transferred to the 7631 during a control operation (Figure 27). The address data transferred is not needed to execute prevent seek complete; therefore, the B address must address a group mark with a word mark.

~~This instruction is effective only on the 7631 models 3 and 5 (shared system operation)~~. It is used to prevent seek complete interrupts to the 1410 system (equipped with the priority feature) caused by seek operations of the sharing system. The instruction turns on a latch that blocks seek-complete signals from the 1411 caused by the sharing system. The 1410 that issued the prevent seek complete resets the latch when it issues a seek instruction.

Although the prevent seek complete order is not effective on a 7631 model 1, it can be decoded to prevent an invalid op code error when a program written for model 3 or 5 is used with a model 1.

Eight-Bit Mode (7000)

- **Control cycle—sets 8 bit mode in file control but does not gate any address data.**
- **All following file operations operate in 8-bit mode.**
- **End 8 bit mode operation by setting 6 bit mode, or release on Models 3 or 4.**
- **End this order at completion of control cycle.**

The order code for eight-bit mode is 08 (Figure 26). The eight-bit mode order code is transferred to the 7631 during a control operation (Figure 27). No address data is needed or transferred; only the two-digit order code is transferred to the 7631.

The order conditions the 7631 bit ring to operate in eight-bit mode. This mode of operation is required when the using system is operating in the packed mode. (Packed mode is the packing of two numeric digits into one eight-bit character.) The normal data rate of the file control in the eight-bit mode is 70,100 characters per second with a maximum of 2,165 data characters for data track capacity. When using packed format, however, data rate is 140,200 digits per second with a maximum of 4,330 digits for a data track capacity.

Six-Bit Mode (7000)

- **Control cycle—sets 6 bit mode in file control but does not gate any address data.**
- **All following operations operate in 6 bit mode.**
- **End 6 bit mode operation by setting 8 bit mode or release on Models 3 or 4.**
- **End this order at completion of control cycle.**

The operation code for six-bit mode is 09 (Figure 26). The six-bit mode order is transferred to the 7631 during a control operation (Figure 27). No address data are transferred; only the two-digit order code is transferred to the 7631. The order conditions the file control bit to operate in the six-bit mode. The data rate for the file control when operating in the six-bit mode is 90,100 characters per second with a maximum track capacity of 2,800 characters.

Sense (7000)

- **Initiated by sense command.**
- **7631 transfers 10 bytes of sense data.**
- **Indicates error and attention status of 7631 and 1301 files.**

Receipt of the sense command signals the 7631 to start the timing circuits and transfer ten bytes of sense data. Because the sense operation does not require synchronization with the 1301, the oscillator pulses are used for the timing source. The sense command disables the immediate stop on error signal to allow all sense data to transfer without interruption. Beginning with DN the first service request is issued in order to transfer the first byte of sense data; odd parity is assigned to each byte of sense data transferred. Sense data transfers continue for each digit cycle until D10 prevents service requests and causes the 7631 to signal normal end to the data channel.

Timing Sources

- Use 625KC oscillator in 7631 or 625KC clock track signal from selected 1301 at 1.6 μs rate.
- Oscillator or clock signal develops selected phase signal.
- Selected phase drives the delay line pulse generator.
- Delay line pulse generator drives all timing circuits in 7631.

Two signal sources are used for 7631 timing. A 625 KC oscillator is used for control, sense, and prepare to read-write cycle timing, and the 1301 clock track signal is used for read and write timing. Either selected timing source is applied to the delay line pulse generator input via the selected phase line when delay line pulse generator timing is needed (Figure 29). The delay line pulse generator develops one complete cycle of output

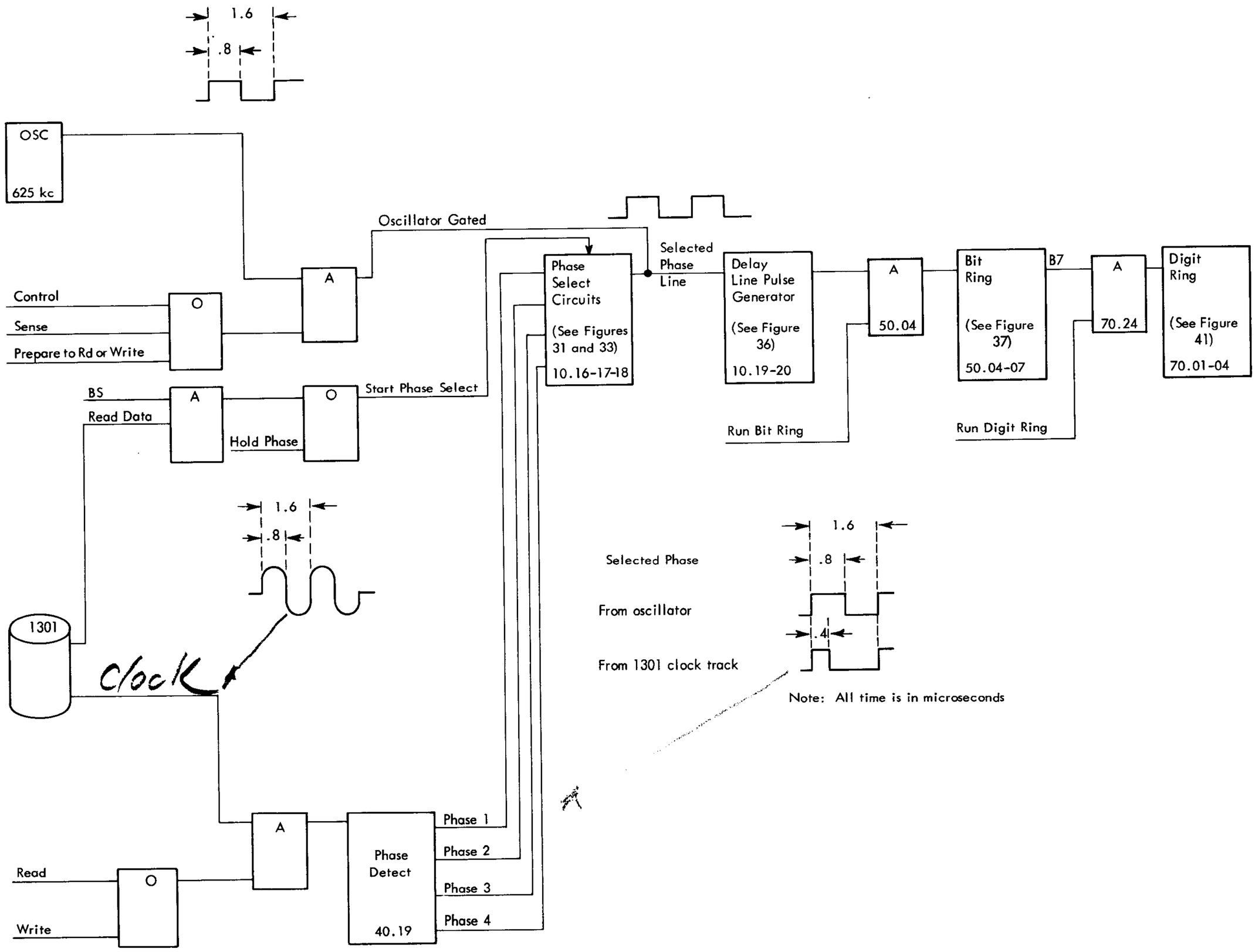


Figure 29. Timing Scheme

pulses for each selected phase input cycle. A second group of timing pulses, bit ring timings, are developed from one of the delay line pulse generator outputs. Finally, digit ring timing is developed from one of the bit ring outputs (Figure 29).

Oscillator or clock track timing is used for the selected phase. Selected phase is the input to the delay line pulse generator (Figure 30). The delay line pulse generator outputs are used to read and write data, operate the shift register, and to step bit ring. When digit ring timing is needed, bit ring timing is used to advance the digit ring. Digit ring timing is used to start all machine operations. Briefly, one complete cycle of the delay line pulse generator timing equals one bit time. One complete cycle of the bit ring equals one character time (depending on the machine bit mode, either seven or nine bit times); 13 bit ring cycles equal one complete digit ring cycle.

Phase Select Scheme

- **Use 1301 clock track signal when reading or writing on disk.**
- **Clock track signal develops selected phase in phase select circuits.**
- **Selected phase drives delay line pulse generator.**
- **Delay line drives bit ring which controls read or write data flow.**
- **7631 bit ring timing and read or write data flow must be synchronized.**

The phase select circuits provide timing pulses to the delay line pulse generator input. These fundamental bit timing signals, derived from either the clock track or the oscillator, are gated via the selected phase line to the delay line pulse generator (Figure 30). The delay line pulse generator outputs sample 1301 read data at the output of data trigger A, operate the shift register, sample write data going from the 7631 to 1301, and provide a precise sample for compare circuit operations.

One of the delay line pulse generator outputs is used to drive the bit ring. Bit ring outputs gate the output of data trigger B (read data) into the correct serial register storage position; this allows each read character to be correctly assembled before transferring the character to the system. Because the clock track signal is the timing source that advances the bit ring when reading, the bit ring outputs hold a critical time relationship to the read data bits; therefore, the clock track and read data must be synchronized. Loss of synchronization could cause the read data bits to be stored in the wrong serial register storage positions and cause data errors.

Read data and clock track signals require synchronization because the clock track and data heads are mounted on the ends of non-stable arms subject to vibration. The phase select circuits synchronize the read and clock track signals for reliable read operation. The phase select circuits have two different modes of operation: read mode and hold phase.

Read Mode

- **1301 clock signal is divided into four 400 nanosecond phases.**
- **When reading data, data bit S of every character selects a clock phase.**
- **The selected phase provides timing for that character in step with read data.**
- **Two phase select circuits (A and B) are used alternately to allow an earlier phase to be selected when reading, if necessary.**
- **Hold phase is used to operate phase select circuit when writing or reading and valid read data is not available.**
- **Hold phase selects any phase and holds it until hold phase is reset.**

Read and clock signal synchronization occurs when bit-sync is read from the data track. (Bit-sync is not part of the system write data, but is generated and written by the 7631 as the first bit of each character.) Bit-sync is the first bit of each read character; bit-sync is compared with the four 1301 clock phases to select

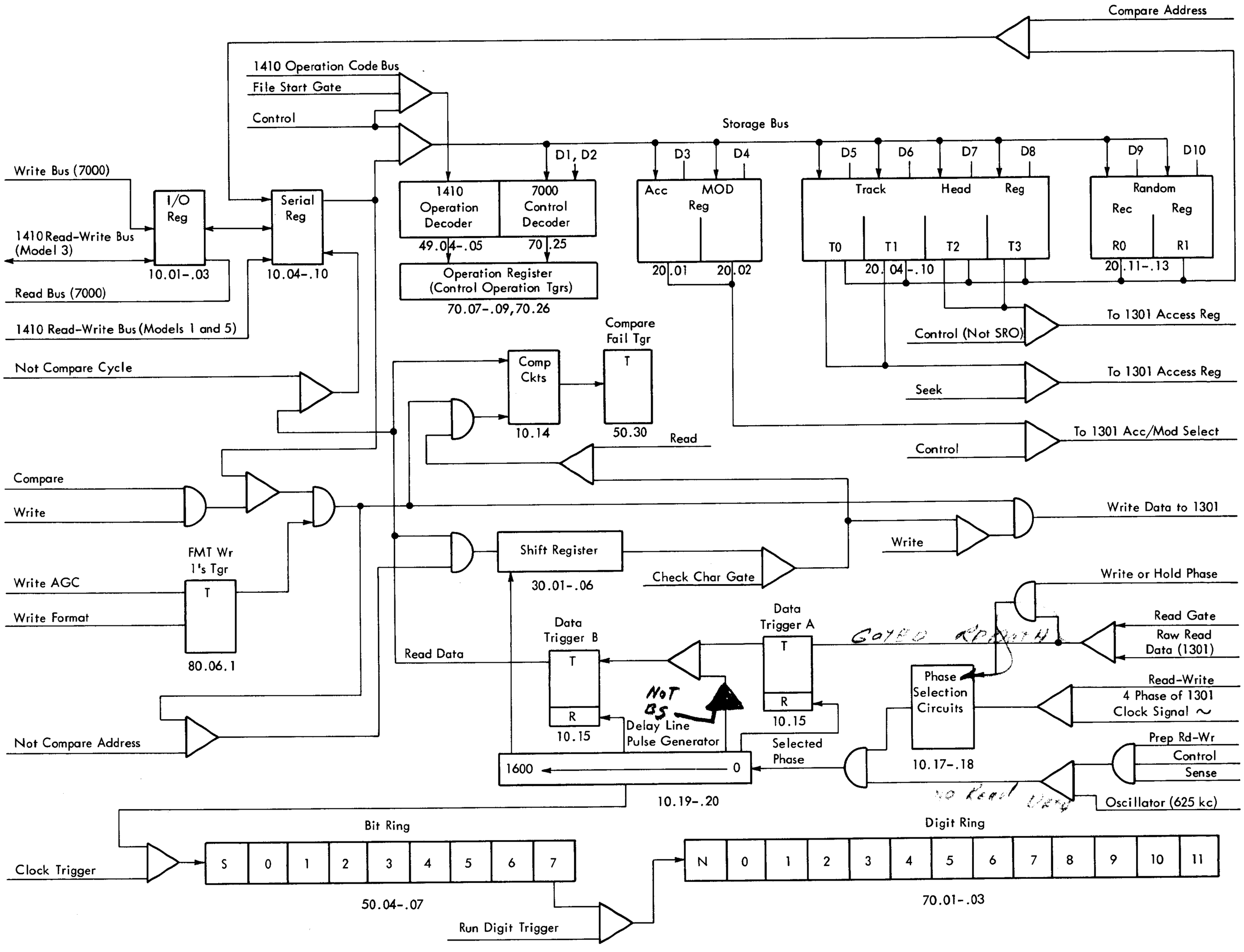


Figure 30. Data Flow Diagram

the comparing phase. The comparing phase, selected phase in ALD terms, is the delay line pulse generator input, and the delay line pulse generator and the bit ring outputs are synchronous with read data.

Each bit-sync is used to select the phase for the following read data bits to insure read synchronization. The phase select circuits are designed to compare and select a phase for every character read; however, it is improbable that head vibration and disk speed variations could cause a new phase selection more often than once every 60 characters. Because bit-sync is only needed for timing purposes and it is not part of system write data, bit-sync is never transferred to the system with a read data character.

Read Phase Select Operation

When reading data, the phase select circuits provide a selected phase input to the delay line pulse generator; the resultant delay line pulse generator outputs are used to sample data, operate the shift register, and drive the bit ring. Two identical phase selectors, phase selector A and B, are alternately used to select the delay line pulse generator input. Four phase selector gates control clock phase outputs 1 through 4 for each phase selector. The output gates are labeled $\phi 1$, $\phi 2$, $\phi 3$ and $\phi 4$ in Figure 31. The input clock phases are supplied by the phase detector (Figures 29 and 31). The phase detector divides each 1.6 microsecond clock track signal into four phases; each phase is 400 nanoseconds in duration (Figure 32). The 7631 must select one of the phases for each character read.

Phase selectors A and B are identical. (The following description refers to phase selector B shown on the lower half of Figure 31.) The output gates of phase selector B each have a different phase input; the output gates are controlled by the B select odd and B select even triggers. The B select odd and even triggers are set and reset with same four phase signals that are applied to the output gates. When the B odd and even triggers are continuously set and reset, a selected phase output cannot be obtained from phase selector B because the output gate conditioning signals cannot AND with the input phase signals. For example, if phase two ($\phi 2$) is the required selected phase, two simultaneous conditions must occur to gate phase two ($\phi 2$).

1. The B phase select odd trigger must be reset.
2. The B phase select even trigger must be reset.

If these two conditions remain unchanged, phase two ($\phi 2$) is gated to the delay line pulse generator via the selected phase line. Assume the input gates are also conditioned: Figure 31 shows the B select odd trigger has been set since the previous phase one ($\phi 1$) signal and the B select even is set when the phase two ($\phi 2$) arrives; these conditions not only prevent phase two ($\phi 2$) from getting on the selected phase line, but they are the inverse of the conditions needed to gate phase two. (See the B selector phase two ($\phi 2$) output gate shown in Figure 31.) This difference between phase timing and phase gating never changes; therefore, when the input gates are conditioned, the phase selector cannot supply a selected phase output.

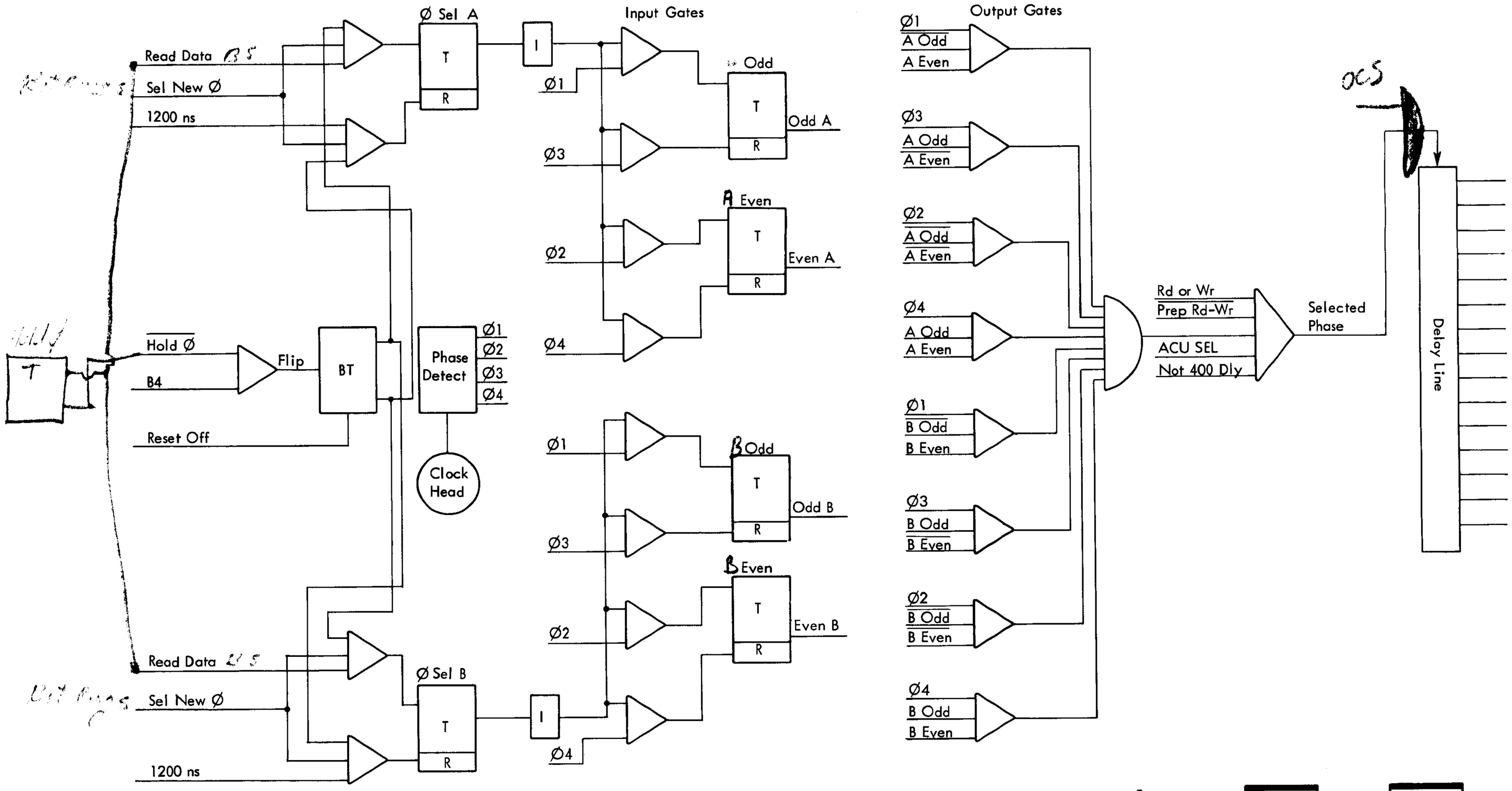
When phase one ($\phi 1$) is available, output phase gate $\phi 3$ is conditioned; similarly, when phase two is available, output phase gate $\phi 4$ is conditioned (Figure 31). The two-phase difference between input and output gating prevents a phase selection when phase select trigger B output conditions the input phase gates.

The conditioning signal must be removed from the input gates to stop the select odd and even triggers; stopping the select odd and even triggers gates one of the four phase signals to the selected phase line. (Figure 34 shows the condition of the select odd and even triggers required to gate each phase.) When set, phase select B trigger blocks the B selector input gates; therefore, phase select B trigger stops the B select odd and even triggers and permits output phase gating (a phase selection).

If the set pulse timing to the phase select B trigger is controlled, the selected phase can be controlled. For example, Figure 34 shows the select odd and even triggers are set at phase two time, and that the phase four ($\phi 4$) output gate is conditioned, so that phase four is selected. Because reading requires that the selected phase has a fixed timing relationship to the 1301 read data phase, the selected phase is applied to the delay line pulse generator input, and the data sample, the shift register, the bit ring, and digit ring timing (if digit timing is needed) are generated. Raw read signals from the 1301 are then sampled (converted to pulses) to determine if the data bits are ones or zeros.

To select the correct read phase signal, bit-sync (the first bit read), BS from the bit ring, and the binary trigger output AND; phase select B trigger sets (Figure 33). Phase select B trigger blocks the B selector input gates; the time the bit-sync arrives in relation to one of the four phases determines when the odd and even triggers stop. For example, if bit-sync is coincident with phase three, phase one is the selected phase. (Figure 34 shows the coincidence of bit-sync with each phase and the resultant selected phase output.) Selected phase one ($\phi 1$) drives the delay line pulse generator to sample data and drive the bit ring.

When the bit ring steps from B7 (the last output pulse) it returns to BS, the starting output. While reading the first character and stepping the bit ring, the binary trigger is flipped with the B4 bit ring output. The binary trigger conditions the phase select B trigger reset and the phase select A trigger set; these con-



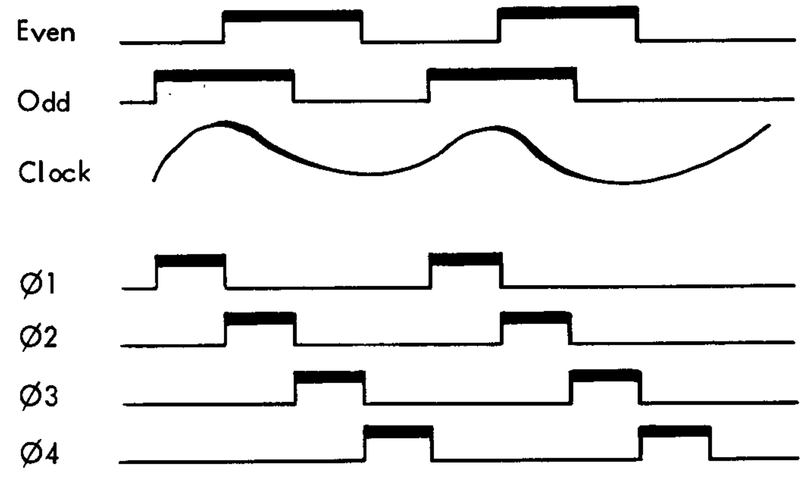


Figure 31. Phase Selector Circuits—Simplified

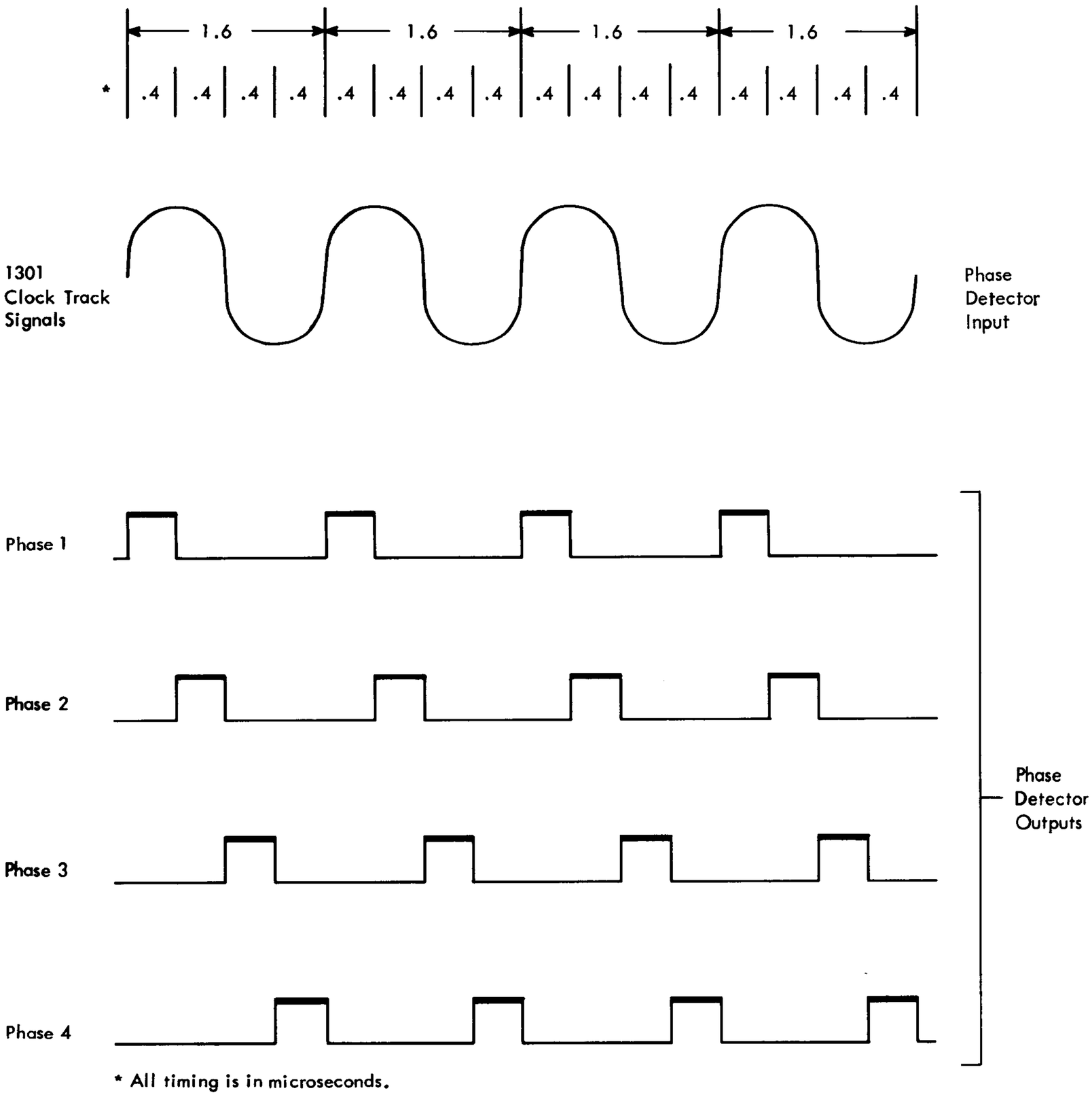


Figure 32. Phase Detector Inputs and Outputs

ditions gate the next bit sync to set phase select A trigger. When phase select A trigger is set, it provides a selected phase for the second character read from the 1301. (Phase selector A operates in the same manner as phase selector B for the next character cycle.) Phase select B trigger is reset with 1200 delayed (from the delay line pulse generator), gated with BS from the bit ring, and phase selector B stops operation. (In Figure 35, lines 1 through 13 show the read data timing sequence, and lines 10 and 11 show how read timing causes phase select A and B triggers to alternately set and reset.) Phase select A trigger is set while the first address character is read, then phase control is switched to phase select trigger B for the second address character. The phase select triggers alternate the phase selectors until the read data is processed.

Figure 35, line 7, shows when the read gate is on; the timing circuits operate in read mode when the read gate is on. Note that the D7 (line 13) digit ring output has greater duration than the D6 output. The gap preceding the last address data character is always written without a bit-sync, so that there are no read data bits to select phase. Because both phase select A and B triggers remain reset in the data gap, the read timing is suspended and, in this case, D7 is available for an extended time interval. Whenever both phase select A and B triggers are reset and the read gate is set, the phase selectors are conditioned to detect missing sync. (See the AND circuit between phase selectors A and B on Figure 33.) The missing sync detection AND circuit output is used to prepare the 7631 to process the check characters read immediately after the last address or record data character.

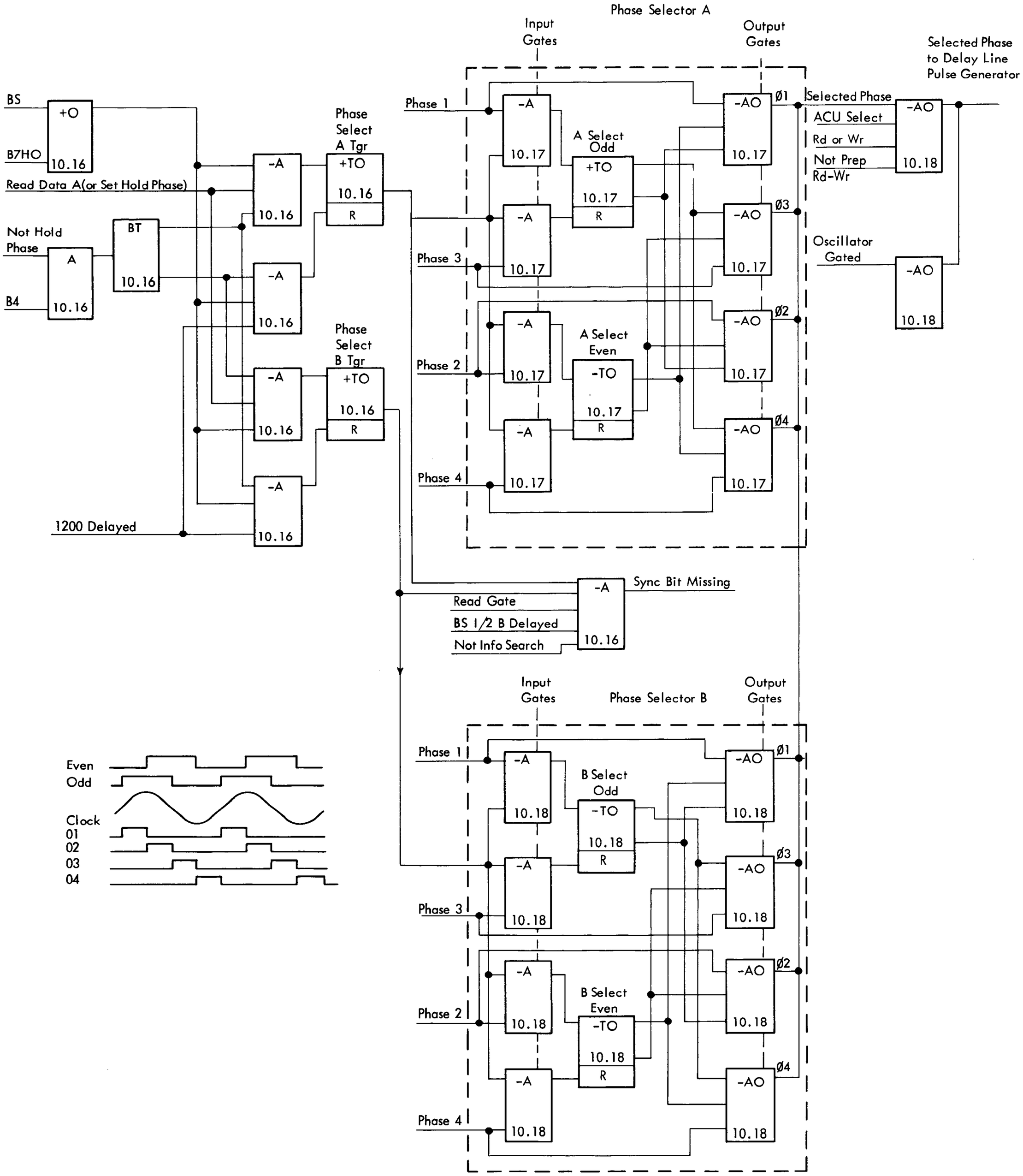
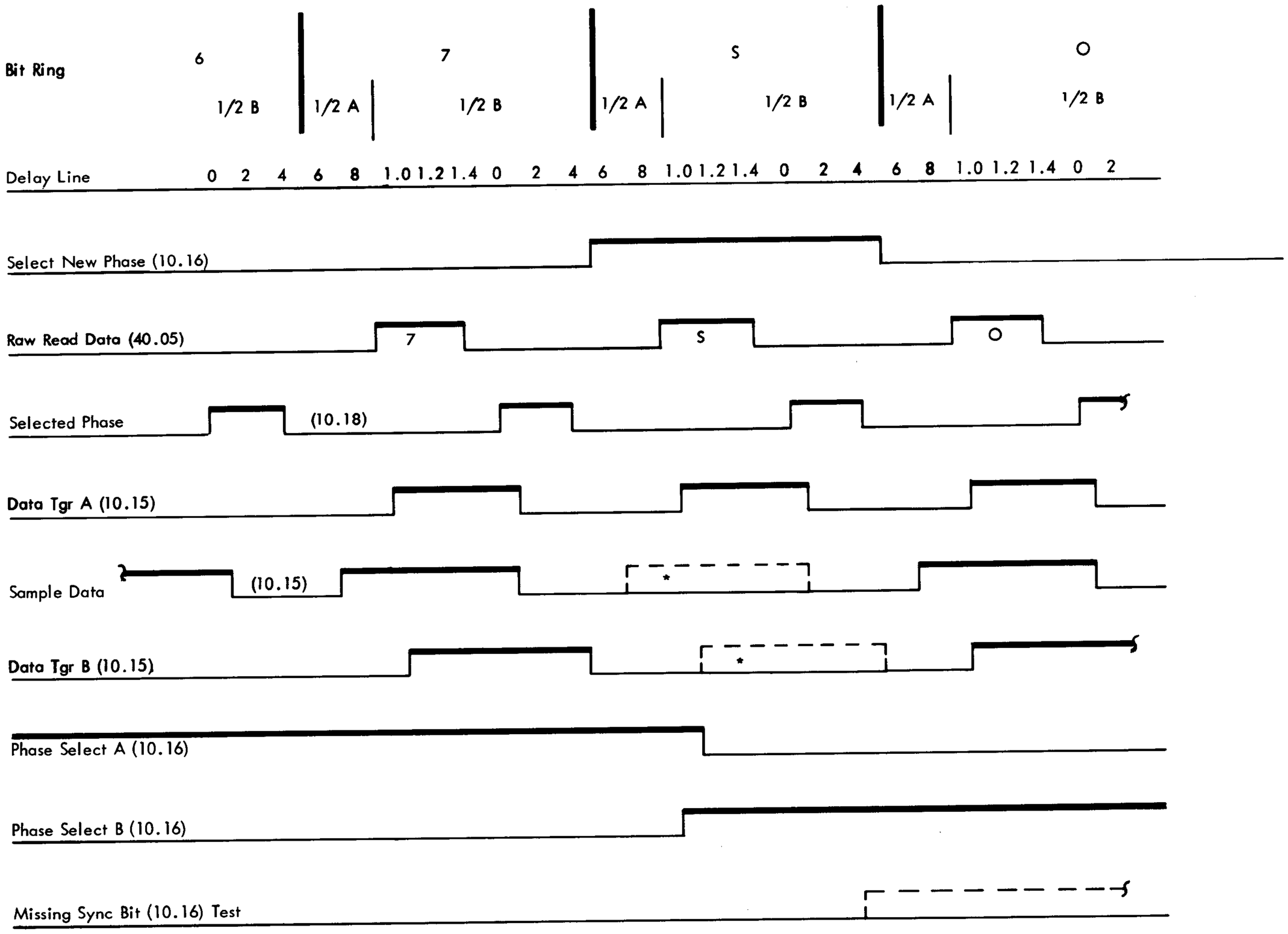


Figure 33. Phase Selector Circuits



*Suppressed on Bit S

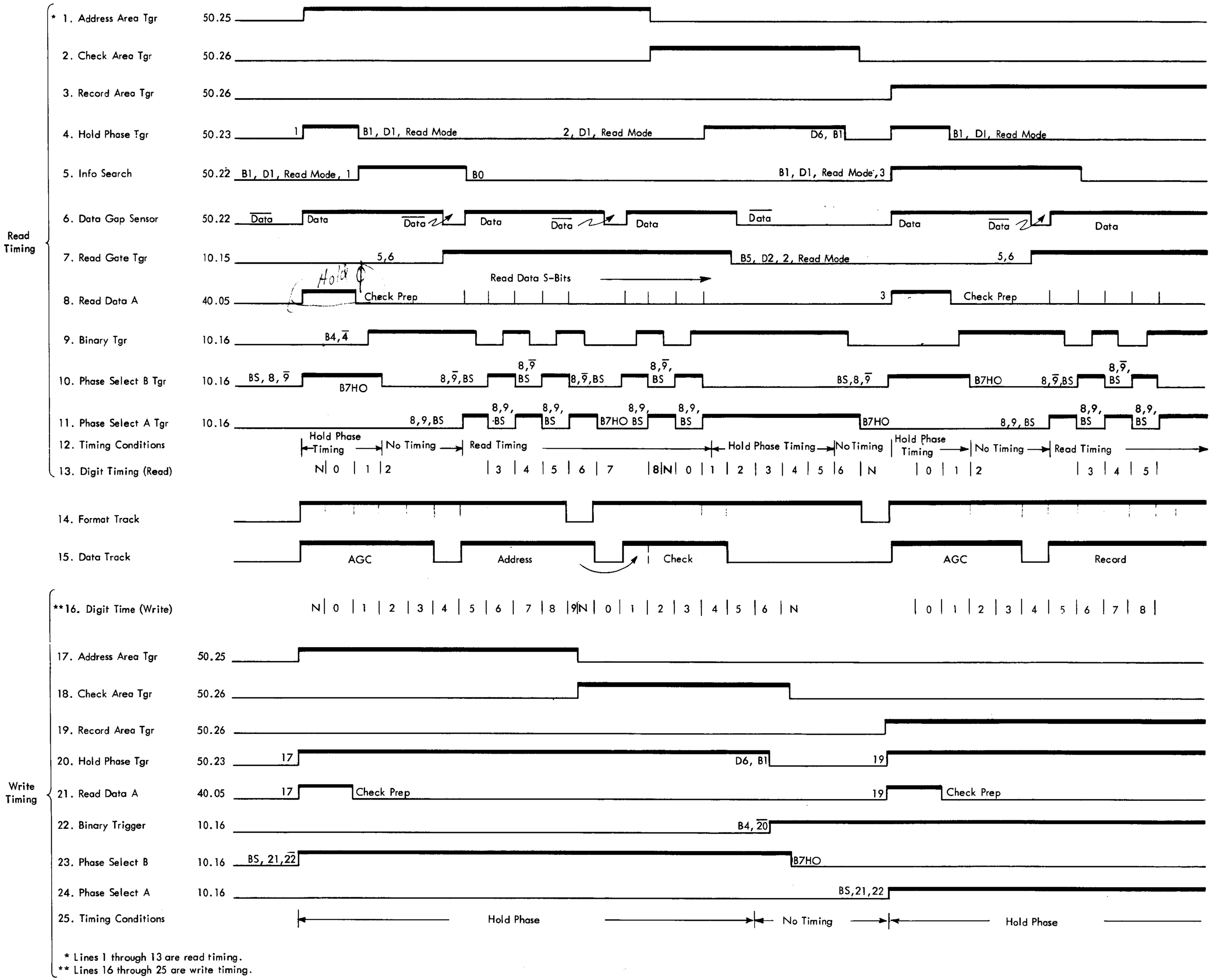
Input	Odd Trigger	Even Trigger	Output Selected Phase
01	Set	Reset	03
02	Set	Set	04
03	Reset	Set	01
04	Reset	Reset	02

Figure 34. Phase Gating and Select New Phase

Hold Phase

- **Selects a phase at random to provide write timing.**
- **Selects a phase to provide read operation timing when the read gate is off.**
- **Inhibits phase selector operation to prevent a phase change.**

The phase select circuits are also used for write timing, but they are used differently. Any phase signal is selected and applied to the delay line pulse generator input. The selected phase remains selected for a complete write data cycle; the particular phase is not important because it is only needed to generate one bit-time every 1.6 microseconds. The 7631 gates the 1301 clock track signal to the phase detection circuits. The 7631 converts the push-pull signal to four phases of clock track timing each 90 degrees apart. One of the four phases is selected at random and is gated to the delay line pulse generator. The timing de-



* Lines 1 through 13 are read timing.
** Lines 16 through 25 are write timing.

Figure 35. Phase Selection Timing

veloped from the phase signal selected at random is used to write, starting with the address, record, or index area to the end of the write data area. The signal that maintains the phase selection until the writing is completed is called the hold phase.

The hold phase signal starts write timing. Set hold phase forces a pulse on the read data line causing either phase select A or phase select B trigger to set. Set hold phase (generated when the 7631 finds an address or record area) also sets the hold phase trigger; the hold phase trigger output prevents B4 from changing the binary trigger (Figure 33). Because the hold phase signal is present until the complete address or record is written, including the check characters, the phase selection cannot be changed. When writing, the phase selector and the writing phase used are unimportant; however, it is important that the phase selector and the writing phase do not change. A phase change when writing could cause excessive write data timing variations and cause read data failures. Any normal variation in bit density that occurs in writing is corrected when reading.

Another mode of timing circuit operation is used in read mode, but not when reading address, record, or check character data. These areas are the AGC area preceding the read data and the area immediately following the check characters. (Figure 35, line 15, shows the data track.) The read gate is not set in these areas; therefore, the phase selectors cannot operate with read data. (Figure 35, line 7, shows when the read gate is set.) Set hold phase on address or record is used to select a phase and operate one of the phase selectors at the start of each address or record AGC area.

Set hold phase on address or record sets one of the phase select triggers and the hold phase trigger (upper left corner, Figure 33). This process is identical to the sequence used to generate write timing; however, in read mode the hold phase signal is reset when the digit ring count is D1 (Figure 35, line 4). After D1, the next B4 pulse can flip the binary trigger; either phase select A or B trigger resets at the next B7 time. Because B7 also steps the digit ring, the digit ring is stepped to D2 with the last B7 bit ring output (Figure 35, line 13). The bit ring stops with a BS output until read data is gated restart read timing.

A continuation of the hold phase concept is also applied after the last check character is read to provide timing to reset circuits used to read data and check characters. (Figure 35, line 4, shows where the hold phase trigger is set a second time in a read operation.) While reading the last check character, a pulse is generated to set the hold phase trigger. Hold phase prevents the binary trigger from changing; the unchanged binary trigger blocks the phase select trigger reset. This causes the last selected phase to remain selected to the end of the check area; then the hold phase trigger is reset and the binary trigger is flipped at B4 time to permit the last BS, at 1200 delay time, to reset the phase select trigger. (Figure 35, line 11, shows phase select A trigger is set with the first bit of the last check character and remains selected until timing pulses are not required.)

The last type of 7631 timing operation uses oscillator pulses. Since control, prep rd-wr, and sense operations do not transfer read or write data to or from the 1301, the 7631 625-KC oscillator is used. When the oscillator timing is needed, it is gated directly onto the selected phase line and into the delay line pulse generator, bypassing the phase select circuits (Figure 30). Figure 33 shows where the oscillator pulses are gated onto the selected phase line.

Delay Line Pulse Generator

- **Provides timed pulses at 1.6 μs rate to run bit ring, shift register and gate data.**
- **Driven by 400 nanosecond selected phase pulse.**
- **Delay line delays selected phase pulse up to 1600 nanoseconds.**
- **Timing pulses are developed by AND and OR circuits using delayed pulse.**

Control, sense, and prepare to read-write cycles cause the 7631 to gate oscillator timing to the selected phase line. During these cycles the 7631 does not transfer read or write data to or from the disk storage; therefore, the oscillator serves as the input to the delay line pulse generator. The 1.6 microsecond (625-KC) oscillator output is gated to the delay line pulse generator via the selected phase line (Figure 29).

The output pulses developed by the delay line pulse generator are derived from the selected phase line with

gated delays. For example, reset data trigger A output is developed by the delay line pulse generator using a negative AND circuit that is controlled by the selected phase delayed. The reset data trigger A output is developed from a 100-nanosecond delayed and a not 300-nanosecond delayed signal; this results in a reset data trigger A pulse starting at 100 time and ending at 300 time. The delay line pulse generator outputs are all developed in a similar manner (ALD 01.10.19).

When the oscillator is the selected timing source, the delay line pulse generator input signal is 800 nanoseconds in duration; when the clock track signal is the selected timing source, the input signal is 400 nanoseconds in duration (Figure 29). The delay line pulse generator design prevents the input signal duration from affecting the output pulse duration if the signal is greater than 400 nanoseconds in duration; therefore, the 800 nanosecond oscillator output causes the delay line pulse generator to produce the nominal outputs shown in Figure 36. When the clock track is the selected timing source, the selected phase line is gated with an in-phase 100-nanosecond delayed signal and an out-of-phase 400-nanosecond delayed signal (ALD 01.10.18). The in-phase 100-nanosecond delayed signal is used to prevent the selected phase signal from being less than 400 nanoseconds in duration at the input to the delay line pulse generator. The out-of-phase 400-nanosecond delayed signal is used to prevent the selected phase from being more than 400 nanoseconds long at the input to the delay line pulse generator.

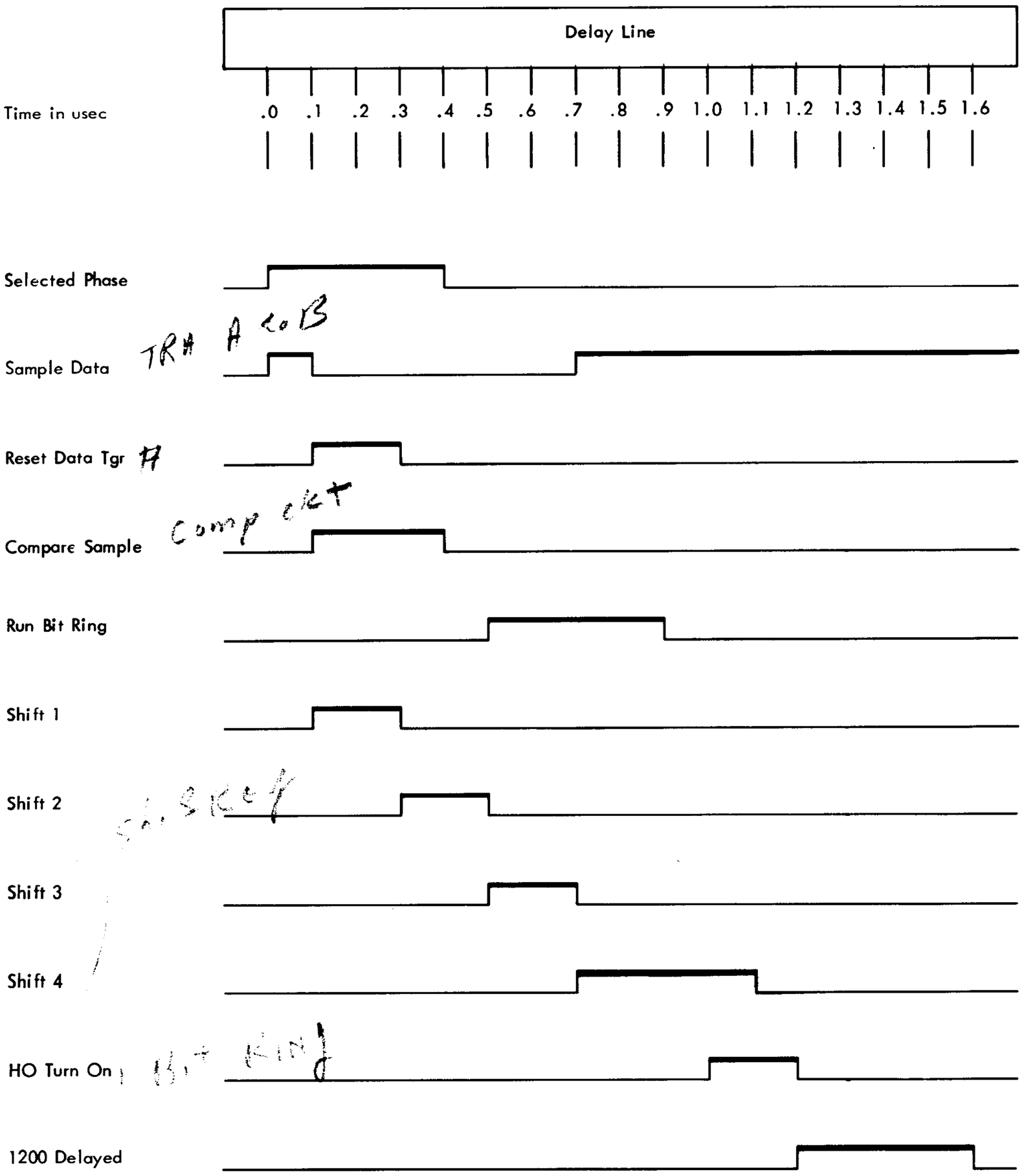


Figure 36. Delay Line Pulse Generator Timing

Bit Ring

- **Provides bit timing for each character of control, sense, read or write data.**
- **Driven by delay line pulse generator if clock trigger is on.**
- **Generates 7 pulses in six bit mode (BS, B0, B1, B4, B5, B6, B7)**
- **Generates 9 pulses in eight bit mode (BS, B0, B1, B2, B3, B4, B5, B6, B7)**
- **Bit ring reset to BS time.**

The bit ring is a nine-position trigger ring with a binary trigger drive. The ring triggers are: BS + B0, B0 + B1, B1 + B2, B2 + B3, B3 + B4, B4 + B5, B5 + B6, B6 + B7, and B7 + BS. In addition to the ring triggers two holdover triggers, BSHO and B7HO, are for special timing requirements (Figure 37). The binary trigger drive is comprised of two latch type triggers: the latch type triggers are labeled bit drive and AB (Figure 38). Bit ring timing pulses are used to sequence the 7631 control and data transfer circuits because the 1301 and 7631 are serial devices. The bit ring is advanced one bit time for each cycle of the selected phase input to the delay line pulse generator. The bit ring timing outputs BS, BSHO, B0, B1, B2, B3, B4, B5, B6, B7, and B7HO are generated during each complete bit ring cycle. When digit ring timing is needed, B7 is gated to advance the digit ring: the digit ring advances one digit time for each complete bit ring cycle (Figure 29).

The bit ring can operate in six or eight-bit mode (Figure 39, sheet 1 of 2). If the 7631 is programmed for six-bit mode, ring triggers B2 + B3, and B3 + B4, cannot be set (Figure 37). In six-bit mode, the ring is conditioned to set the B4 + B5 trigger on the bit drive cycle following B1 time, and B2 and B3 outputs are not generated. The second bit ring sequence shown in Figure 39, sheet 2 of 2, is labeled six-bit mode; line one shows the sequence of six-bit mode timings.

Reset

At the beginning of each programmed operation the bit ring is started from the reset state. Bit ring starting conditions are established by the machine idle reset. Machine idle reset, which follows the previous completed operation, sets bit triggers BS + B0 and B7 + BS. The remaining ring triggers and the binary drive triggers are reset. Because BS + B0 and B7 + BS triggers are set with machine idle reset, the bit ring is reset to BS time. The bit ring triggers form a closed loop and produce bit timing when drive pulses are applied.

Binary Trigger Drive

The binary trigger alternately supplies drive pulses bit drive A and bit drive B to advance the bit ring. Delay line pulse generator timing is gated to the binary trigger drive when bit ring timing is required (Figure 38). The clock trigger controls the delay line pulse generator input to the bit ring binary drive; if the clock trigger is off, the bit ring remains inoperative. When bit ring timing is needed, the clock trigger is set to gate 100 to 300 and 500 to 700 signals to the binary trigger drive (Figure 39, sheet 1 of 2, lines 1 and 2). The 500 to 700 signal is generated when 500-900 AND's with not 700-1000 or not 700-1100 (Figure 38). The binary trigger drive is made of the bit drive and AB triggers; outputs from the set and reset sides of the AB trigger are called bit drive B and bit drive A, respectively.

The bit drive and AB triggers control bit drive generation; for example, when the AB trigger is reset, bit drive B is available. Receipt of the first 500 to 700 signal, gated by the reset bit drive trigger, causes the AB trigger to set and produce bit drive A. Receipt of the first 100 to 300 delayed signal has had no effect on the bit drive trigger (Figure 39, sheet 1 of 2, lines 5 and 6). The second 100 to 300 delayed signal, gated by the set AB trigger, causes the bit drive trigger to set. Receipt of the second 500 to 700, gated by the set bit drive trigger, causes the AB trigger to reset and produce bit drive B. The effect of the binary trigger operation is to develop bit drive A and bit drive B alternately. Bit drive A is used to gate the set pulse to the trigger positions labeled B0 + B1, B2 + B3, B4 + B5, and B6 + B7; bit drive B is used to gate the set pulse to the trigger positions labeled BSHO, B1 + B2, B3 + B4, B5 + B6, and B7 + BS.

Bit Timing

Because the bit ring is always stopped or reset to BS time, the first time pulse generated is B0. The sequence to generate B0 is: receipt of the first 500 to 700 causes the AB trigger to set and produce bit drive A. Bit drive A, gated by BS + B0, causes B0 + B1 trigger to set and the B7 + BS trigger to reset; the rise of the B0 + B1 output and bit drive A produce the B0 output (ALD 01.50.06). This cycle repeats to advance the ring with the receipt of each 500-700 delay line pulse generator output.

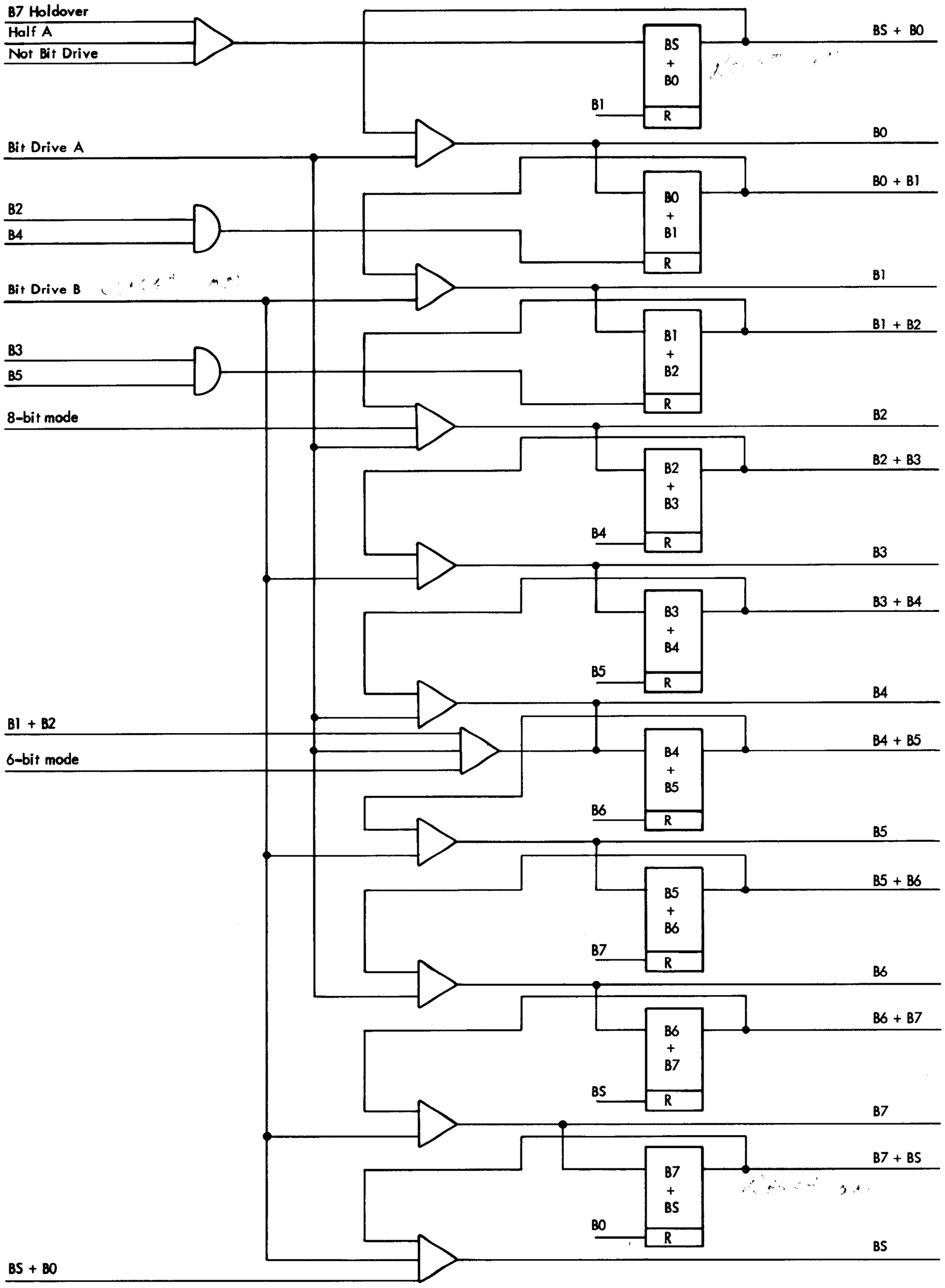


Figure 37. Bit Ring

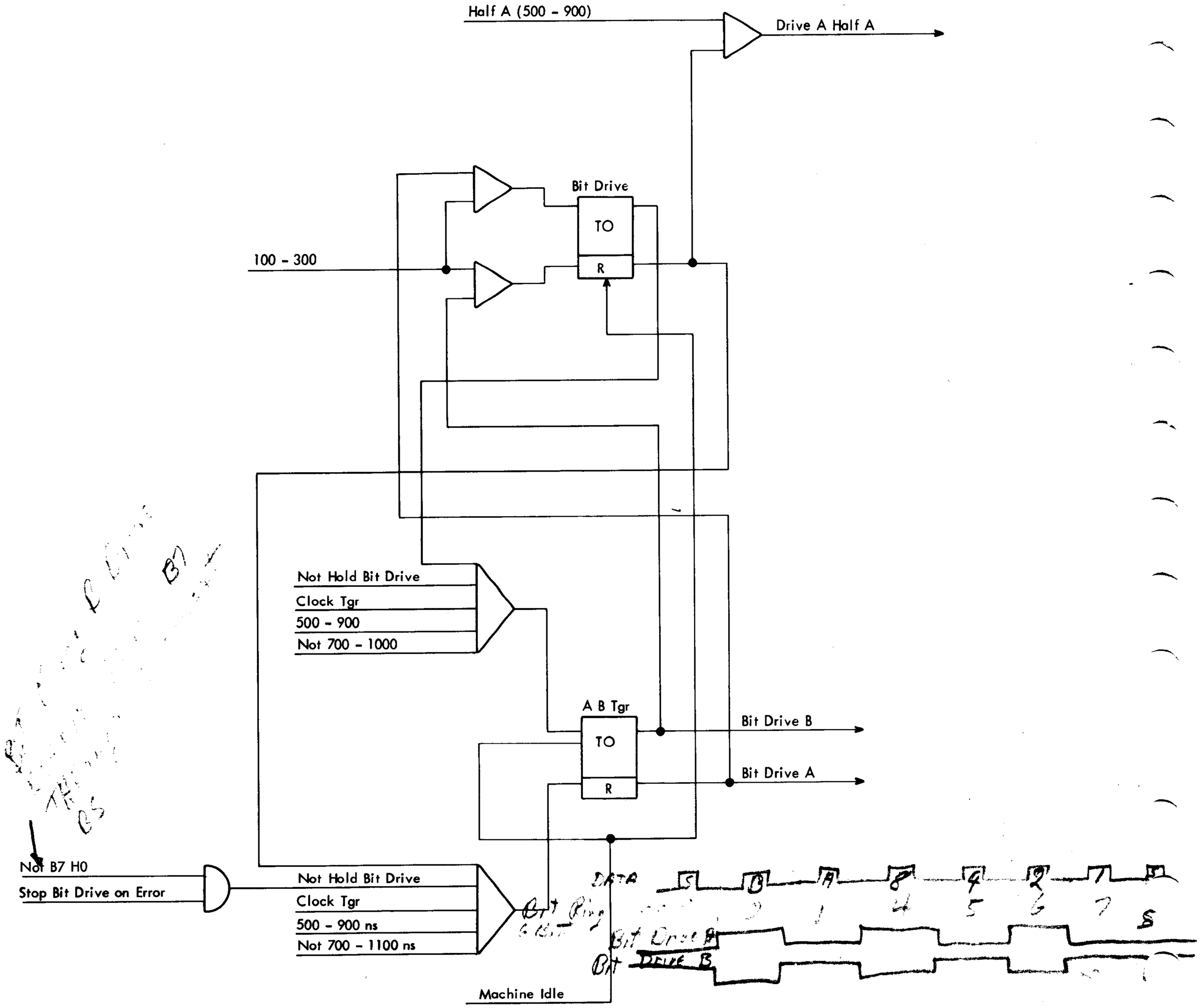


Figure 38. Bit Ring Drive

Holdovers

In addition to the sequential outputs, BS through B7, two holdover timing outputs, BSHO and B7HO are generated also. Holdover signals are generated to serve special timing requirements. A holdover signal, such as B7HO, starts at 1000 time of B7 and ends at 1000 time of BS. Since bit timing starts at 500 delayed and ends at the next 500 delayed, the holdover timing (1000 to 1000) overlaps the last half of one bit timing and the first half of the next bit timing. BSHO is not generated at the start of the first bit ring cycle following machine idle reset because the 1000-1200 delayed signal is not generated during the first BS time (Figure 39, sheet 1, line 11).

Because the ring develops an odd number of bit timings (depending on bit mode, seven or nine), the binary drive sequence must be altered before each succeeding bit ring cycle. Failure to alter the bit ring drive sequence prior to entering the next bit ring cycle causes the ring to start operation with an incorrect bit drive phase. To alter the bit drive phase, B7HO is applied to the hold bit drive line (Figure 38). Hold bit drive is applied (as inhibit to the binary trigger drive) to prevent 500-700 from setting the AB trigger during B7HO; hold bit drive causes bit drive B to remain unchanged for two consecutive bit timings; the bit drive is synchronized in this manner for the next bit ring cycle (Figure 39, lines 5 and 6). The bit ring timings are further divided into two parts. The first part is called ½A and is 500-900 delayed; the remaining (900-500) is ½B.

Digit Ring

- **Supplies 12 digit pulses to sequence 7631 file operations.**
- **Driven by B7 of bit ring if run digit trigger is on.**
- **Run digit trigger turned on by control, sense, prep R/W cycles or address, record, check area triggers or FMT stop/index.**
- **Digit ring reset to digit nothing time at B6 if digit reset trigger is on.**
- **Digit reset turned on by D11 time, end of address, record or check area and end of prep R/W cycle.**

The digit ring supplies 12 digit pulses to sequence control, read, write and sense operations. When digit ring timing is required, the ring is advanced one step for each complete cycle of the bit ring. The bit ring seven (B7) output advances the digit ring (Figure 29). The six-position digit ring requires 12 advance pulses to generate digit zero (D0) through eleven (D11) pulses.

The digit ring is advanced twice for each complete cycle of digit timing. When the first run trigger is set, the first six advance pulses generate D0 through D5 pulses. Digit 11 output occurs for the duration of bit six (B6) during D5 time. This extraneous output is normal and does not cause a timing problem.

When the last six advance pulses are applied to the ring, the first run trigger is reset and allows the same six ring triggers to generate D6 through D11. The digit ring is reset with the D5 + D0 trigger on and the remaining triggers off. Digit nothing (DN) is a common reference to a bit ring cycle that occurs while the digit ring is reset (Figures 40 and 41).

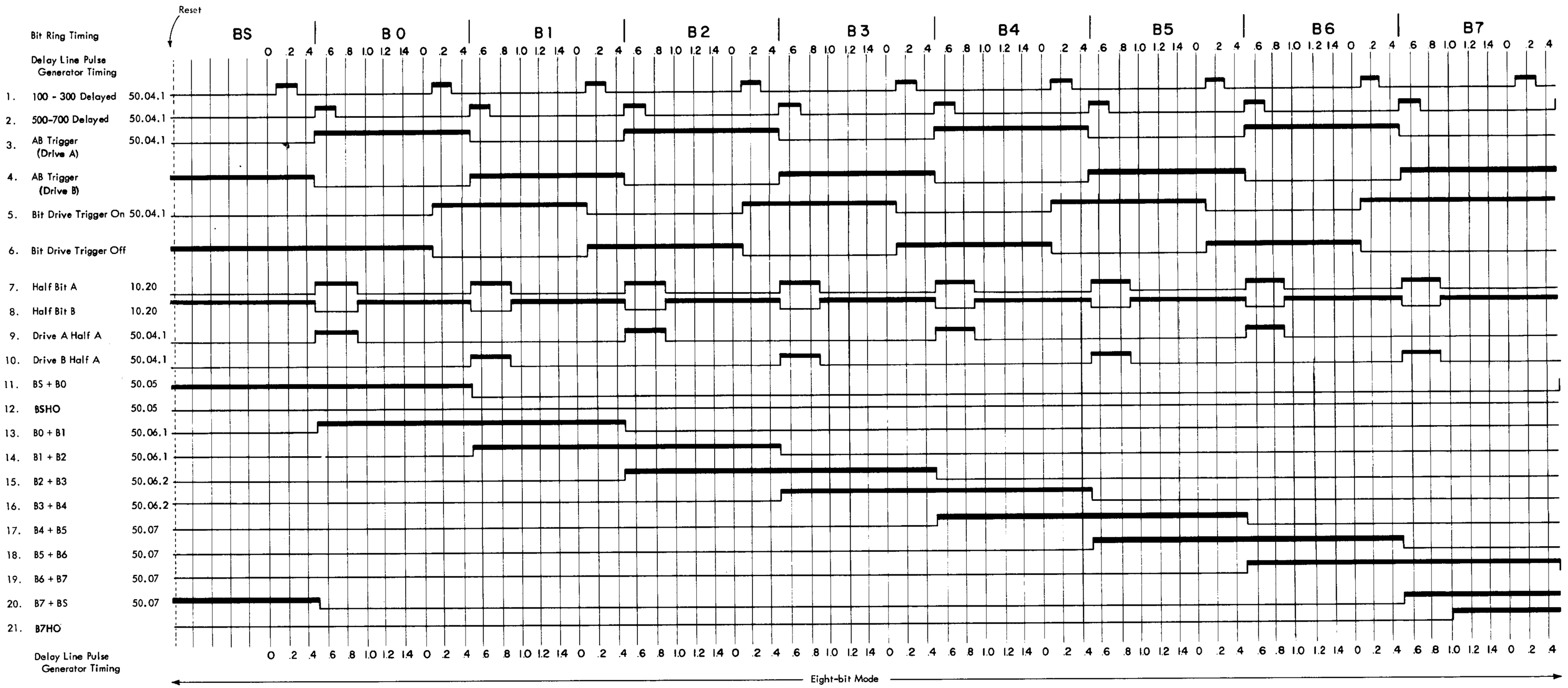


Figure 39. (Sheet 1 of 2). Bit Ring Timing—Eight-Bit Mode

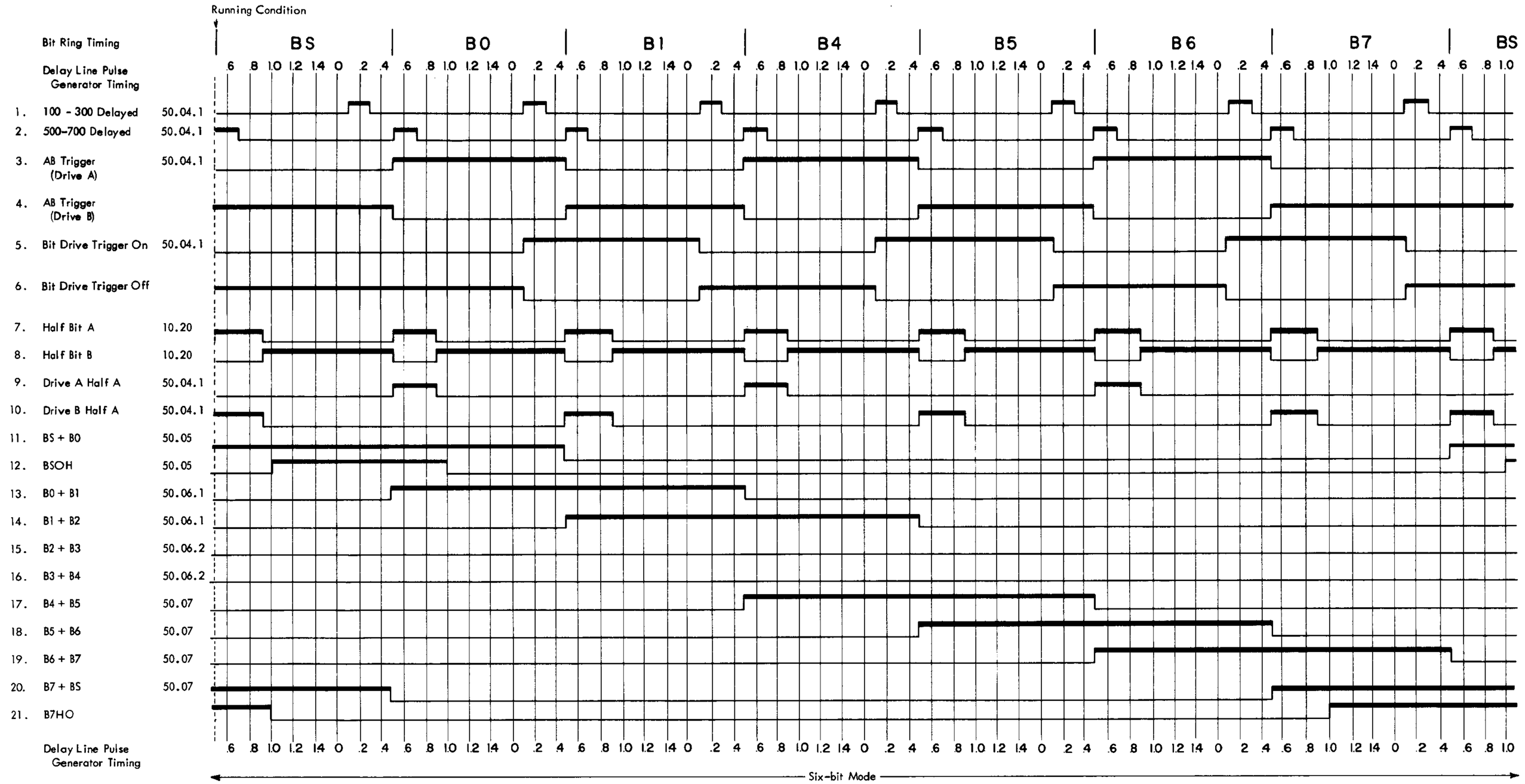


Figure 39. (Sheet 2 of 2). Bit Ring Timing—Six-Bit Mode

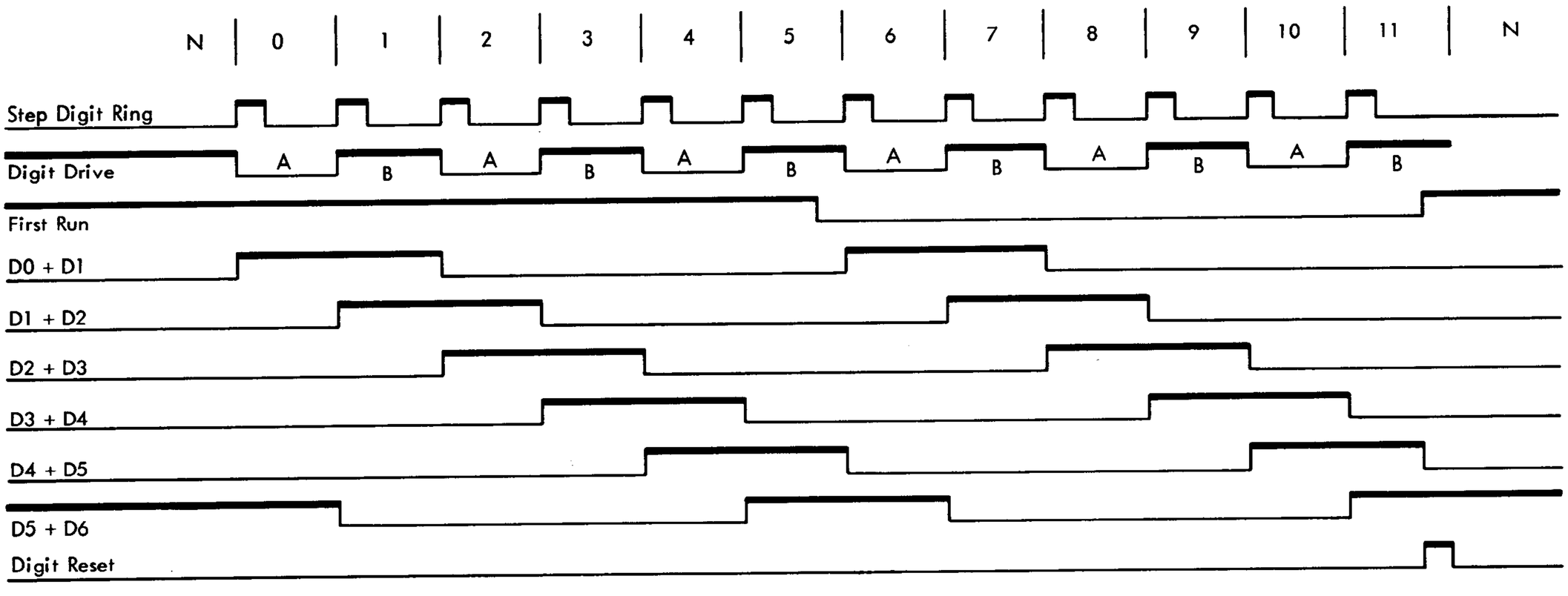


Figure 40. Digit Ring Controls

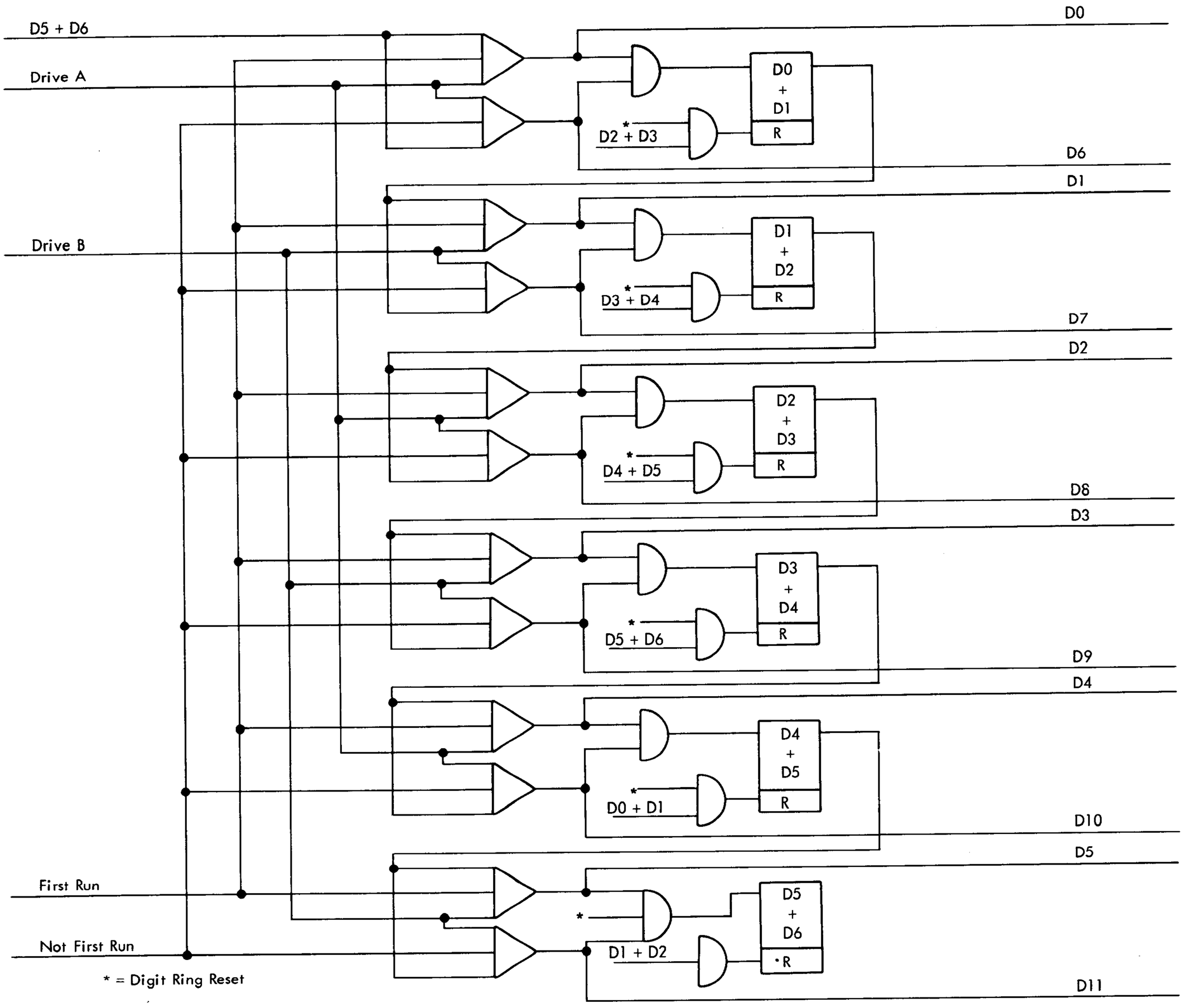


Figure 41. Digit Ring

Index Operation

- **Index pulses define disk revolutions and the beginning and end of data tracks.**
- **Successful completion of prep R/W cycle turns on index prep (prepare for index).**
- **Index prep gates index pulses to index trigger and index holdover trigger.**
- **Index holdover is used to indicate a disk revolution when reading or writing.**
- **An incomplete operation is recognized at second index and late index and indicates a file adapter (7631) error.**

A disk revolution is defined with index pulses. Early and late index signals are issued by the 1301 once for each disk revolution. The time between early and late index signals is 475 microseconds; the time for one disk

revolution is approximately 34 milliseconds. All disk operations, with the exception of SRO, begin with the first early index issued after a successful prepare to read write cycle. Operations not completed before late index is detected a second time are ended with second index. An incomplete operation, late index and second index cause the 7631 to indicate a file adapter circuit check (Figure 42).

When the first early index following the prepare to read-write cycle sets the index trigger, the 7631 generates first index. Late index, following first index, causes the index holdover trigger to set. Index holdover is used to identify the second index signal as second index. Because index holdover is used to detect late index (late index is used to start most operations), index holdover is a good scope sync point to use for a read or write display for loop mode operation. When using the CE panel switches, the index prep trigger is set with late index. Since early index and index prep are used to set the first index and index holdover triggers, read or write loop mode operations are started on alternate disk revolutions.

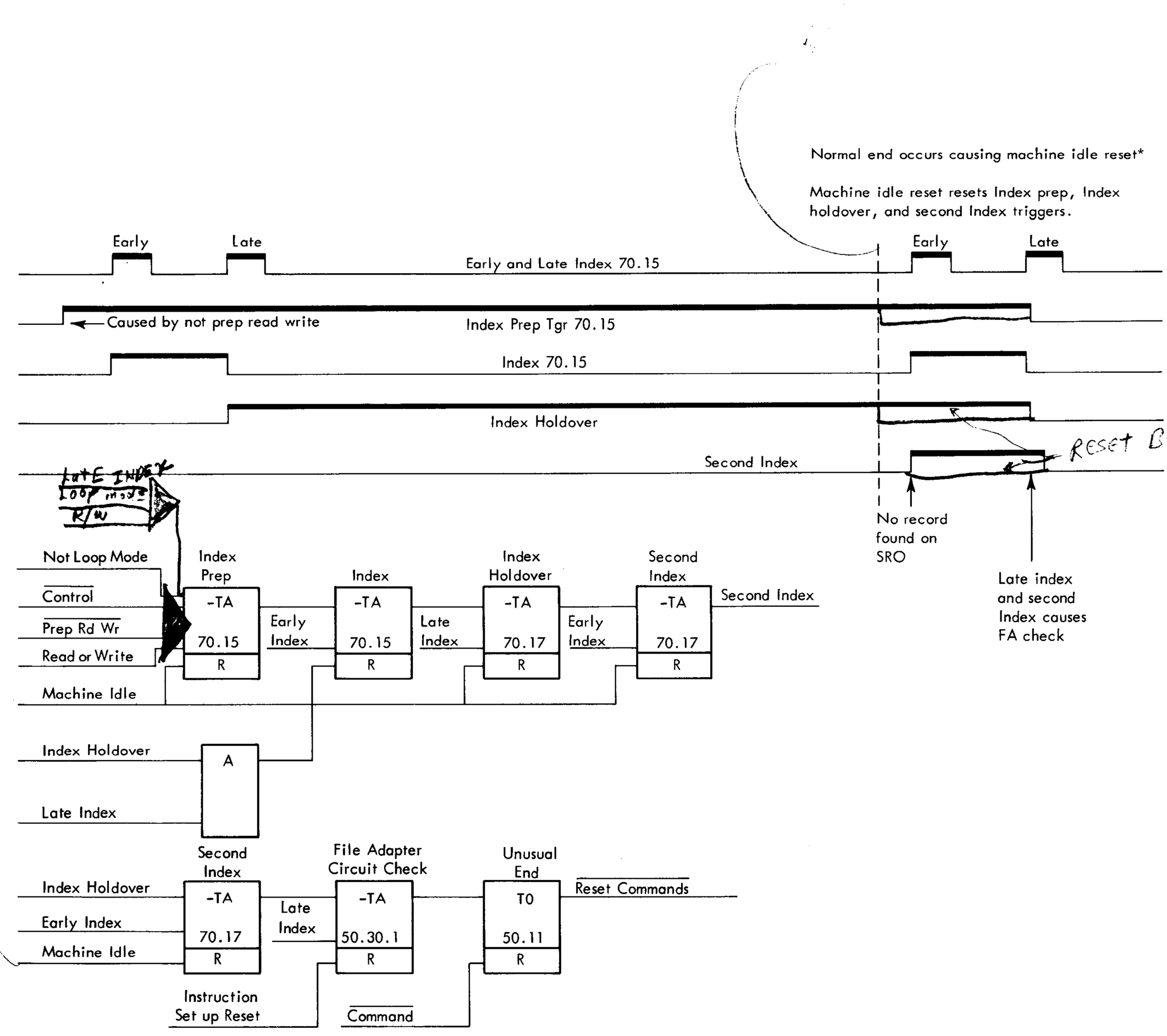


Figure 42. Index Operation

Registers

Shift Register

- **When writing, develop check character from serial write data and write on disk for each data area.**
- **When reading, develop check character from serial read data and compare to check character read from disk.**
- **Failure to compare when reading = no record found if address verify cycle, or parity if read data cycle.**
- **Test shift register before use while writing AGC burst of every write data area.**
- **Failure to test = file adaptor circuit check.**

The shift register generates check characters for each address and record written on a 1301 data track. Check characters are generated from the serial write data transferred from the processor, and they are written on the disk immediately following the written address or record. The 7631 uses check characters for the read data check; the read data check compares check characters generated from read data with check characters read from the disk (Figure 30).

The 16-position shift register receives serial read or write data as input. Six additional triggers of the check character generator are used as temporary storage (Figure 43 shows that data flow through the register is serial). The sequence of data flow through the generator is serial. Four sequential shift pulses are applied to the generator's 22 triggers during each cycle of bit timing, excluding bit sync time when the shift pulses are inhibited. The contents of the triggers are transferred in parallel groups of five or six bits at a time. The four shift pulses move data through the 16 positions serially until 16 bits of data are entered (Figure 43).

The feedback loop is active when the sixteenth data bit is entered. The next cycle of four shift pulses modify the data entering the X0, X1, and X14 positions with the contents of position X15 stored (Figure 43). If the input bit and the feedback (contents of X15) stored are different, the exclusive OR input to these stages causes the position to set. If the feedback bit and input bit to these stages are the same, the trigger position is reset.

Check character generation is started and ended with each record or address area. The shift register contents (three characters of check character code) are shifted out and written in the disk check area following the written record or address. In a read operation, the shift register contents (three characters of check character code) are read out and compared with the check characters read from the disk. Failures are indicated as no compare signals further classified by the error indicating circuits as data failures or as no record found conditions. Three characters of check code are generated for read or write operations regardless of the machine bit mode; 18 bits of check character code are generated in six-bit mode operation and 24 bits of check data are generated in eight-bit mode operation.

A shift register test is performed before writing each address or record area. Twenty-eight AGC data bits and two zero bits are entered for the test. The shift register reset is adjusted to allow the specified number of AGC bits and zero bits to enter the register before the test regardless of the machine bit mode. Failure to enter the correct number of bits or any circuit failure within the shift register is detected by the test. An error of this type causes the 7631 to indicate a file adapter circuit check and to signal immediate unusual end to the system. Shift register controls are summarized in Figure 44.

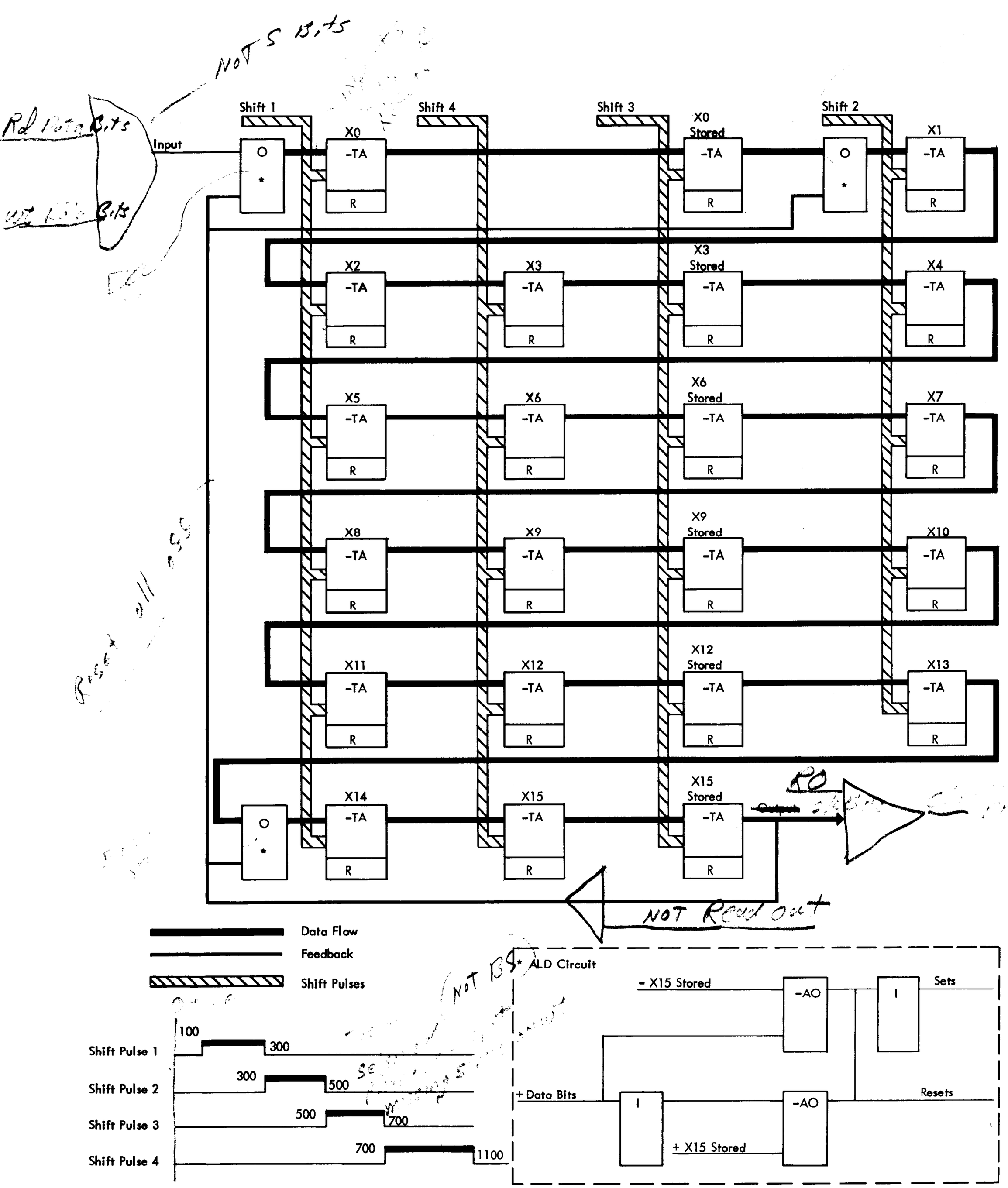


Figure 43. Shift Register

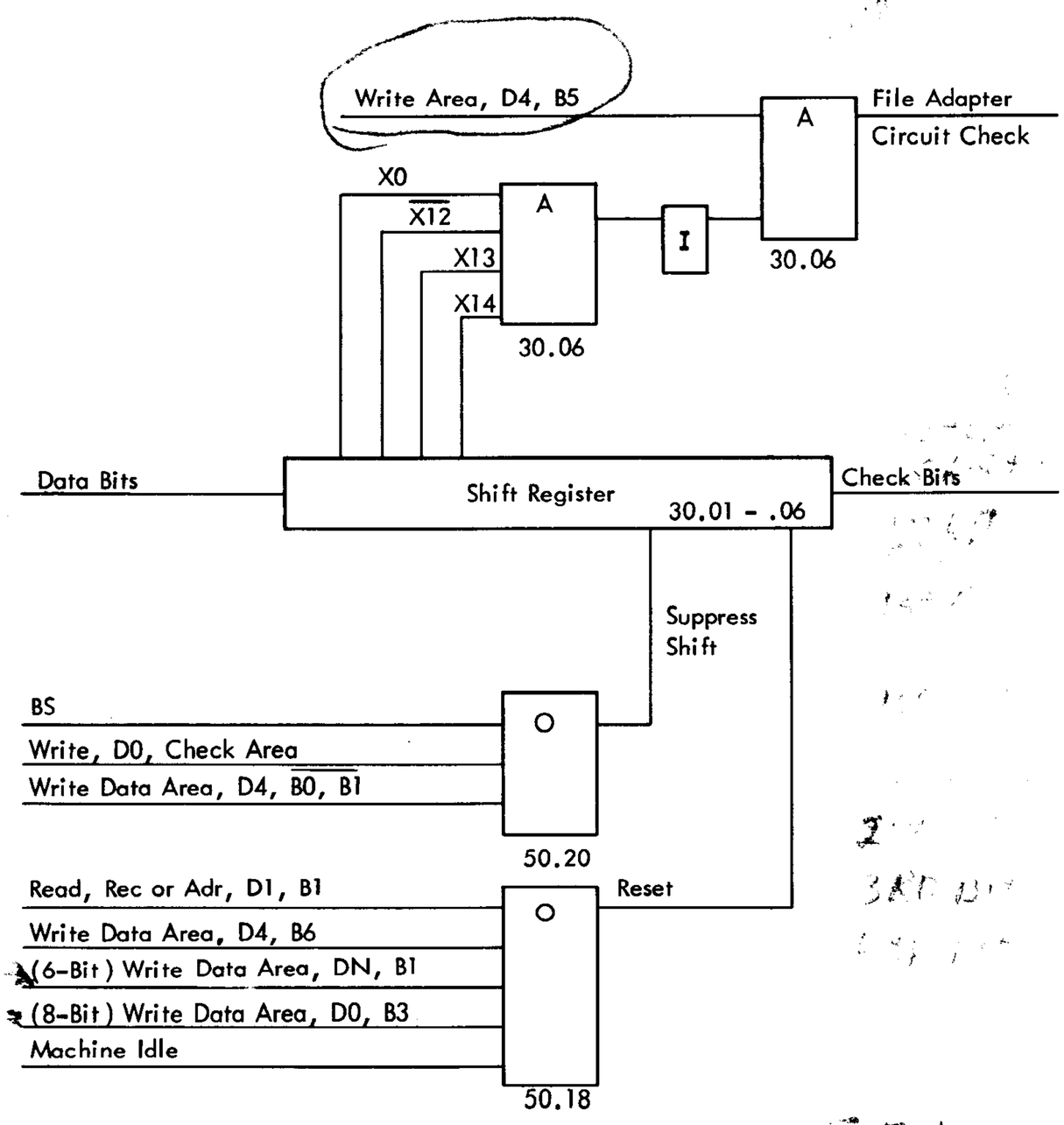


Figure 44. Shift Register Controls

Input Register

- **Nine-position register to buffer data flow on a Model 2, 3 or 4.**
- **Input is system data or a control or write operation.**
- **Input is serial register on a read or sense (7000) operation.**

The input register is a nine-position register used to buffer data flow between a 7000 or a 1410 model 3 system and the 7631 (Figure 30). The nine positions, bit zero through seven with parity, are loaded in parallel with information from the write bus during control and write operations. Data are parallel-transferred from the serial register to the input register during read and sense operations (ALD 01.10.01-03).

Serial Register

- **Nine position register, bit 0 through bit 7 and parity position.**
- **Input is one of the following depending on operation: system data, sense data (7000), track register, random record register, random record reg 0, flag character.**

The serial register is a nine-position register, bit zero through seven and parity, used for several purposes. Write data, parallel-transferred from either the input register or the 1410 write bus, is parity-checked and stored in the serial register until it is serially transferred to the 1301 write circuits (Figure 30). Address data from 7000 and 1410 systems are parity-checked and stored in the serial register until they are decoded or

stored in the 7631 address register. Serial read data are assembled and assigned parity in the serial register before parallel readout to the input register or the 1410 read bus.

Status information requested by a 7000 system processor is transferred from the status circuits into the serial register where parity is assigned before it is transferred to the input register (ALD 01.10.04-07).

Read and write address verification also requires the use of the serial register. Address data stored in the 7631 address register are parallel-transferred to the serial register during address verify cycles. The serial register contents are serially read out to the compare circuits where they are compared bit by bit with the address information read from the 1301 disk track.

Address Register

- **Store address data during control cycle.**
- **Consists of access, module, track and random record registers.**
- **Access and module register used to select the proper file.**
- **Track register (4 numeric registers) contain track address of file operation (HA1).**
- **Random record register (2 alpha-numeric registers) contain HA2 identifiers.**
- **SRO operation uses track and random record register for record address data.**

The address register is used to store address information required to seek or verify the address of 1301 data track. Beginning at D3 and ending at D10 address information is stored in the eight-section address register; address register loading occurs when the 7631 control trigger is set by either a 1410 file operation instruction or a 7000 system control command (Figure 30).

The numeric bits B4, B5, B6, and B7 are stored in the serial register at D3; they are decoded and cause the access selection. Numeric module selection data is transferred from the serial register and stored in four module selection triggers at D4. Module select information is decoded in the 7631 and permits one of ten module selections. The four bytes of numeric track and head selection data are transferred from the serial register to track register T_0, T_1, T_2, and T_3 on digit cycles D5 through D8. The serial register bits B4, B5, B6, and B7 are stored in track register bits B0, B1, B2, and B3, respectively. The track register information is used as address data storage required for verification or seek operations. Binary or BCD zeros do not produce outputs from the track register. Figure 45 shows how the data is encoded for the 1301.

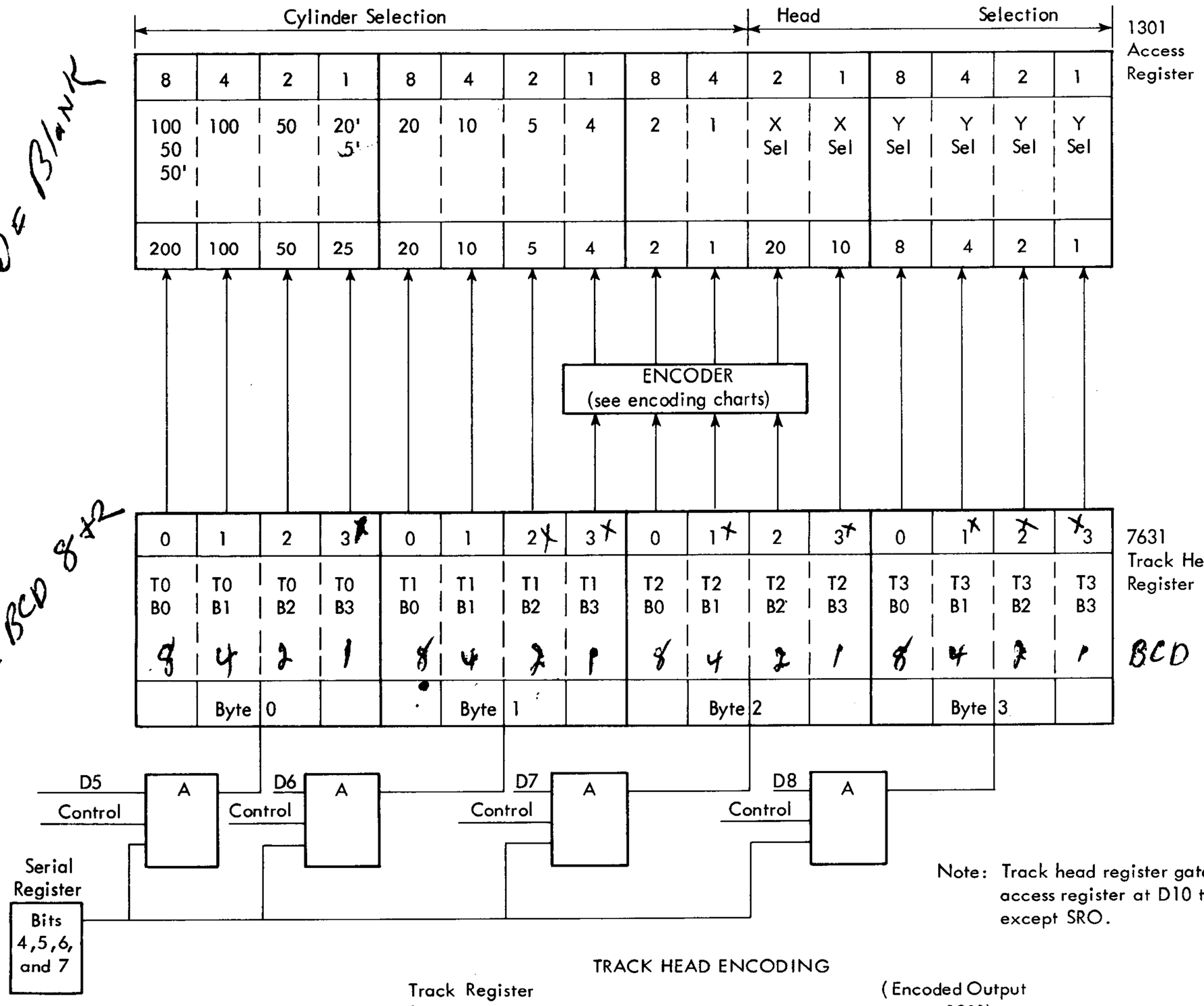
Random record register bytes R_0 and R_1 are used to store alphabetic or numeric information. These two bytes of address information are each stored in six trigger positions labeled B0 through B5, and are loaded with digit cycles D9 and D10. They are used also to store HA2 or the last two record address digits.

Serial Register Parity

- **Determines if bit configuration of serial register is odd or even parity.**
- **Incoming data characters from the system are parity checked and must be odd or parity error is indicated.**
- **Read and sense (7000) data is assigned correct odd parity before transfer to the system.**

Serial register parity is an AND-OR circuit combination used to determine serial register parity. The circuit verifies the parity of incoming control and write data and assigns parity to read and sense data transferred to the processor. Serial register outputs, bit parity through seven, are applied to the serial register parity circuit to

TRACK HEAD AND ACCESS REGISTER RELATIONSHIP



Note: Track head register gated to access register at D10 time except SRO.

TRACK HEAD ENCODING

Track Register (Encoder Input)					(Encoded Output to 1301)				
T1 B3	T2 B0	T2 B1	T2 B2	T2 B3	T1 B3	T2 B0	T2 B1	T2 B2	T2 B3
				X					X
			X					X	
			X	X				X	X
		X					X		
		X		X			X		X
		X	X				X	X	
		X	X	X			X	X	X
	X					X			
	X			X		X			X
X						X		X	
X				X		X			X
X			X			X		X	X
X			X	X		X	X		
X		X				X	X	X	
X		X		X		X	X	X	X
X		X	X		X				
X		X	X	X	X				X
X	X				X			X	
X	X			X	X			X	X

Note: ~~Track register bytes~~ 0, 2, and 3 ~~eliminate zeros~~ (BCD2 and 8 bits). Byte 1 eliminates zeros except on BCD 1, 2 and 8 bits (#).

ALD 20.06

Figure 45. 7631 Track-Head Register and 1301 Access Register Relationship

determine if the bit count is odd or even. Whenever the count is even, the circuit signals +S generate parity on read or +S VRC on write (VRC means vertical redundancy check). Generate parity on read sets the input register parity trigger or indicates parity directly to an attached 1410. VRC on write indicates that invalid data has been transferred to the 7631. Invalid control or write data causes the 7631 to issue an unusual end command to a 7000 system or file control to CPU data check to a 1410 system.

The serial register bits are compared in pairs; where a compared pair is odd, an output is developed (Figure 46). Two AND circuits are used to compare each pair of bits. For example, AND 1 compares B0 with not B1 and AND 2 compares B1 with not B0. An output from AND 1 or 2 indicates the partial parity is odd. Similar comparisons are made for the remaining bit pairs. Partial parity outputs derived from compared pairs are used to determine partial parity for two pairs (four bits). Again, the parity circuit compares the first bit group (B0, B1, B2, and B3) partial parity with the second bit group (B4, B5, B6, and B7) to determine if the bit count is odd or even. Partial parity for groups one and two is finally compared with B7 to determine serial register parity. B7 is compared with partial parity of groups one and two to avoid logic delays.

Format Recognition Scheme

- **A write format order will write the format track.**
- **A format track controls 40 read/write data tracks in the cylinder.**
- **Format read data is used to define data areas when writing on data tracks.**
- **Format read data is used to define data areas when reading except on a read HAO operation.**

The format tracks permit the disk user to organize each 1301 disk cylinder according to its use. The format to data track relationship can be compared to program housekeeping functions or masking a storage area for future use. Before data can be written or read from a track, the related format track must be written. The format track controls the location, record address and record sizes, and the total number of records on the track, and remains unchanged until it is rewritten.

The format write data transferred to the 7631 are a series of BCD characters organized to control the format track layout. Each BCD character received by the 7631 is decoded and converted to a six- or eight-bit mode character of all-bits or no-bits. The address, record, and check areas of the data tracks are defined by writing a specific number of these characters in each area of the format track. The address or record area defined with the all-bit format characters is separated from the adjacent areas with gaps of no-bits characters (Figure 47, line 3).

Format control of the data track starts when raw format read data are applied to the short and long gap singleshots. These singleshots convert the format data to signals that represent the long and short gaps. The gap lengths and their sequence is significant to the format recognition logic.

Starting with late index gated, the format recognition circuits identify the first area of the disk as home address area one, and the next area as the check area of home address area one (Figure 48). Home address area two is identified as a record area by the format recognition circuits. The next area identified is the home address two check area. The recognition circuits continue operation as the disk rotates, and alternately signal address, check, record, and check area.

Recognition logic operates in two modes: read and write. When the 7631 is writing data, format recognition logic controls the operation with the signals developed by the short and long gap sensor singleshots. Write timing is developed by switching the phase selector circuits to the hold phase operation mode. Write data operations are sequenced primarily by format data. Because of skew (variation between the 1301 clock track read head and the position of the format read head) the format recognition logic is assisted by the format skew detector when the 7631 is in write

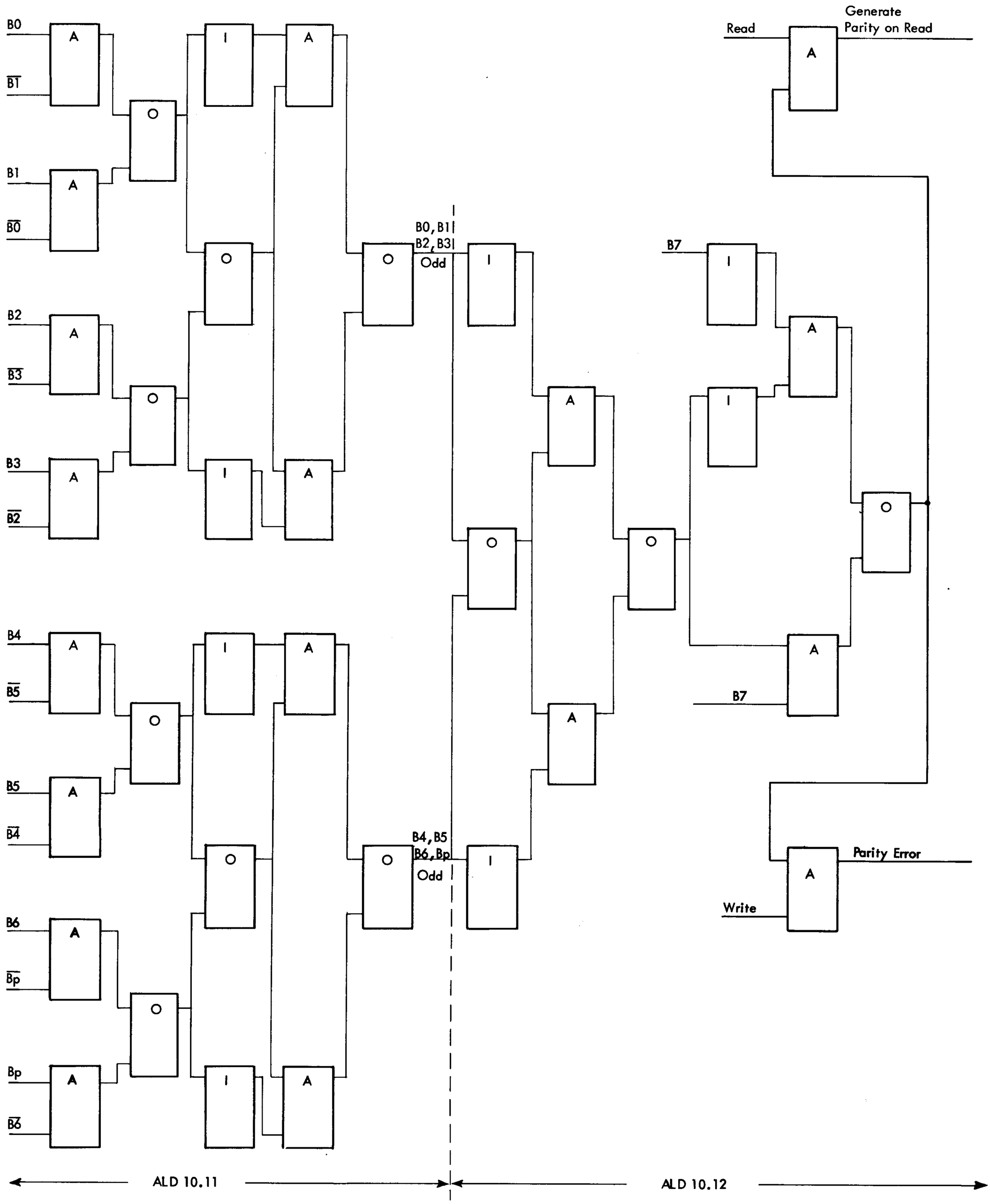
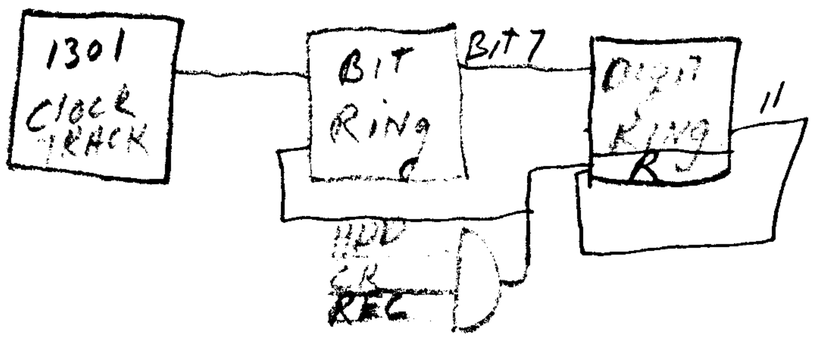


Figure 46. Parity Circuit



WRITE OPP.

BIT + DIGIT RINGS RUN ONLY
WHEN ADD-REC OR CK AREA
TGRS ARE ON.
BIT RING RESETS DIGIT RING

WRITE GAP WHEN D4 WHEN
IN ADDRESS OR RECORD AREA
WRITE MISSING SYNC GAP EVERY
D0 WHEN IN CK AREA

HA2 IS RES
MISSING

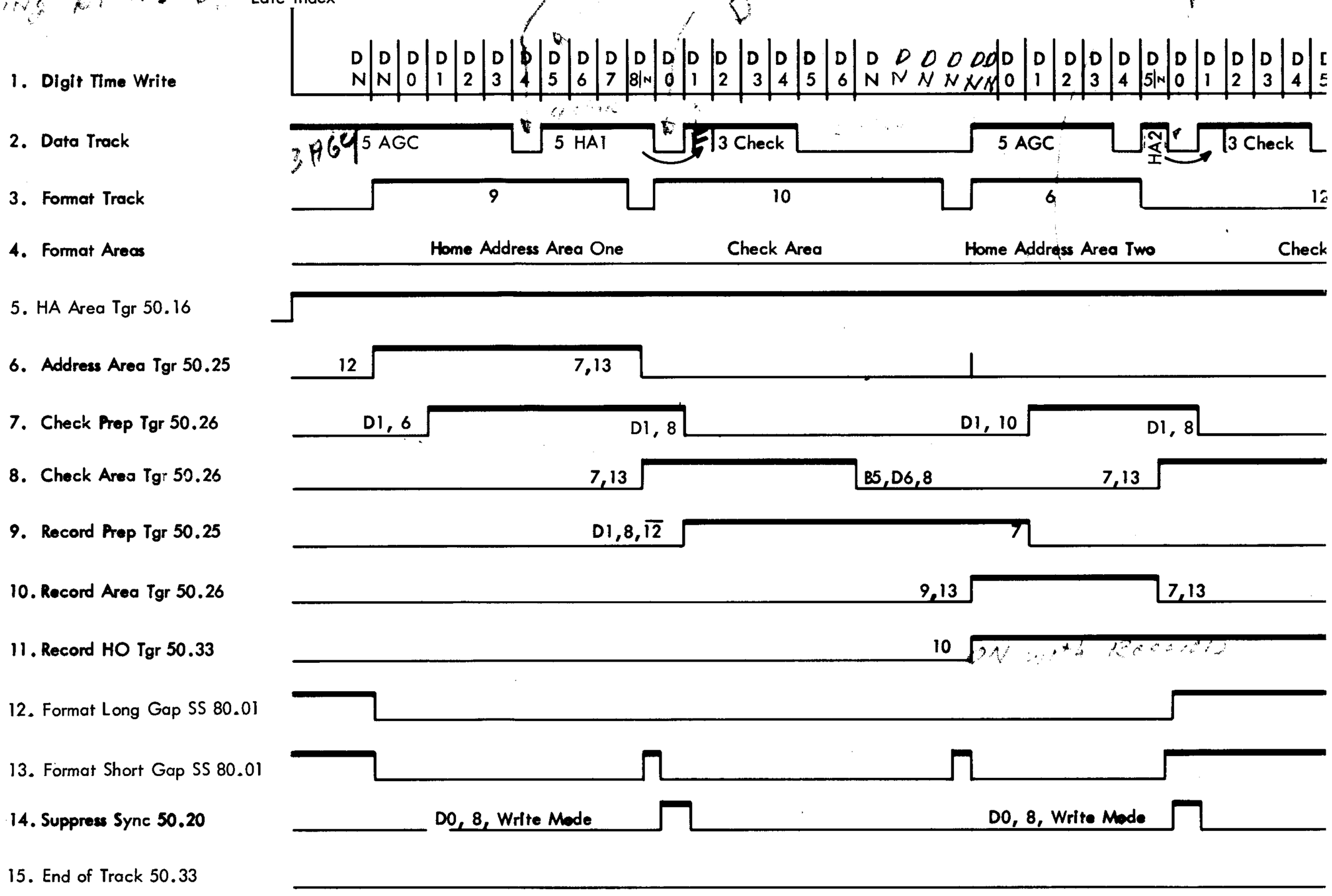


Figure 47. Format Recognition-Write Mode

FORMAT SS HOLD

LONG GAP = 200 MS
SHORT GAP = 3 MS

TO WRITE D
ADDRESS AREA
CK AREA = 5
RECORD AREA =

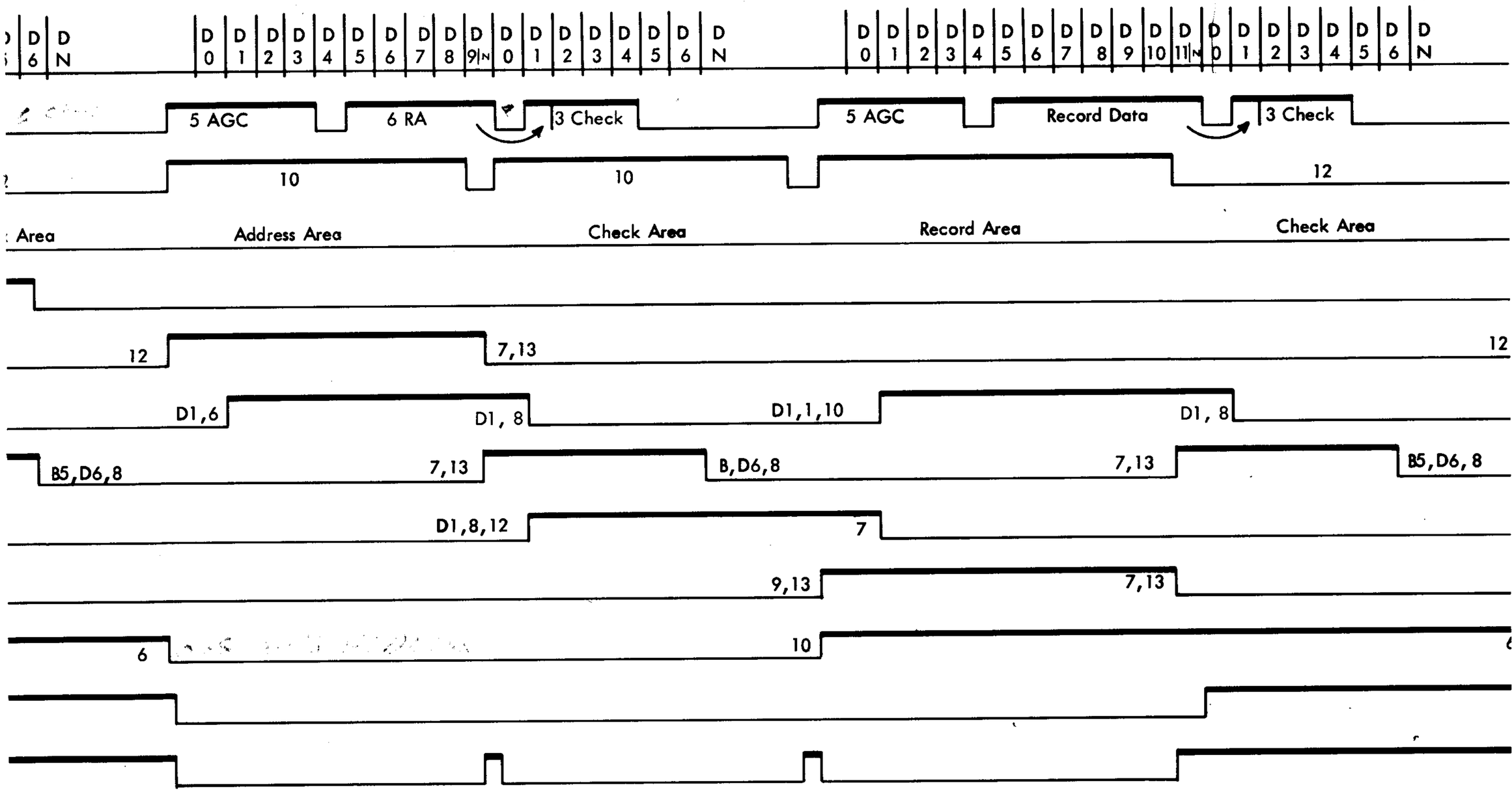
CK PREP ON
REC PREP ON

HA1 1ST CHAR

D4	D5	D6

5 6 7 5 0 1 2 3 4 5 6 7 5

Char 4 IN
8 BIT mode



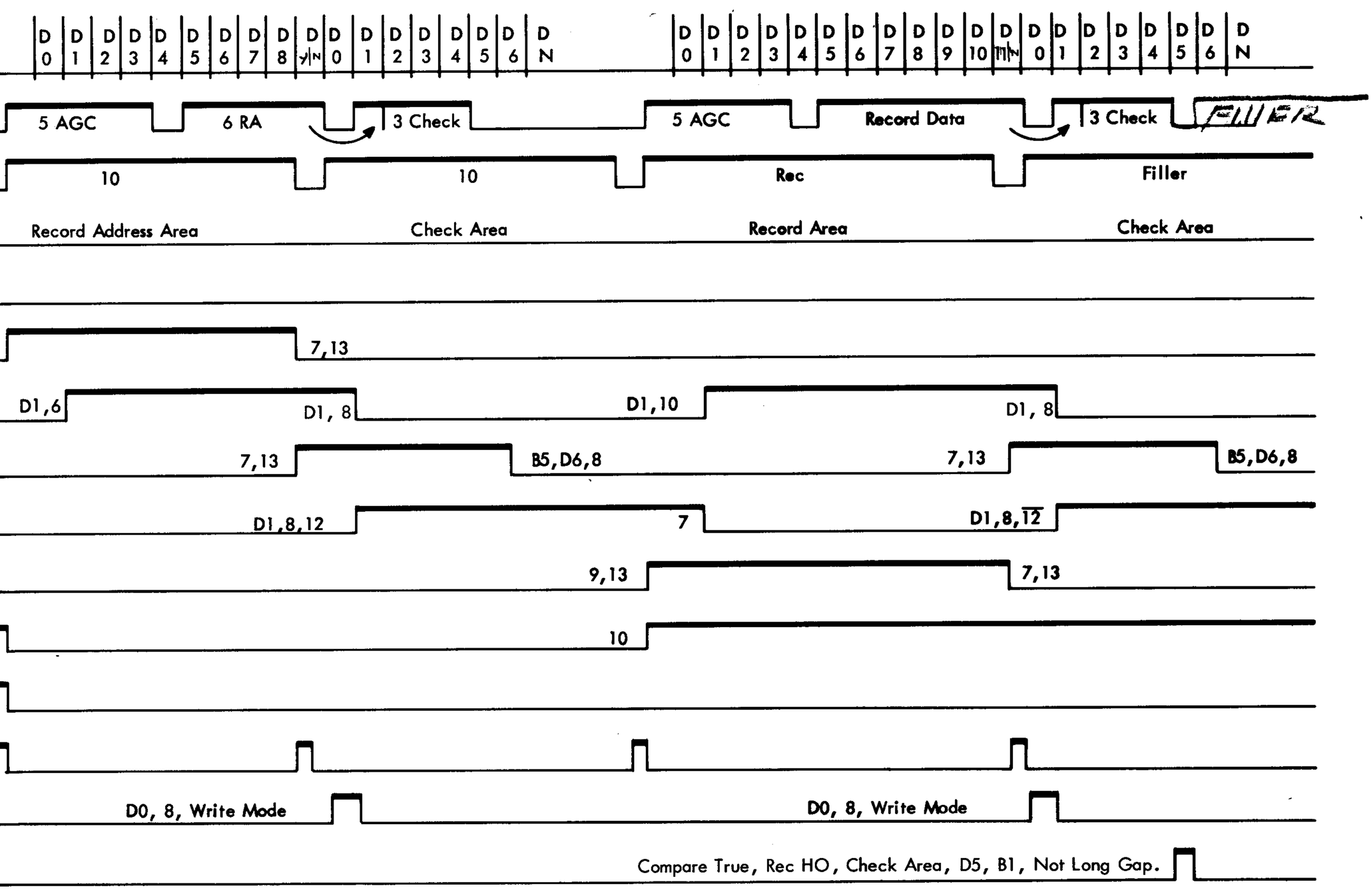
D0, 8, Write Mode

D0, 8, Write Mode

ATA

= TRailing EDGE of Long Gap
Short Gap + CK Area
TRailing EDGE of Short Gap + Area for CK

WHEN IN REC OR RDD AREA
WHEN IN RDD AREA


D 0 D 1 D 2 D 3 D 4 D 5 D 6 D 7 D 8 D y/N D 0 D 1 D 2 D 3 D 4 D 5 D 6 D N
D 0 D 1 D 2 D 3 D 4 D 5 D 6 D 7 D 8 D 9 D 10 D m/N D 0 D 1 D 2 D 3 D 4 D 5 D 6 D N
5 AGC
6 RA
3 Check
5 AGC
Record Data
3 Check
FWER
10
10
Rec
Filler
Record Address Area
Check Area
Record Area
Check Area
7,13
D1,6
D1, 8
D1,10
D1, 8
7,13
B5,D6,8
7,13
B5,D6,8
D1,8,12
7
D1,8,12
9,13
7,13
10
D0, 8, Write Mode
D0, 8, Write Mode
Compare True, Rec HO, Check Area, D5, B1, Not Long Gap.

mode. The write mode format recognition text following assumes no skew is present and excludes the format skew detection scheme which is explained in "Format Skew Detector."

When the 7631 is in read mode, recognition logic operates with a combination of format and data track signals. Timing is developed from both hold phase and read data timing schemes. The recognition logic sequence uses format track signals to identify address and record areas and the read data missing sync signal to identify check areas. Check area recognition prepares the format recognition logic to use the next format short gap signal to identify the next record area. Again, the missing sync bit in the data track record area gap is used to find the related check area. In read mode, format recognition logic operates repetitively by alternately signalling address, check, record, and check as the disk rotates until the recognition logic or the operation end causes the process to stop.

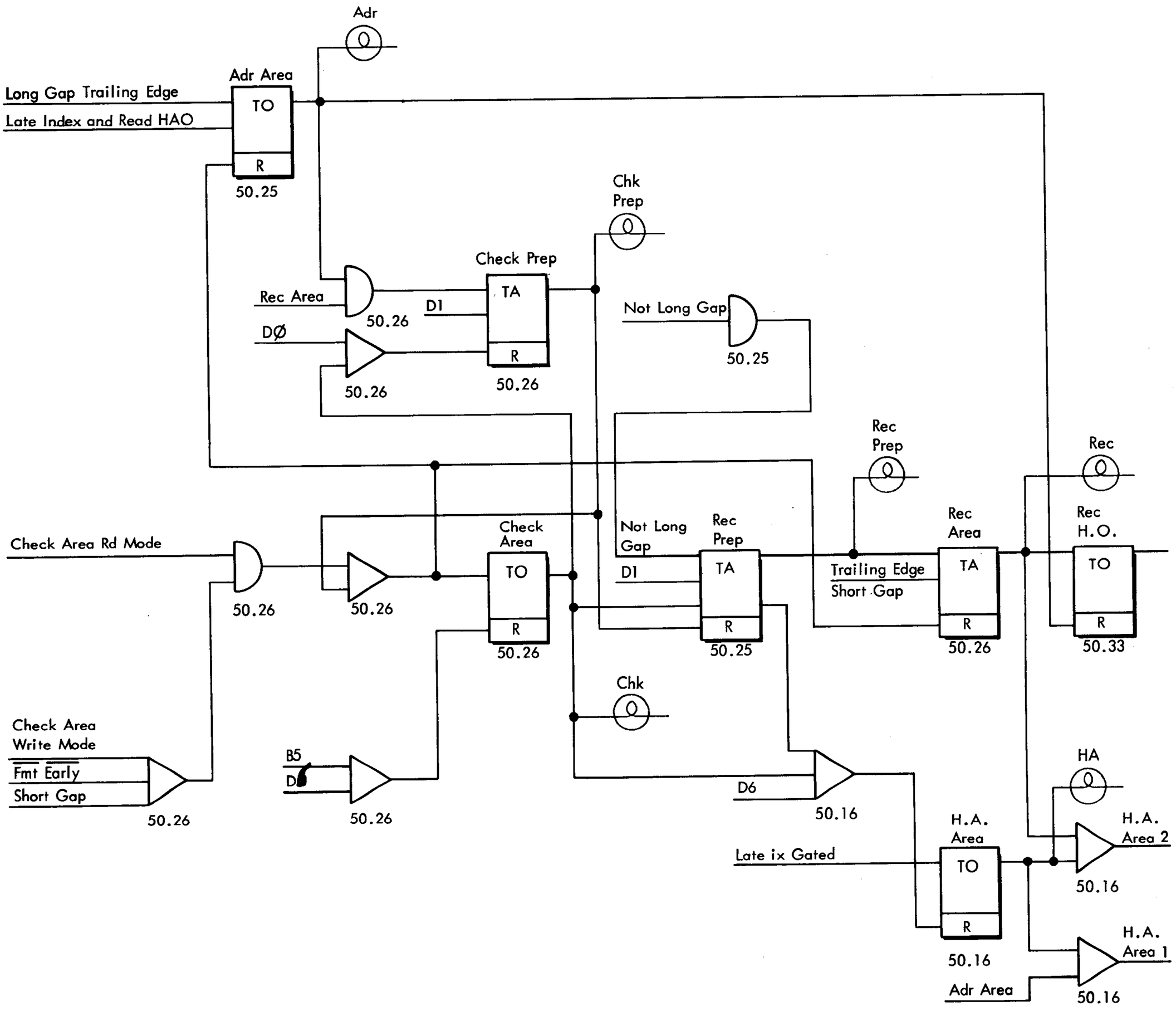


Figure 48. Format Recognition Logic

Gap Detectors

- **Format read data is gated to a long gap and a short gap singleshot.**
- **Long gap singleshot times out and indicates long gap 24 microseconds into gap on format track.**
- **Short gap singleshot times out and indicates short gap 3 microseconds into gap on format track.**

Format read data is applied to the gap sensor singleshots to detect the presence of format read data. The gap sensor singleshots convert the raw format read data to long and short gap signals that represent the programmed format areas and their associated gaps. When writing, the format recognition logic uses the gap senser outputs to identify the address, check, and record areas of the related data tracks (Figure 47, lines 12 and 13).

The two singleshots are called long and short gap. The format data applied to both gap sensors is raw format read data. Input one-bits prevent the singleshots from timing out; input zero-bits permit the singleshots to time out and produce active signals (ALD 01.80.01).

The format head reads gaps of no-bits between the address areas, record areas, and in the area preceding HA1. Gaps are either one, three, or twelve no-bits characters in length. The short gap sensor is designed to time out three microseconds after the last input bit and the long gap sensor is designed to time out 24 microseconds after the last input bit. The format track gaps cause the short gap sensor to signal short gap for every format track gap while the long gap sensor signals long gap for three and twelve character gaps. The format recognition logic is designed to give precedence to the long gap signals when they coincide with a short gap signal.

Write Mode Format Recognition

- **Address area is defined by trailing edge of a long gap on the format track.**
- **Check area is defined by short gap on the format track, check prep and not format early.**
- **Record area is defined by trailing edge of a short gap and record prep.**
- **End of track is defined by not long gap, record holdover and check area.**

Write mode format recognition circuit text is based on an assumed HAO-CE operation that causes the format recognition circuits to identify all track areas with format track signals. (Other operations cause portions of the data track to be read for the address compare cycle; during the compare cycle the recognition circuits operate in read mode).

Recognition circuit operations begin when the long gap trailing edge following late index causes the address area trigger to set (Figures 47 and 48). The address area trigger starts the timing circuits in hold phase, and the resultant timing pulses are used to set the check prep trigger. Check prep gates the next short gap signal to set the check area trigger and reset the address area trigger. During check area, the check prep trigger is reset and the record prep trigger is set. Timing pulses are used to reset the check area trigger.

Record area (HA2), following the first address area (HA1), is identified when the record prep trigger output gates the next short gap trailing edge signal; the record area trigger and the record holdover triggers are set. Identification of the related check area occurs when the check prep trigger, set during record area AGC, gates the next short gap signal to set the check area trigger. During check area, timing pulses are used to reset the check prep trigger and to end check area. Following HA2 check area the format recognition cycle repeats. The next long gap trailing edge sets the address area trigger, and the operation remains cyclic until the end of the programmed operation occurs.

Read Mode Format Recognition

- **Not effective on a read HAO operation.**
- **Address area is defined by trailing edge of a long gap on format track.**
- **Check area is defined from data track by missing sync bit indication from phase select circuit.**
- **Record area is defined by trailing edge of a short gap on the format track and record prep.**
- **Read gate is defined by a data gap singleshot (6.6 μs) which times out in gap after AGC burst on data track.**
- **End of track is defined by not long gap, record holdover and check area.**

The read mode format recognition circuit is based on an assumed track operation (TRO) which causes the recognition circuits to operate in read mode for a complete disk revolution. Recognition circuit operations begin when the long gap trailing edge causes the address area trigger to set (Figures 48 and 49). The address area trigger starts the timing circuits in hold phase, and the resultant timing pulses are used to set the check prep trigger. The check prep trigger is used to sequence the recognition logic to identify the next check area. The hold phase trigger is reset at B1 of D1, which causes the delay line pulse generator timing to stop at BS of D2 (Figure 49, line 1, read timing). A data track gap sensor singleshot locates the gap that separates data AGC bits from read data. The data track gap sensor output sets the read gate trigger when the data gap sensor locates the gap and times out. The read gate trigger causes the address data (HA1) to enter the read data path in the 7631 logic and the machine timing circuits. Timing pulses are developed synchronously with the read data until the last of the related check characters are read.

The format recognition circuits operate in the same way to identify address area and record area in read and write mode. While the address data is read, the timing circuits monitor read data in search of the missing bit-sync; the missing sync gap precedes the last character of address or record data. When the timing circuits have detected the missing bit-sync, the three zeros triggers are reset to recognize the last address or record character (Figure 49). At bit-sync ½ B (BS1/2B) of the first check character, the three zeros and the check prep triggers cause the format recognition logic to signal check area (Figure 49, line 8). Check area causes the 7631 to read the check characters, set the record prep trigger (if not in a long gap), and reset the check prep trigger. The check area trigger is reset at B5 of D6.

The record area following check area is recognized the same way in both read and write mode. The record prep trigger and the short gap signal set the record area trigger. The record area trigger causes the record holdover trigger to set. Record area and timing pulses cause the record prep trigger to reset and the check prep trigger to set. Again, the record area missing bit-sync causes the three zeros triggers to reset and enables check area identification. The recognition cycle repeats when the next address area is recognized. The recognition cycle continues until the programmed operation end occurs.

Format Skew Detector

- **Used to help define check area when writing.**
- **Compensates electronically for mechanical timing variations (skew) between clock track and format track.**
- **Prevents writing one character short if format appears early.**
- **File adaptor circuit check if skew circuit fails.**
- **File frame circuit check if skew is excessive.**

The format skew detector compensates electronically for mechanical timing variations in the 1301 during write operations.

Write timing is generated from two basic sources:
1301 Clock track
Format tracks

AREAS ARE SYNCED BY SYNC
+STOPED BY missing SYNC Detection

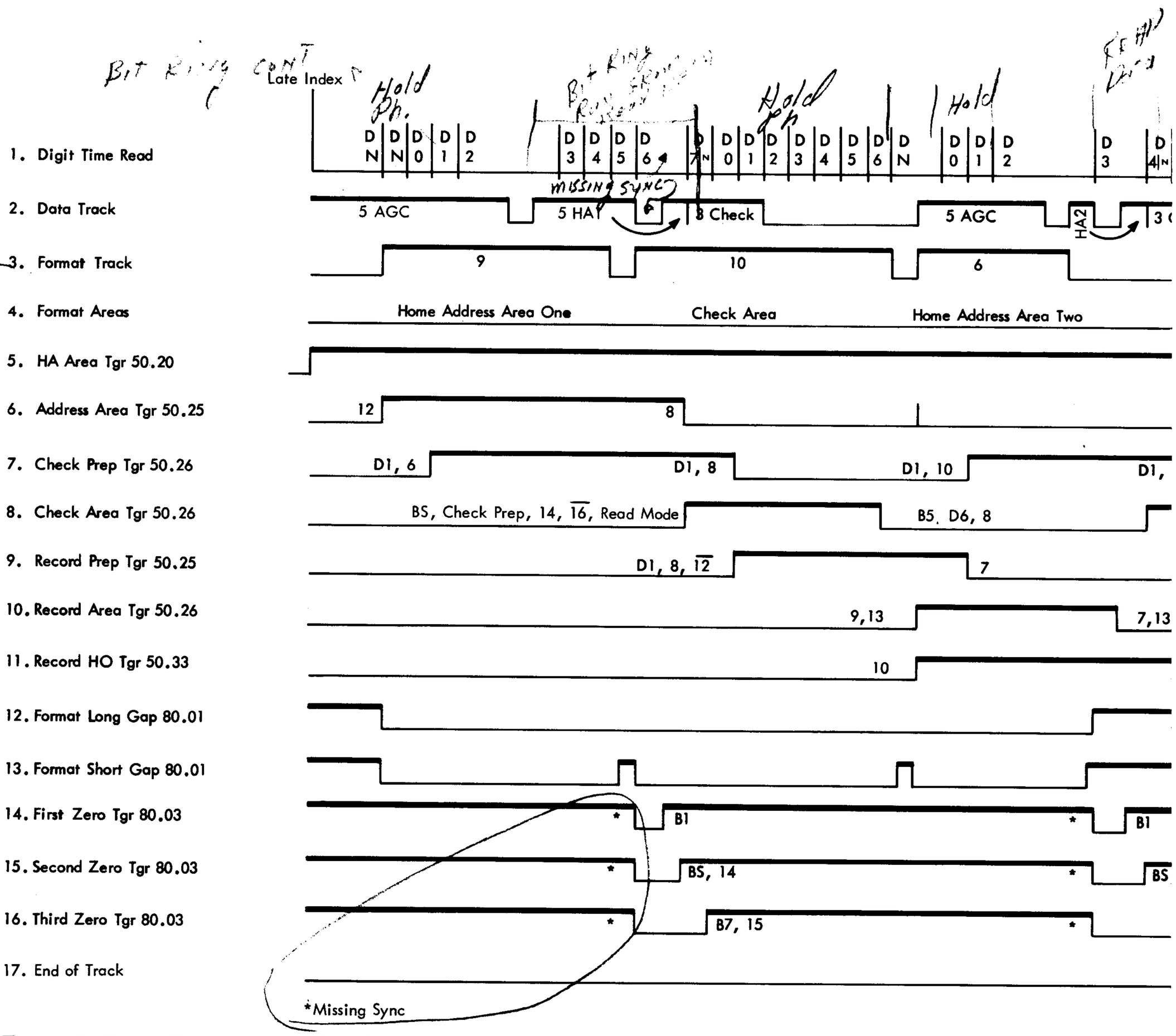
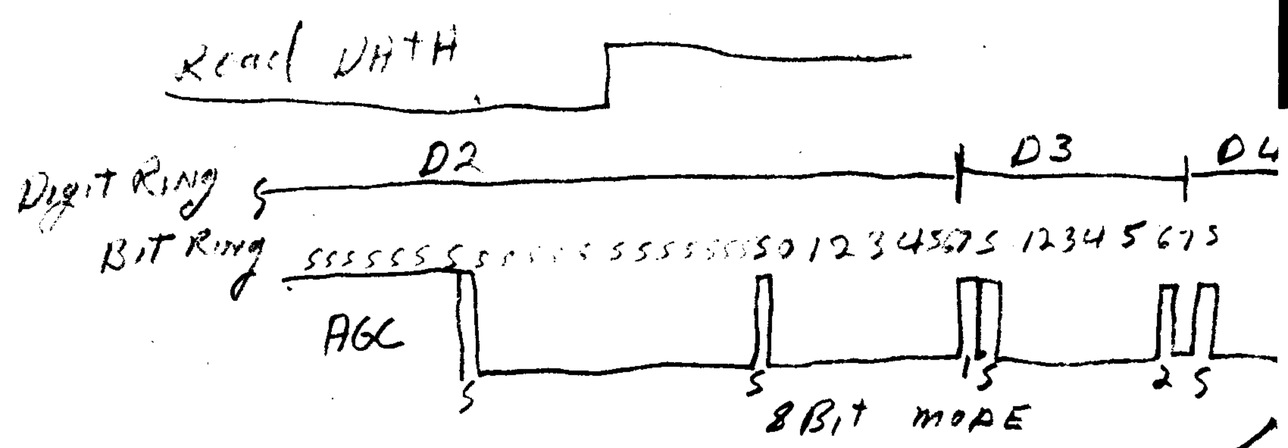
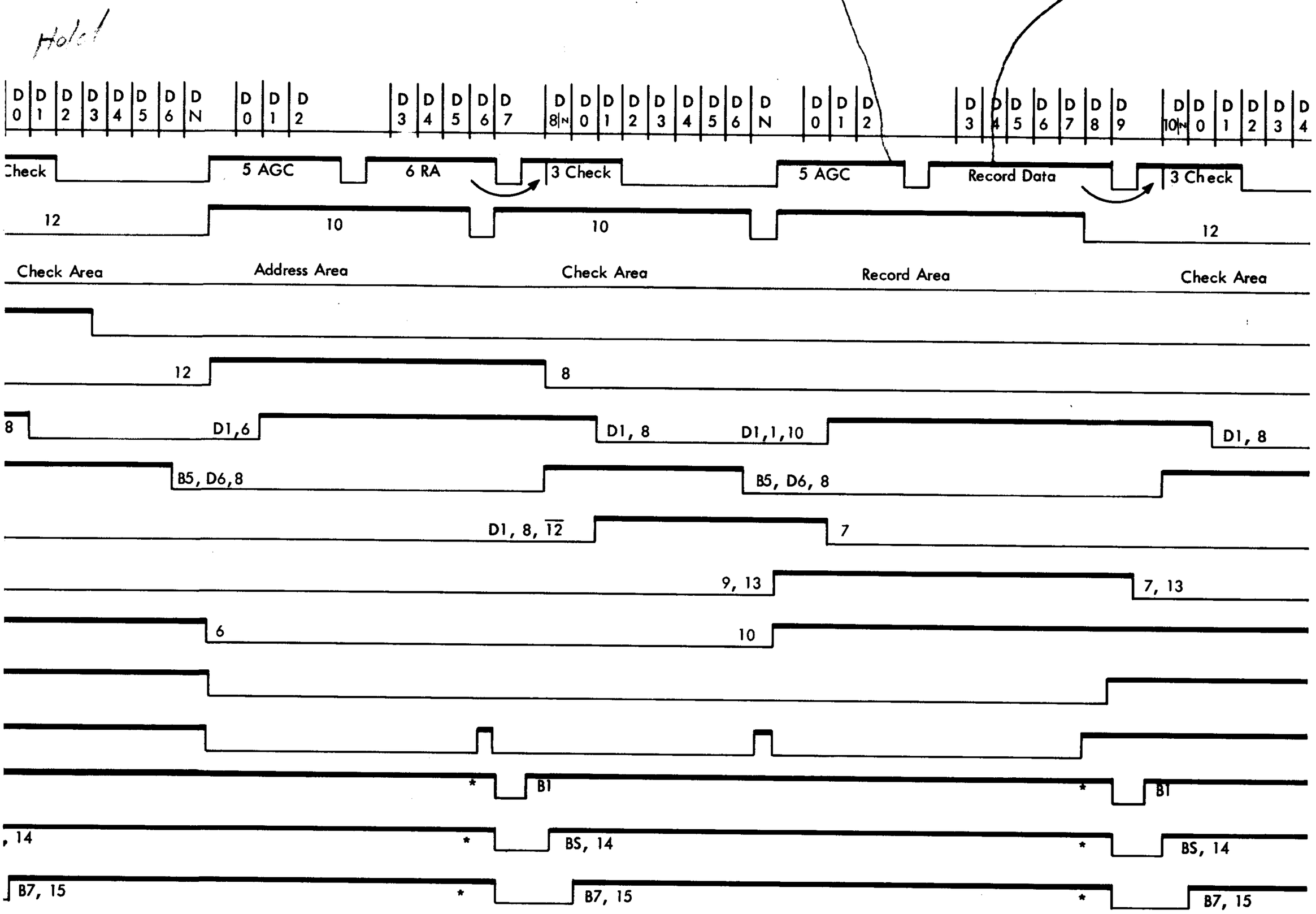


Figure 49. Format Recognition-Read Mode—Not HAO CE

Read Op. = Not HAO

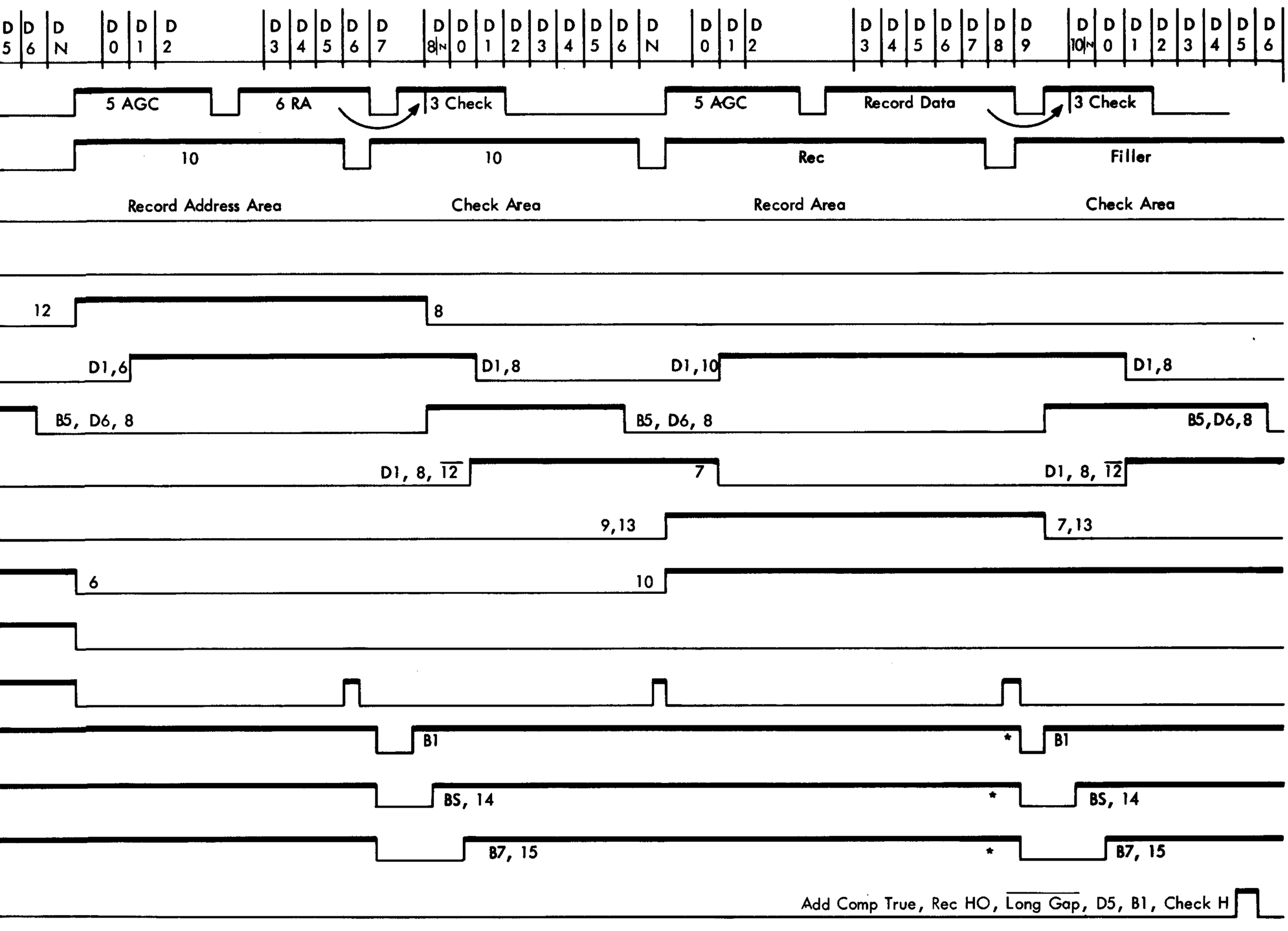
1. ADDRESS AREA - TRAILING EDGE Long Gap
2. CK AREA - MISSING SYNC + 3 ZERO TGRS (MISSING SYNC +2
3 RECORD AREA - TRAILING EDGE of Short Gap + REC. PREP





Char Times) + CK Prep.

Digit RINT
Stepping on Read gp.



Two separate read heads sense the clock and format track outputs. These heads are not rigidly mounted and their relationship may not remain constant under all conditions. For example, if the format head vibrates and moves against the rotational direction of the array, format bits are read at a faster rate than clock track bits. This tends to compress or shorten the format area and causes the short gap to be recognized early in relation to clock track (write data) timing; this is called a format early condition.

If the format head vibrates and moves with the rotational direction of the array, format bits occur at a rate slower than clock track timing. This tends to expand, or lengthen, the format area and causes the short gap to be recognized late in relation to clock track (write data) timing; this is called a format late condition. If no mechanical displacement exists between the clock and format heads, the format bits are synchronous with the clock track (write data) timing; this is called a format equal condition.

The format skew detector permits the 7631 to accurately locate check area when the format equal, early, or late condition exists.

Format Equal

The following explains write data check area recognition for each of three possible conditions. It assumes that the format skew circuitry does not exist, and shows the problems that the skew detector solves. Figure 50, Example A, shows the format equal condition, the ideal relationship where no mechanical or electronic skew exists. Assume a six-character record, char-

Figure 50. Format Equal, Early, and Late

acters C1-C6, is to be written. (Only that portion of the sequence chart that occurs after the end of format is pertinent.) Example A shows that the last format bit occurs at BS of write data character C5. The short gap singleshot times out and causes the generation of check area write mode at about B1 time of C5. When check area write mode is sensed, the digit ring is reset to DN. A data strobe (or service request) is generated during C5 to transfer the sixth and last character, C6, into the I-O register. At B7 of write data character C5, the digit ring is stepped to D0. The coincidence of check area write mode and D0 generates suppress sync. Suppress Sync blocks the write bus and data strobe (or service request) during D0 and creates a no-bit character or gap (G). At B7 time of D0 (gap G), the digit ring steps to D1; the last character, C6 (placed in serial register during BS of D0), is written (Figure 50, Example A). The check character gap (not shown) is generated and the three check characters are written after the last data character.

Format Early

Figure 50, Example B, shows a format early condition that would cause a write data failure. Example B shows that the last format bit occurs at B3 time of write data character 4, C4. The short gap ss times out and generates check area write mode at B5 of C4. The digit ring is reset to DN when check area write mode is sensed; the digit ring is stepped to D0 at B7 of C4. A data strobe (or service request) generated during C4 transfers data character C5 into the I-O register. The coincidence of D0 and check area write mode generates suppress sync. Suppress sync blocks the write bus and data strobe (or service request) during D0 and creates a no-bit character or gap (G). In this example, the gap (G) is created one character early, and the last data character (C6) is not written.

Format Late

Figure 50, Example C, shows a format late condition that would cause a write data failure. Example C shows that the last format bit occurs at B7 of write data character C5. The short gap ss times out and generates check area write mode at B0 time of C6. The digit ring is reset to DN when check area write mode is sensed; the digit ring is stepped to D0 at B7 of C6. An extra data strobe (or service request) is generated during C6 because suppress sync is generated too late. The digit ring steps to D0 at B7 of character C6. The coincidence of check area write mode and D0 will generate suppress sync, which blocks the write bus and creates the gap (G). The gap is created a character late and an extra strobe character, or service request, is issued. The bit configuration of the extra character depends on the using system and/or the length of the record.

The format skew detection circuitry compensates, within limits, for format early and format late conditions. If the skew exceeds these limits, the format skew detector indicates an error. The time that check area write mode is sensed determines: when that suppress sync is to be generated, when the digit ring is reset to DN, and when suppress sync creates the gap between the main body of an address or record and its last character.

The format skew detector consists of a format bit ring (binary counter) and the format early trigger; the skew detector compares format bit timing to clock disc (write data) timing (Figures 51 and 52). If format is early or equal, the format early trigger is set. If format is late, or format bit-seven (FB7) and BS are sensed, the format early trigger is reset. With the addition of the format skew detector, the format early trigger must be reset to generate check area write mode. The format skew detector adjusts the time that the check area write mode is recognized and indicates a failure (FF circuit check), if the skew exceeds the detector adjustment limits. The format bit ring (binary counter) is checked for proper operation; and if it steps incorrectly, an error condition (FA circuit check) is indicated.

Skew Detector Timing

Format Equal

Assume the last format bit (FB7) was sensed at BS of write data character C5, the format early trigger resets at BS1/2A (Figure 53, Example A). (Format early trigger must be reset to generate check area write mode.)

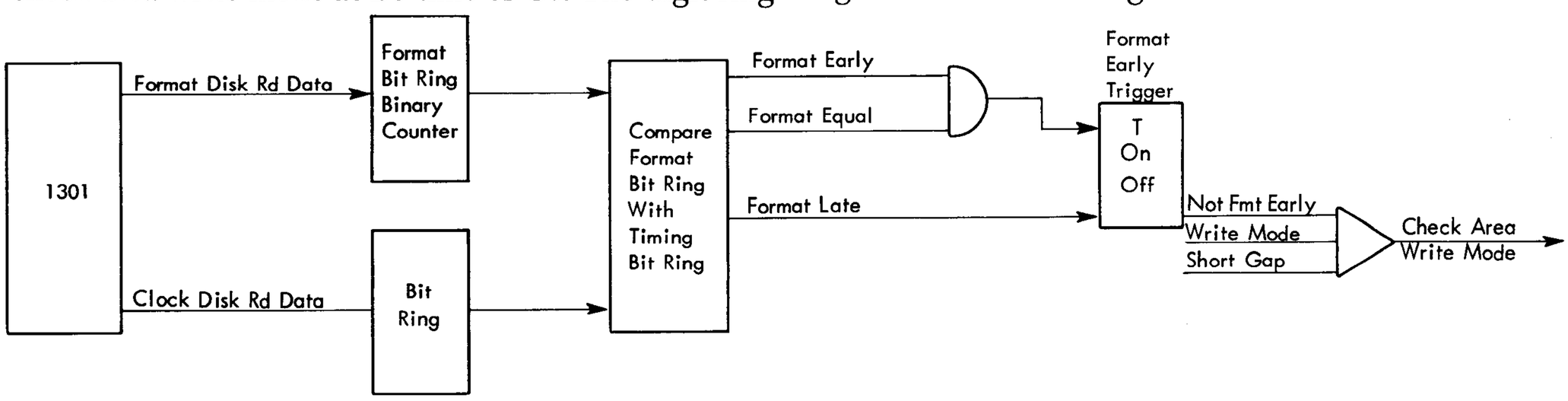


Figure 51. Format Skew Detection Circuits

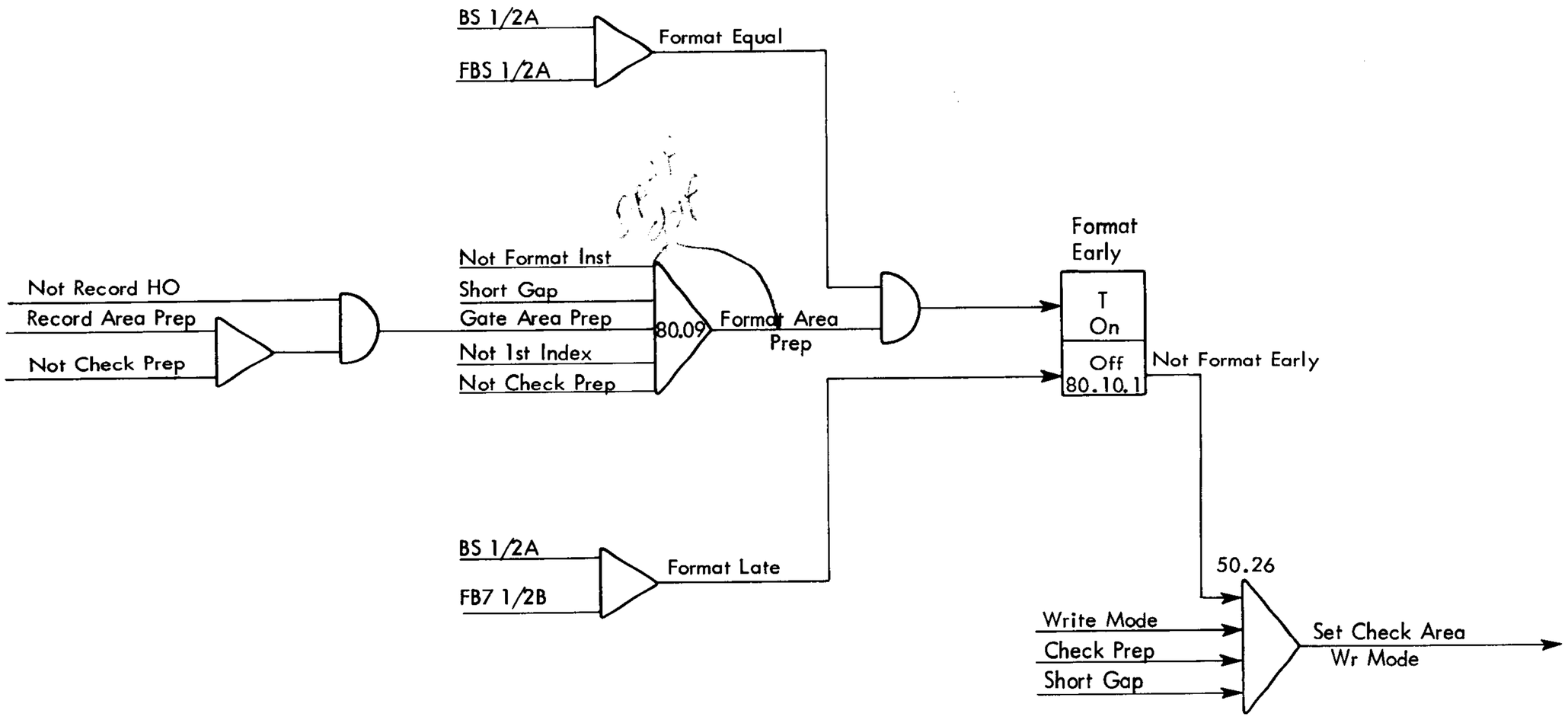


Figure 52. Format Skew Detector

The short gap singleshot times out at B1 of C5. The conditions required to generate check area write mode, format early trigger off and short gap are satisfied (Figure 52).

When check area write mode is sensed, the digit ring is reset to DN. At B7 time of character C5, the digit ring stepped to D0; suppress sync line (not shown) is generated and writing is suppressed to create gap G. The bit ring continues to run in the gap and at B7 time of the gap the digit ring steps to D1. Because writing is only suppressed during D0 with check area write mode active, write data character C6 is written. The check character gate (not shown) is generated to allow check character writing during D2, D3, and D4.

Because the short gap was detected after the coincidence of BS1/2A and FB1/2B, the format early trigger is reset; the last format bit steps the format bit ring to B7, where it remains. Short gap detection causes check area write mode at the same time the short gap is detected. Check area write mode must be generated during the character cycle preceding the last character of each address or record for correct operation.

Format Early

The last format bit FB7 occurs at B4 time of character C4 (Figure 53, Example B). The short gap is detected during B5 of character C4. If check area write mode is signalled at this time, character C6 is deleted. Check area write mode cannot be signalled until FB71/2B and BS coincide. This coincidence occurs at BS time of character C5. At BS of C5, the format early trigger is reset and satisfies the not format early condition needed to generate check area write mode (Figure 52). Check area write mode is generated at BS time of character C5. Check area write mode must be generated during the character cycle preceding the last character of each address or record area for correction operation.

Format Late

The last format bit FB7 occurs at B4 time of character C5 (Figure 53, Example C). The format early trigger is turned off during BS of character C3, with the format late in reference to write data timing. When short gap is sensed, the circuits signal check area write mode (Figure 52). Short gap is sensed at B5 of character C5. Check area write mode must always be generated during the character cycle preceding the last character of each address or record area for correct operation.

Error Indications

If the format data timing is too early (with relation to write data timing), and a coincidence of FBS1/2A and BO1/2A occurs, a FF circuit check is indicated.

If the format data timing is too late (with relation to write data timing), and a coincidence of FBS1/2A and BS1/2B occurs, a FF circuit check is indicated (Figure 54).

The format bit ring should always stop at FB7 and short gap should be recognized about three microseconds later (Figure 53, Example A). If short gap is recognized with the format bit ring at a position other than FB7, the format ring has stepped improperly and a FA circuit check occurs (Figure 54).

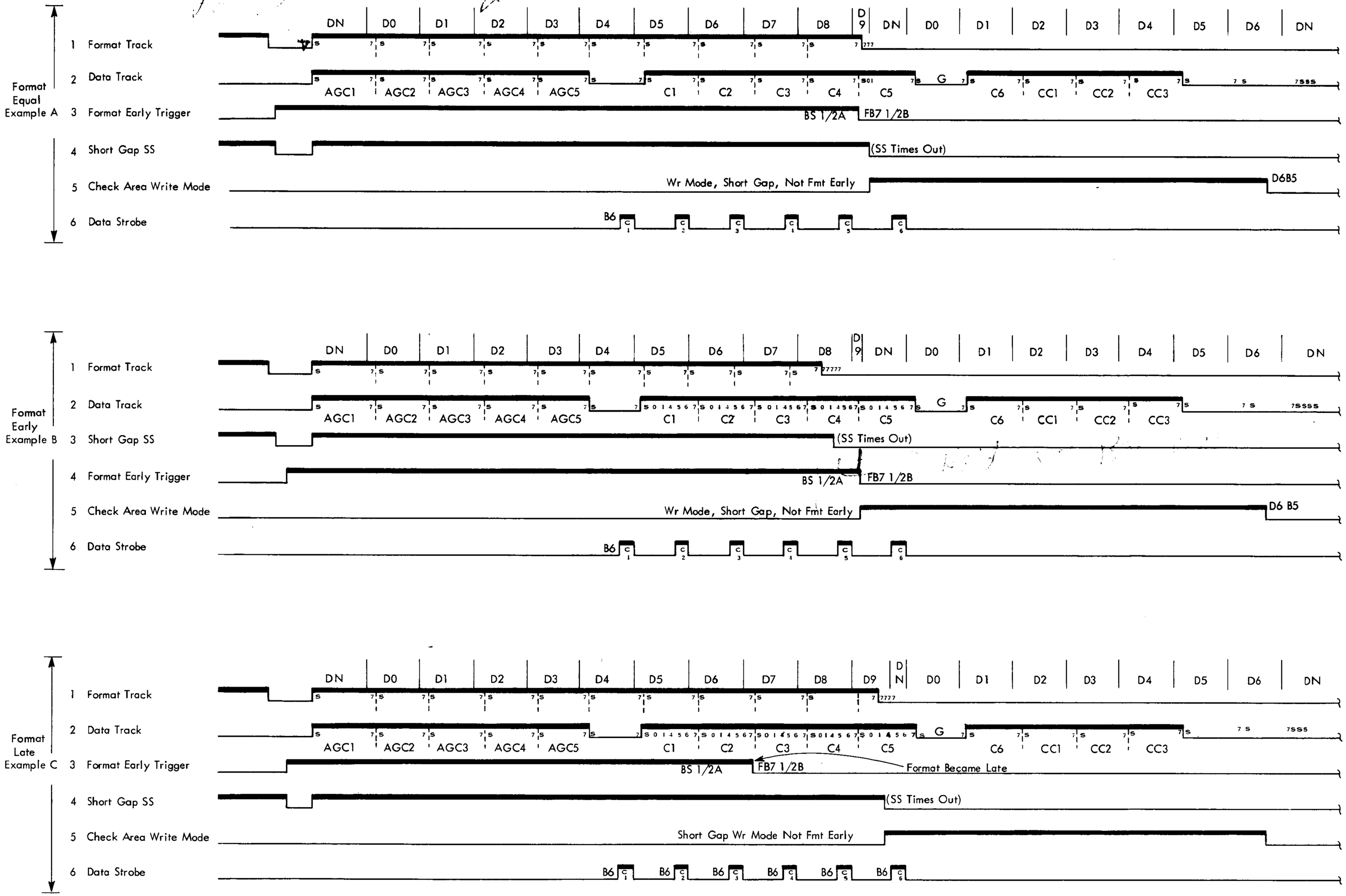


Figure 53. Format Skew Timing

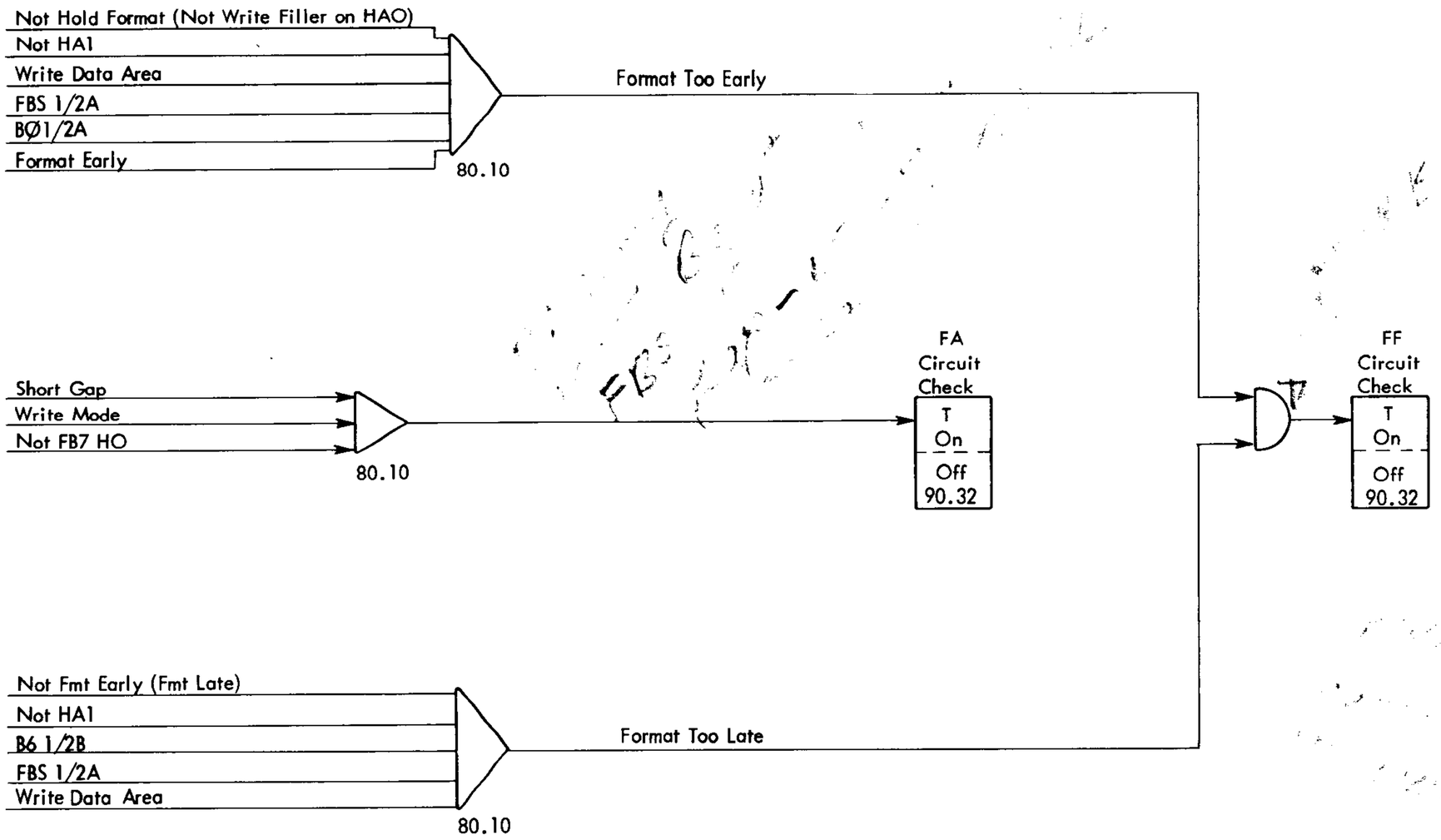


Figure 54. Format Skew Errors

Format Binary Counter

The format binary counter develops format bit timing from input format read data. The timing outputs are: format bit sync 1/2A (FBS1/ +2A), format bit seven (FB7), and format bit seven holdover (FB7HO). When the 1301 clock track and format track are in step (no skew), the format bit timing is coincident with bit ring timing. Format read data has less logic delays than clock track timing; therefore, the write data area begins with the format early trigger set.

The format binary counter starts operation from a lockup condition (Figure 55). The lockup condition permits the counter to be reset in any check area and prevents any remaining format-read one bits, such as those that separate address and record areas, from starting the counter operation before the following record area. Without the lockup AND circuit, the counter would step with format read data before entering a record area.

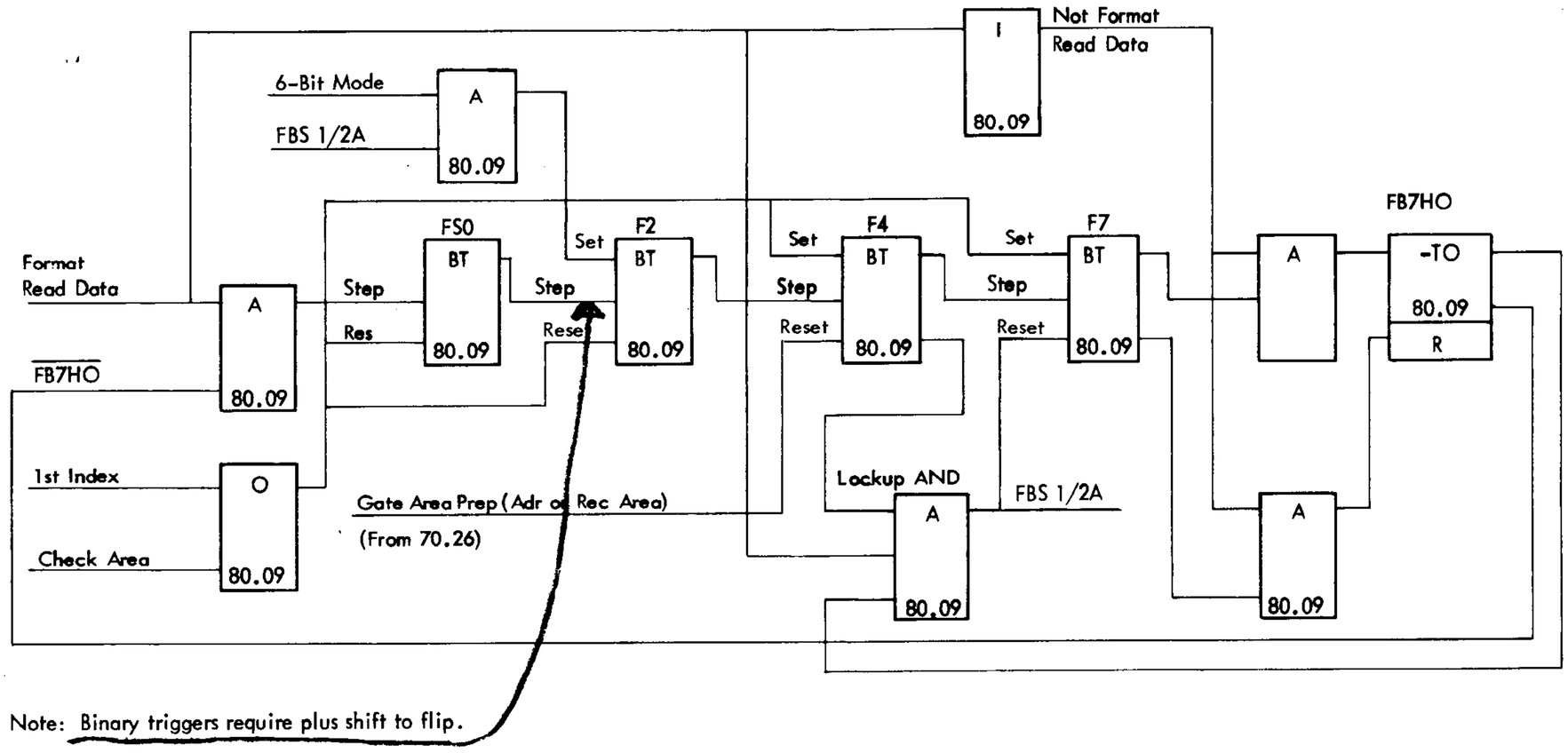
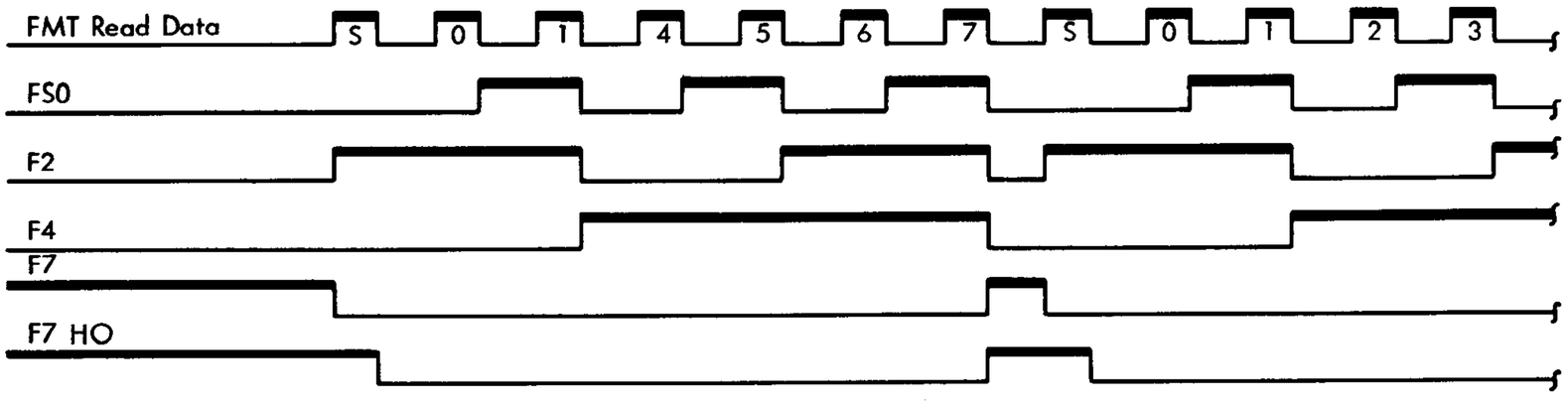
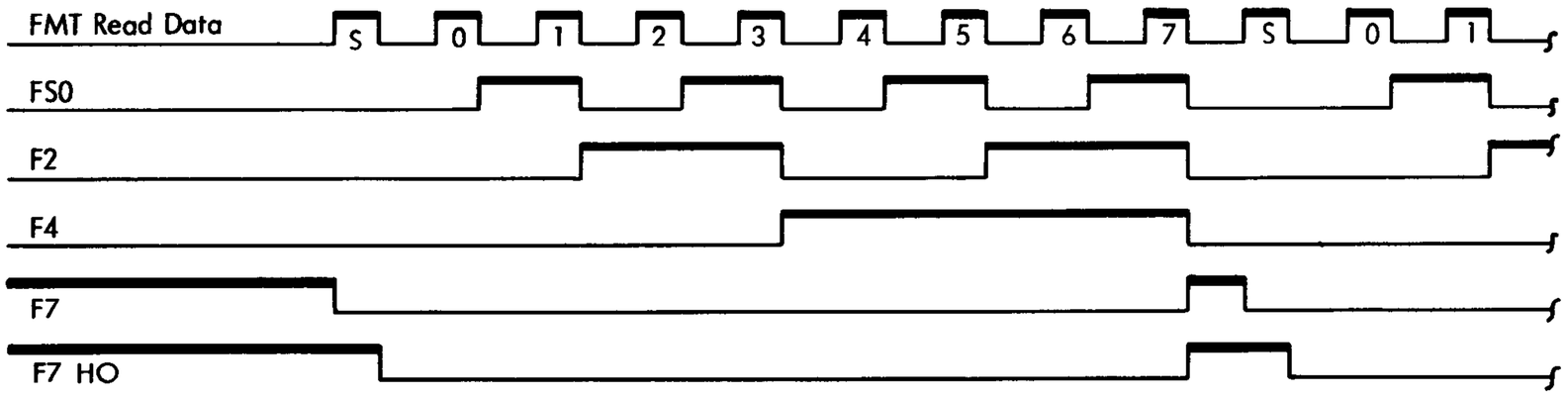


Figure 55. Format Binary Counter



6 BIT MODE



8 BIT MODE

Figure 56. Format Binary Counter Timing

The gate area prep signal conditions the unlock AND, and allows the format read data bits to step the format binary counter (Figure 55). Each format read data pulse steps the counter, and the resultant format timing pulse outputs are used to determine the direction and amount of skew. The counter operates in eight-bit mode (Figure 56). If the 7631 is a six-bit mode, collector pullover is applied at FBS1/2A time to force the F2 trigger to set, shortening the count sequence by two pulses for six-bit mode operation.

Counter operation is monitored to determine whether it is counting correctly; a file adapter circuit check occurs if the counter stops operation with any output except FB7HO in any gap area (Figure 54). The short gap and write mode signals gate the not-FB7HO signal to indicate file adapter circuit check and cause the 7631 to issue an immediate unusual end.

Compare Circuit

- **Compare serial read and write data bit by bit and indicate compare fail if input bits are different.**
- **Compare fail during address verify cycle indicates no record found.**
- **Not a compare fail during address verify cycle indicates compare true and allows a read or write data cycle to follow.**
- **Compare circuit tested during address verify cycle; if bad indicates a file adaptor circuit check.**
- **Data not compare during check character time of read data cycle indicates parity.**
- **Data not compare during write check operation indicates write check error.**

The compare circuits compare data bit by bit to insure the validity of read or write data. The compare circuits compare check characters read from a selected data track with check characters generated when the data is read. The compare circuits compare write data with read data to verify the previous write operation (Figure 30). The compare circuit uses exclusive ORS to compare data (Figure 57). A compare failure occurs when the input compare bits are different. A no compare signal is generated for every compare failure; how the error is processed depends on the machine cycle in progress when the error occurred.

The compare circuits are tested prior to use in HA1 and SRO verify address cycles. Two tests are performed to insure the compare circuits are operating correctly before their use. Test not compare A signal, generated at D0 time, sets data trigger A to simulate a read one bit. The simulated read one bit is transferred to data trigger B, and the output of data trigger B is compared with the write data line. Because there is no write data, a compare failure occurs: the compare fail signal sets the compare fail trigger. A test follows to determine the status of the compare fail trigger at B4 time. If the compare fail trigger is not set, a file adapter circuit check occurs. The file adapter circuit check indicates the compare circuits cannot detect a compare failure, and the test failure causes the 7631 to issue an immediate unusual end.

Test not compare B, generated at D1 time, compares a simulated write one bit with a read zero bit. The bit timing used for this test is the same as in test A. If the compare fail trigger is not set, it causes a file adapter circuit check, and the 7631 issues an immediate unusual end. Following each successful test the compare fail trigger is reset. (Figure 57 relates the compare circuit to the 7631 error circuits.)

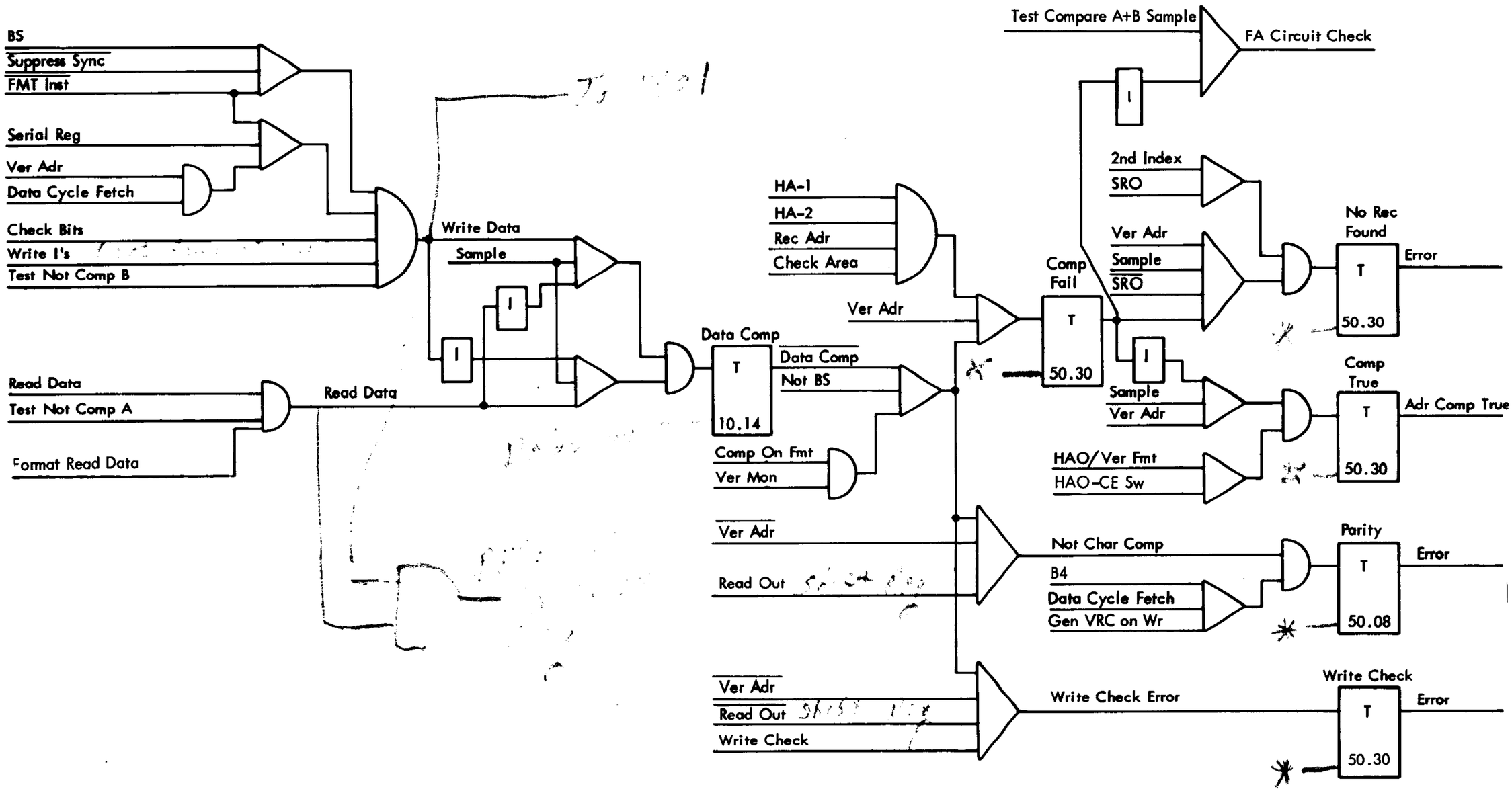


Figure 57. Compare Circuit

Interfaces

- **Interface is the signal and control lines between the system and 7631 file control.**
- **1410 uses a 1410 type of operation.**
- **All 7000's use a standard interface type of operation.**

This section of the manual contains a detailed description of the 1410 I-O interface and the standard interface, and the information relating the system commands, orders, and instructions that are transmitted on the interfaces. Because each 7631 model is designed to attach to specific types and numbers of data processing systems, there are five models:

Model 1—for use with a 1410 system
Model 2—for use with a 7000 system
Model 3—for shared use with a 1410 and a 7000 system
Model 4—for shared use with two 7000 systems
Model 5—for shared use with two 1410 systems

NOTE: In the preceding list of models, the term 1410 system refers to either a 1410 or a 7010 system, and the term 7000 system refers to any one of the following systems: 7040/44, 7070/74, 7080, or 7090/94.

The 7000 systems attach to the 7631 with the standard interface; and both 1410 and 7010 systems attach to the 7631 with the 1410 type of I-O interface. Because the main 7631 model differences are the type and number of systems that can be attached, the 7631 circuit differences are confined to the interface and shared system circuits.

1410 I-O Interface

The 1410 I-O interface permits the attachment of either 1410 or 7010 data processing systems to the 7631 models 1, 3, and 5. Model 1 permits either a 1410 or 7010 system to attach to the 7631 (Figure 58). Model 3 permits either a 1410 or a 7010 and one of the 7000 systems to attach to the 7631 (Figure 59). Model 5 permits the attachment of two 1410, or two 7010, or one 1410 and one 7010 system to the 7631 (Figure 60).

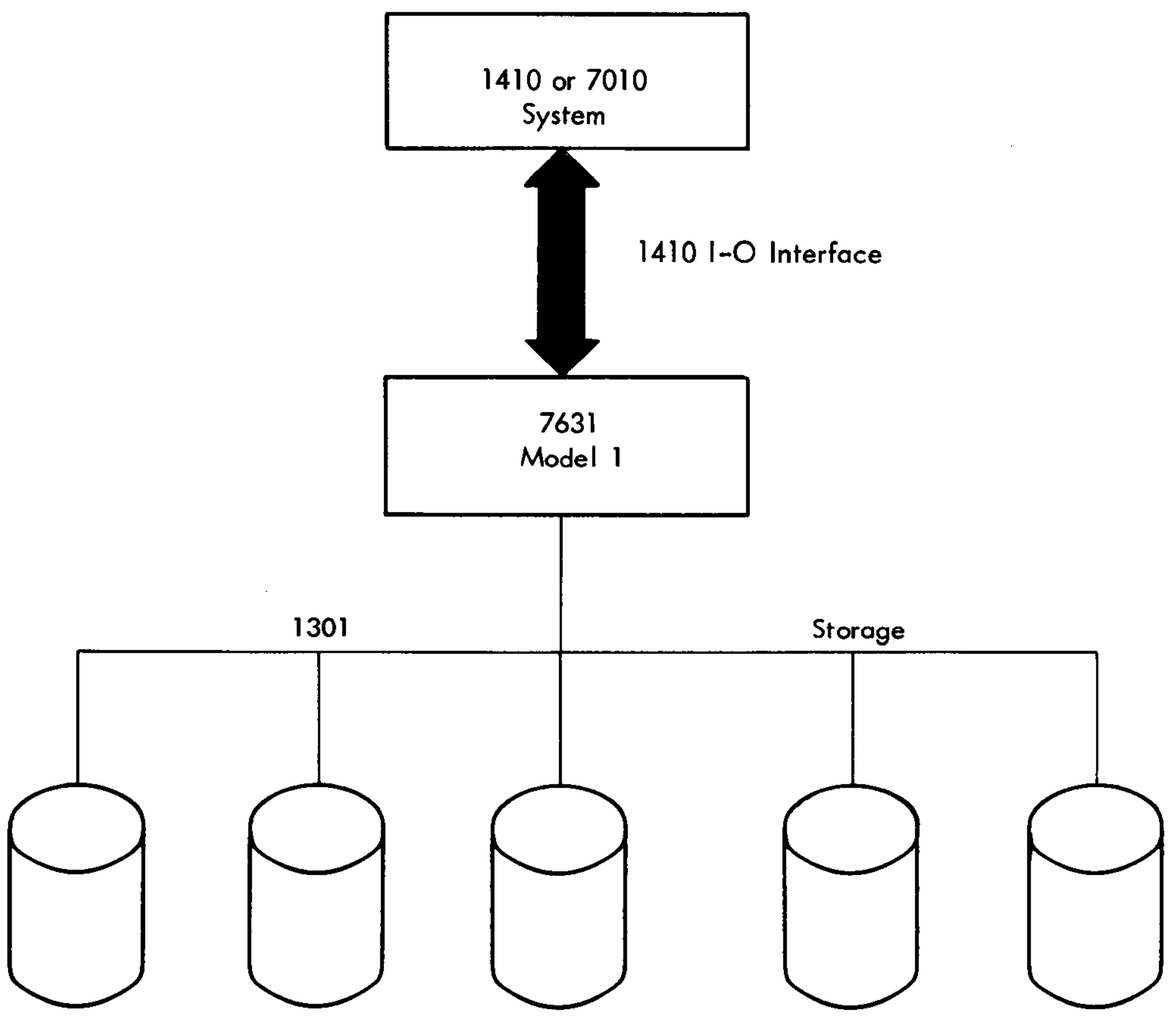


Figure 58. 7631 Model 1

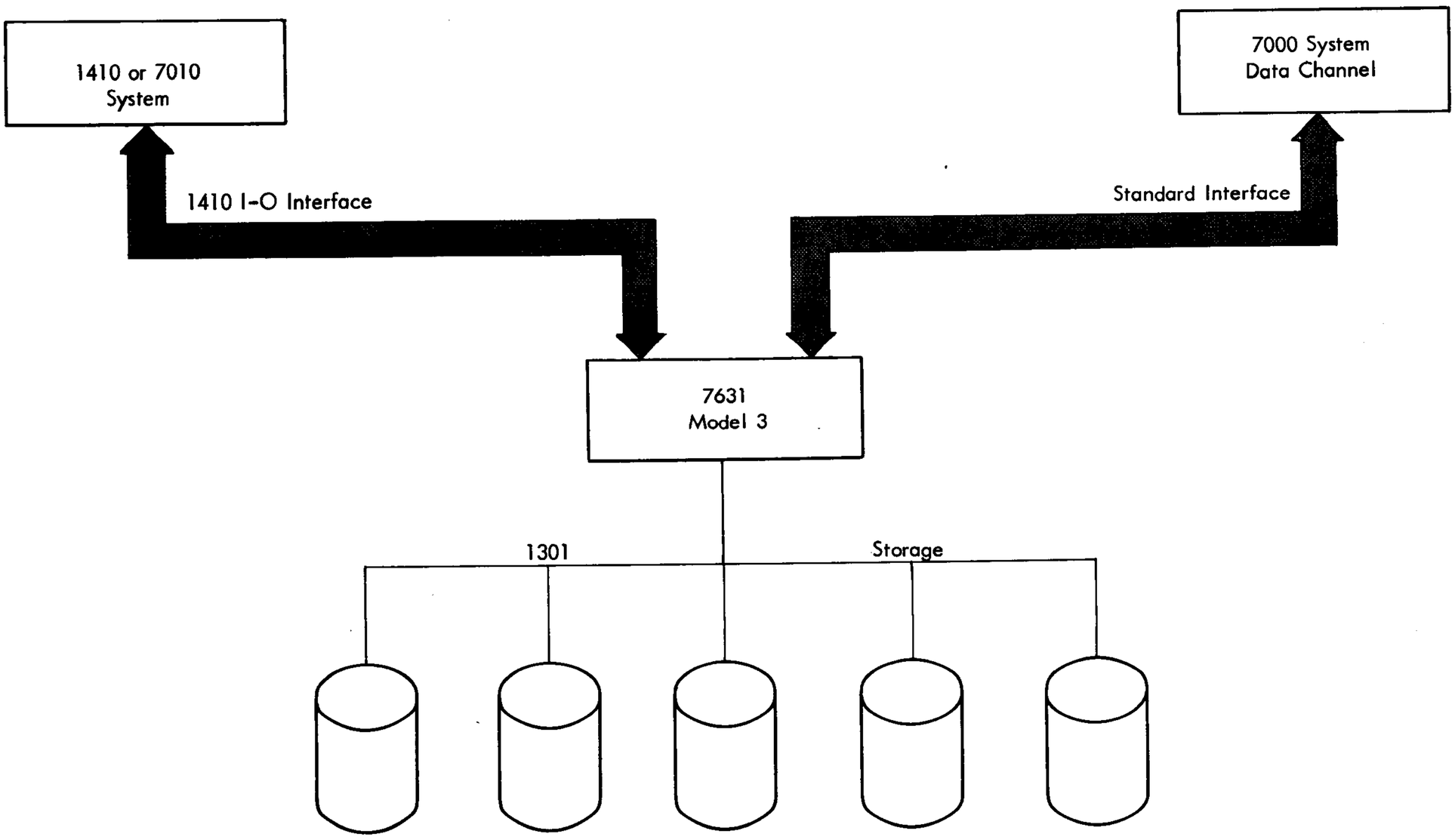


Figure 59. 7631 Model 3

1410 I-O Instruction

- **Operation code must be an M or L and specify bit mode.**
- **X control field contains channel, unit select and unit number register.**
- **B address locates control word in memory (8 characters plus GM-WM).**
- **D character (op modifier) specifies read, write or no-op.**

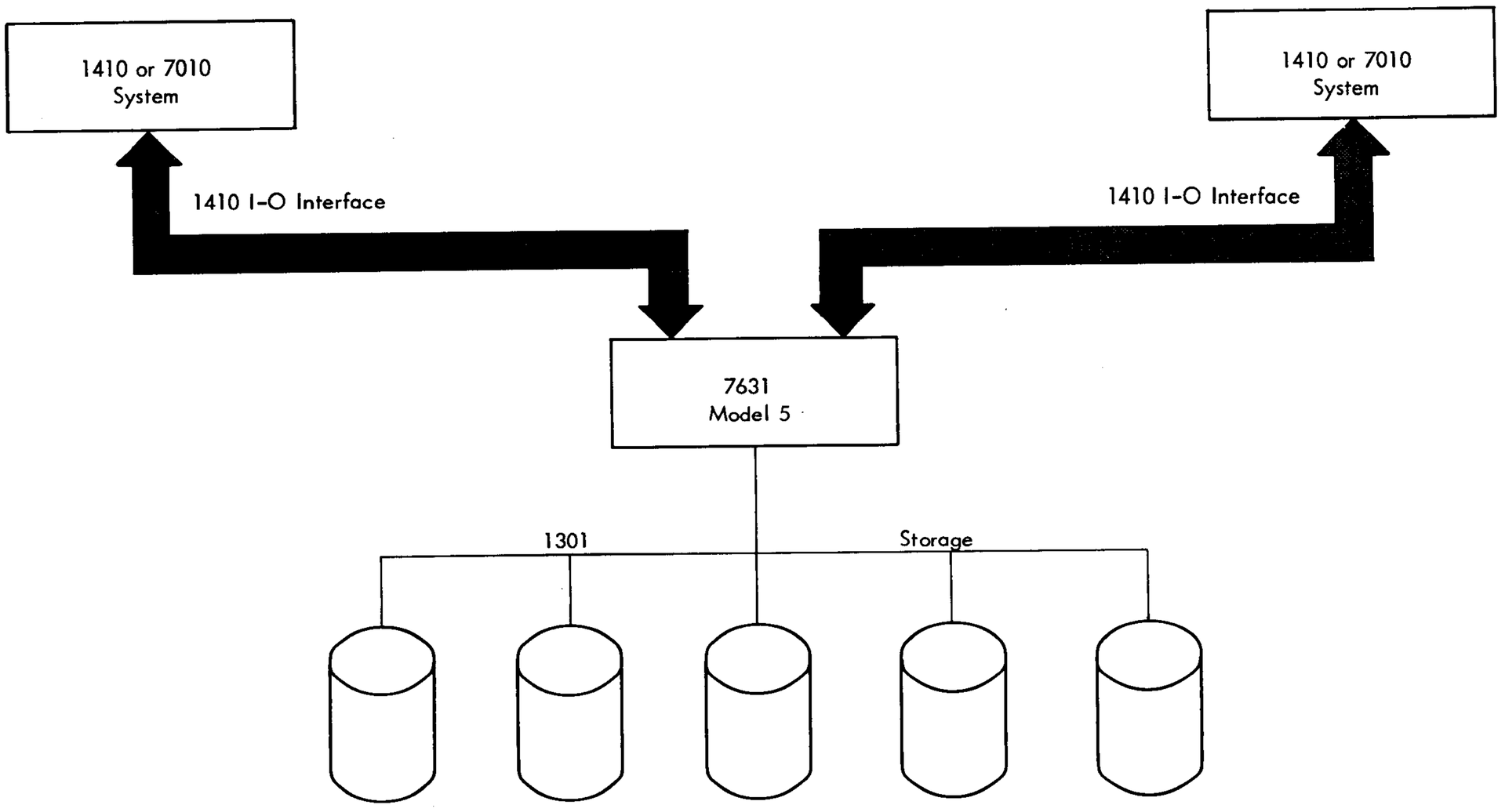


Figure 60. 7631 Model 5

The operations performed by the 1301 disk storage with 7631 file control are started by the 1410 instruction shown in Figure 61. The function of each part of the 1410 instruction follows.

Operation Code: Every file instruction has a move (M) or load (L) operation code. The move operation code specifies six-bit mode operation to the 7631. Since the file control normally operates in six-bit mode, no signal is needed to indicate six-bit mode to the 7631. The load operation code specifies eight-bit mode operation to the 7631. The load signal conditions the 7631 for eight-bit data transfers.

X-Control Field: The high-order position of the X-control field, the channel select register, selects the channel and specifies either overlap or non-overlap status in the 1410.

The second position of the X-control field, the unit select register, is always an F for file operation. The file operation signal starts the 7631 control cycle. The low order position of the X-control field, unit number register, specifies the order (type of 7631 operation) to the 7631.

B-Address: The B-address portion of the 1410 instruction addresses the high-order position of the disk control word. The control word is always followed by a group mark with a word mark (GM-WM). File read and write data are stored following the 1410 control word in core storage.

D-Character: The R and W op modifiers signal read and write to the 7631. The read and write data fields end with a GM-WM, or the end of core storage if it occurs first. When the $ or X op modifier is used to define read or write to the 7631, the 1410 data field is defined by the end of core storage indication. If a Q or V op modifier is used, the 7631 executes a no-op operation.

When the 1410 processes a 1301 disk instruction, the B-field control word is transferred to the 7631. The control word is transferred via the 1410 read-write bus. When a 1410 data field is required, the 1410 data field is stored adjacent to the control word. Depending on the type of 1301 instruction processed by the 1410, some of the control word characters may not be used by the 7631; the unused characters must be valid characters to prevent a 7631 parity error. (Figure 62 shows the 1410 orders and their related control words.) Because the 7631 is designed for use with many systems, the terms used to describe 7631 operations are different than 1410 program terms. (Figure 63 relates 7631 operation terms to the 1410 instructions.)

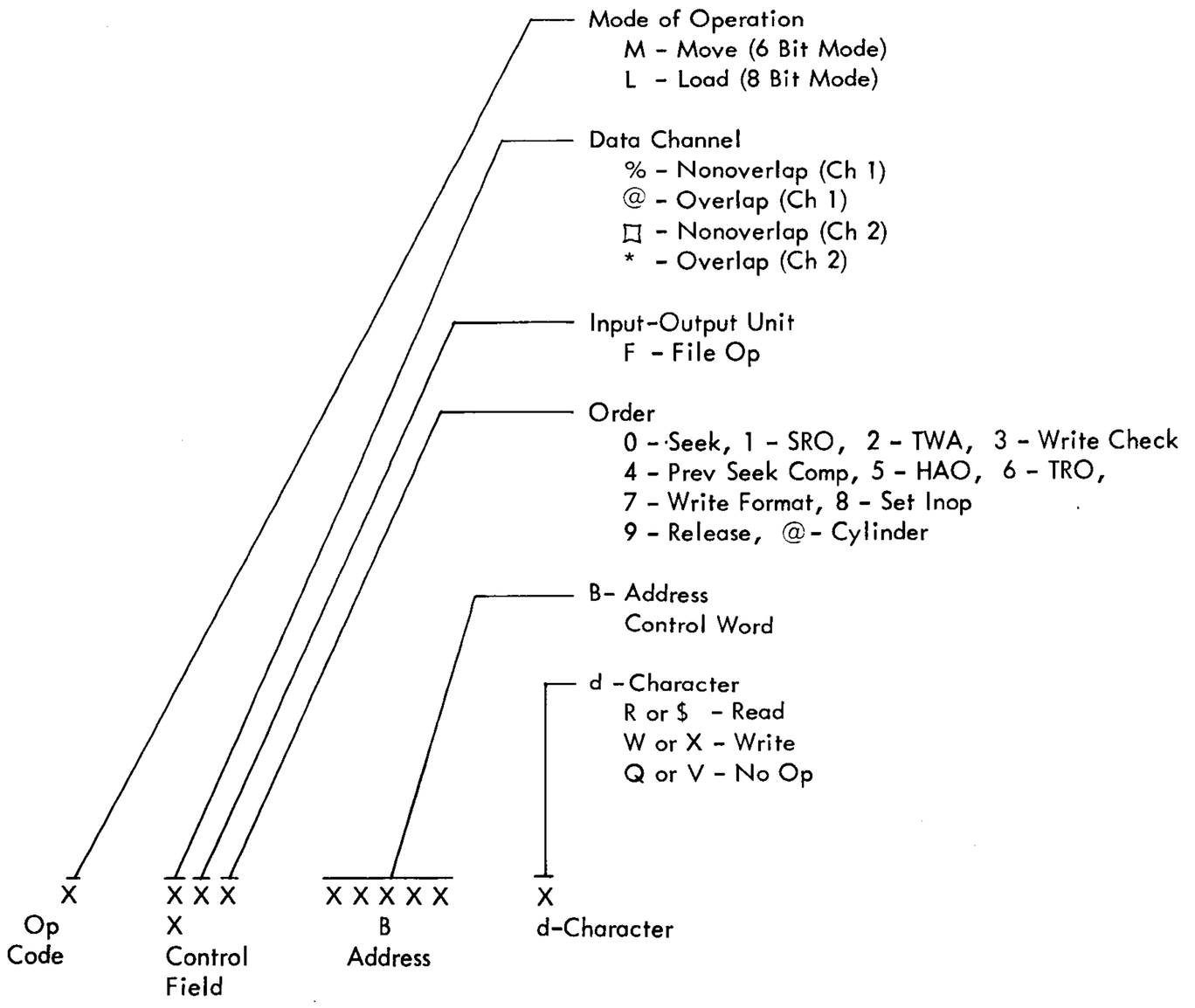


Figure 61. 1410 Disk Storage Instruction Layout

Seek	A	M	H	H	H	H	U	U	‡
SRO	A	M	R	R	R	R	R	R	‡
TWA	A	M	H	H	H	H	I	I	‡
Wr Ch	Note 1								‡
PSC	‡	Note 2							
HAO	A	M	H	H	H	H	U	U	‡
TRO	A	M	H	H	H	H	I	I	‡
Wr Format	A	M	H	H	H	H	U	U	‡
Set In Op	A	M	U	U	U	U	U	U	‡
Rel	‡	Note 2							
Cyl	A	M	H	H	H	H	I	I	‡
No Op	A	M	U	U	U	U	U	U	‡

Code -
- A - Access
- M - Module
- H - Track Address (HA1)
- R - Record Address (SRO Only)
- I - Random Record (HA2)
- U - Unused (Must be Valid Char)

Note 1 - The control word for a write check should be the same as the order being checked.

Note 2 - The PSC or Rel order addresses a group mark with word mark.

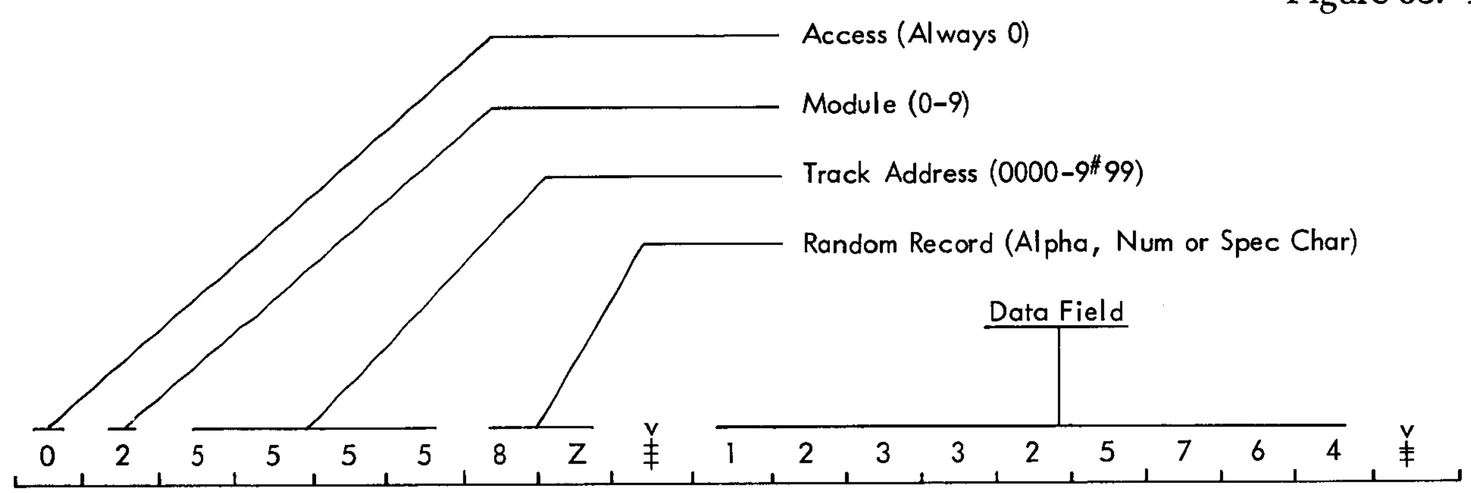


Figure 62. 1410 Control Word-Data Layout

1410	Order No.	7631
Seek Disk (SD)	0	Seek
Write Format Track (WFO)	7	Write Format (Wr Fmt)
Write Full Track with Home Addresses (WHA)	5	Home Address Op (HAO-Write)
Read Full Track with Home Addresses (RHA)	5	Home Address Op (HAO-Read)
Write Full Track with Addresses (WFT)	6	Track Op (TRO-Write)
Read Full Track with Addresses (RFT)	6	Track Op (TRO-Read)
Write Full Track without Record Addresses (WDT)	2	Track without Addresses (TWA-Write)
Read Full Track without Record Addresses (RDT)	2	Track without Addresses (TWA-Read)
Write Cylinder (WCY)	@	Cylinder Op (Cyl-Write)
Read Cylinder (RCY)	@	Cylinder Op (Cyl-Read)
Write Single Record (WD)	1	Single Record Op (SRO-Write)
Read Single Record (RD)	1	Single Record Op (SRO-Read)
Write Disc Check (WDC)	3	Write Check (Wr Ch)
Prevent Seek Complete (PSC)	4	Prevent Seek Complete (PSC)
Release (Rel)	9	Release (Rel)
I-O No Operation (N)	Q/V	No Operation (No Op)
Set Access Inoperative (SAI)	8	Set Inoperative (Inop)

Figure 63. 1410-7631-1301 Disk Storage Instructions

1410 I-O Interface Operation

- **Control cycle initiated by file operation from unit select register.**
- **Order set up by unit number register.**
- **Control word gated from B-address location into 7631 address register.**
- **Prep R/W cycle initiated by channel input or output mode latch.**
- **Read or write data field in 1410 follows ≢ after control word.**

File operations are started when the 1411 issues the required signals, operation code, and data to the 7631. When the 1411 processes a 1301 file instruction, the signals, operation code, and data are issued via the 1410 I-O interface. In a typical file operation, the 1411 usually issues:

1. Control signals used to activate the 7631
2. An operation code that specifies the type of 7631 operation
3. A control word that contains eight address characters

To start a file operation the 1411 must read out a 1301 file instruction (Figure 61). At I5 time, the 1411 signals file op to the 7631 (Figure 64, line 4). The file op signal causes the 7631 to start a control cycle (Figure 64, line 5). The 7631 control trigger, set with the 1410 file op signal, causes the 7631 clock trigger to set (Figure 64, line 6). When operating with a 1410 system, the 7631 timing circuits pause and suspend 7631 operation at digit one time; the 7631 waits for the 1411 to complete instruction readout and to fill registers E1 and E2 in preparation for the address transfer. Figure 64, line 6, shows that the 7631 clock trigger is set until digit one. The clock trigger is reset during the time the 1411 prepares to transfer the eight address character control word to the 7631.

On the last instruction readout cycle, I12, the 1411 generates status sample A. Status sample A is used to sample the channel ready and busy buses to determine the status of the 7631 (Figure 64, line 3). If the busy and not ready status latches are off, the 1411 sets the second address transfer latch (Figure 64, line 8). The second address transfer latch starts a 1411 address transfer.

If the op code is release or prevent seek complete, a control word is not required. To prevent the address transfer, the B-field addresses a GM-WM; as a result, the 1411 internal end of transfer latch is set. With release or prevent seek complete (PSC), the file start gate is issued immediately following status sample A to restart the 7631 timing and gate in the 1410 op code. The 7631 issues end op and sets the 1411 external end of transfer latch. The 1411 generates status sample B to sample all six channel status indicators when both internal and external end of transfer latches are set, completing the operation.

If the op code is not release or prevent seek complete, the second address transfer latch causes the 1411 to operate in output mode; when E2 is full, the file start gate is issued to set the 7631 file start trigger. The 7631 file start trigger output sets the clock trigger to restart the suspended 7631 control cycle and causes the 1411 unit number register output, through the 7631 op decoder, to set a 7631 control operation trigger. (For example, set TRO, TWA, etc.). Starting with digit two and ending with digit nine, the 7631 generates eight data strobes and stores the eight-character control word (Figure 64, line 12).

When a GM-WM is read from core storage, the 1411 recognizes internal end of transfer (Figure 64, line 13). Disconnect is not issued, because the 1411 cannot issue disconnect during a file address transfer. The 7631 issues end of address transfer when the control cycle is complete. End of address transfer is issued to reset the 1411 second address transfer latch. (Figure 64, line 1, shows that the control cycle ends at D11.) The 7631 issues end op at the end of the control cycle for the following:

1. If the op code is see, prevent seek complete, inop, no-op, or release
2. If any errors have occurred during the control cycle

The 7631 end op signal sets the 1411 external end of transfer. The internal and external end of transfer latches cause the 1411 to generate status sample B to sample the six status lines and complete the file operation (Figure 64, line 16).

If the op code is a prepare to verify type, end op is not issued to the 1411 when the control cycle completes, and the 1411 switches to input or output mode following the address transfer, according to the instruction d character. The file start gate is issued a second time to set the 7631 file start trigger. The file start trigger output is used to gate the 1411 CPU to file read or write signal into the 7631. The coincidence of CPU to file read or write, file start, and not control cause the 7631 read or write trigger to set.

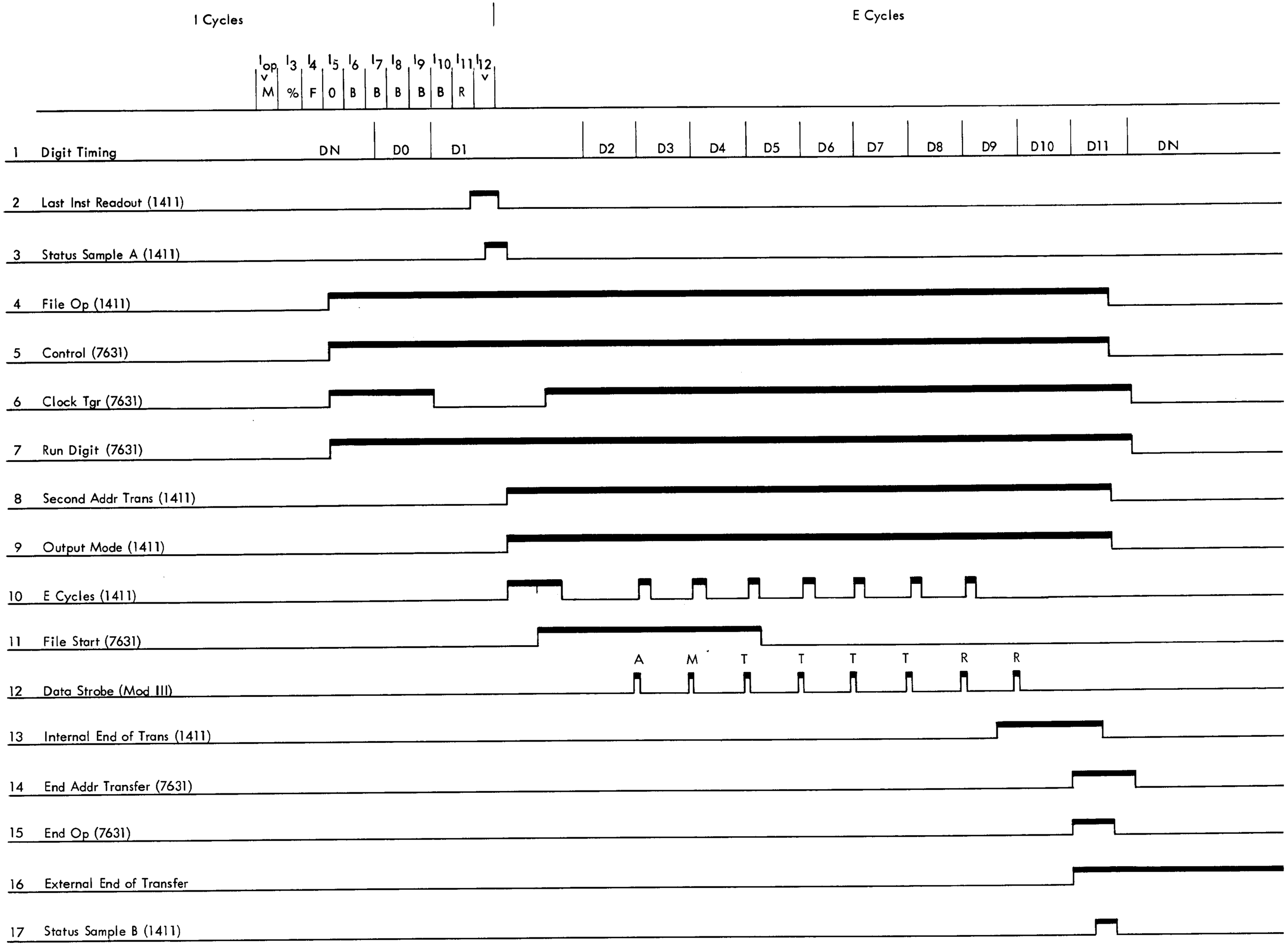


Figure 64. Control (Address Transfer) Cycle

The 7631 read or write trigger starts a prepare to read-write cycle followed by a verify address cycle. Figure 65 shows a 1410-7631 write sequence. Figure 66 shows a 1410-7631 read sequence. During read and write operations, the 7631 issues one data strobe for each character transferred to maintain the 1411-7631 data synchronization. (Figure 67 shows the 1411-7631 operation sequence in flow chart form.)

There are five conditions that can end read or write data transfers:

1. A 1410 master error
2. If the 1411 recognizes a GM-WM or end of storage with an R or W d-modifier
3. If the 1411 recognizes end of storage with a & or X op modifier
4. If the 7631 signals normal end of an operation (for example, end of track, or end of record on SRO)
5. If the 7631 detects an error

Whenever the 7631 signals end op, the 1411 external end of transfer latch is set. The 1411 internal and external end of transfer latches enable the 1411 to generate status sample B and sample the status lines to complete the read or write operation.

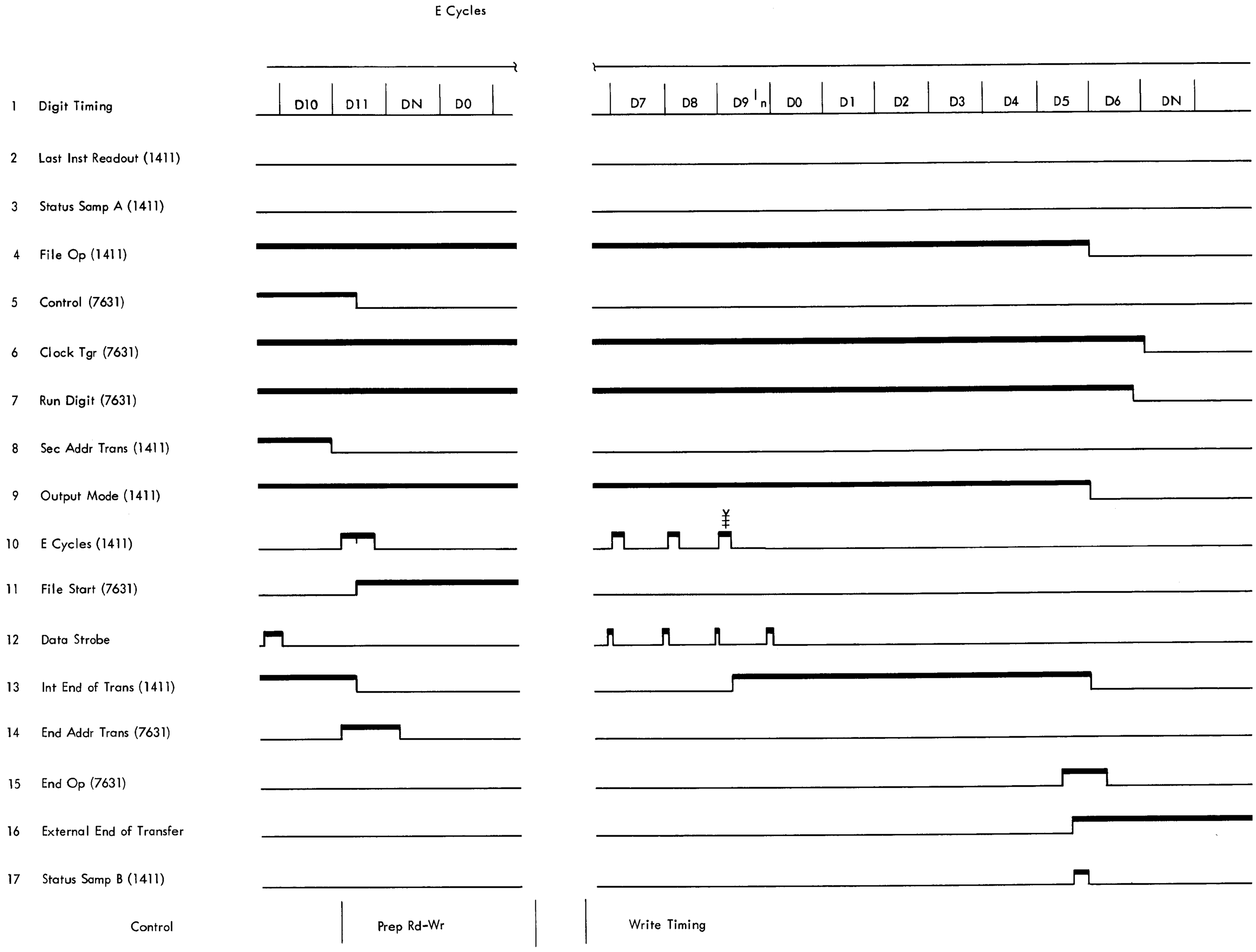


Figure 65. Write Sequence

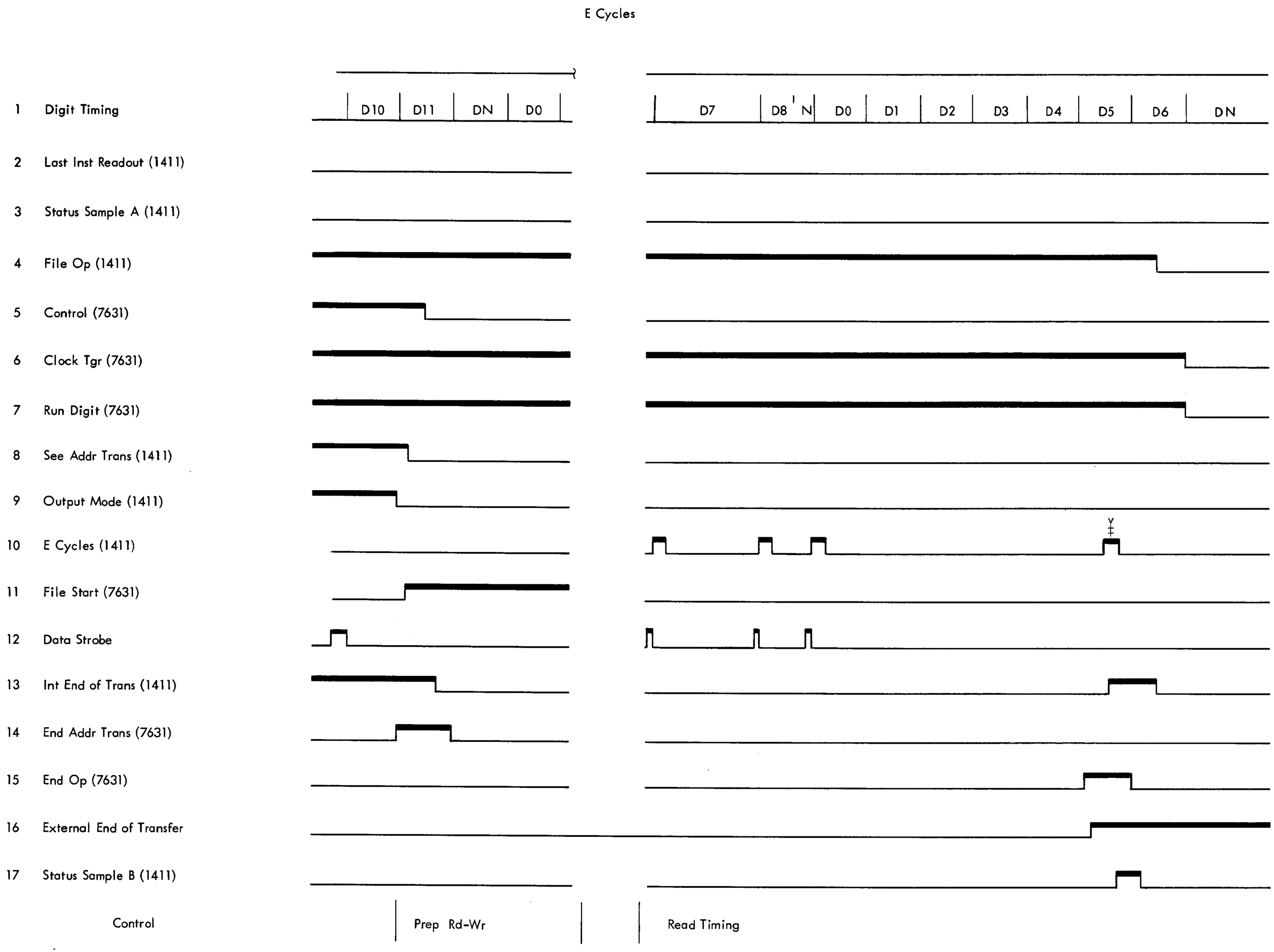
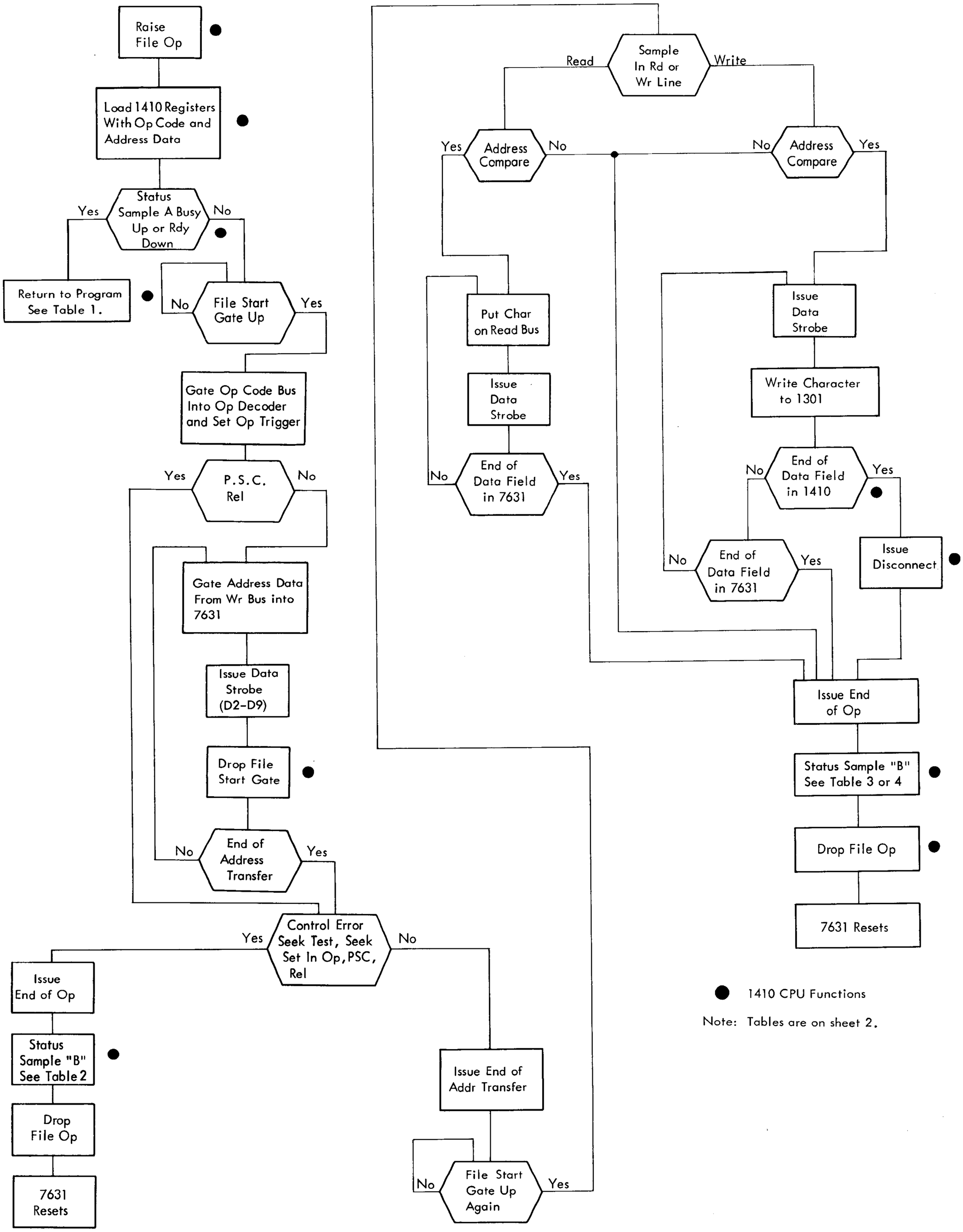


Figure 66. Read Sequence



Note: Tables are on sheet 2.

Figure 67. (Sheet 1 of 2). 1410-7631 Interface Flow Chart

TABLE 1. CONDITIONS OCCURRING BEFORE OR DURING INSTRUCTION READ OUT TO CPU

Status Indicators						
Not Ready	Busy	Data Check	Cond	No Trf	Wrong Length Record	7631 Error Condition
1	0	0	0	0	0	7631 Power Off or Off Line
0	1	0	0	0	0	7631 Mod 3 or 5 Unavailable

Note: B-address register or E-address register = B-address in instruction.

TABLE 2. CONDITIONS OCCURRING DURING FILE ADDRESS TRANSFER

Status Indicators						
Not Ready	Busy	Data Check	Cond	No Trf	Wrong Length Record	7631 Error Condition
1	0	0	0	0	0	Addressed Access Inoperative
1	0	0	0	0	0	Home Addr Sw Chk*
0	1	0	0	0	0	Addressed Access in Motion
0	0	1	0	0	0	Parity Chk
0	0	0	1	0	0	1301 Circuit Chk (FF)
0	0	0	1	0	0	Invalid Op Code
0	0	0	1	0	0	Wr Chk or Wr Fmt with rd d-mod
0	0	0	0	1	0	Release Instruction*
0	0	0	0	1	0	Block Intr Insn * (P.S.C.)

* These conditions are unique to particular instructions (for example, a home address switch check occurs only during a home address operation).

Note: B-address register or E-address register = B-address in instruction +9.

Figure 67. (Sheet 2 of 2). 1410-7631 Interface Flow Chart

TABLE 3. CONDITIONS OCCURRING AFTER FILE ADDRESS TRANSFER AND BEFORE DATA TRANSFER

Status Indicators						
Ready	Busy	Data Check	Cond	No Trf	Wrong Length Record	7631 Error Condition
0	0	0	1	1	0	No Record Found
0	0	0	1	1	0	Chk Char Reg Chk (FA)
0	0	1	0	1	0	Invalid Track No.*(Invalid Addr)
0	0	0	1	1	0	7631 Circuit Chk (FA)
0	0	0	1	1	0	1301 Circuit Chk (FF)

* If an invalid track number is indicated, the programmer will be required to reissue the proper seek instruction twice, unless cylinder zero is required, in which case one seek instruction to zero is sufficient.

Note: For a write operation, the B-address register or the E-address register = B-address in instruction +11. For a read operation, the B-address register or the E-address register = B-address in instruction +9.

TABLE 4. CONDITIONS OCCURRING DURING DATA TRANSFER

Status Indicators						
Ready	Busy	Data Check	Cond	No Trf	Wrong Length Record	7631 Error Condition
0	0	1	0	o	1 or 0	Parity Chk
0	0	1	0	0	1 or 0	Chk Char Reg Chk (FA)
0	0	1	0	0	1 or 0	Write Disk Chk* (Wr Check)
0	0	1	0	0	1 or 0	Format Char Chk* (Code Error)
0	0	0	1	0	1or 0	Wrong Length Format (Too Long)
0	0	0	0	0	1 or 0	7631 Circuit Chk (FA)
0	0	0	0	0	1	Incorrect Format or Data Area**
0	0	0	1	0	1 or 0	1301 Circuit Check (FF)

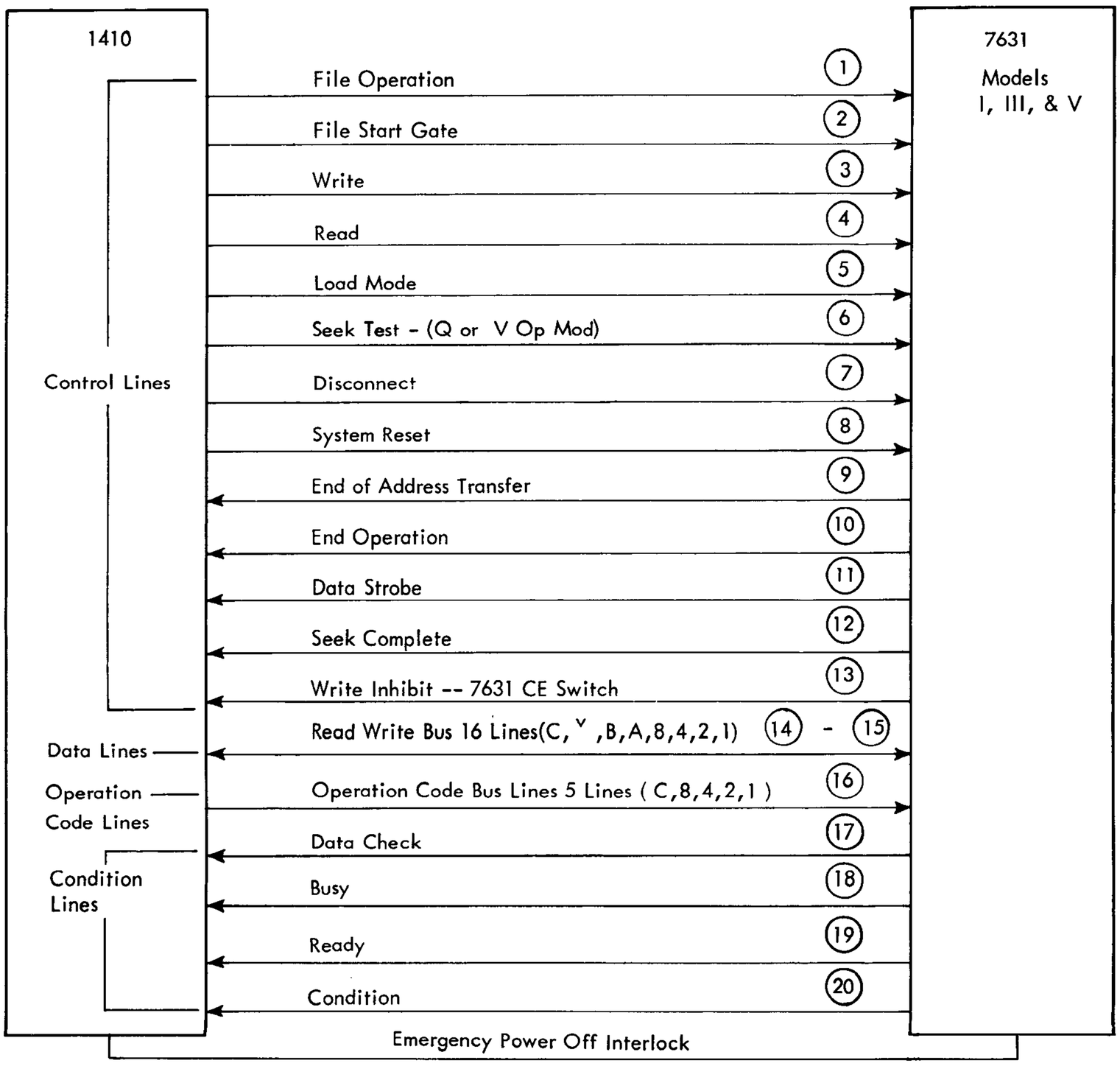
* These Conditions occur only during specific instructions.
** 1301 data is not same length as 1410 data field.

Note: B-address register or E-address register is greater than B-address in instruction + 9.

1410 I-O Interface Lines

- **1410 interface lines can be divided into four groups.**
- **Control lines—initiate and end file operations.**
- **Operation code bus lines—units number register which gates the order into 7631 operation register.**
- **Data lines—8 read data and 8 write data lines to transfer data characters.**
- **Status condition lines—indicate to system error conditions in the 7631.**

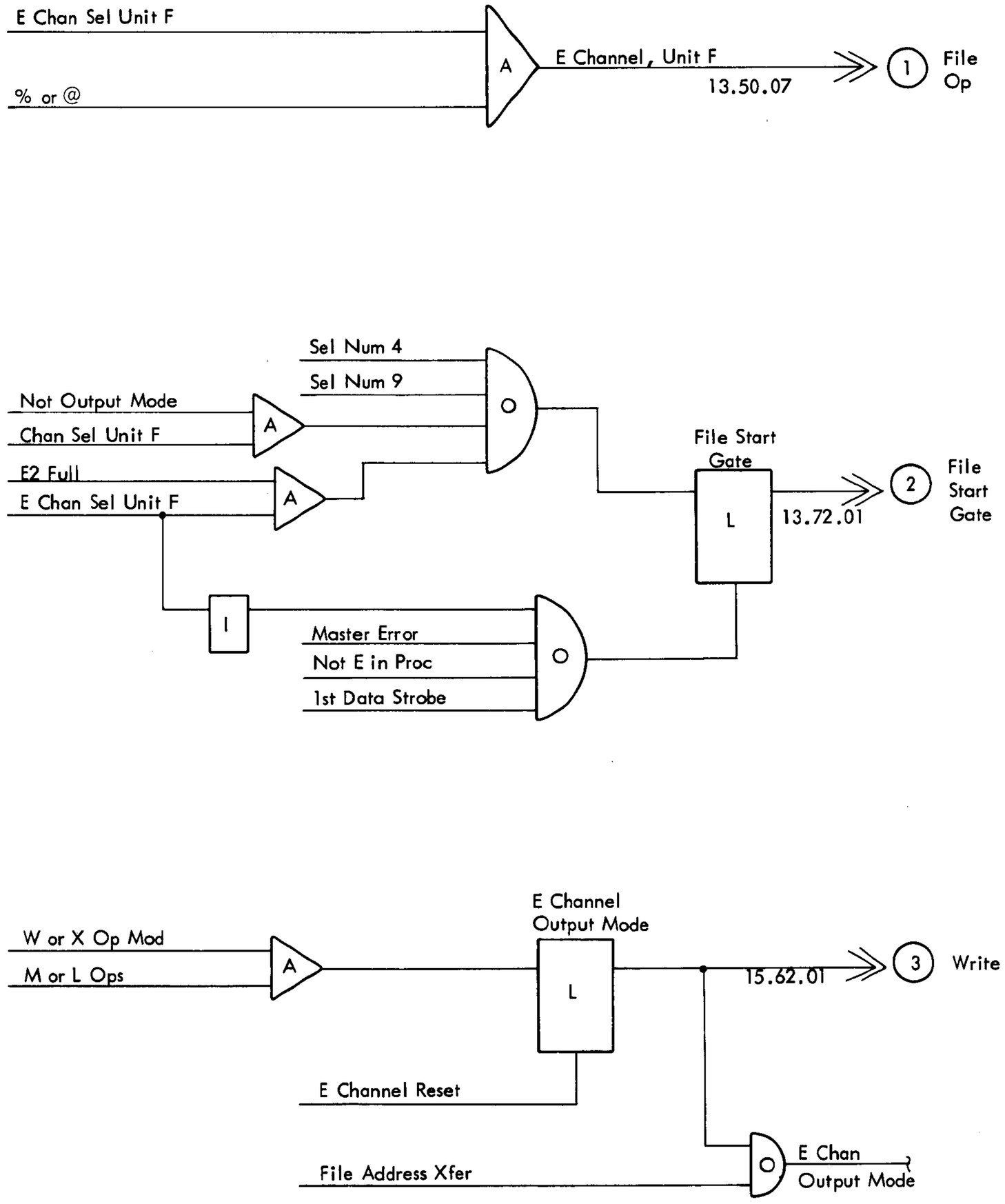
Figure 68 shows the individual lines and their names. Following Figure 68 is a list describing each line. Each line is numbered; these numbers correspond to the circled numbers shown in Figure 69. Figure 69 shows the interface logic circuits.



Note: The Circled Numbers Reference the Logic on Figure 4.12.

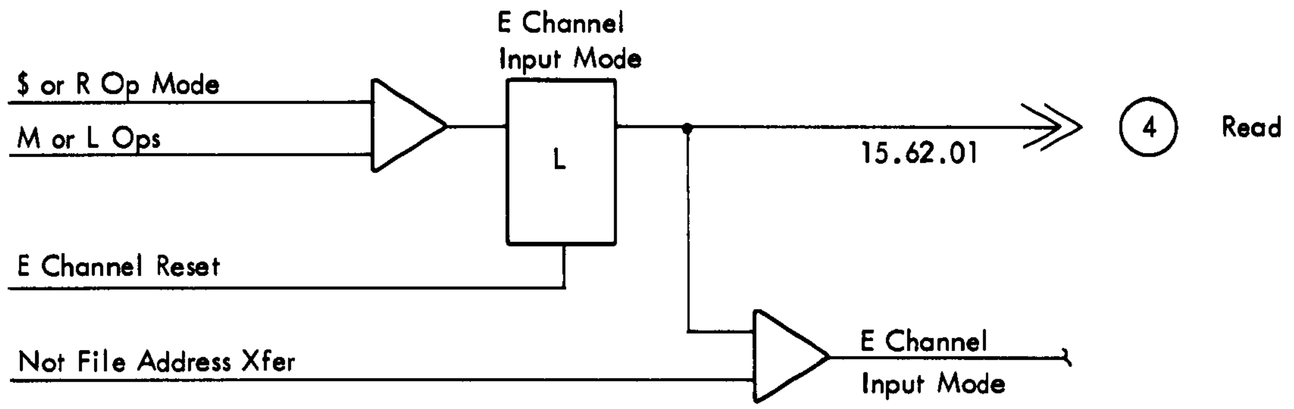
Figure 68. 1410-7631 File Control Interface Lines

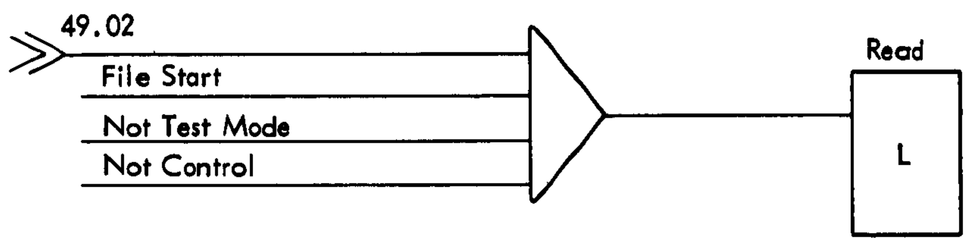
1. File Op:	Signals the 7631 that a file instruction is to be processed. File op remains active for the entire file operation.
2. File Start Gate:	Signals the 7631 that the control word is available or that a read or write operation is to start.
3. Write:	The channel output mode latch activates the write line. The write signal sets the 7631 write trigger.
4. Read:	The channel input mode latch activates the read line. The read signal sets the 7631 read trigger.
5. Load Mode:	The load mode line conditions the 7631 for 8-bit mode operation.
6. Seek Test:	Q or V op modifiers (No-op) activate this line. The seek test line causes the 7631 to end file operation at the end of the control cycle.
7. Disconnect:	This line is made active when a GM-WM or end of storage is recognized, if the 1410 is in output mode. The disconnect latch output ends data transfers.
8. System Reset:	Computer reset resets the 7631 to the reset condition.
9. End Address Transfer:	This signal is issued by the 7631 to indicate the end of a control cycle.
10. End Op:	Is activated by the 7631 when either the normal end or unusual end triggers are set.
11. Data Strobe:	The data strobe gates all data to or from the 1410. One data strobe is issued by the 7631 for each read, write, or control character transferred.
12. Seek Complete:	This signal indicates that an access has completed a seek and remains active until the next file operation.
13. Write Inhibit:	This line is used to indicate that the write inhibit switch is on and that no data was written on the file.
14. Read Bus:	Eight lines, C, WM, B, A, 8, 4, 2, and 1 transfer a character from the 7631 to the 1410.
15. Write Bus:	Eight lines, C, WM, B, A, 8, 4, 2, and 1 transfer a character from the 1410 to the 7631.
16. Op Code Bus:	Five output lines from the 1410 unit number register, C, 8, 4, 2, and 1 that indicate the order to the 7631.
17. Data Check: 18. Busy 19. Ready 20. Condition	Data check, busy, ready, and condition are lines to the 1410 status indicators from the 7631.

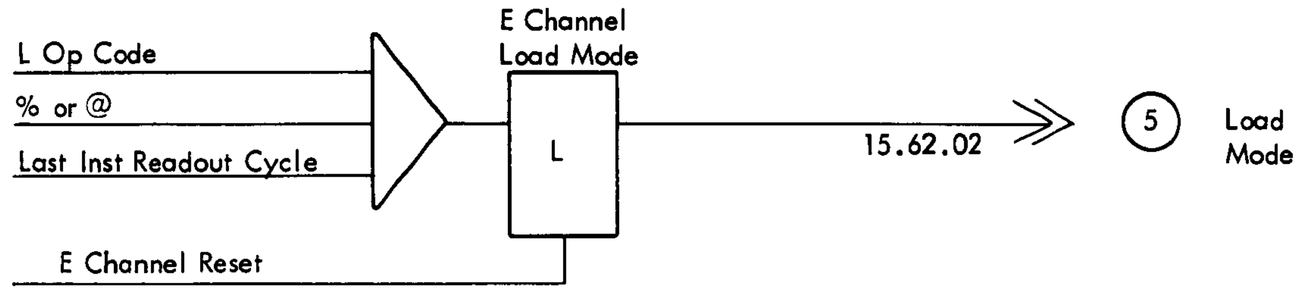


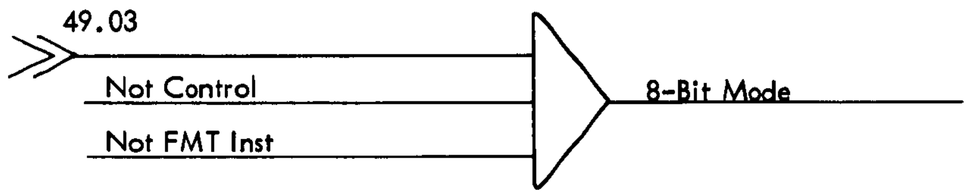
Note: Circled Numbers Refer to Figure 68

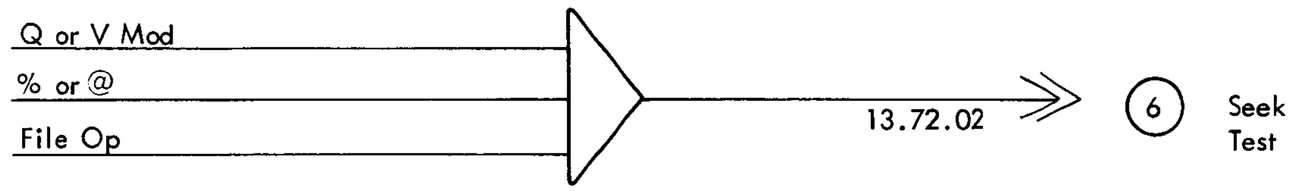
Figure 69. (Sheet 1 of 6). 1410-7631 File Control Interface Logic











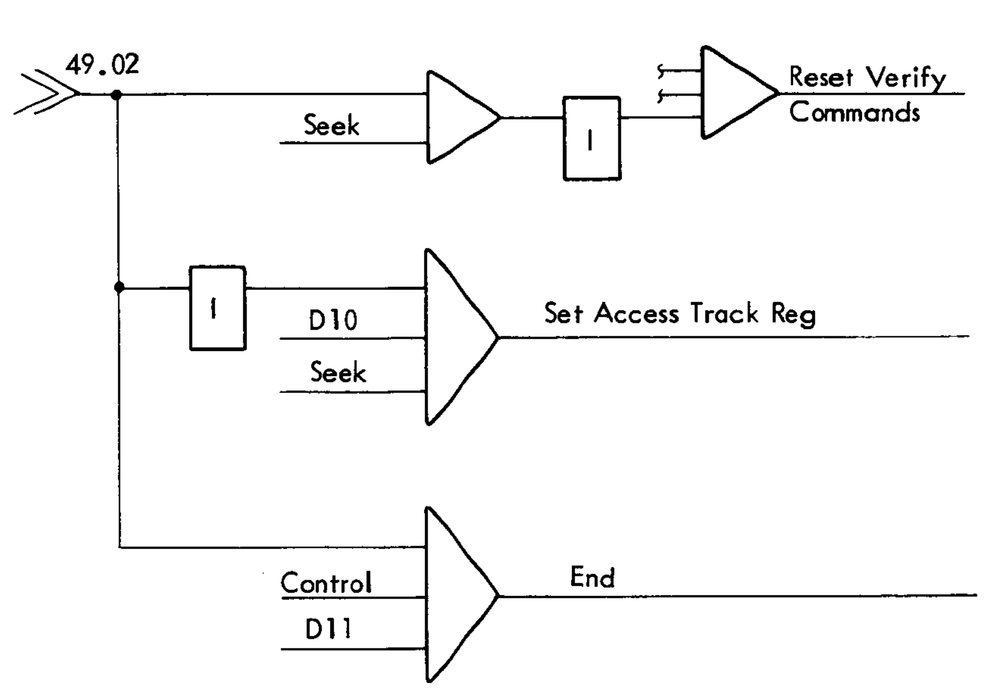
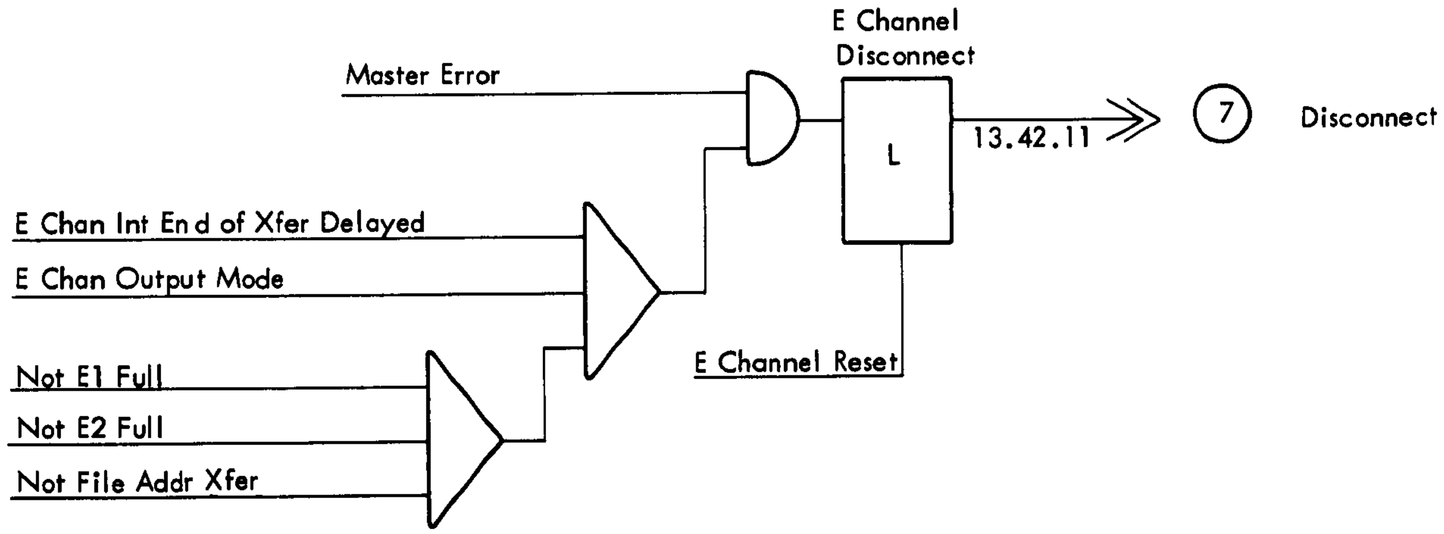
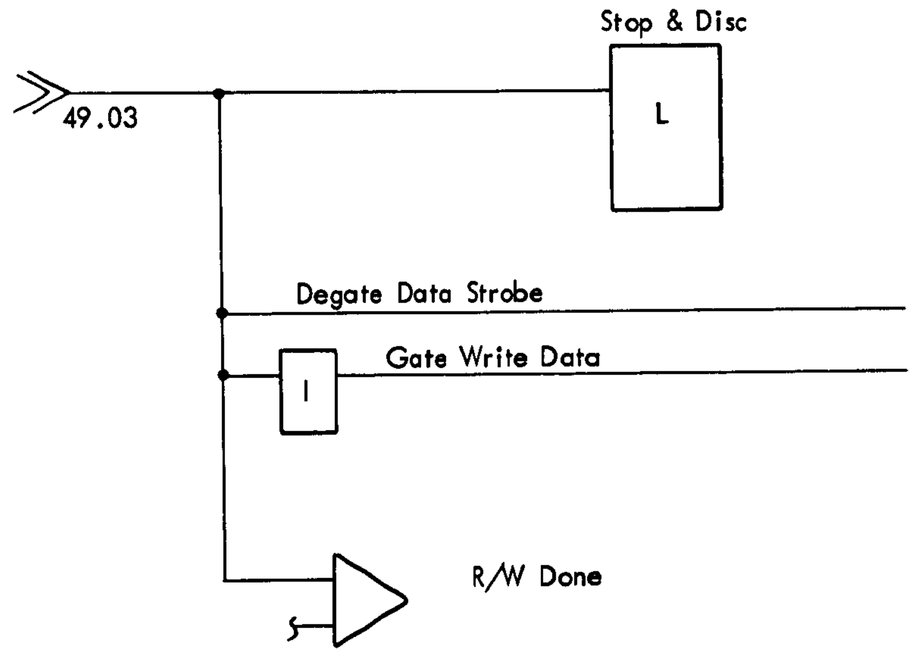
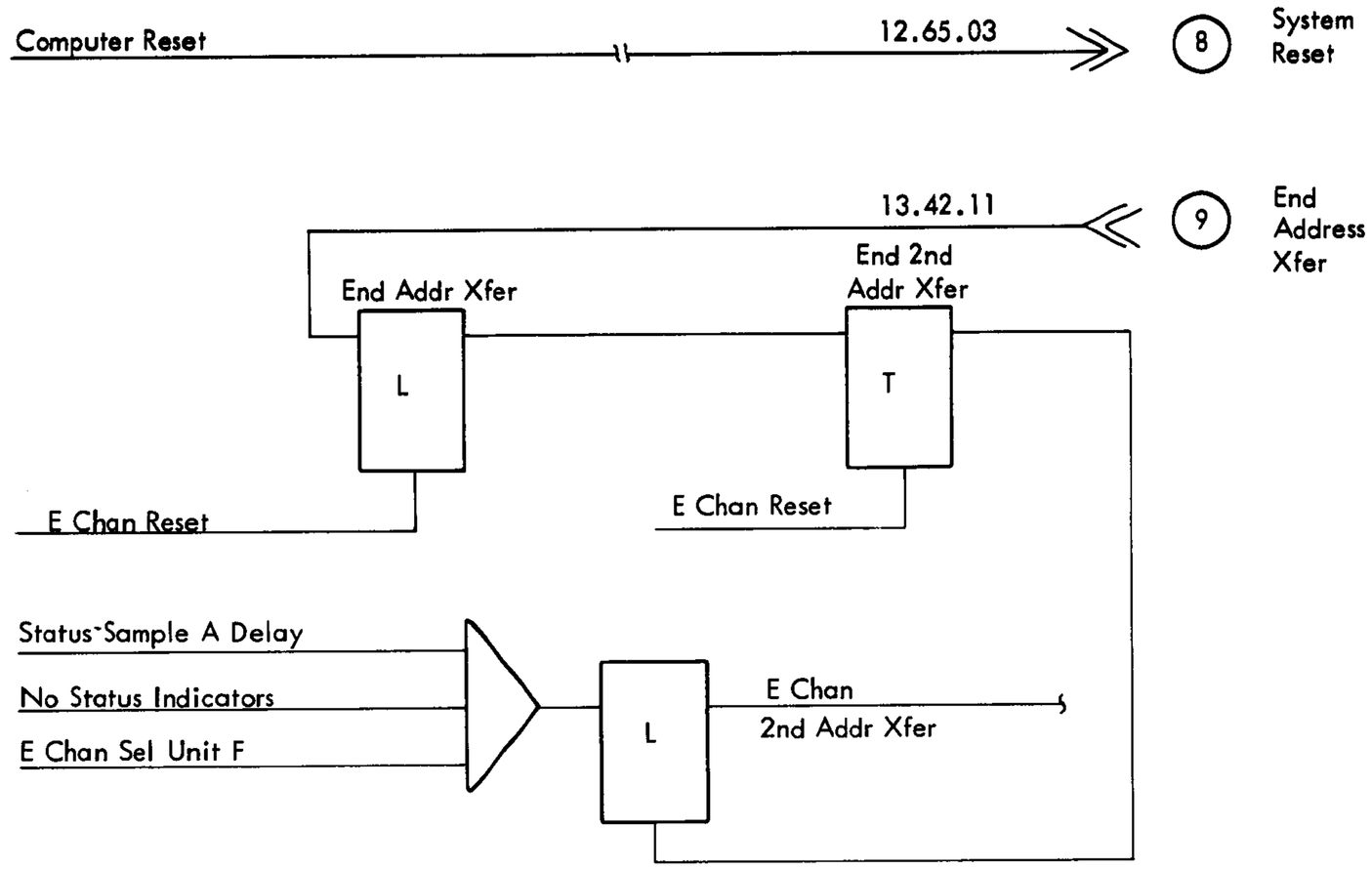


Figure 69. (Sheet 2 of 6). 1410-7631 File Control Interface Logic







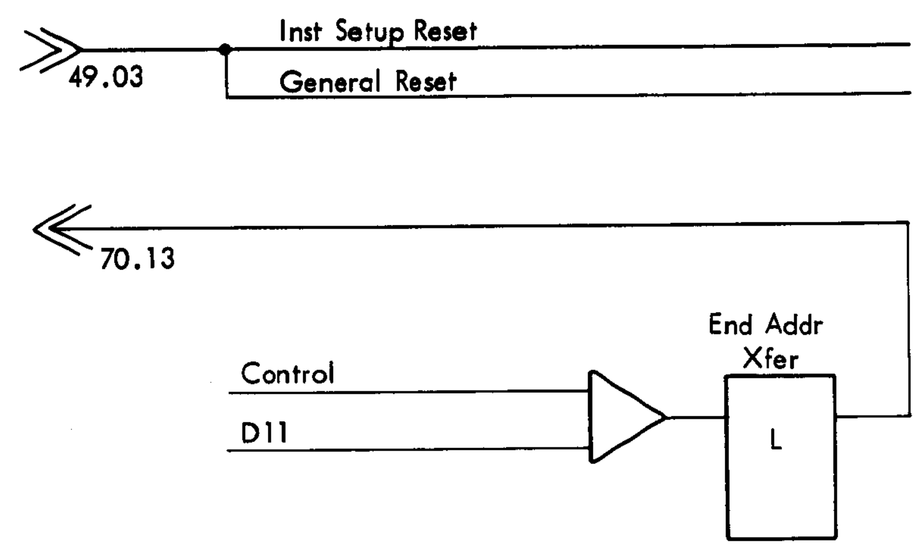


Figure 69. (Sheet 3 of 6). 1410-7631 File Control Interface Logic

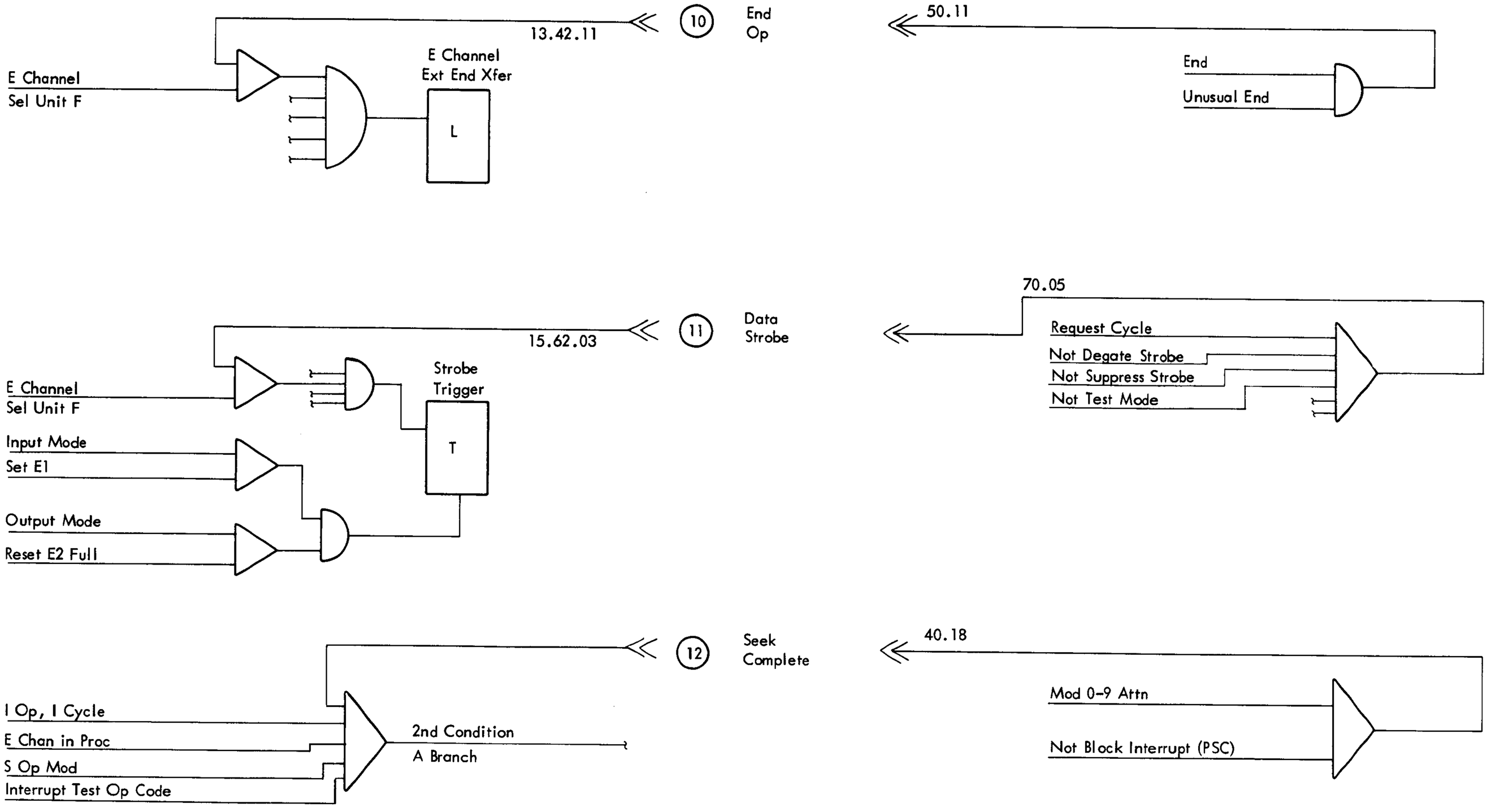


Figure 69. (Sheet 4 of 6). 1410-7631 **File** Control Interface Logic

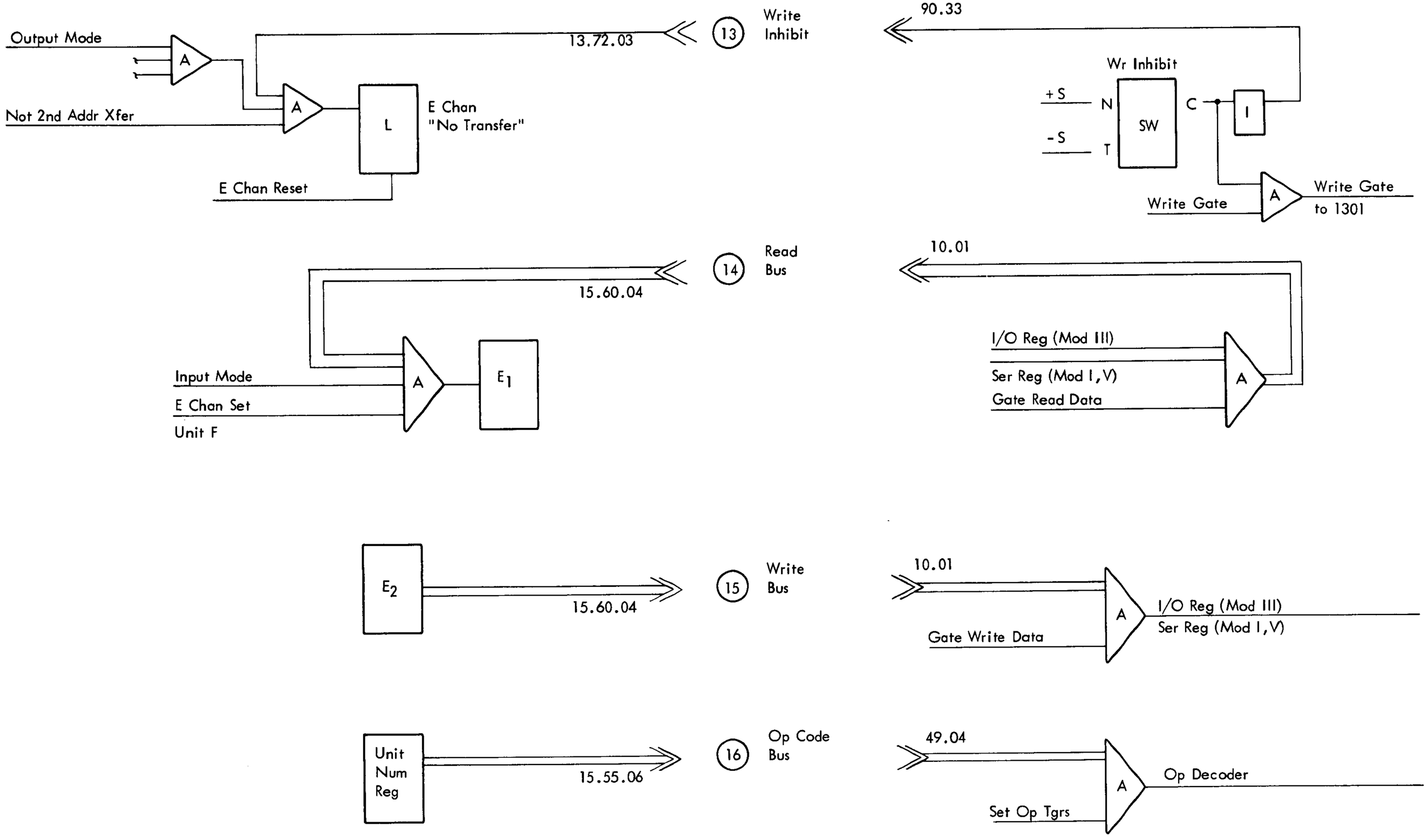


Figure 69. (Sheet 5 of 6). 1410-7631 File Control Interface Logic

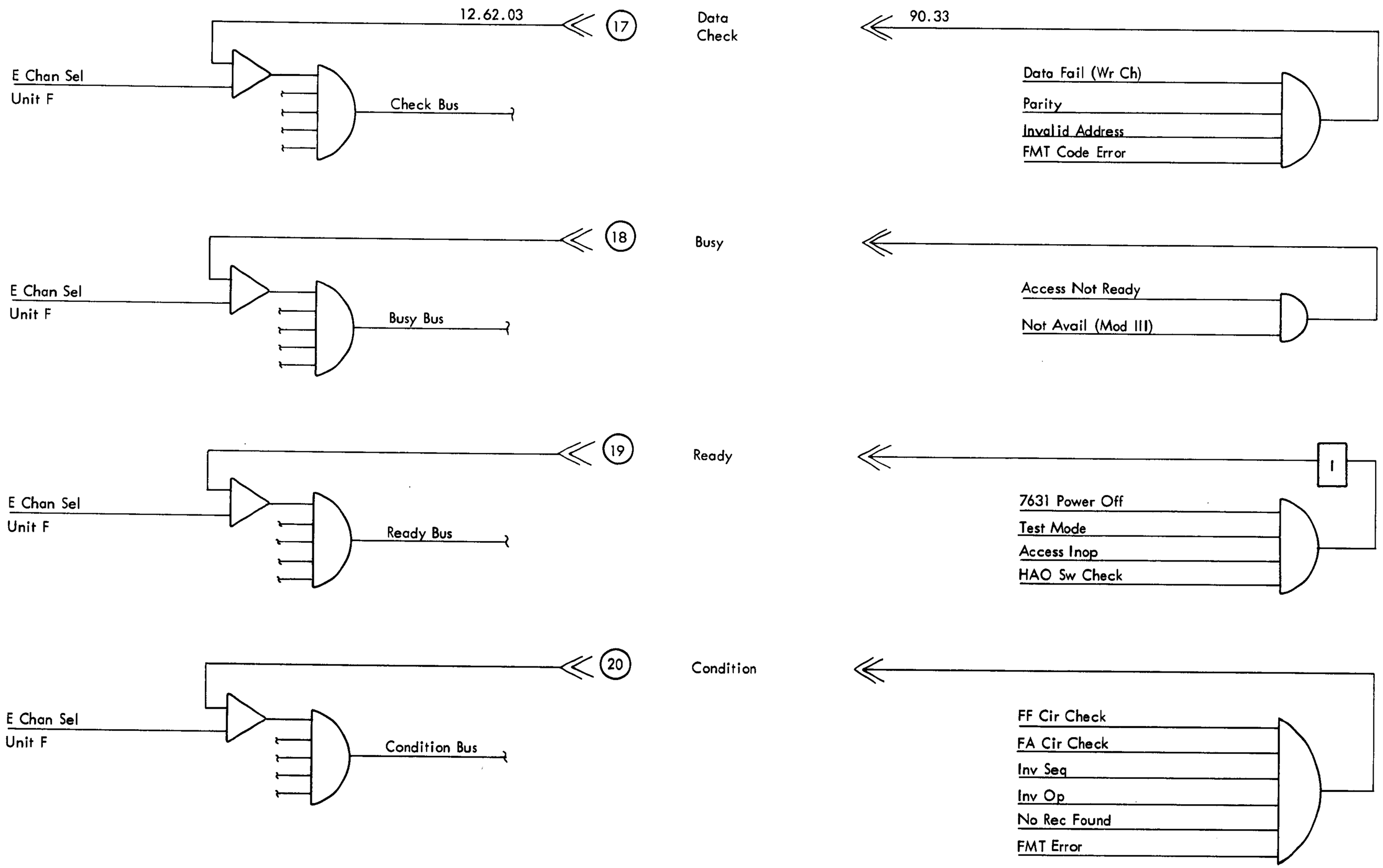


Figure 69. (Sheet 6 of 6). 1410-7631 File Control Interface Logic

Standard Interface

- **Permits a 7631 model 2, 3 or 4 to be attached to 7000 series data channel.**
- **Includes 33 lines that control all file operations and data transfers.**
- **Operates identical in operation to any channel and I-O unit using standard interface.**

The standard interface permits 7631 models 2, 3, and 4 to be attached to 7000 series data processing systems. Model 2 permits one 7000 system to attach to the 7631 (Figure 70). Model 3 permits either a 1410 or a 7010 and one of the 7000 systems to attach to the 7631 (Figure 59). Model 4 permits the attachment of two 7000 systems to the 7631 (Figure 71).

Physically, the standard interface is 33 lines connecting the data channels to 7631 file control; functionally, the standard interface is a set of rules defining the use of the 33 lines. For example, the four operations, control, read, write, and sense, performed by the 7631 are each started by the corresponding channel command line. The channel command lines are: control, read, write, and sense.

The control command starts a 7631 control cycle. This command causes the 7631 to request control data from the data channel over the write bus, and to decode the data and execute the control operation. The coded control data transferred over the write bus define operations other than those designated by the command lines. Figure 72 lists the disk orders that define operations other than those designated by the command lines.

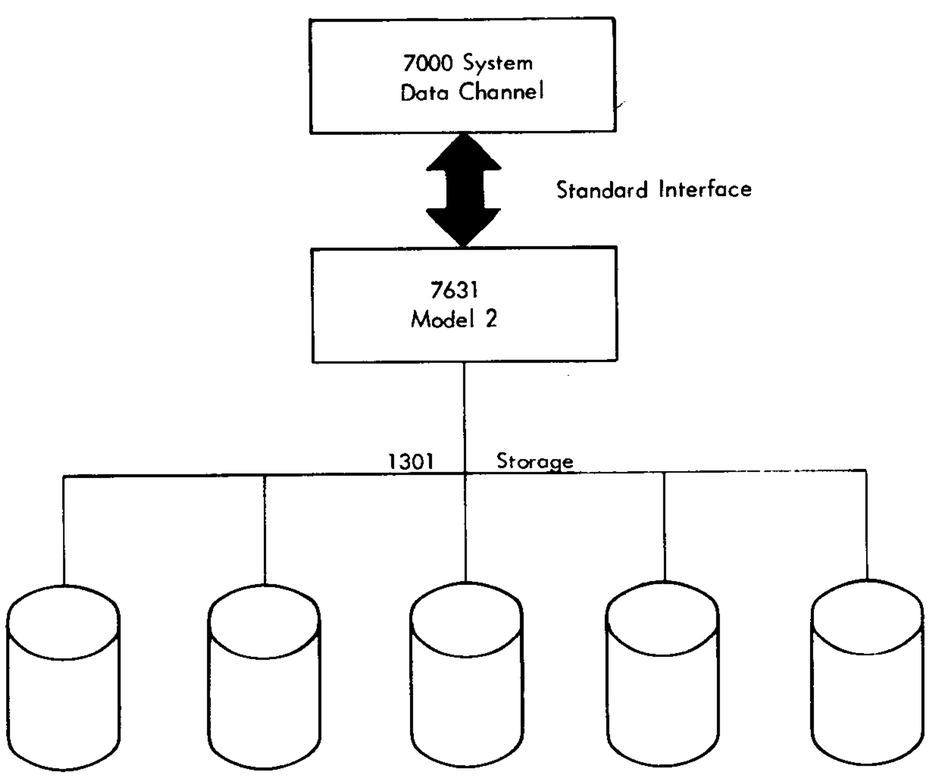


Figure 70. 7631 Model 2

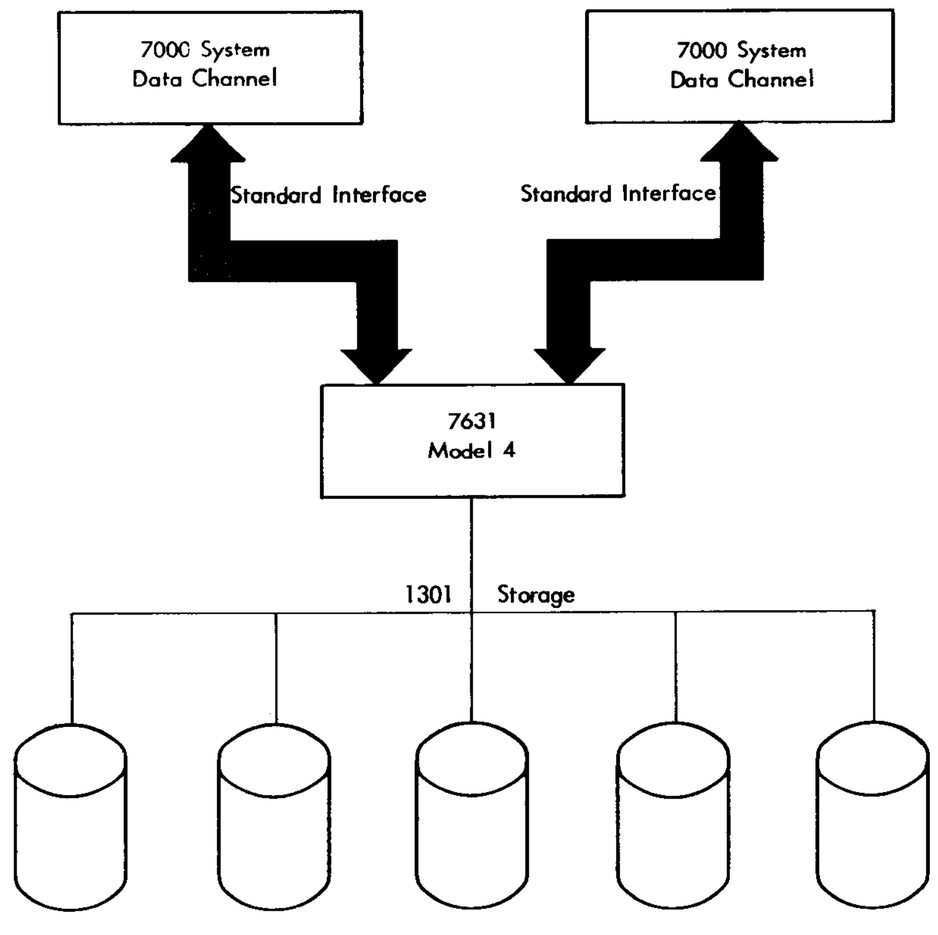


Figure 71. 7631 Model 4

7000 Operation	Mnemonic	Numeric Code	7631 Operation
No Operation	DNOP	00	No Op
Release	DREL	04	Release
Eight Bit Mode	DEBM	08	Set 8 Bit
Six Bit Mode	DSBM	09	Set 6 Bit
Seek	DSEK	80	Seek
Prepare to Verify Single Record	DVSR	82	Single Record Op (SRO)
Prepare to Write Format	DWRF	83	Write Format (Wr Fmt)
Prepare to Verify Track with No Addresses	DVTN	84	Track Without Address (TWA)
Prepare to Verify Cylinder Operation	DVCY	85	Cylinder Op (CYO)
Prepare to Write Check	DWRC	86	Write Check (Wr Ck)
Set Access Inoperative	DSAI	87	Set Inop
Prepare to Verify Track with Addresses	DVTA	88	Track Op (TRO)
Prepare to Verify Home Address	DVHA	89	Home Address Op (HAO)

Figure 72. 7000 Systems Disk Orders

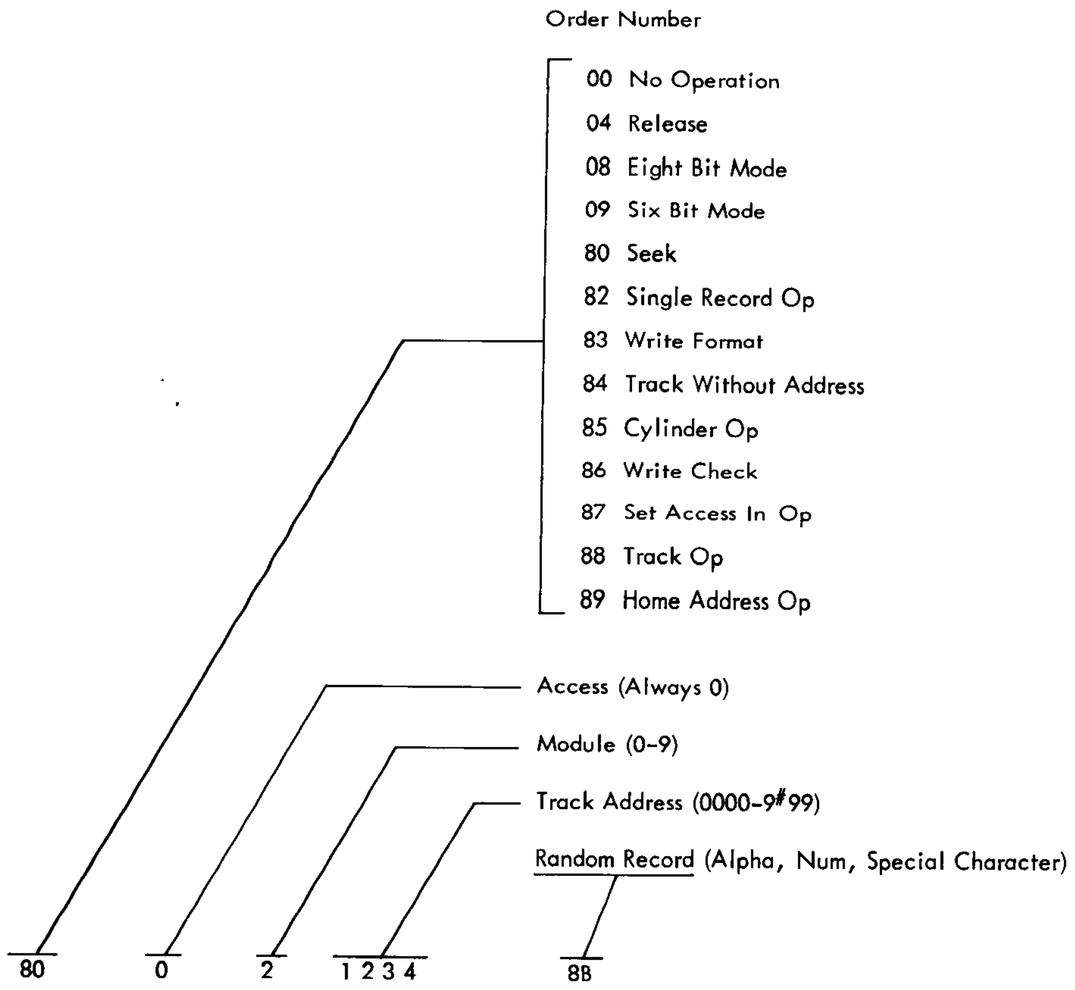


Figure 73. 7000 Systems Control Word Layout

Operation	Op Code	Address Data							
8-Bit	08	X	X	X	X	X	X	X	X
6-Bit	09	X	X	X	X	X	X	X	X
Seek	80	A	M	H	H	H	H	U	U
SRO	82	A	M	R	R	R	R	R	R
TWA	84	A	M	H	H	H	H	I	I
Wr Ch	86	Note 1							
HAO	89	A	M	H	H	H	H	U	U
TRO	88	A	M	H	H	H	H	I	I
Wr Fmt	83	A	M	H	H	H	H	U	U
Set In Op	87	A	M	U	U	U	U	U	U
Rel	04	X	X	X	X	X	X	X	X
Cyl	85	A	M	H	H	H	H	I	I
No Op	00	X	X	X	X	X	X	X	X

Code -
A - Access
M - Module
H - Track Address (HA1)
R - Record Address (SRO Only)
I - Random Record (HA2)
U - Transferred to 7631, but not used.
X - Not required and not transferred.

Note 1 - The control word for a write check should be the same as the order being checked.

Figure 74. 7000 Systems Control Words

The disk orders transmitted over the write bus follow the format shown in Figure 73. A complete order is either two characters or ten characters of control data. If the order is six-bit mode (08), eight-bit mode (09), release (04), or no operation (00), it is a two-character control word; the remaining control words contain ten characters. Figure 74 shows an example control-word layout for each order. The first two characters of each control word are numbers used to specify the order. Ten character orders include eight address data characters. The address data specifies the 1301 access, module, and track or record address required for the operation.

The write command causes the 7631 to execute a write operation. The write operation causes the 7631 to request write data over the write bus from the data channel. A previously stored control word determines the mode of writing and where to write the data.

The sense command causes the 7631 to transfer coded sense information to the data channel on the read bus. The sense data transferred describes the status of the 7631 file control unit and the 1301 disk storage. Ten bytes of sense data are transferred to complete the sense operation. Status data bit assignments are shown in Figure 75.

The read command causes the 7631 to execute a read operation. The read operation causes the 7631 to transfer read data to the data channel on the read bus. A previously stored control word determines the mode of reading and the areas to be read.

Initiation of an Operation

To start an operation in the 7631, the channel activates the command line corresponding to the type of operation required. A command response line is used by the 7631 to signal recognition of a command on any of the four command lines.

Information Transmission

During any operation, the transfer of information (data, orders, or sense information) between a data channel and a 7631 is synchronized by service request signals generated by the 7631 and service response signals produced by the data channel. An operation specified by any of the four commands may be terminated by the data channel or the 7631.

Definition of Standard Interface Signal Lines

A description of the standard interface data and control lines follows (Figure 76, sheets 1 and 2).

Data Channel Lines to 7631

Write Bus Lines

The write bus is used for sending both write data and control information to the 7631. The write bus has nine

Status Char	Bit No.	BCD Bit	Assignment	Comment
0	3	A	Reserved	Summary Byte
	5	4	Program Check	
	6	2	Data Check	
	7	1	Exceptional Condition	
1	3	A	Invalid Sequence	Program Check
	5	4	Invalid Code	
	6	2	Format Check	
	7	1	No Record Found	
2	3	A	Invalid Address	
	5	4	Response Check	Data Check
	6	2	Data Compare Check	
	7	1	Parity or Check Char Code Check	
3	3	A	Access Inoperative	Exceptional Condition
	5	4	Access Not Ready	
	6	2	Disk Storage Circuit Check	
	7	1	File Control Circuit Check	
4	3	A	Reserved	Data Mode
	5	4	Six-Bit Mode	
	6	2	Reserved	
	7	1	Reserved	
5	3	A	Module 0	Attention
	5	4	Module 1 (Disk Only)	
	6	2	Module 2	
	7	1	Module 3 (Disk Only)	
6	3	A	Module 4	Attention
	5	4	Module 5 (Disk Only)	
	6	2	Module 6	
	7	1	Module 7 (Disk Only)	
7	3	A	Module 8	Attention
	5	4	Module 9 (Disk Only)	
	6	2	Reserved	
	7	1	Reserved	
8,9			Reserved	

Figure 75. Status Data Bit Assignment

lines: eight data lines (0, 1, 2, 3, 4, 5, 6, 7) plus one line (parity) for odd parity. Write data or control information is gated from the data channel to the write bus lines during a write or control operation.

Operational Out Line

This line serves essentially as an interlock line. The 7631 recognizes signals from the data channel only while the operational out line is conditioned. This line is also used in resetting the 7631.

Command Lines

An operation is initiated in the 7631 by one of the four command lines: read, sense, write, and control. An activated command line sets the corresponding operation trigger in the 7631.

An operation associated with any of the four command signals must be properly terminated before a new command is issued. The 7631 acknowledges receipt of a command signal by returning a command response to the channel.

Service Response Line

During a write or control operation, a service response signal is generated by the channel each time a character is placed on the write bus. The service response line is controlled by the channel. During a read or sense operation, the service response line indicates that the channel has accepted the character on the read bus.

Attention Response Line

This line is used to acknowledge receipt of an attention signal from the 7631.

Stop Line

A stop signal is sent to the 7631 by the data channel to indicate the end of an operation.

End Response Line

An end response is sent to acknowledge receipt of an end or unusual end signal from the 7631. The end response line resets the control, read, write, or sense command triggers.

7631 Signal Lines to Data Channel

Read Bus Lines

Both read data and sense (status) information are sent to a data channel over the read bus. The read bus has nine lines: eight data lines (0, 1, 2, 3, 4, 5, 6, 7) plus one (parity) line for odd parity. Read data or status information is transferred a character at a time over the read bus to the data channel.

Command Response Line

This line indicates that the 7631 has received one of the four command signals, and is able to start the specified operation. The command response line remains conditioned throughout an operation, and is deactivated when an end response is received by the 7631.

Operational In Line

This line is essentially an interlock line. During an operation, signals from the 7631 are only recognized by the data channel when the operational in line is active. When this line is inactive, all input signals from the 7631 are blocked in the data channel.

Attention Line

The attention signal indicates to the data channel that some 1301 has completed a seek operation. The attention signal from the 7631 causes an attention response signal to be returned to the 7631.

Service Request Line

This line is used to synchronize the transfer of characters between a data channel and the 7631. During a

read or sense operation, a service request signal is generated whenever a character is placed on the read bus by the 7631. The service request signal is removed by the 7631 after a service response is received from the channel.

During a write or control operation, a service request signal is generated by the 7631. The service request causes the channel to place a character on the write bus.

End Line

This line is used to signal the channel that the 7631 has recognized the normal end of an operation. An end signal causes the channel to issue end response.

Unusual End

An unusual end signal is issued by the 7631 to terminate an operation in which some error condition has occurred. Depending on the type of operation and type of error detected, an unusual end signal may be generated either at the time the error is sensed or at the completion of the operation. An end response signal is sent to the 7631 to acknowledge receipt of the unusual end.

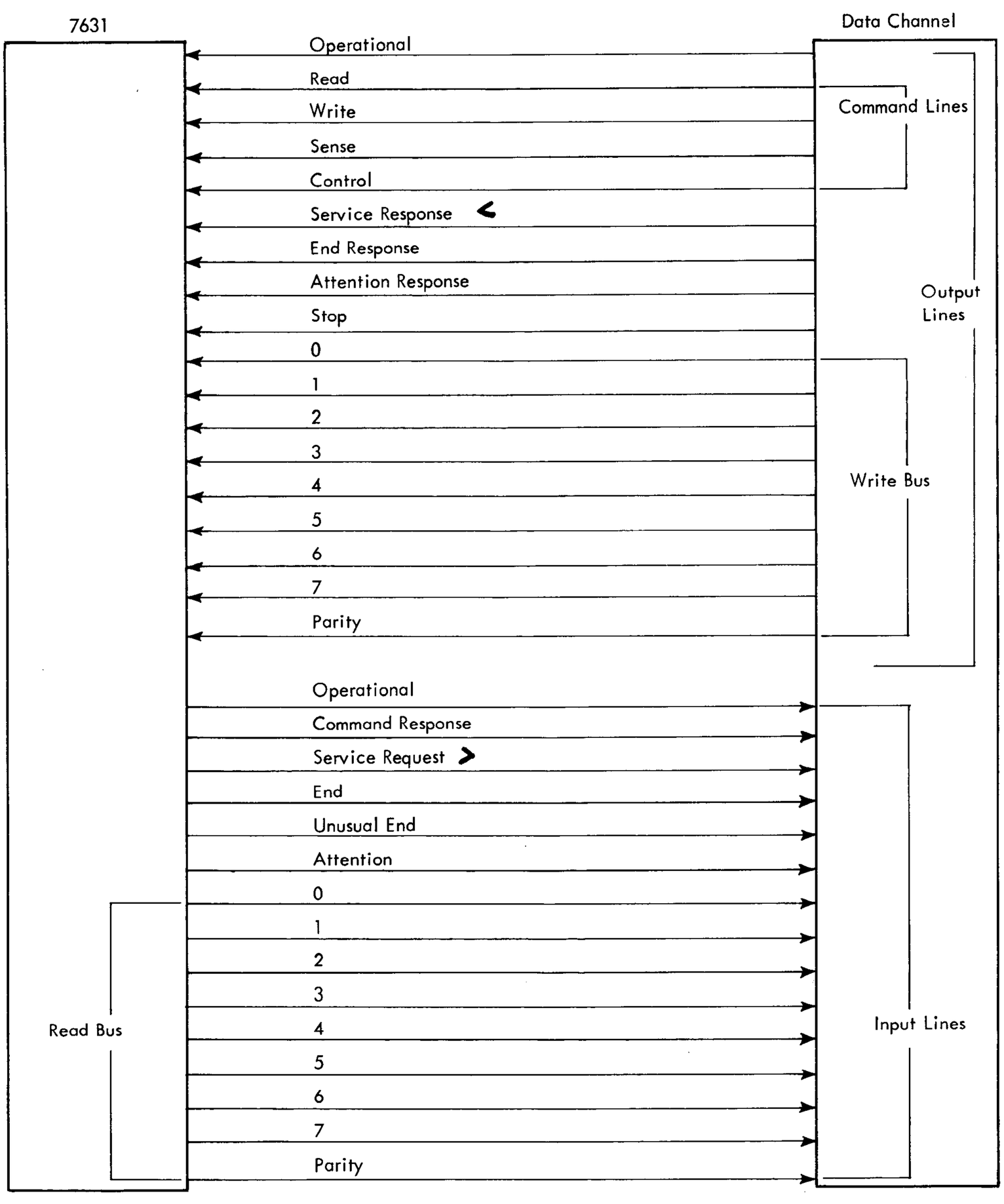
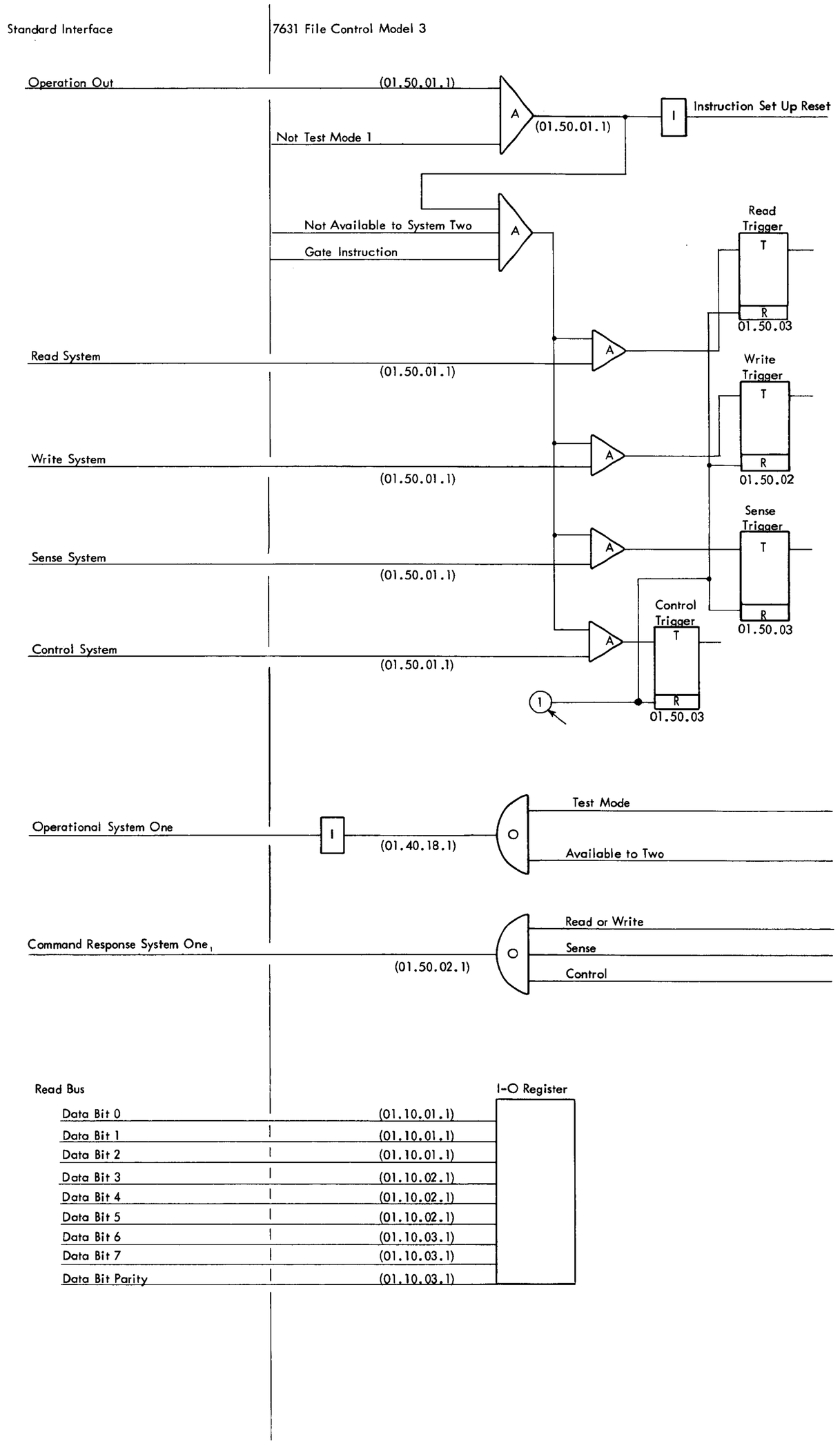
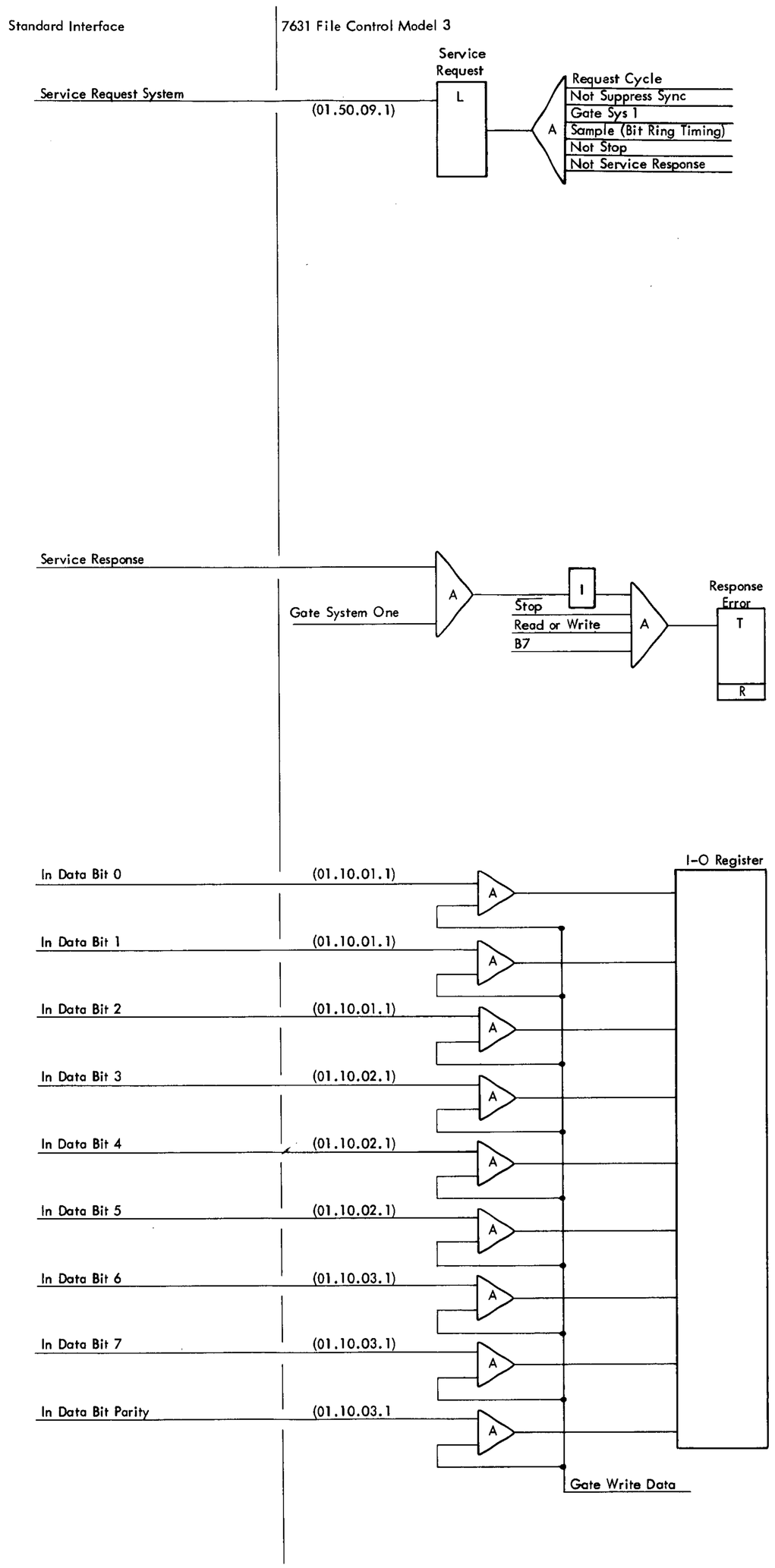


Figure 76. (Sheet 1 of 2). Standard Interface





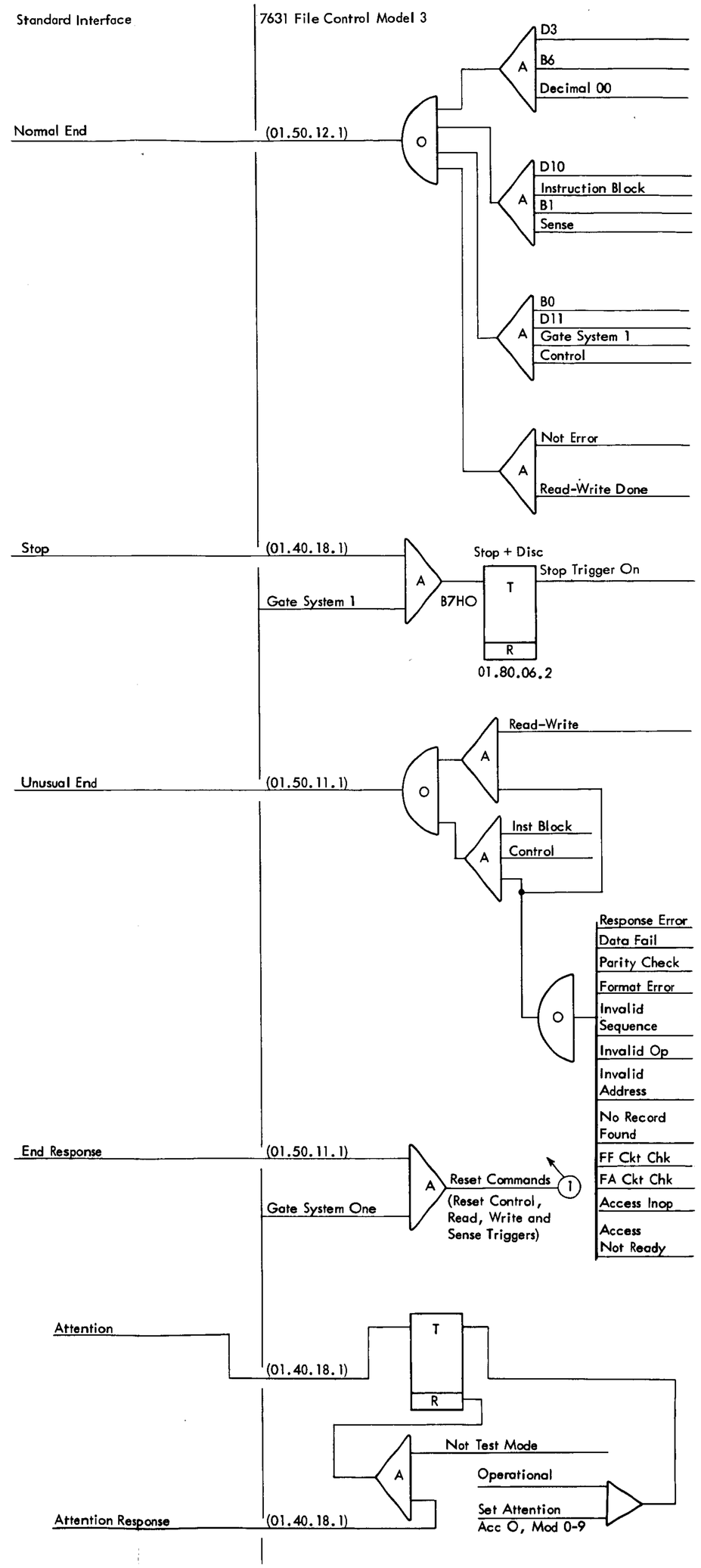


Figure 76. (Sheet 2 of 2). Standard Interface

Operations Timings

Availability

- **This circuitry used on models 3, 4 or 5.**
- **Allows two different systems to operate 7631.**
- **Only one system may operate file control at one time.**
- **Release order or machine reset will allow both systems to be available again.**

Because 7631 models 3, 4, and 5 are used for a shared system operation, availability circuits are provided to prevent one system from interfering with file operation initiated by the sharing system. When the available to one and two triggers are off, either system can start a file operation (Figure 77). Both available triggers are reset with a general reset or a programmed release.

Shared 7631's indicate busy to the 1410 (for models 3 and 5), or not operational to the 7000 system (for models 3 and 4), if the 7631 is available to the sharing system and is not released.

The instruction block trigger prevents the 7631 from accepting a second command or instruction from the controlling system before completing the first instruction. When reset, the instruction block trigger enables the 7631 to accept a new instruction, reset commands, generated when each instruction is completed, that resets the instruction block trigger. Conversely, when set, the instruction block trigger prevents the 7631 from accepting a new command; the first B6, generated at the start of a new instruction, is used to set the instruction block trigger.

In a typical file operation, the using system issues a release instruction after each program sequence to reset the available to one and two triggers. Assume system one issued a control command: the control command sets the available to one trigger, and the available to one trigger blocks file op from system two and conditions the four command gates shown in the lower right corner of Figure 77. Control and B6 set the instruction block trigger; instruction block blocks any instructions issued by system one prior to completing the control command. The available to one trigger output (not available to two) blocks system two's file operation until system one issues the release instruction at the end of a program sequence.

1410 Control Cycle

- **Initiated by file op from 1410.**
- **Can be divided into three areas of operation.**
- **Timing operation—necessary controls for operation of the bit and digit ring.**
- **Request and store circuit operation—develop data strobes to gate control word from 1410 into 7631 address register.**
- **Miscellaneous circuit operation—develop controls to operate the 1301 and tests to determine status of 1301.**

A control cycle executed in response to file op causes the 7631 to decode the character on the op code bus and set the corresponding 7631 control operation trigger. From D2 through D9, the 7631 request circuits gate the control word characters from the write bus into the I-O register. The 7631 issues one data strobe

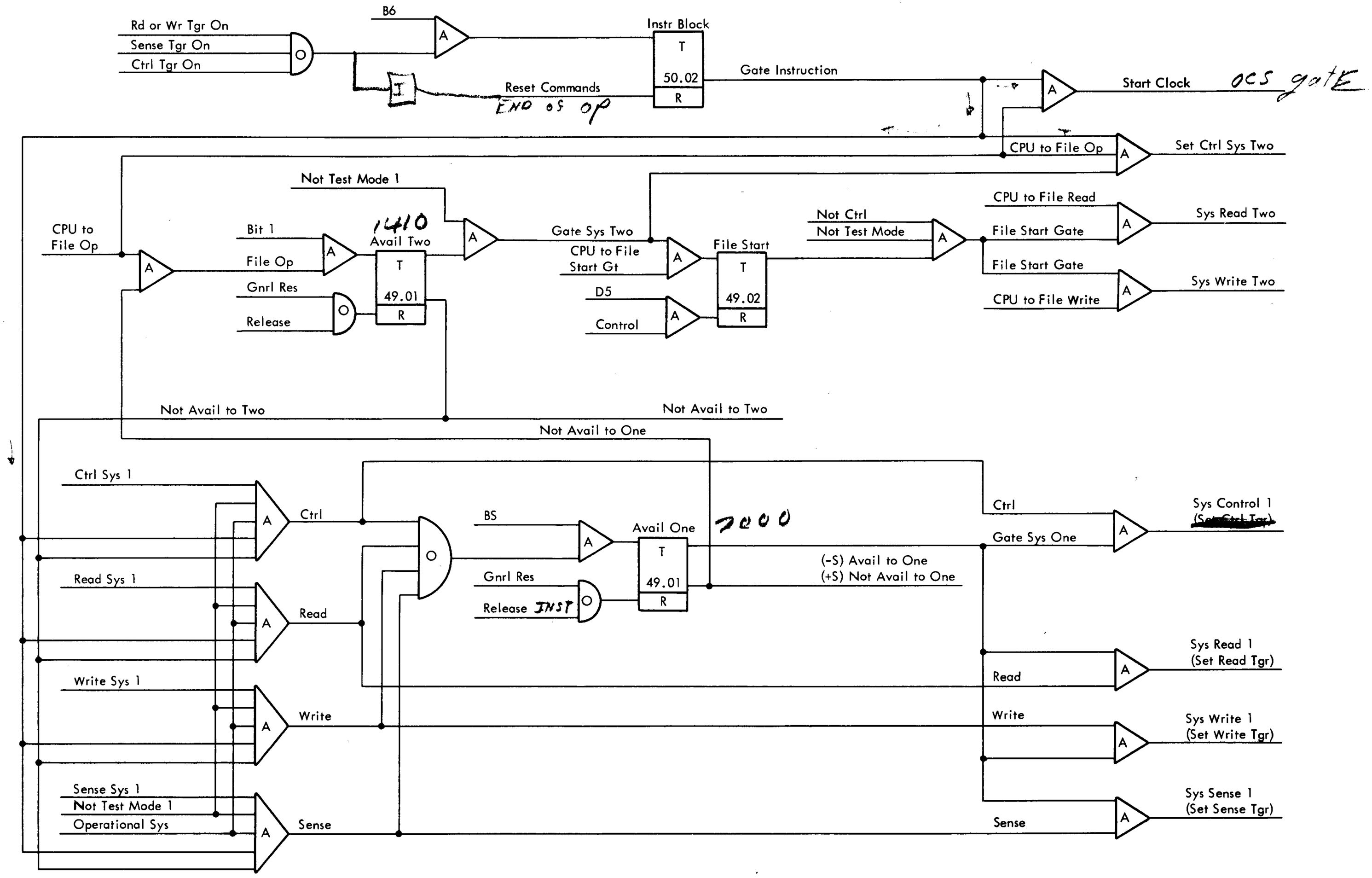


Figure 77. Availability—Model 3

for each character transferred from the write bus into the 7631 I-O register; the I-O register contents are transferred to the serial register. The contents of the serial register are sequentially stored in the access, module, track, and random record registers with pulses D3 through D10, and each character stored in the serial register is parity checked. At D11, the last digit cycle, the 7631 determines if end op or end of address transfer is required.

Briefly, the control cycle operation can be divided into three parts:

1. Timing operations
2. Request and store operations
3. Miscellaneous operations

Timing Operations

Control cycle timing starts with DN and ends at D11. Because the 1410 issues file op to start the 7631 prior to filling registers E1 and E2, the 7631 pauses at BS of D1 until E2 is full; after E2 is full, the 1410 issues the file start gate to restart the 7631 timing circuits (Figure 64, line 11). Because the 1410 is faster than the 7631, the 7631 operates uninterruptedly for the remainder of the control cycle.

When the control trigger is set, the oscillator is gated and the run digit trigger is set (Figure 78, sheet 1). As a result of file op, start clock sets the clock trigger which gates the bit ring drive. Start clock is dropped when B6 sets the instruction block trigger, while the clock trigger is held on until D1. Timing remains stopped at BS of D1 until the 1410 fills E2 and issues the file start gate. Receipt of the file start gate sets the clock trigger, which remains set until the control cycle is completed.

Request and Store Operations

When BS of D2 sets the lead control trigger, data request circuit operations start (Figure 79, line 4). Request cycle fetch is generated when lead control, not read, and not first index AND. Request cycle fetch controls (these references refer to the circled numbers on Figure 78, sheet 1):

1. the input register reset (circle 1)
2. the input register loading (circle 2)
3. the data strobe (circle 4)

B6 of D2 sets the lead holdover trigger. Lead holdover, not read, and not first index control:

1. The serial register reset (circle 7)
2. The input register transfer to the serial register (circle 6)

Figure 79, lines 4 through 13, shows the request and transfer circuit timing details. Figure 79, line 24, shows that load info on control is generated every digit cycle. Load info on control (shown in Figure 78, sheet 2) gates the output of the serial register with pulses D3 through D10 to the access, module, track, and random record registers. Each character stored in the serial register is parity-checked (lower left corner, Figure 78, sheet 2).

Miscellaneous Operations

The following references refer to the circled numbers in Figure 78, sheet 1. Their functions are:

1. B1 of D2 resets the control op triggers if a new prepare to verify order is processed (but not write check), or if the instruction is seek test (circle 8). If the instruction is seek test or write check, the control op trigger reset is inhibited. The seek and set in-op triggers are reset at the end of every control cycle. The bit mode trigger is set for six-bit mode with a release instruction. When eight-bit mode operation is required, the 1410 load line resets the bit mode trigger at the beginning of the control cycle.

2. The address register is reset at B5 of D2 (circle 9). Collectively, the access, module, track, and random record registers are called the address register.

3. Access ready or operative cause file frame circuit checks at D3, because the access and module are not selected until D5 (circles 10 and 11).

4. If no valid op code is decoded, the invalid op trigger is set at D3 (circle 12).

5. The select ACU trigger is set at D5 of each control cycle (circle 13). Select ACU selects the specified access and module; the selected access and module indicate ready and operative, if operating correctly.

6. Set access inoperative is issued to the file frame at B6 of D5, if the instruction is set access inoperative (Figure 79, line 35).

7. The monitor ready operative trigger is set at D9; it tests for the presence of not ready or inoperative from the selected access unit (circles 14 and 15). The monitor ready operative trigger is not set when the instruction is prevent seek complete, release, set in-op, or if an error is detected.

8. If the instruction is seek and there are no errors, set ACU track register is issued to the 1301; set ACU track register transfers the 7631 track register cylinder and head bits to the 1301 at D10 (circle 17).

9. If the instruction is not SRO, set ACU head register is issued to the file frame at D10; set ACU head register transfers the head select bits from the 7631 to the 1301 head register, and resets the monitor ready operative trigger (circle 16).

10. If any error occurred during the control cycle, or if the instruction is in-op, release, seek test, set block

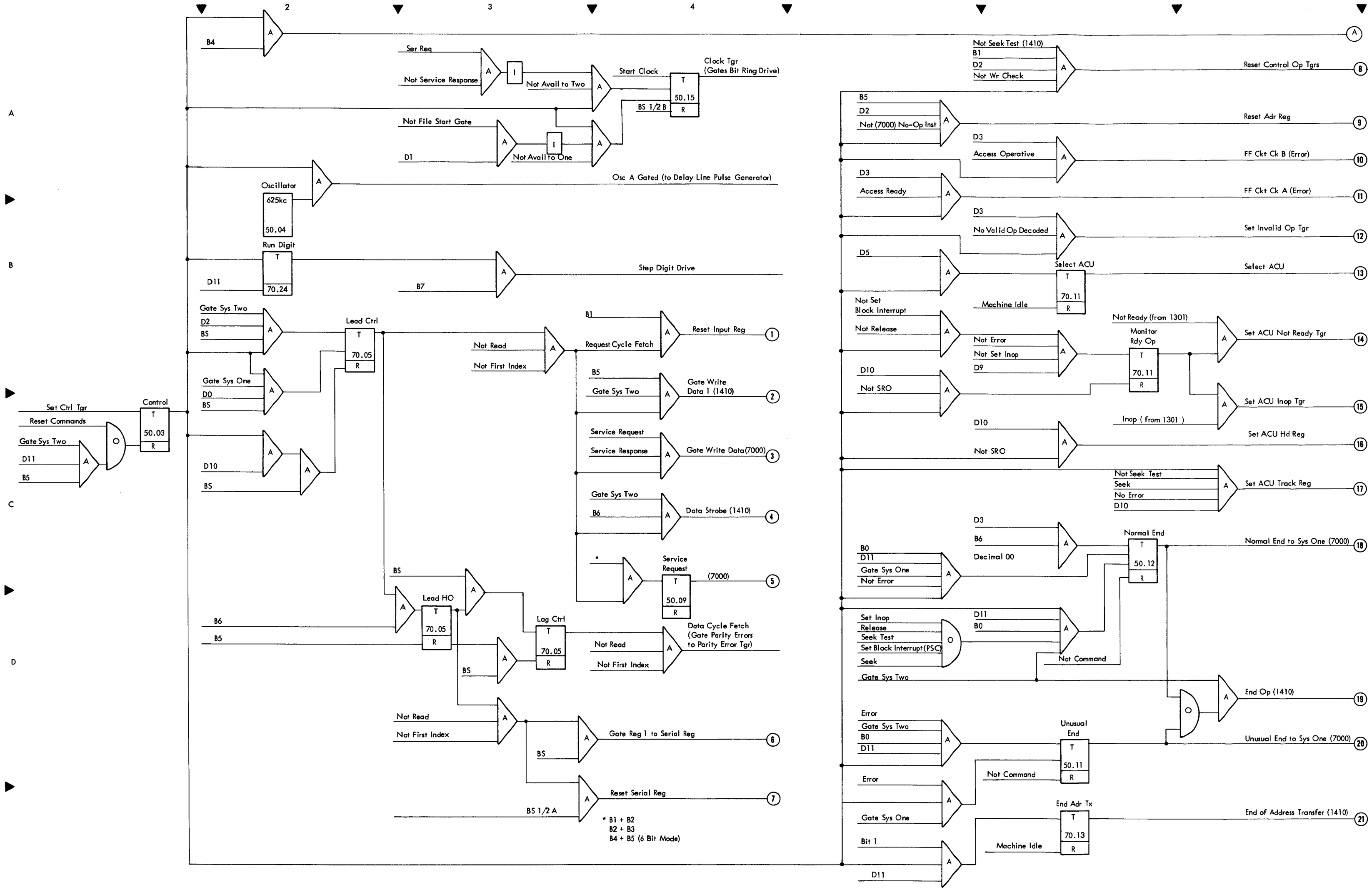


Figure 78. (Sheet 1 of 2). Control Cycle Simplified Logic

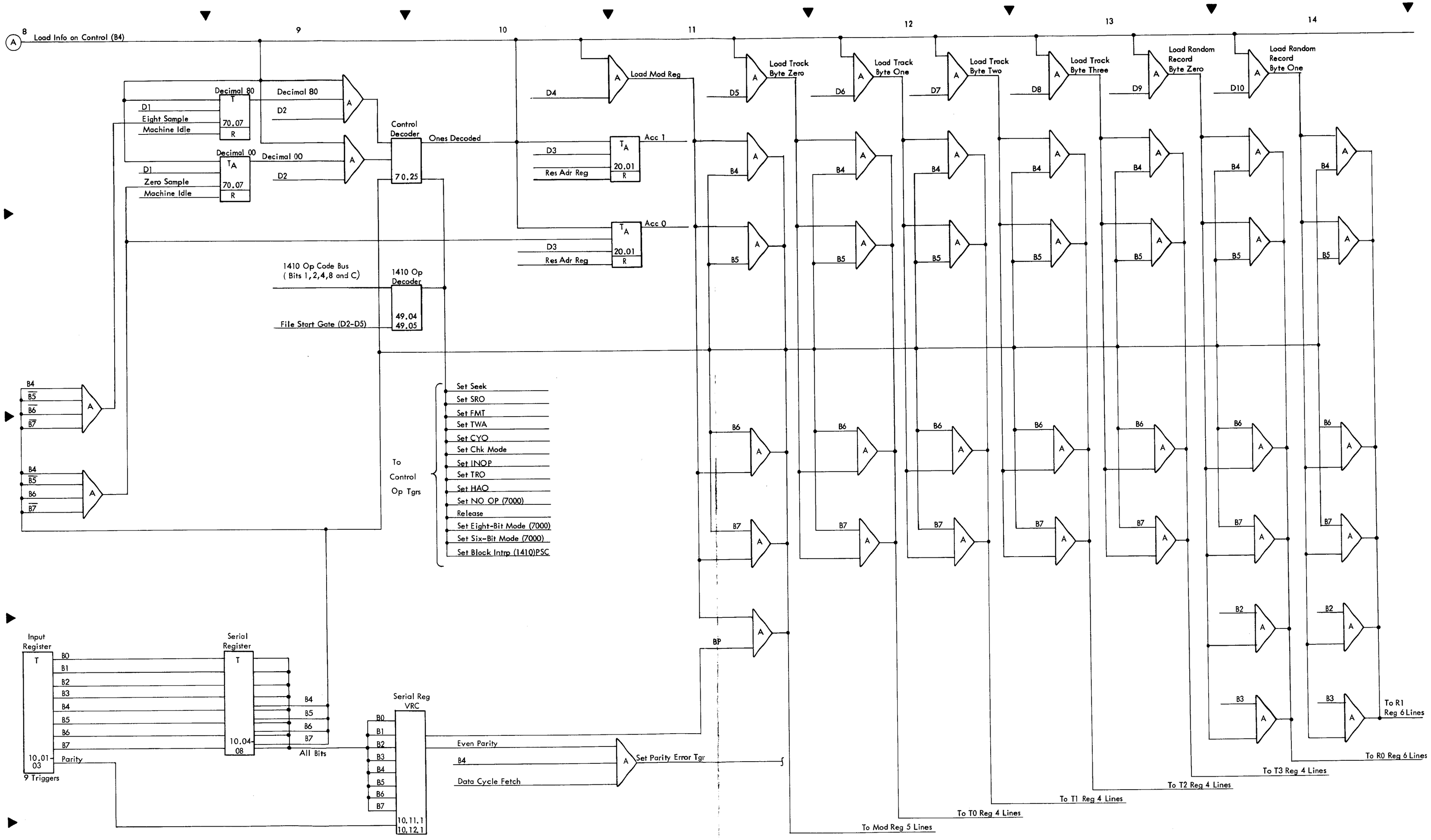
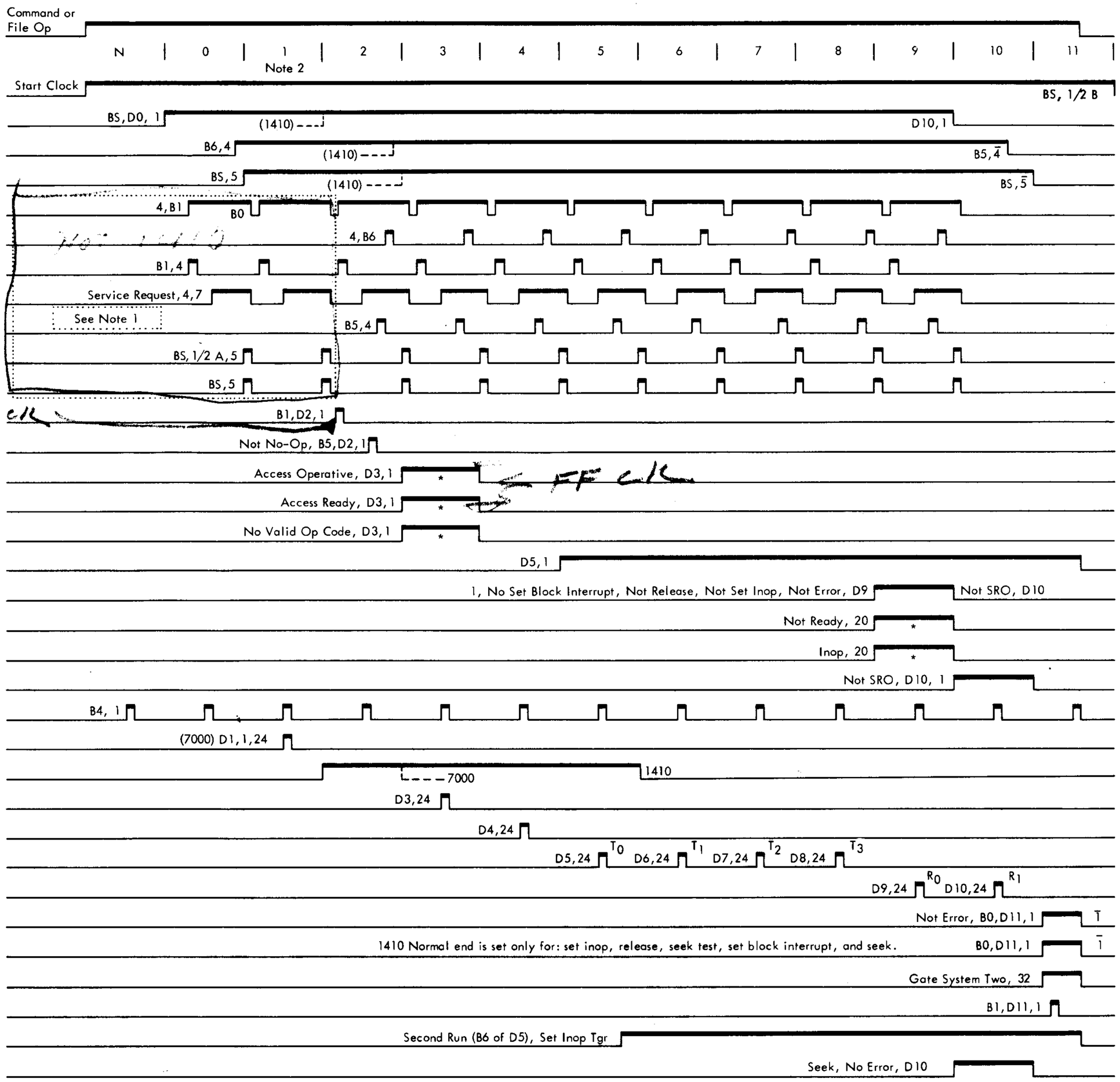


Figure 78. (Sheet 2 of 2). Control Cycle Simplified Logic

1.	Control Tgr	50.03
2.	Digit Time	
3.	Clock Tgr	50.15
4.	Lead Ctrl Tgr	70.05
5.	Lead HO	70.05
6.	Lag Ctrl Tgr	70.05
7.	Service Request	50.09
8.	Data Strobe	70.05
9.	Reset Input Reg	50.08
10.	Gate Write Data (7000)	50.09
11.	Gate Write Data 1 (1410)	50.09
12.	Reset Serial Reg	50.08
13.	Gate Reg 1 to Serial Reg	50.08
14.	Reset Control Op Tgrs	70.09
15.	Reset Address Reg	70.06
16.	FF Ckt Ck B (Error)	70.12
17.	FF Ckt Ck A (Error)	70.12
18.	Set Invalid Op Tgr (Error)	70.10
19.	Select ACU	70.11
20.	Monitor Ready Op	70.11
21.	Set ACU Not Ready Tgr (Error)	70.12
22.	Set ACU Inop Tgr	70.12
23.	Set ACU Hd Reg	70.12
24.	Load Info on Control	50.03
25.	Set Decimal 80 Tgr (7000)	70.07
26.	Set Control Op Tgr	70.08-09
27.	Set Access Reg	20.01
28.	Load Module Reg	20.02
29.	Load Track Reg	20.04-09
30.	Load Random Record Reg	20.11-13
31.	Normal End Tgr (7000)	50.12
32.	Normal End Tgr (1410)	50.12
33.	End Op to 1410	50.11
34.	End of Address Transfer	70.13
35.	Set Access Inop (In-Op Order)	70.08
36.	Set ACU Track Reg	70.12



*: Error Conditions

Note 1: Area enclosed with dots shows timing function that do not occur in 1410 operation.

2: 1410 Pauses in D1

Figure 79. Control Cycle Timing for 1410 and 7000 Systems

interrupt, or seek, end op is issued at B0 of D11; as a result, end op precedes end of address transfer and causes the 1410 to end file operation (circle 19). Figure 80 is a control flow chart; the flow chart serves as a functional review of control operations.

11. If the instruction is not in-op, release, seek test, set block interrupt (PSC), or seek, end of address transfer is issued at B4 of D11; end of address transfer prepares the 1411 for read or write data transfers (circle 21).

7000 Control Cycle

- **Initiated by data channel control command.**
- **Can be divided into three areas of operation.**
- **Timing operation—necessary controls for operation of the bit and digit ring.**
- **Request and store circuit operation—develop service requests to gate order and control word from system.**
- **Miscellaneous circuit operation—develop controls to operate the 1301 and tests to determine status of file.**

The control cycle executed in response to the control command causes the 7631 to decode the first two characters received over the write bus. The control op decoder decodes the first two characters transferred; the decoder output sets the corresponding control op trigger.

If the first character decoded is an eight, the decimal 80 trigger is set; after the second character is decoded, the decoder output sets either the inop, seek, write check or one of the prepare to verify triggers. A two-character order code and eight characters of address data are transferred to complete a control cycle if a decimal 80 order is decoded. If the first order character decoded is a 0, the decimal 0 trigger is set. If the decimal 0 trigger is set, the control cycle ends after the two-character order code is transferred. Decimal 00 orders are: release, six-bit mode, eight-bit mode, or no-op. When a decimal 80 order is decoded, the data request circuits gate the address data from the write bus into the input register with pulses D2 through D9. For each character transferred from the write bus into the input register, the 7631 issues a service request, and pulses D3 through D10 transfer the input register to the serial register. The contents of the serial register are sequentially stored in the access, module, track and random record registers with pulses D3 through D10. At D11, the file control determines whether normal end or unusual end is required to complete the control operation.

Briefly, the control cycle operation can be divided into three parts:

1. Timing operations
2. Request and store circuit operations
3. Miscellaneous circuit operations

Timing Operations

Control cycle timing starts at DN; the control cycle ends at D3 for the decimal 00 type orders, or at D11 for the decimal 80 type orders. The control command sets the control trigger; the oscillator is gated to the delay line pulse generator, and the run digit trigger is set (Figure 78). The control command gates start clock. Start clock sets the clock trigger; the clock trigger gates the bit ring drive. B6 resets the instruction block trigger; start clock is removed from the clock trigger. The clock trigger remains set with the not available to two AND (upper left corner, Figure 78). If a service request is issued and a service response is not received, BS1/2B resets the clock trigger to hold the bit ring until a service response is received. Because the data channel circuits operate faster than the file control, a late response should not occur.

Request and Store Circuit Operations

When the lead control trigger is set with BS of D0, the data request circuit operations start. (The following references refer to the circled numbers on Figure 78, sheet 1.) When lead control, not read and not first index AND, request cycle fetch is generated. Request cycle fetch conditions:

1. Input register reset (circle 1)
2. Input register loading (circle 3)
3. The service request (circle 5)

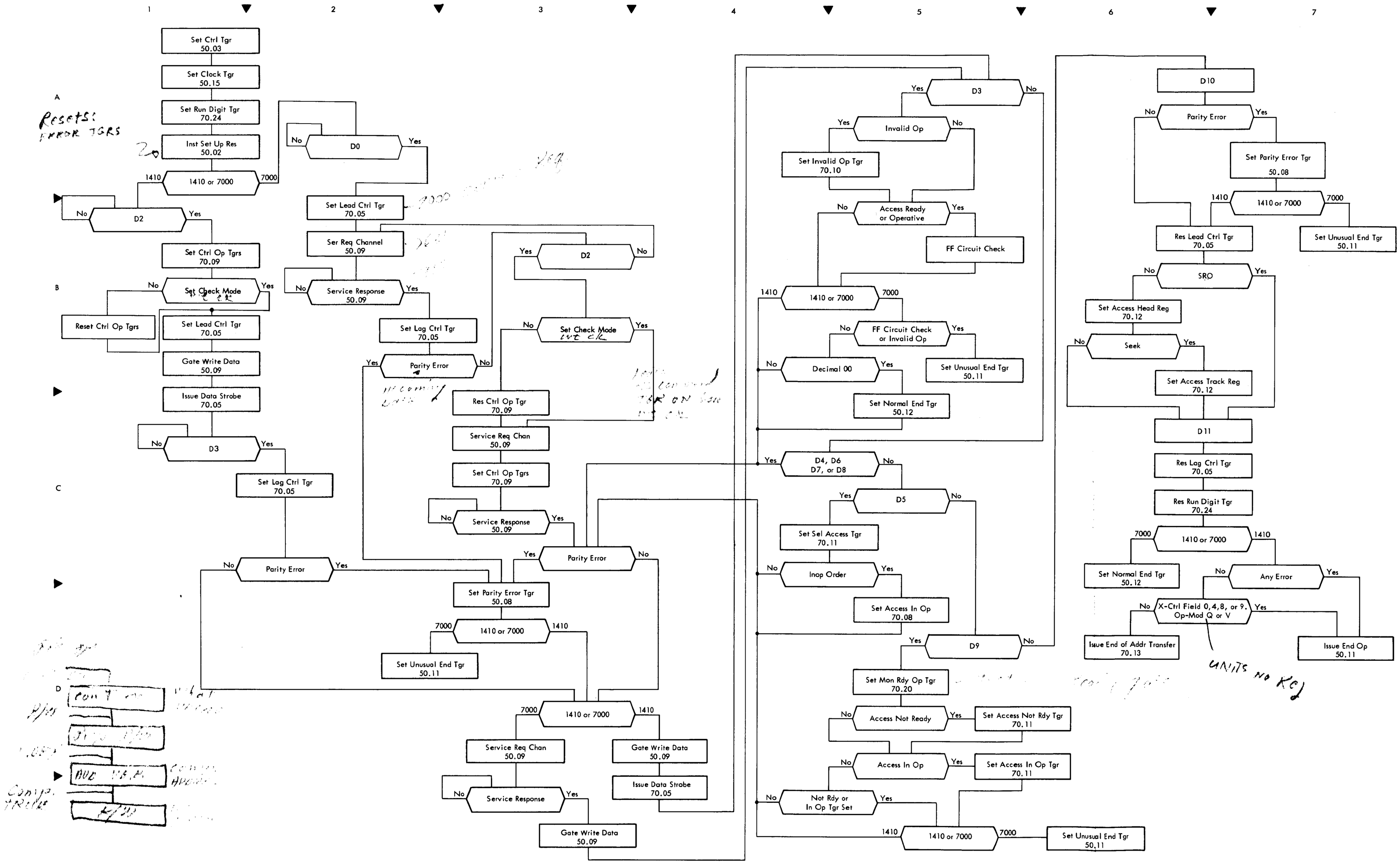


Figure 80. Control Cycle Flow Chart

At B6 of D0, the lead holdover trigger is set. Lead holdover, not read, and not first index AND to control:

1. Serial register reset (circle 7)
2. Transfer from the input register to the serial register (circle 6)

Figure 79, lines 4 through 13, shows the request and transfer circuit timing. Line 24 shows that load info on control is generated for all control digit cycles. Load info on control is generated for all control digit cycles. Load info on control and digit timing are used to store the serial register contents (Figure 78, sheet 2).

At D1, the serial register output is decoded; the decoding determines if the first control character transferred from the system is an eight or a zero (Figure 78, sheet 2, left side). D1, load info on control, and either the eight sample or the zero sample AND to set either the decimal 00 or the decimal 80 trigger. D2, load info on control, and either the decimal 80 or the decimal 00 trigger output AND with the serial register contents (the second character transferred) to set one of the control op triggers. If the order is decimal 80, load info on control gates the serial register contents to the access, module, track, and random record registers with pulses D3 through D10.

Miscellaneous Operations

The following references refer to the circled numbers in Figure 78, sheet 1. Their functions are:

1. B1 of D2 resets the control op triggers for all orders except write check (circle 8). If the order is write check, the control op trigger reset is inhibited. The seek and set in-op triggers are reset at the end of every control cycle, and the no-op trigger is reset at the beginning of every control cycle. The bit mode trigger is set with the six-bit mode and release orders; the bit mode trigger is reset with the eight-bit mode order.
2. The address register is reset at B5 of D2 (circle 9). Collectively, the access, module, track, and random record registers are called the address register.
3. Access ready or operative cause file frame circuit checks at D3, because the access and module are not selected until D5 (circles 10 and 11).
4. If an invalid op code is decoded, the invalid op trigger is set at D3 (circle 12).
5. If the order decoded is decimal 00, the normal end trigger is set with B6 of D3 to complete the control operation (circle 18). If any error is detected, the unusual end trigger is set, and an immediate unusual end results (circle 20). Figure 81 shows decimal 00 timing.
6. For decimal 80 orders, the select ACU trigger is set at D5 (circle 13). Select ACU selects the specified access and module; the selected access and module indicate ready and operative, if operating correctly.
7. Set access inoperative is issued to the file frame at B6 of D5 if the instruction is set access inoperative (Figure 79, line 35).
8. The monitor ready operative trigger is set at D9; it tests for the presence of not ready or inoperative from the selected access unit (circles 14 and 15). The monitor ready operative trigger is not set when the instruction is release, set in-op, or if an error is detected.
9. If the instruction is not SRO, set ACU head register is issued to the file frame at D10; set ACU head register transfers the head register bits from the 7631 to the 1301 head register, and resets the monitor ready operative trigger (circle 16).
10. If the instruction is seek and there are no errors, set ACU track register is issued to the 1301; set ACU track register transfers the 7631 track register cylinder and head bits to the 1301 at D10 (circle 17).
11. If no errors are detected, normal end is issued to the data channel at B0 of D11 to complete the file operation (circle 18). While operating with system one, any control error detected causes immediate unusual end (circle 20).

The control cycle operation is summed up in Figure 80. Figure 78, sheet 2, shows that every character is parity-checked while stored in the serial register. Control parity errors cause immediate unusual end.

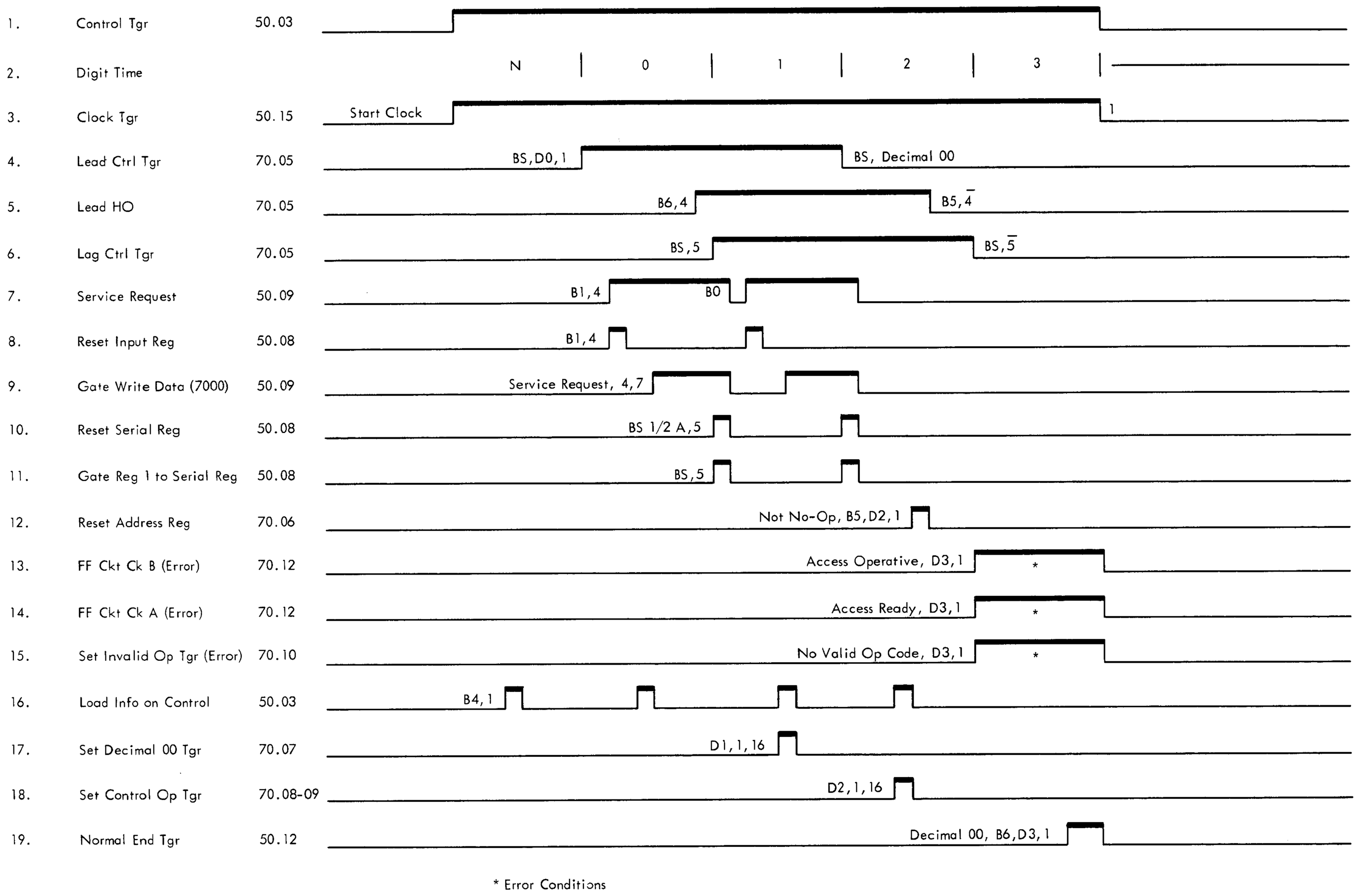


Figure 81. Decimal 00 Control Cycle Timing for 7000 Systems

Prepare to Read-Write Cycle

- **Initiated from 7000 by read or write command.**
- **Initiated from 1410 by read or write signal from channel input or output mode.**
- **Selects and conditions 1301 to read or write.**
- **Performs circuit checks for proper file operation.**
- **Ends at D4 time and is followed by verify address cycle.**

The prep read-write cycle conditions numerous circuits in the 7631 and 1301 prior to starting read or write data operations. When read or write and not select ACU AND, the prep read-write trigger sets. The 7631 read or write triggers are set with 7000 system read or write commands, or when 1410 read or write signals AND with the second file start gate and the not control conditions.

Prep read-write cycle timing is developed from the oscillator because no read or write data transfers occur between the 1301 and the 7631. Read or write sets the prep read-write and run digit triggers. When the prep read-write trigger output gates 1/2 bit B the clock trigger sets; the clock trigger gates the bit ring.

The prep read-write cycle functions are listed and numbered in the following list. Each number in the table corresponds to the circled numbers in Figure 82.

1. *Gate the Timing:* the timing circuits, oscillator, delay line pulse generator, bit and digit rings, are started to sequence the prep rd-wr cycle.

2. *Test the Validity of the Address:* prevents the customer from reading or writing on CE tracks 9 #60 through 9 #99 (254) or when the access mechanism is in the re-zero position. In test mode, the CE track switch must be ON to read or write. Invalid address causes immediate unusual end.

3. *End of Address Transfer Trigger Reset (1410 Only):* resets the end of address transfer trigger when reading or writing follows a control operation.

4. *Test for an Invalid Sequence:* before issuing a read or write signal, the attached system issued the operation code (1410) or order (7000) to the file control. The absence of a prepare to verify op code followed by read or write, or an operation code used only for writing followed by read, causes immediate end with an error indicated.

5. *Select the 1301 Access and Module:* module selection, one of ten possible selections, is gated to the specified 1301. The module and the previously-transferred access selections remain unchanged until the reading or writing is completed.

6. *Set the T2B2 Binary Trigger Position of the Cylinder Counter:* the trigger, if set with head 39 selected, causes overflow to end a cylinder operation (CYO) after reading or writing the last track of the cylinder.

7. *Test the Selected 1301 Access Unit (ACU) for Not Ready and Inoperative Indication:* the ready monitor trigger is set for the duration of the read or write operation; it causes an immediate error stop if the selected access unit indicates not ready or inoperative to the file control.

8. *Test 1301 Read and Write Safety Conditions:* the read monitor trigger is set to gate three possible safety error conditions. If the file frame (1301) read safety is off, write safety is on, or if the write monitor trigger is set and write safety is off, an immediate error stop occurs. The test insures that the 1301 is in read status at the start of each read or write operation; the read status of the 1301 should not change until the file control is prepared to write data.

9. *Transfer Flag on HAO (HAO-CE Only):* an alternate track address transfer occurs from random record register R0 to the serial register to test for flag bits.

10. *Set Head Pulse on HAO (HAO-CE Only):* the function permits a customer engineer to select an alternate data track to replace a damaged data track without physically removing the damaged disk. The set head pulse on HAO gates the serial register flag bits (comment nine of this table) to the selected 1301.

11. *Select the Read-Write Head:* the pulse causes the 1301 to select the specified read-write head.

12. *Generate AGC Squelch Conditions (SRO only):* the SRO operation is not started with index signals. Index area filler cannot be used to adjust the 1301 read amplifier gain prior to reading data; therefore, the file control generates AGC squelch, a 350 μs signal, plus a 200 μs delay to adjust the 1301 read amplifier before reading data.

13. *HAO-CE Format Write Data Request:* the HAO-CE format write operation bypasses the address compare cycle. A format write instruction with an address compare cycle (not HAO-CE type) requests and stores the first two format write data characters at the end of the address compare cycle; therefore, the HAO-CE format prep rd-wr cycle data is needed to insure that two format write data characters are transferred and available for writing before late index.

The common functions that occur during a prepare to read-write cycle are shown in Figure 83. A further review of prepare to read-write cycle operation is presented in flow chart form in Figure 84.

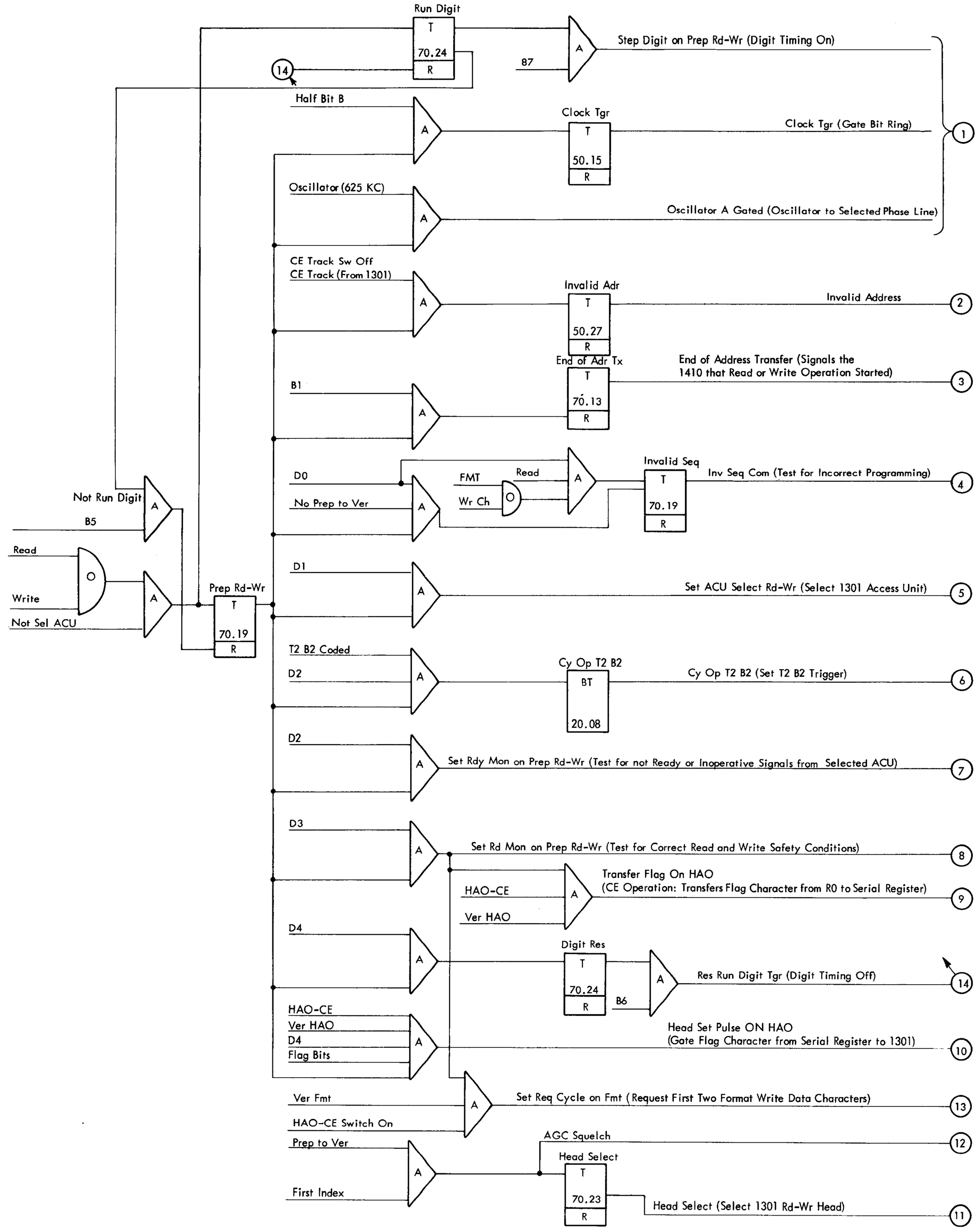


Figure 82. Prep Read-Write Cycle Simplified Logic

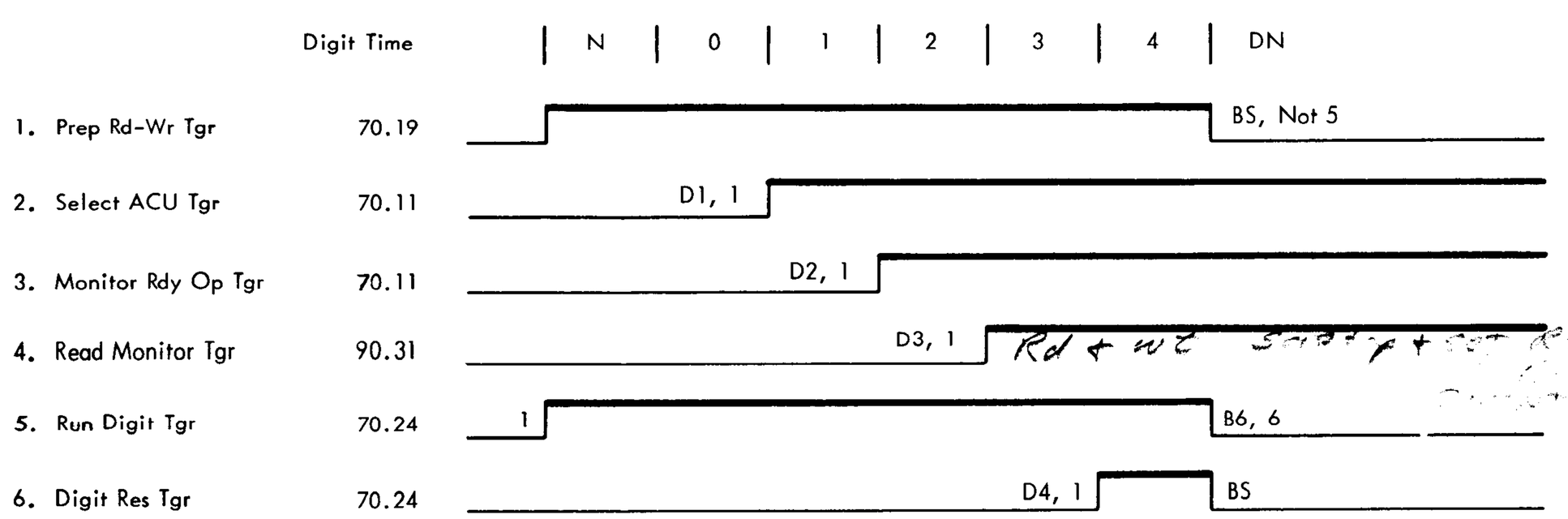


Figure 83. Prep Read-Write Cycle Timing

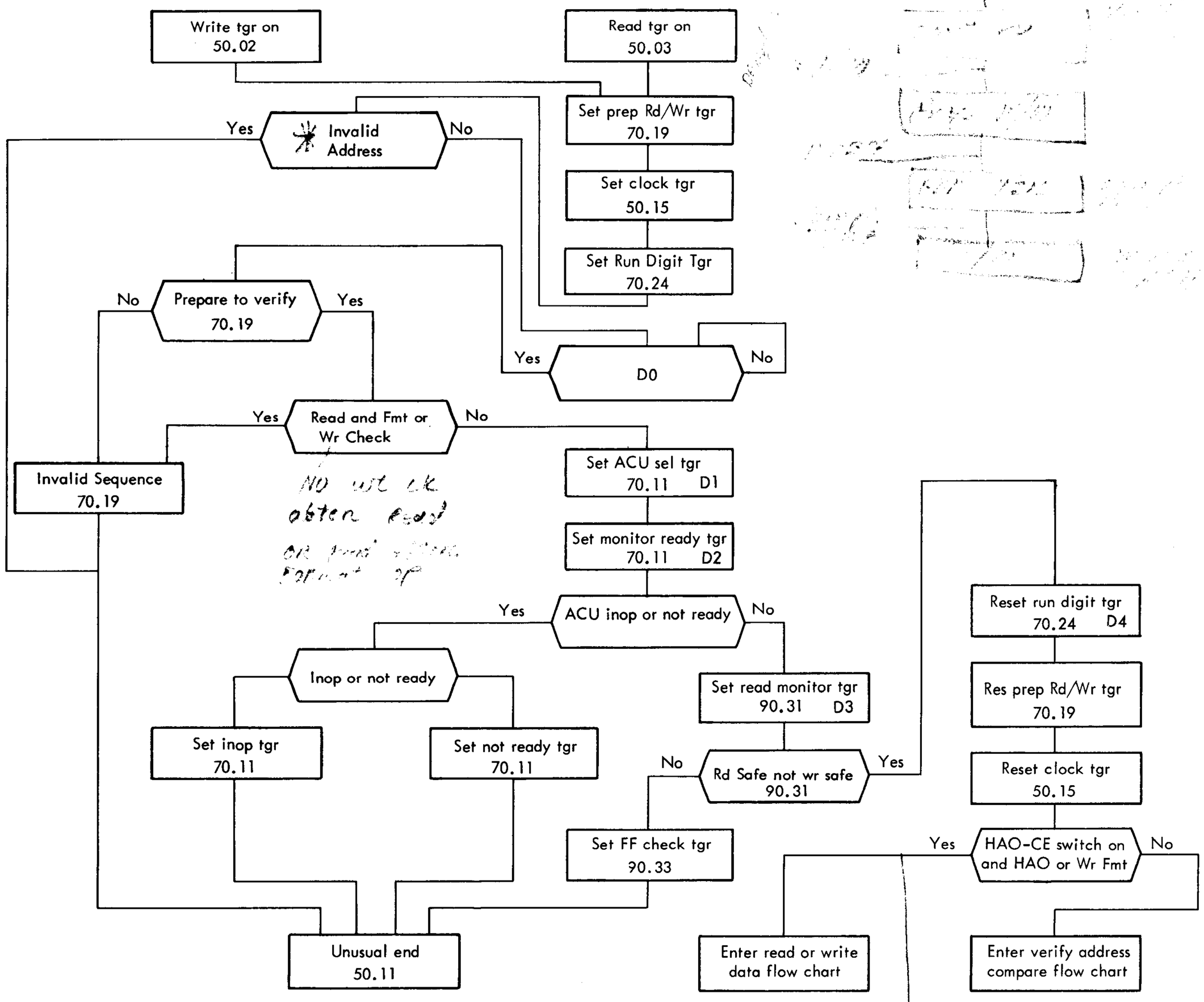


Figure 84. Prep Read-Write Cycle Flow Chart

Verify Address Cycle

- **Compare HA1 with track register.**
- **Indicate compare true if HAO or wr fmt.**
- **Compare HA2 with random record register.**
- **Indicate compare true if TRO, TWA, CYO.**
- **A compare fail indicates no record found.**

When required, the verify address cycle occurs before read or write data transfer. The type of verify address cycle required for each instruction is outlined in Figure 26. Because the majority of the programmed operations verify both HA1 and HA2, Figure 85 shows the verify timing for both of them. The verify address cycle is divided into two major parts:

1. Home Address 1
2. Home Address 2

Because the format recognition, timing, and verify address circuits are so closely related, their operation cannot be presented separately; therefore, the verify address cycle is easier to understand if the objectives are reviewed (assume the following operation is a TRO):

1. Late index gated sets the verify address trigger; verify address and digit timing control the track register compare sequence.

2. The format recognition circuits must locate the address area.

3. Address area is a key signal; it causes this sequence:
   a. Sets the hold phase trigger to provide hold phase timing before reading.
   b. Sets the run digit trigger to start digit ring timing.
   c. Home address area trigger output and address area AND to signal HA1.

4. D0 sets the verify monitor; verify monitor gates the compare circuit output to the compare fail trigger.

5. D0 gates the first compare circuit test; if the compare circuit fails the test, a FA circuit check causes immediate unusual end.

6. D1 gates the second compare circuit test; if the compare circuit fails the test, a FA circuit check causes immediate unusual end.

7. B1 of D1 sets the info search trigger; info search conditions the 7631 to set the read gate in the gap following the AGC.

8. B1 of D1 resets the hold phase trigger to end hold phase timing; the circuits pause at BS of D2.

9. BS of D2 transfers T0 to the serial register in preparation for the first HA1 comparison.

10. The read gate is set when the data gap single shot detects the gap.

11. The read gate permits read data flow to the timing circuit circuits, the shift register and the compare circuits.

12. The timing circuits select a phase and generate read data timing.
   a. Read data timing is used to transfer read data into the shift register.
   b. Read data timing is used to transfer and compare serial register data bits with the read data bits until BS.

13. BS and verify address transfer the next track register character to the serial register.

14. The circuit operation described in steps 11 and 12 repeats until the first four HA1 characters are compared.

15. Because a missing sync gap separates the fourth HA1 character from the flag character, the timing circuits pause in the missing sync gap. Missing sync conditions the three zeros triggers to recognize check area.

16. The verify monitor is reset before reading the flag character to prevent compare failures when reading the flag.

17. The flag character is read and stored in the serial register.

18. The format recognition circuits signal the check area.

19. The verify monitor is set for the check character compare.

20. The check characters are compared with the contents of the shift register.

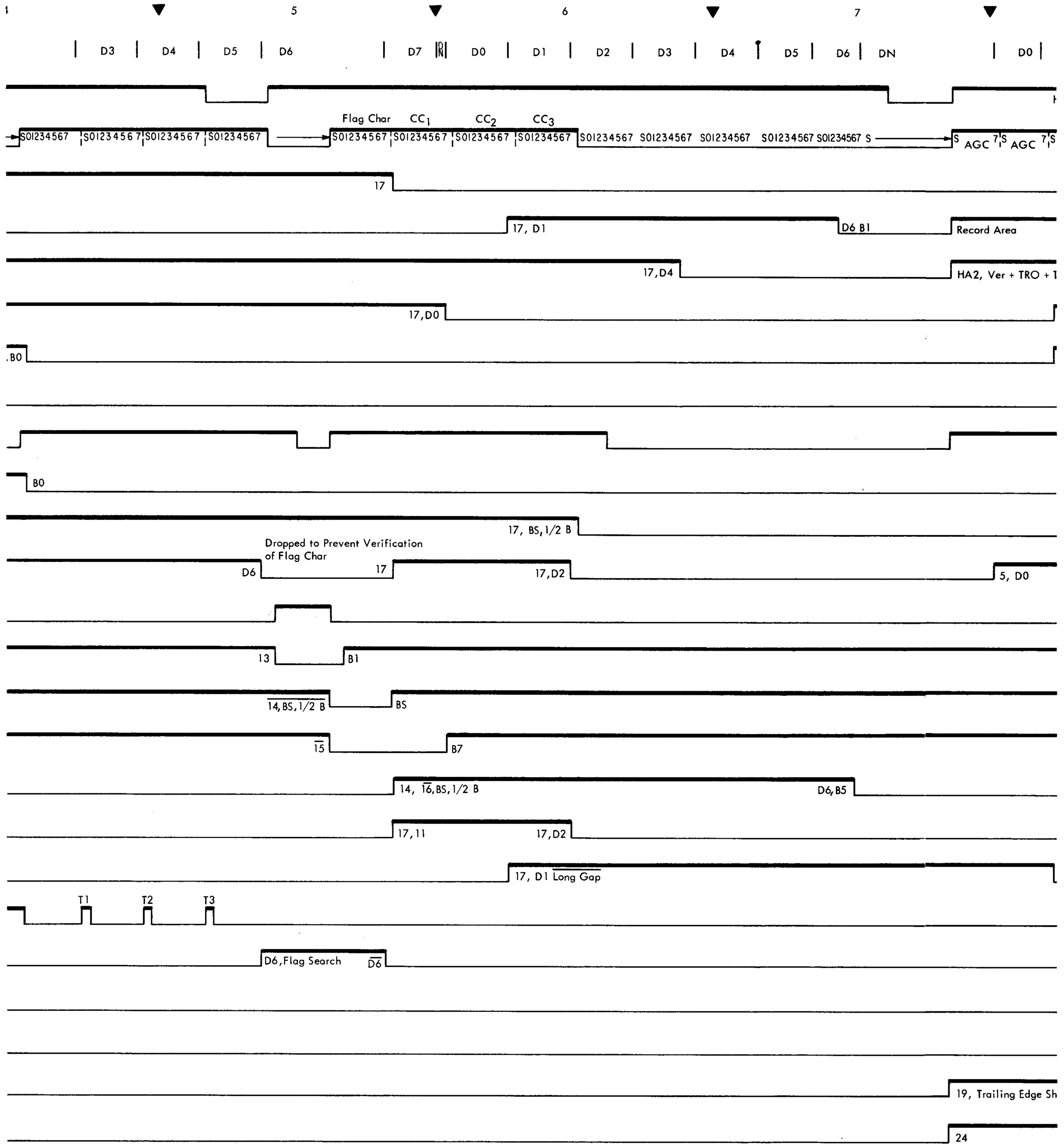
21. The hold phase trigger is set while comparing the last check character to provide timing after the last check character is read.

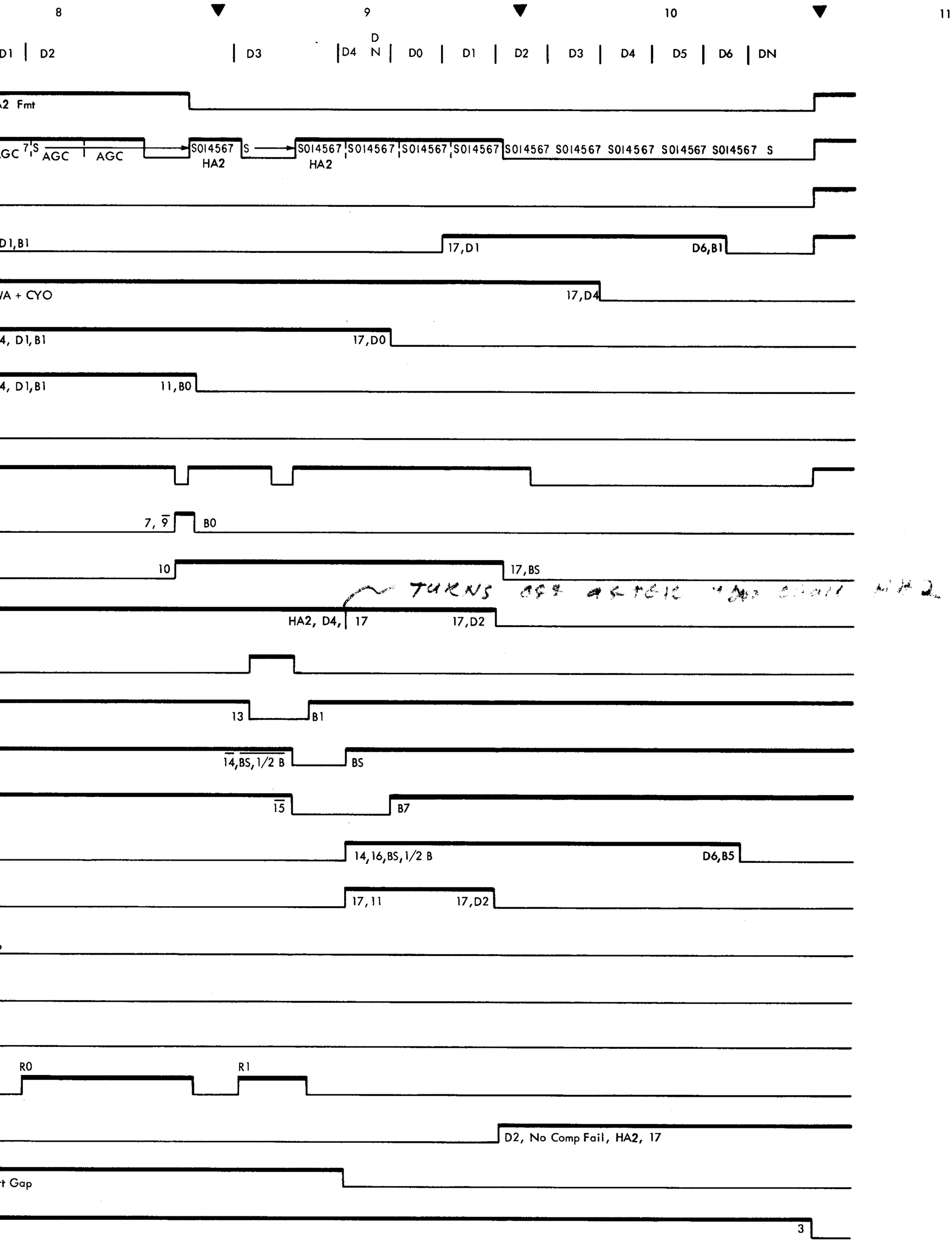
22. Flag bits in the serial register cause action on flag after the last check character is compared.

	1		2	3
				DN | D0 | D1 | D2
	1.	Format		HA1 Fmt
	2.	Data Filler		S AGC 7S AGC 7S AGC 7S AGC AGC
A	3.	Address Area	50.25	Trailing Edge Long Gap
	4.	Hold Ø (Phase)	50.23	Address Area D1,B1
▶	5.	Verify Add	50.28	HA1, Ver TRO + TWA + CYO or WR Fmt + HAO (Not CE)
	6.	Check Prep	50.26	3, D1,B1
	7.	Info Search	50.22	3, D1,B1 11
B	8.	Compare A-B	50.28	D0,B1 D1,B1
	9.	Data Gap SS (6.6 usec)	50.22	
	10.	Info Prep	50.22	7, 9
	11.	Read Gate	10.15	10
▶	12.	Verify Monitor	50.30	5, D0
	13.	Missing Sync Bit	10.16	
C	14.	First Zero Trig	80.03	
	15.	Second Zero Trig	80.03	
	16.	Third Zero Trig	80.03	
	17.	Check Area Read Mode	50.26	
▶	18.	Check Character Gate (Read Out)	50.20	
	19.	Record Prep	50.25	
	20.	Track Reg to Ser Reg on Compare	50.29	T0
D	21.	Serial Rd Data (Gate Flag to Serial Reg)	10.15	
	22.	Record Register to Serial Register on Compare	50.29	
	23.	Compare True	50.30.2	
	24.	Record Area	50.26	
▶	25.	Record Holdover	50.33	

Note: Digit Timings and Format Areas have different Timings for HAO Read (see Figure 5.23).

Figure 85. Verify Address Cycle Timing


1
5
6
7
D3
D4
D5
D6
D7
D0
D1
D2
D3
D4
D5
D6
DN
D0
Flag Char
CC1
CC2
CC3
S01234567
S
AGC 7
17
17, D1
D6 B1
Record Area
17,D4
HA2, Ver + TRO + 1
17,D0
,B0
B0
17, BS,1/2 B
Dropped to Prevent Verification
of Flag Char
D6
17
17,D2
5, D0
13
B1
14,BS,1/2 B
BS
15
B7
14, 16,BS,1/2 B
D6,B5
17,11
17,D2
17, D1 Long Gap
T1
T2
T3
D6,Flag Search
D6
19, Trailing Edge Sh
24


8
9
10
11
D1
D2
D3
D4
D
N
D0
D1
D2
D3
D4
D5
D6
DN
A2 Fmt
GC 7 S
AGC
AGC
S014567 S
HA2
S014567 S014567 S014567 S014567 S014567 S014567 S014567 S014567 S014567 S
HA2
D1,B1
17,D1
D6,B1
VA + CYO
17,D4
4, D1,B1
17,D0
4, D1,B1
11,B0
7, 9 B0
10
17,BS
TURNS OFF ARTIC "DO START HA2
HA2, D4,
17
17,D2
13
B1
14,BS,1/2 B
BS
15
B7
14,16,BS,1/2 B
D6,B5
17,11
17,D2
R0
R1
D2, No Comp Fail, HA2, 17
t Gap
3

Home Address One Timing

- **Locate HA1 area and control timing to operate in read mode.**
- **Test compare A and B developed.**
- **Locate read data and compare serially by bit with serial register which will have track register data.**
- **Locate flag character and read into serial register.**
- **Read and compare HA1 check character.**
- **Test serial register for flag bits (BCD 1, 2 or 4 bit), if present develop action on flag.**

The following verify address text should be related to the Verify Address Cycle Timing in Figure 85. When the format recognition circuits signal home address area one, the verify address sequence starts. Trailing edge long gap sets the address area trigger; address area sets the hold phase trigger. Hold phase conditions the timing circuits to select one of the four clock track phases; the timing is developed for the preparatory verify address functions. If the operation is TRO, address area sets the run digit and verify address triggers. At D0, the verify monitor trigger is set; verify monitor gates the compare circuit output to the compare fail trigger input.

At B1 of D0 test not compare A is generated; test not compare A is gated to the compare circuit read path where it is entered as a simulated read one-bit. The simulated read one-bit is compared with a write 0-bit to test the compare circuits. If a compare failure is detected, the verify monitor gates not data comp, and the compare fail trigger sets. If the compare fail trigger is off, B4 of D0 sets the file adapter circuit check trigger. File adapter circuit check causes immediate stop on error for read, write, or control operation; immediate stop on error sets the unusual end trigger. Unusual end is issued to 7000 systems, and end op is issued to 1410 systems.

Test not compare B is generated at B1 of D1. The bit timing for test not compare B is the same as for test A. The difference between test A and B is that test B compares a simulated read zero-bit with a simulated write one-bit. These two tests insure that compare circuits can detect both types of compare failures.

At B1 of D1 the check prep trigger and the info search trigger are set. With B1 of D1 the hold phase trigger is reset; the timing circuits pause at BS of D2. For the last function in preparation for the verify cycle, BS gates track register T0 contents to the serial register.

When the data gap singleshot times out in the gap following the AGC data, info search and the data gap single shot outputs AND to develop info prep. Info prep sets the read gate during the data gap. When the read gate is set, the phase select circuits sync on the first read data bit-sync, and a phase is selected. The resultant read timing gates read data from the 1301 read bus to data trigger A and then to data trigger B. Data trigger B output is gated to the compare circuits and into the shift register. Each timing bit generated gates the corresponding bit from the serial register to the compare circuit; each read data bit is compared with a bit transferred from the serial register. The bit by bit comparison occurs until BS of D3.

BS of each digit cycle transfers the contents of the next track register position (in this case, the contents of track register T1) to the serial register. A new phase selects with bit sync of D3. The phase select binary trigger is flipped at B4, while reading the first home address one character, to select the alternate phase selector. Also, BS inhibits the shift register operation to prevent read data bit-sync from entering the shift register.

With D3 bit timing, the contents of track register T1 (stored in the serial register) are read out serially by bit and compared with the second character of HA1 read data.

The verify address sequence is again repeated at BS of D4; the contents of track register T2 are transferred to the serial register. Again, the shift register operation is inhibited with BS. Receipt of the next read data bit sync selects a new phase because the binary trigger was flipped at the previous B4. The verify address repeats until the first four HA1 characters are compared with the contents of track registers T0, T1, T2, and T3.

B7 of D5 steps the digit ring to D6; the bit and digit rings stop at BS of D6 because a missing sync gap separates the last HA1 character from the flag character. The missing sync circuit output conditions the three zeros triggers; the three zeros triggers recognize check area after the flag character is read (Figure 85, line 13).

The flag search starts at D6; the flag character is read from the disk and transferred, without comparison, to the serial register. The flag character is stored in the serial register until after the check characters are processed (Figure 86). The verify monitor is reset to prevent compare failures during the flag search (Figure 85).

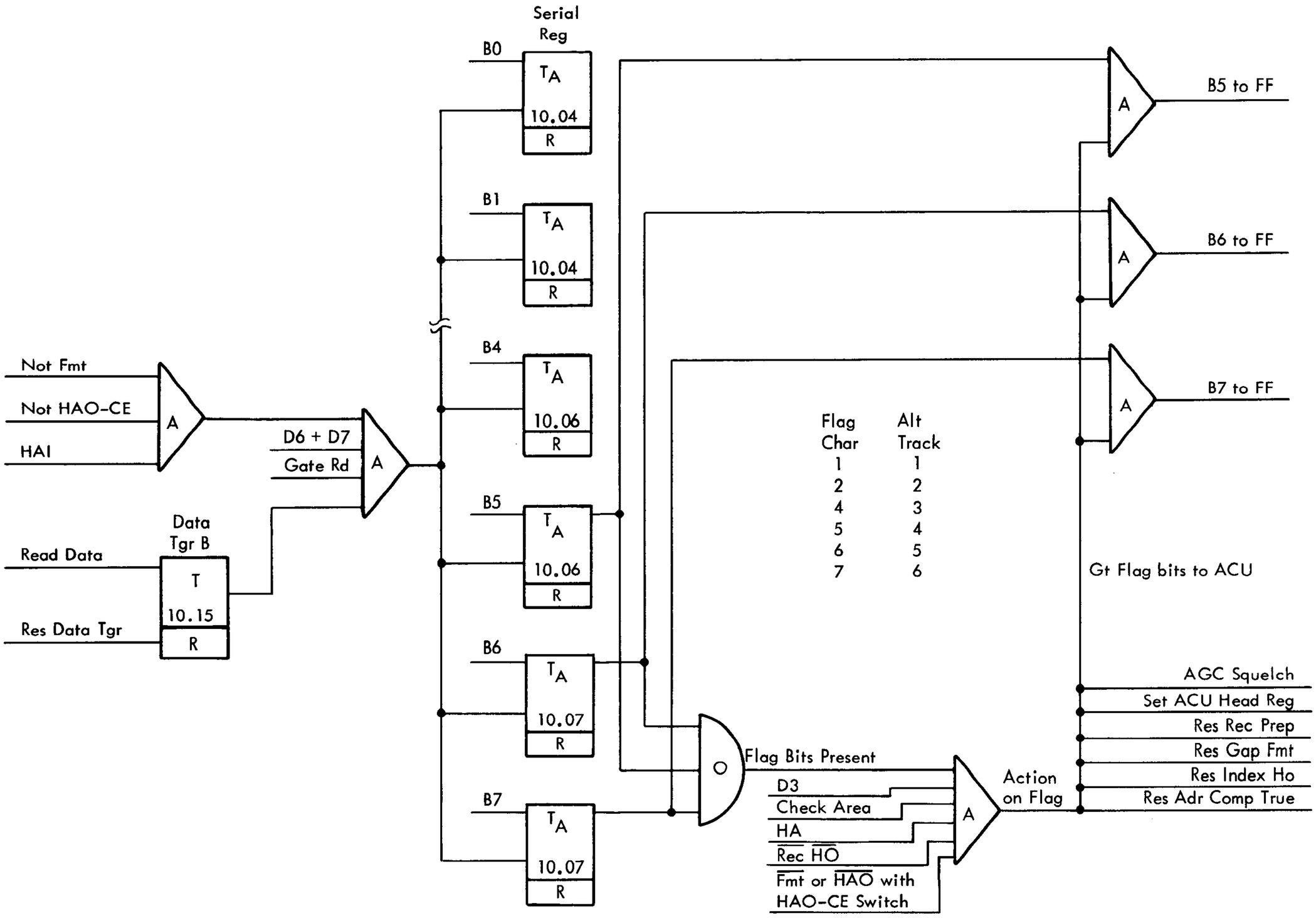


Figure 86. Flag Operation

After the flag is read, the three zeros triggers (Figure 85, lines 14, 15, and 16) set the check area trigger. Check area sets the read out and verify monitor triggers. The shift register contents are read out with the timing pulses developed from check character read data; the check characters generated by the shift register are compared with the check characters read from the disk. After three check characters are compared, the verify monitor trigger is reset because the verify address cycle for HA1 is completed. A compare failure, when comparing the first four characters of HA1, or check characters, sets the compare fail trigger.

The contents of the serial register are examined to determine if a flag operation is required. D3 of check area gates serial register bits five, six, and seven (the flag bits) to the flag circuit (Figure 86). If a flag bit or bits are present (positions five, six, or seven), action on flag occurs. Action on flag gates the contents of serial register positions five, six, and seven to the file frame. In addition, action on flag resets the address compare true, index holdover, gap format, and record prep triggers. Action on flag also causes the 7631 to issue AGC squelch and set ACU head register to the 1301; these conditions select an alternate track and start a verify address cycle on the alternate track.

The timing is required to test for flag bits in the serial register, and to end check area operation before HA2 is developed from the hold phase signal shown on Figure 85, line 4. While reading the last check character, the hold phase trigger is set. Because the binary trigger was flipped at B4 while reading the second check character, the alternate phase selector selects a new phase to read the last check character so that, when the hold phase trigger is set at D1, its operation does not interfere with the phase selection for reading a last check character. Hold phase prevents the binary trigger from flipping at B4 while reading the last check character; the phase selected while reading the last check character provides timing required to test for flag bits, to reset the verify address trigger, and to reset the check area trigger at B5 of D6. The hold phase trigger is reset at bit B1 of D6 to stop hold phase timing generation after D6.

Home Address Two Timing

- **Locate HA2 area and control timing to operate in read mode.**
- **Locate read data and compare first two characters serially by bit with serial register which will have random record register data.**
- **Read and compare HA2 check character.**

The objectives for HA2 verify are:

1. The format recognition circuits must locate record area.

2. Record area is a key signal; it causes the following sequence:

   a. It sets the hold phase trigger to provide hold phase timing before reading

   b. It sets the run digit trigger to start digit ring timing

   c. Home address area trigger output and record area AND to signal HA2.

3. D0 sets the verify monitor; verify monitor gates the compare circuit output to the compare fail trigger.

4. B1 of D1 sets the info search trigger; info search conditions the 7631 to set the read gate in the gap following the ACC.

5. B1 of D1 resets the hold phase trigger to end hold phase timing; the circuits pause at BS of D2.

6. BS of D2 transfers R0 to the serial register in preparation for the first HA2 comparison.

7. The read gate is set when the data gap singleshot detects the gap.

8. The read gate permits read data flow to the timing circuit circuits, the shift register, and the compare circuits.

9. The timing circuits select a phase and generate read data timing.

   a. Read data timing is used to transfer read data into the shift register.

   b. Read data timing is used to transfer and compare serial register data bits with the read data bits until BS.

10. Because a missing sync gap separates R0 from R1, the timing circuits pause in the missing sync gap. Missing sync conditions the three zeros triggers to recognize check area.

11. BS and verify address transfer the next track register character (R1) to the serial register.

12. The circuit operation described in steps nine and ten repeats until R1 is compared.

13. The format recognition circuits signal check area.

14. The check characters are compared with the contents of the shift register.

15. The hold phase trigger is set while comparing the last check character to provide timing after the last check character is read.

The verify address cycle for the HA2 area is similar to the HA1 verify operation. Briefly, the difference between the home address 1 and home address 2 verify operation is:

1. Test not compare A and test not compare B do not occur for HA2, because only one compare circuit test is required for verify address cycle.

2. There is only one flag character per track; therefore, a flag search does not occur for HA2.

The format recognition circuits set the record area trigger when trailing edge short gap is gated with record prep. The record area trigger output serves a similar function in HA2 as the address area trigger served for HA1 operation. For example, the record area trigger causes the hold phase and verify address triggers to set. The hold phase timing generated is used to set the verify monitor trigger at D0. At B1 of D1, the record area trigger causes the record prep and hold phase triggers to reset. The record area trigger also causes the check prep and info triggers to set. Because the hold phase trigger has been reset, the timing circuits stop operation at BS of D2. The contents of random record register R0 are gated with BS of D2 to the serial register, where they remain for the first read data character comparison.

When the data gap singleshot times out in the gap separating the ACC from the first HA2 character, info search and the data gaps singleshot outputs AND, and the read gate sets. Receipt of the first bit-sync from the disk selects a phase. The read timing generated is used to transfer the first HA2 character from data trigger A to data trigger B, and from data trigger B to the compare circuits; each bit is compared with the corresponding bit transferred from the serial register. The read bits are also entered into the shift register.

Comparison continues until the first character has been compared. For a two-character HA2, the missing sync circuit output prepares the three zeros triggers to recognize check area (Figure 85, lines 13, 14, 15, and 16). Timing remains suspended in the gap following the first HA2 character until bit sync of the second HA2 character selects a new phase. While the timing is suspended at D3, the contents of random record reg-

ister R1 are transferred to the serial register to prepare for comparing the second and last HA2 character.

When the first bit sync of the last HA2 character arrives, a new phase is selected to restart the timing. Again, the timing generated is used to compare the contents of the serial register with the last HA2 character.

When the three zeros triggers signal check area, the record area trigger is reset and the readout gate is set. The read timing continues to sync on each check character bit-sync as it is read from the disk. With the readout gate active, the check characters read from the disk are compared with the contents of the check character register. To complete check area timing, hold phase is set at D1 prior to reading the last check character. Hold phase timing resumes immediately after the last check character read to provide the remaining check area timing. At the end of check characters, the readout, verify monitor, and the read gates are reset. If the compare fail trigger is off, the compare true trigger is set; compare true permits a read or write data cycle to follow. If the compare fail trigger is set, compare fail, B2, D2, and check area AND to signal no record found. No record found causes the 7631 to issue unusual end or end op. Finally, the verify address trigger is reset at D4 and the hold phase trigger is reset at B1 of D6 to complete the verify address cycle.

Figure 87 shows the verify address cycle for record and address areas in flow chart form.

Read Data Cycle

- **Initiated after a compare true is set.**
- **Locate read data area and control bit and digit ring to operate in read mode.**
- **Locate read data to assemble read characters in serial register and develop check character in shift register.**
- **Develop necessary gates to transfer read data character to system.**
- **Locate check area and compare check character with shift register.**
- **End operation if system has sent stop.**

A read data cycle can be divided into three parts:

1. Format recognition
2. Timing
3. Data transfer

The operation of the format recognition timing and the data transfer circuits are so closely related that their operation cannot be presented individually. It is easier to understand the read data cycle operation if the objectives are reviewed:

1. A read data cycle cannot occur unless the compare true trigger is set. As shown in the verify address cycle sequence, if no record found occurs the file control prevents further file operation by executing an immediate end. Following a successful verify address cycle the compare true trigger is set.

2. Depending on the prepare to verify instruction, the data transfer circuits remain inactive until the recognition circuits locate the specified address or record area.

3. Hold phase advances the timing in the address or record ACC area.

4. The data gap must be sensed to set the read gate.

5. With the read gate set, the data transfer circuits assemble each read data bit in the serial register and enter the bits into the shift register to generate check characters. Check characters are used to test the validity of the read operation after all the address or record area data has been read and transferred.

6. Each read character assembled in the serial register is assigned parity before being transferred to the system.

7. After all the characters have been transferred from the address or record area, the check characters generated by the shift register are read out to the compare circuits and are compared bit by bit with the check characters read from the track.

8. After check character comparison the read gate is reset; therefore, timing must operate in hold phase to complete the check area timing and to prepare the recognition circuits for the next format record or address area.

9. If a stop or disconnect signal is received while reading record or address data, the file control does not stop operation. Receipt of stop or disconnect resets the data transfer circuits, and data transfers are stopped, but the 7631 continues to read and generate check characters to complete the record or address read. The file control must generate a complete set of

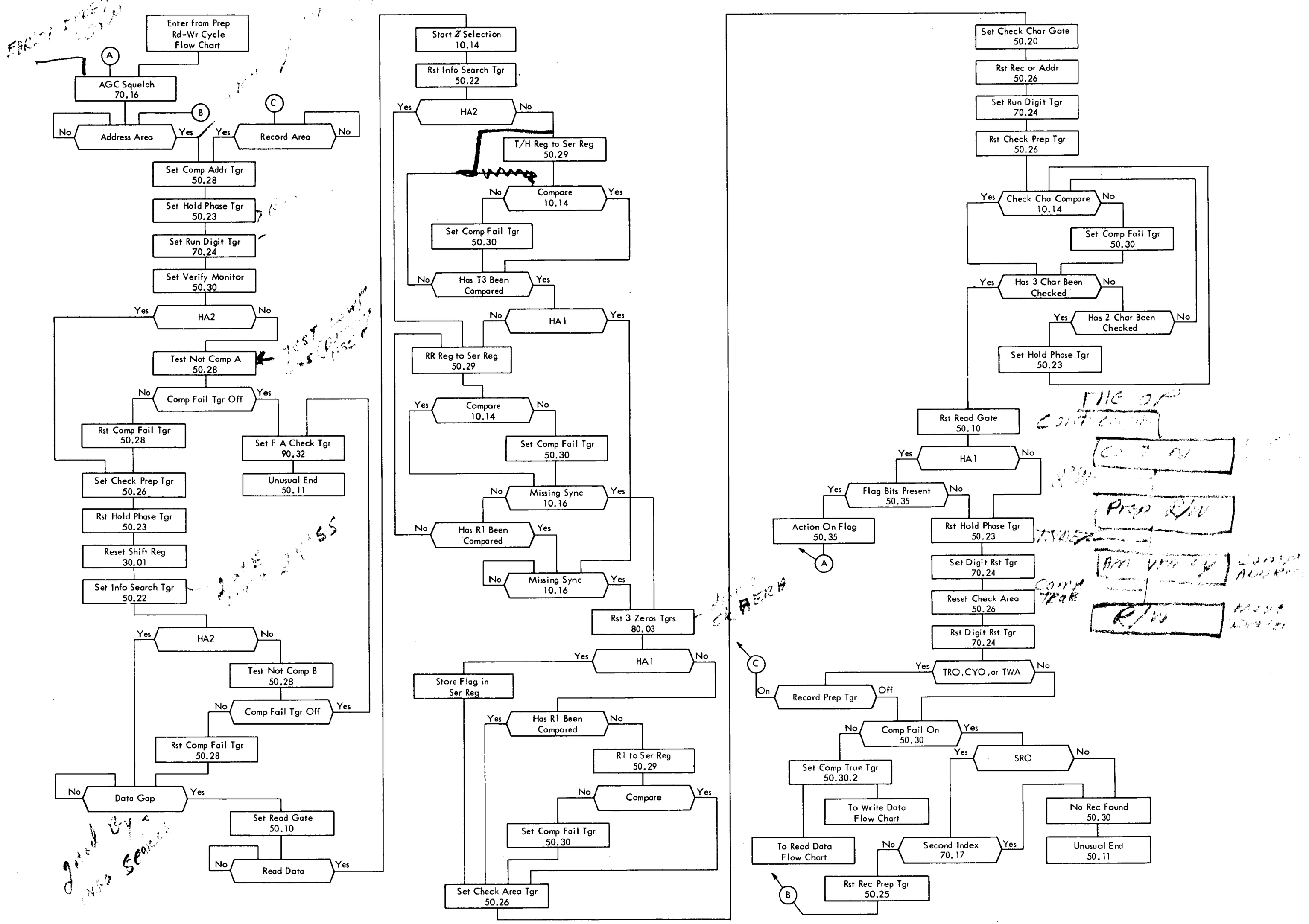


Figure 87. Verify Address Cycle Flow Chart

check characters for the read data; the check characters generated must compare with those read from the disk. After the generated check characters are compared with those read from the disk, the file control signals end to the attached system. (This depends on the type of prepare to verify order.) Because the check characters compared, the file control can signal a normal end.

10. If an error occurred, the parity error trigger is set. The parity error causes a data check to be indicated to a 1410 system or a parity error to be indicated to a 7000 system, but does not cause immediate end.

Read Data Timing

Read data cycle timing is illustrated in Figure 88; examination of the format track shows that it is a record address area. The example timing chart is actually a portion of a TRO read operation; however, Figure 88 (line 3) can be made to illustrate record area read timing by substituting the record area for address area.

The read cycle starts when trailing edge long gap sets the address area trigger. The address area trigger output sets the hold phase trigger. Hold phase timing sets the check prep and info search triggers at B1 of D1. With the check prep trigger set, the format recognition circuits are prepared to continue with check area after the read data is transferred. Info search gates the data gap singleshot output when the data gap is sensed; this sets the read gate in the gap separating AGC from the main body of read data. Also at B1 of D1, the hold phase trigger is reset; the reset hold phase trigger stops the timing circuits at BS of D2. Timing remains suspended until the first bit-sync selects phase.

Info search and BS AND to set the lead control trigger, which prepares the 7631 for read data transfers. Lead control and BS AND to reset the serial register. When the data gap sensor times out in the gap, the read gate is set, and reading starts. Receipt of the first read bit-sync selects a phase. The resultant bit timing is used to gate each read data bit from data trigger A to data trigger B, and from data trigger B to both the serial and shift registers. While reading the first character, B0 resets the info search trigger. Because the read gate is set, info search is no longer required.

The lead holdover trigger must be set at B6 for each character read because lead holdover controls both the I-O register reset (B7), and the serial register transfer to the I-O register (BS1/2A time) (Figure 88, lines 10 through 16).

Summarizing:

1. The serial register is reset
2. The first character is assembled in the serial register
3. The I-O register is reset
4. At the start of the second read digit cycle the first character is transferred from the serial register to the I-O register.

The lag control trigger is set at the start of the second read digit cycle because the first character is in the I-O register with parity assigned. Since the lag control trigger permits generation of data strobes or service requests for each read digit cycle (with the lag control trigger set) either a data strobe or service request is issued to the attached system to indicate a character is in the I-O register.

Receipt of the second read data bit-sync starts the second character read cycle. Again, the read data bits are transferred to data trigger A and then to data trigger B; data trigger B output is applied to both the serial register and the shift register. The read data cycle is repetitious and should continue without interruption until the missing sync circuits detect the missing sync gap that separates the last data character from the main body of the read data. Missing sync is used to condition the three zeros triggers; the three zeros signal "check area" after the last read data character is read. Because of the missing sync, the timing remains suspended at BS of D7 until the next read data bit-sync restarts the circuits.

Receipt of the last read data bit-sync restarts the timing circuits; the last character is assembled in the serial register and shifted into the shift register. Again, B7 resets the I-O register; with BS1/2A the last character is transferred from the serial register to the I-O register. When the three zeros triggers signal the check area, the lead control trigger is reset to start the turn-off of the data transfer circuits and the digit ring is reset to start check area timing. Reading continues, the check characters are read and processed. Check area sets the readout gate; the contents of the shift register are read out to the compare circuit. Bit by bit the generated check characters are compared with the check characters read from the data track. At BS1/2A (while reading the first check character), the last read data character is transferred from the serial register to the I-O register; in addition, the 7631 issues the last service request or data strobe to the controlling system. When the digit timing is advanced to D1, the hold phase trigger is set. Hold phase prevents the binary trigger from being flipped at B4 (while reading the last character) to continue hold phase check area timing after the last check character has been read.

When the digit ring is stepped to D2, the readout gate is reset to stop check character readout. In addition, the read gate is reset at BS of D2; this stops reading. At B1 of D6 the hold phase trigger is reset, causing the check area timing to end at the next BS time. The check area trigger is reset at B5 of D6 to end check area operation. (Figure 89 shows the read data cycle, address and record areas, in flow chart form.)

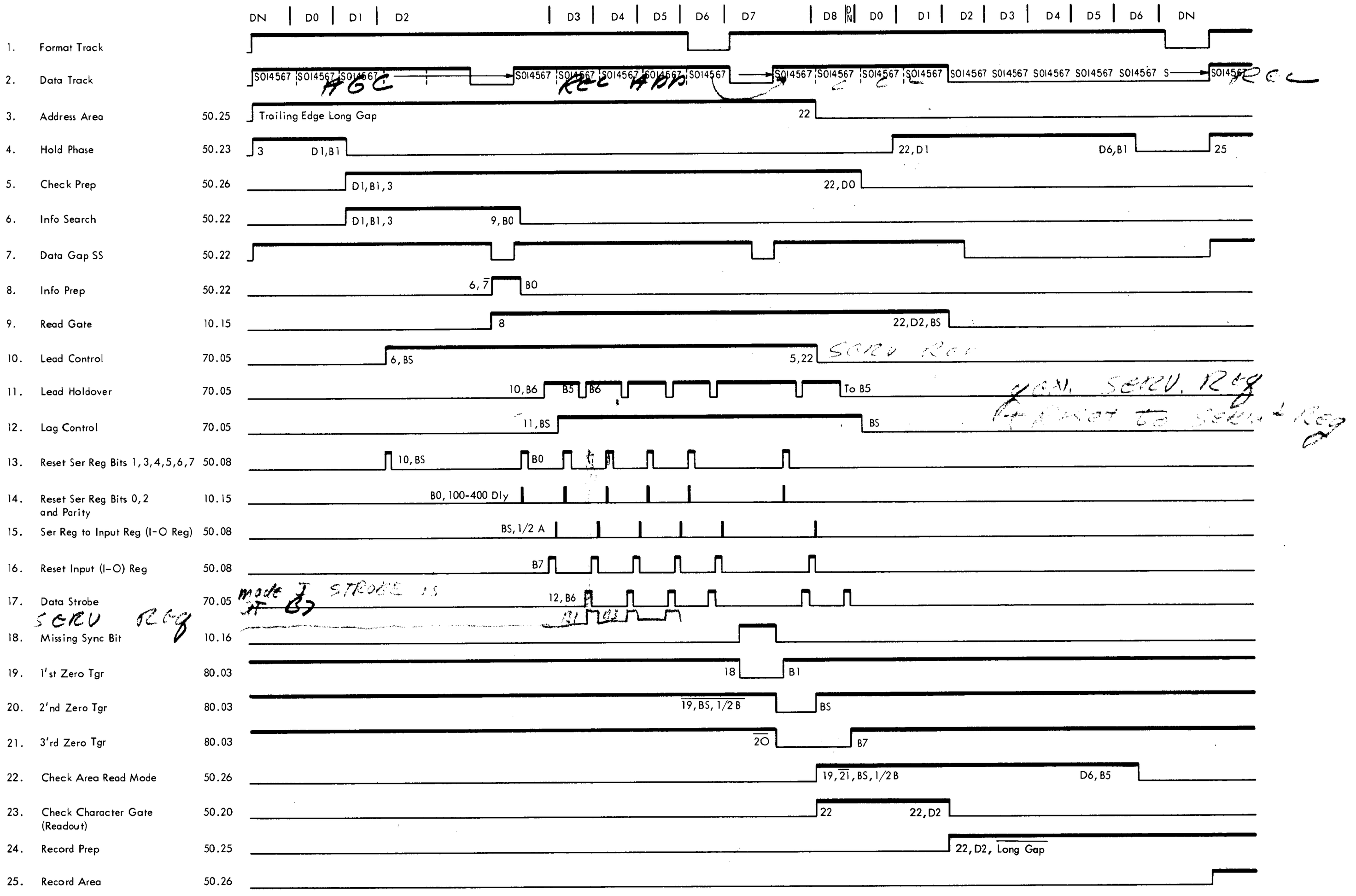


Figure 88. Read Data Cycle Timing

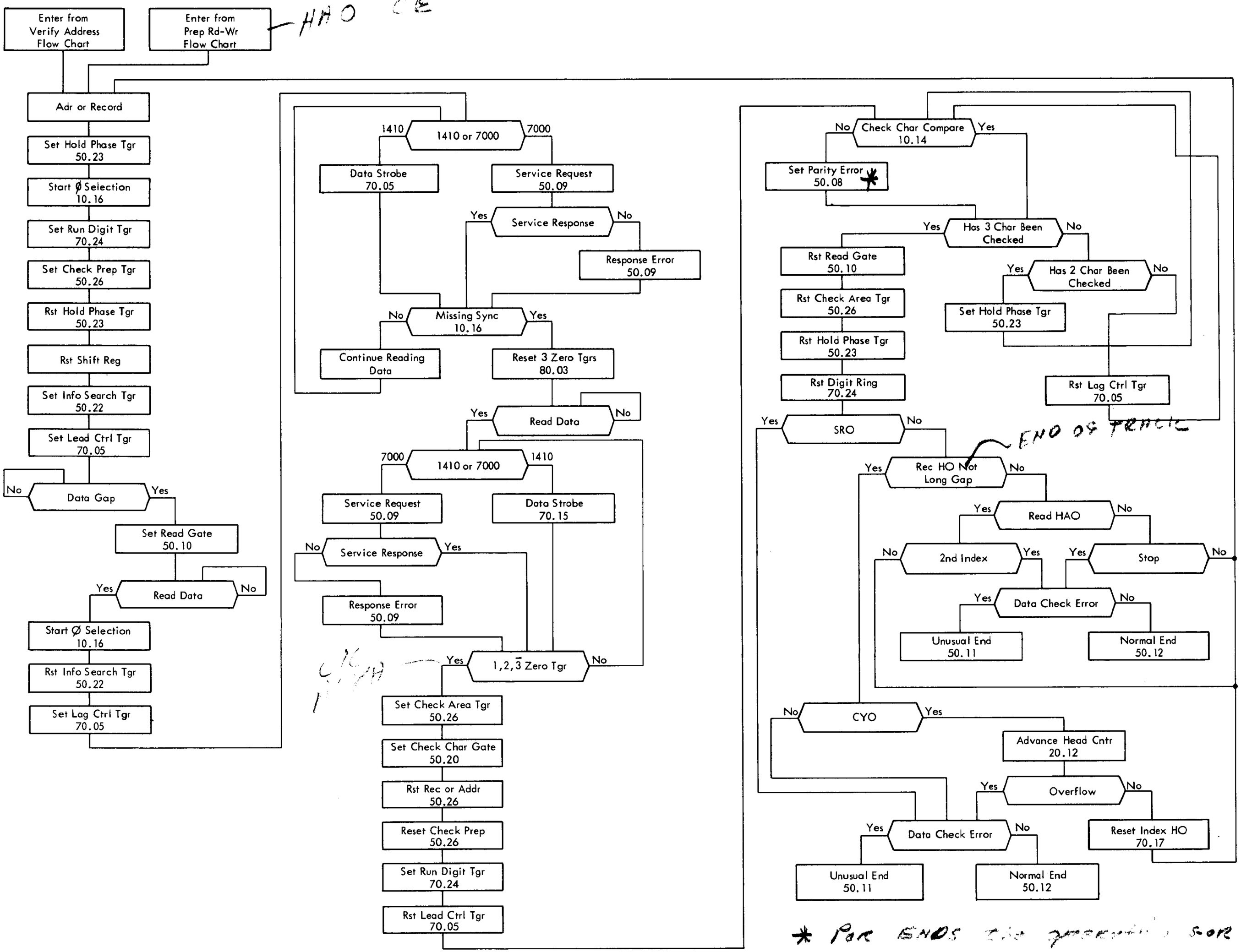


Figure 89. Read Data Cycle Flow Chart

Write Data Cycle

- **Initiated after a compare true is set.**
- **Locate write data area and control bit and digit rings to operate in write mode.**
- **Write AGC and test shift register for proper operation.**
- **Request write data characters and write serially by bit on 1301.**
- **Locate check area and gate shift register to 1301 write circuits.**
- **End operation if system has sent stop.**

Write data cycle circuit operation can be divided into three parts:

1. Format recognition
2. Timing
3. Data transfer

The operation of the recognition circuits, the timing circuits, and the data transfer circuits are so closely related that their operation cannot be presented individually. It is easier to understand these circuits if the objectives of a write data cycle are reviewed:

1. If no record found occurs during the verify address cycle, the 7631 terminates verify address cycle.

2. A write data cycle cannot occur unless the verify address cycle is completed and the compare true trigger is set.

3. Depending on the prepare to verify operation, the write data transfer circuits remain inoperative until the recognition circuits signal address or record area.

4. Address or record area sets the hold phase trigger; hold phase provides timing for the entire write data area.

5. The file control must write five AGC characters.

6. While writing the five AGC characters, some of the AGC data is entered into the shift register for the shift register test.

7. After the five AGC characters are written, the file control writes the gap to separate AGC data from the write data.

8. The shift register operation is tested while writing the gap following AGC.

9. If the shift register test is successful (contains the correct bit configuration) it indicates the shift register generates correct check characters; either a data strobe or service request is issued.

10. The first write data character transferred from the system is loaded into the I-O register while writing the gap.

11. After the gap is written the first write data character is transferred from the I-O register into the serial register.

12. The character is transferred from the serial register bit by bit to both the data track, where it is written, and to the shift register, where check characters are generated. Data writing continues until the format recognition circuits signal check area.

13. When check area is located, a one-character gap is written without a bit-sync (the missing sync gap) and then the last write data character is recorded.

14. After the last write data character is written the contents of the shift register are written on the disk.

15. If a stop or disconnect is issued by the system when writing, the request circuit operation stops; however, the file control writes blanks for the remaining characters.

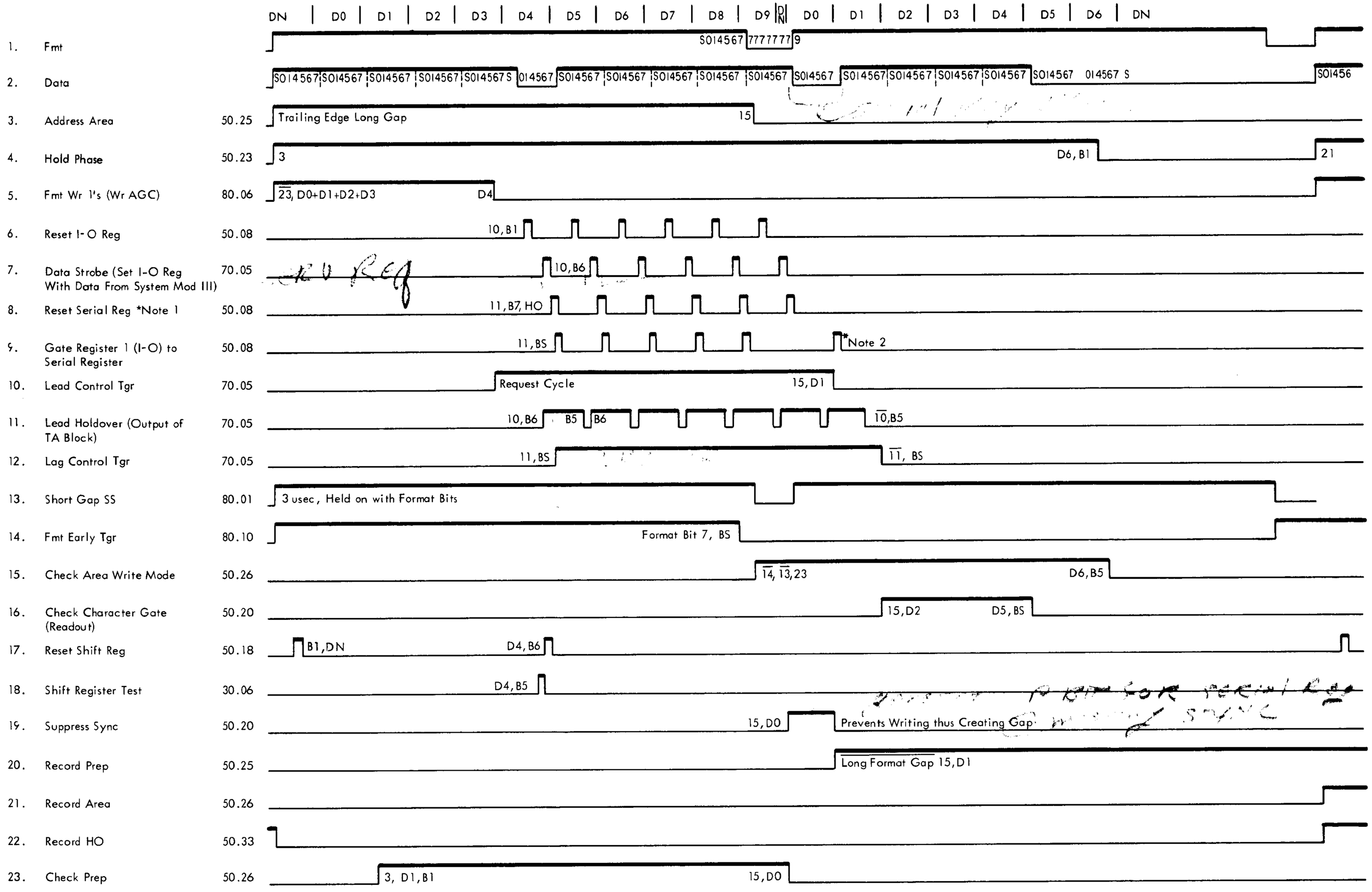
Write Data Timing

Write data cycle timing is shown in Figure 90; examination of the format track shows the write data cycle timing is for address area. Because the write data cycle timing remains the same for address or record area, Figure 90 can also be used for write record data timing, if the record area is substituted for address area.

When the trailing edge long gap sets the address area trigger, address area is used to set the hold phase and run digit triggers. Hold phase remains throughout the write operation. As a result, one of the four phase signals is selected and used until the write operation is completed. As the first step in writing, five AGC characters are written. Not check prep, D0 + D1, and D2 + D3 are used to set the format write one's trigger for five write data cycles. The output of the format write one's trigger is used to write five AGC characters. At D4 the format write one's trigger is reset to stop AGC writing.

Twenty-eight of the AGC bits are entered into the shift register for the shift register test; then two zero-bits are entered while writing the gap that separates AGC from the main body of address or record data. To insure that 28 AGC one-bits are entered prior to the test, the shift register reset is adjusted to agree with the machine bit mode. For example, in six-bit mode the shift register is reset at B1 of DN, and in eight-mode the shift register is reset at B3 of D0; this insures that 28 bits are entered before the test.

The file control writes a bit-sync followed by all



*Note 1: B0 and B2 not reset if I-O register contains B0 or B2 10.04.1

*Note 2: B0 + B2 positions set at B7 HO 10.04.1

Figure 90. Write Data Cycle Timing

zero bits to create the gap that separates AGC from the write data; while writing the gap the lead control trigger is set. In addition to writing the gap, the input register is reset at B1 and the first service request is issued. At B5 the shift register is tested. If the shift register test is unsuccessful, a file adapter (FA) circuit check occurs. File adapter circuit check activates the immediate stop error read-write-control line (ALD 90.33). Immediate stop error read-write-control sets the unusual end trigger; unusual end issues "end op" to a 1410 or "unusual end" to a 7000 system. If the shift register test is successful, B6 resets the shift register, issues a data strobe, sets the lead holdover trigger, and gates the first character from the write bus into the I-O register.

BS of D5 sets the lag control trigger; BS also gates the contents of the I-O register to the serial register to prepare for writing. With the first character in the serial register, each bit time pulse gates the corresponding bit (B0 gates data bit-zero) from the serial register to the 1301 write data bus and to the shift register. In review, lead control gates the I-O register reset, data strobes, and service requests; lead holdover gates the serial register reset, and the I-O register transfer to the serial register.

During each succeeding data character write cycle, a service request or data strobe is issued. The requested character is gated from the write bus to the I-O register at B6; the serial register reset at B7HO receives the contents of the I-O register at BS. After bit-sync is written, the succeeding bit timings gate data bits from the serial register to the 1301 write bus.

Writing continues until the format track short gap and not format early set write mode check area. Check area and B6 reset the digit ring; B7 steps the digit ring to D0. The suppress sync signal is generated at D0 of write mode check area; suppress sync prevents writing for one character. The suppressed writing creates a missing sync gap needed to find check area in read mode operation. The suppress sync signal is also used to suppress the data strobe or service request; it prevents losing a data character. In addition, suppress sync also inhibits the I-O register transfer to the serial register.

After the missing sync gap, the last data character is gated from the I-O register to the serial register, and the lead control trigger is reset. Writing continues until the last character is written from the serial register; while writing the last data character, the lead holdover trigger is reset. The readout gate gates the contents of the shift register to the 1301 write bus. After the check characters are written the readout gate is reset, but the file control continues and writes blank characters to the end of check area. B1 of D6 resets hold phase and B5 of D6 resets check area to complete the write data cycle. Figure 91 shows the write data cycle, for address and record areas, in flow chart form.

TRO Read and Write

- **After compare true, locate record address and record areas.**
- **Transfer data from/to system for every address and record area.**
- **End operation at end of an area when system sends stop.**
- **End operation at end of track if system has not sent stop.**

Track read and write operations are started when the read or write trigger is set, following a successful control cycle. The read or write trigger output starts these circuit sequences:

1. Prep read-write cycle
2. AGC squelch conditions
3. Verify address cycle
4. Read or write cycle

The first sequence, the prep read-write cycle, starts when the read or write trigger output sets the prep read-write trigger. When the prep read-write cycle is completed, the ACU select, ready monitor, and read monitor triggers are set, and the prep read-write trigger resets.

The second circuit sequence, AGC squelch conditions, starts when prepare to verify and first index AND. Because the track operation verifies HA1 and HA2, the 1301 read amplifiers must be conditioned to HA1. To insure that the read amplifiers are properly conditioned, a squelch signal is generated by the file control and applied to the 1301 read amplifier during first index. The squelch condition is generated by a

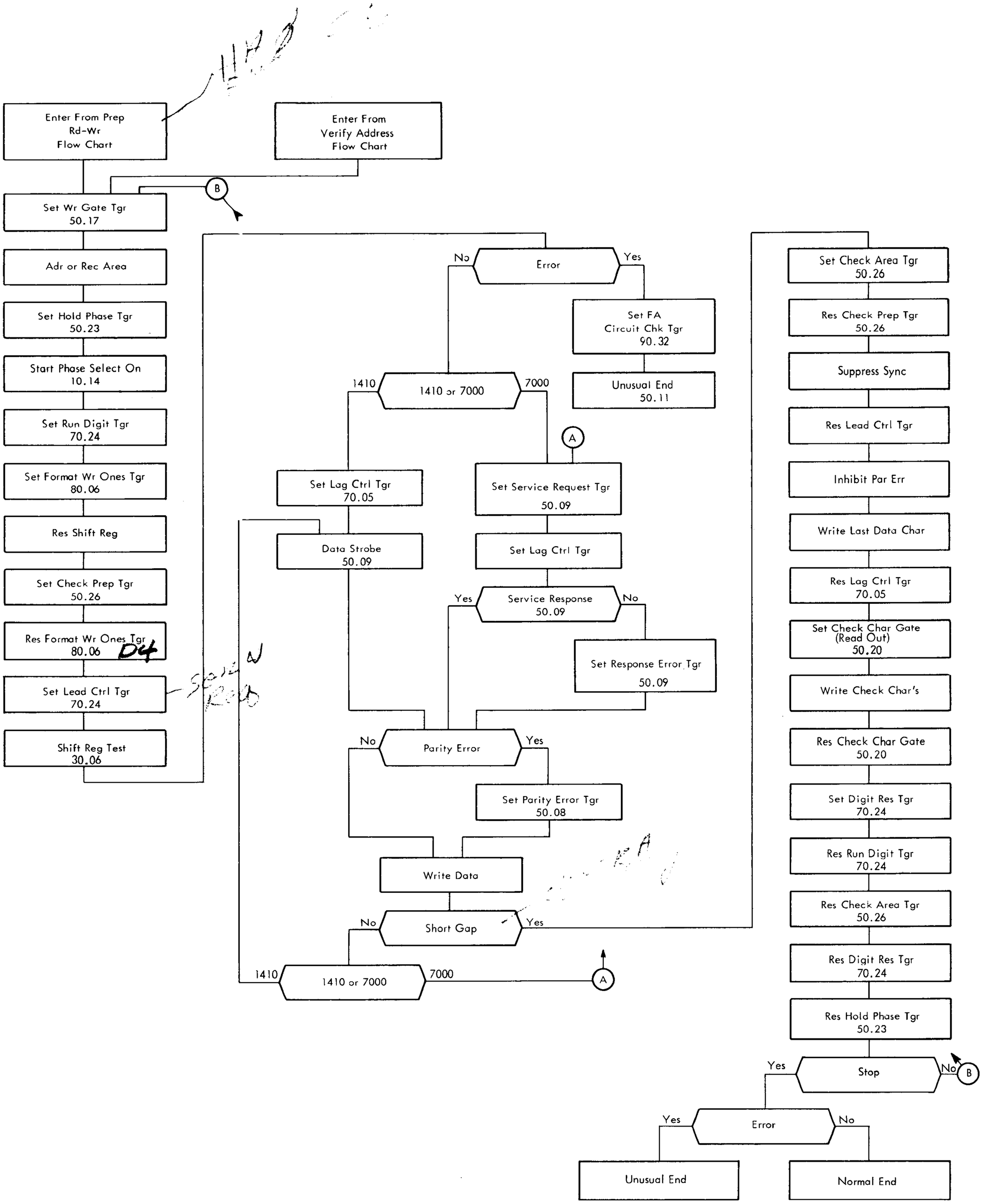


Figure 91. Write Data Cycle Flow Chart

350 microsecond singleshot output (Figure 92, line 2). First index and prepare to verify AND to fire the AGC squelch singleshot. The detailed timing from the prep read-write cycle to the AGC squelch conditions are shown in Figure 94, lines 2 through 7. The squelch signal is used to raise the 1301 read amplifier gain to the maximum. The previously recorded AGC data, between early and late index, restores the amplifier gain to the level required to accurately read the home address area 1. After the AGC squelch singleshot times out, the next late index gated with first index sets the index holdover trigger and resets the index trigger and first index.

When trailing edge long gap sets the address area trigger, the verify address cycle starts. (Figure 92, line 3. Details of the verify address cycle are shown in Figures 85, 86, and 87.) Immediately after HA2 check characters are compared, the compare true trigger is set if the compare fail trigger is off. Compare true is required to continue with a read or a write data cycle. If the compare fail trigger is not off, no record found is generated immediately after the check characters (HA2) are compared. No record found causes an immediate stop. Immediate stop sets the unusual end trigger; the file control issues end op to a 1410 or unusual end to a 7000 system.

When the compare fail trigger is off, the compare true trigger is set immediately following the HA2 check character comparison: compare true and the next B1 set the write gate, if the TRO trigger is set. The write gate normally remains on until end of track causes a machine idle reset: machine idle resets the write gate trigger. The write gate (set after the verify address cycle and reset at the end of track) permits the file control TRO operation to write addresses and records.

For TRO read, compared true conditions the read gate to set for each address and record until end of track stops the file operation.

Because the first area read or written for TRO is an address, the detailed data cycle timing shown in Figure 88 can be used as an example of detailed read data cycle timing. Similarly, the detailed write data cycle timing shown in Figure 90 can be used as an example of a track operation write data cycle timing.

Receipt of stop or disconnect causes the 7631 read or write data transfers to stop, but the 7631 completes the area. End occurs when not long gap, check area, B1, record holdover and D5 AND; the read-write done trigger is set. If one or more of the data characters contained incorrect parity, the parity error trigger is set. When the read-write done trigger is set, the file control indicates unusual end to a 7000 system or end op with a data error to a 1410 system. If the computer does not issue a stop or disconnect, end of last check area sets the read-write done trigger. End of last check area is generated when check area, B1, D5, address compare true, record holdover and not long gap AND; the read-write done trigger is set. Again, if no errors occurred while reading or writing, the file control issues normal end to a 7000 system or end op to a 1410 system without errors.

TWA Read and Write

- **After compare true, locate record areas.**
- **Transfer data from/to system for every record area.**
- **End operation at end of a record area when system sends stop.**
- **End operation at end of track if system has not sent stop.**

Track without address read and write operations are started when a read or write trigger is set following a successful control cycle. The read or write trigger output starts these circuit sequences:

1. Prep read-write cycle
2. AGC squelch conditions
3. Verify address cycle
4. Read or write cycle

The first sequence, the prep read-write cycle, starts when the read or write output sets the prep read-write trigger. When the prep read-write cycle is successfully completed, the cycle ends with an ACU select, ready monitor and read monitor triggers set, and the prep read-write trigger reset.

The second circuit sequence, AGC squelch conditions, results from a successfully completed prep read-write cycle. Because the TWA operation verifies HA1 and HA2, the 1301 read amplifier must be conditioned

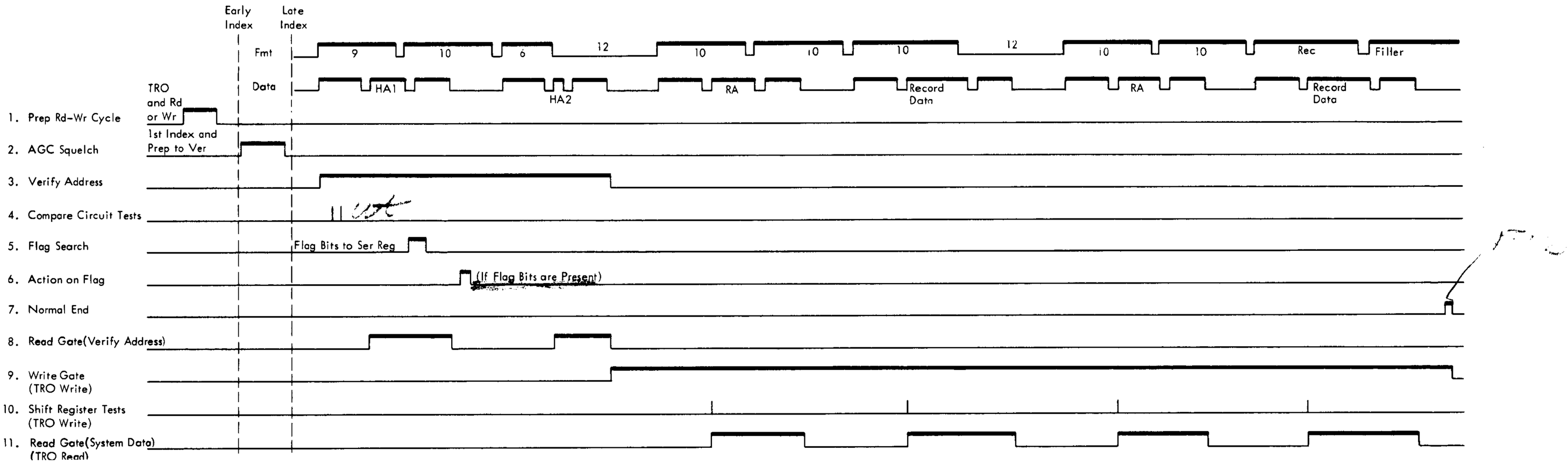


Figure 92. TRO Read and Write Sequence

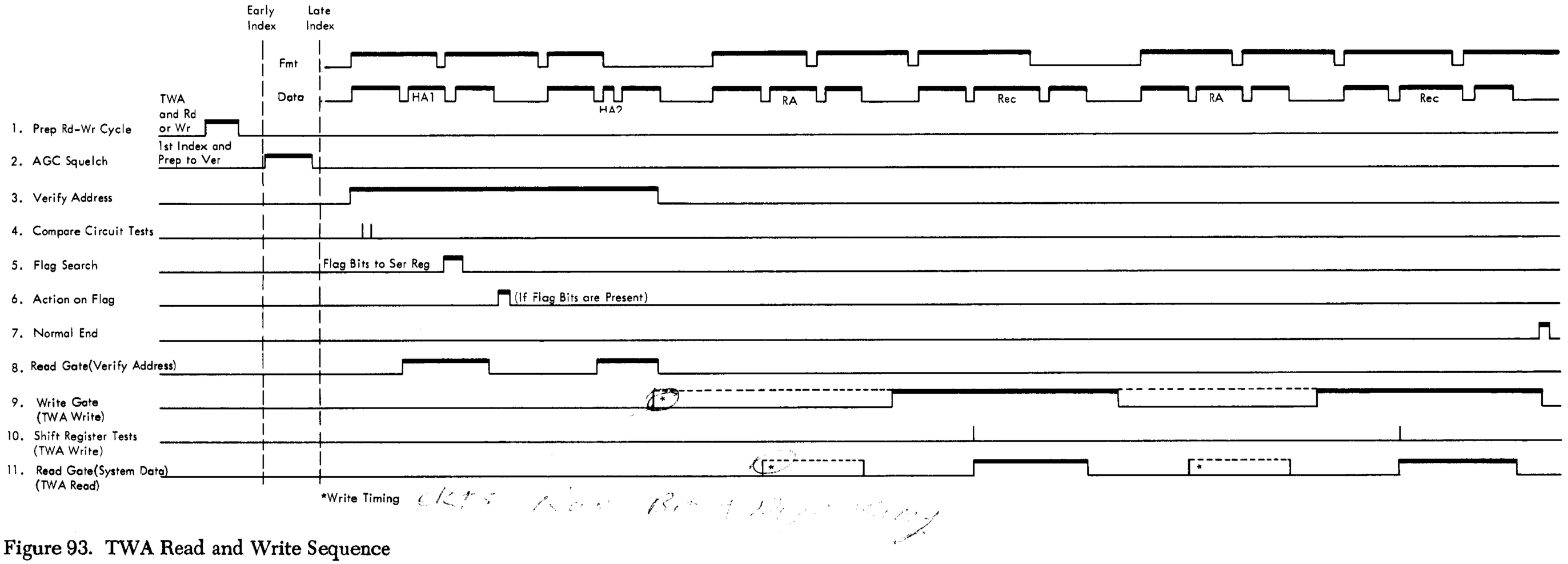


Figure 93. TWA Read and Write Sequence

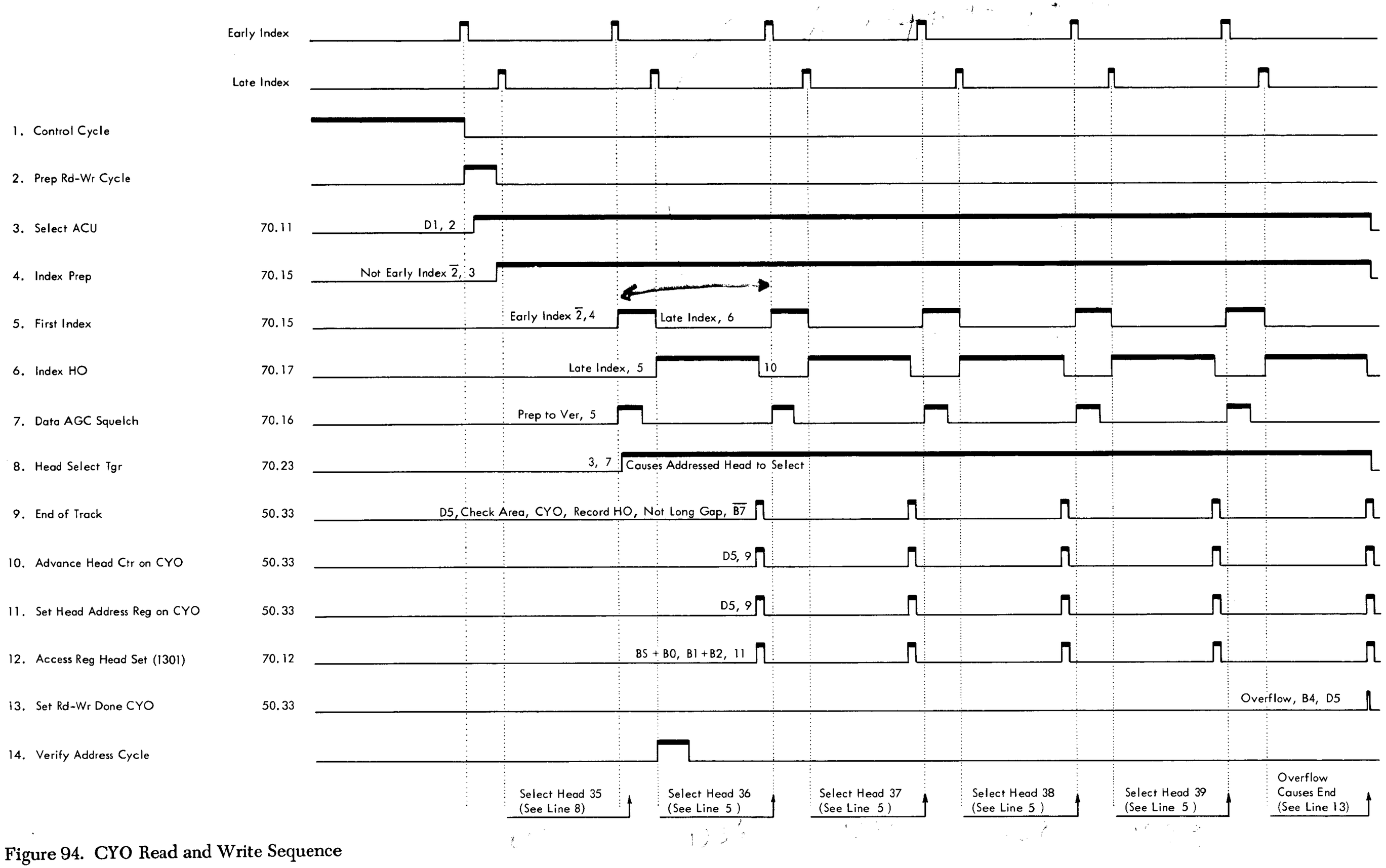


Figure 94. CYO Read and Write Sequence

and ready to read home address before late index. To insure that the read amplifiers are properly conditioned, the squelch signal is applied to the 1301 read amplifiers. The squelch condition is generated by 350 microsecond singleshot (Figure 93, line 2). First index and prepare to verify AND to fire the AGC squelch singleshot. The detailed timing from the prep read-write cycle to the generation of the AGC squelch is shown in Figure 94, lines 2 through 7. The squelch condition is used to raise the 1301 amplifier gain to maximum. Previously recorded AGC data (contained between early and late index) restore the amplifier gain to the level required to accurately read HA1. After the AGC squelch singleshot times out, the next late index gated with first index sets the index holdover trigger and resets the index trigger; first index drops.

When trailing edge long gap sets the address area trigger, the verify address cycle sequence starts (Figure 93, line 3). (Details of the verify address cycle are shown in Figures 85, 86, and 87.) Immediately after HA2 check characters are compared, if the compare fail trigger is off, the compare true trigger is set. Compare true is used to continue the TWA operation with a read or a write data cycle. If the compare fail trigger is set during the HA1 or HA2 comparison, the no record found trigger is set. No record found during a TWA operation causes immediate stop. Immediate stop sets the unusual end trigger; the 7631 issues end op to a 1410 system or unusual end to a 7000 system.

Because TWA operation does not process (read or write) record address areas, write mode is forced (for both TWA read and TWA write) to keep the format recognition circuit operation synchronized with the data track across each record address. Specifically, the record prep trigger must be set at D1 of the record address check area to permit the 7631 to recognize and process the following record area.

Since check area cannot be recognized without either read mode or write mode signals, it is essential to define a mode for each record address to recognize check area and ultimately set the record prep trigger. Briefly, write mode is forced during every record address area when the operation is TWA read or TWA write. Not home address area, not record holdover, TWA or CYO, and index holdover are AND'ed (ALD 50.32.1) to generate inhibit on CYO or TWA; inhibit on CYO or TWA is used to force write mode (ALD 50.17.1) during record address areas. (See "Functional Units, Write Mode Format Recognition" for details of write mode format recognition circuit operation.)

When the recognition circuits signal record area, inhibit on TWA drops, and the read or write data cycle starts. Record reading or writing continues for each record area until the system issues a stop or disconnect, or the file control, end of last check area, sets the normal end trigger.

CYO Read and Write

- **After compare true, locate record areas.**
- **Transfer data from/to system for every record area.**
- **At end of track, add one to track register to select next head in cylinder and continue to transfer record data.**
- **End operation at end of a record area when system sends stop.**
- **End operation at end of cylinder if system has not sent stop.**

CYO operation (optional feature) is used to read or write a maximum of 40 data tracks. Less than 40 tracks can be processed by specifying a starting head address greater than zero. A CYO operation permits a computer to read or write the record areas without reading or writing record address areas. The CYO operations can be divided into these sequences:

1. Prep read-write cycle
2. ACC squelch conditions
3. Verify address cycle
4. Read or write cycle
5. Cylinder head selection

CYO operation starts when the read or write trigger sets after a successful control cycle. The read or write trigger output sets the prep read-write trigger; a prep read-write cycle starts. In addition to the common prep read-write cycle function, the contents of T2 B2 latch trigger (ALD 20.07) are transferred, at D2 of the prep read-write cycle, to the head selection counter binary trigger T2 B2. Binary trigger T2 B2, the high-

order position of the head selection counter, must be set if the addressed head is any one of the heads numbered 20 through 39; the last carry pulse generated at the end of track 39 causes T2 B2 overflow to end the CYO operation.

After a successful prep read-write cycle ends, select ACU not prep read-write, and not early index set the index prep trigger (Figure 94, line 4). The first early index, with index prep set, gates first index. Prepare to verify and first index gate AGC squelch conditions. Select ACU and AGC squelch conditions AND, and the head select trigger sets. Head select causes the 1301 to select the head specified by the 7631 track register.

Late index and first index set index holdover; index holdover resets first index. Index holdover starts the format recognition circuits; HA1 and HA2 are verified. (Refer to Figure 85 for details of the verify address cycle timing.) If the verify address cycle is unsuccessful, no record found sets unusual end. Unusual end or end op is issued to complete CYO operation. If the verify address cycle is successful, the compare true trigger is set. The compare true trigger remains set until the last track has been read. Because the verify address cycle cannot occur with the compare true trigger set, compare true permits only one verify address cycle; the first track used is verified.

The read or write data cycle occurs after a successful home address comparison. The read or write data cycle operation for CYO operation is identical to a TWA operation.

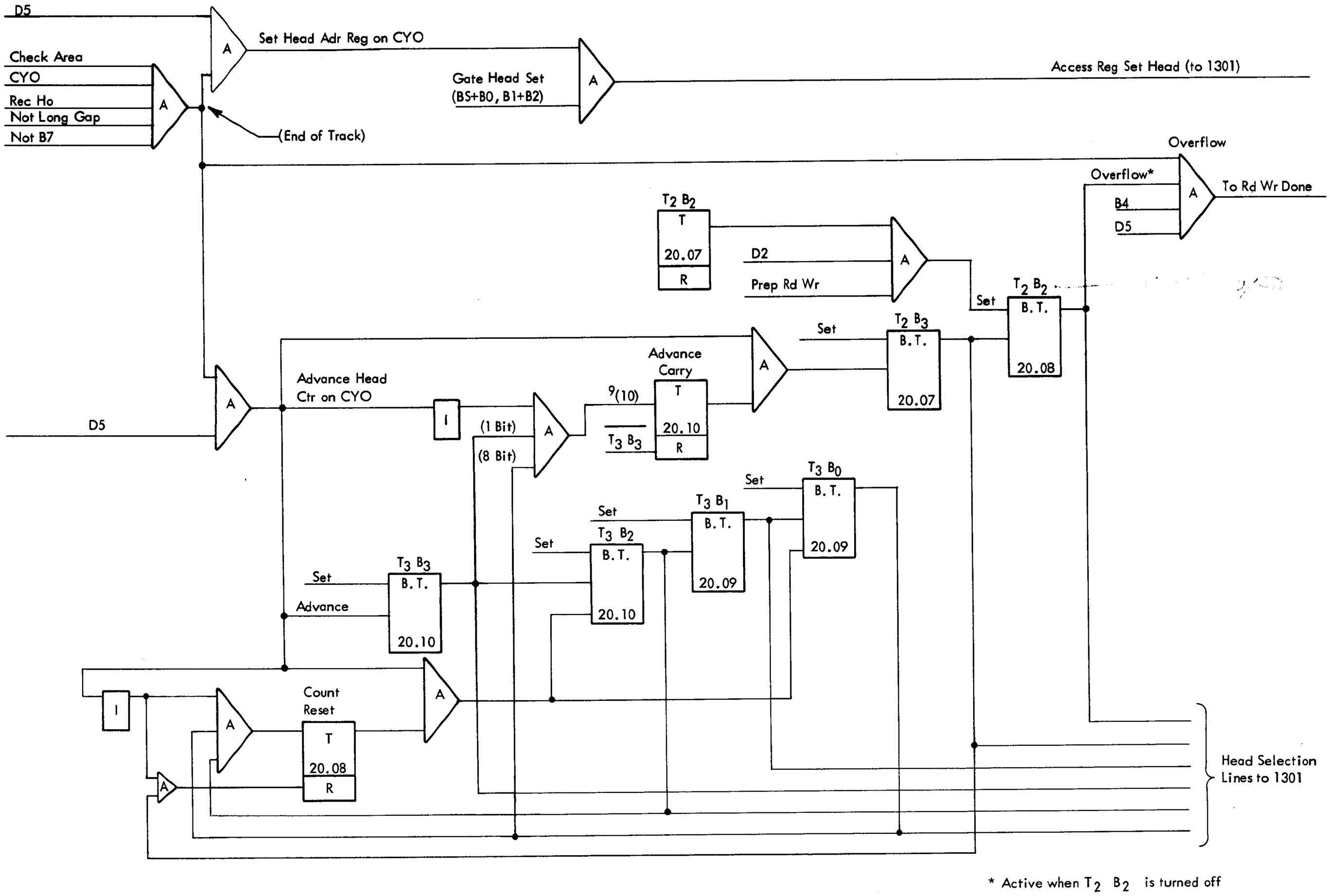
A new cylinder head selection must be effected at the end of each track to continue CYO operation. Compare true, check area, CYO, record holdover, not long gap, not B7, and D5 advance the head counter; a new head selects for the next disc revolution. At D5, the end of track condition steps the cylinder head selection counter (Figure 95). End of track is also used to generate set head address register on CYO. Set head address register on CYO is gated with bit timing (Figure 95) to produce access register set head pulse for the 1301. Access register set head gates the new head selection bits into the 1301 head register. With each new head selected, the index holdover trigger is reset. (Figure 94, line 6). AGC squelch is repeated in the index area prior to each track. The verify address cycle does not repeat after the first track address is verified. CYO operation continues until head 39 has been selected. (A head select sequence is shown below line 14 in Figure 94). When head 39 is selected, the last track is read or written. When end of last check area occurs for track 39, the carry pulse causes the head selection counter to overflow at count 40. Overflow, B4 + B5, and end of last check area set the read-write done trigger to end CYO operation.

SRO Read and Write

- **Compare record addresses with track and random record registers.**
- **If not compare true, no record found is indicated at second index.**
- **If a compare true, locate the following record area.**
- **Transfer data from/to the system for the record which compared true.**
- **End operation at the end of the record.**

SRO operation permits random access to a specified record located anywhere on the selected track. SRO operation permits the 7631 to locate and compare each record address with the contents of the 7631 track, and random record registers. When the compare true trigger is set, the following record information is read or written to complete the SRO operation. Because SRO is not started with index, the 7631 generates 350 microsecond AGC squelch plus a 200 microsecond delay to condition the 1301 read amplifier prior to starting the verify address cycle. (Figure 96). Because the SRO record address is stored in the 7631 track and random record registers, the set-access unit-head register pulse (normally issued during a control operation) is inhibited for SRO control operations, and the previous head address transferred to the 1301 remains unchanged. If set access unit head register were issued to the 1301, a portion of the record address would be transferred as head selection bits; this would cause a no record found error. Because six-track and random record register address characters are stored in the 7631, the track's record addresses must contain at least six characters.

Receipt of SRO, followed by read or write, sets the



* Active when T_2 B_2 is turned off

Figure 95. CYO Head Selection Simplified

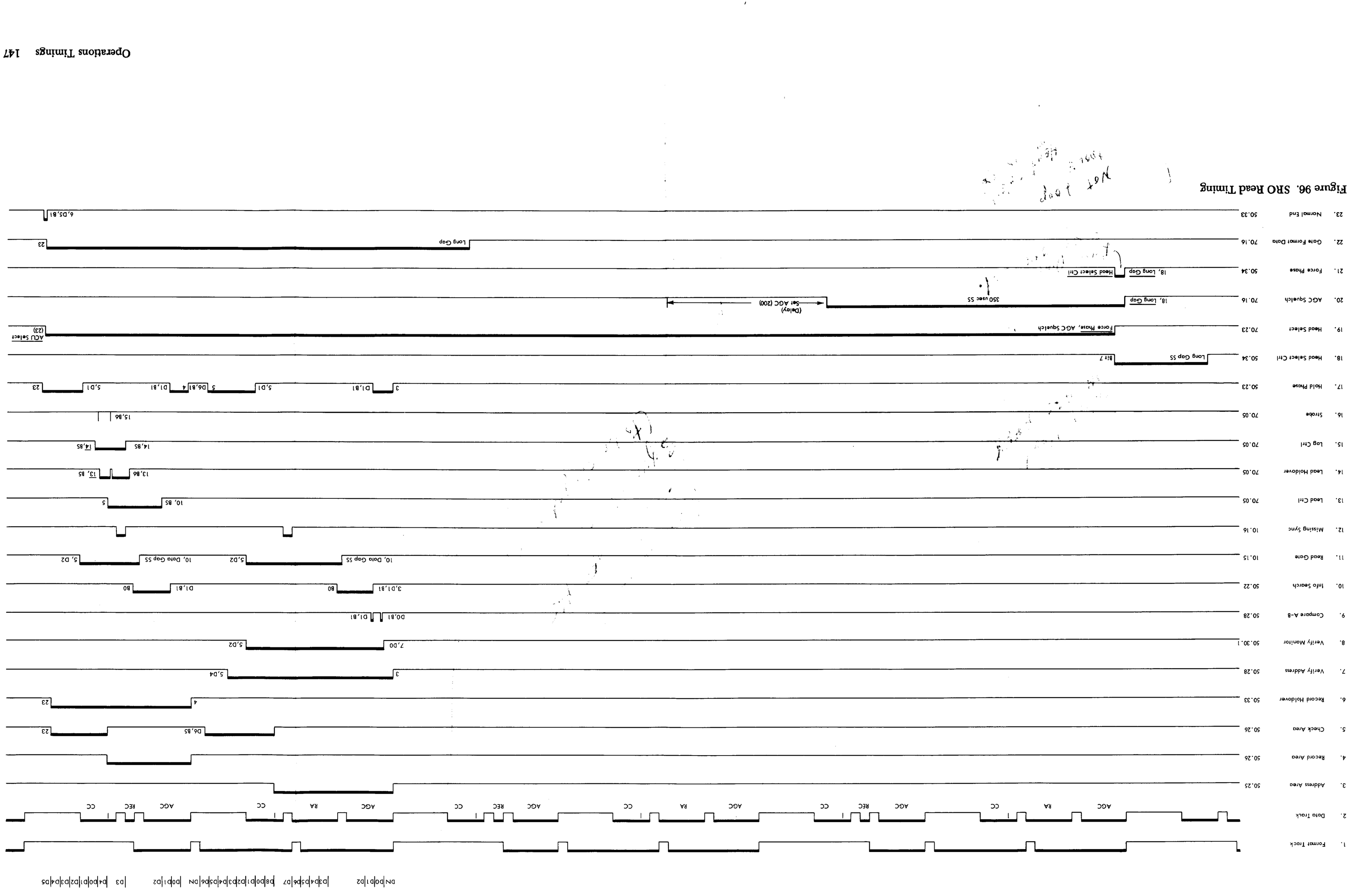


Figure 96. SRO Read Timing

prep read-write trigger. After a successful prep read-write cycle, select ACU, not prep read-write, long gap, SRO, not control, and not head select AND; the head select control trigger sets (Figure 96, line 18). Not long gap and head select control fire the AGC squelch singleshot. Head select control and not long gap generate force phase. Force phase timing (B7) resets the head select control trigger and as a result, force phase drops. Not force phase and AGC squelch conditions set the head select trigger. The head is selected in an AGC area; this insures that the head does not select over data and erase a data bit.

After AGC squelch, the next long gap trailing edge sets the address area trigger. The verify address trigger is set with address area. A verify address cycle is started; test not compare A and B occur during hold phase. If the compare circuit test fails, as in any other verify address cycle, a file adapter circuit check causes immediate end. If the address compares, the read or write data cycle starts. SRO ends when B1, D5, check area, compare true, and SRO set the read-write done trigger.

If the address does not compare, the next record address is verified. If second index occurs, no record found ends the operation.

If the SRO operation is not completed at first index, index or idle reset is generated. Index or idle reset resets the following triggers: digit reset, read gate, record, check, info search, check prep, verify address, address, record prep, and verify monitor. After late index the file control reads HA1. HA1 is read because the track may be flagged. If the track is flagged, action on the flag results. The SRO operation is transferred to the alternate track if action on the flag occurs and continues to verify addresses to complete the SRO.

HAO Write

The HAO operation is the most versatile disc instruction. Its main CE use is to write HA1 on new files or to flag defective tracks. For customer operation, it permits writing HA2 and the record address and record areas following. The positions of two switches used with the HAO operation, the HAO customer switch and the HAO-CE switch, determine what happens during an HAO write. The following text is divided to present each type of HAO operation separately.

Write Home Address One On New Files (HAO-CE Write)

- **Allows CE to write HA1, HA2, record address and record areas.**
- **Two switches are used and must be on: HAO switch on operator's panel, HAO-CE switch on CE panel.**
- **If system sends stop, write blanks in the remaining areas.**
- **Write filler from end of track to index.**
- **If a flag character is written, write filler the remainder of the track.**
- **CE has ability to write on normal data track or alternate surface.**

Home Address area one can be written on new files in this sequence:

1. Set the HAO customer switch on
2. Set the HAO-CE switch on
3. Seek to the desired cylinder
4. Issue the HAO order
5. Issue the write command

Briefly the sequence described causes the following circuit operations:

1. The first step is to seek to the desired cylinder.

2. Issue the HAO order. The track address issued to the file control during the HAO control cycle must contain the correct track and head address. (The random record register R0 must contain a blank or an eight because these characters do not have a BCD four, two, or one bit (flag bits). Any character with a BCD four, two, or one bit stored in the R0 in an HAO operation would cause the HAO write operation to select an alternate track, instead of the track specified by the head selection portion of the track register. The contents of

random record register R1 can be any valid character.

3. The HAO customer switch, as indicated in the previous sequence, must be on before issuing the HAO control order. If the HAO switch is not on during the HAO control operation, the 7631 indicates not ready.

4. Following a successful HAO control operation, the write command is issued.

5. The write command and the HAO-CE switch set the compare true trigger.

Receipt of the write command starts a prep read-write cycle. In addition to the common prep read-write cycle functions, transfer on flag is generated at D3 if the HAO-CE switch is on. Transfer on flag reads out the contents of random record register R0 to the serial register. If flag bits are in the serial register, set head on HAO is generated. This transfers the flag bits from the serial register to the 1301 flag register; however, to simplify the operation assume this is an HAO-CE write without flag bits in the serial register (Figure 97).

After a successfully completed prep read-write cycle, prepare to verify and first index set the head select trigger. The head select trigger output causes the 1301 to use the contents of its head register to select the head. (The head select bits transferred during the control-HAO cycle.) The head is selected when prepare to verify and first index AND. First index sets the hold phase and the format write one's triggers. The first hold phase B0 sets the write monitor and the next B1 sets the write gate. With write mode established, the output of the format write one's trigger is used to write all one bits (filler) until late index sets index holdover; index holdover resets first index.

Before the format write one's trigger resets when first index is reset, home address, long gap, not check area and HAO-CE write set the format write one's trigger (Figure 97). When format recognition circuits recognize address area (home address area one) the set is removed from the format write one's trigger. However, the circuits normally used to write AGC prior to any record or address area set the format write one's trigger. Not check prep, D0 + D1 and D2 + D3 write five AGC characters.

Summarizing the HAO-CE write operation, all one-bit characters are written from first index to D4 of home address area one (Figure 98, line 2). Another important consideration is that the HAO-CE switch (on prior to the HAO control cycle) sets the compare true trigger (Figure 97). The compare true trigger bypasses the verify address cycle and permits HAI writing; also, HAO-CE write gate is set at first index and resets at D6 of second index.

Write timing for each formatted area follows the write data cycle sequence shown in Figure 90. HAO-CE write for each area is shown in Figure 98. Write data characters enter the I-O register from the system write bus. The characters transferred to the serial register are parity-checked, written on the track, and entered into the shift register. After the fifth character (the flag character) is written, the serial register reset is inhibited. The character remains in the serial register until after the check characters are written on the track. At D5 of check area the serial register contents are examined to determine if flag bits are present. Briefly, this first HAO-CE write operation assumes the flag character was a blank or an eight.

Following check character writing, the write gate remains on and blanks are written during D5 and D6 of check area. Similar to any other check area writing, hold phase is reset at B1 of B6 to end the check area timing.

After home address area one is written, the format recognition circuits continue operation to permit home address area two, record addresses, and record data writing.

If the computer is not going to write data after HAI, stop or disconnect is issued. The stop or disconnect signal resets the file control data request circuits, but does not end the HAO-CE write operation; the file control continues to write each area. AGC, gaps, and blanks for data are written to define the remaining address and record areas. The write data cycles continue until end of last check area. End of last check area sets the filler trigger; the format write one's trigger is set (Figure 98, line 4) to write filler until the read-write done trigger is set at D6 of second index. At D6 of second index normal end or end op is issued. Machine idle reset stops the write operation.

Write Home Address One and Flag on a Damaged Track

HAO-CE write can be used to flag a damaged track. To flag a track, a write sequence identical to write home address one on new files is repeated. (Review "Write Home Address one on New Files" up to the point where the first four characters of the main body of home address one are written.) After writing the gap that separates the main body of home address area one from the last character, the flag character is written and the serial register reset is inhibited (Figure 98 shows that the flag character is written at D1 of check area). The contents of the shift register are then read out and written on the disk to complete the home address area one writing. The write gate remains on following the last check character to create a one-character gap at D5. While writing the one character gap, flag bits present, not record holdover, check area, HAO-CE and D5 set the filler trigger. The filler trigger output and B5 set the format write one's trigger; the write circuits write filler (Figure 98, line 4) until D6

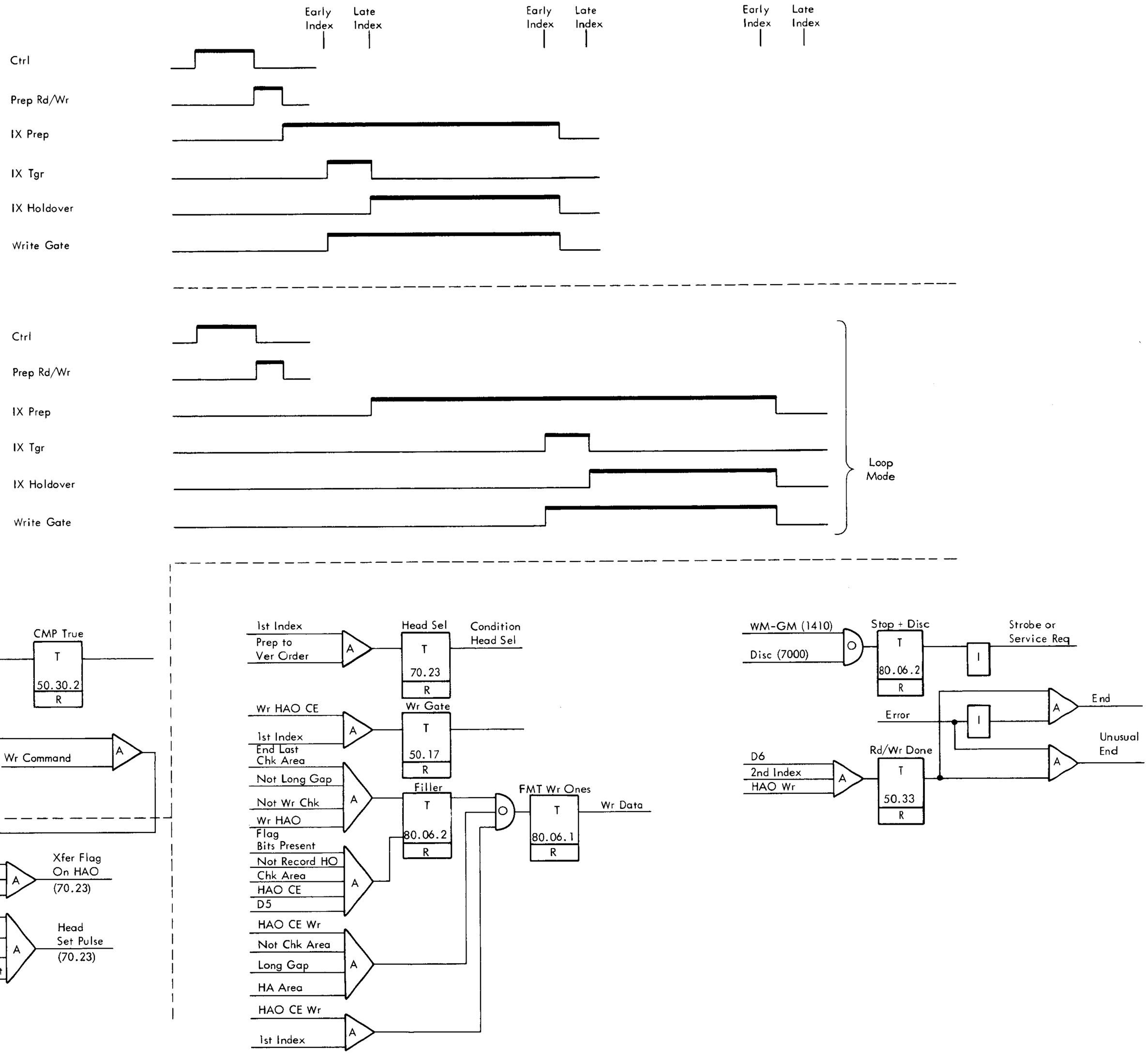


Figure 97. HAO-CE Write Sequence and Simplified Logic

of second index sets the read-write done trigger.

Except for home address area one the entire track is filled with all one-bits characters. Filler is needed to bias the 1301 read amplifier for subsequent SRO operations on the flagged track. For example, after the squelch period, SRO format gating starts. Not compare true results when filler is read, and the file control continues searching for the comparing record address until home address one is read. When home address one is read, the flag character is stored in the serial register. Following the check character comparison, D3, check area, home address area, not record holdover, not format, and not HAO-CE AND, resulting in action on the flag. (Review Figure 86.) Action on the flag gates the serial register flag bits to the 1301 flag register, and set ACU head register to the 1301. Action on the flag causes the SRO operation to continue on the alternate track. (If a parity error occurred when home address area check characters are compared, the parity error trigger is set and remains set. The SRO operation is completed with a parity error indicated.

Write Home Address One on an Alternate Track (HAO-CE Write)

The procedure to write HA1 on an alternate track after a defective track has been flagged does not involve any new principles of HAO operation. Assume track 5555 is defective and has been flagged with a two. It is necessary to write the normal home address 1, 5555, on the alternate track surface.

To write HA1 on the alternate track the HAO-CE control cycle must be executed. The HAO control word must contain access, module, home address 1 (5555), and two random record characters. The contents of R0 must be a two. The two is stored in random record register position R0 and the last character can be any valid character. For example, the HAO control word character could be 555528. The write command is then issued to start the HAO-CE write operation. At D3 of the prep read-write cycle, the contents of random record register R0 are transferred to the serial register (Figure 82, circle 10). The serial register contains a BCD two-bit. At D4 of the prep read-write cycle, HAO-CE and the flag bit (the BCD two bit AND; the conditions gate set head on HAO. Set head on HAO, gated with BS + B0 and B1 + B2, issues access register set head to the 1301. The head set pulse on HAO is OR'ed to force action on the flag (ALD 01.50.35), and the flag bit (a bit-six) is gated to the 1301. The 1301 flag register is set, and the remaining action on the flag functions occur (Figure 86, lower right corner).

Because of action on the flag, the alternate disc surface is addressed with the contents of the 1301 flag register. First index is generated when the next early index sets the index trigger. First index and prepare to verify AND, and the head select trigger sets. Head select is issued to the 1301, which selects the head addressed with the 1301 flag register. The remainder of this HAO-CE write sequence is the same as that previously described in "Write Home Address on new Files."

Summarizing write home address one on an alternate track shows:

1. The HAO customer switch must be on.
2. The HAO-CE switch must be on.
3. The HAO control word must contain the track address of the damaged track.
4. Random record register R0 must contain a flag (the character required to address the alternate track).
5. Random record register R1 can contain any valid character because it has no effect on the operation.
6. The write command must be issued.
7. Transfer flag on HAO (Digit three of the prep read-write cycle, ALD 70.23) gates the contents of random record register R0 to the serial register.
8. Head set pulse on HAO (ALD 70.23) is generated at D4 of the prep read-write cycle. Set head pulse on HAO gates access register set head to the file frame and gates action on the flag. Access register set head and action on the flag gate the flag bits from the 7631 serial register into the 1301 flag register. Action on the flag also resets address compare true, index holdover, gap format, and record prep triggers (Figure 86).
9. The next early index sets the index trigger, and first index rises. First index and prepare to verify set the head select trigger. Head select is issued to the 1301; the contents of the 1301 flag register select the head.
10. The alternate track is selected. Starting with the first index the 7631 writes filler. The write sequence to "Write Home Address 1 On New Files" is repeated.

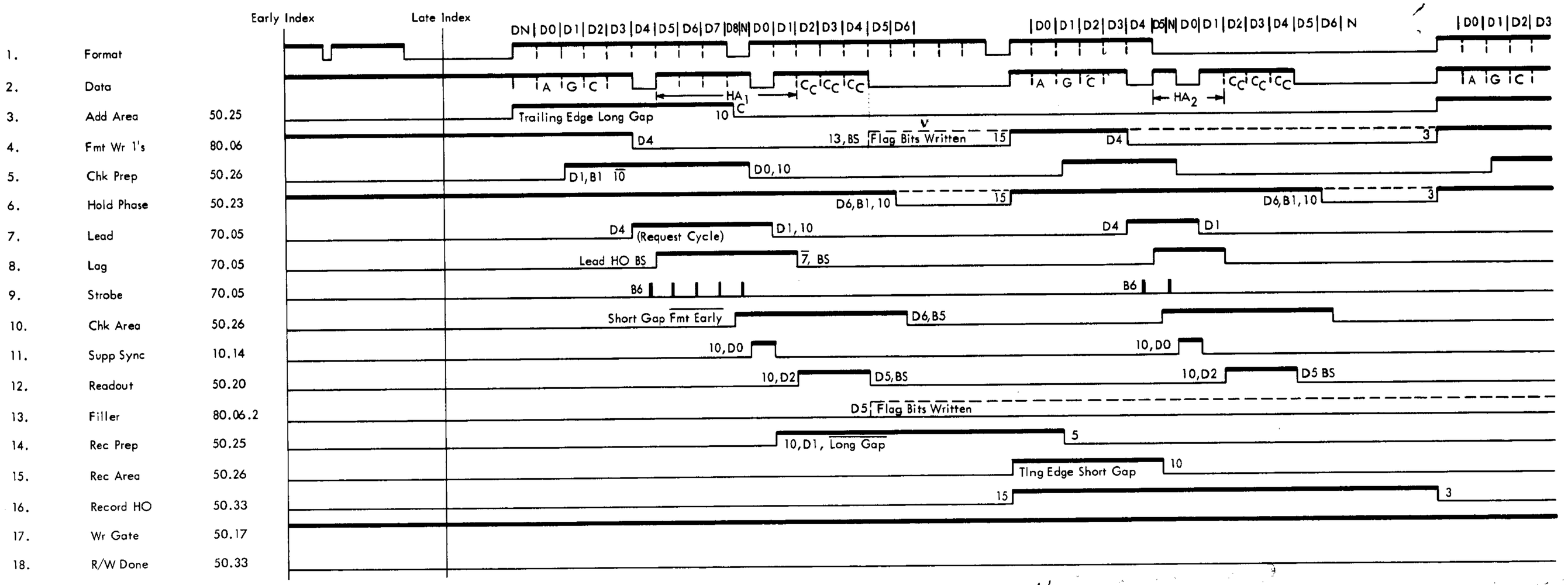


Figure 98. HAO-CE Write Timing

HAO Customer Write (HAO-CE Switch Off)

- **Allows writing HA2, record address and record areas.**
- **HAO switch on operator's panel ON.**
- **If system sends stop, write blanks for remainder of track.**
- **Write filler from end of track to index.**

HAO customer operation permits the user to verify HA1 and begin writing with HA2. Similar to the previously described HAO operations, after writing starts it continues until D6 of second index. This permits the customer to write HA2, record addresses, and records to the end of last check area. Immediately after end of last check area, the filler trigger is set; the filler trigger sets the format write one's trigger. The 7631 writes filler from end of last check area until D6 of second index.

If stop or disconnect is issued before writing the complete track of record addresses and records, the data request circuits reset, but the HAO operation continues. The file control writes blanks for each formatted record address and record area until end of last check area. Again, at end of last check area, the filler trigger is set permitting the format write one's trigger to write filler from end of last check area until D6 of second index. The write timing detail for HA2, record addresses, record areas, and filler bit writing is shown in Figure 98.

Because the HAO-CE switch is off there are two major differences between HAO customer write and HAO-CE write. Transfer flag on HAO and head set pulse on HAO are not generated when the HAO-CE switch is off. Because transfer flag on HAO and head set pulse on HAO are not generated, the content of random record register R0 can contain any valid character, including those that contain flag bits without causing the alternate track to select. Another major difference between HAO customer write and HAO-CE write is the verify address cycle. The verify address cycle is different than a TRO, TWA, and CYO verify address cycle because only HA1 is compared. If HA1 compares correctly, the compare true trigger is set at BS of D2 in check area for HA1.

If the HAO customer write verified HA1 and flag bits were read, a flag operation occurs (Figure 86). The flag operation for HAO customer write is the same as the flag operation that might occur for TRO or TWA operations. The result of flag operation after the home address verify cycle causes the HAO customer operation to write on the alternate track.

HAO-CE Read

The HAO-CE read operation reads data from a track that does not have a format track or when the format track has been damaged. The HAO-CE read operation is designed to read without format track signals, starting with late index gated HA1, HA2, record addresses, and records are read.

In a similar manner, HAO-CE read can be used to read HA1, HA2, record addresses, and records from an alternate track.

Read Home Address One from a Customer Track

- **Allows CE to read HA1, HA2 record address and record data.**
- **Two switches are used and must be on: HAO switch on operator's panel, HAO-CE switch on CE panel.**
- **Format track is not used to define read data areas; therefore index is end of track.**
- **End operation at the end of an area if system sends stop.**
- **CE has ability to read a normal data track or alternate track.**

To execute HAO-CE read the following sequence is used.

1. HAO-CE switch on
2. HAO customer switch on
3. Seek to the desired cylinder
4. Execute the HAO control cycle
5. Issue the read command

Receipt of the read signal starts the read operation. Similar to HAO-CE write, the first cycle is the prep read-

write cycle. The common prep read-write cycles functions occur, and because the HAO-CE switch is on, the contents of random record register R0 are transferred to the serial register. Briefly, assume random record register R0 contains a blank or an eight to prevent action on the flag. This permits the HAO operation to read the track specified by the head selection bits transferred to the 1301 during the control HAO cycle.

AGC squelch conditions and head selection occur when a prepare to verify and first index AND. Late index gated starts the read operation. Late index gated sets the address area trigger, and address area sets the hold phase trigger. Hold phase timing is needed to set the check prep and info search triggers and to reset hold phase. Because the HAO-CE switch is on, compare true is forced when read AND's with HAO-CE. The read gate is set in the data gap to read HA1 and the following check characters. The compare true condition permits the lead control trigger to set in the data gap. When the lead control trigger is set, the data transfer circuits operate while reading HA1 (Figure 99). Read timing, with the exception of the address area trigger turn-on, is not different from any other read operation.

End of check area shows differences between HAO-CE read and other read operations. Figure 99, line 6, shows that record prep, read HAO and D6 must AND to set the record area trigger. Format signals are not available. As a result of this difference the hold phase trigger remains set after the check area reset because of the record area trigger output (Figure 99, line 10). B1 of D1 sets the info search and check prep triggers and resets the hold phase trigger, and another read cycle starts. The data gap singleshot output and info search set the read gate in the next AGC gap. Reading continues, and HA2 is transferred to the system. At the end of check area (Figure 99, line 6), record prep, read HAO, and D6 AND; the record area trigger is set.

The following record address is processed as a record area. The read and data transfer timing for the record address processed as a record area is not different than that of any other read data cycle. Line 7 shows that the record holdover trigger is set during HA2 when the record area trigger is set. Note that record holdover is not reset until the end of the HAO read operation. Address area is required to reset the record holdover trigger. Because format track signals are not used, trailing edge long gap is not available; therefore, address area cannot reset record holdover. HAO-CE processes the remaining record and address areas until second index and verify HAO AND; the read-write done trigger is set. Read-write done causes the 7631 to issue end op to a 1410 system or normal end to a 7000 system.

If stop or disconnect is issued before reading a complete track, the data transfer circuits reset, but the file control continues to read until D5 of the next check area. The HAO operation ends when D5 of check area sets the read-write done trigger.

Read Alternate Track (HAO-CE)

HAO-CE read can be used to read the data from a specified alternate if the correct flag character is stored in random record register R0 during the HAO control cycle. Following an HAO control cycle that stored a flag character into random record register R0, the read signal starts the prep read-write cycle. At D3 the contents of random register R0 are transferred to the serial register; at D4 the flag bits present cause action on the flag. Action on the flag gates the flag bits from the serial register to the 1301 flag register. When the head selection occurs at first index, the 1301 uses the content of the flag register to select head; the 1301 selects the specified alternate track. With the exception that an alternate track is being read, there are no read timing differences when reading an alternate track (Figure 99).

HAO Customer Read (HAO-CE Switch Off)

- **Allows reading of HA2, record address and record data.**
- **HAO switch on operator's panel ON.**
- **Format track is not used to define read data areas; therefore index is end of track.**
- **End operation at the end of an area if system sends stop.**

HAO customer read permits reading to start with HA2 and to continue until second index sets the read-write done trigger. There are some differences between HAO-CE and HAO read. Because the HAO-CE switch is off, action on the flag cannot occur during the prep read write cycle; also, the verify address cycle compares home address area one with the contents of the track register. Since the HAO-CE switch is off, a flag search occurs while reading home address area one. After home address area one check characters are processed,

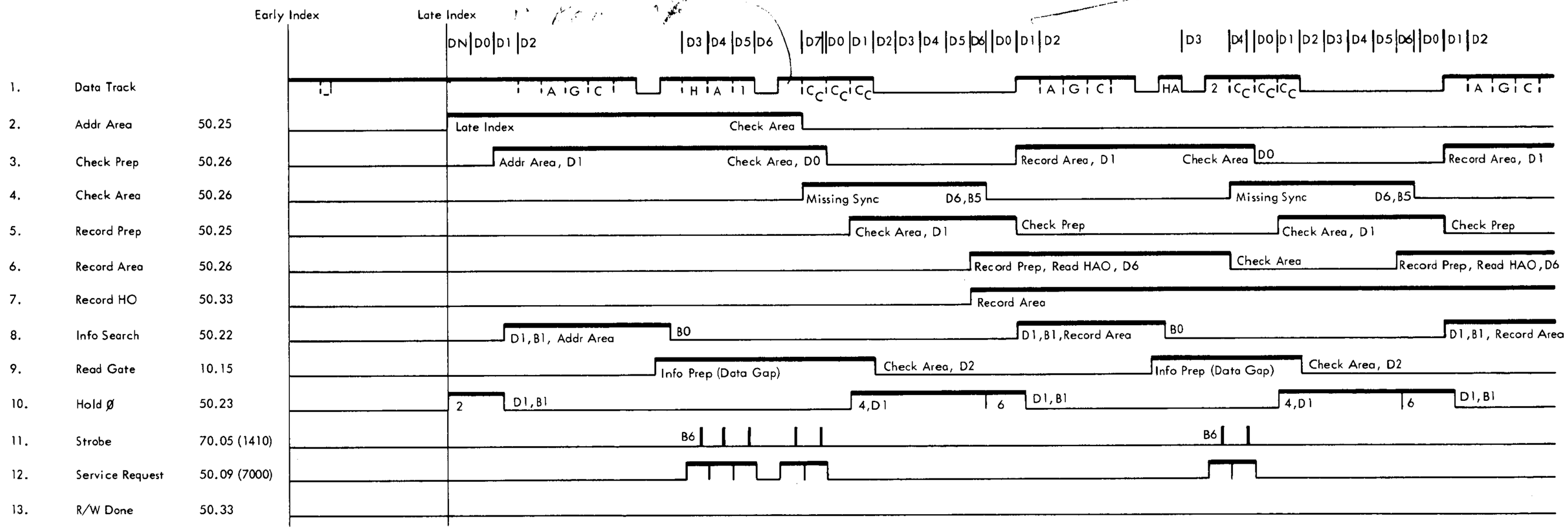


Figure 99. HAO-CE Read Timing

flag bits in the serial register cause action on flag. Action on flag switches the HAO customer read to the alternate track. Because the compare true trigger is reset with action on the flag, the HAO customer operation starts on the alternate track with a verify address cycle. After the verify address cycle, read data transfers start with HA2. Each remaining address and record is read and transferred to the system until second index sets the read-write done trigger.

If HA1 is verified and a flag character is not present, the HAO customer read operation continues on the specified track and starts read data transfers with HA2. End occurs when second index sets the read-write done trigger. As in the other HAO operations, if the computer issues stop or disconnect prior to the end of the track the data transfer circuits are reset and 7631 reads to the next check area. D5 of check area sets the read-write done trigger.

Write Format

- **Allows a format track to be written from system.**
- **1301 write format set to write.**
- **If HAO-CE switch is on, force a compare true.**
- **Decode system write data to: write bits or no bits on format track, set bit mode of bit ring, test for code error (must be 1, 2, 3 or 4).**
- **Write filler from system stop to index.**
- **Filler must be written for 11 characters or format error is indicated (format too long).**

The format tracks are written to define how the storage space of the tracks is to be divided into records, identified and used. Before writing, a complete format image must be assembled in the computer's storage. The computer's format track image must consist of the correct sequence of BCD ones, twos, threes, and fours for three reasons: firstly, the BCD characters determine if the file control is to write ones or blanks on the format track (BCD one and three cause the file control to write all bits. BCD two and four cause the file control to write blanks); secondly, BCD one and two control six-bit mode writing, and BCD three and four control eight-bit mode writing; thirdly, the file control is designed to indicate a code error if any BCD character other than one, two, three, or four is received. A code error causes an immediate format write end.

If the HAO-CE switch is on, the write format verify address cycle is bypassed. If the HAO-CE switch is off, the file control verifies the track address specified in the track register's head selection bits. Two write format sequences are shown at the top of Figure 100. The top write sequence shows a control cycle, followed by a prep read-write cycle, and the index holdover trigger reset before second index. Assume that, while the index holdover trigger is set, a verify address cycle occurs. If the verify address cycle is successful, format compare true resets the index holdover trigger. Because format write timing cannot be started until first index, file control operation remains suspended until the next first index. AGC writing starts as the first step in a write format sequence. Where a verify address cycle is required, the sequence at the top of Figure 100 shows it takes at least two disk revolutions to complete a format write operation.

If the HAO-CE switch is on, the format write sequence also takes a minimum of two disk revolutions to complete. Verify format and HAO-CE AND (ALD 70.15) to inhibit the normal index prep trigger turn-on. Index prep is set with the first late index following the prep read-write cycle, delaying first index until the next early index pulse. Thus, format write with or without a verify address cycle takes a minimum of two disk revolutions to complete.

Another possible variation in format write disk timing occurs if action on flag occurs after HA1 has been verified. Action on flag resets the index holdover trigger and causes the verify address cycle to occur on the alternate track. The alternate track format compare true resets the index holdover, and write format is delayed one more disk revolution (Figure 100, second write sequence).

Writing begins when prepare to verify and first index fire the 350-μs data AGC squelch singleshot. Write format and data AGC squelch conditions AND; the format

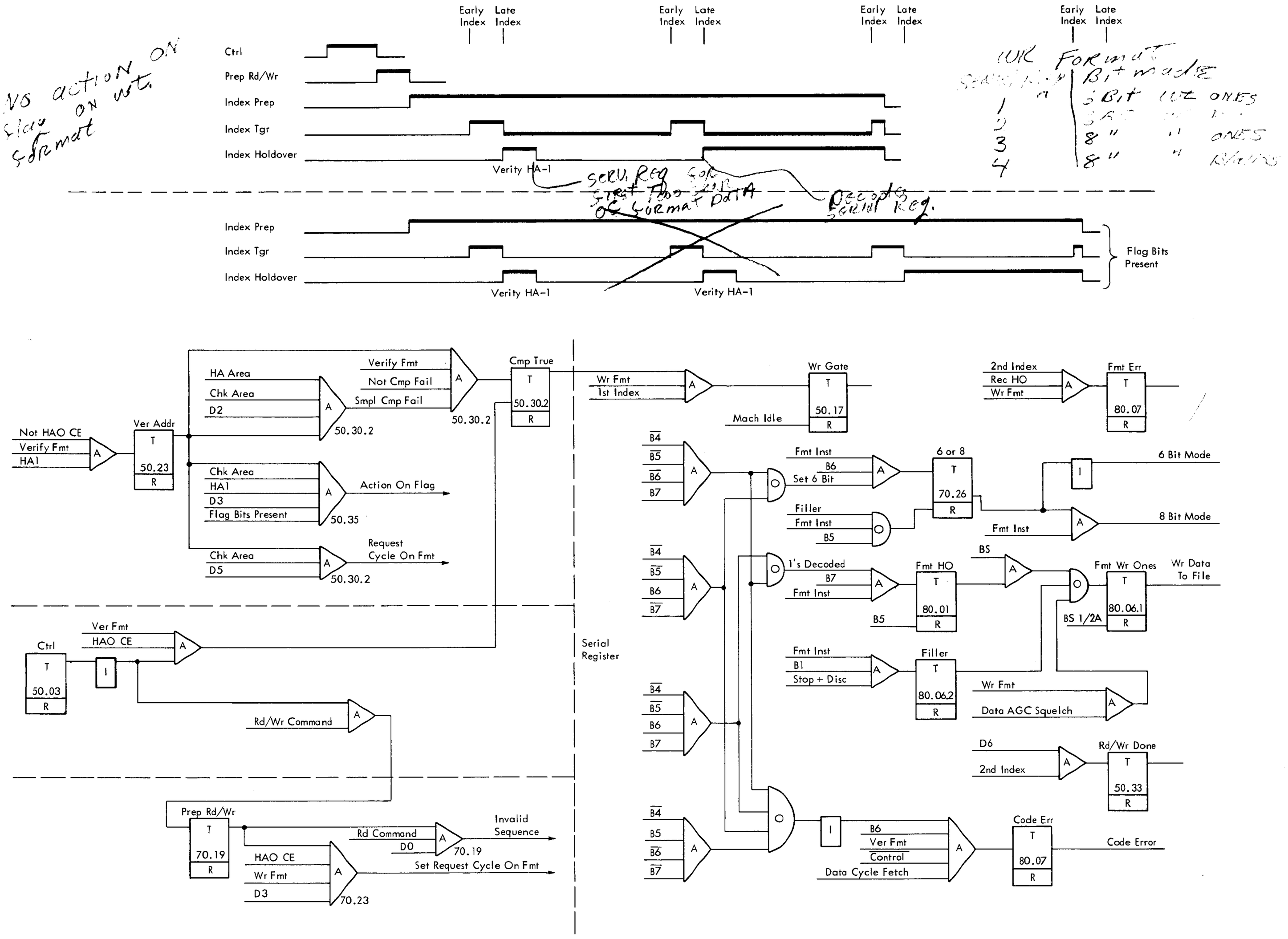


Figure 100. Format Write Sequence and Simplified Logic

write ones trigger is set. First index sets hold phase and the write gate, and writing starts. When the 350-μs data AGC squelch singleshot times out, the write gate remains on to create a gap between the AGC data and late index. Beginning with late index, format write data is written from the computer. Figure 100 shows the write data path for format write data.

The first data strobes or service requests cannot wait to be issued at late index. Requests or strobes for the first two characters are issued during the prep read-write cycle if the operation is HAO-CE write format. The first data character received is transferred from the I-O register to the serial register, and is decoded and stored in the format holdover trigger ready for use. The second character is stored in the serial register. The format holdover trigger remains reset because the first character is a BCD four (Figure 101). The second character requested remains stored in the serial register ready for decoding and use after the first character is written. If the HAO-CE switch is off, the first two characters are requested at the end of the verify address cycle.

Receipt of late index sets the record holdover trigger. Record holdover, pulse one, and pulse two trigger outputs AND to gate run clock on format write. Run clock on format write sets the clock trigger and restarts the bit ring. The first B7 samples the output of the decoder; if the decoder output is a zero the format holdover trigger is not set. Because the first three characters decoded are BCD fours, no-bits are written for the first three characters. The format holdover trigger remains reset until the fourth character is decoded. (Figure 100 shows the decoder outputs are monitored to determine the machine bit mode and to set code error if an invalid character is received. Figure 101, line 1, shows the write format data sequence.)

Starting with late index gated, eight bit mode characters are written to format HA1. After HA1 is formatted, six-bit mode characters are shown. With the exception of HA1, the remaining format track areas can be written in six- or eight-bit mode.

The format write instruction is the only instruction that requires the computer to issue stop or disconnect. Stop or disconnect sets the run digit and filler triggers. Eight-bit mode filler is written until D6 of second index, when machine idle resets the write gate. D11 must reset the record holdover trigger before second index to prevent a format too long error; second index, record holdover, and write format cause a format error. A format error means that stop or disconnect has been issued too late to have D11 reset record holdover before second index; this indicates the program did not allow space to write at least 11 characters of filler after the format track.

Write Check

- **Permits checking data previously written on disk.**
- **System operates in write mode.**
- **1301 operates in read mode.**
- **7631 compares system write data with 1301 read data.**
- **A failure to compare during data comparison is indicated by write check error.**
- **A failure to compare during check character comparison is indicated by parity error.**

Write check provides a method of checking data previously written on a disk. If the write check operation is used, it should follow the write operation to be write-checked. Write check conditions the 7631 to request write data from the system and compare it with the read data from the 1301. The type of write check operation performed (TRO, TWA, SRO, or CYO) depends on the preceding mode of operation; that is, if SRO preceded the write check instruction, then the check is a write check SRO. The prepare to verify triggers are not reset when write check is decoded during the write check control cycle. This permits the previously set prepare to verify trigger to sequence the write check operation. For example, if the prepare to verify TRO trigger is set, write check and receipt of write cause the file control to execute a prep read-write cycle, a HA verify address cycle, and to write check the following record address and records. (Figure 103 shows write check timing for the first record address and record of a TRO write check operation. Lines 1 through 16 show

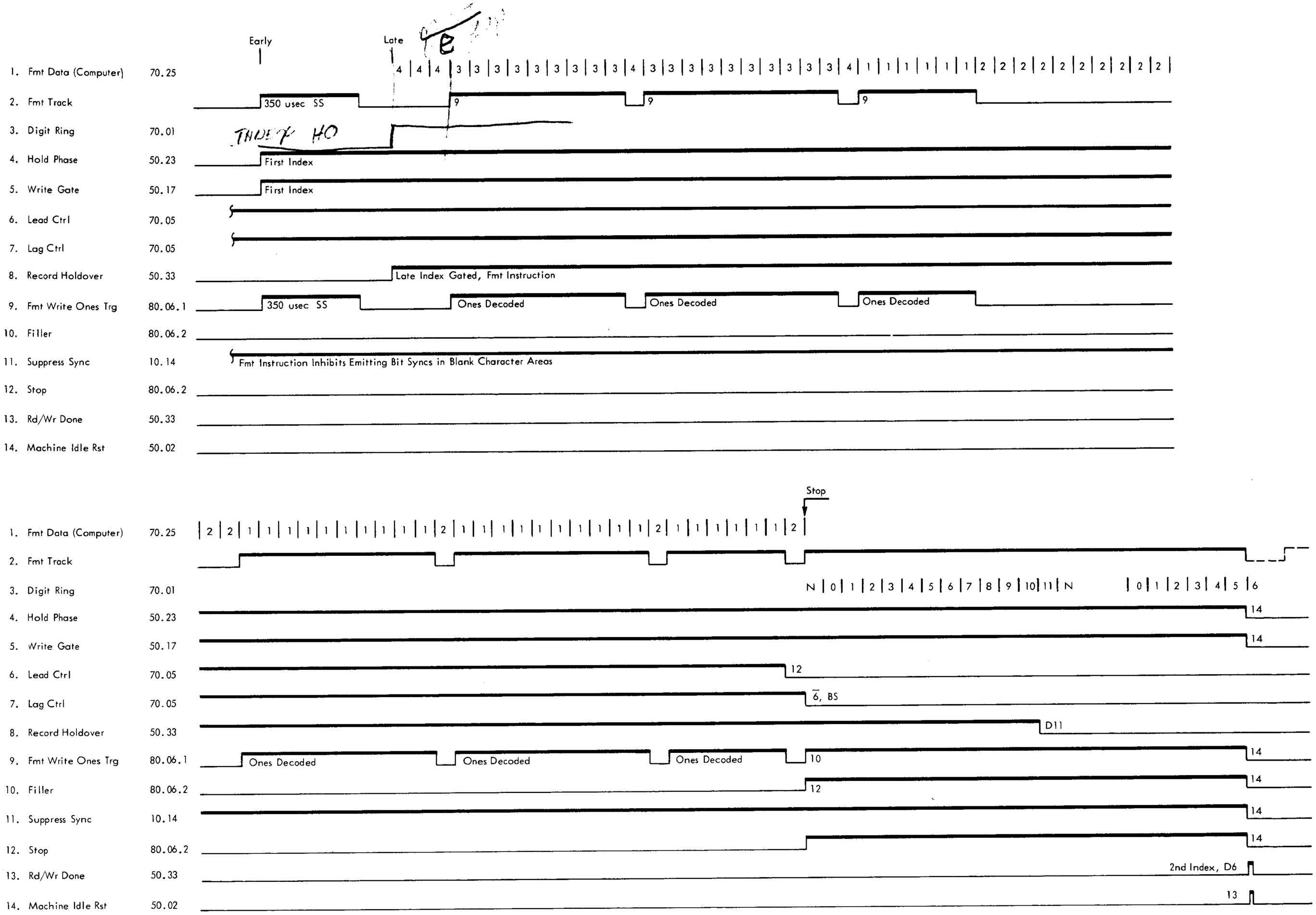


Figure 101. Format Write Timing

that the read timing is identical to any record address or record read data cycle.)

Figure 102 shows write check data flow. The heavy dashed line shows write data flow from the serial register to the compare circuits. Read data flow follows a normal read data path: from data trigger A, to data trigger B, to the shift register, and to the compare circuits. Check characters are generated from the read data; they are read out and compared with the check characters read from the disk track.

The sequence of a write check operation follows the sequence of the previous write operation. For example, if the previous operation was a TRO operation, it can be followed by write check.

Two exceptions occur during write check. Firstly, a write gate is not generated for a write check. Secondly, because write data is compared with read data, the first write data character must be stored in the serial register ready for comparison before reading the first data bit from the disk; therefore, D1, record or address, and write check are used to set the lead control trigger. The first data strobe is issued at B6 or the first service request is issued at B1 when the lead control trigger is set.

Because file control timing is operating in read mode, the hold phase reset stops the timing at BS of D2. (Figure 103, line 21, shows that the service request trigger remains on until timing resumes with the receipt of the first read data bit sync.)

Request cycle fetch is generated when lead control, not read, and not first index AND. Request cycle fetch controls:

1. the input register reset (B1)
2. the input register loading (gate write data one, at B5)
3. the data strobe (B6)

B6 of D2 sets lead holdover. Lead holdover, not read, and not first index control:

1. the serial register reset (BS1/2A).
2. the input register transfer to the serial register (gate register one to serial register)

When the data gap sensor times out in the gap separating AGC from the read data, the read gate is set and reading starts. Receipt of the first read sync-bit causes a phase selection. The read bit timing is used to gate each read data bit from data trigger A, to data trigger B, from data trigger B to the compare circuits, and into the shift register. The read data bit timings are also used to gate the corresponding bit of write data from the serial register to the compare circuit, where the write check comparison is made.

Each data character transferred to the file control is compared with the corresponding read data character from the track. The read and write data comparisons continue until check area (Figure 103, line 22, shows the readout gate). The check characters generated with read data are then compared bit by bit with the check characters read from the data track. (Figure 103 shows that check area read mode timing ends at D6. Since a TRO write check operation is assumed, the timing sequence required to compare write data with read data is shown starting with the following record area.)

The write check operation ends are the same as the operation being write-checked. The write check end op can be the result of stop or disconnect after the last write data character is transferred, or of end of track if a complete track of records and addresses is written. The verify monitor is set when each record address or record is write-checked; the monitor gates not compare conditions to the write check error trigger. A write check error is indicated for not compare condition. If a not compare condition occurs while comparing check characters, a parity error will be indicated.

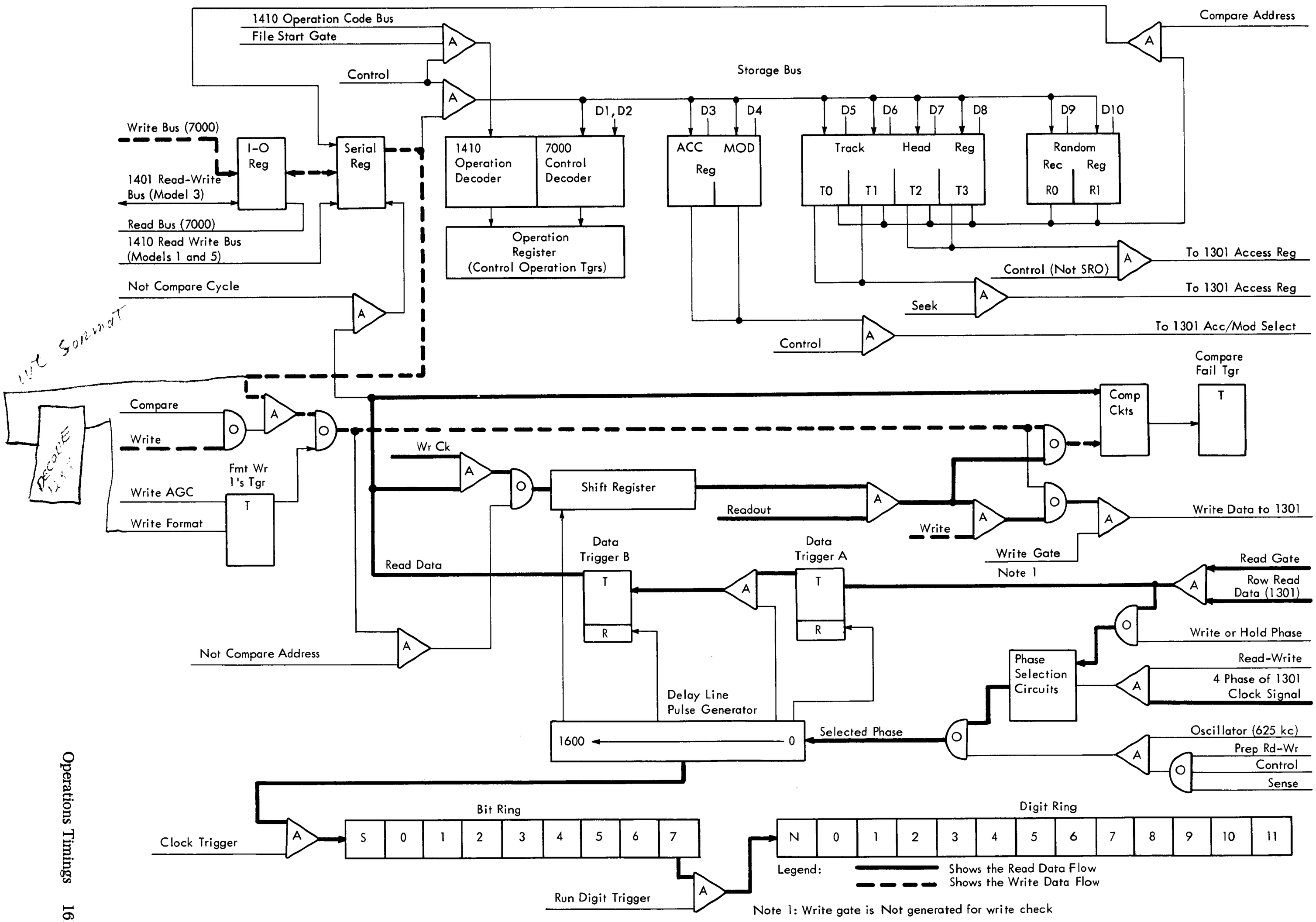


Figure 102. Write Check Data Flow Diagram

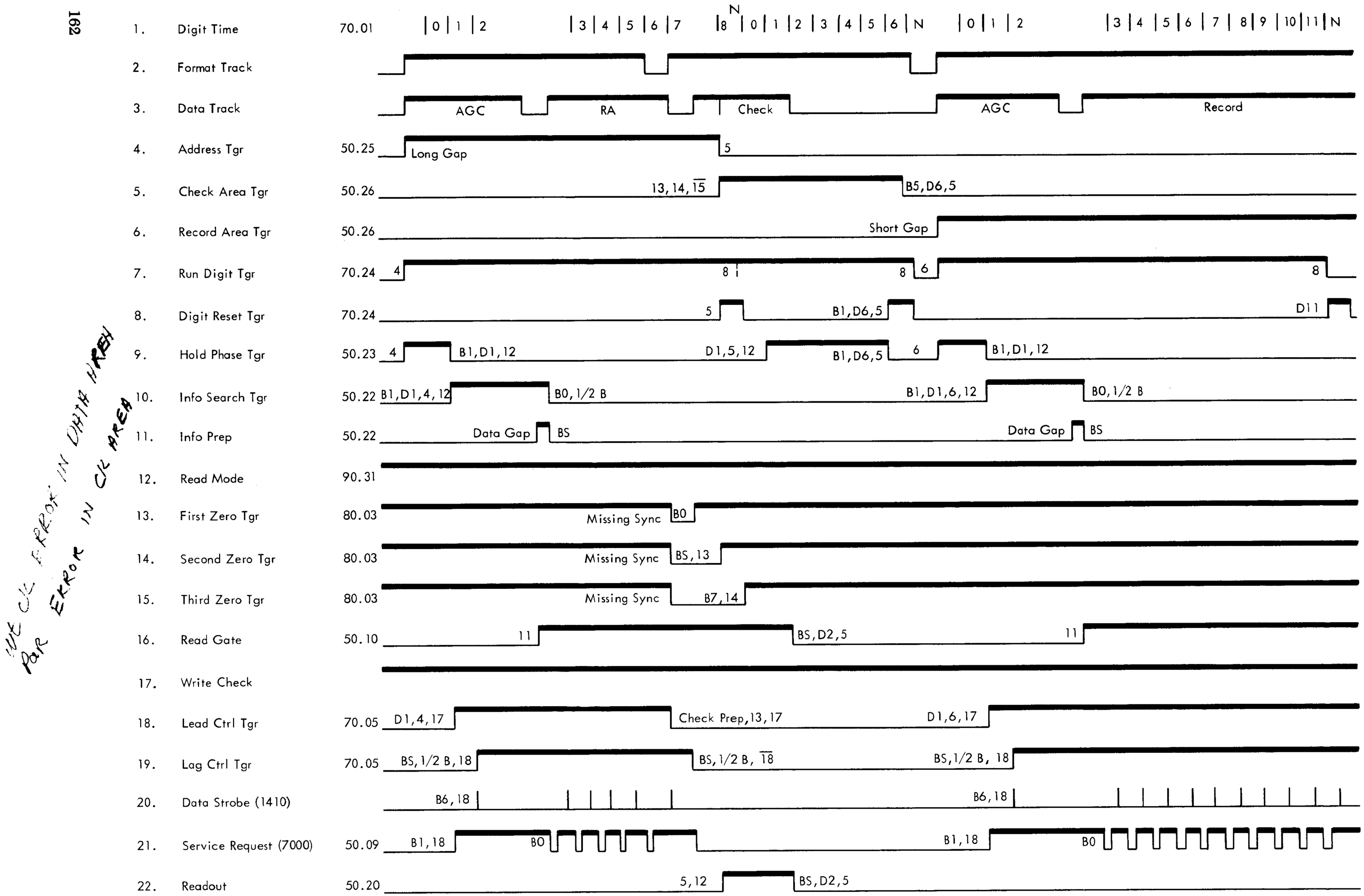


Figure 103. Write Check Timing

Format Write Check

- **Permits write checking of a write format instruction.**
- **Compares system write data decoded to bits or no bits with format read data.**
- **Failure to compare causes write check error.**
- **Also tests format long and short gap singleshots, and if incorrect indicates a file adapter circuit check.**

Format write check conditions the file control to read and compare the format track data with format write data transferred from the system. In addition, the gap detectors and the three zeros triggers outputs are compared to determine if the format track gaps are correct, or if the gap detectors are operating correctly. A read and write data comparison failure sets the write check error trigger. If the gaps or gap detectors cause a failure, a file adapter circuit check results.

As in format writing, format write check data flows from the serial register to the control decoder where the one's decoded output is used to set the format holdover trigger (Figure 104). The format holdover trigger output is used to set the format write ones trigger; the format write ones trigger output is used for compare data. Check characters are also generated from the format write ones trigger output, and because check characters are not needed, the readout gate is not generated. Read data flows from the format track to data trigger A, to data trigger B, and to the compare circuits. Format read data is also used to operate the phase select circuits to generate read data timing.

Compare Circuits

Figure 105 shows the simplified format write check compare logic. A compare failure during write check sets the write check error trigger. When write data (BCD twos or fours) are decoded, the format write ones trigger is reset. The lower portion of Figure 105 shows the simplified logic used to test for the presence of gaps or inoperative gap detectors. Five tests are made in a format write check operation. The first test is made to compare format read data (all one bits) with decoded format write data. Serially by bit, the format read one-bits are compared with format write one-bits (Figure 105). If a bit fails to compare, the write check error trigger is set.

The remaining four tests are used to test for the absence of gaps or for inoperative gap detectors. The first gap test, no short gap, compares format not write ones with no short gap; these conditions indicate no short gap and cause a file adapter circuit check (Figure 105). The second gap test, short gap detector inoperative, compares format write ones with short gap; these conditions indicate short gap detector inop and cause a file adapter circuit check (Figure 105). The third gap test, long gap det to short, compares format write ones with long gap; these conditions indicate long gap det to short and cause a file adapter circuit check (Figure 105). The fourth gap test, no long gap, compares format not write ones and not long gap; these conditions indicate no long gap and cause a file adapter circuit check (Figure 105).

Timing Circuits

The starting sequence for the format write check operation is the same as that of format write (format write check timing is shown in Figure 106). Beginning with the first index the data AGC squelch singleshot is pulsed. The data AGC squelch singleshot output sets the format write ones trigger because the write gate is not generated during the write check the format write ones trigger output during first index is not used. First index is also used to set the hold phase trigger. Hold phase is required to develop timing for the write check operation when reading gaps in the format track. The write check operations start with late index gated. Late index gated sets the record holdover trigger (Figure 106). Record holdover and format check set the read gate and clock triggers.

Because the first read data characters are blanks, hold phase timing is used to sequence the format write check operation for the first three character cycles. After the first three blank characters are compared, the first bit of format read data is used as bit-sync by the phase select circuits. Normal read data timing is developed until the next blank character is read from the format track.

To illustrate the above, (ALD 10.16) circuits 5A and 5B cannot gate B4 to flip the binary trigger because circuit 5A is inhibited with hold phase and circuit 5B is inhibited with not decode ones when the format write data decodes as zeros. When ones are decoded, decode ones, format check, and B4 flip the binary trigger to effect a normal read data phase selection. The format write ones trigger is set for each ones decoded. The

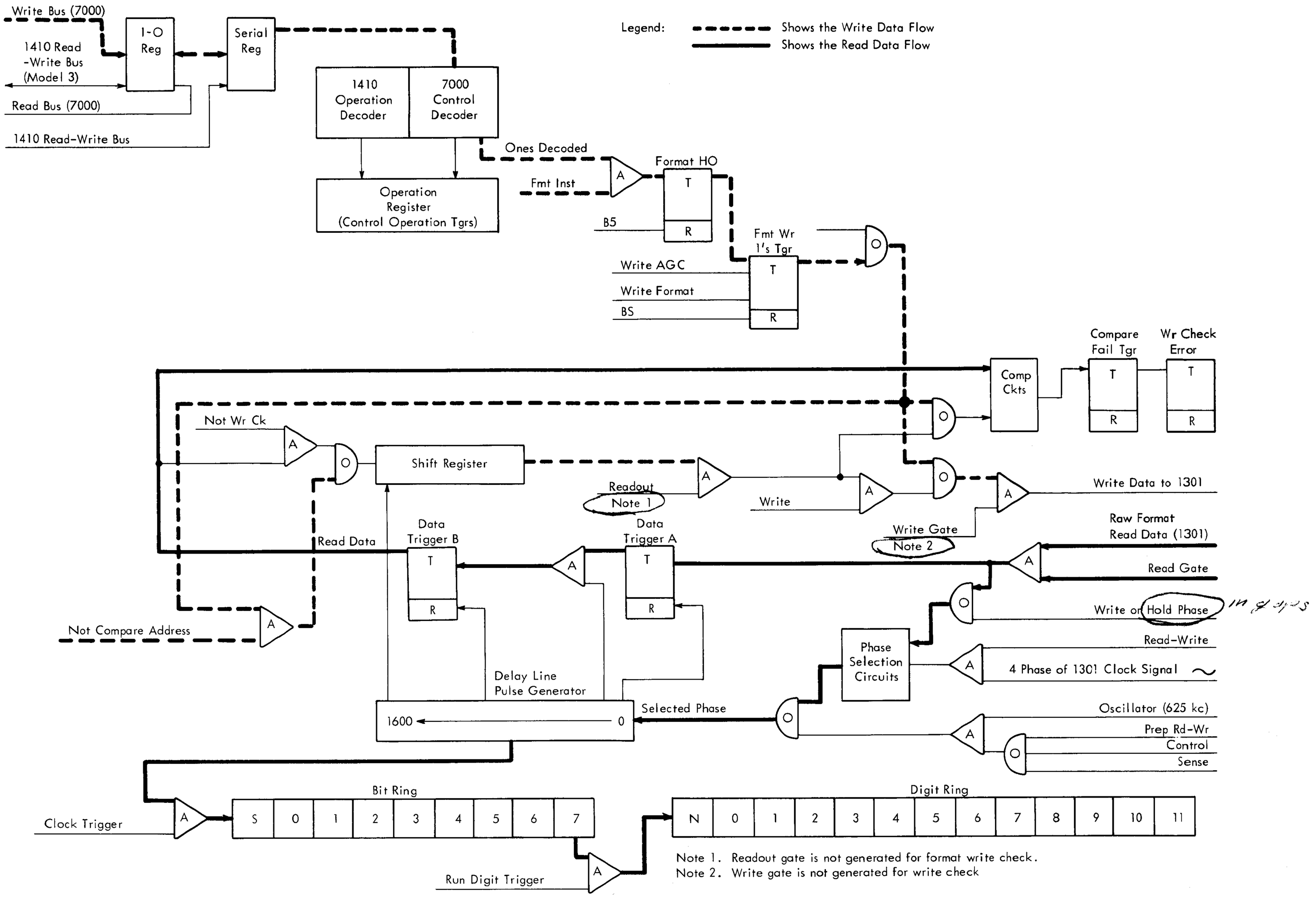
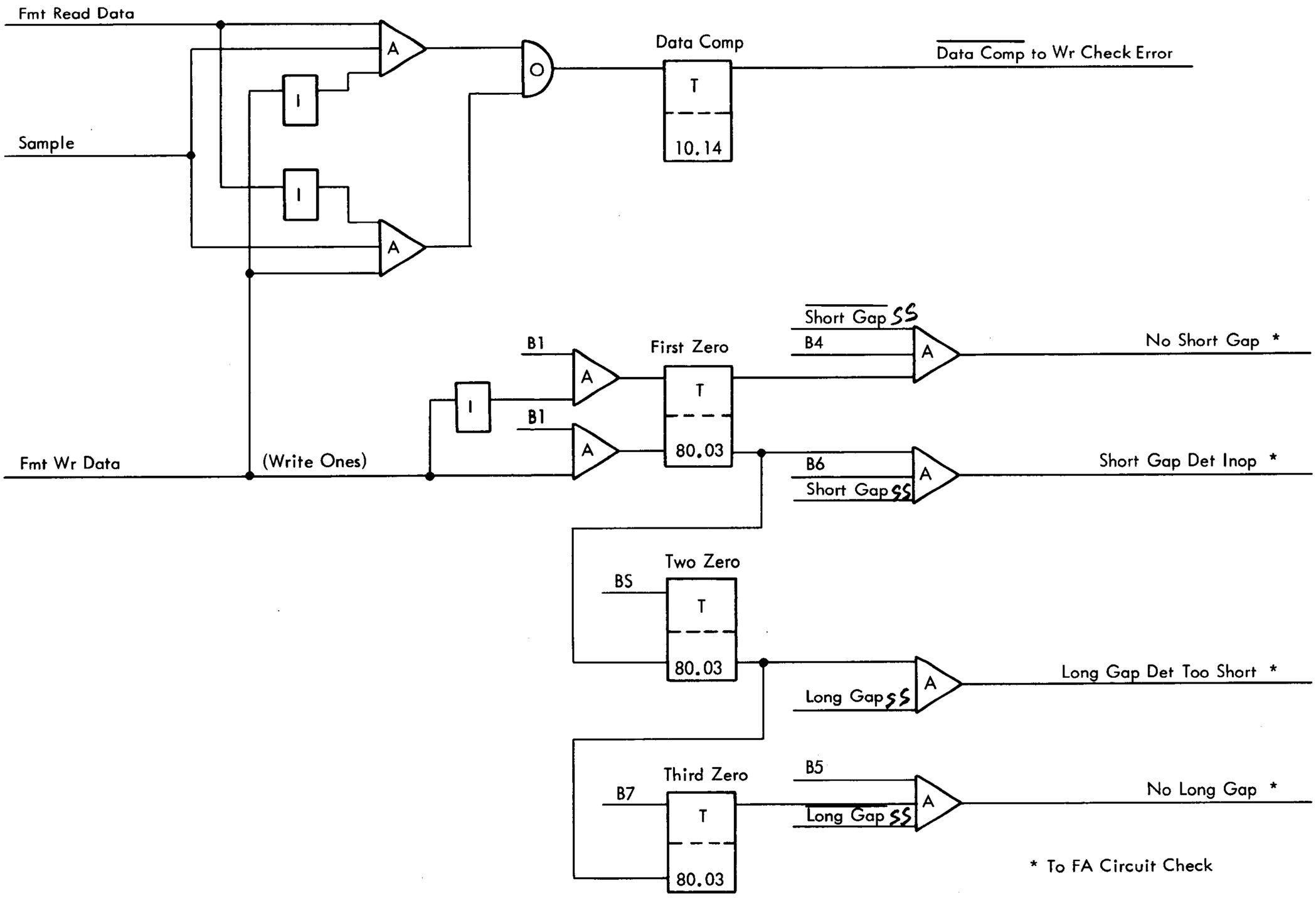


Figure 104. Format Write Check Data Flow Diagram

decode ones output conditions block 5B to permit read data phase selection when not in a gap area. The write check operation continues until stop or disconnect is received; stop resets the lead control trigger and sets the filler trigger. The filler trigger and the first BS reset the read gate. Stop also sets the run digit trigger, and run digit gates the digit ring. The digit ring operates with hold phase timing until D11 resets the record holdover trigger. Second index, record holdover and format instruction AND to test for format too long. The format write check operation ends when D6 and second index set the read-write done trigger.



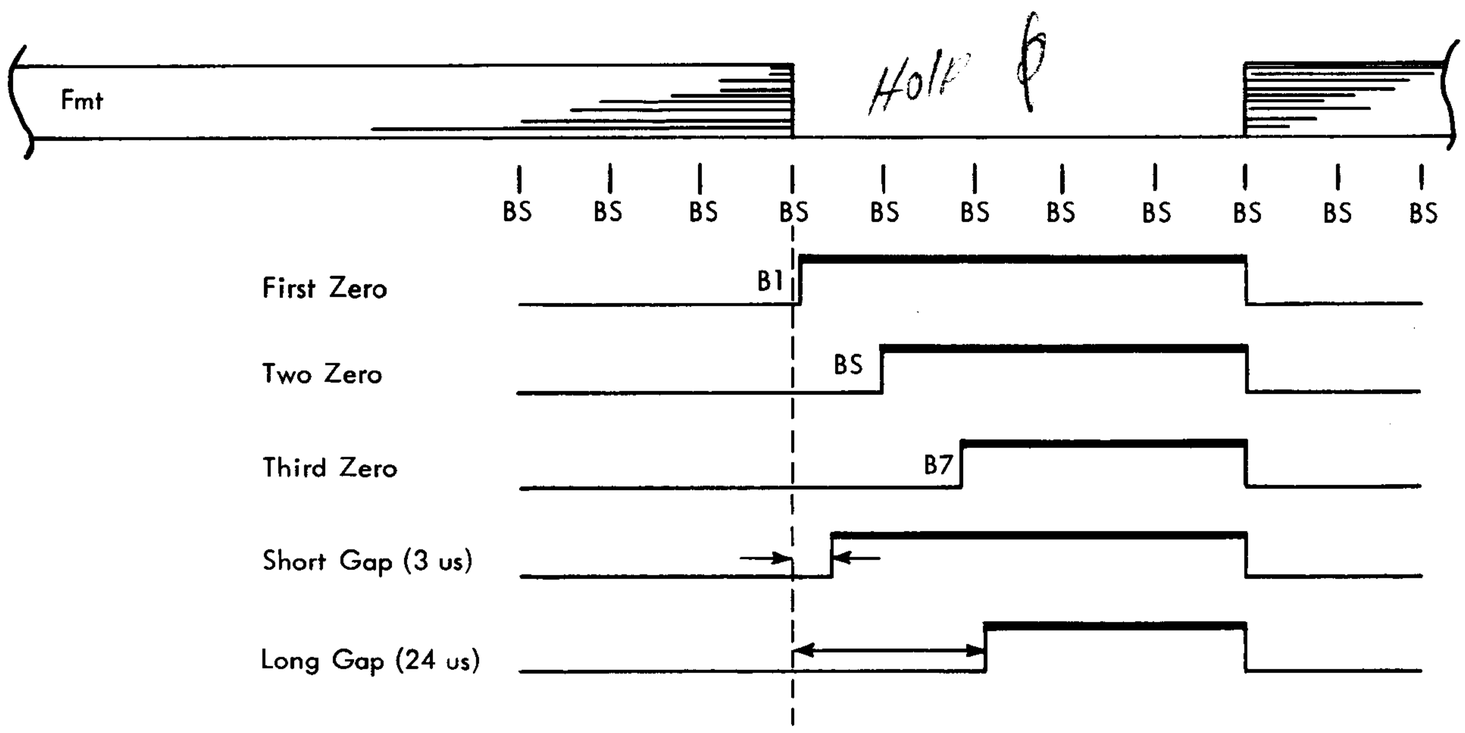


Figure 105. Format Write Check Simplified Logic

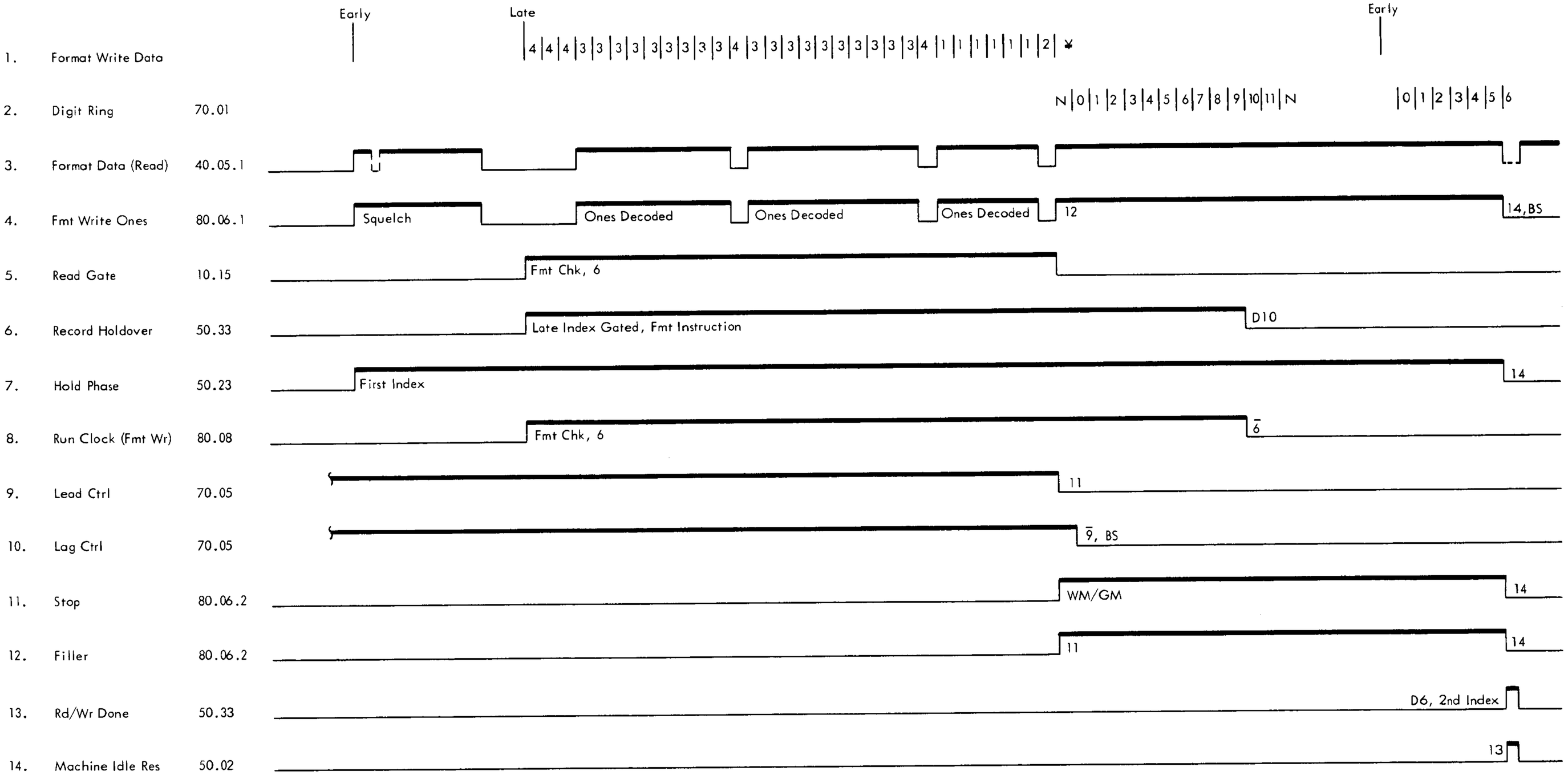


Figure 106. Format Write Check Timing

Sense (7000)

- **Control timing circuits and transfer ten bytes of sense data.**
- **Indicates error and attention status of 7631 and 1301's.**

The sense command is used to obtain status information from the 7631. The status word contains ten four-bit bytes of error and attention status information. The first byte, the summary byte, indicates the type of error. The next three bytes indicate specific errors that occurred on the preceding instruction. The next byte indicates whether the 7631 is programmed for six-bit mode. The next three bytes indicate the accesses which have been programmed to seek and have come to rest waiting for use. The last two bytes are reserved (Figure 107).

Receipt of the sense command signals the 7631 to start the timing circuits and transfer ten bytes of data. Oscillator pulses are used as the source of sense timing. The sense command disables the immediate stop on error signal to allow all sense data to transfer without interruption. Beginning with D0, the first service request is generated to transfer the first byte of sense data. Odd parity is assigned to each byte of transferred sense data. Sense data transfers continue for each digit cycle until D10 prevents service requests and causes the 7631 to signal normal end to the data channel (Figure 108).

Status Char	Bit No.	BCD Bit	Assignment	Comment
0	3	A	Reserved	Summary Byte
	5	4	Program Check	
	6	2	Data Check	
	7	1	Exceptional Condition	
1	3	A	Invalid Sequence	Program Check
	5	4	Invalid Code	
	6	2	Format Check	
	7	1	No Record Found	
2	3	A	Invalid Address	
	5	4	Response Check	Data Check
	6	2	Data Compare Check	
	7	1	Parity or Check Char Code Check	
3	3	A	Access Inoperative	Exceptional Condition
	5	4	Access Not Ready	
	6	2	Disk Storage Circuit Check	
	7	1	File Control Circuit Check	
4	3	A	Reserved	Data Mode
	5	4	Six-Bit Mode	
	6	2	Reserved	
	7	1	Reserved	
5	3	A	Module 0	Attention
	5	4	Module 1 (Disk Only)	
	6	2	Module 2	
	7	1	Module 3 (Disk Only)	
6	3	A	Module 4	Attention
	5	4	Module 5 (Disk Only)	
	6	2	Module 6	
	7	1	Module 7 (Disk Only)	
7	3	A	Module 8	Attention
	5	4	Module 9 (Disk Only)	
	6	2	Reserved	
	7	1	Reserved	
8,9			Reserved	

Figure 107. Status Data Bit Assignment

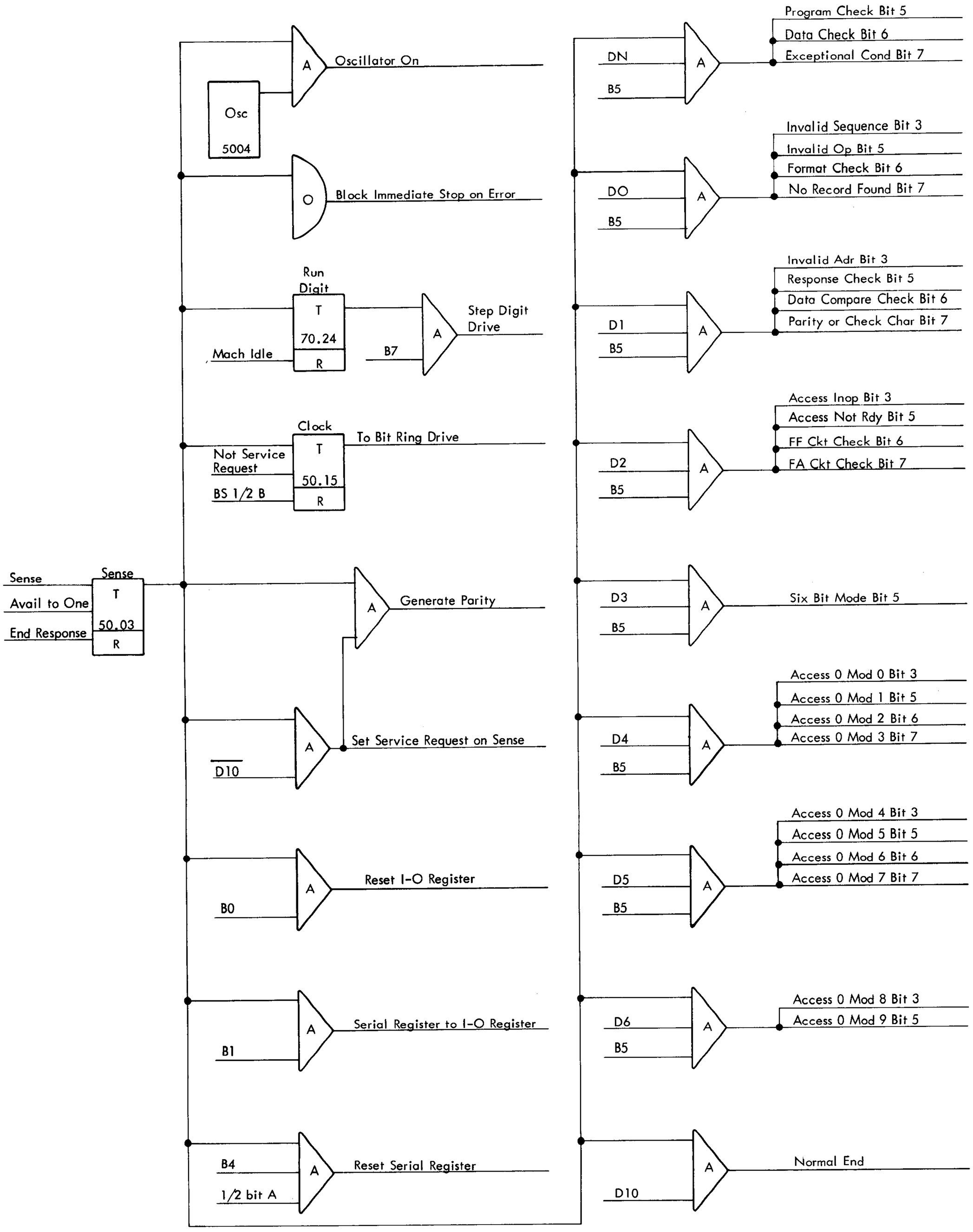


Figure 108. Sense—7000

Drum Control Feature

- **The drum control feature can be installed on any one of the five 7631 models.**
- **The drum provides reduced access time and higher data transmission rates.**
- **Mixed 1301 and drum units can be connected to one 7631A.**
- **Drum operation is essentially the same as 1301 operation.**
- **The drum has 400 tracks: 10 cylinders of 40 tracks.**

The drum control feature of the 7631A file control* permits one or more 7320 drum units to be connected to the 7090/94 or 1410 systems. The drum control feature can be installed on any one of the five 7631A models. The drum provides the system with reduced access time and higher data transmission rates to and from the data stored at random. Mixed 1301 and drum units can be connected to the 7631A with a drum control feature installed; this feature permits the drum to be used as an index for 1301 data storage or as intermediate storage for data to or from the 1301 data storage.

The drum control feature is packaged in a logic panel containing 84 (3 × 28) socket positions; the 7631A has space for three panels of this size. The drum control feature uses saturating drift transistor-diode logic and SDTRL. The voltages for this logic feature are available in the 7631A; therefore, field installation of this feature is possible.

The high speed 7631A circuits make it possible to function with the drum control feature. However, the drum control feature cannot be used with 7631 because it does not have the required high speed circuits. When the drum is connected to the 7631A, its operation is essentially the same as 1301 operation. The drum can be controlled by 1301 programs without major program revisions. Some of the drum and 1301 differences are:

Capacity (six-bit characters)	1301 Module-28×10^6	Drum-1.27×10^6
Character frequency maximum	1301-90-KC	Drum-208-KC
Rotational speed maximum	1301-1795 rpm	Drum-3550 rpm
Rotational delay average	1301-17 ms	Drum-8.5 ms

The drum data organization closely parallels the 1301 disk data organization. The 1301 has 250 cylinders of 40 tracks each. The drum has its 400 tracks arranged in ten cylinders of 40 tracks each. The 1301 has a format track for each of its 250 cylinders. The drum has one format track for the entire 400 data tracks. The format track in either case is program-controlled.

The 7631A has provisions to connect five files; with the control feature, these units may be either drum units or 1301 disk files in any combination up to the five unit limit.

*The 7631A designation pertains to units of the 7631 File Control having Serial Numbers 12000 and higher.

Operational Characteristics

- **Seek operation requires electronic head switching—no mechanical motion.**
- **Drum read and write operations are identical to 1301.**
- **Set access in-op is an invalid drum operation.**
- **The drum does not use flag bits.**

Since the drum and the 1301 are organized similarly, only the operation differences are presented.

Seek

The drum seek requires only electronic head switching; no mechanical motion is necessary as in the 1301. This

means the program-interrupt that is generated when a seek is completed will always arrive during the seek with the drum unit. The 1301 signals not ready while the arms are in motion as a result of a seek. The drum has no provision for the not ready signal.

Write Operations

The writing modes available with the drum are identical to 1301 writing modes. The writing modes are: write single record, write full track, write track without addresses, write home address, write cylinder, and write format. To perform a format write with either the 1301 or the drum a switch must be thrown on the selected module.

Read Operations

The modes of reading available with the drum are identical to 1301 modes of reading. They are: read single record, read full track, read track without addresses, read home address, and read cylinder.

Write Check

Drum operation with write check is essentially identical to 1301 operation.

Set Access Inoperative

The set access inoperative command is invalid to a drum.

Cylinder Operation

Cylinder operation is an optional feature of the 7631 file control. The cylinder mode drum appears to be ten cylinders of 40 tracks each; this makes drum cylinder operation the same as 1301 cylinder operation.

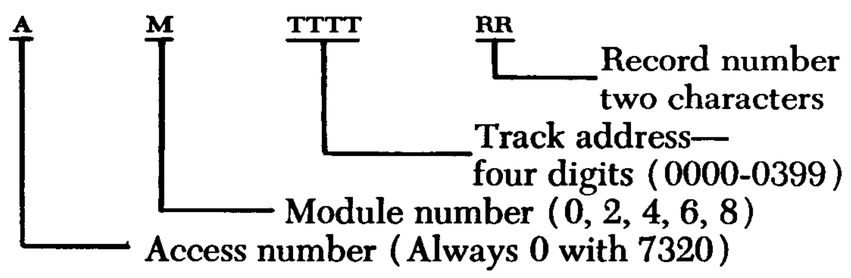
Alternate Surface Flagging

The drum does not use flag bits. Defective drum tracks are replaced by permanently wiring in a head provided for the purpose. The defective track will not have a read-write head. The alternate head acts as a permanent replacement for the defective location.

Address Organization

- **A circuit check is made to insure the use of access zero only.**
- **The drum assumes the same module number as a single module 1301.**

The address format in the 7631A file control is as shown:



The drum unit is addressed as access 0 because multiple accesses are not meaningful with the drum. A circuit check is made to insure the use of access zero only.

The module number for a drum depends on which of the five cable connectors on the 7631A is being used with the file. The drum assumes the same module numbers as single module 1301's connected in the same manner. The drum unit is: module 0 if connected to the first cable connector of the 7631A; module two if connected to the second cable connector; module four on the third cable connector; module six on the fourth cable connector; and module eight on the fifth cable connector. An odd number in the module field will result in an unusual end due to access inop.

The method for addressing the drum track is to use a number between 0000 and 0399. The highest order address digit is not needed but is carried along for 1301 compatibility.

The two random record number characters serve the same purpose on either the 1301 or the drum.

Instruction Times

- **The drum takes one half the time to execute a comparable 1301 operation.**
- **A new line, drum on line, is added to the 7631A interface to differentiate, in the 7631A, between 1301 and 7320.**
- **Squelch is not used but recovery delay is needed after head switching.**
- **The format skew detector is disabled with drum on line.**
- **Format sync bits are not used.**
- **Phase selection is not needed with 7320.**
- **The 7320 clock track is the same as 1301, but two data bits are written for each 1.6 μs cycle.**

Read and write operations vary in time duration depending on the length of the data field involved. In general, the drum takes one-half the time taken by the identical operation on the 1301. Access time, of course, is much faster than that of a 1301.

Service requests or data strobes occur as often as once each 4.8 microseconds with the drum when six-bit characters are transferred. The 7631A checks for an overrun condition 3.32 microseconds after a service request rises at the output of the line driver to the interface.

Control, prep read-write and sense operations are timed by the 7631A oscillator; the operation is the same time with either a drum or a 1301.

A new line, drum on line, is added to the 7631A interface to differentiate in the 7631A between a 1301 and a 7320.

The AGC burst is not needed by the 7320 but is written for 1301 compatability.

Squelch is not used with the 7320 but recovery time delay is necessary after switching heads, so the squelch logic is retained to give this time delay on SRO.

The format skew detector is disabled with drum on line.

The index area is 475 ±35 microseconds.

There are 350 microseconds (478 bits) left to the programmer for re-addressing at the end of the track.

Format short gap is the initial controlling factor determining the end of a data area and the start of check area when reading or writing.

Formatting is similar to that in the 1301, but since there are no format sync bits, there is space for 384 more characters in six-bit mode or 286 more characters in eight-bit mode.

Phase selection is not required with the 7320 because of the fixed and rigid head mounting.

Because phase selection is not required, sync bits are not required except for a few specified positions on the data track. Circuit delays require sync bits with the first and last characters of each address or record, the first check character and the first AGC character. No sync bits are written on the format track.

The drum feature enables the bit ring to bypass BS time in all areas where sync bits are not written and to remain in step with the data with drum on line.

The drum bit rate is double that of the 1301: 0.8 microseconds as opposed to 1.6 microseconds.

The prerecorded clock track on the 7320 has the same frequency as the 1301.

With drum on line, two bit cycles occur within each 1.6 microsecond clock cycle.

The 1301 selects one of the four phases of each 1.6 microsecond clock cycle for data gating. The 7320 must use two of the four phases (phases one and three) each clock cycle to accommodate the double bit rate of the 7320.

With drum on line, the 7631A chooses phases one and three of each 1.6 microsecond clock cycle to provide data clocking at a 0.8 microsecond rate.

Drum Feature Functional Units

Phase Pulse Control

- **Phase pulse control circuits start and stop drum read and write timing instead of phase select circuits.**
- **Drum phases one and three mixed are used for timing.**
- **The delay line pulse generator is pulsed twice for each 1.6 μs clock cycle.**

The phase pulse control circuits, three triggers labeled phase select, reset phase, and data sync, are used only for drum operation. This circuit is used to start and stop all drum read and write timing instead of the phase selection circuits required for 1301 operation. Drum on line, available when a drum is selected, disables the phase selection circuits used for 1301 operation and enables the drum feature phase pulse control circuits (see Figure 109, circled numbers one and two).

Briefly, the phase pulse control circuits OR drum phases one and three and gate the two phases to the begin drum bit cycle line. The begin drum bit cycle line becomes the selected phase input to the delay line pulse generator. Because two phases of each drum clock cycle are gated onto the selected phase line, the delay line pulse generator is pulsed twice for each clock track cycle, or once every 0.8 microseconds.

Since drum and 1301 operations are similar, some of the turn-on and turn-off conditions for the selected phase are similar. Figure 110 summarizes the drum phase control on and off conditions. For example, see the circled number one on the left side of Figure 110; set hold phase on index is used for both 1301 and drum operations. Set hold phase on index is needed during HAO-CE write operations to generate timing used to write index area filler.

A difference between 1301 and drum operation can be shown by the absence of the drum phase select trigger reset required to end read mode hold phase timing at BS of D2. To simulate 1301 timing when operating with the drum, the drum phase select trigger is not reset at BS of D2 and clock phases one and three continue to appear on the selected phase line after BS of

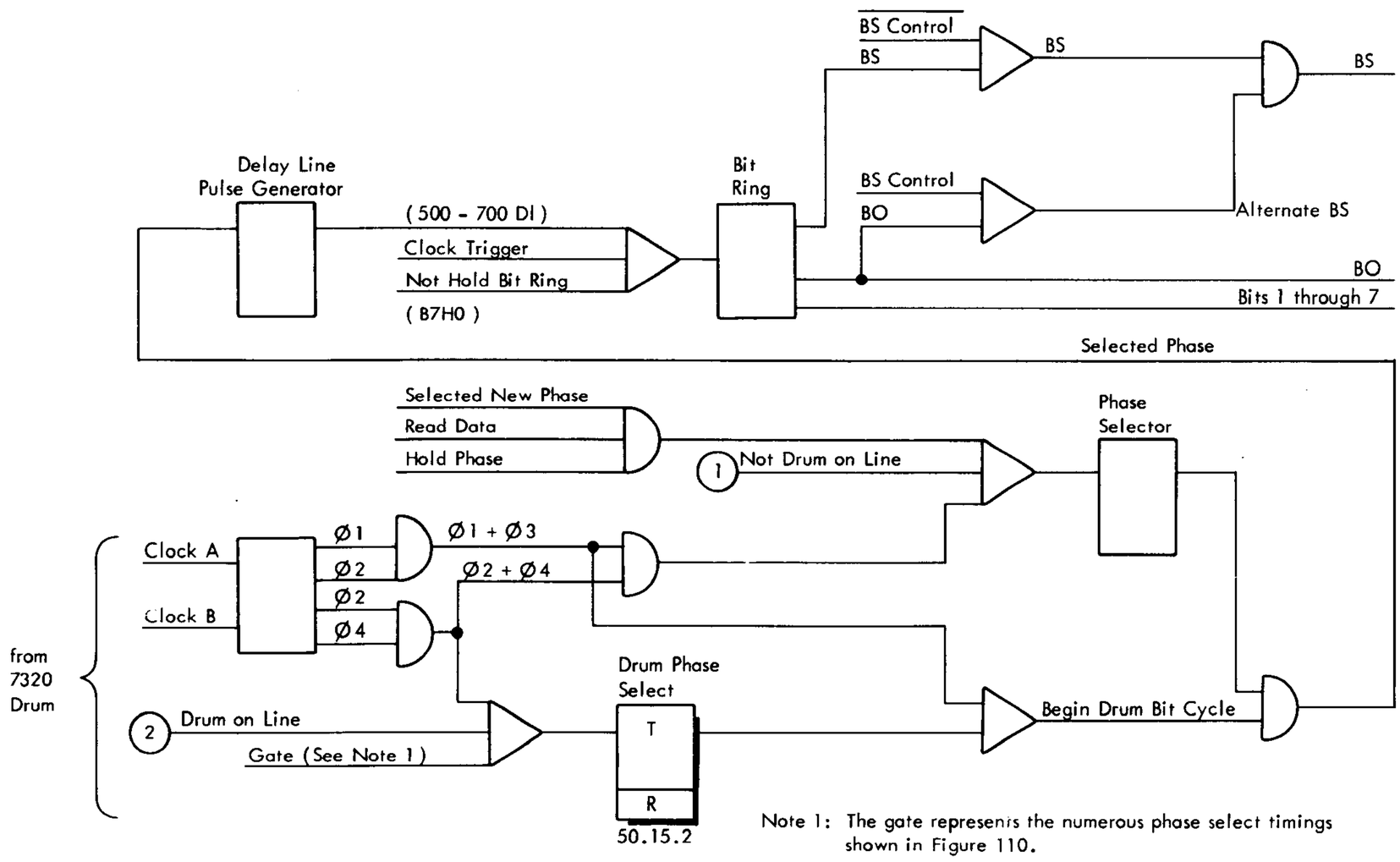


Figure 109. Phase Pulse Generation and Bit Ring Control

D2. To stop drum read timing at BS of D2, the clock trigger is reset to stop bit and digit ring operation until the first read data bit-sync sets the clock trigger to resume bit and digit ring timing, as in 1301 operation.

Another difference in 1301 and drum operation is check area timing. Because the check area trigger is reset in read and write mode with timing pulses, check area ends at D5 for drum operation (D6 with 1301 operation) when the reset phase trigger is reset. (See Figure 110, circled number two.) The early check area reset, for drum operation, insures that the next address or record area will not be modified by a check area timing circuit delay caused by skew.

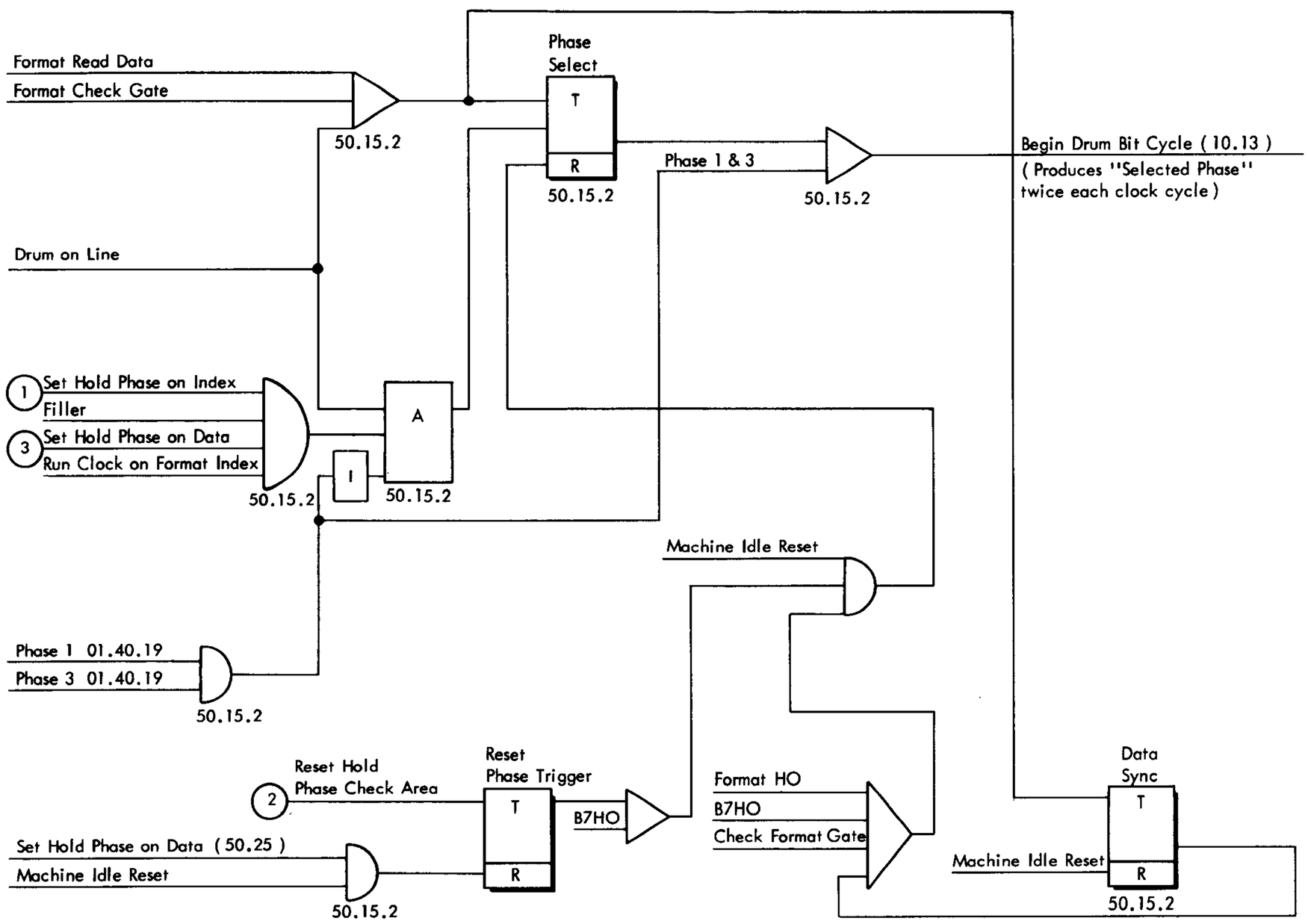


Figure 110. Drum Phase Pulse Control

Bit-Sync Control

- **The bit-sync control circuits alter the bit ring sequence.**
- **The BS control trigger starts the bit ring from B0.**

The bit-sync control circuit is needed for all drum read and write operations. The circuit is needed because only certain characters written on the drum have sync-bits. When the BS control trigger is on, the bit ring cycle starts from B0 rather than BS, and steps through to B7 and directly to B0 again.

During 1301 operation the bit ring develops an odd number of bit timings (depending on bit mode, seven or nine); thus, the binary drive sequence must be altered before each succeeding bit ring cycle. Failure to alter the bit ring drive sequence before entering the next bit ring cycle causes the ring to start operation with the incorrect bit drive phase, drive A for BS. To alter the bit drive phase sequence, B7HO is applied to the hold bit drive line (ALD 01.50.05). Hold bit drive is applied (as inhibit to the binary trigger drive) to pre-

vent 500-700 from setting the AB trigger during B7HO. Hold bit drive causes bit drive B to remain unchanged for two consecutive bit timings; in this manner the bit drive is synchronized for the next bit ring cycle.

During drum operation the output of the B7HO trigger, hold bit drive, is inhibited if the drum BS control trigger is set. The BS control trigger output causes the bit ring to step from B7 time and drive B to drive A. If drive A is present following B7 and drive B, the bit ring is conditioned to produce the B0 output rather than the BS output.

The bit-sync control circuit, with the BS control trigger set, gates B0 as an alternate BS; therefore, B0 and alternate BS occur simultaneously (Figure 111). Although the alternate BS is never written on the drum, it is needed for 7631 operation and is gated to the BS signal line (ALD page 01.50.05.1).

Because more normal sync-bits are inhibited than are generated, OR-1 of Figure 111 shows the reset conditions for the BS control trigger to show where normal sync-bits are required.

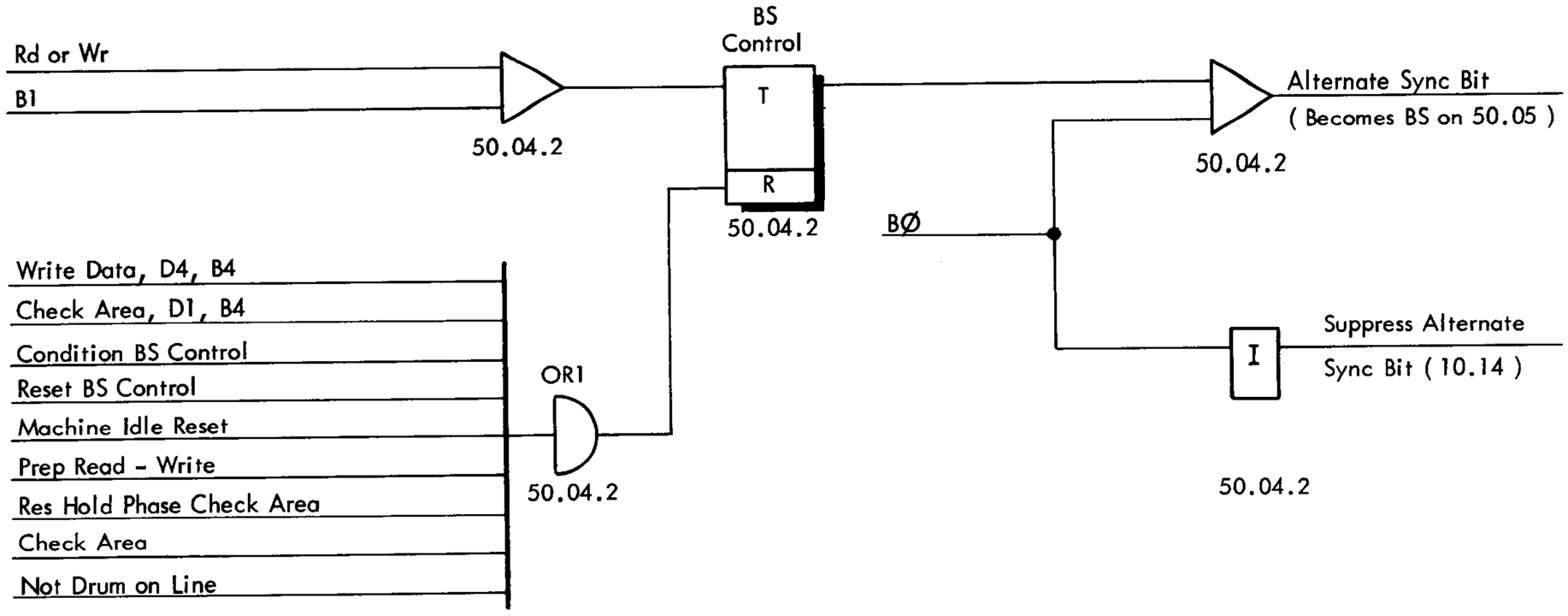


Figure 111. Bit-Sync Control

Missing Sync Bit Detection

- **All drum characters do not have sync bits.**
- **Drum missing sync detection is needed to locate the missing gap that precedes the last character of every address or record.**

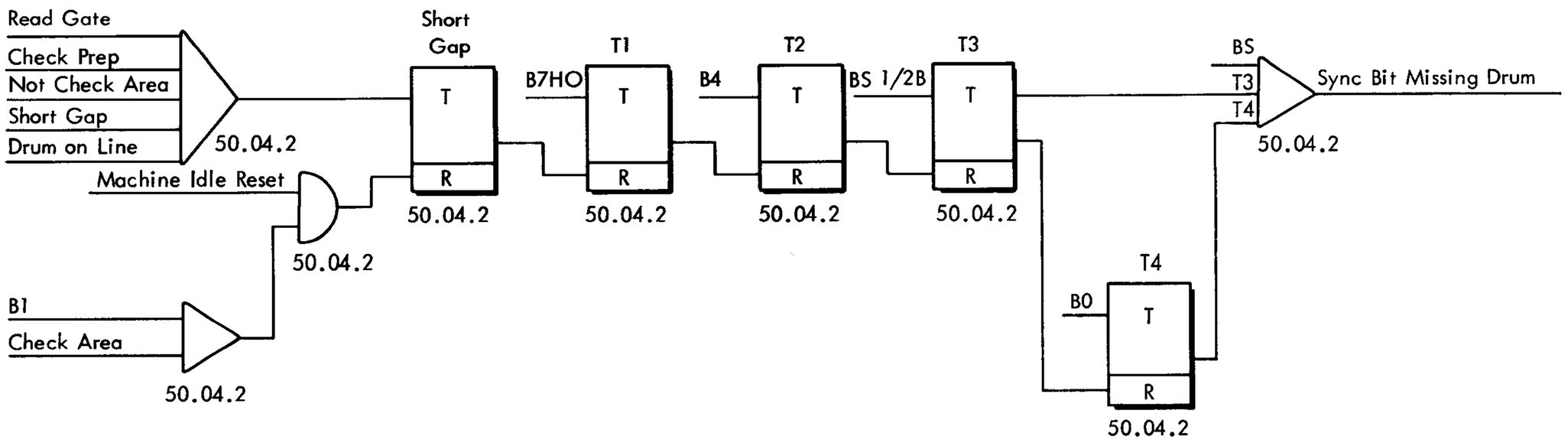
When reading from a 1301, the gap between the main body of an address or record and the last four characters, consisting of the last data character and three check characters, is recognized by sensing a missing sync bit in the gap. The missing sync bit line activates the three zeros circuitry to provide definition of the gap, last data character, and the check characters.

When reading from a drum, more sync bits are missing than are present. Some other means to insure accurate definition of these areas must be used. Five triggers have been added to the drum feature for missing sync detection (Figure 112). The five trigger sequence, started by the format track short gap singleshot output starts the sequence. The sequence uses the timing pulses shown in Figure 112 to locate accurately the missing sync gap that precedes the last character of every address or record area. Once the missing sync signal is generated, check area recognition depends on the action of the three zeros triggers; the operation is exactly the same as the 1301 operation after the missing sync gap is located.

Clock Trigger Control

- **The clock trigger control circuits are only used to read the drum.**
- **Clock trigger control is used to stop bit and digit ring operation to simulate 1301 timing.**

The clock trigger control circuit is used for drum read operations. The block read clock trigger, when set, causes the clock trigger to reset and to prevent further bit and digit ring operation (Figure 113). Because the drum read data phase is stable, the drum phase select circuits are started at the beginning of each address or record area and are not stopped until the end of check area (Figure 110, circled numbers two and three). To simulate 1301 read timing, some means must be provided to stop the bit and digit ring advance in two areas of a drum read operation.



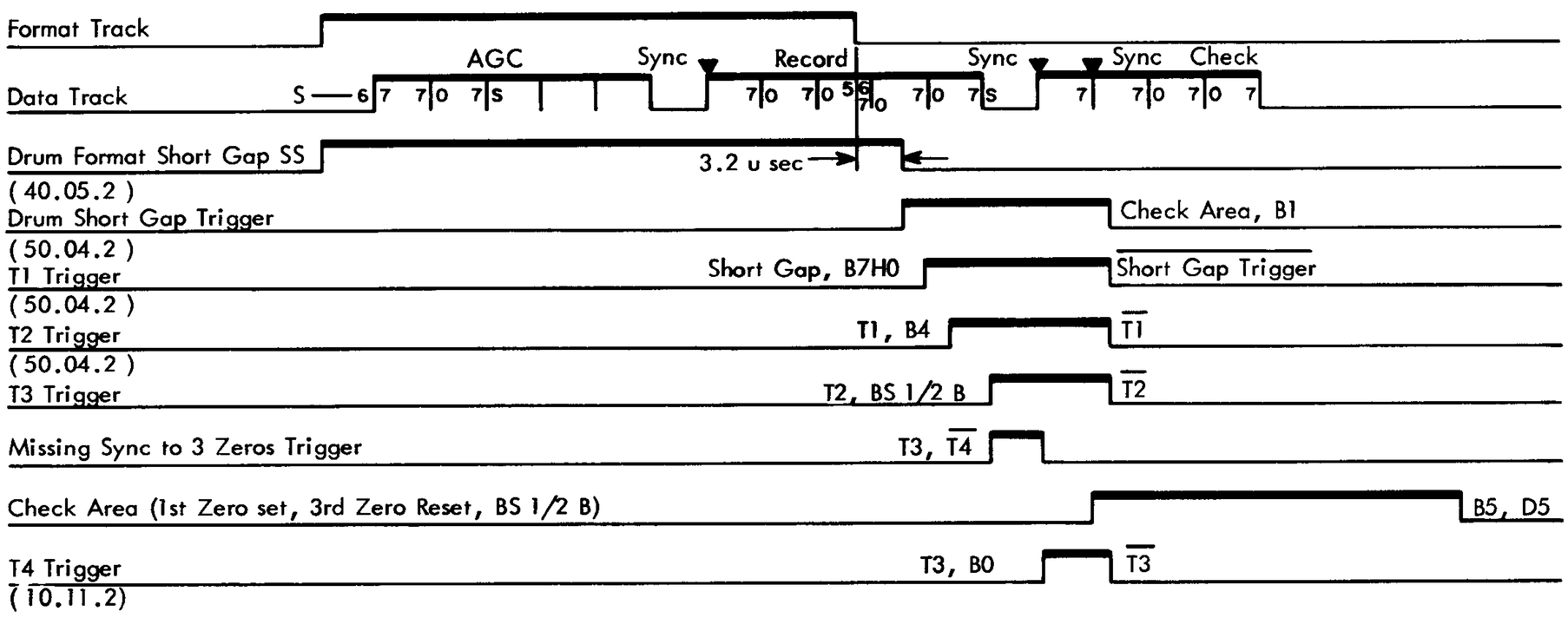


Figure 112. Missing Sync on Read

The first area is the five-character AGC burst where 1301 hold phase timing is stopped at BS of D2 (Figure 114, top line of digit timing). To stop drum bit and digit ring timing at BS of D2, the info search, D1 and drum on-line signals are AND'ed to set the block read clock trigger. The block read clock trigger causes the clock trigger to reset and stop the bit and digit ring advance without disturbing the drum phase pulse generation circuits. Bit and digit ring timing remains at BS of D2 until the first read data bit-sync resets the block read clock trigger. The clock trigger is set with either address or record and check prep signals to restart the bit and digit ring timing after the block read clock trigger reset (Figure 113).

The second area where bit and digit ring advance must be stopped to simulate 1301 read timing is the missing sync gap. (Figure 114, line two, shows the missing sync gap; line one shows the bit and digit ring timing stopped during the gap at BS of D7.) Triggers T2 set and T3 reset provide the signal needed to set the block-read clock signal to suspend until the first read data bit-sync after the gap causes the block-read clock trigger to reset, allowing bit and digit ring timing to resume (Figure 113).

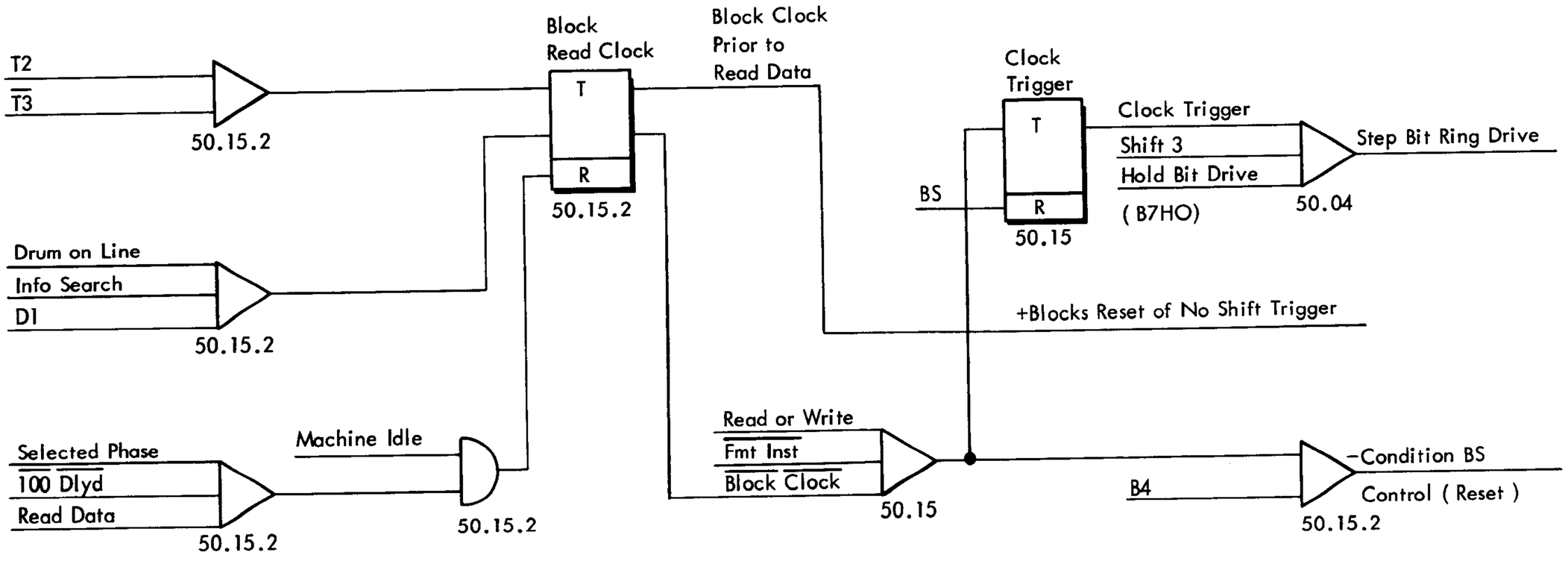


Figure 113. Clock Trigger Control

Skew

- **Drum skew is a fixed delay difference between drum clock and data signals.**
- **The 7320 delay adjustments correct the skew.**

The six-bit displacement between the format and data tracks represents 4.8 microseconds, one drum character of electronic skew: the worst case condition (Figure 114). This displacement occurs because of data write circuit delays. When the data track is written, five circuit delays are added before address or record area is recognized. Additional delay in the turn-on path to the format write ones trigger, line delay to the 7320, and write circuit delays also add to the skew, making the total about two microseconds. This displacement oc-

curs in 1301 operation also, but 4.8 microseconds only represent three bits of 1301 data. The same amount of displacement, 4.8 microseconds, must be considered to read and write correct length drum records and addresses.

While reading the data track, more displacement is added because the format read data path delays are less than the read data path delays. The total read-write displacement, 4.8 microseconds, is shown in Figure 114. The write sequence chart (Figure 115) is shown without any displacement between format and data. Once the write operation starts, the timings are relative.

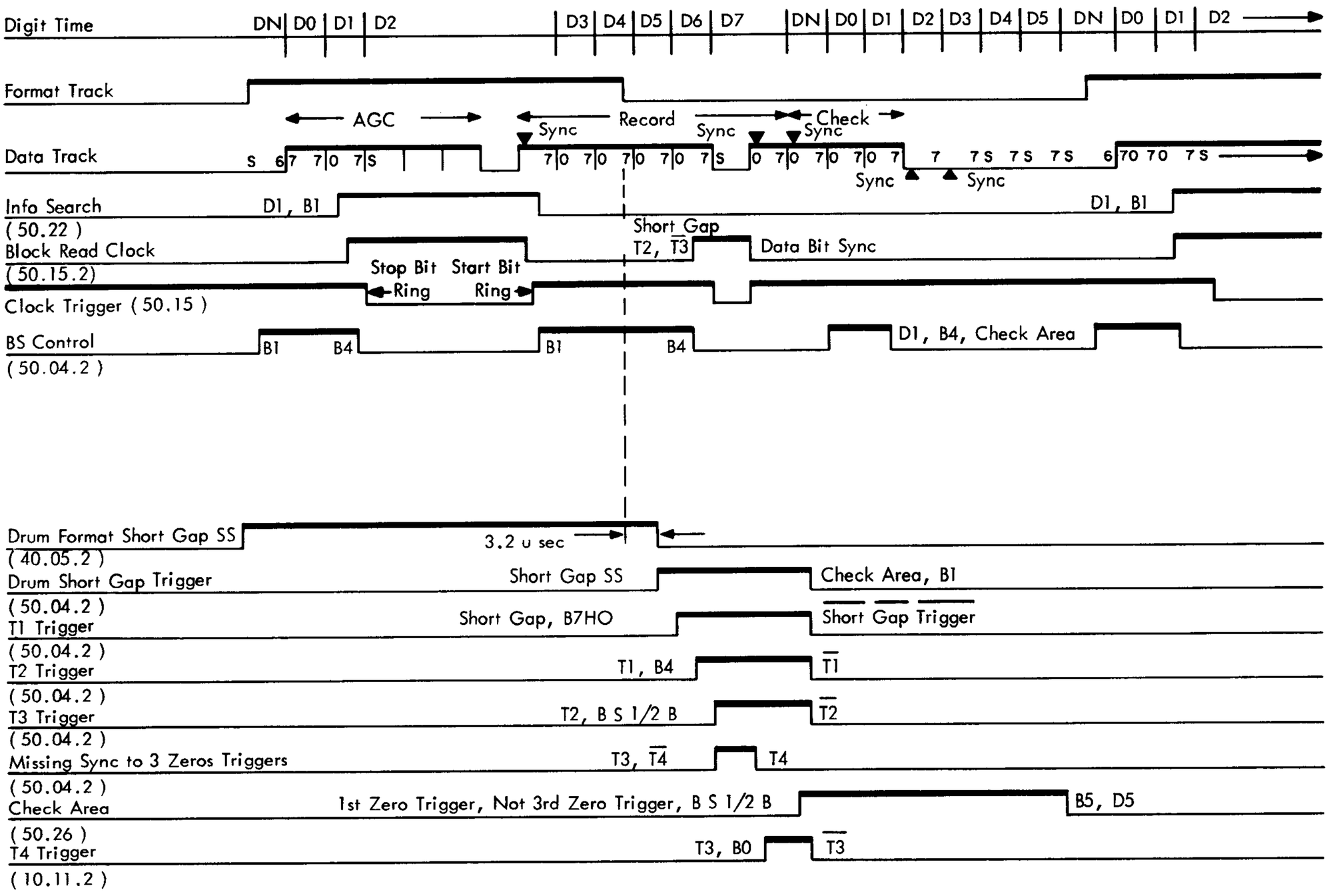


Figure 114. Drum Read Sequence

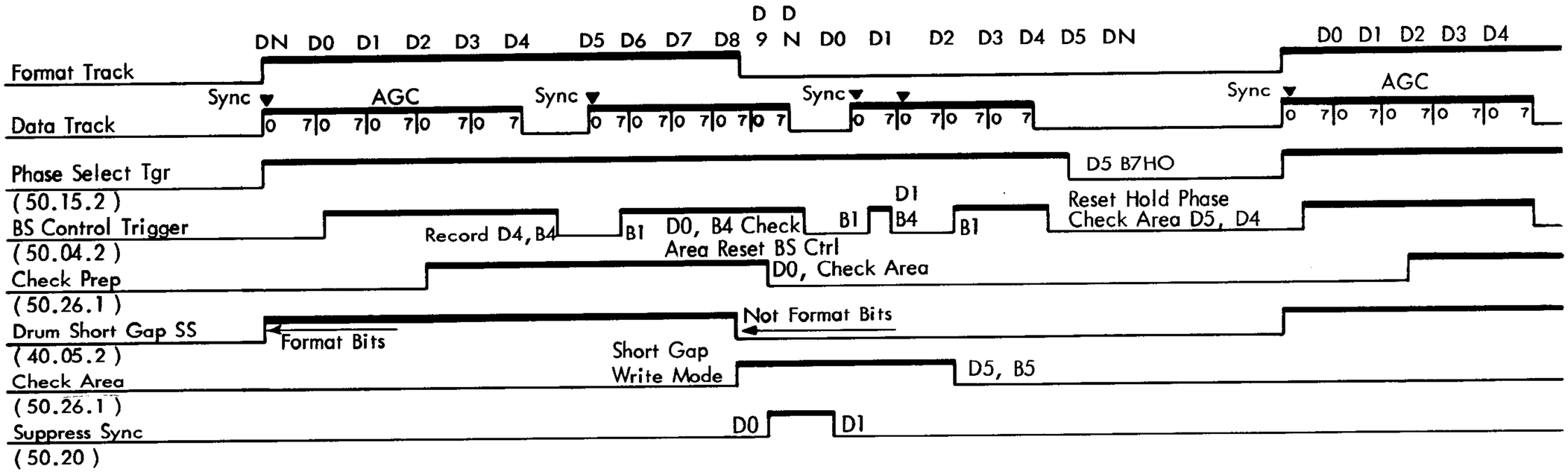


Figure 115. Drum Write Sequence

Clocking

- **7320 clock cycle is 1.6 μs, the same as 1301.**
- **Two 7320 data clockings are generated from each 1.6 μs clock track cycle.**
- **Phases one and three are used as the selected phase.**

The bit rate of the 7320 drum storage unit is twice that of the 1301. Because the frequency of the prerecorded clock track is the same as that of the 1301, two data clocking cycles are generated within each 1.6 microsecond clock timing.

In clocking data from the 1301, the clock cycle is divided into four equal phase timings and one of the four is selected for use. The selected phase pulse is transmitted down the delay line pulse generator which provides all the necessary control pulses for data handling.

In clocking data from the 7320, two of the four phase pulses, one and three, are selected and transmitted down the delay line causing the data handling rate to double (Figure 109).

Read-Write Heads

- **Read-write heads are rigidly mounted.**
- **Data and clock pulse relationships are fixed.**

Unlike the 1301, the 7320 heads are rigidly mounted and do not move. This rigidity assures that the data and clock pulse relationship will not change. When using the 7320, the need for phase selection is eliminated and the simpler phase pulse control circuits are used.

Phase Pulse Generation

- **Phase pulse generation controls phase one and three gating.**
- **Four sync bits are written in each data and related check area.**

The selected phases one and three, or drum bit cycles, start at the beginning of each address or record area and continue under control of the drum phase select trigger until after the check characters are processed. The drum phase select trigger controls the gating of drum bit cycle phase pulses on both read and write operations (Figure 116).

In order to clock data and to allow the read controls to function properly, four sync bits are written in each data and related check area (Figure 115). The first and last characters of each address or record, the first AGC character, and the first character of each check group have sync bits. To insure that the bit ring is in step with the first data character, it is allowed to step to BS and stop in the AGC area (Figure 114). This action is under control of the block clock and clock triggers. When the sync bit of the first data character is sensed, it sets the clock trigger to run the bit ring. There is a time delay between the time the clock trigger receives the turn-on pulse and the time the clock trigger actually turns on and allows the bit ring to be advanced to B0. If the circuits had worse case delay, and the sync bits were not written, the bit ring could not be advanced in time to accept a data bit at B0 time, and would be out of step with the data for the entire record or address. The sync bits are a built-in delay to insure proper operation.

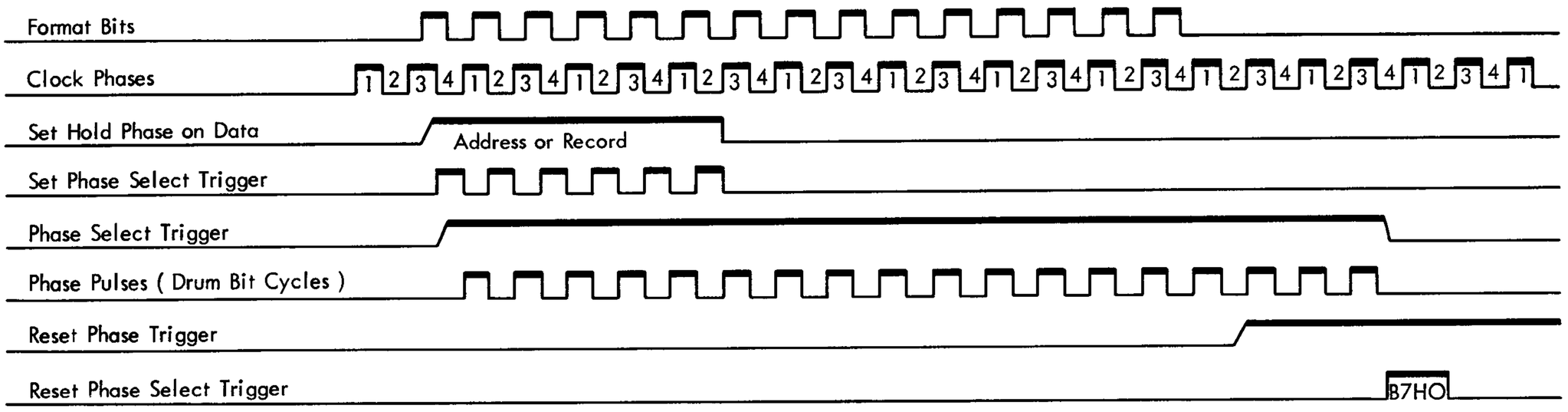


Figure 116. Read-Write Select Phase Pulses

Read Data Sequence

- **7320 drum read timing is the same as 1301 read timing.**
- **Phases one and three are used to read.**
- **Check area ends with D6 forced at D5.**

The 7320 drum read data sequence is the same timing sequence that occurs for 1301 operation. The drum control feature circuits, operating during the drum read sequence, modify the 7631A circuit operation to cause 7320 drum read timing to match 1301 read timing. The following read data sequence listing and figure references establish the sequence of drum control feature circuit operation with respect to a read sequence (Figure 114). The listing calls attention to the specific areas of the drum read sequence where action is required by the drum feature circuits. The listing also applies to the drum verify address cycle because address data must be read from the drum before verification.

1. The phase select trigger is set with address or record area (Figure 109).
2. Clock phases one and three are gated to delay line by the begin drum bit cycle line (Figure 109).
3. The 500-700 delayed output from delay line steps bit ring (Figure 117).
4. At bit one, the BS control trigger is set (Figure 114).

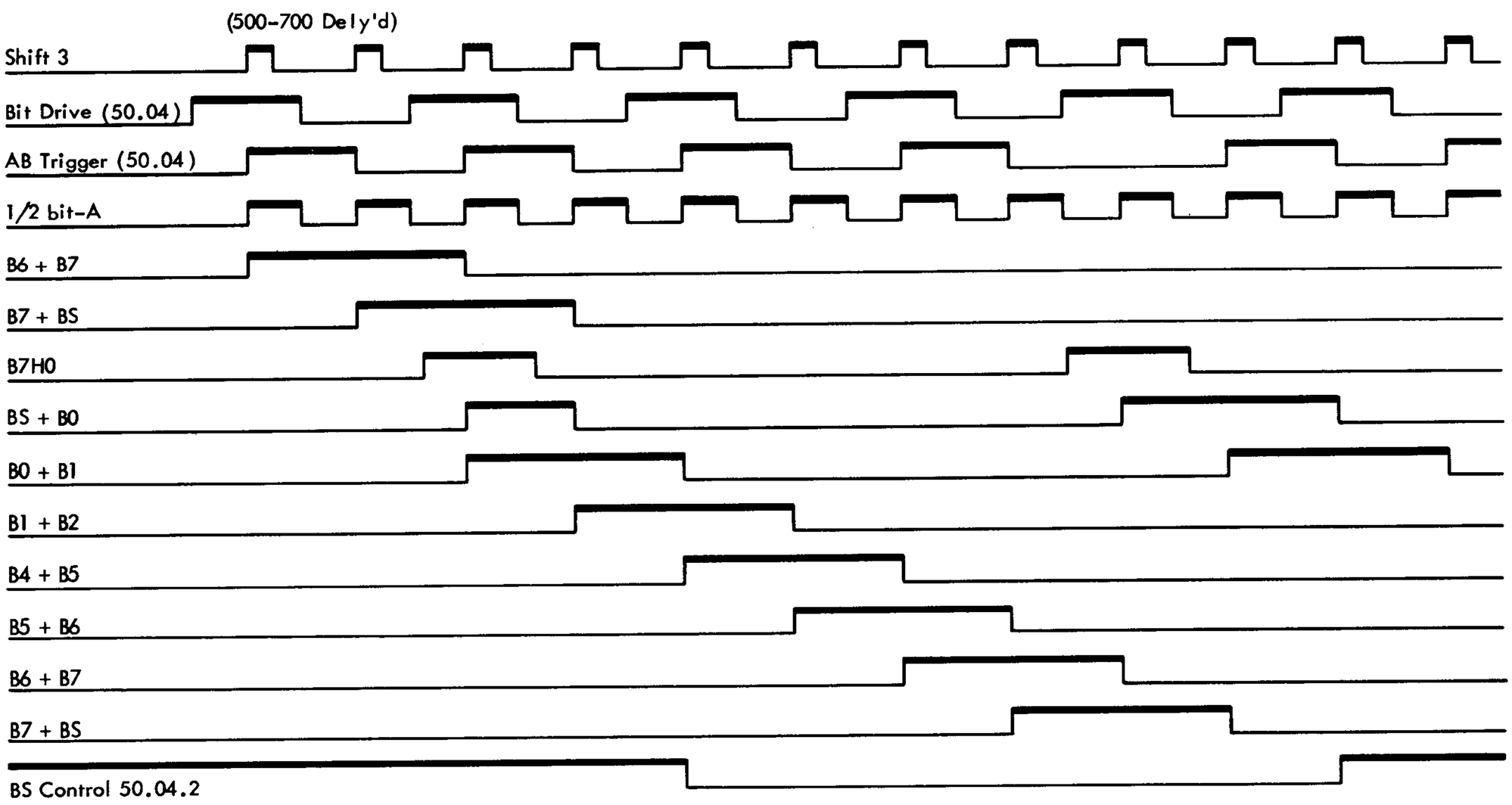


Figure 117. Bit Ring

5. BS control line causes bit ring to skip BS time (Figure 117).

6. The bit ring steps digit ring, and at D1 B1 turns on block read clock trigger (Figure 114).

7. Block read clock trigger allows the clock trigger to reset at the following BS time. The BS control trigger is reset at previous B4 time so the bit ring can step to BS (Figure 114).

8. Bit ring hangs up at BS and the digit ring stops at D2 (Figure 114).

9. The drum data gap detector (01.50.04.2) brings brings up info prep in the AGC gap, and the search for data begins exactly like the 1301 operation.

10. When the first data bit-sync sets data trigger A (01.10.15.1) block read clock trigger is reset (Figure 114).

11. The clock trigger is set.

12. The bit ring timing restarts.

13. Bit sync control is set again and blocks BS (Figure 114).

14. Set of lead and lag control, generation of service requests or data strobe, proceeds as in 1301 operation.

15. Drum format short gap is detected.

16. The short gap trigger is set (Figure 114).

17. Next B7H0 sets T1 to start the missing sync detection circuits.

18. The next B4 sets T2; BS control is reset and block read clock is set (Figure 114).

19. The bit ring steps to BS and stops.

20. When bit ring reaches BS (start of gap), T3 is turned on.

21. The missing sync bit line is simulated and activates three zeros as in 1301 operation.

22. When sync bit of last data character reaches data trigger A, the block read clock trigger is reset.

23. The bit ring starts and the last data character is processed.

24. At BS of first check character (BS control reset), check area is signalled and the BS control trigger is set.

25. Check characters are processed as in the 1301.

26. Check area is reset at D5 B5 rather than D6 B6 as in the 1301 operation.

Write Data Sequence

- **7320 drum read timing is the same as 1301 read timing.**
- **Phases one and three are used to write.**
- **Check area ends with D6 forced at D5.**

The write operation is identical to 1301 operation, with the following exceptions:

1. The phase select trigger is set with address or record area (Figure 114).

2. Beginning drum bit cycle causes clock phases one and three to be gated to delay line (Figure 109).

3. The BS control trigger suppresses the writing of sync bits (Figure 115).

4. Format short gap is recognized by the drum short gap singleshot.

5. Check area is reset at D5 B5 rather than D6 B6 as in the 1301.

Read Data and Read Format Delay Line Adjustment

The 7320 has variable delay lines in the read paths of both format and data. These delays, when adjusted properly, will compensate for variations in the data to clock track relationship. These variations are due to minimum and maximum cable and logic delays in production machines.

Both format and data delay adjustments should be performed after:

a. Initial installation

b. Any changes in the cables between the 7631A and the 7320

c. Any circuit changes, or logic card replacements that effect significant delays in the read or write paths of the 7631A and 7320.

(Refer to pages 02.02.20.1 and 02.02.20.2 in the 7320 Systems and 01.10.15.1 in the 7631A Systems Diagrams.)

Requirements: Tektronix Oscilloscope 535A; Tektronix Pre-Amp, Type CA.

Format Delay Procedure

1. Write the format track on the 7320.

2. Loop the program in a format write-check operation.

3. Observe output of data trigger A at 1G09F and −Y sample data trigger signal at 1G09E of the 7631A

in the middle of a long burst of one bits. Both are negative going signals (Figure 118).

4. Adjust the format data delay line in the 7320 so that the leading edge of the data trigger A signal is 450 ± 30 ns before the trailing edge of the −Y sample data trigger signal. Use the ten percent transition point as a time reference. The adjustment is made by selective placement of the back panel jumper on the delay card. The delay times for the different jumper positions are given in note one in Systems 02.02.20.2. Be sure not to disturb the format pulse-forming delay line by mistake.

Read Data Delay Procedure

Each of the 400 data heads has different delay characteristics. This adjustment is made so that a head having a delay midway between that of the fastest and the slowest heads will have a specified delay; then, all other heads meet requirements. Since no head having the exact midpoint delay necessarily exists, the head to be used and the adjustment figure must be calculated as in step one.

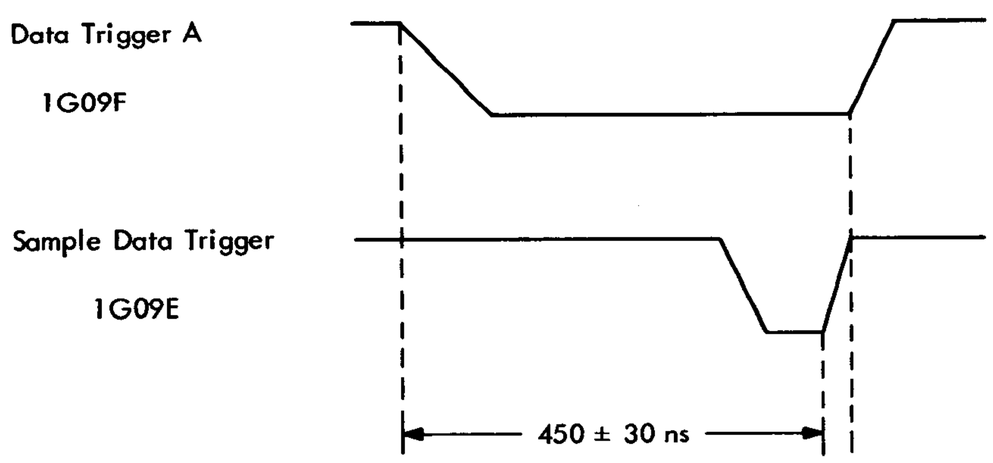


Figure 118. Read Delay Adjustment

1. Referring to page 02.01.63.0 of the 7320 Systems, obtain the maximum head to head delay variation, and divide by two to get the midpoint head delay time. Obtain the delay time of any one of the ten heads given in the table that is closest to the midpoint delay time. Subtract head delay from midpoint delay and add the difference to 450 ns to obtain the adjustment figure. (If head delay is greater than the midpoint delay, subtract the difference from 450 ns.)

For example:

a. Maximum head to head variation	300 ns	SD 02.01.63.0
b. Midpoint delay time	150 ns	(half of item 0)
c. Cyl. 0, Head 00 delay time	130 ns	SD 02.01.63.0
d. Difference of midpoint delay time to Cyl. 0, Head 00 delay time	+ 20 ns	(item b minus item c)
e. Midpoint adjustment figure	450 ± 30 ns	
f. Cyl. 0, Head 00 adjustment figure	470 ± 30 ns	(item e plus item d)

2. Write HA1's on all tracks.

3. Loop the program on read HAO using the selected head.

4. Observing 7631A pins 1G09F and 1G09E in the middle of a long burst of one bits (Figure 118), adjust the read data delay line in the 7320 for the adjustment figure obtained in 1, ±30 ns from the leading edge of data trigger A to the trailing edge of the sample data trigger signal.

The control panel of the 7631 is primarily intended for maintenance simulation purposes. The panel is mounted on the right front cover of the frame. It has an exposed section and a hidden section intended for customer engineering usage. Indicator lights on the exposed section reflect the status of data and controls within the 7631. Operator switches are located in a light-and-switch assembly above the indicator lights (Figure 119). The CE section of the panel is covered and contains switches for simulation of data, commands and responses from the channel, and responses from the files (Figure 120).

Operator's Switch and Light Panel (Figure 119)

Power On Switch: depressing this switch causes the following:

1. Applies +12 and −12 volts DC to the IBM 7631.
2. Applies DC voltages to the IBM 1301's if they are set in the CE remote power control.
3. Causes the blower motor in the 7631 to rotate.
4. Sequences AC power to the drive motors and hydraulic power supplies on all 1301 units connected to the 7631 one at a time. When AC power of the first 1301 is sequenced up, the power sequencing to the second 1301 starts. The sequence continues until AC power is applied to all 1301 units connected to the 7631.
5. Depressing this switch with DC power down brings up DC power on the 7631 and 1301.

DC On Light goes on when DC power is on in the 7631.

Power On Light goes on when AC power is on in the 7631 and the 1301 is in the remote status.

Power Off Switch removes DC and AC power from the 7631 and 1301 (if the 1301 is in remote status) except the 24 volts AC. The 24 volts AC power is removed from the 7631 when the power plug is removed from the wall receptacle or when the main line circuit breaker is thrown off.

HAO Switch allows the execution of the home address operation.

Write Inhibit Switch allows the file control to simulate writing without actually writing on a 1301 file unit.

Write Inhibit Light is on when the write inhibit switch is in the on position.

Test Mode Light is on when the rotary switch on the CE panel is in TM1 or TM2 position.

DC Off Switch removes DC power from the 7631 and all connected 1301's in the remote status.

Thermal Light indicates that the thermal switch control has caused DC power to be removed from the machine. It also lights if the logic gate temperature exceeds 115°F. (The thermal light is on when power is first applied.)

Fuse light indicates that the tripping of AC circuit breaker CB2 has caused DC power to be removed from the machine. The blowing or removal of either of the 1.6 ampere blower fuses stops the blower motor.

NOTE: the 208/24 volt transformer is fused with 0.5 ampere slow-blow fuses. When the file control is off-line, power cannot be brought up unless plugs (IBM P/N 553298) are in the two right-hand emergency interlock receptacles on the tailgate.

Customer Engineering Test Panel and Machine Indicating Lamps (Figure 120)

1410 and 7000 Switches

Block Oscillator Switch prevents the oscillator from driving the bit ring. This switch is activated to drive the bit ring with the single step or single cycle switch.

Block Parity Switch prevents parity errors. This switch permits use of the bit switches without assigning correct parity.

Reset I-O Register Switch causes the I-O and serial registers to reset. This switch is available on 7631 models 2, 3, and 4.

Single Step Switch allows the bit ring to advance one-half bit each time the single step switch is activated up or down. At the end of each bit ring cycle the digit ring advances one digit if the digit ring run lamp is on.

Single Cycle Switch causes the machine to advance through a complete cycle of the bit ring and advance the digit ring one digit if the digit ring run lamp is on.

Rotary Switch in the TM2 position simulates the computer and file lines to the file control. The TM2 position tests the file control by itself. This switch in the TM1 position allows simulation of the computer lines to the file control. The TM1 position tests the file control with a file. The switch in the normal position is for operation of the file control with a computer and a file. All the CE panel switches except mach reset, write CE track, and HAO must be in the normal position when the CE panel rotary switch is in the N position.

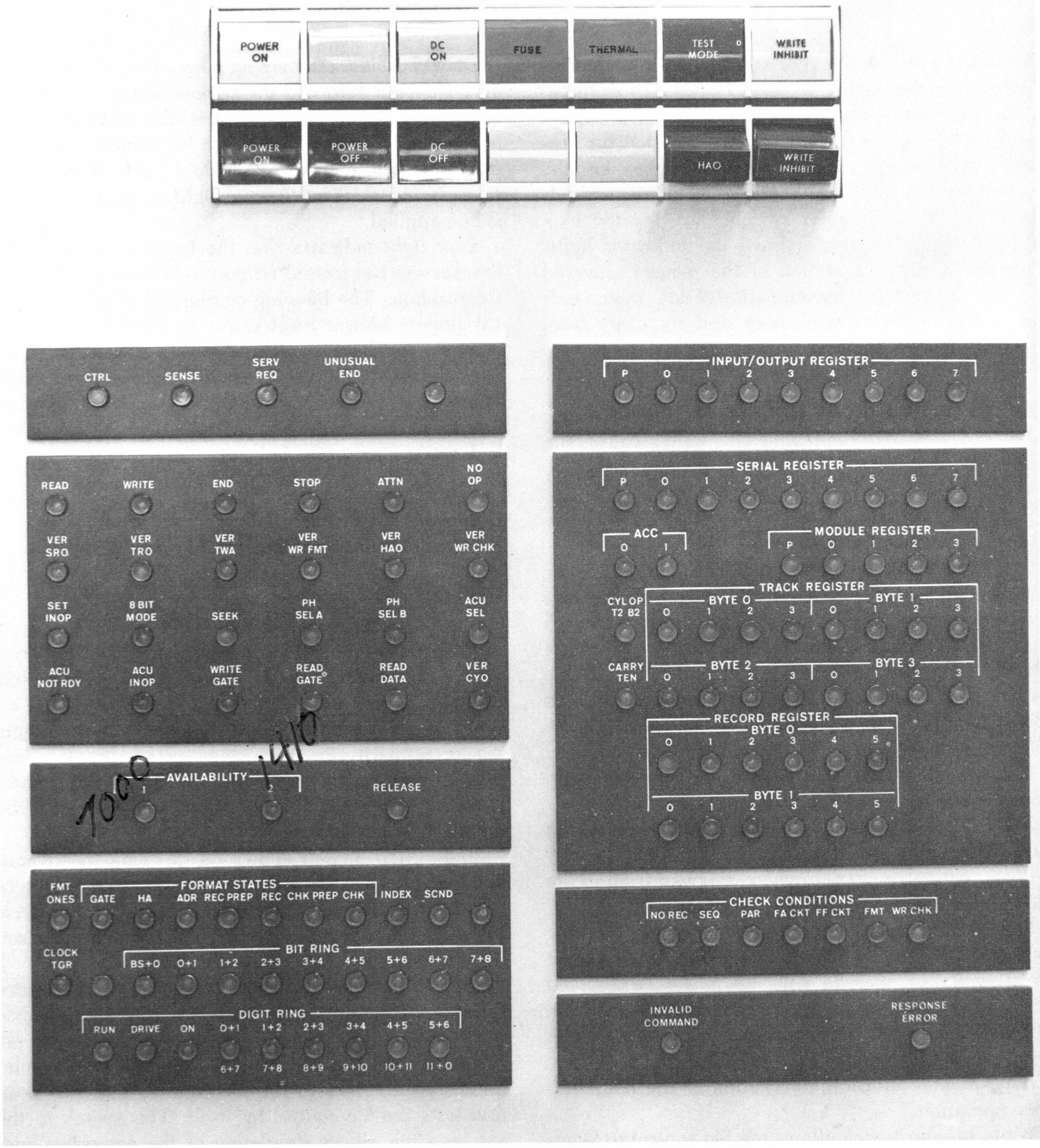


Figure 119. Operator's Switch and Light Panel

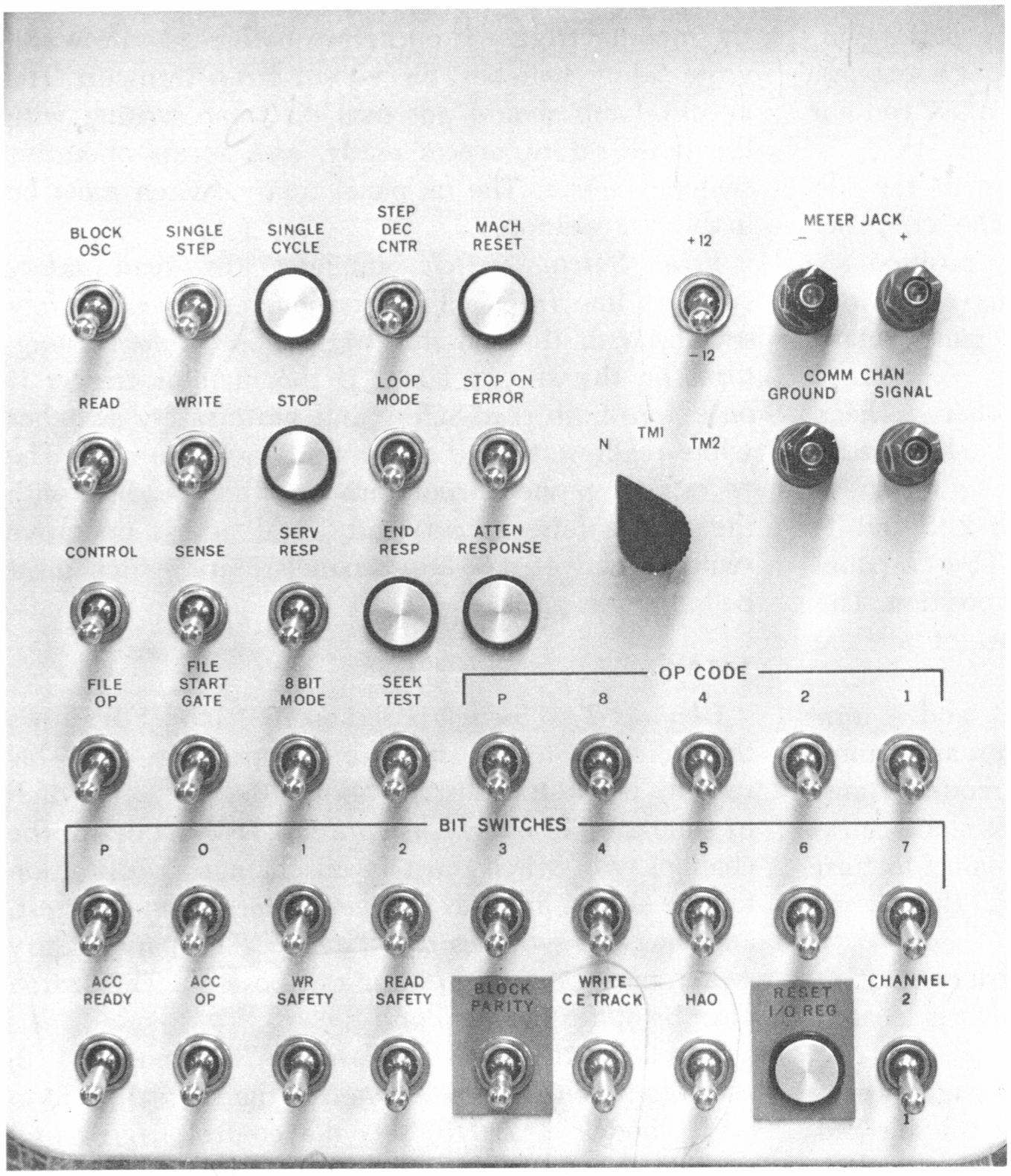


Figure 120. Customer Engineering Test Panel

Step Decimal Counter Switch (Step Dec Cntr): (This switch is used on machines with the CYO operation.) Activating this switch allows single-stepping of track registers T2 and T3 until the number 39 is indicated on the CE panel. The CE panel rotary switch must be in the TM1 and TM2 position and the block oscillator switch must be activated. Each flip of the single-step switch advances the counter one step.

Machine Reset resets all triggers in the file control to their initial condition. If the file control is in eight-bit mode, it will change to the six-bit mode.

Read Switch allows reading in the following modes: home address (HAO), track without addresses(TWA),single record operation (SRO), track operation (TRO), and cylinder operation (CYO) (optional feature).

Write Switch allows writing in the following modes: home address (HAO), track without addresses (TWA), single record (SRO), track (TRO), CYO (optional feature)

and format (the format operation can be performed, but a valid format cannot be written without a system). When write checking, the bit switches must contain the same character as read data.

Stop Switch terminates the data flow in the file control and turns on the stop lamp. The CE panel rotary switch must be in the TM1 or TM2 position.

Loop Mode Switch allows continuous repetitions of the read or write functions. The CE panel rotary switch must be in the TM1 position.

Stop On Error stops the file control when a check condition occurs. The CE panel rotary switch must be in the TM1 or TM2 position.

Control Switch (Used on 7631 models 2, 3 and 4) turns on the control trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The control switch allows manual operation of all the orders under the control command.

Bit Switches on the 7631 models 2, 3, and 4 turn on their respective input register trigger and lamp. The zero-bit switch is not used on 7631 models 1 and 5. These switches activated on the 7631 model 1 cause its respective serial register trigger and lamp to turn on. The CE panel rotary switch must be in the TM1 or TM2 position.

Write CE Track Switch allows reading or writing on a 1301 inner or outer CE track, if the access is located at either of these tracks.

HAO Switch allows reading or writing the physical HA1, HA2, record addresses and records of the selected head and track with the operator panel HAO switch activated.

+12 and −12 Volt Switch: This switch in the −12 position causes −12 volts to appear at the (−) meter jack and ground to appear at the (+) meter jack. This switch in the +12 position causes ground to appear at the (−) meter jack and +12 volts to appear at the (+) meter jack.

Access Ready Switch simulates file ready signal from a file. If this switch is activated before the monitor trigger is turned on during a control, read, or write operation, the file frame circuit check (FF CKT) lamp turns on. If this switch is activated after the monitor trigger is on, the ACU not ready check cannot occur. The CE panel rotary switch must be in the TM2 position.

Access Operative Switch simulates an access operative line from a file. If this switch is activated after the monitor trigger is on, the ACU not ready check cannot occur. The CE panel rotary switch must be in the TM2 position.

Write Safety Switch simulates the write safety line from a file. The activated read safety switch, with the monitor trigger on when writing, turns on the file frame circuit check lamp (FF CKT). When writing, if the monitor trigger is on before both read safety and write safety switches, the FF CKT lamp turns on. The FF CKT lamp should not turn on when writing with the write safety, access ready, and access operative switches active. The CE panel rotary switch must be in the TM2 position.

Read Safety Switch simulates the read safety switches line from a file. The activated write safety switch, with the monitor trigger on while reading, turns on the FF CKT lamp. If the monitor trigger is on before both read safety and write safety switches while reading, the FF CKT lamp should turn on. The FF CKT lamp should not turn on when reading with the read safety, access ready, and access operative switches activated. The CE panel rotary switch must be in the TM2 position.

1410 Switches

Channel Two Switch (Used on 7631 model 3) allows the file op switch to simulate file operation one. This switch, when transferred, allows the file op switch to simulate file operation two. On 7631 model 3, the channel two switch must be in channel two position for the file op, file start gate, eight-bit mode, seek test, and op code switches to be active. The panel rotary switch must be in the TM1 or TM2 position. The switch must be off for models 1 and 5.

File Operation Switch (Used on 7631 models 1, 3, and 5) with channel two switch in the normal position (7631 models 1 and 5) sets the control trigger and permits the available one lamp to turn on. In 7631 model 3 this switch activated, with channel two switch transferred, sets the control trigger and allows the available two lamp to turn on. The CE panel rotary switch must be in the TM1 or TM2 position for the above conditions.

File Start Gate Switch (Used on 7631 models 1, 3, and 5) sends the file start gate to the file control. This switch, used in conjunction with the file op switches, allows completion of the control instructions. The CE panel rotary switch must be in the TM1 or TM2 position. The channel two switch must be in the channel two position for 7631 model 3.

Eight-Bit Mode Switch (Used on 7631 models 1, 3, and 5) causes reading and writing in the eight-bit mode. The eight-bit mode lamp turns on. The CE panel rotary switch must be in the TM1 or TM2 position. The channel two switch must be in the channel two position for the 7631 model 3.

Seek Test Switch (Used on 7631 models 1, 3, and 5) simulates a system CPU to the file seek test. This switch, used in conjunction with a seek operation, prevents the file access mechanism from moving, turns on the end op trigger and prevents the VER SRO, VER TRO, VER TWA, and VER HAO triggers from being reset. The CE panel

rotary switch must be in the TM1 or TM2 position. The channel two switch must be in the channel two position for 7631 model 3.

Op Code Switches (Used on 7631 models 1, 3, and 5) allows the proper control operation trigger to turn on. The file start and control triggers must be on and the CE panel rotary switch must be in the TM1 or TM2 position. The channel two switch must be in the channel two position for 7631 model 3.

7000 Switches

Control Switch (Used on 7631 models 2, 3, and 4) turns on the control trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The control switch allows manual operation of all the orders under the control command.

Sense Switch (Used on 7631 models 2, 3, and 4) turns on the sense trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The sense switch allows the data of the ten four-bit bytes of error and attention information to transfer from the status latches to the serial register and then to the I-O register.

Service Response Switch (Used on 7631 models 2, 3, and 4) simulates the computer service response. This switch allows the resetting of the service request trigger and lamp. The CE panel rotary switch must be in the TM1 or TM2 position. The service response switch, when the rotary switch is in TM1 position, allows the gating of write data through the file control.

End Response Switch (Used on 7631 models 2, 3, and 4) resets the four basic command triggers of read, write, control, and sense; the end trigger; and the unusual end trigger. The CE panel rotary switch must be in the TM1 or TM2 position.

Attention Response Switch (Used on 7631 models 2, 3, and 4) resets the attention one and two triggers and the attention lamp. The CE panel rotary switch must be in the TM1 or TM2 position.

Communication Channel Jacks

Ground always appears at the ground test jack. A sync signal sent from the file appears at the signal jack.

CE Panel Operating Instructions (Test Mode One)

If an error is made while performing any operation from the CE panel, turn all switches off, push machine reset and restart at step 1.

7631 Model 1 or 5 CE Panel Operating Instructions (TM1)

Address Transfer Cycle

1. Set rotary switch to test mode 1 (TM1).
2. Set block osc switch on.
3. Set op code switches.
4. Set file op switch on.
5. Press single cycle button until the digit ring does not step (two depressions of button).
6. Set file start gate up and then down.
7. Set access byte into bit switches.
8. (a) Press single cycle button until access register is set (three depressions of button). (b) Press single cycle until module, track and record register are set (change bit switches as desired for each byte).

To Read or Write After Address Transfer

9. Set read or write switch on.
10. Set loop mode switch on.
11. Set file start gate up.
12. Choose mode required (six-bit or eight-bit).
13. Set bit switches for character to be written (write operation only).
14. Set clock osc switch off.
15. Stop on error on if desired.

To Return to On Line Operation

1. Set all toggle switches down.
2. Press machine reset button.
3. Set rotary switch to normal position (N).

7631 Model 2 and 4 CE Panel Operating Instructions (TM1)

Address Transfer Cycle

1. Set rotary switch to test mode 1 (TM1).
2. Set block osc switch on.
3. Set control switch up and then down.
4. Press single cycle button until service request lights (two depressions of button).
5. Set bit switches up and then down for first byte of op code.
6. Set service response switch up.
7. Press single cycle button.
8. Set bit switches up and then down for second byte of op code.
9. Press single cycle button (repeat steps 8 and 9 until access, module, track and record registers are set).
10. Press single cycle button until end light comes on (two depressions of button).
11. Press end response button.

To Read or Write After Address Transfer

12. Set read or write switch on.
13. Set loop mode switch on.
14. Set bit switches for character to be written (write operation only).
15. Set block osc switch down.
16. Stop on error on if desired (If error occurs, turn off).

17. If needed, push end response to continue looping.

To Return to On Line Operation

1. Set all toggle switches down.
2. Press machine reset button.
3. Set rotary switch to normal (N).

7631 Model 3 CE Panel Operating Instructions Channel 1 (TM1)

1. Set rotary switch to test mode 1 (TM1).
2. Set block osc switch on.
3. Set control switch up and then down.
4. Press single cycle button until service request light comes on (two depressions of button).
5. Set bit switches up and then down for first byte of op code.
6. Set service response switch up.
7. Press single cycle button.
8. Set bit switches up and then down for second byte of op code.
9. Press single cycle button (repeat steps 8 and 9 until access, module, track and record registers are set).
10. Press single cycle button until end light comes on (two depressions of button).
11. Press end response button.

To Read or Write After Address Transfer

12. Set read or write switch on.
13. Set loop mode switch on.
14. Set bit switches for character to be written (write operation only).
15. Set block osc switch down.
16. Stop on error on if desired (If error occurs, turn off).
17. If needed, push end response to continue looping.

To Return to On-Line Operation

1. Set all toggle switches down.
2. Press machine reset button.
3. Set rotary switch to normal (N).

7631 Model 3 CE Panel Operating Instructions Channel 2 (TM1)

Address Transfer Cycle

1. Set rotary switch to test mode 1 (TM1).
2. Set block osc switch on.
3. Set up code switches.
4. Set file op switch on.
5. Press single cycle button until the digit ring does not stop (two depressions of button).
6. Set file start gate up and then down.
7. Press single cycle button twice.
8. Set bit switches up and then down for access byte.
9. Press single cycle button until module, track and record register are set (change bit switches as desired for each byte).

To Read or Write After Address Transfer

10. Set read or write switch on.
11. Set loop mode switch on.
12. Set file start gate up.
13. Choose mode required (six-bit or eight-bit).
14. Set bit switches for character to be written (write operation only).
15. Set block osc switch off.
16. Stop on error on if desired.

To Return to On-Line Operation

1. Set all toggle switches down.
2. Press machine reset button.
3. Set rotary switch to the normal position (N).

Test Mode 2 CE Panel Switches

The following four switches are used when operating the 7631 in test mode 2; the switches simulate the 1301 lines to the 7631. Correct use of the switches requires that 1301 DC power be off.

Access Ready Switch simulates the access ready line from a file. When executing a control or address transfer, the access ready switch should be turned on when the ACU SEL indicator lights (D4 of control or address transfer). If the switch is turned on before ACU SEL, it causes a FF circuit check.

Access Operative Switch simulates the access operative line from a file. When executing a control or address transfer, the access operative switch should be turned on when the ACU SEL indicator lights (D4 of control or address transfer). If the switch is turned on before ACU SEL, it causes a FF circuit check.

Write Safety Switch simulates the write safety line from the 1301. If the write safety switch is turned on during the control (or address transfer) or prep read-write cycles, it causes a FF circuit check.

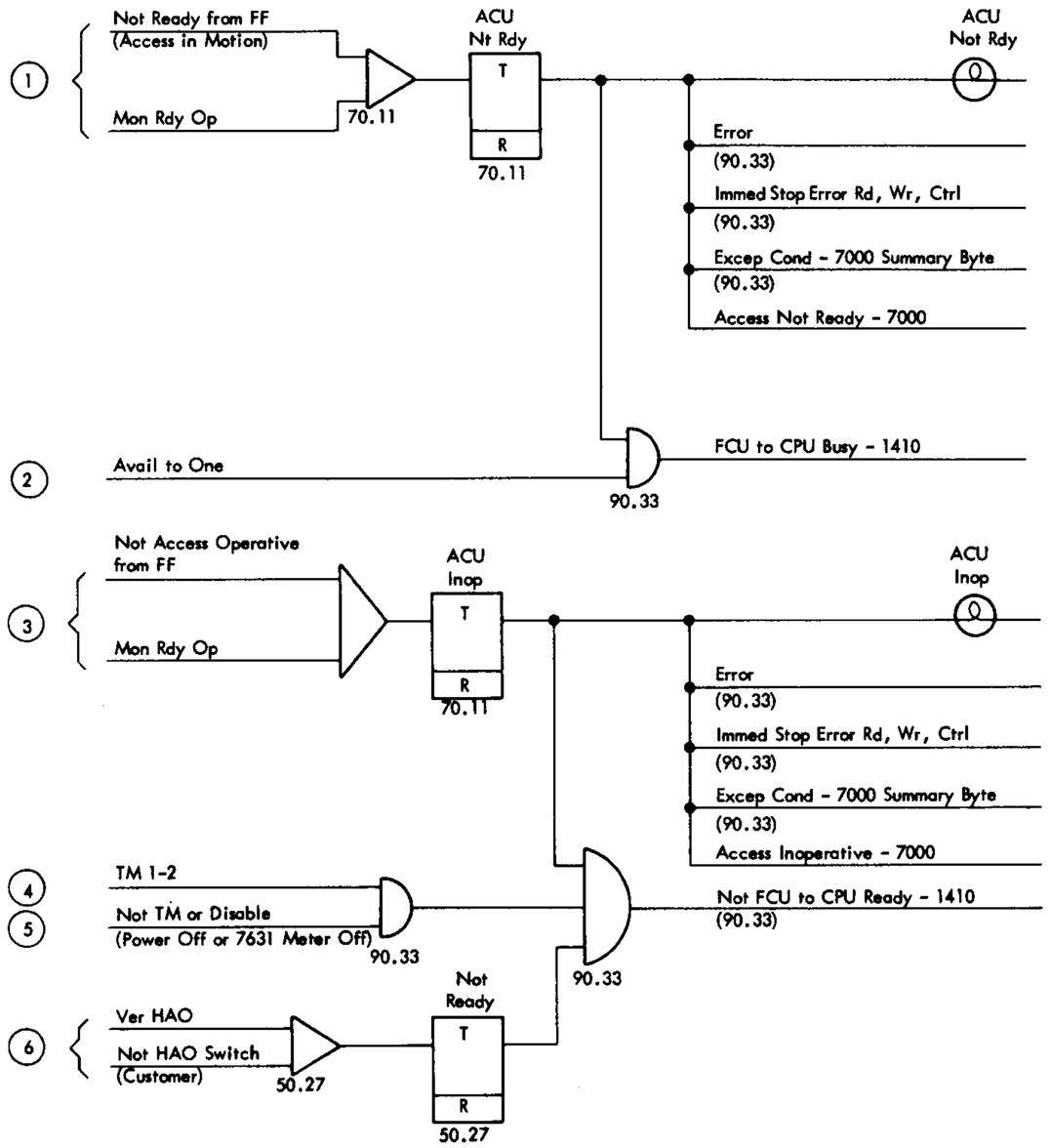
Read Safety Switch simulates the read safety line from the 1301. If the switch is turned off during the control (or address transfer) or prep read-write cycles, it causes a FF circuit check.

1410 Status Conditions

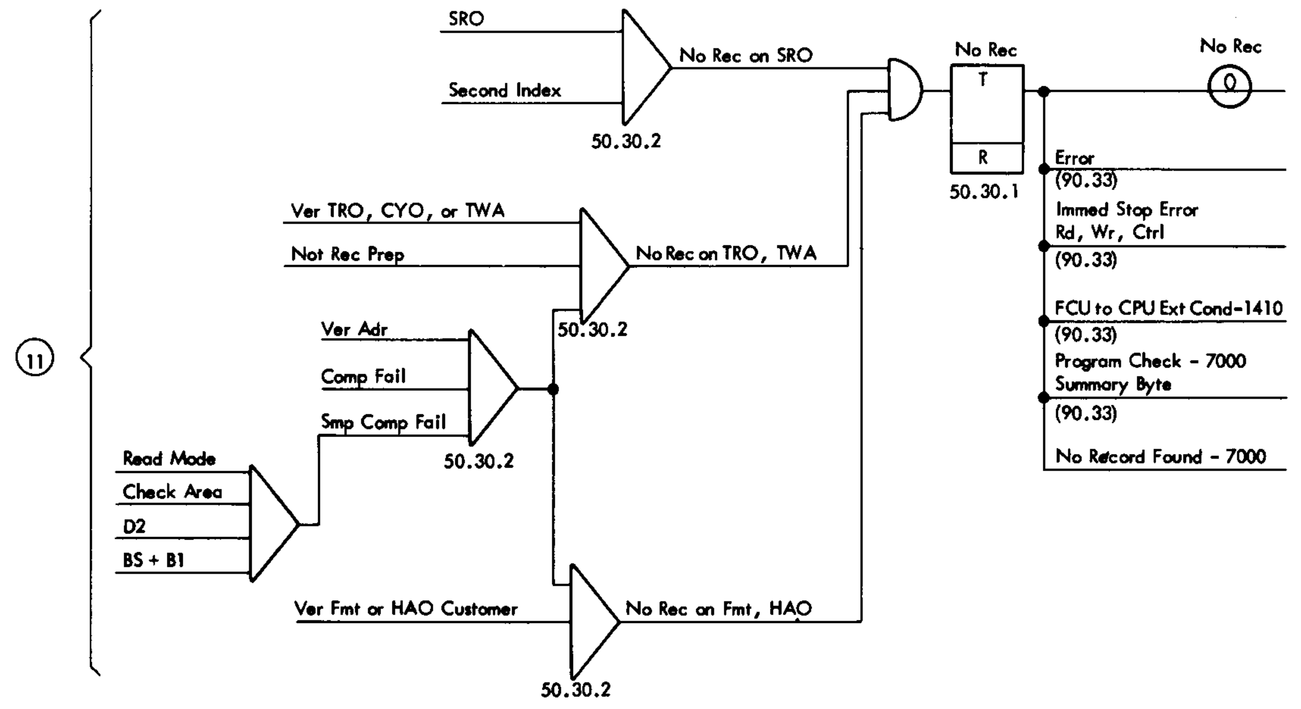
Busy

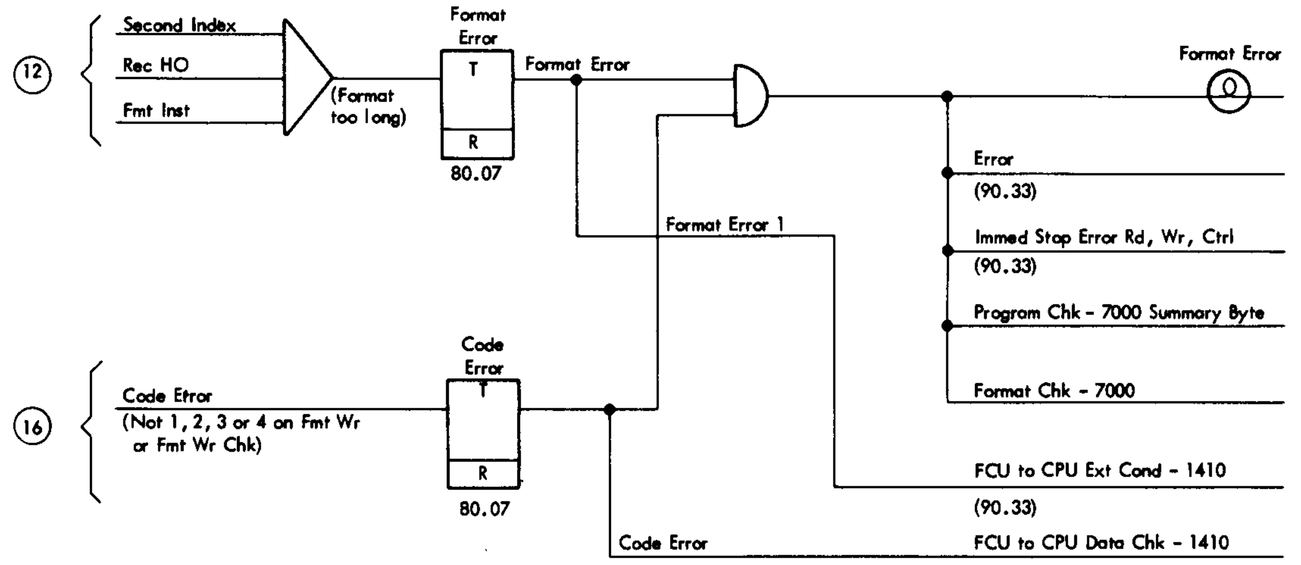
Access not ready (70.11), D9 of control.** (1)
Avail to one (49.01), when 7631 is not released.(2)

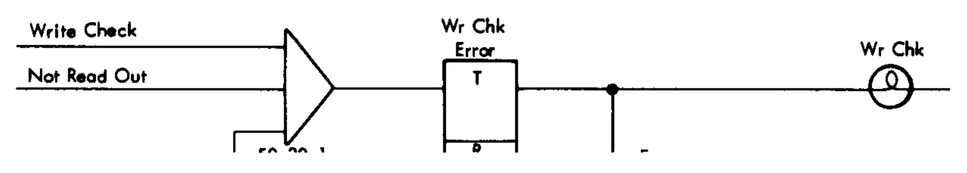
**Each number corresponds to the circled numbers shown on Figure 121.

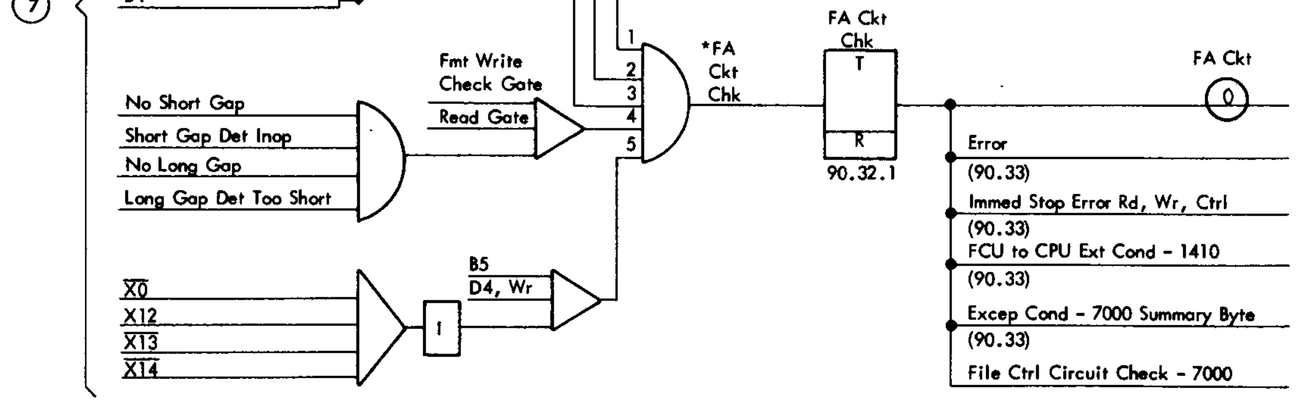


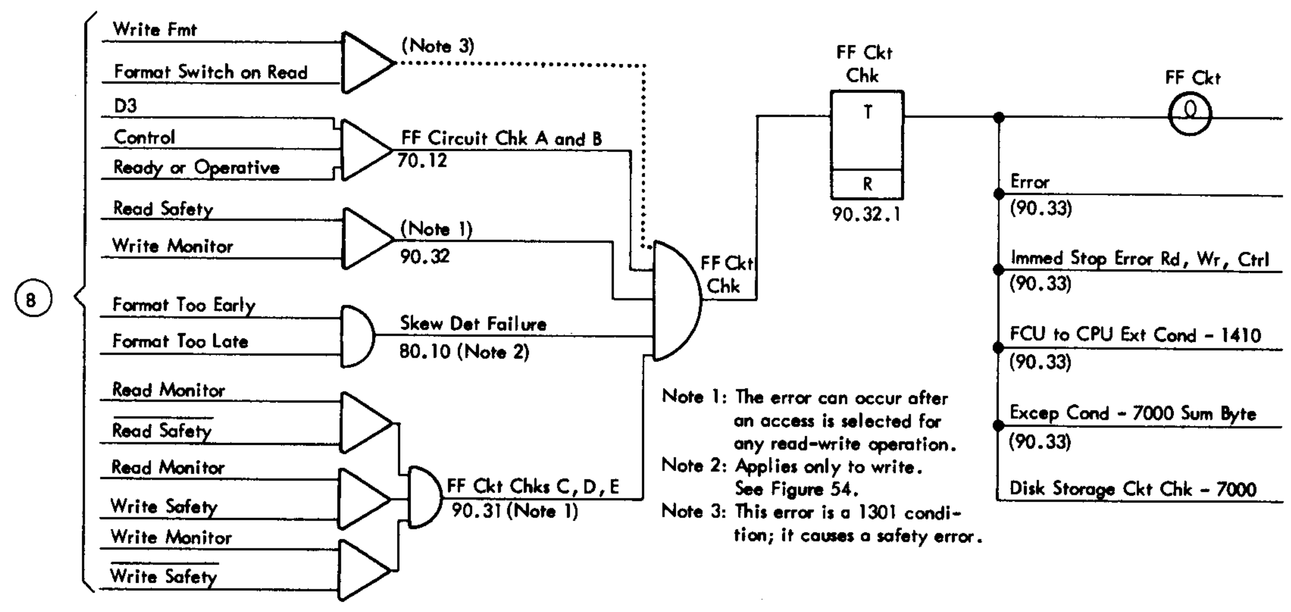
*1. Failure to complete any read or write operation 90.32
*2. a. Skew Detector Failure Format binary counter improperly, stepped 80.10
b. Incorrect bit mode (programming error)
*3. Test Not Compare A and B 50.28
*4. Format Write Check only 80.07
*5. Shift Register Test prior to writing any address or record data 30.06

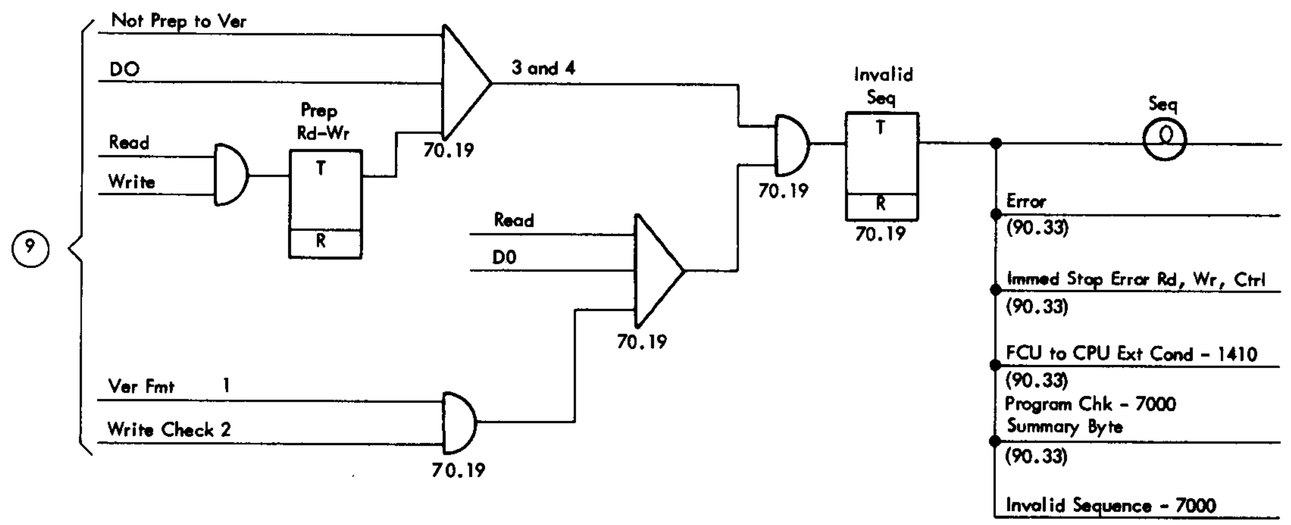






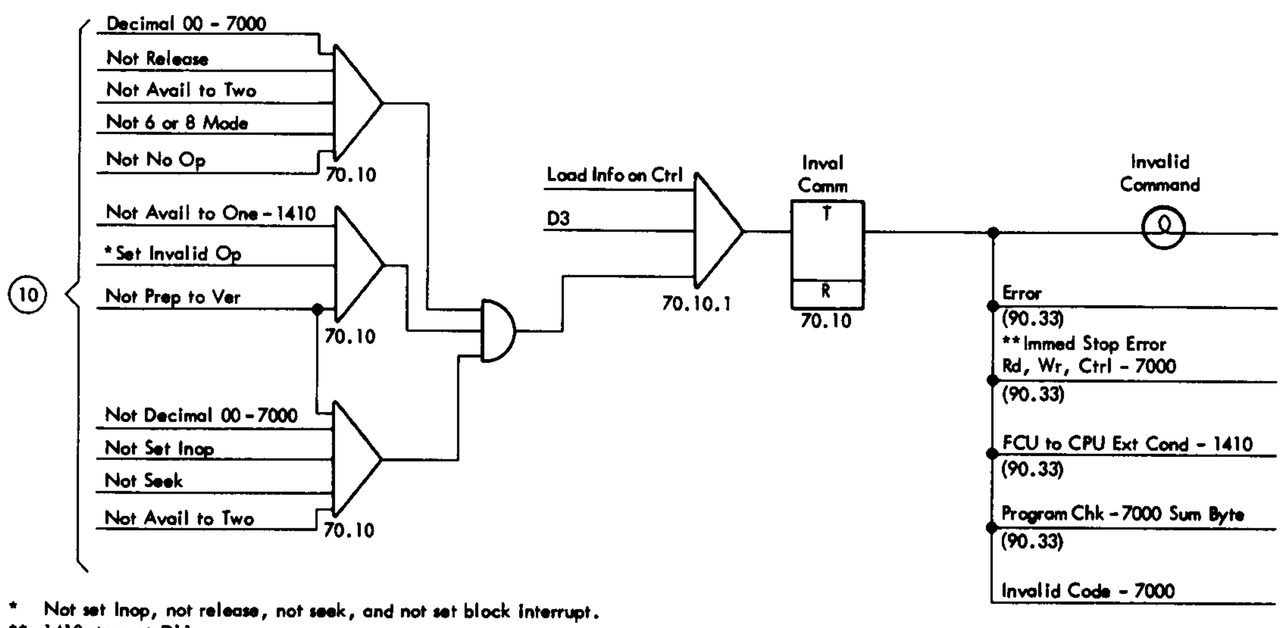






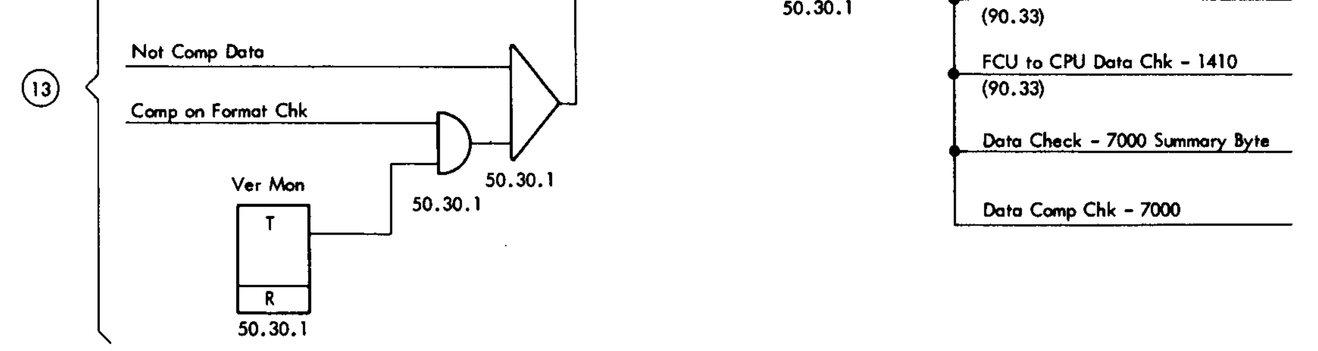
7000
1. Ver Fmt order and a read command.
2. Wr Check order and a read command.
3. HAO order with HAO - Customer switch off.
4. Read or write command without a prepare to verify latch on.

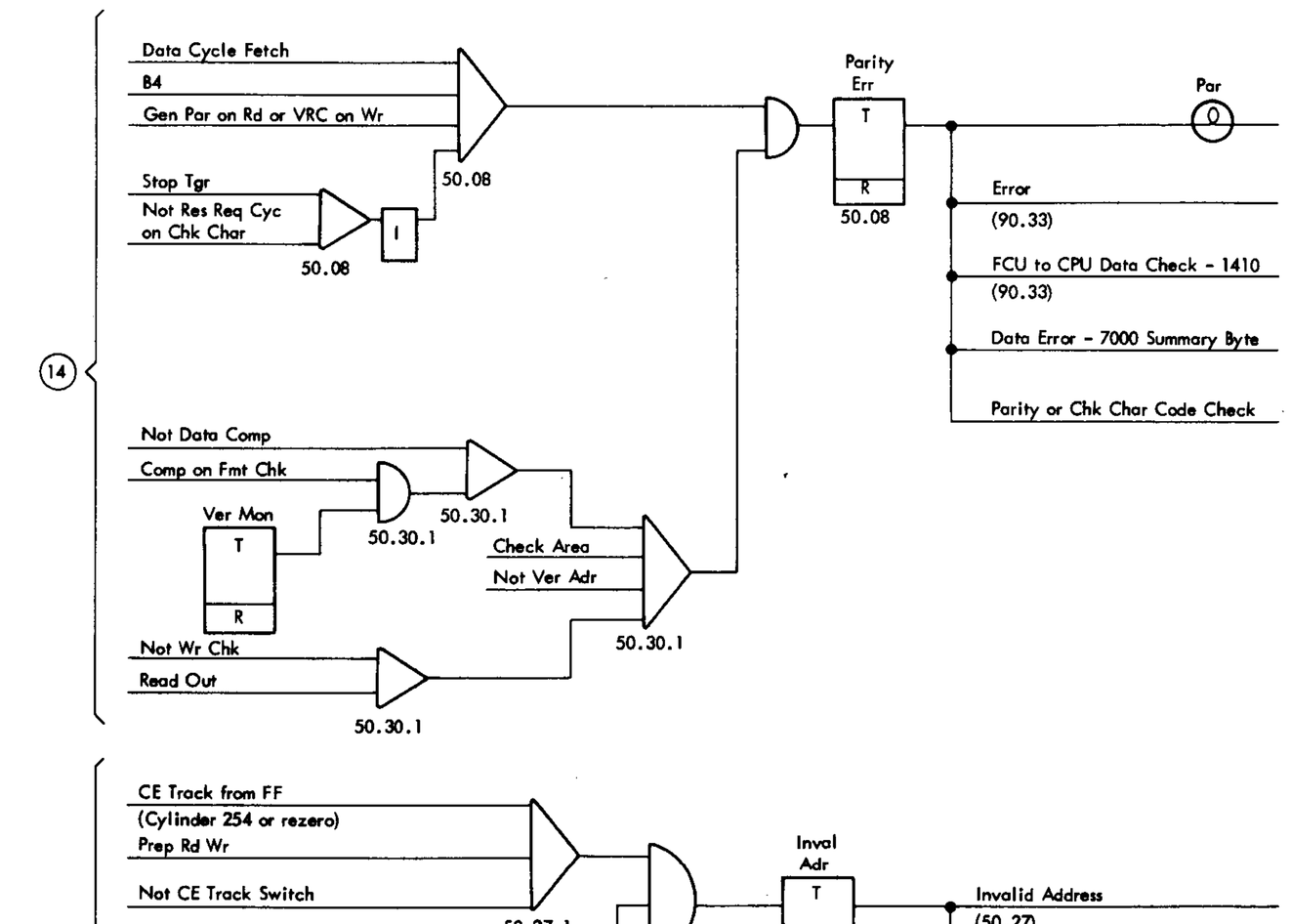
1410
1. Ver Fmt order and a read d-modifier.
2. Wr Check order and a read d-modifier.
3. HAO order with HAO - Customer switch off

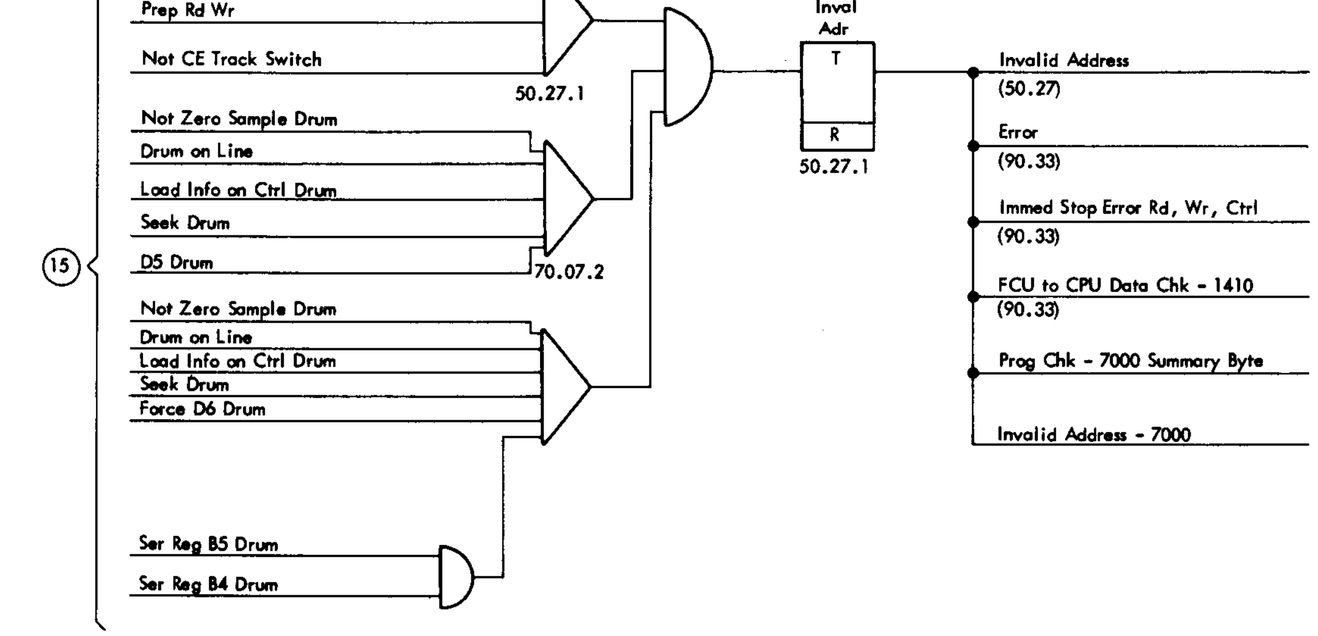


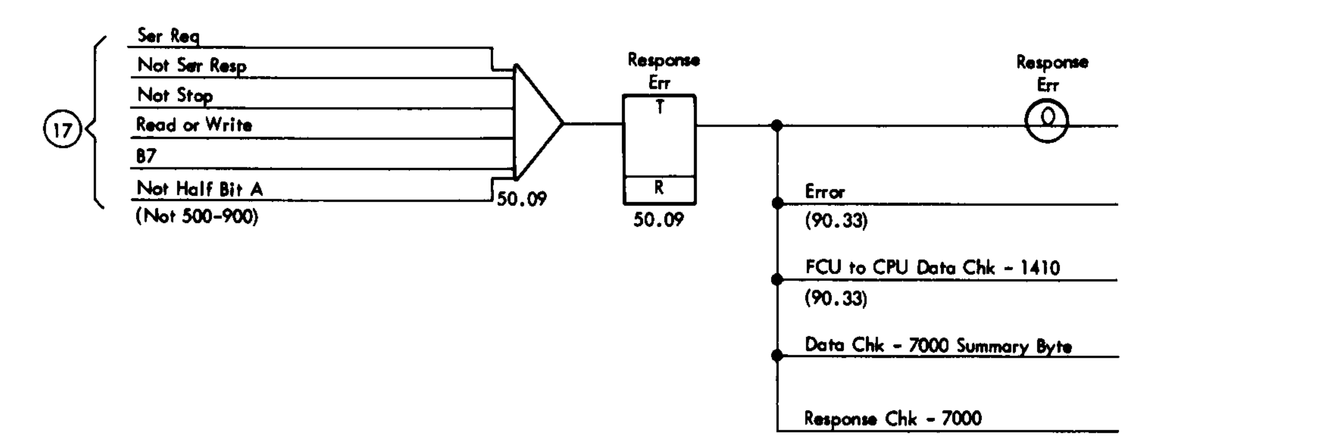
* Not set Inop, not release, not seek, and not set block interrupt.
** 1410 stops at D11.

Figure 121. Error Circuits









Not Ready

7631 power off, active with power off.* (5)
Test mode-CE.* (4)
Access inop (70.11), D9 of control. (3)
HAO Switch off-HAO up (50.27), D2 of Control. (6)

Condition

FA circuit check (90.32). (7)
FF circuit check (90.32). (8)
Invalid sequence (70.19), D0 of prep read-write. (9)
Invalid op code (70.10), D3 of control. (10)
No record found (50.30), D2 of HA1 or HA2 or SRO and second index. (11)
Format error (80.07), write fmt and second index. (12)

Data Check

Data fail (50.30), write check only. (13)
Parity (50.08), input character even or check character on read. (14)
Invalid address (50.27), prep read-write. (15)
Format code error (80.07), write fmt or fmt write check. (16)

7000 Error Conditions

Program Check

No record found (50.30), D2 of HA1 or HA2 or SRO and second index.** (11)
Invalid address (50.27), prep read-write. (15)
Invalid op code (70.10), D3 of control. (10)
Format error—code error (80.07), write format and second index, or write fmt, or fmt write check (12) (16)
Invalid sequence (70.19), D0 of prep read-write. (9)

Exceptional Condition

Access inop (70.11), D9 of control. (3)
Access not ready (70.11), D9 of control. (1)
FA circuit check. (7)
FF Circuit check. (8)

Data Error

Response error (50.09), late or missing response for read or write. (17)
Parity check (50.08), input character even or check character on read. (14)
Data fail (50.30), write check only. (13)

Unusual End

The unusual end signal is issued by the 7631 if any of 7000 error conditions occur. Any error and the read-write done trigger output cause the unusual end.

*Error can occur any time during an operation.
**Each number corresponds to the circled numbers shown on Figure 121.

Singleshot Timings

SYSTEMS PAGE	NAME	NOMINAL DURATION	ACCEPTABLE DURATION
01.50.22.1	Data Gap	6.6 μs	6.3-6.9 μs
01.70.16.1	Data Squelch	350 μs	335-365 μs
01.70.16.1	Set AGC	200 μs	190-210 μs
01.80.02.1	Long Gap	24 μs	23-25 μs
01.80.02.1	Short Gap	3.0 ± 0.3 μs	2.9-3.1 μs

The oscillator generates 625-KC ± pulses.

There are 475 ± 20 microseconds between the early and late indexes from the 1301 file for timing control purposes in the 7631.

Gap Detector Adjustments

The three gap sensors in the 7631 must be adjusted to the following settings for proper operation:

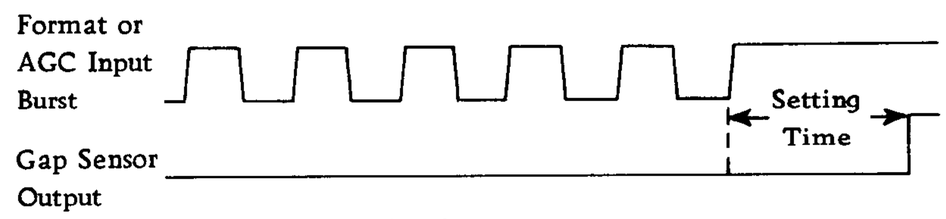
Short Gap sensor	(01B1F05)	3.0 ± 0.1 μs
Long gap sensor	(01B1E05)	24 ± 1.0 μs
Data gap sensor	(01B1B11)	6.6 ± 0.3 μs

The gap sensors must be adjusted dynamically with a 1301 file or a file simulator. They may be adjusted off-line through the 7631 CE panel or on-line with the system in a loop in any one of the prepare to verify and read operations of HAO, TRO, SRO, or TWA. If only the short and long gap sensors must be adjusted, a format write check loop may be used.

Description of Adjustments

To adjust the gap sensors, use an oscilloscope that can display two signals simultaneously, and has a continuously variable delayed sync. The Tektronix 555 is preferable for this purpose, although other oscilloscopes can be used.

The setting of a gap sensor is to be measured from the fall of the last pulse of a long train of pulses, at the input, to the rise of the output of the gap sensor:



The data gap sensor should not be adjusted on a few random data bits. An AGC burst must be used.

Gap sensor input — pin C
Gap sensor output — pin H

To adjust a gap sensor off-line through the 7631 CE panel, set up any of the above mentioned prepare to verify control instructions, then turn on loop mode, service response, and read switches in that order. This should form a repetitive loop on one operation that will supply format or data information to the inputs of the gap sensors.

All of the above instructions assume that some format and data are present on the file. In the case of a new file or one that has been recently restacked, the

format must first be written. With format write check loop, adjust the long and short gap sensors; next, write HA1, and then loop on HA1 write check or read and adjust the data gap sensor.

Flag Operation

Flag operations permit a defective disk track to be removed permanently from the customer disk address scheme through program action by the Customer Engineer. If the defective track's home address area one is free of defects, a flag character can be written with HA1; as a result, all subsequent read or write operations with the flagged address (defective track) switch to the *alternate* disk track. The flag character, written on the defective track, is the address of one of six alternate disk tracks in the cylinder. The final step in a flag operation requires that the defective track's HA1 is also written on the alternate track. (NEVER write a flag character on the alternate track or a disk storage system hang-up will occur.)

Procedure to Write and Flag Tracks

1. Assume track 5555 is defective.
2. Seek to the desired cylinder.
3. Verify the address of the track to be flagged. Perform a TRO, TWA, or HAO customer operation to verify track 5555.
4. Set the HAO and HAO-CE switches on.
5. Execute a HAO write operation whose address specifies the access module and track address of the defective track. Random record digits R0 and R1 must be blanks or BCD eights.

   Address: 555588

The data for the HAO write operation must be HA1 and a fifth character, the flag. The flag should specify the desired alternate track for that cylinder. (Assume the alternate track two (2), is desired.)

Data: 55552

The data is written as home address one (HA1) to flag the track and switch all subsequent read and write operations to alternate track two (2) of that cylinder.

6. It is necessary to write the normal home address one (HA1), 5555, on the alternate surface. Execute a second HAO write operation with both HAO switches on. The address of the second HAO control word should correspond to the track address 5555 and should include the desired alternate surface select digit as the fifth character, position R0 of the control word.

   Address: 555528

Replace the alternate track digit in the data field with a BCD eight or blank and write.

Data: 555588

7. Turn off both HAO switches. The track 5555 is now flagged to alternate surface two (2).

Power Distribution and Control Sequence

The AC CB1 supplies power to pick K1 through the emergency off reset. K1 applies power to T1. R6 holds with T1 power if the system interlock and emergency off are a complete circuit. The power on switch depressed causes R1, K2 and R2 to pick and the power on indicator to light. K2 applies power to the blower. R1 picks R3 and the thermal indicator goes off. R3 picks K3; K3 applies line power to the DC +12 and −12 volt supplies. The output of the supplies causes R5 to pick. (R5 picks at 22 volts and drops at 14 volts.) R5 picks R4 and causes the DC on indicator to light; R4 drops R1 to complete the sequence. If the DC power drops below 14 volts, R5 drops causing K3 and R4 to drop, which removes the line power from both DC supplies. The DC off has the same effect as R5.

Minus six volts for NAND circuits in supplies from SMS cards are shown on ALD page 90.34. The ACY card at 5A supplies the reference (−6 volts) for the remaining driver cards on ALD page 90.34.

SHIFT REGISTER TEST (Eight-bit Mode)

HAO-CE WRITE AGC of HA-1
(All active levels are negative)

For convenience, set the write inhibit switch on and a seek to a CE track is not necessary.

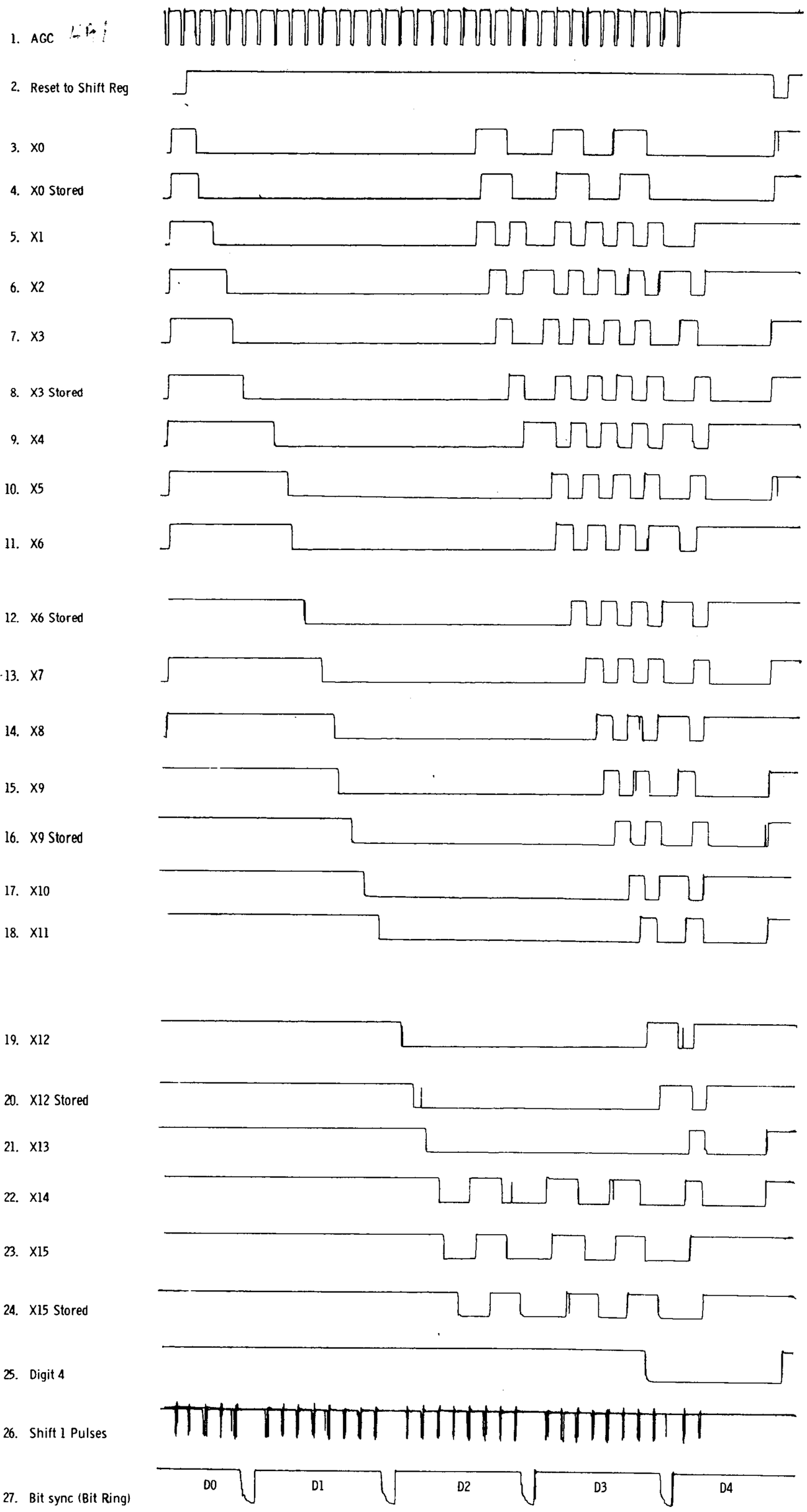


Figure 122. Shift Register Test Eight-Bit Mode

COMMENT SHEET

IBM 7631 FILE CONTROL

CUSTOMER ENGINEERING INSTRUCTION–MAINTENANCE, FORM 223–2766–1

FROM

NAME _____

OFFICE NO. _____

FOLD

CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

FOLD

☐ SUGGESTED ADDITION (PAGE , TIMING CHART, DRAWING, PROCEDURE, ETC.)

☐ SUGGESTED DELETION (PAGE)

☐ ERROR (PAGE)

EXPLANATION

CUT ALONG LINE

FOLD

FOLD

NO POSTAGE NECESSARY IF MAILED IN U.S.A.

FOLD ON TWO LINES, STAPLE, AND MAIL

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 81

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