

IBM

Customer Engineering
Instruction - Reference

1414 Input-Output Synchronizer

Models 3, 4, 5, 6 and 8





Instruction-Reference
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Preface

This manual provides instruction and reference material for all models of the 1414 except those models (1, 2, and 7) that control magnetic tape units.

It includes magnetic core theory, integrated synchronizer theory, print storage operation, paper tape reader operation, serial scan operation, CE panel off-line operation, and the 1402 reader-punch operations (including the column binary feature).

For information concerning the individual input-output units controlled by the 1414, consult the CE manual for the specific machine. The 1414 can be used with several different data processing systems; therefore, program instructions are not included in this manual.

1402 Card Read-Punch	Form 231-0002
1403 Printer (Manual of Instruction)	Form 225-6492
1403 Printer (Reference Manual)	Form 225-6493
1009 Attachment to 1414	Form R23-2557
1011 Paper Tape Reader	Form 227-5546
1014 Remote Inquiry	Form R23-9913
1410 Telegraph Feature	Form R23-9770

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1414 Input-Output Synchronizer

The IBM 1414 Input-Output Synchronizer serves as the intermediate storage and control unit between a data processing system and a large group of input-output devices. A customer may choose from several models to meet specific requirements of input-output device combinations. Model variations also permit the 1414 to be used with several different IBM Data Processing Systems: 1410, 7070, 7080, 7090, 7094, 7040, 7044, and 7010. Input-Output devices controlled by the 1414 include magnetic tape units, the IBM 1402 Card Read Punch, the IBM 1403 Printer, and the following TELE-PROCESSING® machines:

- 1009 Data Transmission Unit
- 1011 Paper Tape Reader
- 1014 Remote Inquiry Telegraph Feature

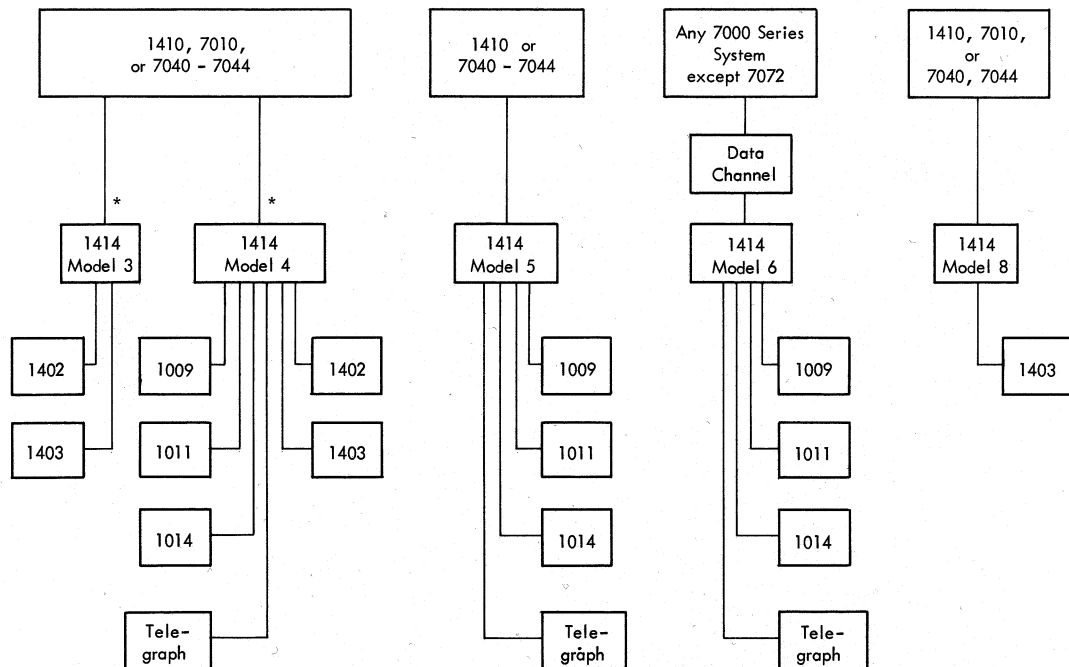
Eight different models, divided into two broad classifications, are available: those that control magnetic

tape units (Models 1, 2, and 7), and those that do not control tape units (Models 3, 4, 5, 6, and 8). The second group of models is further distinguished from the tape controlling models by use of magnetic core storage buffers.

The tape control models are the subject of a separate manual: *CE Instruction-Reference Manual, IBM 1414 I-O Synchronizer Models 1, 2, and 7, Form 223-2554.*

1414 Model Applications

Different models of the 1414 and the different input-output devices they control present many possible combinations. Some possible combinations are shown in Figure 1. The following paragraphs briefly describe each of the five models discussed in this manual.



* With a 7040 - 7044 System, either a 1414 Model 3 or a 1414 Model 4, but not both.

Figure 1. 1414 Models 3, 4, 5, 6, and 8

Model 3

The 1414 Model 3 contains the integrated synchronizer and controlling circuits for the 1402 Card Read Punch. The Model 3 also can have the print buffer and controls for the 1403 Printer.

Physically, the Model 3 is one standard rack and panel module with power supplies mounted in the 1402.

The 1414 Model 3 can be attached to either of the two available channels of the IBM 1410 Data Processing System, or to Channel A of an IBM 7040 or 7044 Data Processing System.

Model 4

The 1414 Model 4 differs from the Model 3 in that it has additional magnetic core buffers that permit attaching TELE-PROCESSING machines e.g., 1009, 1011, 1014, and telegraph. Six additional buffers are available and many combinations of TELE-PROCESSING machine attachments are possible within the limits of the six buffers. Details of these possibilities are discussed elsewhere in this manual.

Adapter circuits for these optional features require the addition of a second rack and panel, Module C (Figure 2).

Model 5

The Model 5 is similar to the Model 4 in that it can control the same TELE-PROCESSING machines. The

Model 5, however, does not include control of the 1402 or 1403. Like the Model 3 or 4, the Model 5 may be attached to either the 1410 or a 7040-7044 System.

Model 6

The Model 6 controls the same group of input-output devices as the Model 5, but by the addition of conversion circuits, presents the Simplex I-O Interface to the using system. Therefore, the Model 6 can be used with any system that has a Simplex I-O Interface channel.

Circuits common to Models 3, 4, 5, and 6 are covered in this manual. However, for those circuits that apply only to Model 6, see the supplementary manual, *IBM 1414 Model 6 Input-Output Synchronizer*, Form R23-9914.

Model 8

The 1414 Model 8 is used with the 1410, 7040, or 7044 Systems. Model 8 is identical with the printer control portion of the 1414 Model 3 or 4. The integrated buffer and the 1402 controls are omitted, limiting the Model 8 to a 1403 Printer control unit. Power supplies for the 1414 that are in the 1402 for a Model 3 or 4 are located in the panel 2 position of the 1414 Model 8.

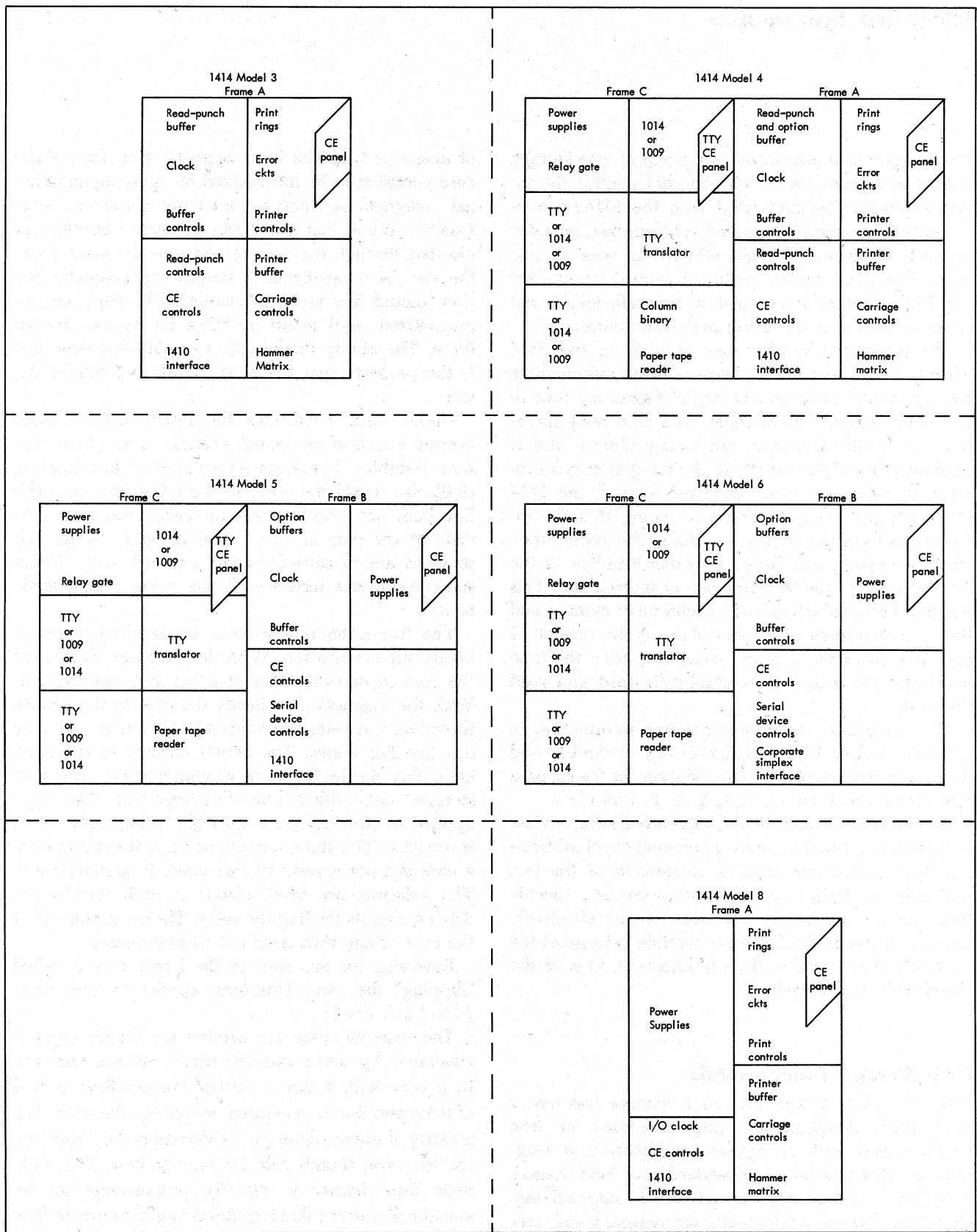


Figure 2. 1414 Panel Layout

Integrated Synchronizer

The integrated synchronizer is a group of core storage buffers and their control circuits that control the input-output devices associated with the 1414-I-O Synchronizer. The term, integrated synchronizer, includes up to a maximum of eight 80-position core storage units. The print buffer (with its control circuits for the 1403 printer) is completely separate and is not considered part of the integrated synchronizer.

The integrated synchronizer is used in the 1414 Models 3, 4, 5 and 6 and, because of its intermediate storage ability, provides a saving of processing time to the using system. For example, on a card read operation, the system continues processing while a card is read into the reader section of the integrated synchronizer storage unit. After the card is read, the 1414 sends a signal to the system indicating that the information from the card is available. The system then stops processing and issues a read instruction to the 1414 to transfer the 80 characters of information. This transfer between integrated synchronizer storage and the system storage unit takes place at the rate of 11 usec per character, a much faster rate than the time necessary (75 msec) to mechanically feed and read the card.

The integrated synchronizer stores information in BCD form and each position stores any of the 64 valid characters represented by combinations of the six data bits plus a check bit (1, 2, 4, 8, A, B, and C).

The unusual feature of the integrated synchronizer is that all eight buffers share a common set of addressing rings and driver circuits. Regardless of the fact that only one buffer operation can occur at a specific time, several input-output devices can be effectively in use at the same time. This is possible because of the relatively slow speed of the I-O devices in view of the speed of the buffer itself.

Core Storage Fundamentals

Magnetic core storage uses as a storage medium a very small doughnut-like ring composed of iron oxides mixed with manganese carbonate and magnesium. This mixture is pulverized and heat-treated, a binder is added, and the mixture is stamped into ring-shaped cores. Additional heat-treating steps complete the manufacturing process.

The ferrite core is a bistable storage device. It has the ability to store a bit of information in the form

of magnetic flux. The ferro-magnetic properties of the core permit it to be magnetized by applying an external magnetizing action or magnetomotive force (MMF). Wires that carry direct electric current are inserted through the core to generate the MMF. Once the core is magnetized, it retains the magnetic flux even though the MMF is removed. The core remains magnetized until again operated on by an external force. The ability of the core to retain magnetic flux is the property that makes it useful as a storage device.

Under static conditions the ferrite core is magnetized in one of two possible stable states (hence the term bistable). In one state the magnetic flux lines are clockwise inside the core; in the other, the magnetic flux lines are counterclockwise inside the core. The state of the core at any instant depends on the last previous action caused by the external MMF. Under static conditions ferrite cores are never magnetically neutral.

The two states of the cores are used to represent binary bit information. With the magnetic flux inside the core in one direction, it is set and contains a 1. With the magnetic flux inside the core in the reverse direction, it is reset and holds a 0. Note that each core has two flux states. The actual polarity of the magnetic flux inside the core is unimportant. The core storage units utilize only flux reversals. The logic applied to core storage is this: If reading from a core reversed its flux state, it contained a 1; if reading from a core did not reverse its flux state, it contained a 0. The polarities are fixed relative to each core by the driving circuits feeding the cores. The exact polarity of the core at any time need not be determined.

Reversing the flux state of the ferrite core is called "flipping" the core. This term applies to both cases (0 to 1 and 1 to 0).

The external MMF for driving the ferrite cores is generated by wires carrying direct electric currents. In a wire with a direct electric current flow, a field of magnetic flux is generated, encircling the wire. The polarity of the flux lines can be determined by applying the left-hand thumb rule for current flow. The magnetic flux density is directly proportional to the amount of current flowing. Reversing the current flow in the wire reverses the flux line direction, but the magnetic flux density is again directly proportional to the amount of current flowing. The polarity and

density of the magnetic flux generated around a conductor are therefore dependent on the direction and amount of current flow.

The magnetism produced as a magnetomotive force applied to a core can be expressed graphically. The graph of flux density (B) versus magnetizing force (H) is called a B - H curve or hysteresis loop (Figure 3). For an electrical coil $H = NI$ where N is the number of turns in the coil and I is the current. In ferrite core storage the wires pass through the core only once; therefore, $N = 1$. With single turn windings, the magnetomotive force is numerically equal to the current; it is simpler, therefore, to express H in terms of I .

An ideal ferrite core would have a rectangular B - H curve; this condition does not exist, however. A typical B - H curve is shown in Figure 3.

The ferrite core operates along the path of the B - H curve. Consider a core initially with no magnetic flux ($B = 0$). String the core on a conductor. Passing current through the conductor generates a magnetomotive force, magnetizing the core. The path followed is from A to J as shown by the dotted line in Figure 3. After reaching point J the ferrite core becomes saturated with magnetic flux. Any increase in I (current) beyond point J causes little increase in the flux inside the core. The value of current necessary to just saturate the core is referred to as full current (I). When I is reduced to zero, the flux state of the core resides at point L . Application of $-I$ (reversing current in the conductor) flips the core along the path L to N . (Notice that $1/2 I$ is not sufficient to flip the core.) Removal of the $-I$ lets the core reside in the flux state represented by point Q . Application of $+I$ flips the core along the path from Q to J . Removing the $+I$ lets the core again reside at point L . When the core is in the flux state as represented by point L , it is arbitrarily said to be in the 1 flux state. Point Q represents the 0 flux state.

It is essential that the core be sensitive to application of $+I$ and $-I$ but insensitive to applications of $+1/2 I$, and $-1/2 I$. The following table shows the paths followed for the application and removal of the four currents (Figure 3).

CURRENT PULSE APPLIED	RESULTING PATH (CORE HOLDING 0)	RESULTING PATH (CORE HOLDING 1)
$-I$	Q to N , back to Q	L to N , N to Q (flips)
$-1/2 I$	Q to P , back to Q	L to M , back to L (app)
$+1/2 I$	Q to R , back to Q (app)	L to K , back to L (app)
$+I$	Q to J , J to L (flips)	L to J , back to L (flips)

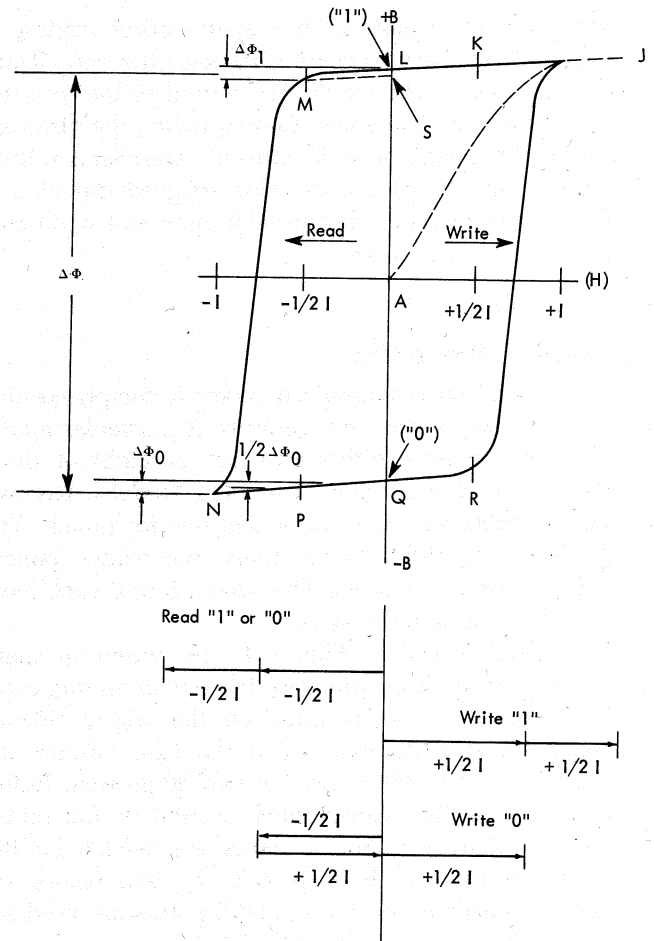


Figure 3. Core Outputs and Core Currents

The following conclusions can be drawn:

1. $+I$ is required to flip the core from the 0 to 1 flux state.
2. $-I$ is required to flip the core from the 1 to 0 state.
3. Application of $+1/2 I$ and $-1/2 I$ cannot flip the core, regardless of its flux state.
4. The core never comes to rest in a neutral flux state ($B = 0$).

To take information from a core, the core is read. Any core selected for reading has a full $-I$ applied to it. Therefore, current in the minus direction is called read current (Figure 3). Putting information into a core is called writing into it. The selected core has a full $+I$ applied. Therefore, current in a plus direction is called write current.

The directions chosen for read and write currents are arbitrary. The important fact is that the read current and the write current magnetomotive forces have opposite polarities as felt by the core.

Writing a 1 into a core stores flux with 1 polarity. Reading from the core reverses the flux and resets the

core to 0. A change of flux state during reading is detected by a sense winding through the core. Thus, a rapid rate of change of flux is used to interpret information stored in cores. Consequently, the direction assigned to read and write currents must remain fixed with respect to each core. This assigned direction is fixed by the circuits that provide read and write current to the ferrite cores.

Physical Properties

The integrated synchronized buffer is comprised of a group of 80-position storage units. A particular model of 1414 can have either two, six, or eight of these 80-position storage units. The 1414 Model 3 has two storage units; one for reader and one for punch. The Model 4 has eight storage units: the reader, punch, and six optional buffers. The Model 5 or 6 each have only the six optional buffers.

The buffer cores (Figure 4) are wired in small planes that are approximately the size of an sms card. However, they are mounted on the wiring side of panel 2, row B, in frame A of the 1414 (Figure 2). Each plane has 160 cores for two 80-position buffer sections and the reader-punch section of the buffer requires 13 planes. Seven planes are needed for the seven BCD bits (C, B, A, 8, 4, 2, 1), four planes are used for checking purposes, and 2 planes are used for reading from the brushes of the 1402.

If the 1414 is a Model 4, the buffer consists of 24 additional planes of cores for the six optional 80-position sections, making a total of 37 planes. These 24 additional planes are divided into three groups of eight planes with the seven BCD planes and one plane for control purposes (Figure 8).

Buffer Core Winding

The buffer cores are wound as shown in Figure 4. This winding method, called bilateral winding, is different from other core storage units. In place of one X and one Y winding to select a core, four wires are used. Separate read and write wires are used rather than reversing the current direction in a single wire.

Only one core in a plane can be selected during any one cycle. The selected core is read from during the read portion of the cycle. The same core is written into during the write portion of the same cycle. This concept is important: the selected core in a plane is first read from and then written into during the same cycle.

A coincident current selection method locates a single core on a plane. Assume that 270 milliamperes of current is flowing in the same direction in each of

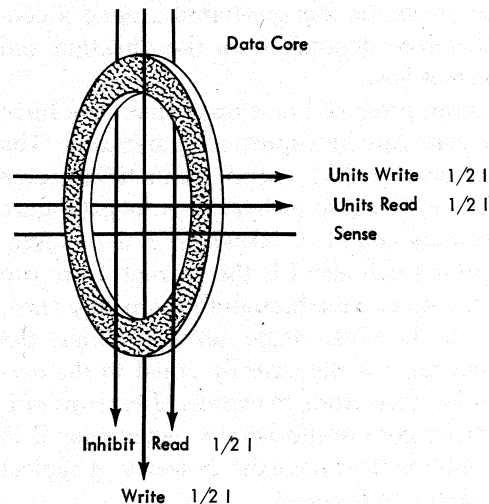


Figure 4. Integrated Synchronizer Cores (Bilateral Winding)

the two parallel wires through a ferrite core (Figure 5A). The resulting MMF's from each wire are additive. The net effect is equivalent to one wire carrying 540 milliamperes of current. Now visualize one of the wires 90° with respect to the other and the ferrite core at the intersecting point (Figure 5B). With the current flowing as shown, the MMF's of the two wires are additive at the crossover point. Thus the force felt on the core is the result of 540 milliamperes of current. The MMF from full current forces the core to flip. To use a core as a storage device, it is necessary to be able to flip it either direction. The core could be re-flipped by reversing the currents in the two wires; however, the same effect is produced by adding a second pair of wires parallel to the first pair but passing them through the core in the opposite direction (Figure 5C). Thus current in the read windings resets the selected core, and current in the write windings sets the selected core.

The four wires shown in Figure 5C select one of the cores on a plane. Two more wires, to make a total of six, are needed as shown in Figure 4. These two additional windings are called sense and inhibit.

Any core storage unit must have two kinds of controlling circuits. Stated simply, you must tell it *where* and *what*. The *where* is the function of the addressing circuits — read and write windings. The *what* is the data or information to be stored and is the function of the sense and inhibit windings. The sense winding tells *what* at read time and the inhibit winding tells *what* at write time. The *where* or addressing circuits select one location for a complete cycle that consists of both a read and a write time.

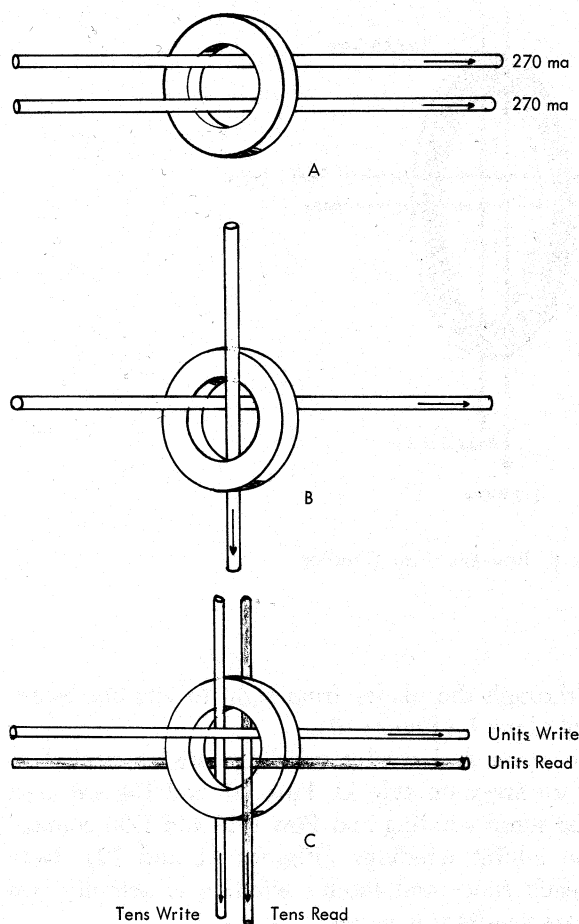


Figure 5. Coincident Currents

The Sense Winding

At read time, the sense winding interprets the information stored in the selected core. This winding must be able to distinguish between the 1 or 0 state of the core.

The sense winding passes through every core in a plane. Because only one core in a plane is interrogated during a cycle, one sense winding is adequate to interpret the information stored in all the cores in one plane.

The selected core has coincident read current applied to it during read time. If the selected core holds a 1, it is flipped to 0. This causes a large flux change in the core ($\Delta \phi$ in Figure 3). The large flux change cuts the sense winding, inducing a large pulse on it. If the selected core held a 0 before the read current was applied, only a little change in flux inside the core is noted ($\Delta \phi_0$ in Figure 3). This induces only a small pulse on the sense winding. Thus, the status of the core before reading is determined.

The sense winding connects to a sense amplifier. The sense amplifier increases the amplitude of any

pulses induced on the sense winding. If the core held a 1, a pulse is present at the output of the sense amplifier, and the ferrite core is flipping. Time sampling is necessary because at points in the cycle, large unwanted noise pulses are induced on the sense winding. To eliminate recognizing unwanted noise as a bit, the sense winding is sampled for a bit only at read time.

The Inhibit Winding

An inhibit winding passes, like a sense winding, through each core of one plane. Inhibit current is used during write time to control *what* is written into the selected core.

The write time of a core storage cycle is always preceded by a read time. During read time the selected core is reset to its 0 state. The currents in the selecting windings are such that in the write portion of the cycle the selected core is set to its 1 state. If the information to be stored requires a particular core to be set to its 1 state, the addressing windings set the core.

However, if the data requires a core not to have a 1 but to remain in the reset or 0 state, current is allowed to flow in the inhibit winding. Since inhibit current is effectively $\frac{1}{2}$ read current, the net effect felt by the core is full write current plus $\frac{1}{2}$ read current. The inhibit current cancels half of the full write current and prevents (inhibits) setting the core to its 1 state.

Row Bit Cores

The buffer must accept information from a card that is read in a parallel fashion. The fact that a card is read a row at a time requires an intermediate storage device capable of storing 80 bits of information at one time. This storing of a complete row of card information is performed by a plane of 80 cores called row bits. Each set of card read brushes has its own group of 80 row bit cores (Figure 8).

Because of their different logical use, the row bit cores are wound differently from the rest of the buffer cores. The write windings originate in the 1402 brush circuits (Figures 6 and 7). These write windings are completely separate from the write windings of the buffer data cores. One write winding has six turns (Figure 6). These six turn windings are connected to the 80 brushes and supply half current to the core in the write or set direction. The other half write current comes from a cb controlled brush driver circuit (Figure 7).

To read out of the row bit cores, two read windings are required. These read windings are the same windings that read out the data cores. For example, at

the same time position 5 of the buffer is being addressed, row bit position 5 (corresponding to column 6 of the card) is addressed and read out. Write time of a buffer cycle cannot affect row bits because the buffer write windings do not go through row bit cores.

As a further example, during read time of a punch buffer cycle all the cores of one address (one of the 80 possible storage positions), which includes the seven BCD cores, the four checking cores, and one row bit core, are selected and reset to read out. During the write half of the same cycle all of the same cores *except* the row bit core are selected to be written into.

Core Array

Figure 8 shows how the core planes are grouped into an array. The planes are numbered from 1 through 41, left to right, facing the wiring side of the machine (1414 Model 4).

The core array is referred to in the ALD's as the "buffer package." The buffer package has its four sides identified for wiring purposes as follows: the top is side A, the front or wiring side is side B, the bottom is side C, and the rear or card side is side D. Each plane of the array has wiring pins on all four sides. Sides A and C pins are numbered 1 through 48, back to front, and sides B and D pins are numbered 1 through 32, top to bottom (Figure 9).

Read and write addressing windings enter the buffer package at plane 17 (Model 3) or plane 41 (Model 4). The read windings pass through all planes and terminate at row bit plane 2. The write windings also

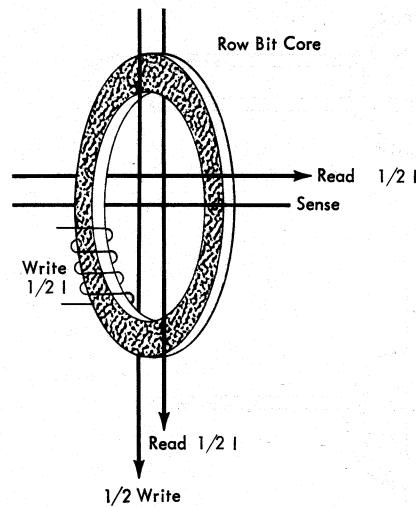


Figure 6. Row-Bit Core Winding

pass through the planes from right to left but terminate at plane 7. (Figure 10).

The sense and inhibit windings are connected to the core array on side D. Pins D1 and D4 are used for the sense winding and Pins D29 and D30 connect to the inhibit windings (Figures 11 and 12). Note that each sense and inhibit winding is actually two separate windings in series.

The integrated synchronizer section of the 1414 Model 3 contains 17 planes (planes 1 through 17, Figure 8). Four of these (1, 3, 4, and 6) are dummy planes used for wiring and do not contain cores. Each

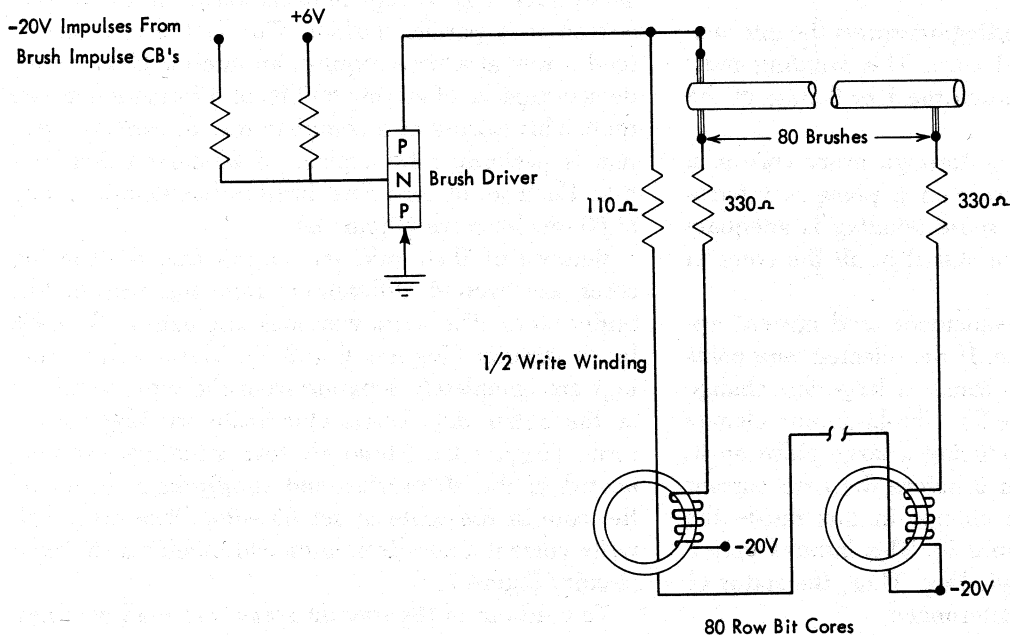


Figure 7. Row-Bit Read-In

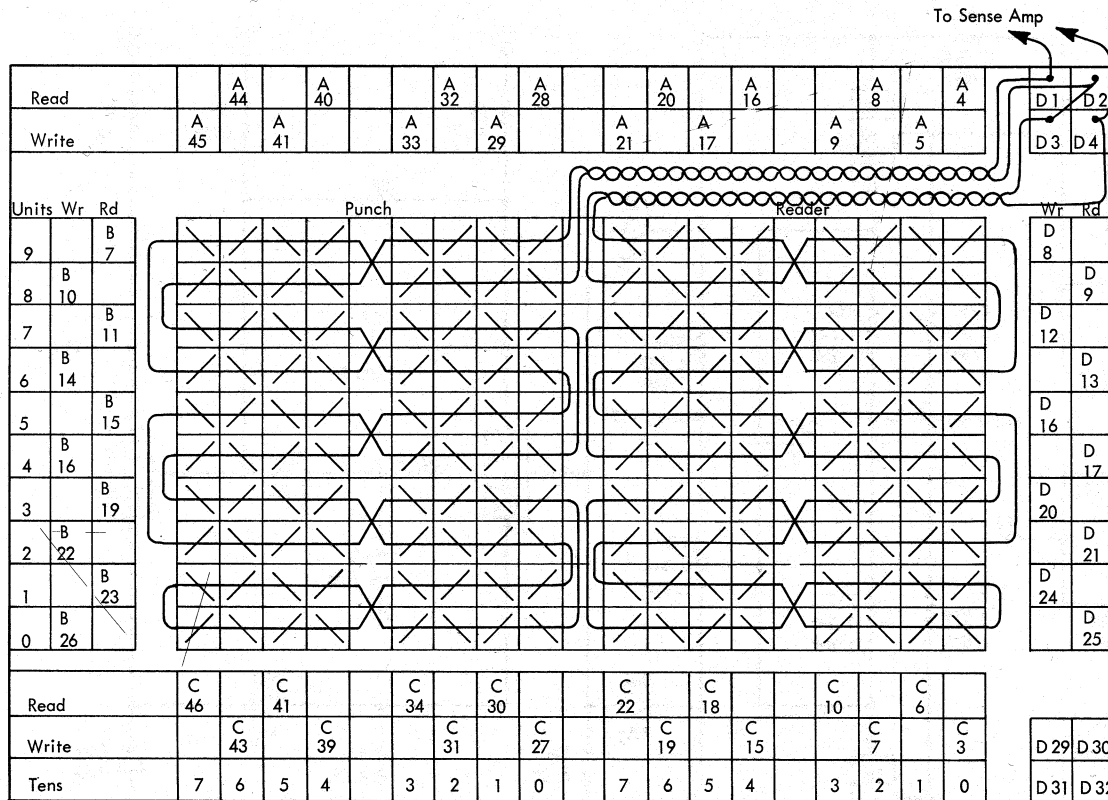


Figure 12. Sense Winding

four planes of each bit effectively have one larger sense and inhibit winding connected to the same set of sense and inhibit circuits. For example, as shown in Figure 16, the B-bit inhibit driver is connected to pin D32 of plane number 36, but the inhibit windings of planes 20, 28, and 36 are jumpered across the additional planes placing all four B-bit inhibit windings in series. To compensate for the change in loading to the inhibit driver circuit, the terminating resistors are changed from 40.2 ohms (FP Card, 1414 Model 3) to 37.4 ohms (RF Card, Model 4).

Addressing

Clock

All operations within the 1414 are controlled by an 11-stage, free-running, closed ring (Figure 17). This ring is driven by a 1-megacycle oscillator which results in a cycle time of 11 microseconds. During one 11-usec cycle one position of storage can be read out of and regenerated or cleared and replaced with a new character. The timing pulses produced by this clock ring are designated 00.0 through 10.0 (in Systems the decimal point is omitted: 000, 010, etc.) and provide all the gates and pulses necessary to control the storage units.

Between the oscillator and the clock is a power inverter (51.30.01). The input to this inverter is called "+ S not clock 2." The "not clock 2" pulse and the clock drive pulse are thus out of phase with each other but driven from the same source, the oscillator. This "not clock 2" pulse is used to develop timing gates between the regular clock outputs. For example the inhibit pulse (06.5-10.5) is developed by AND-ing 060-070 and "not clock 2" to turn on the gate; and 100-000 and "not clock 2" to turn it off. Other half time pulses are generated in a similar way as shown on Systems 51.30.05. As an example, Figure 18 shows how the inhibit pulse is generated.

Ring Addressing

Two rings, units and tens, are used to address the core-storage units. The units ring consists of ten triggers (0-9). Outputs of the triggers drive ten units switches. The units switches select one of ten rows of core positions in one direction. The tens ring consists of eight triggers (0-7). Outputs of these triggers drive eight tens switches. The tens switches select one of eight rows of core positions in the other direction. For example, Figure 19 shows punch position 26 select windings. The tens 2 row and the units 6 row intersect to cause coincidence at position 26 or column 27 of a card.

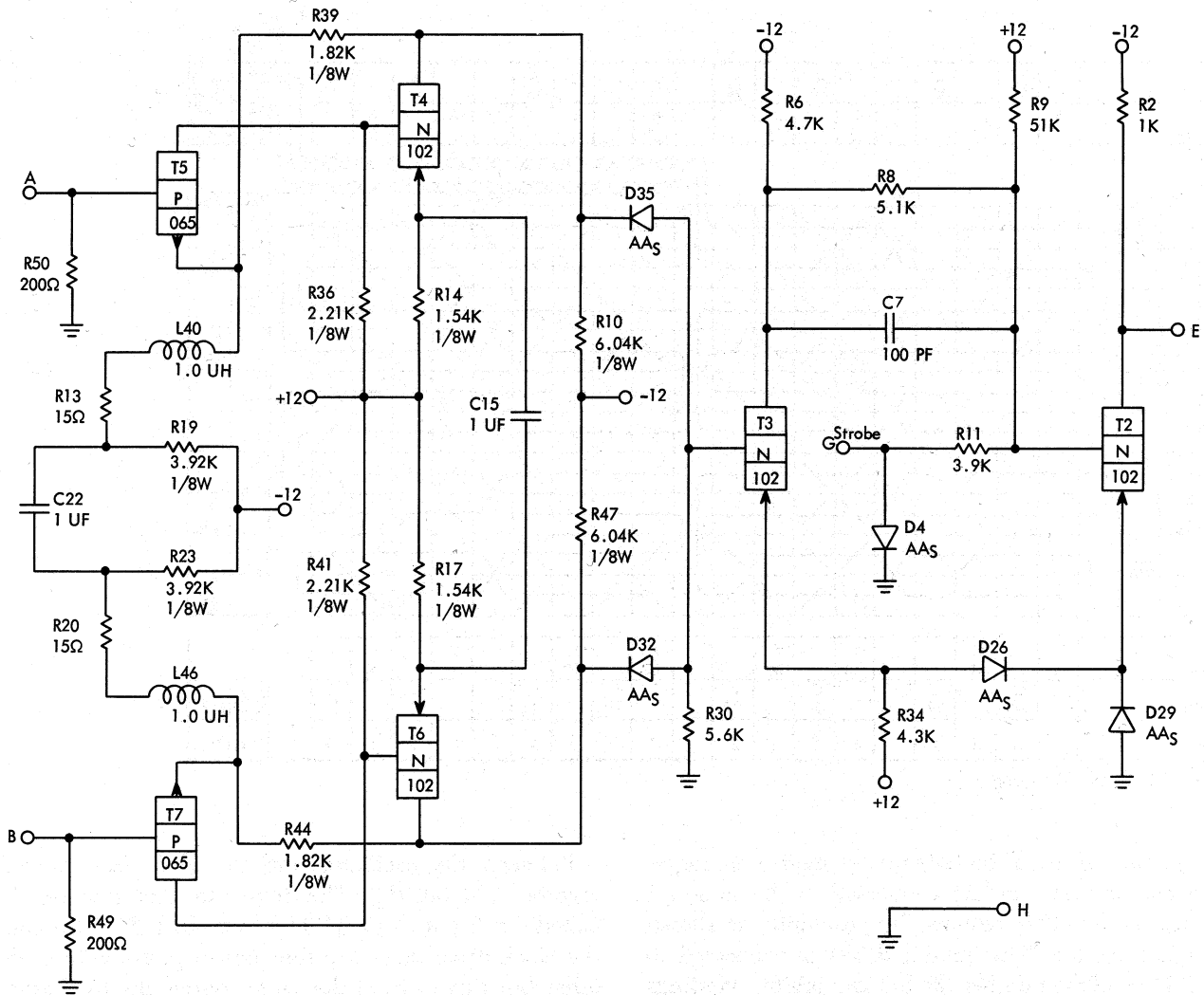


Figure 13. Buffer Sense Amplifier

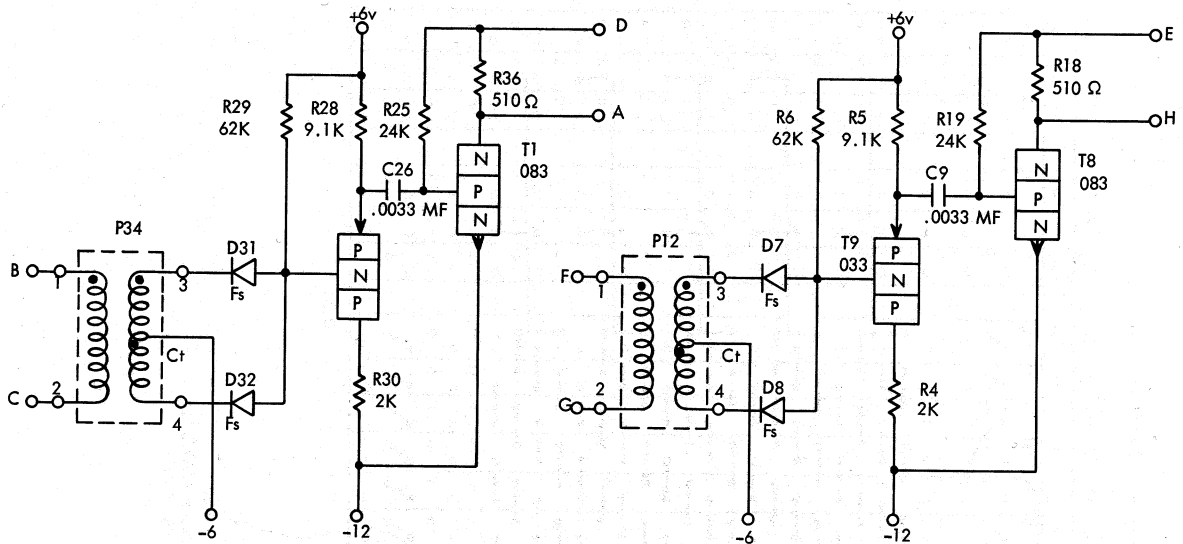


Figure 14. Alloy-Sense Amplifier – Card Type AER

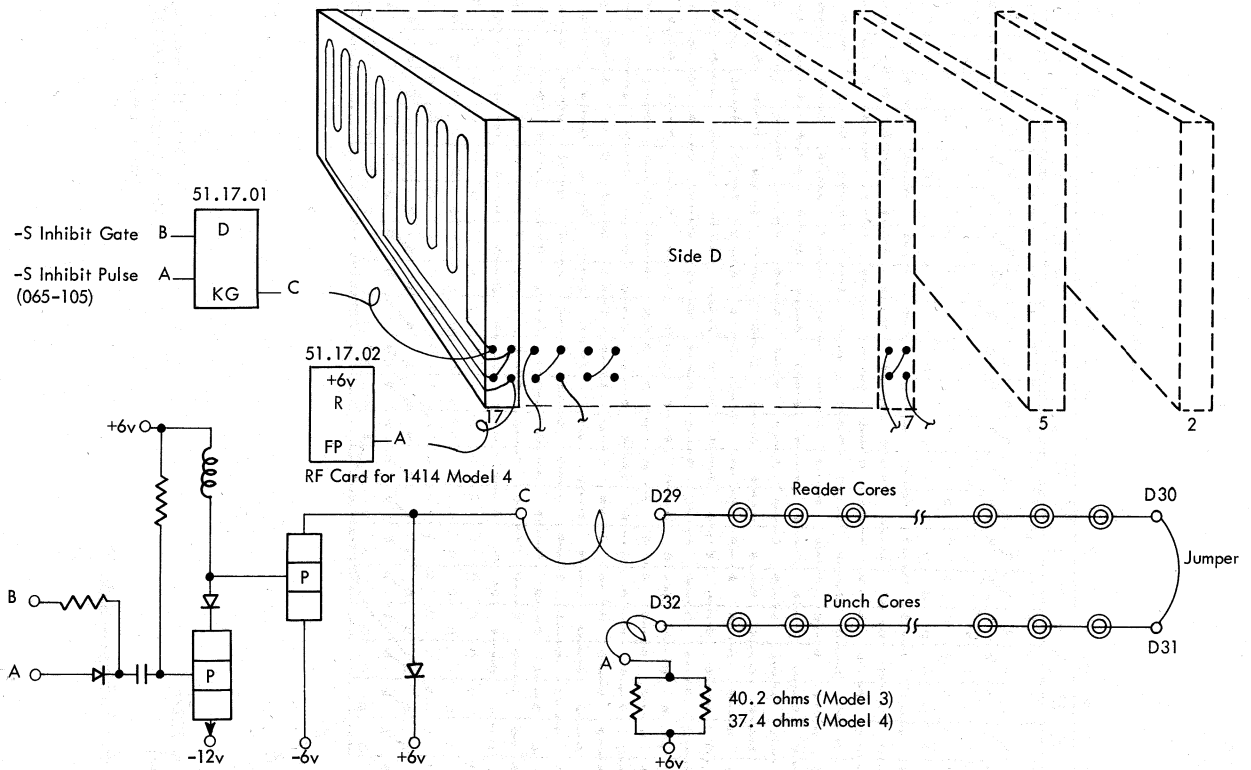


Figure 15. Inhibit Driver

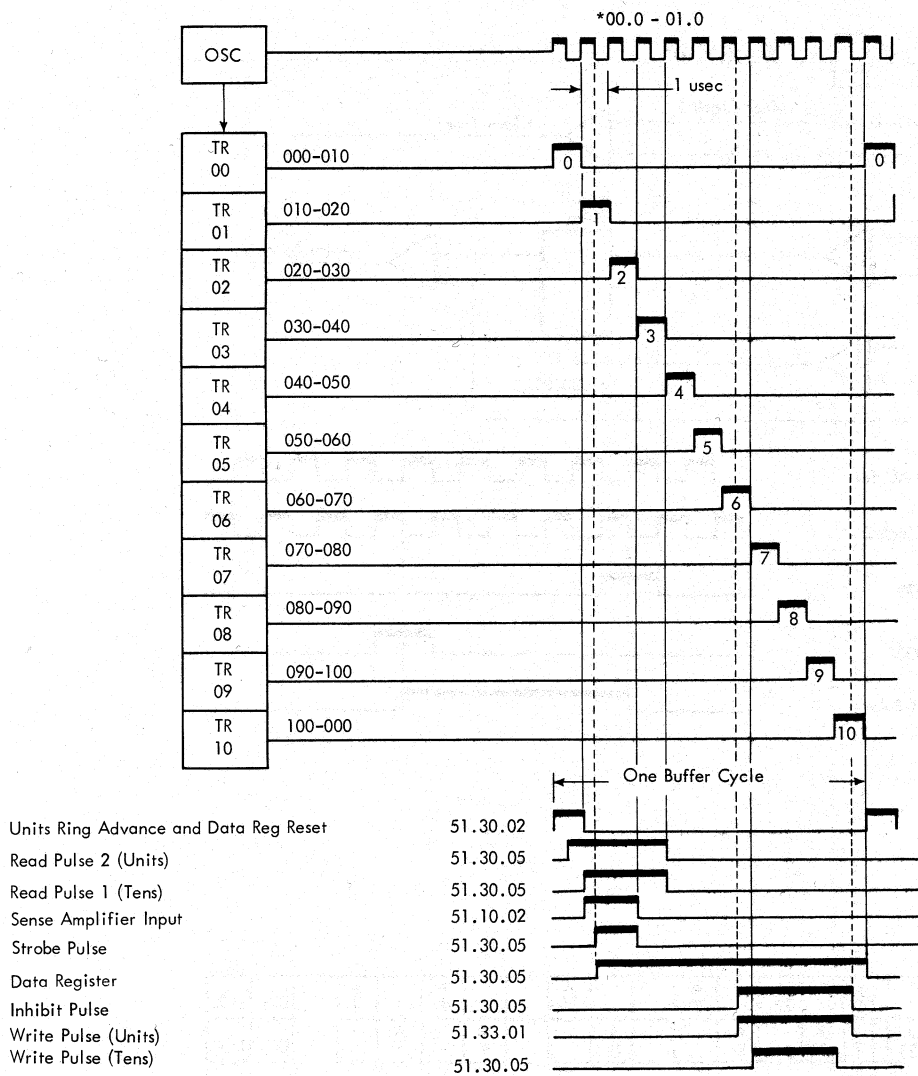


Figure 17. Integrated Buffer Timing Chart

Units ring windings pass through all the cores of both reader and punch (and the optional buffers if a Model 4 is used). The tens ring, however, controls parallel sets of windings, one for each section of the buffer as shown in Figures 20 and 21. Only one tens winding can conduct current at a time; therefore, selecting a buffer section requires the select circuits to gate the correct group of tens windings.

The two rings, units and tens, select each of the 80 possible locations by combinations of the ring outputs. However, the integrated buffer addressing differs from the random addressing of the larger core storage units found in central processing units. Rather than randomly selecting a single location of core storage, the integrated buffer sequentially addresses a group of positions. This sequence is a numerical progression starting at position 00 and, using an 11-microsecond buffer cycle for each position, progresses through all

80 positions ending with position 79. This sequence of cycles requires 880 μ s and is called a scan.

Buffer Scans

Except for operations that use TELE-PROCESSING devices or the Column Binary feature, a scan is a fixed number of 80 buffer cycles. Once started, a scan continues for the full 80 cycles.

When the buffer is not in use, all triggers of both the units and the tens rings are off and the end of scan trigger is on. To start a scan, the end of scan trigger (Figure 22) is turned off and the 0 trigger in both the units and the tens rings is turned on. Each succeeding buffer cycle advances the units ring at 000-010 time by the line "data reg reset 2." When the units ring advances from 9 to 0, the tens ring is advanced. As the rings step to the last position of the

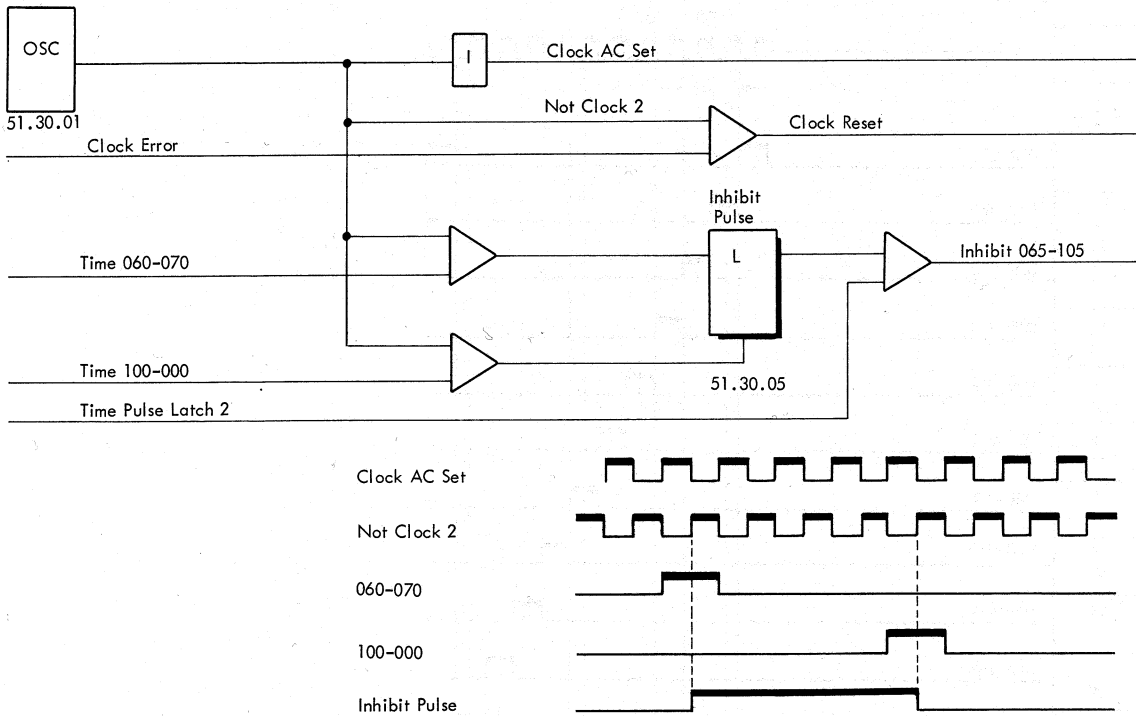


Figure 18. Not Clock 2

Read		A 44		A 40		A 32		A 28		A 20		A 16		A 8		A 4	D 1	D 2	
Write		A 45		A 41		A 33		A 29		A 21		A 17		A 9		A 5	D 3	D 4	
Units	Wr																Wr	Rd	
9																	D 8		
8	B 10																	D 9	
7																	D 12		
6	B 14																	D 13	
5																	D 16		
4	B 18																	D 17	
3																	D 20		
2	B 22																	D 21	
1																	D 24		
0	B 26																	D 25	
Read		C 46		C 41		C 34		C 30		C 22		C 18		C 10		C 6			
Write			C 43		C 39		C 31		C 27		C 19		C 15		C 7		C 3	D 29	D 30
Tens		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	D 31	D 32

Figure 19. Units-Tens Winding Punch Position 26

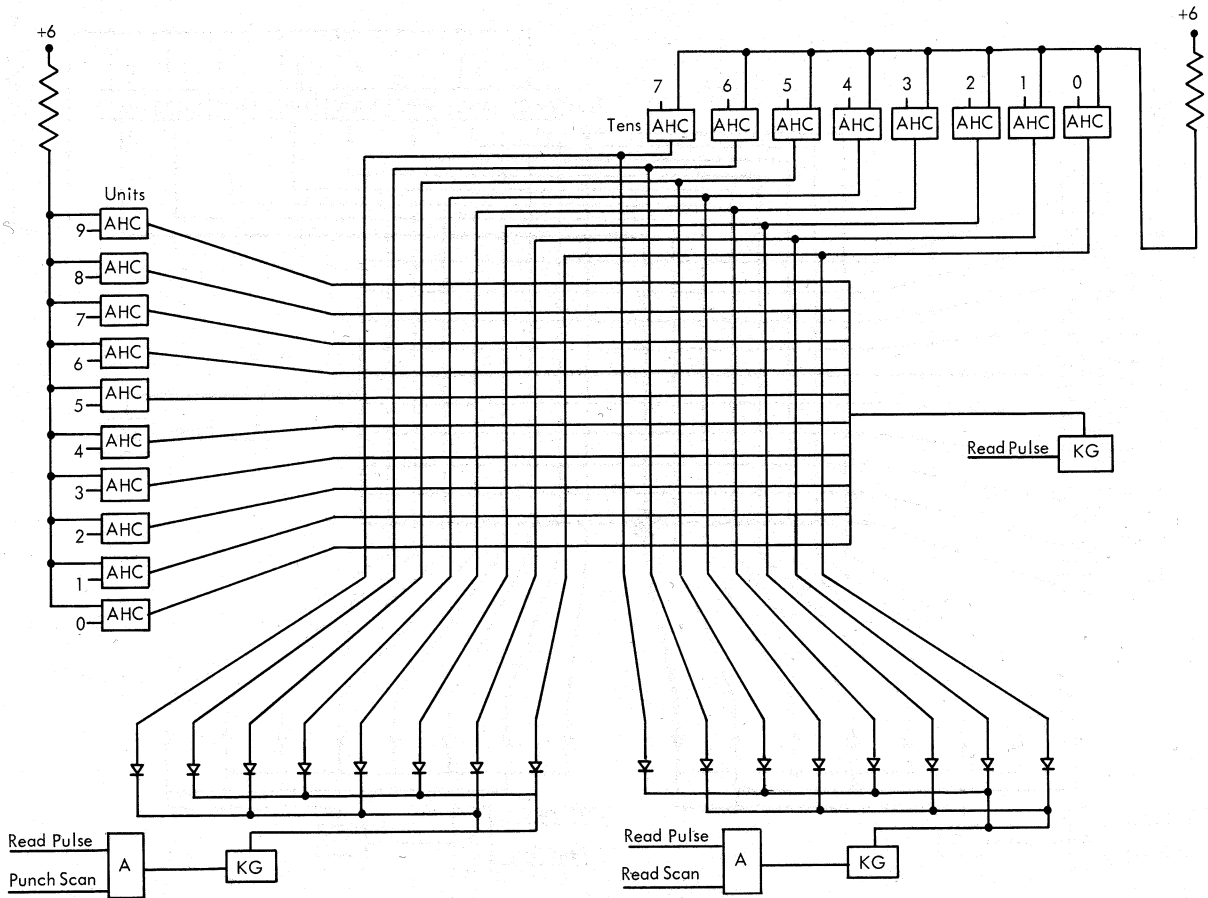


Figure 20. Write Windings

storage unit, "units ring 9" and "tens ring 7" identify the last cycle of the scan. The end of scan trigger is turned on and the rings are reset.

The tens ring AC latch controls the carry from units ring to tens ring and the turn-on of tens 0 at the beginning of a scan. Note that the units ring 0 trigger is actually turned on by the last data reg reset 2 pulse that turns on end-of-scan. However, end-of-scan and 010-020 time cause a DC ring reset to reset all the triggers in both rings.

The ring advance pulse, "data reg reset 2," is produced by a latch called "Time PL1." This latch is turned on at 030-040 time by "some scan" and "not single cycle mode." Time PL1 turns off at 080 time and back on at 090 of each cycle. This is for single-cycle operation from the CE panel. With Time PL1 latch on, the first 000-010 time turns on Time PL2. Time PL2 stays on for the complete scan until a 000-010 time occurs with Time PL1 off (Figure 29 and Systems 51.30.02). Time PL2 gates the read, write, and inhibit pulses to control the current drivers.

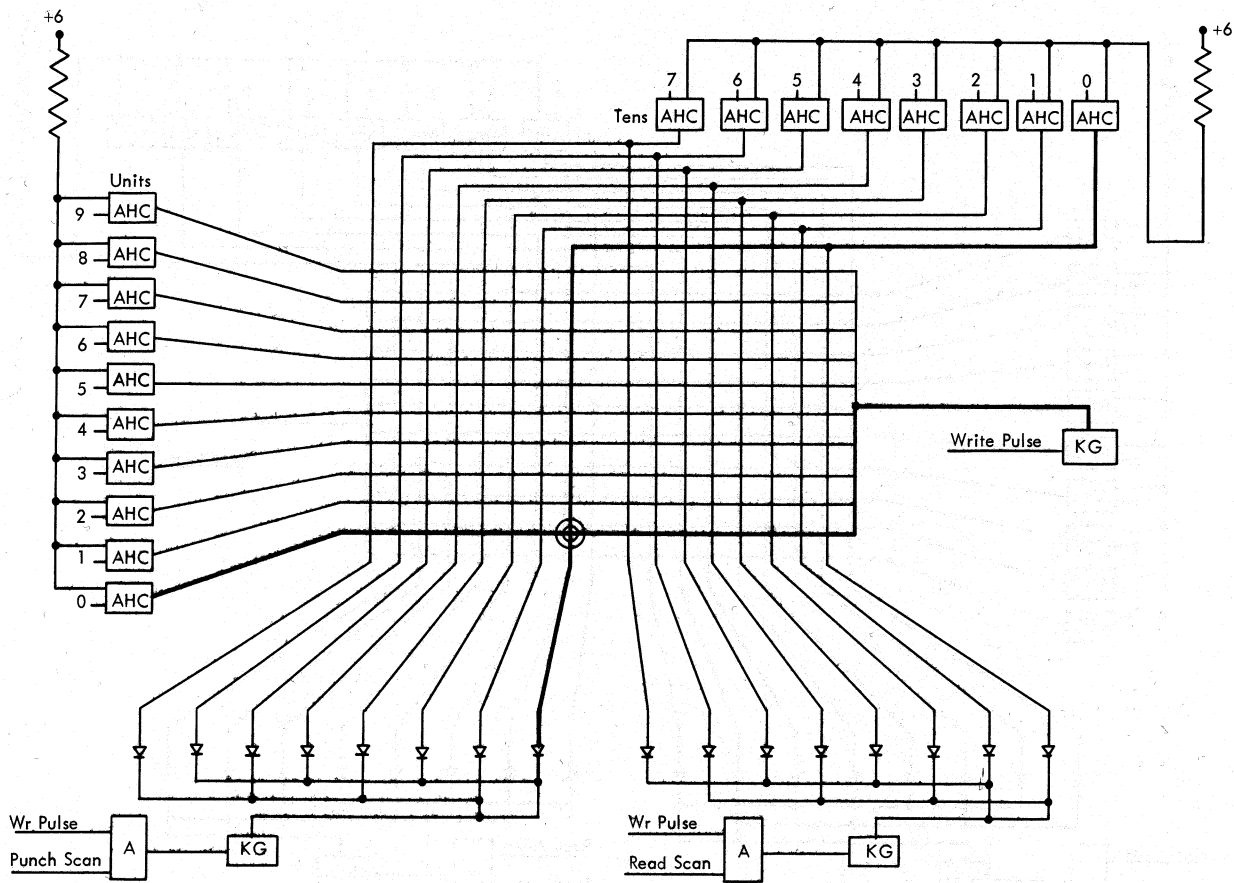


Figure 21. Read Windings

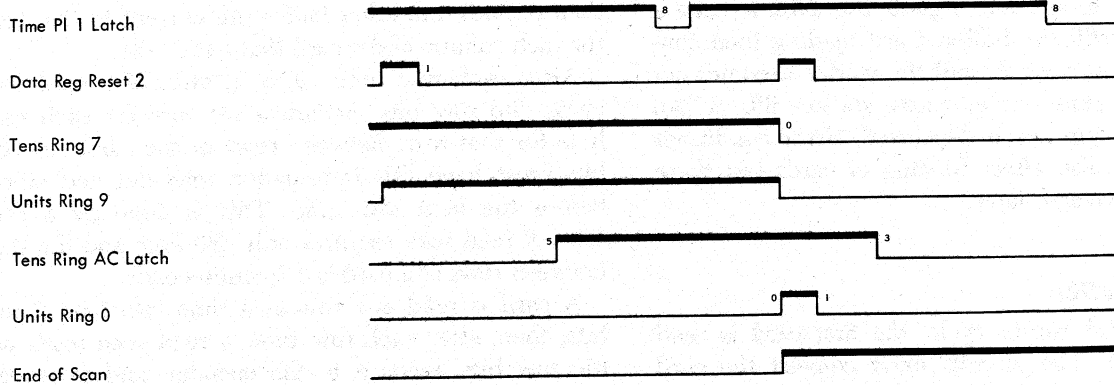
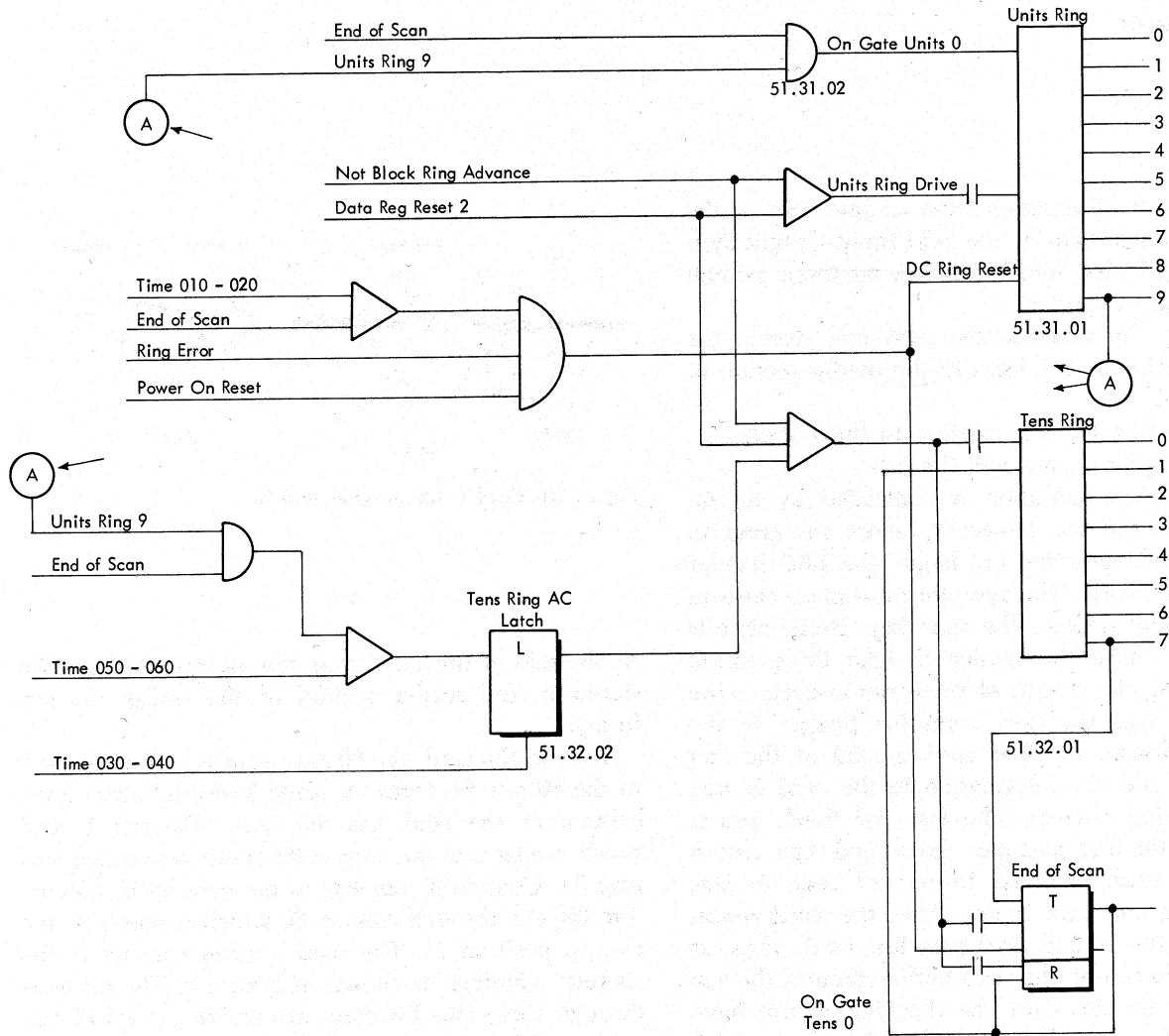


Figure 22. Buffer Ring Controls

Card Reader

The transfer of information from an IBM card to the data processing system by the 1414 Input-Output Synchronizer is divided into the following three general control circuit categories:

1. Reading the holes in the card and storing the information in BCD form in the reader section of the 1414.
2. Transferring this information to the system.
3. Checking the accuracy of the data.

The card read operation is controlled by an instruction from the CPU. However, before any program controlled read operation can begin, the 1402 Reader must be made ready. The operator must place cards in the hopper and depress the start key. Relay circuits in the 1402 cause the reader to take three run-in cycles. During the second of these run-in cycles (the first cycle moves the card from the hopper to the first read station), the first card is read at the first read station and the information in the card is sent to the checking circuits. The last (or third) run-in cycle moves the first card past the second read station where it is read, changed from card code to BCD, and stored in the read buffer. Also, the third run-in cycle moves the second card past first read. Thus, at the end of the run-in, the read buffer contains the BCD equivalent of the first card, the checking circuits have stored the information from the second card, the third card has advanced from the hopper and is positioned ready to be read by first read on the next feed cycle, and the reader ready is turned on (Figure 23).

With the first card in the read buffer and the reader ready, no further action occurs until the CPU issues a read instruction. The programmed read instruction transfers the stored information contained in the read buffer to CPU storage and signals the 1402 to take a feed cycle to refill the buffer. Card reading then continues under CPU control until the reader becomes not ready; hopper runs out of cards, stacker fills, a jam occurs, or the stop key is depressed. Error conditions and end-of-file also affect feeding of cards but these variations are covered later.

Reader to Buffer

During the third run-in cycle, the first card is read at second read. The circuits must convert the card information from card code to BCD and effect this code conversion while reading the card one row at a time (all 9's followed by all 8's, all 7's, etc. through 12's).

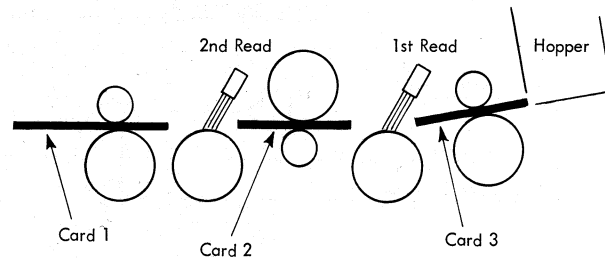


Figure 23. Card Positions After Run-In

At the end of the feed cycle the information must be stored in the reader section of the buffer (in BCD form).

To read the card, the 80 read brushes are connected to the 80 row bit cores on plane 5 of the buffer. Each column of the card has one core. Column 1 read brush connects to the core at 00 (units ring 0 and tens ring 0). Column 2 connects to the core at 01, column 3 to 02, etc. through column 80 which connects to the core at position 79. The read brushes connect to the six-turn windings as shown in Figure 6. The currents through these row bit cores are under control of CB's in the 1402. A CB impulse is generated for each row time of the card which fires a 600- μ s single-shot. This ss conditions a brush driver transistor (in the 1402) that has a split load. One of the parallel outputs of the brush driver transistor feeds a current line that provides half write current for all 80 of the row bit cores. The other output feeds the common brush of the second read station (Figure 7). The brushes then provide the other half write current to the cores for each column of the card that has a hole.

After each row time (9, 8, 7, etc.) of a card feed cycle, the row bits contain a set core for each card hole for that row. Between rows of the card, the row bits must have this information read out and stored before the next row time. This is done by a read scan. A read scan requires only 880 usec and the time between rows of a card is 3.75 milliseconds.

A card is read one row at a time into read 2 row bits; then, after each row time, a read scan reads out the row bits, feeds it to the encoder, and stores the encoded BCD information in the reader storage unit (planes 11-17). During each of the 12 read scans all the reader section cores of all 80 locations are read

out. As stated in the buffer addressing description, the units and tens read windings pass through all cores including row bits. However, since each buffer cycle has a read and write time, any positions previously encoded (or partially encoded) are written back into or regenerated.

Read Encode

The purpose of the read encoder is to combine all the punches of a card column (alphabetic or special character) into a single, valid BCD character. This circuit has three distinct inputs (Figure 24): bit "X" which is the read 2 data register output, CB pulses from the 1402 to identify the card row being scanned, and the BCD data registers (7 bits). The encoder output is seven BCD bit lines that control the inhibit drivers of the storage unit.

The CB pulses that identify the card row are made up of combinations of seven separate CB's. These combinations are shown in the chart in Figure 25. The read encoder is used 80 times for each of the 12 read scans to encode all of the 960 possible holes of an IBM card.

Consider the following example: Assume that an alphabetic G (12 and 7 punches) is punched in the

card in column 1 and that the rest of the card is blank. If the example card is the first card, the feed cycle that moves this card past the second read station is the third run-in cycle as explained above. However, if it were preceded by at least one card, the feed cycle is initiated as the result of a program instruction from CPU that transferred the previous card information from the buffer to CPU. Regardless of how the feed cycle starts, the actual reading of the card and encoding to BCD is the same.

At the end of the 12 read scans for this example card, the read buffer must have a B-, A-, 4-, 2-, and 1-bit combination in position 00, and C bits only in positions 01 through 79.

As the card moves past the second read brushes, the CB's which are in time with the card motion generate the row identifying pulses. The first read CB impulse coincides with the time the brushes are in position to read the 9 holes of the card. However, the example card has no 9 holes so none of the row bit cores are set at 9 time. After allowing time to read 9 holes, a read scan is taken. The start of the scan is further conditioned by the priority controls and the fact that a scan is not in process.

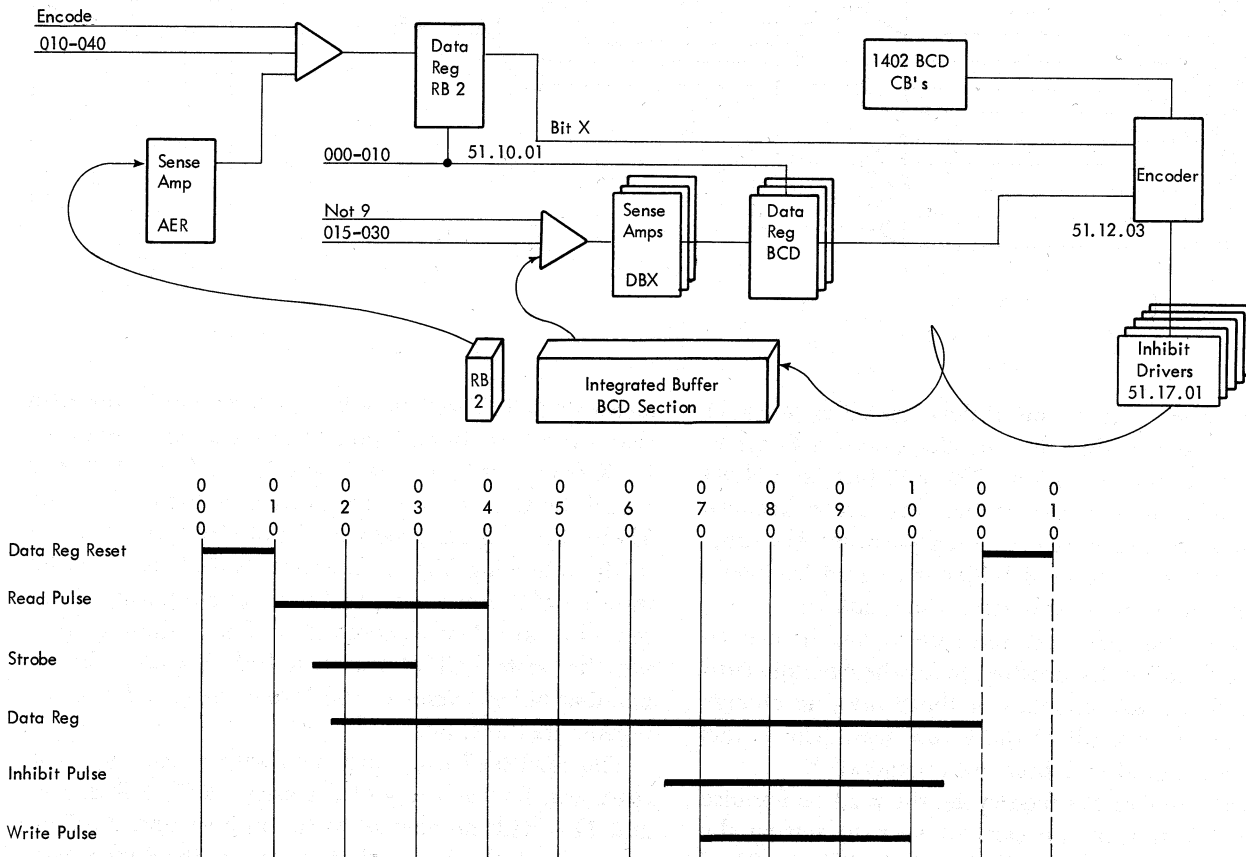
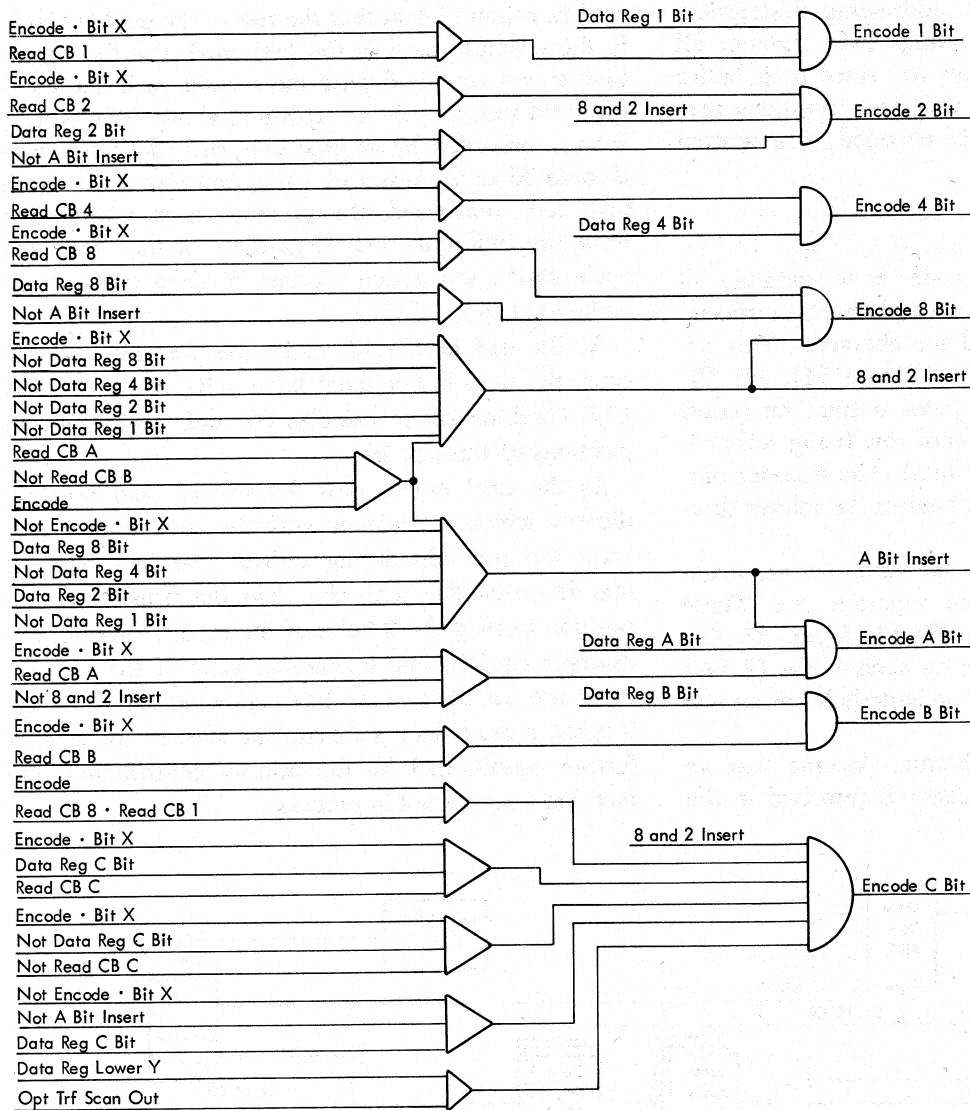


Figure 24. Read Buffer Storage Cycle



Card Row	CB
12	A · B · C
11	B
0	A
1	1
2	2
3	1 · 2 · C
4	4
5	1 · 4 · C
6	2 · 4 · C
7	1 · 2 · 4
8	8
9	1 · 8 · C

Figure 25. Read Encode

The read scan at 9 time differs from the other 11 scans to follow in that the encoder causes a C bit to be placed in all 80 positions. These C bits are placed in the buffer on the first of the read scans because parity must be generated for each position. Also during this first scan the read buffer is cleared by blocking the strobe pulse to the BCD sense amplifiers.

The card then advances until the 8 row is in position to be read by the brushes. Since the example card does not have any punches in the 8 row, no change takes place as a result of the 8 row scan. The C bits that were inserted at 9 time are regenerated.

At 7 row time of the feed cycle, the read CB impulse causes the 7 row of the card to be read setting the row bit core at position 00 (7 hole in column 01 of the example card). After the read time, a read scan is

again started. The first buffer cycle of this 7 row read scan causes the three inputs to the read encoder to be: bit X from position 00 of row bits, read CB's 4, 2, and 1, and the C bit of the 7 data bits from the read buffer. These three inputs produce outputs from the encoder of the following bits: 1, 2, and 4. Note that the C bit inserted at 9 time is dropped to maintain parity. These three bits are then written into buffer position 00 during the write half of this first buffer cycle. The remaining buffer cycles of the 7 row scan read out and regenerate the C bits.

The card feed cycle proceeds with a read time and read scan for each row of the card - 6, 5, 4, 3, 2, 1, 0, and 11 - with no change to the buffer contents. During each of the scans, 6 through 11, the buffer contents are read out and because of the lack of bit X

are regenerated and unchanged through the encoder.

At 12 time of the card feed cycle the 12 hole in column 1 reads and sets the same row bit core in position 00 that was set at 7 row time. The 12 row scan is started, and after the read half of the first buffer cycle, the encoder inputs are: bit X; read CB's A, B, and C; and data register 4, 2, and 1. These inputs to the encoder cause outputs of 1, 2, 4, A, and B bits, the correct BCD coding for an alphabetic G. The remaining buffer cycles of the 12 row scan (positions 01 through 79) regenerate the C bits; so, at the end of the 12 read scans the buffer contains the correct information.

Other examples could prove the fact that the encoder is capable of providing the correct BCD character of any valid combination of the 960 possible card holes.

CB Impulses

Figure 26 is a timing chart for the read CB impulses and their relation to the read brush timings. The brush impulse CB and CB reset timings shown are the resultant timings of several individual CB's. For the individual breakdown of these pulses, refer to the 1402 timing chart.

The read CB's that are used to identify the card rows for the encoder are also shown in Figure 26. These CB impulses are brought into the 1414 and gated by the brush single shot to set a latch (Systems 51. 20. 01 and 02). These latch outputs are then used as the CB inputs to the encoder and are reset by the CB reset at the beginning of each row time.

Priority

As previously explained, the integrated buffer requires a scan to read in a row of a card. Although there are different kinds of scans (transfer, punch, reader option), the differences are in the way the scan is started. All buffer scans cause the addressing rings to step and to read out and write in positions of a selected buffer section. Because there is only one set of address rings, drivers, inhibit drivers, sense amplifiers, and data registers to serve all sections of the buffer and because the I-O devices using the buffer sections operate at different speeds, some system of sequence of use must control the start of a scan. With more than one I-O device operating simultaneously, the time comes when two or more I-O devices need to use the buffer rings (request a scan) at the same time. This paradoxical situation provides the need for the

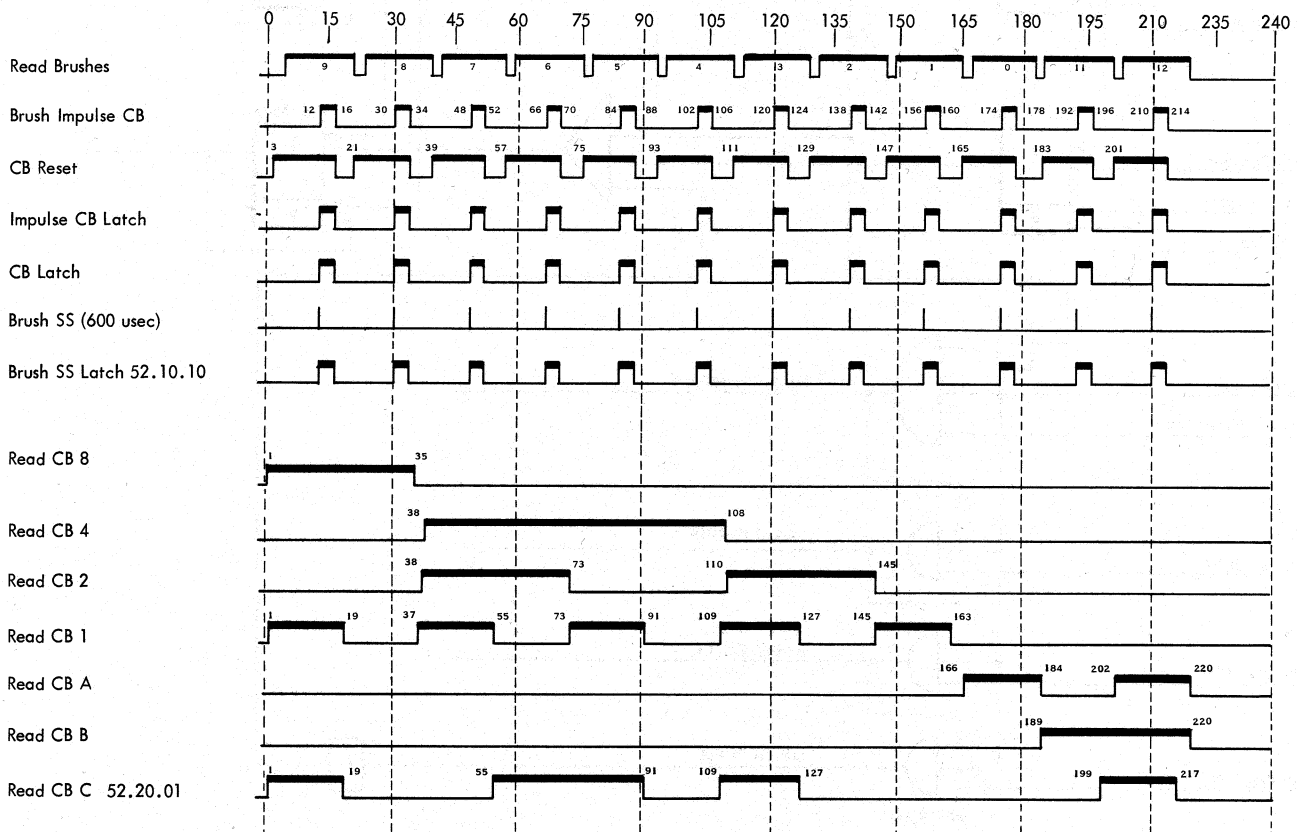


Figure 26. Reader CB Timings

the sequence. A priority request blocks any other request that is assigned a lower position in the sequence.

“Read Priority Gate” turns on the read priority request trigger in Figure 27. The read priority gate can be brought up two different ways. The read request trigger requests a read scan for each row of the card. The read transfer trigger requests a read scan as a result of a CPU read instruction. The flow chart in Figure 28 gives the sequence for both types of read scan.

Read Buffer to CPU

At the end of the read feed cycle the reader waits for the CPU to issue a read instruction. If the time between the read instruction from CPU is short enough (less than 65 ms), the read feed of the 1402 will run continuously (unless the hopper empties, a stacker fills, or an error occurs).

The execution of the read instruction causes 80 characters of information to be sent to the CPU. This is called a transfer scan. A transfer scan differs from the read scans for a particular row of a card in one way – the read encoder is not used. Priority circuits are used to turn on the same read scan trigger (Figure 29) which causes a read scan, but the fact that read request is off prevents the line “encode” from controlling the encoder. The data register outputs are sent unchanged through the encoder onto the read bus to CPU.

The start of a transfer scan requires the turn on of “read transfer request” (Figure 30). The CPU starts the transfer scan by the line “ready to buffer” turning on the ready 2 latch (Systems 51. 40. 04). If no other scan is in process, the ready 1 latch turns on at 040-050 time. Then, if the reader is ready (mechanically) and not busy, the read transfer request latch turns on. From this point on, the transfer scan is just like the read scan described above. The data flow for the transfer scan is shown by heavy lines in Figure 31.

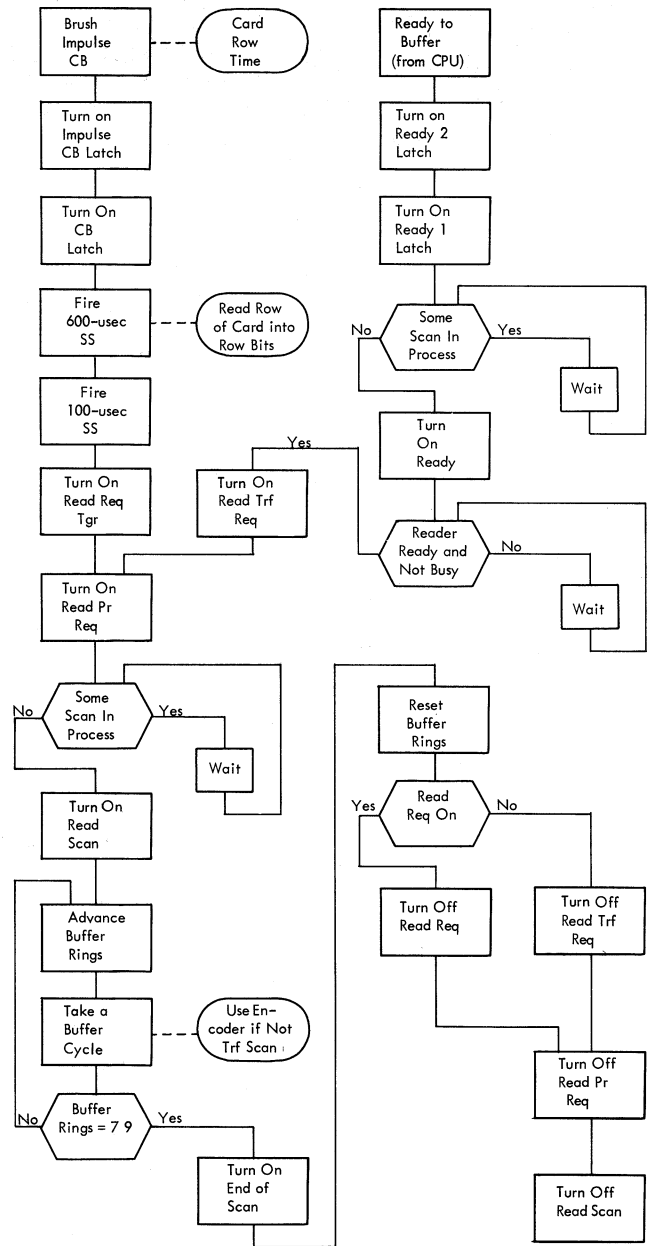


Figure 28. Reader Priority Controls

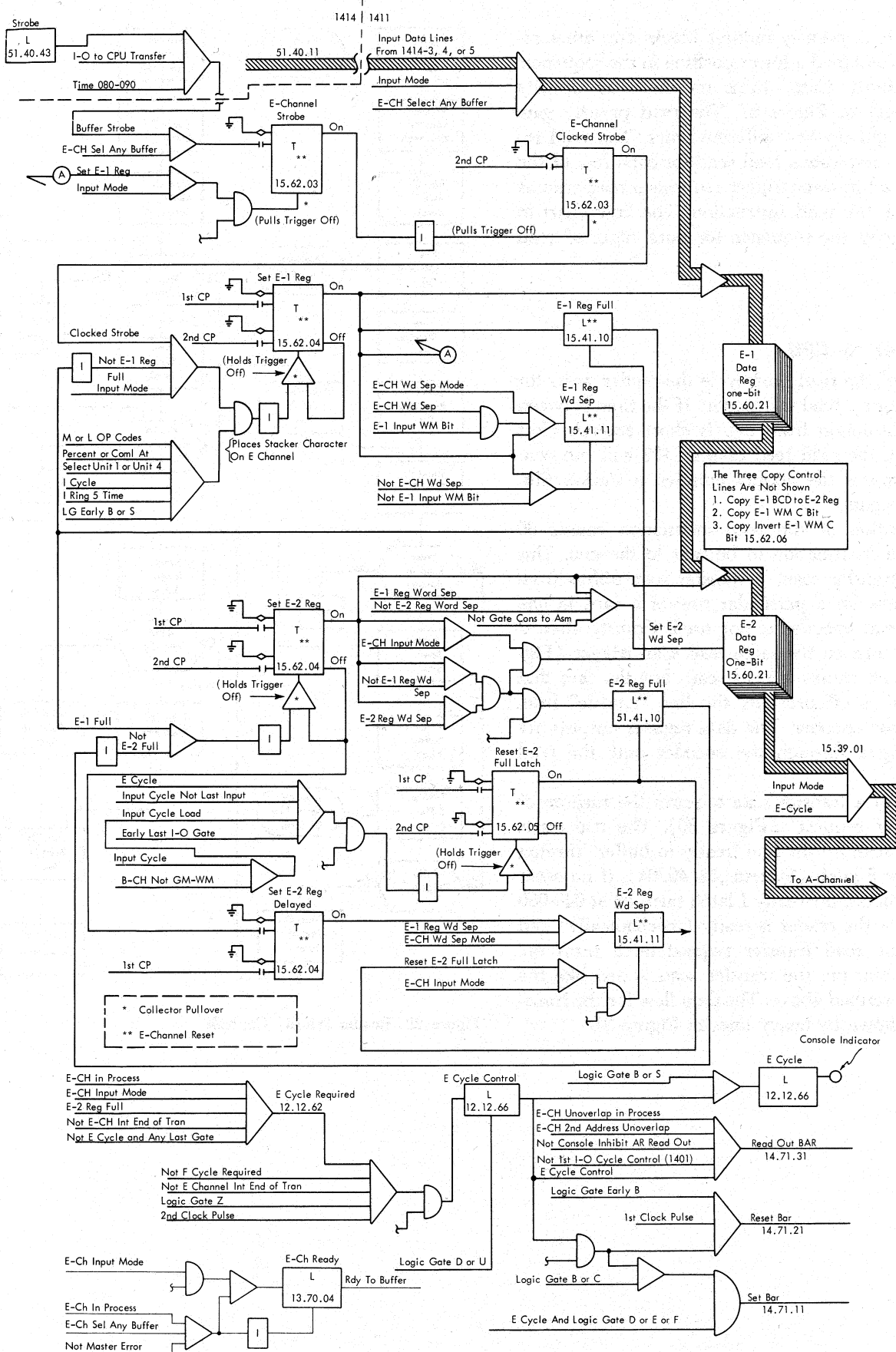
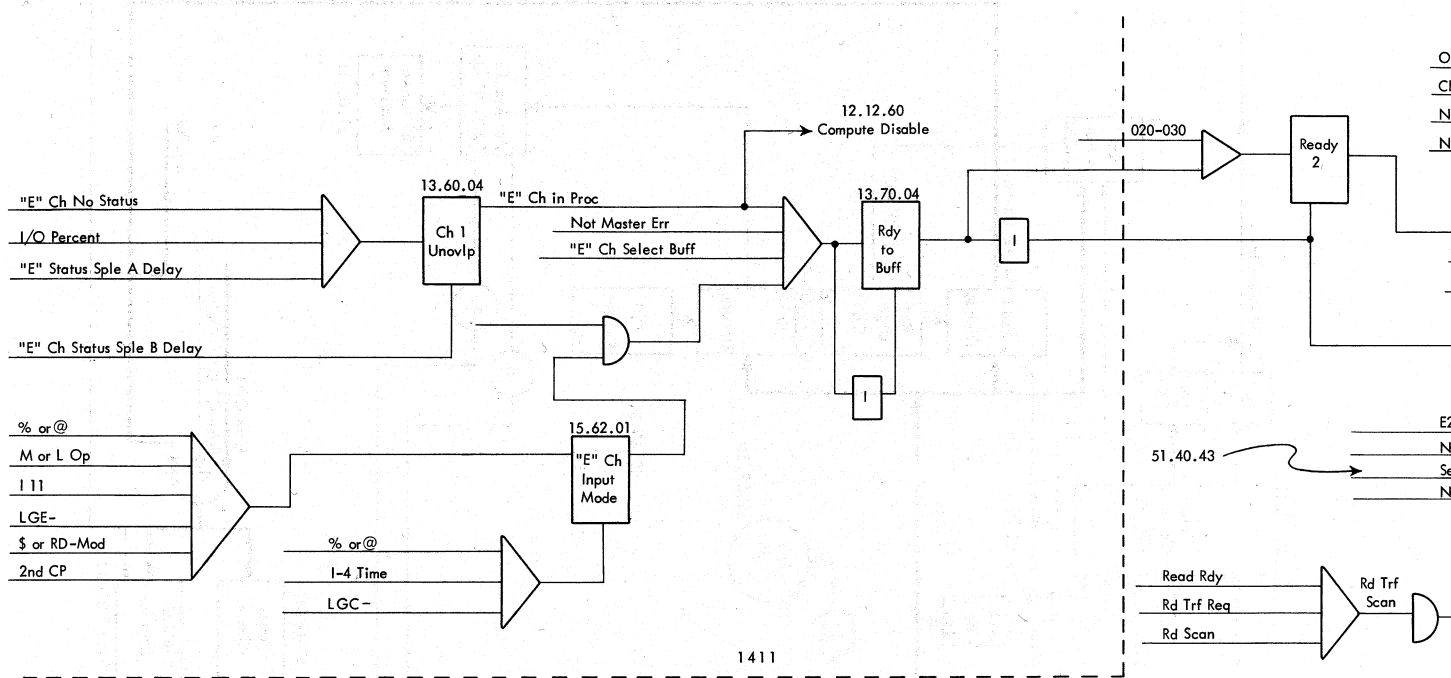


Figure 29. Channel Register Operations - Reader



1411

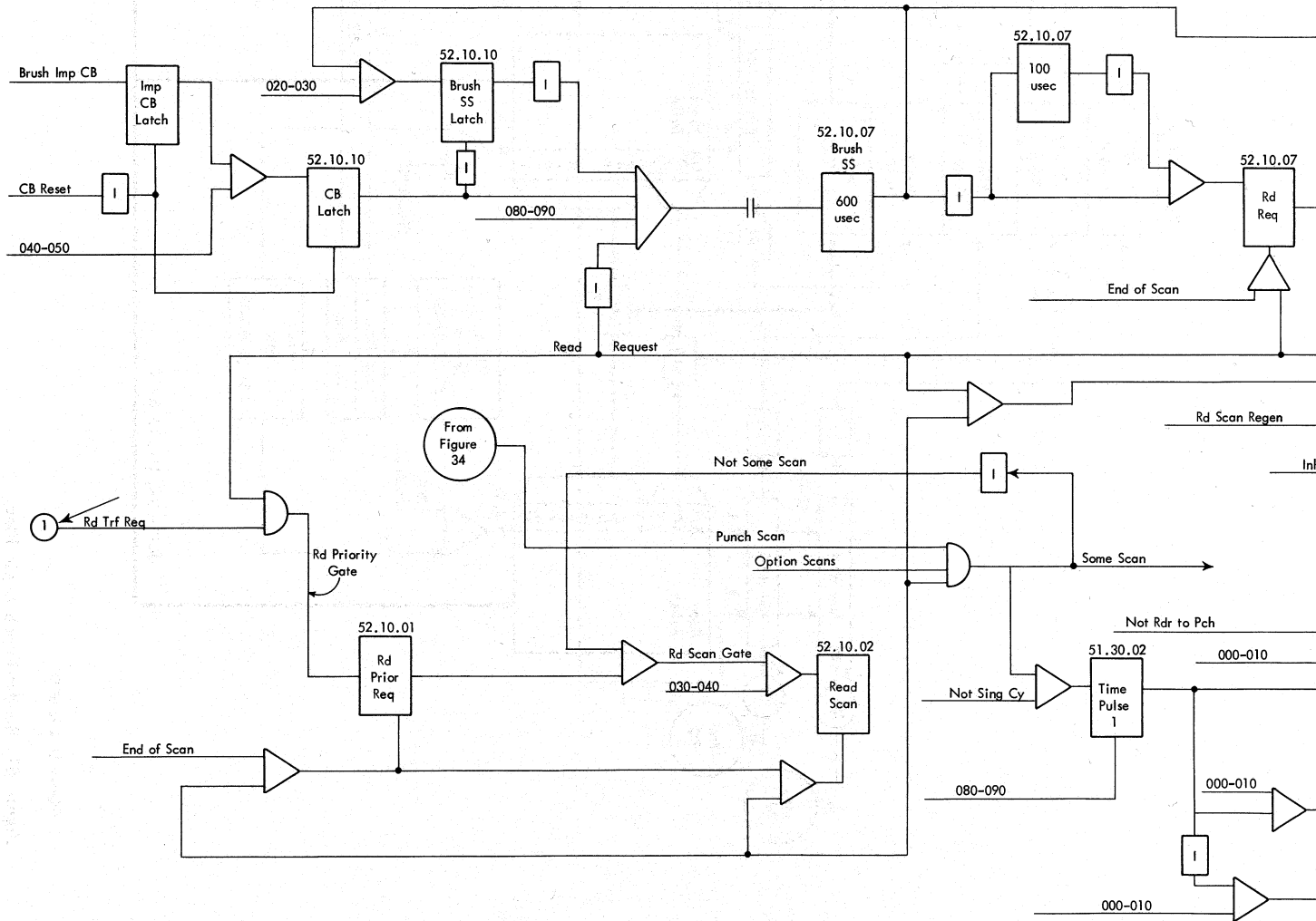
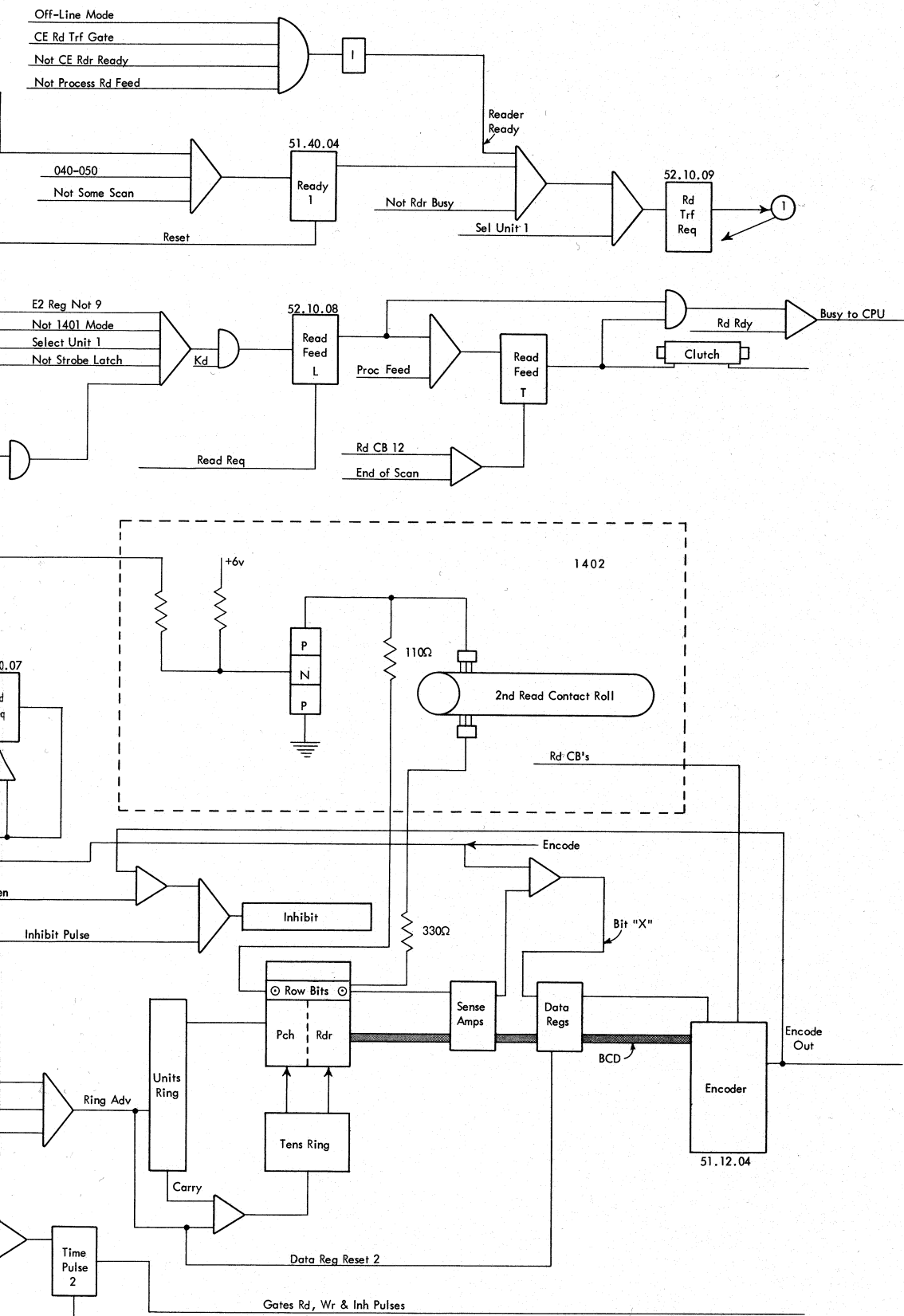
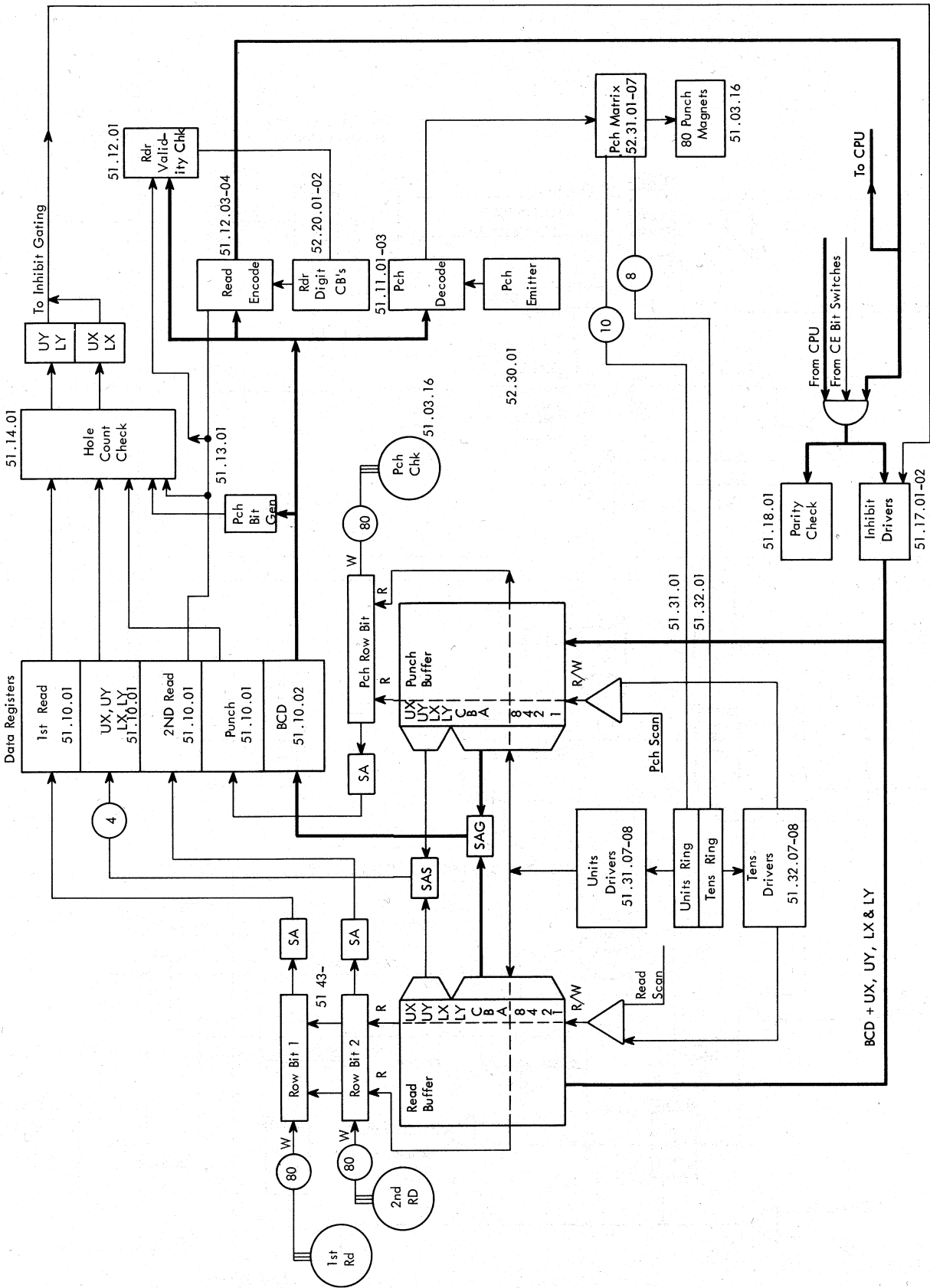


Figure 30. Reader Logic





(Heavy Line is BCD)
 Figure 31. Reader-Punch Logic Flow

The card punch section of the 1402 operates independently of the reader section. Either reader or punch or both can process cards at the same time. The speed of a buffer scan (880 usec) compared with the mechanical motion of cards (240 MS per card and 15 MS between rows of the punch feed cycle) is such that reader and punch can actually be in motion simultaneously.

A card punch operation is quite similar to a read operation, but in the reverse sequence. A transfer scan fills the punch section of the buffer with data from CPU, the punch clutch is energized to start the punch feed cycle, and the punch buffer is scanned out and decoded for each row of the card.

CPU to Buffer

A card punch operation is started by the execution of a CPU instruction that stores 80 characters of data in the punch section of the buffer. Before this transfer scan can start, the punch must be made ready. The operator must place blank cards in the hopper and press the start key. Relay circuits cause two run-in cycles. At the end of run-in, a blank card is in position just before the punching station so that the next feed cycle will move this first blank card past the punching station. If run-in is correctly completed (no card jams, hopper not empty, stacker not full), the punch is ready.

With the punch ready, the CPU can initiate the sequence of operation to punch a card. The same "ready to buffer" line used for reader signals to the 1414 that CPU is ready to start the transfer scan (Figures 32 and 33). "Ready to buffer" turns on the ready latches (Systems 51.40.04). "Ready 1" ANDed with "punch ready," "punch not busy," and "select unit 4" turns on the punch transfer request trigger which turns on punch priority request. After satisfying the priority requirements (Figure 27), punch scan is turned on and the transfer scan can start (Figure 34).

The transfer scan consists of 80 buffer cycles, and 80 characters of data are moved from CPU to the punch buffer. Before the first data character is transferred, the stacker select character must be processed. This character (0, 4, or 8) is part of the CPU instruction which permits the program to select one of the available stackers. This stacker select character comes into the 1414 on the data bus the same as a data character, but is stored in latches before the start of the first buffer cycle (Figure 34). The operation of

the QD circuit provides the delay of one punch feed cycle needed to stack the card. This cycle of delay is needed because at the start of the transfer scan the card is ready to enter the punching station and the stacker select station is one full feed cycle later. The QD circuit is a relay driver that has a logical AND circuit on its input (Figure 35). The gate must be active (minus) before the set goes active (minus to plus), or the driver is not turned on. The punch stack select latch (set) is on before the stack four or eight latches are turned on (gate). Therefore, the stacker four or eight driver latches cannot turn on until the following transfer scan when the punch stack select latch turns off and back on again. Figure 36 shows the timings for the start of a transfer scan and the timings of the start of the punch feed cycle.

Punch Buffer to Card

At the end of the transfer scan that fills the punch buffer, a test of the error circuits in the CPU determines whether or not the transfer is correct. The lack of an error at this time allows the CPU to send the signal "correct transfer to buffer" to the 1414. Correct transfer to buffer signal turns on the punch feed latch (Figure 37) which energizes the punch clutch to start the punch feed cycle. From this point on, the operation is under the control of punch CB's in the 1402.

Punch Decode

The 80 characters of data stored in the punch buffer are in BCD form. To punch these characters into a card, a reverse of the process described under reader encoding, called decode, changes the characters from BCD to card code.

Decoding the characters (Figure 37) requires a punch scan of the punch buffer for each of the 12 rows of the card. A CB in the 1402 that makes for each row of the card requests the scan. The punch decode emitter identifies the card row and controls the punch decoder. As the scan for each row is taken, all 80 positions of the punch buffer are read out in sequence and regenerated. The output of the decoder feeds the punch matrix which, under control of the units and tens buffer rings, energizes the punch magnets.

For example, if position 00 of the buffer contains a "G" (B, A, 4, 2, and 1 bits) and the other buffer

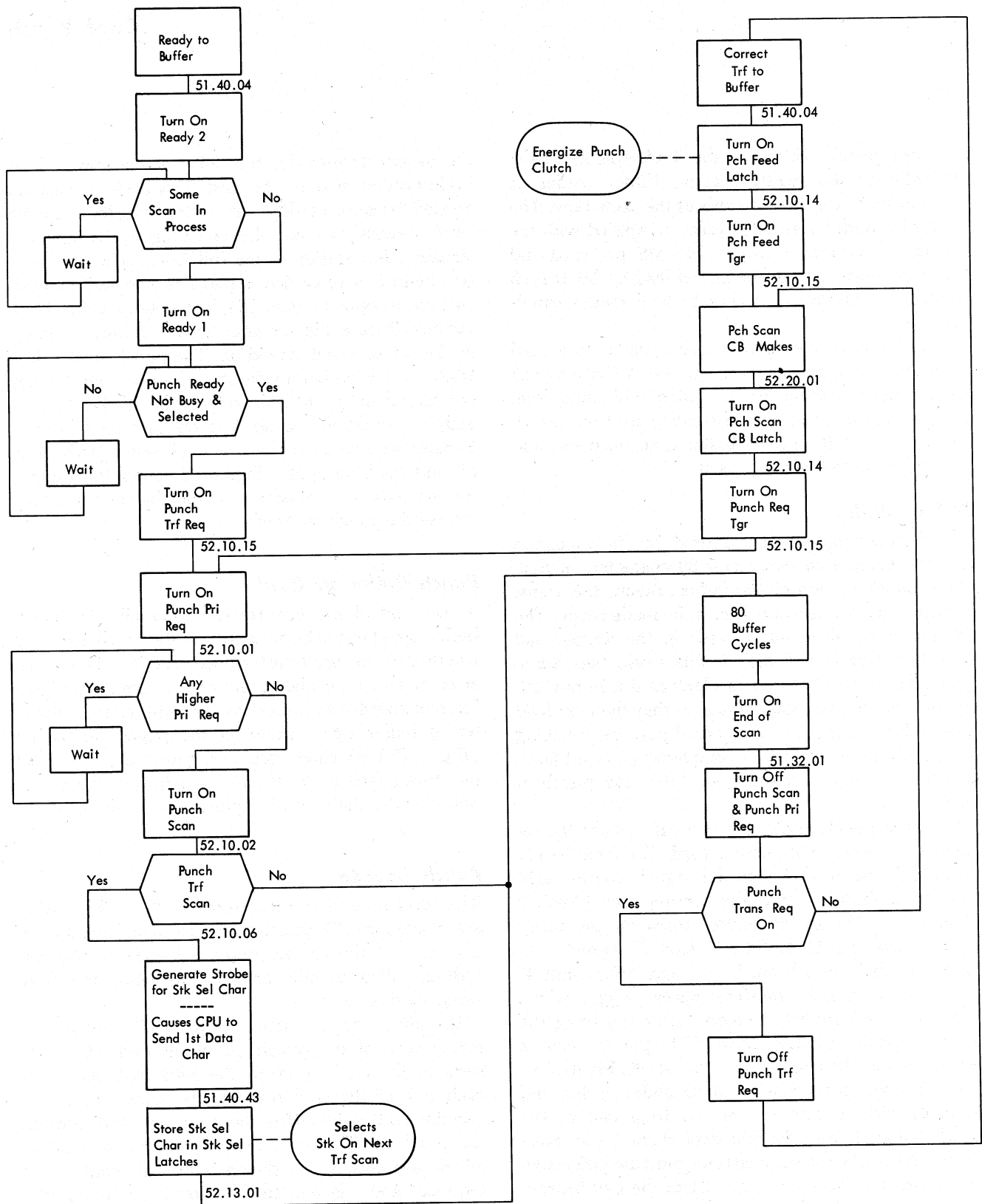


Figure 32. Punch Scan Controls

positions are blank, the card must have two holes punched — one in the 12 row of column one, and one in the 7 row of column 1.

Assume that the punch is ready and not busy, and that the transfer to punch buffer from CPU was correct. The correct transfer to buffer signal starts the punch feed cycle which causes the blank card to start feeding past the punching station. Shortly before 12 row time, the punch scan \overline{CB} sends an impulse to the 1414 that requests a punch scan. If no higher priority scan has been requested and no other scan is in process, the scan for the 12 row is started. The first buffer cycle of this scan reads out the "G" in position 00 and sends it into the punch decoder (Figure 37). The punch decoder combines the B, A, 4, 2, and 1 bits with the punch decode emitter and produces an output that is sent into the punch matrix. The punch matrix is conditioned by the units and tens rings (00) and energizes the punch magnet driver for column one of the card. Because the remaining 79 positions of the buffer contain only C bits, the 12 row scan does not energize any more punch magnets.

After the 12 row scan is completed, punch \overline{CB} 's (PA 5-8) complete the circuit to the punch magnets and

punch the hole in column one (12 row). The punch scan \overline{CB} makes again for the 11 row of the card, to start another scan. This example has no BCD characters to decode that require 11 row punches, therefore no punch magnets are energized for the 11 row scan. Each scan causes all 80 positions of the buffer to be read out and regenerated, but the punch decoder determines if any punch magnet is to be energized and the buffer rings through the punch matrix determine which punch magnet, if any, is energized.

This example card continues feeding and a scan for each row repeats for the 0, 1, 2, 3, 4, 5, and 6 rows without punching any holes. The 7 row however, causes the decoder to again energize the column 1 punch magnet. The 8 and 9 row scans, like the 11 through 6 scans, do not cause any punching. After the 9 row of the card has had time to punch, a \overline{CB} called the after 9 \overline{CB} makes to start one more scan. (This thirteenth scan is used to complete the hole count checking which is described in the checking features section). Thus the card is punched with two holes in column one, a 12 and a 7, the correct card code for a "G."

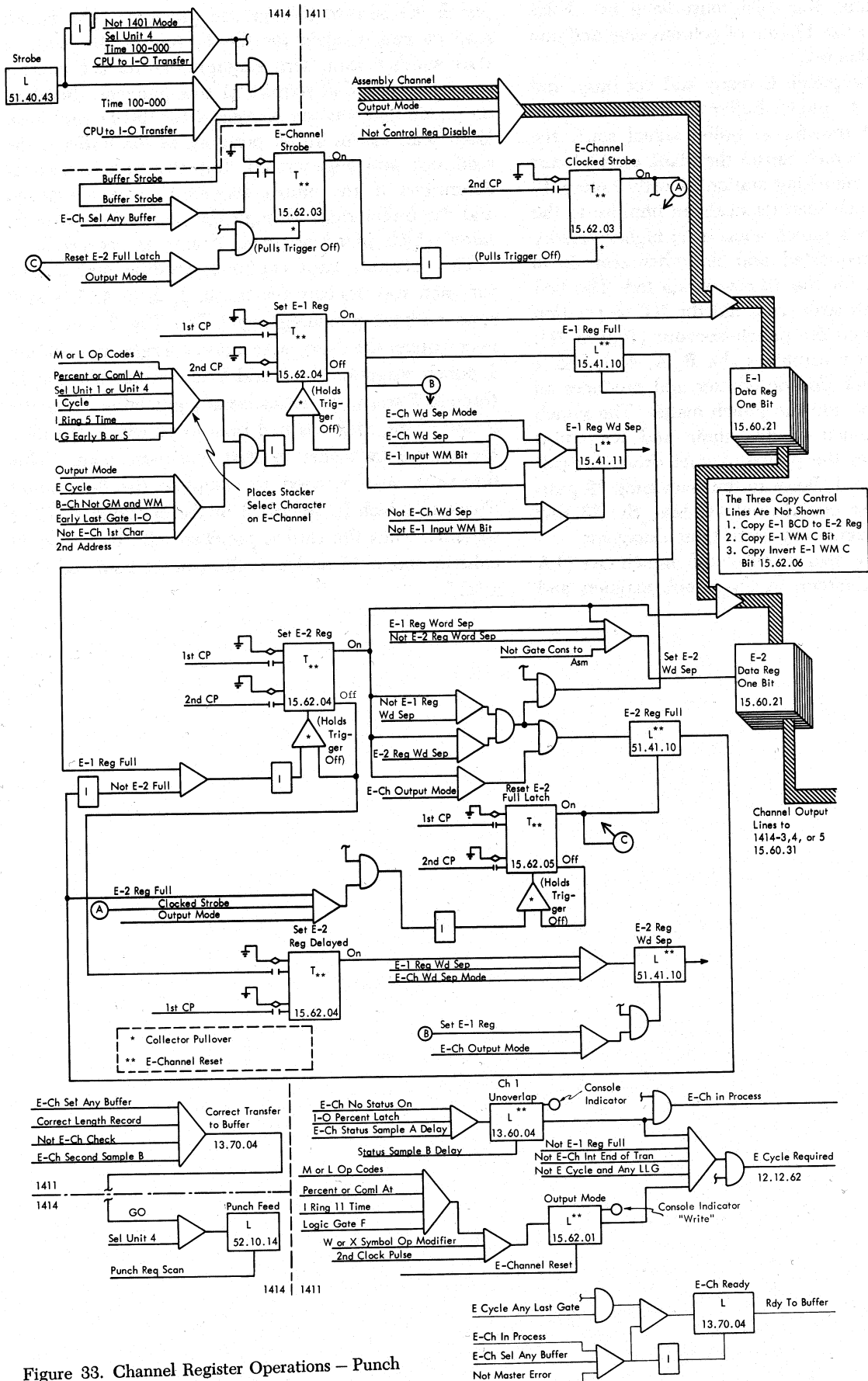
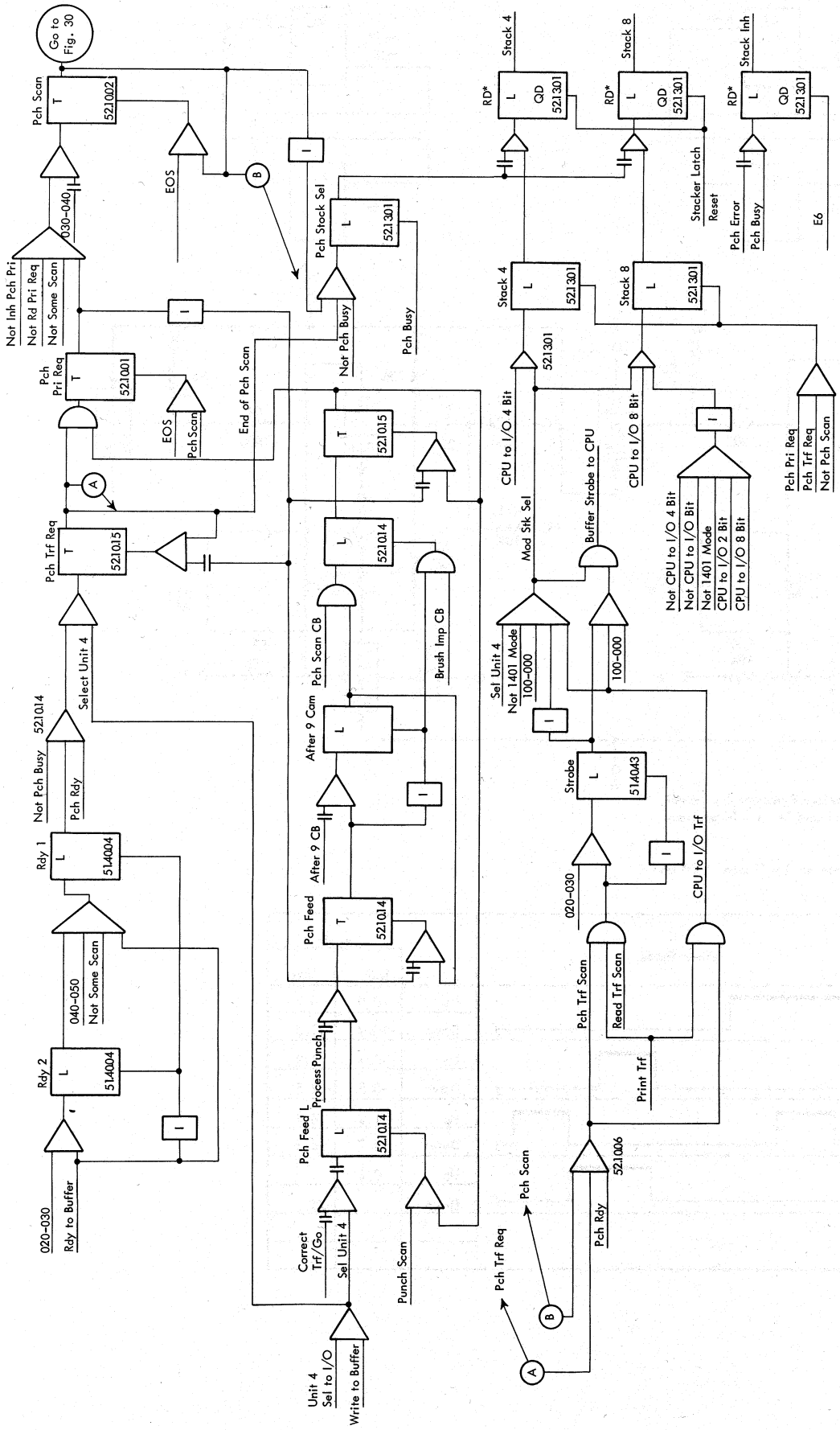
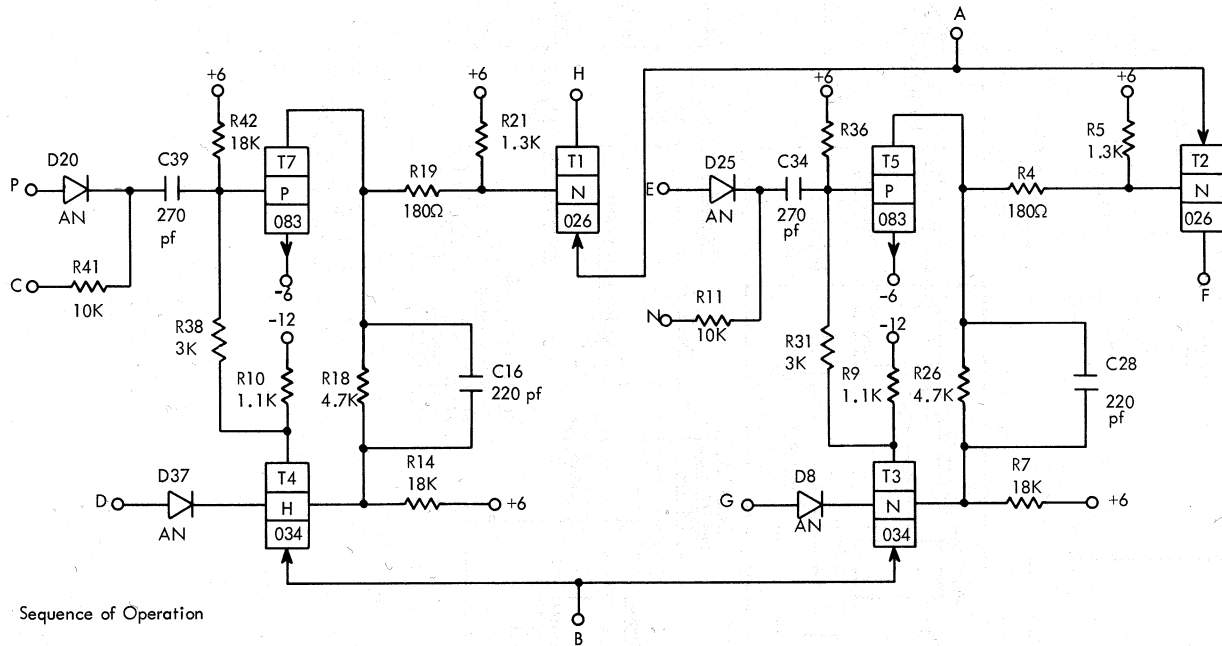
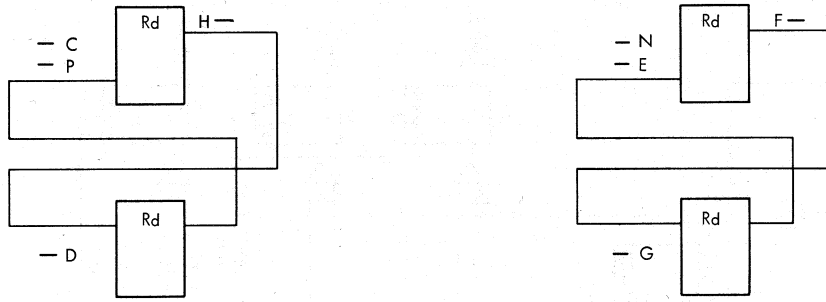


Figure 33. Channel Register Operations – Punch



*See Text

Figure 34. Punch Controls



Sequence of Operation

1. Pin C must be down 7.5 usec before P goes to "up" level, turning T7 on. "T7 on" turns T1 and T4 on. T4 provides latch back to hold T7 on.
2. Up level at D or mechanical reset at B will turn T4 off and open latch back to T7.

Pins	Signal Name	Wave Shape	Levels		
			Min	Max	
C, N	U	Input	Up	-3.0	0.2
			Down	-10.0	-12.5
P, E	U	Input	Up	-0.5	0.2
			Down	-8.5	-12.5
D, G	T	Reset	Up	1.4	6.2
			Down	-0.7	-6.2
H, F	W	Output	Up	0.2	
			Down		-45

Figure 35. qD Card Circuit

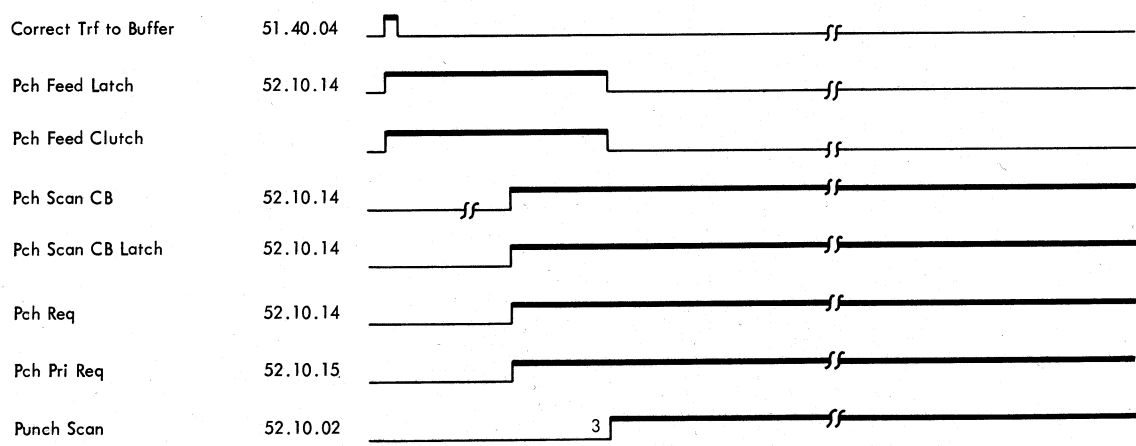
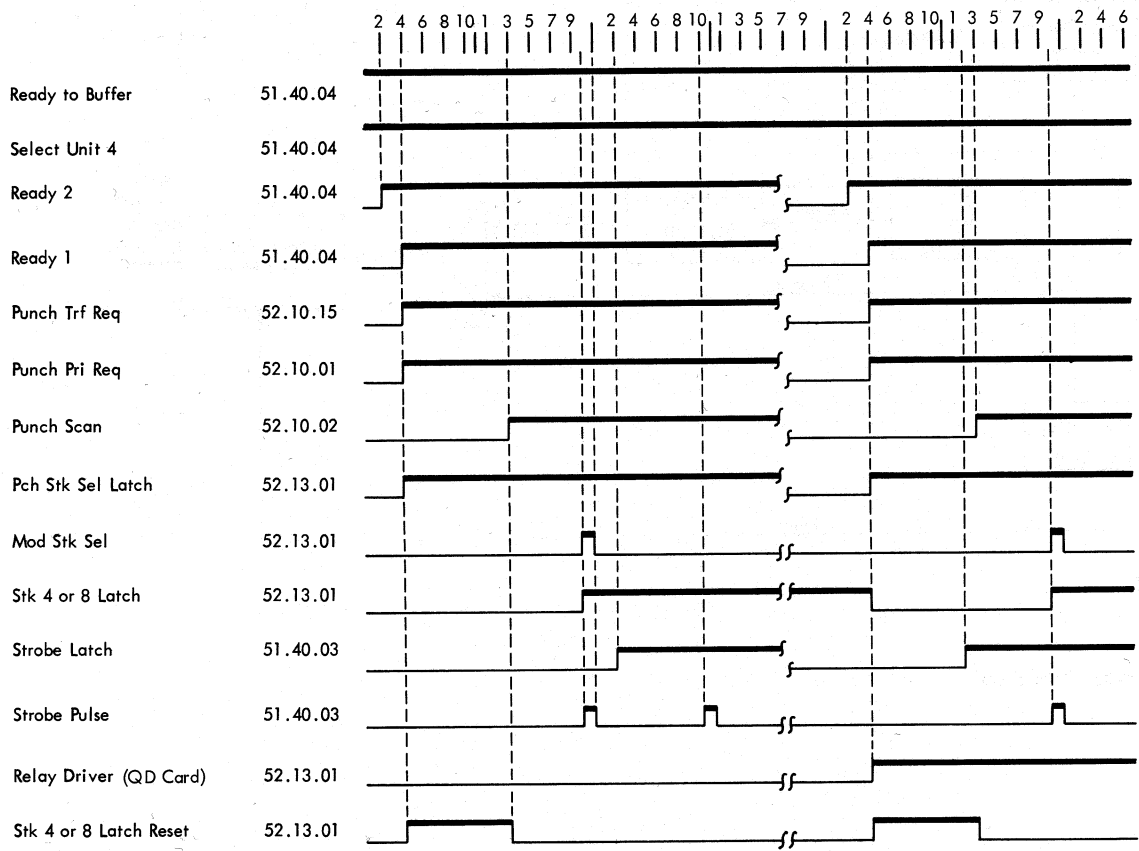


Figure 36. Punch Scan Timings

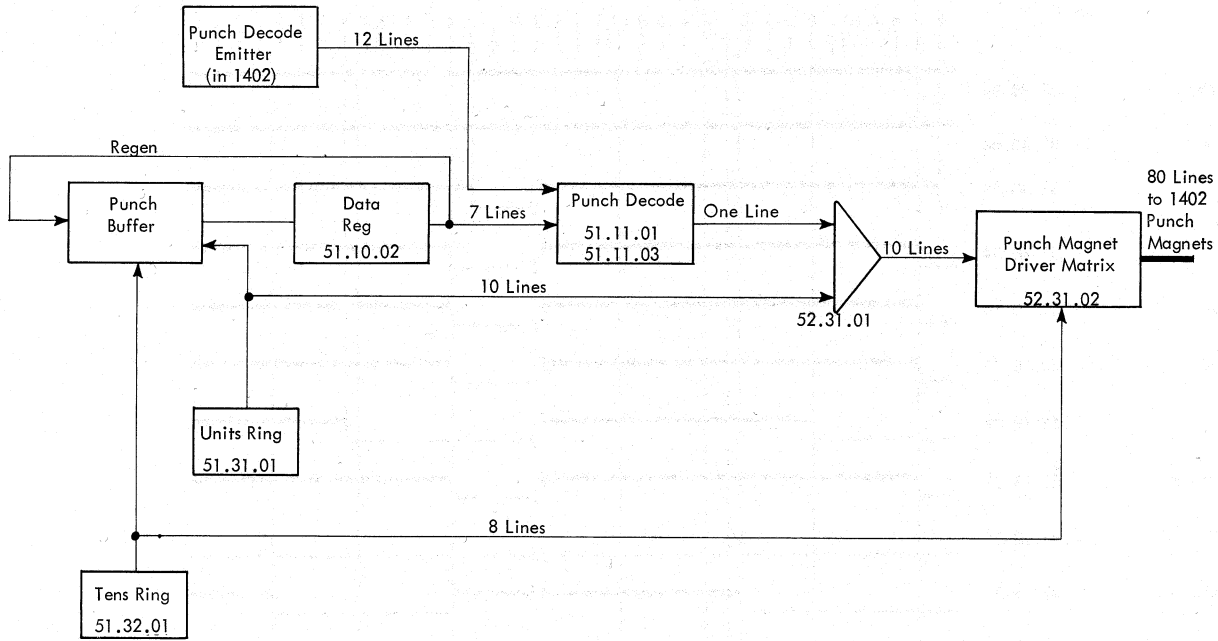


Figure 37. Punch Scan Data Flow

Parity Check

Information is stored in the integrated-synchronizer core-storage unit in odd parity form. That is, every character must contain an odd number of bits. The bits that are set up at the inhibit driver inputs are switched to two parity check triggers (Figure 38 and Systems 51. 18. 01). Both triggers are reset off at the beginning of each memory cycle. Binary trigger inputs allow each trigger to flip on and off with successive set pulses. The C, A, 4, and 1 bits are switched to the upper trigger at 6, 7, 8, and 9 times, respectively. The B, 8, and 2 bits are switched to the lower trigger at 6, 7, and 8 times, respectively. If there is an even number of bits at the inhibit driver inputs, the two triggers are either both on or both off at ten time when the error sample occurs. An odd number of bits causes the triggers to be opposite (not both on or off)

when they are tested at ten time, in order to prevent an error. On a serial device, the 8th, or control, bit must be considered in the parity check of each character. This 8th bit is accounted for by an entry to the lower trigger at 9 time.

Ring Check

A ring check circuit maintains a constant check on the proper progression of the units and tens ring triggers except for two stages on at the same time. For each ring, there is a check trigger driven by the corresponding ring drive pulse. Each check trigger has a binary input; therefore, each incoming drive pulse flips the trigger to the opposite state. The outputs of the check triggers are compared with the outputs of the corresponding ring triggers. The check triggers should be on when the even numbered ring triggers

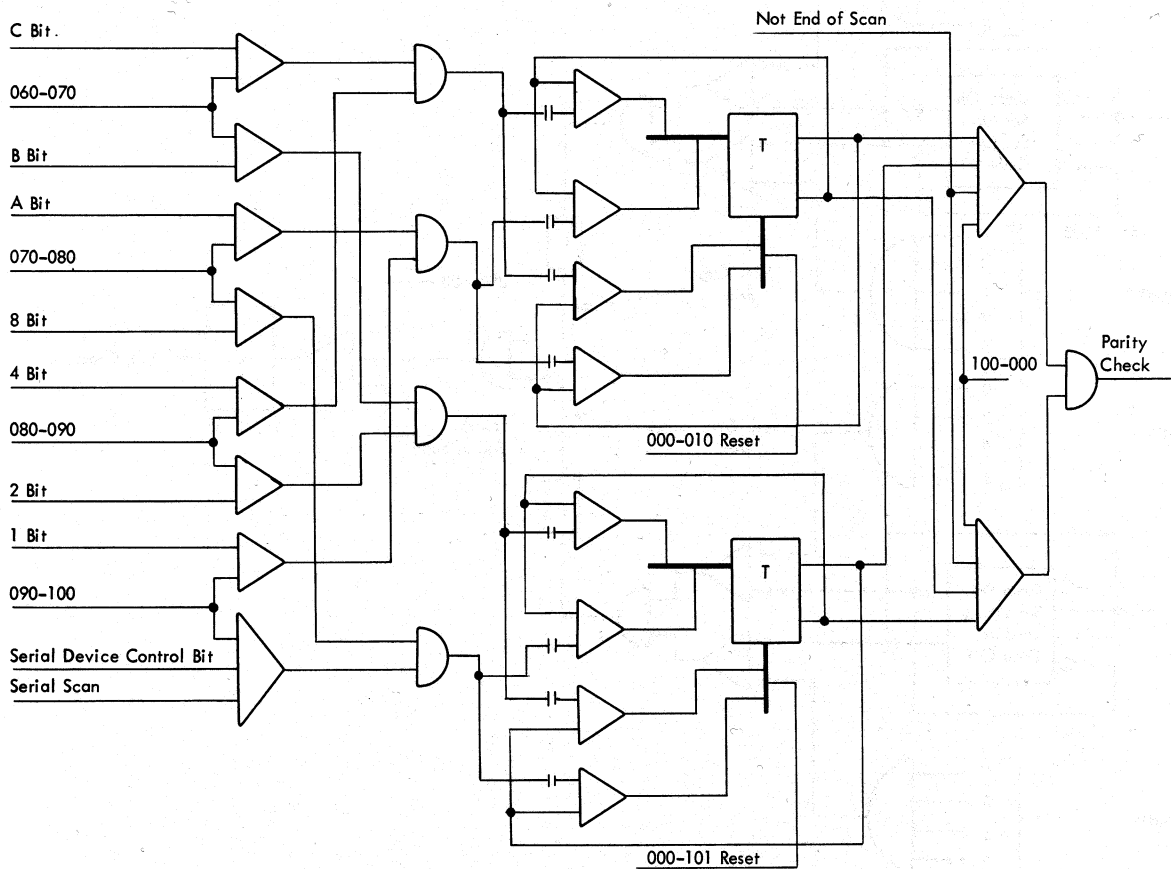


Figure 38. Integrated Synchronizer Parity

are on, and off when the odd numbered triggers are on. Any deviation from this indicates incorrect ring progression and produces a ring check (Figure 39 and Systems 51. 31. 02, 51. 32. 02).

The ring check, in addition to resetting all ring triggers, sets the check latch of the unit that is being addressed when the error is detected. For example, if a ring check occurs during a punch scan, the punch check latch is set.

Clock Check

The clock check circuit detects any incorrect progress of the clock triggers. Clock pulses drive a binary input check trigger. Because the memory cycle has an odd number of pulses, the check trigger resets ON at zero time of each memory cycle. The check trigger (reset ON at zero time) is on at 0, 2, 4, 6, 8, and 10 times, and off at 1, 3, 5, 7, and 9 times. The outputs of the even numbered clock triggers are compared with the ON output of the check trigger. The outputs

of the odd numbered clock triggers are compared with the OFF output of the check trigger (Figure 40).

If a clock check occurs, the clock triggers are reset and allowed to restart. In addition, the check latch of the unit that is being addressed is set to indicate a data error. To start the clock initially, a clock error is forced to reset all triggers OFF except 0-10 time. The bottom AND circuit in Figure 40 produces a clock error signal at 10 time if more than one stage of the clock turns on at the same time.

A clock error is developed by clock pulses mixing with the clock check trigger outputs. Then the clock error line resets the clock triggers which removes the condition that produces the clock error. This sequence results in a close timing condition that would cause a failure of the clock error line to operate reliably if it were not for the trigger at 5J on Systems 51. 30. 01. The purpose of this trigger is to make sure the clock error line is active long enough to reset the clock and turn on an error indicator. This trigger (at 5J) is reset

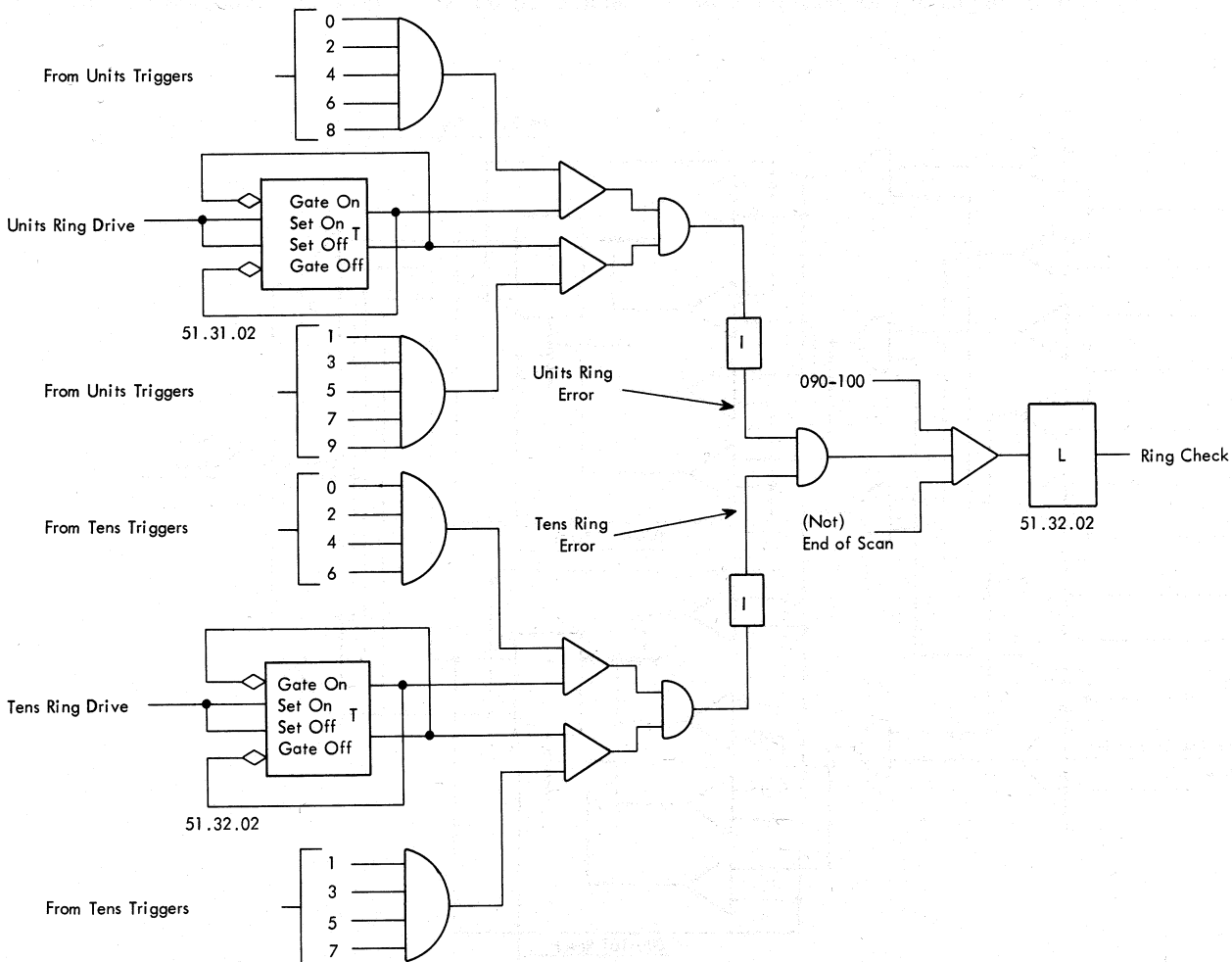


Figure 39. Ring Check

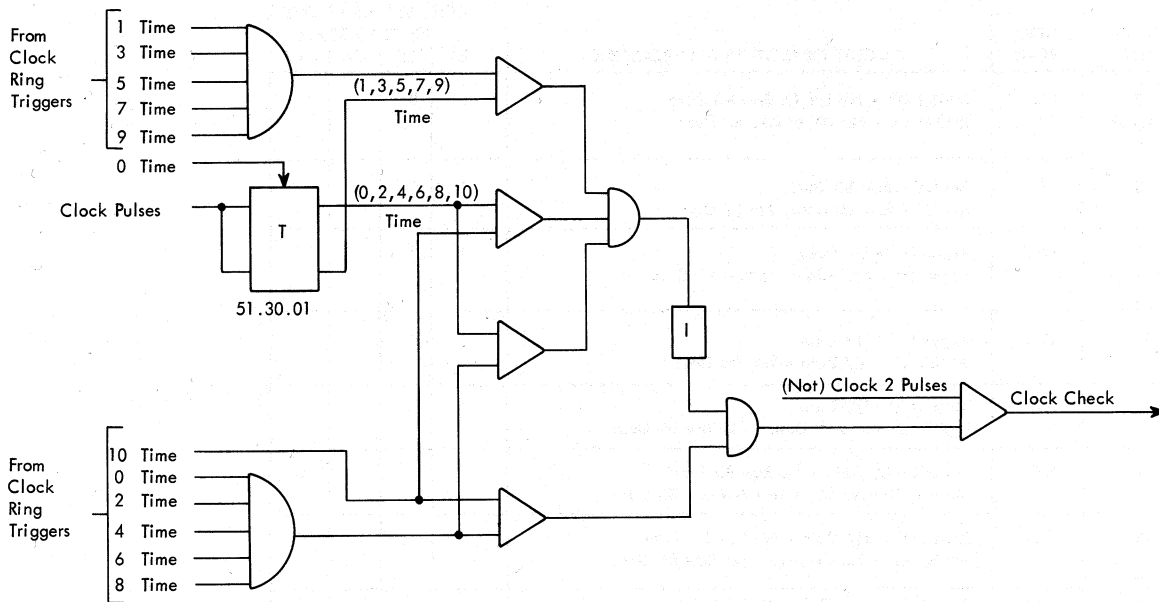


Figure 40. Clock Check

off by the power on reset line. When a clock error occurs, the oscillator pulse that steps the clock into the error condition is the clock AC set line from the inverter at 6B. "Not clock 2," which comes half a clock time later, samples the error through the AND circuit at 6D and brings up the clock error line through the inverter at 6H. The input to this inverter feeds into pin P of the trigger at 5J pulling it on (collector pull-over). The trigger stays on until the rise of the next "not clock 2" pulse keeping the clock error line active for a full microsecond.

Hole-Count Check

OPERATION

To ensure integrity of card input-output data, the 1414 uses a hole-count check circuit that consists of eight 80-core planes and their associated circuitry. Four of these are used by the card reader and four are used by the card punch. These planes are labeled *Upper X* and *Upper Y*, and *Lower X* and *Lower Y* for each machine.

Hole counting by the card reader is a comparison of the number of holes that are counted in each card column at the two read stations. Essentially, the machine counts the holes in each column of a card when it is read at the read-check station. It then subtracts the holes in each column from the same card when it reaches the read station. The result should always be zero, because the same number of holes should be read at both read stations.

There are two hole-count check cores that are associated with each read-one and read-two-row bit-core position.

The upper Y(UY) and lower Y(LY) cores do the counting at the read-check station. The upper X(UX) and lower X(LX) cores count the information from the read station.

At the beginning of the card feed cycle, all cores are in the 0-status. During every read scan, all 80 positions of the check cores are successively addressed and are set with the required hole-count information.

The first hole in each card column that is sensed at the read-check station causes both Y-cores associated with that column to flip. Thereafter, the UY-core remains unchanged, while the LY-core status is reversed with each successive hole that is read in its respective column. At the end of the first card-feed cycle, the reader Y-planes define two conditions for each card column: whether a hole was read (UY), and whether the total count was odd or even (LY). At reader-9-time during the next card-feed cycle, the contents of all 80 UY and LY cores are transferred to the X-plane circuits. As the card passes the read brushes, the punched card data combines with the transferred Y-plane data. The result, at reader-12-time, is a 0-status of all cores in the X-planes.

LOGIC (FIGURES 41 AND 42)

The memory cycle, that contains both read and write times, controls the status of the check cores. As each hole-count check position is addressed, the cores that

CARD FEED CYCLE	READER TIME	HOLE READ	CIRCUIT OBJECTIVES AND REASONS	CORE STATUS AT END OF READ SCAN			
				UY	LY	UX	LX
1 ↓	9 Through 4	NO	Inhibit UY - No UY Or Row Bit Data Inhibit LY - No UY or Row Bit Data	0	0		
	3	YES	Set UY - Row Bit Data Set LY - Row Bit Data, No LY Data	1	1		
	2 Through 0	NO	Regen UY - UY Data Regen LY - LY Data - No Row Bit Data	1	1		
	11	YES	Regen UY - UY Data Inhibit LY - LY Data - Row Bit Data	1	0		
	12	NO	Regen UY - UY Data Inhibit LY - No LY Data - No Row Bit Data	1	0		
2 ↓	9	NO	Set UX - Uy Data - No Row Bit Data Inhibit LX - No LY Data - No Row Bit Data			1	0
	8 Through 4	NO	Regen UX - UX Data - No Row Bit Data Inhibit LX - No LY Data - No Row Bit Data			1	0
	3	YES	Inhibit UX - UX Data - Row Bit Data Set LX - No LY Data - Row Bit Data			0	1
	2 Through 0	NO	Inhibit UX - No UX Data - No Row Bit Data Regen LX - LX Data - No Row Bit Data			0	1
	11	YES	Inhibit UX - No UX Data - Row Bit Data Inhibit LX - LX Data - Row Bit Data			0	0
	12	NO	Inhibit UX - No UX Data - No Row Bit Data Inhibit LX - No LX Data - No Row Bit Data Prevent Error - No Data To Cores			0	0

Figure 41. Hole-Count Check Example

are associated with that position read out in order to set data registers. The core-controlling circuit analyzes the read data along with incoming data from row-bit storage, and determines whether the core should be set or inhibited on the write portion of the cycle. This takes place 80 times for each of the 12 rows of information in a card.

CIRCUITS (FIGURES 43 AND 44)

The card with an L(11-3) punched in card column 2 is read in and checked by the card reader. The following discussion is based on a no-error condition.

1. At reader-9-through-4-time, no holes are read from the card. At reader-3-time, during the second memory cycle, the three punch from card column two is read out of read-one-row bit-storage (position two), and is switched to set both UY and LY cores for that

position. Both cores must be set, because this is the first hole that is read in that column.

SIGNAL	CONTROL	LOGIC
Data reg out 1st rd	Read pulse 010-040	51. 10. 01
Hole-ct to inh drvtr up Y	Data reg out 1st rd	51. 14. 01
Hole-ct to inh drvtr lwr Y	Data reg out 1st rd (not) Data reg out LY	51. 14. 01

2. During the second memory cycle of read-scan 11, position 2 of UY is regenerated, and the input to LY-core for position 2 is blocked, because this is the second hole that is read in that column.

SIGNAL	CONTROL	LOGIC
Data reg out 1st rd	Rd pulse 010-040	51. 10. 01
Hole-ct to inh drvtr UY	Data reg out uy or Data reg out 1st rd	51. 14. 01
(not) Hole-ct to inh drvtr LY	Data reg out LY	51. 14. 01

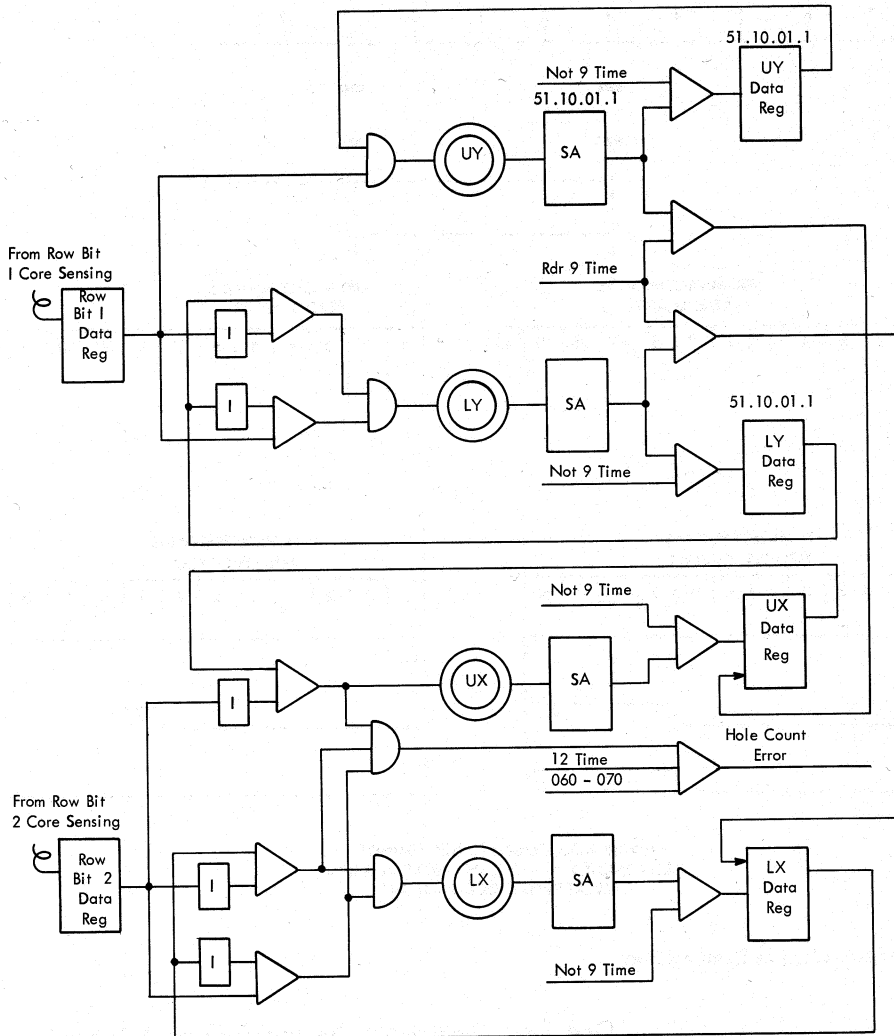


Figure 42. Reader Hole-Count Logic

3. At reader-9-time of the second card-feed cycle, the contents of all Y-cores are transferred to the respective X-cores on successive memory cycles. Before setting the X-cores, the Y-data is combined with any read-two-row bit-data that is present. In this case, however, no holes are read at 9-time, so that there is no read-two bit-data.

SIGNAL	CONTROL	LOGIC
Y A Trf	Rd scan Read-9-time Read pulse 010-040	52. 10. 05

4. At 3-time of the second card-feed cycle, the read-two-row bit-data from card column two combines with position-two X-core-data to prevent setting of position-two-ux, and to set position-two-lx.

SIGNAL	CONTROL	LOGIC
Data reg out 2nd rd (not) Hole-ct to inh drv up X	Rd pulse 010-040 Data reg out up X Data reg out 2nd rd	51. 10. 01 51. 14. 01
Hole-ct to inh drv lwr X	Data reg out lwr X (not) Data reg out 2nd rd	51. 14. 01

5. At reader-11-time of the second card-feed cycle, the read-two-row bit-data combines with X-data to block the setting of both ux and lx cores for position two.

SIGNAL	CONTROL	LOGIC
Data reg out 2nd rd (not) Hole-ct to inh drv up X	Rd pulse 010-040 (not) Data reg out up X	51. 10. 01 51. 14. 01
(not) Hole-ct to inh drv lwr X	Data reg out lwr X Data reg out 2nd rd	51. 14. 01

6. To detect a hole-count error, the output of reader X-plane switching is tested at 12-time in order to determine whether any cores are to be set (any X-core set after 12-time indicates a hole-count error).

SIGNAL	CONTROL	LOGIC
Hole-ct chk gate (not) Hole-ct err	Rd req rd scan Reader 12 time (No data from chk cores)	52. 10. 06 51. 14. 01

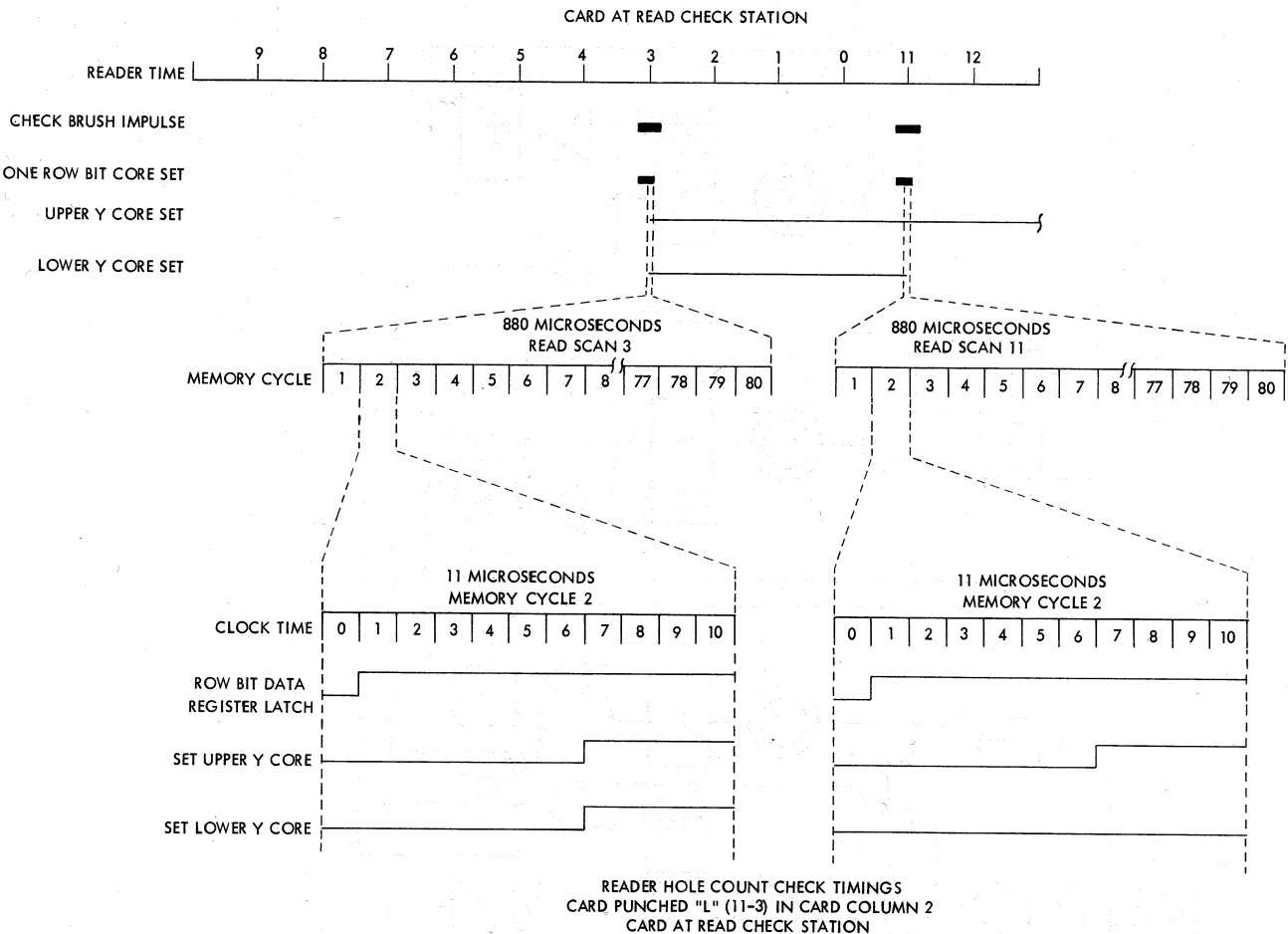


Figure 43. Reader Hole-Count Check Timings – Card at Read Station

Punch Hole-Count Checking

The hole-count check circuit for the card punch is similar to that for card reader. The same “X” and “Y” hole-count plane switching circuits and data registers are used by both reader and punch, since only one type of scan (reader or punch) can occur at any given time. The differences lie in the sources of hole count input data and the times when the scans occur.

Hole Count Data Sources

The punch, instead of having two reading stations, has one punch station and one read station. The card is first punched and one card feed cycle later is read at the reading station.

As the card is being punched, the BCD data register is viewed by “bit generator” circuitry to determine the number of punches which should be punched in each card column. The output of this “bit generator” controls the setting of Upper Y and Lower Y cores. Thus the bit generator effectively converts BCD to “row bit” type information and serves the same purpose for punch hole count checking as did the first read station in the reader.

One feed cycle later the punched card is read at the punch check station. The information is read into punch row bit cores and controls the Upper X and Lower X core circuits. The function of these punch check brushes is the same for punch as the second read station is for reader. In punch as well as in reader, a correct hole count should result in all X cores being in zero status after the card is read at the punch check station.

The Bit Generator

The bit generator converts BCD data to row bit form as illustrated in Figure 45.

This circuitry operates on the principle that the maximum number of punches that can appear in a given column is three, assuming all characters valid. The minimum number of punches is of course zero for a blank column. It should be noted that a complete scan of punch buffer occurs at each digit time to set up the punch magnets.

The bit generator circuitry is designed to sample the BCD content of each buffer position during three of these scans. Only three samplings are necessary to

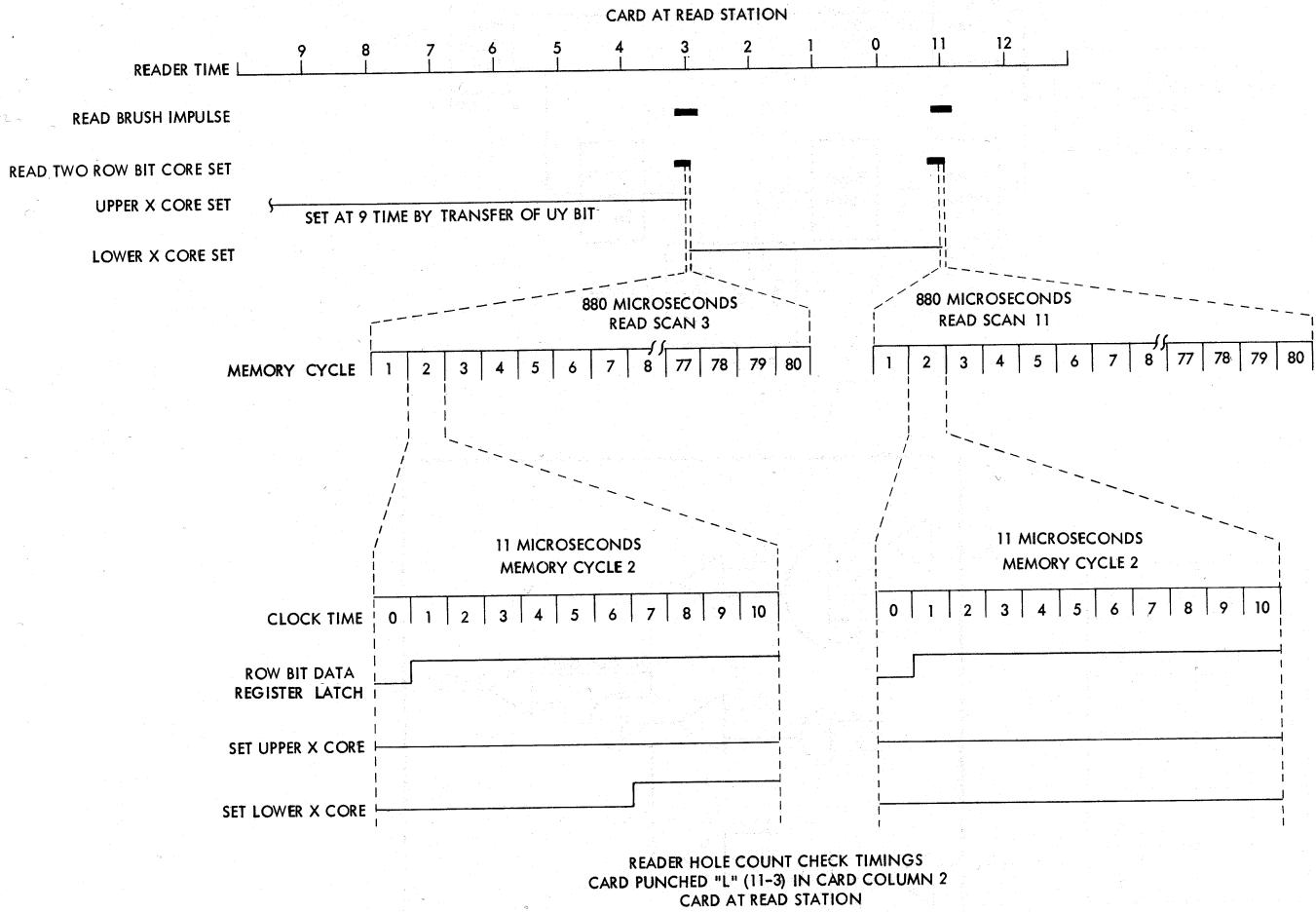


Figure 44. Reader Hole-Count Check Timing – Card at Read Check Station

detect any number of punches from 0 to 3. The three emitter times selected for sampling are 11, 1, and 2. There is no specific reason for selecting these emitter times. Any emitter times would give satisfactory results as long as three samplings occur.

An example of bit generator conversion is explained here for the punching of the character “E” in column 1 (C, B, A, 4, and 1 bits). The resulting card code should be a 12-punch and a 5-punch. Thus the bit generator should give an output at two emitter times to indicate to hole-count circuits that two punches should appear in column 1.

At emitter 12 time there is no bit generator output since this is not one of the sampling times. At emitter 11 time one of the AND circuits (Figure 44) is conditioned by E11. The other leg of this AND circuit is also conditioned since the BCD data register contains both a 1 and a 4 bit. The bit generator gate is up for each punch scan so the bit generator output is active. This first output should result in setting both the uy and LY cores for that position.

The next sampling time is emitter 1 time and there is no bit generator output.

At emitter 2 time, the presence of the A and B bits in the data register causes a second bit generator output. This output blocks regeneration of the LY core for that position. Thus a hole count for that column has been accumulated to be compared with the count at the punch check station.

Note that the emitter time at which a bit generator output occurs has no relationship to the time at which actual punching occurs. In the example given, bit generator outputs occurred at 11 and 2 times while punching should occur at 12 and 5 times.

The chart in Figure 45 illustrates that all numbers, letters and special characters are considered at one or more of the sampling times.

Complete Punch Hole-Count Check

The accumulated hole count from the bit generator is transferred from “Y” cores to “X” core circuits at emitter 12 time as the card starts by the punch check station.

The card is then ready to be read in order to complete the hole-count check. In order to punch holes in a card, the punch magnets must be set up before

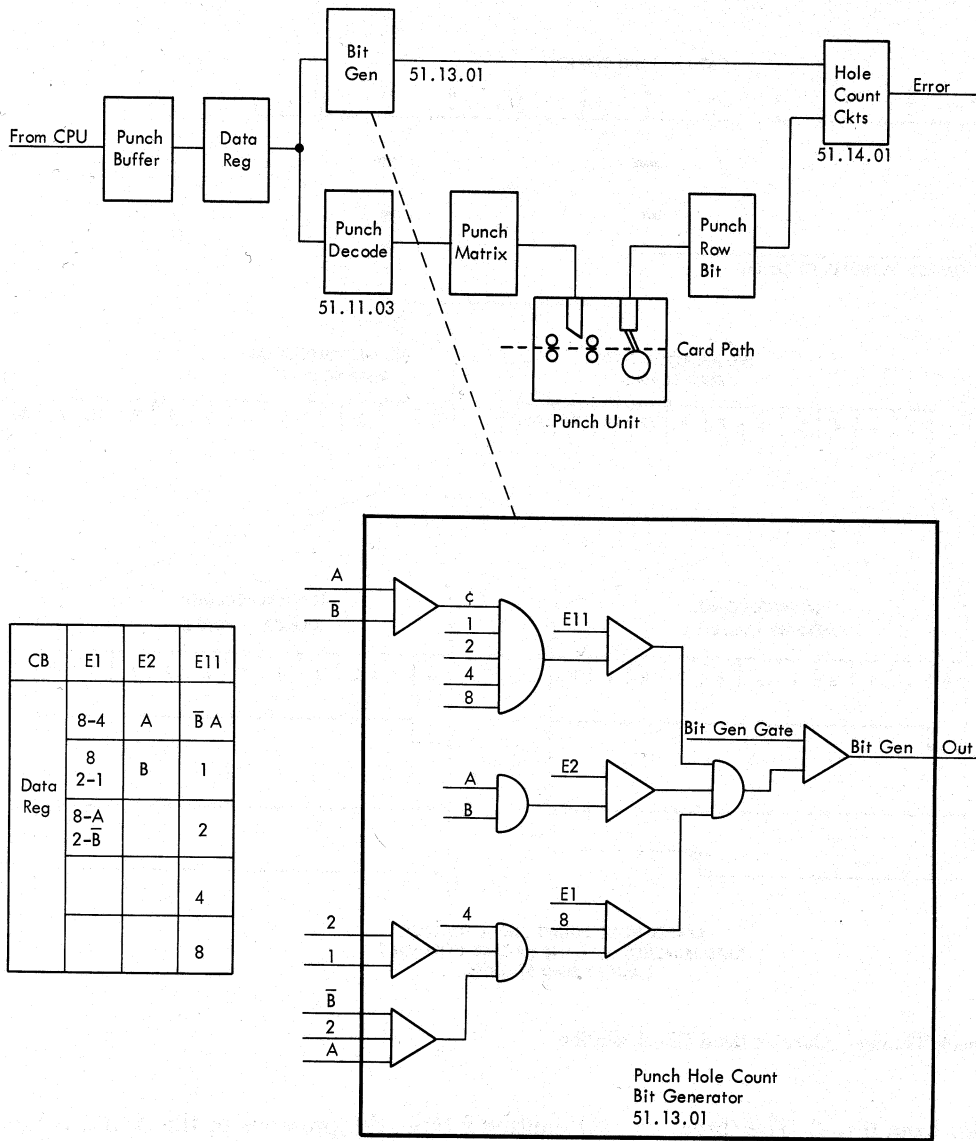


Figure 45. Punch Hole-Count Check

actual punching time. This means that the first scan takes place before 12 time of the punch cycle. At this time, the 12 row of the card at the punch check station has not yet been read into row bit cores and therefore cannot affect the "X" hole-count circuits. The 12 row bit data is scanned out of row bit storage to hole-count circuits during the second scan or while the 11 row data are being set up for punching. Consequently, hole-count data from the punch check brushes is always scanned out to hole count circuits one cycle point late with respect to punching. At 9 time, the "9" row is set up for punching and the "8" row bit data is scanned out to hole count circuits. In order to complete the hole count check, an after 9 cam initiates an extra (thirteenth) scan. This additional scan causes no punch magnet set up, but allows the "9" row bit data to be scanned out to complete the hole count check. This is illustrated in the sequence chart, Figure 46.

Note in Figure 47 that the row bit two core plane which contains reader and punch row bits has separate sense lines and sense amplifiers for the reader and punch sections. This is the only plane in buffer in which the reader and punch sections do not share a common winding. This is necessary since with both reader and punch cycles in progress, it would be possible to set one section of row bit 2 cores while the other section is being scanned out. Separate sense windings must be used to prevent one operation from affecting the other.

Reader Validity Check

OPERATION

An IBM card, with its 12 punching positions per column, can contain a great number of punch combinations. Of these, only 64 are recognized as representing valid characters. All other combinations are considered

Time	Punch Magnet Set Up	Actual Punching at Punch Station	Read from Punch Brushes into Row Bits	Transfer from Row Bits to X Hole Count
12 row scan prior to 12 time	Set up to punch 12's			
12 time		Punch 12's	Read 12's	
11 row scan prior to 11 time	Set up to punch 11's			Transfer 12 row bit data
11 time		Punch 11's	Read 11's	
9 row scan prior to 9 time	Set up to punch 9's			Transfer 8 row bit data
9 time		Punch 9's	Read 9's	
After 9 scan 13th scan				Transfer 9 row bit data

Figure 46. Hole-Count Check Sequence

invalid. The reader validity-check circuit analyzes each character as it is being coded. The sensing of any incorrect character coding results in an invalid-card code signal.

During each read scan, information that is scanned out of row-bit storage combines with information that is scanned out of the read buffer in order to determine the validity of all characters while they are being developed. This check must be performed during every memory cycle of each read scan, because the machine reads in a parallel manner by row and serially by card hole.

The reader validity-check circuit consists of three sections. Each can detect a different type of coding error (Figure 48). The conditions that each section must meet determine the validity of each character, as follows:

1. *Section A:* When coding any punches from 9 through 2, the addressed position of the read buffer should not already contain a 4, 2, or 1-bit.
2. *Section B:* When coding a 1- or 9-punch, the addressed position of the read buffer should not already contain an 8, 4, or 2-bit.
3. *Section C:* When coding an 11- or 12-punch, the addressed position of the read buffer should not already contain an A- or B-bit.

Any invalid-card code is detected by one of the three sections. This results in an invalid-card code signal.

Read-request, read-scan and bit X-signals develop the encode-bit X signal. Bit X represents read-two-row bit-data.

CIRCUITS

A card column that contains a 9- and an 8-punch is checked to indicate a validity error.

The 9-punch from row-bit storage feeds to the validity-check circuit and is called *bit X*. No error is indicated because there are no bits in the addressed buffer position.

SIGNAL	CONTROL	LOGIC
Encode	Rd req rd scan	52. 10. 05
Encode bit X	Encode	51. 12. 01

At reader-8-time, the 8 from row-bit storage (*bit X*) combines with the 8-bit and 1-bit from the addressed buffer position to produce an invalid-card code signal.

SIGNAL	CONTROL	LOGIC
Invalid-card code	Bit X, data reg out 1-bit and read CB8.	51. 12. 01

Reader End-of-File

Depressing the end-of-file key on the 1402 causes all cards in the read feed to be processed when the hopper becomes empty. Reader ready to CPU is held active by end-of-file circuits. Figure 105 shows the second level circuits for end of file.

The end-of-file relay being up prevents the read stop line from resetting the CE reader ready latch until the last card has been read at the second read station (Systems 52. 11. 01 and 51. 03. 12). The end-of-file latch being on then forces up reader ready until CPU tests for end-of-file status and resets the end-of-file latch (Systems 52. 11. 02).

CORES

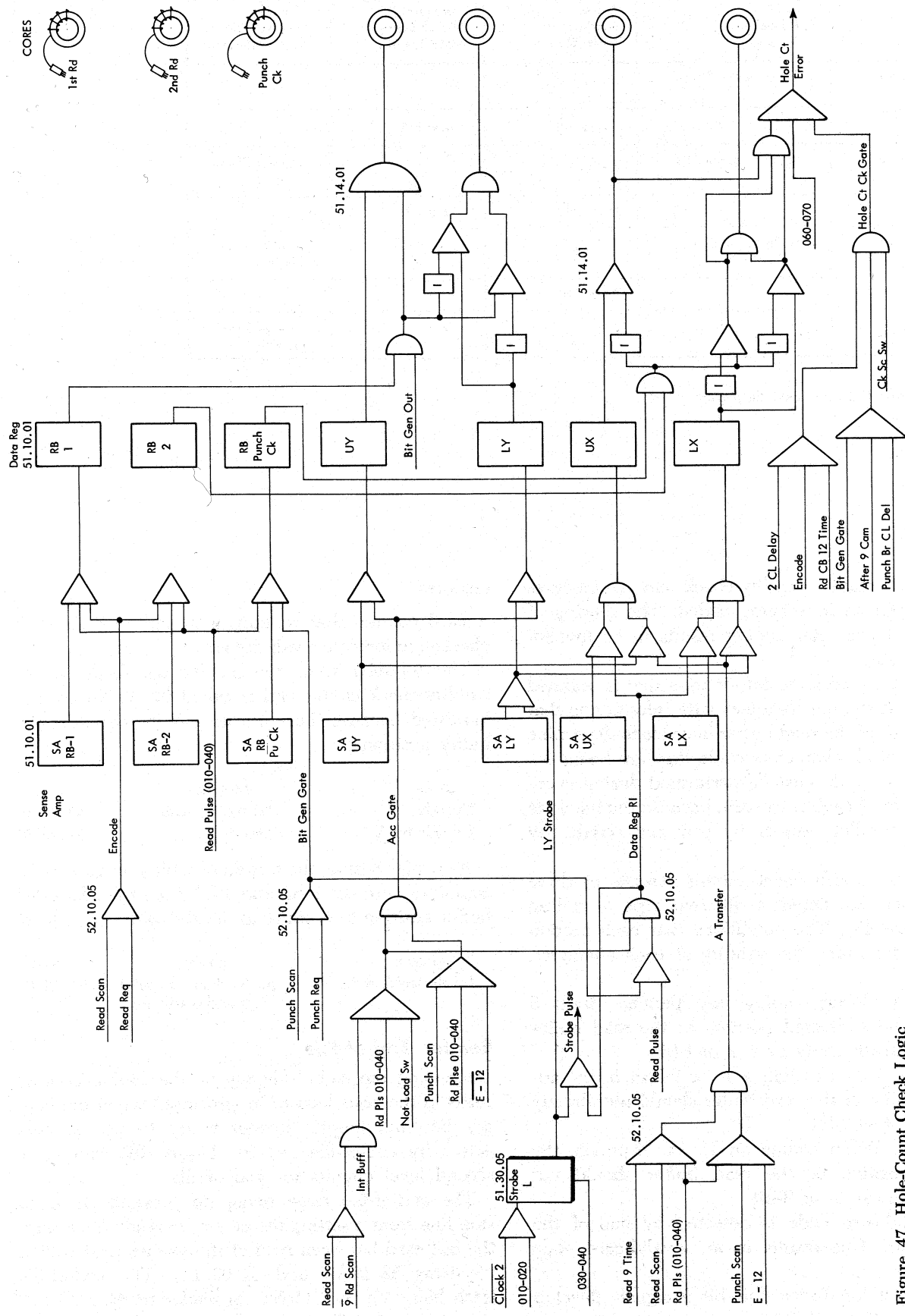
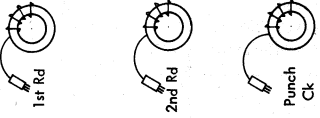


Figure 47. Hole-Count Check Logic

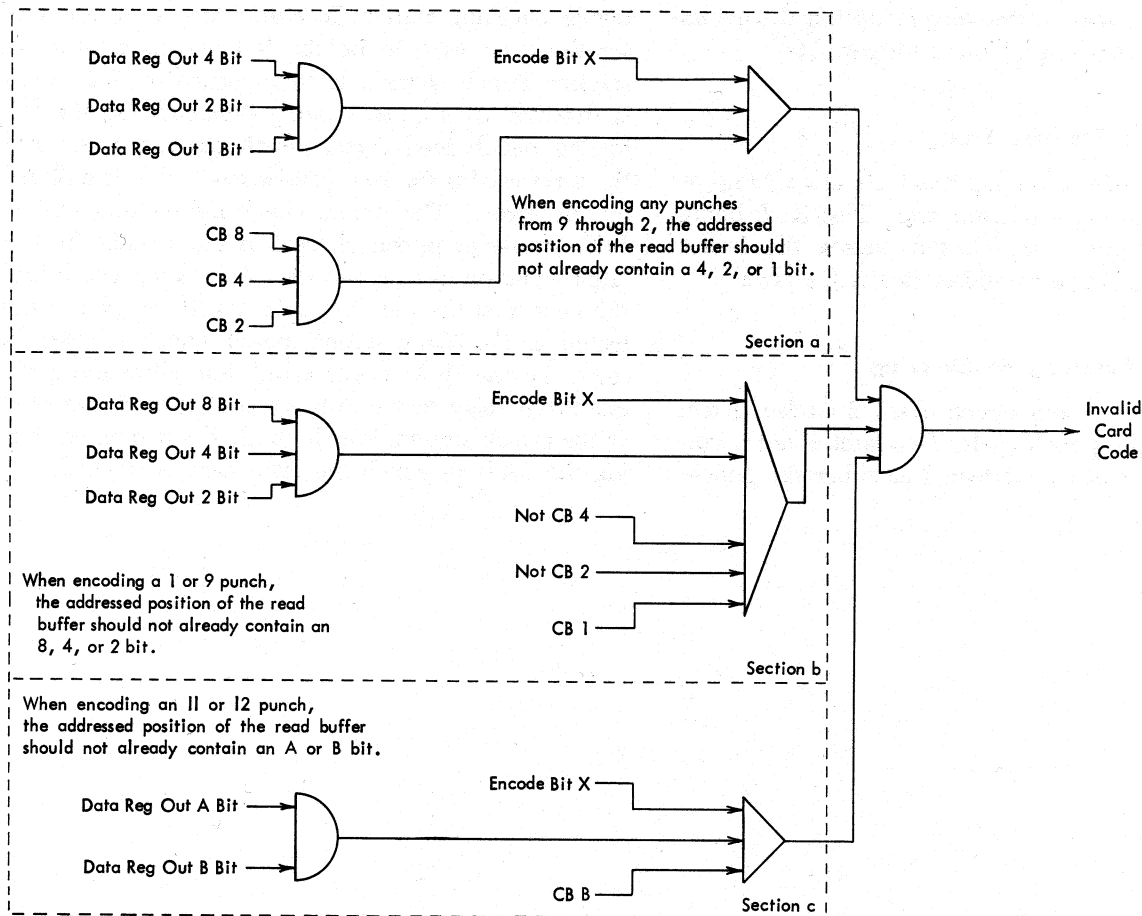


Figure 48. Reader Validity Check

Systems 52.11.01 shows the end-of-file circuits. With reader ready held up, all cards can be processed without the normal stop when the hopper becomes empty. As the last card passes the second read station, the end-of-file delay latch is set. When this card is fed out to the stacker, the end-of-file latch is set. (During this cycle, the contents of the last card should be transferred to CPU.) At this time, the end-of-file relay drops to allow the reader to stop. The end-of-file latch remains on to hold up reader ready (Systems 52.11.02). The last card is now in the stacker. The end-of-file latch being on signals end-of-file to CPU the *next time* an attempt is made to read a card. The end-of-file latch is then reset by CPU. If CPU attempts to read a card again, a not ready indication results since the end-of-file latch is now off.

Read Check Latch

The read check latch, when on, indicates errors to the operator and to CPU. Figure 105 illustrates the read check latch circuits. Errors during a read scan set the read check latch. It remains set until the reset pulse at Reader 9 time and causes the reader check indicator to glow on the 1402. In addition, the read check latch causes the "buffer error" line to be active whenever the reader is selected by CPU indicating that the card image being transferred to CPU is in error. A Reader Check nullifies stacker selection.

Punch Check and Punch Transfer Error Latches

These latches detect any type of punch error and signal CPU that an error has occurred. Errors may oc-

cur during a punch-transfer scan or during the actual punching and checking of cards (Figure 102).

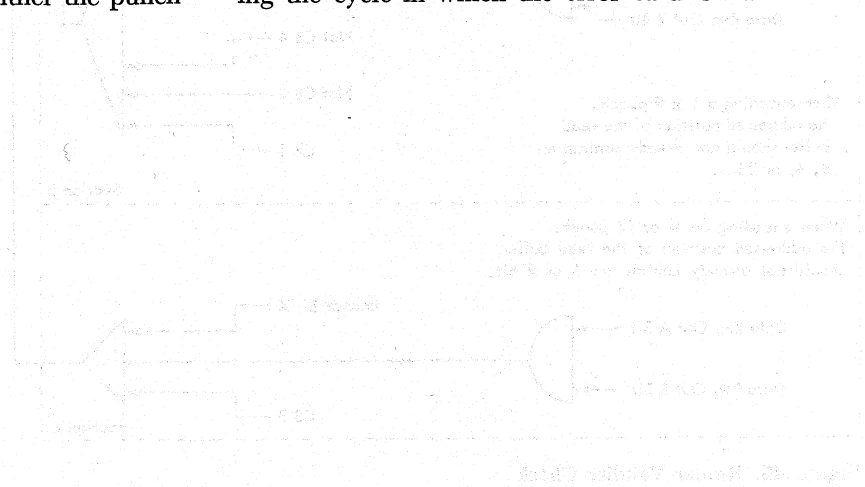
Errors During a Transfer Scan

The punch transfer error latch detects clock, ring, or parity errors during a transfer scan. This latch being on when the punch is selected causes the buffer error line to be active to inform CPU of the error.

Errors During Punching or Checking

The punch check 1 and punch check 2 latches detect errors during the punch cycle. Two latches are necessary since errors can be detected at either the punch-

ing or checking station. In either case, it is desirable for the error card to be the last one in the normal stacker. Punch check 1 latch is turned on if an error is detected *as a card is being punched*. On the following punch feed cycle, punch check 2 is set and the error card is stacked. (Stacker selection is nullified by the error.) The punch check light glows on the 1402 whenever punch check 2 is on. Punch check 2 latch being on also signals CPU of a "buffer condition" the next time the punch is selected. If an error is detected *at the check station*, punch check 2 is set directly by the "hole count error" line eliminating the one cycle delay that results when an error is detected at the punch station. Punch check 2 is turned on during the cycle in which the error card is stacked.



The read check latch, when an inherent error in the punch transfer error latch occurs during a transfer scan, the read check latch is set. It remains set until the read check latch is cleared by the punch transfer error latch. It is set when the punch transfer error latch is set and cleared when the punch transfer error latch is cleared. It is set when the punch transfer error latch is set and cleared when the punch transfer error latch is cleared. It is set when the punch transfer error latch is set and cleared when the punch transfer error latch is cleared.

Figure 102 shows the read check latch. The read check latch is set when an inherent error in the punch transfer error latch occurs during a transfer scan. It remains set until the read check latch is cleared by the punch transfer error latch. It is set when the punch transfer error latch is set and cleared when the punch transfer error latch is cleared. It is set when the punch transfer error latch is set and cleared when the punch transfer error latch is cleared.

Paper Tape Reader Attachment

The IBM 1011 Paper Tape Reader is used in conjunction with the integrated synchronizer to provide a buffered paper-tape input to the IBM 1410 Data Processing System. There are 13 lines that connect the 1011 and the integrated synchronizer. The names and functions of these lines are:

LINE	FUNCTION
Paper-tape-ready	Output line from the 1011. Indicates that power is on, that tape is properly loaded, and that the start key was pressed.
PT parity error	Output line from the 1011. Indicates an 8-channel tape-parity error.
End-of-record	Output line from the 1011. Indicates that the end-of-record character was detected.
Data output (7 lines)	Output lines from the 1011 output data register (register B).
Data sync	Output line from the 1011. Indicates that a character is present on the data-output lines.
Character received	Input line to the 1011. Indicates that the character on the data-output lines was received and stored.
Go	Input line to the 1011 that requests a character.

Core Storage

The integrated synchronizer can have eight 80-position core-storage units (Figure 49). One of these storage units can be assigned to the paper tape reader. Eighty characters from the paper tape (PT) reader are stored in the PT storage unit. When the storage unit is filled, the contents can be transferred to the CPU. PT storage has eight planes: seven planes store the characters in BCD form; the eighth, or control plane, locates the storage positions for incoming characters. When used with the integrated synchronizer, the PT reader uses the circuitry assigned to option 4.

PT storage uses the same addressing system, data registers, and clock as the other integrated synchronizer storage units.

Input Serial Scan Control

Once the go signal is received, the PT reader sends a character to PT storage every two milliseconds. Each time a character is received, the addressing rings locate the next storage position in sequence. The character is stored and the rings reset. As soon as the rings reset, they can be used to scan other storage units until the next PT character is received.

PT read-in begins with all eighth-bit cores set ON. When a character is written into a PT storage position, the corresponding eighth-bit is set OFF. For example, assume that a PT read-in is in process, and positions 1-23 have characters with no control bits in them. Positions 24-79 contain control bits. A data sync pulse from the PT reader requests a serial scan. The scan starts with the rings addressing position 09. Position 09 reads out, and because there is no control bit, the character is regenerated. The tens ring then advances and position 19 reads out. Again there is no control bit, so that the character is regenerated, and the tens ring advances to address position 29. When position 29 reads out, a control bit is detected. This indicates that the desired position is somewhere in the positions 20 to 29. The tens ring is now prevented from advancing, and the units ring is allowed to advance to address and to read out positions 20, 21, 22, and 23 before the next control bit is sensed. When position 24 reads out, pre-sense of the control bit brings up the gate that allows the incoming character to be written into this position, during the write portion of the memory cycle. The control bit is not regenerated, in order to indicate that this position is filled. The rings are then reset and the PT storage circuitry waits for the next data-sync pulse.

Paper Tape Read-In

Paper tape read-in is initiated by a go signal from the integrated synchronizer (Figure 50). The go signal is generated with a power-on reset, or after a read transfer scan takes place. When the IBM 1011 receives the go signal, the drive mechanism is set in motion, and as each character becomes available at the output bit lines, a data-sync pulse is sent to the paper-tape storage circuitry. The data-sync pulse requests a serial scan to store the incoming character. Requesting the scan gates the character into a data register, and then signals the 1011 that the character is received.

After priority conditions are satisfied, a scan is initiated to locate the first blank position. When the correct position is located, the character is stored, and the rings are reset. After 80 data sync pulses are received, or if the 1011 signals an end of record, the go line is dropped to stop paper tape reading. These conditions also reset the paper-tape-busy latch to allow a paper-tape-read-transfer instruction to be executed. Figure 51 shows the relative timings involved in storing a character.

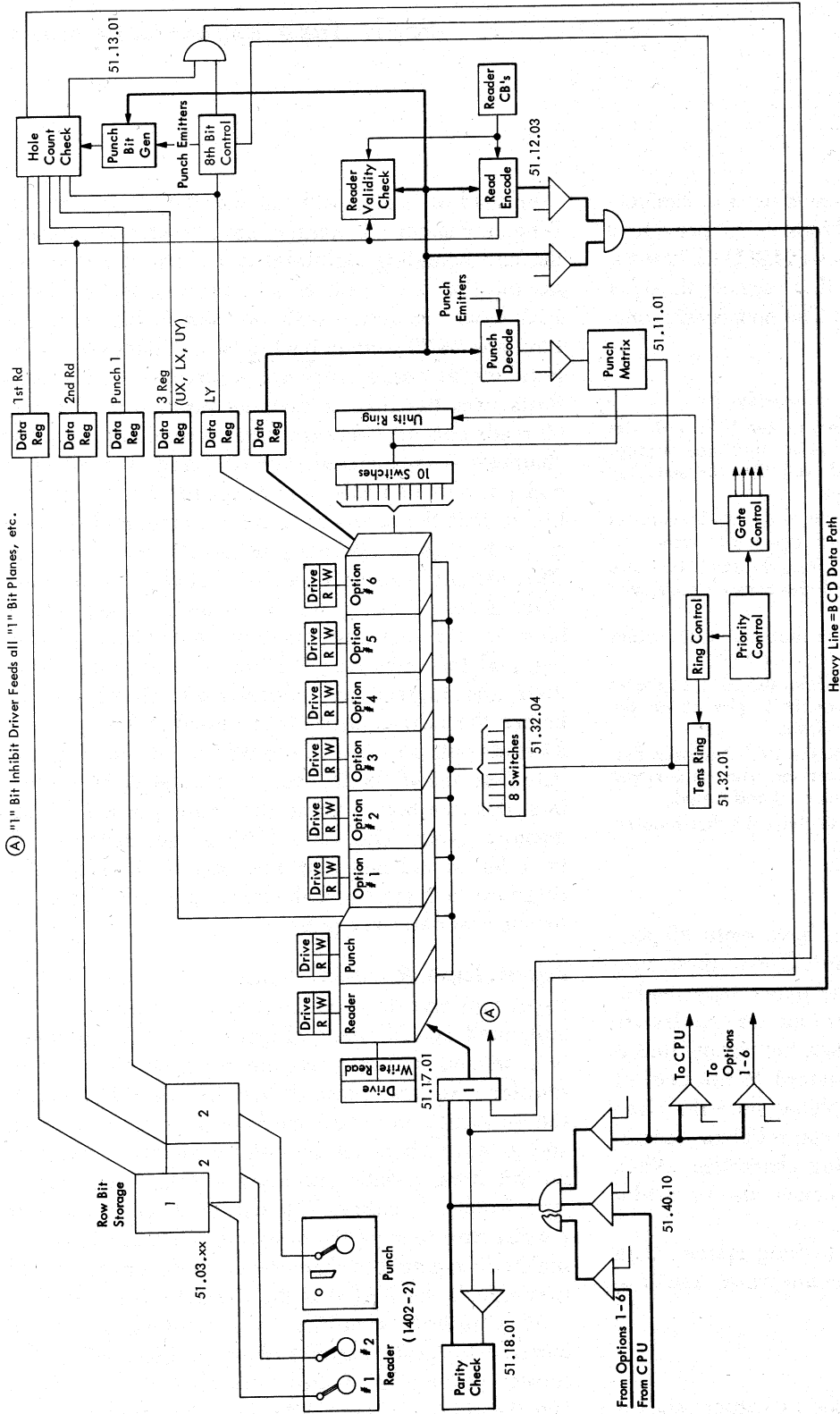


Figure 49. 1414 Integrated Synchronizer Data Flow

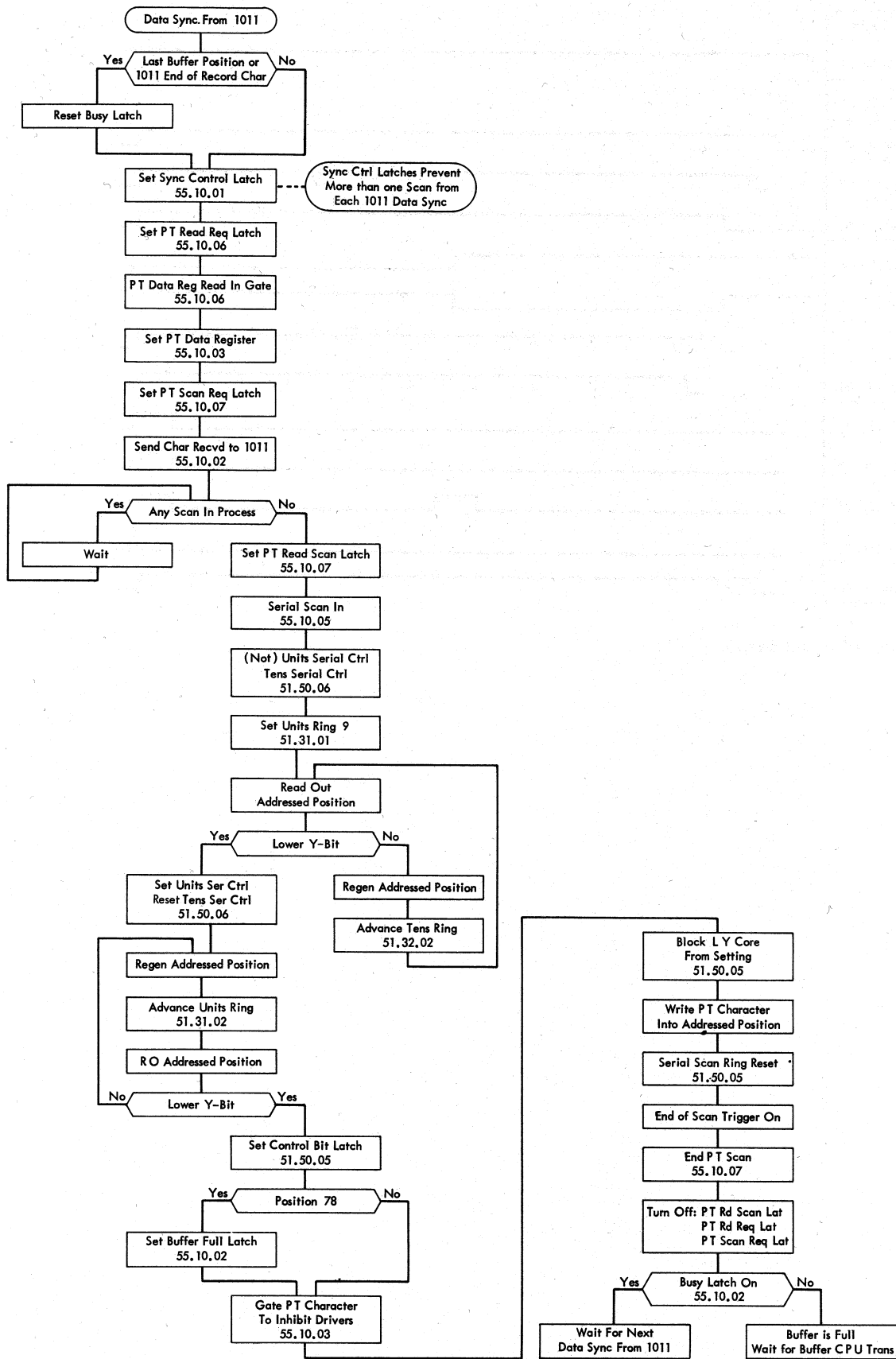


Figure 50. Paper Tape Read-In

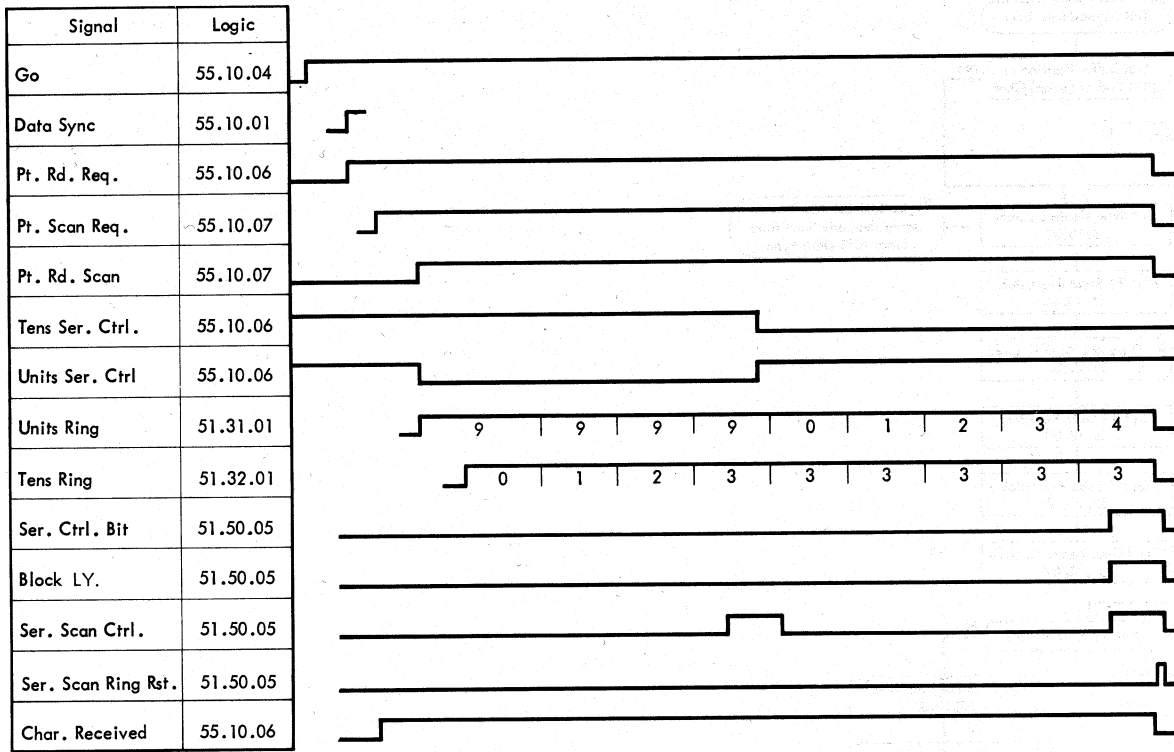


Figure 51. Paper Tape Character Storage

The IBM 1414 Input-Output Synchronizer, Models 3, 4, 6, or 8, can contain the core storage and related control circuits that permit the 1403 Printer to be an on-line output device for several systems (Figure 1). The print buffer serves as an intermediate storage that allows the using system to proceed while a line as actually printed under control of the 1414. This section describes the printer core storage and the control circuits necessary to operate the 1403 Printer and its carriage. For information on principles of operation of the printer and carriage, refer to the publication, *IBM 1403 Customer Engineering Manual of Instruction*, Form 225-6592-1.

The print operation can be divided into two parts; filling the print buffer with data from the CPU, and reading out the characters to be printed in the sequence and at the speed that the 1403 requires. The print circuits operate independently from the integrated synchronizer, but no other CPU to I-O operation can be in process while a print transfer scan is in process.

Printer Core Storage Unit

Printer storage serves the same purpose for the 1403 that the reader punch section of the integrated synchronizer serves for the 1402.

Thirteen planes physically similar to the ones in the integrated synchronizer are mounted on the wiring side of panel three to make up the print core storage unit (Figure 2). Also the bilateral winding method (Figure 4) is used. Each plane has ten rows of 16 cores for a total of 160 of which only 132 are used. Of the 13 planes, only 11 actually have cores. Planes 11 and 13 are dummy planes used for wiring (Figure 52). Seven core planes (C, B, A, 8, 4, 2, 1) store characters in a modified BCD code (Figure 53), and the remaining four planes (hammer check, print line complete, equal compare, and hammer fire row bits) detect print errors.

On a read-in operation, print information is translated into the modified BCD code that the printer requires. The translated characters are placed in print storage in the seven data bit planes of the addressed position. An odd bit parity check is made of the modified BCD characters. Each character is also tested to determine whether it can be printed. The CPU recognizes 64 valid characters, but the printer can print only 51 characters (on 48 type characters).

Scan-out occurs after read-in is complete. As each position is addressed, the information in the cores reads out to set the data register latches. If the character that reads out corresponds to the type character

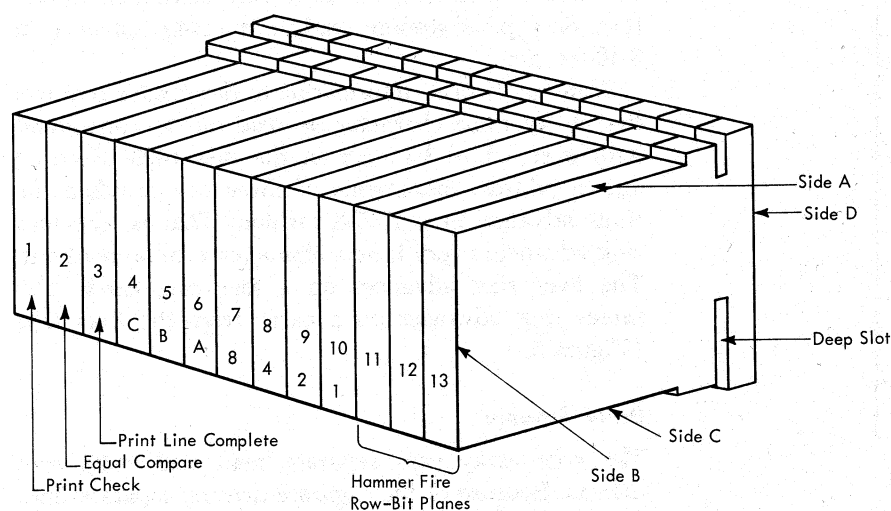


Figure 52. Print Buffer Core Planes

	B	A	8	4	2	1
1						1
2					2	
3					2	1
4				4		
5				4		1
6				4	2	
7				4	2	1
8			8			
9			8			1
0			8		2	
#			8		2	1
@			8	4		
/		A				1
S		A			2	
T		A			2	1
U		A		4		
V		A		4		1
W		A		4	2	
X		A	8		2	1
Y		A	8			
Z		A	8			1
#		A	8		2	
,		A	8		2	1
%		A	8	4		
J	B					1
K	B				2	
L	B				2	
M	B			4		
N	B			4		1
O	B			4	2	
P	B			4	2	1
Q	B		8			
R	B		8			1
-	B		8		2	
\$	B		8		2	1
*	B		8	4		
A	B	A				1
B	B	A			2	
C	B	A			2	1
D	B	A		4		
E	B	A		4		1
F	B	A		4	2	
G	B	A		4	2	1
H	B	A	8			
I	B	A	8			1
&	B	A	8		2	
.	B	A	8		2	1
□	B	A	8	4		

Figure 53. Modified BCD Code

that is aligned at the print position, an equal compare results and the hammer fires. After the compare operation, the character is placed back in storage until the next print scan.

The core array is arranged physically and electrically in such a way that information from the CPU reads into sequential print storage positions (1, 2, 3, 4, etc.). When this information is to be printed, it is scanned out in address increments of three (1, 4, 7, 10, etc.), as the printer requires.

Addressing Rings

Three rings control core storage addressing (Figures 54 and 55). The rings are called the threes, fives, and tens rings from the number of positions they contain. The tens ring selects a row of cores in one direction. The threes and fives rings together select a row of cores in the other direction. The coincidence of the two selected lines produces a selected character position.

For example, assume that core position 1 is to be selected. The 0 position of the tens ring selects the tens row that contains core position 1. The first position of the fives ring selects three lines in the other direction. Of the three lines, the core driver actuates only one. The output of the threes ring selects the correct core driver.

When core position 1 is selected, position 2 can be addressed by advancing the threes ring to the next position. When the threes ring advances to position 3, it selects core position 3. The next pulse to the threes ring causes position 1 to come back on. However, going from position 3 to position 1 develops a threes ring carry that, when fed to the tens ring, causes the tens ring position 1 to come on. With position 1 on in all three rings, core position 4 is selected. When the tens ring carries, the fives ring advances. Therefore, on a print storage read-in, the rings advance in 3-10-5 order.

Scan-out of print information to the printer requires that every third character be read out to correspond with every third hammer in the IBM 1403. Reading out in address increments of three occurs when the rings advance in a 10-5-3 fashion. That is, the tens ring advances every time a character is to be read out. The fives ring advances on a tens ring carry. The threes ring advances on a carry from the fives ring (Figure 56).

Drive Scheme

The core array uses separate read and write core drivers. Because of the separate drivers, separate lines must be used for reading and writing. Figure 4 identifies the six lines through each core. The read and

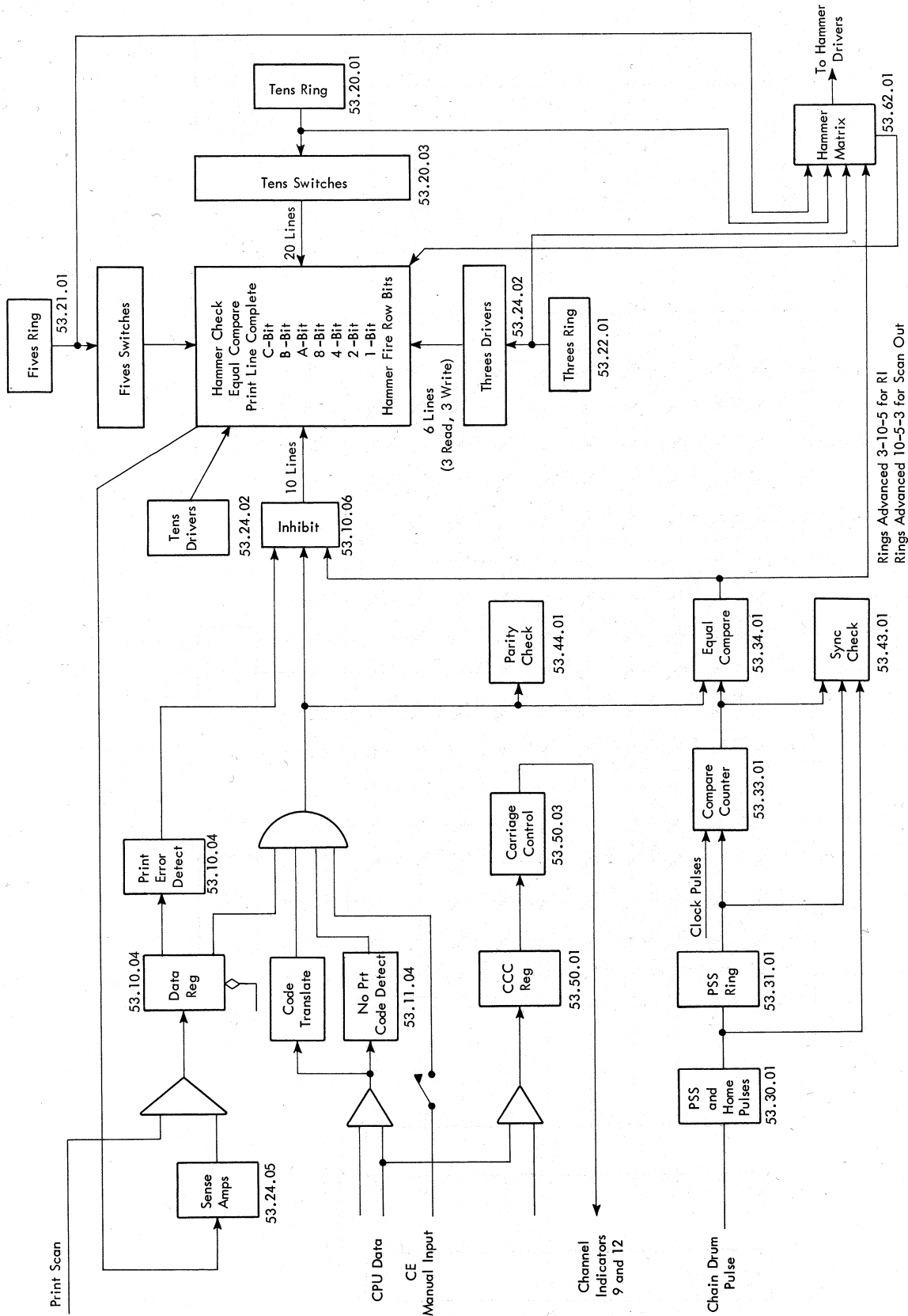


Figure 54. Print Storage

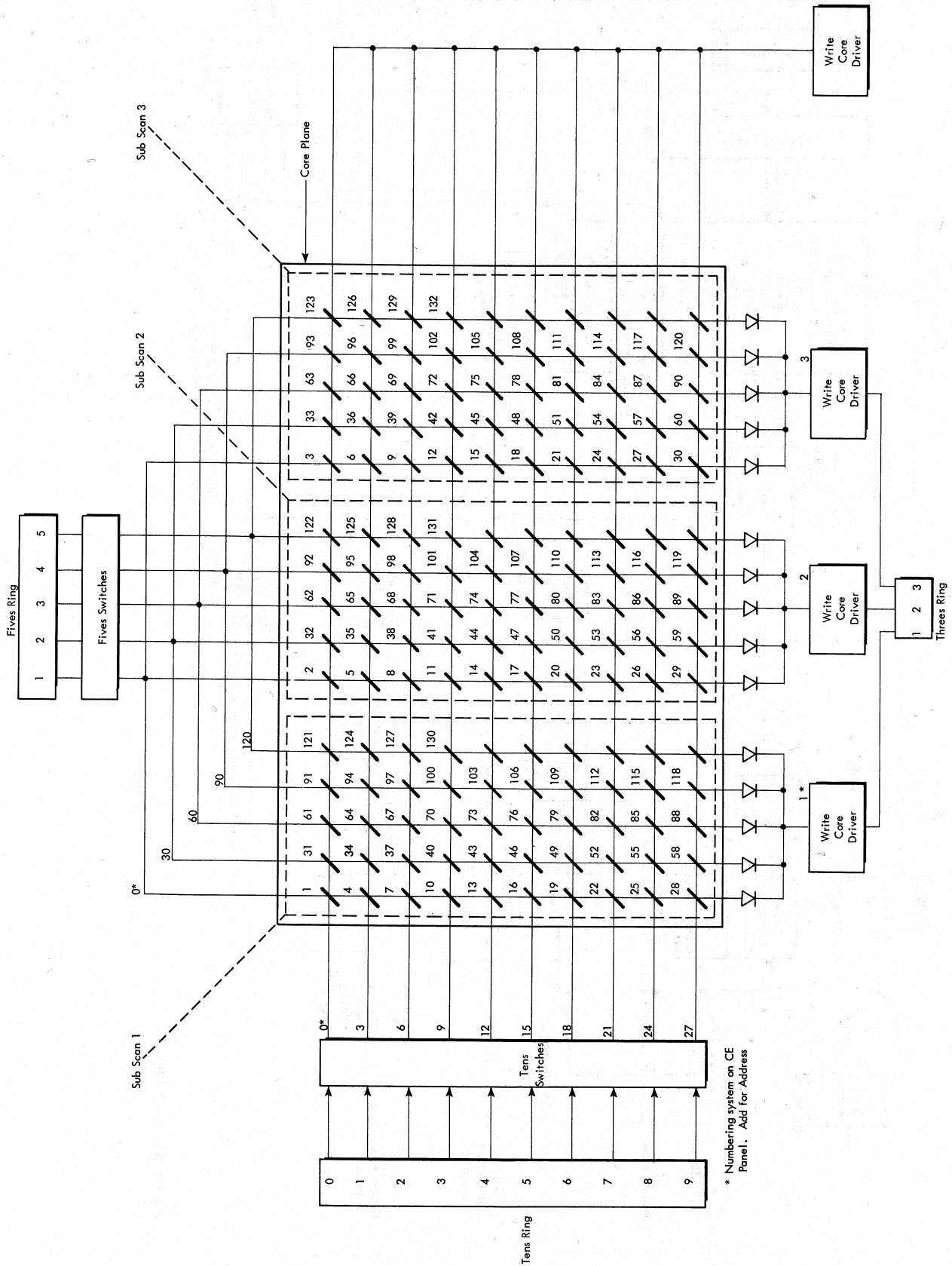


Figure 55. Print Storage Addressing

write windings pass through the cores in opposite directions. A row bit core is shown in Figure 6.

Eight current drivers supply current through the core windings for reading and writing. There is one read and one write driver for the ten (T0 through T9) tens switches. The fives switches require three read and three write current drivers (Figure 57).

Figures 58 and 59 show the basic timings of the print storage circuit. At the beginning of the cycle, the ring advance pulse addresses a particular position. The read pulse that is supplied by the core drivers flips the cores that were set to induce a current into the sense winding. The sense winding current is amplified to set a data register latch. Later in the memory cycle, the write pulse sets the proper cores. The inhibit pulse cancels the effect of the write pulse for the addressed cores that are not to be set.

Read-In

The transfer scan that moves the 132-character record (100 characters for a 1403 Model 1) from CPU to the print buffer is called read-in. Read-in is very similar to a punch transfer scan. However, during the transfer two additional things occur; the characters are translated into the modified BCD code, and each character is tested to see if it is a printable character.

As shown in Figure 60, the 8 and 2 bits are added to BCD characters that are made up of zone bits only. This translates the three characters ¢, -, and &, to ¤, !, and ?. However, ! and ? are replaced on the type chain by a dash (—) and an ampersand (&) so ¢, !, and ? are dropped. The chart in Figure 60 shows the code translation.

Also during the transfer scan that fills the print buffer, each character is tested to see if it is a printable character. The type chain on the 1403 has 48 different type characters. This leaves 16 characters of the 64 BCD code that the printer cannot print. Three are dropped in the code translation described above and the other 13 are not printed, as shown in Figure 61. On the printed paper output, three of the 16 characters are changed to different characters and 13 print as blanks.

On a read-in operation the threes ring advances at the beginning of every memory cycle. The tens ring advances at the beginning of every third cycle (threes ring carry). The fives ring advances every 30th cycle (tens ring carry). Each ring is gated to function as a closed ring until position 132 is reached (Systems 53. 23. 01-02). Position 132 stops the rings from advancing and gates the home trigger on.

With machines that have only 100 print positions, all 132 are read in and scanned out. On Systems 53. 11. 05, C bits are inserted during read-in in all

positions after print position 100, to prevent parity errors while scanning out (Figure 62).

Scan-Out

During a scan-out, characters are read out in address increments of three on successive memory cycles. All 11 cores read out of each addressed position during the read portion of the memory cycle. The six data bits feed to the equal compare circuitry to determine whether the correct type character is aligned to the addressed print position. The data bits that are read out during the read portion of each memory cycle are regenerated during the write portion of the cycle so that the characters will be available on successive print scans. The error-detection cores (equal compare, hammer fire, and hammer check) are set up on each memory cycle. They are not tested until one print scan later. That is, print scan 20 is not tested for error until print scan 21, etc. To test print scan 48 (the last print scan) for errors, an additional or 49th scan must be taken. For conditions that are recognized as errors see "Print Error Detector" in this publication.

On a scan-out operation, the tens ring advances at the beginning of each memory cycle. The fives ring advances every ten cycles (tens ring carry). The threes ring advances every 44 cycles (end of subscan).

Three ring advance triggers provide the pulses necessary to control the advance of the three rings (Systems 53. 23. 02).

Type Synchronization

Timing drum pulses are amplified and used to develop the print subscan and home pulses (Figure 63). The print subscan (PSS) pulse occurs whenever a type character aligns at one of the first three printing positions. The home pulse occurs when the type character 1 aligns at print position 1.

The PSS pulse drives a three-position closed PSS ring. The outputs of the ring triggers (called PSS-1, PSS-2, and PSS-3 pulses) identify the subscan that is taking place.

There are 49 print scans within any print line. A six-position print scan counter advances at the beginning of each print scan along with the PSS-1 pulse to count the number of print scans (Systems 53. 32. 01 and Figure 64).

The printer circuitry uses a compare counter to identify the type character that is eligible to print. The compare counter is a six-position, alphameric counter. Its six positions represent the six data bits of a character. The counter advances so that its contents always define the type character in position to print. Figure 65 shows the activity of the compare counter during a print scan.

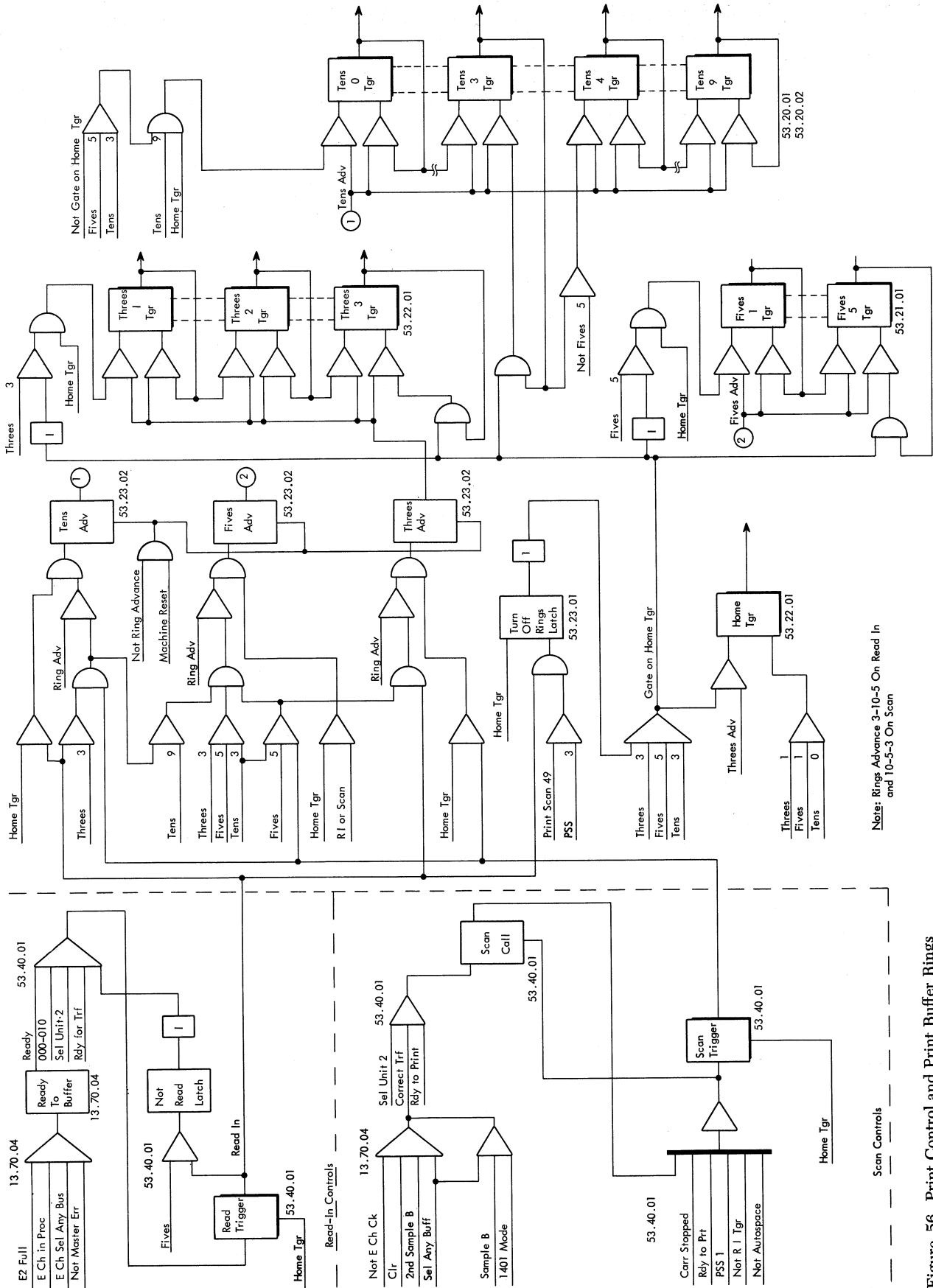


Figure 56. Print Control and Print Buffer Rings

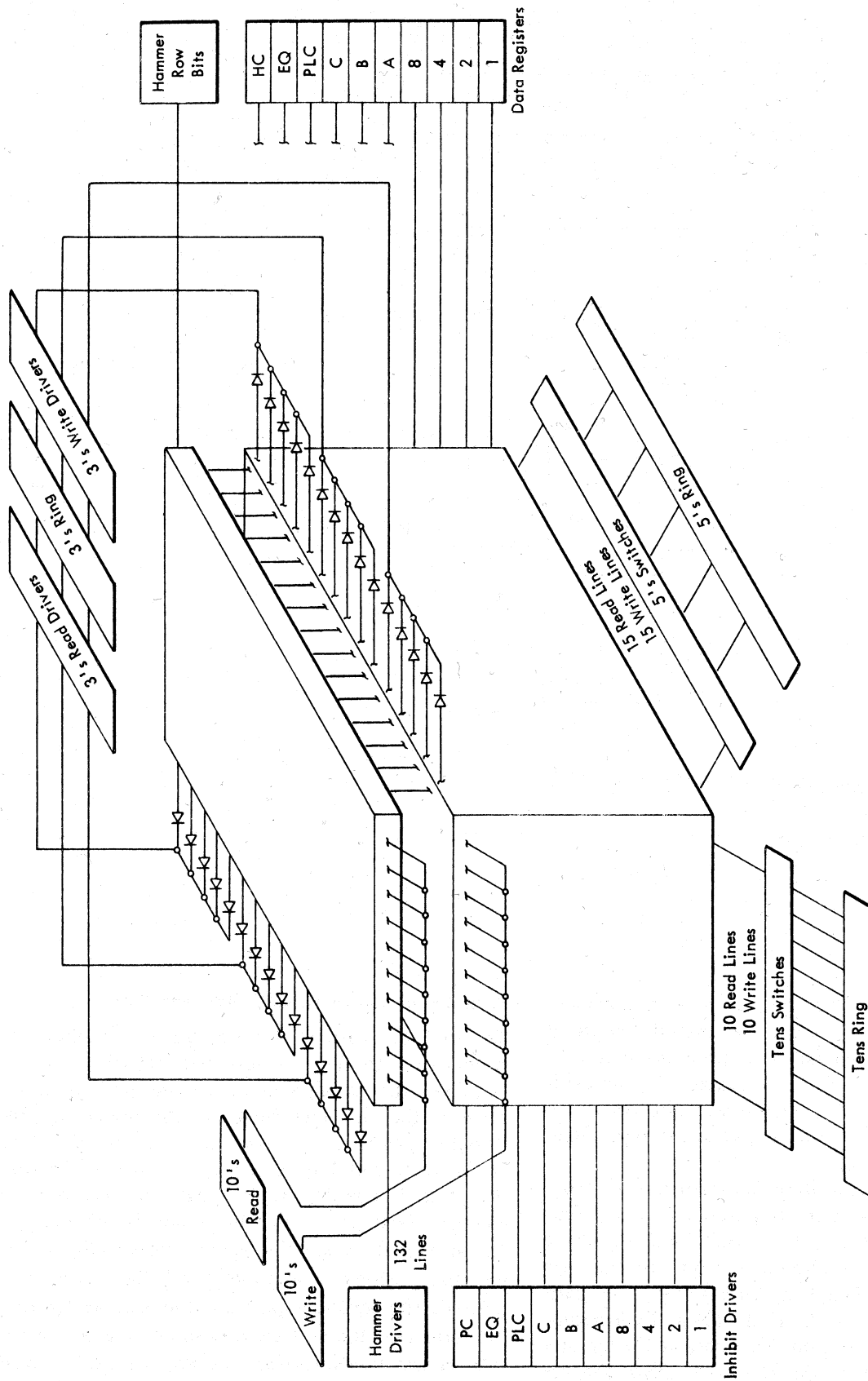
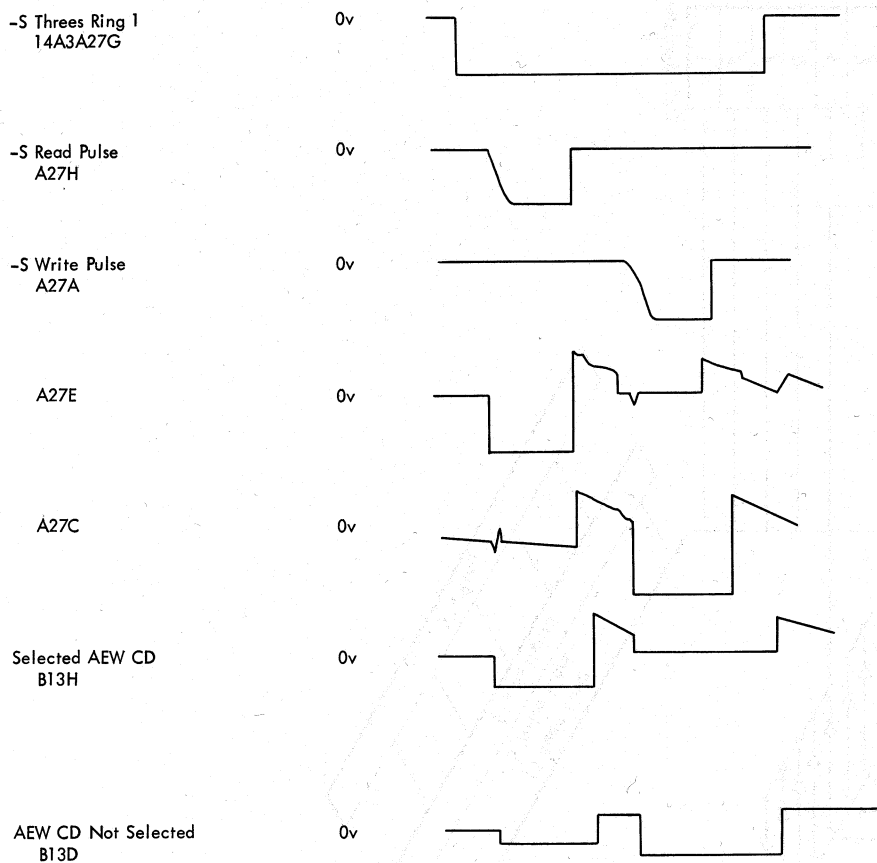


Figure 57. Print Storage Array



Waveforms from 53.24.01. Sync on -S Read-In or Scan Off-Line.
Load Mode. 2 usec/div. 5v/div

Figure 58. Print Buffer Waveforms

When not printing, the compare counter advances by one with each PSS-1 pulse. This provides constant identification of the character at print position 1. A print line can begin with any character at print position 1 (Figure 66). The home-reset pulse resets the compare counter to 1 to synchronize the type chain and the compare circuitry.

A subscan is approximately 555 microseconds long. Scanning 44 print positions requires only 484 microseconds (44 memory cycles). A delay latch is set at the end of 44 memory cycles and is reset with the start of the next subscan. The delay time is used to prepare the compare counter for the next subscan by bringing up an advance-by-two gate. This gate is up for one memory cycle (Systems 53.33.05) to allow the required number of advance-by-two pulses to reach the compare counter. The counter-advance pulses are developed on Systems 53.33.06.

Print Equal Compare and Hammer Fire

To print the correct character in any position, the printer circuitry must be able to detect when the type character that is aligned to a print position is the same as the character from the corresponding print storage position. A compare matrix (Systems 53.34.01-02 and Figure 67) compares the bits from the print storage data register with the bits from the compare counter. If the bit structure of the two characters is the same, the hammer driver (Figure 68) for that position is impulsed, and the character is printed. The equal-compare and the hammer-fire row-bit cores (for the addressed position) are set to provide information for error detection on the following scan.

The same three-ring addressing scheme that selects storage positions is used to select hammer drivers in

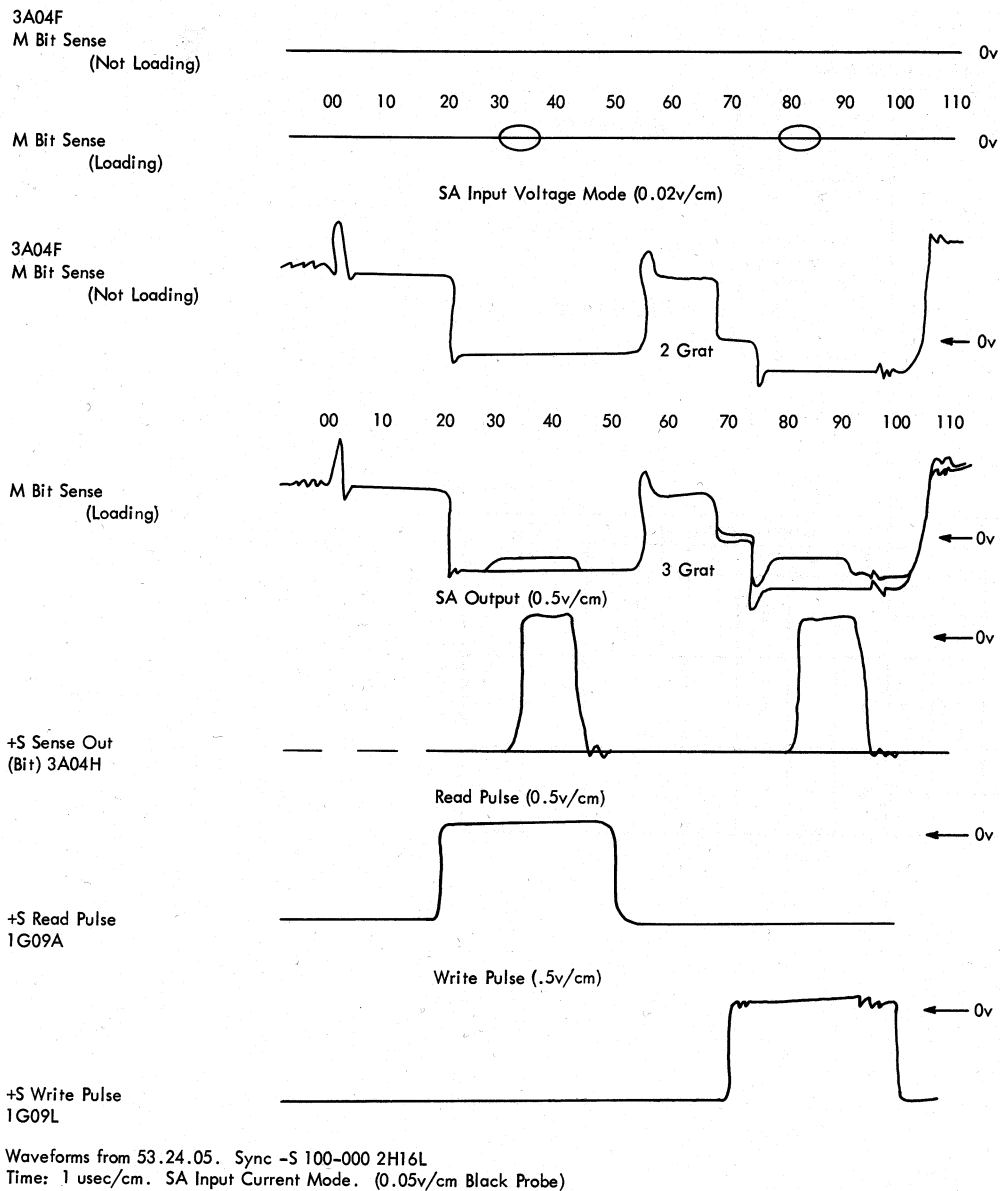


Figure 59. Print Buffer Scope Patterns

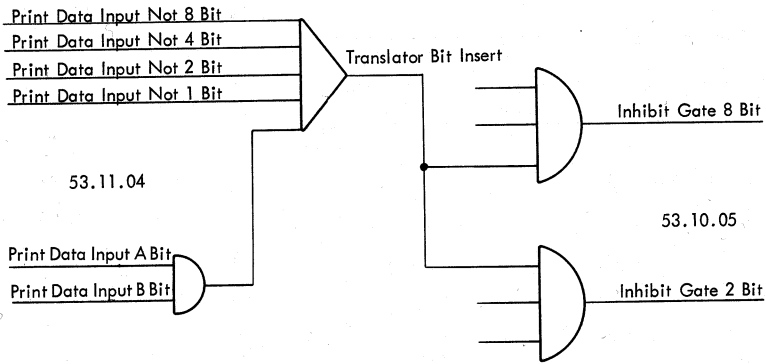
the driver matrix. A driver can be selected but it is not fired unless an equal compare condition exists. The chain is moving when printing occurs; therefore, all hammers should energize for the same length of time for proper print alignment. A latch-type hammer driver produces a timed hammer-magnet impulse for approximately 1.5 milliseconds. The driver set impulse that an equal-compare condition produces initiates the hammer-magnet current. This current continues until the reset pulse arrives. Ideally, each hammer driver would have its own reset pulse timed to occur exactly 1.5 milliseconds after the set pulse. However, this accuracy is not necessary and six timed reset pulses reset all the hammer drivers. The resets provide

nominal 1.5 millisecond hammer magnet impulses. Figure 69 shows the development of the six reset pulses. Figure 70 shows the location of the hammer-driver cards in panel 14A3.

Carriage Control

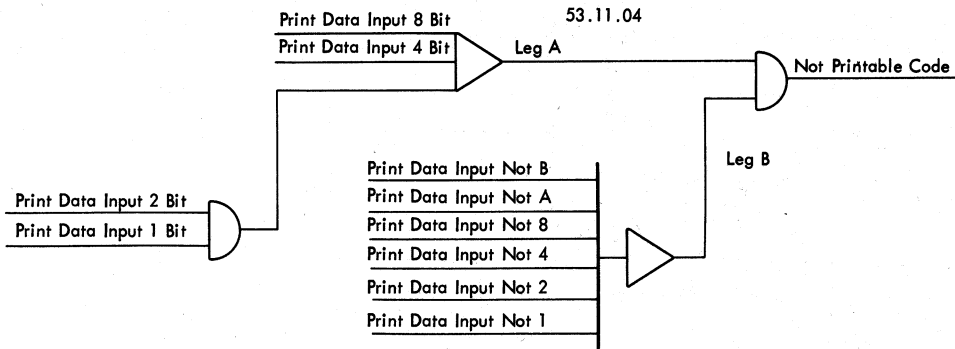
Carriage-Control Character Register and Decode

A forms control instruction is included in stored programs to provide program control of carriage spacing and skipping. This instruction sends a single carriage-control character(ccc) to the printer circuitry, where the character is gated to the ccc register. A decode circuit reconstructs the character from the bits present



BCD Character	BCD Code						Modified BCD Code						Type Character	
	B	A	8	4	2	1	B	A	8	4	2	1		
¢		A						A	8			2		‡
‡		A	8		2									
-	B						B		8			2		-
!	B		8		2									
&	B	A					B	A	8			2		&
?	B	A	8		2									

Figure 60. Code Translate



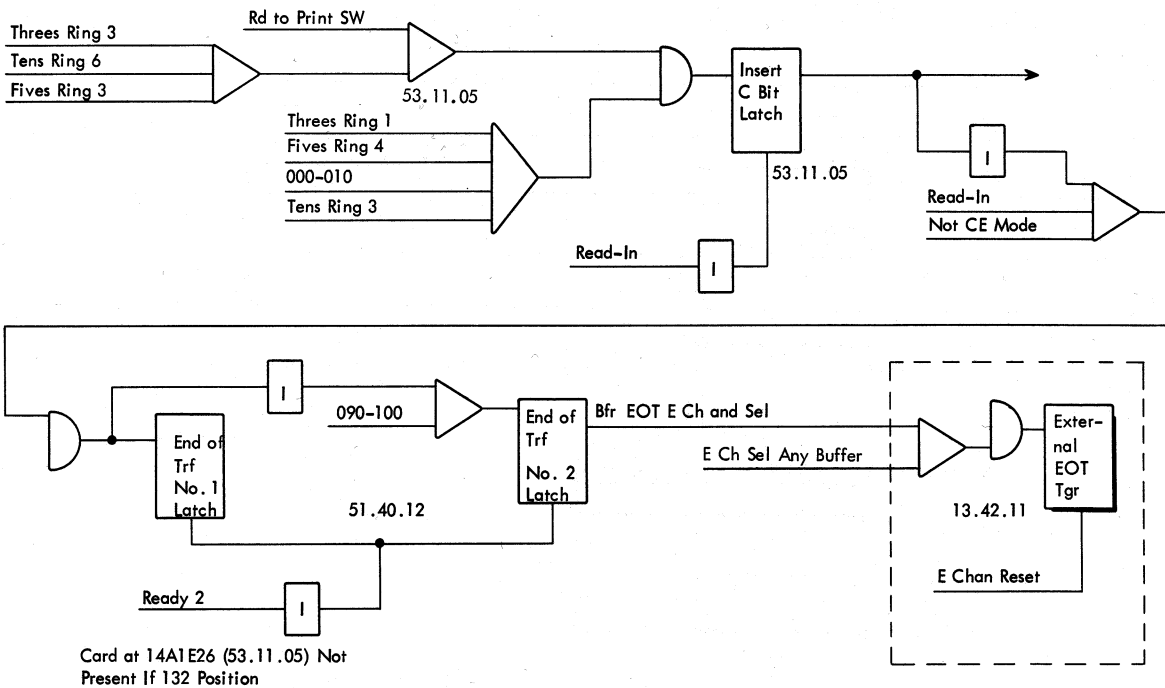
Notes:

Leg A defines characters containing combination of bits 8, 4 and 1 or 8, 4 and 2, so the following characters are considered "not printable":

((BA841)	;	(CB842)	"	(A8421)
<	(BA842)	△	(BB421)	:	(841)
≠	(CBA8421)	=	(CA841)	>	(842)
)	(CB841)	'	(CA842)	√	(C8421)

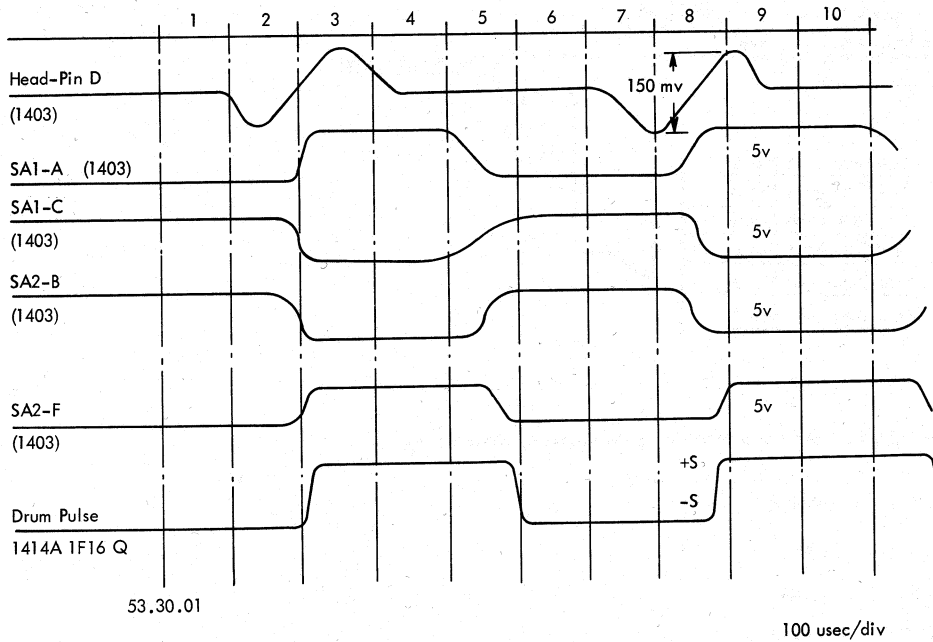
Leg B defines a blank, which is also considered a "not printable" character, making a total of 13 "non printables." The other three are dropped in the code translation.

Figure 61. Not Printable Code



Card at 14A1E26 (53.11.05) Not Present If 132 Position

Figure 62. C-Bit Insert



Sync Point: Chain Home Trigger 14A1F15P
 Use Delaying Sweep: A-Sweep - 100 usec/div
 B-Sweep - 500 usec/div

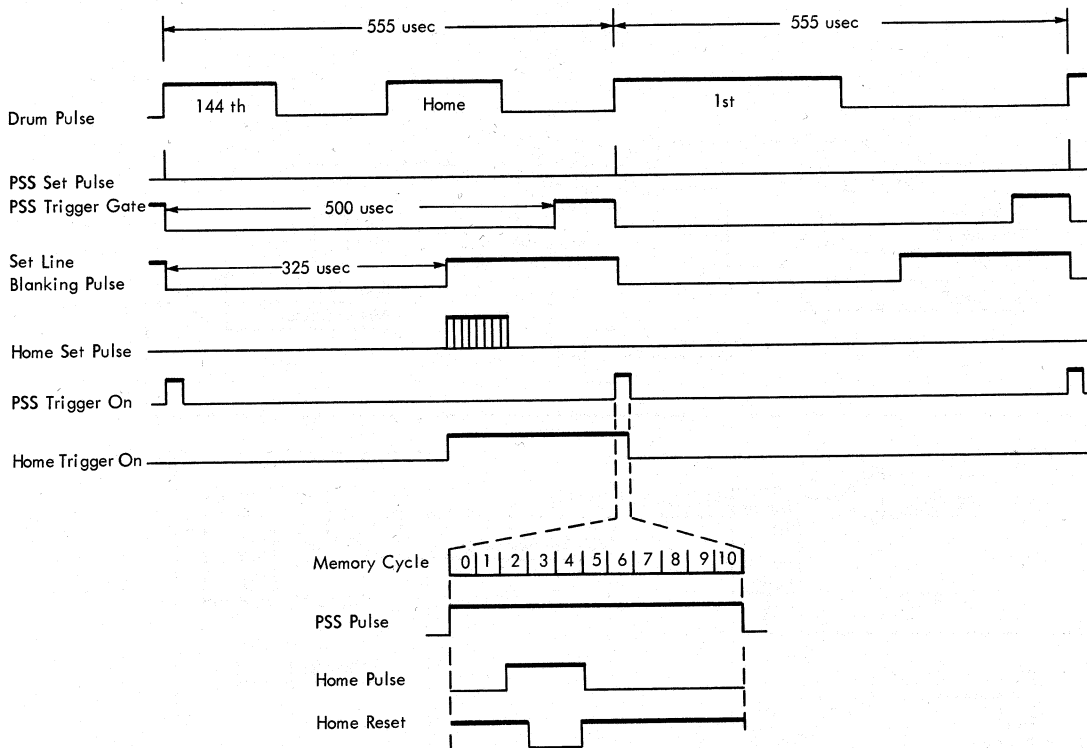
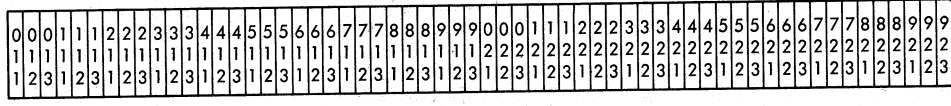
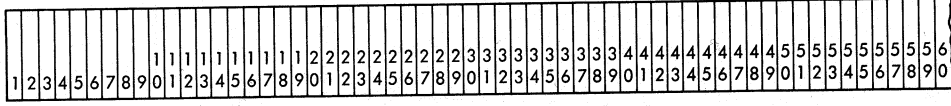


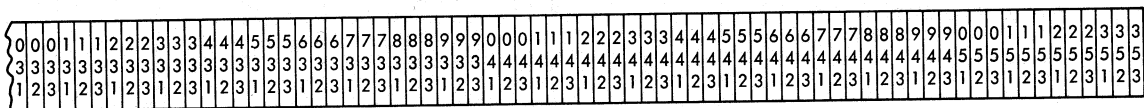
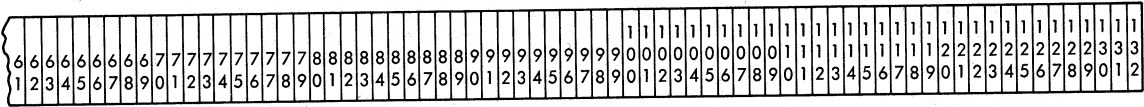
Figure 63. pss, Home, and Home Reset Pulses

Standard Type Array Character Sequence -- Type A2
 1234567890#@/STUVWXYZ+,%JKLmnopqr-\$.ABCDEFGHI&.

Rings Advance 3 10 5 on Read-In
 Rings Advance 10 5 3 on Scan-Out



Tens
 Fives
 Threes



Tens
 Fives
 Threes

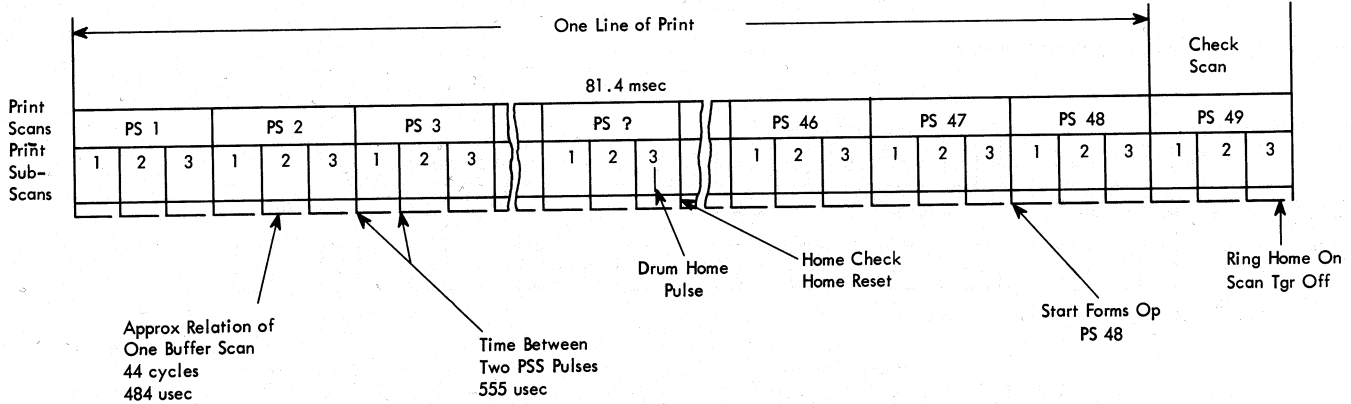


Figure 64. Print Scans

Print Time	Scan Time	Previous Character	Counter Activity	Resultant Character
Print Scan 1	PSS-1 mem cycle 1 (home pos)		Reset to 1	1
	PSS-1 mem cycle 2	1	Advance by 2	3
	↓	↓	↓	↓
	PSS-1 mem cycle 44	A	Advance by 2	C
	Between PSS-1 & PSS-2	C	Advance by 2	1
			5 Times	
	PSS-2, mem cycle 1	1	Advance by 1	2
	PSS-2 mem cycle 2	2	Advance by 2	4
	↓	↓	↓	↓
	PSS-2 mem cycle 44	B	Advance by 2	D
	Between PSS-2 & PSS-3	D	Advance by 2	2
			5 Times	
PSS-3 mem cycle 1	2	Advance by 1	3	
PSS-3 mem cycle 2	3	Advance by 2	5	
PSS-3 mem cycle 44	C	Advance by 2	E	
Between PSS-3 & PSS-1	E	Advance by 2	1	
		4 Times		
Print Scan 2	PSS-1 mem cycle 1	1	Advance by 1	2

Figure 65. Compare Counter Sequence

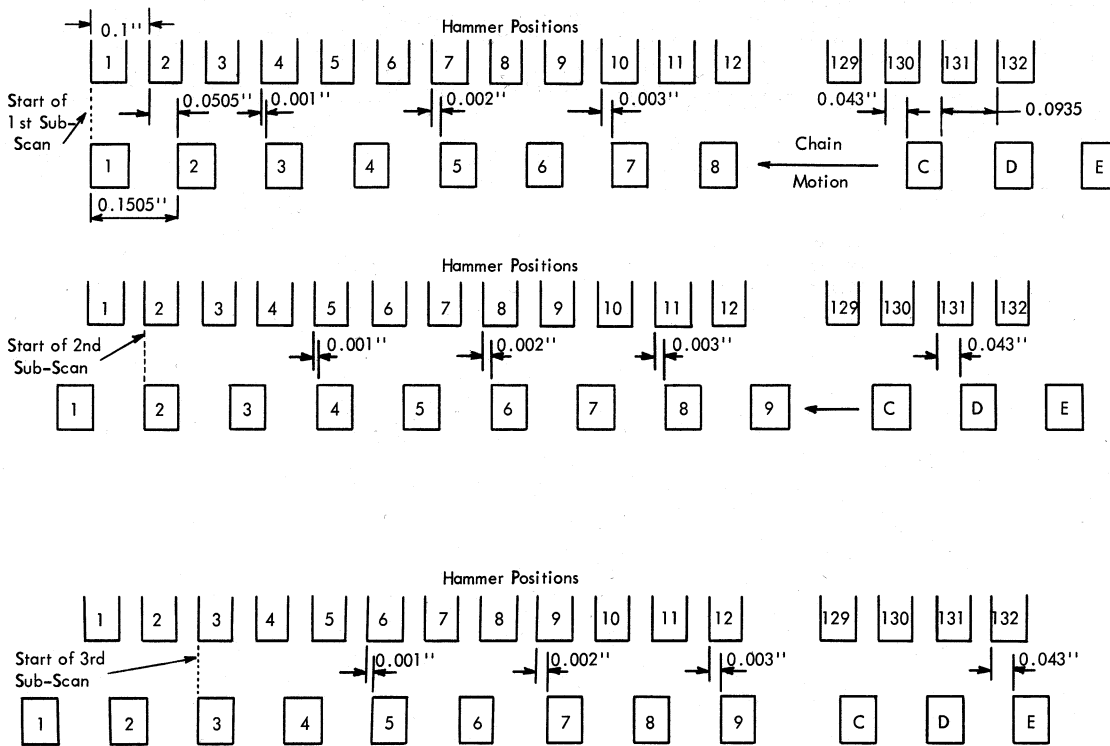


Figure 66. Hammer Position-Type Relationship

43.45.01
 BUFF PULSES
 RD 20-50
 WR 70-100
 INH 65-105
 RD GATE 20-50

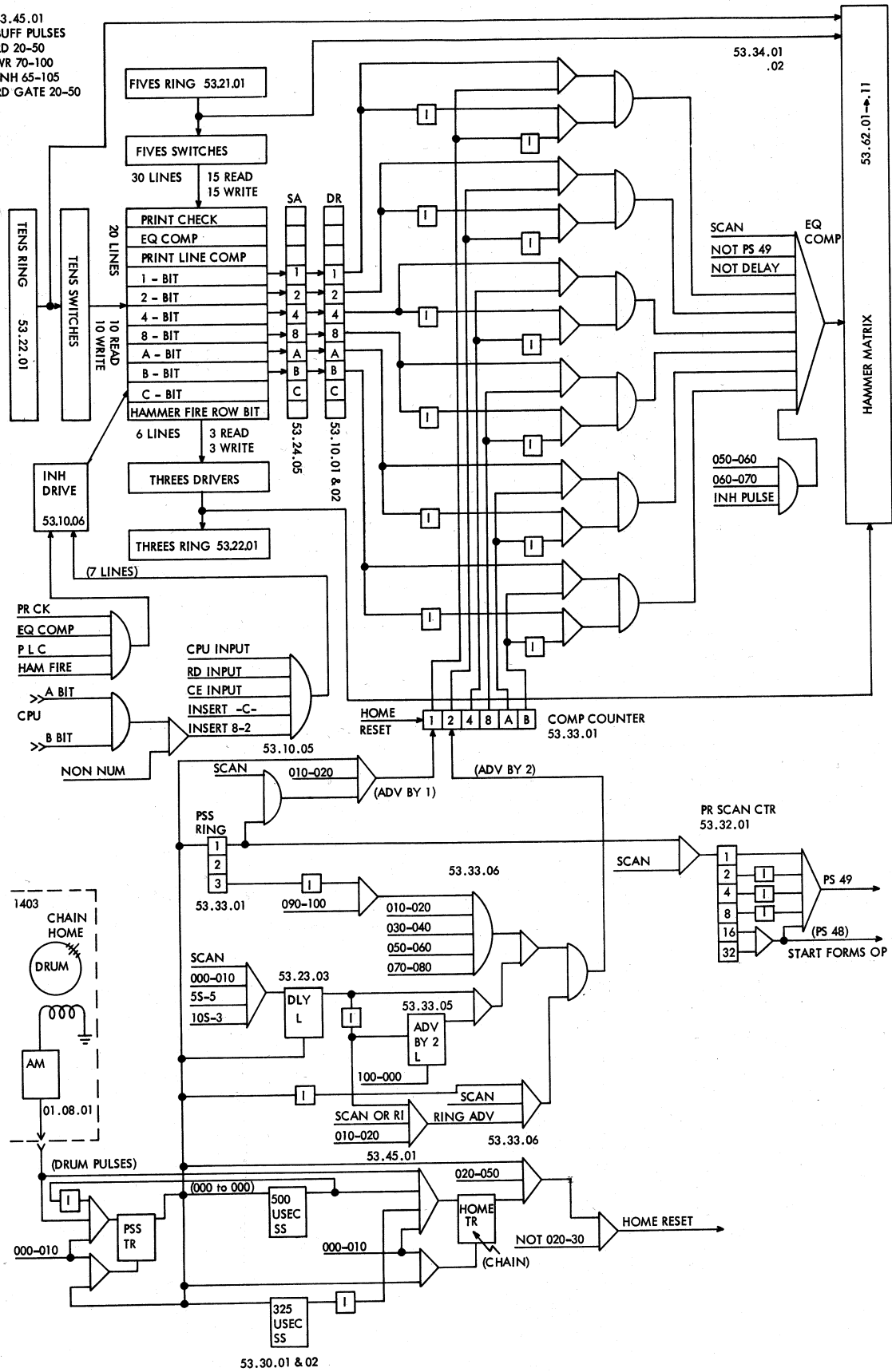


Figure 67. Compare Matrix

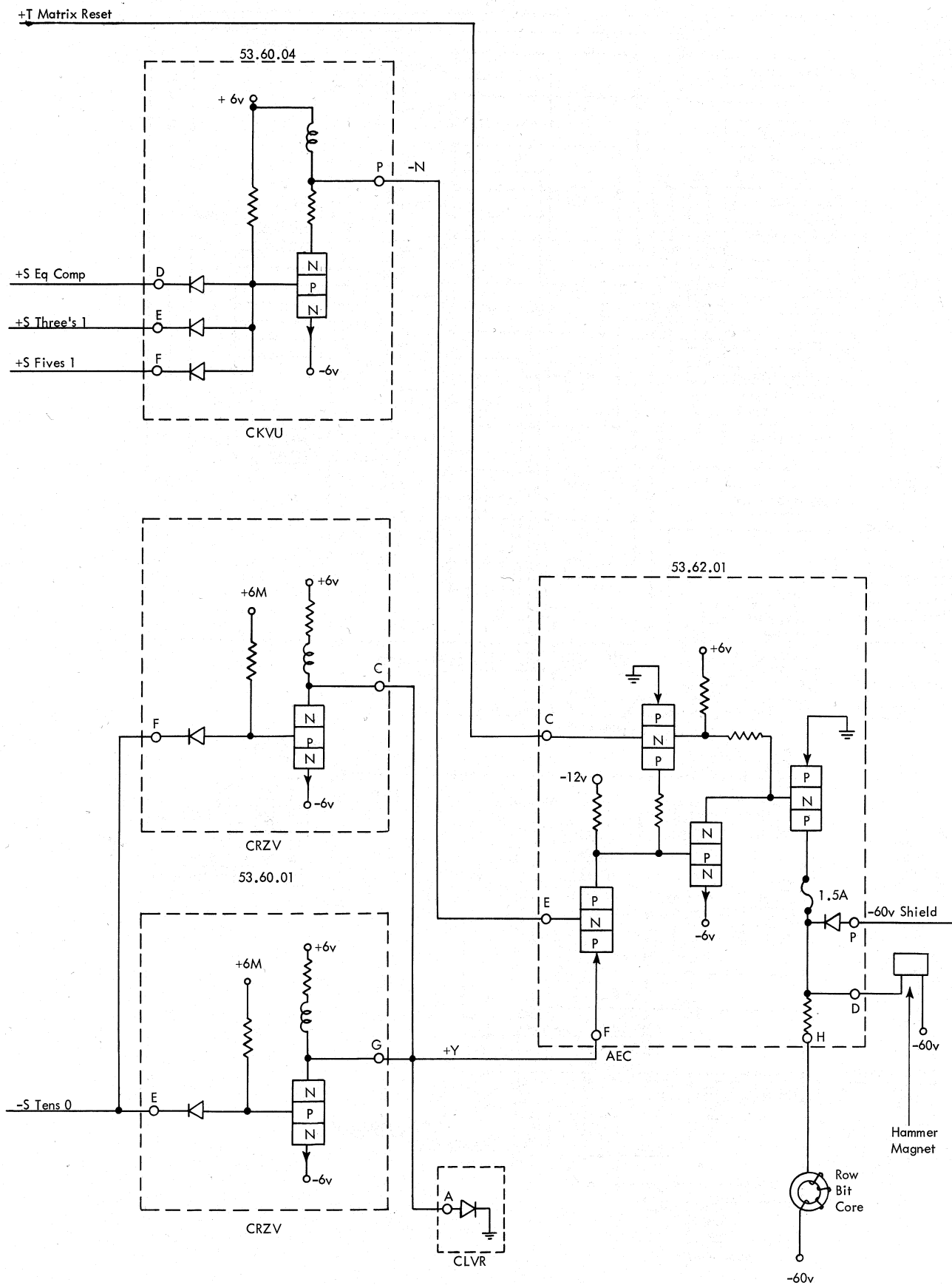
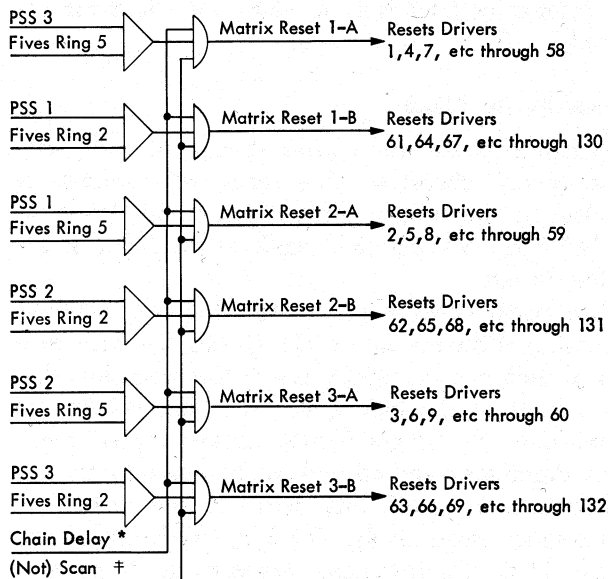


Figure 68. Hammer Drive



* Prevents printing until chain attains correct speed.
 † Prevents printing when not scanning out of the buffer.

Figure 69. Hamer Driver Resets

in the CCC register to determine the operation that is to be performed by the carriage.

The CCC register consists of six latches to store the six data bits, B, A, 8, 4, 2, 1 (Systems 53. 50. 01). The six bits are gated by a CCC register gate that signifies that the carriage is ready to accept a character, and that a forms-control instruction is called for.

Carriage Fast and Stop Controls

The carriage is a two-speed device. Speed depends on the operation that is being performed. All space

operations take place at slow speed. The speed of all skip operations (except manual restore) is governed by the length of the skip. Skips of eight spaces or greater start at high speed. The last seven spaces of any skip are made at slow speed. Thus, if a skip is seven spaces or less, it is made at slow speed. The condition of the channel latches controls skip speeds. Each latch is set by the stop brush and reset by the slow brush that corresponds to that position (Figure 71).

Carriage Magnet Control

There are four carriage magnets, labeled *space on* and *space off*, and *skip on* and *skip off*. For a slow-speed operation, the space-on and skip-off magnets energize. During a high-speed operation, both space-on and skip-on magnets must energize.

The space-on magnet energizes whenever the carriage is set in motion. The skip-on magnet energizes only for skips of eight or more spaces.

Spacing is accomplished by keeping the space-on magnet energized until the form moves the required distance (1, 2 or 3 spaces). The space-on magnet receives an impulse whose duration of which depends on the number of spaces desired. The impulse is formed by firing one of three single shots.

With a skip of eight spaces or more, the carriage-fast line is up and the carriage stop line is down (Figure 71). This energizes both space-on and skip-on magnets. When the slow brush signals that seven spaces remain in the skip, the carriage-fast line goes down. This removes the drive to the skip-on magnet, and impulses the skip-off magnet. However, the carriage stop line is still down; this maintains the space-on magnet-drive. The skip continues at slow speed

	00	10	20	30	40	50	60	70	80	90	100	110	120	130
0		H24	J22	K21	H19	J16	K15	H13	J11	K10	H07	J05	K04	H02
1	H25	J24	K22	H20	J19	K16	H14	J13	K11	H08	J07	K05	H03	J02
2	J25	K24	H22	J20	K19	H16	J14	K13	H11	J08	K07	H05	J03	K02
3	K25	H23	J22	K20	H17	J16	K14	H12	J11	K08	H06	J05	K03	
4	H25	J23	K22	H20	J17	K16	H14	J12	K11	H08	J06	K05	H03	
5	J25	K23	H21	J20	K17	H15	J14	K12	H10	J08	K06	H04	J03	
6	K25	H23	J21	K20	H17	J15	K14	H12	J10	K08	H06	J04	K03	
7	H24	J23	K21	H19	J17	K15	H13	J12	K10	H07	J06	K04	H02	
8	J24	K23	H21	J19	K17	H15	J13	K12	H10	J07	K06	H04	J02	
9	K24	H22	J21	K19	H16	J15	K13	H11	J10	K07	H05	J04	K02	

Figure 70. Hammer Driver Card Locations – Panel 14A3

until the brush senses the addressed tape-channel hole and brings up the carriage stop line.

With a manual restore operation, the addressed tape channel is 1, and the carriage spaces until the hole in channel 1 is sensed. A restore operation takes place at slow speed.

Channel Indicators 9 and 12

Two channels in the carriage tape determine the forms position. Impulses from the stop brushes for channels 9 and 12 set latches that the stored program can interrogate. Sensing holes in tape channels 9 and 12 sets corresponding channel indicator latches. The next hole that is read in any tape channel resets the latches.

A forms stop interlocks the 1403, and manual intervention is required to restore the printer to the ready status.

Forms Control Operation

A single character is sent to the carriage circuitry to control forms skipping and spacing (Figure 72). The bit structure of this character signals the tape-controlled carriage either to take a single, double, or triple space (Figure 73), or to skip to the next hole in a designated tape channel. The spacing and skipping can be executed either immediately or after the next print command.

If printing is taking place when the forms command is initiated, the carriage operation is delayed until the end of the print line. Also, if the forms command is an after print command, the carriage operation is delayed until the end of the next print line.

The carriage control character register resets at completion of the forms operation to prevent repetitive operation.

Checking Features

Printer Sync Check

To print correct information, the printer-compare circuitry synchronizes with the type chain. The 1-type slug always aligns at print position 1 when the home pulse occurs because of mechanical linkage between the chain and the timing disk. The compare counter should always contain a 1 and the PSS-1 trigger should be on at this time, if they are properly synchronized with the chain. If the compare counter contains anything but a 1-bit at home-pulse time, a sync check sets the indicator latch (Figure 74). In addition, if printing is taking place when the sync check occurs,

the print-error latch sets to show that an error occurred.

Printer Parity Check

Information is stored in print storage in odd-parity form. Every character that reads into storage is checked by the printer parity-check circuit (Systems 53.44.01-02). The check is made at the input of the inhibit drivers.

Two parity-check triggers are reset OFF near the beginning of the memory cycle. During the write portion of each memory cycle, any of the seven bits that are present at the inputs of the inhibit drivers are switched to the trigger inputs. Binary trigger inputs allow flipping on and off with successive set pulses.

The 1, 4, A, and C bits switch to TR-1 at 6, 7, 8, and 9 times, respectively. The 2, 8, and B bits switch to TR-2 at 6, 7, and 8 times, respectively. If an even number of bits is at the inhibit-driver inputs, the triggers are either both on or both off at ten-time when the error sample occurs, and a C-bit check results. An odd number of bits causes one trigger to be on and one off when they are tested at ten-time. Therefore, the C-bit check signal is not generated.

Print-Error Detector

Four core planes of print storage detect and store errors. These are: print-line-complete, equal-compare, hammer-fire row-bits, and hammer-check.

The print-line-complete cores set during a CPU transfer for those print positions that contain a printable character. During a memory cycle, an equal-compare blocks the regeneration of the print-line-complete core, and sets the equal-compare core for that position. If an equal-compare occurs for a position that does not contain a printable character, an error is indicated, and the hammer-check core is set for that position.

An equal-compare condition impulses the hammer driver that sets the corresponding hammer-fire row-bit core. If an equal-compare core is set, the corresponding hammer-fire row-bit core should be set, and vice versa. If either core sets without the other, a print error results on the following print scan when that position again reads out. The error sets the corresponding hammer-check core.

After the 48th scan, all positions that contained a printable character should be printed, and no print-line-complete core should remain set. Any print-line-complete core that remains on when the 49th scan occurs causes a print error.

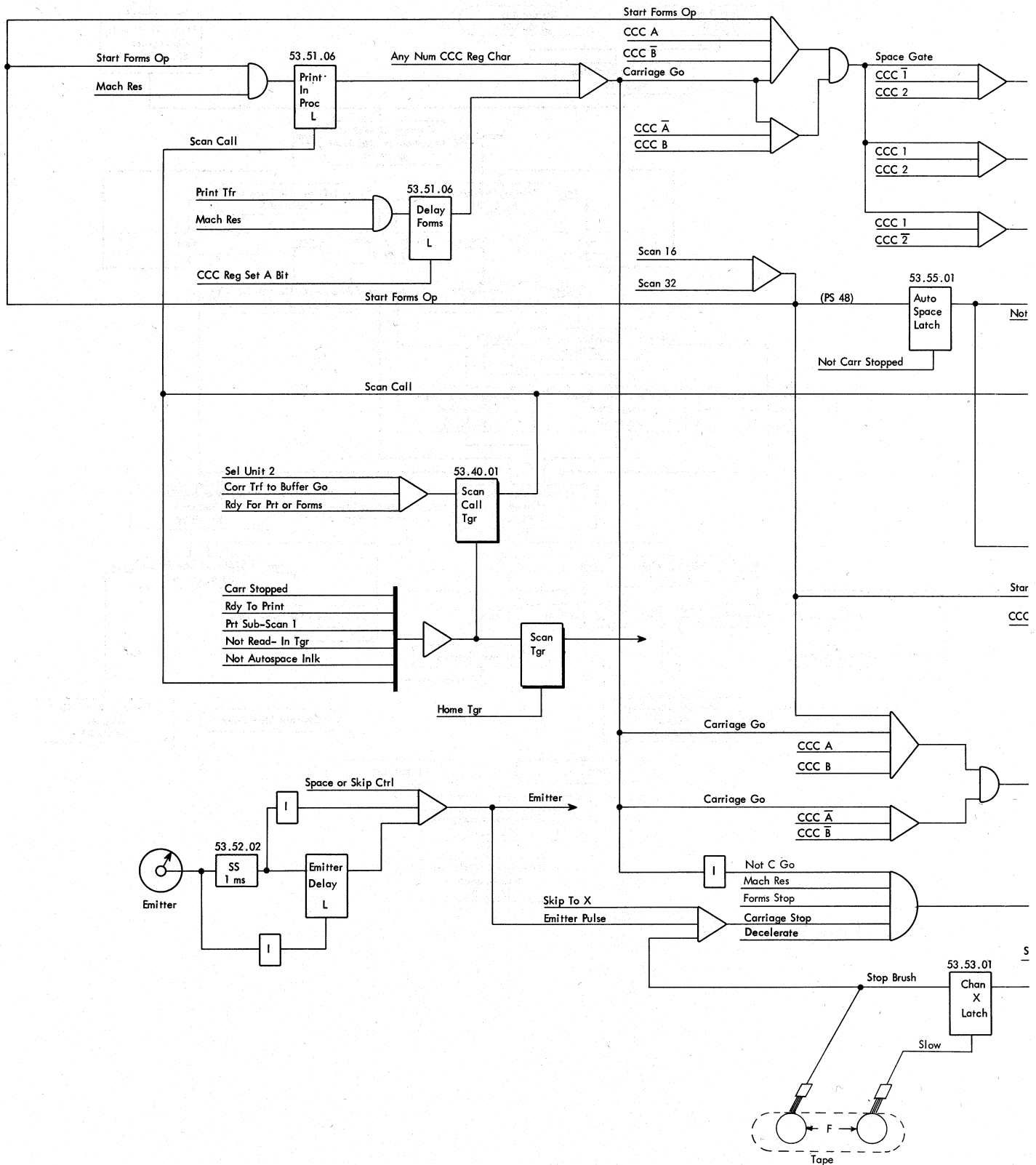
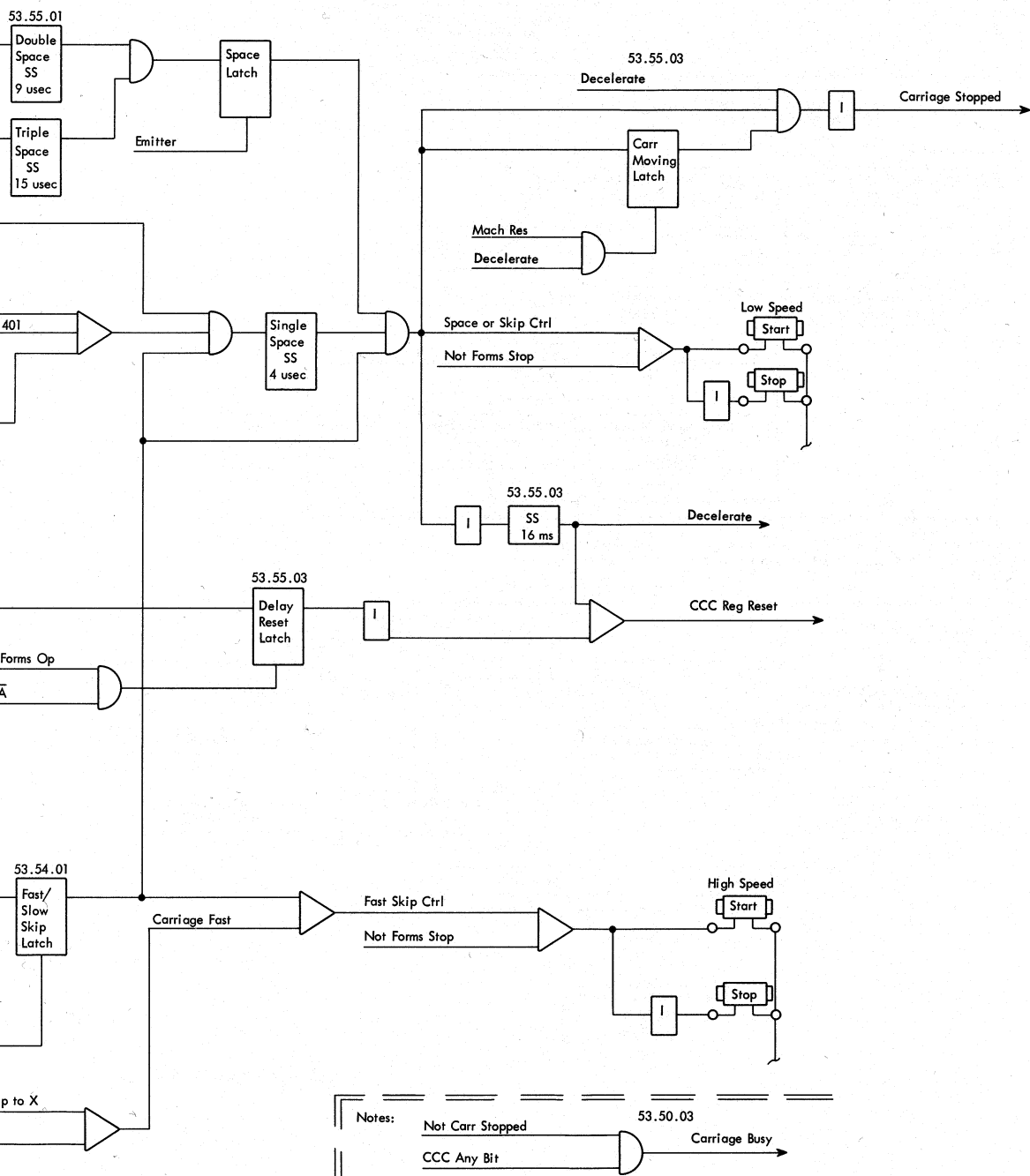


Figure 71. Carriage Controls



Notes:

Not Carr Stopped $\overline{53.50.03}$

CCC Any Bit $\overline{53.50.03}$ Carriage Busy

$\overline{A} \cdot \overline{B}$ Immed Skip

A · B After Skip

A · B After Skip

$\overline{A} \cdot \overline{B}$ Immed Space

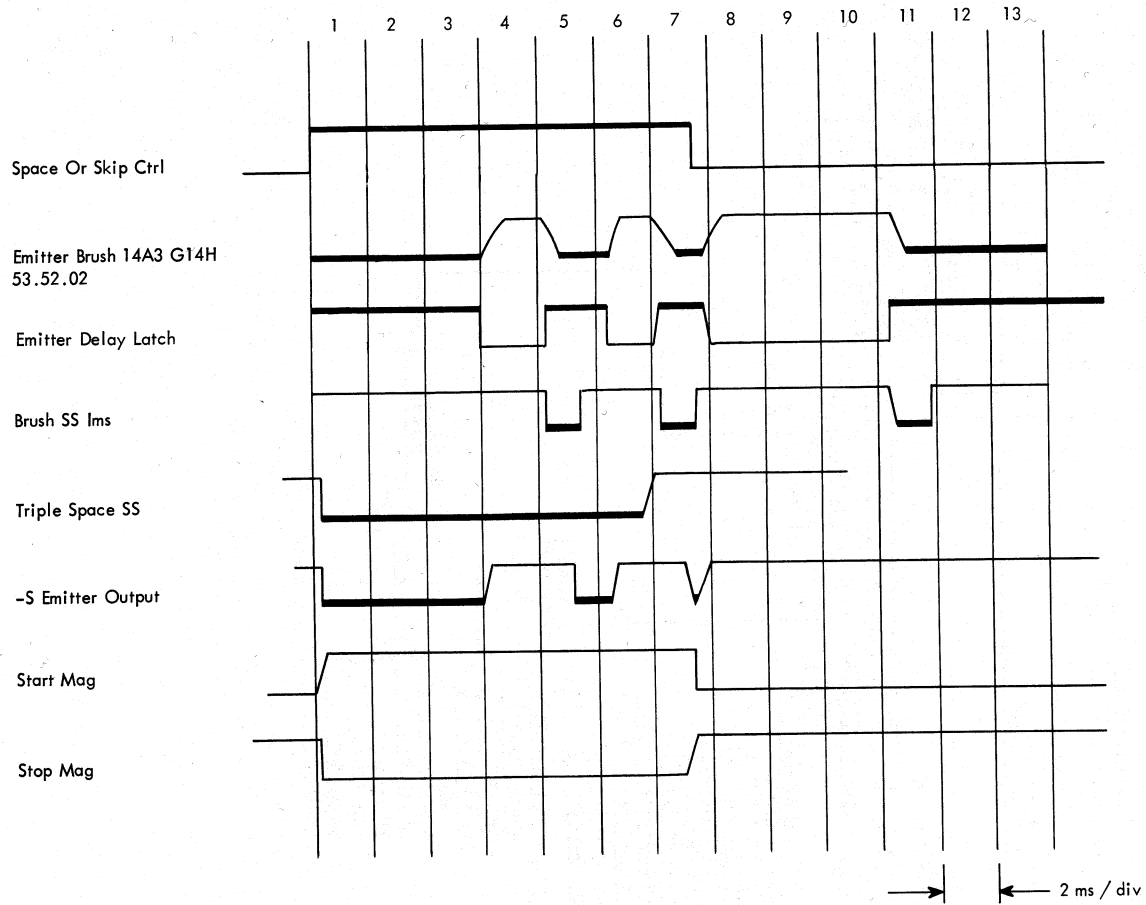


Figure 73. Triple Space Waveforms

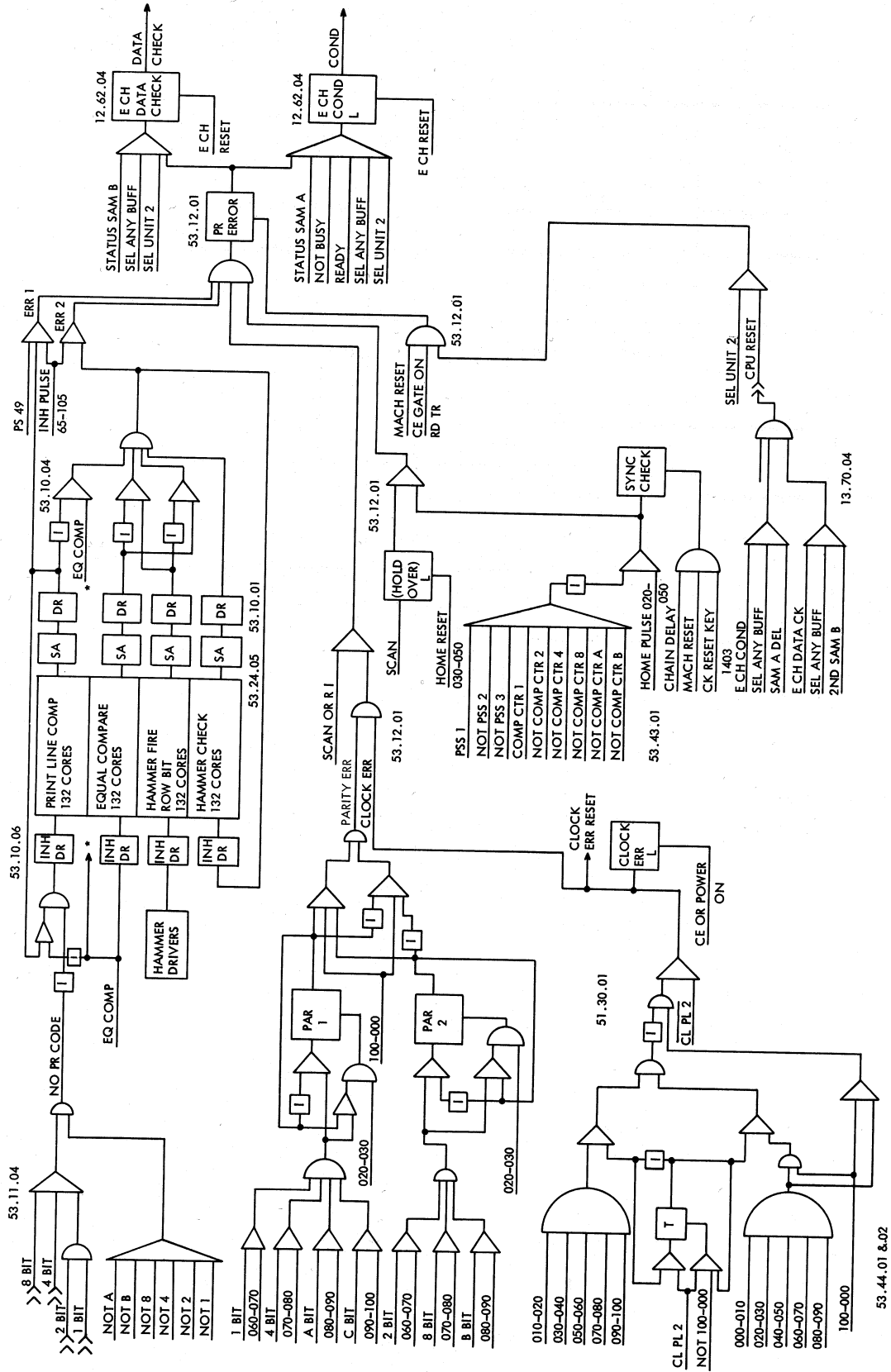


Figure 74. Print Error Circuits

The CE panel provides the Customer Engineer with full control of the integrated buffers and print buffers as well as the I-O devices. The panel allows him to remove selected I-O units from CPU control so that he can test and service these units off-line. Flexibility in the controls allows many diagnostic procedures to be set up as aids in trouble analysis. Each buffer can be isolated from its I-O device for testing, or it can be tested in conjunction with the mechanically active I-O device.

Switches, Keys, and Lights

The diagnostic panel (Figure 75) consists of two functional areas: an indicator panel and a switch panel. The first area is made up of various yellow lights which identify characters by bit structure, buffer address, and the buffer with which they are associated. Error indications are shown by red lights.

The second area contains the controlling switches and keys for off-line operations.

Panel Indicators

Figure 75 shows the CE panel. The upper half of the panel contains the indicators which will be discussed individually.

INTEGRATED BUFFER

Integrated buffer lights indicate which integrated buffer section is in operation. These lights go on when the associated "scan latch" is set (Systems 51.45.04).

BUFFER ADDR

Buffer addr lights show the buffer address of each character as it is scanned by the integrated buffer circuits. The indications refer to card columns for customer convenience. The CE must realize that the buffer location actually addressed is one position less than the address indicated.

NOTE: When operating in single cycle mode, the indicated buffer location has been already processed.

Also, a light indicates an end-of-scan condition. This light is normally on unless a scan of integrated buffer is in progress (Systems 51.45.01).

BUFFER REG

The bit structure of each character is displayed as it appears in the BCD data register. Hole-count check core status is also indicated. Parity and hole-count

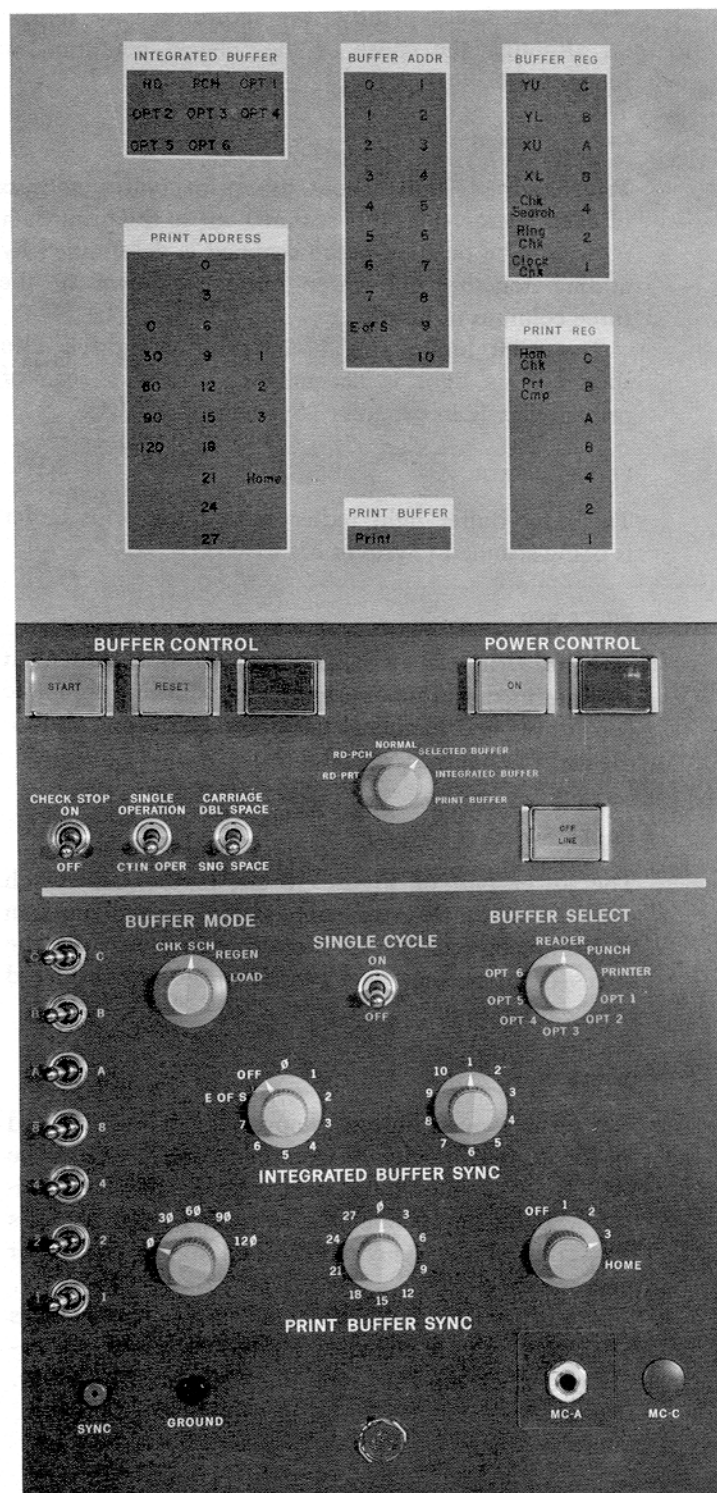


Figure 75. IBM 1414 CE Panel

errors are also indicated by the red check-search light with appropriate switch settings. Red lights also show ring-check and clock-check conditions (Systems 51. 45. 01-.03).

NOTE: Once they are on, the ring check and clock check lights will remain on until reset by the CE panel reset key. Consequently, the indicator may remain on although the cause of the "check" condition no longer exists.

PRINT ADDRESS

Print address lights show the print buffer address of each character as it is scanned out to the print data register. The position being scanned is determined by adding together the three numbers shown in the three columns of lights.

The print buffer ring home position light is also shown. This light is normally on unless a scan of print buffer is in progress (Systems 51. 45. 04).

PRINT BUFFER

The print buffer light indicates that the print buffer is being scanned (Systems 51. 45. 06).

PRINT REG

The bit structure of each character is shown as it appears in the print data register. Print-line-complete core status and hammer-check core status are also indicated (Systems 51. 45. 06).

Panel Switches

The lower half of Figure 75 shows the CE switch panel. The function of each switch is explained in the following paragraphs. Note that in most cases the status of more than one switch must be considered for the operation.

OFF-LINE

The off-line push button removes the buffer selected by the CE panel switches from CPU control. When the 1414 is in off-line status, this push button is illuminated. Each depression of the push button changes the status of the synchronizer (on-line to off-line or vice-versa).

In off-line mode, the CE panel power control keys are activated. All switches on the CE panel are ineffective when the 1414 is on-line (Systems 51. 45. 09).

POWER CONTROL

Two keys (ON and OFF) control power to the synchronizer when the 1414 operates off-line. When operating on-line, the using system controls power.

BUFFER CONTROL

Three keys provide start, stop and reset functions. The start key initiates the selected operation when in off-line mode. Under normal operation, CPU controls this function.

Pressing the reset key resets some of the error-detection circuits and activates the stop circuits (the stop might occur before the operation is completed).

Pressing the stop key stops the synchronizer after the operation in progress ends (Systems 51. 45. 13).

CHECK STOP

With the check-stop switch on, the synchronizer stops after the operation in which an error was detected. When this switch is off, the operation continues after an error if all other switch settings call for continuous operation.

NOTE: The check-stop switch is effective only when the Off-line mode switch is in the RD-PRT, RD-PCH, or SELECTED BUFFER position (Systems 51. 45. 09).

OP CONTROL (SINGLE OP/CTIN OP)

In the continuous operation position this switch has no effect on synchronizer operation. When the switch is in the SINGLE OPERATION position, it causes the 1414 to perform only a single operation each time the start key is depressed. The operation can be a single card, single scan, single print line, as controlled by other switch settings (Systems 51. 45. 09).

NOTE: The setting of the check-search or single-cycle switches may prevent a complete operation.

SPACE

The space switch causes either a single or double spacing on the printer when operating off-line.

OFF-LINE MODE (UNLABELED ON CE PANEL)

The off-line mode rotary switch (Systems 51. 45. 11) selects the type of off-line operation to be performed. It allows only one or two buffer units to be removed from the line, leaving other buffer units available for use. The switch is active only when the 1414 is in off-line mode. This switch must be set in a position other than normal before any off-line operation can be started. The function of each switch position is as follows:

Rd-Prt (Reader to Printer): Cards are read from the 1402 and listed on the 1403.

Rd-Pch (Reader to Punch): Cards are read by the reader section of the 1402 and reproduced, card for card, by the punch section of the 1402.

Selected Buffer: This position allows selection of any buffer under control of the buffer-select switch. Only the selected buffer is removed from the line.

The I-O unit associated with the selected buffer also operates mechanically.

Integrated Buffer: This position removes the integrated buffer from the line for servicing. The buffer-select switch further determines which buffer is to be tested (reader, punch or one of the six options).

NOTE: The INTEGRATED BUFFER position does not permit testing of the print buffer and does not mechanically activate the I-O devices. Regardless of the integrated buffer portion selected, the operation is further controlled by the buffer mode switch setting (see "Buffer Mode" in this publication).

Print Buffer: This setting removes the print buffer from the line for servicing. At this setting, the positioning of the Buffer Select switch has no effect and the printer cannot be mechanically operated. Print buffer testing is further controlled by the buffer mode switch.

BUFFER SELECT

The buffer select switch, in conjunction with the off-line mode switch, selects a particular buffer to operate off-line (Systems 51. 45. 10, 51. 45. 14 and 51. 45. 15).

This switch is effective only when the off-line mode switch is set at the SELECTED BUFFER OR INTEGRATED BUFFER position. Refer to the description of these two settings of the off-line mode switch to determine the full affect on the synchronizer.

BIT ENTRY SWITCHES (UNLABELED ON CE PANEL)

The seven bit entry switches (C, B, A, 8, 4, 2, and 1) are used to enter any character into a selected buffer position. They are active with the off-line mode switch in the INTEGRATED BUFFER OR PRINT-BUFFER position if the buffer mode switch is set to LOAD position as explained in the description of that switch.

The bit entry switches are also active if the off-line mode switch is in the SELECTED BUFFER position and if an *output* device is selected by the buffer select switch. In this case, all positions of the selected buffer are loaded with the switch contents before the buffer is scanned out to the output device (Systems 51. 45. 07).

BUFFER MODE

The buffer mode switch (Systems 51. 45. 12) allows three types of operations when the off-line mode switch is in the INTEGRATED BUFFER OR PRINT BUFFER position. Each switch setting is used as follows:

Load: This operation causes regeneration of the data from the selected buffer to be blocked and the bit switch contents to be entered in its place.

Regen: This operation allows data read from the selected buffer to be regenerated. Errors are ignored.

Chk Sch (Check Search): This operation allows data

read from the selected buffer to be regenerated. If an error occurs, the operation is stopped. If the stop occurs in integrated buffer mode, the check search indicator goes on. Errors will cause a stop in print buffer mode without lighting the check search indicator.

NOTE: The check search light may glow when the buffer mode switch is in the "regen" position. A stop will not occur however, unless the buffer mode switch is set at CHK SCH position.

SINGLE CYCLE

The single cycle switch is effective when the off-line mode switch is in the INTEGRATED BUFFER OR PRINT BUFFER position. When on, it causes the 1414 to stop at the end of each buffer cycle. When off, it has no effect (Systems 51. 45. 09).

INTEGRATED BUFFER SYNC

The integrated buffer sync switches develop a sync signal (available at the sync hub) corresponding to the integrated buffer address dialed. The selected address refers to card columns, not the actual buffer address as the CE knows it. The sync pulse occurs at 080-100 time of the selected buffer cycle (Systems 51. 50. 04 and 51. 45. 08).

An "end-of-scan" setting also develops a positive pulse when end of scan is reached.

NOTE: The print buffer sync switches must be off when using these switches.

PRINT BUFFER SYNC

These print buffer sync switches develop a pulse, available at the sync hub, corresponding to the address selected. The sync pulse occurs at 080-100 time of the selected buffer cycle (Systems 51. 45. 08 and 51. 50. 04).

An additional setting supplies a positive sync pulse when the printer home trigger comes on at the end of a scan.

NOTE: The integrated buffer sync switches must be off when using these switches.

SYNC

The sync hub emits pulses to synchronize an oscilloscope during servicing. The sync switches define the pulses. The CE should be aware that a "CE AND" circuit is provided for further conditioning of the sync pulse (Systems 51. 50. 04).

GROUND

Ground potential for the oscilloscope (Systems 51. 45. 09).

REMOTE BOX RECEPTACLE (UNLABELED ON THE CE PANEL)

When the remote box is plugged into the receptacle, it gives the CE remote start, stop, and reset control (Systems 51. 45. 13).

MC-A, MC-C

The MC-A and MC-C hubs provide marginal checking of frames 1414, A and C respectively. The marginal checking power supply is plugged into these jacks. If only an A frame is installed, the hub is labeled MC with no frame designation.

CE Panel Switch Circuits

Figure 76 shows the back panel terminal numbering of the CE panel (chassis 8).

Figure 77 shows the wiring of the major off-line mode switches. Here the gating lines are developed to control off-line buffer selection. These lines in conjunction with the CE Go circuits (Figure 79) control the selected off-line operations.

CE Off-Line Start-Stop Circuits

The logic of the CE start controls is shown in Figure 78. This logic applies to all off-line operations excluding single cycling.

The major components involved are the start latch the CE Go trigger and the stop latch (Figure 79). Each component will be discussed individually.

Start Latch

The start latch is set each time the start key is depressed and is reset when the start key is released.

When the start latch is reset, a pulse is generated to set the CE Go trigger.

CE Go Trigger

The CE Go trigger coming on initiates the selected off-line operation. When the operation gets under way, the CE Go trigger is reset. When the operation ends, an attempt is made to set the CE Go trigger again. If this attempt is successful, the r-o operation is repeated. If not, the start key must be depressed in order to set the CE Go trigger and start the operation.

Two things can prevent the automatic set of the CE Go trigger at the end of an operation: an r-o check stop condition or the stop latch being on. (r-o check stop conditions can exist only in reader to punch, reader to printer or selected buffer modes.)

Stop Latch

The stop latch on prevents setting the CE Go trigger at the end of an operation. It comes on under one of the following conditions:

1. A selected r-o device becomes not ready.
2. The stop key has been depressed.
3. The reset key has been depressed.
4. The op control switch is in the SINGLE OP position.
5. The 1414 is in integrated-buffer mode and the single-cycle switch is on.

NOTE: Since the single cycle switch is effective only in integrated-buffer and print buffer modes, its effect is not shown in Figure 78. See the text on integrated buffer operation for the function of the single cycle switch and the single cycle trigger.

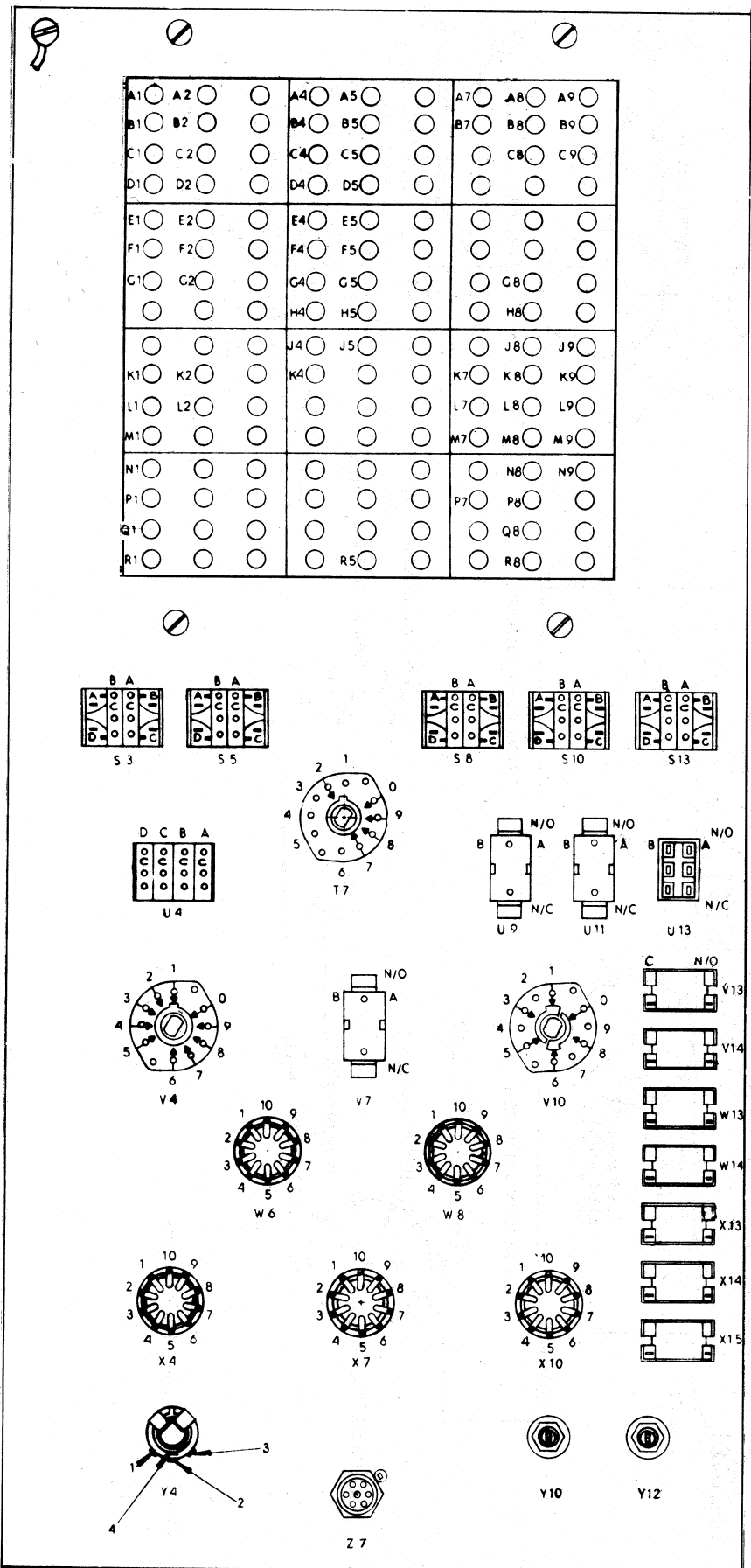


Figure 76. CE Panel - Wiring Side

OFF-LINE SW
51.45.11.1

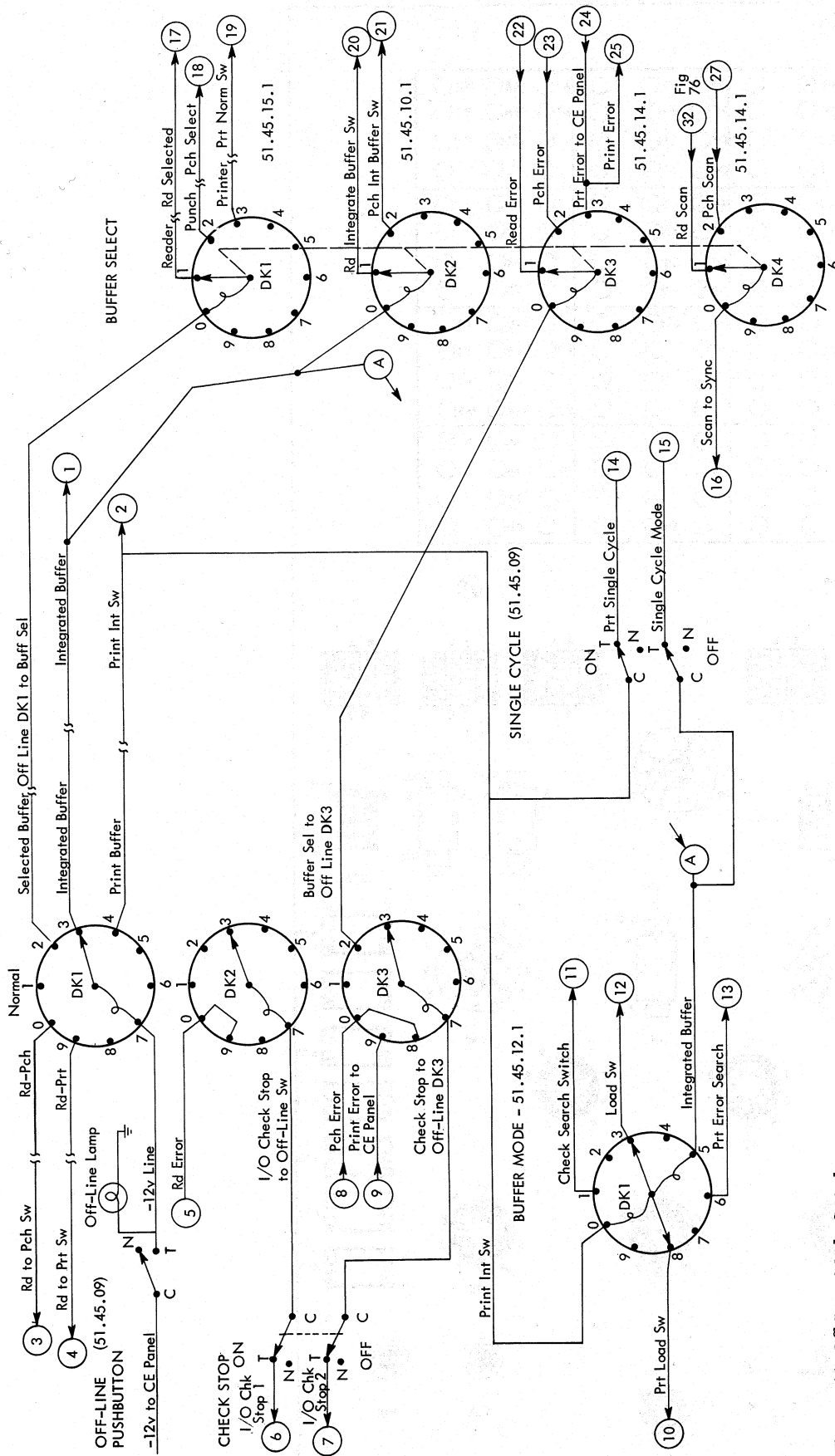
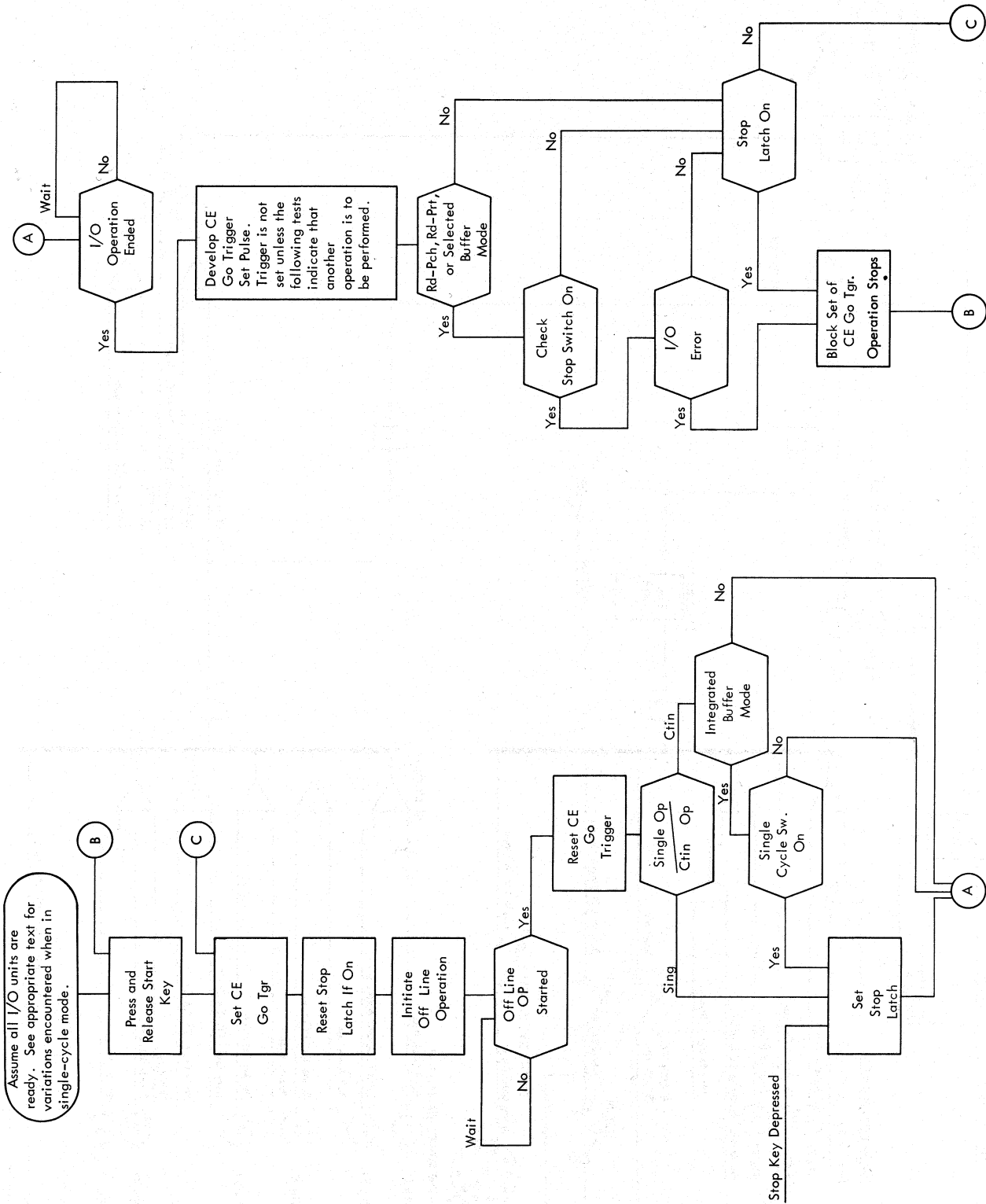


Figure 77. Off-Line Mode Switches



Assume all I/O units are ready. See appropriate text for variations encountered when in single-cycle mode.

Figure 78. Off-Line Start-Stop Controls

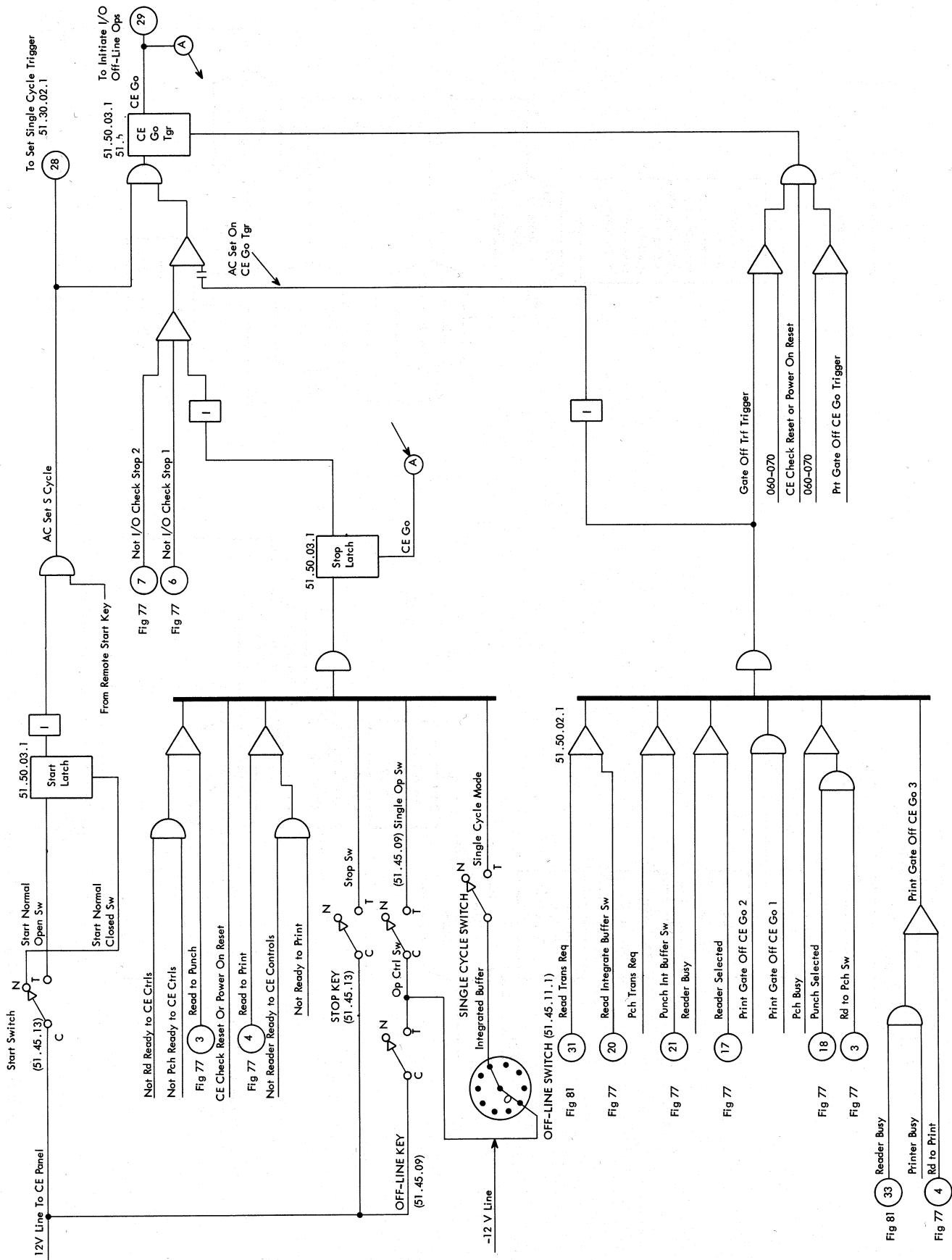


Figure 79. Start-Stop Controls

Card Reader Selected Off-Line Mode

Functions

In the selected-read buffer off-line mode, the read buffer is removed from CPU control without affecting the other integrated buffer units. A transfer scan is taken during which read buffer contents are regenerated. When the scan is complete, the card reader clutch is energized, and the next card is read into buffer. (Reader must be made ready beforehand.)

NOTE: The reader ready light does not come on in off-line mode even though cards are properly run in. The operation is under control of the op control and check stop switches.

Errors during entry to buffer from the card are detected and stop the machine if the check stop switch is on. Errors occurring during the transfer scan will not cause a stop regardless of switch settings.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	Push button illuminated. Enables off-line mode switch.
Off-Line Mode	Selected Buffer	Enables buffer select switch.
Buffer Select	Reader	Removes only the reader from CPU control.
Check Stop	ON	Stops the operation after the reader cycle in which an error occurs.
Op Control	Single Op	Stops the operation after each card feed cycle. Depressing the start key restarts the operation.
	Ctin Op	Allows continuous operation until the reader becomes not ready or a "check stop" occurs.
Buffer Mode	-	No effect.
Single Cycle	-	No effect.
Bit Switches	-	No effect.

Before attempting to isolate a failure in this mode, the CE should first test reader buffer in integrated mode. If the 1414 fails in integrated mode, the CE should analyze the failure in that mode since fewer circuits and no mechanics are involved.

Operation

Figure 80 illustrates the reader selected mode.

Control Circuits

Figure 81 is the second level diagram for initiation of the transfer scan and energization of the reader clutch.

Data Flow

Figure 82 shows the data flow for both reader and punch in selected or integrated mode.

Checking Circuits

Figure 83 shows the read check latch and its effect on reader-selected operation.

Card Reader Integrated Buffer Off-Line Mode

Functions

The read integrated buffer off-line mode allows the read buffer to be selected and scanned under control of the other CE panel switches. The read buffer circuits are exercised, but the card reader is not needed. All units associated with the integrated buffer are removed from CPU control.

This mode may be used to determine the cause of check stops which occur in reader selected off-line mode. The CE can "check search" read buffer and detect errors which occurred on read-in.

Reader buffer operation can be tested thoroughly by proper use of the buffer mode switch when in "integrated" mode.

NOTE: Before attempting to isolate a failure in reader integrated mode, the CE should also run a test in punch integrated mode. Considerable scoping time can be saved by this check, since many circuits are common to all units in the integrated buffer.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	Push button illuminated. Enables off-line mode switch.
Off-Line Mode	Integrated Buffer	Enables buffer select switch. Removes all units associated with the integrated buffer from CPU control.
Buffer Select	Reader	Controls read scan circuits.
Check Stop		No effect.
Op Control	Ctin Op	Permits continuous scanning. (Dependent upon the setting of the single cycle and check search switches.)
	Single Op	Stops the operation at the end of each scan.
Buffer Mode	Chk Sch	(Check search.) Each position of read buffer is read out and regenerated. The operation stops after a buffer cycle in which an error occurs, and the check search light comes on. The buffer register lights display the character in error. Depressing the start key resets the check search light and restarts the operation.
	Regen	Each position of read buffer is read out and regenerated. Errors do not cause a stop.
	Load	Each position of read buffer is read out but regeneration is blocked. The character read out is replaced by the character defined by the bit switches. NOTE: The bit structure of the character read out is not displayed in the buffer register lights because entry to the register is blocked to prevent regeneration.
Single Cycle	ON	The operation stops after each buffer cycle. Depressing the start key restarts the operation.
	OFF	The operation is under control of the op control and check search switches.
Bit Switches	ON	(Flipped to the right.) Control inhibit gating for insertion of one bits into buffer when the buffer mode switch is in the load position.
	OFF	(Flipped to the left.) No effect. Causes zero bits to be written into buffer in load mode.

Operation

Figure 84 shows the logic flow for reader integrated mode.

Control Circuits

Figure 85 shows the circuitry for the repeated transfer scans which occur in integrated mode.

Data Flow

Figure 82 shows the data flow for reader integrated mode in heavy lines.

Checking Circuits

Figure 83 shows the CE check latch and its function in a check search operation. Note that although the read check latch can be set in integrated mode, it has no effect on the operation.

Timing

Figure 86 shows the timings involved in repeated transfer scans. The first chart shows a complete transfer scan. The second chart shows initiation of the transfer scan and the first two buffer cycles.

Card Punch Integrated Buffer Off-Line Mode Function

The punch integrated buffer off-line mode allows the punch buffer to be selected and scanned under control of the other CE switches. The punch buffer circuits are exercised, but the punch is not needed. All units associated with the integrated buffer are removed from CPU control.

The punch buffer contents can be displayed and a transfer scan can be started to search for errors.

Regeneration can be blocked and new information can be entered into punch buffer from the bit switches.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	Push button illuminated. Enables off-line mode switch.
Off-Line Mode	Integrated Buffer	Enables buffer select switch. Removes all units associated with the integrated buffer from CPU control.
Buffer Select	Punch	Enables punch transfer scan circuits.
Check Stop		These switches have the same effect in punch integrated mode as they do in reader integrated mode. See the description under Card Reader Integrated Buffer Off-Line Mode, substituting punch buffer for read buffer.
Op Control		
Buffer Mode		
Single Cycle		
Bit Switches		

Operation

Figure 87 shows the logic flow for punch integrated off-line mode for all switch settings.

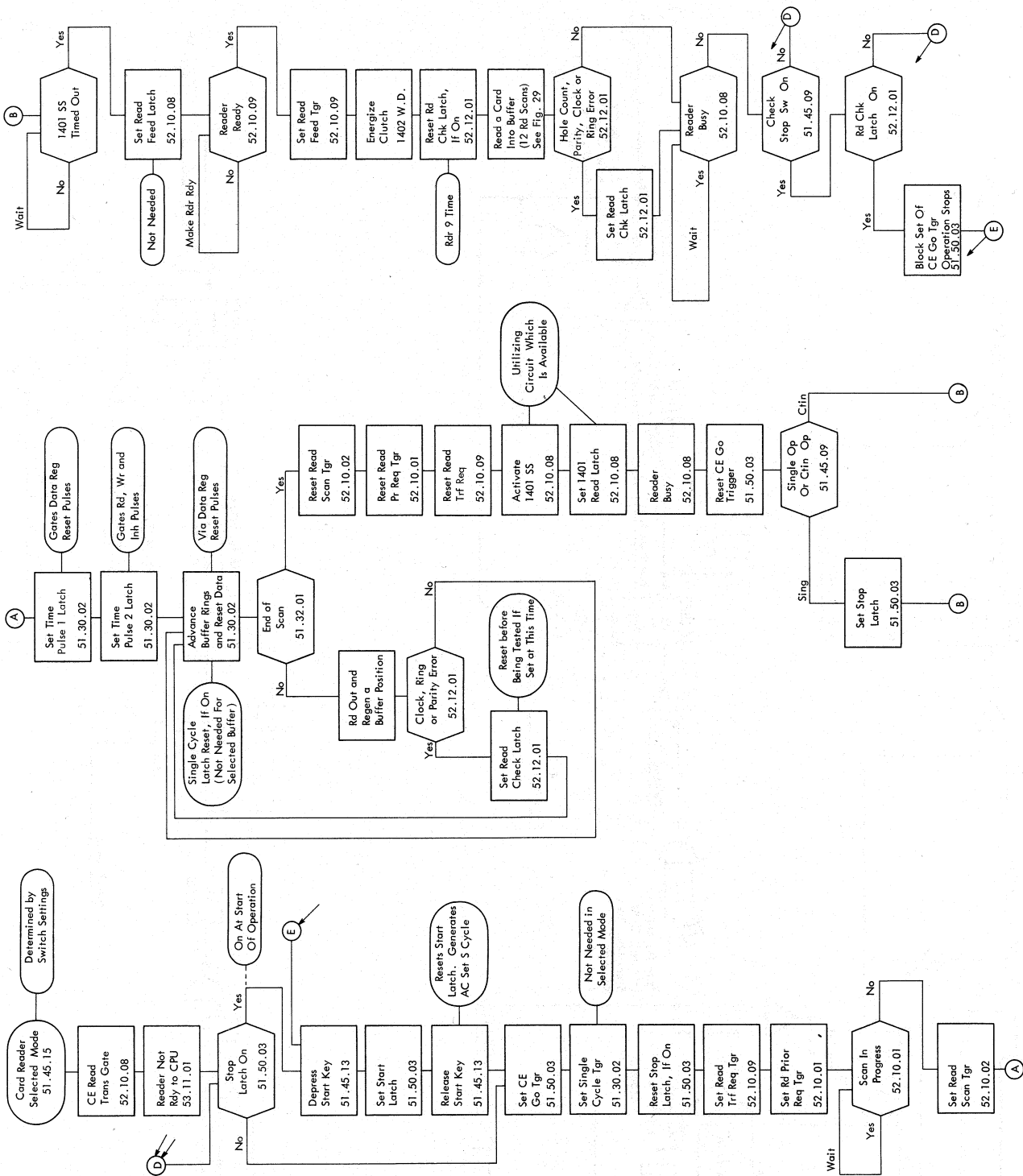


Figure 80. Card Reader Selected Off-Line Mode

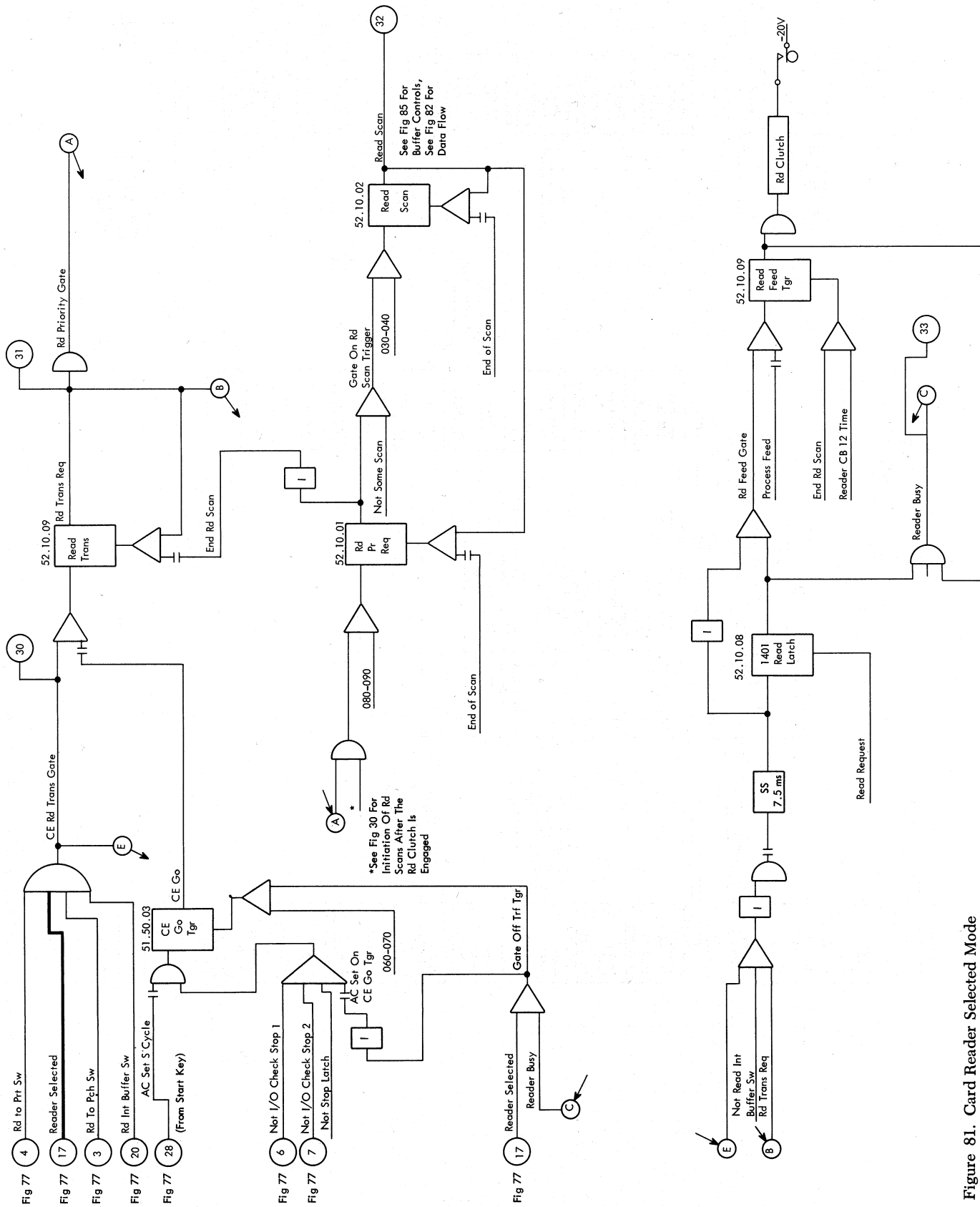


Figure 81. Card Reader Selected Mode

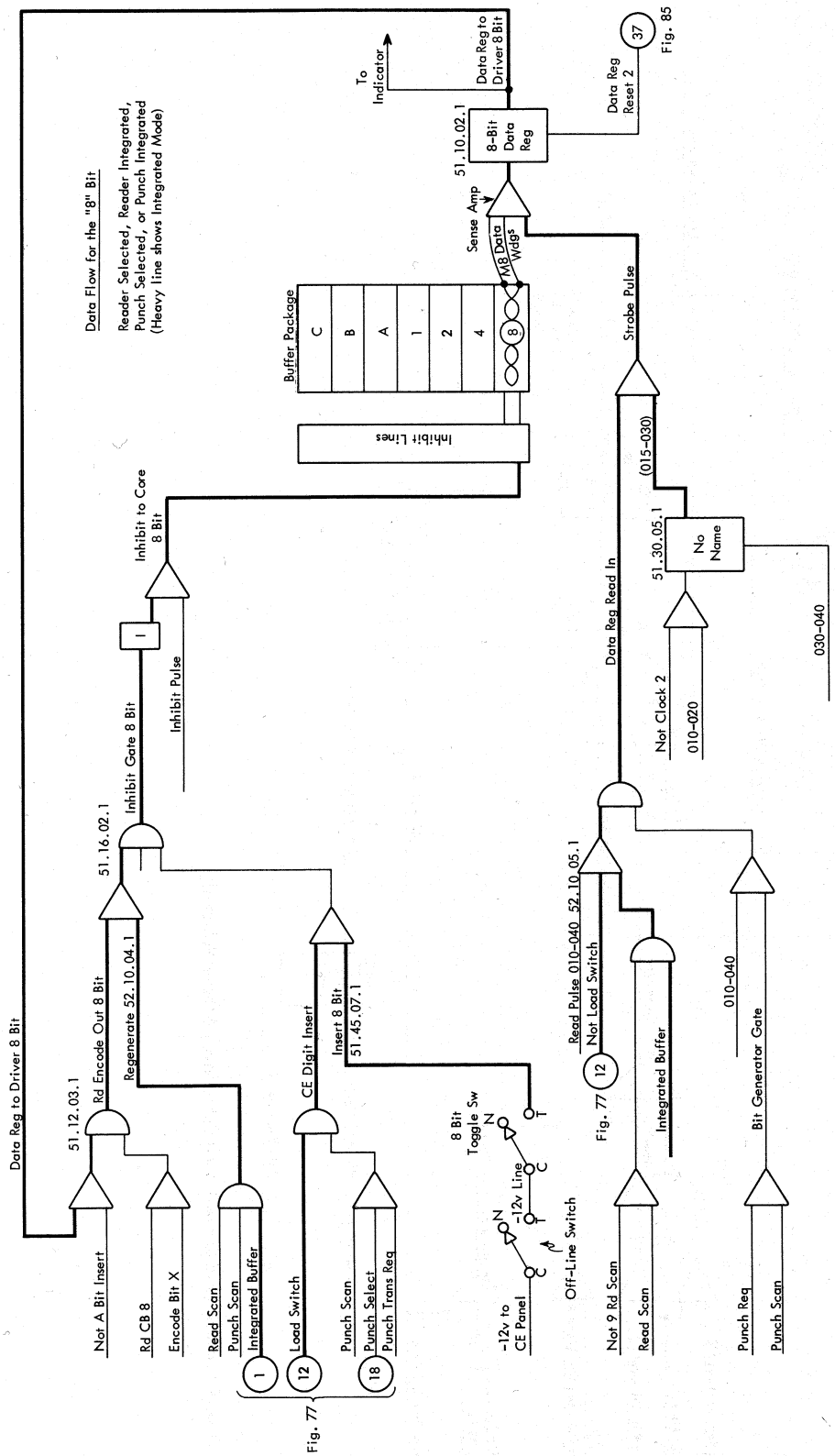


Figure 82. BCD Off-Line Data Flow — Reader or Punch

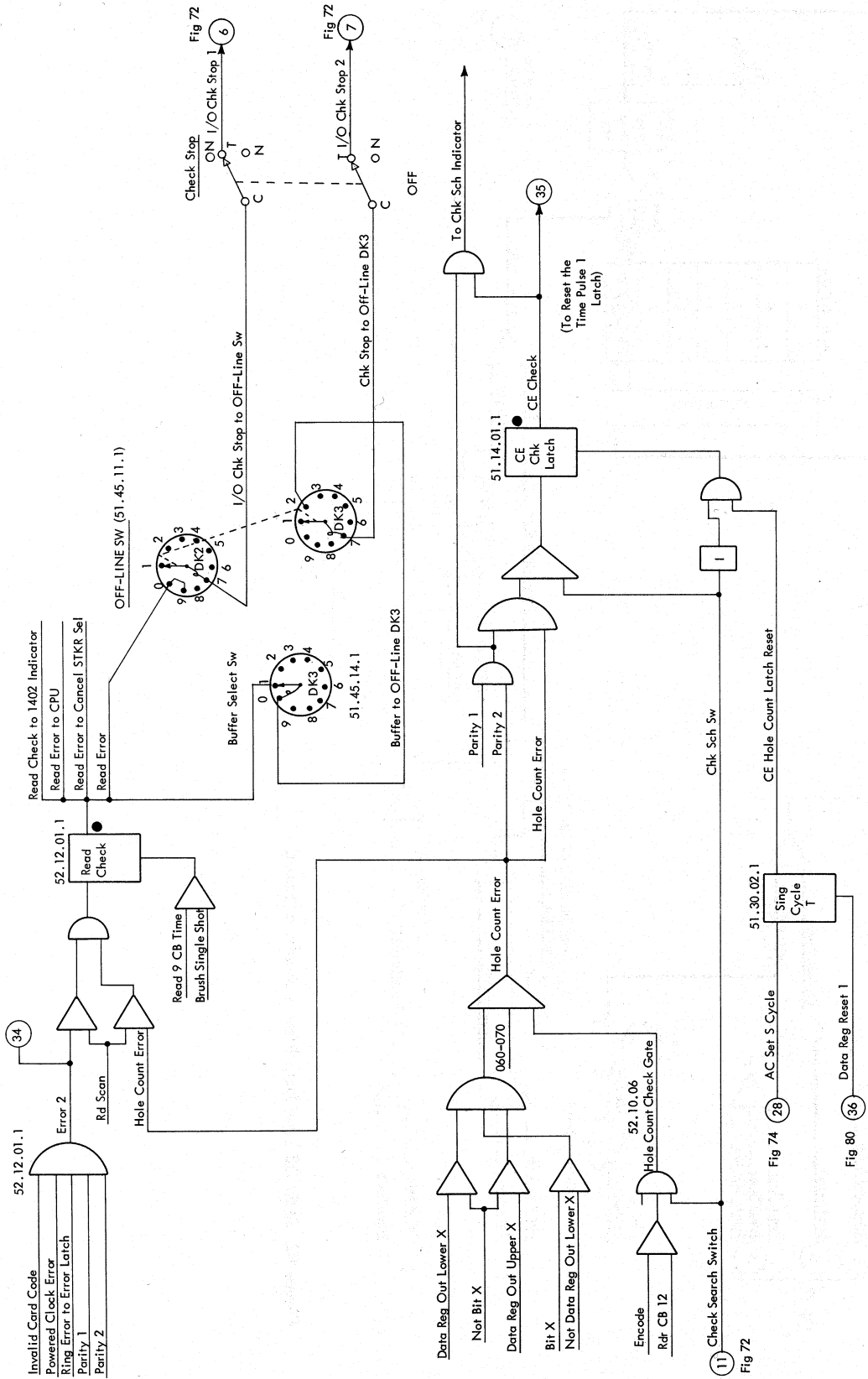


Figure 83. Checking (Reader or Punch Integrated, Reader Selected)

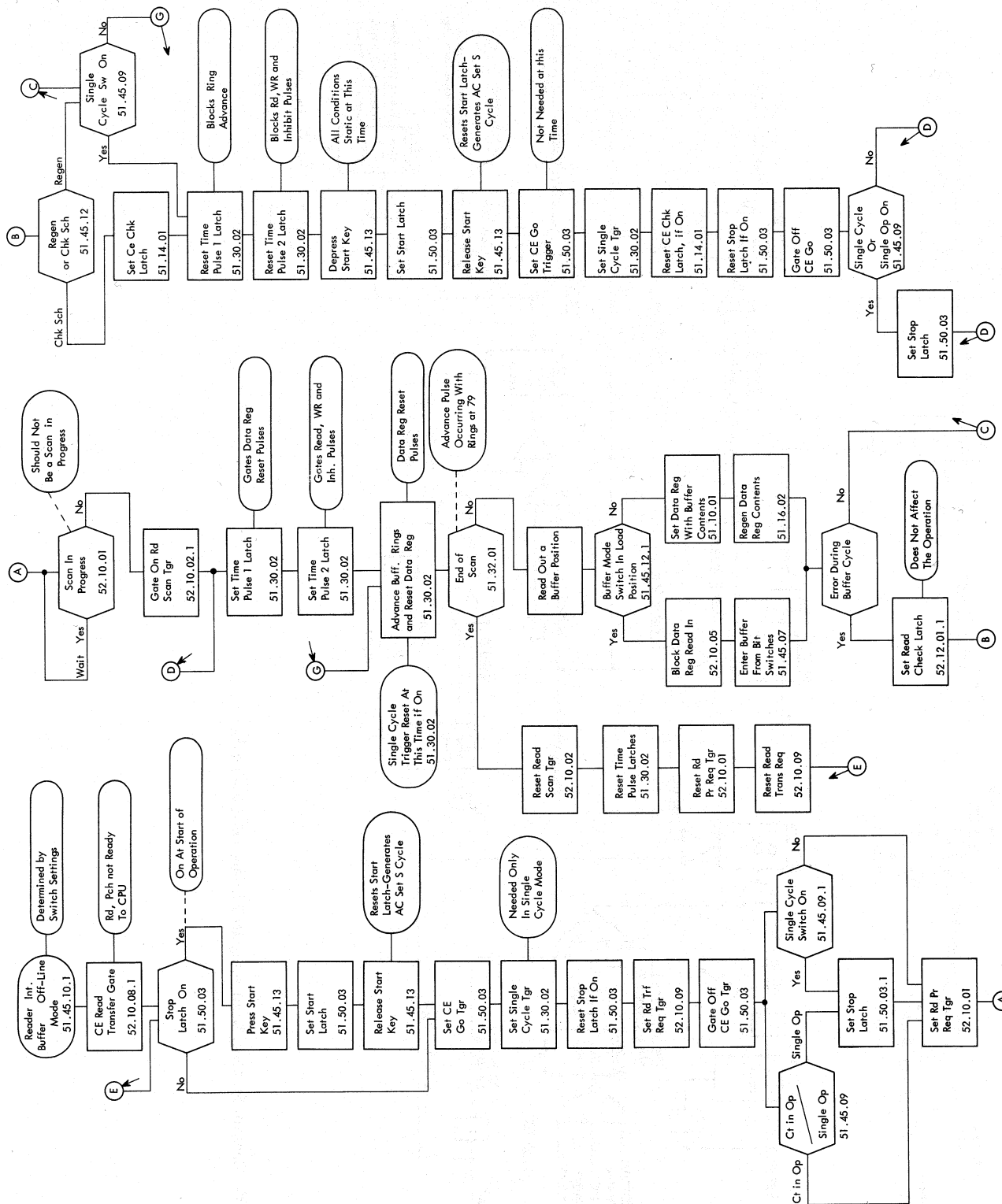


Figure 84. Card Reader Integrated Off-Line Mode

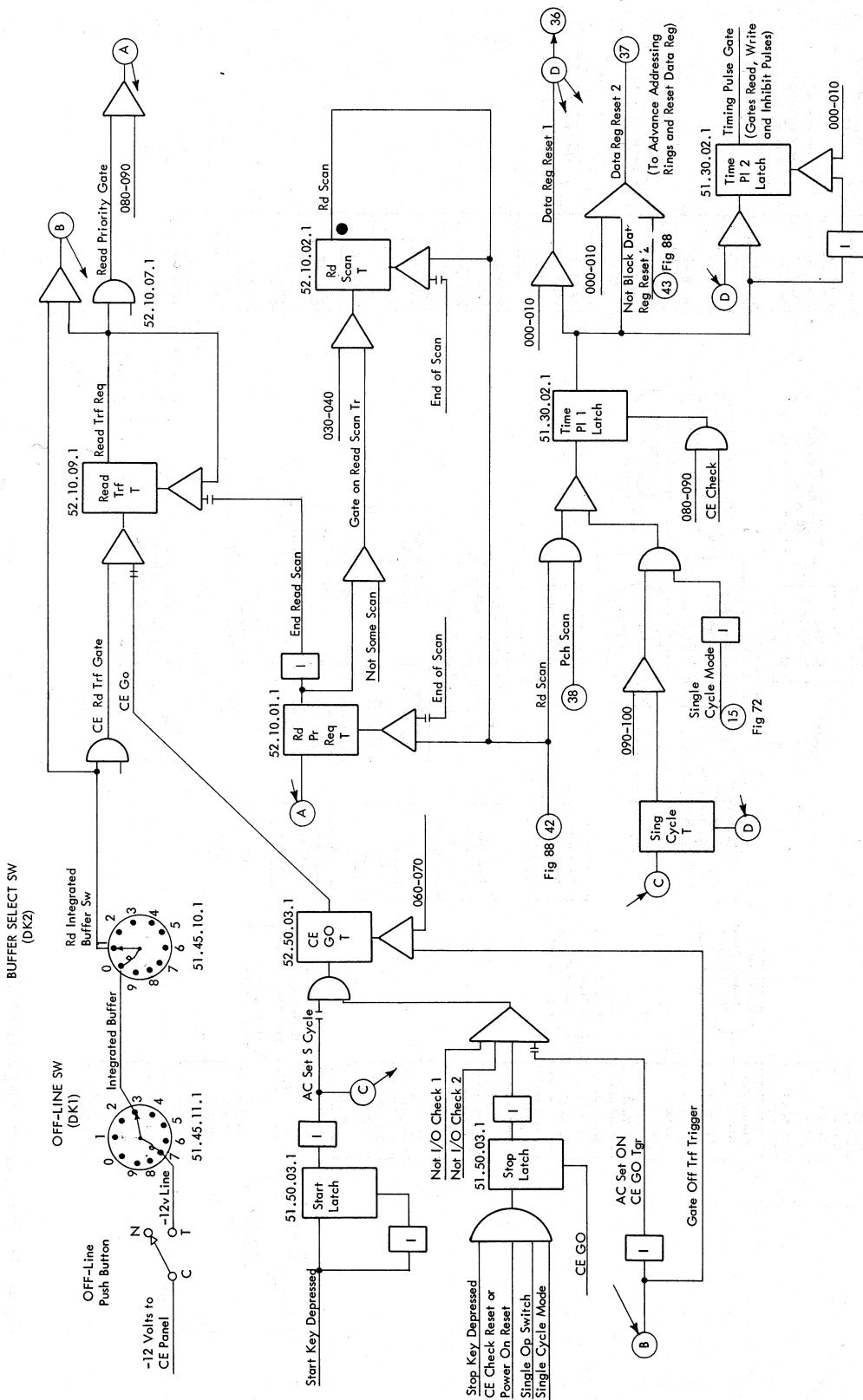
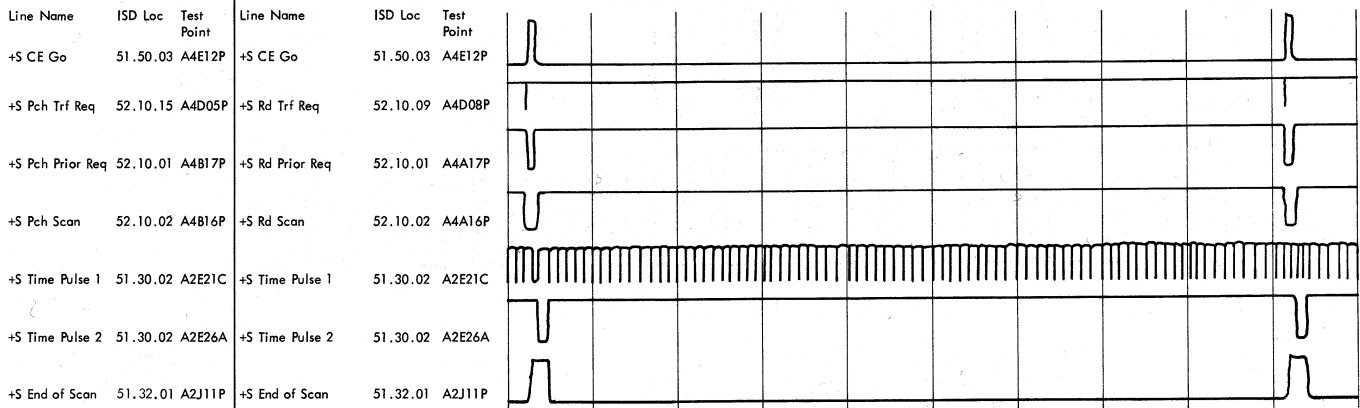


Figure 85. Controls for Card Read Integrated Buffer Off-Line Mode

Regen All Bits
Punch
Integrated Mode

Regen All Bits
Reader
Integrated Mode

Read or Punch Transfer Scan (Complete Scan)
Sync - +External on CE Go Sweep 0.1ms Per Division



First Two Buffer Cycles of a Read or Punch Transfer Scan
Sync +External on CE Go Sweep 5usec Per Division

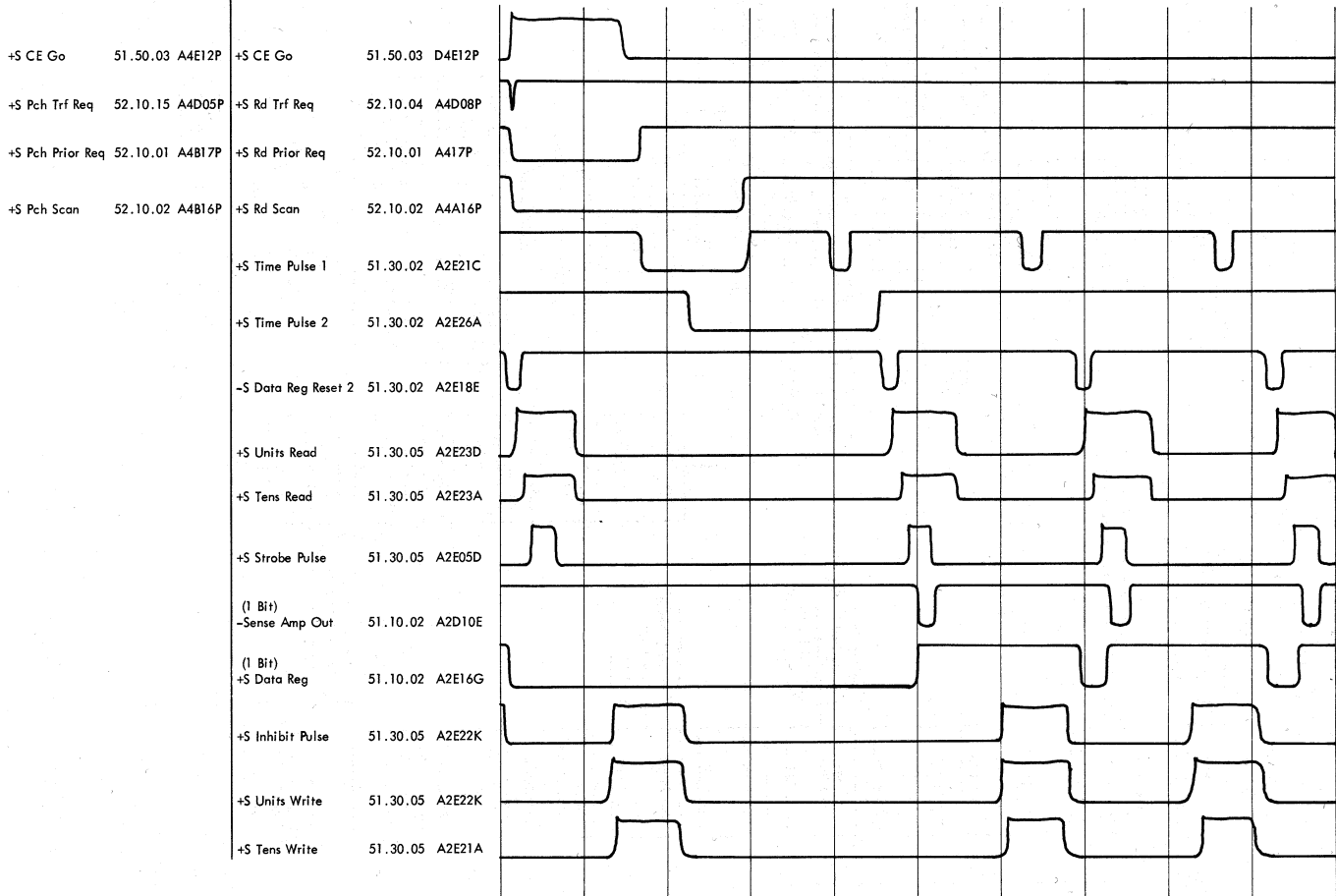


Figure 86. Waveforms

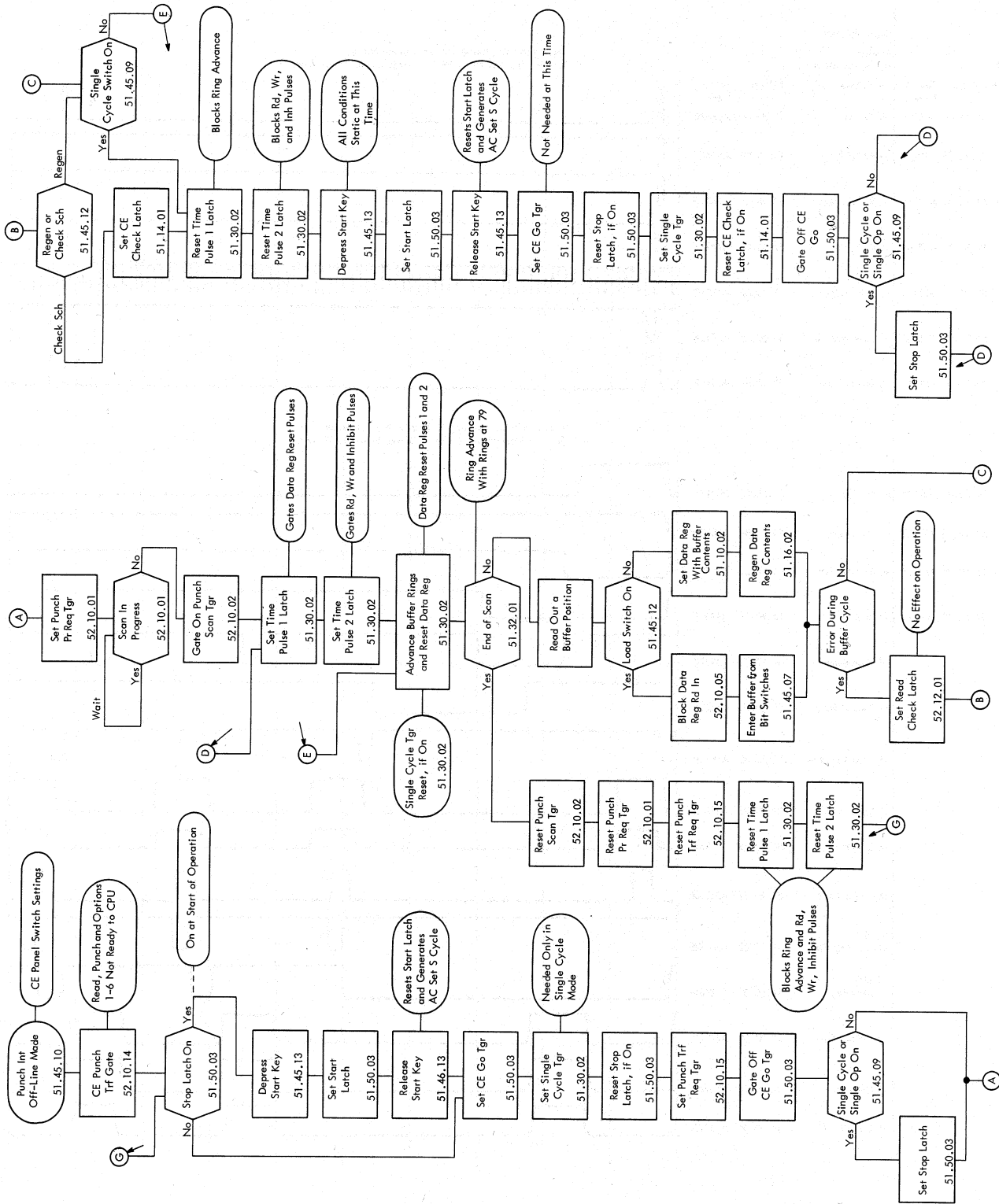


Figure 87. Card Punch Integrated Off-Line Mode

Control Circuits

The second level circuits for initiation of the punch transfer scan are shown in Figure 88.

Data Flow

Figure 82 illustrates the data flow for punch integrated off-line mode.

Checking Circuits

Figure 83 shows the CE check latch and its function in punch integrated buffer mode.

Timing Charts

Figure 86 shows the timing for a complete transfer scan in the first chart. The second chart shows only the first two buffer cycles of a transfer scan. In both cases, the scope picture was of continuous transfer scans.

Card Punch Selected Off-Line Mode

Function

This operation takes a punch transfer scan to fill punch buffer. All 80 positions contain the character defined by the bit switches at the end of the transfer scan. After the transfer scan, the record is punched into a card. Punch buffer is removed from CPU control without affecting the other integrated buffer units.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	Push button illuminated. Enables off-line mode switches.
Off-Line Mode	Selected Buffer	Enables buffer select switch.
Buffer Select	Punch	Removes only the punch from CPU control.
Check Stop	ON	Stops the operation when an error is detected. (Errors may occur during punching or read checking of a card. In either case, the error card will be the last card in the stacker.)
	OFF	Errors are ignored.
Op Control	Single Op	Stops the operation after each card.
	Ctin Op	Cases continuous operation until punch becomes not ready or a "check stop" occurs.
Buffer Mode	-	No effect. Characters are always loaded from bit switches during the transfer scan.
Single Cycle	-	No effect.
Bit Switches	-	Insert bits during transfer scan.

Operation

Figure 89 illustrates the logic flow for card punch selected mode. Because the other integrated buffer units are still under CPU control, a complete scan must be taken each time an operation starts in order to free the buffer rings for other operations. This means that single cycle and check search operations cannot be performed in this mode.

Cards must be run into the punch to put the punch in ready status.

NOTE: The punch ready light does not come on in off-line mode although cards may be positioned properly.

The start key is depressed to start the operation. Once started the operation continues under control of the op control and check stop switches.

Control Circuits

Figure 90 shows the second level circuits for starting the transfer scan and energizing the punch clutch.

Data Flow

Figure 82 shows the data flow for punch selected mode. The same figure also shows data flow in integrated modes and reader selected mode.

Checking Circuits

Figure 91 shows the second level circuits for punch checking. There are 2 punch check latches. This is necessary to detect errors at both the punch and the punch check stations and insure that the error card is always the last card in the stacker when a check stop occurs. Note that although the punch transfer check latch is affected, it does not effect off-line operation. This latch is used only to signal CPU when the punch is operating on-line.

Reader To Punch Off-Line Mode

Function

The reader to punch off-line mode duplicates each card that feeds through the read feed. The 1402 reads each card and places it in read buffer. From the read buffer, the card transfers to the punch buffer. After the transfer is complete, the 1402 punches a new card with the information just transferred to punch buffer.

Both reader and punch are removed from CPU control.

Errors cause a stop with the check stop switch on. The read check and punch check lights on the 1402 aid in determining the cause of the stop.

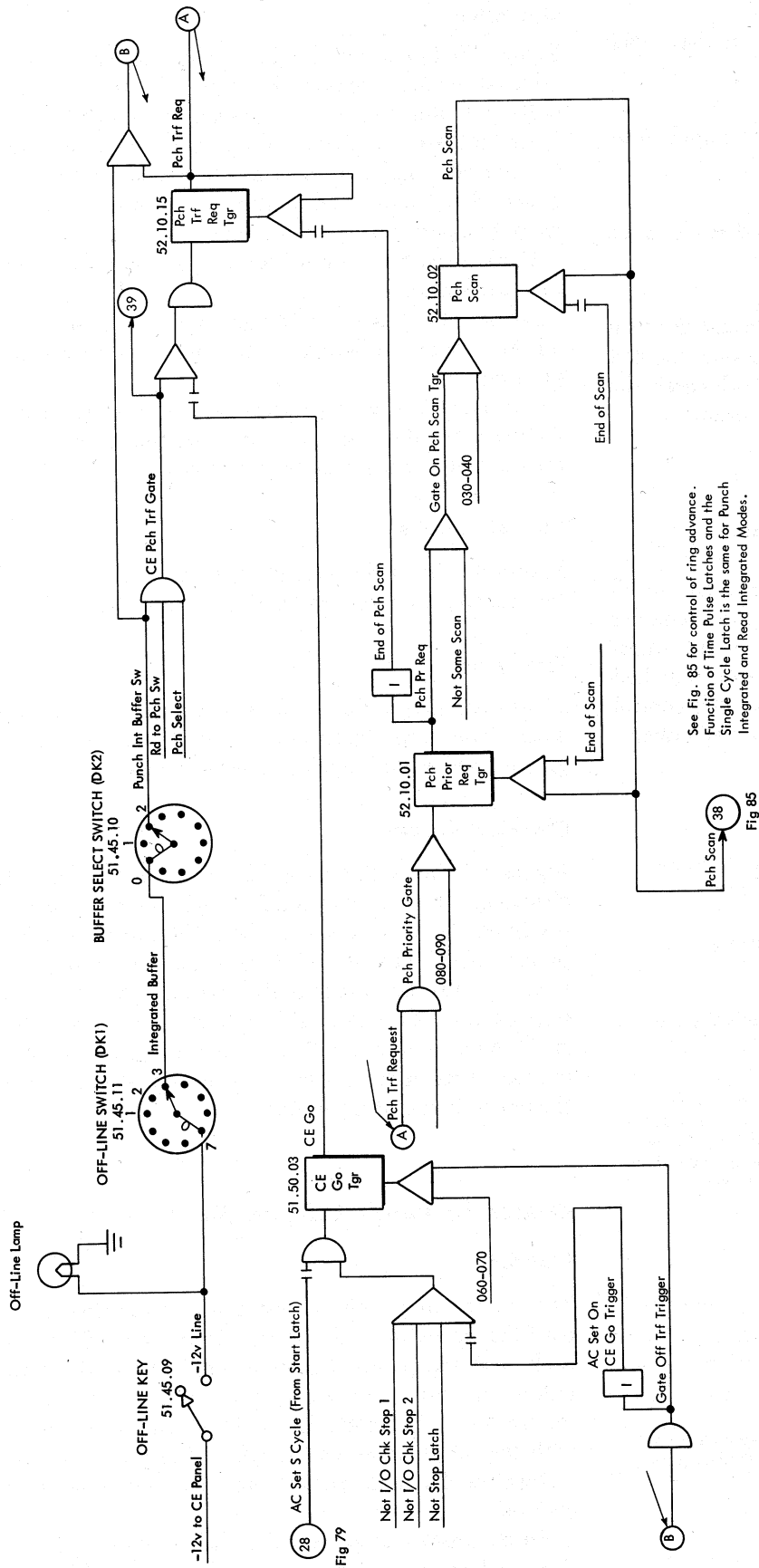


Figure 88. Card Punch Integrated Off-Line Mode Controls

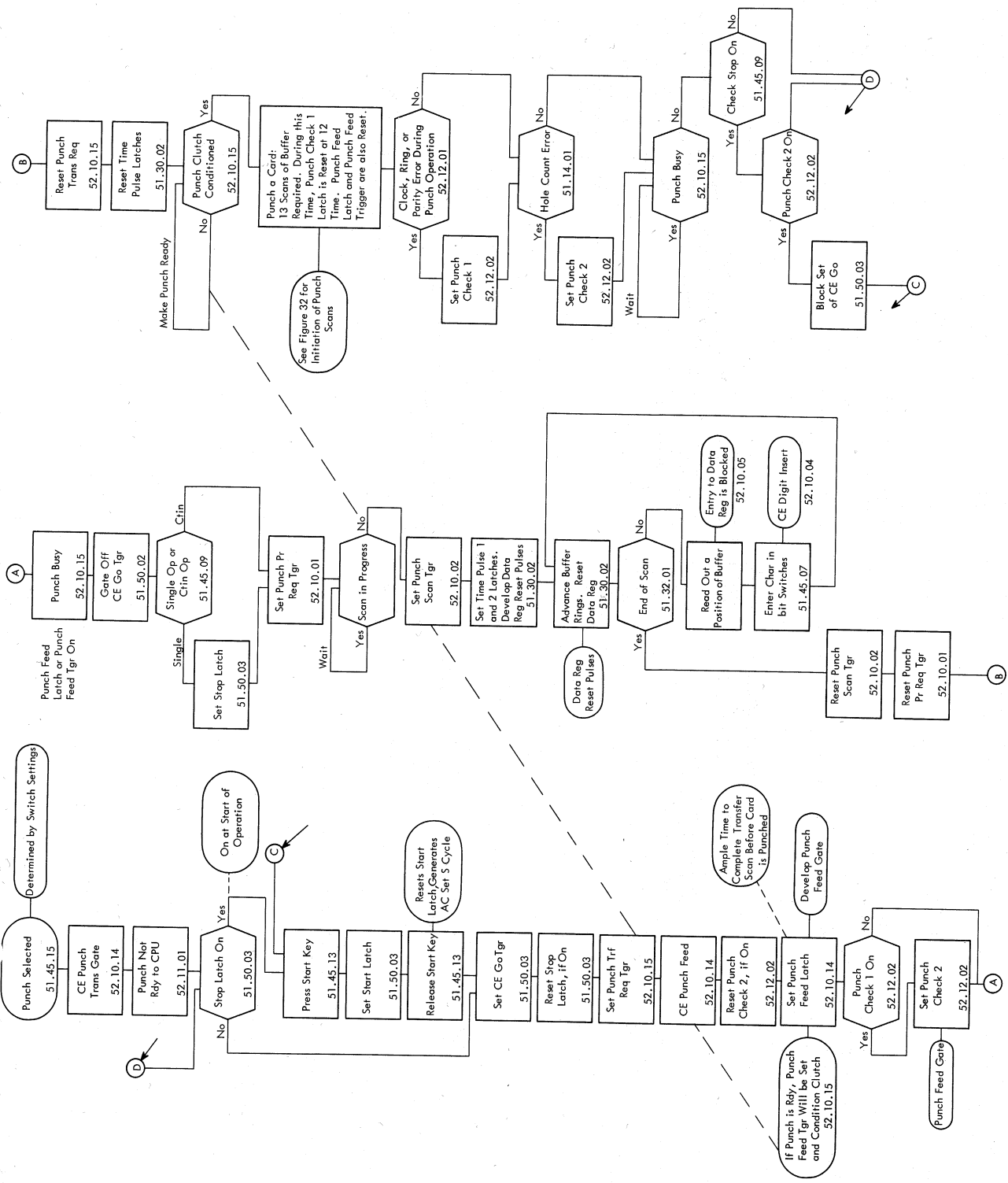


Figure 89. Card Punch Selected Off-Line Mode

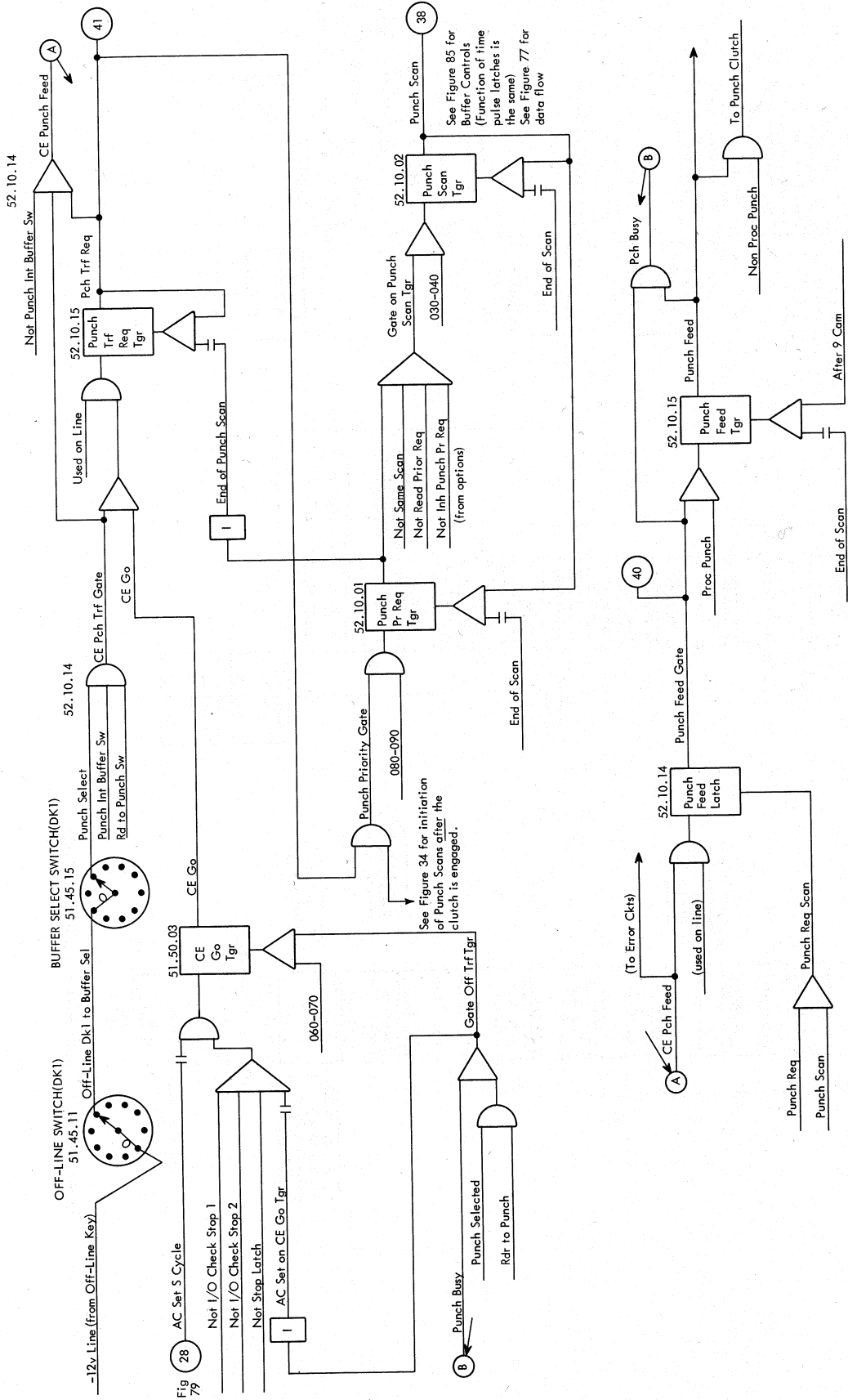
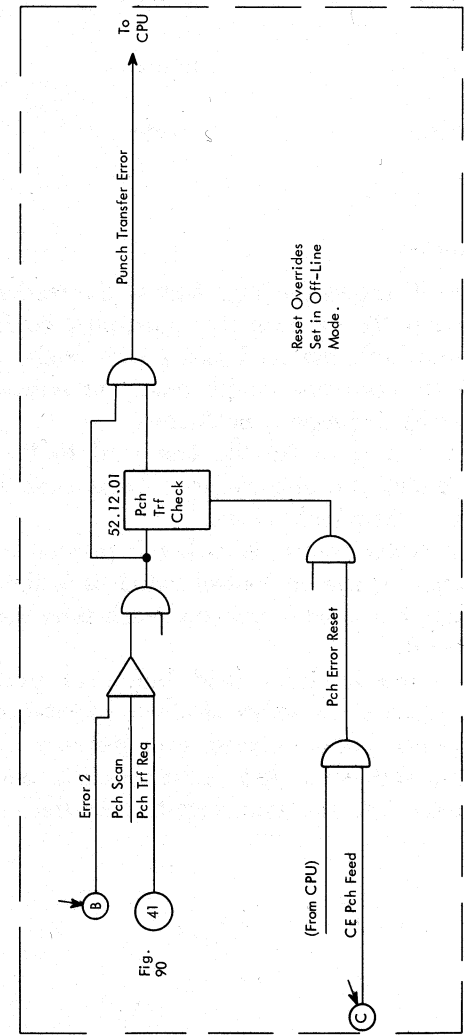
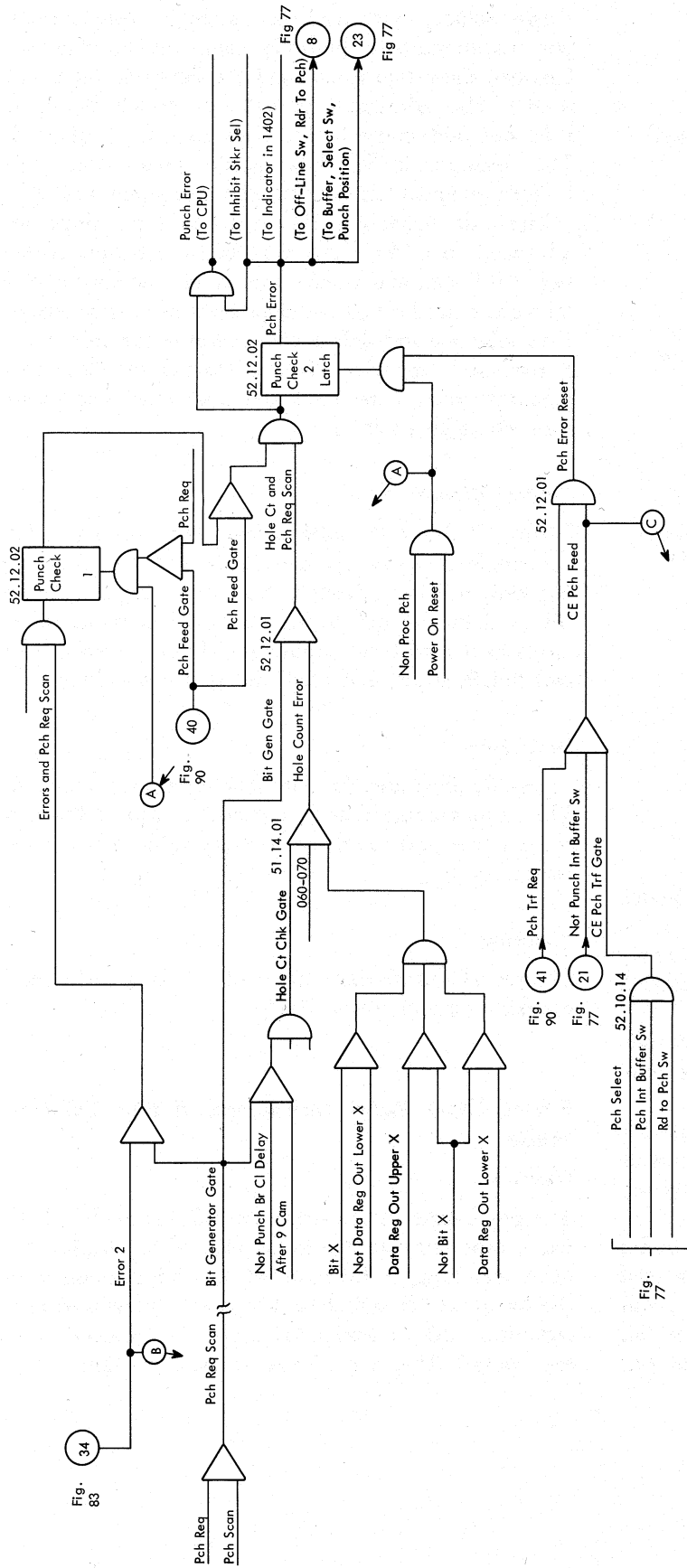


Figure 90. Card Punch Selected Buffer Off-Line Mode Controls



Punch Check 1 - Reset just prior to "12" punch scan.
Set during any punch scan in which an error occurs.

Punch Check 2 - Reset just prior to the punch transfer scan.
Set at the end of transfer scan if Pch Check 1 is on.
Set during last pch scan if a hole count error occurs.

Figure 91. Checking Circuits Punch Select Mode

Switch Settings

Switch	Setting	Notes
Off-Line	ON	Push button illuminated. Enables off-line mode switch.
Off-Line Mode	Rd-Pch	Removes the reader and punch from CPU control.
Buffer Select		No effect.
Check Stop	ON	Stops the operation after the card in which an error occurs.
	OFF	Errors are ignored.
Op Control	Single Op	Stops the operation after each card is read and duplicated.
	Ctin Op	The operation continues until either machine becomes not ready or a "check stop" occurs.
Buffer Mode	-	No effect.
Single Cycle	-	No effect.
Bit Switches	-	No effect.

Operation

Figure 92 shows the logic flow of the reader to punch operation. To perform this operation, cards must be run into both the read and punch feeds. The ready lights do not come on for reader or punch although cards may be properly positioned.

This run-in causes the first card to be read into read buffer and also causes a blank card to be positioned at the punch station.

The buffer control start key is pressed to start the operation. If the op control switch is in the SINGLE OP position, one card is punched each time the start key is pressed.

The transfer from read buffer to punch buffer takes place via a series of *single memory cycle* read and punch scans. A read scan memory cycle reads out the addressed read buffer position, and sets this character into the data register. At the end of this

single memory cycle read scan, a single memory cycle punch scan starts. (The buffer rings are not advanced between these two cycles and the data register is not reset.) The addressed position of punch buffer is read out and entry to the data register is blocked. The character in the data register (read from read buffer previously) is then entered into punch buffer.

The data register is then reset and the rings are advanced to address the next buffer position. Alternate read scan and punch scan single memory cycles take place until all 80 positions have been transferred. Ring advance and data register reset occur only when a read scan memory cycle is started to allow two memory cycles (one read and one punch) to occur for each buffer position.

Control Circuits

Figure 93 shows the second level control circuits for the single memory cycle controls and the alternate blocking of ring advance. Note the purpose of the "block data register" latch. Figure 93 contains references to second level circuits for clutch controls, read and punch scans, and read and punch checking.

Data Flow

Figure 82 illustrates the data flow for reader to punch. The CE must remember that alternate read and punch scans occur and only one memory cycle takes place for each scan.

Checking

Figures 83 and 91 show the read checking and punch checking circuits, respectively.

Paper Tape Read Integrated Buffer Off-Line Mode

Function

The paper-tape integrated-buffer off-line mode allows paper-tape (PT) storage to be scanned for display, for error searching, or for entering new information from the CE panel bit switches. The entire integrated synchronizer and all associated units are removed from CPU control. The PT reader is not set in motion.

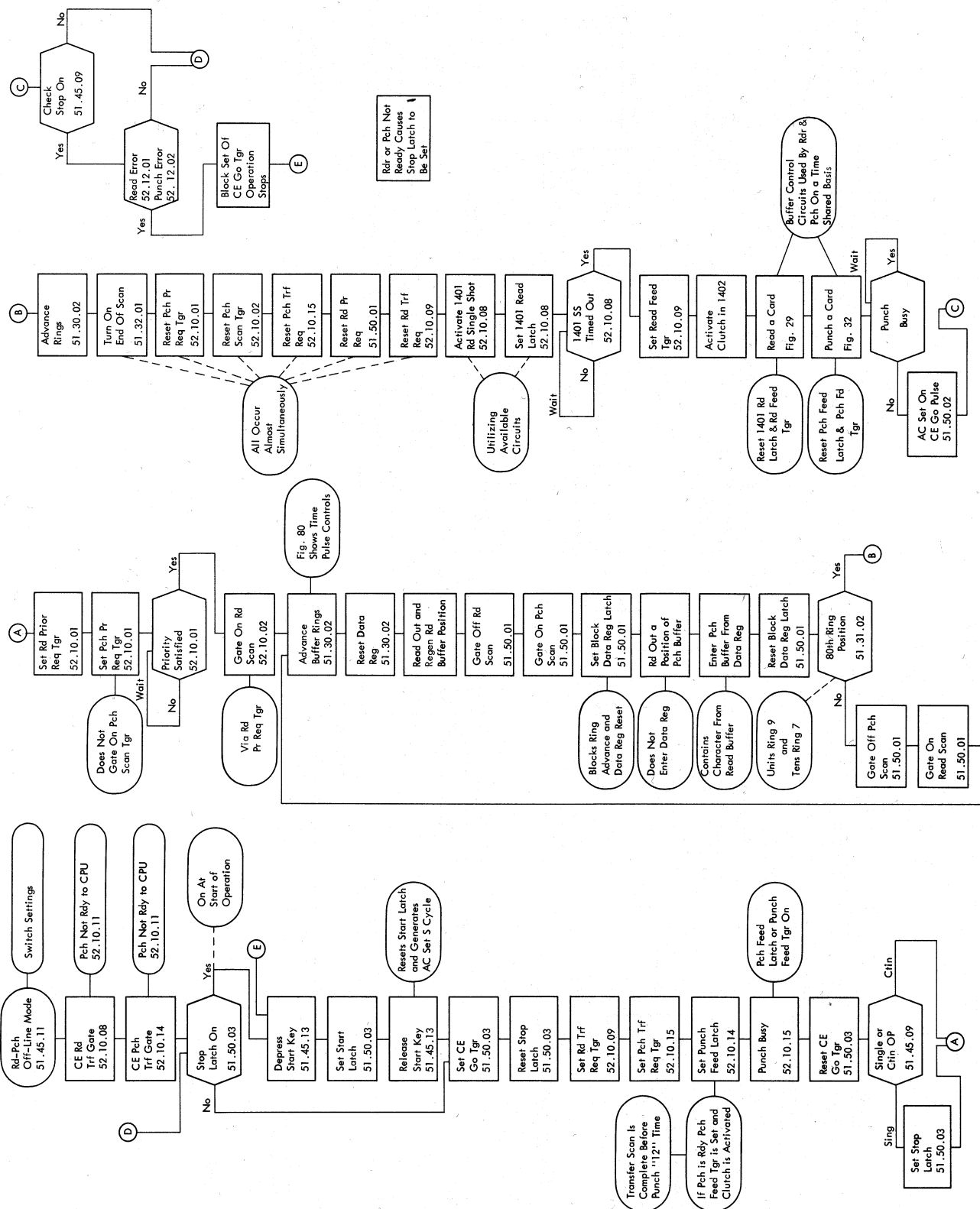


Figure 92. Reader to Punch Off-Line Mode

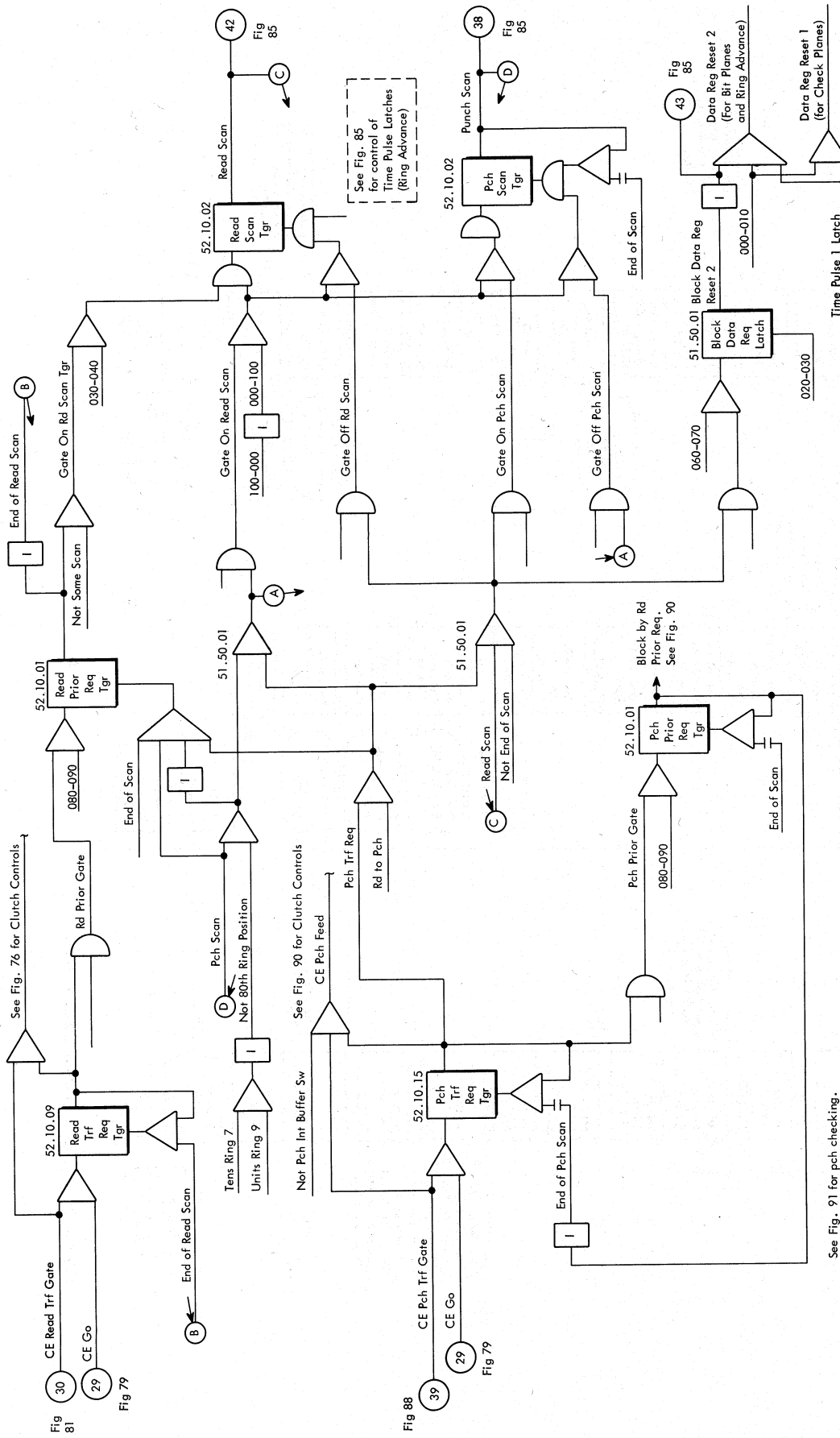


Figure 93. Reader to Punch

See Fig. 91 for pch checking.
 See Fig. 88 for rd checking.
 See Fig. 34 for pch scans after clutch is engaged.
 See Fig. 30 for rd scans after clutch is engaged.

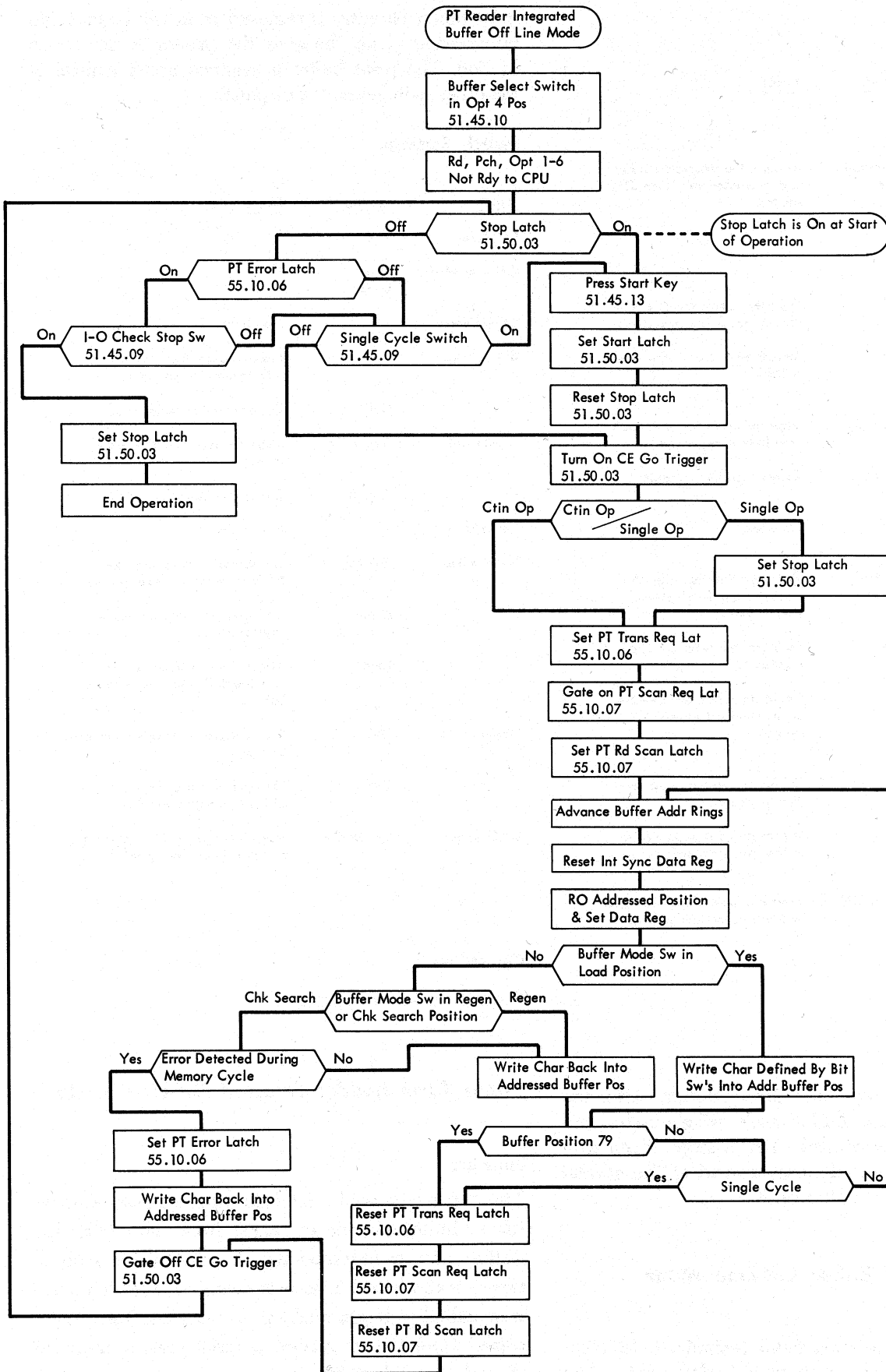


Figure 94. Paper Tape Read Integrated Buffer Off-Line Mode

Switch Settings

Switch	Setting	Notes
Off-Line	ON	
Off-Line Mode	Integrated Buffer	Removes the integrated buffer and associated units from CPU control.
Buffer Select	Opt 4	
Check Stop	ON	Stops the operation after the scan in which the error occurs.
	OFF	Ignores errors (see buffer-mode switch).
Op Control	Single Op	Stops the operation after each scan (80 memory cycles).
	Ctin Op	Causes repetitive scanning.
Carriage		No effect.
Buffer Mode	Chk Sch	The operation stops after the memory cycle in which the error occurs.
	Regen	Each position reads out and is regenerated.
	Load	Places the characters that the bit switches define into PT storage.
Single Cycle	ON	The operation stops after each memory cycle.
	OFF	The operation is under control of the op-control switch.
Bit Switches	OFF or ON	Insert bits when the buffer-mode switch is in the load position.

Operation

Pressing the start key starts the operation. After the operation starts, the buffer-mode, single-cycle, and Op-control switches control when it stops. Each scan is a full 80-memory-cycle scan instead of the normal serial scan that can vary in length.

Print Integrated Buffer Off-Line Mode

Function

The print integrated-buffer mode is similar in function and operation to the integrated-buffer mode. The

print buffer circuitry is removed from CPU control. No information prints, because the printer is not set in motion. The print buffer is scanned under control of the other switches on the CE panel.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	-
Off-Line Mode	Print Buffer	-
Buffer Select		No effect.
Check Stop	ON	Stops the operation after the scan in which error occurs.
	OFF	Causes errors to be ignored.
Op Control	Single Op	Stops the operation after each scan.
	Ctin Op	Causes continuous scanning
Carriage	-	No effect.
Buffer Mode	Chk Sch	The operation stops after the cycle in which the error occurs.
	Regen	Each position reads out and is regenerated.
	Load	Allows the characters that the bit switches define to enter into the buffer.
Single Cycle	ON	The operation stops after each memory cycle.
	OFF	The operation is under the control of the op-control switch.
Bit Switches	OFF or ON	Insert bits when the buffer-mode switch is in the load position.

Operation

See Figure 95 for operation.

Paper Tape Reader Selected Off-Line Mode

Function

The paper-tape-reader-selected off-line mode removes the PT buffer and the PT reader from CPU control for testing and troubleshooting. A PT transfer scan is taken, and when this scan is complete, the PT reader is signalled to begin reading. As each character is received from the PT reader, a serial scan is taken to store the incoming character.

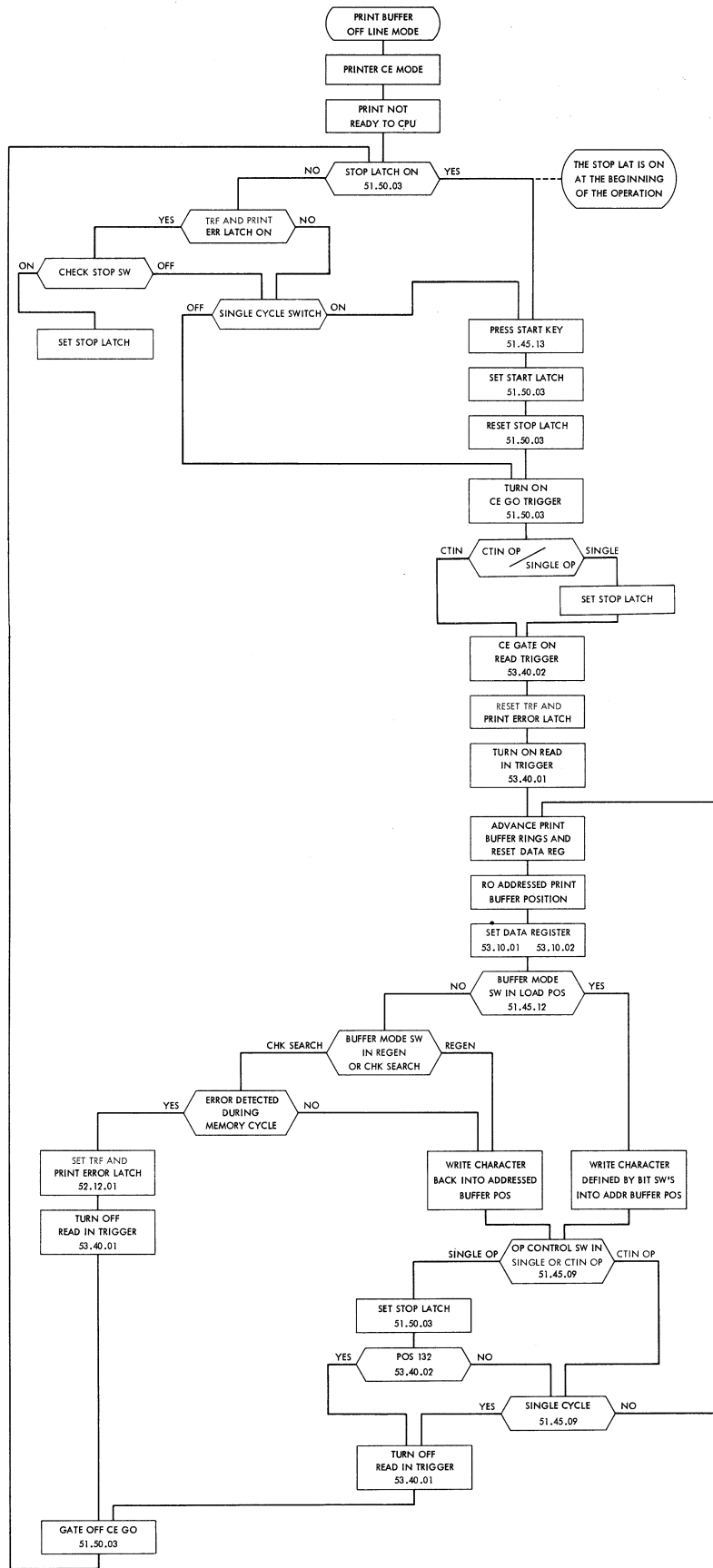


Figure 95. Print Integrated Buffer Off-Line Mode

Switch Settings

Switch	Setting	Notes
Off-Line	ON	-
Off-Line Mode	Selected Buffer	-
Buffer Select	Opt 4	Opt 4 (PT reader) removes from CPU control.
Check Stop	ON	Stops the operation after the PT record in error.
	OFF	Causes errors to be ignored.
Op Control	Single Op	Stops the operation after each PT Record.
	Ctin Op	Causes continuous operation until the PT reader becomes not-ready.
Carriage	-	No effect.
Buffer Mode	-	No effect. Data are regenerated during transfer scan.
Single Cycle	-	No effect.
Bit Switches	-	No effect.

Operation

The start key starts this operation. (See Figure 96.) Once the operation starts it continues under control of the Op control and check stop switches.

Printer Selected Off-Line Mode

Function

This operation causes a print-transfer scan. During the transfer scan, the character defined by the bit switches is loaded into all print storage positions. The record is

then printed. Either single lines or continuous printing can be started, depending on the setting of the Op-control and check-stop switches. Print storage is the only unit removed from CPU control.

Switch Settings

Switch	Setting	Notes
Off-Line	ON	-
Off-Line Mode	Selected Buffer	-
Buffer Select	Printer	Removes only the printer from CPU control.
Check Stop	ON	Stops the operation after the print line in which an error occurs.
	OFF	Causes errors to be ignored.
Op Control	Single Op	Stops the operation after each print line.
	Ctin Op	Causes continuous operation until the printer becomes not-ready.
Carriage	Single Space	The automatic-carriage single-spaces after each print line.
	Double Space	The automatic carriage double-spaces after each print line.
Buffer Mode	-	No effect. Characters are always loaded from bit switches during the transfer scan.
Single Cycle	-	No effect.
Bit Switches	OFF or ON	Insert bits during the transfer scan.

Operation

Figure 97 shows printer selected off-line mode operation.

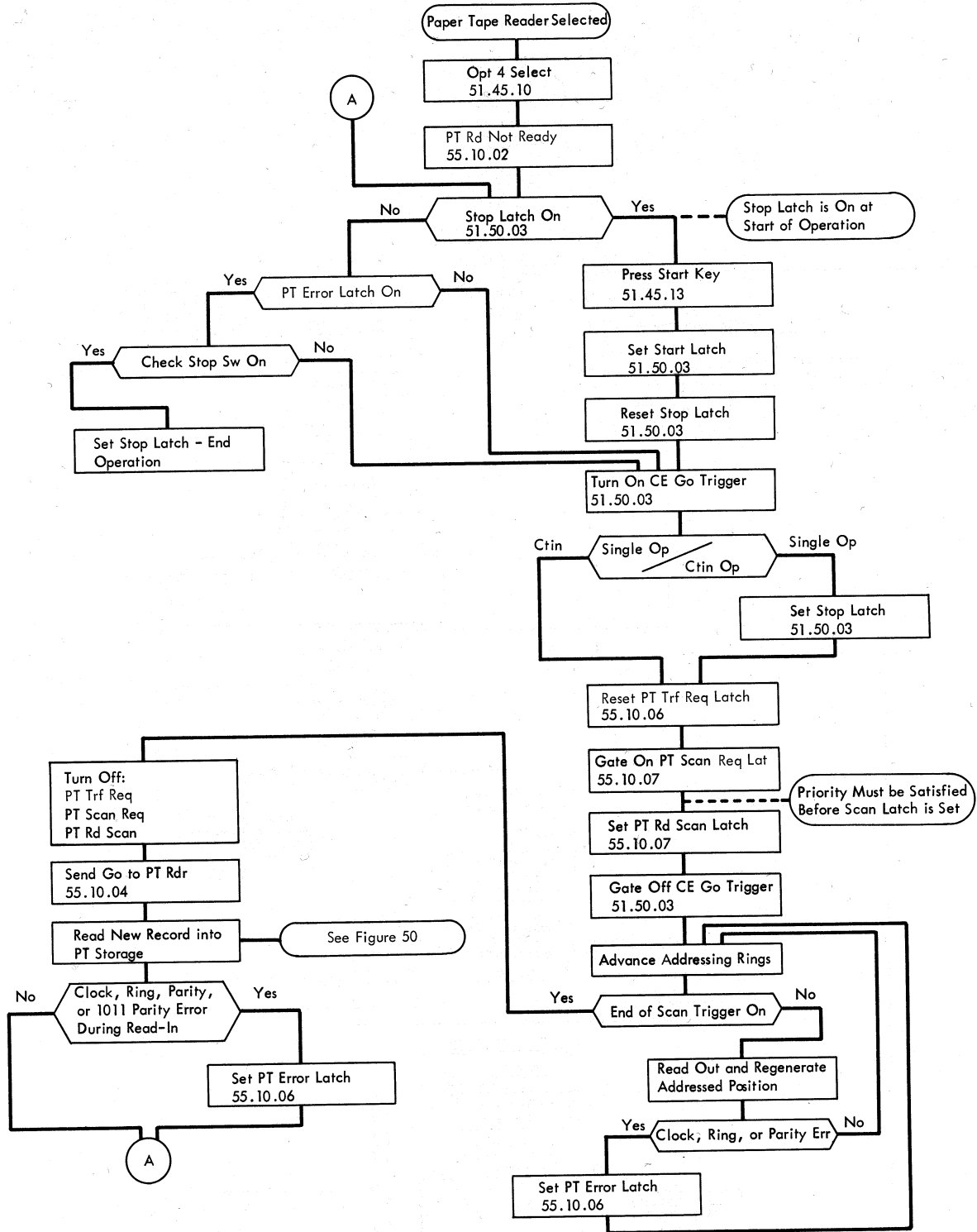


Figure 96. Paper Tape Reader Selected Off-Line Mode

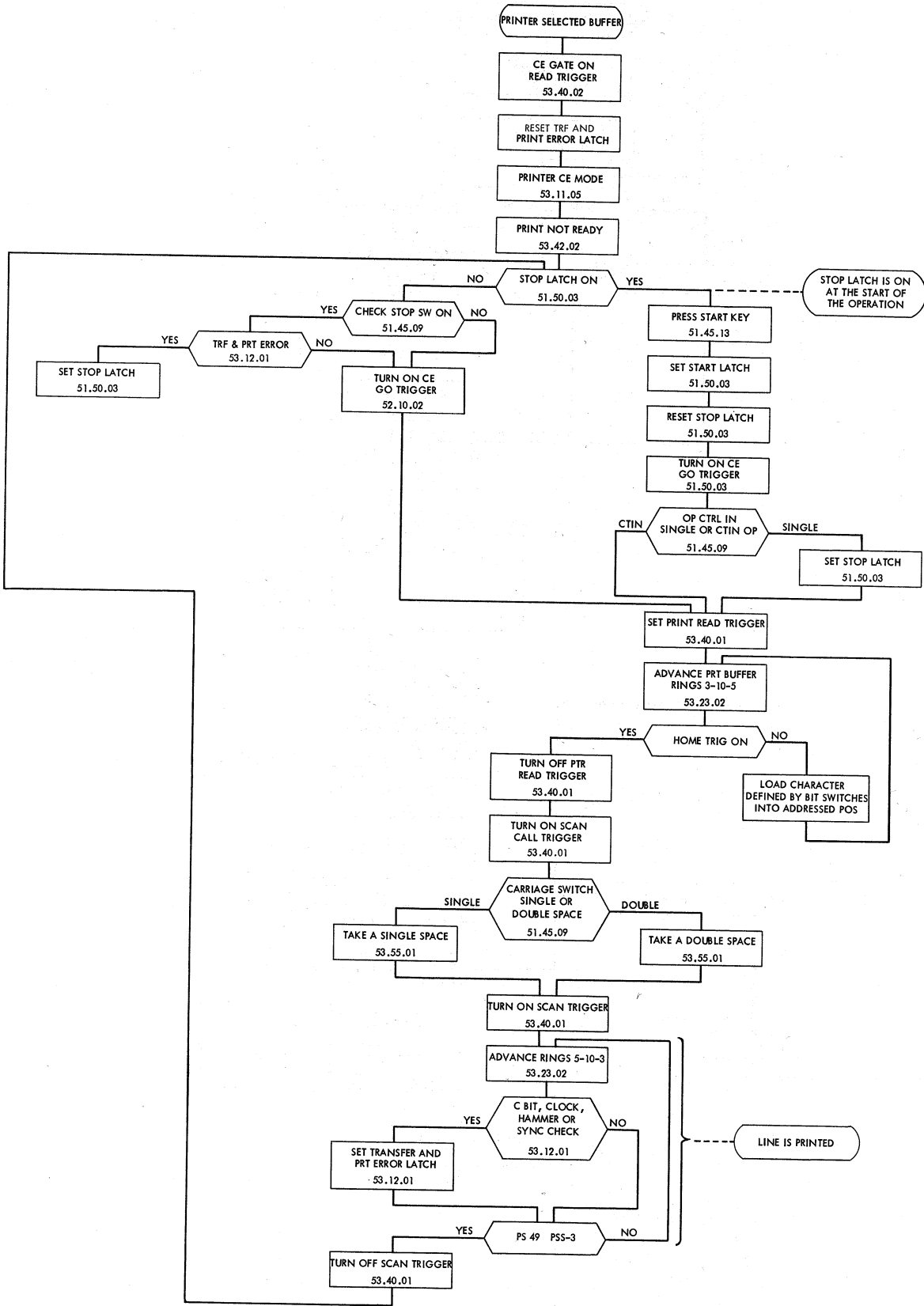


Figure 97. Printer Selected Off-Line Mode

Read and Punch Column Binary Feature

The read and punch column binary feature is available for the IBM 1414 Model 4 Input-Output Synchronizer and its attached IBM 1402 Model 2 Card Reach Punch. This feature permits column binary cards or standard IBM coded cards to be intermixed in both read and punch operations.

On a read operation a column binary card is identified by a 7 and 9 punch in column 1. On a punch operation the program instruction identifies a column binary card by an additional select line that controls the 1414 punch circuits.

Each of the possible 960 holes in a card is used to represent a binary bit of information. Each column of the card is divided into two 6-bit BCD characters. Rows 12 through 3 of column 1 contain the first 6-bit BCD character and the 4 through 9 rows the second character. Consequently, each column can store two characters instead of the usual one, resulting in a single card storing 160 characters of information (Figure 98).

Because the column binary card can contain 160 characters, the 80-position read and punch buffers in the 1414 must have expanded capacities. The additional positions needed are obtained by using two of the six optional buffers available in the 1414 Model 4.

Any two of the six optional buffers can be used for column binary, but once the feature is installed, the assignment is fixed. One optional buffer is assigned to the reader and one to the punch and with the column binary feature installed the assigned optional buffers are limited in their use to column binary.

Column Binary Read

To allow the 1402 to process both normal IBM code and column binary cards, several major additions to the normal read procedure are necessary:

1. A method of detecting the identifying 9-7 punches in column one of the column binary cards.
2. Since two punching codes are to be used, provision must be made for bypassing the read encode circuits.
3. Additional storage for the second 80 characters.
4. The transfer scan to CPU must be doubled in length to move the 160 characters of a column binary card.
5. A column binary identification signal must be sent to CPU that can be program interrogated.
6. The reader validity check circuit must be disabled when reading a column binary card.

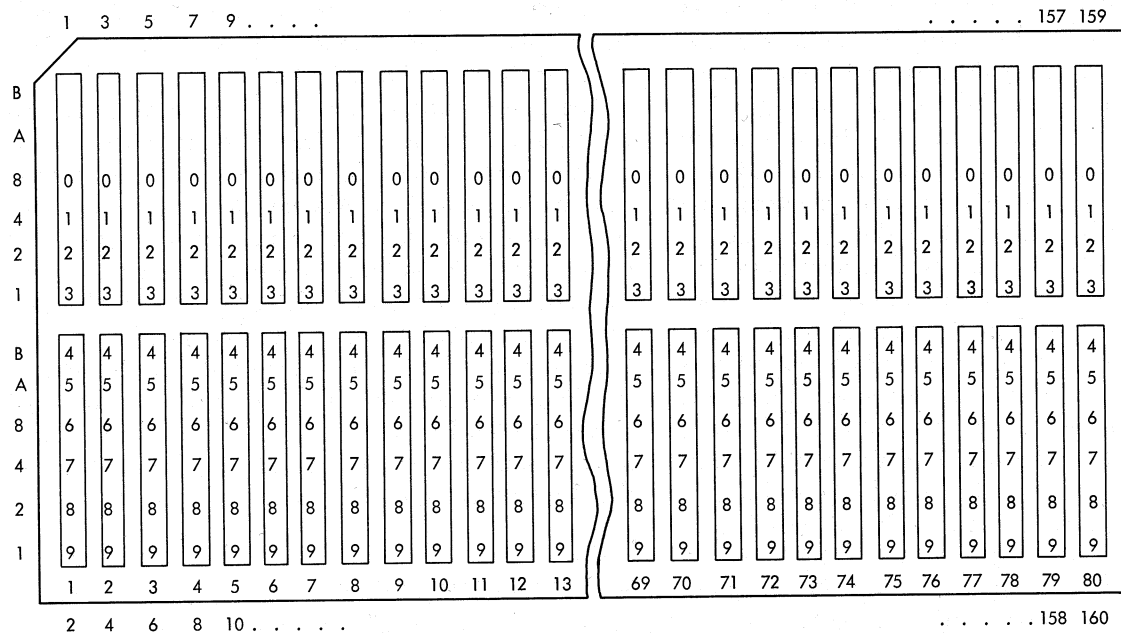


Figure 98. Column Binary Card

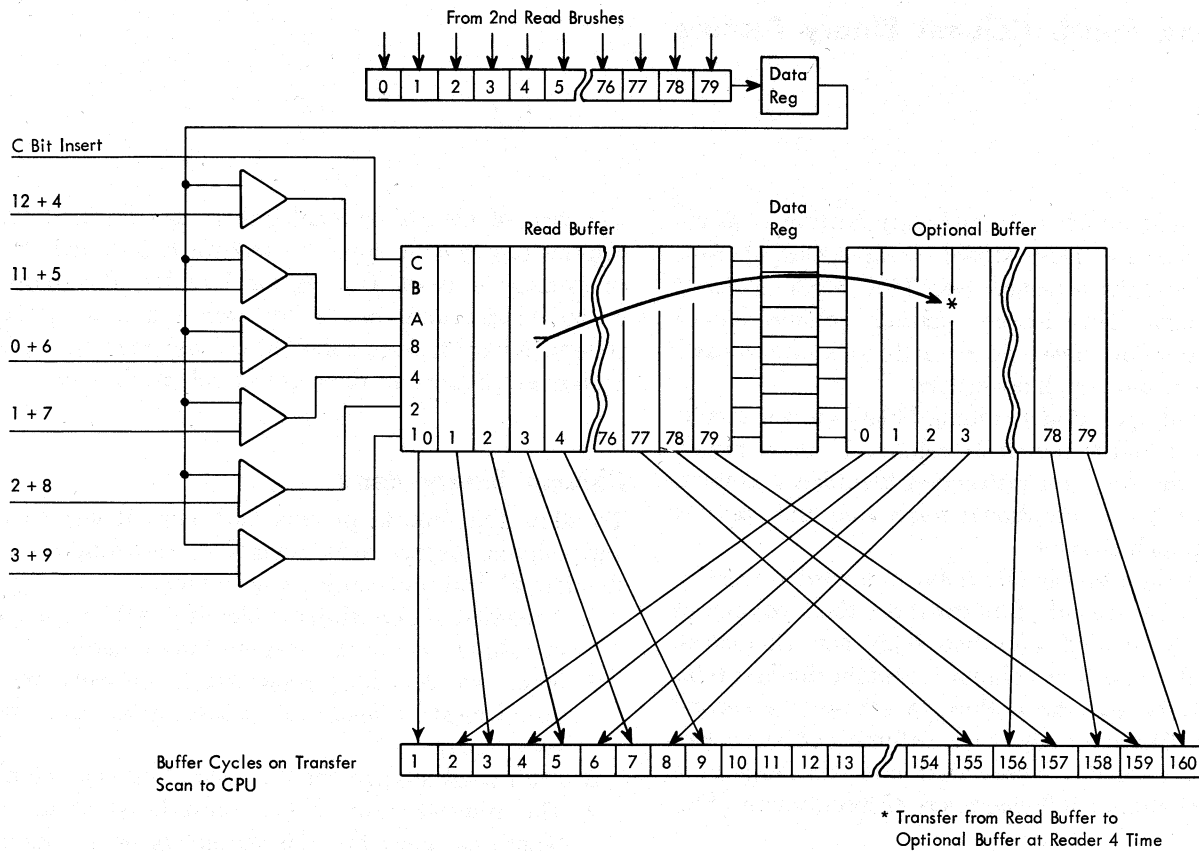


Figure 99. Column Binary Read

It must be kept in mind that the column binary controls are additions to the normal read circuits and in no way affect the reading of normal IBM code cards.

The sensing of the combination of the 9 and 7 punches in column 1 occurs on the card feed cycle that the column binary card passes the first read station. Hole-count checking occurs in the normal way regardless of which type of card is detected. If a 9 and 7 punch combination in column 1 is sensed, the indication is stored and then activates the controlling circuits on the next card feed cycle which is the cycle that the column binary card passes the second read station.

The first six rows of the column binary card (rows 9 through 4) are stored in the normal read buffer. However, the read encode circuits are bypassed and the 9 through 4 rows of the card are stored bit-for-bit in the 1 through B bit rows of the read buffer (Figure 99). At reader 4 time the read buffer is full, but only half of the column binary card has been read and a double-length read scan occurs. The double-length scan first stores the 4-row punches, then transfers the entire contents of the read buffer into the assigned optional buffer. The read buffer contents are thus moved before 3 time so that the second half of the

card can read into the read buffer (rows 3 through 12).

At the end of the card feed cycle the column binary card information is stored in two buffers. Rows 9 through 4 are in the optional buffer and rows 3 through 12 are in the normal read buffer.

The column binary circuits remain active until after the transfer scan to CPU. The program must test the column binary indication and set up a read instruction that can handle a 160-character record. A normal read instruction then starts the transfer scan, but because the column binary control circuits are not reset until the next reader 9 time a double-length transfer scan occurs (1760 usec). The column binary controls cause this long scan to send the first character to CPU from the read buffer, the second from the optional buffer, the third from the read buffer, etc., alternating buffers until the 160 characters, or the contents of both buffers, are transferred to CPU.

Column Binary Punch

The CPU program must set up a 160-character record and issue a special instruction to punch a column

binary card. (M/L %SN BBBB W for 1410). If the identifying 7-9 punches for column 1 of the card are to appear in the output cards, the data must contain the 1 and 4 bit in the second position of the 160-character record.

The transfer scan that places the 160-character record in the 1414 is a double-length scan. The first character is stored in the first position of the punch buffer, the second in the first position of the optional buffer, the third in the second position of the punch buffer, etc. until both buffers are filled (1760 usec).

After the transfer scan, the punch clutch is energized and punching from the punch buffer starts like a normal punch operation. However, the column binary controls cause the punch decode to be bypassed and the punch buffer punches out bit-for-bit. For example, the B bits of the punch buffer are punched as a row in the 12 row of the card.

At 4 time of a punch cycle, a long scan is taken that reads out the 4 row together with the remaining characters from the B-bit row of the option buffer and transfers the contents of the punch optional buffer into the punch buffer. Then, at punch 4 time the punch buffer again begins to punch out, continuing through 9 time to complete the cycle.

In summary: The 160-cycle transfer scan fills the two buffers by alternating between the punch and optional buffer. All punching is done from the punch buffer. Because the punching is done on a direct hole-for-bit basis, the punch buffer is empty after punching the 3 row of the card. Then, before the punch scan for the 4 row occurs, the punch buffer is refilled by transferring the contents of the optional buffer into the punch buffer. The 4 through 9 rows are then punched from the punch buffer by reading out the punch buffer a second time (Figure 100).

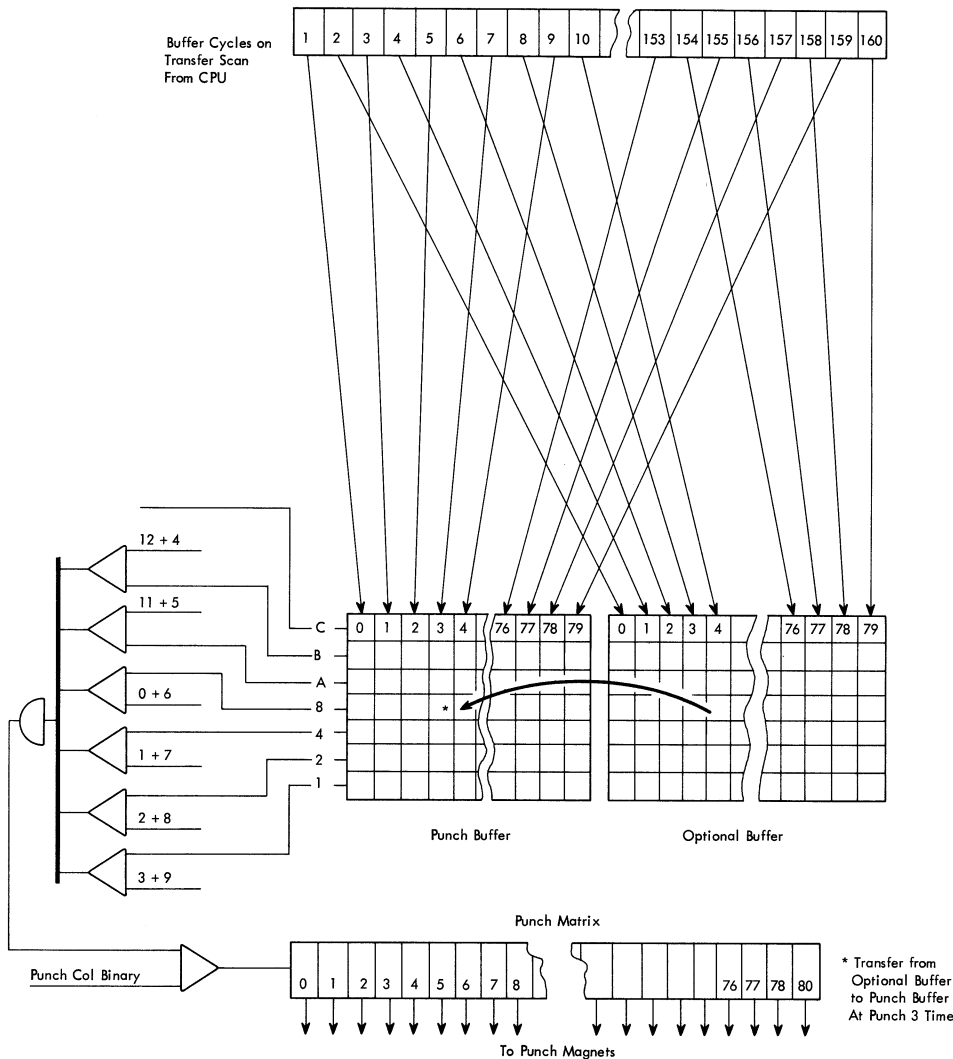


Figure 100. Punch Column Binary

Second Level Diagrams and Timing Charts

Figures 101 through 104 show the modifications and additions to the standard circuits necessary to accommodate the column binary feature.

Figures 105 through 118 present the logic of the standard 1414.

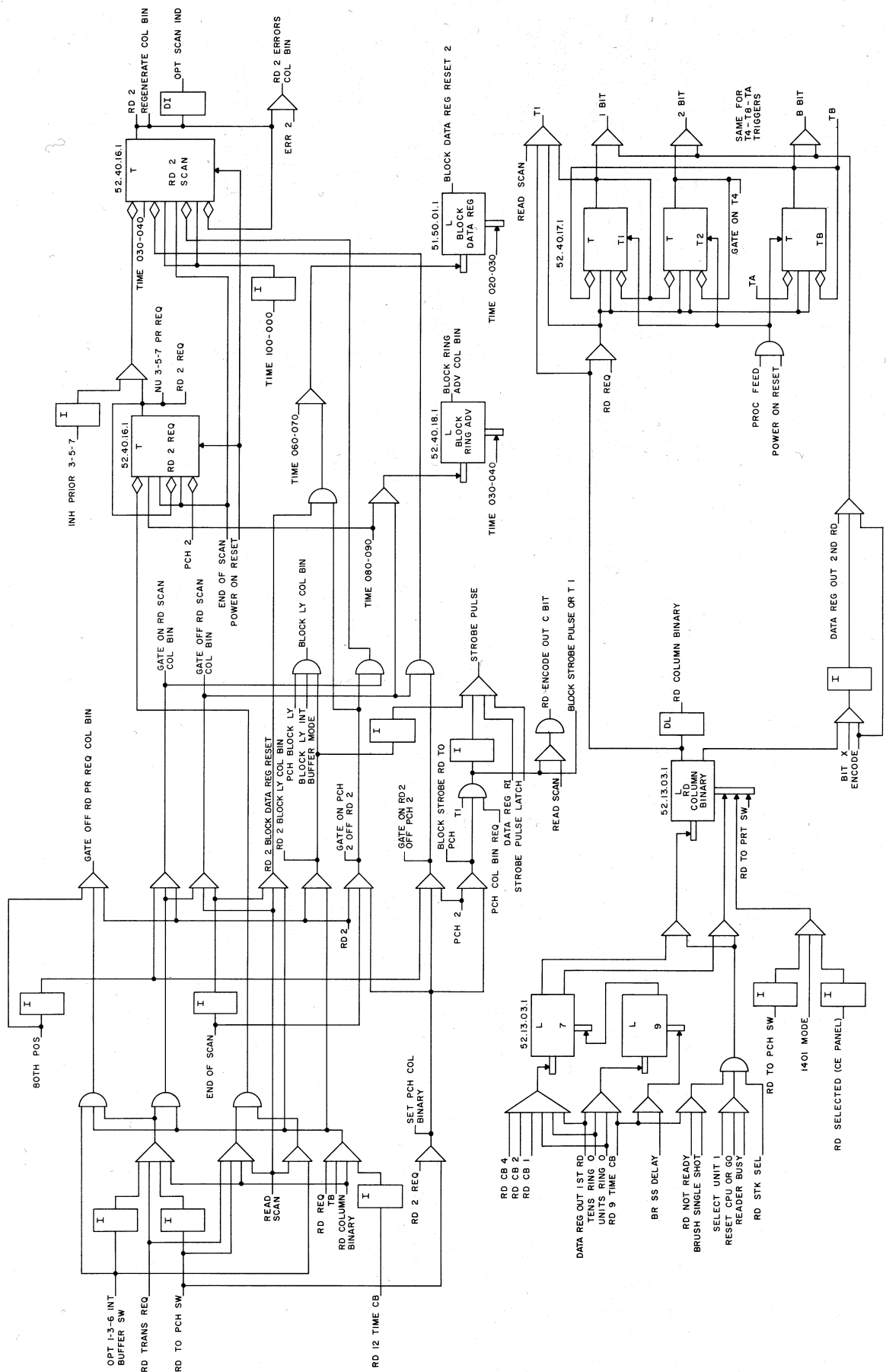


Figure 101. Reader Controls - Column Binary

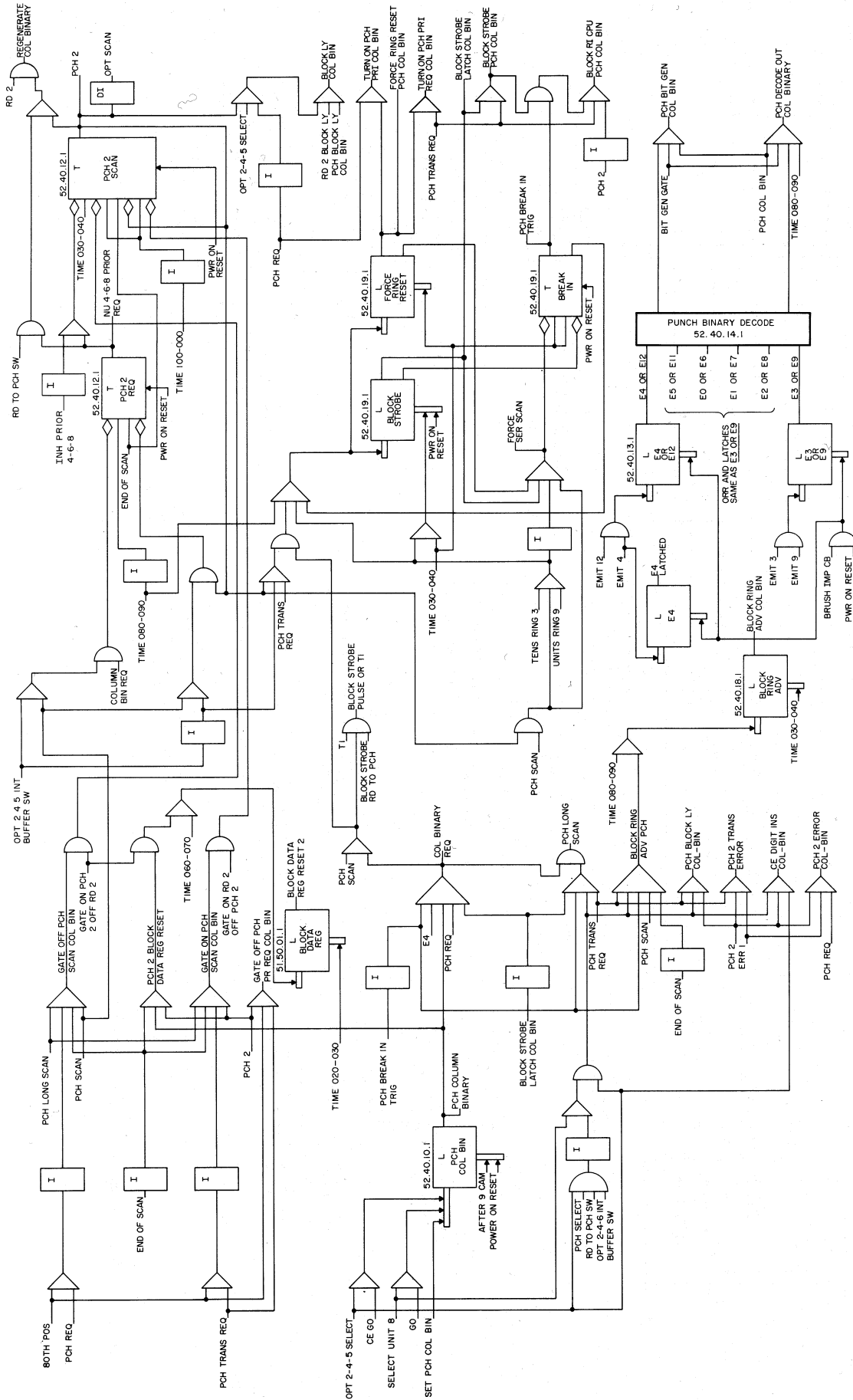


Figure 102. Punch Controls - Column Binary

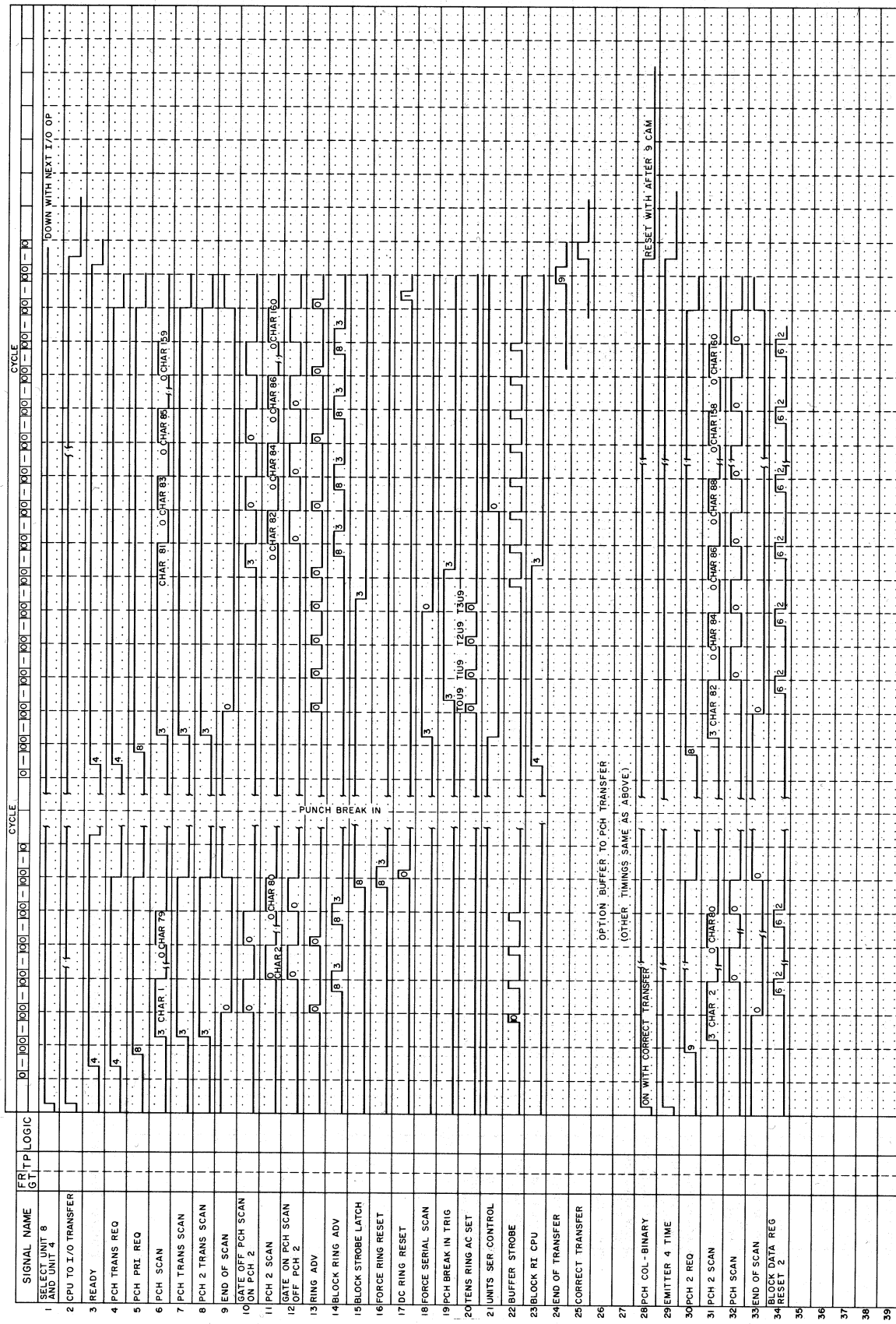


Figure 103. Punch Timing - Column Binary

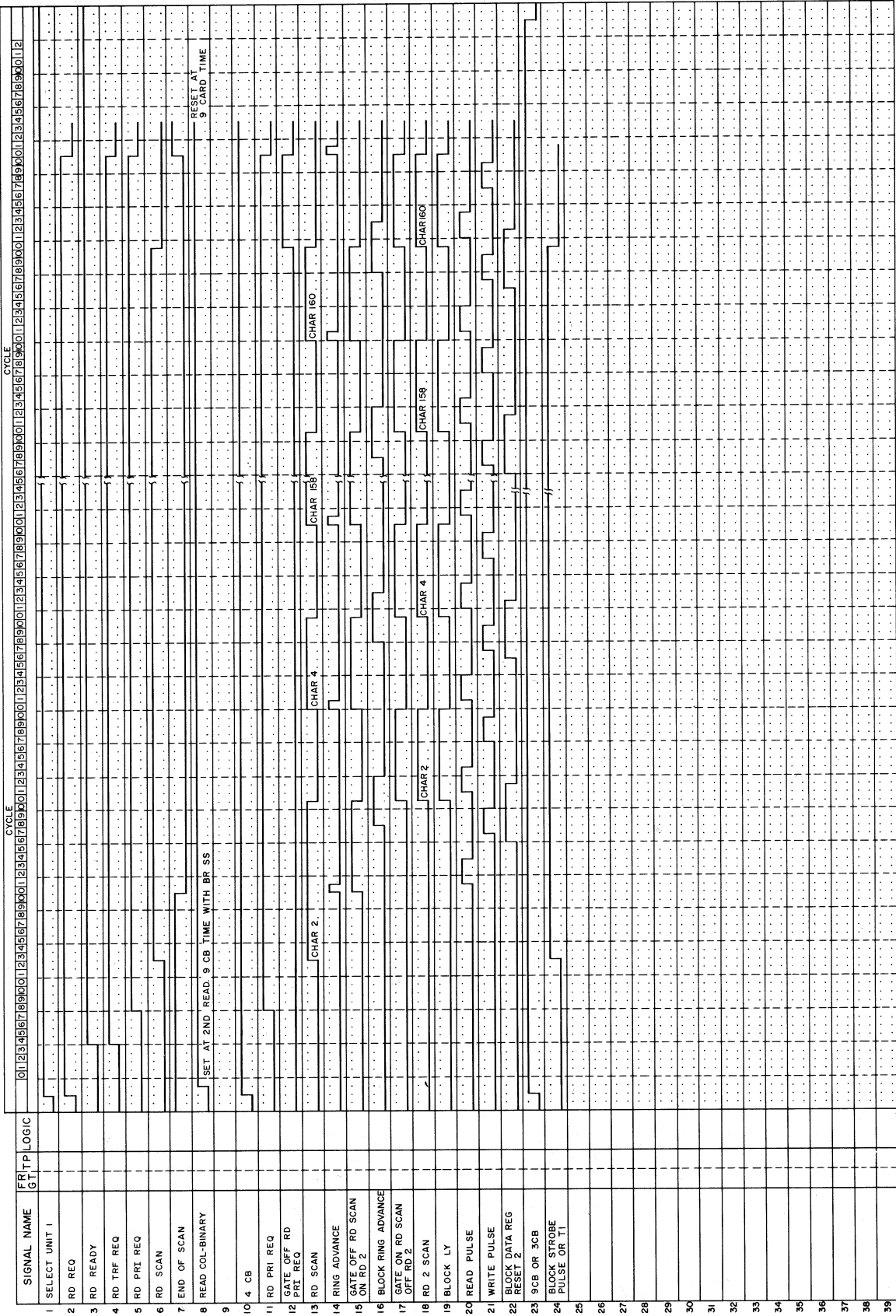


Figure 104. Read Timing - Column Binary

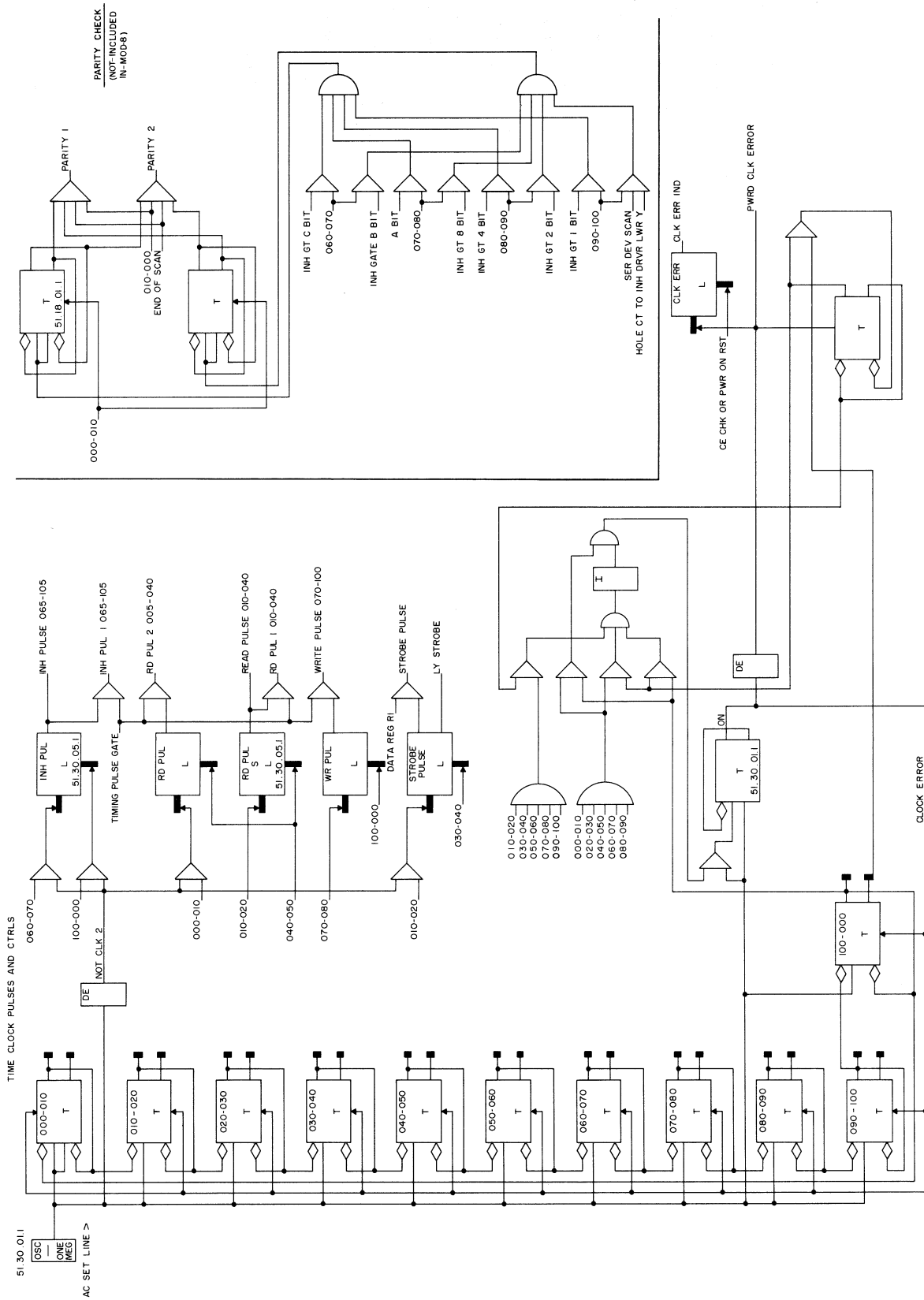


Figure 105. Time Clock and Controls

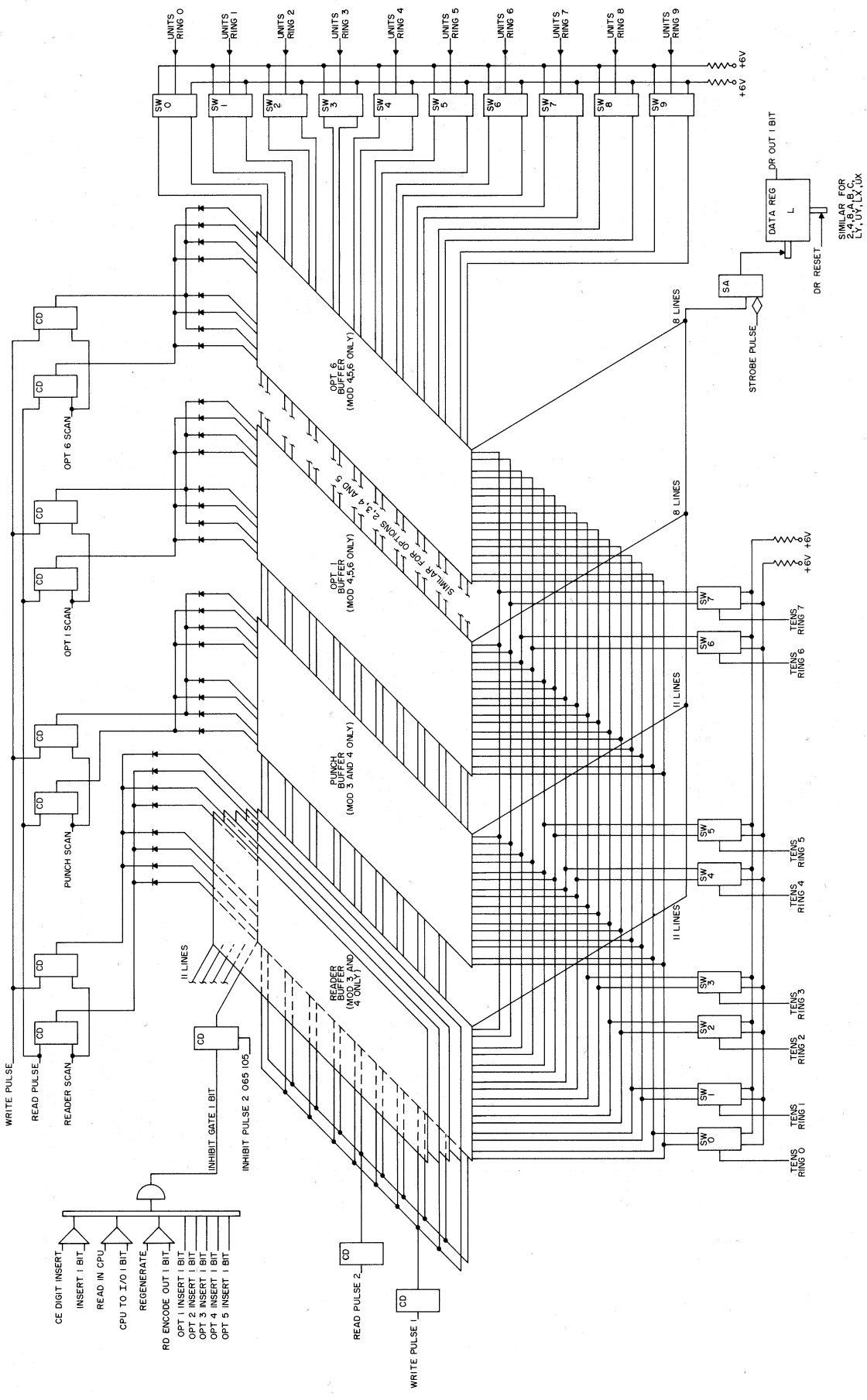


Figure 106. Buffer Controls

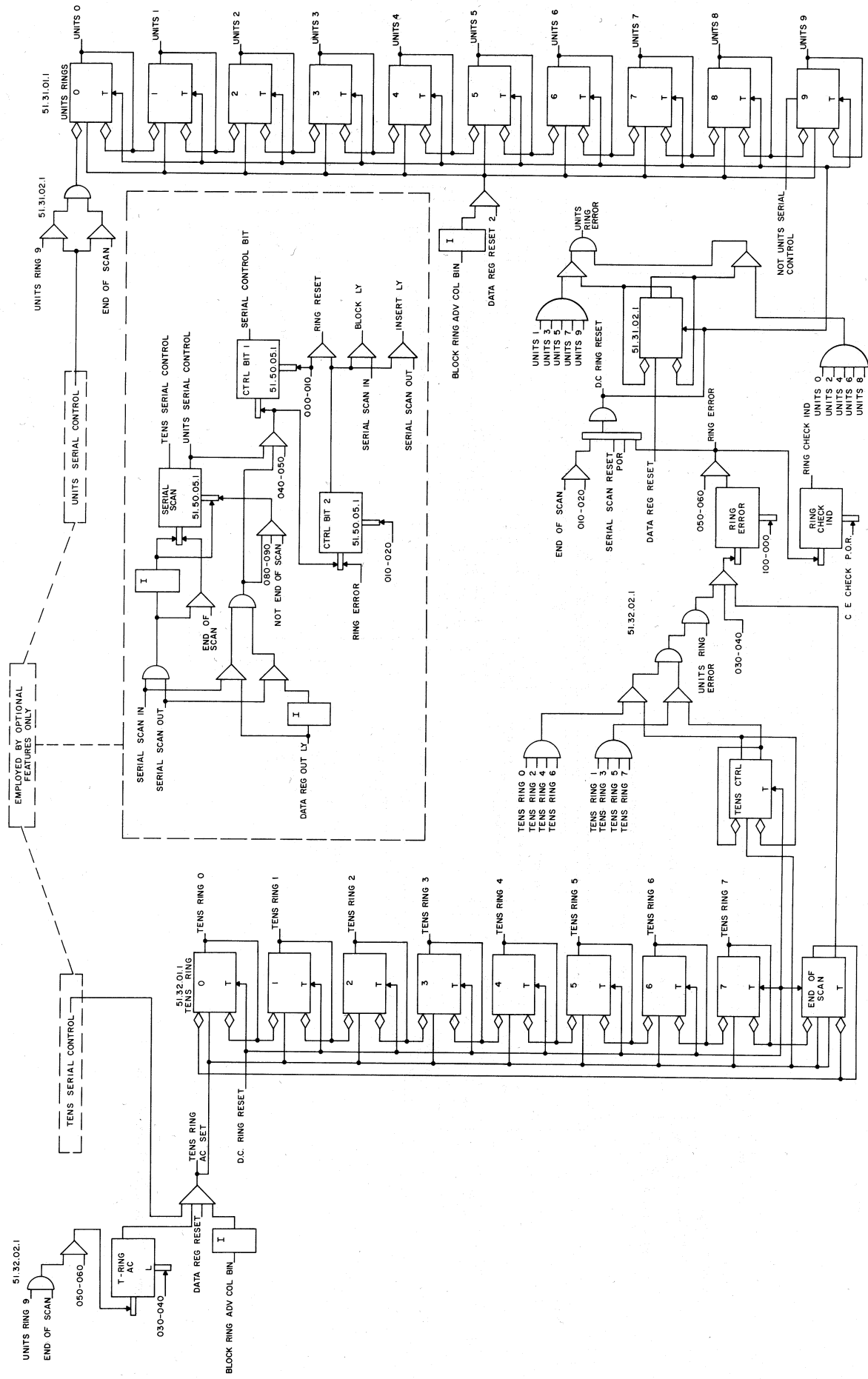


Figure 107. Buffer Rings

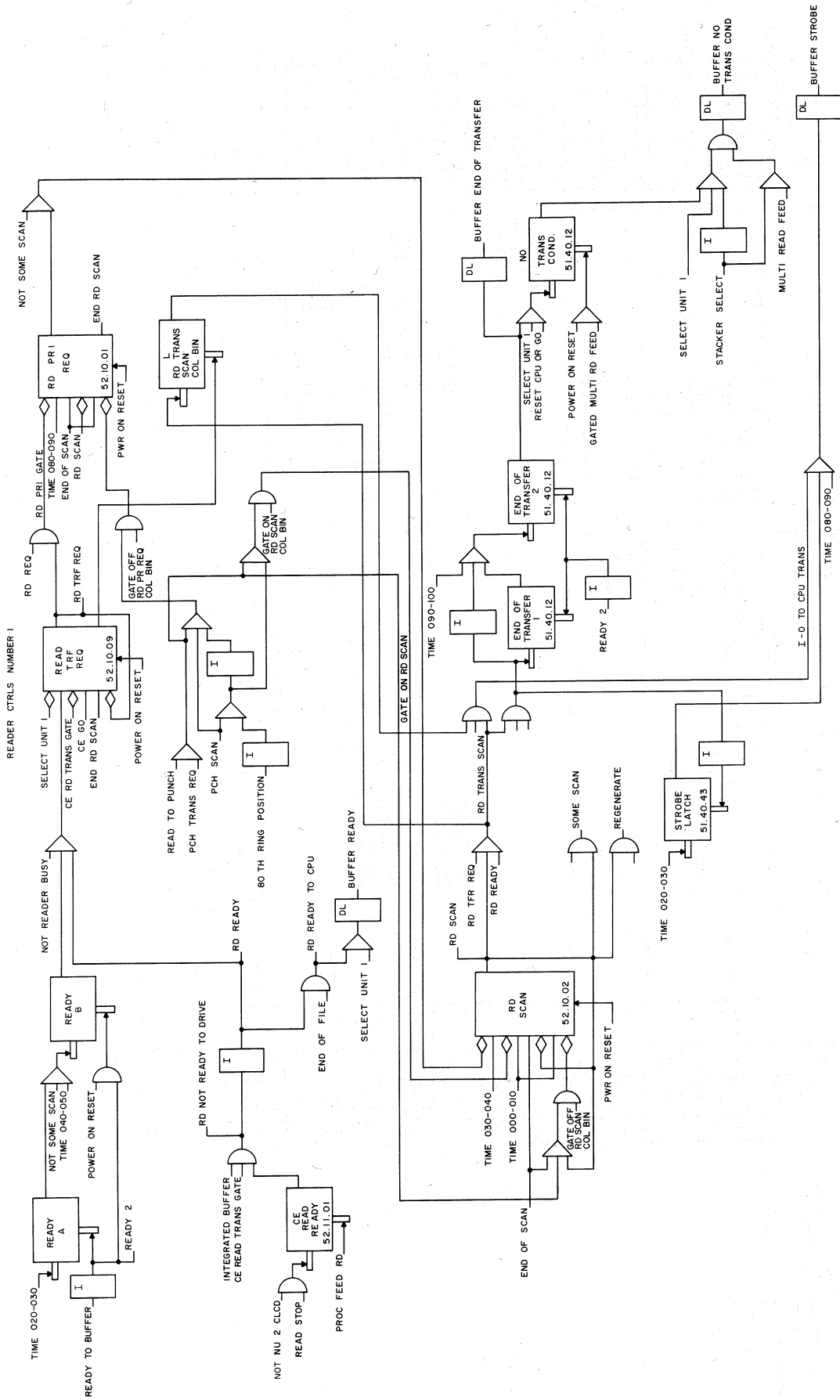


Figure 108. Reader Controls - No. 1

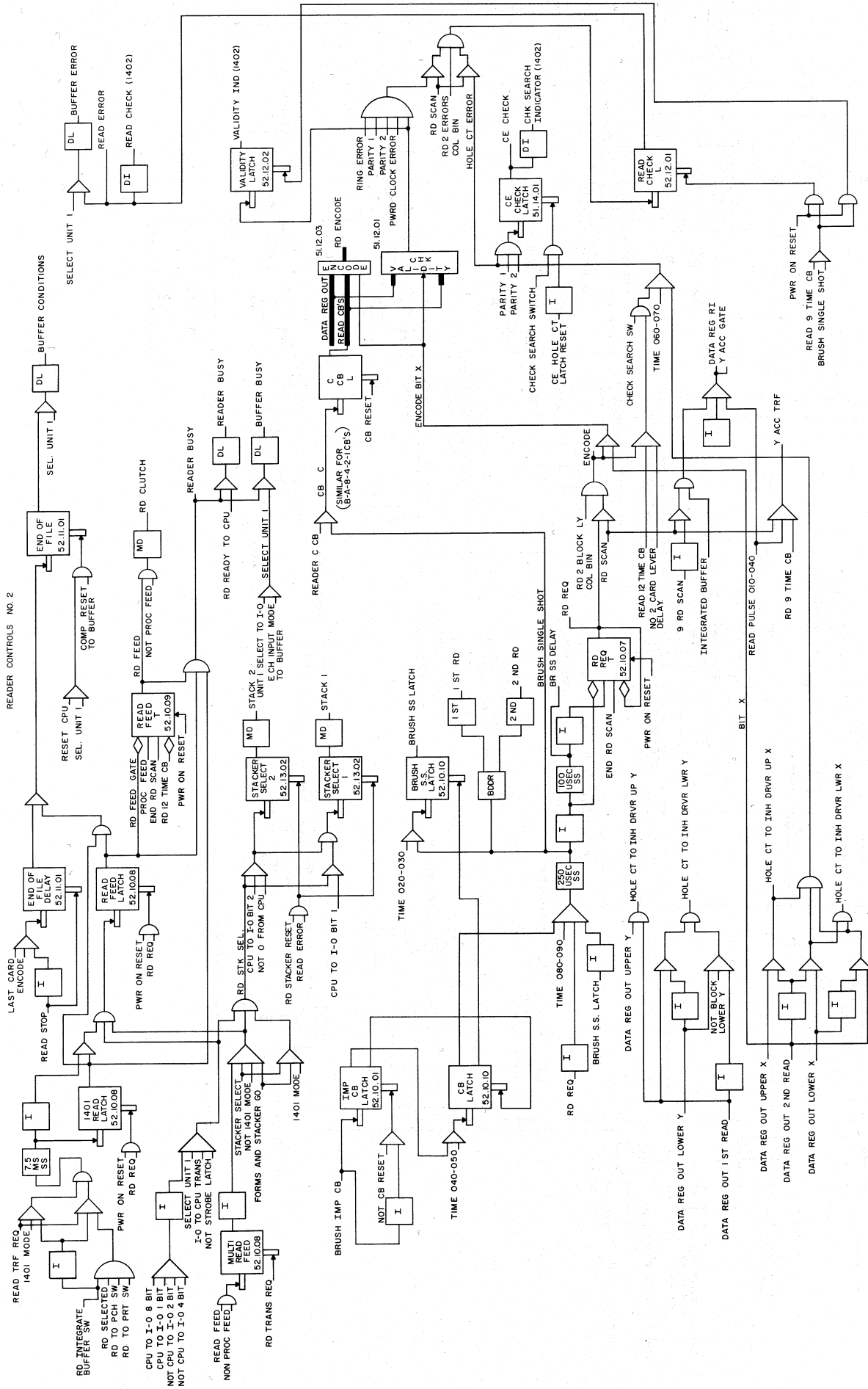


Figure 109. Reader Controls

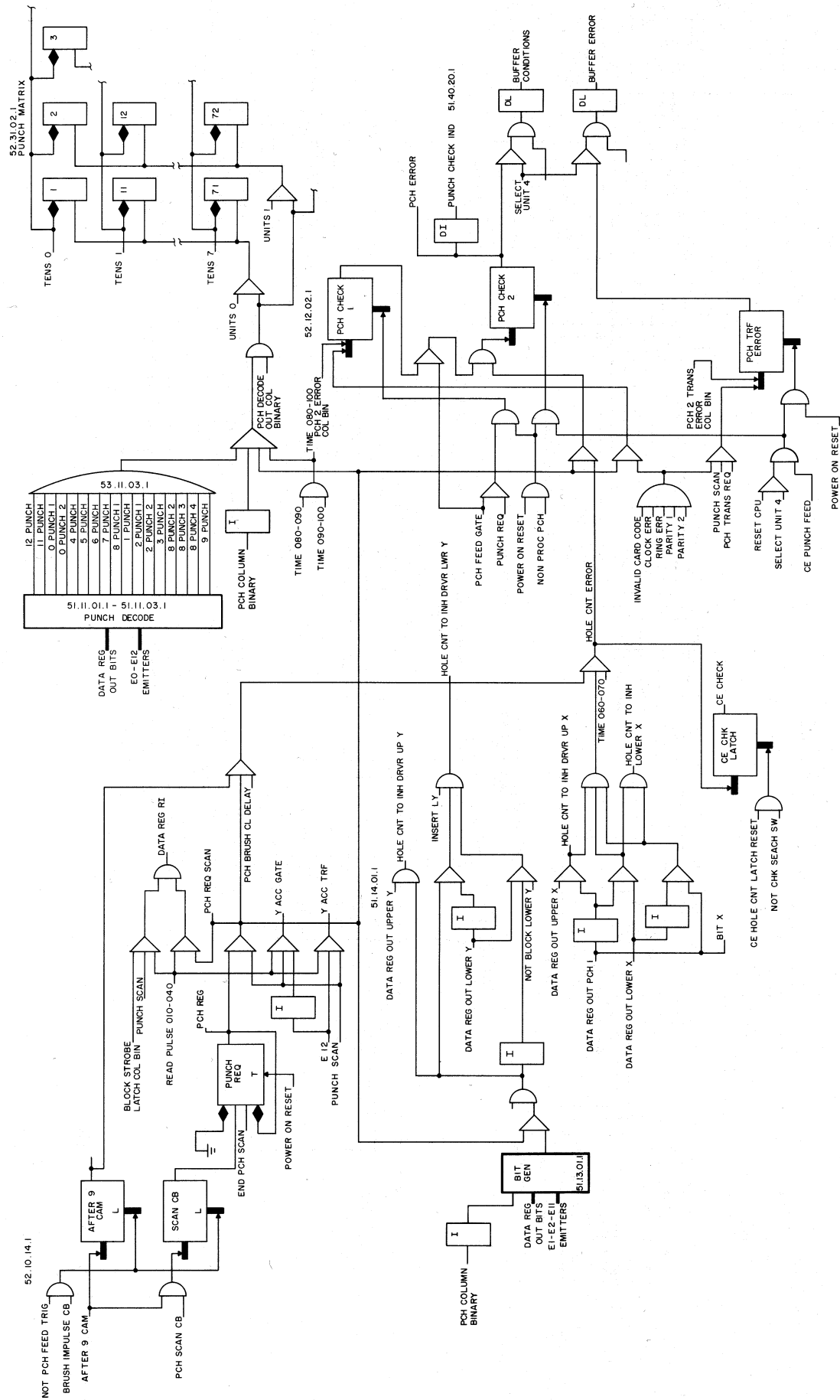


Figure 111. Punch Controls

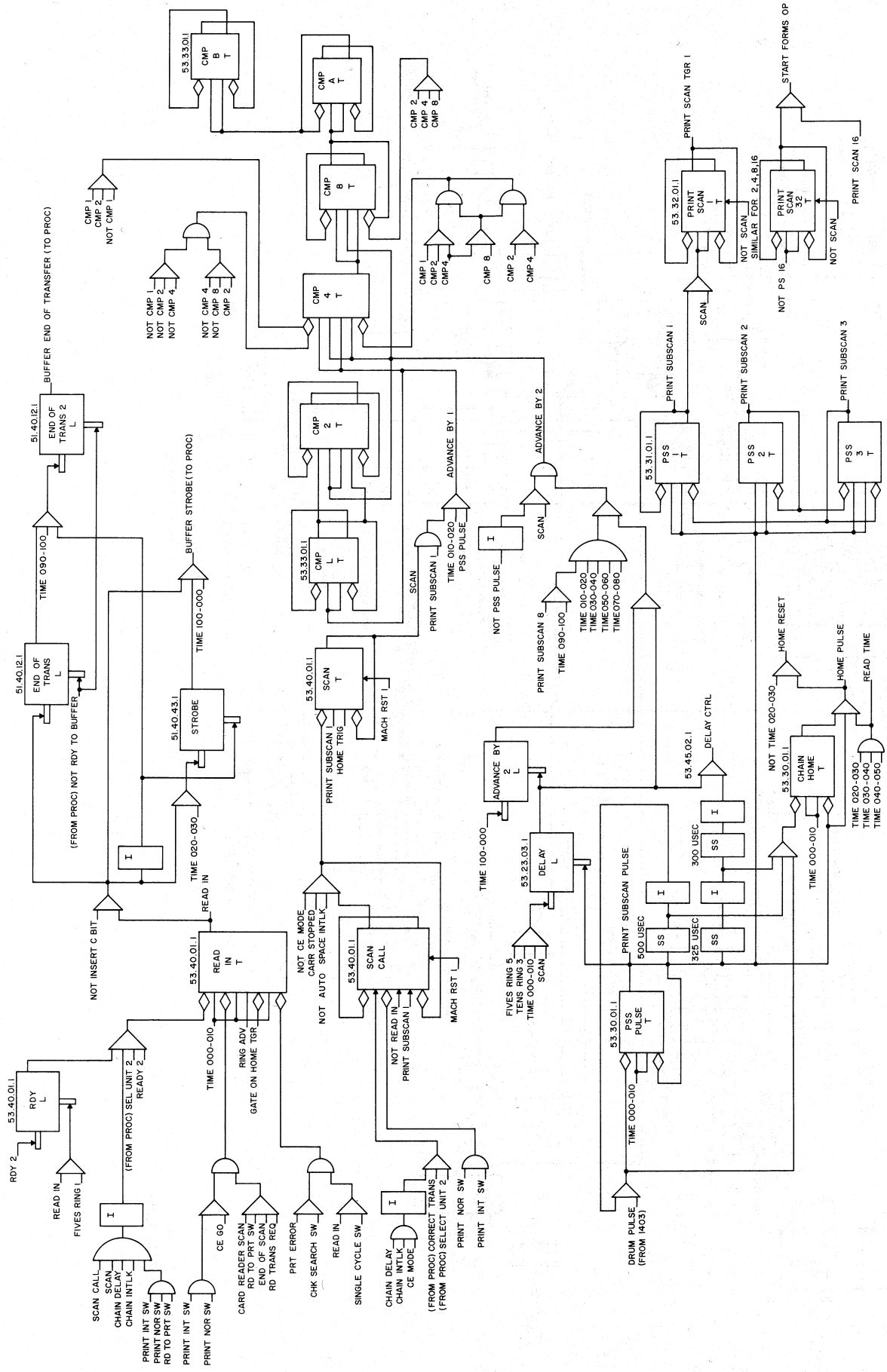


Figure 112. Printer Controls

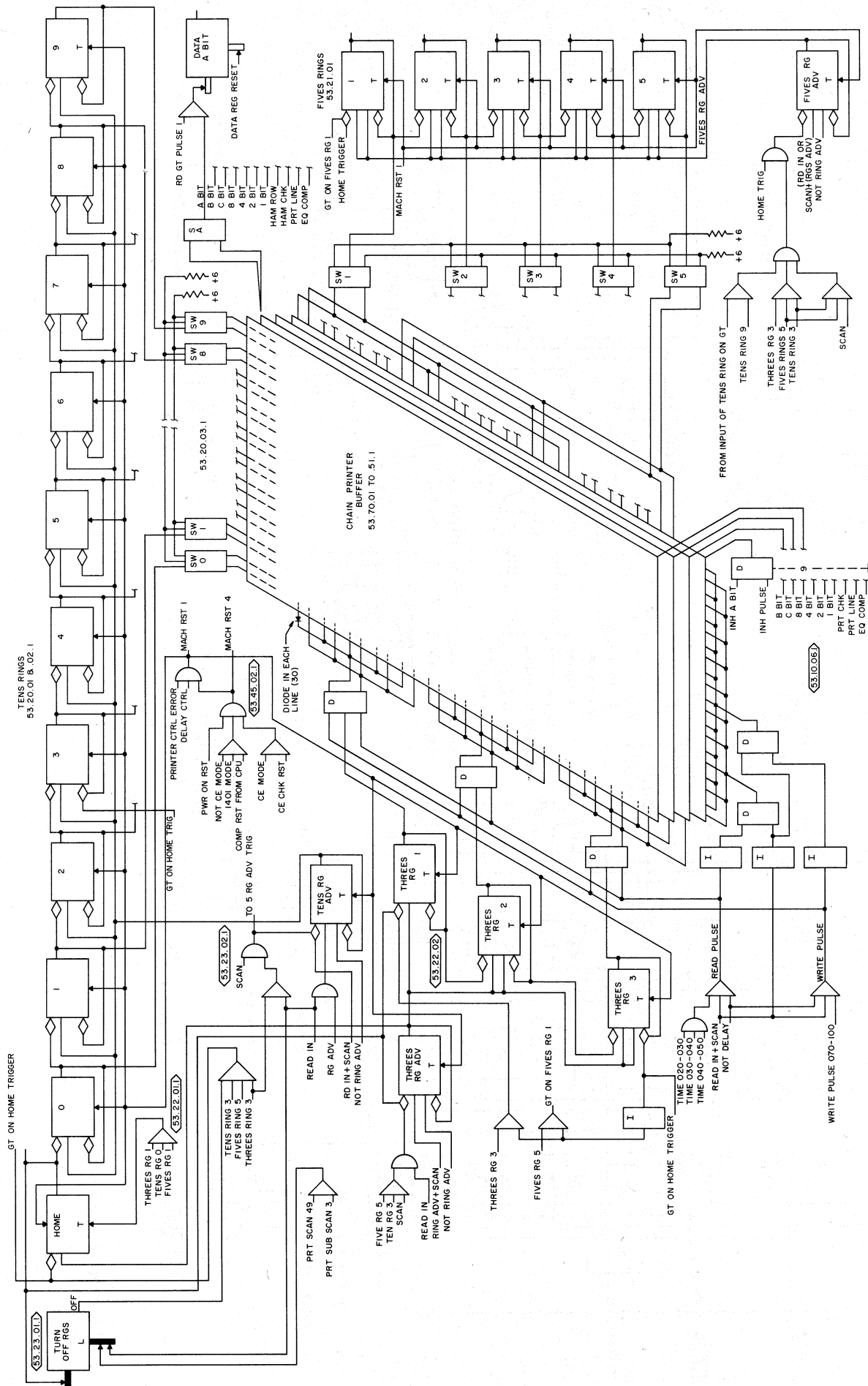
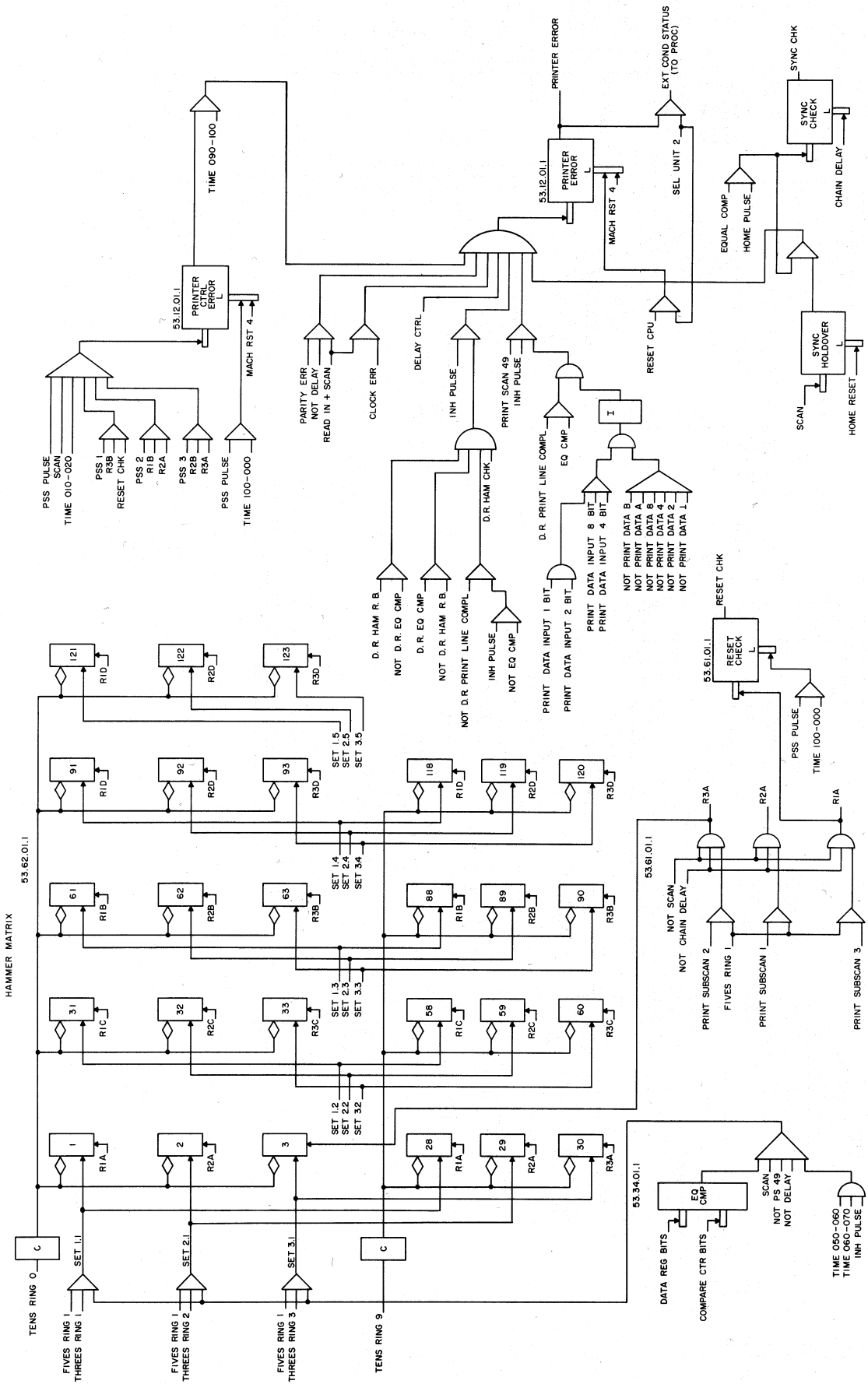


Figure 113. Chain Printer



ABOVE SIGNALS FOR OTHER RESETS

Figure 114. Hammer Matrix and Printer Status

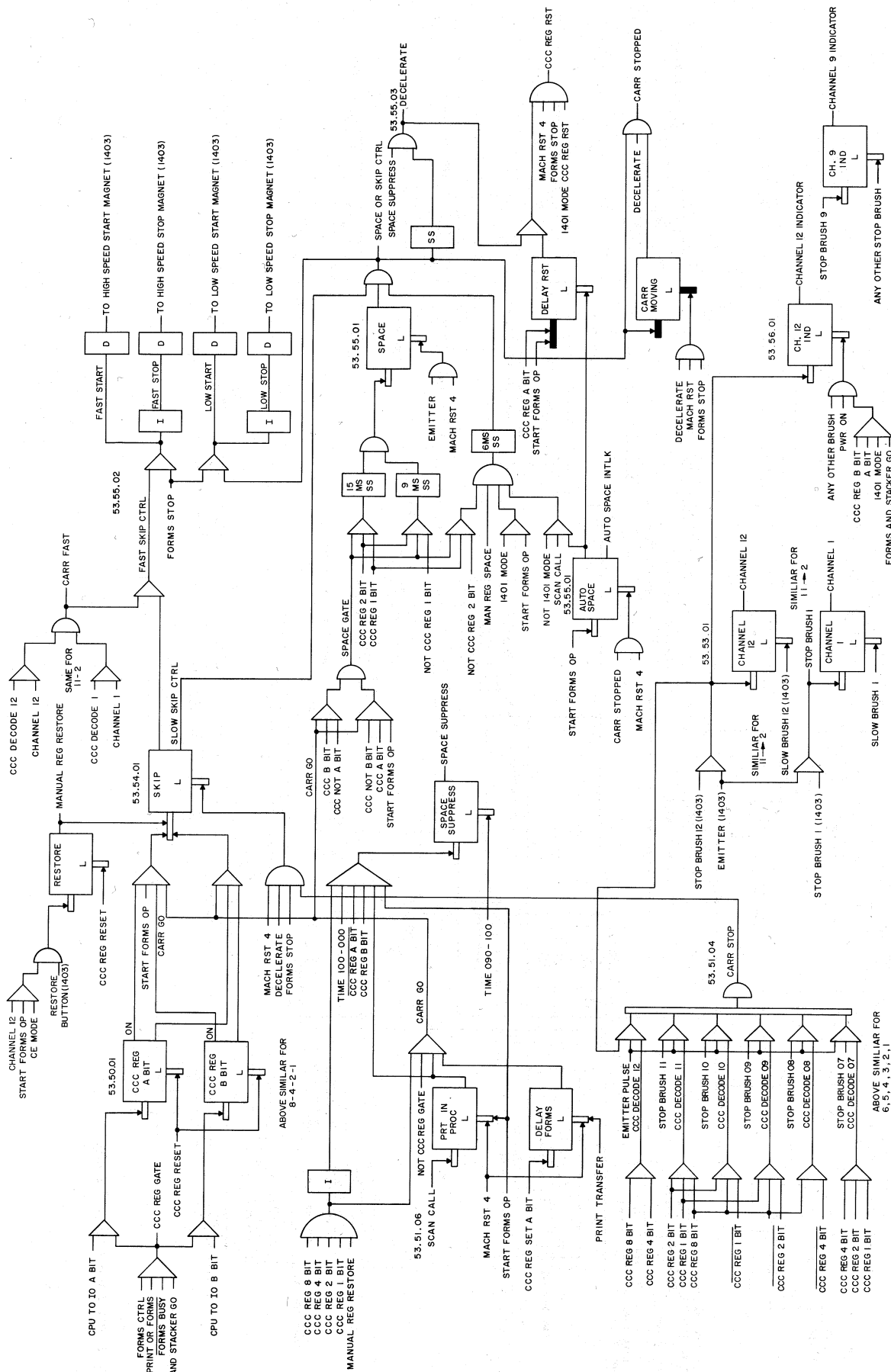


Figure 115. Carriage Control Circuits

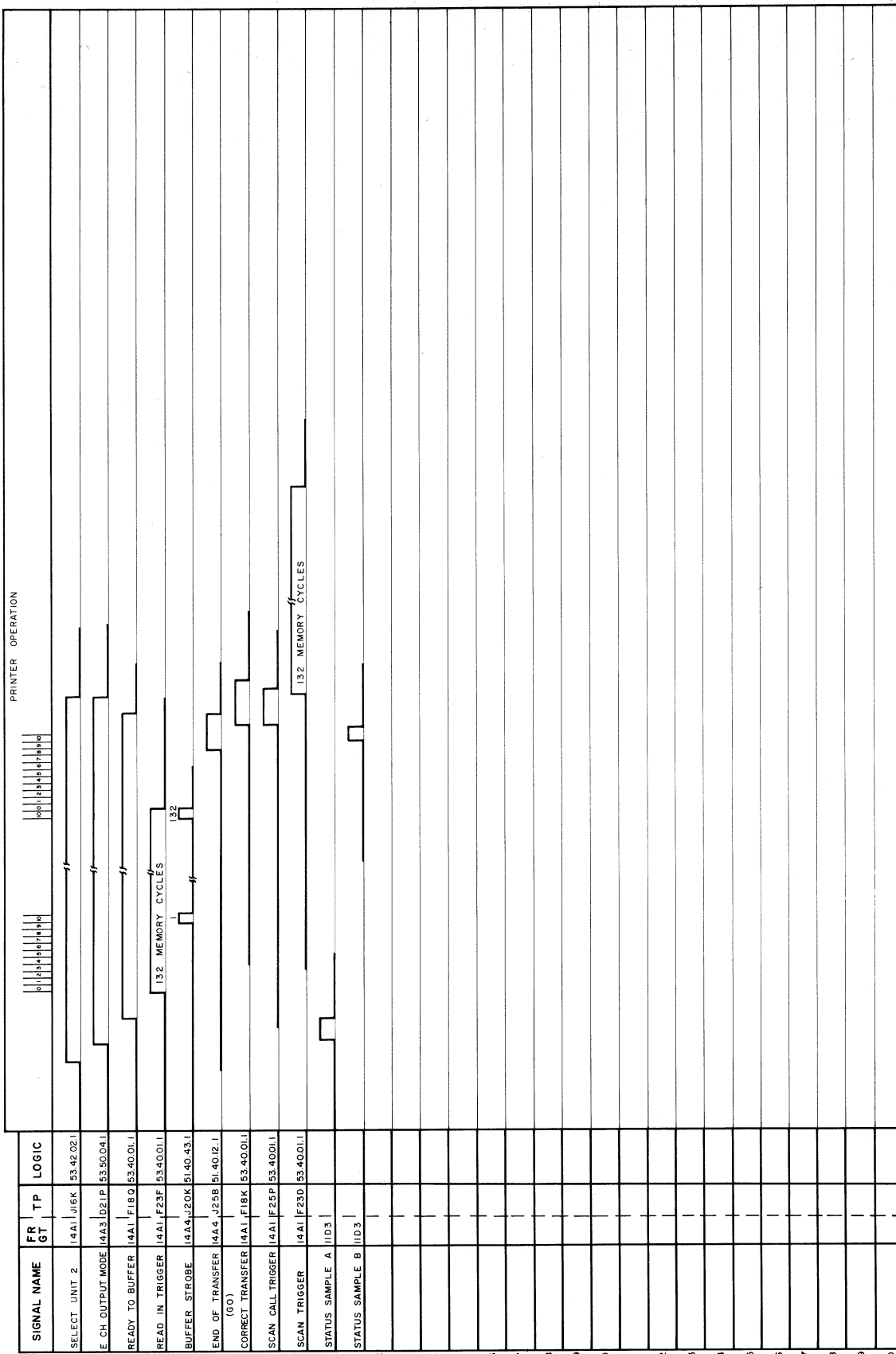


Figure 118. Printer Timing



COMMENT SHEET

IBM I414 INPUT-OUTPUT SYNCHRONIZER
MODELS 3, 4, 5, 6 AND 7

CUSTOMER ENGINEERING INSTRUCTION-REFERENCE, FORM 223-2590

FROM

NAME _____

OFFICE NO. _____

FOLD

CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

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SUGGESTED ADDITION (PAGE , TIMING CHART, DRAWING, PROCEDURE, ETC.)

SUGGESTED DELETION (PAGE)

ERROR (PAGE)

EXPLANATION

CUT ALONG LINE

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NO POSTAGE NECESSARY IF MAILED IN U. S. A.
FOLD ON TWO LINES, STAPLE, AND MAIL

STAPLE

STAPLE

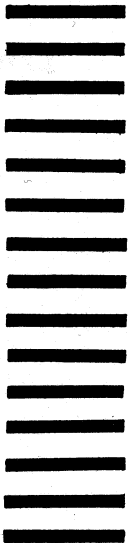
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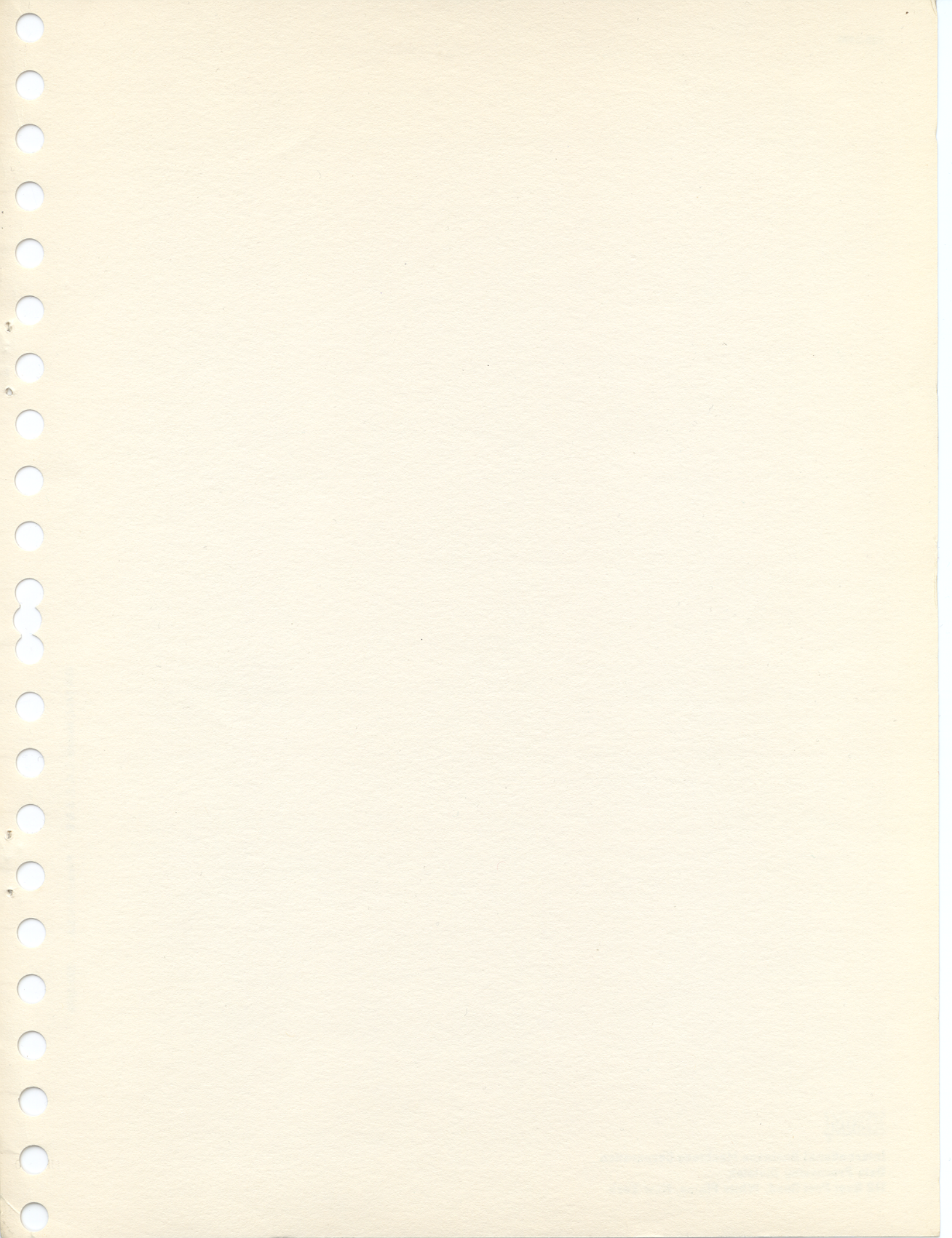
ATTN: CE MANUALS, DEPARTMENT B96

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STAPLE



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