HP 13255

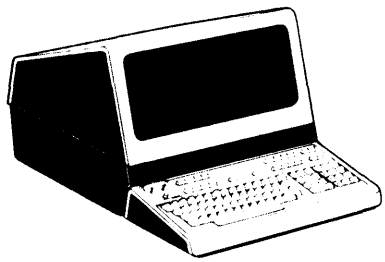
HIGH-SPEED PARALLEL PORT MODULE

Manual Part No. 13255-91146

PRINTED

AUG-01-76

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The High-Speed Parallel Port Module provides byte-parallel data transfer directly into the terminal RAM from a host computer without intervention by the terminal processor. Transfer from the keyboard to the computer is under terminal processor control. Provision is made for a self-test of the functional hardware on this PCA.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the High-Speed Parallel Port Module is contained in tables 1.0 through 6.3.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60146	High-Speed Parallel Port PCA	12.9 x 4.0 x 0.5	0.42
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Number of Backplane Slots Required: 1

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B ( ) Other:
Restrictions:	Type tested at product level
Failure Rate:	1.310 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 680 mA	@ mA	@ mA	@ mA
	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
PG0	Add 256 to initial store address of module	Add 0 to initial store address of module
PG1	Add 512 to initial store address of module	Add 0 to initial store address of module
PG2	Add 1K to initial store address of module	Add 0 to initial store address of module
PG3	Add 2K to initial store address of module	Add 0 to initial store address of module
PG4	Add 4K to initial store address of module	Add 0 to initial store address of module
PG5	Add 8K to initial store address of module	Add 0 to initial store address of module
PG6	Add 16K to initial store address of module	Add 0 to initial store address of module
PG7	Add 32K to initial store address of module (All in is initial store address of 255)	Add 0 to initial store address of module (All out is initial store address of 65K)
MSBI	Do not invert $\overline{\text{ADDR14,15}}$	Invert $\overline{\text{ADDR14,15}}$
INT	EOP interrupt on $\overline{\text{ATN}}$ line	$\overline{\text{ATN}}$ line not used
INT2	EOP interrupt on $\overline{\text{ATN2}}$ line	$\overline{\text{ATN2}}$ line not used
PL0-PL6	Respond to poll by pulling $\overline{\text{BUSn}}$ low corresponding to PLn	Do not respond to poll on $\overline{\text{BUSn}}$
INH	Do not recognize home-up or backspace codes	Act upon home-up or backspace codes
CRLF	Do not recognize carriage return or line feed codes	Ignore carriage return, change line feed to EOL code

5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	POLL	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	BUS0	Negative True, Data Bus Bit 0
-F	BUS1	Negative True, Data Bus Bit 1
-H	BUS2	Negative True, Data Bus Bit 2
-J	BUS3	Negative True, Data Bus Bit 3
-K	BUS4	Negative True, Data Bus Bit 4
-L	BUS5	Negative True, Data Bus Bit 5
-M	BUS6	Negative True, Data Bus Bit 6
-N	BUS7	Negative True, Data Bus Bit 7
-P	WRITE	Negative True, Write/Read Type Cycle
-R	ATN2	Negative True, CTU and Polled Interrupt Request
-S	WAIT	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	PROC ACTIVE	Negative True, Processor Active (Controlling Bus)
-W	BUSY	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	REQ	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	GND	Ground
- 2	GND	Ground
- 3	GND	Ground
- 4	GND	Ground
- 5	GND	Ground
- 6	GND	Ground
- 7	GND	Ground
- 8	$\overline{\text{DOUT0}}$	Negative True, Data Out Bit 0
- 9	$\overline{\text{DOUT1}}$	Negative True, Data Out Bit 1
-10	$\overline{\text{DOUT2}}$	Negative True, Data Out Bit 2
-11	$\overline{\text{DOUT3}}$	Negative True, Data Out Bit 3
-12	$\overline{\text{DOUT4}}$	Negative True, Data Out Bit 4
-13	$\overline{\text{DOUT5}}$	Negative True, Data Out Bit 5
-14	$\overline{\text{DOUT6}}$	Negative True, Data Out Bit 6
-15	$\overline{\text{DOUT7}}$	Negative True, Data Out Bit 7

Table 5.1 Connector Information (Cont'd.)

Connector and Pin NO.	Signal Name	Signal Description
P2, Pin A	$\overline{\text{DIN0}}$	Negative True, Data In Bit 0
-B	$\overline{\text{DIN1}}$	Negative True, Data In Bit 1
-C	$\overline{\text{DIN2}}$	Negative True, Data In Bit 2
-D	$\overline{\text{DIN3}}$	Negative True, Data In Bit 3
-E	$\overline{\text{DIN4}}$	Negative True, Data In Bit 4
-F	$\overline{\text{DIN5}}$	Negative True, Data In Bit 5
-H	$\overline{\text{DIN6}}$	Negative True, Data In Bit 6
-J	$\overline{\text{DIN7}}$	Negative True, Data In Bit 7
-K	GND	Ground
-L	$\overline{\text{DIA}}$	Negative True, Data In Acknowledge
-M	$\overline{\text{DIR}}$	Negative True, Data In Request
-N	GND	Ground
-P	$\overline{\text{DOA}}$	Negative True, Data Out Acknowledge
-R	$\overline{\text{DOR}}$	Negative True, Data Out Request
-S	GND	Ground

Table 6.0 Module Bus Pin Assignments

Function Performed: Read to Set TEST Mode	Value	Bus Signal
	X	ADDR 15
Poll Bit: BUS0 - BUS6	X	ADDR 14
Depends on the setting of	X	ADDR 13
jumpers PL0 - PL6, respectively	X	ADDR 12
	1	ADDR 11
	1	ADDR 10
Module Address: (ADDR11,10,9,4) = (1100)	0	ADDR 9
	X	ADDR 8
	X	ADDR 7
Function Specifier: ADDR 5 = 1	0	ADDR 6
ADDR 6 = 0	1	ADDR 5
	0	ADDR 4
Data Bus Bit Interpretation: None	X	ADDR 3
	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
	X=Don't Care	

Table 6.1 Module Bus Pin Assignments

Function Performed: Read to Reset TEST Mode	Value	Bus Signal
	X	ADDR 15
Poll Bit: BUS0 - BUS6	X	ADDR 14
Depends on the setting of	X	ADDR 13
jumpers PL0 - PL6, respectively	X	ADDR 12
	1	ADDR 11
Module Address: (ADDR11,10,9,4) = (1100)	1	ADDR 10
	0	ADDR 9
	X	ADDR 8
Function Specifier: ADDR 5 = 0	X	ADDR 7
ADDR 6 = 0	0	ADDR 6
	0	ADDR 5
	0	ADDR 4
Data Bus Bit Interpretation: None	X	ADDR 3
	X	ADDR 2
	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
	X=Don't Care	

Table 6.2 Module Bus Pin Assignments

Function Performed: Read Status of Output Handshake

Poll Bit: BUS0 - BUS6
Depends on the setting of jumpers PL0 - PL6, respectively

Module Address: (ADDR11,10,9,4) = (1100)

Function Specifier: ADDR 6 = 1
ADDR 5 = 0

Data Bus Bit Interpretation:

B7: Not Used

B6: Not Used

B5: Not Used

B4: Not Used

B3: Not Used

B2: Not Used

B1: Not Used

B0: 0 = Output handshake not in progress
1 = Output handshake in progress

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
1	ADDR 11
1	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
0	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function Performed: Write Output Data	Value	Bus Signal
	X	ADDR 15
	X	ADDR 14
	X	ADDR 13
	X	ADDR 12
Poll Bit: BUS0 - BUS6	1	ADDR 11
Depends on the setting of	1	ADDR 10
jumpers PL0 - PL6, respectively	0	ADDR 9
	X	ADDR 8
	X	ADDR 7
Module Address: (ADDR11,10,9,4) = (1100)	1	ADDR 6
	1	ADDR 5
	0	ADDR 4
Function Specifier: ADDR 6 = 1	X	ADDR 3
ADDR 5 = 1	X	ADDR 2
	X	ADDR 1
Data Bus Bit Interpretation:	X	ADDR 0
	B7	BUS 7
B7 - Data Output Bit 7	B6	BUS 6
	B5	BUS 5
B6 - Data Output Bit 6	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
B5 - Data Output Bit 5	B1	BUS 1
	B0	BUS 0
B4 - Data Output Bit 4	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
	X=Don't Care	
B3 - Data Output Bit 3		
B2 - Data Output Bit 2		
B1 - Data Output Bit 1		
B0 - Data Output Bit 0		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts list (02640-60146) located in the appendix.

This PCA provides the capability of transferring 8-bit parallel information between the terminal and a host computer. Data received by the PCA from the computer is transferred directly into RAM memory without the aid of the terminal processor. Data transfer to the computer is under terminal processor control. All data transfers occur using a 2-wire handshake.

3.1 BUS CONTROLLER.

3.1.1 This block is responsible for controlling the transfer of data from an external computer into the terminal RAM memory.

3.1.2 U11, U12, and U13 form a state machine which is synchronized to the terminal clock. U11 is a multiplexor which selects the inputs of interest in any particular state. U12 is a counter which contains the present state of the controller. U13 is a decoder which provides the control signals based upon the present state of the state machine. If a home-up code (313 octal) is present, the bus controller resets the address control and stores an EOP code (316 octal) in the terminal memory. If a backspace code (312 octal) is present, the bus controller increments the address control by 1 and stores an EOP code in the terminal memory. If any other code is present, the bus controller stores the code in the terminal memory, decrements the address control and then stores an EOP code.

In state 0, the bus controller waits for the next data byte, holding NEW DATA OK high. When an input handshake occurs in the data path and handshake block, this fact is relayed to the bus controller by the DATA RDY signal, causing the state to change from 0 to 1.

In state 1 PRIOR OUT is changed to low to inhibit lower priority devices on the terminal bus from obtaining control of the bus.

The bus controller waits for the PRIOR IN and $\overline{\text{BUSY}}$ signals to be high, indicating that no other module is currently using the terminal bus. This causes the bus controller to change from state 1 to state 2.

In state 2, U19, Pin 7, the EXTRA/$\overline{\text{EOP}}$ flip-flop, is set which will indicate to the bus controller in state 7 that an extra data transfer is required to store an EOP code. Also, $\overline{\text{BUSY}}$ is held low to prevent

other devices on the terminal bus from requesting control of the bus. If either a home-up code or backspace code is present in the data path and handshake section (as indicated by the HU+BS signal), the bus controller changes to state 3; otherwise, state 4 is entered.

In state 3, U19, Pin 7, the EXTRA/$\overline{\text{EOP}}$ flip-flop, is reset to indicate that only one transfer to memory is required for the code present in the data path and handshake block. Also, drive enables U54 through U57, allowing $\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$ and $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR15}}$ to be active on the terminal bus. $\overline{\text{WRITE}}$ is held low to indicate that a write (to memory) will occur. If $\overline{\text{HOME UP}}$ is low, then $\overline{\text{RST ADDR}}$ will be low, causing the counters in the address control block to increment by 1. Control is then transferred to state 4.

State 4 enables U54 through U57 in the same manner as state 3. However, U19, Pin 7 is not reset. Control is passed to state 5.

In state 5, $\overline{\text{REQ}}$ is brought low to strobe the data on $\overline{\text{L0}}$ through $\overline{\text{L7}}$ into the terminal memory. The bus controller remains in state 5 until $\overline{\text{WAIT}}$ goes high, indicating that the memory has received the data. At this point, the state changes to state 6.

State 6 asserts the same signals as state 5. However, control passes immediately from state 6 to state 7.

In state 7, $\overline{\text{REQ}}$ is allowed to go high. If U19, Pin 7 is set, then an EOP code must be written to memory and control transfers to state 8; otherwise, control is returned to state 0.

In state 8, U19, Pin 7 is reset so that only the EOP code will be stored in memory. Also $\overline{\text{DEC ADDR}}$ is low, causing the counters in the address control block to decrement by 1 (pointing to the next lower memory location). U54 through U57 are not enabled in this state. Control is immediately transferred to state 4. Control passes through states 4, 5, 6, and 7. When state 7 is reached (since state 8 has reset U19, Pin 7), control goes to state 0.

3.2 ADDRESS CONTROL.

3.2.1 This block allows the bus controller to access the particular memory location into which the next data byte is to be stored.

3.2.2 U44 through U47 are 4-bit presetable up/down counters configured to form one 16-bit counter, with U47, Pin 7 as the most-significant bit and U44, Pin 3 as the least-significant bit. U44 through U47 will be referred to as the "address counter" in the following discussion.

The address counter is preset if one of three conditions occur:

1) When the $\overline{\text{PON}}$ signal from the bus controller is low.

2) When the $\overline{\text{RST ADDR}}$ signal from the bus controller is low, indicating the presence of a home-up code.

3) When the address counter attempts to increment past a value of 177777 octal.

The value that is preset into the address counter is

$\overline{\text{PG7}}\overline{\text{PG6}}\overline{\text{PG5}}\overline{\text{PG4}}\overline{\text{PG3}}\overline{\text{PG2}}\overline{\text{PG1}}\overline{\text{PG0}}$11111111 binary, where PG0 through PG7 are straps inserted in U17. The preset bit value from a strap is "1" when the strap is removed and "0", when the strap is inserted.

The address counter is incremented by 1 if the $\overline{\text{INC ADDR}}$ signal from the bus controller is low. Similarly, the address counter is decremented by 1 if the $\overline{\text{DEC ADDR}}$ signal is low.

To allow for both 16K and 64K memory address spaces, U68 is used as a programmable inverter; when the MSB1 strap is out, U68, Pin 8 is inverted from U47, Pin 7 and U68, Pin 6 is inverted from U47, Pin 6.

The DRIVE signal from the bus controller enables U54 through U57, allowing the value of the address counter to be presented on $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR15}}$. If DRIVE is low, the outputs of U54 through U57 are in a high-impedance state.

3.3 INTERRUPT LOGIC.

3.3.1 This logic recognizes the presence of an EOP code in the data path and handshake block. The PCA may be configured to interrupt when this occurs.

3.3.2 When the REOP signal from the data path and handshake block is high, U31, Pin 6 goes low. If the INT strap is in, then the $\overline{\text{ATN}}$ line is pulled low, indicating an interrupt condition to the terminal processor. Similarly, if the INT2 strap is in, then the $\overline{\text{ATN2}}$ line is pulled low, indicating an interrupt condition. The interrupt condition is cleared only when a different code replaces the EOP code in the data path and handshake block.

If REOP is high and $\overline{\text{REQ}}$, $\overline{\text{I/O}}$, $\overline{\text{WRITE}}$, and $\overline{\text{POLL}}$ are all pulled low by the terminal processor (to determine the source of an interrupt), then U31, Pin 3 goes low, and $\overline{\text{BUS0}}$ through $\overline{\text{BUS6}}$ are pulled low if straps PL0 through PL6 are in, respectively; only one of these straps should be inserted at any time.

3.4 DATA PATH AND HANDSHAKE.

3.4.1 This block is responsible for routing data between the external CPU, the terminal processor, and the display memory. Logic is provided to perform a bi-directional two-wire handshake between the external CPU and the PCA. Finally, a "self-test" facility is provided to form a data path between the terminal processor and the display memory through the PCA.

3.4.2 This block is divided for purposes of description into data path, handshake without test, and handshake with test sections.

3.4.2.1 Data Path. Output from the terminal processor on signals $\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$ is clocked into U58 and U59 by the LATCH DATA signal from the handshake section. This data is presented continuously to the external CPU on the output lines $\overline{\text{DUUT0}}$ through $\overline{\text{DUUT7}}$ connected to U410 and U510. The data sent from the external CPU to the terminal on lines

DIN0 through DIN7 is inverted by U210 and U310 to provide high-true signals to multiplexors U48 and U49. If the TEST signal is high, then D0 through D7 are selected (data from the terminal processor); otherwise DIN0 through DIN7 are selected (data from the external CPU).

At this point, L0 through L7 are examined by a comparator composed of U69, U51, and U38. If the code represented by L0 through L7 is a carriage return (15 octal), then the signal CR is high (U28, Pin 8). If the code represented by L0 through L7 is a line feed (12 octal), then the signal LF is high (U28, Pin 12). If LF is high, L7, L6, L2, and L1 will be inverted by U39. This causes the input to U26 and U27 to change from a line feed (12 octal) to an EOL code (314 octal). If the CRLF strap is inserted, then the CR and LF signals remain low and no conversion takes place.

L0, M1 and M2, L3 through L5, M6, and M7 are clocked into U26 and U27 by the handshake section. U18, U310, Pin 6, and U25 form a comparator. If the code in the flip-flops U26 and U27 is a home-up code

then the signal HOME UP (U25, Pin 4) is low. If the code is backspace then U25, Pin 3 will be low. If either a home-up or backspace code is present then HU+BS (U21, Pin 3) will be high. If the code is an EOP then the REOP signal (U68, Pin 11) will be high. The INH strap forces the HU+BS signal low if it is inserted, irrespective of the code that is present.

If EOP is high, the outputs of U26 and U27 are selected by multiplexors U36 and U37; otherwise, an EOP code is forced on the 1A through 4A inputs of U36 and U37. The final code is presented to the terminal

bus by the signals BUS0 through BUS7 when the DRIVE signal is high.

3.4.2.2 Handshake Without Test. The following presentation assumes that U19, Pin 4 is high, i.e., TEST is false (low). This module is selected by

the terminal processor when ADDR4,9 are high and ADDR10, ADDR11, REQ,

and I/O are low.

Transfer of data from terminal processor to external CPU.

The processor must first determine if a previous transfer from the terminal to the CPU is still being processed by performing a status

request. Status is requested by leaving WRITE and ADDR5 high and

pulling $\overline{\text{ADDR6}}$ while selecting this module. This causes decoder U43, Pin 10 to go low and U31, Pin 9 to go high. If either DORI (U28, Pin 4) or U310, Pin 8 are high, then $\overline{\text{BUSO}}$ (U31, Pin 8) will be low, indicating that a previous output handshake has not been completed. The processor must wait until $\overline{\text{BUSO}}$ goes high before sending the next data byte to this module for output.

To transfer data to this module for output to the CPU the processor holds $\overline{\text{ADDR5,6}}$ and $\overline{\text{WRITE}}$ low while selecting this module. This sets, U43, Pin 15 low and LATCH DATA (U33, Pin 12) high, causing processor data to be clocked into U58 and U59, and a low pulse of one state time to appear at U51, Pin 11 after $\overline{\text{REQ}}$ goes high. This pulse causes U19, Pin 9 to go low and, since TEST is low, $\overline{\text{DOR}}$ (U610, Pin 3) goes low, initiating the handshake and informing the CPU that data is ready to be read from the terminal. The CPU acknowledges receipt of the data by setting $\overline{\text{DOA}}$ low, U28, Pin 2 goes low, causing U19, Pin 9 to go high, U28, Pin 4 goes low, and U610, Pin 3 goes low, completing the handshake.

Transfer of data from external CPU to the display memory.

The CPU sets $\overline{\text{DIR}}$ low to indicate data is ready to be read into the terminal. This initiates the input handshake; U310, Pin 12 goes nigh and four state-times later (800 nanoseconds) U41, Pin 3 goes high. Since U19, Pin 4 is high, U29, Pin 11 goes low, U29, Pin 6 goes high and the handshake does not proceed further until the NEW DATA OK signal from the bus controller goes high. When this occurs, U29, Pin 8 goes low, causing U28, Pin 10 to go high, clocking the data into U26 and U27. When U28, Pin 10 goes high U52 and U51 generate a low-level pulse for one state time at U51, Pin 3 causing DATA RDY to go high to the bus controller if CR is low (i.e., the bus controller does not process carriage return codes). Also, a half state-time pulse at U42, Pin 8 causes U19, Pin 9 to go high. Finally, U19, Pin 13 goes high, causing $\overline{\text{DIA}}$ (U610, Pin 6) to go low to acknowledge the receipt of the data to the external CPU.

When $\overline{DIR}$ returns to a high state, U41, Pin 3 immediately goes low causing U29, Pin 11 to go high and U29, Pin 6 to go low. This causes U19, Pin 13 to go low, $\overline{DIA}$ (U610, Pin 6) goes high, and the handshake is completed.

Entering the self-test mode.

To enter the self-test mode, the processor selects this module with $\overline{ADDR6}$ and $\overline{WRITE}$ high and $\overline{ADDR5}$ low. This sets U43, Pin 9 low and U19, Pin 4 low, causing the TEST signal (U28, Pin 6) to go high.

3.4.2.3 Handshake With Test. The following presentation assumes that U19, Pin 4 is low, i.e., TEST is true (high).

Transfer of data from the terminal processor to the display memory.

When the processor drives the bus signals so that U43, Pin 15 goes low, then LATCH DATA (U33, Pin 12) goes high and DORI (U28, Pin 4) goes high (see the analysis in section 3.4.2.2 for transfer from the processor to CPU). Since TEST is high, $\overline{DOR}$ does not change its level (no handshake with the external CPU occurs) and U29, Pin 3 goes low, and U29, Pin 6 goes high. When NEW DATA OK goes high, U29, Pin 8 goes low, U28, Pin 10 goes high, clocking U26 and U27 and initiating a one state-time pulse on U51, Pin 3. This low pulse will cause DATA RDY to go high if CR is low and the half state-time pulse generated at U42, Pin 8 will cause U19, Pin 9 to go high and DORI to go low. Then U29, Pin 3 goes high, U29, Pin 6 goes low, U29, Pin 8 goes high and the internal handshake is completed. Since TEST is high, U29, Pin 11 and $\overline{DIA}$ (U610, Pin 6) are forced high, inhibiting any handshake with the external CPU.

Leaving the self-test mode.

To leave the self-test mode the module is selected with $\overline{WRITE}$ and $\overline{ADDR5,6}$ high. This sets U43, Pin 7 low and U19, Pin 4 high, causing the TEST signal (U28, Pin 6) to go low.

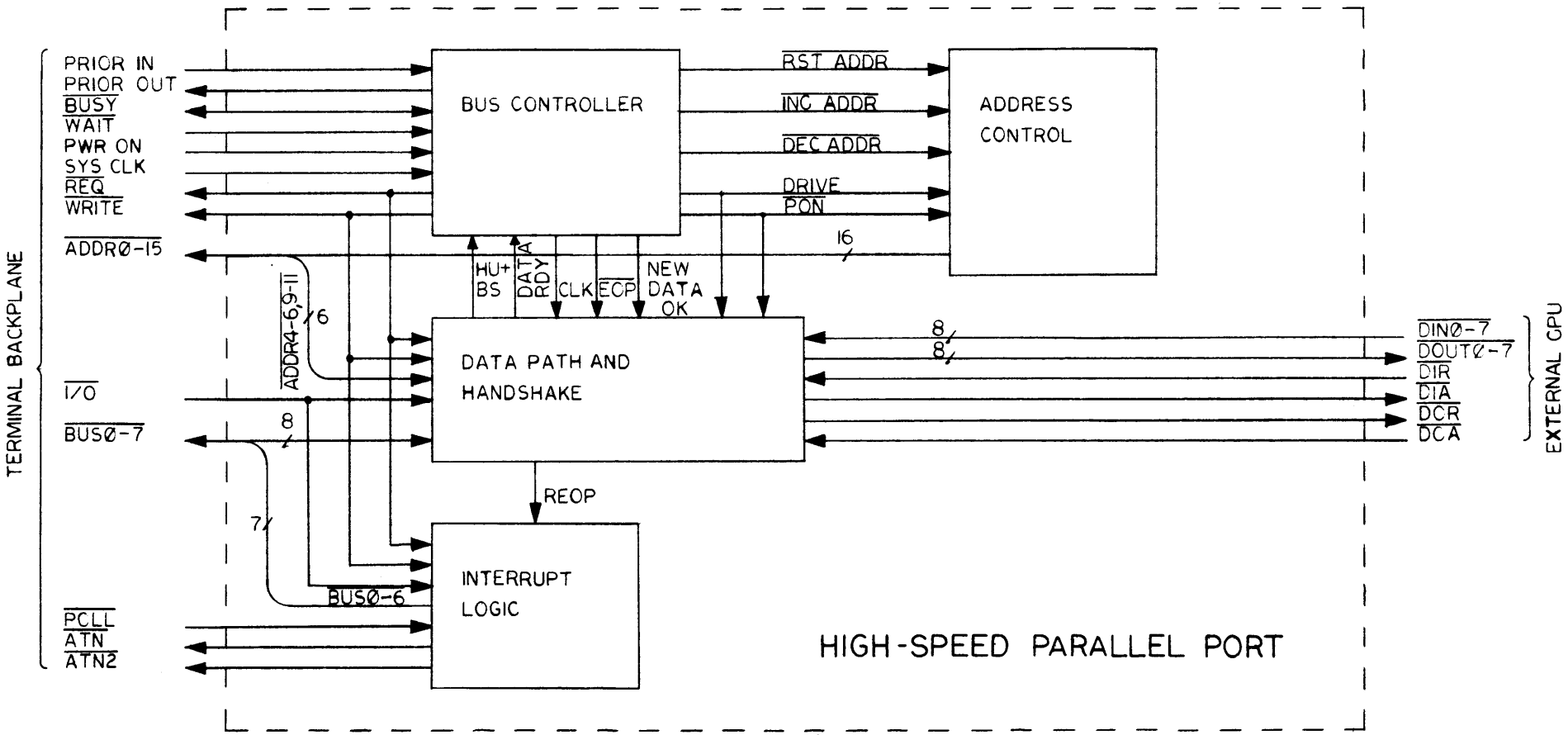

Figure 1
High-Speed Parallel Port Block Diagram
AUG-01-76 **13255-91146**

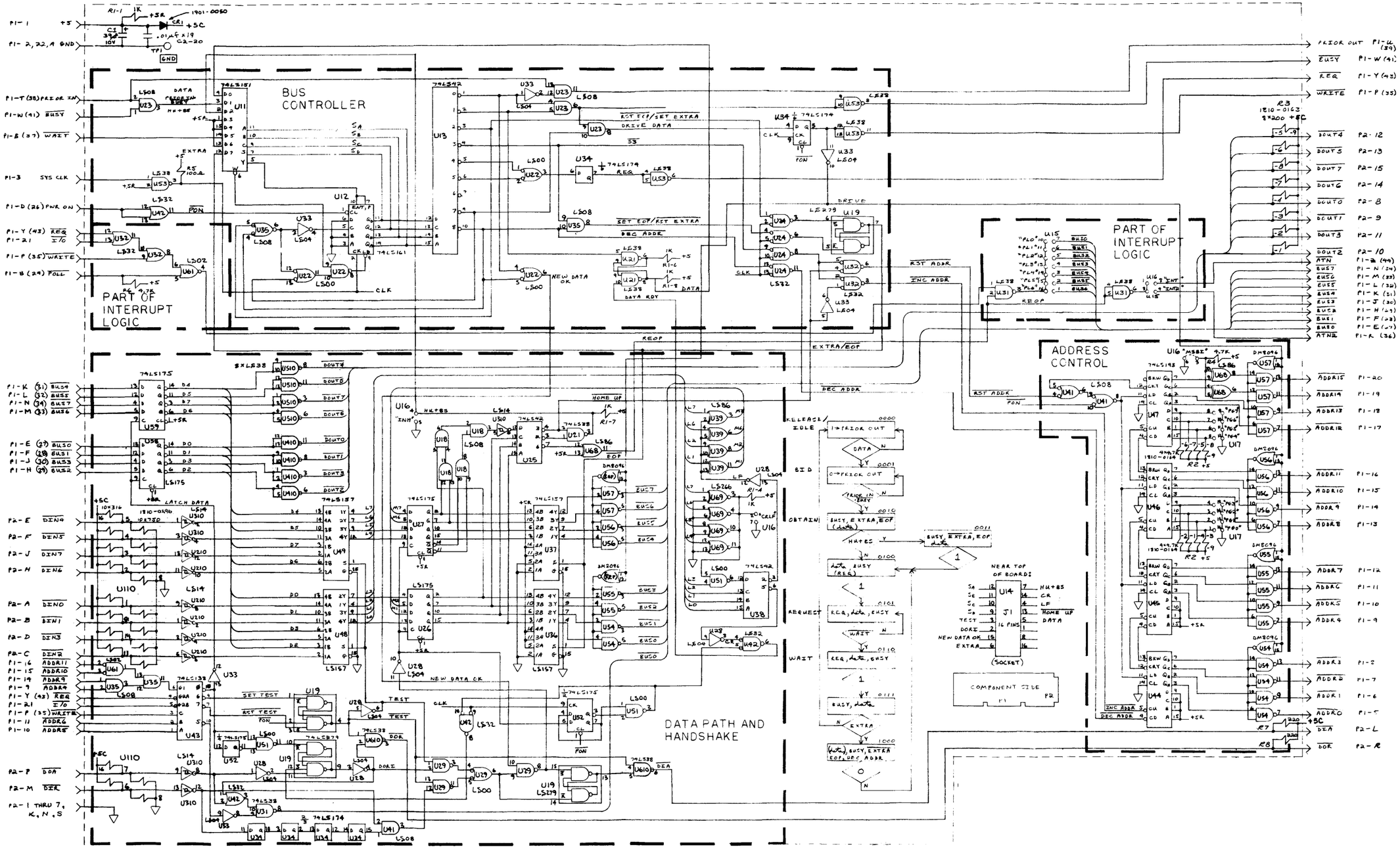

Figure 2
High-Speed Parallel Port PCA Schematic Diagram
AUG-01-76 **13255-91146**

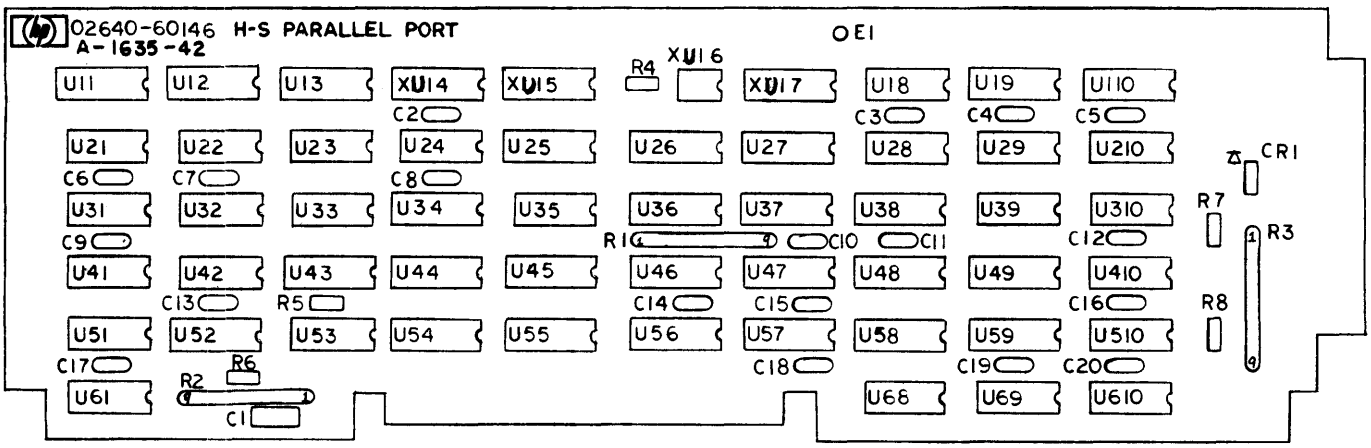

Figure 3
High-Speed Parallel Port PCA
Component Location Diagram
AUG-01-76 13255-91146

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60146	1	HIGH SPEED PARALLEL PORT ASSEMBLY DATE CODE: A-1635-42 REVISION DATE: 10-23-76		
C1	0180-0393	1	CAP 39UF 10V		
C2	0160-2055	19	CAP .01UF		
C3	0160-2055		CAP .01UF		
C4	0160-2055		CAP .01UF		
C5	0160-2055		CAP .01UF		
C6	0160-2055		CAP .01UF		
C7	0160-2055		CAP .01UF		
C8	0160-2055		CAP .01UF		
C9	0160-2055		CAP .01UF		
C10	0160-2055		CAP .01UF		
C11	0160-2055		CAP .01UF		
C12	0160-2055		CAP .01UF		
C13	0160-2055		CAP .01UF		
C14	0160-2055		CAP .01UF		
C15	0160-2055		CAP .01UF		
C16	0160-2055		CAP .01UF		
C17	0160-2055		CAP .01UF		
C18	0160-2055		CAP .01UF		
C19	0160-2055		CAP .01UF		
C20	0160-2055		CAP .01UF		
CR1	1901-0050	1	DIODE-SILICON		
R1	1810-0164	1	NETWORK-RES DIP		
R2	1810-0121	1	RES NET 8 X 1K		
R3	1810-0163	1	RES NET 8 X 200		
R4	0683-4725	2	RES 4700 5% .25		
R5	0683-1015	1	RES 100 5% .25		
R6	0683-4725		RES 4700 5% .25		
R7	0683-2215	2	RES 220 5% .25		
R8	0683-2215		RES 220 5% .25		
U11	1820-1217	1	IC SN74LS151N		
U12	1820-1818	1	IC DIG 74LS161		
U13	1820-1418	3	IC SN74LS42N		
U18	1820-1201	4	IC SN74LS08N		
U19	1820-1440	1	IC SN74LS279N		
U21	1820-1209	6	IC SN74LS38N		
U22	1820-1197	3	IC SN74LS00N		
U23	1820-1201		IC SN74LS08N		
U24	1820-1208	3	IC SN74LS32N		
U25	1820-1418		IC SN74LS42N		
U26	1820-1195	5	IC SN74LS175N		
U27	1820-1195		IC SN74LS175N		
U28	1820-1199	2	IC SN74LS04N		
U29	1820-1197		IC SN74LS00N		
U31	1820-1209		IC SN74LS38N		
U32	1820-1208		IC SN74LS32N		
U33	1820-1199		IC SN74LS04N		
U34	1820-1196	1	IC SN74LS174N		
U35	1820-1201		IC SN74LS08N		
U36	1820-1470	4	IC SN74LS157N		
U37	1820-1470		IC SN74LS157N		
U38	1820-1418		IC SN74LS42N		
U39	1820-1211	2	IC SN74LS86N		
U41	1820-1201		IC SN74LS08N		
U42	1820-1208		IC SN74LS32N		
U43	1820-1216	1	IC SN74LS138N		
U44	1820-1194	4	IC SN74LS193N		
U45	1820-1194		IC SN74LS193N		
U46	1820-1194		IC SN74LS193N		
U47	1820-1194		IC SN74LS193N		
U48	1820-1470		IC SN74LS157N		
U49	1820-1470		IC SN74LS157N		
U51	1820-1197		IC SN74LS00N		
U52	1820-1195		IC SN74LS175N		
U53	1820-1209		IC SN74LS38N		
U54	1820-1368	4	IC DM8096N		
U55	1820-1368		IC DM8096N		
U56	1820-1368		IC DM8096N		
U57	1820-1368		IC DM8096N		
U58	1820-1195		IC SN74LS175N		
U59	1820-1195		IC SN74LS175N		
U61	1820-1144	1	IC SN74LS02N		
U68	1820-1211		IC SN74LS86N		
U69	1820-1297	1	IC SN74LS266N		
U110	1810-0296	1	RES PACK-DIP		
U210	1820-1416	2	IC SN74LS14N		
U310	1820-1416		IC SN74LS14N		
U410	1820-1209		IC SN74LS38N		
U510	1820-1209		IC SN74LS38N		
U610	1820-1209		IC SN74LS38N		
XU14	1200-0482	3	SOCKET 16 DIP LO		
XU15	1200-0482		SOCKET 16 DIP LO		
XU16	1200-0455	1	SOCKET 8 DIP LO		
XU17	1200-0482		SOCKET 16 DIP LO		
TP1	0360-0124	1	STUD SOLDER TERM		