HP 13255

EXTENDED CTU INTERFACE MODULE

Manual Part No. 13255-91137

PRINTED

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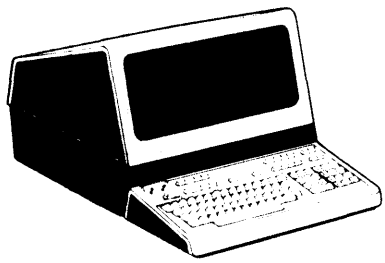
DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

The Extended CTU Interface Module is used with a Read/Write PCA, a CTU Top Plane Assembly, two CTU Transport Assemblies, and one or more mini tape cartridges. The detailed description and material lists for these are contained in module section 13255-91032.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Extended CTU Interface Module is contained in tables 1.0 through 5.3.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60137	CTU Interface PCA	12.5 x 4.0 x 0.5	0.40

Number of Backplane Slots Required: 1

1.0 INTRODUCTION.

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02640-60137	CTU Interface PCA	12.5 x 4.0 x 0.5	0.40
Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 0.823 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 800 mA	@ mA	@ mA	@ mA
	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 4.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V	$\overline{\text{PROC ACTIVE}}$	Negative True, Processor Active (Controlling Bus)
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X	RUN	Allow Processor to Access Bus
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Data Comm Interrupt Request

Table 4.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1 thru -22		} Not Used
P3, Pin A	$\overline{LO}$	Negative True, Lamp Unit 0
-B	$\overline{HOL0}$	Negative True, Hole Unit 0 Detected
-C	$\overline{L1}$	Negative True, Lamp Unit 1
-D	$\overline{HOL1}$	Negative True, Hole Unit 1 Detected
-E	+5V	+5V Supply
-F	$\overline{RE}$	Negative True, Record Enable (Read Enable)
-H	US0	Unit Select 0 (select left unit)
-J	$\overline{DATA}$	Negative True, write Data (high writes flux in north seeking pole direction)
-K	2XTACH	Two Times Tachometer Frequency
-L	RUNG	Running (>1 ips forward or reverse)
-M	TACH	Tachometer Frequency
-N	DZX	Data Zero Crossing (testing purposes only)
-P	GAP	Gap Detector
-R	CIN0	Cartridge Inserted in Unit 0
-S	CIN1	Cartridge Inserted in Unit 1
-T	RIP	Record In Progress
-U	$\overline{DZX}$	Negative True, Data Zero Crossing
-V	$\overline{STOP}$	Obsolete (tied to +5V thru 4.7 kilohms)
-W	$\overline{FFD}$	Negative True, Fast Forward
-X	$\overline{SFD}$	Negative True, Slow Forward
-Y	$\overline{FREV}$	Negative True, Fast Reverse
-Z	$\overline{SREV}$	Negative True, Slow Reverse

Table 5.0 Module Bus Pin Assignments

Function Performed: Read Data From CTU

Poll Bit: Bit 7

Module Address: (ADDR 11,10,9,4) = (1011)

Function Specifier: ADDR5 = 1

Data Bus Bit Interpretation:

B7 Data Bit 7
(Most significant bit of data)

B6 Data Bit 6

B5 Data Bit 5

B4 Data Bit 4

B3 Data Bit 3

B2 Data Bit 2

B1 Data Bit 1

B0 Data Bit 0
(Least significant bit of data)

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
1	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 5.1 Module Bus Pin Assignments

Function Performed: Write Data To CTU

Poll Bit: Bit 7

Module Address: (ADDR 11,10,9,4) = (1011)

Function Specifier: ADDR5 = 1

Data Bus Bit Interpretation:

B7 Data Bit 7
(Most significant bit of data)

B6 Data Bit 6

B5 Data Bit 5

B4 Data Bit 4

B3 Data Bit 3

B2 Data Bit 2

B1 Data Bit 1

B0 Data Bit 0
(Least significant bit of data)

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
1	ADDR 11
0	ADDR 10
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 5.2 Module Bus Pin Assignments

Function performed: Input Status From CTU

Poll Bit: Bit 7

Module Address: (ADDR 11,10,9,4) = (1011)

Function Specifier: ADDR5 = 0

Data Bus Bit Interpretation:

B7 - TKI is set when a TAK status (B3) 0-to-1 transition occurs. It is cleared when status is read.

B6 - BYTE RDY is set when a byte is ready or when preamble is detected (in Read mode), or when a new byte can be accepted (in Record mode).

B5 - GAP is the output of the gap detector on the Read/Write PCA (high when Gap is present).

B4 - HOLE indicates a hole is present, or a hole interrupt is present. It is cleared when a hole is absent and status is read.

B3 - TAK is the frequency of the tachometer divided by 2. There are 58.4 transitions of the TAK status per inch of tape movement.

B2 - RIP indicates the presence of head current while recording a gap. The state of this signal is not defined during read operations or while data is being recorded.
0 = No write current (tape protected)
1 = Write current present while in gap

B1 - CIR indicates that a cartridge is inserted in the right CTU Transport Assembly and is cleared when the cartridge is removed.
0 = No cartridge in right CTU Transport Assembly
1 = Cartridge inserted in right CTU Transport Assembly

B0 - CIL indicates that a cartridge is inserted in the left CTU Transport Assembly and is cleared when the cartridge is removed.
0 = No cartridge in left CTU Transport Assembly
1 = Cartridge inserted in left CTU Transport Assembly

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
1	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 5.3 Module Bus Pin Assignments

Function Performed: Output Command to CTU	Value	Bus Signal
	X	ADDR 15
Poll Bit: Bit 7	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (1011)	X	ADDR 12
	1	ADDR 11
	0	ADDR 10
	1	ADDR 9
Function Specifier: ADDR5 = 0	X	ADDR 8
	X	ADDR 7
	X	ADDR 6
Data Bus Bit Interpretation:	0	ADDR 5
	1	ADDR 4
B7 - ANL	X	ADDR 3
0 = Turns off the left eject button light	X	ADDR 2
1 = Turns on the left eject button light	X	ADDR 1
	X	ADDR 0
B6 - ANR	B7	BUS 7
0 = Turns off the right eject button light	B6	BUS 6
1 = Turns on the right eject button light	B5	BUS 5
	B4	BUS 4
B5 - GEN	B3	BUS 3
0 = Disables gap recording	B2	BUS 2
1 = Record gap on tape (Bit 3 must also be 1)	B1	BUS 1
	B0	BUS 0
B4 - USL	1=Logical 1=Bus Low	
0 = Route command to right drive	0=Logical 0=Bus High	
1 = Route command to left drive	X=Don't Care	
B3 - REC		
0 = Read mode		
1 = Record mode (enable write circuit)		
B2 - FST		
0 = Run tape at slow speed (10 ips)		
1 = Run tape at high speed (60 ips)		
B1 - FWD		
0 = Forward		
1 = Reverse		
B0 - RUN		
0 = Stop tape		
1 = Move tape according to FST and FWD		

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts list (02640-60137) located in the appendix.

The terminal processor communicates with the Extended CTU Interface Module via the terminal bus (Backplane Assembly). The Extended CTU Interface Module is responsible for converting processor commands into signals to control tape motion, unit selection, read or write operation, and the state of the eject button lights. The Extended CTU Interface Module provides status information allowing the processor to determine the present state of the selected CTU Transport Assembly. Finally, the Extended CTU Interface Module encodes data bytes into serial patterns of bit transitions to be recorded on the tape and vice versa (i.e., decodes bit transitions on the tape into data bytes).

3.1 BUS FUNCTION DECODER AND TIMING LOGIC.

3.1.1 The bus function decoder and timing logic generates signals based upon inputs from the terminal bus which control the flow of commands, status, and data bytes to and from the terminal bus.

3.1.2 The bus function decoder (U45) generates one of four command signals by decoding $\overline{\text{WRITE}}$ and $\overline{\text{ADDR5}}$. The commands are enabled by $\overline{\text{I/O}}$ (for an I/O module), $\overline{\text{REQ}}$ (bus data is valid), $\overline{\text{ADDR4}}$, $\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, and $\overline{\text{ADDR9}}$. In addition, DATA CLOCK, RD+WRT, RD/WRT SELECT, READ EN, STATUS EN, and CMMD CLK are generated.

3.2 COMMAND LOGIC.

3.2.1 The purpose of the command logic is to acquire command information from the terminal bus when the signals are valid. The command information completely specifies the operation as well as the selection of the CTU Transport Assemblies. In addition, when a hole is detected by the hole detect logic, the command logic stops tape motion thus preventing tape runoff.

3.2.2 The command signals from the terminal bus are latched into U35, U23, (Pin 2 and Pin 12), and U22 by the CMND CLK signal from the bus function decoder and timing logic.

Two versions of the Run command are contained in the command register (U23). SRUN (Servo Run) is generated at U23, Pin 5 to enable the tape motion decoder (U45). SRUN is cleared if the hole edge detector (U36, Pin 12) detects a transition into a hole. IRUN (Interface Run) is generated at U23, Pin 9 to enable the slow forward tape motion decoder at U36, Pin 6 which generates $\overline{\text{ISF}}$ (used only by the encoder/decoder logic). This prevents a discontinuity in encoded or decoded data when moving across a hole. Both SRUN and IRUN are cleared after a system reset.

The $\overline{\text{SRUN}}$, $\overline{\text{FORWARD}}$, and $\overline{\text{FAST}}$ signals are translated in this block into the signals $\overline{\text{SREV}}$ (slow reverse), $\overline{\text{SFD}}$ (slow forward), $\overline{\text{FREV}}$ (fast reverse), and $\overline{\text{FFD}}$ (fast forward) which are used by the servo electronics on the Read/Write PCA.

The CLRINT signal is generated for the interrupt logic by U51, Pin 3 when the processor performs a status request, enabling the STATUS EN signal. The CLRINT signal is present for one cycle of SYS CLK after STATUS EN goes low.

3.3 DATA PATH CONTROL.

3.3.1 The data path control circuitry transfers data to and from the terminal bus. It also converts serial bits read from the tape into bytes and converts bytes from the terminal bus into serial bits for recording on the tape.

3.3.2 The data I/O buffer (U32 and U33) is an 8-bit register with a 2-port input multiplexer. It provides one byte of buffering between the terminal bus and the serial data register.

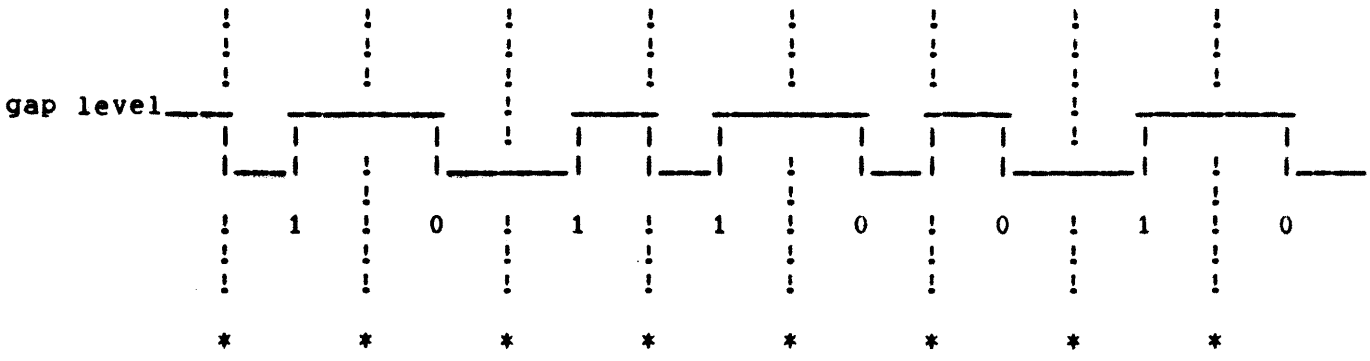
3.3.3 In Record mode, the data is loaded into the data I/O buffer from the terminal bus, enabled by RD/WRT SELECT being low. (Note that the data buffer is loaded with complement data since it is loaded from the

ground true terminal bus.) The data byte is loaded into the serial data register after the previous byte has been encoded. The serial data register is then shifted right (via $\overline{\text{REC DATA}}$) into the encoder at mid cell point (data transition position) and the encoder is complemented at end cell point (phase position).

3.3.4 In Read mode, the serial biphase data is read into the transition detector (U11, Pin 14) of the encoder/decoder logic and shifted into the serial data register at the appropriate time (corresponding to the zone for data transitions). When the last data bit has been detected at the decoder (there are 7 bits in the serial data register), the data I/O buffer is parallel loaded from the serial data register (shifted right one bit). The data I/O buffer is subsequently output to the terminal bus via drivers U41 and U44.

3.4 ENCODER/DECODER LOGIC.

3.4.1 This logic provides the timing and control functions for encoding or decoding a data byte. The operation of the encoder/decoder logic is based upon the following theoretical analysis. The code that is recorded on the cartridge tape is Serial Biphase Mark Code (see below). Therefore, the code shown below would be seen at the encoder output (U110, Pin 10) when in Record mode or at the transition detector (U11, Pin 15) in Read mode. The code rules state that there is always a data transition at mid cell (a 1-bit is a transition towards gap level while a 0-bit is a transition away from gap level), and a phase transition occurs at a cell boundary if adjacent data transitions are the same.



*Indicates cell boundaries (125 microseconds)

3.4.2 Timing and control for the encode and decode operations is provided by a cell decode counter (U210) and a variable modulus (divide by N) counter (U510, U410, U49, and U59) which are both synchronous with the bus System Clock. The variable modulus counter generates a carry output at time intervals equal to one biphase cell period divided by eight which increments the cell decode counter. By initializing both counters at the beginning of a biphase cell, timing points (for encoding phase and data transitions in Record mode) and timing zones (for decoding phase and data transitions in Read mode) can be decoded from the cell decode counter and variable modulus counter carry output.

The variable modulus counter consists of two counters. One is an 8-bit counter (U510 and U410) which counts from a base state to the overflow state (which generates a carry output); the second is an 8-bit up-down counter which contains the value of the base state. The up-down counter is loaded with the two's complement of the desired modulus. In Record mode, the up-down counter is reset (U49, Pin 11 and U59, Pin 11) to the two's complement of 115 octal (77 decimal) giving a carry output at

$$\frac{N}{4.9150}\ \text{microsecond} = \frac{77}{4.9150}\ \text{microsecond} = \frac{\text{nominal biphase cell period}}{8}$$

In Read mode, the up-down counter is initialized to the same value. Then, based on the actual frequency of the phase/data transitions, the up-down counter is incremented or decremented. (Note that incrementing the up-down counter decrements the modulus of the counter.)

The cell decode counter is decoded as follows when in Record mode.

U210, Pins					
A	B	C	D	CIN	FUNCTION
1	0	0	1	1	Phase Position
1	1	0	1	1	Data Position

When in Read mode, the cell decode counter appears as follows.

	U210, Pins A	B	C	D	FUNCTION
Initialize State	0	1	1	0	Illegal Zone
	0	1	1	1	For Transitions
Decrement	1	0	0	0	
N	1	0	0	1	Zone For Phase
Increment	1	0	1	0	Transitions
N	1	0	1	1	
Decrement	1	1	0	0	
N	1	1	0	1	Zone For Data
Increment	1	1	1	0	Transitions
N	1	1	1	1	

3.4.3 The encoder operation can be best explained by considering the recording of a gap and a 2-byte preamble. The preamble consists of a zero byte and a byte with the value 200 octal.

First, the command RUN.FORWARD.RECORD.GAP is output to the command register from the processor. This sets the encoder to record flux in the gap direction. Additionally, the command sets the modulus of the variable modulus counter to 77 and enables the preset signals of the variable modulus, bit, and cell decode counters. while the gap is being recorded, the serial data register is shifted right for each bit time. Since $\overline{DZX}$ is high when in record mode, this results in the serial data register being loaded serially with all 1's. Because the data register contains the complement data, the register is effectively loaded with the first preamble byte (all zeroes).

After the proper gap interval has been recorded, the GAP command is turned off and the second preamble byte is loaded into the data I/O buffer. When $\overline{REC\ GAP}$ is set, the preset signals on the variable modulus, bit, and cell decode counters are removed and the encoder is no longer forced to record in the gap direction.

Each bit is recorded (encoded) as follows:

1) The variable modulus counter counts up and generates a carry output (CIN) every 77 system clocks. The carry output increments the cell decode counter.

2) The cell decode counter is decoded at end cell setting the encoder to the same value as $\overline{\text{DATA}}$ (the value of the rightmost bit of the serial data register), and the serial data register is shifted right one bit.

3) At mid cell, the bit counter increments, the encoder is complemented, and the cell decode and variable modulus counters are initialized.

The process is repeated for each of the eight data bits. After all eight bits have been encoded, the bit counter, cell decode counter, and the variable modulus counter are initialized. The serial data register is loaded from the data I/O buffer and BYTE RDY is set. If BYTE RDY signal is already set, then data is not loaded from the data I/O buffer and the same byte is recorded, shifted right one bit.

3.4.4 The decoder operation can be similarly explained by decoding a record consisting of a gap, a 4-byte preamble and a 1-byte record. First, the command RUN.SLOW.FORWARD is output to the command register from the processor. While the gap is being read, the gap detect circuitry on the Read/Write PCA causes the modulus of the variable modulus counter to be preset to 77, initializes the variable modulus and cell decode counters, and clears READ SYNC (U110, Pin 6).

When the preamble begins to be read, the gap detect circuitry indicates data present. This causes the preset to be removed from the modulus of the variable modulus counter which allows the modulus to be adjusted accordingly. The decoder then proceeds as follows-

The variable modulus counter counts up and generats CIN every N system clocks (N is initially 77). CIN increments the cell decode counter. When a transition is sensed by the $\overline{\text{DZX}}$ transition detector, it is decoded using the cell decode counter and results in one of three possible actions:

1) Transition occurs in the illegal zone--the cell decode and variable modulus counters are initialized. The process continues waiting for the next transition.

2) Transition occurs in the phase zone- the modulus of the variable modulus counter is incremented or decremented (see 3.4.2) and the cell decode and variable modulus counters are initialized. The process continues waiting for the next transition.

3) Transition occurs in the data zone- the modulus of the variable modulus counter is incremented or decremented (see 3.4.2) and the cell decode and variable modulus counters are initialized. If the data is decoded as a zero ("0"), the process continues waiting for the next transition. Otherwise, a one ("1") indicates the end of the preamble and causes READ SYNC and BYTE RDY to be set.

When READ SYNC is set, the decoder will automatically switch modes to read in data bytes. The initial BYTE RDY indicates that the end of the preamble has been found. BYTE RDY must be cleared by either a $\overline{\text{RD DATA}}$ or $\overline{\text{WR DATA}}$. However, the data byte read will be meaningless.

While reading in data, transitions detected are handled in the same manner as when reading the preamble except for transitions occuring in the data zone. In this case, RD DATA is shifted right into the serial data register and bit counter is incremented. when the last bit is decoded, the data I/O buffer is parallel loaded from the serial data register (shifted right one bit), BYTE RDY is set, and the process is repeated for the next byte. The data in the I/O buffer must be read (which clear BYTE RDY) before the next byte is decoded in order to avoid losing data.

3.5 HOLE LOGIC.

3.5.1 This circuitry detects the presence of a hole in the tape of either CTU Transport Assembly (depending on which transport is selected) and generates the DHOL and DHOL DET signals.

3.5.2 The Read/Write PCA provides the signals $\overline{\text{HOL0}}$ and $\overline{\text{HOL1}}$ that indicate the presence of a hole on Unit 0 or Unit 1, respectively when the signal is low. When Unit 1 is selected and a hole is detected U47, Pin 6 will be low. When Unit 0 is selected and a hole is detected U43, Pin 3 will be low. Pins 3 and 6 of U47 are ORed into U11, Pin 6 where they are synchronized to SYS CLK and provide the DHOL signal at U11, Pin 7. DHOL at U11, Pin 7 is exclusive-ORed with DHOL delayed by one cycle of

SYS CLK at U11, Pin 10 and generates the DHOL DET signal which provides a pulse when a hole is initially detected and another pulse when it is no longer detected. It should be noted that DHOL and DHOL DET are ANDed in the command logic to provide a single pulse when a hole is initially detected.

3.6 TACH LOGIC.

3.6.1 The tach logic divides the TACH signal from the Read/Write PCA by a factor of two and uses the resulting signal to generate the signals TACH/2 and DTACH/2.

3.6.2 The TACH signal is used as the clock input for U19, which is configured as a T flip-flop, and results in one transition of the signal at U19, Pin 6 for every two transitions of the TACH signal. U11 synchronizes the signal from U19, Pin 6 with the SYS CLK and generates the TACH/2

signal for the status drivers. The TACH/2 signal is delayed one cycle of SYS CLK by U11, Pin 2 and is then exclusive-ORed to produce DTACH/2 at U12, Pin 6. DTACH/2 produces a pulse at each transition of TACH/2 with a width equal to one cycle of SYS CLK. It should be noted that DTACH/2 is ANDed with U11, Pin 2 to provide a pulse on positive going DTACH/2 edges only.

3.7 STATUS DRIVERS.

3.7.1 The status drivers present status information for the module to the terminal bus.

3.7.2 The CIN0, CIN1, RIP, and TACH/2 signals are gated onto the terminal bus by U31 which is enabled by STATUS EN. The signals are inverted on the bus to provide ground true logic levels. The TACH, HOLE, GAP, and BYTE RDY signals are gated onto the terminal bus by U34 which is enabled by STATUS EN.

3.8 INTERRUPT LOGIC.

3.8.1 The interrupt logic provides an interrupt when a positive transition occurs in the TACH/2 signal, when transition into a hole occurs, or when a byte of data must be received or sent from the processor. The TACH and hole interrupts are cleared by a read status, BYTE RDY is cleared by READ or WRITE DATA.

3.8.2 The DTACH/2 signal sets flip-flop U21, causing Pin 10 to be high when a positive transition occurs in TACH/2. The CLRINT signal from the command logic resets U21, causing Pin 10 to go low. The DHOL signal sets flip-flop U21, causing Pin 6 to be high, and indicates the presence of a hole in the tape. The CLRINT signal resets U21, causing Pin 6 to go low. When U21, Pin 10 is high or U21, Pin 6 is high or BYTE RDY is high, or some combination of these events occurs, then INTERRUPT will be high. This causes $\overline{\text{ATN2}}$ to be low thereby indicating an interrupt condition to the processor. If U21, Pin 6 and Pin 10 are low and $\overline{\text{BYTE READY}}$ is high, then no interrupt condition exists and INTERRUPT will be low.

3.8.3 In response to an interrupt on $\overline{\text{ATN2}}$, the Extended CTU Interface Module is polled by $\overline{\text{POLL.REQ.I/O.WRITE}}$; if the interrupt initiated is from the Extended CTU Interface Module, then Bit 7 will be asserted and U46, Pin 6 will be low.

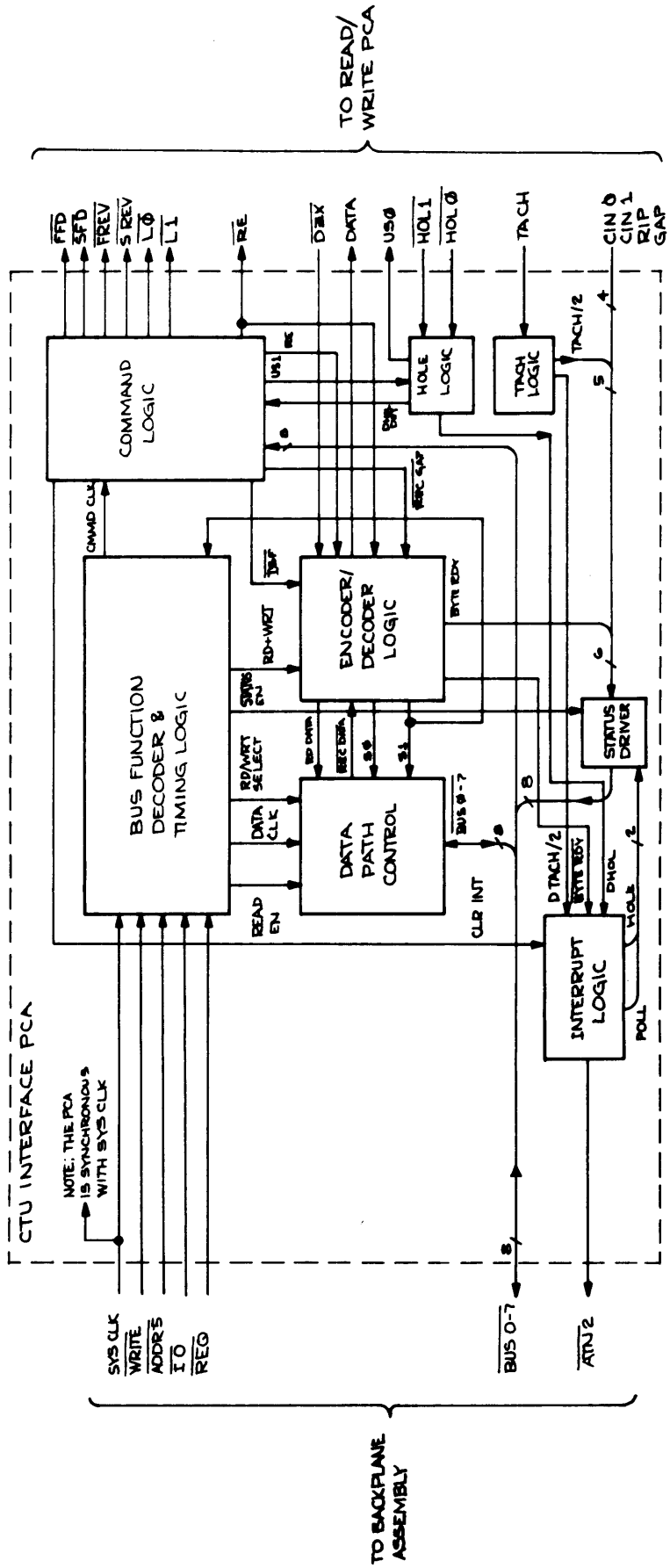


Figure 1
CTU Interface PCA Block Diagram
AUG-01-76 13255-91137

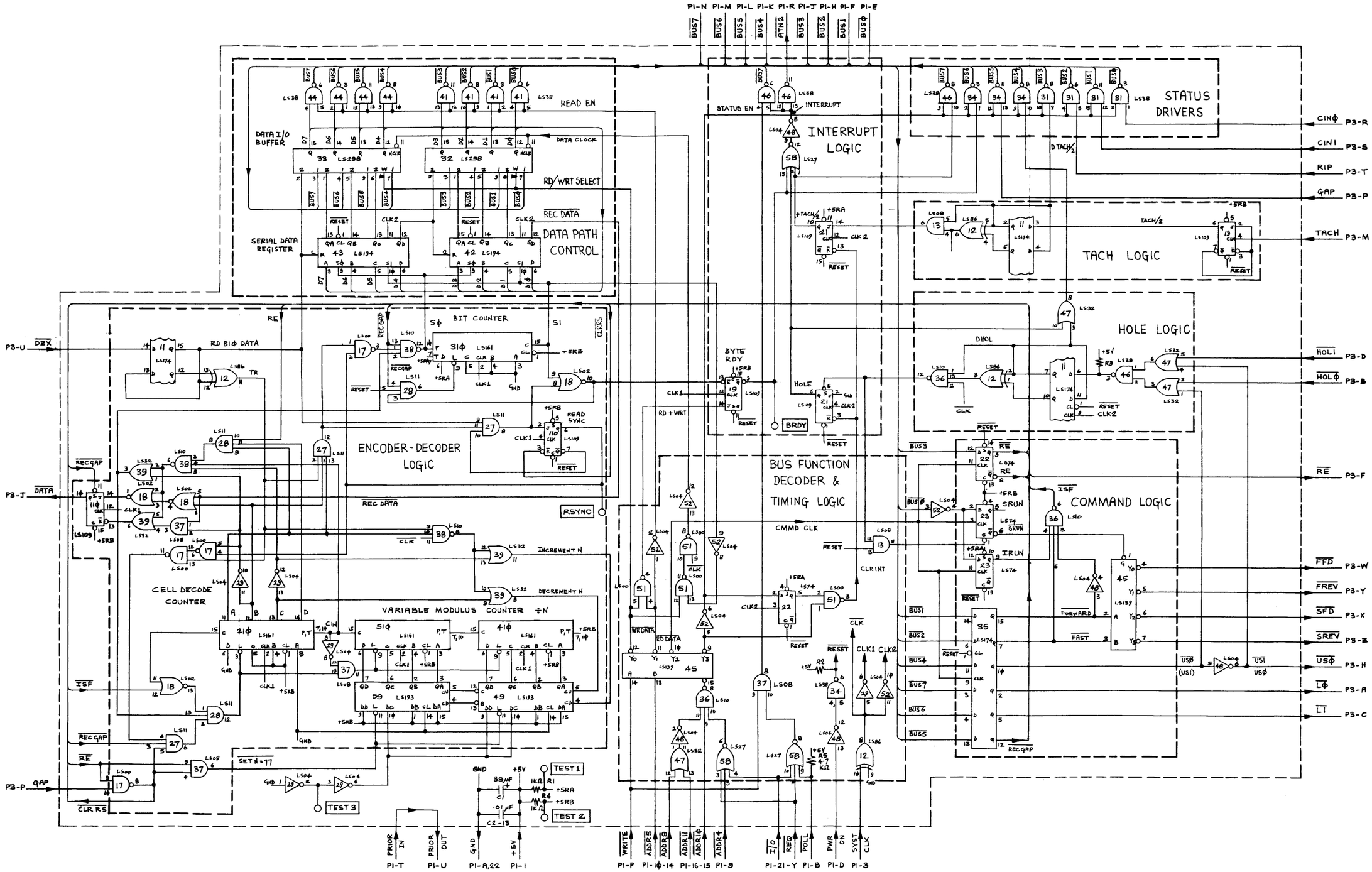


Figure 2
CTU Interface PCA Schematic Diagram
AUG-01-76 13255-91137

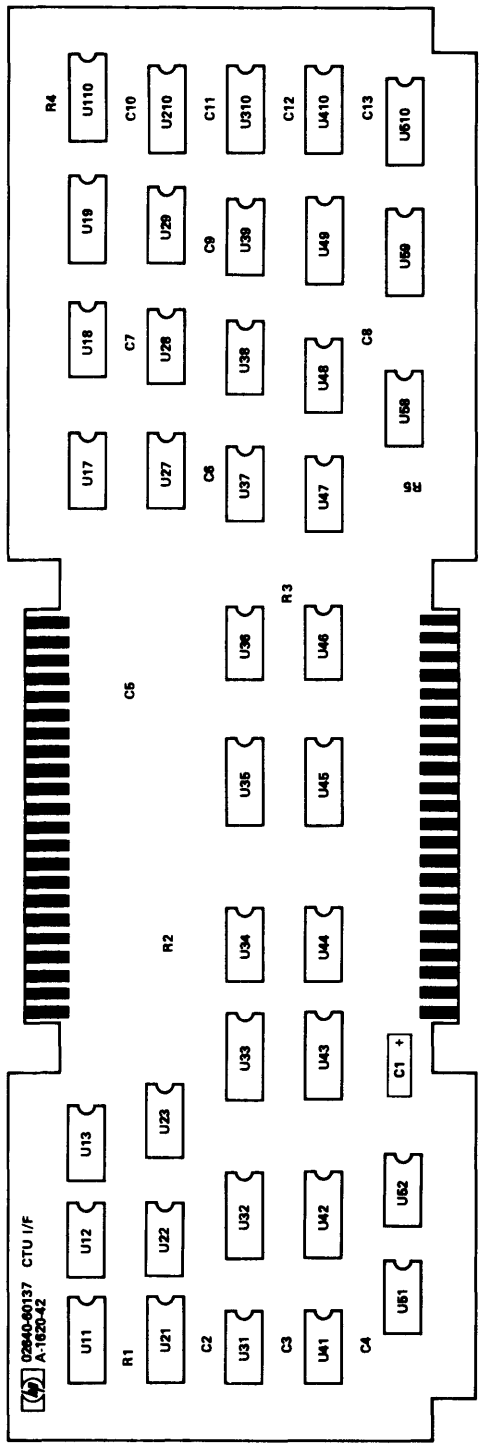


Figure 3
CTU Interface PCA Component Location Diagram
AUG-01-76 13255-91137

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60137	1	CTU INTERFACE ASSEMBLY DATE CODE: A-1620-42 REVISION DATE: 11-19-76	28480	02640-60137
C1	0160-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0160-2055	12	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C3	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	6	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E5	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E6	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	0683-1025	4	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R3	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
U11	1820-1196	2	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U12	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N
U13	1820-1201	2	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U17	1820-1197	2	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U18	1820-1144	1	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U19	1820-1282	3	IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
U21	1820-1282		IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
U22	1820-1112	2	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U23	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U27	1820-1203	2	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U28	1820-1203		IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U29	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U31	1820-1209	5	IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U32	1820-1100	2	IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U33	1820-1100		IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U34	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U35	1820-1196		IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U36	1820-1202	2	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U37	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U38	1820-1202		IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U39	1820-1208	2	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U41	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U42	1820-1276	2	IC-DIGITAL SN74LS194AN TTL LS R-S	01295	SN74LS194AN
U43	1820-1276		IC-DIGITAL SN74LS194AN TTL LS R-S	01295	SN74LS194AN
U44	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U45	1820-1281	1	IC-DIGITAL SN74LS139N TTL LS DUAL 2	01295	SN74LS139N
U46	1820-1209		IC-DIGITAL SN74LS38N TTL LS QUAD 2 NAND	01295	SN74LS38N
U47	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U48	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U49	1820-1194	2	IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
U51	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U52	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U56	1820-1206	1	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
U59	1820-1194		IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
U110	1820-1282		IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
U210	1820-0716	4	IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U310	1820-0716		IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U410	1820-0716		IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N
U510	1820-0716		IC-DIGITAL SN74161N TTL BIN SYNCHRO	01295	SN74161N