# OPERATING AND SERVICE MANUAL 

## PART 3

## 7970B/7970C

DIGITAL MAGNETIC TAPE UNIT

READ MODULES

Printed-Circuit Assemblies:
07970-60390, Series 1014
07970-60500, Series 1318
07970-62166, Series 1218
07970-62168, Series 1218
07970-62170, Series 1218
07970-62171, Series 1218
07970-62167, Series 1218
07970-60570, Series 1218
07970-62000, Series 1201
07970-62187, Series 1040

# SECTION I <br> DESCRIPTION 

## 1-1. INTRODUCTION.

1-2. This section describes the read modules of the HP 7970B/7970C Digital Magnetic Tape Units. A functional description and circuit description is also included to aid in servicing the read modules.

## 1-3. PHYSICAL DESCRIPTION.

1-4. The read modules consist of the read magnetic head assembly, a read preamplifier printed-circuit assembly, a read assembly and an optional density select assembly. The magnetic head assembly is a seven- or nine-track, read or read-while-write, NRZI head. Channel scrambling is accomplished in the head assembly wiring. From the reference edge of the tape (edge facing the operator) the nine-track channel designations are $5,7,3, P, 2,1,0,6$, and 4 . The seven-track channel designations are $7,6,5,4,3,2$, and $P$.

1-5. The read preamplifier is located near the head assembly. The preamplifier contains nine identical channels. Seven-track units do not use channels 0 and 1.

1-6. The read assembly consists of a card cage assembly (motherboard) that contains a read control printed-circuit assembly, a single-channel read data printed-circuit assembly and three or four dual-channel read data printed-circuit assemblies. Seven-track units will have three dual-channel read data printed-circuit assemblies and nine-track units will have four dual-channel printed-circuit assemblies.

1-7. The optional density select switch assembly allows the operator to select read densities of 200,556 or 800 cpi . The option consists of a three-button, interlocked switch assembly with indicators and a printed-circuit assembly that contains line-drivers. Units not equipped with the density select switch option are hard-wired to read data at a tape packing density of 800 cpi .

## 1-8. FUNCTIONAL DESCRIPTION.

1-9. Information to be read from the magnetic tape has been recorded in NRZI (non-return-to-zero-ones inverted) form, in seven or nine tracks. A "one" bit is represented by a flux reversal and a "zero" bit is represented by the absence of a flux reversal. The character bytes are recorded at a density of 200,556 , or 800 character bytes per inch (cpi).

1-10. As the tape moves across the read head, tracks that contain a flux reversal ("one" bit) generate an analog signal from the head. The coding of information on the tape is such that every byte contains a flux reversal in at least one of the tracks. All bits that make up a character byte may not
arrive at the head at the same time. The read data circuits detect the flux transitions in each track and produce a parallel digital output with all bits of the character byte presented simultaneously.

1-11. The recovery of the data is accomplished by generating a fixed-time window or character gate. Starting with the first detected flux reversal, all remaining bits must arrive during the character gate. At the end of the character gate time, a read strobe pulse samples the contents of all input registers, transfers the data to the output registers and conditions the input registers for the next data byte.

## 1-12. CIRCUIT DESCRIPTION.

1-13. Each of the seven- or nine-track low level analog outputs from the read head are independently amplified by an integrated-circuit preamplifier located on the preamplifier printed-circuit assembly. The gain of each preamplifier is adjustable.

1-14. The amplified analog signal representing data from the tape is processed by the read data circuits and the read control circuits. The following paragraphs describe the operation of these circuits. Figure 1-1 is a timing diagram showing the relationship of generated signals and data.

## 1-15. READ CONTROL CIRCUITS.

1-16. The read control circuits consist of a density select circuit, a read enable circuit, a threshold generator, a skew gate circuit, and a character gate generator. Figure 1-2 is a block diagram of the read control circuits.

1-17. The read enable circuit is controlled by commands from the tape unit control and status circuits. When the read enable circuit is satisfied, the Read Enable signal conditions the read data input and output registers. The Read Enable signal is also gated with the character gate generator output to provide the "not" Read Clock signal ( $\overline{\mathrm{RC}}$ ).

1-18. The threshold generator circuit establishes the bias level for the threshold circuits of the read data circuits. Two threshold levels are used. When reading tape previously recorded, the threshold is 22 percent of the nominal peak amplitude. When reading data that has just been written by the write head (read-while-write), the threshold is increased to 40 percent of the nominal peak amplitude. In a read-whilewrite mode the signal level on tape produces a higher output than tape that has been written and wound on a reel. This effect is primarily due to self erasure from adjacent tape on the pack. Also, when writing data it is important that tape imperfections do not result in marginal signal amplitudes.


Figure 1-1. Read Data Circuits Timing Diagram

1-19. The skew gate circuit provides a voltage for the skew delay circuit of the read data circuits. The purpose of skew delay is to compensate for channel-to-channel time differentials introduced in the read system. There are two major sources of interchannel time displacements (static skew). One source is due to non-perfect alignment of individual track gaps in the read head (gap scatter) and the centerlines of the head may be tipped with respect to the tape edge (azimuth misalignment). As a result, certain bits of the byte will be detected before the others. Since the tape speed is constant, the effects of delaying each track so that all outputs occur simultaneously when reading an "all ones" alignment tape, is the same as mechanically aligning the read stack. When reading in a reverse mode, the earliest tracks become the later tracks and a different set of compensating delays are required. The second source of static skew is differential phase delays in the individual data channels. The phase response of the head varies from track-to-track because of inductance variance. The overall analog channel bandwidths may be different and reflect differential phase delays at operating frequency.

1-20. During a read forward operation the skew delay voltage is through Q4 of the read control printed-circuit assembly. During a read reverse operation, Q4 is cut off, and skew delay voltage is through Q1. When changing direction, the voltage sources (Q1 and Q4) do not switch simultaneously ; there is a time lag in the switching to prevent the absence of a skew delay voltage.

1-21. The character gate generator provides a "not" Read Strobe ( $\overline{\mathrm{STROBE}}$ ) pulse and a clock pulse that is gated with
tape unit status to provide a "not" Read Clock ( $\overline{\mathrm{RC}}$ ) pulse. The first "one" bit detected by the read data circuits conditions the "nor" bus (low) and starts the character gate generator. The width of the character gate is 40 percent of the nominal byte-to-byte spacing and is automatically controlled by the density status input from the tape unit density select switch assembly. Tape units not equipped with the density select switch are hard-wired so that the character gate operates a 40 percent of 800 cpi byte-to-byte spacing.

1-22. The output of the character gate generator is coupled to a strobe one-shot through a schmitt-trigger. The trailing edge of the character gate triggers the strobe oneshot, generating the "not" Read Strobe ( $\overline{\mathrm{STROBE}}$ ) pulse. The "not" Read Strobe pulse is an 800 nanosecond pulse used by the read data circuits to sample the output register and set the input register for the next data byte.

1-23. The trailing edge of the "not" Read Strobe pulse triggers the clock one-shot. The output of the clock one-shot is a 3 -microsecond pulse that is gated with Read Enable to generate the "not" Read Clock ( $\overline{\mathrm{RC}}$ ) pulse. The read clock pulse indicates that a data byte has been recovered and is on the read data interface lines.

## 1-24. READ DATA CIRCUITS.

1-25. The analog outputs from the preamplifiers are directly coupled to seven or nine identical data channels located in the read data assembly. Figure 1-3 is a block diagram of the read data circuits. The analog signal from a given


Figure 1-2. Read Control Circuits, Simplified Logic Diagram


Figure 1-3. Read Data Circuit, Simplified Logic Diagram
channel is phase inverted, fullwave rectified, and threshold clipped so that only the portion of the signal that exceeds the threshold level is processed. This prevents noise or minor tape imperfections from generating erroneous responses.

1-26. The portion of the signal exceeding the threshold level is differentiated and the zero-crossing representing the peak amplitude of data is detected by a high-gain amplifier (10-20.9 ips tape units) or a Schmitt trigger circuit (21-45 ips tape units). The positive-going edge of the trigger output therefore represents the peak of the analog input signal, independent of signal amplitude.

1-27. The positive-going signal triggers the skew delay pulse generator. When the skew delay generator times-out, a short duration negative-going pulse directly clears the input register.

1-28. When the input register is cleared by the detected "one" bit, the input register outputs are set ( $Q$ output is low and $\bar{Q}$ output is high). With the input register cleared, the "nor" bus is activated. The "nor" bus is normally at a positive potential; however, when the "nor" bus is activated by the first "one" bit detected, the bus goes low (near 0 -volts). When the "nor" bus goes low, the read control character gate is activated. The $\mathbf{Q}$ output of the input register (low) is also applied to the output register.

1-29. When the character gate times-out, the leading edge of "not" Read Strobe ( $\overline{\text { STROBE }}$ ) clocks the input register contents to the output register and resets the input register. This transfers the data bit to the output register and prepares the input register for the next data byte. The output of the output register is gated with Read Enable to provide the interface with the read data bit.

# SECTION II <br> MAINTENANCE 

## 2-1. INTRODUCTION.

2-2. This section provides maintenance information for the read modules of the HP 7970B/7970C Digital Magnetic Tape Units. Maintenance information consists of performance checkout procedures and adjustment procedure. Prior to performing any maintenance to the read modules, ensure that the transport is functioning properly. (Refer to part 2.)

## 2-3. TEST EQUIPMENT REQUIRED.

2-4. In addition to the equipment required for transport maintenance (refer to part 2), the following tapes and test items are required to perform maintenance procedures described in this section.
a. Master Alignment Tape (all " 1 's", full-width at 800 cpi), part number 9162-0027.
b. Reference Amplitude Test Tape (all " 1 's", full-width at 200 cpi ), part number 5080-4547. This tape is recommended for read-only units.

## Note

The HP 13193A Read Test Board is available as an accessory. When used in conjunction with the HP 13191A Control and Status Test Board and the HP 13192A Write Test Board, maintenance procedures can be performed without the aid of an interfaced computer.

## 2-5. PERFORMANCE TEST PROCEDURES.

$2-6$. The following test procedures verify that the read data circuits conform to published specifications. The test procedures described assume the use of an on-line computer or the use of off-line test accessories. Prior to performing the test procedures, ensure that all transport adjustments have been made. (Refer to part 2.)

## 2-7. READ PREAMPLIFIER GAIN TEST.

2-8. For read-after-write units, write an alternate "ones" and "zeros" data pattern at 800 cpi . Measure the peak-topeak output voltage at the preamplifier test points. The voltage should be $6.4 \pm 0.3$ volts p-p. For read only units, load the Reference Amplitude Test Tape HP part number 50804547. Note the signal level indicated on the test tape label. Measure the peak-to-peak output voltage at the preamplifier test points. The measured voltage should be within $\pm 0.3$ volt of level indicated on the test tape label. (Typically 85 percent of 6.4 V p-p.)

## 2-9. READ THRESHOLD LEVEL TEST.

2-10. Use oscilloscope and check dc voltage level on the threshold test point on the read control card. Values should be as follows:
a. During read-after-write mode: $+1.27 \pm 0.060$ volts dc.
b. During read only mode: $+0.450 \pm 0.010$ volt dc.
c. During high-speed read: 1.7 volts dc $\pm 1 \%$.

## 2-11. READ HEAD STATIC SKEW TEST.

2-12. Read head static skew is measured optically during head manufacturing and is also verified electrically on special test facilities. When installed on the tape transport, certain electrical and mechanical considerations enter as factors. These may modify the static skew to a minor degree. Measurement may be used as additional information for analysis of field performance. The electronic read de-skewing effectively eliminates this factor in normal operation. Measurement is as follows:
a. Use the master alignment tape as the source of data.
b. Connect channel A of the oscilloscope to the P (parity) track preamplifier output and adjust the sweep to synchronize near the zero axis crossover on the positive slope.
c. Channel B of the oscilloscope will be connected to the various skew test points on the read cards. Channels will be used in alternate mode.
d. With the delayed sweep operated under a sweep rate of 2 microseconds $/ \mathrm{cm}$, adjust the delay to display the positive-going step at the start of the channel $P$ skew delay ramp on the center of the oscilloscope. This will be the zero time reference for all other measurements. Adjust channel B gain as required to obtain good resolution.
e. Without making any further adjustments to the oscilloscope time base, move the channel B probe to each skew delay test point in sequence and note its relative position to the center of the oscilloscope. Signals to the left of center are early, and may be noted as "plus" with those to the right noted as "minus" as they are later than the signal from track $P$.
f. When all measurements have been completed in the forward direction; the same sequence can be repeated for the reverse. It will be necessary to readjust the time delay for positioning track P to center.
g. Review data taken and determine the two tracks that are the earliest (largest plus number) and latest (largest minus number). The time differential between them (sum of the two times) converted to microinches for the tape speed involved is the read head static skew. This number should not exceed 225 microinches.

## Note

For readings between 200 and 225 microinches, correct for the electronic time delay variation in the peak detection circuitry. This may be measured by repeating steps " $a$ " through " f " except that the oscilloscope channel A probe must be connected to the preamplifier output corresponding to the skew test point on the oscilloscope channel B probe. These figures must be subtracted from the normal readings (taken with channel $\mathbf{P}$ as the only sync) to determine the true head skew. Under these conditions, a true head skew in excess of 200 microinches is higher than normal but will not cause any practical problems.

## 2-13. COMPENSATED STATIC READ SKEW TEST.

2-14. Compensated static read skew is a measure of the degree to which the electronic time delays are effective in eliminating the read head static skew. The termination of each track skew delay is the fall (or negative-going trailing edge) of the positive-going ramp visible at the SKEW testpoints on each read card. With perfect compensation these will all coincide. As a matter of practical consideration this seldom happens except during the period of adjustment with a specific master alignment tape. When comparisons are made using alignment tapes other than the one used for adjustment, or where the same tape is subject to possible damage, it is not uncommon to see a time difference of several microseconds depending on tape speed. Considering only a $\pm 1$ percent error in the alignment tapes and complete stability of the skew delay, there could be a difference of 25 microinches between two tapes (allowing a time difference from 2.5 microseconds at 10 ips to 0.5 microsecond at 50 ips ). Evaluate compensated skew using the following procedure.
a. Use channel A of the oscilloscope for the master reference for all skew measurements. Connect probe to the skew test point for channel P read card.
b. Sync the main sweep to the negative slope of the channel A waveform and set sweep speed to display two bit-to-bit distances. This will result in a negative-going trailing edge at the center of the oscilloscope and another at the right side. If there is time asymmetry in the master tape (some tapes have this and some do not), there will be double trailing edges in the center of the screen with the time difference corresponding to the recorded pulse asymmetry on the tape. If this is visible, refer to the note following step "e." Use the
variable setting of the main sweep to position pulses as stated. This will assure the visibility of write time asymmetry on the master tape.
c. The delayed sweep will be used to position the next sequential bit in the center of the screen. Use the internal sync, positive slope position on the delayed sweep, and adjust the trigger level for a stable waveform. The delayed sweep should be adjusted (from the ccw position) only as far as required to permit the delayed sweep to internally trigger on the next pulse.
d. Establish final positioning of the $P$ track reference point (negative-going trailing edge) at the center of the screen by use of the sweep positioning controls. Be sure that the delayed sweep remains correctly calibrated since correct time differences in microseconds will be required. Some positioning can also be done with the trigger level.
e. Use channel B of the oscilloscope and the chopped mode to observe the relative position of all other tracks. Note these positions and determine the earliest and latest tracks. The maximum difference should be 30 microinches or less. If displays are between 30 and 50 microinches, check the write/read skew for the unit. If this skew results in the difference being less than 25 microinches, no adjustment should be made unless there is agreement between two master skew tapes showing that the same relative error exists between the same tracks. If this occurs it can be presumed that the unit adjustments have remained stable (write/read skew within $\pm 1$ percent since last adjustment), but the previous read skew adjustment was made with a bad master alignment tape.

## Note

Skew measurements can become somewhat difficult if significant write time asymmetry exists. This asymmetry will be observed on some master alignment tapes as well as tapes generated by the tape units. No special steps can be taken when reading the master alignment tape, but when writing tapes for check of write/read skew it is important that all write pulses start with the same relative flux polarities on tape. This can be assured if there is a sequence of reverse/stop/ forward drive commands prior to a skew measurement. The forward command assures complete write reset conditions as the WSW line is made true.
g. Measurement of compensated static read skew in the reverse direction may be made by the same technique (steps "a" through " $e$ "). Evaluation of this area becomes somewhat complex, as the magnetic characteristics of the pulse waveforms in the reverse direction will not necessarily be symmetrical with the forward direction waveform. This is true for alignment tapes as well as for tapes written on the tape unit.

## 2-15. READ CHARACTER GATE, STROBE, AND READ CLOCK TEST.

2-16. The read character gate is initiated by the first " 1 " bit to complete a read skew delay period. The fall of read skew delay provides a trigger at the "nor" bus, causing it to move in a negative direction. This fall triggers the read character gate period which is nominally 40 percent of the bit-to-bit period for each density. Termination of the gate will cause the "nor" bus to move in a positive direction, which does two things. It sets the data levels at the read outputs and initiates the leading edge of the read strobe pulse. The read strobe trailing edge then generates the read clock output. The strobe delay time provides an interval for the read data outputs to settle before the read clock output occurs. Measure these characteristics as follows:
a. Generate an appropriate data pattern, starting with an all " 1 's" program under read-after-write conditions.
b. Sync the scope on the NOR test point with the negative slope. Then adjust the main sweep rate so that the next negative-going edge occurs 10 division later. (Each division now is 10 percent of the bit-to-bit period.)
c. Observe that the positive-going edge (end of gate) occurs between 35 and 45 percent of the bit-to-bit period. If the density select option is included, check for all three densities using appropriate clock rates.

2-17. Strobe pulse delay and read clock relationships to data are measured as follows:
a. Generate a data pattern that will move a single bit through all data channels in sequence. This will provide a data output pattern and will exercise each read channel in terms of initiating a read strobe.
b. Connect oscilloscope channel A to the data output of any read channel using the negative sync and auto triggering mode.
c. Remove the read data connector to establish standard measurement conditions. (Various lengths of cables and associated capacity will effect measurement.)
d. Set sweep speed to 0.2 microsecond/division and establish a stable pattern for the leading edge of data (for both negative and positive sync).
e. Using the alternate triggered by A mode, connect oscilloscope channel B to the read clock test point on the read control card.
f. Observe the time difference between the leading edge of data and the leading edge of clock. The clock delay must be between 0.5 and 1.5 microseconds.
g. Observe the pulse width of the read clock. This should be between 2 and 3 microseconds.
h. The read clock output should be continuous. (Verifies that read strobe is being initiated by each read channel.)

## 2-18. ADJUSTMENT PROCEDURES.

2-19. The adjustment procedures for the read modules consist of preamplifier gain adjustments, forward static skew adjustments, reverse static skew adjustments, and read character gate adjustments. Prior to performing the read data adjustment procedures, ensure that all transport adjustments have been made and that all adjustments are within tolerance.

## 2-20. PREAMPLIFIER GAIN ADJUSTMENTS.

2-21. The gain/bandwidth characteristics of the preamplifier will cause small changes in phase that will effect the static skew compensation if the preamplifier gain control is adjusted. Therefore, it must be adjusted prior to the read static skew compensation, and if changed, the read static skew adjustment should be rechecked. Adjustment is made as follows:
a. Read-Only Units; preferred method where a read-afterwrite equipped tape unit is available:
(1) Load the write test tape and place the tape unit in write mode and write a full reel of all " 1 's" data at 200 cpi density. Do not rewind.
(2) Transfer the test tape to the read only tape unit.
(3) Read the tape in reverse.
(4) Adjust preamplifier gain variable resistors for an average peak-to-peak output of $6.4 \pm 0.2$ volts.
b. Read-Only Units; method utilizing a reference amplitude test tape.
(1) Load the test tape (HP 5080-4547).
(2) Operate the tape unit in read mode.
(3) Adjust preamplifier gain variable resistors to obtain the average peak-to-peak output voltage specified on the test tape reel tolerance specifications, $\pm 0.2$ volt p-p.
c. Read/Write Units:
(1) Load the transport with the write test tape and place the tape unit in write mode. Write all " 1 's" at 200 cpi .
(2) Connect an oscilloscope to each preamplifier test point and adjust each preamplifier for an output of 6.4 V (peak-to-peak).

## 2-22. FORWARD STATIC SKEW COMPENSATION ADJUSTMENTS.

2-23. The techniques for rapid adjustment and for evaluating the need for adjustment differ. Figure 2-1 shows poor skew alignment and proper skew alignment. To adjust static skew compensation proceed as follows:
a. Load the Master Alignment Tape, HP part number 9162-0027, and place the tape unit in synchronous forward mode for the adjustment operation. Preset all skew delay controls fully cew (minimum delay).
b. Perform the compensated static skew test (paragraph 2-13) to determine which channel is lagging.
c. Adjust FWD skew delay control of channel 2 until it is slightly lagging the channel determined in step "b." Channel 2 will be reference channel for remaining adjustments.
d. Connect the oscilloscope channel A probe to the FWD SKEW test point of the reference channel (2). Connect the oscilloscope channel B probe to each FWD SKEW test point in succession and algebraically add oscilloscope channels A and B.
e. Adjust the oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next), with the oscilloscope vertical deflection at approximately $2 \mathrm{~V} / \mathrm{cm}$.
f. Adjust each channel skew delay variable resistor for a maximum displayed amplitude.

## 2-24. REVERSE STATIC SKEW COMPENSATION ADJUSTMENTS.

2-25. Reverse static skew compensation is accomplished in exactly the same manner as that used for forward skew except for the use of reverse drive mode and adjustment of reverse skew controls. The same SKEW test points are used for both adjustments.

2-26. When considering the need for readjustment, it must be recognized that there are small differences in the master skew tapes. For example, if there is an observed difference of 1 microsecond between channels, this would correspond to 25 microinches at a tape speed of 25 ips . If the previous adjustment had been made with one master tape and checked with another, and if both master tapes were accurate to $\pm 1$ percent ( $\pm 12.5$ microinches), this small difference could occur even with complete stability of adjustment of the part of the electrical and mechanical factors involved in the tape unit.

## 2-27. READ CHARACTER GATE ADJUSTMENTS.

2-28. The read character gate is adjusted to allow a period equal to 40 percent of the bit-to-bit distance for all of the read bits in a character to be placed in the output register. At the end of this period a read strobe occurs which sets all read data lines. One microsecond later, a read clock is generated which lasts 2 to 3 microseconds as an output signal. The read character gate is adjusted as follows:
a. Load the tape unit with the Master Alignment Tape, HP part number 9162-0027 (or any all "ones" 800 cpi tape), place the unit in synchronous forward operation, and select 800 cpi operation (seven-track units only).
b. Synchronize the oscilloscope (negative slope) to the NOR test point on the read control card. (The first data bit of a character will start the gate time when this line goes to ground.)
c. Observe the bit-to-bit time (negative-going edge to negative-going edge). The low (or ground) portion of this signal represents the character gate time.
d. Using the read control gate control (R29), adjust the $\overline{\mathrm{NOR}}$ (ground portion) of the signal to 40 percent of the nominal bit-to-bit time. Ensure that the bit-to-bit time is consistent with the data transfer rate.


10-20.9 IPS TAPE UNITS


21-37-1/2 IPS TAPE UNITS

Figure 2-1. Skew Alignment Waveforms

## SECTION III

## REPLACEABLE PARTS

## 3-1. INTRODUCTION.

3-2. This section provides information for ordering replacement parts for the read modules of the HP 7970B/ 7970C Digital Magnetic Tape Units.

3-3. This section contains assembly parts list, supporting illustrations, ordering information, and a part number cross reference.

## 3-4. ASSEMBLY PARTS LISTS.

3-5. The assembly parts lists represent a breakdown of all replaceable parts of the read modules. The information contained in the lists are under the following headings:
a. FIGURE \& INDEX NO.
b. PART NUMBER.
c. DESCRIPTION.
d. UNITS PER ASSY.

## 3-6. FIGURE AND INDEX NUMBER.

3-7. The figure and index number column identifies the figure that illustrates each listed item and the index number that identifies the item on the illustration.

## 3-8. PART NUMBER.

3-9. The part number column provides the HewlettPackard part number for each item listed in the assembly parts list.

## 3-10. DESCRIPTION.

3-11. The description column describes the items within the article. An indented column arrangement is used to show the relationship between a part and the next higher assembly. The top assembly of each listing appears in indention 1. Primary subassemblies (of top assembly) and attaching parts
appear in indention 2. This method of indention is continued through indention 3, 4, etc, until all replaceable parts are listed. Attaching parts are listed immediately following the part they attach. Attaching parts are identified by the abbreviation (AP) enclosed in parentheses at the end of the description.

3-12. Reference designation and manufacture information (if applicable) is also included in the description column.

## 3-13. UNITS PER ASSEMBLY.

3-14. The quantity shown in the units per assembly column reflects the total quantity of a part required by the next higher assembly of that part. This quantity is not necessarily the total used for the complete equipment. The abbreviation AR is used to indicate usage as required of a particular item. The abbreviation REF is used to indicate that the quantity of an item used per assembly is listed in the next higher assembly of the group assembly parts list.

## 3-15. ORDERING INFORMATION.

3-16. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered.
a. Identification of the unit, kit, or assembly containing the part.
b. Hewlett-Packard part number for each part.
c. Description of each part.
d. Circuit reference designation (if applicable).

## 3-17. PART NUMBER CROSS REFERENCE.

3-18. Table $3-1$ at the end of this section provides a cross reference between Hewlett-Packard part numbers and manufacturer's part numbers.


Figure 3-1. Density Select Switch Assembly A12

| $\begin{gathered} \text { FIGURE } \\ \& \\ \text { INDEX } \\ \text { NO. } \end{gathered}$ | PART <br> NUMBER | 12345 DESCRIPTION | $\begin{aligned} & \text { UNITS } \\ & \text { PER } \\ & \text { ASSY } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| 3-1- | 07970-62087 | DENSITY SELECT SWITCH ASSEMBLY A12. | REF |
| -1 | 07970-60350 | . LENS BLOCK ASSEMBLY, density select switch . . . . | 1 |
| -2 | 0624-0077 | . . SCREW, no. 4-40, 0.312-inch pozi (AP) . | 2 |
| -3 | 2190-0416 | . . WASHER, flat (AP) . . | 2 |
| -4 | 07970-60090 | . DENSITY SELECT PC ASSEMBLY A1 | 1 |
| -5 | 0757-0419 | . . RESISTOR, fxd , 681 ohms, $1 \%, 1 / 8 \mathrm{~W}(\mathrm{R} 1, \mathrm{R} 2, \mathrm{R} 3)$. . . . | 3 |
| -6 | 1820-0256 | . . INTEGRATED CIRCUIT (U1) . . . . . . . | 1 |
| -7 | 0757-0428 | . . RESISTOR, fxd, 1.62k, 1\%, 1/8W (R4, R5, R6) | 3 |
| -8 | 2140-0209 | . . LAMP, 14V, 0.08A (DS1, DS2, DS3) | 3 |
| -9 | 3101-0847 | . . SWITCH ASSEMBLY (S1, S2, S3) (not field replaceable) . . . | 1 |



Figure 3-2. Read Preamplifier PC Assembly A15


Figure 3-2. Read Preamplifier PC Assembly A15 (Sheet 2 of 2 )


7970-A-078

Figure 3-2. Read Preamplifier PC Assembly A15 (Sheet 1 of 2)

| $\begin{gathered} \text { FIGURE } \\ \& \\ \text { INDEX } \\ \text { NO. } \end{gathered}$ | PART NUMBER | 12345 DESCRIPTION | UNITS PER ASSY |
| :---: | :---: | :---: | :---: |
| 3-1- | 07970-60500 | READ PREAMPLIFIER PC ASSEMBLY A15, 10-20 ips . . |  |
| 3-1- | 07970-62000 | READ PREAMPLIFIER PC ASSEMBLY A15, $21-45 \mathrm{ips}$. . . . . |  |
| -1 | 0180-0228 | - CAPACITOR, fxd, $22 \mu \mathrm{~F}(\mathrm{C} 47, \mathrm{C} 48)$. | 2 |
| -2 | 0180-1704 | . CAPACITOR, $\mathrm{fxd}, 47 \mu \mathrm{~F}$ ( $\mathrm{C} 2, \mathrm{C} 8, \mathrm{C} 12, \mathrm{C} 18, \mathrm{C} 22, \mathrm{C} 28, \mathrm{C} 32, \mathrm{C} 38, \mathrm{C} 42)$ | 9 |
| -3 | 0160-2055 | CAPACITOR, fxd, $0.01 \mu \mathrm{~F}$ (C5, C6, C15, C16, C25, C26, C35, . . . . . C36, C45, C46) | 10 |
| 4 | 0180-0291 | . CAPACITOR, $\mathrm{fxd}, 1.0 \mu \mathrm{~F}$ (C49) . . . . . . . . . . . . . . | 1 |
| -5 | 0140-0210 | . CAPACITOR, $\mathrm{fxd}, 270 \mathrm{pF}(\mathrm{C} 1, \mathrm{C} 7, \mathrm{C} 11, \mathrm{C} 17, \mathrm{C} 21, \mathrm{C} 27, \mathrm{C} 31, \mathrm{C} 37, \mathrm{C} 41)$. . | 9 |
| -6 | 0698-3136 | RESISTOR, $\mathrm{fxd}, 17.8 \mathrm{k}, 1 \%, 1 / 8 \mathrm{~W}$ (R1, R5, R9, R13, R17, R21, . . . . . R25, R29, R33) | 9 |
| -7 | 0160-2225 | - CAPACITOR, $\mathrm{fxd}, 2000 \mathrm{pF}(\mathrm{C} 3, \mathrm{C} 9, \mathrm{C} 13, \mathrm{C} 19, \mathrm{C} 23, \mathrm{C} 29, \mathrm{C} 33, \mathrm{C} 39, \mathrm{C} 43)$. . | 9 |
| 8 | 0160-2200 | . CAPACITOR, fxd, $43 \mathrm{pF}(\mathrm{C4}, \mathrm{C} 10, \mathrm{C} 14, \mathrm{C} 20, \mathrm{C} 24, \mathrm{C} 30, \mathrm{C} 34, \mathrm{C} 40, \mathrm{C} 44)$. . | 9 |
| -9 | 0757-0346 | . RESISTOR, fxd , 10.0 ohms, $1 / 8 \mathrm{~W}(\mathrm{R} 36, \mathrm{R} 37)$. . . . . . . . . | 2 |
| -10 | 0757-0401 | RESISTOR, fxd, 100 ohms, 1/8W (R2, R6, R10, R14, R18, R22, R26, . . . . R30, R34) | 9 |
| -11 | 0757-0462 | RESISTOR, fxd, 75k, 1\%, 1/8W (R4, R8, R12, R16, R20, R24, R28, . . . . R32, R38) | 9 |
| -12 | 1826-0044 | - INTEGRATED CIRCUIT, operational amplifier (U1 thru U5) | 5 |
| -13 | 2100-3251 | RESISTOR, var, 500 ohms, 1/2W (R3, R7, R11, R15, R19, R23 . . . . . R27, R31, R35) | 9 |


| $\begin{gathered} \text { FIGURE } \\ \& \\ \text { INDEX } \\ \text { NO. } \end{gathered}$ | PART NUMBER | 12345 DESCRIPTION | UNITS PER ASSY |
| :---: | :---: | :---: | :---: |
| 3-2. | 07970-60500 | READ PREAMPLIFIER PC ASSEMBLY A15, 10-20 ips . . |  |
| 3-2- | 07970-62000 |  |  |
| -1 | 0180-0228 | CAPACITOR, fxd, $22 \mu \mathrm{~F}$ ( $\mathrm{C} 47, \mathrm{C48}$ ) . | 2 |
| -2 | 0180-1704 | CAPACITOR, $\mathrm{fxd}, 47 \mu \mathrm{~F}$ ( $\mathrm{C} 2, \mathrm{C} 8, \mathrm{C} 12, \mathrm{C} 18, \mathrm{C} 22, \mathrm{C} 28, \mathrm{C} 32, \mathrm{C} 38, \mathrm{C} 42$ ). | 9 |
| -3 | 0160-2055 | CAPACITOR, fxd, $0.01 \mu$ F (C5, C6, C15, C16, C25, C26, C35, . . . . . C36, C45, C46) | 10 |
| -4 | 0180-0291 | CAPACITOR, $\mathrm{fxd}, 1.0 \mu \mathrm{~F}$ (C49) . . | 1 |
| -5 | 0160-0157 | CAPACITOR, fxd, 4700 pF (C1, C7, C11, C17, C21, C27, C31 . . . <br> C37, C41) (10-20 ips) | 9 |
| -5 | 0140-0210 | CAPACITOR, fxd, 270 pF (C1, C7, C11, C17, C21, C27, C31, C37, C41) . <br> (21-45 ips) | 9 |
| -6 | 0698-3155 | RESISTOR, fxd, 4.7k, 1\%, 1/8W (R1, R5, R9, R13, R17, R21, . . . . . R25, R29, R33) (10-20 ips) | 9 |
| -6 | 0698-3136 | RESISTOR, $\mathrm{fxd}, 4.64 \mathrm{k}, 1 \%, 1 / 8 \mathrm{~W}$ (R1, R5, R9, R13, R17, R21, . . . . <br> R25, R29, R33) (21-45 ips) | 9 |
| -7 | 0160-2225 | . CAPACITOR, fxd, 2000 pF (C3, C9, C13, C19, C23, C29, C33, C39, C43) | 9 |
| -8 | 0160-2200 | . CAPACITOR, fxd, $43 \mathrm{pF}(\mathrm{C} 4, \mathrm{C} 10, \mathrm{C} 14, \mathrm{C} 20, \mathrm{C} 24, \mathrm{C} 30, \mathrm{C} 34, \mathrm{C} 40, \mathrm{C} 44)$. | 9 |
| -9 | 0757-0346 | . RESISTOR, fxd, 10.0 ohms, 1/8W (R36, R37) | 2 |
| -10 | 0757-0399 | RESISTOR, fxd, 82.5 ohms, $1 / 8$ W (R2, R6, R10, R14, R18, R22, R26,. . . <br> R30, R34) ( 10 - 20 ips) | 9 |
| -10 | 0757-0401 | RESISTOR, fxd, 100 ohms, $1 / 8 \mathrm{~W}$ (R2, R6, R10, R14, R18, R22, R26, . . . R30, R34) ( 21 - 45 ips ) | 9 |
| -11 | 0757-0462 | RESISTOR, fxd, $75 \mathrm{k}, 1 \%, 1 / 8 \mathrm{~W}$ (R4, R8, R12, R16, R20, R24, R28, . . . R32, R38) | 9 |
| -12 | 1826-0044 | INTEGRATED CIRCUIT, operational amplifier (U1 thru U5) | 5 |
| -13 | 2100-3251 | . RESISTOR, var, 500 ohms, 1/2W (R3, R7, R11, R15, R19, R23, . . . . R27, R31, R35) | 9 |


| $\begin{gathered} \text { FIGURE } \\ \& \\ \text { INDEX } \\ \text { NO. } \end{gathered}$ | PART NUMBER | 12345 DESCRIPTION | UNITS PER ASSY |
| :---: | :---: | :---: | :---: |
| 3-1- | 07970-60500 | READ PREAMPLIFIER ASSEMBLY A15, 10-20 ips. | REF |
| 3-1- | 07970-62000 | READ PREAMPLIFIER PC ASSEMBLY A15, 21 - 45 ips. | REF |
| -1 | 0683-1525 | . RESISTOR, fxd, 1.5k, 5\%, 1/4W (R4, R104, R204, R304, R404, . . . . . R504, R604, R704, R804) | 9 |
| -2 | 0683-1025 | RESISTOR, fxd, $1 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ (R6, R106, R206, R306, R406, . . . . . . R506, R606, R706, R806) | 9 |
| -3 | 0683-4325 | RESISTOR, fxd, 43.k, 5\%, 1/4W (R5, R105, R205, R305, R405, . . . . . R505, R605, R705, R805) | 9 |
| -4 | 0757-0460 | RESISTOR, fxd, 61.9k, 1\%, 1/8W (R3, R103, R203, R303, R403, . . . . . R503, R603, R703, R803) | 9 |
| -5 | 2100-1758 | RESISTOR, var, ww, 1k, 5\%, 1W (R2, R102, R202, R302, R402, . . . . . R502, R602, R702, R802) | 9 |
| -6 | 0683-6825 | RESISTOR, fxd, 6.8k, 5\%, 1/4W (R1, R101, R201, R301, R401, . . . . . R501, R601, R701, R801) (used on 07970-60500) | 9 |
| -6 | 0698-3136 | RESISTOR, fxd, 17.8k, 1\%, 1/8W (R1, R101, R201, R301, R401, . . . . R501, R601, R701, R801) (used on 07970-62000) | 9 |
| -7 | 0160-2055 | CAPACITOR, fxd, $10 \mu \mathrm{~F}, 10 \%, 30 \mathrm{Vdcw}$ (C4, C5, C104, C105, C204, C205, C304, C305, C404, C405, C504, C505, C604, C605, C704, C705, C804, C805) | 18 |
| -8 | 07970-80050 | . INTEGRATED CIRCUIT, pretested (U1, U2, U3, U4, U5, U6, U7, U8, U9) | 9 |
| -9 | 0340-0456 | . . INSULATOR, integrated circuit pad . . | 1 |
| -10 | 0180-0228 | . CAPACITOR, fxd, $22 \mu \mathrm{~F}, 10 \%, 15 \mathrm{Vdcw}(\mathrm{C} 7, \mathrm{C} 8$ ) . | 2 |
| -11 | 0140-0208 | CAPACITOR, fxd, 680 pF, 5\%, 300 Vdcw (C3, C103, C203, C303, C403, . . C503, C603, C703, C803) (used on 07970-60500) | 9 |
| -11 | 0160-2208 | CAPACITOR, fxd, 330 pF, 5\%, 300 Vdcw (C3, C103, C203, C303, C403, . . . C503, C603, C703, C803) (used on 07970-60510) | 9 |
| -12 | 0160-3449 | CAPACITOR, fxd, $2000 \mathrm{pF}, 10 \%, 250 \mathrm{Vdcw}$ (C6, C106, C206, C306, . . . . C406, C506, C606, C706, C806) | 9 |
| -13 | 0160-2213 | CAPACITOR, fxd, $620 \mathrm{pF}, 5 \%, 300$ Vdcw (C1, C101, C201, C301, C401, . C501, C601, C701, C801) (used on 07970-60500 and 07970-60510) | 9 |
| -13 | 0140-0210 | CAPACITOR, fxd, $270 \mathrm{pF}, 5 \%, 300 \mathrm{Vdcw}$ (C1, C101, C201, C301, C401, . C501, C601, C701, C801) (used on 07970-62000) | 9 |
| -14 | 1901-0040 | DIODE, Si (CR1, CR101, CR201, CR301, CR401, CR501, CR601, . CR701, CR801) | 9 |
| -15 | 0180-0291 | . CAPACITOR, fxd, $1 \mu \mathrm{~F},+10 \%, 35 \mathrm{Vdcw}$ (C9) . . . . . . . | 1 |
| -16 | 0180-1704 | CAPACITOR, fxd, $47 \mu \mathrm{~F}, 10 \%, 6 \mathrm{Vdcw}$ (C2, C102, C202, C302, C402, . . C502, C602, C702, C802) | 9 |
| -17 | 07970-00430 | . BRACKET, read preamplifier . | 1 |
| -18 | 2360-0195 | . . SCREW, no. 6-32, 0.312-inch, pozi (AP) . . | 4 |
| -19 | 2190-0085 | . . WASHER, lock, helical, no. 6 (AP) | 4 |
| -20 | 3050-0228 | . . WASHER, no. 6 (AP) . . . . . . . . . | 4 |



Figure 3-3. Read Assembly A18


Figure 3-3. Read Assembly A18



Figure 3-4. Read Control PC Assembly (Sheet 1 of 2)


Figure 3-4. Read Control PC Assembly (Sheet 2 of 2)

| $\begin{aligned} & \text { FIGURE } \\ & \& \\ & \text { INDEX } \\ & \text { NO. } \end{aligned}$ | PART NUMBER | $\begin{array}{llllll}1 & 2 & 3 & 4 & 5 & \text { DESCRIPTION }\end{array}$ | UNITS PER ASSY |
| :---: | :---: | :---: | :---: |
| 3-4- | 07970-62170 | READ CONTROL PC ASSEMBLY A18A1, 10-20.9 ips | REF |
| 4. | 07970-62171 | READ CONTROL PC ASSEMBLY A18A1, 21 - 45 ips | REF |
| -1 | 0683-2225 | . RESISTOR, fxd, 2.2k, 5\%, 1/4W (R2, R4, R8, R22, R29). | 5 |
| -2 | 2100-1758 | . RESISTOR, var, ww, 1k, 5\%, 1W (R29) . . | 1 |
| -3 | 0683-1235 | . RESISTOR, fxd, 12k, 5\%, 1/4W (R23) . . . . . . . . | 1 |
| -4 | 0698-3132 | . RESISTOR, fxd, 261 ohms, 1\%, 1/8W (R28) . . . . . . | 1 |
|  | 0757-0280 | . RESISTOR, fxd, $1 \mathrm{k}, 1 \%, 1 / 8 \mathrm{~W}$ (R43). . . . . . . . . . . | 1 |
| -5 | 0757-0428 | . RESISTOR, fxd, 1.62k, 1\%, 1/8W (R10, R26) . . . . . . . . . | 2 |
| -6 | 0698-3438 | . RESISTOR, fxd, 147 ohms, 1\%, 1/8W (R27) . | 1 |
| -7 | 0757-0199 | . RESISTOR, fxd, 21.5k, 1\%, 1/8W (R25) . . . . . . . . . . . | 1 |
| -8 | 0683-8235 | . RESISTOR, fxd, 82k, 5\%, 1/4W (R30, R37, R38) . . | 3 |
| -9 | 0683-1025 | . RESISTOR, fxd, 1k, 5\%, 1/4W (R3, R7; R11, R31, R32, R39) . | 6 |
| -10 | 0683-2725 | . RESISTOR, fxd, 2.7k, 5\%, 1/4W (R34) . . . . . . . . . . . | 1 |
| -11 | 0683-6815 | . RESISTOR, fxd, 680 ohms, 5\%, 1/4W (R33) . . . . . . . . . . | 1 |
| -12 | 0757-0442 | . RESISTOR, fxd, 10k, 1\%, 1/8W (R35) . . . . . . . . . . . . | 1 |
| -13 | 0757-0444 | . RESISTOR, fxd, 12.1k, 1\%, 1/8W (R36) . . . . | 1 |
| -14 | 0757-1094 | . RESISTOR, fxd, 1.47k, 1\%, 1/8W (R16, R42) . . . . . . . . . | 2 |
| -15 | 0683-1525 | . RESISTOR, fxd, 1.5k, 5\%, 1/4W (R41) . . . . . . . . . . . | 1 |
| -16 | 0683-6825 | . RESISTOR, fxd, 6.8k, 5\%, 1/4W (R1, R9, R40) | 3 |
| -17 | 0757-0401 | . RESISTOR, fxd, 100 ohms, 1\%, 1/8W (R15) . . . . . . . . . | 1 |
| -18 | 0757-0280 | . RESISTOR, fxd, $1 \mathrm{k}, 1 \%, 1 / 8 \mathrm{~W}$ (R13) | 1 |
| -19 | 0698-0082 | . RESISTOR, fxd, 464 ohms, 1\%, 1/8W (R12) | 1 |
| -20 | 0683-3325 | . RESISTOR, fxd, 3.3k, 5\%, 1/4W (R6, R17, R19) | 3 |
| -21 | 0683-3335 | . RESISTOR, fxd, 33k, 5\%, 1/4W (R14) | 1 |
| -22 | 0683-2235 | . RESISTOR, fxd, 22k, 5\%, 1/4W (R5). | 1 |
| -23 | 0757-0439 | . RESISTOR, fxd, 6.81k, 1\%, 1/8W (R20) . | 1 |
| -24 | 0757-0443 | . RESISTOR, fxd, 11k, 1\%, 1/8W (R21) . . . . . . | 1 |
| -25 | 1854-0071 | . TRANSISTOR, NPN, Si, 2 N3494 (Q2, Q2, Q5, Q6, Q7, Q12) . | 6 |
| -26 | 1901-0040 | . DIODE, Si (CR1 thru CR11) . | 11 |
| -27 | 1854-0270 | . TRANSISTOR, NPN, Si, 2 N 4265 (Q8, Q10, Q11) . . . . . . . . | 3 |
| -28 | 1853-0015 | . TRANSISTOR, PNP, Si, 2N3640 (Q9) . . . . . . . . . . . . | 1 |
| -29 | 0160-0162 | . CAPACITOR, fxd, $0.022 \mu \mathrm{~F}, 10 \%$ (C8) (10-20.9 ips) . . . . . . . | 1 |
| -29 | 0160-0161 | . CAPACITOR, fxd, $0.01 \mu \mathrm{~F}, 10 \%$ (C8) (21-45ips) . | 1 |
| -30 | 0160-2307 | . CAPACITOR, fxd, $47 \mathrm{pF}, 5 \%, 300 \mathrm{Vdcw}$ (C9) . . . | 1 |
| -31 | 1820-0088 | . INTEGRATED CIRCUIT, type 851 (U5, U6) . . . . . . | 2 |
| -32 | 0140-0193 | . CAPACITOR, fxd, $82 \mathrm{pF}, 5 \%, 300 \mathrm{Vdcw}(\mathrm{C} 10)$. . . . . . . | 1 |
| -33 | 0160-2209 | . CAPACITOR, fxd, $360 \mathrm{pF}, 5 \%, 300 \mathrm{Vdcw}$ (C11) . . . . . . . . | 1 |
| -34 | 1820-0069 | . INTEGRATED CIRCUIT, type 7420N (U2) . . . . . . . . . . . | 1 |
| -35 | 0180-1701 | . CAPACITOR, fxd, $6.8 \mu \mathrm{~F}, 20 \%, 6 \mathrm{Vdcw}(\mathrm{C} 12, \mathrm{C} 13)$. . . . . . . . | 2 |
| -36 | 1820-0348 | . INTEGRATED CIRCUIT, type 844 (U1) . . . . . . . . . . . | 1 |
| -37 | 1820-0376 | . INTEGRATED CIRCUIT (U3) . . . . . . . . . . . . . . | 1 |
| -38 | 1853-0036 | . TRANSISTOR, PNP, 2 N3906 (Q1, Q4) | 2 |
| -39 | 0160-2055 | . CAPACITOR, fxd, $0.01 \mu \mathrm{~F}, 100 \mathrm{Vdcw} \mathrm{(C1}, \mathrm{C2}, \mathrm{C3}, \mathrm{C4}, \mathrm{C5}, \mathrm{C6)} \mathrm{}$. | 6 |
| -40 | 0180-1704 | . CAPACITOR, fxd, $47 \mu \mathrm{~F}, 10 \%, 6 \mathrm{Vdcw}(\mathrm{C} 7) . \mathrm{l}$. . . . . . . . | 1 |
| -41 | 1820-0349 | . INTEGRATED CIRCUIT (U4) . . . . . . . . . . . . . . | 1 |
| -42 | 0180-0210 | . CAPACITOR, fxd, $3.3 \mu \mathrm{~F}, 20 \%, 15 \mathrm{Vdcw}(\mathrm{C} 14, \mathrm{C} 15)$. . . . . . . . | 2 |



Figure 3-5. Single Channel Read Data PC Assembly (10-20.9 IPS)

| ```FIGURE & INDEX NO.``` | PART NUMBER | $\begin{array}{llllll}1 & 2 & 3 & 4 & 5 & \text { DESCRIPTION }\end{array}$ | UNITS PER ASSY |
| :---: | :---: | :---: | :---: |
| 3-5- | 07970-62167 | READ DATA PC ASSEMBLY A18A2, single-channel (10-20.9 ips) . | REF |
| -1 | 0683-4715 | . RESISTOR, fxd, 470 ohms, 1/4W (R14). | 1 |
| -2 | 2100-1923 | . RESISTOR, var, 50k (R21, R22) | 2 |
| -3 | 0180-1701 | . CAPACITOR, fxd, $6.8 \mu \mathrm{~F}, 6 \mathrm{~V}$, tant (C1, C8, C9) | 3 |
| -4 | 1901-0040 | . DIODE, Si, 30V, 30 mA (CR5, CR6, CR7, CR8) . . | 4 |
| -5 | 0757-0289 | . RESISTOR, fxd, 13.3k, 1\%, 1/8W (R20) . . . . . . . . . . . | 1 |
| -6 | 0160-0160 | . CAPACITOR, $f \times d, 0.0082 \mu \mathrm{~F}, \mathrm{My}(\mathrm{C} 3, \mathrm{C} 7)$. . . . . . . . | 2 |
| -7 | 1820-0515 | . INTEGRATED CIRCUIT, MV 9602 (U4) . . . . | 1 |
| -8 | 0683-4725 | . RESISTOR, fxd, $4.7 \mathrm{k}, 1 / 4 \mathrm{~W}$ (R11, R19) . . . . . . . . | 2 |
| -9 | 0683-2725 | . RESISTOR, fxd, 2.7k, 1/4W (R18) . . . . . . . . . . | 1 |
| -10 | 0140-0197 | . CAPACITOR, fxd, 180 pF , mica (C6) | 1 |
| -11 | 0683-2225 | . RESISTOR, fxd, 2.2k, 1/4W (R4, R16, R17) . . . . . . | 3 |
| -12 | 0683-1025 | . RESISTOR, fxd, $1 \mathrm{k}, 1 / 4 \mathrm{~W}$ (R24) . | 1 |
| -13 | 0757-0429 | . RESISTOR, fxd, 1.62k, 1\%, 1/8W (R23) . . . . | 1 |
| -14 | 1820-0348 | . INTEGRATED CIRCUIT, type 844 (U3) . | 1 |
| -15 | 1820-0077 | . INTEGRATED CIRCUIT, type SN7474 (U1) . . | 1 |
| -16 | 0180-0210 | . CAPACITOR, $\mathrm{fxd}, 3.3 \mu \mathrm{~F}, 15 \mathrm{~V}$ (C2, C4, C10, C11). . . . . | 4 |
| -17 | 0683-1515 | . RESISTOR, fxd, 150 ohms, 1/4W (R26) . . . . . | 1 |
| -18 | 1854-0071 | . TRANSISTOR, 2N3391 (Q1, Q2, Q3, Q4) . . . . | 4 |
| -19 | 0698-4477 | . RESISTOR, fxd, 10.5k, 1\%, 1/8W (R2) . . . . . | 1 |
| -20 | 0757-0442 | . RESISTOR, fxd, 10k, 1\%, 1/8W (R1). . . . . . | 1 |
| -21 | 0160-3449 | . CAPACITOR, fxd, $2000 \mathrm{pF}, 10 \%$ (C12) . | 1 |
| -22 | 0683-3635 | . RESISTOR, fxd, 36k, 1/4W (R3) . | 1 |
| -23 | 0683-1035 | . RESISTOR, fxd, 10k, 1/4W (R5, R8, R9) . | 3 |
| -24 | 1901-0450 | . DIODE, Si (CR1, CR2, CR3) | 3 |
| -25 | 0683-2255 | . RESISTOR, fxd, 2.2M, 1/4W (R7) | 1 |
| -26 | 0683-1045 | . RESISTOR, fxd, 100k, 1/4W (R10) | 1 |
| -27 | 0683-6825 | . RESISTOR, fxd, 6.8k, 1/4W (R6). | 1 |
| -28 | 0160-3573 | . CAPACITOR, fxd, 680 pF, cer (C5) . . . . . | 1 |
| -29 | 1826-0065 | . INTEGRATED CIRCUIT, comparator, LM 311 (U5) . | 1 |
| -30 | 0683-4735 | . RESISTOR, fxd, 47k, 1/4W (R15) . . . . . . . . . | 1 |



Figure 3-6. Single-Channel Read Data PC Assembly (21-45 IPS)



Figure 3-7. Dual Channel Read Data PC Assembly (10-20.9 IPS) (Sheet 1 of 2)


Figure 3-7. Dual Channel Read Data PC Assembly (10-20.9 IPS) (Sheet 2 of 2)



Figure 3-8. Dual-Channel Read Data PC Assembly (21-45ips) (Sheet 1 of 2)


7970-370

Figure 3-8. Dual-Channel Read Data PC Assembly (21-45ips) (Sheet 2 of 2)


Table 3-1. Part Number Cross Reference

| $\begin{gathered} \text { HP } \\ \text { PART } \end{gathered}$ NUMBER | MFR CODE | MFR PART NUMBER |
| :---: | :---: | :---: |
| 0140-0193 | 28480 | 0140-0193 |
| 0140-0197 | 14655 | RDM15F181J3C |
| 0140-0208 | 72136 | RDM15F681J3C |
| 0140-0210 | 28480 | 0140-0210 |
| 0160-0155 | 56289 | 192P33292-PTS |
| 0160-0156 | 56289 | 192P39292-PTS |
| 0160-0159 | 56289 | 192P68282-PTS |
| 0160-0160 | 56289 | 192P82292-PTS |
| 0160-0161 | 56289 | 192P10392-PTS |
| 0160-0162 | 56289 | 192P22392-PTS |
| 0160-2055 | 56289 | C023F101F103ZS22-CDH |
| 0160-2208 | 28480 | 0160-2208 |
| 0160-2209 | 72136 | RDM15F361J3C |
| 0160-2213 | 28480 | 0160-2213 |
| 0160-2307 | 28480 | 0160-2307 |
| 0160-3449 | 56289 | C067B251F202KS25-CDH |
| 0160-3572 | 56289 | C067F501F331 KS22-CDH |
| 0160-3573 | 56289 | C067F501F681KS22-CDH |
| 0180-0210 | 56289 | 150D335X0015A2-DYS |
| 0180-0228 | 56289 | 150D226X9015B2-DYS |
| 0180-0291 | 56289 | 150D105X9035A2-DYS |
| 0180-1701 | 28480 | 0180-1701 |
| 0180-1704 | 28480 | 0180-1704 |
| 0340-0456 | 13103 | 7717-122-N-WHT |
| 0624-0077 | 00000 | OBD |
| 0624-0098 | 00000 | OBD |
| 0683-1015 | 01121 | CB 1015 |
| 0683-1025 | 01121 | Св 1025 |
| 0683-1035 | 01121 | CB 1035 |
| 0683-1045 | 01121 | CB 1045 |
| 0683-1235 | 01121 | CB 1235 |
| 0683-1515 | 01121 | CB 1515 |
| 0683-1525 | 01121 | CB 1525 |
| 0683-2225 | 01121 | CB 2225 |
| 0683-2235 | 01121 | CB 2235 |
| 0683-2255 | 01121 | CB 2255 |
| 0683-2725 | 01121 | CB 2725 |
| 0683-3325 | 01121 | CB 3325 |
| 0683-3335 | 01121 | CB 3335 |
| 0683-3635 | 01121 | CB 3635 |
| 0683-4715 | 01121 | CB 4715 |
| 0683-4325 | 01121 | CB 4325 |
| 0683-4725 | 01121 | CB 4725 |
| 0683-4735 | 01121 | CB 4735 |
| 0683-6815 | 01121 | CB 6815 |
| 0683-6825 | 01121 | CB 6825 |
| 0683-8235 | 01121 | EB 8235 |


| $\begin{gathered} \text { HP } \\ \text { PART } \end{gathered}$ NUMBER | MFR CODE | MFR PART NUMBER |
| :---: | :---: | :---: |
| 0698-0082 | 28480 | 0698-0082 |
| 0698-3132 | 28480 | 0698-3132 |
| 0698-3136 | 28480 | 0698-3136 |
| 0698-3438 | 28480 | 0698-3438 |
| 0698-4477 | 28480 | 0698-4477 |
| 0757-0199 | 28480 | 0757-0199 |
| 0757-0279 | 28480 | 0757-0279 |
| 0757-0280 | 28480 | 0757-0280 |
| 0757-0401 | 28480 | 0757-0401 |
| 0757-0419 | 28480 | 0757-0419 |
| 0757-0428 | 28480 | 0757-0428 |
| 0757-0439 | 28480 | 0757-0439 |
| 0757-0442 | 28480 | 0757-0442 |
| 0757-0443 | 28480 | 0757-0443 |
| 0757-0444 | 28480 | 0757-0444 |
| 0757-0460 | 28480 | 0757-0460 |
| 0757-1094 | 28480 | 0757-1094 |
| 1251-0159 | 71785 | 251-15-30-261 |
| 1400-0292 | 95987 | 1/4-6B |
| 1400-0795 | 05593 | SWP-1/4XXT(100') |
| 1810-0044 | 56289 | 200C1791-CRR |
| 1820-0069 | 01295 | SN7420N |
| 1820-0077 | 01295 | SN7474N |
| 1820-0088 | 04713 | MC851P |
| 1820-0256 | 04713 | MC858P |
| 1820-0348 | 04713 | MC844P |
| 1820-0349 | 04713 | MC849P |
| 1820-0376 | 01295 | SN74H40N |
| 1853-0015 | 80131 | 2N3640 |
| 1853-0036 | 80131 | 2N3906 |
| 1854-0071 | 28480 | 1854-0071 |
| 1854-0270 | 80131 | 2N4265 |
| 1901-0040 | 07263 | FDG1088 |
| 1901-0450 | 28480 | 1901-0450 |
| 2100-1758 | 28480 | 2100-1758 |
| 2100-1761 | 28480 | 2100-1761 |
| 2140-0209 | 03508 | 382 |
| 2190-0085 | 00000 | OBD |
| 2190-0416 | 00000 | OBD |
| 2190-0452 | 95987 | D6-140 |
| 2360-0195 | 00000 | OBD |
| 2360-0199 | 00000 | ObD |
| 2420-0001 | 78189 | OBD |
| 3030-0143 | 00000 | OBD |
| 3050-0227 | 80120 | AN960AC-6 |
| $3050-0228$ $8120-1523$ | 80120 | MS15795-305 |

## SECTION IV MAINTENANCE DIAGRAMS

This section contains schematic and parts location diagrams for the read modules of the HP 7970B/7970C Digital Magnetic Tape Units.


Figure 4-1. Density Select Switch Assembly A12, Parts Location Diagram


Figure 4-2. Density Select Switch Assembly A12, Schematic Diagram






Figure 4-3. Read Preamplifier PC Assembly A15, Parts Location Diagram




Figure 46. Read Control PC Assembly A18A1, Patts Location Diagam






