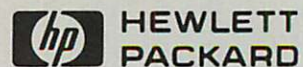
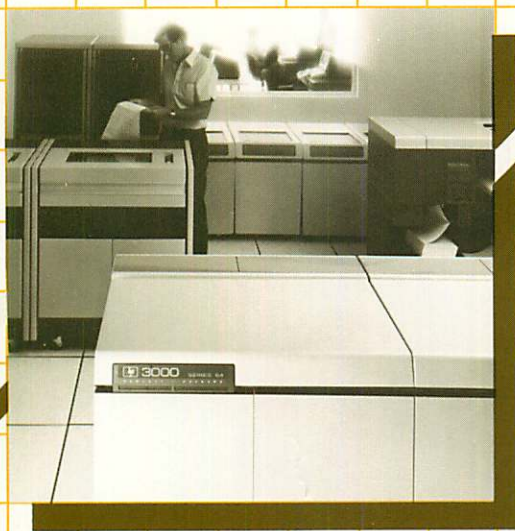


Distributed Systems Network



Advanced Terminal Processor
(DSN/ATP)
Offline Diagnostic Manual



DISTRIBUTED SYSTEMS NETWORK

Advanced Terminal Processor (DSN/ATP) Offline Diagnostic Manual



**INFORMATION NETWORKS DIVISION
19420 HOMESTEAD ROAD, CUPERTINO, CALIFORNIA 95014**

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First Edition March 1982

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First Edition March 1982

PREFACE

This manual describes the Offline Diagnostics for the Advanced Terminal Processor (ATP). The ATP is an asynchronous device controller for HP 3000/44 and HP 3000/64 computer systems. The ATP interfaces with the Intermodule Bus (IMB) for I/O data transfer. A minimum ATP subsystem consists of one System Interface Board, (SIB), and one Hardwired Port Controller or one Modem Port Controller. It requires 2 I/O slots, uses one IMB channel address and supports 12 ports. The maximum subsystem consists of one System Interface Board, and eight Port Controllers. It requires nine slots, uses one IMB channel address and can support 96 terminal ports. An HP 3000/64 computer may have a maximum of 2 ATP subsystems installed, which support 144 terminals. Each ATP subsystem requires one unique IMB channel address.

This manual is written for the HP Customer Engineer (CE) with the assumption that the reader has a good working knowledge of the HP 3000 system environment, and is specifically trained on troubleshooting HP 3000 products. This manual provides information and instructions for setting up the ATP subsystem, and for diagnostic testing. This manual may be used in conjunction with related documentation for the HP 3000 Series 44/64 Computer Systems. Related documents include the following technical manuals:

- HP 3000 Computer Systems, Console Operator's Guide, (for series II/III/30/33/40/44/64) part number 32002-90004.
- HP 3000 Computer Systems, Communication Handbook, part number 30000-90105
- HP 3000 Computer Systems, Systems Manager/System Supervisor Reference Manual, part number 30000-90014
- HP 3000 Distributed Systems Network/Advanced Terminal Processor Installation Manual, part number 30144-90002
- HP 3000 Distributed Systems Network/Advanced Terminal Processor On-Line Diagnostic Manual, part number 30144-90004
- HP 3000 Asynchronous Serial I/O Reference Manual, part number 30000-90250

PREFACE (Continued)

This manual is organized as follows:

Section I, General Information, briefly describes the main areas of importance in terms of diagnostic needs. It includes descriptions of the required software and hardware. It also discusses testing philosophy and limitations of the Advanced Terminal Processor diagnostics.

Section II, Operating Instructions, contains information pertaining to the proper operating procedures for the diagnostics. It explains the commands, prompts and program organization.

Section III, Execution Times, contains information pertaining to approximate run times of the diagnostic tests.

Section IV, Test Descriptions, covers the SIB, AIB and Port Connector test applications. Test explanations and a sample dialog are given.

Section V, Error Interpretation, supplies information for test result analysis. It also supplies sample error messages.

Appendix A, Troubleshooting Flow Chart, supplies information on troubleshooting the subsystem through the use of the diagnostics.

Appendix B, Loopback Hoods, contains pictures of the Loopback Hoods needed for running the Loopback Tests.

Appendix C, Wiring Diagrams, contains pictures for cable wiring.

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GENERAL INFORMATION

SECTION

I

INTRODUCTION

This diagnostic test program confirms correct operation of the System Interface Board, Asynchronous Interface Board, Port Connector Assembly and associated cabling. The Port Connector assembly consists of a Mother Board, either modem or direct connect, three or six Mini-Boards, and one cable. It operates on HP 3000 Series Series 44 and Series 64 systems. Communication with the operator is via the system console.

Hereafter, in this document, the following acronyms will be used:

System Interface Board.....SIB
Asynchronous Interface Board.....AIB
Advanced Terminal Processor.....ATP

Board replacement is the standard operating procedure and the diagnostics are designed to easily identify malfunctioning boards within the ATP system. The diagnostics allow you to run specific individual tests or all the tests as a group. After all the tests have been run on a particular board, a pass/fail indication will be displayed to indicate which SIB/AIB has passed or failed. We recommend you run the diagnostics by issuing the "ALL" command rather than specifying particular individual tests.

REQUIRED HARDWARE

The following hardware is required:

- a. A minimal mainframe configuration.
- b. A minimal ATP system, ie: one SIB, one Port Controller, which consists of one AIB and one Port Connector Assembly, either Modem or Direct Connect.
- c. Loopback Hoods which are included in the product support package (p/n 30144-67801).

One Standard 72 Pin Edge Connector	30145-60005
Twelve 25 Pin Hoods for HP-Modem B Connection	30146-60002
Twelve 3 Pin Hoods for HP-DC B Connection	30148-60002
Twelve 5 Pin Hoods for HP-DC A Connection	30147-60002

General Information

If necessary, the SIB can be tested without an AIB being present. Also, the AIB can be tested without Port Connectors being present. However, the most thorough testing is done with all ATP hardware installed.

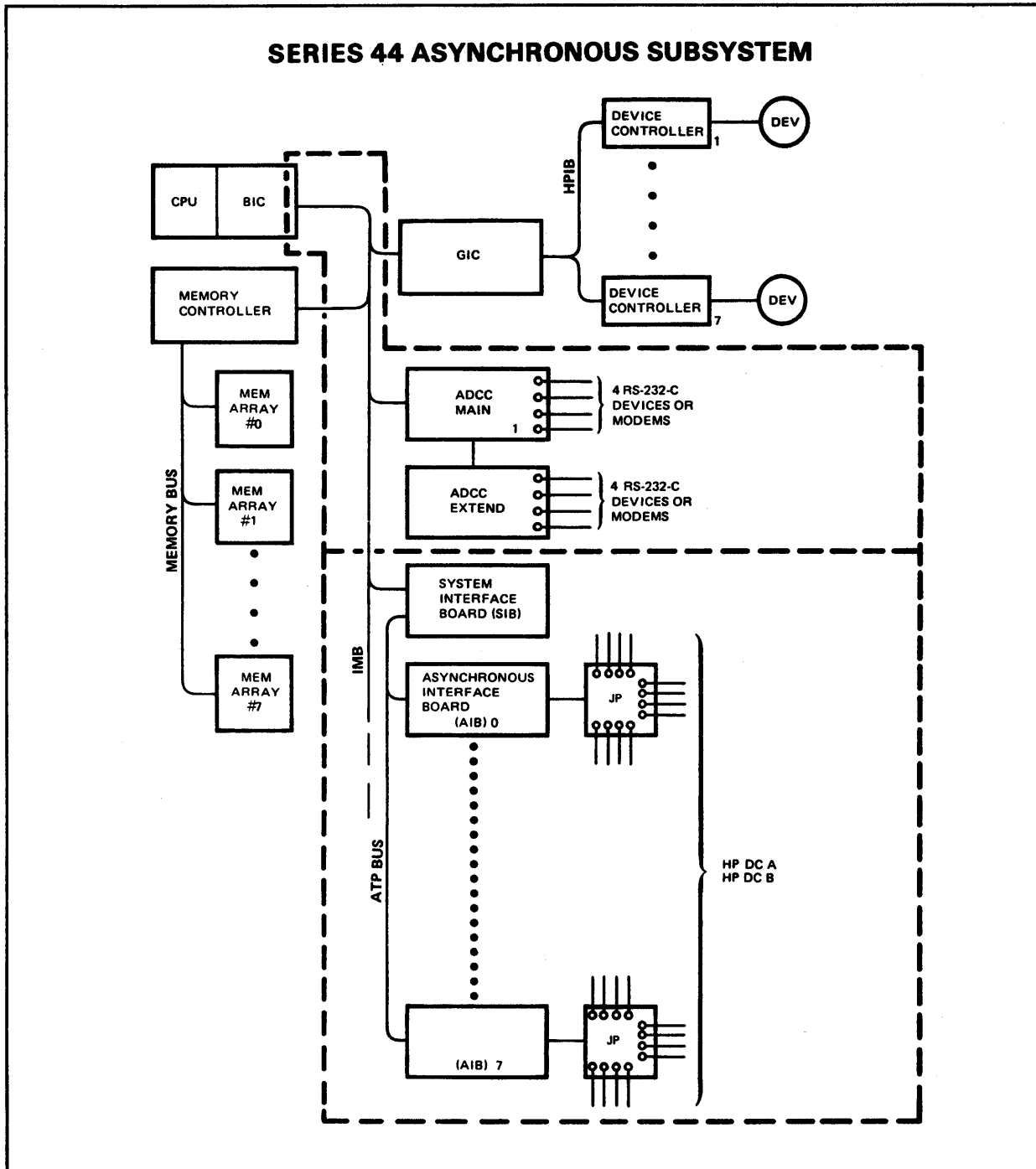


Figure 1-1. Series 44 Asynchronous Subsystem

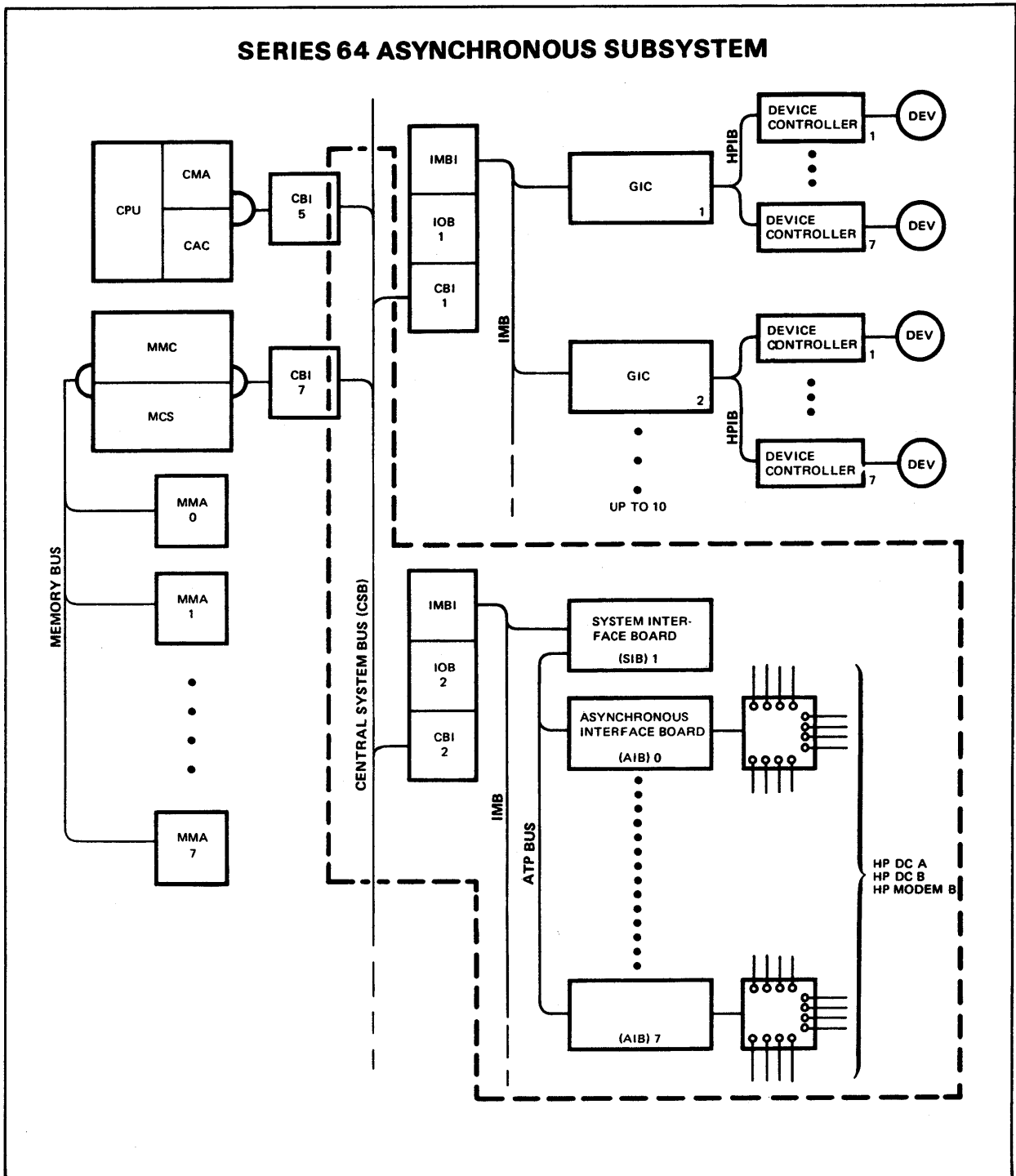


Figure 1-2. Series 64 Asynchronous Subsystem

General Information

REQUIRED SOFTWARE

The Diagnostic Utility operating System (DUS) tape or diskette, and the ATP Offline Diagnostics are required.

TESTING PHILOSOPHY

The offline diagnostics are designed to test the ATP hardware and a subset of the code resident in the Port Controller Chips (PCC), Modem Controller Chips (MCC), and Modem Scanner Chips (MSC), if applicable. Only a subset of the code can be tested because it is impossible to emulate all of the actions of terminals and/or modems simply by using loopback mechanisms. The SIB must be functioning correctly in order for the other components of the ATP to be tested. The recommended procedure is to initiate the diagnostics by thoroughly exercising the SIB to ensure that it is operating correctly. To initiate the SIB tests, respond with the "ALL" reply when prompted by the diagnostic. If the console goes through the SIB under test, the results must be directed to a line printer. Ensure that the line printer is on-line before you test the SIB. If the diagnostics find that the SIB is properly operating, testing of the AIB commences. It is recommended that the "ALL NO LOOPBACK" tests be run first. If these tests fail, the AIB must be replaced. If they pass, the loopback test should be performed with loopback hoods on the Port Connectors. If these loopback tests fail, loopback tests should be performed with loopback hoods on the AIB. By performing the tests in this sequence and through the use of multiple loopback hoods, each port on AIB is tested individually to ensure that the logic associated with it is operating. Thus all the ports on the AIB under test are analyzed.

DIAGNOSTIC LIMITATIONS

The diagnostic test limitations of the ATP are the following:

1) When the console is connected to the SIB under test, the messages must be output to a line printer. Make sure that the line printer being used is on line, when the DUS is brought up.

2) In order to be able to initiate the ATP offline diagnostics, the console port must be working. Therefore the console microdiagnostics supplied with the SPU microdiagnostics must be relied upon for diagnosing the console if there are any problems with it.

3) Sometimes it will be difficult to isolate the problem area to either the SIB or the AIB unless there are known good SIBs and/or AIBs with which to test.

OPERATING INSTRUCTIONS

SECTION

II

INTRODUCTION

The ATP diagnostics are designed to be operated easily. The tests can be run individually if so specified or as a group. We recommend that you do not specify individual tests since by running the tests as a group you will receive the same results in a much faster time.

To operate the diagnostics, the following steps must be executed:

- (1) Load the Diagnostic/Utility System (DUS) Tape or Diskette
- (2) Bring up the Diagnostic/Utility System (DUS)
"Enter Program Name" is displayed.
- (3) Respond 'ATPDIAG' to initiate the Diagnostic.
The ATP Diagnostic Program displays its title message and prompts for the Channel # of the SIB.

Respond accordingly to the questions presented.

MESSAGES AND PROMPTS

Four types of messages are output by the diagnostic: prompt, help, information and error messages.

Prompt messages (e.g., which channel number to test, etc.) require you to input the requested information.

Help messages are displayed whenever the HELP command is given, and provide a more complete description of what is needed.

Information messages (e.g., pass/fail) are displayed with no program pause.

Error messages are used to tell you when the ATP responded unexpectedly to a given stimulus. Error messages are normally inhibited. These are of the most use when doing actual debugging and repair of the individual boards.

Operating Instructions

Before the diagnostics are started you can specify whether the diagnostics should stop after the first error or whether they should continue to test as much of the system as possible. You can also specify whether success messages or failure messages should be printed. We recommend you respond with a NO to the questions concerning errors and messages, since the results will be summarized at the end of the diagnostic testing.

SAMPLE DIALOG

Advanced Terminal Processor Offline Diagnostic V-00.20

Enter HELP in response to any question for an explanation of what is required.

Enter EXIT in response to any question to terminate the program.

Channel number of IMB interface SIB is attached (0-3) 0
SERIES 64 ONLY

Enter the channel number of the SIB under test: 1
Print failure messages? NO
Print success messages? NO
Output results to line printer? YES
Stop on errors? NO
Loop count-(zero for continuous looping): 1
Enter SIB tests to be run:
>ALL
Enter AIB tests to be run:
>ALL NO LOOPBACK
Enter ports to be tested, separated by commas:
>AO

EXECUTION TIMES

SECTION

III

INTRODUCTION

The exact execution time for each test or for a group of tests is determined by the following constraints:

- the number of ports under test
- the computer system on which the test is being conducted (Series 44, 64)
- the selection of test sections to be executed

BOARD	TEST	APPROXIMATE RUN TIME
SIB	ALL	<10 seconds
AIB	ALL NO LOOPBACK	<2 minutes

EXAMPLE:

The total run time per pass on a fully loaded Series 64 with eight AIBs and 96 ports with no errors is:

SIB	ALL	2 seconds
AIB	ALL NO LOOPBACK	36 seconds

The execution times listed above are based on the fastest time; slower machines, of course, will result in slower pass times.

DESCRIPTION OF TESTS

SECTION

IV

ATP OFFLINE DIAGNOSTIC TESTS

Following is an explanation of the ATP Offline Diagnostic tests. You must specify which SIB to test to the diagnostics. The diagnostics ask for the channel address of the SIB and the ports which are to be tested. Listed below are all of the sub-tests involved in the diagnostics. The diagnostics run through all of the sub-tests in sequence.

OFFLINE DIAGNOSTIC ORGANIZATION

The SIB is considered to be the foundation of the ATP system. All of its modules must be operational in order to be able to communicate with any ports. Therefore, the SIB modules are tested first. These modules are:

- 1) Logic for responding to IMB commands,
- 2) registers,
- 3) memory,
- 4) DMA State Machine, and
- 5) ATP Bus State Machine.

Each port on the AIB is tested individually, in succession. The test on each port involves the following tests:

- 1) PCC self-test,
- 2) PCC RAM dump,
- 3) PCC/MCC Communication,
- 4) PCC diagnostic loopback,
- 5) PCC loopback of data signals offboard--requiring loopback hood.
- 6) MCC/MSC self-test which sends results back to the mainframe, and
- 7) MCC/MSC RAM Dump.

Description of Tests

SIB Tests

Following is a list of test names that can be performed on the SIB:

- | | | |
|------|----------------------------|------|
| (1) | IMB-SIB Communication | (IM) |
| (2) | Initial Register Values | (IN) |
| (3) | SIB Memory | (M) |
| (4) | Sequencing | (SE) |
| (5) | Time Out | (T) |
| (6) | Board Counter/Enable | (BO) |
| (7) | ATP Bus Buffers | (L) |
| (8) | Direct Command | (DI) |
| (9) | FIFO | (F) |
| (10) | DMA State Counter | (ST) |
| (11) | DMA Address Counter | (DM) |
| (12) | Comp/Counter Loopback | (C) |
| (13) | Read IMB | (R) |
| (14) | Write IMB | (W) |
| (15) | Begin Flag/Left-Right Flag | (BE) |
| (16) | None | (N) |
| (17) | All | (A) |

The test names may be abbreviated as indicated. You may enter a list of tests, separated by semi-colons. ALL indicates that all available SIB tests are to be run. NONE indicates that testing of the SIB will not be done. Pressing carriage return in response to this question will cause the last SIB tests specified (if any) to be retained.

NOTE: ALL is the recommended response.

TEST

DESCRIPTION

IMB-SIB
COMMUNICATION

This procedure does preliminary testing of the SIB determining that all the allowable IMB commands can be executed.

INITIAL REGISTER
VALUES

This procedure tests the values obtained from the readable registers after initialization.

Description of Tests

SIB MEMORY	This procedure tests the memory on the SIB. This memory is used to store the IMB memory offset, pack byte and flags associated with each of the 128 DMA paths. It is tested by writing/reading a checkerboard pattern and writing/reading the address of each location. The checkerboard test is done with the MDiag bit of the diagnostic control register both on and off. This tests all of the pack byte, as well as the flags.
SEQUENCING	This procedure tests the sequencing of the ATP bus state machine. It sets up a given set of conditions (e.g. no direct command, bus opcode=idle, board enabled) and then checks the ATP bus as it single stepped through the logic.
TIMEOUT	This routine tests the timeout which terminates the wait for either BusEnd from the ATP bus, or Halt from the DMA state machine.
BOARD COUNTER/ENABLE	This procedure tests the operation of the board counter on the SIB. It checks that the counter is incremented each time the ATP bus state machine passes through state zero. The counter must be checked by disabling all but one board, and checking when the state machine sees the current-board-enabled signal.
ATP BUS BUFFERS	This procedure tests the ATP Bus buffers. It first uses DMA test code to write data to the ATP bus and reads the looped back data. It then makes sure that the value of the port pointer looped back matches the value written into the port pointer register.
DIRECT COMMAND	This procedure tests the data paths which get a direct command to the ATP Bus.
FIFO	This procedure tests the operation of the FIFO which stores the number of each port wishing to generate an interrupt.
DMA STATE COUNTER	This procedure checks the function of the DMA state counter. It sets up an opcode which points to diagnostic DMA code containing all NOPS. This test simply checks that the counter increments each time until it gets to the halt command, and then resets to zero.

Description of Tests

DMA ADDRESS COUNTER This procedure uses test 1 of the diagnostic DMA code to check the operation of the DMA address counter. After an channel initialization, the counter value should be preset to !FFFF. On the next increment it should overflow and go to zero. It will then count up from zero. Each value of the counter will be stored in memory.

COMP/COUNTER LOOPBACK This procedure tests the DMA logic's COMP register and address counter. It loads the DMA registers from memory, and then runs the test which dumps the registers back to memory.

READ IMB This procedure tests an IMB read operation using the diagnostic DMA routine which reads a single word from the IMB and puts it in the SIB RAM.

WRITE IMB This procedure tests an IMB write operation using the diagnostic DMA routine which writes a single word from the SIB RAM and puts it in IMB memory.

**BEGIN FLAG/
LEFT-RIGHT
FLAG** This procedure tests the operation of the BeginFlag and LeftRightFlag on the SIB. The basic tool used in this test is the diagnostic DMA operation which increments the counter a different number of times for each state of BeginFlag and LeftRightFlag, then stores the count in memory. First each of the four possible states are written to SIB memory register 1 and the test is used to check that the DMA logic sees the correct value of the flags. Then the BeginFlag, LeftRightFlag are both set to 1 and the test is used to check the automatic updating of the flags.

Port Controller Tests

Nine diagnostic tests are performed on the AIB and Port Connector Assembly. The test names are listed below:

AIB

- | | | |
|------|---------------------------------|---------|
| (1) | Port Controller Chip Self-Test | (PCC S) |
| (2) | Modem Controller Chip Self-Test | (MCC D) |
| (3) | Port Controller Chip Dump | (PCC D) |
| (4) | Modem Controller Chip Dump | (MCC D) |
| (5) | PCC-MCC Communication | (PCC M) |
| (6) | Diagnostic Loopback | (D) |
| (7) | Off-board Loopback | (L) |
| (8) | ALL | (A) |
| (9) | All no Loopback | (ALL N) |
| (10) | None | (N) |

MODEM PORT CONNECTOR ASSEMBLIES

- (11) Modem Scanner Chip Self Test
- (12) Modem Scanner Chip Dump

The test names may be abbreviated as indicated. You may enter a list of tests separated by semi-colons. ALL indicates that all available AIB tests are to be run. ALL NO LOOPBACK indicates all AIB tests, except those which require a loopback hood, are to be run. NONE indicates that testing of the AIB is not to be done. Pressing carriage return in response to the prompt will cause the last AIB tests specified (if any) to be retained.

NOTE: ALL NO LOOPBACK is the recommended response when using the diagnostics. If loopback connectors have been installed, ALL is recommended.

Excluding the Modem Scanner Chip self-test and the Modem Scanner Chip dump, which cannot be separated from their MCC counterparts, each test is run individually, and the diagnostics are designed to run the tests sequentially in an order which exercises all the necessary components.

Before you begin the diagnostic tests, the AIB can be tested by initiating the on-board diagnostic as explained below. The offline diagnostic can then begin with the testing of the SIB. After it has been determined that the SIB is functioning properly, diagnostic tests on the AIB may begin.

- a. Flip the tiny toggle momentary switch on the edge of the AIB PCA to manually reset the AIB so that the self-test can be initiated. To initiate the self-test, use a screwdriver or a similar tool to short out Test Point 5 and Test Point 7, which are between the Junction Panel power switch and the thumbwheel switch on the AIB. (See figure 2-7 in Installation Manual).

Description of Tests

- b. Watch the 13 self-test light-emitting-diode (LED) indicators as the self-test program goes through its cycle. Upon completion of the self-test (approximately one second in duration), the LEDs will stop blinking. If no LEDs are lit, the AIB is working properly. If any LEDs are still lit, the AIB is malfunctioning.

The steps above test 90% of the logic on the chips on the AIB board. Once you have confirmed that the AIB chips are functioning, you can begin the AIB diagnostic tests. The diagnostics are able to pinpoint which board is malfunctioning and needs to be replaced. The response for each test is pass or fail. Since board replacement is the standard operating procedure, pass/fail is the only information needed from the diagnostic tests.

A quick way to check if the Modem Scanner Chip is properly functioning on the Modem Mother Board is to attach loopback hoods on the mini-boards and flip the momentary toggle switch on the rear of the mother board. If the LED remains lit, the mother board is malfunctioning and should be replaced. This test checks the modem logic on the mother board and therefore should not be used when the diagnostics are running.

TEST	DESCRIPTION
SELF TESTS (3)	This procedure verifies the operational status of the PCC. The maskable interrupt path to the PCC/MCC/MSD and the data and control paths from the PCC to the mainframe are tested.
PORT CONTROLLER CHIP	The tests exercise all the PCC's and return the results to the mainframe.
MODEM CONTROLLER CHIP	The self-tests includes a ROM check-sum, a RAM diagnostic and a timer test.
MODEM SCANNER CHIP	
DUMP TESTS (3)	This procedure freezes the PCC, issues a dump command and dumps the contents of RAM and Control Registers to mainframe memory. The non-maskable interrupt path to the PCC, the maskable interrupt path and the freeze code in the PCC are all tested. The test also writes known data from the PCC to the mainframe.
PORT CONTROLLER CHIP	
MODEM CONTROLLER CHIP	
MODEM SCANNER CHIP	
PCC-MCC COMMUNICATION	This procedure checks the data path between the PCC and the MCC and the PCC code involved in talking to the MCC, by having the PCC write one byte to the MCC and read one byte from the MCC.

Description of Tests

DIAGNOSTIC LOOPBACK

This procedure loops back 256 bytes of data as far as the PCC, but not to the UART or the Port Connector assembly. The data sent is very specific and the PCC expects the bytes in a specified order. If a byte is received out of order, the PCC interrupts the mainframe. During the test the diagnostics check the data and can now see whether the error occurred on the write path to the PCC or on the read path from the PCC.

OFF BOARD LOOPBACK TEST

This procedure reads data from the mainframe and writes it back to the mainframe through the use of a loopback hood. The read and write paths from and to the mainframe are tested. The test will send 62 bytes to the PCC and then back to the mainframe and the data is compared. This test requires the use of one or more of the supplied loopback hoods.

NOTE: In order to execute this test, you must place the loopback hood on the mini-boards or the AIB. If the loopback hood is placed on the AIB, you must power OFF the Port Connector Assembly via the power switch on the appropriate AIB. (See figure 4-1) This must be done in order to remove the port connector cable from the AIB and place the loopback hood on. When placing the loopback hoods on the mini-boards, the power may be on or off, however, when running the tests, the power out to the junction panel must, of course, be on.

The loopback test can exercise the AIB or the Port Connectors. If the hood is placed on the AIB, the SIB and AIB are tested. If it is placed on the Port Connectors, the SIB, AIB and Port Connectors are tested. If the AIB loopback fails, the AIB is malfunctioning. If the loopback passes the AIB test, but the Port Connectors fail, either the Port Connector cable is bad or a Port Connector is bad.

Description of Tests

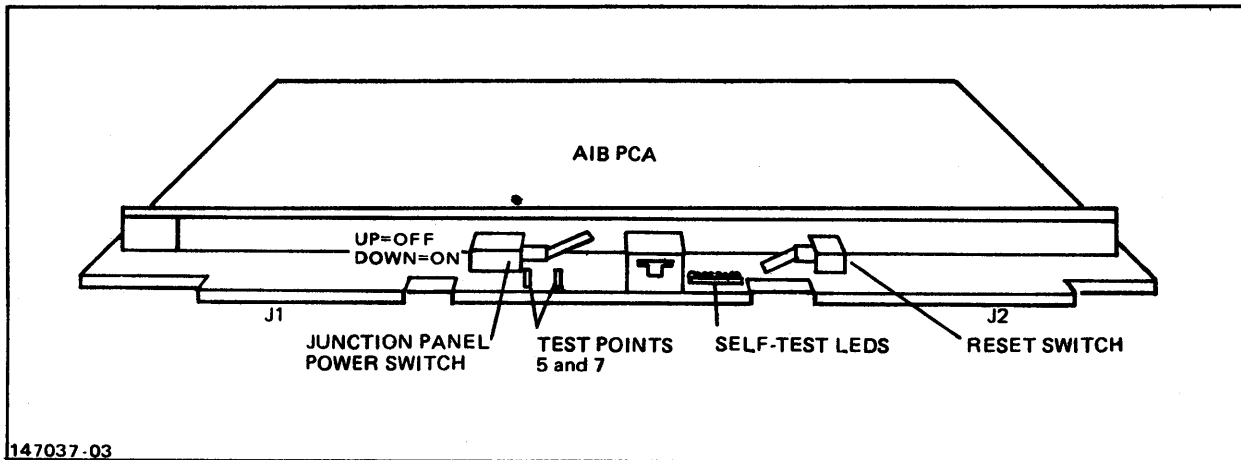


Figure 4-1. Location of AIB Power Switch

ERROR INTERPRETATION

SECTION

V

ANALYSIS OF TEST RESULTS

As each sub-test is completed, the diagnostic records a pass/fail indication for that sub-test and any pertinent information related to it. If a failure has occurred but it is still possible to proceed with other sub-tests, the diagnostics will do so unless you have previously specified stopping after the first error. At the end of the entire test, the diagnostic analyzes the test data and displays the results. The following examples are a representation of the messages that will be displayed after the tests have completed running.

SIB Test Results

SIB testing completed-without errors

Error(s) were detected during testing of the SIB.
Testing of the AIB will not be done.

AIB Test Results

AIB# 0		PASSED
AIB# 1		PASSED
AIB# 2		PASSED
AIB# 3	Port 2	FAILED
AIB# 4		PASSED
AIB# 5	Port 11	FAILED
AIB# 6	Port 7	FAILED

Error Interpretation

The recommended procedure for running the diagnostics is to respond no to the questions prompting for error messages to be printed. However, if you respond yes, the diagnostics will output error messages in three distinct formats. The responses will not be identical to the examples given, but the formats will be very similar. The information given will supply the user with the name of the board tested, the test exercised and the results of the test. Examples of the formats are listed below:

NOTE: These messages will only be displayed if you ask for success/failure messages to be printed. We do not recommend such an action and list the following for informational purposes only.

SIB Test Error Message Example

```
*** SIB Error      In: FIFO (test name)
Expected: %377;    Received: %357. Bad data read from
interrupt FIFO.
```

SIB Hardware Error Test Example

```
SIB hardware error detected:
  ATP Bus Timeout
```

AIB Test Error Message Example

```
AIB# 0      PORT# 1      FAILED  Real Loop (test name)
Receive buffer did not compare with source buffer.
Expected buffer
0123456789ABCDEF GHIJKLMNOPQRSTUVWXYZabcdefghijklmnopqrst
Received buffer
01234567899ABCDEF GHIJKLM
```

Error Interpretation

The following is an example of the diagnostic test results. The SIB is exercised first, followed by the AIB tests.

IMB-SIB communication test	passed
Initial Register Value test	passed
SIB Memory test	passed
ATP Bus State Sequencing test	passed
Timeout test	passed
Board Counter test	passed
ATP Bus Buffer test	passed
Direct Command test	passed
FIFO test	passed
DMA State Counter test	passed
DMA Address Counter test	passed
Comp Reg/Address Counter test	passed
IMB Read test	passed
IMB Write test	passed
BeginFlag/LeftRightFlag test	passed

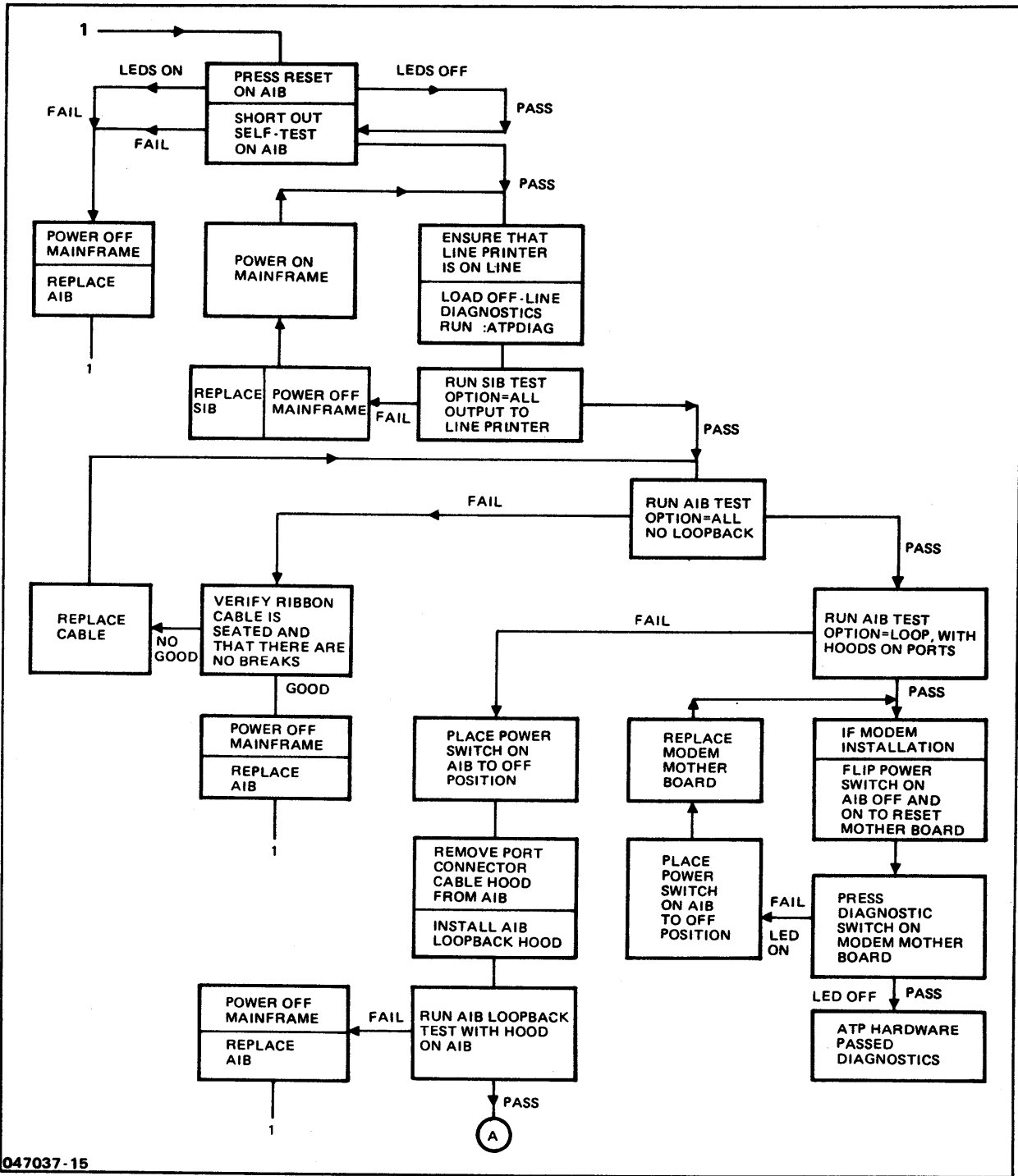
SIB testing completed - without errors

AIB# 0	PORT# 1	PASSED	SELF TEST
AIB# 0	PORT# 1	PASSED	DUMP TEST
AIB# 0	PORT# 1	PASSED	PCC/MCC/MSC SELF TEST
AIB# 0	PORT# 1	PASSED	MCC DUMP TEST
AIB# 0	PORT# 1	PASSED	PCC MCC TEST
AIB# 0	PORT# 1	PASSED	DIAGNOSTIC LOOP
AIB# 0	PORT# 1	PASSED	REAL LOOP
AIB# 0	PORT# 2	FAILED	SELF TEST
AIB# 0	PORT# 2	FAILED	DUMP TEST
AIB# 0	PORT# 2	FAILED	PCC/MCC/MSC SELF TEST
AIB# 0	PORT# 2	FAILED	MCC DUMP TEST
AIB# 0	PORT# 2	FAILED	PCC MCC TEST
AIB# 0	PORT# 2	FAILED	DIAGNOSTIC LOOP
AIB# 0	PORT# 2	FAILED	REAL LOOP

TROUBLESHOOTING FLOW CHART

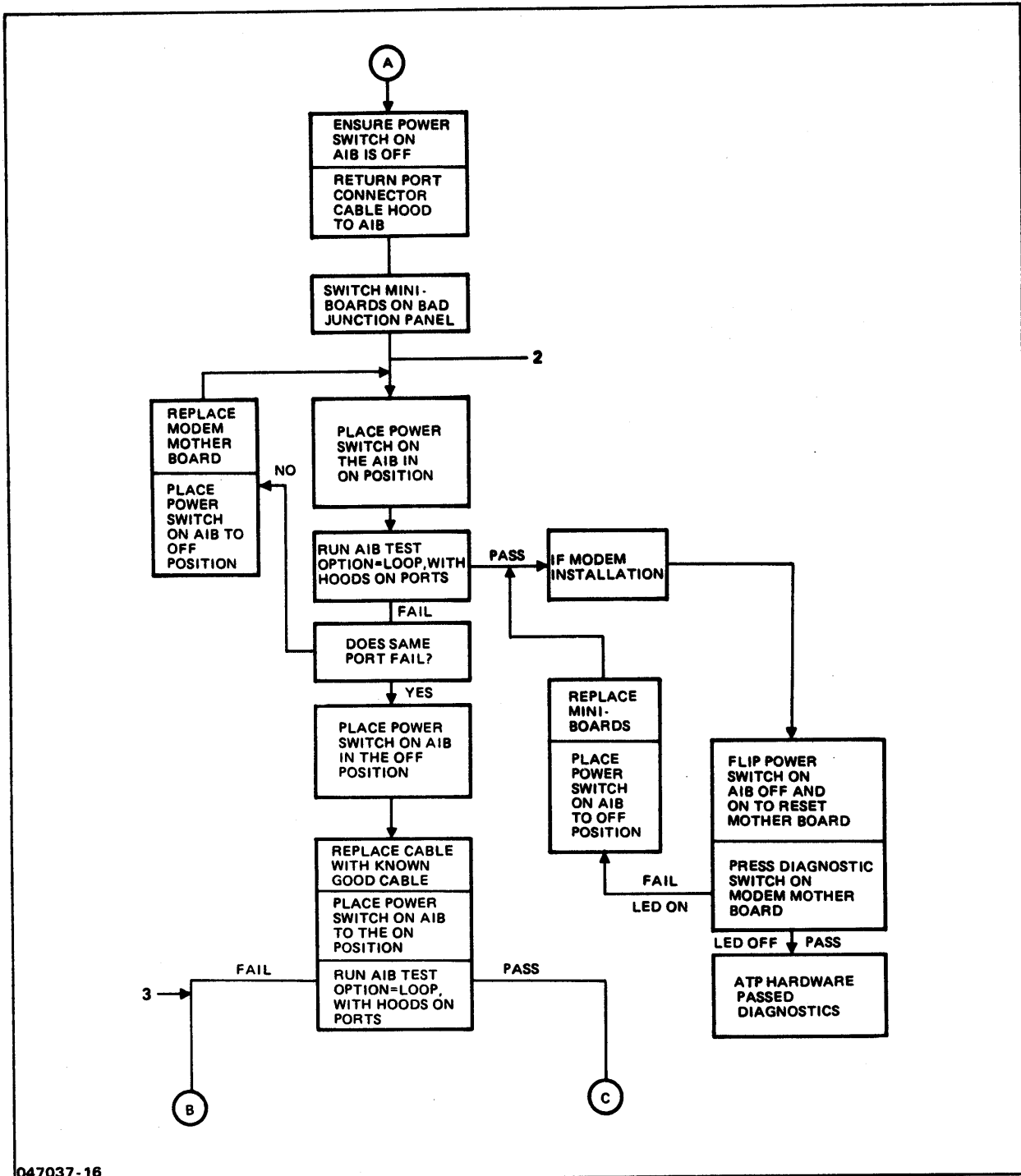
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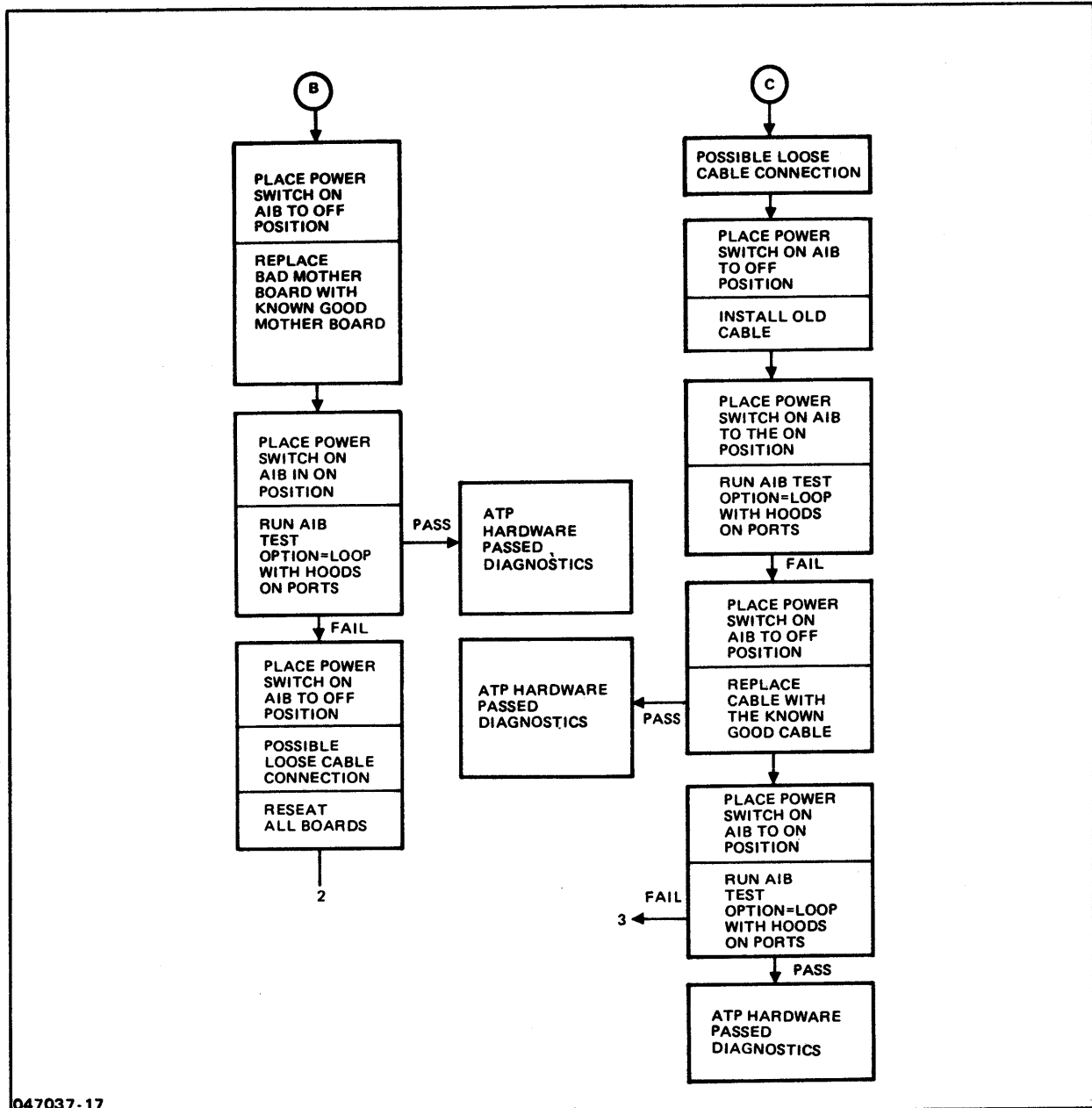


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Appendix A



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LOOPBACK HOODS

APPENDIX

B

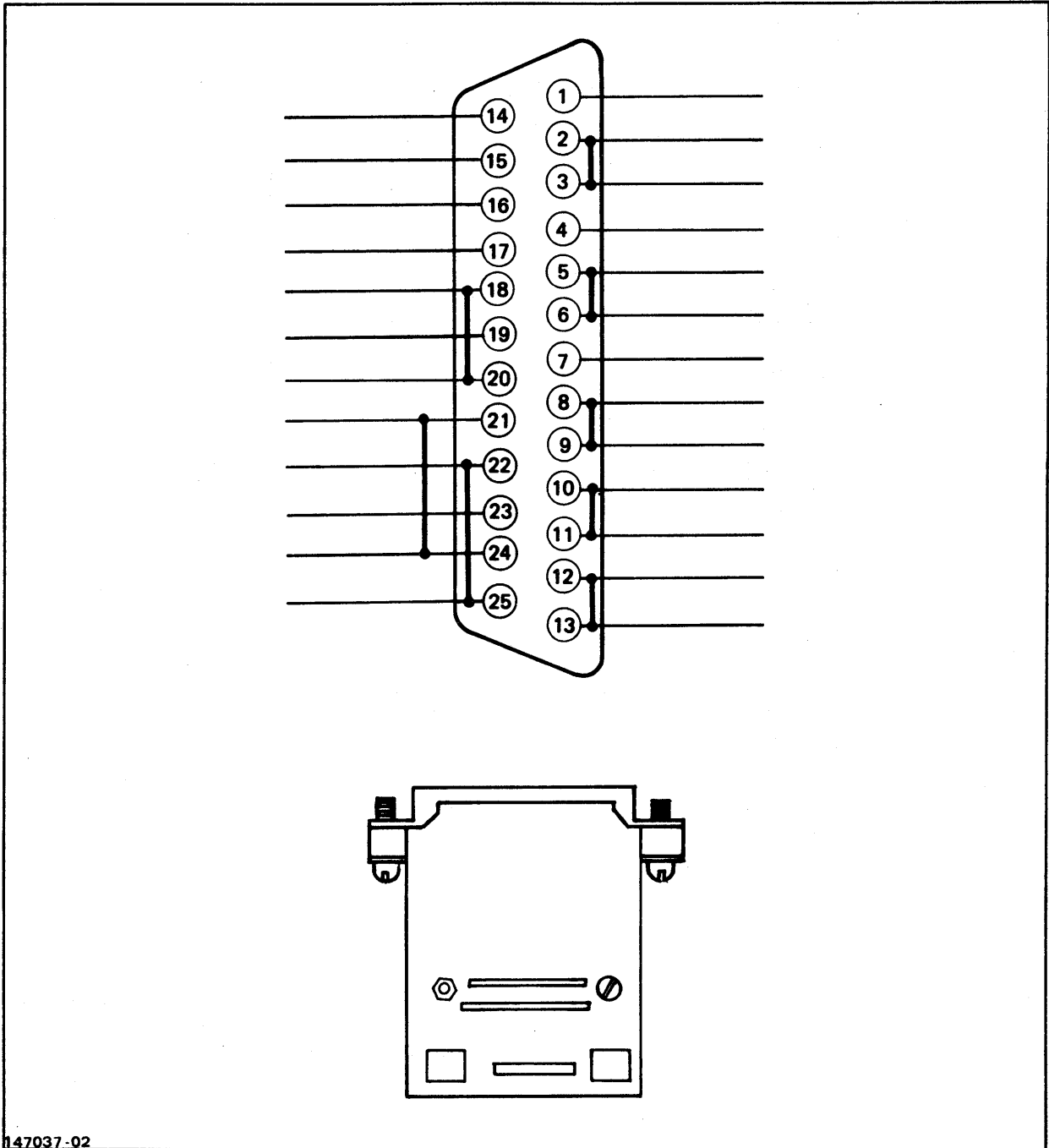
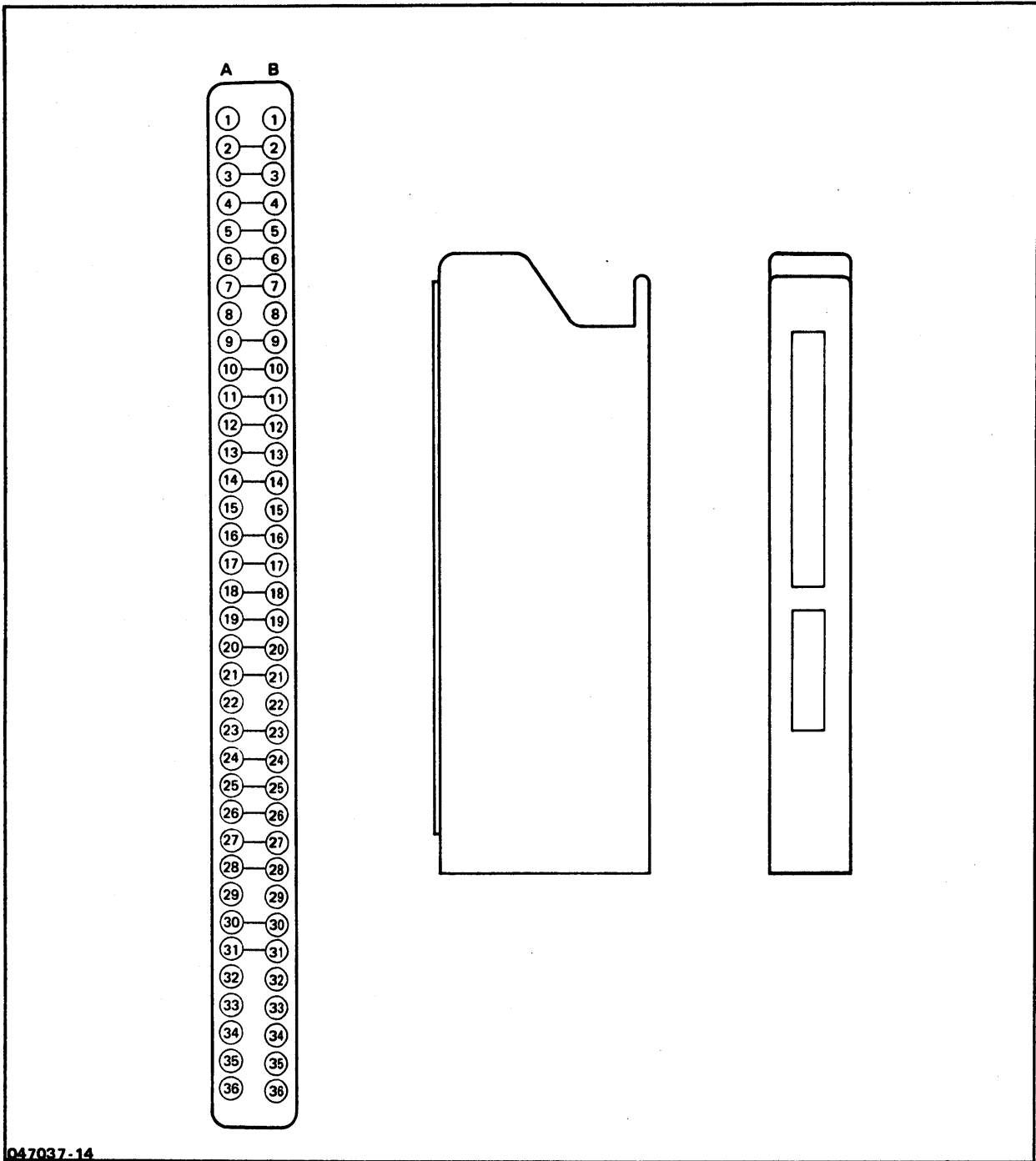


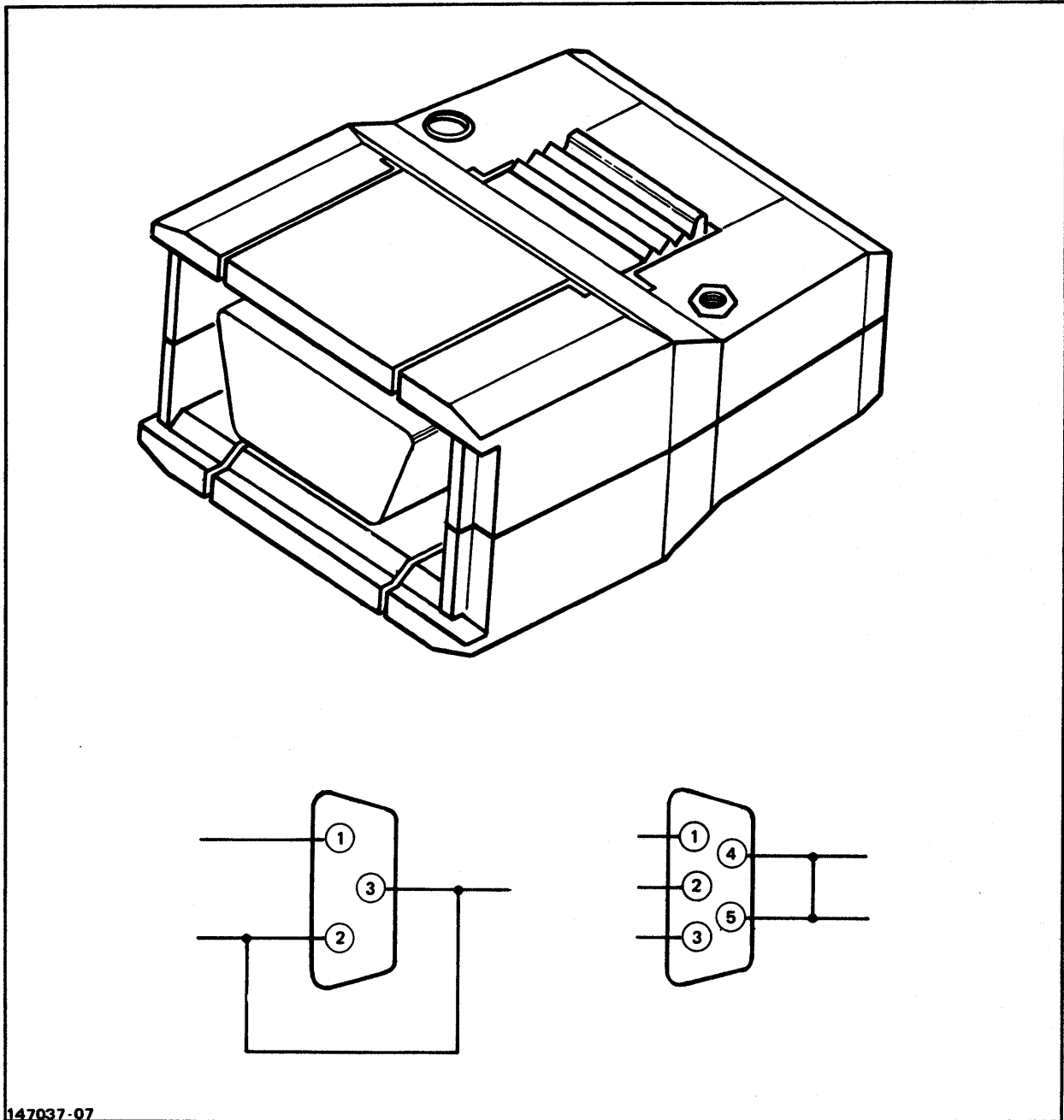
Figure B-1. HP-Modem B Loopback Hood

Appendix B



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Figure B-2. AIB Loopback Hood



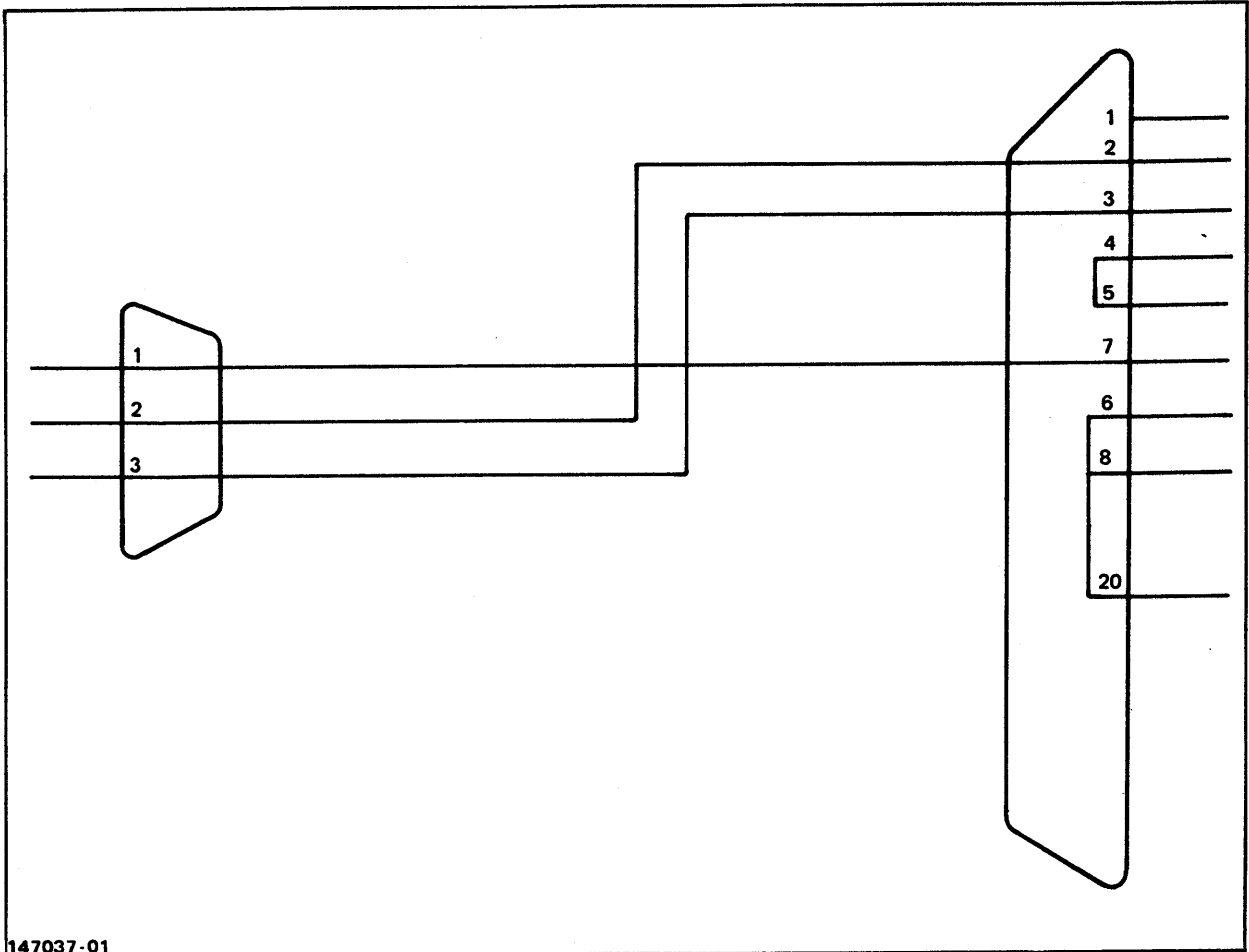
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Figure B-3, HP DC A and HP DC B Loopback Hoods

WIRING DIAGRAMS

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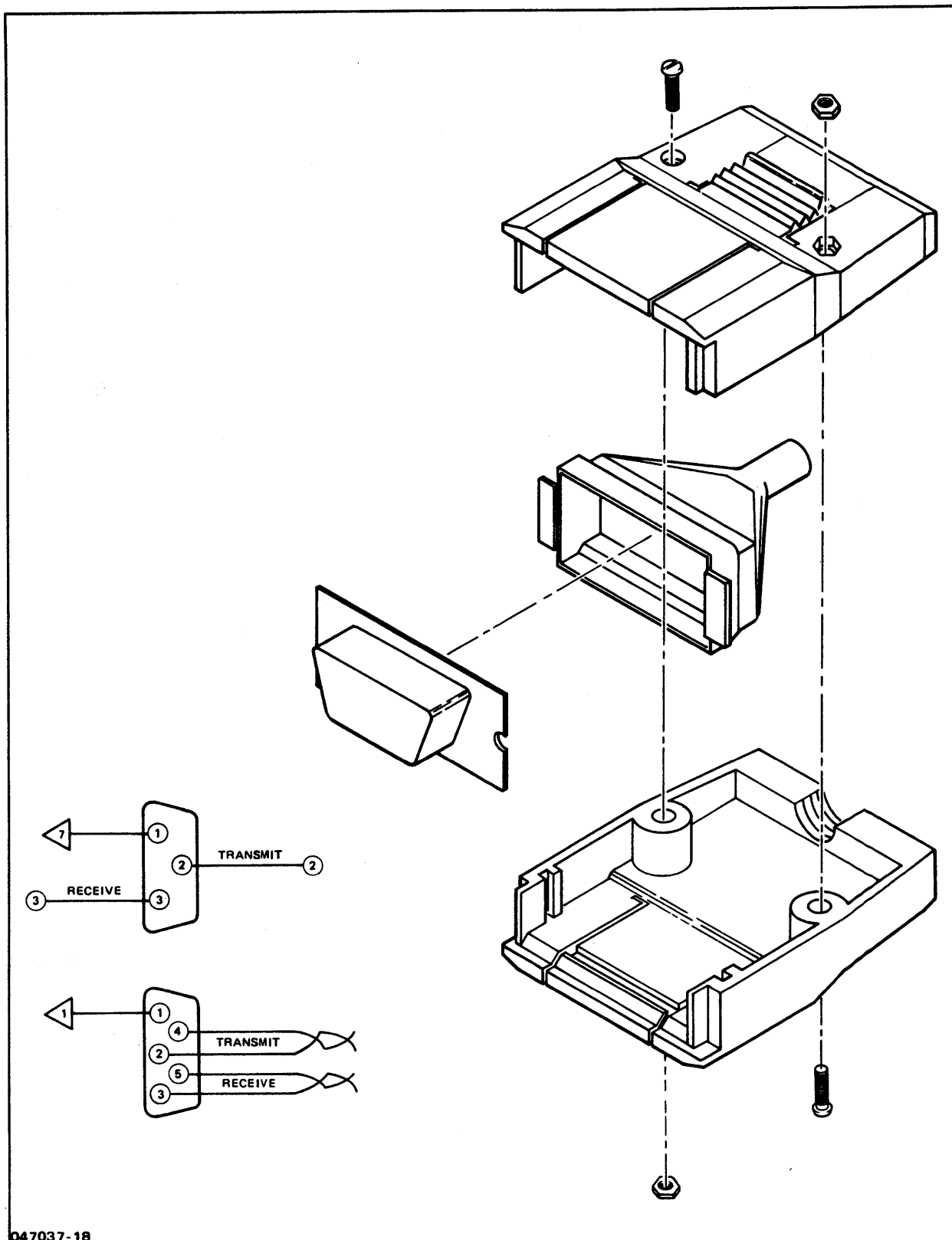
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Figure C-1. Wiring Diagram for HP DC B Adapter Cable

Appendix C



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Figure C-2. Cable Wiring for HP DC A and HP DC B

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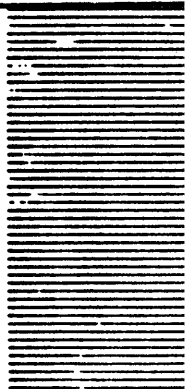
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See United Kingdom



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Arranged alphabetically by country

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Telex: 215962 RKAR GR
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Eliopoulos Brohers Ltd.
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Bldg. Gloucester
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Tel: (5) 200922
Telex: 85148 CET HX
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Schmidt & Co. (Hong Kong) Ltd.
18th Floor, Great Eagle Centre
23 Harbour Road, Wanchai

HONG KONG

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Elding Trading Company Inc.
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Blue Star Ltd.
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Telex: 041-379
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Cable: BLUEFROST
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SECUNDERABAD 500 003

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CASABLANCA
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A,CH**,E,M



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Arranged alphabetically by country

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CH,CS,CM,E,P

Northrop Instruments & Systems Ltd.
369 Khyber Pass Road
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A,M

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Sturdee House
85-87 Ghuznee Street
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See United Kingdom

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N-1345 OCUSTERÅS

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OMAN

Khimjil Ramdas
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MUSCAT

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Suhail & Saud Bahwan
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MUSCAT

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Telex: 3274 BAHWAN MB
E

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MUTRAH

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Telex: 5741 Tawoos On
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Cable: FEMUS Islamabad
A,E,M,P*

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Telex: 2894 MUSKO PK

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Apartado 4929

PANAMA 5

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Telex: 3483 ELECTRON PG
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Los Flamencos 145, San Isidro
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LIMA 1

Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

SAMS

Río De La Plata 305

SAN ISIDRO

Tel: 419928
Telex: 394 20450 PELIBERTAD
P

PHILIPPINES

The Online Advanced Systems
Corporation

Rico House, Amoroso Cor. Herrera
Street

Legaspi Village, Makati
P.O. Box 1510

Metro MANILA

Tel: 815-38-11 (up to 16)
Telex: 63274 Online PN
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Electronic Specialists and
Proponents Inc.

690-B Epifanio de los Santos
Avenue

Cubao, QUEZON CITY

P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83

Telex: 40018, 42000 ITT GLOBE MAC-
KAY BOOTH
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PORTUGAL

Mundinter
Intercambio Mundial de ComAercio
S.A.R.L.

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P-LISBON

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M

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Av. da Liberdade, 220-2
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P

Telectra-Empresa Técnica de
Equipamentos Eléctricos S.A.R.L.

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P-LISBON 1

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CM,E

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