64000

HP64000 Logic Development System

Model 64304A Emulation Bus Preprocessor

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its option, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environment specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

FOLD HERE

HEWLETT PACKARD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY CARD

FIRST CLASS PERMIT NO. 1303 COLORADO SPRINGS, COLORADO

POSTAGE WILL BE PAID BY ADDRESSEE

HEWLETT-PACKARD

Attn: Logic Publications Dept.
Centennial Annex - D2
P.O. Box 617
Colorado Springs, Colorado 80901-0617

FOLD HERE

Your cooperation in completing and returning this form will be greatly appreciated. Thank you.

READER COMMENT SHEET

Part Number: 64304-90902

Your comments are important to us. Please answer this questionaire and return it to us. Circle the number that best describes your answer in questions 1 through 7. Thank you.

1. The information in this book is complete:

Doesn't cover enough (what more do you need?)	1	2	3	4	5	Covers everything

2. The information in this book is accurate:

Too many errors	1	2	3	4	5	Exactly right

3. The information in this book is easy to find:

I can't find things I need	1	2	3	4	5	I can find info quickly

4. The Index and Table of Contents are useful:

Helpful	1	2	3	4	5	Missing or inadequate

5. What about the "how-to" procedures and examples:

No help	1	2	3	4	5	Very helpful
Too many now	1	2	3	4	5	I'd like more

6. What about the writing style:

Confusing	1	2	3	4	5	Clear

7. What about organization of the book:

Poor order	1	2	3	4	5	Good order

8. What about the size of the book:

too big/small	1	2	3	4	5	Right size

Comments: _____

_____

_____

_____

Particular pages with errors?

_____

Name (optional): _____

Job title: _____

Company: _____

Address: _____

Note: If mailed outside U.S.A., place card in envelope. Use address shown on other side of this card.

Emulation Bus Preprocessor

LOGIC SYSTEMS DIVISION
COLORADO SPRINGS, COLORADO, U.S.A.

Printing History

Each new edition of this manual incorporates all material updated since the previous edition. Manual change sheets are issued between editions, allowing you to correct or insert information in the current edition.

The part number on the back cover changes only when each new edition is published. Minor corrections or additions may be made as the manual is reprinted between editions. Vertical bars in a page margin indicate the location of reprint corrections.

First Printing..... August 1983 (Part No. 64304-90902)

Reprinted..... October 1983

Table of Contents

List Of Illustrations

List Of Tables

Chapter 1

GENERAL INFORMATION

The Model 64304A Emulation Bus Preprocessor is a 64000 series emulation probe for the Model 64620S 10-MHz Logic State/Software Analyzer. It brings the powerful feature set of the Model 64620S to the emulation user, connecting directly to the emulation bus for analysis of all emulation software, even when executing entirely in emulation memory. It is designed to take the place of a Model 64300A or 64302A Internal Analyzer on the emulation bus, but it can be used along with the internal analyzer, if desired.

The preprocessor operates with both 8-bit and 16-bit emulators, providing all signal conversion required by the Model 64620S and it includes the hardware for the 16-bit emulation single-step feature that normally requires an internal analyzer board. The preprocessor identifies the particular emulator being probed, so that the Model 64620S can automatically load the predefined format and inverse assembler files for that processor.

The Model 64620S analyzer can reside in the same development station with the Model 64304A or it can be located in another station. Operation is identical in either configuration. Also, more data acquisition boards with Model 64635A General Purpose Data Probes can be added to the Model 64620S providing external signal probing capability.

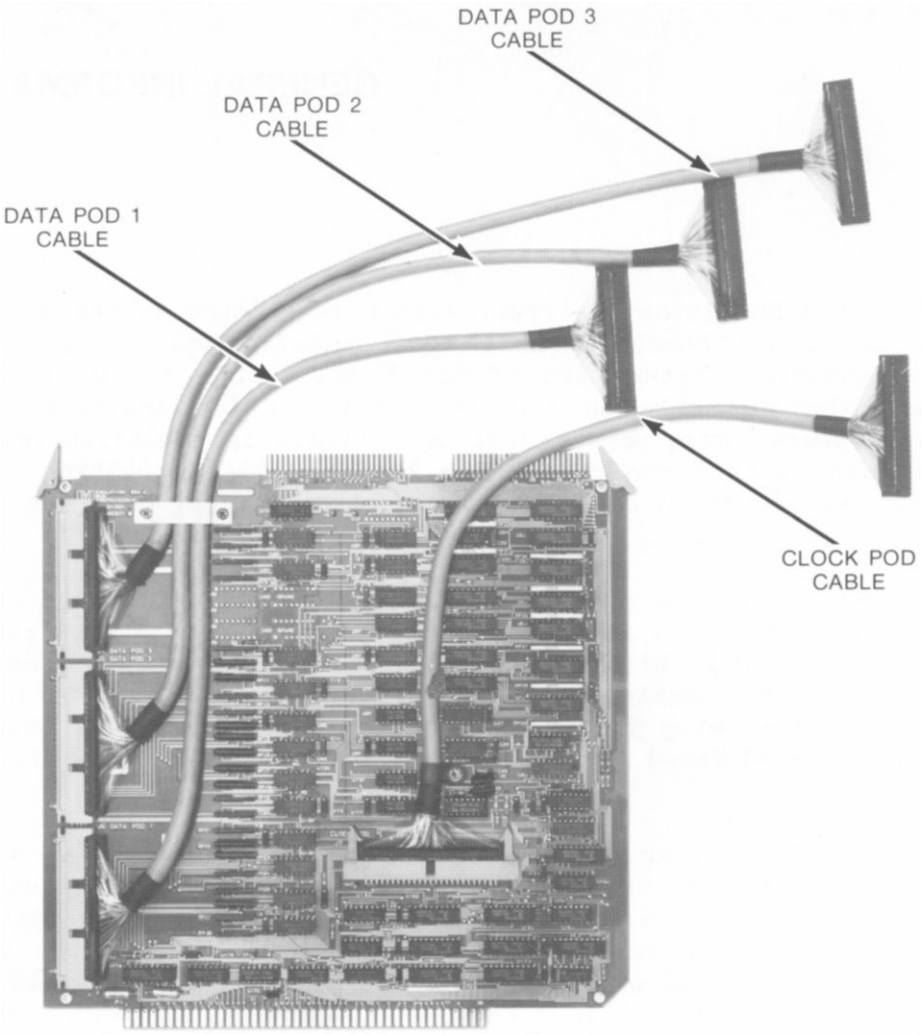

Figure 1-1. Emulation Bus Preprocessor Circuit Board

Chapter 2

INSTALLATION

SYSTEM CONFIGURATION

Minimum hardware requirements for state analysis of 8-bit emulation are:

a. Model 64621A state control circuit board

b. Model 64622A 40-channel data acquisition circuit board

c. Model 64304A emulation bus preprocessor circuit board, including one clock cable and three data cables (one data cable will not be used for 8-bit analysis).

Minimum hardware requirements for state analysis of 16-bit emulation are:

a. Model 64621A state control circuit board

b. Model 64622A 40-channel data acquisition circuit board

c. Model 64623A 20-channel data acquisition circuit board

d. Model 64304A emulation bus preprocessor circuit board, including one clock cable and three data cables

The clock and data cables included with the preprocessor are designed for use with the analyzer located in the same development station. If longer cables are desired for configuring the analyzer in a separate development station, the general purpose clock cable and general purpose data cables supplied with the Model 64620S can be substituted.

HARDWARE INSTALLATION

CAUTION

To prevent equipment damage, be certain to turn off power to the development station whenever boards and cables for the state analyzer, preprocessor, or emulator are being installed or removed.

Install the emulation boards toward the front of the development station in the lower numbered slots as described in the emulator operating manual. Before installing the Model 64304A preprocessor circuit board, make note of the labels on the board for the clock and data pods to aid in connecting the preprocessor to the analyzer.

For automatic configuration of the Model 64620S analyzer or if an internal analyzer is present, the preprocessor MUST be installed in the next HIGHER slot after its emulation control board. The internal analyzer should be installed next to the preprocessor board for easier cable connection. An example configuration follows.

Example:

BOARD	64100A SLOT NUMBER
10-MHz 20-Channel Acquistion board (if required)	7
10-MHz 40-Channel Acquistion board	6
10-MHz State Control board	5
Internal Analyzer board (optional)	4
Emulation Bus Preprocessor board	3
Emulation Control board	2
Memory Controller board (optional)	1
Memory board (optional)	0

Install the emulation bus cables on the center and right edge connectors of the memory control board, emulation control board, and emulation bus preprocessor (and the internal analyzer if used) as shown in Figure 2-1.

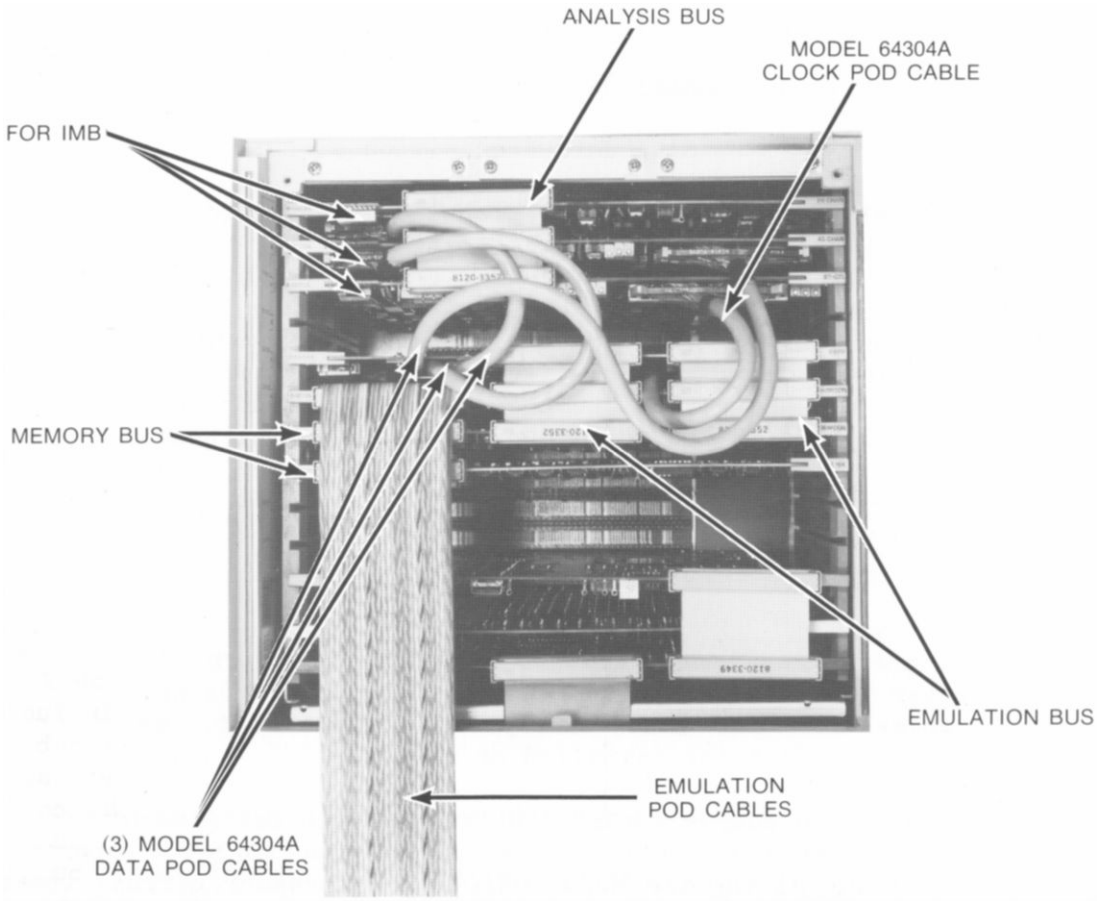

Figure 2-1. Emulation and Analysis Cabling

Refer to the Model 64620S Logic State/Software Analyzer Reference Manual for installation of the analysis hardware. The analyzer circuit boards should be located in the slots toward the back of the development station, as shown in the previous example. Insert the round 50-conductor clock and data pod cables from the preprocessor into the sockets of the Model 64620S control and acquisition boards in the positions shown in Figure 2-2. Be certain to align pin 1 of the connector (marked with a triangle or groove) with pin 1 of the socket (marked with a triangle). The clock pod connector is also notched in the center to separate it from the data pods. It may be necessary to slide the Model 64620S boards partially out of their slots to make the connections. Then, install the analysis bus cable on the edge connectors of the state control board and acquisition boards (refer to Figure 2-1). The round cables should be arranged across the top of the circuit boards to allow the development station cover to be replaced.

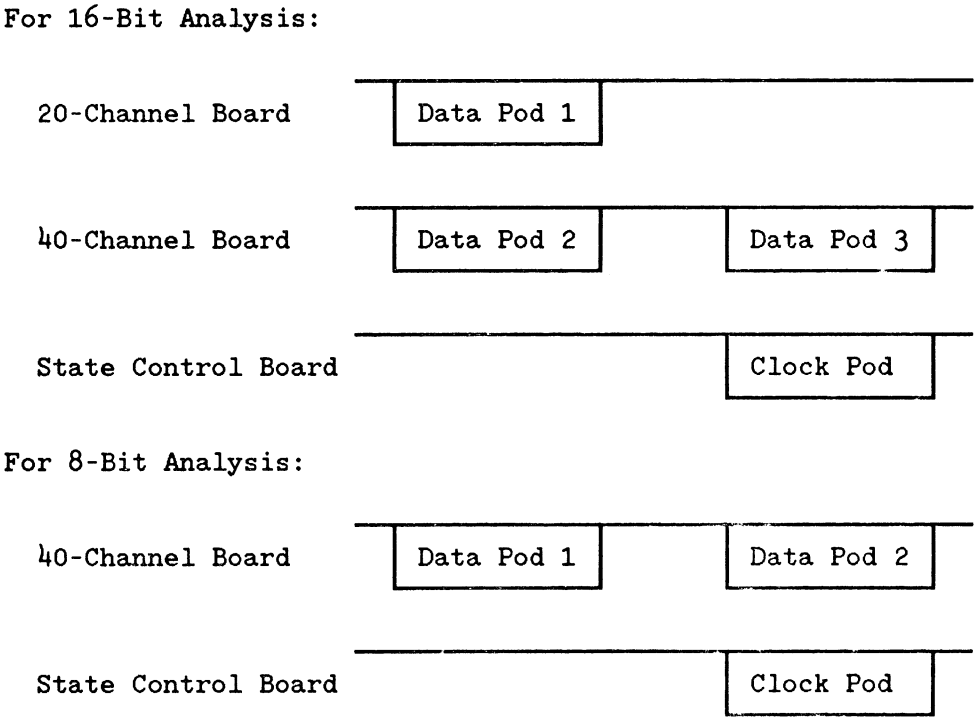

Figure 2-2. Clock and Data Pod Connections

It is possible to interface the preprocessor with a Model 64620S in another development station by replacing the short probe cables included on the preprocessor board with the longer general purpose probe cables included with the Model 64620S. Remove the screws holding the cable clamps to the preprocessor board and then carefully separate the cable connectors from their sockets. Detach the hard plastic connector housing from one end of each of the long cables by removing the four housing screws. Insert this end on each of the four cables into the sockets on the preprocessor board, aligning pin 1 on the connector (marked with a triangle or groove) with pin 1 of the socket (marked with a triangle).

Remember, the clock pod cable connector is notched in the center to prevent confusion with the data probe cables. Reinstall the cable clamps to secure the cables to the preprocessor board. Follow the previous installation instructions for the respective board sets. The emulator/preprocessor and the analyzer should be installed toward the rear of their respective development stations for convenience of cabling.

Chapter 3

OPERATION

INTRODUCTION

The emulation bus preprocessor monitors processor bus cycle data on the emulation bus, processes the data into the proper Model 64620S format, and transfers it to the analyzer. Also included is the necessary circuitry for 16-bit emulation single-stepping. The preprocessor has logic for driving the emulation break function with signals generated by the Model 64620S analyzer. All preprocessor programming is performed by the emulation software module and, except for enabling and disabling emulation breaks from the Model 64620S, is transparent to the user. A preprocessor block diagram is shown in Figure 3-1.

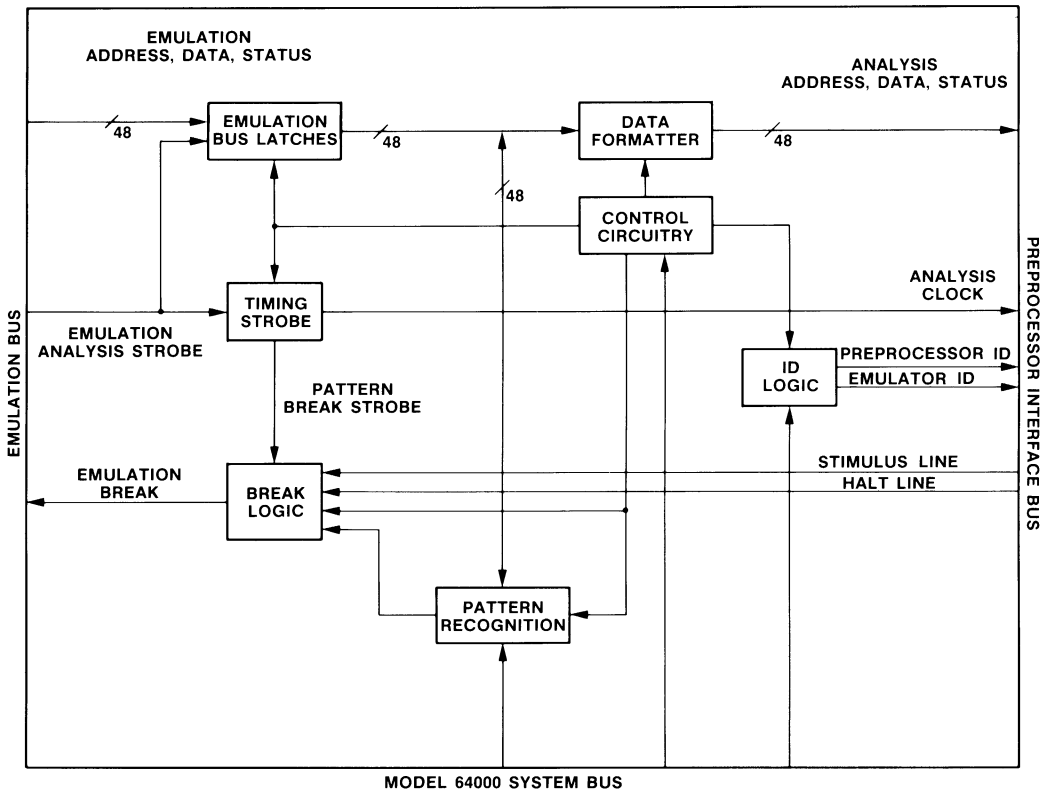

Figure 3-1. Preprocessor Block Diagram

The preprocessor emulation bus interface consists of latches that capture emulation bus cycle data relative to the emulation bus analysis

strobe. The preprocessor can capture up to 48 channels of information each cycle, consisting of: 24 channels of processor address, 16 channels of data, and 8 channels of status. The information is then processed into an 8-bit or 16-bit analysis format and passed to the analyzer over the preprocessor interface bus, which is composed of the clock and data probe cables. The information is passed relative to an analysis clock generated from the emulation bus analysis strobe.

The latched emulation bus information is also routed to pattern detection logic for 16-bit emulation single-stepping. When the "step" command is executed in a 16-bit emulator, the emulator programs the preprocessor pattern detection logic through the Model 64000 system bus to recognize the next program counter value and cause an emulation break when that pattern is recognized on the emulation bus.

Logic in the analysis interface on the preprocessor identifies the preprocessor to the analyzer and identifies the emulator being probed (programmed by emulation software). The STIMULUS and HALT lines sent from the Model 64620S over the clock cable can be used to drive the emulation break logic. The occurrence of these signals is specified by the analyzer, but their use in emulation break is controlled through the emulator.

Local or external operation is possible with the preprocessor. With local operation, the preprocessor couples the emulation bus to the Model 64620S residing in the same development station. This configuration is shown in Figure 3-2.

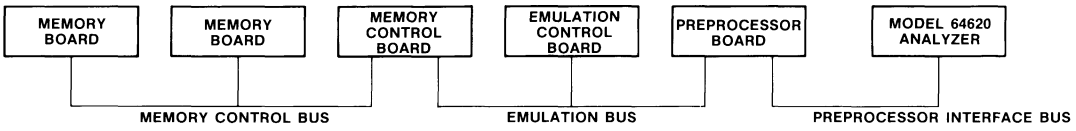

Figure 3-2. Local Preprocessor Application

In external operation, the preprocessor interfaces to a Model 64620S in a separate development station. This configuration allows simultaneous access to both emulation and analysis. Operation is identical to the local configuration. Figure 3-3 shows a block diagram of this application.

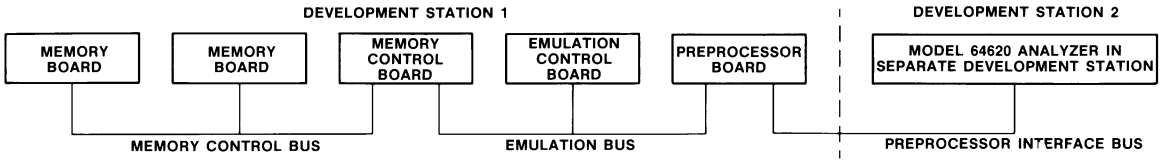

Figure 3-3. External Preprocessor Application

EMULATION WITH THE PREPROCESSOR

In the configuration section of the emulation module, you must enter the preprocessor slot number in response to the prompt "Select board for analysis:". Note, the preprocessor is considered the analyzer from the emulator viewpoint. The following questions replace those for an internal analyzer in the configuration interactive measurement section. These questions allow state analyzer signals to cause an emulation break. Your response will program the preprocessor to drive or not to drive the emulation break logic when a signal is received on one or both of these lines.

```
enable break on stimulus line?  enable (disable)
enable break on halt line?  enable (disable)
```

Refer to the configuration section in the emulator operating manual you are using for a complete description of the emulator setup.

After emulator configuration is completed, notice that none of the "trace" feature soft keys appear. It is not practical to reproduce the user interface to the Model 64620S feature set within the emulation module. The measurement system should be operating in the analysis module to set up analysis specifications and execute and display traces. Emulator configuration and current operating conditions are preserved while in the measurement system even though the system is not in the emulation module. Optionally, the Model 64620S can be placed in a development station separate from the emulator allowing access to both modules at one time.

The intermodule measurement features of the Model 64000 (when operating in the same development station) make it easy to control and synchronize execution of the emulator and analyzer. For example, always driving Master Enable on the intermodule bus (IMB) with the analyzer and then using the "specify run" feature in emulation will allow both modules to be controlled with the "execute" command from either module. Also, Model 64000 command files are supported in both modules and can be used to set up measurements. These features are thoroughly described in the Emulator/Analyzer manual for your processor and the Model 64620 Logic State Software Analyzer Reference manual.

The "run until" feature, which is an internal analysis operation, is not available when using the preprocessor. However, it can be simulated along with all internal analysis "trace break_on" type measurements by using the STIMULUS or HALT line from the Model 64620S to drive the emulation break function. In the following section are examples using the STIMULUS and HALT lines.

STATE ANALYSIS WITH THE PREPROCESSOR

OPERATION

In the local application, when you install the boards as shown in the example configuration in Chapter 2, the Model 64620S will automatically load the correct configuration and inverse assembler files. The analyzer headings will then confirm this by stating which emulator is being probed; e.g., "68000 emulation bus". The Model 64620S will also load the correct configuration and inverse assembler files in the external application if you select measurement system (or the emulator module) before selecting measurement system (or the analysis module) in the other development station. If automatic configuration is not accomplished, then the Model 64620S loads a default configuration file and the analyzer headings will read "emulator interface". At this point, the proper configuration files should be loaded manually as described in the following procedure.

In most cases, the configuration files are the same files used with the Model 64650A General Purpose Preprocessor and Interface modules. The file is named "Cxxxxx:HP:trace", where xxxxx is the name of the processor; e.g., "C68000:HP:trace". However, with some emulators the processor status information on the emulation bus is slightly different than what

would be passed to the analyzer through a Model 64650A. For these emulators, a modified version of the configuration file has been substituted and is named "Cxxxxx_E:HP; e.g., "C8086_E:HP. The processor specific inverse assembler files specified in the configuration file keep the same name "Ixxxxx:HP; e.g., "I68000:HP. You can also specify and load these files manually when entering the analysis module or by using the "configuration load_from " command if the particular emulation and analysis hardware setup does not allow for automatic configuration. Note that any user specified file will always override the automatically loaded file.

The configuration file contains information required by the analyzer format specification to properly group the signals coming from the preprocessor into address, data, and status of the emulator/ processor being probed. The analysis clock definition is also part of this information. In addition, the configuration file specifies an inverse assembler for the particular emulator/processor so that the analyzer can provide a mnemonic display of the signals from the preprocessor that will closely resemble the actual assembly source code. See Table 3-1 for basic preprocessor mapping of address, data, and status signals.

Table 3-1. Preprocessor Mapping of Address, Data, and Status

16-bit Emulation:

	POD 3 (Bits)	POD 2 (Bits)	POD 1 (Bits)
Address		0-3	0-19
Data		4-19	
Status	0-7		

8-bit Emulation:

	POD 3 (Bits)	POD 2 (Bits)	POD 1 (Bits)
Address			0-15
Data		4-11	
Status		12-19	

For either configuration, the analyzer clock is specified as the falling edge of the signal on clock channel 0. All signal thresholds are TTL.

NOTE

No modification of the ADDRESS, DATA, or STATUS labels in the format specification should be made if inverse assembly is required. Any changes may cause incorrect results. If the trace specification is qualified to store only some bus cycles, incorrect or incomplete inverse assembly may occur.

Refer to the analysis section in your emulator operating manual for a table showing the processor status bits on the emulation bus.

All preprocessor hardware control is performed by the emulator. This eliminates the need for preprocessor specification software within the analyzer. A "file not found" type error message will occur in the state analyzer if the preprocessor specification is selected and no further action is taken.

All of the Model 64620S analysis features are available for tracing and debugging emulation software. Refer to the Model 64620S operating manual for a complete description of analyzer features and operation. As mentioned earlier, the STIMULUS and HALT analyzer signals can be activated to drive the emulation break function through the preprocessor. The STIMULUS and HALT signals are defined within the trace specification to occur at selected analysis events. The STIMULUS line can be asserted on a trigger, window, or sequencer event. The HALT line can be asserted on a trace point or a measurement completion. Corresponding signals can also be sent to the BNC ports on the back of the development station for use in the user's target system, which does not affect how they are used by the preprocessor.

EXAMPLE SIMULATIONS OF INTERNAL ANALYSIS FEATURES

Although the "run until" and "trace break_on" features are not available within emulation when using the preprocessor, they are easily reproduced with the Model 64620S using the STIMULUS and/or HALT line to drive emulation breaks.

With STIMULUS line breaks enabled from within emulation, the following analysis specification would have the same effect as an emulation "run until" or internal analysis "trace break_on trigger":

a. The desired trigger point is defined in the analyzer trace_specification. For example:

```
trigger on Address = 02000H
```

b. The STIMULUS line is defined in the trace specification to become active on trigger using the following syntax:

```
assert stimulus_line on all_triggers
```

When executing the analyzer, an emulation break will occur when the specified trigger pattern occurs on the emulation bus.

With HALT line breaks enabled within emulation, an internal analysis "trace break_on measurement_complete" might be simulated as follows:

a. Define the desired trigger point. For example:

```
trigger on Address = 02000H
```

b. Define the HALT line to become active on measurement completion as follows:

```
assert halt_line on measurement_complete
```

When executing the analyzer, an emulation break will occur after the specified trigger pattern occurs on the emulation bus and the rest of the analyzer trace memory is filled.

When an emulation break is received from the preprocessor (including emulation single-stepping), the message "break asserted" will be displayed on the Status line within the emulation module. This message can be used as an indication that a particular analysis event has occurred, driving the STIMULUS or HALT line as specified, while operating in the emulation module. The message will be cleared upon execution of any new emulation command.

Remember, even if the STIMULUS or HALT line is activated in the trace specification, the signals will be ignored by the preprocessor if not specifically enabled within emulation.

These examples just illustrate how the Model 64304A Emulation Bus Preprocessor combined with the Model 64620S Logic State Analyzer might be used to perform familiar emulation features. The powerful feature set of the Model 64620S including complex trace specification and software performance analysis, which is described in the Model 64620S operating manual, will provide greatly improved software debugging capability to the emulation user.

USING THE PREPROCESSOR WITH AN INTERNAL ANALYZER

It is possible to use both the preprocessor and an internal analyzer with the emulator. When the internal analyzer is selected, the emulator will program the preprocessor for a "listen-only mode," resetting it and disabling all breaks. There will be no further interaction between the emulator and the preprocessor and all internal analysis features will become available. The Model 64620S will still be able to trace all emulation bus activity through the preprocessor, but it cannot drive emulation breaks. Remember to follow the guidelines under Hardware Installation in Chapter 2 for this configuration.

64304-90902, OCTOBER 1983
Replaces: 64304-90902, August 1983

PRINTED IN U.S.A.