HEWLETT hp PACKARD

DETAILED DIAGRAMS MANUAL

HP 3000 COMPUTER SYSTEM

03000-90023

HEWLETT-PACKARD COMPANY
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1-1. INTRODUCTION.

1-2. This Detailed Diagrams Manual, part no. 03000-90023, is one of a set of manuals that document the Hewlett-Packard 3000 Computer System (figure 1-1). This manual provides wiring and schematic diagrams for the CPU /IOP, memory, power supply, and device controllers. Other system components and accessories such as the maintenance panels are documented in separate manuals.

1-3. This manual contains an explanation of the logic symbology used to document the HP 3000 Computer System. Operating characteristics for integrated circuits used in the system are also provided.

1-4. Each manual is configured to match the hardware composition of the computer system. Information contained in this manual applies only to the HP 3000 system shipped with the manual.

1-5. SCOPE

1-6. This manual is intended for use by maintenance personnel who are familiar with system theory and maintenance procedures for the HP 3000. A thorough understanding of the information presented in the system reference and maintenance manuals is essential in using the material in this manual.

1-7. Sections II, III, and IV of this manual contain the following information:

a. Section II, Logic Symbology. Section II describes the logic symbology used in this manual. It also provides integrated circuit diagrams and descriptions of the operation of complex logic elements.

b. Section III, Wiring Information. Section III contains cable wiring information and a wire list for the CPU/ IOP interconnection wiring.

c. Section IV, Diagrams. Section IV contains a complete list of active drawing sets for the HP 3000. Additional drawings, not assigned to a drawing set, are documented separately in the maintenance manuals. The drawing sets required for this particular system are arranged in set number order following the list of sets. The drawing sets contain schematic, part location, signal, and part number information for the printed circuit assemblies (PCA's) used in the system.

1-7. SYSTEM CONFIGURATION.

1-8. This diagram manual contains the drawing sets required to document one computer system configuration. Therefore it should not be used when servicing a system other than that shipped with the manual.

1-9. UPDATING.

1-10. This manual is maintained current by updating supplements. These supplements are used to correct errata and to make the manual applicable to computer systems which have been modified at the system site.

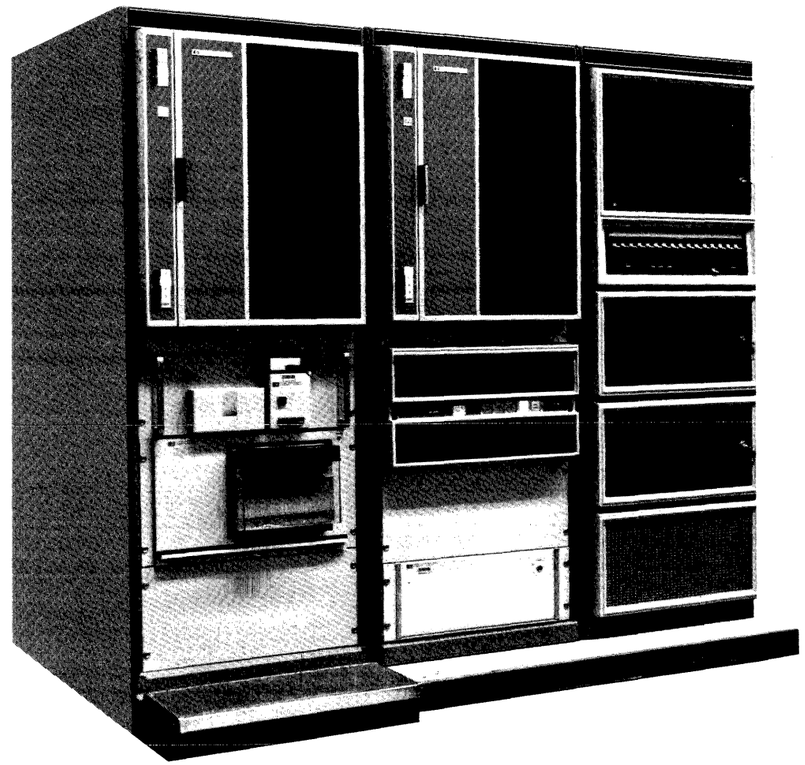


Figure 1-1. Hewlett-Packard 3000 Computer System

2-1. INTRODUCTION.

2-2. This section covers basic logic information and symbology as used in this and related manuals. Following the description of symbology is a table of integrated circuits containing diagram symbols for most circuits and descriptions of operation for complex logic functions.

2-3. LOGIC STATES.

2-4. The logic signals are always in one of two possible states, a "1" or a "0." These two states are also referred to as high (H) or low (L). The high and low states reflect the relative voltage levels of the signals; the high state is always relatively more positive than the low state. Note that both states may have actual voltage values that are positive, or both may be absolutely negative; the significance is in the *relative* levels of the two states. In the text of the manuals, logic states are normally described as "high" or "low."

2-5. The "not" bar associated with signal names is used to indicate whether the "active" state of the signal is high or low. For example, if the presence of data on a signal line is represented by a low signal, the signal name for the line might be "not" Data 1; if a signal clears the output register when the signal is low, the signal might be described as "not" Clear Output Register ($\overline{\text{COR}}$). The "not" bar must be considered an integral part of the signal name; this means that there are high states for "not" signals and low states for "not" signals, just as there are high and low states for signals without the "not" bar.

2-6. INVERSION.

2-7. Logic inversion is indicated by an inversion dot at the input or output of a logic symbol. When this dot appears at the input of a logic symbol, the input will be effective when the input signal is low. When the dot appears at the output of a logic symbol the output will be of the opposite state to what would be delivered if the dot were not present.

2-8. LOGIC SYMBOLOGY.

2-9. Three basic symbol shapes distinguish the major classes of logic circuits depicted in this manual. These are gates, regenerative switching elements, and amplifiers. Each symbol and a brief explanation of its operation is given in the following paragraphs.

2-10. In addition to the basic symbols, a general multipurpose symbol is used wherever a standardized logic symbol does not exist. A brief explanation of this multipurpose symbol is included.

2-11. GATES.

2-12. A gate is a circuit that produces a binary output when certain input conditions are met. The gate symbol has input lines connecting to one side of the symbol, and output lines connecting to the other side, as shown in figure 2-1. Since the inputs and outputs are easily identifiable, the symbol can be shown left-facing, right-facing, or facing up or down.

2-13. There are four basic types of gates: "and," "or," "nand," and "nor," each named for the logic function that it performs. Each of these gates is described in the following paragraphs. In addition, a brief explanation of an "expander" gate is given following the descriptions of the basic logic gates.

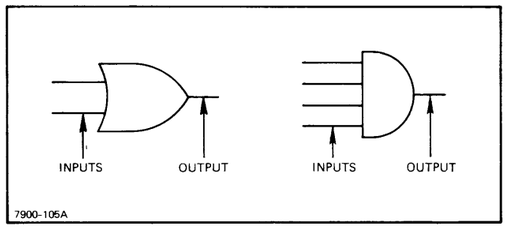
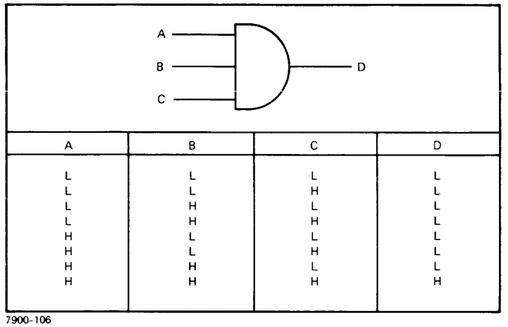


Figure 2-1. Gate Symbols

2-14. "AND" GATE.

2-15. The "and" gate shown in figure 2-2 performs a logical "and" function. It will produce a high output only when all of the input lines are high. Input A *and* input B *and* input C must be high for a high output to be generated.

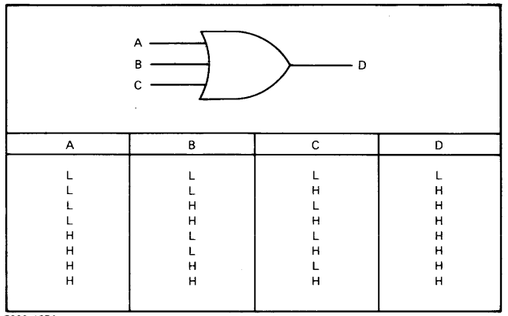


A	B	C	D
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Figure 2-2. Three-Input "And" Gate Logic Symbol and Truth Table

2-16. "OR" GATE.

2-17. The "or" gate performs a logical "or" function. It produces a high output when one *or* more inputs are high. The truth table in figure 2-3 shows the various states of a three-input "or" gate.

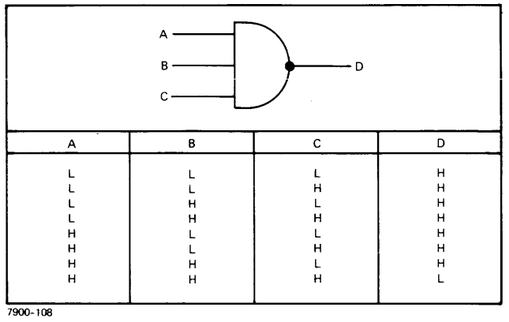


A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

Figure 2-3. Three-Input "Or" Gate Logic Symbol and Truth Table

2-18. "NAND" GATE.

2-19. The "nand" gate is similar to the "and" gate described previously, except that its output is inverted. The gate generates a low output when all inputs are high. The various states of a three-input "nand" gate are shown in the truth table in figure 2-4.

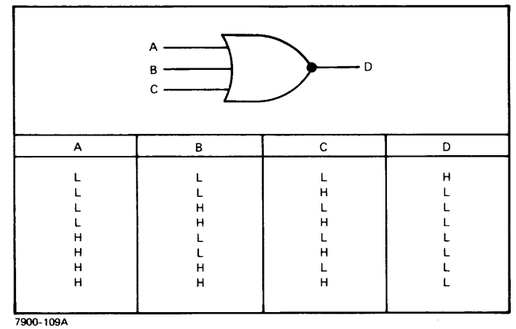


A	B	C	D
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure 2-4. Three-Input "Nand" Gate Logic Symbol and Truth Table

2-20. "NOR" GATE.

2-21. The "nor" gate is identical to the "or" gate described previously, except that its output is inverted. The gate generates a low output when one or more inputs are high. The various states of a three-input "nor" gate are shown in the truth table in figure 2-5.

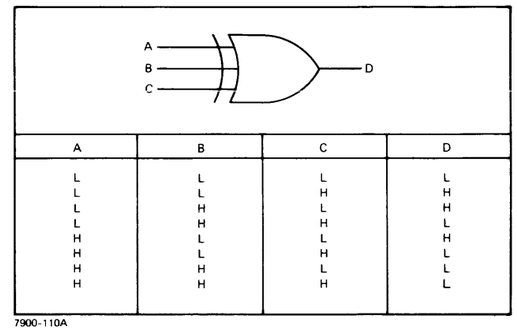


A	B	C	D
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Figure 2-5. Three-Input "Nor" Gate Logic Symbol and Truth Table

2-22. "EXCLUSIVE OR" GATE.

2-23. The "exclusive or" gate is a variation of the basic "or" gate. It has two or more input signals. The output is high when only one input is high. The truth table in figure 2-6 shows the functioning of a three-input exclusive "or" gate.



A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

Figure 2-6. Three-Input "Exclusive Or" Gate Logic Symbol and Truth Table

2-24. EXPANDER GATE

2-25. Some logic gates have additional input lines which may be used to increase or "expand" the number of input signals. These expanding input lines use different signal levels than the normal gate input. The expander gate provides these special signal levels. The expander gate may provide one or two output lines to drive the expanded gate.

2-26. An expanded input will normally be indicated by the letter "E". Figure 2-7 shows both single and double line expanded inputs. When more than one expander gate is used the expanded inputs are connected together.

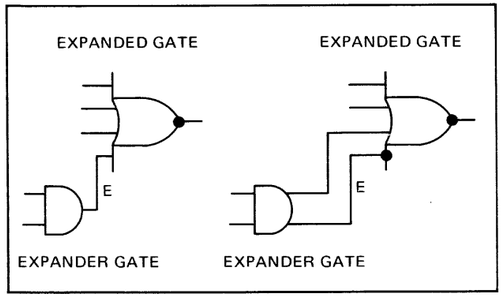


Figure 2-7. Expander Gate Logic Symbol

2-27. STROBE LINES.

2-28. Strobe lines may be used to enable the output lines of tri-state logic elements. The strobe inputs are shown connected at right angles to the normal signal flow. Examples of a strobe controlled gate and amplifier are shown in figure 2-8.

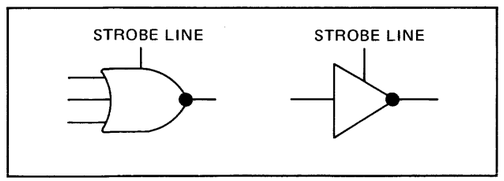


Figure 2-8. Strobe Controlled Gate and Amplifier Symbols

2-29. ENCODING GATE.

2-30. The encoding gate (figure 2-9) has one input and multiple outputs. When the input is high, all outputs (B, C, and D) are high. When the input is low, the outputs are all low.

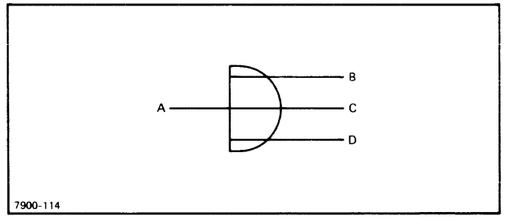


Figure 2-9. Three-Input Encoding Gate, Logic Symbol

2-31. A typical circuit for an encoding gate is shown in figure 2-10. With A high, all diodes conduct and all outputs are clamped high. With A low, each diode is practically an open circuit, and points B, C, and D assume the voltage level of the circuit to which each is connected.

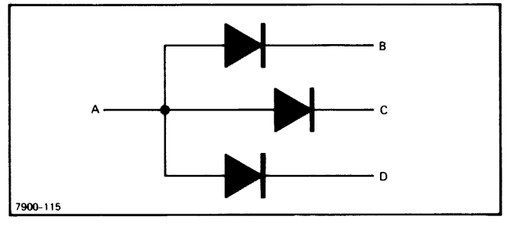


Figure 2-10. Typical Encoding Gate Circuit

2-32. MULTIVIBRATORS.

2-33. The multivibrators described here are of four main types: flip-flops, Schmitt trigger circuits, one-shot multivibrators, and free-running multivibrators. All furnish a binary output. However, unlike gate circuits, the duration of a multivibrator output signal is not dependent on the duration of an input signal.

2-34. The basic logic symbol for a multivibrator is a rectangle as shown in figure 2-11. Letters in the symbol indicate the type of multivibrator. The rectangle is divided horizontally, with the upper portion representing the "set side" and the lower portion representing the "clear side." The multivibrator is considered set when the output from the set side is high. It is considered cleared when the output from the clear side is high. To avoid confusion, the symbol is always oriented as shown in figure 2-11; inputs on the left, outputs on the right.

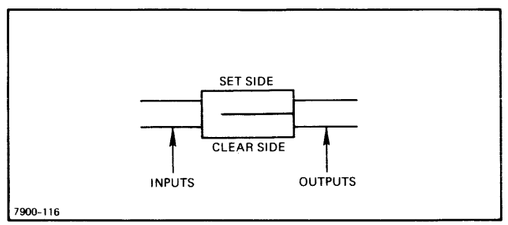


Figure 2-11. Basic Logic Symbol Multivibrator

2-35. FLIP-FLOP.

2-36. The symbol for a flip-flop is shown in figure 2-12. The letters "FF" preceded by the name of the flip-flop distinguish this symbol from other types of multivibrators. Additional identification, described later, identifies the particular type of flip-flop.

2-37. A flip-flop is a bistable switching device; an external signal is required to set the flip-flop and another to clear it. The flip-flop remains in its current state until switched to the opposite state by the appropriate external signal. Various forms of flip-flops exist, of which seven are described here: the R-S (reset-set), clocked R-S, J-K, clocked J-K, toggle, latch, and delay flip-flops.

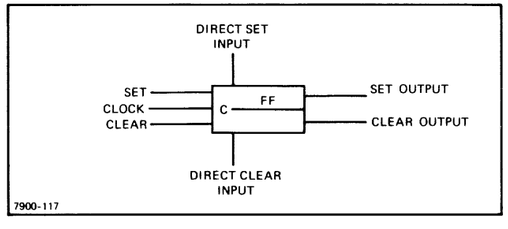
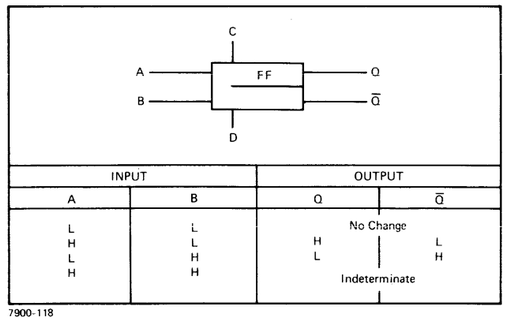


Figure 2-12. General Flip-Flop Logic Symbol

2-38. R-S FLIP-FLOP. The symbol for the R-S flip-flop as shown in figure 2-13 can be recognized by the fact that there is no information in the symbol identifying it as one of the other six types. The R-S flip-flop has a minimum of two input terminals (A and B in figure 2-13) and one or two output terminals Q and $\overline{Q}$. One or two additional input terminals, C and D, may be used.

2-39. The R-S flip-flop is set by a high input at A (assuming no inverting dot at this point). It can also be set by a high input at C, if this input terminal is present. The flip-flop is cleared by a high input at B or D. Figure 2-13 includes a truth table, showing the flip-flop outputs resulting from various input conditions.



INPUT		OUTPUT	
A	B	Q	$\overline{Q}$
L	L	No Change	
H	L	H	L
L	H	L	H
H	H	Indeterminate	

Figure 2-13. R-S Flip-Flop, Logic Symbol, and Truth Table

2-40. After being set or cleared, the R-S flip-flop remains in that condition after termination of the set or clear pulse. If the flip-flop is either set or clear and it receives an input to place it in the existing state no change takes place in the state of the flip-flop.

2-41. Simultaneously high set and clear input signals normally are not permitted, and circuit design usually prevents occurrence of this condition at a time when the flip-flop outputs are used. If simultaneous set and clear inputs are received, both outputs of the flip-flop are high for the duration of the simultaneous inputs. The eventual state of the flip-flop is determined by the input that remains high longest.

2-42. CLOCKED R-S FLIP-FLOP. The clocked R-S flip-flop is similar to the R-S flip-flop, but it has a clock pulse input as shown in figure 2-14. The logic symbol can be recognized by the letter "C" at this input terminal. At the positive-going transition of the clock pulse, the flip-flop becomes set if input A is high, or it becomes clear if input B is high (assuming no inverting dot at the clock pulse input terminal). If inputs A and B are both low during the clock pulse, the flip-flop does not change state. It is not permissible that A and B both be high when the positive-going clock pulse transition takes place.

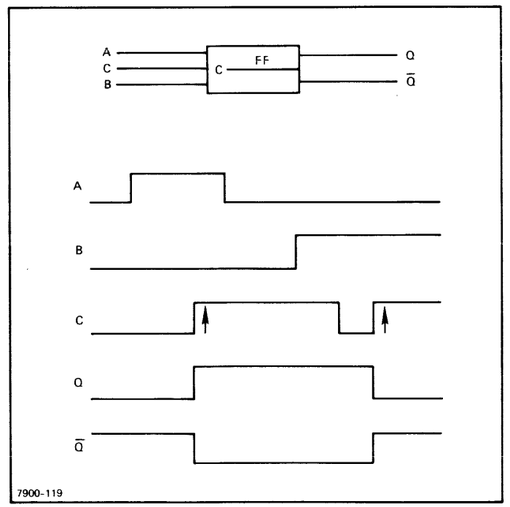


Figure 2-14. Clocked R-S Flip-Flop, Logic Symbol, and Switching Waveforms

2-43. When the clocked R-S flip-flop has an inverting dot at the clock pulse input (figure 2-15), the negative-going transition of the clock pulse is the transition that is effective in setting or clearing the flip-flop.

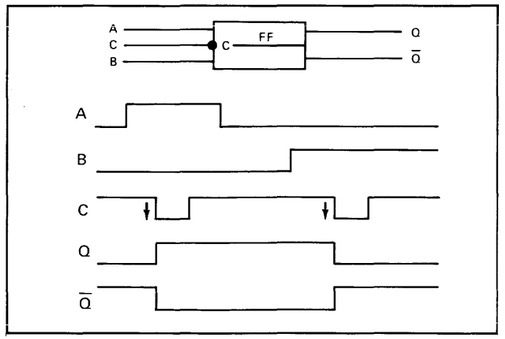


Figure 2-15. R-S Flip-Flop with Inverted Clock Input, Logic Symbol, and Switching Waveforms

2-44. In some cases the clocked R-S flip-flop has a set and clear input at the top and bottom of the logic symbol (inputs D and E, figure 2-16). These inputs are independent of the clock pulse, and are referred to as the direct set and direct clear inputs. They function as a result of a high or low level, rather than a positive- or negative-going transition. An inverting dot at the direct set or clear input indicates that a low level is required to set or clear the flip-flop. No dot indicates that a high level is required. The direct set and clear inputs are also used on other types of flip-flops.

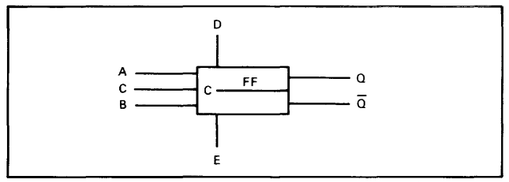


Figure 2-16. Logic Symbol for Clocked R-S Flip-Flop with Direct Set and Direct Clear Inputs

2-45. TOGGLE FLIP-FLOP. The symbol for the toggle flip-flop as shown in figure 2-17 can be recognized by the letter "T" in the symbol. This flip-flop has a single input. If there is no inverting dot at this input, each time the input signal becomes high, outputs Q and $\overline{Q}$ change state. Since two inputs are required to produce one complete cycle of the output, the toggle flip-flop functions as a divide-by-two element, and is commonly used in groups in counting circuits, with the output of one flip-flop driving the next. Figure 2-17 shows the switching waveforms for one flip-flop.

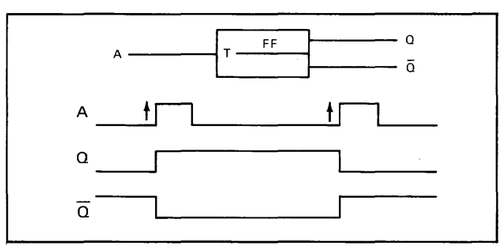


Figure 2-17. Toggle Flip-Flop Logic Symbol and Switching Waveforms

2-46. If a toggle flip-flop symbol has an inverting dot at the input connection, the flip-flop changes state at the negative-going transition of the input. The symbol and waveforms for this type of flip-flop are shown in figure 2-18.

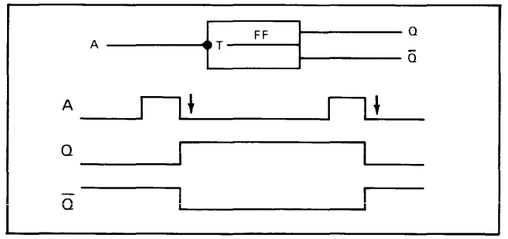


Figure 2-18. Toggle Flip-Flop with Inverted Input, Logic Symbol, and Switching Waveforms

2-47. J-K FLIP-FLOP. In the J-K flip-flop, simultaneous high inputs for both set and clear will reverse the existing state of the flip-flop. This requires some method of storing two conditions, the previous output state and the new output state, until the clock pulse time. The set and clear inputs are labeled J and K respectively. In order to provide the necessary output storage the flip-flops are combined in a dual-rank configuration, together with the necessary gates to form a single logic element. For simplicity the internal dual-rank arrangement of the flip-flop is not usually shown. (See figure 2-19.)

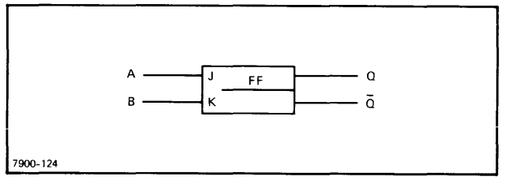


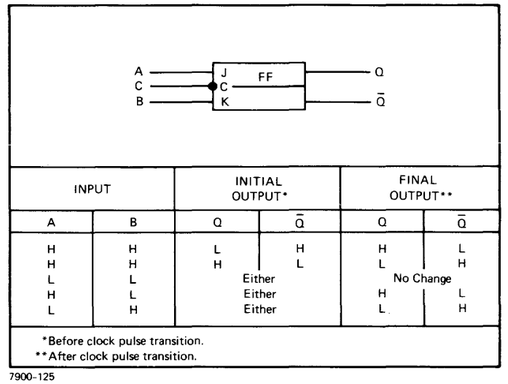
Figure 2-19. J-K Flip-Flop Logic Symbol

2-48. CLOCKED J-K FLIP-FLOP. The clocked J-K flip-flop as shown in figure 2-20 is similar to the clocked R-S flip-flop. However, simultaneous set and clear inputs to the J-K flip-flop are permissible. Under these conditions, the J-K flip-flop changes its state at the occurrence of each positive-going clock pulse transition. With an inverting dot at the clock pulse input, the flip-flop changes state at the negative-going clock pulse transition. If both J and K inputs are high, the flip-flop will toggle when a clock pulse is received.

2-49. The J-K flip-flop can also be operated with one high input and one low input. It then functions in the same manner as the clocked R-S flip-flop.

2-50. Figure 2-20 includes a truth table showing operation of the J-K flip-flop. Note that with both inputs high at the time of clock pulse transition, the final state of the flip-flop (after clock pulse transition) depends on the state before the transition. With only one input high, the initial state of the flip-flop is immaterial.

2-51. In some cases the J-K flip-flop consists of two separate flip-flops, with the output of one applied to the input of the other. Usually, a single flip-flop logic symbol is used to illustrate this circuit. The clock pulse inverting dot, or the lack of it, indicates the clock pulse transition that affects the output flip-flop of the pair.



INPUT		INITIAL OUTPUT*		FINAL OUTPUT**	
A	B	Q	$\overline{Q}$	Q	$\overline{Q}$
H	H	L	H	H	L
H	H	H	L	L	H
L	L	Either		No Change	
H	L	Either		H	L
L	H	Either		L	H

*Before clock pulse transition.
**After clock pulse transition.

7900-125

Figure 2-20. Clocked J-K Flip-Flop Logic Symbol and Truth Table

2-52. LATCH FLIP-FLOP. The latch flip-flop shown in figure 2-21 can be recognized by the letter "L" in the symbol. The flip-flop has a clock input and a data input. Although the logic symbol shows one input-signal connection to the flip-flop, this seperates inside the integrated circuit package to form two inputs to the pack. After separation, one input is inverted (indicated by the inverting dot) before application to the flip-flop.

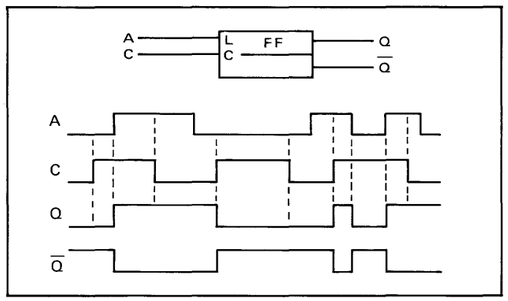


Figure 2-21. Latch Flip-Flop Logic Symbol and Switching Waveforms

2-53. The set-side input is responsive to high signal levels at A in figure 2-22, and the clear input is responsive to low signal levels at A. If there is no inverting dot at the clock input, this response takes place when the clock pulse is high. While the clock pulse remains high, the outputs follow any changes in the logic level at A as these changes take place. When the clock pulse becomes low, the flip-flop retains its current state, and no longer responds to changes of the input signal.

2-54. If the clock input connection of a latch flip-flop has an inverting dot, the flip-flop responds to the input signal while the clock pulse is low.

2-55. DELAY FLIP-FLOP. The delay flip-flop shown in figure 2-22 is identified by a letter "D" inside the flip-flop symbol. This type of flip-flop is similar to the latching flip-flop, except that it responds to the input signal only at the transition of the clock pulse. The delay flip-flop thus does not follow changes in the input signal as these changes take place.

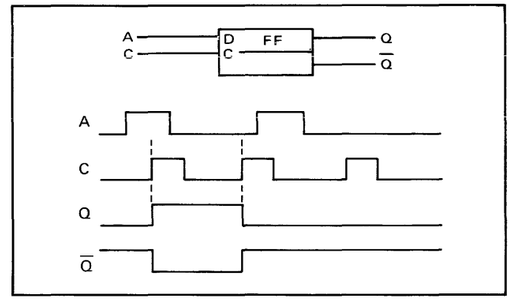


Figure 2-22. Delay Flip-Flop Logic Symbol and Switching Waveforms

2-56. GATE FLIP-FLOP. The gate flip-flop is made up of two logic gates, connected as shown in figure 2-23. The number of inputs to each gate can vary from that shown. The flip-flop can also be made up of two "nor" gates. The circuit may have a set output, a clear output, or both.

2-57. The gate flip-flop functions like an R-S flip-flop, but it has the advantage that it can "or" inputs without the addition of a separate "or" gate. Another reason for use of the gate flip-flop is that if two spare gates are available in integrated circuits on a circuit card, they can be employed as an R-S flip-flop without the need to add another integrated circuit to the card.

2-58. If the flip-flop is made up of two "nand" gates, as in figure 2-23, it is set by a low input at either A or B. Similarly, it is cleared by a low input at C or D. When the flip-flop is in the quiescent state (not undergoing transition), the inputs at A, B, C, and D are all high.

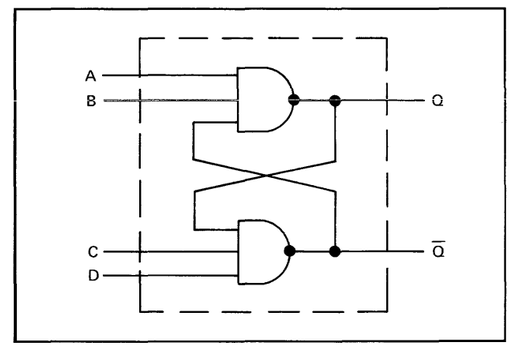


Figure 2-23. "Nand" Gate Flip-Flop, Logic Symbol

2-59. A "nor" gate flip-flop is shown in figure 2-24. In this type of flip-flop all inputs are low when the device is in the quiescent state. A high input at A sets the flip-flop, and a high input at B clears it. The outputs cross in the illustration in order to align the set and clear inputs with the set and clears outputs, respectively.

2-60. In most circuits using the "nand" or "nor" gate flip-flop, input signals are such that the flip-flop does not receive high set and clear input signals simultaneously. If circuit design does permit this to occur, both the set- and the clear-side outputs are high for the duration of the condition. The eventual state of the flip-flop is determined by the input that remains longest in the activating condition.

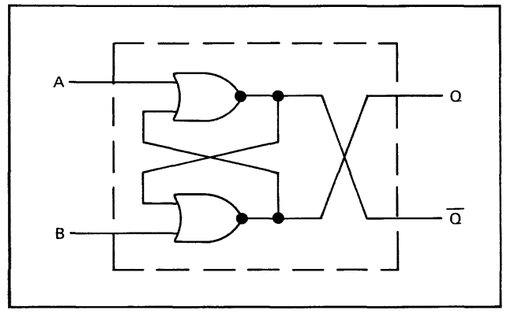


Figure 2-24. "Nor" Gate Flip-Flop Logic Symbol

2-61. SCHMITT TRIGGER.

2-62. The Schmitt trigger circuit shown in figure 2-25 can be identified by the letters "ST" appearing in the logic-diagram symbol. Like the various types of flip-flops this circuit is a two-state device which does not perform a Boolean function. It serves for level sensing or signal squaring. It may have a set-side output, a clear-side output, or both.

2-63. When the input voltage at A is below a certain level, the Schmitt trigger is in the clear state. When the input voltage rises above the reference level, the trigger assumes the set state. Circuit constants establish the reference level.

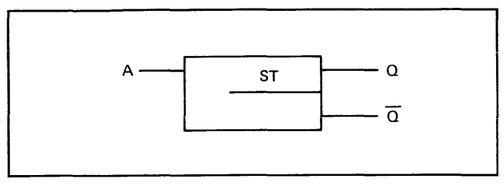


Figure 2-25. Schmitt Trigger Circuit Logic Symbol

2-64. Switching between states takes place rapidly, and the Schmitt trigger is therefore useful for squaring signals that have poor rise and fall times. It can produce a square-wave from a sine wave. Other uses of the Schmitt trigger are voltage level restoration, and detection of the rise of the input signal above a given level.

2-65. ONE-SHOT

2-66. The one-shot multivibrator (figure 2-26) is a monostable switching element, used to produce a pulse of predetermined duration. The device is triggered into its unstable state by an external signal. It returns to the stable state after a time interval determined by circuit constants.

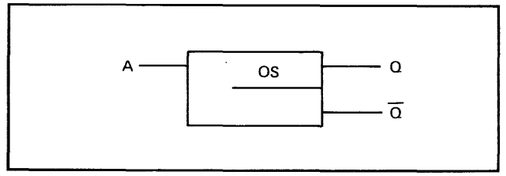


Figure 2-26. One-Shot Multivibrator Logic Symbol

2-67. If there is no inverting dot at the input, triggering is accomplished when input A undergoes a positive-going transition. If there is an inverting dot, a negative-going transition is required. The one-shot multivibrator may have a set-side output, a clear-side output, or both.

2-68. The symbol for the one-shot multivibrator is always drawn with the orientation shown in figure 2-26, with the input at the left and the output or outputs at the right.

2-69. FREE-RUNNING MULTIVIBRATOR.

2-70. The free-running multivibrator shown in figure 2-27 can be distinguished by the letters "MV" appearing in the symbol. This device produces trains of complementary pulses at Q and $\overline{Q}$. Pulse width is determined by circuit constants.

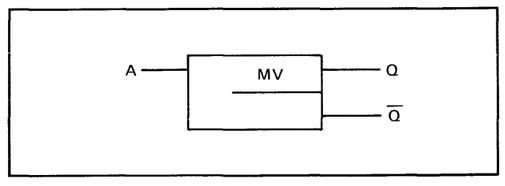


Figure 2-27. Free-Running Multivibrator Logic Symbol

2-71. In some instances a control signal is applied to the free-running multivibrator. If there is no inverting dot at the signal input to the symbol, the multivibrator runs when the control signal is high, and stops when the signal is low. When it is stopped, the multivibrator is in the clear condition. If there is an inverting dot at the control signal input, a low input is required to bring the multivibrator into operation. This type of multivibrator is in the set condition when it is not running.

2-72. Figure 2-28 shows typical waveforms for a controlled free-running multivibrator that runs when the control signal is high. The high and low portions of the output waveforms need not be of equal duration.

2-73. The symbol for the free-running multivibrator is always drawn with the orientation shown in figure 2-28, with the input (if any) at the left, and the output or outputs at the right.

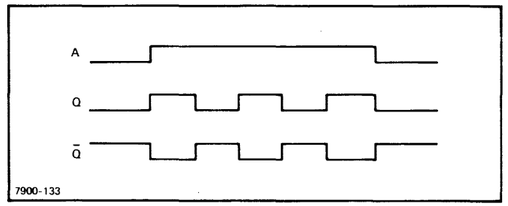


Figure 2-28. Input and Output Waveforms of Controlled Free-Running Multivibrator

2-74. AMPLIFIER.

2-75. The symbol for an amplifier is shown in figure 2-29. A differential amplifier is illustrated in figure 2-30. Like gates, these symbols may be oriented in any of four positions.

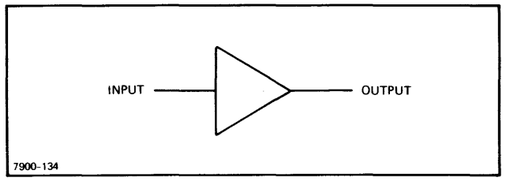


Figure 2-29. Amplifier Logic Symbol

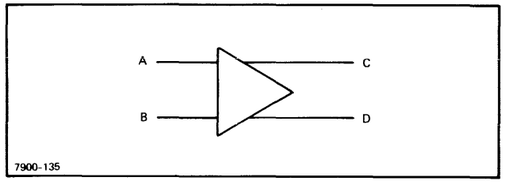


Figure 2-30. Differential Amplifier Logic Symbol

2-76. In most instances, the amplifier symbol has a non-binary input. A circuit which restores the voltage level of a binary input, or which furnishes a low-impedance output from a binary input, is indicated by a one-input "and" gate symbol. An inverting dot at the output of an amplifier symbol indicates that the amplifier inverts the input signal.

2-77. MULTIPURPOSE LOGIC SYMBOL.

2-78. The multipurpose logic symbol is used to indicate a logic function that has not received a standardized logic symbol. The multipurpose symbol is also used to depict multiple logic elements that act together to perform a single overall logic function such as decoding, data storage, or counting. The symbol shown in figure 2-31 may be of varying proportions (mostly commonly 2:1 or 1:2), but rectangular in shape. The symbol includes a descriptive name indicating the overall logic function performed. All active inputs should be labeled to indicate the effect on the overall function. Other descriptive information may be included as needed.

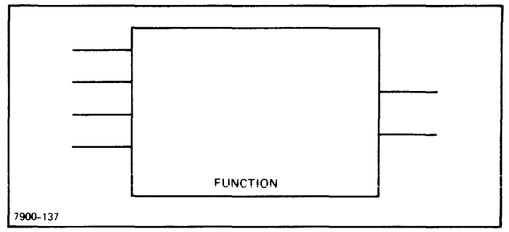


Figure 2-31. Multipurpose Logic Symbol

2-79. Examples of nonstandard symbols are given in figure 2-32. Figure 2-32a shows a binary-to-octal decoder. Figure 2-32b shows a four-bit up/down counter.

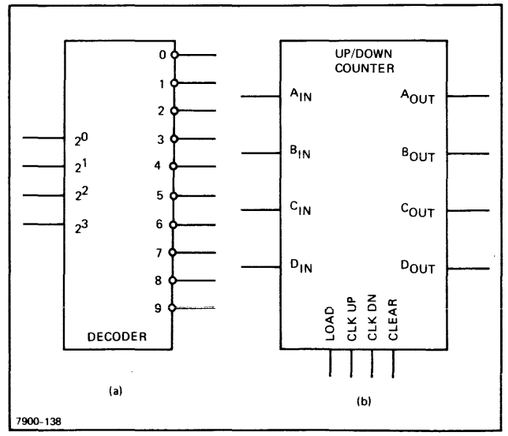
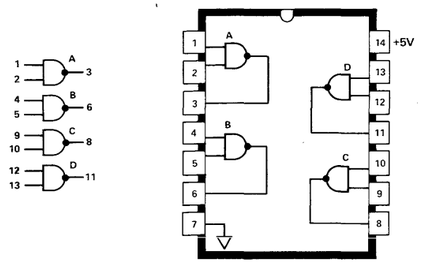
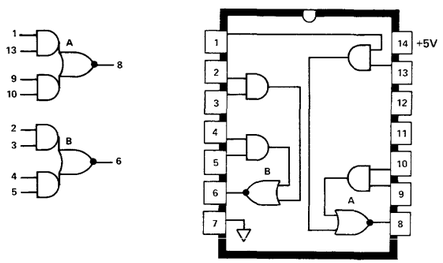


Figure 2-32. Nonstandard Logic Symbols

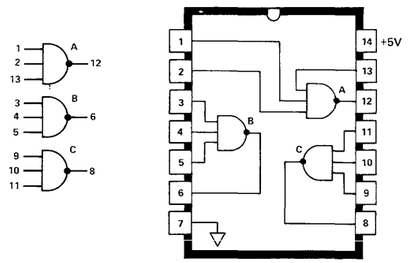
1820-0054



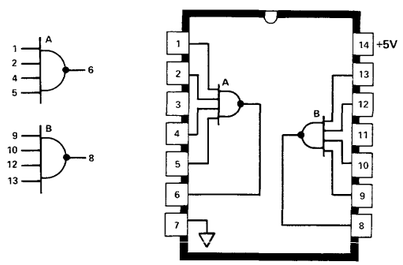
1820-0063



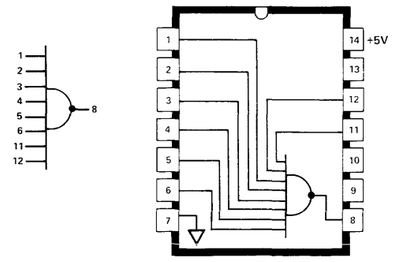
1820-0068



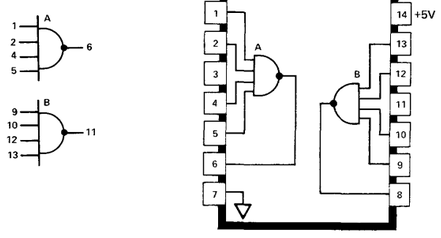
1820-0069



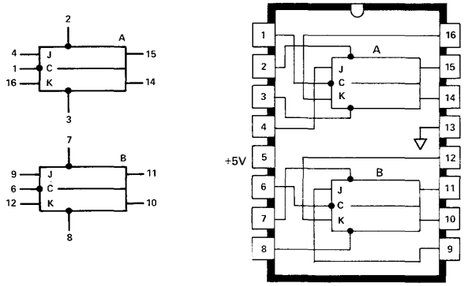
1820-0070



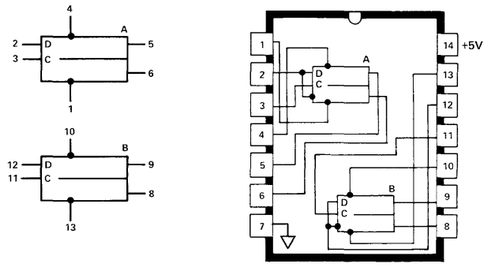
1820-0071



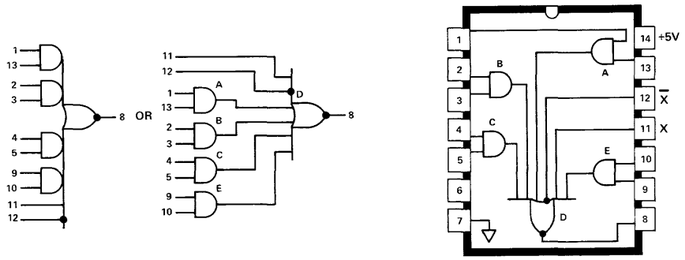
1820-0076



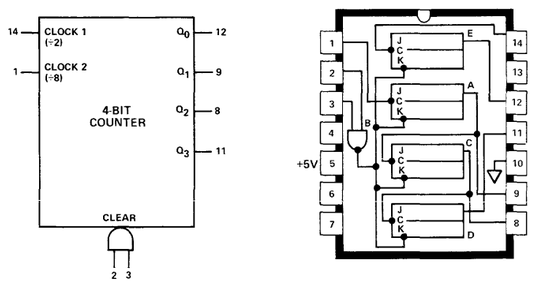
1820-0077



1820-0084

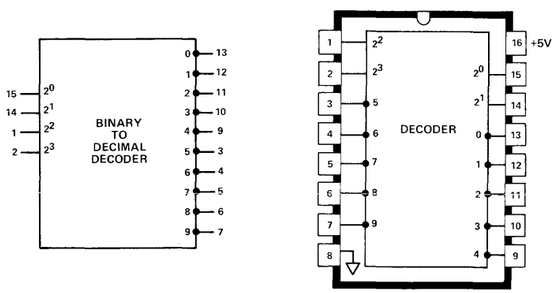


1820-0099



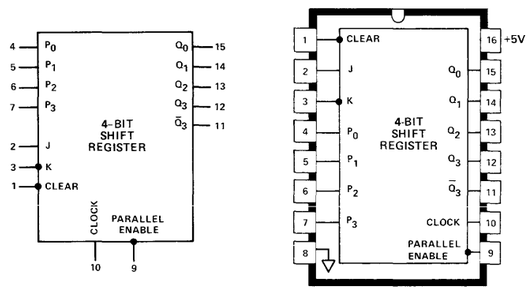
High input signals on the clock 1 line cause the output at Q_0 to toggle. High input signals on the CLOCK 2 line cause outputs Q_1-Q_3 to count. If the Q_0 output is used as the CLOCK 2 input, then the circuit will act as a simple 4-bit (÷ 16) counter. Simultaneous high signals at pins 2 and 3 will clear the counter.

1820-0111



Data on the input lines is interpreted as a binary number. The output line representing the decimal equivalent of the binary input will go low and remain low until the input data is changed. Input data for decimal numbers greater than 9 result in all outputs being high.

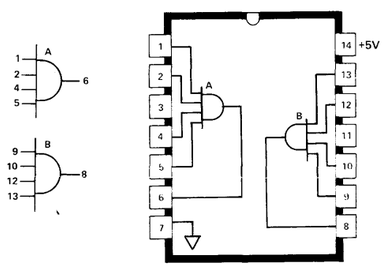
1820-0134



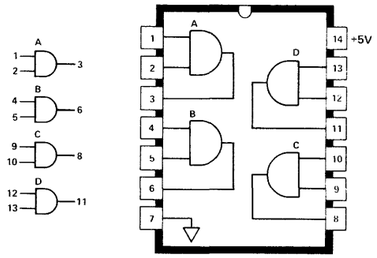
Serial data is entered on the J and K lines. One bit is entered for each clock pulse, most significant bit first. After the clock pulse the data bit will appear at the Q_0 output.

Parallel data is entered by placing the data on the P_0-P_3 input lines and applying a negative PARALLEL ENABLE pulse. A negative CLEAR pulse will clear the register.

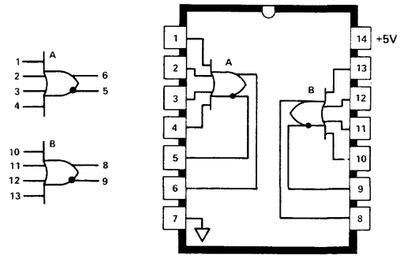
1820-0140



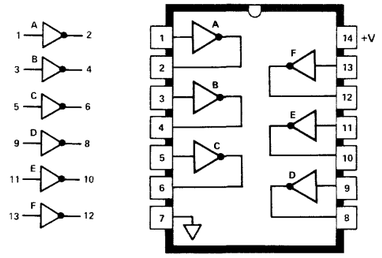
1820-0141



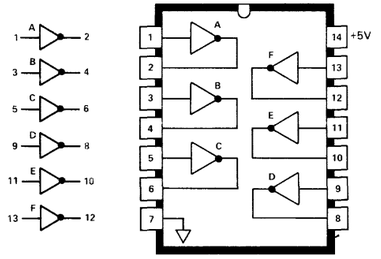
1820-0142



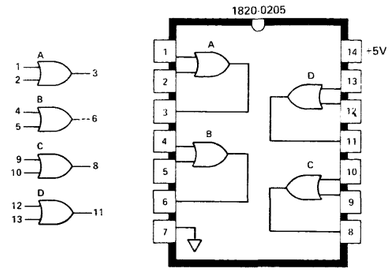
1820-0174



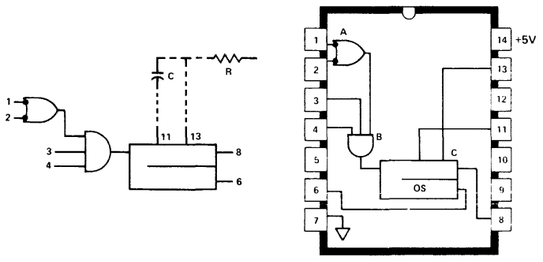
1820-0175



1820-0205

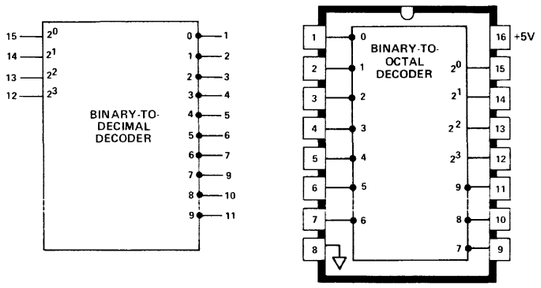


1820-0207



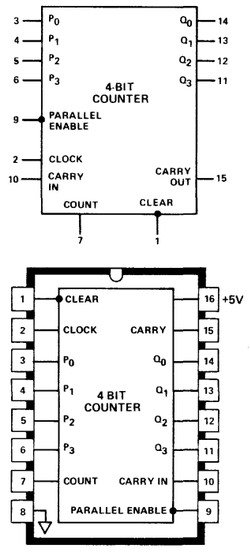
The one-shot is triggered by the input signal. This produces a pulse with duration determined by the external RC elements.

1820-0214



The binary code on the input lines (2^0-2^3) is decoded and the appropriate output line (0-9) will go low. Codes greater than 9 result in all output lines remaining high.

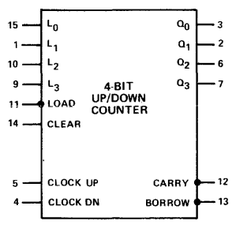
1820-0231



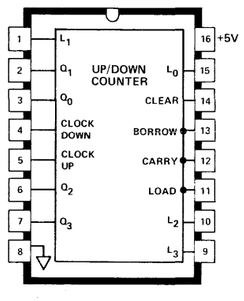
The counter is set from the parallel input lines. When the clock input line goes high and a negative input is applied to the PARALLEL ENABLE line, the counter is loaded. When the clock goes high and both the COUNT and CARRY IN lines go high, the counter will be incremented. The new count will be present on the output lines following the low-to-high transition of the clock.

The CARRY OUT line will be high if the CARRY IN line is high and the counter lines are all high.

1820-0233

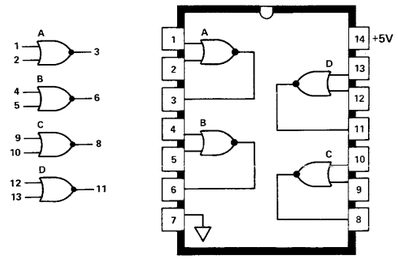


A negative pulse at the LOAD input will set the counter with the data on the input lines. A positive pulse on the CLEAR line will clear the counter. The counter is decremented for each positive-going pulse on the CLOCK DOWN line and incremented for each positive-going pulse on the CLOCK UP line.

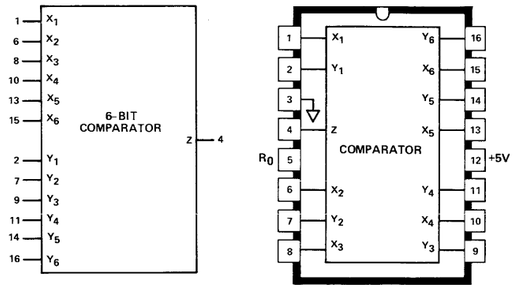


A negative pulse occurs on the CARRY line when the outputs of the counter are all high and a negative pulse on the CLOCK UP line occurs. A negative pulse on the BORROW line occurs when the counter outputs are all low and a negative pulse on the CLOCK DOWN line occurs. When a BORROW pulse is generated the counter is set to all "ones".

1820-0239



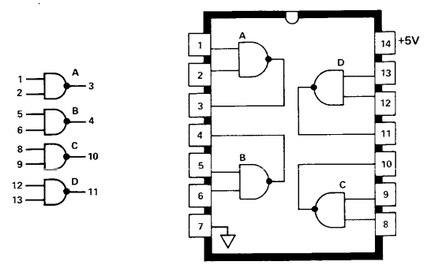
1820-0250



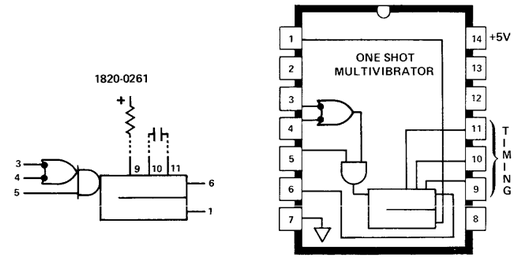
A Z output is generated when each X input is equal to the respective Y input.

$$Z = \overline{(X_1 \oplus Y_1)} \cdot \overline{(X_2 \oplus Y_2)} \cdot \overline{(X_3 \oplus Y_3)} \cdot \overline{(X_4 \oplus Y_4)} \cdot \overline{(X_5 \oplus Y_5)} \cdot \overline{(X_6 \oplus Y_6)}$$

1820-0256

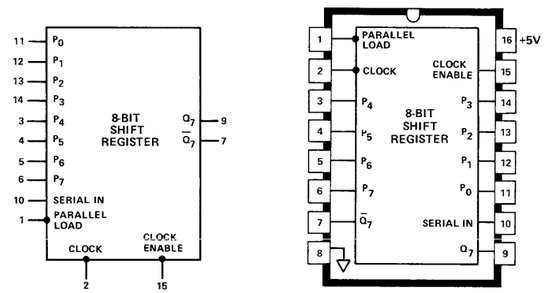


1820-0261



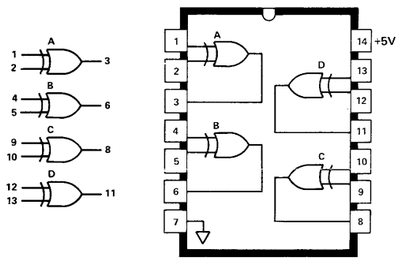
When input conditions are present an output pulse is generated. The pulse width may be determined by external timing circuits.

1820-0262

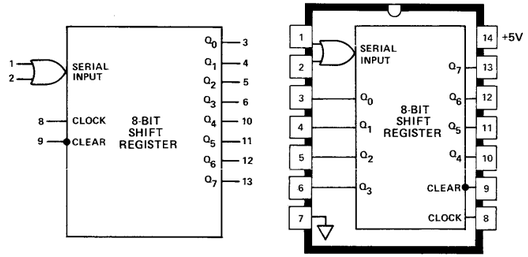


A negative pulse on the PARALLEL LOAD line will load the register with the data on the parallel input lines. A low CLOCK ENABLE line allows negative clock pulses to store serial data, one bit at a time. Each time a clock pulse occurs the data in the register is shifted one bit position. Data is loaded on the positive going edge.

1820-0282

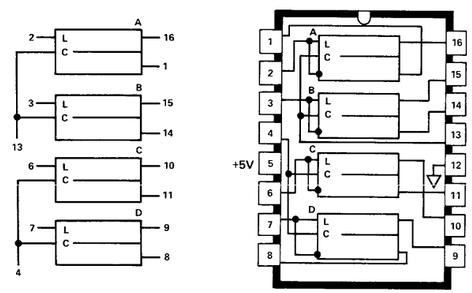


1820-0294

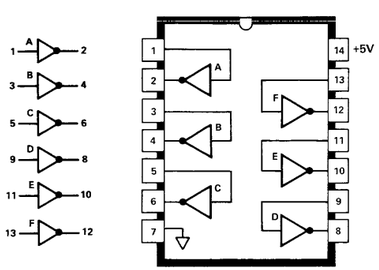


A positive clock pulse shifts the register contents one bit position and loads serial data into position Q_0. A low CLEAR signal clears the register.

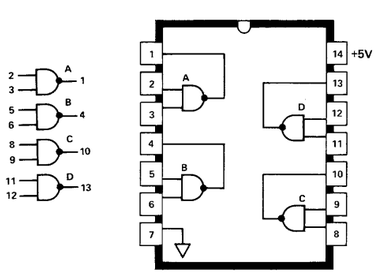
1820-0301



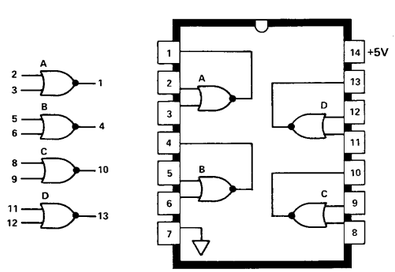
1820-0307



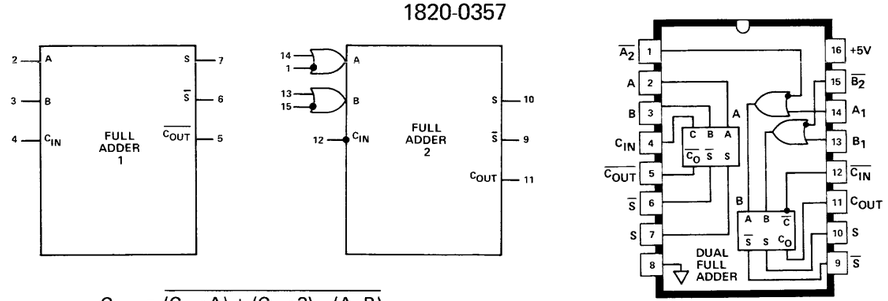
1820-0327



1820-0328



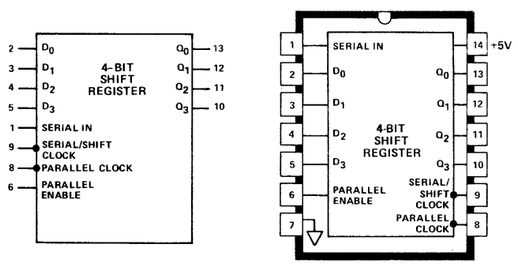
1820-0357



$$C_{out} = \overline{(C_{in} \cdot A) + (C_{in} \cdot 3) - (A \cdot B)}$$

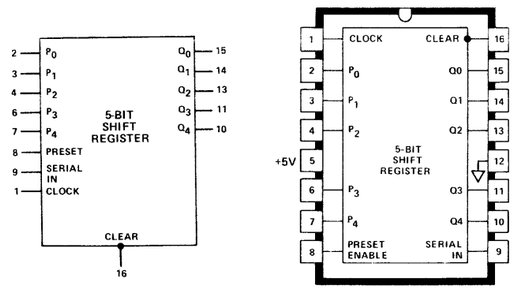
$$S = A \cdot \overline{B} \cdot \overline{C}_{in} + \overline{A} \cdot B \cdot \overline{C}_{in} + \overline{A} \cdot \overline{B} \cdot C_{in} - A \cdot B \cdot C_{in}$$

1820-0367



When the PARALLEL ENABLE line is high and a clock pulse occurs on the PARALLEL CLOCK line, data on parallel input lines (D_0-D_3) will be stored in the register. Data is transferred to the output lines when the clock signal goes low. A clock pulse on the SERIAL SHIFT CLOCK line and a low on the PARALLEL ENABLE line will cause the contents of the register to be shifted one bit position. Data on the SERIAL IN line will be stored in the Bit 0 position. Data is transferred to the output lines when the clock goes low.

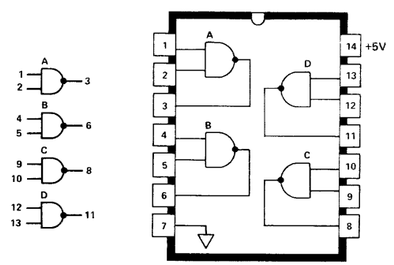
1820-0368



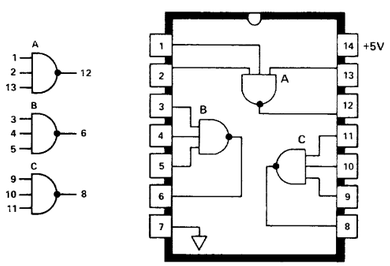
A high input signal on the PRESET line causes the register bits to be set if the corresponding P input line is high.

A clock signal loads the data present on the SERIAL IN line into the first register position and shifts the contents of the register.

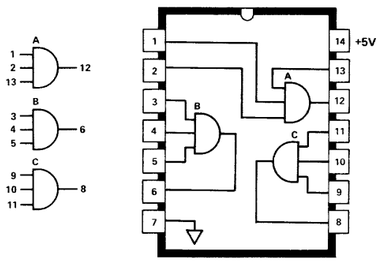
1820-0370



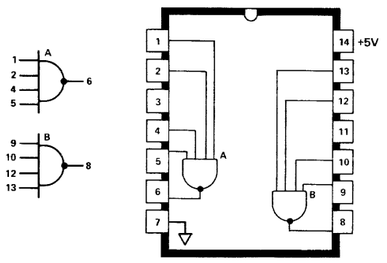
1820-0371



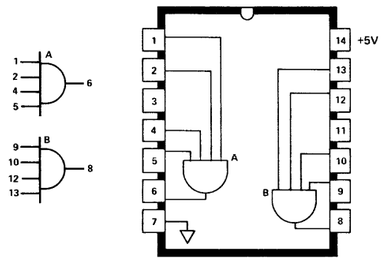
1820-0372



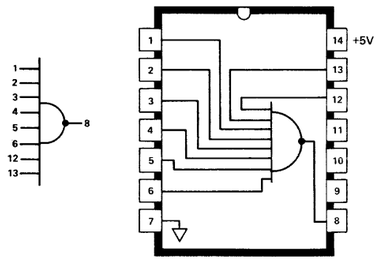
1820-0373



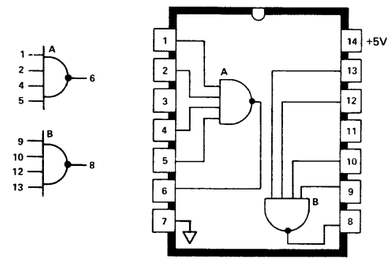
1820-0374



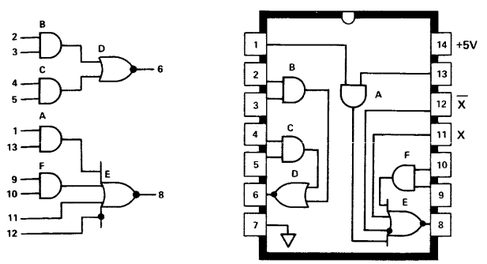
1820-0375



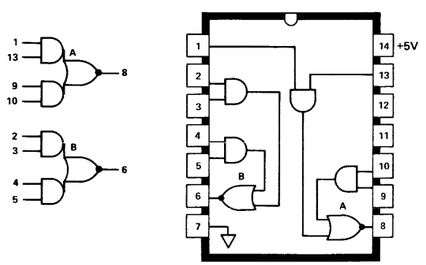
1820-0376



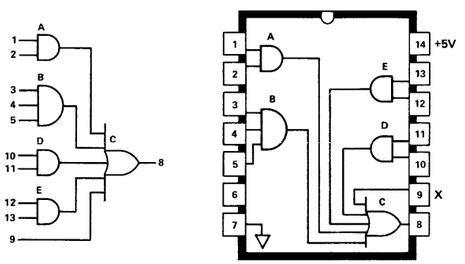
1820-0377



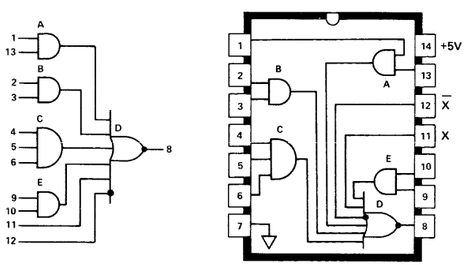
1820-0378



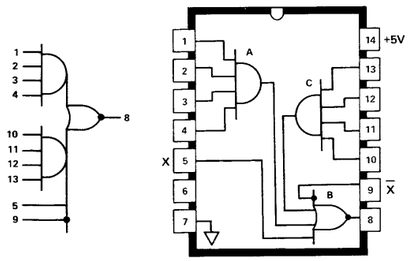
1820-0379



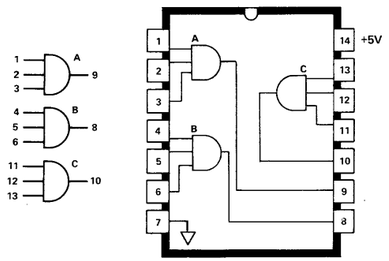
1820-0380



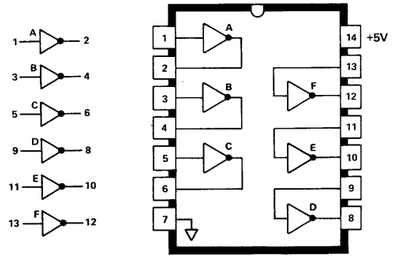
1820-0382



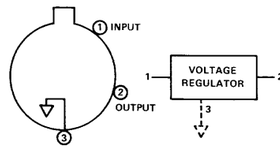
1820-0384



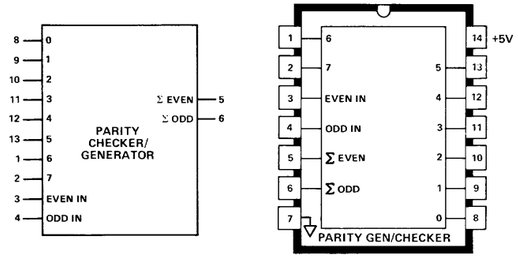
1820-0424



1820-0429



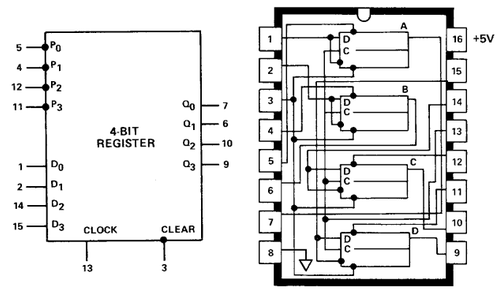
1820-0435



0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
–	1	1	0	0
–	0	0	1	1

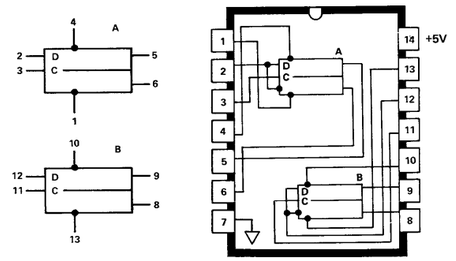
The eight data lines are tested to determine whether the true bits are even or odd. The EVEN and ODD inputs are interpreted as parity from another parity checker. (Note: the EVEN and ODD lines may also be interpreted as the expected parity.) The SUM EVEN and SUM ODD outputs are the combined parity of the two sets of data, refer to the table above. If the parity check mode is used the output of the SUM ODD line will indicate a parity error.

1820-0437

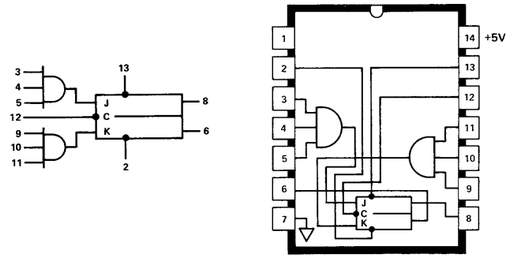


A low signal on any of the preset inputs (P_0-P_3) will cause the corresponding register bit to be set. A high on the clock line will cause the data on the D_0-D_3 lines to be stored. Data is stored on the positive going edge of the clock. A low on the CLEAR line clears the register.

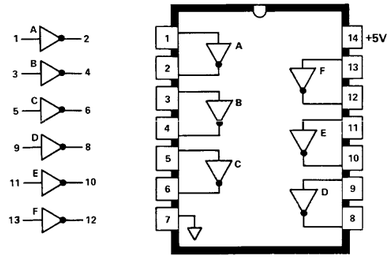
1820-0449



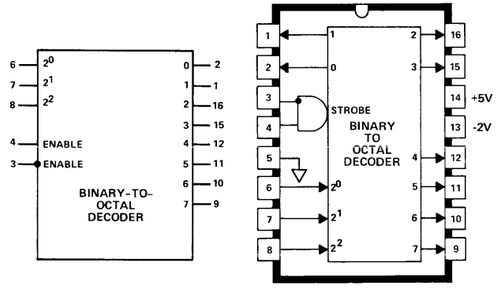
1820-0469



1820-0471

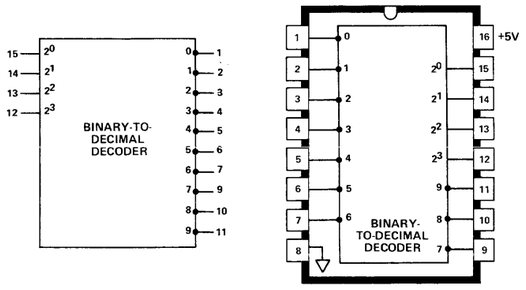


1820-0482



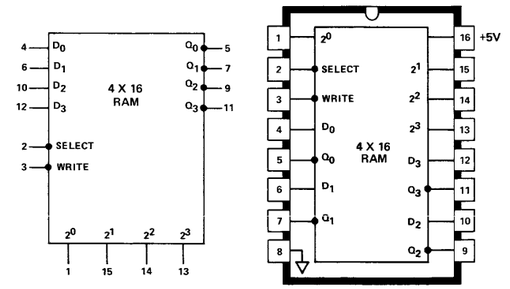
Binary input data is decoded to octal when both ENABLE conditions are met. For a given input only one output line will be high.

1820-0491



The binary input lines 2^0 through 2^3 appear directly as a decimal equivalent on the output lines 0 through 9 the selected output will be low. For binary inputs equivalent to decimal numbers greater than 9, all output lines will be high.

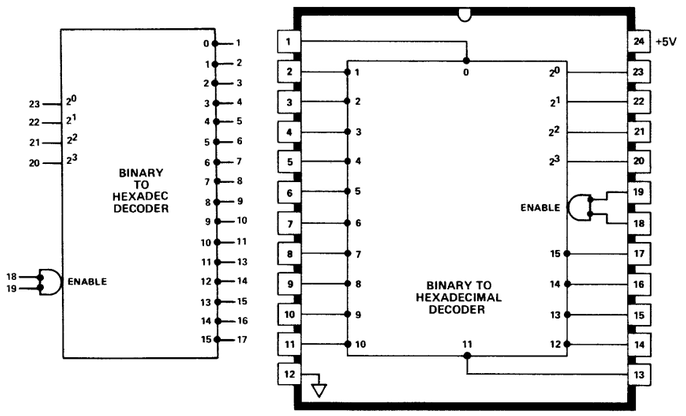
1820-0494



A low on the WRITE line will cause the data on the input lines (D_0-D_3) to be written into one of sixteen register locations. The location is selected by the address lines (2^0-2^3).

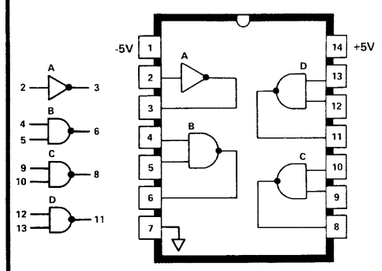
A low on the READ line will cause the data in the addressed location to be present on the output lines (Q_0-Q_3). The output data is inverted.

1820-0495

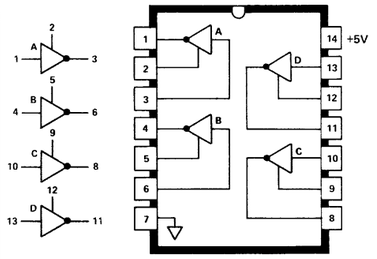


When both ENABLE inputs are low the binary coded input lines (2^0-2^3) are decoded and the equivalent output line (0-15) goes low.

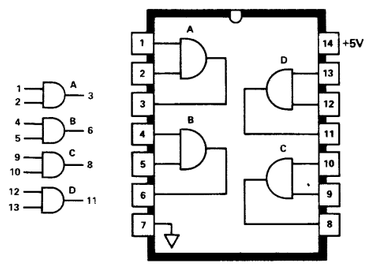
1820-0509



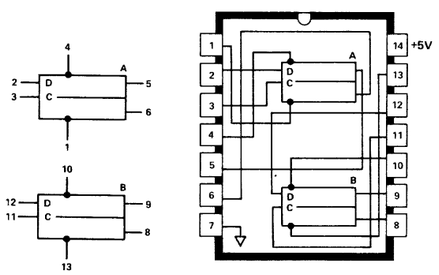
1820-0510



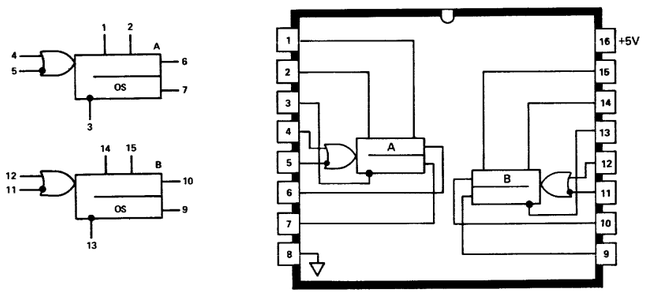
1820-0511



1820-0512

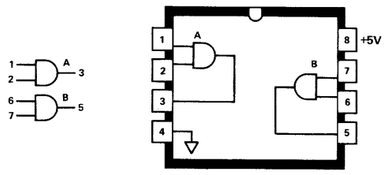


1820-0515

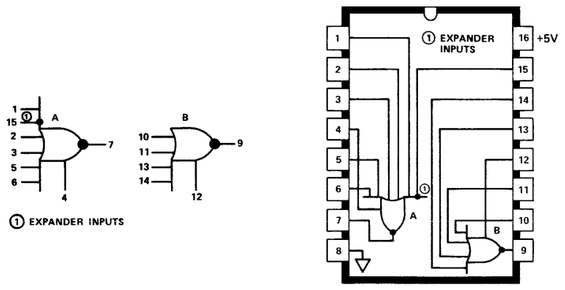


When either input condition is met the one-shot will generate an output pulse. The pulse width is determined by an external RC network. The circuit may be initialized by a low clear input.

1820-0535

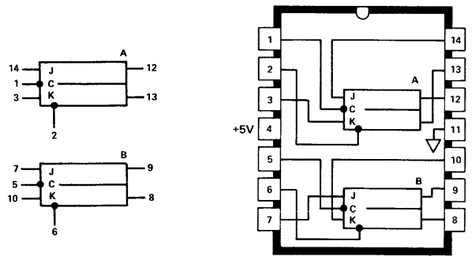


1820-0538

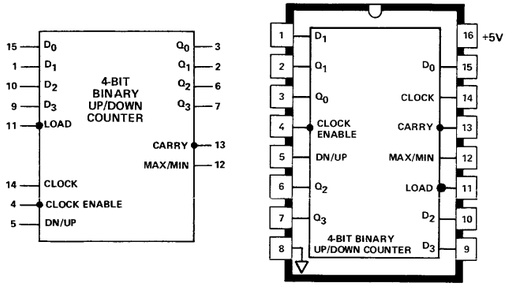


If any of the input lines are high or conditions for both expander inputs are present when the strobe input goes high, the output will go low.

1820-0544

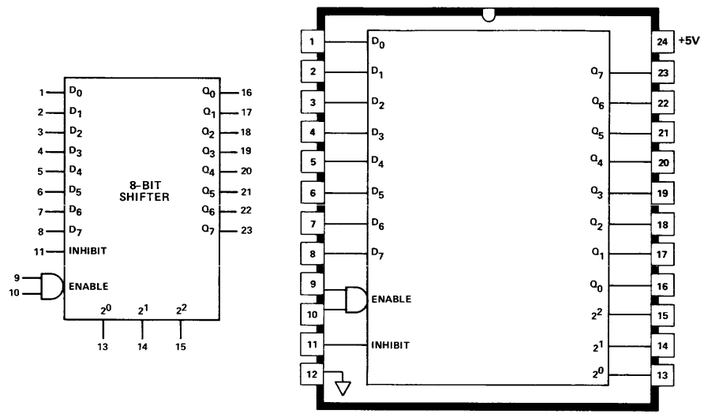


1820-0545



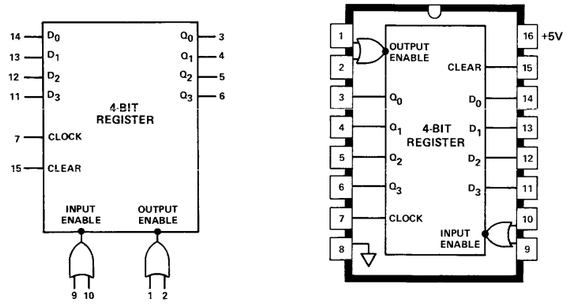
The counter is clocked by a low to high transition of the CLOCK line. The clock is effective only if the CLOCK ENABLE line is low. The CLOCK ENABLE line may only be changed while the CLOCK line is high. The direction of count is determined by the DN/UP line. If the DN/UP line is low the count is up. If the line is high the count is down. The counter may be preset with a low signal on the LOAD line. This will cause the data present on the input lines (D_0-D_3) to be stored. A low output signal is generated on the CARRY line if either a carry or borrow condition occurs. The MAX/MIN line outputs a high signal when the above conditions occur, but for a full clock cycle. This signal is used in "look-ahead carry" applications.

1820-0569



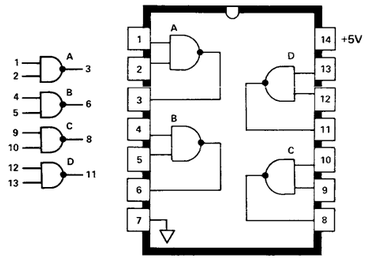
When the ENABLE conditions are met and the INHIBIT line is low, data on the input lines (D_0-D_7) is shifted and placed on the output lines (Q_0-Q_7). The control lines (2^0-2^2) determine the number of bit positions that are shifted. For example a code of 010 on 2^0-2^3 respectively will shift input bit D_2 to output bit position Q_0. Similarly input bit D_3 will be shifted to bit Q_1. Bits D_0 and D_1 will be lost. Bits Q_6 and Q_7 will contain "1's".

1820-0574

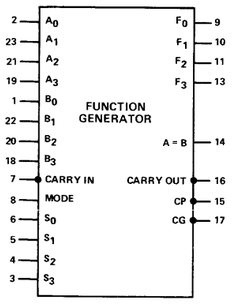


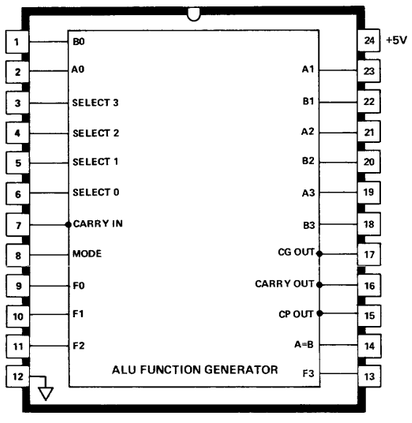
When INPUT ENABLE is true (both signal lines false) a true clock signal will cause data on the input lines to be stored. A true signal on the CLEAR line will clear the register. When OUTPUT ENABLE is true (both signal lines false) the contents of the register are gated to output lines Q_0 through Q_3.

1820-0605



1820-0606





The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A=B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met: $CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$

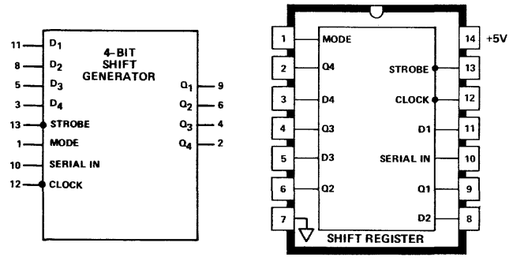
If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

The CG line will go false if the pack addition results in a true CARRY OUT independent of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

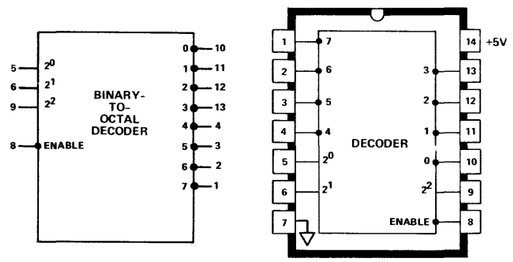
FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	F = A+$\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

1820-0607



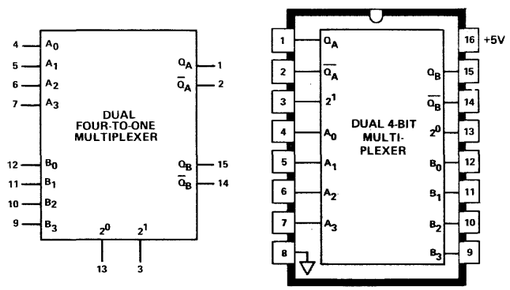
Data may be entered in serial or parallel. To enter serial data the MODE line must be low. Data is placed on the SERIAL Input line and a clock pulse is then used to enter the data. Parallel data entry is accomplished with the MODE line high and the data on the D input lines. The data is then entered by a STROBE pulse. Serial right shifting is accomplished by lowering the MODE line and pulsing the CLOCK line.

1820-0608



Binary data is decoded to octal when the ENABLE input is low. For a given input only one output line will be low.

1820-0610



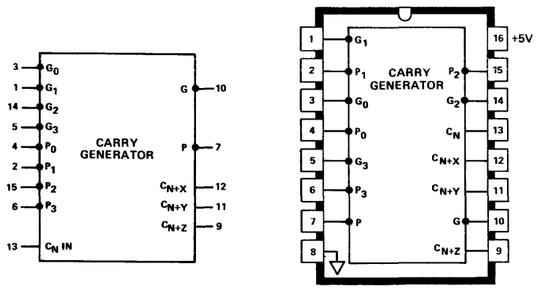
A two bit code selects one out of four bits to be propagated through the multiplexer. The dual output allows both states of the output bit to be used. A truth table of input codes and the resulting bit transfer is given above.

TRUTH TABLE

SELECT LINES		INPUTS				OUTPUTS	
2^1	2^0	A_0	A_1	A_2	A_3	Q_A	Q_A
0	0	0	X	X	X	0	1
0	0	1	X	X	X	1	0
0	1	X	0	X	X	0	1
0	1	X	1	X	X	1	0
1	0	X	X	0	X	0	1
1	0	X	X	1	X	1	0
1	1	X	X	X	0	0	1
1	1	X	X	X	1	1	0

X = irrelevant

1820-0611



This circuit is used together with 1820-0606 to provide fast addition. The Carry Generator uses CP (Carry Propagate) and CG (Carry Generate) signals from the adder circuits (P_0-P_3 and G_0-G_3) as well as the Carry In signal to the first adder circuit to provide carry in signals to succeeding adder circuits (C_{N+X}, C_{N+Y}, and C_{N+Z}). This is done without waiting for the "ripple carry" to propagate from adder to adder.

The G and P signals provide inputs to additional look ahead circuits if they are used. The output signals are defined as follows:

$$C_{N+X} = G_0 + P_0 C_N$$

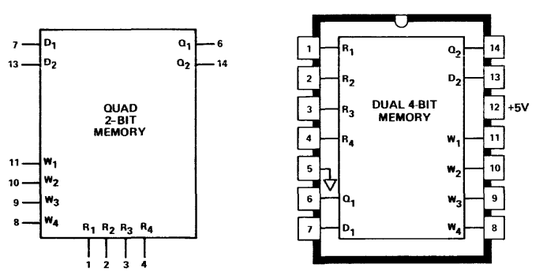
$$C_{N+Y} = G_1 + P_1 G_0 + P_1 P_0 C_N$$

$$C_{N+Z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_N$$

$$G = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$

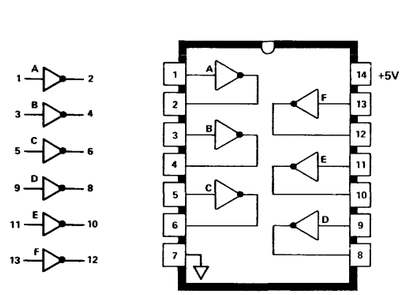
$$P = \overline{P_3 P_2 P_1 P_0}$$

1820-0612

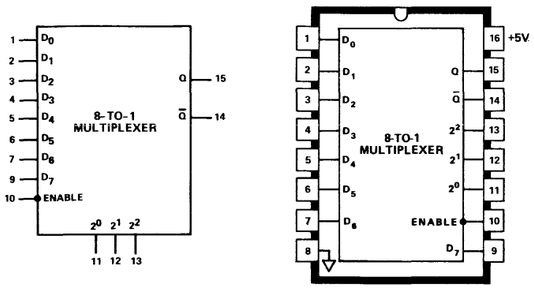


Data is written into the memory by placing the data on the D inputs and pulsing the appropriate W (Write) line. Data is read from the memory by pulsing the desired R (Read) line. The data will then be placed on the Q output lines for the duration of the read signal.

1820-0613

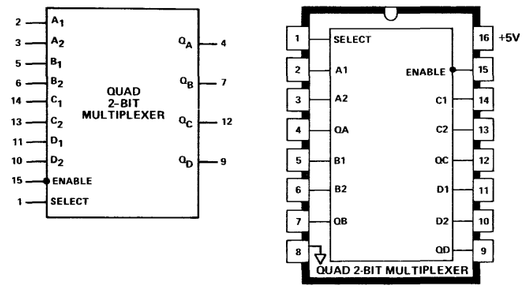


1820-0615



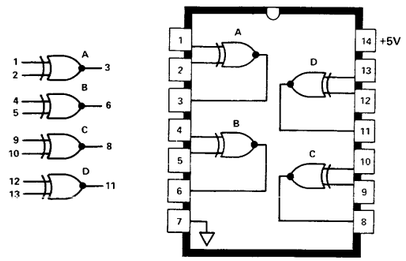
Data on one of the 8 input lines is transferred to the output line when the ENABLE line goes false. The specific input line to be transferred is determined by the three select lines.

1820-0616

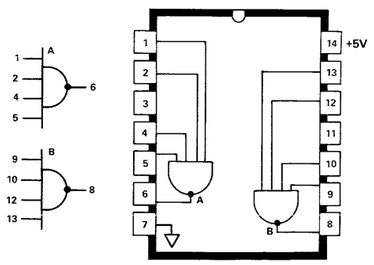


The circuit is used to select one of two four bit data words. The ENABLE must be low to allow the selection. The SELECT line is used to determine which data word will be transmitted. A "0" on the select line will transmit data word 1. A "1" on the select line will transmit data word 2.

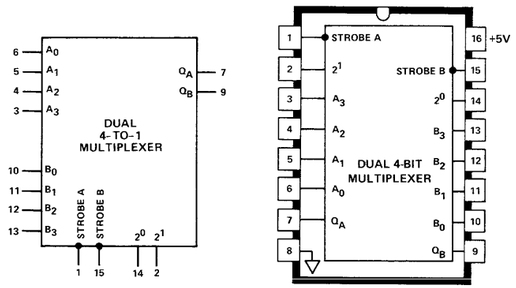
1820-0617



1820-0619



1820-0620



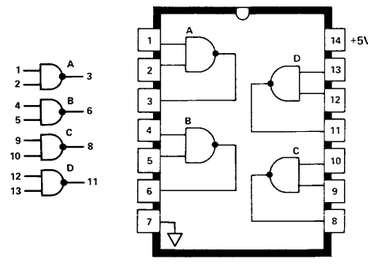
Each part of the multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

TRUTH TABLE

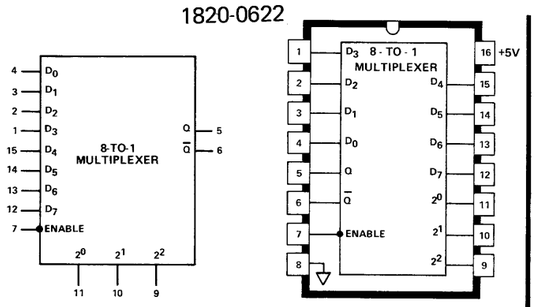
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs 2^0 and 2^1 are common to both sections.
X = irrelevant

1820-0621

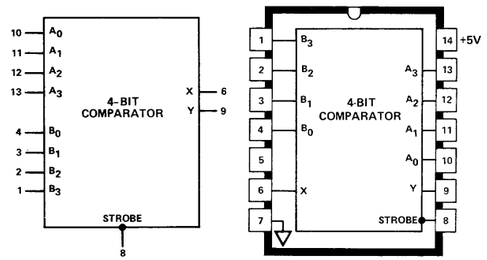


1820-0622



When the ENABLE line is false, the binary select lines 2^0 through 2^2 are used to determine one of the eight input through D_7 and apply it to the output lines Q and Q.

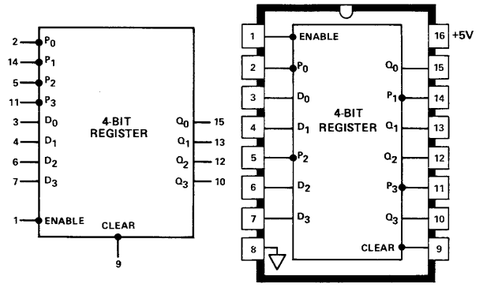
1820-0623



When the STROBE line goes low the A bits are compared with the B bit. The result of the comparison is present on the output lines for the duration of the strobe. The output is decoded according to the truth table shown.

RELATION	X	Y
A > B	1	0
A < B	0	1
A = B	1	1

1820-0626

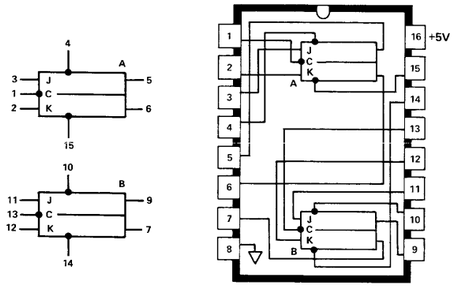


A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using the P input lines.

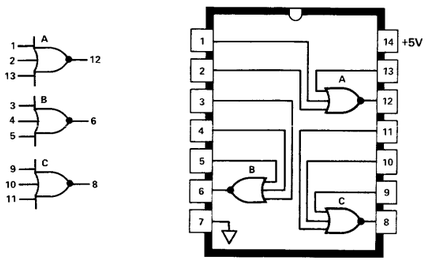
If the D inputs are used the P inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

If the S inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the S line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and S modes of operation.

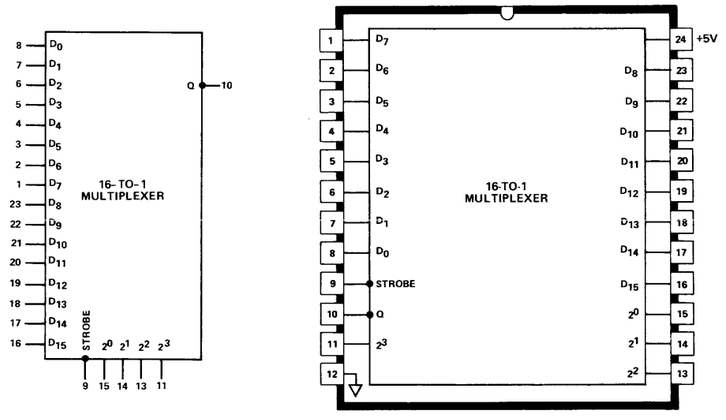
1820-0629



1820-0637

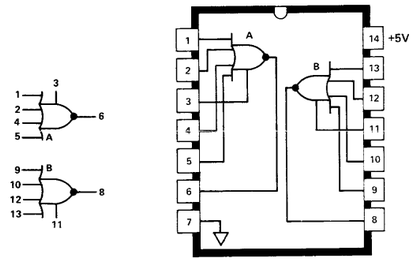


1820-0640



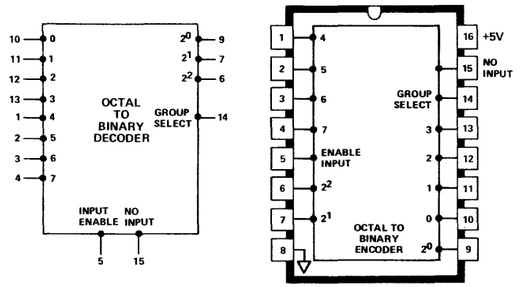
One of the 16 input data lines is selected by the select lines 2^0-2^3. A low signal on the STROBE line causes the selected data line to be inverted and made available on the Q output.

1820-0655



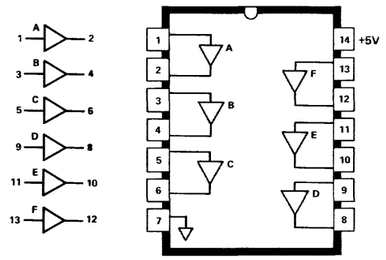
When the gate enable (strobe) is high and any gate input is high the gate output will go low.

1820-0657

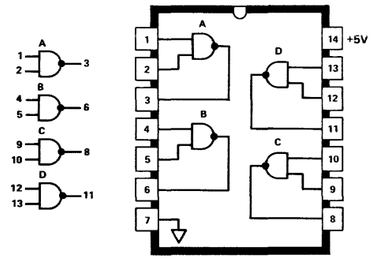


When the ENABLE INPUT line is low and one or more of the input lines 0-7 are low then the output lines making up the binary equivalent of the highest input line will go low. When this occurs the GROUP SELECT output signals also goes low. If the INPUT ENABLE line is low and none of the input lines are selected (go low) then the NO INPUT line goes low. This allows the next stage of a decoder to be enabled.

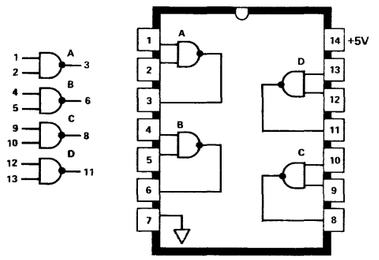
1820-0668



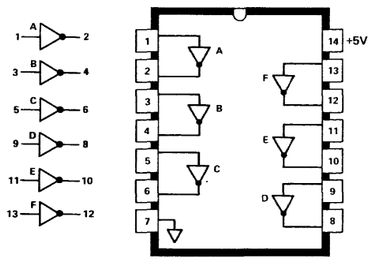
1820-0681



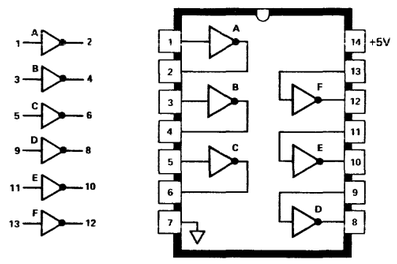
1820-0682



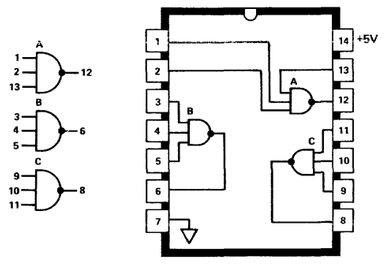
1820-0683



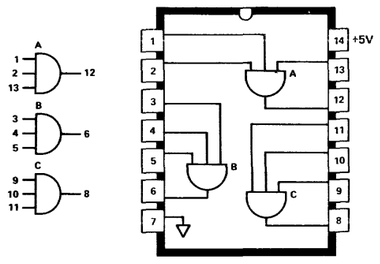
1820-0684



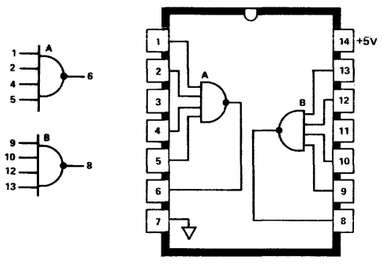
1820-0685



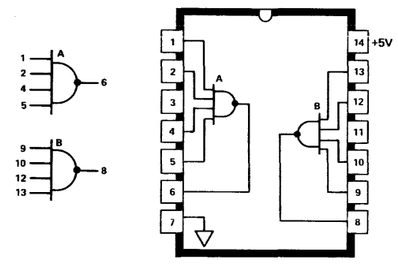
1820-0686



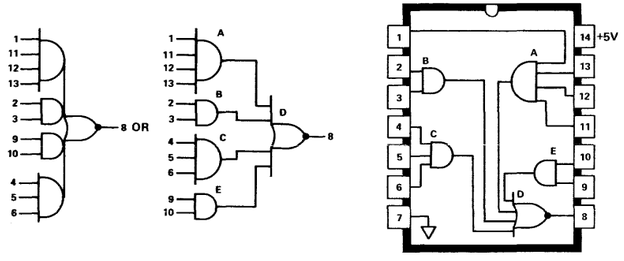
1820-0688



1820-0690



1820-0691



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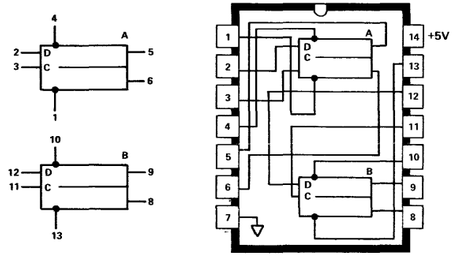
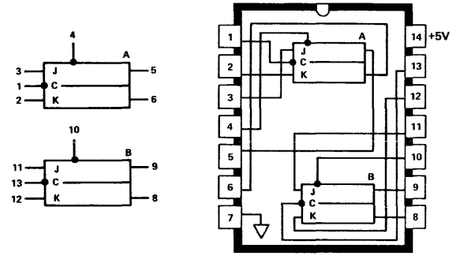


1820-0695



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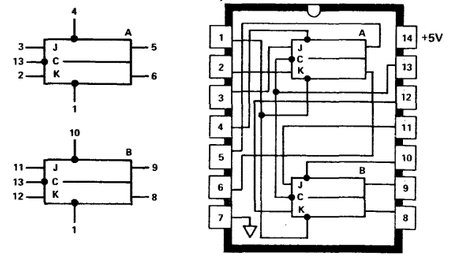
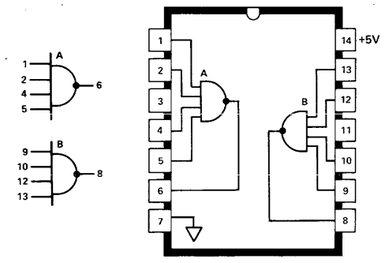
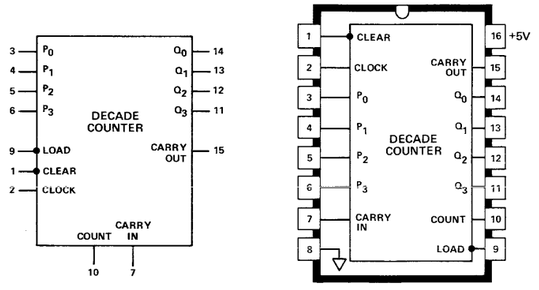


1820-0697



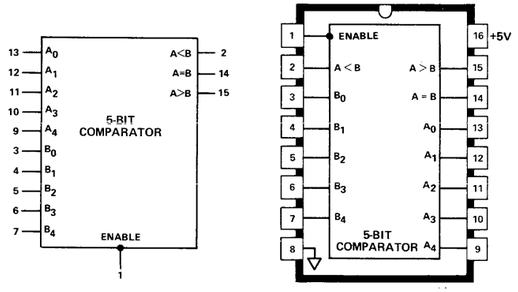
1820-0705



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

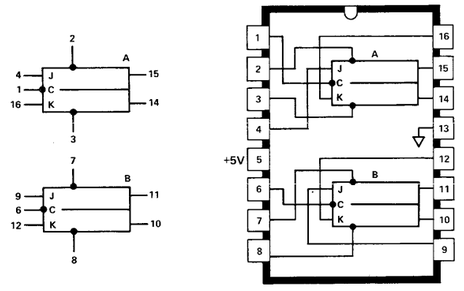
The CARRY OUT line will be high if the output lines Q_0-Q_3 equal nine (1001) and the CARRY IN line is high. The counter will be set to 0000 when the CLOCK line goes low.

1820-0706

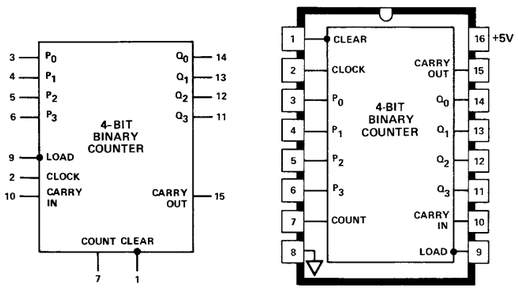


When the ENABLE line is low, input lines A_0 through A_4 are compared with B_0 through B_4. The appropriate output A>B, A=B, or A<B becomes true. The output remains unchanged until the ENABLE signal is removed and the input line signals changed.

1820-0715



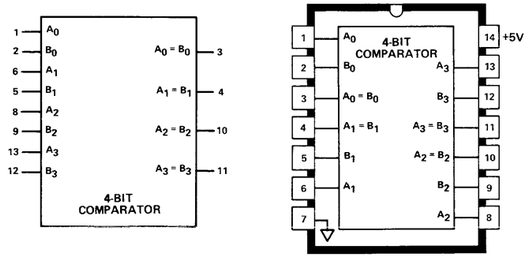
1820-0716



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0- P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0- Q_3) following the high-to-low transition of the clock.

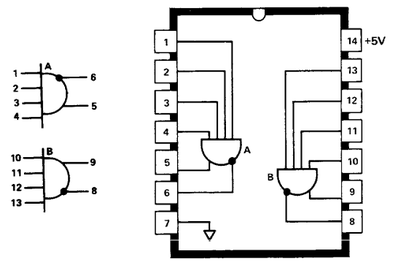
The CARRY OUT line will be high if the output lines Q_0- Q_3 are all high and the CARRY IN line is high.

1820-0719

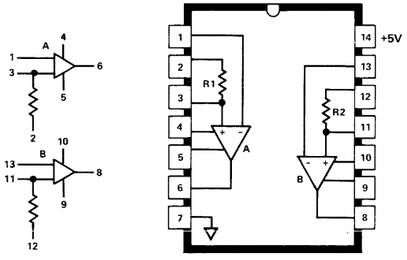


Four sets of two bits each are compared. If a set contains equal bits, the respective A_i=B_i output line becomes true. The output line remains true until the input bit pattern is changed.

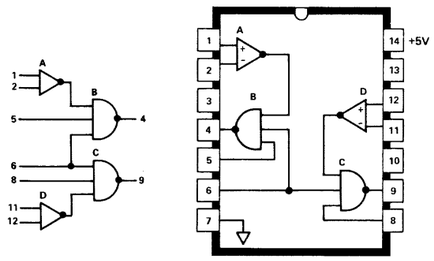
1820-0720



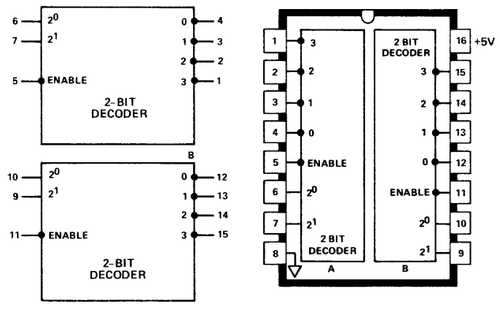
1820-0721



1820-0723

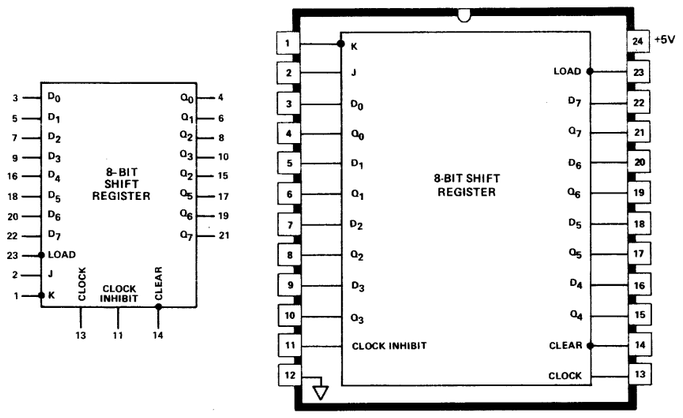


1820-0724



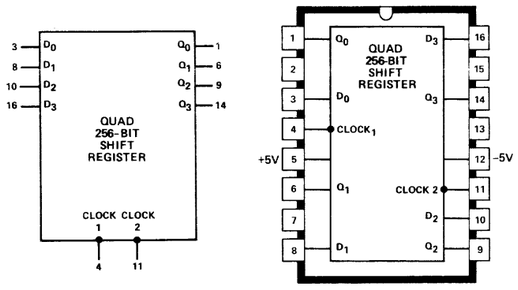
When the ENABLE line is low the input lines 2^0-2^1 select one of four output lines 0-4. The select line goes low.

1820-0726



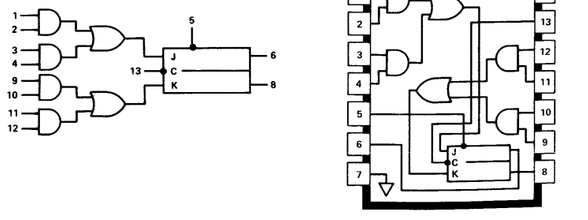
When the LOAD line is low data on the parallel input lines D_0-D_7 is loaded into the register. A low on the CLEAR line clears the register. The contents of the register are shifted one bit position (from D_0 to D_1 etc.) when the CLOCK INHIBIT line is low and a positive clock transition occurs. At this time the J and K inputs will be used to determine the next state of the D_0 bit position.

1820-0733

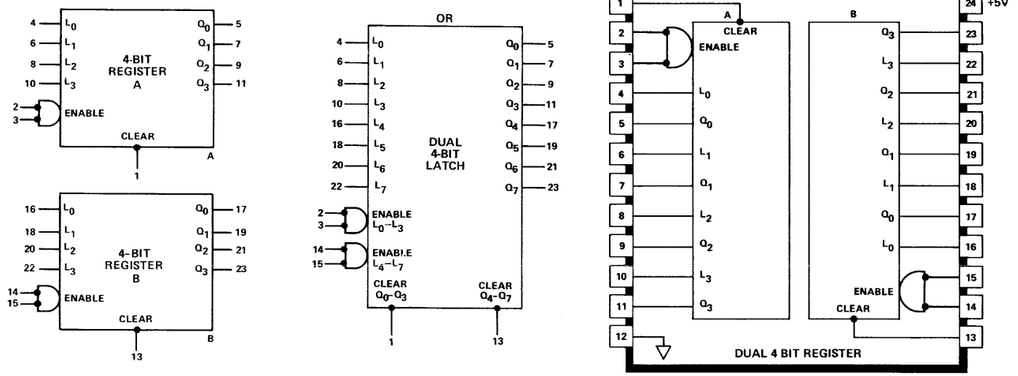


Data on input lines D_0-D_3 is loaded into the register by a high to low transition of either the CLOCK1 or CLOCK2 line. The same clock signal shifts the contents of the register one position and presents the next output bits on the Q_0-Q_3 lines. The register is circular containing 256 4-bit words.

1820-0739

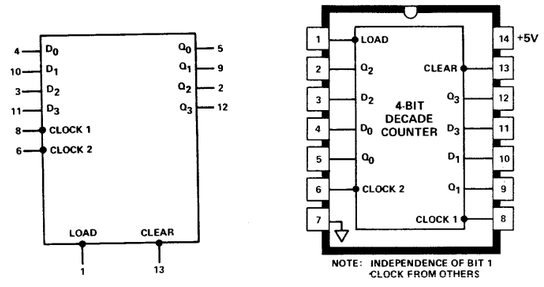


1820-0742



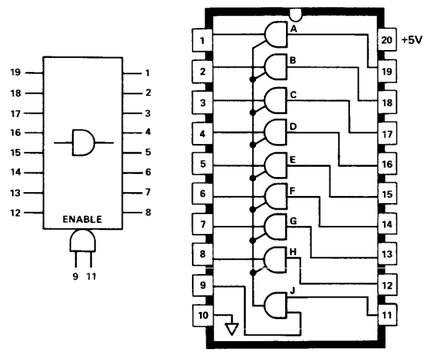
High inputs on both enable lines will cause the input data (L_0-L_3) to be stored in the register. The data is stored on the leading edge of the ENABLE signal. A low signal on the CLEAR line clears the register.

1820-0751

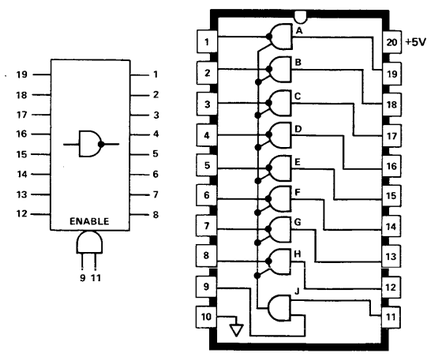


A low input on the LOAD line presets the counter with the data on the input lines D_0 through D_3. A low signal on the CLEAR line clears the counter. A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the counter to be incremented (counting to 5). If the Q_0 output is used to provide the CLOCK2 input, the counter will act as a decade counter.

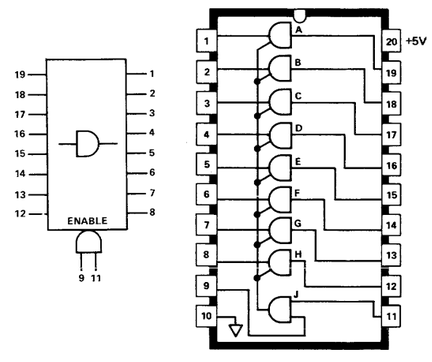
1820-0755



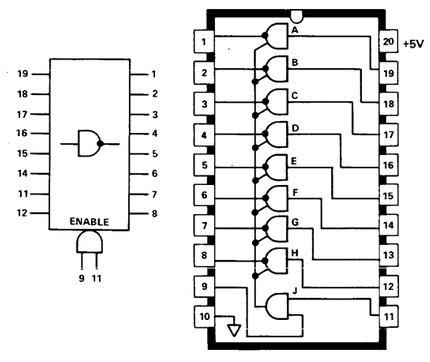
1820-0756



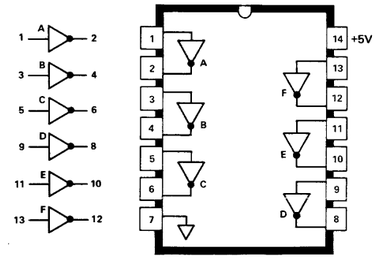
1820-0759



1820-0760

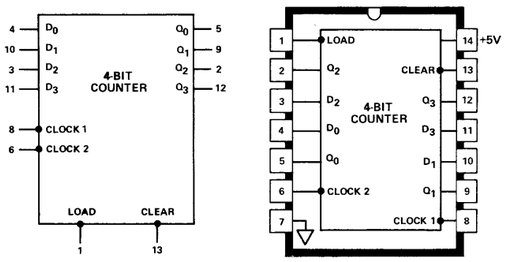


1820-0761



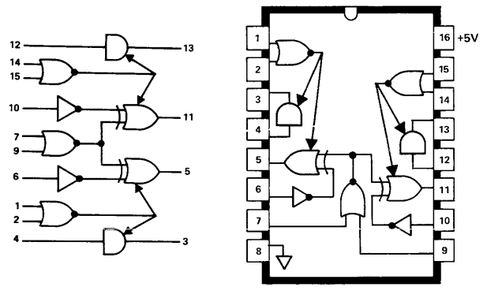
High signals on both enable lines gate the input data. The output data is inverted for 1820-0756 and 1820-0760.

1820-0765

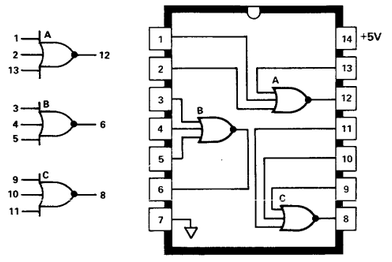


A low signal on the LOAD line presets the counter with the data on the input lines D_0 through D_3. A low signal on the CLEAR line clears the counter. A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the register to be incremented by one (counting to 7). If the Q_0 output is used to provide the CLOCK2 signal, the counter will act as a 4-bit binary counter.

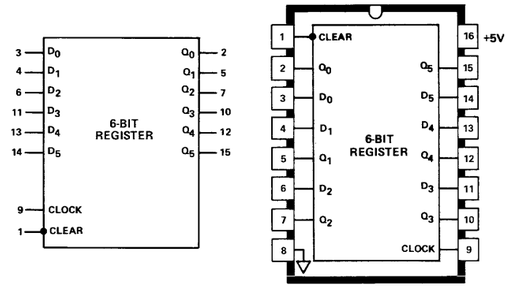
1820-0780



1820-0782

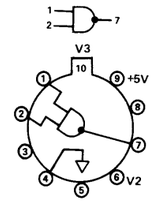


1820-0788



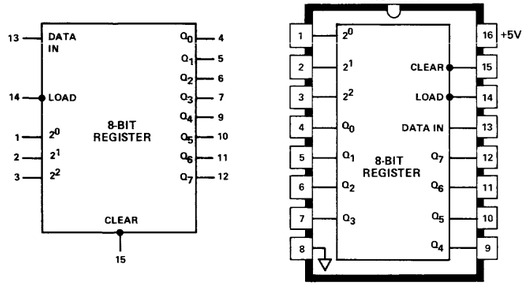
Data on the input lines is entered into the register by a positive going transition of the CLOCK line. The register is cleared by a low input on the CLEAR line.

1820-0832



Voltage references V2 and V3 determine the output signal level.

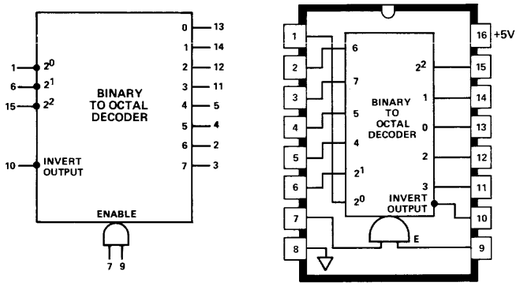
1820-0833



When the LOAD line is low the information on the DATA IN line will be stored in the register position selected by the address lines (2^0-2^2). A low CLEAR signal together with a high LOAD signal will cause the register to be cleared.

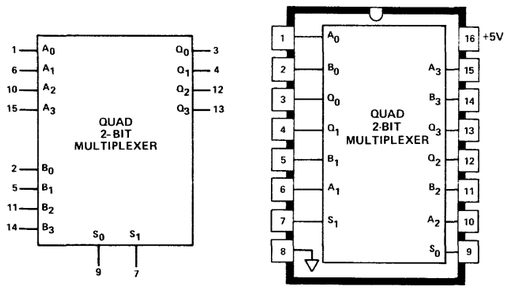
If both LOAD and CLEAR lines are low the register will act as a multiplexer, routing information on the DATA IN line to the output selected by the address lines.

1820-0834



When both enable inputs are high the binary code inputs (2^0-2^2) are decoded. The equivalent octal output (0-7) will go high or low if the INVERT input is high or low respectively.

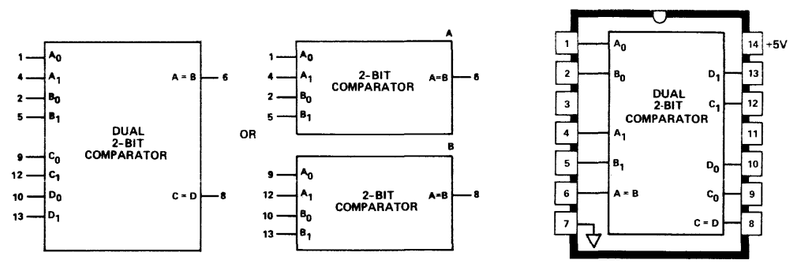
1820-0835



Input data (A_0-A_3 or B_0-B_3) is routed to the output lines (Q_0-Q_3) according to the table given below.

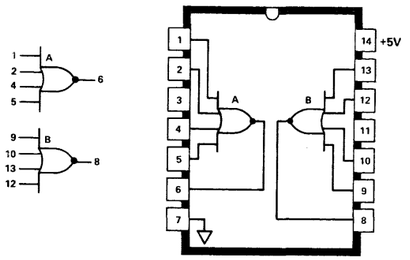
SELECT LINES		OUTPUT
S_0	S_1	Q_N
0	0	B_N
0	1	B_N
1	0	$\overline{A}_N$
1	1	1

1820-0836

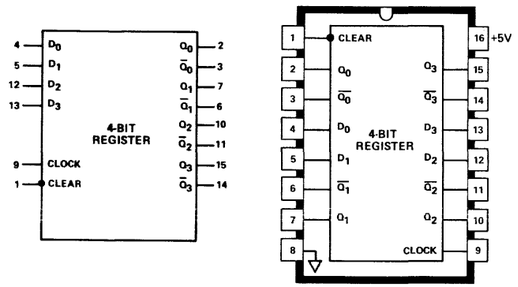


If the input bits A_0 and A_1 compare with the input bits B_0 and B_1 then the output line A=B will go high. Similarly for C and D bits.

1820-0837

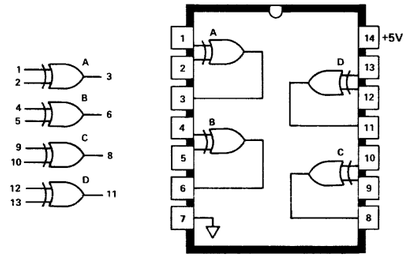


1820-0839

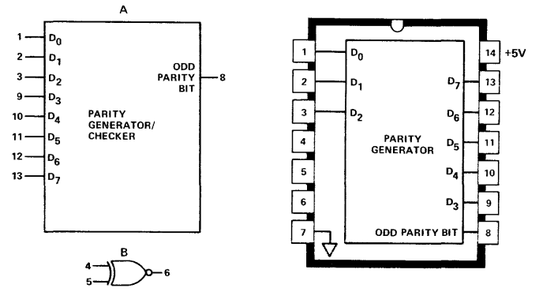


Data on the input lines (D_0-D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

1820-0841

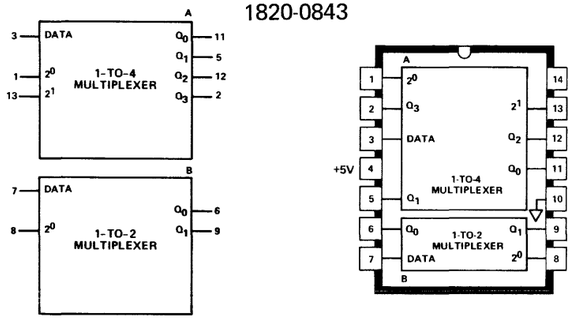


1820-0842



If all of the A input lines compare respectively with the B input lines, the A=B output line will go high. If the C input line compares with the D input line the C=D output line will go high.

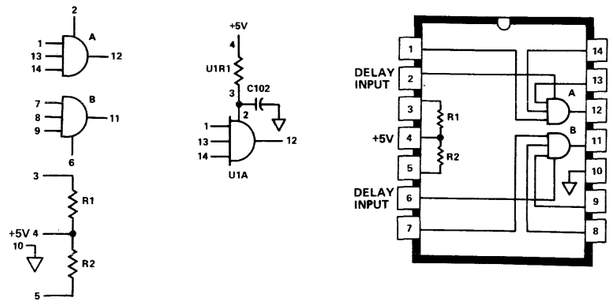
1820-0843



Element A multiplexes data on the DATA line to one of four output lines Q_0-Q_3. The output line is selected by the select lines 2^0 and 2^1.

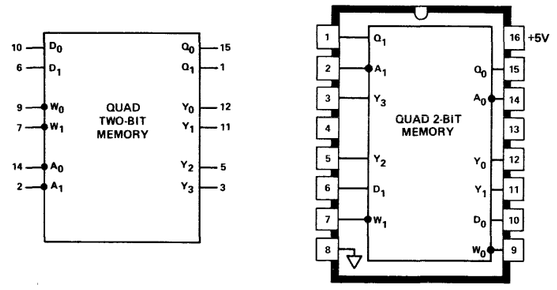
Element B multiplexes the data on the input line to one of the two output lines Q_0-Q_1. The output line is selected by the 2^0 select line.

1820-0844



The outputs of the gates are delayed by an amount determined by an external RC network.

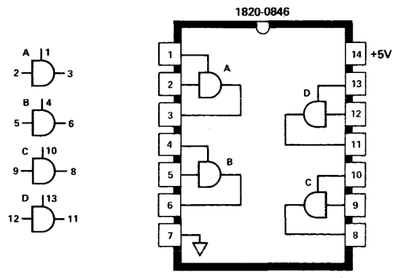
1820-0845



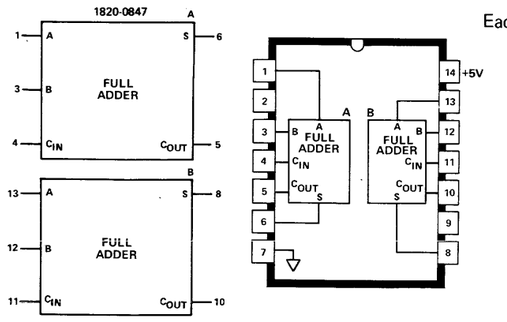
The memory is loaded by selecting the desired address with the W_0 and W_1 lines. Data present on the input lines D_0 and D_1 is then stored in the addressed word.

A word is read from memory by addressing the word with the A_0 and A_1 lines. The word content is then output to the Q_0 and Q_1 lines.

1820-0846



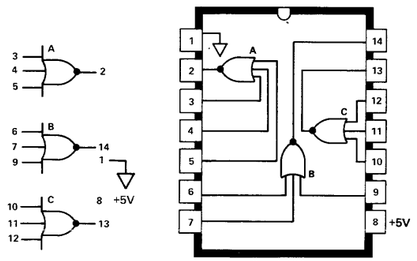
1820-0847



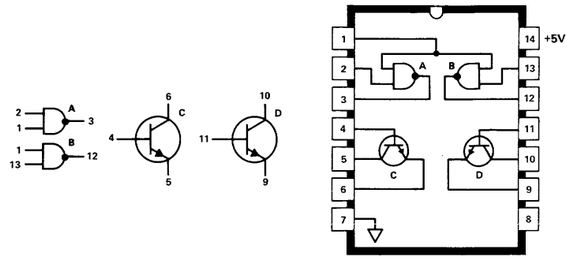
Each adder circuit functions as a normal full adder. Refer to the table given below.

A	B	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

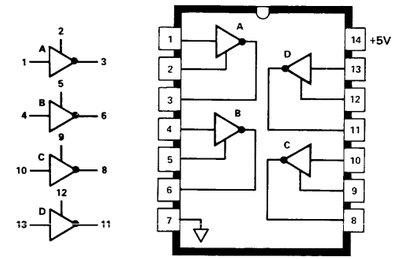
1820-0900



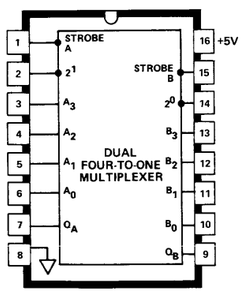
1820-0902



1820-0990



1820-0998



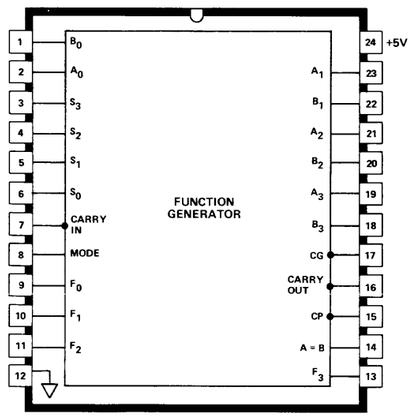
TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs S_0 and S_1 are common to both sections.
X = irrelevant

Each part of the multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

1820-0999



The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A=B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for the fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met:

$$CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$$

If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

The CG line will go false if the pack addition results in a true CARRY OUT independant of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	F = A+$\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

3-1. INTRODUCTION.

3-2. This section contains interconnecting wiring information for the computer. Signal lists for input/output PCA cabling as well as the backplane wiring list for the computer are provided. Instructions for replacing wiring are contained in the Central Processor Unit/Input Output Processor Unit (CPU/IOP) Maintenance Manual. Replace lead wires with the same color and size as on the original installation.

3-3. INPUT/OUTPUT BUS WIRING.

3-4. Power and some control signals are provided through the Power Bus to connector P1 of each input/output PCA. The Power Bus is located on a connector board mounted at the rear of the PCA module. The remaining input/output control and data signals are provided through two flat ribbon cables to connectors P2 and P3 of each input/output PCA. Connector P2 carries signals from the Multiplexer Channel (MUX CHAN) Bus and connector P3 carries signals from the Input/Output Processor (IOP) Bus.

3-5. If the PCA is used with the Selector Channel option, a fourth bus is used. This bus, the Selector Channel (SEL CHAN) Bus replaces the MUX CHAN Bus at connector P2 of the PCA. These two channel busses are the same except for the signal at pin 17.

3-6. Table 3-1 lists the four busses and the signals on each pin. A duplicate signal index is provided in section four with the diagram set for each input/output PCA.

3-7. BACKPLANE WIRING.

3-8. Signals between CPU/IOP PCA's are connected through the backplane wiring at the rear of the PCA module. Table 3-2 lists all of the signals in the backplane in alphabetic order. Signal names containing a bar (—) are listed separately. Each signal goes to only one pin of a given PCA. The connector and pin of each assembly wired to a signal is listed to the right of the signal name. For example, the signal BUSOP is connected to assembly 1A3, connector P2, pin 77 and to assembly 1A4, connector P1, pin 76.

3-9. POWER SUPPLY WIRING.

3-10. Information on the interconnection of power supply assemblies is contained in section four of this manual as a part of 30310A Power Supply Detailed Diagram Set DD-700. A power supply overall interconnection diagram is included as part of this diagram set. For further information concerning power supply wiring, refer to the separate power supply manual.

3-11. CABINET AND INTERMODULE WIRING.

3-12. Details concerning cabinet and PCA module wiring are contained in the cabinet and module maintenance manuals respectively.

Table 3-1. Input/Output Bus Wiring

POWER BUS P1		MUX CHAN BUS P2		SEL CHAN BUS P2		IOP BUS P3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1		1	CHAN SO	1	IODPRTY
2	+5V	2	CHAN SO	2	COM	2	IOD PE
3	+5V	3	COM	3	SR CLOCK	3	COM
4	+5V	4	SR CLOCK	4	COM	4	IOCMD 00
5	PF WARN	5	COM	5	DEV END	5	IOCMD 02
6	ENTIMER	6	DEV END	6	COM	6	IOCMD 01
7	(SPARE)	7	COM	7	ACK SR	7	COM
8	(SPARE)	8	ACK SR	8	COM	8	DEVNO 00
9	PWR ON	9	COM	9	CHAN ACK	9	DEVNO 01
10	COM	10	CHAN ACK	10	COM	10	COM
11	IORESET	11	COM	11	DEVNO DB	11	DEVNO 02
12	COM	12	DEVNO DB	12	SIO ENABLE	12	DEVNO 03
13	MCUCLKS	13	SIO ENABLE	13	EOT	13	COM
14	COM	14	EOT	14	JMP MET	14	DEVNO 04
15	COM	15	JMP MET	15	COM	15	DEVNO 05
16	COM	16	COM	16	TOGGLE INXFER	16	COM
17	-5V	17	TOGGLE INXFER	17	CHAN SR	17	DEVNO 06
18	-5V	18	TOGGLE OUTXFER	18	TOGGLE OUTXFER	18	DEVNO 07
19	COM	19	TOGGLE SIO OK	19	TOGGLE SIO OK	19	COM
20	COM	20	COM	20	COM	20	IOD 00
21	+15V	21	XFER ERROR	21	XFER ERROR	21	IOD 01
22	+15V	22	REQ	22	REQ	22	COM
23	+15V	23	COM	23	COM	23	IOD 02
24	+15V	24	SR 15	24	SR 15	24	IOD 03
25	-15V	25	SR 14	25	SR 14	25	COM
26	-15V	26	SR 13	26	SR 13	26	IOD 04
27	-15V	27	SR 12	27	SR 12	27	IOD 05
28	-15V	28	SR 11	28	SR 11	28	COM
29	COM	29	SR 10	29	SR 10	29	IOD 06
30	COM	30	COM	30	COM	30	IOD 07
31	-20V	31	SR 9	31	SR 9	31	COM
32	-20V	32	SR 8	32	SR 8	32	IOD 08
33	-20V	33	SR 7	33	SR 7	33	IOD 09
34	-20V	34	SR 6	34	SR 6	34	COM
35	+20V	35	SR 5	35	SR 5	35	IOD 10
36	+20V	36	COM	36	COM	36	IOD 11
37	+20V	37	SR 4	37	SR 4	37	COM
38	+20V	38	SR 3	38	SR 3	38	IOD 12
39	+20V	39	SR 2	39	SR 2	39	IOD 13
40	+20V	40	SR 1	40	SR 1	40	COM
41	HSREQ	41	SR 0	41	SR 0	41	IOD 14
42	COM	42	COM	42	COM	42	IOD 15
43	COM	43	P CMD 1	43	P CMD 1	43	COM
44	INTPOLL OUT	44	SET JMP	44	SET JMP	44	INTREQ
45	(SPARE)	45	P STATUS STB	45	P STATUS STB	45	(SPARE)
46	COM	46	P CONT STB	46	P CONT STB	46	COM
47	COM	47	RD NEXT WD	47	RD NEXT WD	47	(SPARE)
48	INTROLL IN	48	P WRITE STB	48	P WRITE STB	48	(SPARE)
49	SI	49	SET INT	49	SET INT	49	COM
50	COM	50	P READ STB	50	P READ STB	50	INTACK
51	COM						
52	DATAPOLL OUT						
53	SO						
54	COM						
55	COM						
56	DATAPOLL IN						

Table 3-2. Backplane Wiring List

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
ALUFC					P2-67						
ANDT				P1-49	P2-62						
BUSOP			P2-77	P1-76					P1-51		
CARRY				P2-22	P1-37						
CHACT									P2-62	P2-76	
CLOCK	P1-78	P1-78	P1-78	P1-78	P1-78	P1-78	P1-78	P1-78	P1-78		
CLOCKS				P1-11				P1-42	P1-42	P1-78	
CLSR				P2-50		P1-11					
CMPRFF	P2- 7							P1- 8			
CPURST	P2-78	P2-78	P2-78	P2-78	P2-78	P2-78	P2-78	P2-78	P2-78	P2-78	
CPURSTS				P1-23				P1- 3			
DATA			P2-42						P1-49		
DEVNO00										P2-37	P3-08
DEVNO01										P2-36	P3-09
DEVNO02										P2-38	P3-11
DEVNO03										P2-41	P3-12
DEVNO04										P2-43	P3-14
DEVNO05										P2-42	P3-15
DEVNO06										P2-44	P3-17
DEVNO07										P2-45	P3-18
DISPIOP	P1-1						P1-70				
DISPLAY	P2-27		P1-17	P1-41	P2-66	P1-72				P2-22	
DRTINH									P1-63	P1-16	
DSPFLAG					P2-72			P1- 1			
FREEZE	P1-79	P1-79	P1-79	P1-79	P1-79	P1-79	P1-79	P1-79	P1-79		
FUBUS	P2-23				P2-63						
HALT				P2-54				P1- 6			
HSREQ										P1-35	P1-41
INCSR				P2-55		P1- 5					
INCTR				P2-56			P2-61				
INTACK										P2-67	P3-50
INTREQ										P2-63	P3-44
IOCMD00										P2-33	P3-04
IOCMD01										P2-35	P3-06
IOCMD02										P2-34	P3-05
IOD 00										P2-47	P3-20
IOD 01										P2-46	P3-21
IOD 02										P2-48	P3-23
IOD 03										P2-49	P3-24
IOD 04										P2-51	P3-26
IOD 05										P2-50	P3-27
IOD 06										P2-52	P3-29
IOD 07										P2-53	P3-30
IOD 08										P2-55	P3-32
IOD 09										P2-54	P3-33
IOD 10										P2-56	P3-35
IOD 11										P2-57	P3-36
IOD 12										P2-59	P3-38
IOD 13										P2-58	P3-39
IOD 14										P2-62	P3-41
IOD 15										P2-61	P3-42
IOD PE										P2-31	P3-02
IODPRTY										P2-32	P3-01
IOFRZ									P1-61	P1-76	
IORESET				P1-12					P2-71	P1- 7	
IORSTSW				P1-21				P1- 4			
JBNDV				P2-63				P2-63			
JMPFRZ				P2-17					P1-33		
JMPGATE			P2-49	P1-69							
JMPJSBI					P2-56	P2-17					
JSBI			P2-72		P2-55						
MCU RST									P2-17		P2-49
MCUCL1R				P1- 6							
MCUCL2R				P1-10							
MCUCL3R				P1-14							
MCUCL4R				P1-18							
MCUCLK1				P1- 5							P1-13
MCUCLK2				P1- 9							P1-13
MCUCLK3				P1-13							P1-13
MCUCLK4				P1-17							P1-13
MCUCLK5				P1-30							P1-13
MCUCMPH	P2-25							P1-24			
MCUD PE									P2-15	P2- 6	P2-47
MCUHINT	P2-32							P1- 5			
MPIFRZ	P2-22								P1-35		
MSKRTRN										P1-45	

Table 3-2. Backplane Wiring List (Cont.)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
NOP				P1-51				P2-45			
NOP2				P1-37	P2-45	P2-79					
NOP2B			P2-41	P2- 4	P2-69						
NXT2				P1-24	P1-30						
NXTFINH				P1- 7					P1-32		
OUTBND										P1-17	
OUTBNDR										P1-18	
OVFL				P2-16	P1-44						
PADDX						P1- 3		P2-79			
PF WARN										P1-21	P1-05
PFWARNB				P1-16						P1-11	
PSELECT							P1-24		P2-58		
QUP							P2-75				
RARDIS		P2-65	P2-65								
RDIOM							P2-57			P2-18	
RDOPND							P2-71	P1-59	P1-25		
REPN					P2-68		P2-62				
ROMFCNT				P1-77	P1-66						
RSB			P2-71	P1-28							
RSSEL			P2-15		P2-34						
SAME				P1-68	P1-77						
SFQ0						P2- 7	P1-17				
SHFTCLK	P1-75				P2-53	P1-47		P1-47	P2-38	P1-15	
SI										P1-41	P1-49
SKIPNOP				P1-64	P1-73						
SLOAD	P1-76				P2-61	P2-56		P1-48	P2-37	P1-14	
SO										P1-43	P1-53
SPV			P2-51					P2-44			
STIOM				P2-24			P2-76			P1-62	
STKBNOP				P1-52				P2-49			
SWLDRAR	P2-17	P2-47	P2-47		P1-65			P2-22			
SYS PE									P2-33	P2- 3	P2-48
T=0				P2-18	P1-76						
TENB									P2-34		
TINT		P1-17		P1-26							
TMRFRZI				P2-41					P1-47		
TR0						P1-52	P2-67				
TR1						P1-69	P2-65				
TR2						P1-15	P2-64				
TR3						P1-25	P2-63				
UBNT				P1-67	P2-11						
UNFRZ	P2-24								P1-29		
4XCLK				P1- 1							
4XCLKR				P1- 2							
ALPHA				P2-36		P2-10					
ALUMODE					P1-75						
ALUS0					P1-26						
ALUS1					P1-29						
ALUS2					P1-28						
ALUS3					P1-27						
BMCUPRTY								P2- 3	P1-37		
BNDV	P1- 7			P2-12				P1-22			
CARRY	P1- 6			P2- 9	P1-38						
CCPX	P1-77			P2-52	P1-68			P1-17	P1-56	P2-11	
CIR 04						P2-12		P1-49			
CIR 07					P2-29			P1-50			
CIR 08					P2-31			P1-51			
CIR 12						P2-72		P1-52			
CIR 13						P2-74		P1-53			
CIR 14						P2-75		P1-54			
CIR 15						P2-76		P1-55			
CLFLAG03			P2-48							P2-26	
CLOCKENB	P2-31		P1-27								
CNTRMAX			P1-63				P2-59				
COR 00							P1-29		P2-52		
COR 01							P1-28		P2-54		
COR 02							P1-27		P2-56		
COR 10							P2-25		P1-41		
COR 11							P2-26		P1-43		
COR 13							P2-29		P1-46		
COR 14							P2-27		P1-44		
COR 15							P2-28		P1-45		
CPUHRFF									P2-64		
CPUIN								P2- 4	P1- 4		
CPULOSEL	P1-19								P2-63		

Table 3-2. Backplane Wiring List (Cont.)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
CPULRFF									P2-61		
CPUSEL							P2-37		P1-76		
CPUTIMER	P1- 3			P2-69					P1-24		
DATAPE								P2- 7	P1-21		
DATAPOLL										P1- 1	
DATAPOLR										P1- 2	
DECSR				P2-43		P1-32					
DISPFLAG	P1-36				P1-67						
DS	P1-26					P2- 4		P2-70			
DVSB				P2-26	P2-57						
ENABLE00									P2-25		P2-40
ENABLE01									P2- 9		P2-41
ENABLE02									P2-27		P2-42
ENABLE03									P2-11		P2-43
ENABLE04									P2-29		P2-44
ENABLE05									P2-13		P2-45
ENABLROM		P2-68	P2-68								
ENTIMER	P2-21			P2-75					P1-31	P1-23	P1-06
ERFRZINH	P2-26								P1-23		
EXTCLK				P1- 3							BNC
EXTINT	P1- 9							P1- 9		P1- 8	
FHB				P2-38	P1-13						
FLAG1	P1-13			P2-19	P1-15						
FLAG2	P1-15			P2- 3	P1-74						
FLAG3	P1-16			P1-61						P1- 5	
FPNLOS	P2- 5							P1-19			
FROM 00									P2- 4		P2-25
FROM 01									P2-12		P2-26
FROM 02									P2- 6		P2-27
FRUNCLK	P1-29			P1-38							
INCNAMFR				P2-58		P1-35					
INCP				P1-25			P1- 7				
INDIRECT				P1-34				P2-68			
INHROMJ1		P2-66	P2-66								
INSTSEL	P1-23								P2-41		
INTCLKM	P2-38			P1-15							
INTFLAG	P1-35				P1-48						
INTPOLL										P1-79	
INTPOLLR										P1-80	
INTRP	P1- 5			P1-59				P1-14	P1-27		
IOAPE										P2-12	
IOCMP									P2-70	P1- 3	
IOERROR									P2-49	P2- 7	
IOFLG1				P2-23						P2-19	
IOHIREQ									P2-45	P1- 4	
IOHRQFF									P2-36	P2-10	
IOHSEL									P2-53	P2-24	
IOHSREQ									P1-62	P1-10	
IOILG										P2- 9	
IOINP	P1-32								P1-64	P2- 5	
IOLOREQ									P2-47	P2-27	
IOLOSEL									P2-55	P2-21	
IOLRQFF									P2-35	P2- 8	
IOMOP 00									P1-66	P2-25	
IOMOP 01									P1-67	P1- 6	
IORESET										P1-33	P1-11
IOSTROBE									P2-51	P1-12	
IOTIMER	P1- 4				P1-46				P1-65	P2-23	
IOTO 01									P1-69	P2-75	
IOTO 02									P1-68	P2-77	
JLUI1		P2-61		P1-24							
JLUI2			P1-22	P1- 3							
JMPJSR			P2-10	P2-71							
JUMPER01							P1-25				
							P2-15				
JUMPER02							P1-26				
							P2-17				
LUTGATE	P1-27	P2-55	P1-75					P2-57			
MCIOTMR									P2-68	P2-29	
MCUCMP	P1-17							P1- 7			
MCUCMPL	P2- 3							P1-23			
MCUD 00							P1-54	P1-63		P1-51	P2-02
MCUD 01							P1-53	P1-62		P1-49	P2-03
MCUD 02							P1-56	P1-65		P1-55	P2-04
MCUD 03							P1-55	P1-64		P1-53	P2-05

Table 3-2. Backplane Wiring List (Cont.)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
MCUD 04							P1-58	P1-67		P1-59	P2-06
MCUD 05							P1-57	P1-66		P1-57	P2-07
MCUD 06							P1-61	P1-68		P1-61	P2-09
MCUD 07							P1-62	P1-69		P1-63	P2-10
MCUD 08							P2-43	P1-70		P1-65	P2-11
MCUD 09							P2-44	P1-71		P1-67	P2-12
MCUD 10							P2-45	P1-72		P1-69	P2-13
MCUD 11							P2-46	P1-73		P1-71	P2-15
MCUD 12							P2-47	P1-74		P1-73	P2-16
MCUD 13							P2-48	P1-75		P1-75	P2-17
MCUD 14							P2-49	P1-76		P1-77	P2-18
MCUD 15							P2-50	P1-77		P1-70	P2-19
MCUDPRTY									P1-72	P1-72	P2-20
MCUINT								P1-10	P1-22		
MDPARITY							P2-13		P1-77		
MODINT								P1-12	P1-38		
MOP 00									P2-14		P2-28
MOP 01									P2- 8		P2-29
NEXT				P1-57					P2-72		
NIP	P1-33							P2- 5	P2-74		
NIPTOCIR				P2-79				P2-24			
NOP1	P1-11			P1-65	P2- 1				P1-26		
NOP2	P1-12			P1-66	P2-52	P1-49	P1-73		P1-52		
NUMERIC				P2-34		P2-32					
NXT1			P2-63		P1-23						
NXT=1	P1-37		P2-53	P1-53							
NXT=2	P1-38		P2-57	P1-55	P1-71	P1-71					
NXTDCD				P1-33			P2-73	P2-47	P1-30		
NXTGATE				P1-35		P2-34					
OFCENB				P2-35	P2-79						
OPINP	P1-34							P2- 1	P2-76		
OPNDSEL	P1-24								P2-66		
OVFL	P1- 8			P2-21							
P-T01							P1-19		P2-28		
P-T02							P1-21		P2-32		
P1-14										P1-37	P1-45
P1-3										P1-27	P1-08
P1-4										P1-25	P1-07
P3-45										P2-64	P3-45
P3-47										P2-66	P3-47
P3-48										P2-65	P3-48
PADDIN08								P2-27		P2-74	
PADDIN09								P2-26		P2-67	
PADDIN10								P2-25		P2-73	
PADDIN11								P2-24		P2-72	
PADDSUR								P1- 7		P2-77	
PADDXS00								P1-13		P2-75	
PADDXS01								P1- 9		P2-76	
PANLREAD	P2-18				P2-33						
PANLSTOR	P2-19		P2-32		P2-17						
PAUSE										P2-65	
POLLORS0									P1-28	P1-30	
PRTYMODE					P1-43		P2-16				
PWR ON				P1-36						P1-29	P1-09
PWR ONR			P2-69	P1-19				P2-69			
PWRFAIL				P1-29				P1-11			
QS	P1-25							P2-71	P2- 3		
R 00			P1-65		P1-12	P1-21					
R 01			P1-67		P1-11	P1-22					
R 02			P1-66		P1- 9	P1-23					
R 03			P1-68		P1-10	P1-24					
R 04			P1-69		P1-61	P1-50					
R 05			P1-71		P1-62	P1-51					
R 06			P1-70		P1-63	P1-53					
R 07			P1-72		P1-64	P1-55					
R 08			P1-74		P2-10	P2-15					
R 09			P1-75		P2- 9	P2-21					
R 10			P1-73		P2- 8	P2-22					
R 11			P1-76		P2- 7	P2-23					
R 12			P1-50		P2-47	P2-61					
R 13			P1-56		P2-48	P2-64					
R 14			P1-52		P2-49	P2-63					
R 15			P1-54		P2-51	P2-66					
RAR 00	P2-61	P1-16	P1-16								
RAR 01	P2-62	P1-15	P1-15								

Table 3-2. Backplane Wiring List (Cont)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
RAR 02	P2-58	P1-14	P1-14								
RAR 03	P2-57	P1-13	P1-13								
RAR 04	P2-54	P1-12	P1-12								
RAR 05	P2-53	P1-11	P1-11								
RAR 06	P2-56	P1-10	P1-10								
RAR 07	P2-55	P1- 9	P1- 9								
RAR 08	P2-51	P1- 8	P1- 8								
RAR 09	P2-52	P1- 7	P1- 7								
RAR 10	P2-49	P1- 6	P1- 6								
RAR 11	P2-50	P1- 5	P1- 5								
RDCIR						P2-13		P1-46			
RDCPX1							P2-53	P1-25	P1- 5		
RDCPX2					P1-45		P2-54	P1-57	P2-44		
RDJMPR					P1-55	P2-11					
RDMOD							P2-55		P1-75		
RDSWITCH							P1-41	P1-58			
READY 00									P2- 1		P2-33
READY 01									P2-19		P2-34
READY 02									P2- 3		P2-35
READY 03									P2-21		P2-36
READY 04									P2- 5		P2-37
READY 05									P2-23		P2-38
READY 06									P2- 7		P2-31
REPEAT	P1-10		P2-33	P1-48	P2-41						
RESRVD A	P1-22										
RESRVD B	P1-21										
RF 00	P1-49		P2-56			P2-16					
RF 01	P1-47		P2-54			P2- 5					
RF 02	P1-48		P2-52			P2-54					
RF 03	P1-45		P2-50			P1-58					
RFINH					P2-54	P1-70					
RFSAME					P2-27	P2-31					
RMCUCPX1								P1-21	P1- 6		
ROM 00		P1- 4	P1- 4								
ROM 01		P1- 3	P1- 3								
ROM 02		P1-21	P1-21								
ROM 03		P1-24	P1-24								
ROM 04		P1-27	P1-27								
ROM 05		P1-25	P1-25								
ROM 06		P1-23	P1-23								
ROM 07		P1-26	P1-26								
ROM 08		P1-28	P1-28								
ROM 09		P1-36	P1-36								
ROM 10		P1-32	P1-32		P1-31						
ROM 11		P1-31	P1-31		P1-32						
ROM 12		P1-35	P1-35		P1-33						
ROM 13		P1-34	P1-34		P1-34						
ROM 14		P1-33	P1-33		P1-35						
ROM 15		P1-38	P1-38								
ROM 16		P1-41	P1-41								
ROM 17		P1-43	P1-43								
ROM 18		P1-45	P1-45								
ROM 19		P1-47	P1-47								
ROM 20		P1-51	P1-51								
ROM 21		P1-53	P1-53								
ROM 22		P1-55	P1-55								
ROM 23		P1-57	P1-57								
ROM 24		P1-42	P1-42								
ROM 25		P1-44	P1-44								
ROM 26		P1-46	P1-46								
ROM 27		P1-48	P1-48								
ROM 28		P1-61	P1-61								
ROM 29		P1-64	P1-64								
ROM 30		P1-63	P1-63								
ROM 31		P2-18	P2-18								
ROMFCN1			P1-37		P2-32						
RORT 10	P1-52				P2-44						
RORT 11	P1-53				P2-43						
RORT 12	P1-46				P2-24						
RORT 13	P1-43				P2-25						
RORT 14	P1-44				P2-46						
RORT 15	P1-41		P2-17	P1-62			P2-72				
RORT 16	P1-72		P2- 6	P2-14			P2-56				
RORT 17	P1-71		P2- 5	P1-74			P2-58				
RORT 18	P1-70		P2- 4	P1-72			P2-66				

Table 3-2. Backplane Wiring List (Cont.)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
RORT 19	P1-69		P2- 3	P1-70			P2-68				
RORT 20	P1-63		P2-10		P1-59						
RORT 21	P1-64		P2- 9		P1-49						
RORT 22	P1-65		P2- 8		P1-50						
RORT 23	P1-66		P2- 7	P2-53					P1-53		
RORT 24	P1-54		P2-25	P2-47					P1-54		
RORT 25	P1-57		P2-27	P2-49					P1-59		
RORT 26	P1-56		P2-28	P2-44					P1-57		
RORT 27	P1-55		P2-29	P2-46					P1-55		
RPTFCN				P1-50	P2-12						
RREG 00				P2-57	P1-41						
RUNFF	P2- 4			P2-77				P1-13			
S 00					P1- 1	P1-26	P1- 3	P1-26	P1- 9	P1-22	
S 01					P1- 4	P1-43	P1- 4	P1-27	P1- 3	P1-24	
S 02					P1- 5	P1-44	P1- 5	P1-28	P1- 7	P1-26	
S 03					P1- 6	P1-37	P1- 6	P1-29	P1- 1	P1-28	
S 04					P1-54	P1-12	P1-35	P1-31	P1-70	P1-32	
S 05					P1-53	P1-10	P1-36	P1-32	P1-74	P1-34	
S 06					P1-52	P1- 8	P1-37	P1-33	P1-73	P1-36	
S 07					P1-51	P1- 6	P1-38	P1-34	P1-71	P1-38	
S 08					P2- 3	P2-70	P2- 3	P1-35	P1-12	P1-42	
S 09					P2- 4	P2-65	P2- 4	P1-36	P1-14	P1-44	
S 10					P2- 5	P2-68	P2- 5	P1-37	P1-11	P1-46	
S 11					P2- 6	P2-67	P2- 6	P1-38	P1-16	P1-48	
S 12					P2-38	P2-69	P2-33	P1-41	P1-18	P1-50	
S 13					P2-37	P2-71	P2-34	P1-43	P1-15	P1-52	
S 14					P2-36	P2-73	P2-35	P1-44	P1-17	P1-54	
S 15					P2-35	P2-77	P2-36	P1-45	P1-19	P1-56	
SCIR	P2-14							P1-56			
SDISFLAG				P2-45	P1-70						
SF 00	P1-67		P2-21				P2-49	P1-13			
SF 01	P1-68		P2-24				P1-66	P1-16			
SF 02	P1-74		P2-23				P2-50	P1-18			
SF 03	P1-73		P2-26				P2-48	P1-75			P1-66
SF 04	P1-62		P2-22				P2-47	P1-76			P1-68
SFSAME					P2-28		P2-74				
SINTFLAG				P2-51	P1-69						
SIOP	P2- 9										P1- 9
SKIP	P1-28		P2-70	P1-42							
SMCUDATA	P2-13							P1-61			
SP1 00					P2-76	P1- 1					
SP1IN					P2-65	P2-57					
SP1SHIFT					P2-75	P2- 9					
SP3 15					P2-64		P2-51				
SP3IN					P2-26		P1- 8				
SP3SHIFT					P2-58		P2-77				
SR 00				P1-58		P1-27		P2-61			
SR 01				P1-71		P1-33		P2-51			
SR 02				P2- 6		P1-34					
SRBUS	P2-12					P2-58					
SRDYENRL	P2-15								P2-43		
SRREG	P2-59				P2-77						
SRVOUT1									P2-50	P1-19	
SSBUS	P2-11					P2-55					
SSREG	P2-29				P2-73						
ST 00	P1-61		P2-35			P2-51	P2- 1		P2-67		
ST 01	P1-59		P2-36			P2-53	P1-14		P2-65		
ST 02	P1-58		P2-37			P2-52	P1-15		P2-69		
ST 03	P1-50		P2-38			P1-54	P1-71		P1-50	P1-64	
ST 04	P1-51		P2-34			P1-56	P1-72			P1-58	
STATUS00				P1-56			P1-47				
STATUS01				P1-45			P1-48	P1-16	P1-34	P1-13	
STATUS02				P1-43			P1-49	P1-18			
STATUS03				P1-54			P1-50	P2- 6			
STATUS04				P2- 7			P1-43	P1-15			
STATUS05				P2-11			P1-44				
STATUS06				P2- 5			P1-45				
STATUS07				P2-15			P1-46				
STOFROM	P2-16								P1-58		
STORAR		P2-48				P2- 6		P2-21			
STSTATUS				P1-31			P2-69				
SYSPRTY									P2-18		P2-32
T 00				P2-33	P1-16						
T 15					P1-25						
TEST1				P1- 4							

Table 3-2. Backplane Wiring List (Cont.)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
TEST2				P1- 8							
TNAME 00	P1-18					P1-77	P1-51				
TNAME 01	P1-14					P1-75	P1-52				
TO 00									P2-16		P2-22
TO 01									P2-22		P2-23
TO 02									P2-10		P2-24
U 00	P2-77			P2-25	P1- 8	P1-57	P1- 9	P2-23			
U 01	P2-10			P1-44	P1-14	P1-61	P1-10		P1-36		
U 02	P2-75			P1-46	P1- 7	P1-63	P1-11		P1- 8		
U 03	P2-76			P1-47	P1-17	P1-65	P1-12	P2-26			
U 04	P2-72			P2-32	P1-18	P1-67	P1-31	P2-27			
U 05	P2-71			P2-31	P1-19	P1- 4	P1-32	P2-28			
U 06	P2-74			P2-29	P1-21	P1-45	P1-33	P2-29	P1-10		
U 07	P2-73			P2-13	P1-22	P1-46	P1-34	P2-31	P1-48		
U 08	P2-69			P2- 8	P2-13	P2-35	P2- 7	P2-32		P2-13	
U 09	P2-70				P2-14	P2-36	P2- 8	P2-33			
U 10	P2-68				P2-15	P2-33	P2- 9	P2-34			
U 11	P2-67				P2-16	P2-37	P2-10	P2-35			
U 12	P2-65				P2-19	P2-44	P2-21	P2-36			
U 13	P2-66				P2-21	P2-43	P2-22	P2-37			
U 14	P2-63				P2-22	P2-46	P2-23	P2-38			
U 15	P2-64			P2-27	P2-23	P2-45	P2-24	P2-41			
U-T01							P1-23		P2-24		
U-T02							P1-22		P2-26		
V 00	P2-45		P2-76					P2- 8			
V 01	P2-48		P2-75					P2- 9			
V 02	P2-47		P2-74					P2-10			
V 03	P2-42		P2-73					P2-11			
V 04	P2-46		P2-46					P2-12			
V 05	P2-43		P2-45					P2-13			
V 06	P2-44		P2-44					P2-14			
V 07	P2-41		P2-43					P2-15			
V 08	P2-36		P2-14					P2-16			
V 09	P2-33		P2-13					P2-17			
V 10	P2-35		P2-12					P2-18			
V 11	P2-37		P2-11					P2-19			
W	P1-31							P2-55			

4-1. INTRODUCTION.

4-2. This section contains diagram sets for the printed circuit assemblies (PCA's) used in the HP 3000 Computer System. Diagrams for cabinet electrical power systems are contained in separate manuals.

4-3. Each diagram set contains a schematic diagram, signal index, part location diagram, and integrated circuit index for one assembly. The diagram set documenting the 30310A Power Supply (set no. 700) treats the entire power supply as a single assembly. The diagram sets are numbered according to the list given in table 4-1.

4-4. SCHEMATIC DIAGRAMS.

4-5. The schematic diagrams are multisheet drawings. The drawings use a grid coordinate system which runs continuous over the entire drawing set. Each schematic sheet is broken into vertical grids A, B, C, etc. The horizontal grids start with grid 1 and continue numerically, ten grids for each sheet, throughout the diagram set.

4-6. Signals entering or leaving a sheet are shown with the grid coordinate of the source or destination. the Grid coordinate is always made up of a letter and a number and is set off from the signal name by parentheses.

4-7. An explanation of the logic symbology used in the schematic diagrams following this section is provided in section II. Section II also contains descriptions of the operation of complex integrated circuits used in the computer system.

4-8. SIGNAL INDEXES.

4-9. Each diagram set contains a signal index. This index lists the signals present at each pin of the various PCA connectors. Signals not used on the PCA but present on the connector pin are listed for reference. The signals are listed by pin number for each connector used. Some PCA's do not use all six connectors.

4-10. Signals between PCA's may be CPU/IOP Bus, or device controller signals. Signals used by the CPU/IOP PCA's are shown in a backplane wiring list, table 3-2. Signals on the I/O Bus are shown in table 3-1. Device controller signals are listed with the diagram sets and in the respective controller manuals.

4-11. PART LOCATION DIAGRAMS.

4-12. Each diagram set contains a part location diagram for the PCA or PCB documented by the set. The part location diagram provides information for locating connectors, pins, and components.

4-13. INTEGRATED CIRCUIT INDEXES.

4-14. Each diagram set contains an integrated circuit index for the PCA or PCB documented by the set. The integrated circuit index provides a cross reference between the integrated circuit references used on the schematic diagrams and the HP part number of the circuit. The part number may be used to reference a circuit description in section II or to replace the part.

Table 4-1. Detailed Diagrams Index

IN THIS MANUAL	DD SET NO.	TITLE
	200	READ-ONLY MEMORY (ROM) PCA (30001-60001)
	201	SKIP AND SPECIAL FIELD (SSF) PCA (30001-60002)
	202	ARITHMETIC AND LOGIC UNIT (ALU) PCA (30001-60003)
	203	R-BUS PCA (30001-60004)
	204	S-BUS PCA (30001-60005)
	205	CURRENT INSTRUCTION REGISTER (CIR) PCA (30001-60006)
	206	MODULE CONTROL UNIT (MCU) PCA (30001-60007)
	207	INPUT/OUTPUT PROCESSOR (IOP) PCA (30001-60008)
	208	CENTRAL DATA BUS TERMINATOR PCA (30001-60009)
	209	INPUT/OUTPUT PROCESSOR BUS TERMINATOR PCA (30001-60016)
	210	POWER BUS TERMINATOR PCA (30001-60021)
	211	CONTROL PCB (30001-60010)
	300	MEMORY LOAD PCA (30005-60001)
	301	MEMORY DATA AND CONTROL PCA (30005-60002)
	302	MEMORY DRIVE AND SENSE PCA (30006-60002)
	404	SYSTEM CLOCK/CONSOLE INTERFACE PCA (30031-60001)
	405	MULTIPLEXER CHANNEL PCA (30035-60001)
	500	UNIVERSAL INTERFACE (TTL) PCA (30050-60001)
	501	UNIVERSAL INTERFACE (DIFFERENTIAL) PCA (30051-60001)
	502	UNIVERSAL INTERFACE (TTL) PCA (30050-60003)
	503	SYNCHRONOUS SINGLE LINE CONTROLLER PCA (30055-60001)
	508	TERMINAL DATA INTERFACE PCA (30060-60001)
	509	TERMINAL CONTROL INTERFACE PCA (30061-60001)
	600	DISC FILE READ/WRITE PCA (30202-60001)
	601	DISC FILE BUS PCA (30202-60002)
	602	DISC CONTROLLER PROCESSOR PCA (30202-60003)
	603	DISC MEMORY CONTROLLER PCA (30203-60001)
	604	DISC MEMORY DATA PCA (30203-60002)
	605	CARD READER INTERFACE PCA (30206-60001)
	606	CARTRIDGE DISC CONTROLLER PCA (30210-60001)
	607	MAGNETIC TAPE (9 TRACK) CONTROLLER PCA (30215-60001)
	608	MAGNETIC TAPE CONTROLLER PROCESSOR PCA (30215-60002)
	609	MAGNETIC TAPE (7 TRACK) CONTROLLER PCA (30217-60001)
	700	30310A POWER SUPPLY
	800	AUXILIARY CONTROL PANEL INPUT PCB (30350-60001)
	801	AUXILIARY CONTROL PANEL DISPLAY PCB (30350-60002)
	802	AUXILIARY CONTROL PANEL INTERFACE PCA (30350-60006)
	803	INPUT/OUTPUT MAINTENANCE PANEL INTERFACE PCA (30351-60001)
	804	HARDWARE MAINTENANCE PANEL INPUT PCB (30352-60001)
	805	HARDWARE MAINTENANCE PANEL DISPLAY PCB (30352-60002)

Changed 9 FEB 1973

CPU/IOP DETAILED DIAGRAM SET

DD-200

READ ONLY MEMORY (ROM) PCA

30001-60001

SERIES ~~1314~~ 1403

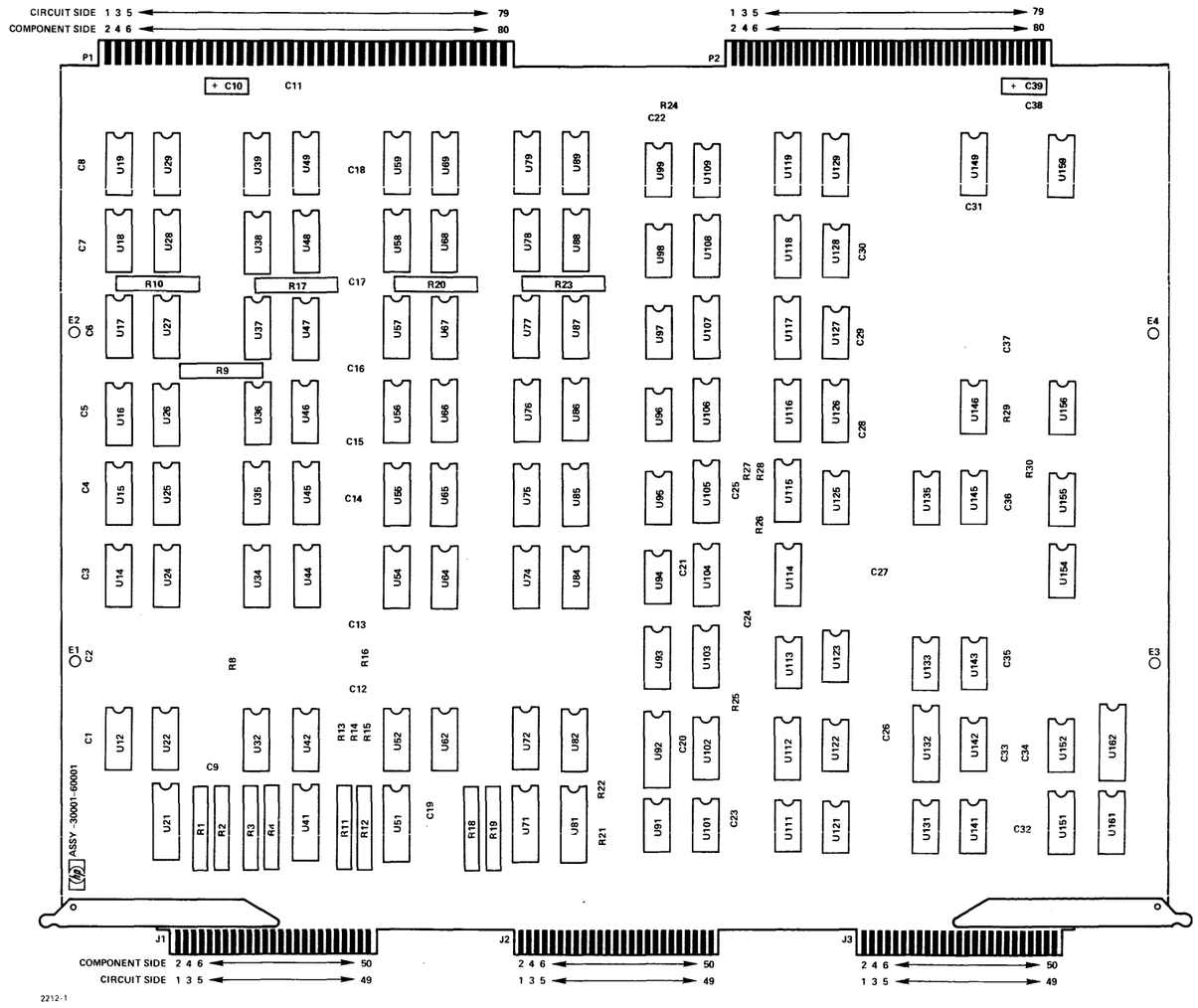
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	COM	1	COM	1	—
2	COM	2	COM	2	—
3	ROM01	3	RORT19	3	IROM16
4	ROM00	4	RORT18	4	IROM0
5	RAR11	5	RORT17	5	IROM17
6	RAR10	6	RORT16	6	IROM1
7	RAR09	7	RORT23	7	IROM18
8	RAR08	8	RORT22	8	IROM2
9	RAR07	9	RORT21	9	IROM19
10	RAR06	10	RORT20	10	IROM3
11	RAR05	11	V11	11	IROM20
12	RAR04	12	V10	12	IROM4
13	RAR03	13	V09	13	IROM21
14	RAR02	14	V08	14	IROM5
15	RAR01	15	RSSEL	15	IROM22
16	RAR00	16		16	IROM6
17	DISPLAY	17	RORT15	17	IROM23
18	+5V	18	ROM31	18	IROM7
19	+5V	19	+5V	19	IROM24
20	+5V	20	+5V	20	IROM8
21	ROM02	21	SF00	21	IROM25
22	+5V	22	SF04	22	IROM9
23	ROM06	23	SF02	23	IROM26
24	ROM03	24	SF01	24	IROM10
25	ROM05	25	RORT24	25	IROM27
26	ROM07	26	SF03	26	IROM11
27	ROM04	27	RORT25	27	IROM28
28	ROM08	28	RORT26	28	IROM12
29	COM	29	RORT27	29	IROM29
30		30		30	IROM13
31	ROM11	31		31	IROM30
32	ROM10	32	PANLSTOR	32	IROM14
33	ROM14	33	REPEAT	33	IROM31
34	ROM13	34		34	IROM15
35	ROM12	35		35	—
36	ROM09	36		36	ENABLROM
37	ROMFCN1	37		37	BRAR0
38	ROM15	38		38	BRAR1
39	COM	39	COM	39	BRAR2
40	COM	40	COM	40	BRAR3
41	ROM16	41	NOP2B	41	BRAR4
42	ROM24	42	DATA	42	BRAR5
43	ROM17	43	V07	43	BRAR6
44	ROM25	44	V06	44	BRAR7
45	ROM18	45	V05	45	BRAR8
46	ROM26	46	V04	46	BRAR9
47	ROM19	47	SWLDRAR	47	BRAR10
48	ROM27	48	STORAR	48	BRAR11
49	COM	49	JMPGATE	49	—
50	R12	50	RF03	50	—
51	ROM20	51	SPV		
52	R14	52	RF02		
53	ROM21	53	NXT=1		
54	R15	54	RF01		
55	ROM22	55	LUTGATE		
56	R13	56	RF00		
57	ROM23	57	NXT=2		
58	+5V	58			
59	+5V	59	+5V		
60	+5V	60	+5V		
61	ROM28	61	JLUI1		
62	+5V	62			
63	ROM30	63	NXT1		
64	ROM29	64			
65	R00	65	RARDIS		
66	R02	66	INHROMJ1		
67	R01	67			
68	R03	68	ENABLROM		
69	R04	69	PWR ONB		
70	R06	70	SKIP		
71	R05	71	RSB		
72	R07	72	JSB1		
73	R10	73	V03		
74	R08	74	V02		
75	R09	75	V01		
76	R11	76	V00		
77		77	BUSOP		
78	CLOCK	78	CPURST		
79	FREEZE	79	COM		
80	COM	80	COM		

NOTE: "XXX" INDICATES A CONNECTION WITH NO SIGNAL NAME.
"—" INDICATES NO CONNECTION TO PIN.

I.C. INDEX

U	1820-	U	1820-	U	1820-
21,41,51,71	0759	121	0373	151	0574
81	0755	122	0282	152	0282
		123	0374	154	0374
91	0373	125	0141	155	0424
92	0755	126	0574	156	0837
93	0574	127,128	0846		
94	0690	129	0574	161	0574
95	0140			162	0755
96-98	0846	131	0424		
99	0686	132	0755		
		133	0372		
101	0373	135	0424		
102-108	0574				
109	0846	141	0239		
111	0373	142	0374		
112	0574	143	0141		
113	0282	145	0373		
114-119	0574	146	0371		
		149	0574		



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PC-22-1531	A-1235-22
D	PC-22-1577	A-1244-22
E	22-1609	A-1247-22
F	22-1661	A-1303-22
G	22-1767	A-1314-22
H	22-1814	B-1314-22

SAVE

RAR

ROR 1

ROR 2

CLK (TO ALL 20 REGISTERS)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1K

30001-60001 TITLE SHEET 1-2

READ ONLY MEMORY (ROM) PCA

ENGINEER | APPROVED | DATE

NEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

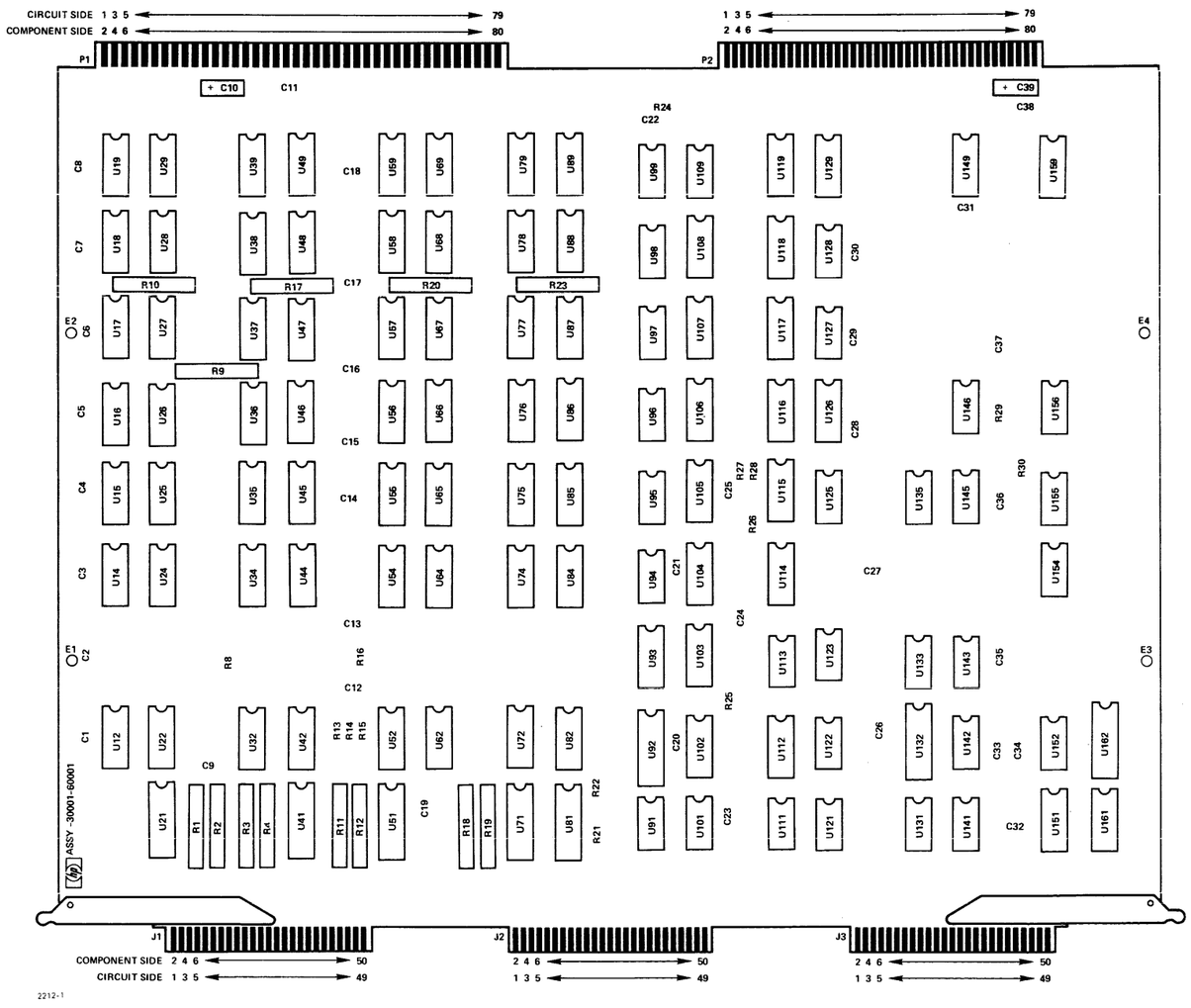
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	COM	1	COM	1	—
2	COM	2	COM	2	—
3	ROM01	3	RORT19	3	IROM16
4	ROM00	4	RORT18	4	IROM0
5	RAR11	5	RORT17	5	IROM17
6	RAR10	6	RORT16	6	IROM1
7	RAR09	7	RORT23	7	IROM18
8	RAR08	8	RORT22	8	IROM2
9	RAR07	9	RORT21	9	IROM19
10	RAR06	10	RORT20	10	IROM3
11	RAR05	11	V11	11	IROM20
12	RAR04	12	V10	12	IROM4
13	RAR03	13	V09	13	IROM21
14	RAR02	14	V08	14	IROM5
15	RAR01	15	RSSEL	15	IROM22
16	RAR00	16		16	IROM6
17	DISPLAY	17	RORT15	17	IROM23
18	+5V	18	ROM31	18	IROM7
19	+5V	19	+5V	19	IROM24
20	+5V	20	+5V	20	IROM8
21	ROM02	21	SF00	21	IROM25
22	+5V	22	SF04	22	IROM9
23	ROM06	23	SF02	23	IROM26
24	ROM03	24	SF01	24	IROM10
25	ROM05	25	RORT24	25	IROM27
26	ROM07	26	SF03	26	IROM11
27	ROM04	27	RORT25	27	IROM28
28	ROM08	28	RORT26	28	IROM12
29	COM	29	RORT27	29	IROM29
30		30		30	IROM13
31	ROM11	31		31	IROM30
32	ROM10	32	PANLSTOR	32	IROM14
33	ROM14	33	REPEAT	33	IROM31
34	ROM13	34		34	IROM15
35	ROM12	35		35	—
36	ROM09	36		36	ENABLROM
37	ROMFCN1	37		37	BRAR0
38	ROM15	38		38	BRAR1
39	COM	39	COM	39	BRAR2
40	COM	40	COM	40	BRAR3
41	ROM16	41	NOP2B	41	BRAR4
42	ROM24	42	DATA	42	BRAR5
43	ROM17	43	V07	43	BRAR6
44	ROM25	44	V06	44	BRAR7
45	ROM18	45	V05	45	BRAR8
46	ROM26	46	V04	46	BRAR9
47	ROM19	47	SWLDRAR	47	BRAR10
48	ROM27	48	STORAR	48	BRAR11
49	COM	49	JMPGATE	49	—
50	R12	50	RF03	50	—
51	ROM20	51	SPV		
52	R14	52	RF02		
53	ROM21	53	NXT=1		
54	R15	54	RF01		
55	ROM22	55	LUTGATE		
56	R13	56	RF00		
57	ROM23	57	NXT=2		
58	+5V	58			
59	+5V	59	+5V		
60	+5V	60	+5V		
61	ROM28	61	JLUI1		
62	+5V	62			
63	ROM30	63	NXT1		
64	ROM29	64			
65	R00	65	RARDIS		
66	R02	66	INHROMJ1		
67	R01	67			
68	R03	68	ENABLROM		
69	R04	69	PWR ONB		
70	R06	70	SKIP		
71	R05	71	RSB		
72	R07	72	JSB1		
73	R10	73	V03		
74	R08	74	V02		
75	R09	75	V01		
76	R11	76	V00		
77		77	BUSOP		
78	CLOCK	78	CPURST		
79	FREEZE	79	COM		
80	COM	80	COM		

NOTE: "XXX" INDICATES A CONNECTION WITH NO SIGNAL NAME.
"—" INDICATES NO CONNECTION TO PIN.

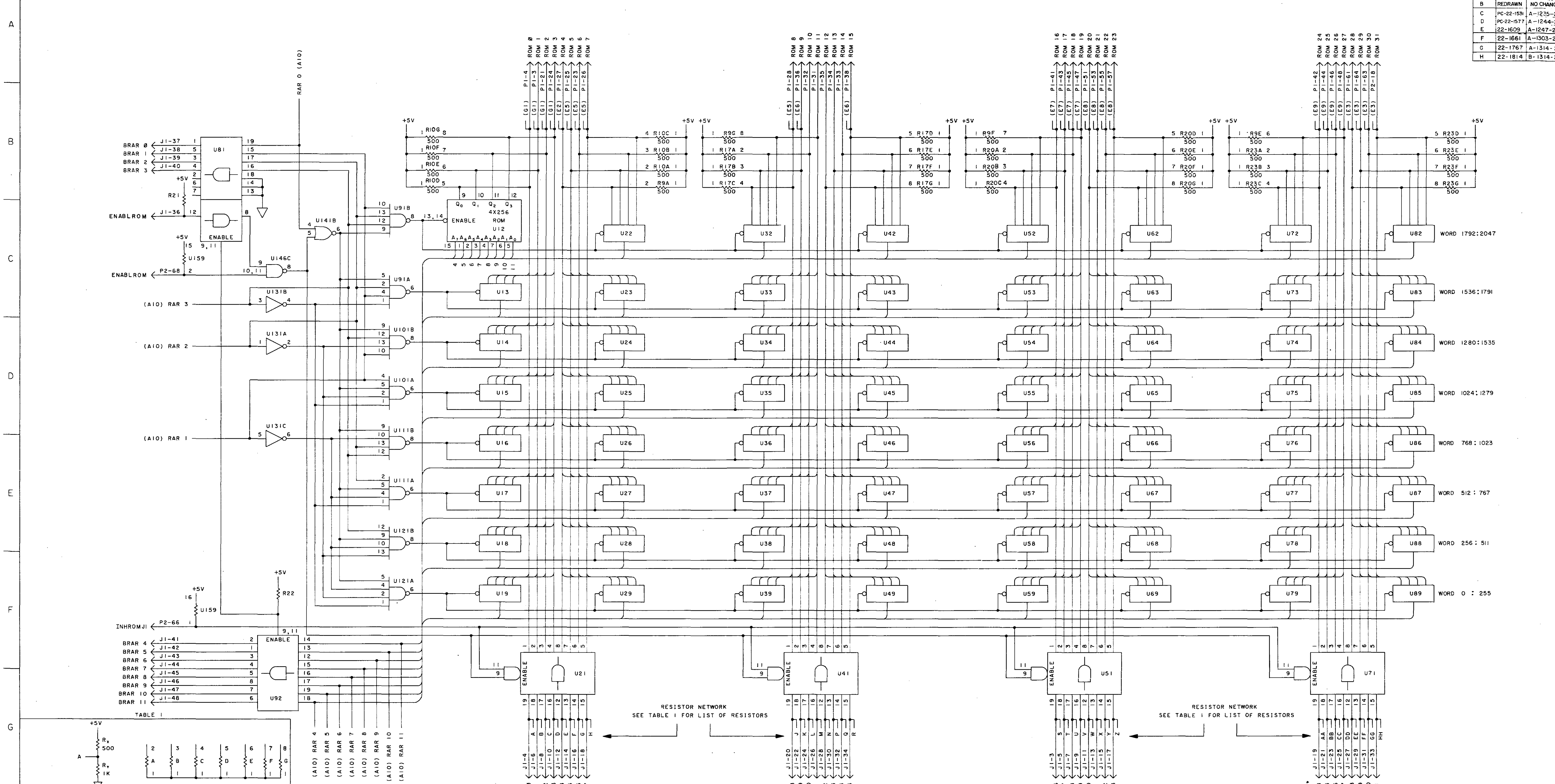
I.C. INDEX

U	1820-	U	1820-	U	1820-
21,41,51,71	0759	121	0373	151	0574
81	0755	122	0282	152	0282
		123	0374	154	0374
91	0373	125	0141	155	0424
92	0755	126	0574	156	0837
93	0574	127,128	0846		
94	0690	129	0574	161	0574
95	0140			162	0755
96-98	0846	131	0424		
99	0686	132	0755		
		133	0372		
101	0373	135	0424		
102-108	0574				
109	0846	141	0239		
111	0373	142	0374		
112	0574	143	0141		
113	0282	145	0373		
114-119	0574	146	0371		
		149	0574		



1548A-1 1548B-1

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PC-22-1531	A-1235-22
D	PC-22-1577	A-1244-22
E	22-1609	A-1247-22
F	22-1661	A-1303-22
G	22-1767	A-1314-22
H	22-1814	B-1314-22



LET.	R_x	R_y	LET.	R_x	R_y	LET.	R_x	R_y	LET.	R_x	R_y
A	R5	R6	L	R3F	R4F	W	R12D	R11D	GG	R19B	R18B
B	R1G	R2G	M	R3E	R4E	X	R12C	R11C	HH	R19A	R18A
C	R1F	R2F	N	R3A	R4A	Y	R12B	R11B			
D	R1E	R2E	P	R3B	R4B	Z	R12A	R11A			
E	R1A	R2A	Q	R3C	R4C	AA	R15	R16			
F	R1B	R2B	R	R3D	R4D	BB	R19G	R18G			
G	R1C	R2C	S	R14	R13	CC	R19F	R18F			
H	R1D	R2D	T	R12G	R11G	DD	R19E	R18E			
J	R8	R7	U	R12F	R11F	EE	R19D	R18D			
K	R3G	R4G	V	R12E	R11E	FF	R19C	R18C			

30001-60001 TITLE 2-2

READ ONLY MEMORY (ROM) PCA

ENGINEER APPROVED DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

ASSEMBLY # 30001-60001

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
C1-8,12-18,22-33,35-37	0160-2055	CAPACITOR,FXD,CER,0.01 UF,+80 -20%,100VDCW	28480	0160-2055	30
C9,19-21,34	0150-0121	CAPACITOR,FXD,CER, 0.1UF,+80-20%,50 VDCW	56289	5C50B1-CML	5
C10,39	0180-0229	CAPACITOR,FXD,ELECT,33 UF,10%,10 VDCW	28480	0180-0229	2
C11,38	0160-0127	CAPACITOR,FXD,NON-ELECT,1UF	56289	5C13C-CML	2
E1-4	0360-0294	TERMINAL,STUB,0.063 DIA.	88245	2018-2	4
R1,3,9-11,17,18,20,23	1810-0080	RESISTOR,7 X 500 OHMS,5%,500 PPM	56289	200C-1854-CRR	9
R2,4,12,19	1810-0030	RESISTOR,7 X 1K OHM,5%,500PPM	56289	200C1618-CRR	4
R5,8,13,16	0757-0416	RESISTOR,FXD,FLM,511 OHMS,1%,1/8W	28480	0757-0416	4
R6,7,14,15,21,22,24-27,30	0757-0280	RESISTOR,FXD,FLM,1K,1%,1/8W	28480	0757-0280	11
R28,29	0698-0082	RESISTOR,FXD,FLM,4640HMS,1%,0.125W	19701	MF4C,T-0	2
U12	1816-0073	IC, ROM, 4 X 256 BIT	28480	1816-0073	1
U14	1816-0277	IC, ROM, 4 X 256 BIT	28480	1816-0277	1
U15	1816-0075	IC, ROM, 4 X 256 BIT	28480	1816-0075	1
U16	1816-0240	IC, ROM, 4 X 256 BIT	28480	1816-0240	1
U17	1816-0077	IC, ROM, 4 X 256 BIT	28480	1816-0077	1
U18	1816-0078	IC, ROM, 4 X 256 BIT	28480	1816-0078	1
U19	1816-0079	IC, ROM, 4 X 256 BIT	28480	1816-0079	1
U21,41,51,71	1820-0759	IC,LP 8-BIT RECEIVER NON-INVERTING(TRI-STATE),TTL	28480	1820-0759	4
U22	1816-0080	IC, ROM, 4 X 256 BIT	28480	1816-0080	1
U24	1816-0278	IC, ROM, 4 X 256 BIT	28480	1816-0278	1
U25	1816-0082	IC, ROM, 4 X 256 BIT	28480	1816-0082	1
U26	1816-0241	IC, ROM, 4 X 256 BIT	28480	1816-0241	1
U27	1816-0084	IC, ROM, 4 X 256 BIT	28480	1816-0084	1
U28	1816-0085	IC, ROM, 4 X 256 BIT	28480	1816-0085	1
U29	1816-0086	IC, ROM, 4 X 256 BIT	28480	1816-0086	1
U32	1816-0087	IC, ROM, 4 X 256 BIT	28480	1816-0087	1
U34	1816-0279	IC, ROM, 4 X 256 BIT	28480	1816-0279	1
U35	1816-0089	IC, ROM, 4 X 256 BIT	28480	1816-0089	1
U36	1816-0242	IC, ROM, 4 X 256 BIT	28480	1816-0242	1
U37	1816-0091	IC, ROM, 4 X 256 BIT	28480	1816-0091	1
U38	1816-0092	IC, ROM, 4 X 256 BIT	28480	1816-0092	1
U39	1816-0093	IC, ROM, 4 X 256 BIT	28480	1816-0093	1
U42	1816-0094	IC, ROM, 4 X 256 BIT	28480	1816-0094	1
U44	1816-0280	IC, ROM, 4 X 256 BIT	28480	1816-0280	1
U45	1816-0096	IC, ROM, 4 X 256 BIT	28480	1816-0096	1
U46	1816-0243	IC, ROM, 4 X 256 BIT	28480	1816-0243	1
U47	1816-0228	IC, ROM, 4 X 256 BIT	28480	1816-0228	1
U48	1816-0099	IC, ROM, 4 X 256 BIT	28480	1816-0099	1
U49	1816-0100	IC, ROM, 4 X 256 BIT	28480	1816-0100	1
U52	1816-0101	IC, ROM, 4 X 256 BIT	28480	1816-0101	1

ASSEMBLY # 30001-60001 (CONTINUED)

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
U54	1816-0281	IC, ROM, 4 X 256 BIT	28480	1816-0281	1
U55	1816-0103	IC, ROM, 4 X 256 BIT	28480	1816-0103	1
U56	1816-0244	IC, ROM, 4 X 256 BIT	28480	1816-0244	1
U57	1816-0105	IC, ROM, 4 X 256 BIT	28480	1816-0105	1
U58	1816-0245	IC, ROM, 4 X 256 BIT	28480	1816-0245	1
U59	1816-0107	IC, ROM, 4 X 256 BIT	28480	1816-0107	1
U62	1816-0108	IC, ROM, 4 X 256 BIT	28480	1816-0108	1
U64	1816-0282	IC, ROM, 4 X 256 BIT	28480	1816-0282	1
U65	1816-0110	IC, ROM, 4 X 256 BIT	28480	1816-0110	1
U66	1816-0246	IC, ROM, 4 X 256 BIT	28480	1816-0246	1
U67	1816-0227	IC, ROM, 4 X 256 BIT	28480	1816-0227	1
U68	1816-0113	IC, ROM, 4 X 256 BIT	28480	1816-0113	1
U69	1816-0114	IC, ROM, 4 X 256 BIT	28480	1816-0114	1
U72	1816-0115	IC, ROM, 4 X 256 BIT	28480	1816-0115	1
U74	1816-0283	IC, ROM, 4 X 256 BIT	28480	1816-0283	1
U75	1816-0117	IC, ROM, 4 X 256 BIT	28480	1816-0117	1
U76	1816-0247	IC, ROM, 4 X 256 BIT	28480	1816-0247	1
U77	1816-0119	IC, ROM, 4 X 256 BIT	28480	1816-0119	1
U78	1816-0120	IC, ROM, 4 X 256 BIT	28480	1816-0120	1
U79	1816-0121	IC, ROM, 4 X 256 BIT	28480	1816-0121	1
U81,92,132,162	1820-0755	IC,8-BIT DRIVER NON-INVERTING(TRI-STATE),TTL	28480	1820-0755	4
U82	1816-0122	IC, ROM, 4 X 256 BIT	28480	1816-0122	1
U84	1816-0284	IC, ROM, 4 X 256 BIT	28480	1816-0284	1
U85	1816-0124	IC, ROM, 4 X 256 BIT	28480	1816-0124	1
U86	1816-0248	IC, ROM, 4 X 256 BIT	28480	1816-0248	1
U87	1816-0126	IC, ROM, 4 X 256 BIT	28480	1816-0126	1
U88	1816-0127	IC, ROM, 4 X 256 BIT	28480	1816-0127	1
U89	1816-0128	IC, ROM, 4 X 256 BIT	28480	1816-0128	1
U91,101,111,121,145	1820-0373	IC,HS DUAL 4-INPUT NAND GATE,TTL	01295	SN74H20N	5
U93,102,114-118,126, 129,149,151	1820-1033	IC,QUAD D FLIP-FLOP,TRI STATE OUTPUT,TTL	18324	N8T110B	11
U94	1820-0690	IC,SHS DUAL 4-INPUT NAND BUFFER,TTL	01295	SN74S40N	1
U95	1820-0140	IC,DUAL 4-INPUT AND BUFFER,TTL	04713	SC7513PK	1
U96-98,109,127,128	1820-0846	IC,QUAD BUFFER (TRI-STATE),TTL	27014	DM8094N	6
U99	1820-0686	IC,TRIPLE 3-INPUT AND GATE,SCHOTTKY TT	01295	SN74S11N	1
U103-108,112,119,161	1820-0574	IC,QUAD D FLIP-FLOP W/PAR CLK AND CLEAR,TTL	27014	DM8551N	9
U113,122,152	1820-0282	IC,QUAD 2-INPUT EXCLUSIVE OR GATE,TTL	01295	SN13603	1
U123,142,154	1820-0374	IC,HS DUAL 4-INPUT AND GATE,TTL	01295	SN74H21N	3
U125,143	1820-0141	IC,QUAD 2-INPUT AND GATE,TTL	04713	MC3001P	2
U131,135,155	1820-0424	IC,HS HEX INVERTER,TTL	01295	SN74H04N	3
U133	1820-0372	IC,TRIPLE 3-INPUT AND GATE,TTL	01295	SN74H11N	1
U141	1820-0239	IC,QUAD 2-INPUT NOR GATE,TTL	04713	MC3002P	1
U146	1820-0371	IC,HS TRIPLE 3-INPUT NAND GATE,TTL	01295	SN74H10N	1
U156	1820-0837	IC,DUAL 4-INPUT NOR GATE,TTL	18324	N8815A	1
U159	1810-0037	RESISTOR,ARRAY,8 X 1K OHM,2% EA,1-3/4W	11236	760 SER/16 PIN	1

CPU/IOP DETAILED DIAGRAM SET

DD-201

SKIP AND SPECIAL FIELD (SSF) PCA

30001-60002

SERIES 1247 = Rev A

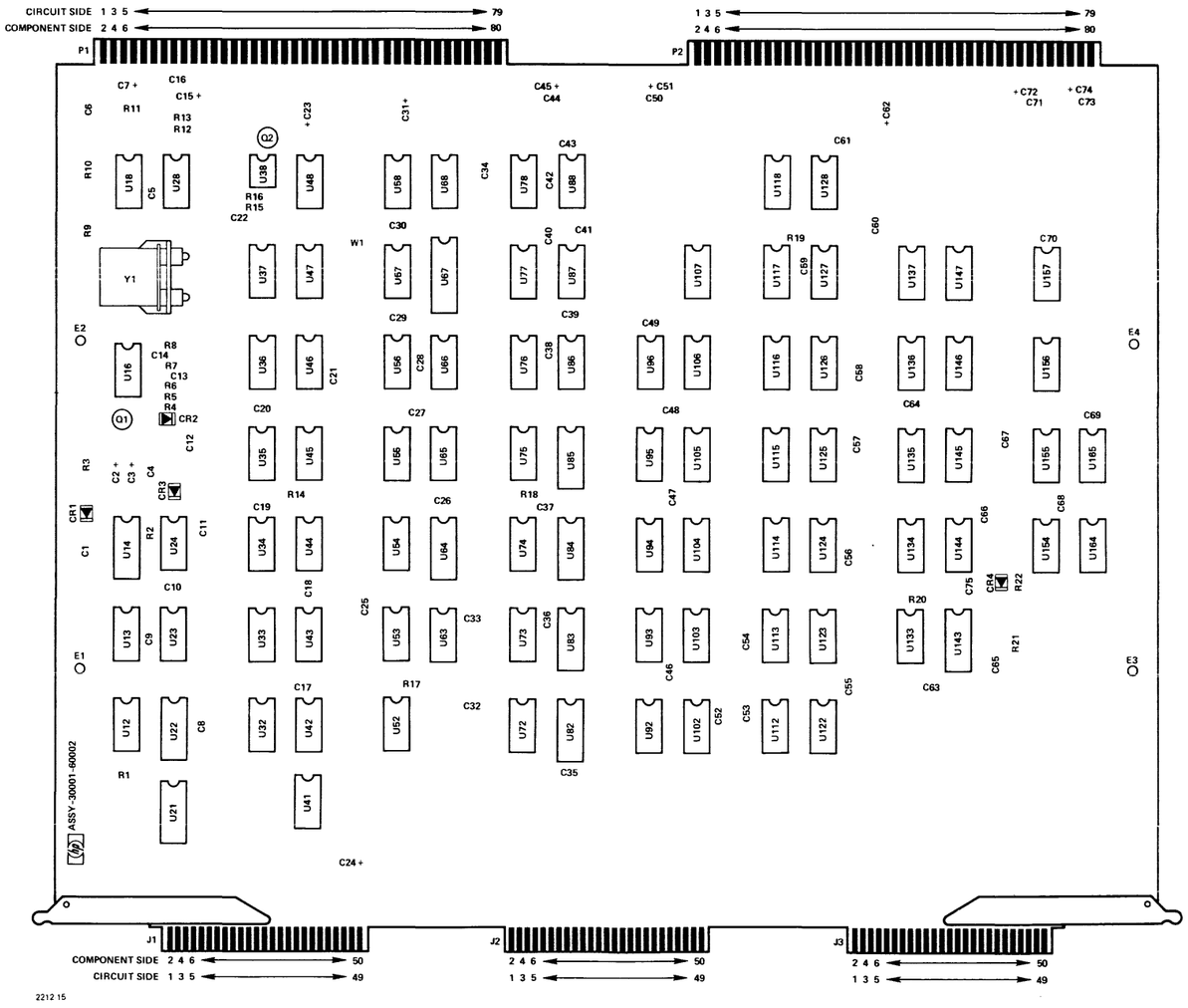
1330 = Rev B

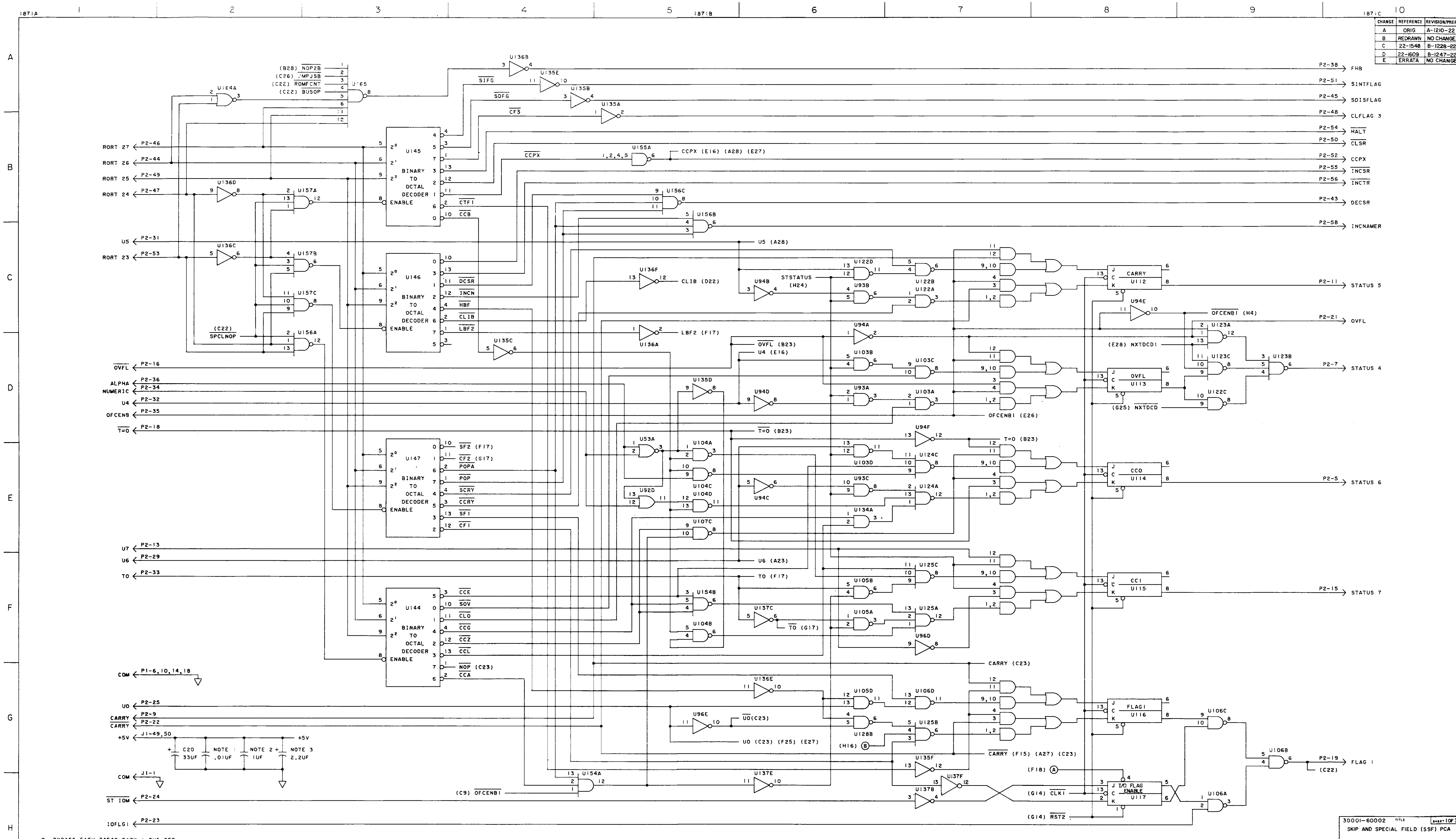
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	4XCLK	1		1	COM
2	4XCLKR	2	COM	2	XXX
3	EXTCLK	3	FLAG2	3	—
4	TEST1	4	NOP2B	4	—
5	MCUCLK1	5	STATUS06	5	—
6	MCUCL1R	6	SR02	6	—
7	NXTFINH	7	STATUS04	7	—
8	TEST2	8	U08	8	—
9	MCUCLK2	9	CARRY	9	—
10	MCUCL2R	10	JMPJSB	10	—
11	CLOCKS	11	STATUS05	11	—
12	IORESET	12	BNDV	12	—
13	MCUCLK3	13	U07	13	—
14	MCUCL3R	14	RORT16	14	—
15	INTCLKM	15	STATUS07	15	—
16	PFWARNB	16	OVFL	16	—
17	MCUCLK4	17	JMPFRZ	17	—
18	MCUCL4R	18	T=0	18	—
19	PWR ONB	19	FLAG1	19	—
20	+5V	20	+5V	20	—
21	IORSTSW	21	OVFL	21	—
22	JLUI2	22	CARRY	22	—
23	CPURSTS	23	IOFLG1	23	—
24	NXT2	24	STIOM	24	—
25	INCP	25	U00	15	—
26	TINT	26	DVSB	26	—
27	CLOCKENB	27	U15	27	—
28	RSB	28		28	—
29	PWRFAIL	29	U06	29	—
30	MCUCLKS	30		30	—
31	STSTATUS	31	U05	31	—
32		32	U04	32	—
33	NXTDCD	33	T00	33	—
34	INDIRECT	34	NUMERIC	34	—
35	NXTGATE	35	OFCENB	35	—
36	PWR ON	36	ALPHA	36	—
37	NOP2	37		37	—
38	FRUNCLK	38	FHB	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	DISPLAY	41	TMRFRZI	41	—
42	SKIP	42		42	—
43	STATUS02	43	DECSR	43	—
44	U01	44	RORT26	44	—
45	STATUS01	45	SDISFLAG	45	—
46	U02	46	RORT27	46	—
47	U03	47	RORT24	47	—
48	REPEAT	48	CLFLAG03	48	—
49	BNDT	49	RORT25	49	+5V
50	RPTFCN	50	CLSR	50	+5V
51	NOP	51	SINTFLAG		
52	STKBNOP	52	CCPX		
53	NXT=1	53	RORT23		
54	STATUS03	54	HALT		
55	NXT=2	55	INCRS		
56	STATUS00	56	INCTR		
57	NEXT	57	RREG00		
58	SR00	58	INCNAMER		
59	INTRP	59			
60	+5V	60	+5V		
61	FLAG3	61			
62	RORT15	62			
63	CNTRMAX	63	JBNDV		
64	SKIPNOP	64			
65	NOP1	65			
66	NOP2	66			
67	UBNT	67			
68	SAME	68			
69	JMPGATE	69	CPUTIMER		
70	RORT19	70			
71	SR01	71			
72	RORT18	72			
73		73			
74	RORT17	74			
75	LUTGATE	75	ENTIMER		
76	BUSOP	76			
77	ROMFCNT	77	RUNFF		
78	CLOCK	78	CPURST		
79	FREEZE	79	NIRTOCIR		
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12,13	0512	41	0141	64	0724	92	0205	133	0696
14	0515	42	0205	65	0696	93	0681	134	0141
16	0142	43	0688	66	0685	94	0683	135–137	0424
18	0697	44	0837	67	0760	95	0374		
21	0370	45	0512	68	0697	96	0683	143	0515
22	1035	46	0686					144–147	0608
23	0424	47	0141	72,73	0371	102	0691		
24	0695	48	0370	74	0424	103–107	0370	154	0372
28	0697			75	0141	112–116	0739	155	0376
		52	0372	76	0686	117	0696	156,157	0371
32	0141	53	0239	77	0685	118	0373		
33	0739	54	0370	78	0681			164	0239
34	0685	55	0696			122	0370	165	0375
35	0375	56,57	0695	82–85	0615	123–126	0371		
36	0695	58	0376	86	0690	127	0373		
37	0681			87	0697	128	0681		
38	0535	63	0424	88	0690				





CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1548	B-1228-22
D	22-1609	B-1247-22
E	ERRATA	NO CHANGE

NOTES: UNLESS OTHERWISE SPECIFIED
1. BYPASS EACH 74S__ PACK .01UF CER
2. BYPASS EACH 74S40 PACK 1.0UF CER

30001-60002 TITLE SKIP AND SPECIAL FIELD (SSF) PCA SHEET 1 OF 3

ENGINEER | APPROVED | DATE

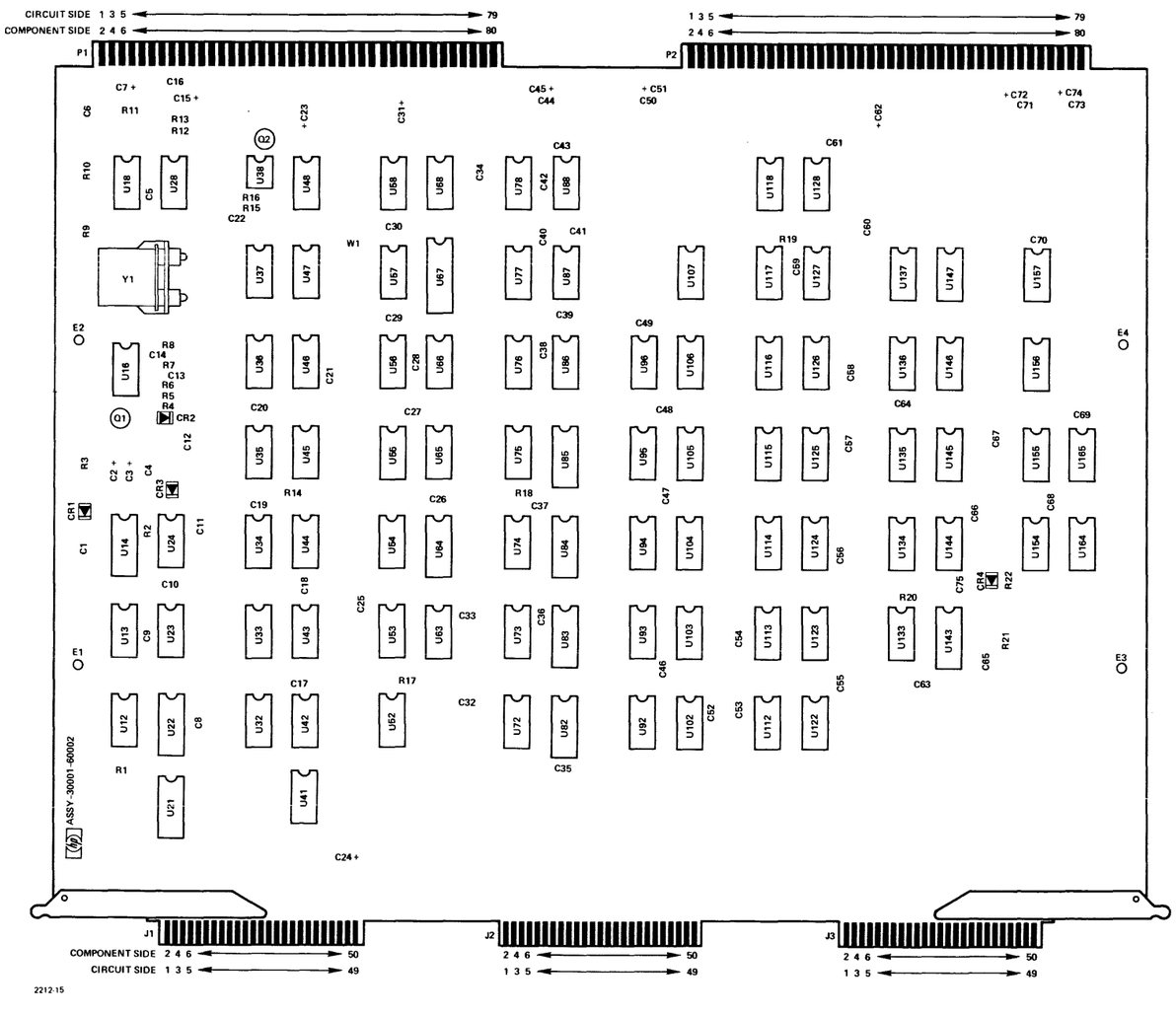
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

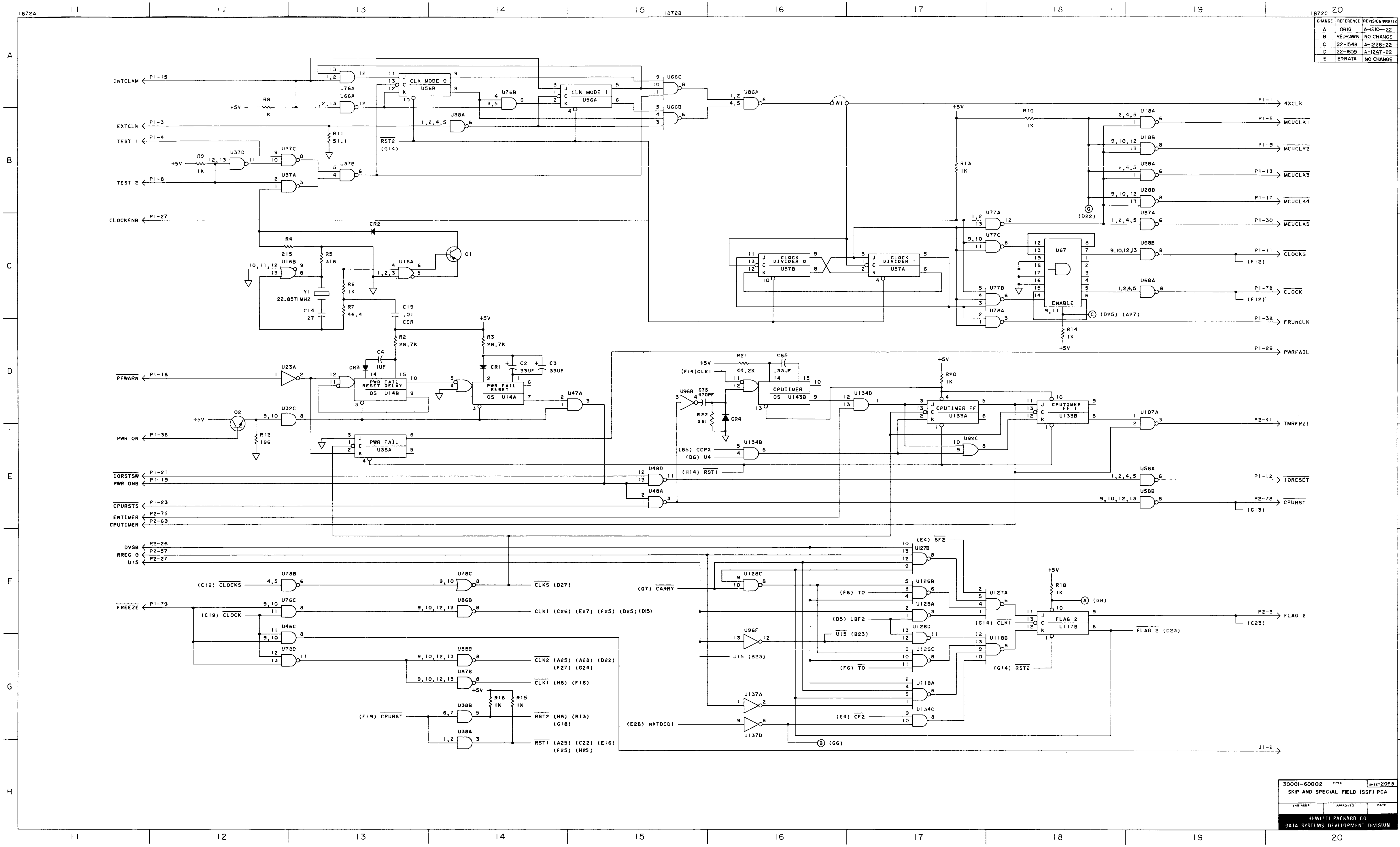
P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	4XCLK	1		1	COM
2	4XCLKR	2	COM	2	XXX
3	EXTCLK	3	FLAG2	3	—
4	TEST1	4	NOP2B	4	—
5	MCUCLK1	5	STATUS06	5	—
6	MCUCL1R	6	SR02	6	—
7	NXTFINH	7	STATUS04	7	—
8	TEST2	8	U08	8	—
9	MCUCLK2	9	CARRY	9	—
10	MCUCL2R	10	JMPJSB	10	—
11	CLOCKS	11	STATUS05	11	—
12	IORESET	12	BNDV	12	—
13	MCUCLK3	13	U07	13	—
14	MCUCL3R	14	RORT16	14	—
15	INTCLKM	15	STATUS07	15	—
16	PFWARNB	16	OVFL	16	—
17	MCUCLK4	17	JMPFRZ	17	—
18	MCUCL4R	18	T=0	18	—
19	PWR ONB	19	FLAG1	19	—
20	+5V	20	+5V	20	—
21	IORSTSW	21	OVFL	21	—
22	JLUI2	22	CARRY	22	—
23	CPURSTS	23	IOFLG1	23	—
24	NXT2	24	STIOM	24	—
25	INCP	25	U00	15	—
26	TINT	26	DVSB	26	—
27	CLOCKENB	27	U15	27	—
28	RSB	28		28	—
29	PWRFAIL	29	U06	29	—
30	MCUCLKS	30		30	—
31	STSTATUS	31	U05	31	—
32		32	U04	32	—
33	NXTDCD	33	T00	33	—
34	!NDIRECT	34	NUMERIC	34	—
35	NXTGATE	35	OFCENB	35	—
36	PWR ON	36	ALPHA	36	—
37	NOP2	37		37	—
38	FRUNCLK	38	FHB	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	DISPLAY	41	TMRFRZI	41	—
42	SKIP	42		42	—
43	STATUS02	43	DECSR	43	—
44	U01	44	RORT26	44	—
45	STATUS01	45	SDISFLAG	45	—
46	U02	46	RORT27	46	—
47	U03	47	RORT24	47	—
48	REPEAT	48	CLFLAG03	48	—
49	BNDT	49	RORT25	49	+5V
50	RPTFCN	50	CLSR	50	+5V
51	NOP	51	SINTFLAG		
52	STKBNOP	52	CCPX		
53	NXT=1	53	RORT23		
54	STATUS03	54	HALT		
55	NXT=2	55	INCRS		
56	STATUS00	56	INCTR		
57	NEXT	57	RREG00		
58	SR00	58	INCNAMER		
59	INTRP	59			
60	+5V	60	+5V		
61	FLAG3	61			
62	RORT15	62			
63	CNTRMAX	63	JBNDV		
64	SKIPNOP	64			
65	NOP1	65			
66	NOP2	66			
67	UBNT	67			
68	SAME	68			
69	JMPGATE	69	CPUTIMER		
70	RORT19	70			
71	SR01	71			
72	RORT18	72			
73		73			
74	RORT17	74			
75	LUTGATE	75	ENTIMER		
76	BUSOP	76			
77	ROMFCNT	77	RUNFF		
78	CLOCK	78	CPURST		
79	FREEZE	79	NIRTOCIR		
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12,13	0512	41	0141	64	0724	92	0205	133	0696
14	0515	42	0205	65	0696	93	0681	134	0141
16	0142	43	0688	66	0685	94	0683	135–137	0424
18	0697	44	0837	67	0760	95	0374		
21	0370	45	0512	68	0697	96	0683	143	0515
22	1035	46	0686					144–147	0608
23	0424	47	0141	72,73	0371	102	0691		
24	0695	48	0370	74	0424	103–107	0370	154	0372
28	0697			75	0141	112–116	0739	155	0376
		52	0372	76	0686	117	0696	156,157	0371
32	0141	53	0239	77	0685	118	0373		
33	0739	54	0370	78	0681			164	0239
34	0685	55	0696			122	0370	165	0375
35	0375	56,57	0695	82–85	0615	123–126	0371		
36	0695	58	0376	86	0690	127	0373		
37	0681			87	0697	128	0681		
38	0535	63	0424	88	0690				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1548	A-1228-22
D	22-1609	A-1247-22
E	ERRATA	NO CHANGE



30001-60002	TITLE SKIP AND SPECIAL FIELD (SSF) PCA	SHEET 2 OF 3
ENGINEER	APPROVED	DATE

HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

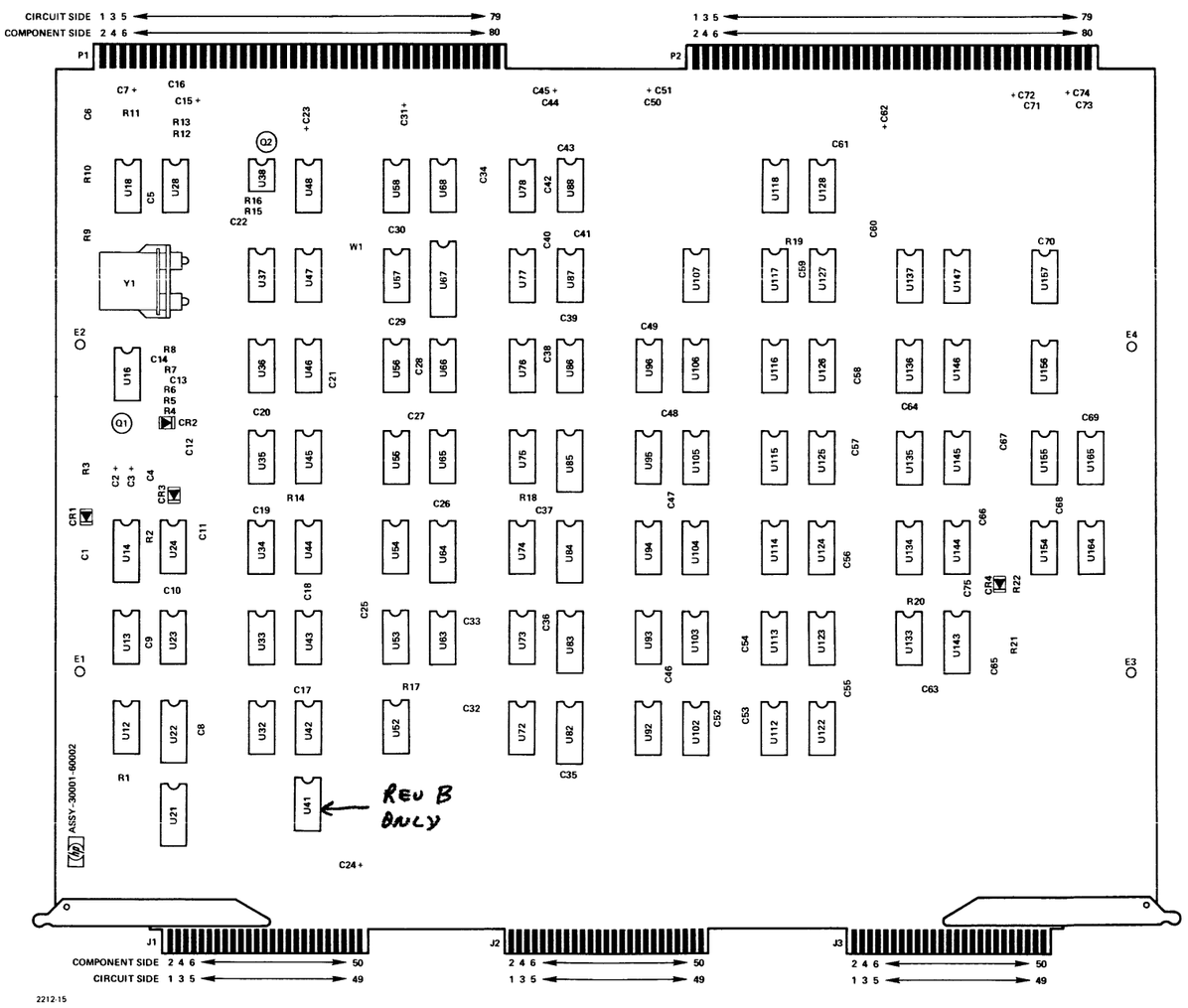
SIGNAL INDEX

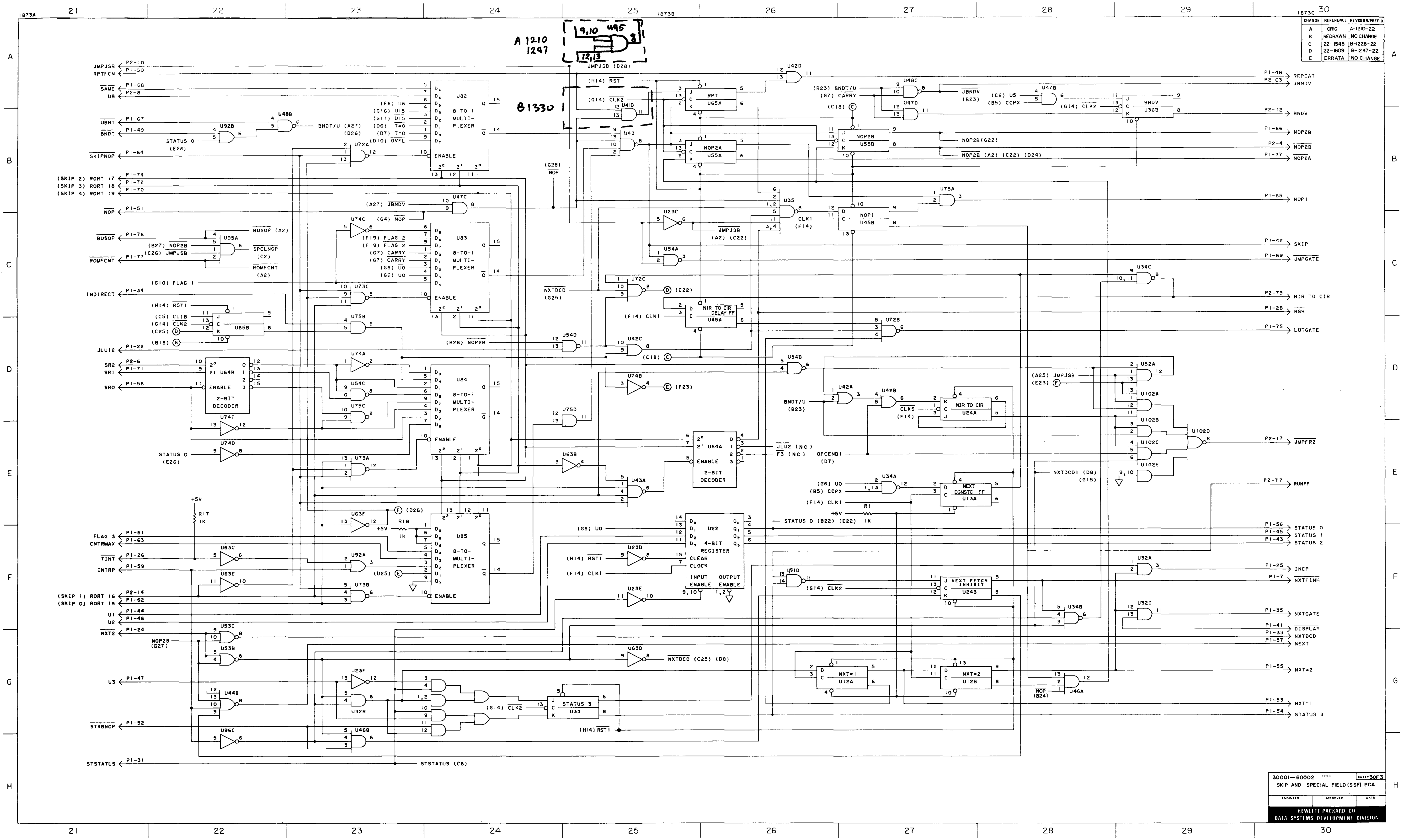
P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	4XCLK	1		1	COM
2	4XCLKR	2	COM	2	XXX
3	EXTCLK	3	FLAG2	3	—
4	TEST1	4	NOP2B	4	—
5	MCUCLK1	5	STATUS06	5	—
6	MCUCL1R	6	SR02	6	—
7	NXTFINH	7	STATUS04	7	—
8	TEST2	8	U08	8	—
9	MCUCLK2	9	CARRY	9	—
10	MCUCL2R	10	JMPJSB	10	—
11	CLOCKS	11	STATUS05	11	—
12	IORESET	12	BNDV	12	—
13	MCUCLK3	13	U07	13	—
14	MCUCL3R	14	RORT16	14	—
15	INTCLKM	15	STATUS07	15	—
16	PFWARNB	16	OVFL	16	—
17	MCUCLK4	17	JMPFRZ	17	—
18	MCUCL4R	18	T=0	18	—
19	PWR ONB	19	FLAG1	19	—
20	+5V	20	+5V	20	—
21	IORSTSW	21	OVFL	21	—
22	JLUI2	22	CARRY	22	—
23	CPURSTS	23	IOFLG1	23	—
24	NXT2	24	STIOM	24	—
25	INCP	25	U00	15	—
26	TINT	26	DVSB	26	—
27	CLOCKENB	27	U15	27	—
28	RSB	28		28	—
29	PWRFAIL	29	U06	29	—
30	MCUCLKS	30		30	—
31	STSTATUS	31	U05	31	—
32		32	U04	32	—
33	NXTDCD	33	T00	33	—
34	!NDIRECT	34	NUMERIC	34	—
35	NXTGATE	35	OFCENB	35	—
36	PWR ON	36	ALPHA	36	—
37	NOP2	37		37	—
38	FRUNCLK	38	FHB	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	DISPLAY	41	TMRFRZI	41	—
42	SKIP	42		42	—
43	STATUS02	43	DECSR	43	—
44	U01	44	RORT26	44	—
45	STATUS01	45	SDISFLAG	45	—
46	U02	46	RORT27	46	—
47	U03	47	RORT24	47	—
48	REPEAT	48	CLFLAG03	48	—
49	BNDT	49	RORT25	49	+5V
50	RPTFCN	50	CLSR	50	+5V
51	NOP	51	SINTFLAG		
52	STKBNOP	52	CCPX		
53	NXT=1	53	RORT23		
54	STATUS03	54	HALT		
55	NXT=2	55	INCRS		
56	STATUS00	56	INCTR		
57	NEXT	57	RREG00		
58	SR00	58	INCNAMER		
59	INTRP	59			
60	+5V	60	+5V		
61	FLAG3	61			
62	RORT15	62			
63	CNTRMAX	63	JBNDV		
64	SKIPNOP	64			
65	NOP1	65			
66	NOP2	66			
67	UBNT	67			
68	SAME	68			
69	JMPGATE	69	CPUTIMER		
70	RORT19	70			
71	SR01	71			
72	RORT18	72			
73		73			
74	RORT17	74			
75	LUTGATE	75	ENTIMER		
76	BUSOP	76			
77	ROMFCNT	77	RUNFF		
78	CLOCK	78	CPURST		
79	FREEZE	79	NIRTOCIR		
80	COM	80	COM		

I.C. INDEX

REV A
1820-1033

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12,13	0512	41	0141	64	0724	92	0205	133	0696
14	0515	42	0205	65	0696	93	0681	134	0141
16	0142	43	0688	66	0685	94	0683	135–137	0424
18	0697	44	0837	67	0760	95	0374		
21	0370	45	0512	68	0697	96	0683	143	0515
22	1035	46	0686					144–147	0608
23	0424	47	0141	72,73	0371	102	0691		
24	0695	48	0370	74	0424	103–107	0370	154	0372
28	0697			75	0141	112–116	0739	155	0376
		52	0372	76	0686	117	0696	156,157	0371
32	0141	53	0239	77	0685	118	0373		
33	0739	54	0370	78	0681			164	0239
34	0685	55	0696			122	0370	165	0375
35	0375	56,57	0695	82–85	0615	123–126	0371		
36	0695	58	0376	86	0690	127	0373		
37	0681			87	0697	128	0681		
38	0535	63	0424	88	0690				





CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG | A-1210-22
B | REDRAWN | NO CHANGE
C | 22-1548 | B-1228-22
D | 22-1609 | B-1247-22
E | ERRATA | NO CHANGE
A 1210
1297
B1330
30001-60002
SHEET 3 OF 3
SKIP AND SPECIAL FIELD (SSF) PCA
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-202

ARITH AND LOGIC UNIT (ALU) PCA

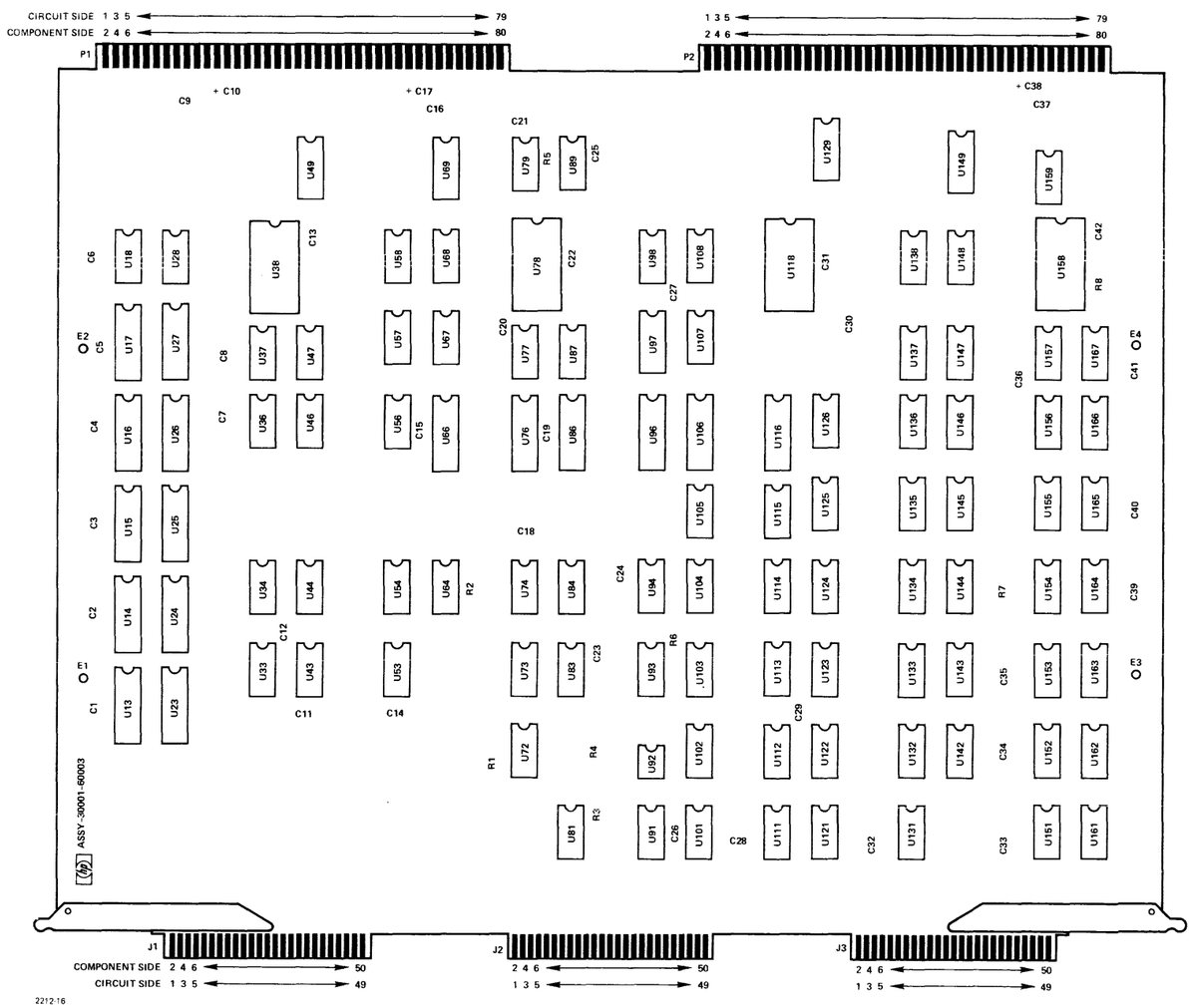
30001-60003

SERIES 1233

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	S00	1	NOP1
2	COM	2	COM
3	JLUI2	3	S08
4	S01	4	S09
5	S02	5	S10
6	S03	6	S11
7	U02	7	R11
8	U00	8	R10
9	R02	9	R09
10	R03	10	R08
11	R01	11	UBNT
12	R00	12	RPTFCN
13	FHB	13	U08
14	U01	14	U09
15	FLAG1	15	U10
16	T00	16	U11
17	U03	17	PANLSTOR
18	U04	18	
19	U05	19	U12
20	+5V	20	+5V
21	U06	21	U13
22	U07	22	U14
23	NXT1	23	U15
24	JLUI1	24	RORT12
25	T15	25	RORT13
26	ALUS0	26	SP3IN
27	ALUS3	27	RFSAME
28	ALUS2	28	SFSAME
29	ALUS1	29	CIR07
30	NXT2	30	
31	ROM10	31	CIR08
32	ROM11	32	ROMFCN1
33	ROM12	33	PANLREAD
34	ROM13	34	RSSEL
35	ROM14	35	S15
36		36	S14
37	CARRY	37	S13
38	CARRY	38	S12
39	COM	39	COM
40	COM	40	COM
41	RREG00	41	REPEAT
42		42	
43	PRTYMODE	43	RORT11
44	OVFL	44	RORT10
45	RDCPX2	45	NOP2
46	IOTIMER	46	RORT14
47		47	R12
48	INTFLAG	48	R13
49	RORT21	49	R14
50	RORT22	50	
51	S07	51	R15
52	S06	52	NOP2
53	S05	53	SHFTCLK
54	S04	54	RFINH
55	RDJMPR	55	JSB1
56		56	JMPJSB1
57		57	DVSB
58		58	SP3SHIFT
59	RORT20	59	
60	+5V	60	+5V
61	R04	61	SLOAD
62	R05	62	BNDT
63	R06	63	FUBUS
64	R07	64	SP315
65	SWLDRAR	65	SP1IN
66	ROMFCNT	66	DISPLAY
67	DISPFLAG	67	ALUFC
68	CCPX	68	REPN
69	SINTFLAG	69	NOP2B
70	SDISFLAG	70	
71	NXT=2	71	JMPJSB
72		72	DSPFLAG
73	SKIPNOP	73	SSREG
74	FLAG2	74	
75	ALUMODE	75	SP1SHIFT
76	T=0	76	SP100
77	SAME	77	SRREG
78	CLOCK	78	CPURST
79	FREEZE	79	OFCENB
80	COM	80	COM

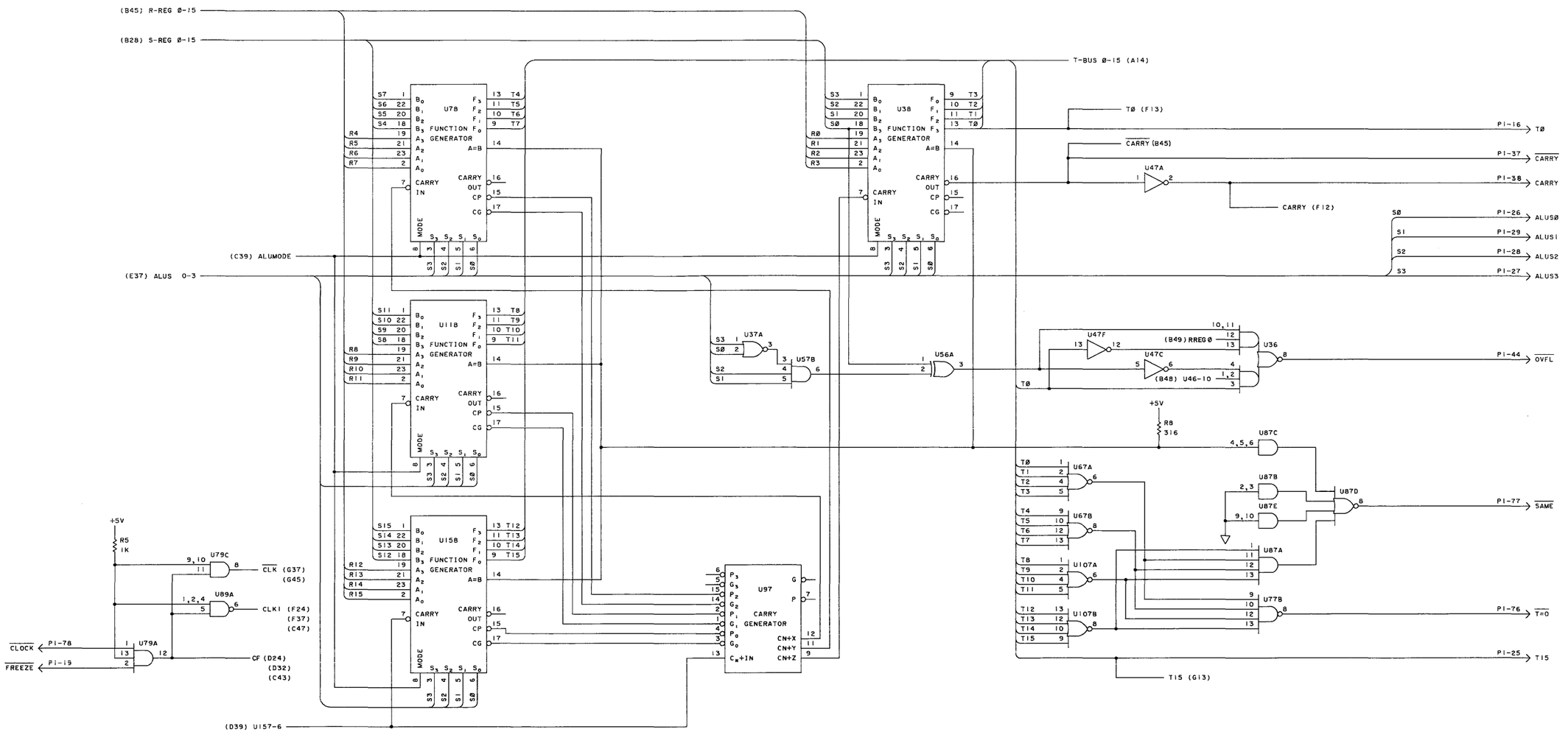
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
13-17	0755	64	0512	93	0375	121	0205	148	0367
18	0367	66	0755	94	0685	122	0141	149	0262
		67	0837	96	0755	123	0371		
23-27	0755	68	0367	97	0611	124,125	0512	151	0239
28	0367	69	0262	98	0367	126	0373	152	0424
						129	0262	153	0608
33	0371	72	0512	101	0141			154	0370
34	0373	73	0372	102	0370	131	0370	155	0384
36	0382	74	0686	103	0373	132	0205	156	0371
37	0239	76	0755	104	0837	133	0608	157	0372
38	0999	77	0688	105	0512	134,135	0512	158	0606
		78	0606	106	0722	136,137	0373	159	0375
43	0683	79	0686	107	0837	138	0367		
44	0370			108	0367			161	0374
46	0424	81	0846			142	0685	162	0379
47	0683	83	0374	111	0379	143	0608	163	0608
49	0262	84	0239	112	0688	144	0837	164	0141
		86	0755	113	0371	145	0239	165	0379
53	0695	87	0691	114,115	0512	146	0373	166	0376
54	0608	89	0690	116	0755	147	0371	167	0370
56	0282			118	0606				
57	0686	91	0696						
58	0367	92	0535						



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-D	A-1233-22	ALL
D	22-1715	B-1233-22	ALL

FUNCTION GENERATOR

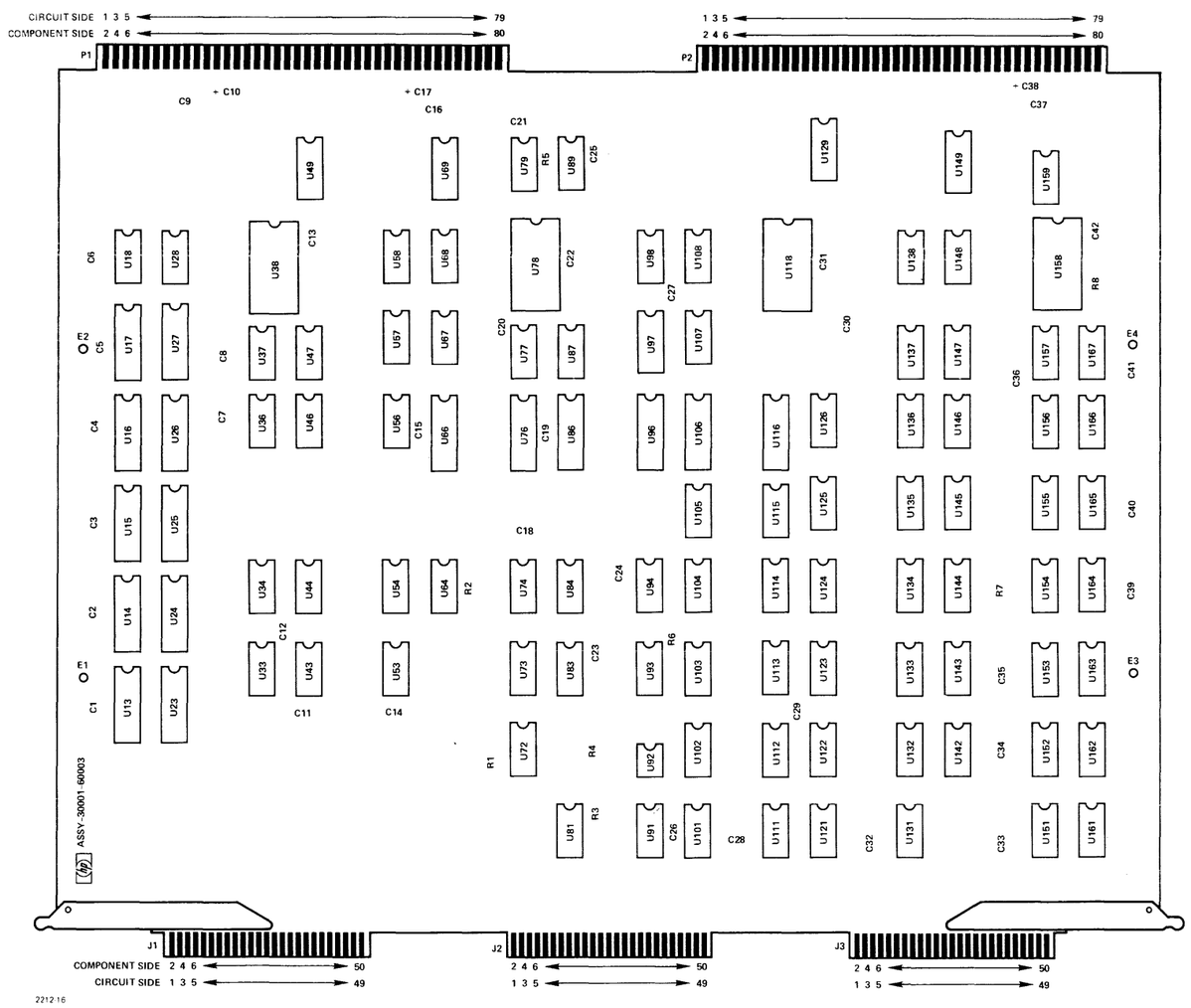


30001-60003	TITLE		SHEET 1 OF 5
ARITHMETIC & LOGIC UNIT (ALU) PCA			
ENGINEER	APPROVED	DATE	
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION			

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	S00	1	NOP1
2	COM	2	COM
3	JLUI2	3	S08
4	S01	4	S09
5	S02	5	S10
6	S03	6	S11
7	U02	7	R11
8	U00	8	R10
9	R02	9	R09
10	R03	10	R08
11	R01	11	UBNT
12	R00	12	RPTFCN
13	FHB	13	U08
14	U01	14	U09
15	FLAG1	15	U10
16	T00	16	U11
17	U03	17	PANLSTOR
18	U04	18	
19	U05	19	U12
20	+5V	20	+5V
21	U06	21	U13
22	U07	22	U14
23	NXT1	23	U15
24	JLUI1	24	RORT12
25	T15	25	RORT13
26	ALUS0	26	SP3IN
27	ALUS3	27	RFSAME
28	ALUS2	28	SFSAME
29	ALUS1	29	CIR07
30	NXT2	30	
31	ROM10	31	CIR08
32	ROM11	32	ROMFCN1
33	ROM12	33	PANLREAD
34	ROM13	34	RSSEL
35	ROM14	35	S15
36		36	S14
37	CARRY	37	S13
38	CARRY	38	S12
39	COM	39	COM
40	COM	40	COM
41	RREG00	41	REPEAT
42		42	
43	PRTYMODE	43	RORT11
44	OVFL	44	RORT10
45	RDCPX2	45	NOP2
46	IOTIMER	46	RORT14
47		47	R12
48	INTFLAG	48	R13
49	RORT21	49	R14
50	RORT22	50	
51	S07	51	R15
52	S06	52	NOP2
53	S05	53	SHFTCLK
54	S04	54	RFINH
55	RDJMPR	55	JSB1
56		56	JMPJSB1
57		57	DVSB
58		58	SP3SHIFT
59	RORT20	59	
60	+5V	60	+5V
61	R04	61	SLOAD
62	R05	62	BNDT
63	R06	63	FUBUS
64	R07	64	SP315
65	SWLDRAR	65	SP1IN
66	ROMFCNT	66	DISPLAY
67	DISPFLAG	67	ALUFC
68	CCPX	68	REPN
69	SINTFLAG	69	NOP2B
70	SDISFLAG	70	
71	NXT=2	71	JMPJSB
72		72	DSPFLAG
73	SKIPNOP	73	SSREG
74	FLAG2	74	
75	ALUMODE	75	SP1SHIFT
76	T=0	76	SP100
77	SAME	77	SRREG
78	CLOCK	78	CPURST
79	FREEZE	79	OFCENB
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
13-17	0755	64	0512	93	0375	121	0205	148	0367
18	0367	66	0755	94	0685	122	0141	149	0262
		67	0837	96	0755	123	0371		
23-27	0755	68	0367	97	0611	124,125	0512	151	0239
28	0367	69	0262	98	0367	126	0373	152	0424
						129	0262	153	0608
33	0371	72	0512	101	0141			154	0370
34	0373	73	0372	102	0370	131	0370	155	0384
36	0382	74	0686	103	0373	132	0205	156	0371
37	0239	76	0755	104	0837	133	0608	157	0372
38	0999	77	0688	105	0512	134,135	0512	158	0606
		78	0606	106	0722	136,137	0373	159	0375
43	0683	79	0686	107	0837	138	0367		
44	0370			108	0367			161	0374
46	0424	81	0846			142	0685	162	0379
47	0683	83	0374	111	0379	143	0608	163	0608
49	0262	84	0239	112	0688	144	0837	164	0141
		86	0755	113	0371	145	0239	165	0379
53	0695	87	0691	114,115	0512	146	0373	166	0376
54	0608	89	0690	116	0755	147	0371	167	0370
56	0282			118	0606				
57	0686	91	0696						
58	0367	92	0535						



2212 16

1469A-1 | 1469B-1 | 1469C-1

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

SHIFTER

FLAG1 ← P1-15
(D38) ROMFCNT
(F39) JMPJSB2
(C32) NOP2B
U161A
RORT22 ← P1-50
RORT21 ← P1-49
RORT20 ← P1-59
U54 BINARY-TO-OCTAL DECODER ENABLE
0 LRZ
1 LLZ
2 SLI
3 SRI
4 RRZ
5 RLZ
6 RDT
7 NOP
FUBUS ← P2-63
U154B
+5V
R7 1K
(G35) COMMAND BUS 0-31
FHB ← P1-13
U46A
(88) T-BUS 0-15
U27 ENABLE
T RIGHT U15 ENABLE
TØ NO SHIFT U26 ENABLE
TI LEFT SHIFT U17 ENABLE
T15 CIR RIGHT U16 ENABLE
U37B
U166B
TASL
TASR
ARITH SH
U104A
CIR8 ← P2-31
U132
CTSS
U132B
CTSD
U132C
CRS
U102C
U122A
CIR7 ← P2-29
U152C
CIR7
U132D
U37D
U43D
U34A
U37C
U151C
U131C
SP3I5 ← P2-64
SP3I5 (G23)
MPAD
U43F
U131A
U131D
U162B
(C9) TØ
U162A
(B49) RREGØ
U162C
U152A
TASL
U162D
(C9) CARRY
U162E
U152F
DVSB
FLAG2 ← P1-74
FLAG2 (B45)
U152B
MPAD
U111B
U151B
(F27)SREG15
U111A
U111C
U152
CTSD
U111D
U152D
TASR
(G9) T15
U111E
U164E
SREGIN (C26)
U164B
RREGIN (F43)
(D17) SPIØ
U142A
TASL
CTSD
DVSB
SPISHIFT (D17)
DVSB (B45)
U142B
TASR
CTSD
MPAD
P2-57 DVSB
P2-58 SP3SHIFT
P2-75 SPISHIFT
P2-26 SP3IN
P2-65 SPIIN
U44D
LRZ
RRZ
LRZ+RRZ
U44C
RDT
RLZ
RDT+RLZ
U33A
LLZ
NOP
LLZ+NOP
ZERO LEFT U25 ENABLE 9,11
RL SWAP U14 ENABLE 9,11
T(10) RIGHT SHIFT U24 ENABLE 9,11
T(2:8) LEFT SHIFT U13 ENABLE 9,11
T(1:7) NO SHIFT U23 ENABLE 9,11
P2-76 SPI 0
SPI 0 (G13)
U164
SPISHFT (G13)
U43A
SLI
U44B
LLZ
RLZ
U33B
NOP
RRZ
NOP+LRZ
U46D
SRI
U44A
LRZ
RDT
RDT+LRZ
U145A
SLI
P1-8 → U0
P1-14 → U1
P1-7 → U2
P1-17 → U3
P1-18 → U4
P1-19 → U5
P1-21 → U6
P1-22 → U7
ZERO RIGHT U76 ENABLE 9,11 → U8 U9 U10 U11 (G44) U12 (G44) U13 U14 U15
NO SHIFT U116 ENABLE → P2-13 U8, P2-14 U9, P2-15 U10, P2-16 U11
LEFT SHIFT U96 ENABLE → P2-19 U12, P2-21 U13, P2-22 U14, P2-23 U15
RIGHT SHIFT U86 ENABLE 9,11
LR SWAP U66 ENABLE 9,11
CIR LEFT U106 ENABLE 9,11

30001-60003	TITLE		SHEET 2 OF 5
ARITHMETIC & LOGIC UNIT (ALU) PCA			
ENGINEER	APPROVED	DATE	
HEWLETT-PACKARD DATA SYSTEMS			

P1

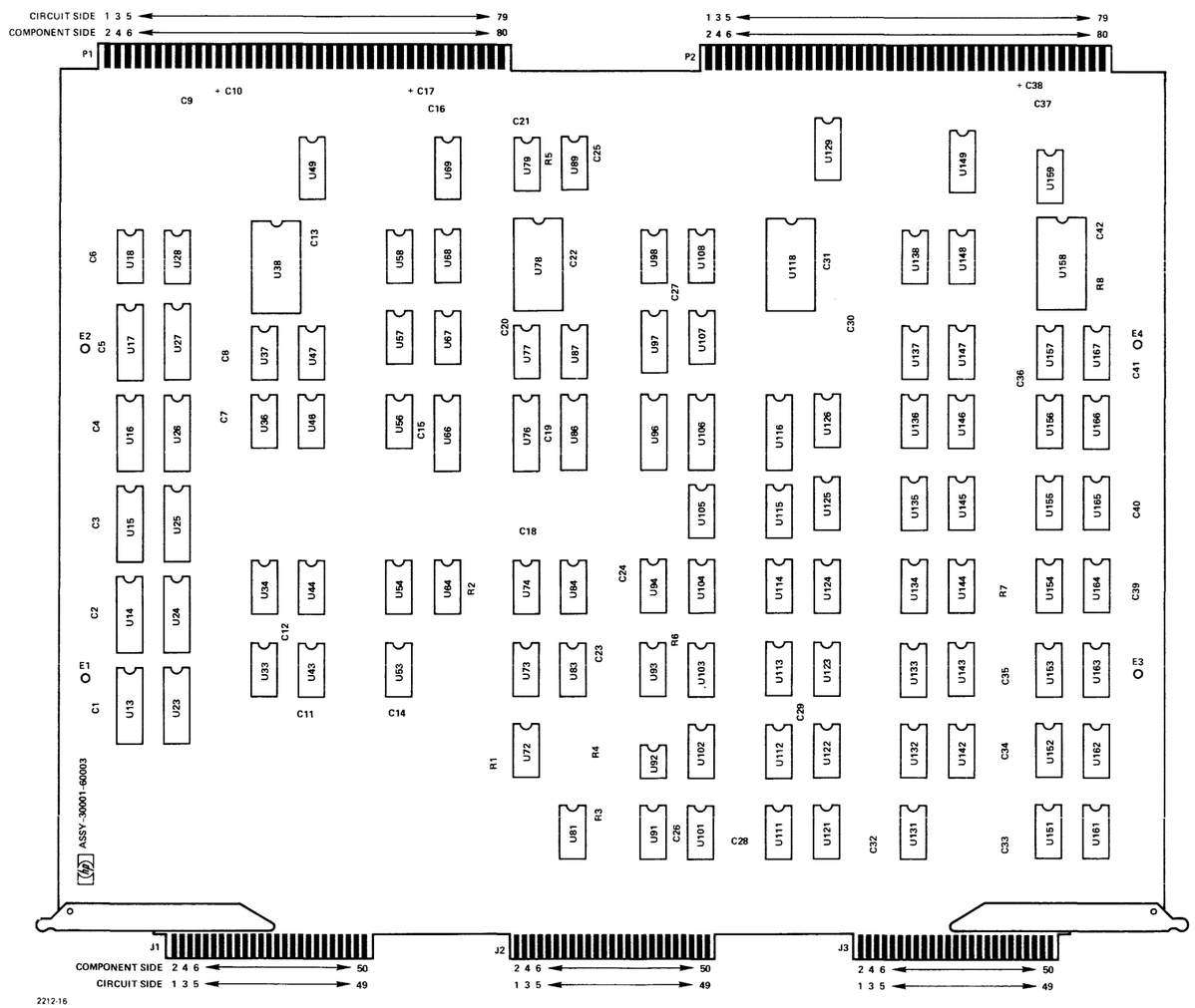
PIN	SIGNAL
1	S00
2	COM
3	JLUI2
4	S01
5	S02
6	S03
7	U02
8	U00
9	R02
10	R03
11	R01
12	R00
13	FHB
14	U01
15	FLAG1
16	T00
17	U03
18	U04
19	U05
20	+5V
21	U06
22	U07
23	NXT1
24	JLUI1
25	T15
26	ALUS0
27	ALUS3
28	ALUS2
29	ALUS1
30	NXT2
31	ROM10
32	ROM11
33	ROM12
34	ROM13
35	ROM14
36	
37	CARRY
38	CARRY
39	COM
40	COM
41	RREG00
42	
43	PRTYMODE
44	OVFL
45	RDCPX2
46	IOTIMER
47	
48	INTFLAG
49	RORT21
50	RORT22
51	S07
52	S06
53	S05
54	S04
55	RDJMPR
56	
57	
58	
59	RORT20
60	+5V
61	R04
62	R05
63	R06
64	R07
65	SWLDRAR
66	ROMFCNT
67	DISPFLAG
68	CCPX
69	SINTFLAG
70	SDISFLAG
71	NXT=2
72	
73	SKIPNOP
74	FLAG2
75	ALUMODE
76	T=0
77	SAME
78	CLOCK
79	FREEZE
80	COM

P2

PIN	SIGNAL
1	NOP1
2	COM
3	S08
4	S09
5	S10
6	S11
7	R11
8	R10
9	R09
10	R08
11	UBNT
12	RPTFCN
13	U08
14	U09
15	U10
16	U11
17	PANLSTOR
18	
19	U12
20	+5V
21	U13
22	U14
23	U15
24	RORT12
25	RORT13
26	SP3IN
27	RFSAME
28	SFSAME
29	CIR07
30	
31	CIR08
32	ROMFCN1
33	PANLREAD
34	RSSEL
35	S15
36	S14
37	S13
38	S12
39	COM
40	COM
41	REPEAT
42	
43	RORT11
44	RORT10
45	NOP2
46	RORT14
47	R12
48	R13
49	R14
50	
51	R15
52	NOP2
53	SHFTCLK
54	RFINH
55	JSB1
56	JMPJSB1
57	DVSB
58	SP3SHIFT
59	
60	+5V
61	SLOAD
62	BNDT
63	FUBUS
64	SP315
65	SP1IN
66	DISPLAY
67	ALUFC
68	REPN
69	NOP2B
70	
71	JMPJSB
72	DSPFLAG
73	SSREG
74	
75	SP1SHIFT
76	SP100
77	SRREG
78	CPURST
79	OFCENB
80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
13-17	0755	64	0512	93	0375	121	0205	148	0367
18	0367	66	0755	94	0685	122	0141	149	0262
		67	0837	96	0755	123	0371		
23-27	0755	68	0367	97	0611	124,125	0512	151	0239
28	0367	69	0262	98	0367	126	0373	152	0424
						129	0262	153	0608
33	0371	72	0512	101	0141			154	0370
34	0373	73	0372	102	0370	131	0370	155	0384
36	0382	74	0686	103	0373	132	0205	156	0371
37	0239	76	0755	104	0837	133	0608	157	0372
38	0999	77	0688	105	0512	134,135	0512	158	0606
		78	0606	106	0722	136,137	0373	159	0375
43	0683	79	0686	107	0837	138	0367		
44	0370			108	0367			161	0374
46	0424	81	0846			142	0685	162	0379
47	0683	83	0374	111	0379	143	0608	163	0608
49	0262	84	0239	112	0688	144	0837	164	0141
		86	0755	113	0371	145	0239	165	0379
53	0695	87	0691	114,115	0512	146	0373	166	0376
54	0608	89	0690	116	0755	147	0371	167	0370
56	0282			118	0606				
57	0686	91	0696						
58	0367	92	0535						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

SBUS REGISTER AND CONTROL

S0 ← P1-1
S1 ← P1-4
S2 ← P1-5
S3 ← P1-6
S4 ← P1-50
S5 ← P1-53
S6 ← P1-52
S7 ← P1-51
S8 ← P2-3
S9 ← P2-4
S10 ← P2-5
S11 ← P2-6
S12 ← P2-38
S13 ← P2-37
S14 ← P2-36
S15 ← P2-35

ROR1/ROR2

ROM 10 ← P1-31 — (D33) U89-8 — U134A — U112-1 (G35), U103-9 (E37)
ROM 11 ← P1-32 — U103-2 (E37) — U134B — U83-10 (H33)
ROM 12 ← P1-33 — U112-2 (G35) — U124A — U103-12 (E37), U83-12 (G33)
ROM 13 ← P1-34 — U94-10 (G35), U103-10 (E37) — U124B — U83-9(G33), U93-5(C45)
ROM 14 ← P1-35 — U103-5 (E37), U93-6 (C45) — PNLR U105A — U83-13 (G34), U93-2 (B46)
(H46) $\overline{RST}$ — PNLR U105B — U94-2 (B33)
(G35) CLK1 — (F3) CLK1
+5V — R2 1K — U72B-10 (B48)
+5V — R1 1K — U114-1 (F37)

U93-1 (E37), U103-1 (E37), U113-3 (G33)

U135A, U135B, U125A, U125B, U115A, U115B

0 → $\overline{0}$, 1 → T, 2 → $\overline{2}$, 3 → $\overline{3}$, 4 → $\overline{4}$, 4B

U165-1 (C35)

X-BUS (E35)

Y-BUS (C32)

SFSAME ← P2-28 — U151A — (F32) NOP1
(G3) CF — U74B
(G35) COMMAND BUS — $\overline{TASR}$ — U101A
24 $\overline{MPAD}$ — U121A — (E12) SP3 15

$\overline{SLOAD}$ ← P2-61
SHFTCLK ← P2-53

S-REG Ø-15 (B2)

U18 4-BIT SHIFT REGISTER — S0 S1 S2 S3 — SERIAL IN (SREG-IN (G14)) — SERIAL/SHIFT CLOCK — PARALLEL CLOCK — PARALLEL ENABLE

U58 4-BIT SHIFT REGISTER — S4 S5 S6 S7

U38 4-BIT SHIFT REGISTER — S8 S9 S10 S11

U138 4-BIT SHIFT REGISTER — S12 S13 S14 S15 — SREG 15 (G13)

U49 8-BIT SHIFT REGISTER — SERIAL IN — PARALLEL ENABLE — CLOCK ENABLE — Q_7, $\overline{Q_7}$

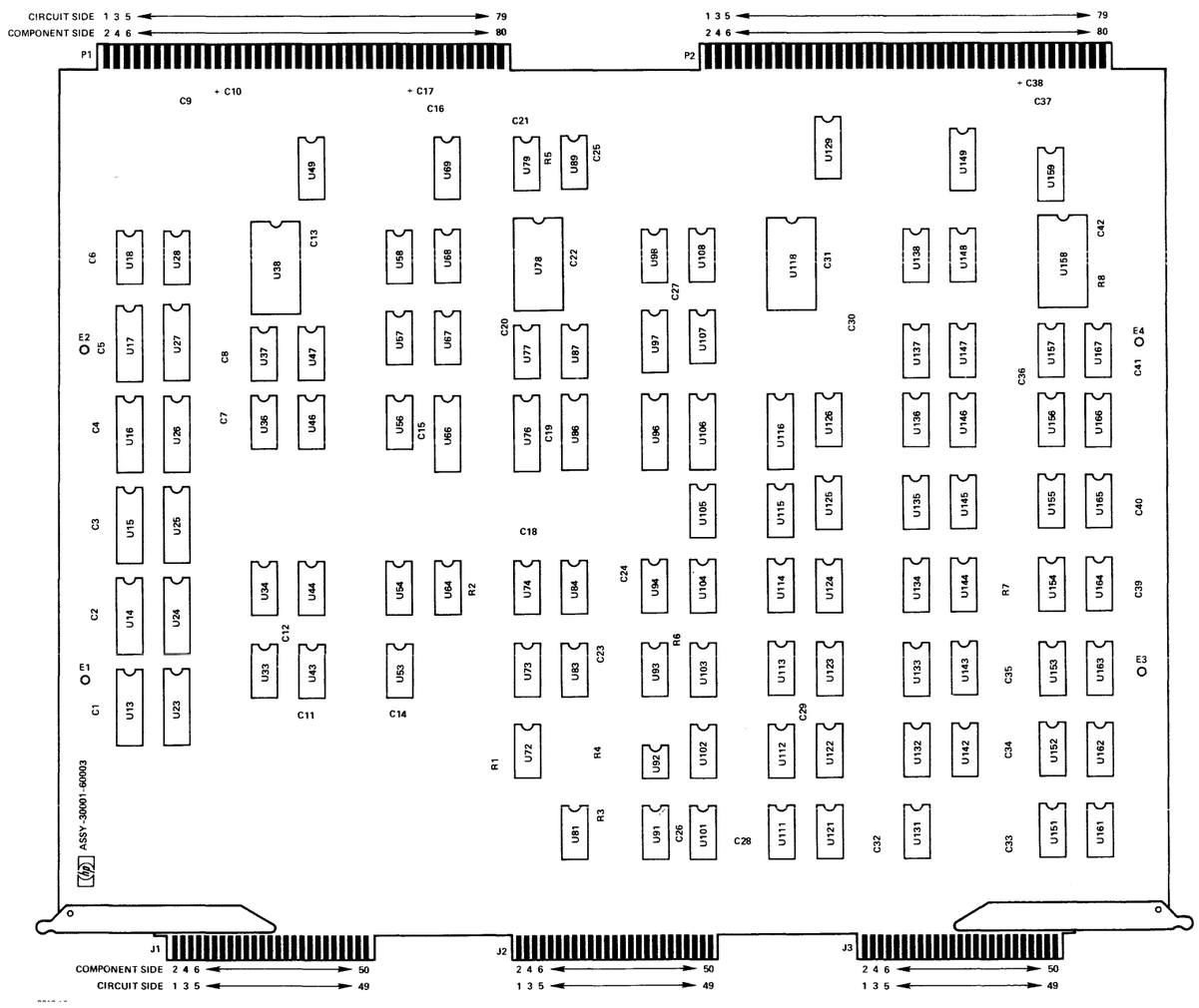
U129 8-BIT SHIFT REGISTER — SERIAL IN — PARALLEL ENABLE — CLOCK ENABLE — Q_7, $\overline{Q_7}$ → P2-73 → SSREG

30001-60003 TITLE	SHEET 3 OF 5
ARITHMETIC & LOGIC UNIT (ALU) PCA	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD	

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	S00	1	NOP1
2	COM	2	COM
3	JLUI2	3	S08
4	S01	4	S09
5	S02	5	S10
6	S03	6	S11
7	U02	7	R11
8	U00	8	R10
9	R02	9	R09
10	R03	10	R08
11	R01	11	UBNT
12	R00	12	RPTFCN
13	FHB	13	U08
14	U01	14	U09
15	FLAG1	15	U10
16	T00	16	U11
17	U03	17	PANLSTOR
18	U04	18	
19	U05	19	U12
20	+5V	20	+5V
21	U06	21	U13
22	U07	22	U14
23	NXT1	23	U15
24	JLUI1	24	RORT12
25	T15	25	RORT13
26	ALUS0	26	SP3IN
27	ALUS3	27	RFSAME
28	ALUS2	28	SFSAME
29	ALUS1	29	CIR07
30	NXT2	30	
31	ROM10	31	CIR08
32	ROM11	32	ROMFCN1
33	ROM12	33	PANLREAD
34	ROM13	34	RSSEL
35	ROM14	35	S15
36		36	S14
37	CARRY	37	S13
38	CARRY	38	S12
39	COM	39	COM
40	COM	40	COM
41	RREG00	41	REPEAT
42		42	
43	PRTYMODE	43	RORT11
44	OVFL	44	RORT10
45	RDCPX2	45	NOP2
46	IOTIMER	46	RORT14
47		47	R12
48	INTFLAG	48	R13
49	RORT21	49	R14
50	RORT22	50	
51	S07	51	R15
52	S06	52	NOP2
53	S05	53	SHFTCLK
54	S04	54	RFINH
55	RDJMPR	55	JSB1
56		56	JMPJSB1
57		57	DVSB
58		58	SP3SHIFT
59	RORT20	59	
60	+5V	60	+5V
61	R04	61	SLOAD
62	R05	62	BNDT
63	R06	63	FUBUS
64	R07	64	SP315
65	SWLDRAR	65	SP1IN
66	ROMFCNT	66	DISPLAY
67	DISPFLAG	67	ALUFC
68	CCPX	68	REPN
69	SINTFLAG	69	NOP2B
70	SDISFLAG	70	
71	NXT=2	71	JMPJSB
72		72	DSPFLAG
73	SKIPNOP	73	SSREG
74	FLAG2	74	
75	ALUMODE	75	SP1SHIFT
76	T=0	76	SP100
77	SAME	77	SRREG
78	CLOCK	78	CPURST
79	FREEZE	79	OFCENB
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
13-17	0755	64	0512	93	0375	121	0205	148	0367
18	0367	66	0755	94	0685	122	0141	149	0262
		67	0837	96	0755	123	0371		
23-27	0755	68	0367	97	0611	124,125	0512	151	0239
28	0367	69	0262	98	0367	126	0373	152	0424
						129	0262	153	0608
33	0371	72	0512	101	0141			154	0370
34	0373	73	0372	102	0370	131	0370	155	0384
36	0382	74	0686	103	0373	132	0205	156	0371
37	0239	76	0755	104	0837	133	0608	157	0372
38	0999	77	0688	105	0512	134,135	0512	158	0606
		78	0606	106	0722	136,137	0373	159	0375
43	0683	79	0686	107	0837	138	0367		
44	0370			*08	0367			161	0374
46	0424	81	0846			142	0685	162	0379
47	0683	83	0374	111	0379	143	0608	163	0608
49	0262	84	0239	112	0688	144	0837	164	0141
		86	0755	113	0371	145	0239	165	0379
53	0695	87	0691	114,115	0512	146	0373	166	0376
54	0608	89	0690	116	0755	147	0371	167	0370
56	0282			118	0606				
57	0686	91	0696						
58	0367	92	0535						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

FUNCTION FIELD DECODER

NXT=Z ← P1-71
(F24) U105-9 → U84D
DISPLAY ← P2-66 → U94A
NOP2 ← P2-52
NOP2 ← P2-45
(F25) Y-BUS → N

NOP2B ← P2-69
NOP2B (D38)(A12) → U123A

SWLDRAR ← P1-65
REPEAT ← P2-41
U102A, U89B → U134-3 (C22)
(G3) U79-12 →

U163 BINARY-TO-OCTAL DECODER ENABLE
0 TASL, 1 TASR, 2 ROMX, 3 ROMN, 4 JSB, 5 CAND, 6 XOR, 7 AND

U153 BINARY-TO-OCTAL DECODER ENABLE
0 DVSB, 1 UBNT, 2 CADD, 3 SINBO, 4 JMP, 5 BNDT, 6 CAO, 7 SUB

U143 BINARY-TO-OCTAL DECODER ENABLE
0 PNLR, 1 PNLS, 2 ROMT, 3 BONT, 4 REPC, 5 REPN, 6 IOR, 7 CTSD

U133 BINARY-TO-OCTAL DECODER ENABLE
0 MPAD, 1 INCD, 2 CRS, 3 ADCO, 4 CTSS, 5 INC, 6 RPTY, 7 ADD

RPTY → 30 → COMMAND BUS 0-31 (B12)(D24) (G22)(A45)

NOP1 ← P2-1
NOP1 (C42)(G23) → U46C
(F24)X-BUS →

NOP2 → U113B
(C24) U134-5
(E24) U124-8
U83B
CLK1(F22)

(F24) U105-6
(E24) U124-6
(D23) U134-8

NOP 2 ← P2-52
NXT 2 ← P1-30
U121B

U155A, U155B, U155C, U165B, U165C, U165A, U165D, U165E, U146A, U146B, U136A, U136B, U145C, U156B, U167B
(F25) U135-9 →
ALUS 0-3 (D2) →

U147C, U144B, U144A, U147A
(F24) U134-6 →
U112A
U94B
U94C
(D24) U124-9 →
U43E

(G46) RST →
(F3) CLK1 →
PNLS FF U114A
(F24) R1 →
(F3) CLK →
PRTY MODE U53B
(F23) R2 →
JMPJSB FF U64B
(A12) JMPJSB2 →
OFCENB FF U114B

U167D, U167C, U145B, U126A
ALUMODE (D3) →
U156B, U147B, U157, U137B
U158-7 (G3) →
U56A
ROMFCNT (A12) →
(C32) NOP2B → U57C
U159A
(C24) U134-5
(E24) U105-5
(D24) U134-9
U103A
(D24) U134-6
(E24) U124-6
U103B
(E24) U124-9 →
U102D
U145D
ROMFCN1(C47) →

P2-33 ← PANLREAD
P2-34 ← NRSSEL
P2-44 ← RORT10
P2-45 ← RORT11
P2-24 ← RORT12
P2-25 ← RORT13
P2-46 ← RORT14
P1-75 ← ALUMODE
P2-67 ← ALUFC
P1-66 ← ROMFCNT
P1-73 ← SKIPNOP
P2-68 ← REPN
P2-79 ← ØFCENB
P2-55 ← JSB1
P2-71 ← JMPJSB
P2-17 ← PANLSTOR
P1-43 ← PRTYMODE
P2-56 ← JMPJSB1
P2-54 ← RFINH
P2-32 ← ROMFCN1

30001-60003	TITLE	SHEET 4 OF 5	
ARITHMETIC & LOGIC UNIT (ALU) PCA			
ENGINEER	APPROVED	DATE	
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION			

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	S00	1	NOP1
2	COM	2	COM
3	JLUI2	3	S08
4	S01	4	S09
5	S02	5	S10
6	S03	6	S11
7	U02	7	R11
8	U00	8	R10
9	R02	9	R09
10	R03	10	R08
11	R01	11	UBNT
12	R00	12	RPTFCN
13	FHB	13	U08
14	U01	14	U09
15	FLAG1	15	U10
16	T00	16	U11
17	U03	17	PANLSTOR
18	U04	18	
19	U05	19	U12
20	+5V	20	+5V
21	U06	21	U13
22	U07	22	U14
23	NXT1	23	U15
24	JLUI1	24	RORT12
25	T15	25	RORT13
26	ALUS0	26	SP3IN
27	ALUS3	27	RFSAME
28	ALUS2	28	SFSAME
29	ALUS1	29	CIR07
30	NXT2	30	
31	ROM10	31	CIR08
32	ROM11	32	ROMFCN1
33	ROM12	33	PANLREAD
34	ROM13	34	RSSEL
35	ROM14	35	S15
36		36	S14
37	CARRY	37	S13
38	CARRY	38	S12
39	COM	39	COM
40	COM	40	COM
41	RREG00	41	REPEAT
42		42	
43	PRTYMODE	43	RORT11
44	OVFL	44	RORT10
45	RDCPX2	45	NOP2
46	IOTIMER	46	RORT14
47		47	R12
48	INTFLAG	48	R13
49	RORT21	49	R14
50	RORT22	50	
51	S07	51	R15
52	S06	52	NOP2
53	S05	53	SHFTCLK
54	S04	54	RFINH
55	RDJMPR	55	JSB1
56		56	JMPJSB1
57		57	DVSB
58		58	SP3SHIFT
59	RORT20	59	
60	+5V	60	+5V
61	R04	61	SLOAD
62	R05	62	BNDT
63	R06	63	FUBUS
64	R07	64	SP315
65	SWLDRAR	65	SP1IN
66	ROMFCNT	66	DISPLAY
67	DISPFLAG	67	ALUFC
68	CCPX	68	REPN
69	SINTFLAG	69	NOP2B
70	SDISFLAG	70	
71	NXT=2	71	JMPJSB
72		72	DSPFLAG
73	SKIPNOP	73	SSREG
74	FLAG2	74	
75	ALUMODE	75	SP1SHIFT
76	T=0	76	SP100
77	SAME	77	SRREG
78	CLOCK	78	CPURST
79	FREEZE	79	OFCENB
80	COM	80	COM

I.C. INDEX

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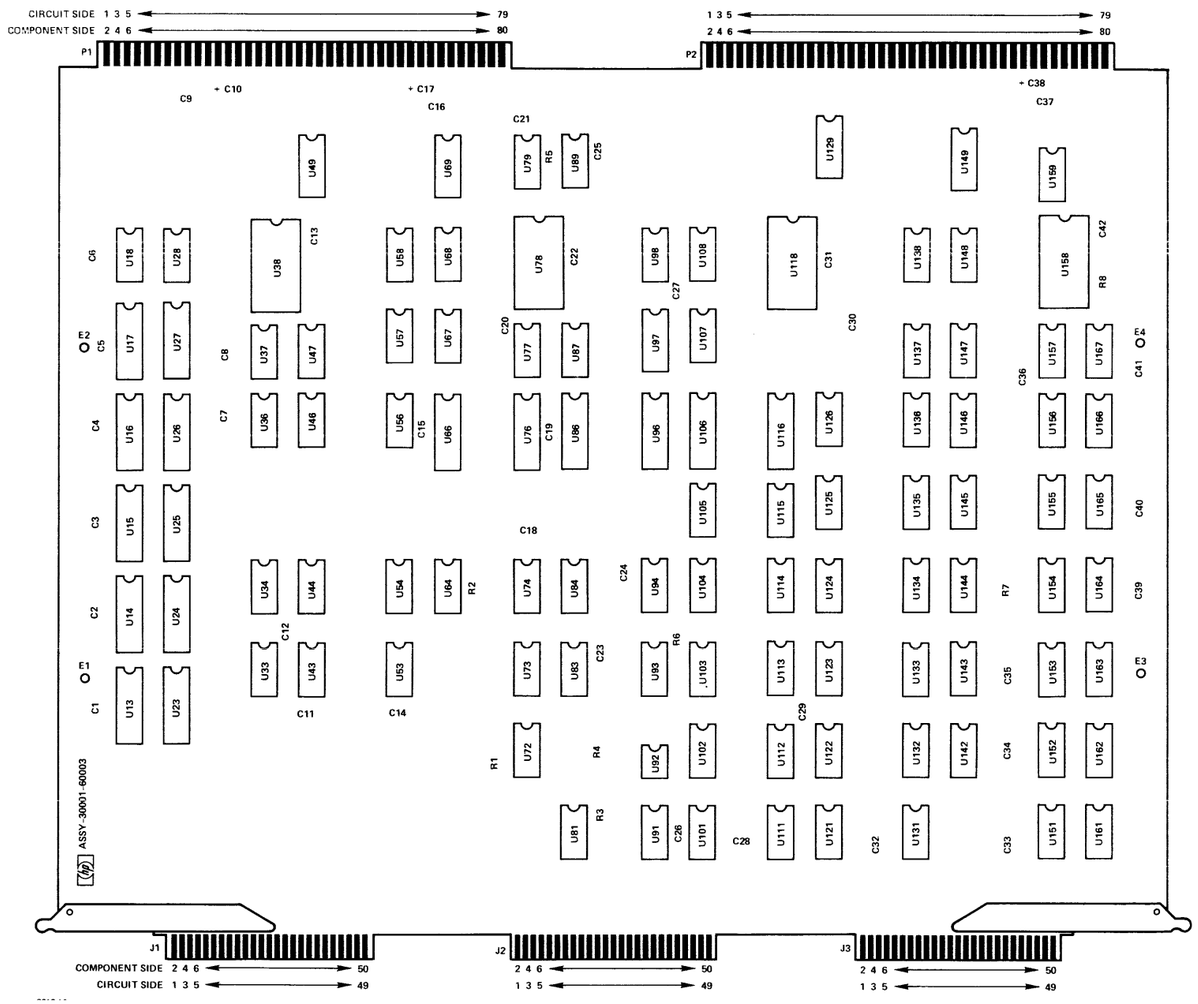
54	0608	89	0690	116	0755	147	0371	167	0370
56	0282			118	0606				
57	0686	91	0696						
58	0367	92	0535						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

RBUS REGISTER AND CONTROL

(G35) COMMAND BUS
REPC
RSPN
U154A
P2-11 UBNT
P2-62 SNOT
P2-12 RPTFCN
P1-41 RREGØ
RREGØ (F13)(DB)
U46E
U36-1,2 (E8)
R-REG Ø-15 (B2)
TASL 2,13
U74A
RREG MODE (D43)
(H13) DVSB
(C8) CARRY
U142A
(C24) 134-5
(F12) FLAG2
U43C
(F24) U105-6
(D24) U124-5
(E24) U124-8
(E24) U105-5
U93A
RPTNI
R6
+5V
1K
U73C
(F23) R2
U72B
P1-30 NXT2
U73B
(H39) ROMFCN1
(F3) CLK1
U72A
P1-3 JLUI2
(H46) RST
NXT1 P1-23
RØ P1-12
R1 P1-11
R2 P1-9
R3 P1-10
U28 D3 D2 D1 D0 4-BIT SHIFT REGISTER
SERIAL IN
SERIAL/SHIFT CLOCK
PARALLEL CLOCK
PARALLEL ENABLE
RFSAME P2-27
(F32) NOP1
U151D
(G2) U79-12
U74C
JLUI1 P1-24
R4 P1-61
R5 P1-62
R6 P1-63
R7 P1-64
U6B
(B46) RREG MODE
SHFTCLK P2-53
R8 P2-10
R9 P2-9
R10 P2-8
R11 P2-7
U10B
SLOAD P2-61
R12 P2-47
R13 P2-48
R14 P2-49
R15 P2-51
U14B
(G14) RREG-IN
SERIAL SHIFT CLOCK
U69 8-BIT SHIFT REGISTER
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE
U149 8-BIT SHIFT REGISTER
P2-77 SRREG
R3 1K +5V
R4 1K +5V
U101C
(B19) U12
U92A
(F3) CLK
U91A
U101D
(B19) U11
U91B
RST (F23)(F37)(C47)
U81A
U81D
U81C
U81B
S13
S12
S11
S10
P1-67 DISPFLAG
P1-48 INTFLAG
5-BUS 10-13
CPURST P2-78
SDISFLAG P1-70
SINTFLAG P1-69
CCPX P1-68
RDCPX2 P1-45
IOTIMR P1-46

30001-60003	TITLE	SHEET 5 OF 5
ARITHMETIC & LOGIC UNIT (ALU) PCA		
ENGINEER	APPROVED	DATE
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		

CPU/IOP DETAILED DIAGRAM SET

DD-203

R-BUS PCA

30001-60004

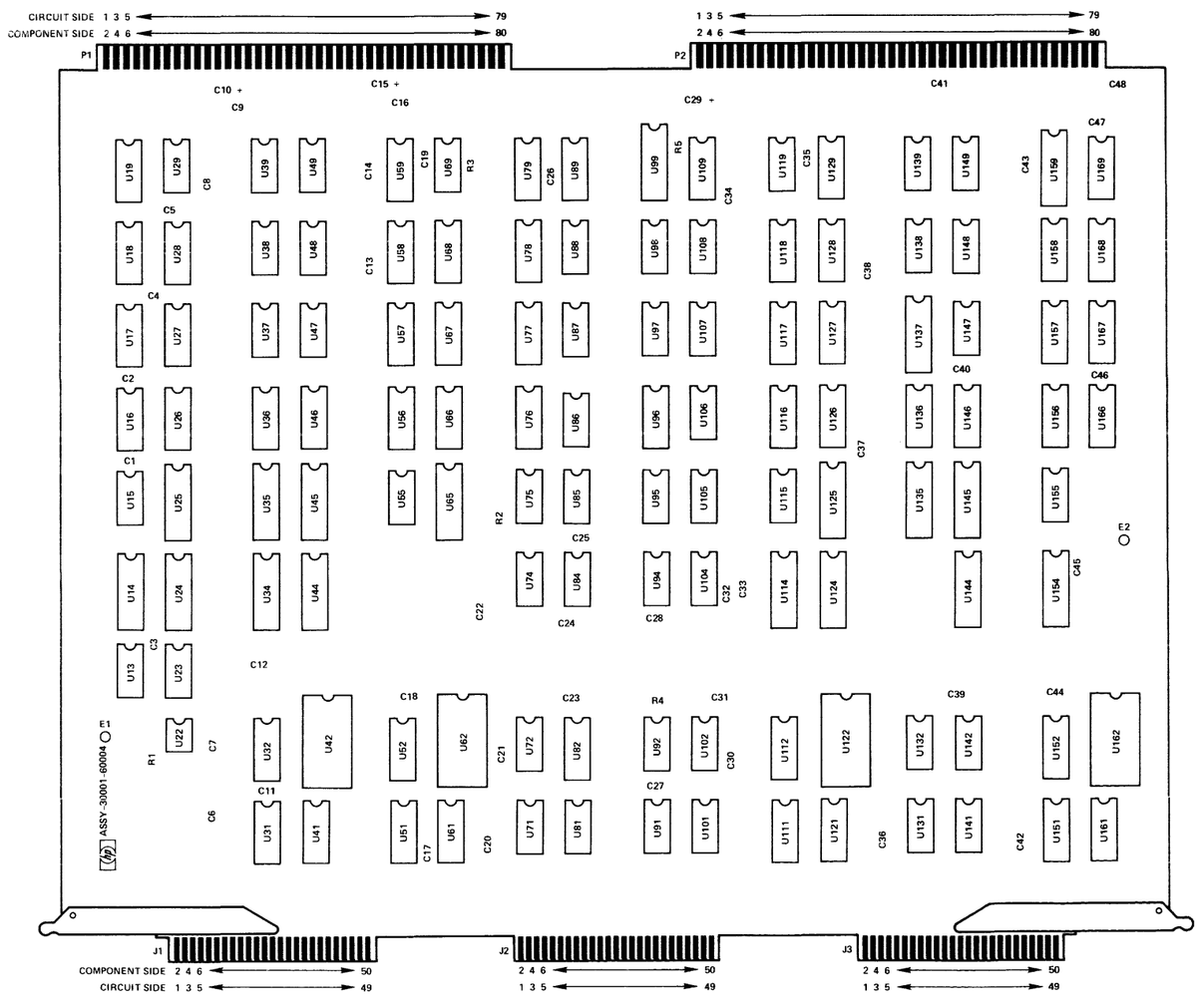
SERIES 1247

REV C

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	SP100	1	
2	COM	2	COM
3	PADDX	3	QS
4	U05	4	DS
5	INCSR	5	RF01
6	S07	6	STORAR
7	PADDSUB	7	SFQ0
8	S06	8	
9	PADDXS01	9	SP1SHIFT
10	S05	10	ALPHA
11	CLSR	11	RDJMPR
12	S04	12	CIR04
13	PADDXS00	13	RDCIR
14		14	
15	$\overline{TR3}$	15	R08
16		16	RF00
17		17	JMPJSB1
18		18	
19		19	
20	+5V	20	+5V
21	R00	21	R09
22	R01	22	R10
23	R02	23	R11
24	$\overline{R03}$	24	PADDIN11
25	TR2	25	PADDIN10
26	S00	26	PADDIN09
27	SR00	27	PADDIN08
28		28	
29		29	
30		30	
31		31	RFSAME
32	DECSR	32	NUMERIC
33	SR01	33	U10
34	SR02	34	NXTGATE
35	INCNAMER	35	U08
36		36	U09
37	S03	37	U11
38		38	
39	COM	39	COM
40	COM	40	COM
41		41	
42		42	
43	S01	43	U13
44	S02	44	U12
45	U06	45	U15
46	U07	46	U14
47	SHFTCLK	47	SF04
48		48	SF03
49	NOP2	49	SF00
50	R04	50	SF02
51	R05	51	ST00
52	TR0	52	ST02
53	R06	53	ST01
54	ST03	54	RF02
55	R07	55	SSBUS
56	ST04	56	SLOAD
57	U00	57	SP1IN
58	RF03	58	SRBUS
59		59	
60	+5V	60	+5V
61	U01	61	R12
62		62	
63	U02	63	R14
64		64	R13
65	U03	65	S09
66	SF01	66	R15
67	U04	67	S11
68		68	S10
69	TR1	69	S12
70	RFINH	70	S08
71	NXT=2	71	S13
72	DISPLAY	72	CIR12
73		73	S14
74		74	CIR13
75	TNAME01	75	CIR14
76		76	CIR15
77	TNAME00	77	S15
78	CLOCK	78	CPURST
79	FREEZE	79	NOP2
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	~~0574~~ 1033	66-68	0574	101	0205	141	0371
		69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574	161	0574
42	0606	87	0140	122	0606	162	0606
44,45	0755	88	0205	124,125	0755	166-169	~~0574~~ 1033
46	0262	89	0724	126-129	~~0574~~ 1033		
47	0847				0239		
48,49	0739	91	0370	131	0374		
		92	0376	132	0755		
51,52	0620	94	0512	135	0262		
55	0367	95	0837	136	0755		
56-59	~~0574~~ 1033	96	0724	137			
		97	0141				



CHANGE	REFERENCE	REVISION PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1809	A-1247-22	ALL
D	22-1715	B-1247-22	1

CIR4 ← P2-12

JMPJSBT ← P2-17

NTX=2 ← P1-71

DISPLAY ← P1-72

DISPLAY(B13)

RFINH ← P1-70

RF3 ← P1-58

RF2 ← P2-54

D5 ← P2-4

Q5 ← P2-3

NXTGATE ← P2-34

RF1 ← P2-5

RF0 ← P2-16

+5V

R5

U119C U91B U132B U131C U95A U86E U106A U97D U107A U106D U86D U105C U19D U86F U148C U148D U138C U978 U96A 2-BIT DECODER U99 ENABLE U139B U96B 2-BIT DECODER U108B U106B U107B U148A U72A U88B U87B

RFNOP

R ← X (D38)

R(8:15) ← 0 (G55)

R(8:7) ← 0 (E55)

R ← SR(G56)

RFQIL (H49)

(D)(F16)

P2-31 → RFSAME

SF2(B12)

SF1(C12)

NTGS

NGT

NG

SF0(B12)

SF3(B12)

SF4(B12)

R ← PADD (E33)

R ← UBUS (D55)

RFQ3(C27)(H49)

RFQ2(H48)

(L)(H41)

U76 DUAL FOUR-TO-ONE MULTIPLEXER

STROBE B

STROBE A

RF(TR0)(H41)

RF(TR1)(H43)

P1-77 → TNAME0

P1-75 → TNAME1

RFQBL(D27)(H48)

U77 FOUR-TO-ONE MULTIPLEXER

STROBE B

STROBE A

RF(TR2)(H44)

RF(TR3)(H46)

TNAME0 (G18)

TNAME1 (G18)

1. PIN 15 OF ALL BSSI IS TO GND. $\overline{S}$ AND $\overline{R}$ OF ALL 74H74 AND 745113 AND 745114 TO 1K RES TO +5V. -25V CONN. MAY BE USED ON ONE RESISTOR.

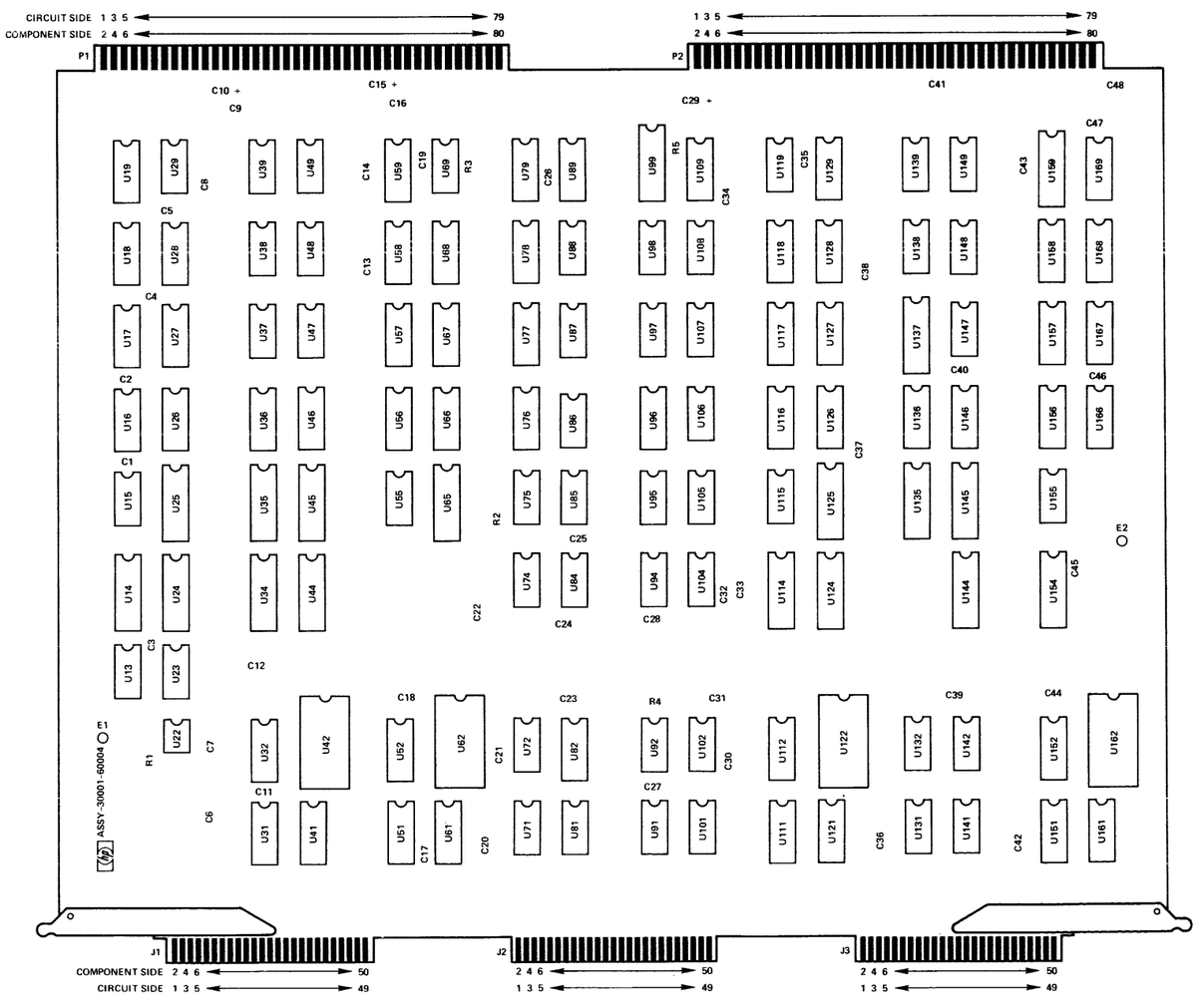
NOTES: UNLESS OTHERWISE SPECIFIED

30001-60004	TITLE	SHEET 1 OF 6
	R-BUS PCA	
ENGINEER	APPROVED	DATE

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	SP100	1	
2	COM	2	COM
3	PADDX	3	QS
4	U05	4	DS
5	INCSR	5	RF01
6	S07	6	STORAR
7	PADDSUB	7	SFQ0
8	S06	8	
9	PADDXS01	9	SP1SHIFT
10	S05	10	ALPHA
11	CLSR	11	RDJMPR
12	S04	12	CIR04
13	PADDXS00	13	RDCIR
14		14	
15	$\overline{TR3}$	15	R08
16		16	RF00
17		17	JMPJSB1
18		18	
19		19	
20	+5V	20	+5V
21	R00	21	R09
22	R01	22	R10
23	R02	23	R11
24	$\overline{R03}$	24	PADDIN11
25	$\overline{TR2}$	25	PADDIN10
26	S00	26	PADDIN09
27	SR00	27	PADDIN08
28		28	
29		29	
30		30	
31		31	RFSAME
32	DECSR	32	NUMERIC
33	SR01	33	U10
34	SR02	34	NXTGATE
35	INCNAMER	35	U08
36		36	U09
37	S03	37	U11
38		38	
39	COM	39	COM
40	COM	40	COM
41		41	
42		42	
43	S01	43	U13
44	S02	44	U12
45	U06	45	U15
46	U07	46	U14
47	SHFTCLK	47	SF04
48		48	SF03
49	NOP2	49	SF00
50	R04	50	SF02
51	R05	51	ST00
52	TR0	52	ST02
53	R06	53	ST01
54	ST03	54	RF02
55	R07	55	SSBUS
56	ST04	56	SLOAD
57	U00	57	SP1IN
58	RF03	58	SRBUS
59		59	
60	+5V	60	+5V
61	U01	61	R12
62		62	
63	U02	63	R14
64		64	R13
65	U03	65	S09
66	SF01	66	R15
67	U04	67	S11
68		68	S10
69	TR1	69	S12
70	RFINH	70	S08
71	NXT=2	71	S13
72	DISPLAY	72	CIR12
73		73	S14
74		74	CIR13
75	TNAME01	75	CIR14
76		76	CIR15
77	TNAME00	77	S15
78	CLOCK	78	CPURST
79	FREEZE	79	NOP2
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	~~0574~~ 1033	66-68	0574	101	0205	141	0371
		69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574	161	0574
42	0606	87	0140	122	0606	162	0606
44,45	0755	88	0205	124,125	0755	166-169	~~0574~~ 1033
46	0262	89	0724	126-129	~~0574~~ 1033		
47	0847				0239		
48,49	0739	91	0370	131	0374		
		92	0376	132	0755		
51,52	0620	94	0512	135	0262		
55	0367	95	0837	136	0755		
56-59	~~0574~~ 1033	96	0724	137			
		97	0141				



1162A

1162B

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1609	A-1247-22
D	22-1715	B-1247-22

S-BUS FIELD DECODER

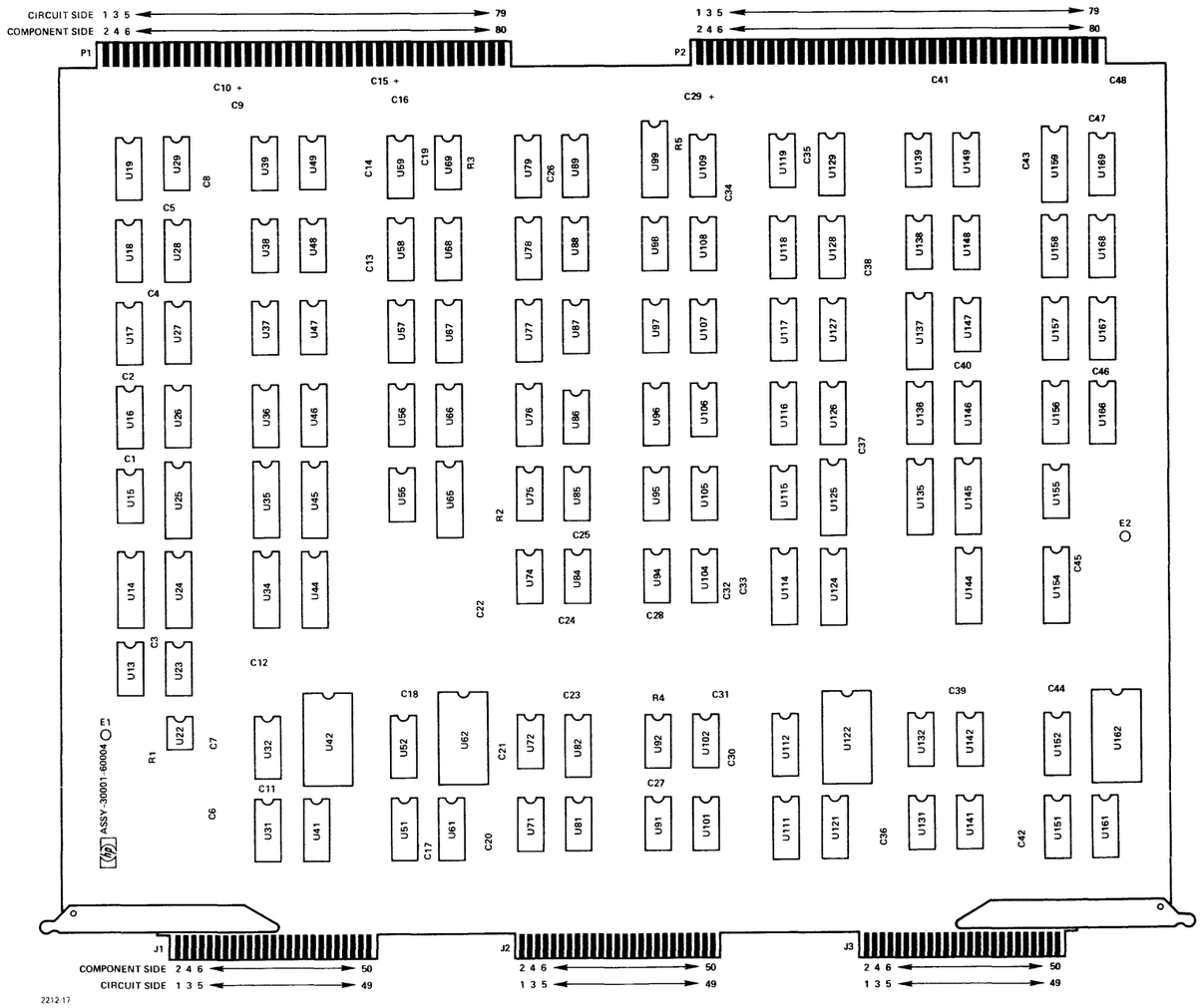
NAMER

30001-60004	SHEET 2 OF 6
R-BUS PCA	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD CO	

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	SP100	1	
2	COM	2	COM
3	PADDX	3	QS
4	U05	4	DS
5	INCSR	5	RF01
6	S07	6	STORAR
7	PADDSUB	7	SFQ0
8	S06	8	
9	PADDXS01	9	SP1SHIFT
10	S05	10	ALPHA
11	CLSR	11	RDJMPR
12	S04	12	CIR04
13	PADDXS00	13	RDCIR
14		14	
15	$\overline{TR3}$	15	R08
16		16	RF00
17		17	JMPJSB1
18		18	
19		19	
20	+5V	20	+5V
21	R00	21	R09
22	R01	22	R10
23	R02	23	R11
24	$\overline{R03}$	24	PADDIN11
25	$\overline{TR2}$	25	PADDIN10
26	S00	26	PADDIN09
27	SR00	27	PADDIN08
28		28	
29		29	
30		30	
31		31	RFSAME
32	DECSR	32	NUMERIC
33	SR01	33	U10
34	SR02	34	NXTGATE
35	INCNAMER	35	U08
36		36	U09
37	S03	37	U11
38		38	
39	COM	39	COM
40	COM	40	COM
41		41	
42		42	
43	S01	43	U13
44	S02	44	U12
45	U06	45	U15
46	U07	46	U14
47	SHFTCLK	47	SF04
48		48	SF03
49	NOP2	49	SF00
50	R04	50	SF02
51	R05	51	ST00
52	TR0	52	ST02
53	R06	53	ST01
54	ST03	54	RF02
55	R07	55	SSBUS
56	ST04	56	SLOAD
57	U00	57	SP1IN
58	RF03	58	SRBUS
59		59	
60	+5V	60	+5V
61	U01	61	R12
62		62	
63	U02	63	R14
64		64	R13
65	U03	65	S09
66	SF01	66	R15
67	U04	67	S11
68		68	S10
69	TR1	69	S12
70	RFINH	70	S08
71	NXT=2	71	S13
72	DISPLAY	72	CIR12
73		73	S14
74		74	CIR13
75	TNAME01	75	CIR14
76		76	CIR15
77	TNAME00	77	S15
78	CLOCK	78	CPURST
79	FREEZE	79	NOP2
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	0574 1033	66-68	0574	101	0205	141	0371
		69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574		
42	0606	87	0140	122	0606	161	0574
44,45	0755	88	0205	124,125	0755	162	0606
46	0262	89	0724	126-129	0574 1033	166-169	0574 1033
47	0847						
48,49	0739	91	0370	131	0239		
		92	0376	132	0374		
51,52	0620	94	0512	135	0755		
55	0367	95	0837	136	0262		
56-59	0574 1033	96	0724	137	0755		
		97	0141				



CHANGE	REFERENCE	REVISION/REL.
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1609	A-1247-22
D	22-1715	B-1247-22

SPI-0 ← P1-1
(D59) R-BUS(4-7)
(C59) R-BUS(0-3)
(F59) R-BUS(12-15)
(D59) R-BUS(8-11)
(A40) S-BUS(4-7)
(A40) S-BUS(0-3)
(C59) U-BUS(0-3)
(B40) S-BUS(12-15)
(B40) S-BUS(8-11)
(D59) U-BUS(4-7)
(G13)STQ3
(G15)STQ8L
(D59) U-BUS(8-11)
(E59) U-BUS(12-15)
(G26)CPURSTB
SPIIN ← P2-57
CPURST ← P2-78
CLOCK ← P1-78
FREEZE ← P1-79
SPISHIFT ← P2-9
(B16)S4-SPI

U25 ENABLE 9,11
U125 ENABLE 9,11
U24 ENABLE 9,11
U124 ENABLE 9,11

U15 4-BIT SHIFT REGISTER
U55 4-BIT SHIFT REGISTER
U115 4-BIT SHIFT REGISTER
U155 4-BIT SHIFT REGISTER
SERIAL IN · SERIAL/SHIFT CLOCK · PARALLEL CLOCK · PARALLEL ENABLE

R-BUS(4-7)(C41)
R-BUS(0-39(A41)
U-BUS(0-3)(B41)
R-BUS(12-15)(F41)
R-BUS(8-11)(E41)
U-BUS(4-7)(D41)
U-BUS(8-11)(F41)
U-BUS(12-15)(G41)

U108C (G7)RFQ3 (F8)RFQ8L → R←SPI
U108D
U104A
U104B
U91A
U94A SPIX15 (E16)
U94B SPIX14 (D16)
+5V R4 1K
+5V R3 1K
+5V R1
U22A → CPURSTB(B19)(E13)
U69B
U69C → CLK 4(B18)
U98A CLK1(D12)(F40)
U98B CLK0(C40) → (V) (B41)

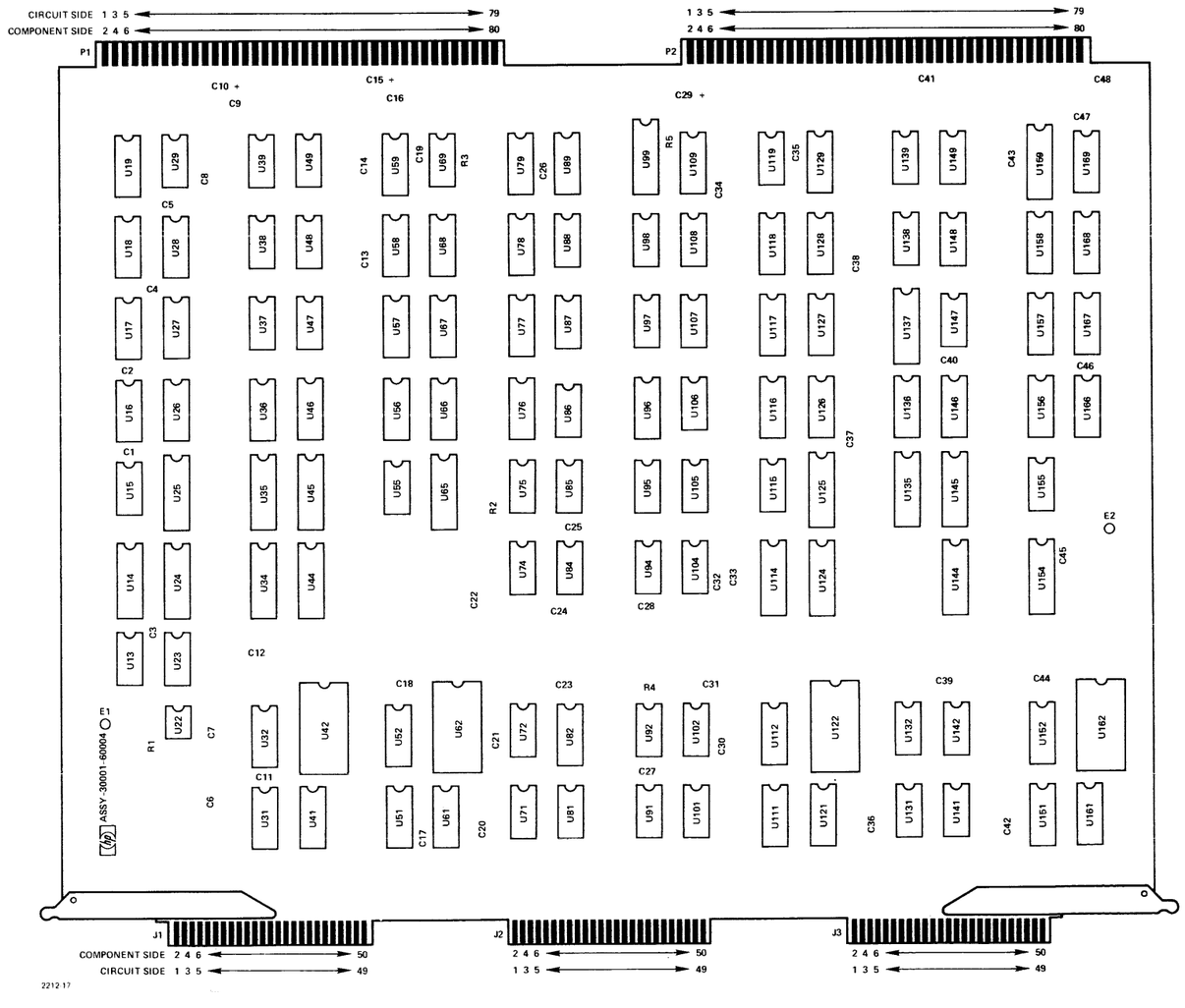
U132A → P2-32 NUMERIC
U31A
U101A
U91D
U101C
U31B
U142D
U81A
U141B
U91C → P2-10 ALPHA
U142C
U141A
U102A
U142E

30001-60004 TITLE		SHEET 30F6
R-BUS PCA		
ENGINEER	APPROVED	DATE
HEWLETT PACKARD		

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	SP100	1	
2	COM	2	COM
3	PADDX	3	QS
4	U05	4	DS
5	INCSR	5	RF01
6	S07	6	STORAR
7	PADDSUB	7	SFO0
8	S06	8	
9	PADDXS01	9	SP1SHIFT
10	S05	10	ALPHA
11	CLSR	11	RDJMPR
12	S04	12	CIR04
13	PADDXS00	13	RDCIR
14		14	
15	$\overline{TR3}$	15	R08
16		16	RF00
17		17	JMPJSB1
18		18	
19		19	
20	+5V	20	+5V
21	R00	21	R09
22	R01	22	R10
23	R02	23	R11
24	$\underline{R03}$	24	PADDIN11
25	$\overline{TR2}$	25	PADDIN10
26	S00	26	PADDIN09
27	SR00	27	PADDIN08
28		28	
29		29	
30		30	
31		31	RFSAME
32	DECSR	32	NUMERIC
33	SR01	33	U10
34	SR02	34	NXTGATE
35	INCNAMER	35	U08
36		36	U09
37	S03	37	U11
38		38	
39	COM	39	COM
40	COM	40	COM
41		41	
42		42	
43	S01	43	U13
44	S02	44	U12
45	U06	45	U15
46	U07	46	U14
47	SHFTCLK	47	SF04
48		48	SF03
49	NOP2	49	SF00
50	R04	50	SF02
51	R05	51	ST00
52	TR0	52	ST02
53	R06	53	ST01
54	ST03	54	RF02
55	R07	55	SSBUS
56	ST04	56	SLOAD
57	U00	57	SP1IN
58	RF03	58	SRBUS
59		59	
60	+5V	60	+5V
61	U01	61	R12
62		62	
63	U02	63	R14
64		64	R13
65	U03	65	S09
66	SF01	66	R15
67	U04	67	S11
68		68	S10
69	TR1	69	S12
70	RFINH	70	S08
71	NXT=2	71	S13
72	DISPLAY	72	CIR12
73		73	S14
74		74	CIR13
75	TNAME01	75	CIR14
76		76	CIR15
77	TNAME00	77	S15
78	CLOCK	78	CPURST
79	FREEZE	79	NOP2
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	0574 1033	66-68	0574	101	0205	141	0371
		69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574	161	0574
42	0606	87	0140	122	0606	162	0606
44,45	0755	88	0205	124,125	0755	166-169	0574 1033
46	0262	89	0724	126-129	0574 1033		
47	0847				0239		
48,49	0739	91	0370	131	0374		
		92	0376	132	0755		
51,52	0620	94	0512	135	0262		
55	0367	95	0837	136	0755		
56-59	0574 1033	96	0724	137			
		97	0141				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1509	A-1247-22
D	22-1715	B-1247-22

(A56)S-BUS(0-3)
(A56)S-BUS(4-7)
(B56)S-BUS(8-11)
(B56)S-BUS(12-15)
PADDIN
PADDSUB
CIR
PADDX
PADDX3
S←PADD (B15)
R←PADD (F7)
(A7) R←X
(H54)U-BUS(0-15)

U45 ENABLE 9,11
U35 ENABLE 9,11
U145 ENABLE 9,11
U135 ENABLE 9,11
U144 ENABLE 9,11
U92A

U82 CARRY GENERATOR
U42 FUNCTION GENERATOR
U62 FUNCTION GENERATOR
U122 FUNCTION GENERATOR
U162 FUNCTION GENERATOR

U31 DUAL 4-TO-1 MULTIPLEXER
U32 DUAL 4-TO-1 MULTIPLEXER
U51 DUAL 4-TO-1 MULTIPLEXER
U52 DUAL 4-TO-1 MULTIPLEXER
U111 DUAL 4-TO-1 MULTIPLEXER
U112 DUAL 4-TO-1 MULTIPLEXER
U151 DUAL 4-TO-1 MULTIPLEXER
U152 DUAL 4-TO-1 MULTIPLEXER

U44
U41 4-BIT REGISTER
U61 4-BIT REGISTER
U121 4-BIT REGISTER
U161 4-BIT REGISTER

S-BUS(0-3)(B21)
S-BUS(4-7)(A21)
S-BUS(8-11)(C21)
S-BUS(12-15)(C21)
R-BUS(4-7)(F54)
R-BUS(0-3)(F54)
CLK Ø(G28)
U-BUS(0-3)(C56)
U-BUS(4-7)(D56)
R-BUS(12-15)(G54)
R-BUS(8-11)(G54)
CLK 1(F28)
U-BUS(8-11)(D56)
STQ5(G13)
STQ2L(F17)
U-BUS(12-15)(E56)

30001-60004 TITLE
R-BUS PCA
SHEET 4 OF 6
ENGINEER | APPROVED | DATE
HEWLETT-PACKARD

P1

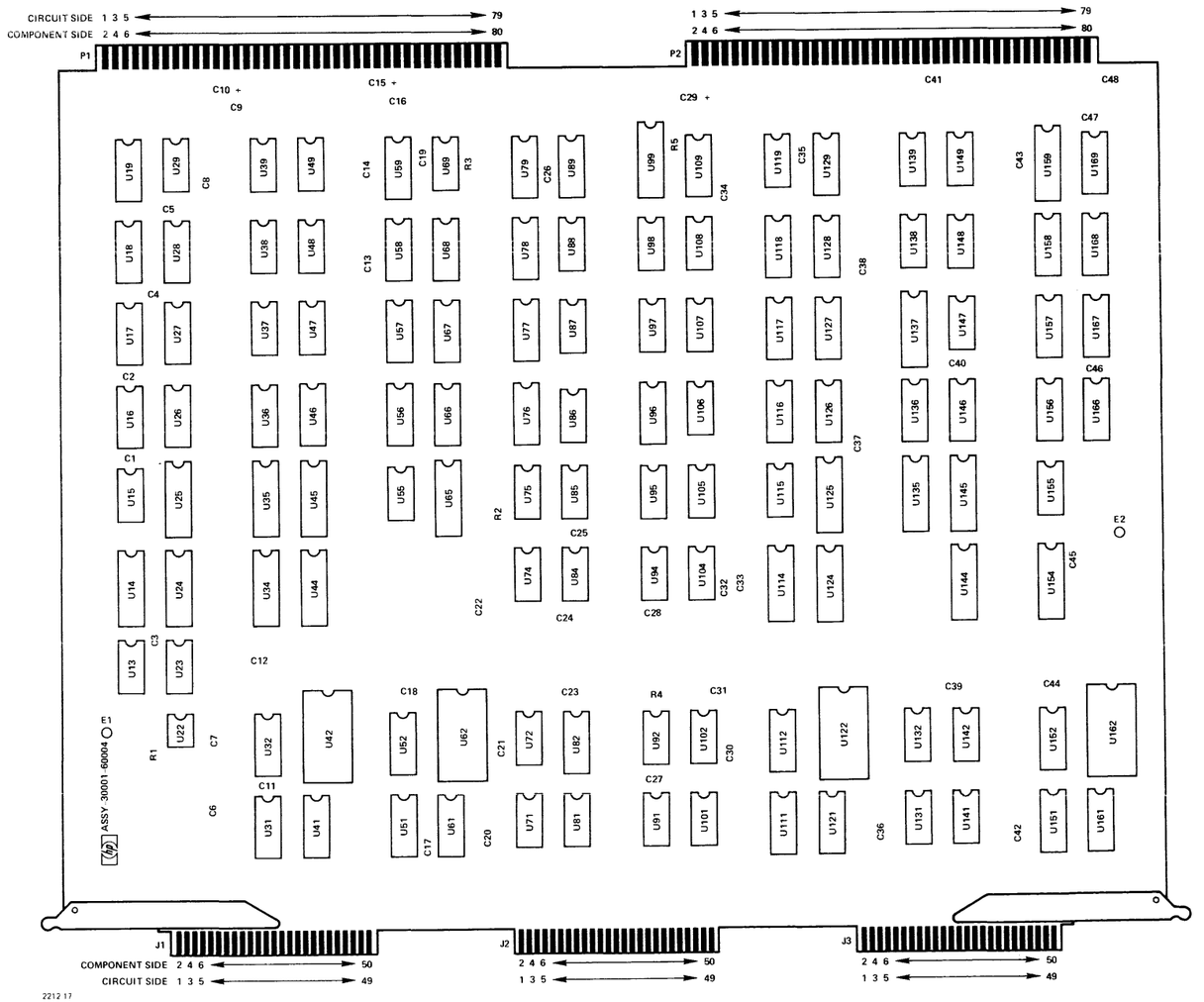
PIN	SIGNAL
1	SP100
2	COM
3	PADDX
4	U05
5	INCSR
6	S07
7	PADDSUB
8	S06
9	PADDXS01
10	S05
11	CLSR
12	S04
13	PADDXS00
14	
15	$\overline{\text{TR3}}$
16	
17	
18	
19	
20	+5V
21	R00
22	R01
23	R02
24	$\overline{\text{R03}}$
25	$\overline{\text{TR2}}$
26	S00
27	SR00
28	
29	
30	
31	
32	DECSR
33	SR01
34	SR02
35	INCNAMER
36	
37	S03
38	
39	COM
40	COM
41	
42	
43	S01
44	S02
45	U06
46	U07
47	SHFTCLK
48	
49	NOP2
50	R04
51	R05
52	TR0
53	R06
54	ST03
55	R07
56	ST04
57	U00
58	RF03
59	
60	+5V
61	U01
62	
63	U02
64	
65	U03
66	SF01
67	U04
68	
69	TR1
70	RFINH
71	NXT=2
72	DISPLAY
73	
74	
75	TNAME01
76	
77	TNAME00
78	CLOCK
79	FREEZE
80	COM

P2

PIN	SIGNAL
1	
2	COM
3	QS
4	DS
5	RF01
6	STORAR
7	SFQ0
8	
9	SP1SHIFT
10	ALPHA
11	RDJMPR
12	CIR04
13	RDCIR
14	
15	R08
16	RF00
17	JMPJSB1
18	
19	
20	+5V
21	R09
22	R10
23	R11
24	PADDIN11
25	PADDIN10
26	PADDIN09
27	PADDIN08
28	
29	
30	
31	RFSAME
32	NUMERIC
33	U10
34	NXTGATE
35	U08
36	U09
37	U11
38	
39	COM
40	COM
41	
42	
43	U13
44	U12
45	U15
46	U14
47	SF04
48	SF03
49	SF00
50	SF02
51	ST00
52	ST02
53	ST01
54	RF02
55	SSBUS
56	SLOAD
57	SP1IN
58	SRBUS
59	
60	+5V
61	R12
62	
63	R14
64	R13
65	S09
66	R15
67	S11
68	S10
69	S12
70	S08
71	S13
72	CIR12
73	S14
74	CIR13
75	CIR14
76	CIR15
77	S15
78	CPURST
79	NOP2
80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	0574	66-68	0574	101	0205	141	0371
	1033	69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574		
42	0606	87	0140	122	0606	161	0574
44,45	0755	88	0205	124,125	0755	162	0606
46	0262	89	0724	126-129	0574	166-169	0574
47	0847				1033		1033
48,49	0739	91	0370	131	0239		
		92	0376	132	0374		
51,52	0620	94	0512	135	0755		
55	0367	95	0837	136	0262		
56-59	0574	96	0724	137	0755		
	1033	97	0141				



2212 17

1165A

1165B

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1290-22
B	RE-DRAWN	NO CHANGE
C	22-1609	A-1247-22
D	22-1715	B-1247-22

(B29)R-BUS(0-3)
(C29)U-BUS(0-3)
(G28)V
(A29)R-BUS(4-7)
(D29)U-BUS(4-7)
(D29)R-BUS(8-11)
(D29)U-BUS(8-11)
(D29)R-BUS(12-15)
(E59)U-BUS(12-15)
(D8)RF(TR0)
(E8)RF(TR1)
(F9)RF(TR2)
(G9)RF(TR3)
(F17)RFQ2L
(F8)RFQ0L
(G7)RFQ2
(C6)RFQIL
(G7)RFQ3
(G7)L

TR0(H18)
TR1(H18)
TR2(G18)
TR3(G18)
STQ2L(F17)
STQ2(G13)
(G14)
(H16)
R-BUS(0-15)(E54)
(H14)
P

U16 4-BIT REGISTER
U17 4-BIT REGISTER
U18 4-BIT REGISTER
U19 4-BIT REGISTER
U26 4-BIT REGISTER
U27 4-BIT REGISTER
U28 4-BIT REGISTER
U56 4-BIT REGISTER
U57 4-BIT REGISTER
U58 4-BIT REGISTER
U59 4-BIT REGISTER
U66 4-BIT REGISTER
U67 4-BIT REGISTER
U68 4-BIT REGISTER
U126 4-BIT REGISTER
U127 4-BIT REGISTER
U128 4-BIT REGISTER
U129 4-BIT REGISTER
U116 4-BIT REGISTER
U117 4-BIT REGISTER
U118 4-BIT REGISTER
U166 4-BIT REGISTER
U167 4-BIT REGISTER
U168 4-BIT REGISTER
U169 4-BIT REGISTER
U156 4-BIT REGISTER
U157 4-BIT REGISTER
U158 4-BIT REGISTER

$D_0D_1D_2D_3$ $Q_0Q_1Q_2Q_3$ CLOCK INPUT ENABLE OUTPUT ENABLE

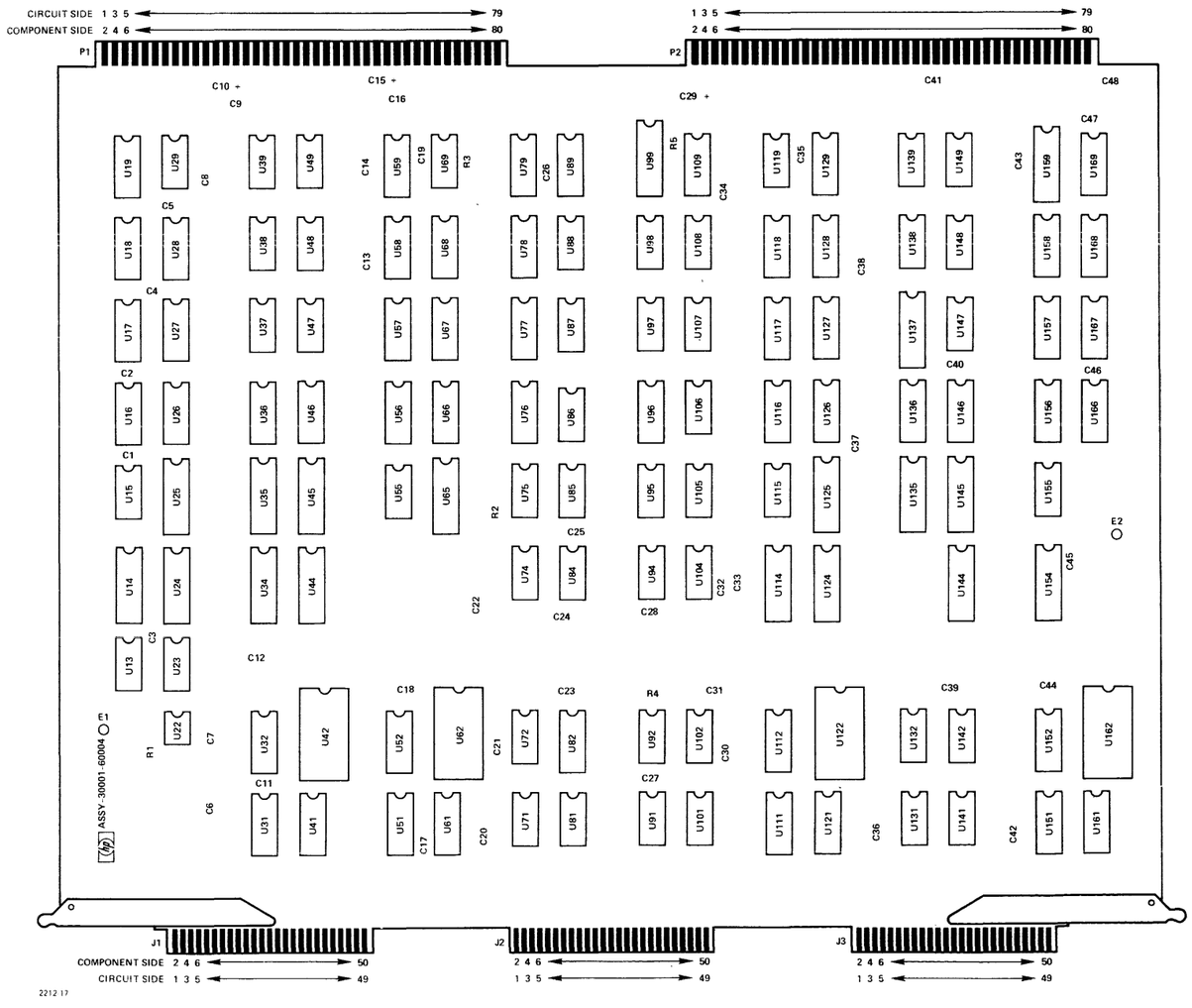
P1-21 → R-BUS0
P1-22 → R-BUS1
P1-23 → R-BUS2
P1-24 → R-BUS3
P1-59 → R-BUS4
P1-51 → R-BUS5
P1-53 → R-BUS6
P1-55 → R-BUS7
P2-15 → R-BUS8
P2-21 → R-BUS9
P2-22 → R-BUS10
P2-23 → R-BUS11
P2-61 → R-BUS12
P2-64 → R-BUS13
P2-63 → R-BUS14
P2-66 → R-BUS15

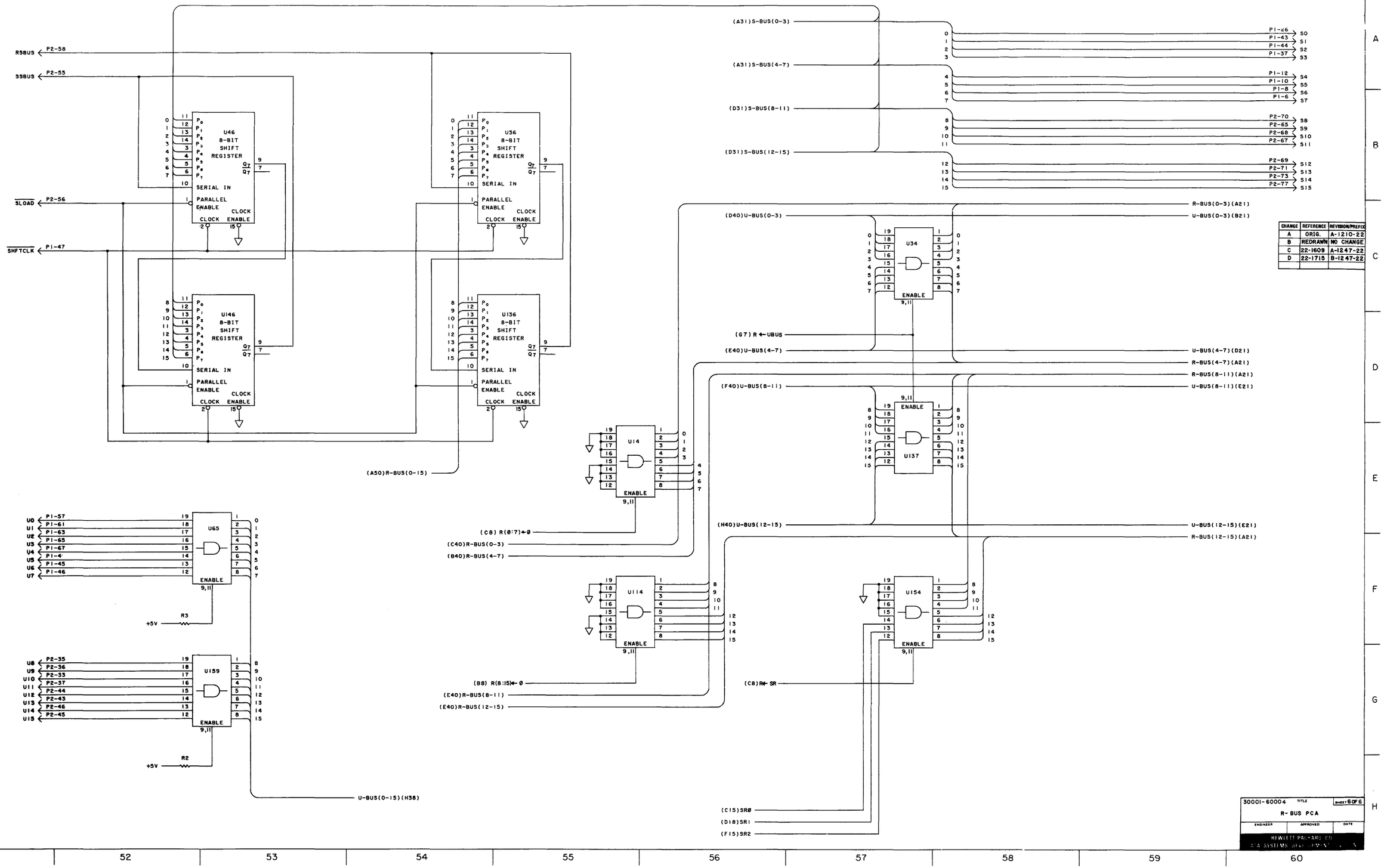
30001-60004 TITLE
R-BUS PCA
SHEET 5 OF 6
ENGINEER | APPROVED | DATE
HEWLETT-PACKARD

P1		P2	
PIN	SIGNAL	PIN	SIGNAL
1	SP100	1	
2	COM	2	COM
3	PADDX	3	QS
4	U05	4	DS
5	INCSR	5	RF01
6	S07	6	STORAR
7	PADDSUB	7	SFQ0
8	S06	8	
9	PADDXS01	9	SP1SHIFT
10	S05	10	ALPHA
11	CLSR	11	RDJMPR
12	S04	12	CIR04
13	PADDXS00	13	RDCIR
14		14	
15	$\overline{TR3}$	15	R08
16		16	RF00
17		17	JMPJSB1
18		18	
19		19	
20	+5V	20	+5V
21	R00	21	R09
22	R01	22	R10
23	R02	23	R11
24	$\underline{R03}$	24	PADDIN11
25	$\overline{TR2}$	25	PADDIN10
26	S00	26	PADDIN09
27	SR00	27	PADDIN08
28		28	
29		29	
30		30	
31		31	RFSAME
32	DECSR	32	NUMERIC
33	SR01	33	U10
34	SR02	34	NXTGATE
35	INCNAMER	35	U08
36		36	U09
37	S03	37	U11
38		38	
39	COM	39	COM
40	COM	40	COM
41		41	
42		42	
43	S01	43	U13
44	S02	44	U12
45	U06	45	U15
46	U07	46	U14
47	SHFTCLK	47	SF04
48		48	SF03
49	NOP2	49	SF00
50	R04	50	SF02
51	R05	51	ST00
52	TR0	52	ST02
53	R06	53	ST01
54	ST03	54	RF02
55	R07	55	SSBUS
56	ST04	56	SLOAD
57	U00	57	SP1IN
58	RF03	58	SRBUS
59		59	
60	+5V	60	+5V
61	U01	61	R12
62		62	
63	U02	63	R14
64		64	R13
65	U03	65	S09
66	SF01	66	R15
67	U04	67	S11
68		68	S10
69	TR1	69	S12
70	RFINH	70	S08
71	NXT=2	71	S13
72	DISPLAY	72	CIR12
73		73	S14
74		74	CIR13
75	TNAME01	75	CIR14
76		76	CIR15
77	TNAME00	77	S15
78	CLOCK	78	CPURST
79	FREEZE	79	NOP2
80	COM	80	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0370	61	0574	98	0690	138	0372
14	0755	62	0606	99	0755	139	0846
15	0367	65	0755				
16-19	0574 1033	66-68	0574	101	0205	141	0371
		69	0686	102	0837	142	0424
22	0535			104,105	0686	144,145	0755
23	0205	71	0608	106	0205	146	0262
24,25	0755	72	0239	107	0374	147	0686
26-28	0574	74	0384	108	0239	148	0239
29	0141	75	0379	109	0724	149	0837
		76-79	0998				
31,32	0620			111,112	0620	151,152	0620
34,35	0755	81	0141	114	0755	154	0755
36	0262	82	0611	115	0367	155	0367
37-39	0739	84	0847	116-118	0574	156,158	0574
		85	0379	119	0424	159	0755
41	0574	86	0424	121	0574	161	0574
42	0606	87	0140	122	0606	162	0606
44,45	0755	88	0205	124,125	0755	166-169	0574 1033
46	0262	89	0724	126-129	0574 1033		
47	0847				0239		
48,49	0739	91	0370	131	0374		
		92	0376	132	0755		
51,52	0620	94	0512	135	0262		
55	0367	95	0837	136	0755		
56-59	0574 1033	96	0724	137			
		97	0141				





CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1609	A-1247-22
D	22-1715	B-1247-22

30001-60004 TITLE SHEET 6 OF 6

R-BUS PCA

ENGINEER | APPROVED | DATE

HEWLETT PACKARD CO

CPU/IOP DETAILED DIAGRAM SET

DD-204

S-BUS PCA

30001-60005

SERIES 1233
1247

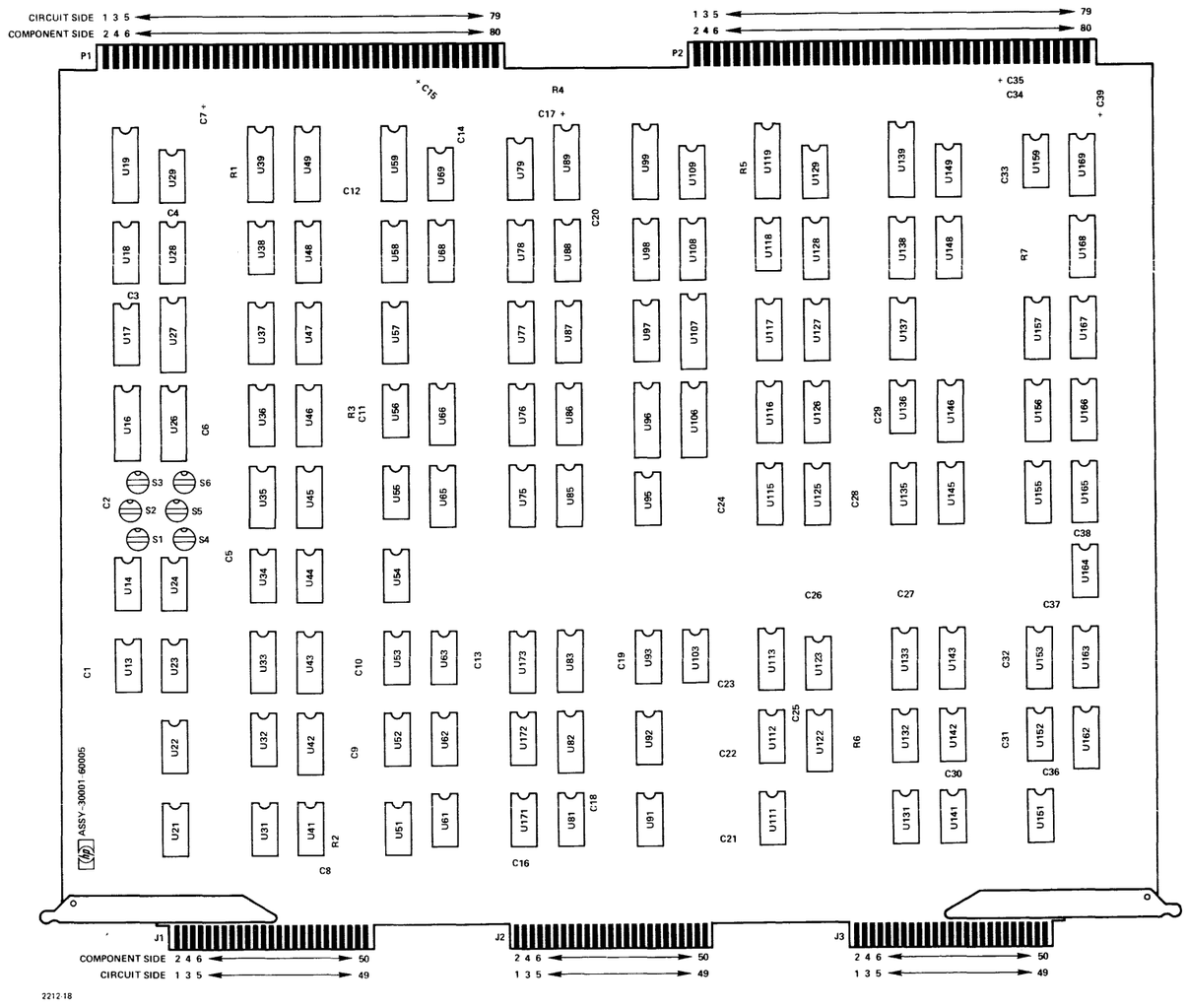
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	ST00	1		1	XXX
2	COM	2	COM	2	XXX
3	S00	3	S08	3	XXX
4	S01	4	S09	4	XXX
5	S02	5	S10	5	XXX
6	S03	6	S11	6	XXX
7	INCP	7	U08	7	XXX
8	SP3IN	8	U09	8	XXX
9	U00	9	U10	9	XXX
10	U01	10	U11	10	XXX
11	U02	11		11	XXX
12	U03	12		12	XXX
13	SF00	13	MDPARITY	13	XXX
14	ST01	14		14	XXX
15	ST02	15	JUMPER01	15	XXX
16	SF01	16	PRTYMODE	16	XXX
17	SFQ0	17	JUMPER02	17	XXX
18	SF02	18		18	XXX
19	PT01	19		19	XXX
20	+5V	20	+5V	20	XXX
21	PT02	21	U12	21	XXX
22	UT02	22	U13	22	XXX
23	UT01	23	U14	23	XXX
24	PSELECT	24	U15	24	XXX
25	JUMPER01	25	COR10	25	XXX
26	JUMPER02	26	COR11	26	XXX
27	COR02	27	COR14	27	XXX
28	COR01	28	COR15	28	XXX
29	COR00	29	COR13	29	XXX
30		30		30	XXX
31	U04	31		31	XXX
32	U05	32		32	XXX
33	U06	33	S12	33	XXX
34	U07	34	S13	34	XXX
35	S04	35	S14	35	XXX
36	S05	36	S15	36	XXX
37	S06	37	CPUSEL	37	XXX
38	S07	38		38	XXX
39	COM	39	COM	39	XXX
40	COM	40	COM	40	XXX
41	RDSWITCH	41		41	XXX
42		42		42	XXX
43	STATUS04	43	MCUD08	43	XXX
44	STATUS05	44	MCUD09	44	XXX
45	STATUS06	45	MCUD10	45	XXX
46	STATUS07	46	MCUD11	46	XXX
47	STATUS00	47	MCUD12	47	XXX
48	STATUS01	48	MCUD13	48	XXX
49	STATUS02	49	MCUD14	49	XXX
50	STATUS03	50	MCUD15	50	XXX
51	TNAME00	51	SP315		
52	TNAME01	52			
53	MCUD01	53	RDCPX1		
54	MCUD00	54	RDCPX2		
55	MCUD03	55	RDMOD		
56	MCUD02	56	RORT16		
57	MCUD05	57	RDIOM		
58	MCUD04	58	RQRT17		
59		59	CNTRMAX		
60	+5V	60	+5V		
61	MCUD06	61	INCTR		
62	MCUD07	62	REPN		
63		63	TR3		
64		64	TR2		
65		65	TR1		
66		66	RORT18		
67		67	TR0		
68		68	RORT19		
69		69	ST STATUS		
70	DISPIOP	70	___		
71	ST03	71	RDOPND		
72	ST04	72	RORT15		
73	NOP2	73	NXTDCD		
74		74	SFSAME		
75	SF03	75	QUP		
76	SF04	76	STIOM		
77	___	77	SP3SHIFT		
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0685	51	0375	91	0239	136	0690
14	0608	52	0373	92	0370	137,138	0574
16	0755	53	0205	93	0205	139	0755
17,18	0574	54	0367	95	0239		
19	0755	55	0424	96	0755	141	0141
		56	0690	97,98	0574	142	0282
21	0375	57-58	0574	99	0755	143	0574
22,23	0685	59	0755			145,146	0620
24	0683			103	0141	148	0716
26,27	0755	61	0239	106,107	0755	149	0367
28	0716	62	0205	108	0716		
29	0367	63	0239	109	0367	151,152	0846
		65,66	0998			153	0574
31	0375	68	0716	111,112	0846	155-157	0574
32	0846	69	0686	113	0574	159	0370
33	0574			115-117	0574		
34	0608	71	0140	118	0842	162,163	0574
35-37	0574	72	0846	119	0755	164	0239
38	0842	73	0574			165-169	0574
39	0755	75-77	0574	122,123	0574		1033
		78,79	0724	125-129	0574		
41	0375				1033		
42,43	0574	81	0376	131	0374		
44	0608	82,83	0574	132	0282		
45-48/1033	0574	85-88/1033	0574	133	0574		
49	0755	89	0755	135	0620		



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-D	A-1233-22	ALL
D	22-1715	B-1233-22	ALL

U18 4-BIT REGISTER — UCOR(0-3) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U17 4-BIT REGISTER — PCOR(0-3) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U58 4-BIT REGISTER — UCOR(4-7) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U57 4-BIT REGISTER — PCOR(4-7) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U98 4-BIT REGISTER — UCOR(8-11) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U97 4-BIT REGISTER — PCOR(8-11) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U138 4-BIT REGISTER — UCOR(12-15) — CLOCK — INPUT ENABLE — OUTPUT ENABLE
U137 4-BIT REGISTER — PC04(12-15) — CLOCK — INPUT ENABLE — OUTPUT ENABLE

UBUS0 ← P1-9 … UBUS3 ← P1-12
UBUS4 ← P1-31 … UBUS7 ← P1-34
UBUS8 ← P2-7 … UBUS11 ← P2-10
UBUS12 ← P2-21 … UBUS15 ← P2-24

(A9) CLK0
(89) CLK1
(89) CLK2
(89) CLK3

STOI (F29)

P2-25 COR10, P2-36 COR11, P2-29 COR13, P2-27 COR14, P2-28 COR15, P1-29 COR0, P1-28 COR1, P1-27 COR2

U59 ENABLE ← P1-62 MCUD7, P1-61 MCUD6, P1-57 MCUD5, P1-58 MCUD4, P1-55 MCUD3, P1-56 MCUD2, P1-53 MCUD1, P1-54 MCUD0
U139 ENABLE ← P2-50 MCUD15, P2-49 MCUD14, P2-48 MCUD13, P2-47 MCUD12, P2-46 MCUD11, P2-45 MCUD10, P2-44 MCUD9, P2-43 MCUD8

P2-37 CPUSEL
P1-7 INCP
P1-78 CLOCK
P1-79 FREEZE

U19 ENABLE — U4-SBUS (C44)
U16 ENABLE — S(0:7)← Ø (D44)
U99 ENABLE
U96 ENABLE — S(8:15)← Ø (E44)

U55A
U55B
NXTDCD

U38 PARITY GENERATOR/CHECKER ODD PARITY BIT — PARITY 1, PARITY 2, PARITY ERROR
U118 PARITY GENERATOR/CHECKER ODD PARITY BIT — PARITY 1, PARITY 2, PARITY ERROR

P1-25, P1-26, P2-17, P2-13, P2-16, P2-15, P1-24, P2-73
JUMPER 2
JUMPER 1
MDPARITY
PRTY MODE
PSELECT
NXTDCD

U28 4-BIT BINARY COUNTER — P(0-3) — LOAD, CLOCK, CARRY IN, CARRY OUT, CLEAR, COUNT
U68 4-BIT BINARY COUNTER — P(4-7)
U108 4-BIT BINARY COUNTER — P(8-11)
U148 4-BIT BINARY COUNTER — P(12-15)

+5V R1 1K
+5V R3 1K
+5V R4 1K
+5V R7 1K

(E29) P←UBUS

U29 4-BIT SHIFT REGISTER — SP3(0-3) — SERIAL IN, CLOCK, PARALLEL ENABLE
U54 4-BIT SHIFT REGISTER — SP3(4-7)
U109 4-BIT SHIFT REGISTER — SP3(8-11)
U149 4-BIT SHIFT REGISTER — SP3(12-15)

U56A, U56B, U69C, U136A, U136B — CLK0 (B29)(B31)(B41) … CLK3 (F2)(F31)(E26)
U69A, U62D — P2-77 → SP3SHIFT

SBUS(0-3)(B12)
SP3(0-3)(D14)
SP34←UBUS (E29)
P1-8 → SP3IN
UBUS(0-3)(D12)
SBUS(4-7)(C12)
SP3(4-7)(D14)
UBUS(4-7)(D12)
SBUS(12-15)(E12)
SP3(8-11)(F14)
UBUS(8-11)(F12)
SBUS(8-11) (E12)
SP3(12-15)(F14)
P2-5 → SP3(15)
UBUS(12-15) (F12)

(L) (D13)
(K) (D13)
(M) (F13)
(N) (F13)

30001-60005	TITLE: S BUS PCA
SHEET 1 OF 5	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION	

SIGNAL INDEX

P1

PIN	SIGNAL
1	ST00
2	COM
3	S00
4	S01
5	S02
6	S03
7	INCP
8	SP3IN
9	U00
10	U01
11	U02
12	U03
13	SF00
14	ST01
15	ST02
16	SF01
17	SFQ0
18	SF02
19	PT01
20	+5V
21	PT02
22	UT02
23	UT01
24	PSELECT
25	JUMPER01
26	JUMPER02
27	COR02
28	COR01
29	COR00
30	
31	U04
32	U05
33	U06
34	U07
35	S04
36	S05
37	S06
38	S07
39	COM
40	COM
41	RDSWITCH
42	
43	STATUS04
44	STATUS05
45	STATUS06
46	STATUS07
47	STATUS00
48	STATUS01
49	STATUS02
50	STATUS03
51	TNAME00
52	TNAME01
53	MCUD01
54	MCUD00
55	MCUD03
56	MCUD02
57	MCUD05
58	MCUD04
59	
60	+5V
61	MCUD06
62	MCUD07
63	
64	
65	
66	
67	
68	
69	
70	DISPIOP
71	ST03
72	ST04
73	NOP2
74	
75	SF03
76	SF04
77	———
78	CLOCK
79	FREEZE
80	COM

P2

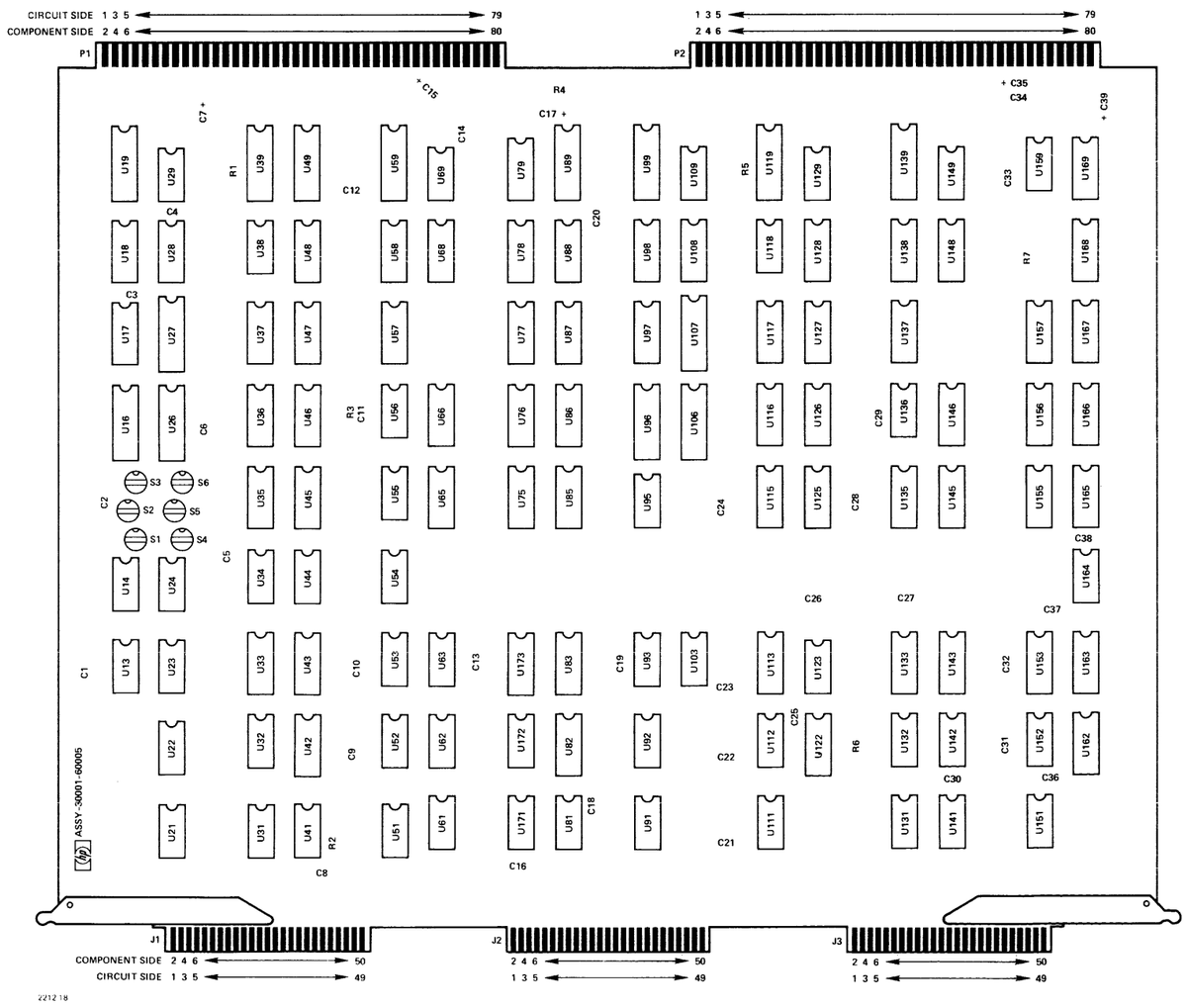
PIN	SIGNAL
1	
2	COM
3	S08
4	S09
5	S10
6	S11
7	U08
8	U09
9	U10
10	U11
11	
12	
13	MDPARITY
14	
15	JUMPER01
16	PRTYMODE
17	JUMPER02
18	
19	
20	+5V
21	U12
22	U13
23	U14
24	U15
25	COR10
26	COR11
27	COR14
28	COR15
29	COR13
30	
31	
32	
33	S12
34	S13
35	S14
36	S15
37	CPUSEL
38	
39	COM
40	COM
41	
42	
43	MCUD08
44	MCUD09
45	MCUD10
46	MCUD11
47	MCUD12
48	MCUD13
49	MCUD14
50	MCUD15
51	SP315
52	
53	RDCPX1
54	RDCPX2
55	RDMOD
56	RORT16
57	RDIOM
58	RORT17
59	CNTRMAX
60	+5V
61	INCTR
62	REPN
63	TR3
64	TR2
65	TR1
66	RORT18
67	TR0
68	RORT19
69	ST STATUS
70	———
71	RDOPND
72	RORT15
73	NXTDCD
74	SFSAME
75	OUP
76	STIOM
77	SP3SHIFT
78	CPURST
79	
80	COM

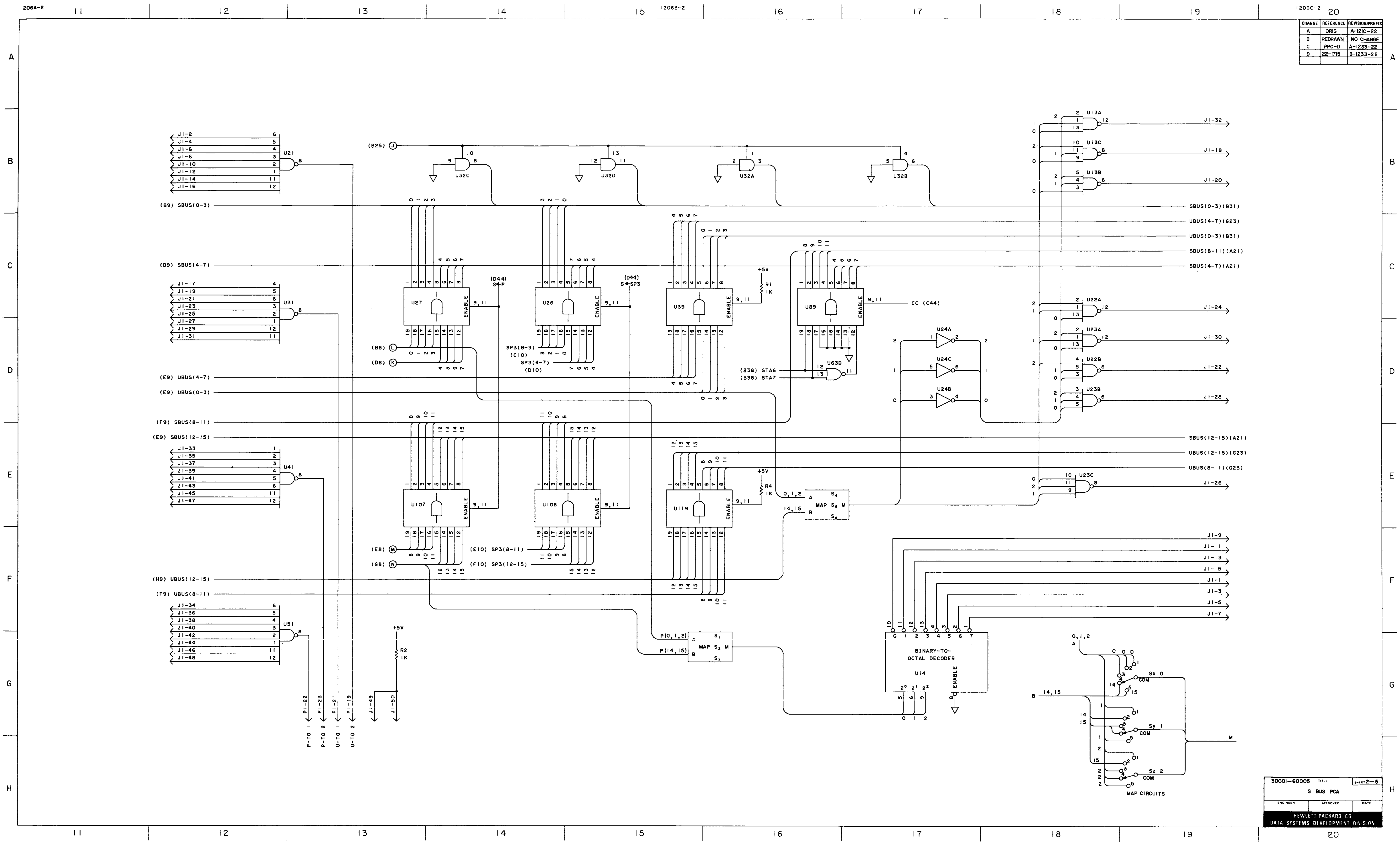
J1

PIN	SIGNAL
1	XXX
2	XXX
3	XXX
4	XXX
5	XXX
6	XXX
7	XXX
8	XXX
9	XXX
10	XXX
11	XXX
12	XXX
13	XXX
14	XXX
15	XXX
16	XXX
17	XXX
18	XXX
19	XXX
20	XXX
21	XXX
22	XXX
23	XXX
24	XXX
25	XXX
26	XXX
27	XXX
28	XXX
29	XXX
30	XXX
31	XXX
32	XXX
33	XXX
34	XXX
35	XXX
36	XXX
37	XXX
38	XXX
39	XXX
40	XXX
41	XXX
42	XXX
43	XXX
44	XXX
45	XXX
46	XXX
47	XXX
48	XXX
49	XXX
50	XXX

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0685	51	0375	91	0239	136	0690
14	0608	52	0373	92	0370	137,138	0574
16	0755	53	0205	93	0205	139	0755
17,18	0574	54	0367	95	0239		
19	0755	55	0424	96	0755	141	0141
		56	0690	97,98	0574	142	0282
21	0375	57 58	0574	99	0755	143	0574
22,23	0685	59	0755			145,146	0620
24	0683			103	0141	148	0716
26,27	0755	61	0239	106,107	0755	149	0367
28	0716	62	0205	108	0716		
29	0367	63	0239	109	0367	151,152	0846
		65,66	0998			153	0574
31	0375	68	0716	111,112	0846	155-157	0574
32	0846	69	0686	113	0574	159	0370
33	0574			115-117	0574		
34	0608	71	0140	118	0842	162,163	0574
35-37	0574	72	0846	119	0755	164	0239
38	0842	73	0574			165-169	0574
39	0755	75-77	0574	122,123	0574		1033
		78,79	0724	125-129	0574		
41	0375				1033		
42,43	0574	81	0376	131	0374		
44	0608	82,83	0574	132	0282		
45-48 1033	0574	85-88 1033	0574	133	0574		
49	0755	89	0755	135	0620		





CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG | A-1210-22
B | REDRAWN | NO CHANGE
C | PPC-D | A-1233-22
D | 22-1715 | B-1233-22
(B25) J
(B9) SBUS(0-3)
(D9) SBUS(4-7)
(E9) UBUS(4-7)
(E9) UBUS(0-3)
(F9) SBUS(8-11)
(E9) SBUS(12-15)
(H9) UBUS(12-15)
(F9) UBUS(8-11)
U21
U31
U41
U51
U32C
U32D
U32A
U32B
U27
U26
U39
U89
U107
U106
U119
ENABLE
(D44) S←P
(D44) S←SP3
SP3(Ø-3) (C10)
SP3(4-7) (D10)
(E10) SP3(8-11)
(F10) SP3(12-15)
(B8) L
(D8) K
(E8) M
(G8) N
(B38) STA6
(B38) STA7
U63D
CC (C44)
+5V
R1 1K
R4 1K
R2 1K
U24A
U24C
U24B
U13A
U13C
U13B
U22A
U23A
U22B
U23B
U23C
SBUS(0-3)(B31)
UBUS(4-7)(G23)
UBUS(0-3)(B31)
SBUS(8-11)(A21)
SBUS(4-7)(A21)
SBUS(12-15)(A21)
UBUS(12-15)(G23)
UBUS(8-11)(G23)
MAP
P(0,1,2)
P(14,15)
BINARY-TO-OCTAL DECODER
U14
P1-22
P1-23
P1-21
P1-19
J1-49
J1-50
P-TO 1
P-TO 2
U-TO 1
U-TO 2
COM
MAP CIRCUITS
30001-60005
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SHEET 2-5
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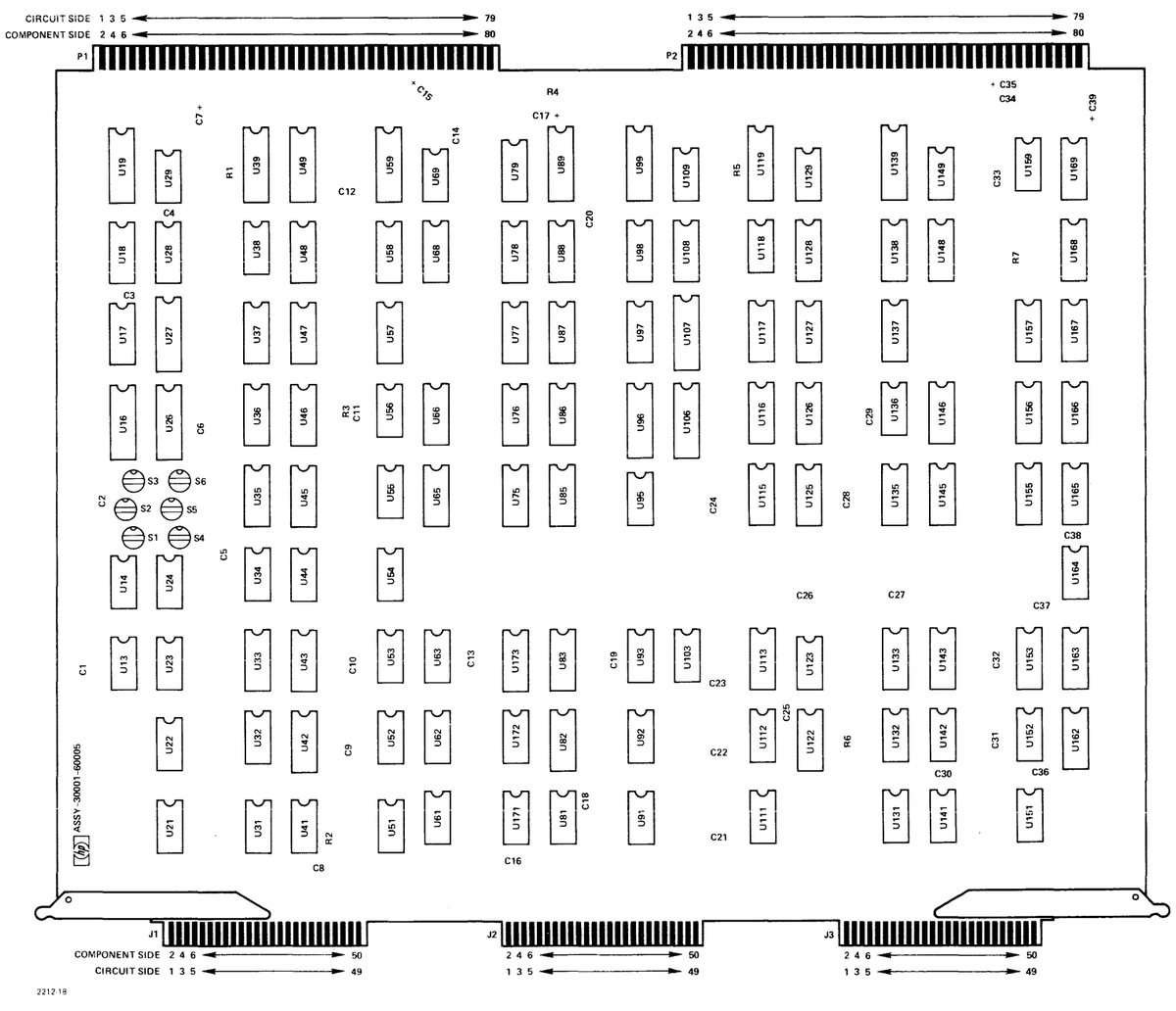
APPROVED
DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	ST00	1		1	XXX
2	COM	2	COM	2	XXX
3	S00	3	S08	3	XXX
4	S01	4	S09	4	XXX
5	S02	5	S10	5	XXX
6	S03	6	S11	6	XXX
7	INCP	7	U08	7	XXX
8	SP3IN	8	U09	8	XXX
9	U00	9	U10	9	XXX
10	U01	10	U11	10	XXX
11	U02	11		11	XXX
12	U03	12		12	XXX
13	SF00	13	MDPARITY	13	XXX
14	ST01	14		14	XXX
15	ST02	15	JUMPER01	15	XXX
16	SF01	16	PRTYMODE	16	XXX
17	SFQ0	17	JUMPER02	17	XXX
18	SF02	18		18	XXX
19	PT01	19		19	XXX
20	+5V	20	+5V	20	XXX
21	PT02	21	U12	21	XXX
22	UT02	22	U13	22	XXX
23	UT01	23	U14	23	XXX
24	PSELECT	24	U15	24	XXX
25	JUMPER01	25	COR10	25	XXX
26	JUMPER02	26	COR11	26	XXX
27	COR02	27	COR14	27	XXX
28	COR01	28	COR15	28	XXX
29	COR00	29	COR13	29	XXX
30		30		30	XXX
31	U04	31		31	XXX
32	U05	32		32	XXX
33	U06	33	S12	33	XXX
34	U07	34	S13	34	XXX
35	S04	35	S14	35	XXX
36	S05	36	S15	36	XXX
37	S06	37	CPUSEL	37	XXX
38	S07	38		38	XXX
39	COM	39	COM	39	XXX
40	COM	40	COM	40	XXX
41	RDSWITCH	41		41	XXX
42		42		42	XXX
43	STATUS04	43	MCUD08	43	XXX
44	STATUS05	44	MCUD09	44	XXX
45	STATUS06	45	MCUD10	45	XXX
46	STATUS07	46	MCUD11	46	XXX
47	STATUS00	47	MCUD12	47	XXX
48	STATUS01	48	MCUD13	48	XXX
49	STATUS02	49	MCUD14	49	XXX
50	STATUS03	50	MCUD15	50	XXX
51	TNAME00	51	SP315		
52	TNAME01	52			
53	MCUD01	53	RDCPX1		
54	MCUD00	54	RDCPX2		
55	MCUD03	55	RDMOD		
56	MCUD02	56	RORT16		
57	MCUD05	57	RDIOM		
58	MCUD04	58	RORT17		
59		59	CNTRMAX		
60	+5V	60	+5V		
61	MCUD06	61	INCTR		
62	MCUD07	62	REPN		
63		63	TR3		
64		64	TR2		
65		65	TR1		
66		66	RORT18		
67		67	TR0		
68		68	RORT19		
69		69	ST STATUS		
70	DISPIOP	70	—		
71	ST03	71	RDOPND		
72	ST04	72	RORT15		
73	NOP2	73	NXTDCD		
74		74	SFSAME		
75	SF03	75	OUP		
76	SF04	76	STIOM		
77	—	77	SP3SHIFT		
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0685	51	0375	91	0239	136	0690
14	0608	52	0373	92	0370	137,138	0574
16	0755	53	0205	93	0205	139	0755
17,18	0574	54	0367	95	0239		
19	0755	55	0424	96	0755	141	0141
		56	0690	97,98	0574	142	0282
21	0375	57-58	0574	99	0755	143	0574
22,23	0685	59	0755			145,146	0620
24	0683			103	0141	148	0716
26,27	0755	61	0239	106,107	0755	149	0367
28	0716	62	0205	108	0716		
29	0367	63	0239	109	0367	151,152	0846
		65,66	0998			153	0574
31	0375	68	0716	111,112	0846	155-157	0574
32	0846	69	0686	113	0574	159	0370
33	0574			115-117	0574		
34	0608	71	0140	118	0842	162,163	0574
35-37	0574	72	0846	119	0755	164	0239
38	0842	73	0574			165-169	0574
39	0755	75-77	0574	122,123	0574		1033
		78,79	0724	125-129	0574		
41	0375				1033		
42,43	0574	81	0376	131	0574		
44	0608	82,83	0574	132	0282		
45-48 1033	0574	85-88 1033	0574	133	0574		
49	0755	89	0755	135	0620		



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

COUNTER

(E19) SBUS(12-15)
(C19) SBUS(8-11)
(D44) S(10:15)←CNTR
(C19) SBUS(4-7)
(C44) CC
(E44) S(4:9)←CNTR

U62C, U72B, U72A, U72D, U72C, U131B, U131A, U141B, U111C, U111D, U112D, U112C, U111B, U111A, U112A, U112B, U152C, U152D, U151D, U151C, U152B, U152A, U151A, U151B

(J) (B13)

U143 4-BIT REGISTER (CLOCK, INPUT ENABLE, OUTPUT ENABLE) — CLK2 (B9)
U133 4-BIT REGISTER (CLOCK, INPUT ENABLE, OUTPUT ENABLE) — CLK3 (B9)

U145 DUAL 4-TO-1 MULTIPLEXER (STROBE B, STROBE A)
U135 DUAL 4-TO-1 MULTIPLEXER (STROBE B, STROBE A)
U146 DUAL 4-TO-1 MULTIPLEXER (STROBE B, STROBE A)

+5V, R6 1K

U132B, U132D, U142B, U132C, U142D, U142C, U141C, U141D

CNTRH/L
CNTRL

U164B, U159A, U159B, U159C

(C19) UBUS(4-7)
(E19) UBUS(8-11)
(E19) UBUS(12-15)

CNTRMAX — P2-59
ROR2(15) — P2-72
ROR2(16) — P2-56
ROR2(17) — P2-58
ROR2(18) — P2-66
ROR2(19) — P2-68
REPN — P2-62
INCTR — P2-61

STORE FIELD DECODER

(H33) $\overline{STQ3L}$
(B26) $\overline{STQ6}$
(H36) $\overline{STQ0L}$
(H35) $\overline{STQ2L}$
(H32) $\overline{STQ1L}$

U92B, U53A, U71A, U53B, U53C

P2-76 — $\overline{ST\ 10M}$
(B) (A44)
SBUS(4-7) (C31)

U78A 2-BIT DECODER (ENABLE)

U55F

P1-73 — NOP2B
P1-71 — ST3
P1-72 — ST4
SBUS(12-15) (E31)
SBUS(8-11) (D31)

U55C, U62B, U164A, U62A, U61C, U164C

P2-75 — QUP
P←UBUS (C8)
SP34←UBUS (C10)
(H32) $\overline{STQ4}$
(H39) $\overline{STQ5}$
$\overline{STQ1}$ (A3)
$\overline{STQ6}$ (B26)
$\overline{STQ7}$ (H36)
P2-69 — STATUS

BINARY-TO-OCTAL DECODER U44 (ENABLE)

UBUS(4-7) (D31)
UBUS(8-11) (E31)
UBUS(12-15) (F31)

ST2 — P1-15
ST1 — P1-14
ST0 — P1-1

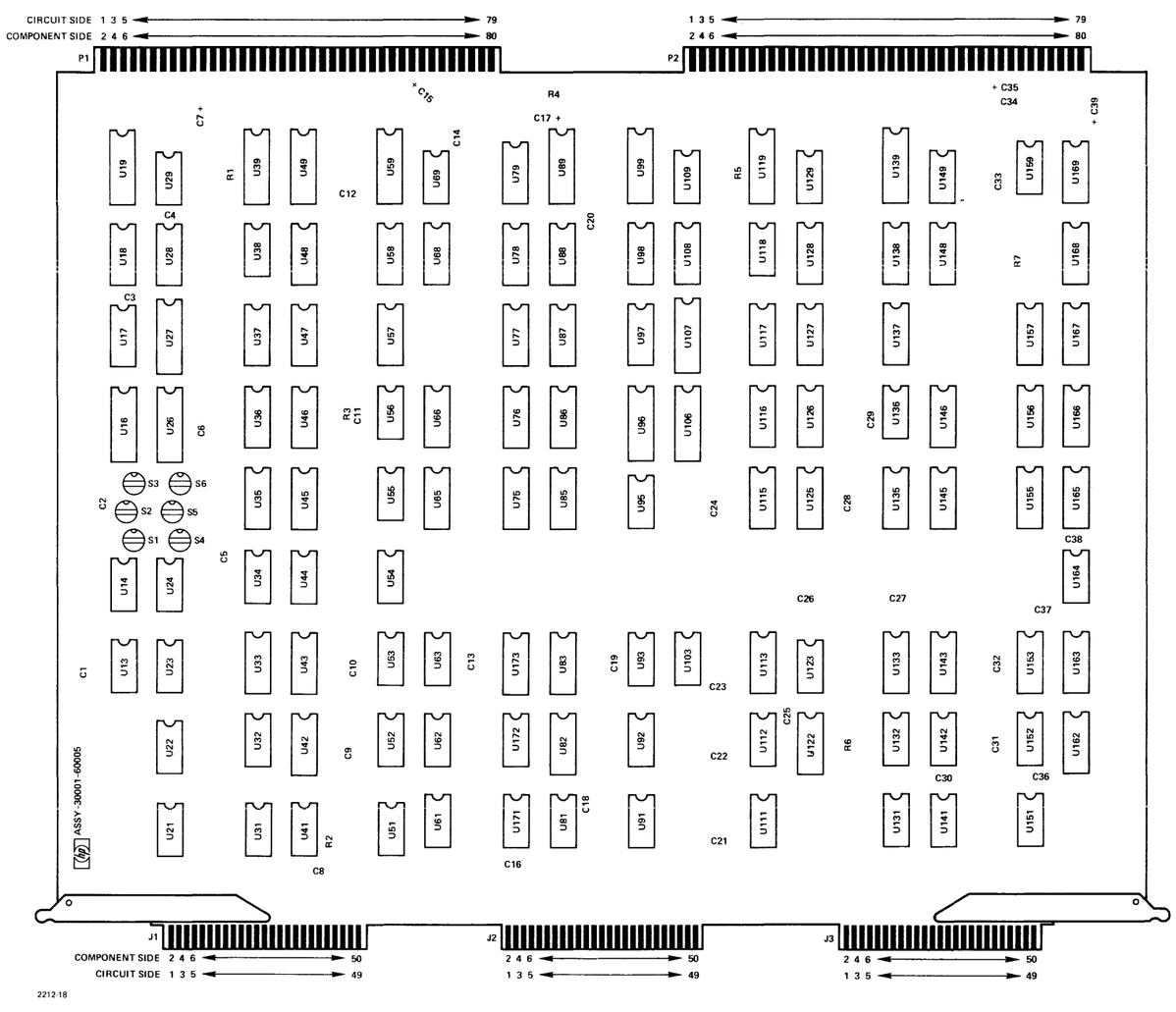
30001-60005 TITLE		SHEET 3-5
S BUS PCA		
ENGINEER	APPROVED	DATE
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	ST00	1		1	XXX
2	COM	2	COM	2	XXX
3	S00	3	S08	3	XXX
4	S01	4	S09	4	XXX
5	S02	5	S10	5	XXX
6	S03	6	S11	6	XXX
7	INCP	7	U08	7	XXX
8	SP3IN	8	U09	8	XXX
9	U00	9	U10	9	XXX
10	U01	10	U11	10	XXX
11	U02	11		11	XXX
12	U03	12		12	XXX
13	SF00	13	MDPARITY	13	XXX
14	ST01	14		14	XXX
15	ST02	15	JUMPER01	15	XXX
16	SF01	16	PRTYMODE	16	XXX
17	SFQ0	17	JUMPER02	17	XXX
18	SF02	18		18	XXX
19	PT01	19		19	XXX
20	+5V	20	+5V	20	XXX
21	PT02	21	U12	21	XXX
22	UT02	22	U13	22	XXX
23	UT01	23	U14	23	XXX
24	PSELECT	24	U15	24	XXX
25	JUMPER01	25	COR10	25	XXX
26	JUMPER02	26	COR11	26	XXX
27	COR02	27	COR14	27	XXX
28	COR01	28	COR15	28	XXX
29	COR00	29	COR13	29	XXX
30		30		30	XXX
31	U04	31		31	XXX
32	U05	32		32	XXX
33	U06	33	S12	33	XXX
34	U07	34	S13	34	XXX
35	S04	35	S14	35	XXX
36	S05	36	S15	36	XXX
37	S06	37	CPUSEL	37	XXX
38	S07	38		38	XXX
39	COM	39	COM	39	XXX
40	COM	40	COM	40	XXX
41	RDSWITCH	41		41	XXX
42		42		42	XXX
43	STATUS04	43	MCUD08	43	XXX
44	STATUS05	44	MCUD09	44	XXX
45	STATUS06	45	MCUD10	45	XXX
46	STATUS07	46	MCUD11	46	XXX
47	STATUS00	47	MCUD12	47	XXX
48	STATUS01	48	MCUD13	48	XXX
49	STATUS02	49	MCUD14	49	XXX
50	STATUS03	50	MCUD15	50	XXX
51	TNAME00	51	SP315		
52	TNAME01	52			
53	MCUD01	53	RDCPX1		
54	MCUD00	54	RDCPX2		
55	MCUD03	55	RDMOD		
56	MCUD02	56	RORT16		
57	MCUD05	57	RDIOM		
58	MCUD04	58	RORT17		
59		59	CNTRMAX		
60	+5V	60	+5V		
61	MCUD06	61	INCTR		
62	MCUD07	62	REPN		
63		63	TR3		
64		64	TR2		
65		65	TR1		
66		66	RORT18		
67		67	TR0		
68		68	RORT19		
69		69	ST STATUS		
70	DISPIOP	70			
71	ST03	71	RDOPND		
72	ST04	72	RORT15		
73	NOP2	73	NXTDCD		
74		74	SFSAME		
75	SF03	75	OUP		
76	SF04	76	STIOM		
77		77	SP3SHIFT		
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0685	51	0375	91	0239	136	0690
14	0608	52	0373	92	0370	137,138	0574
16	0755	53	0205	93	0205	139	0755
17,18	0574	54	0367	95	0239		
19	0755	55	0424	96	0755	141	0141
		56	0690	97,98	0574	142	0282
21	0375	57-58	0574	99	0755	143	0574
22,23	0685	59	0755			145,146	0620
24	0683			103	0141	148	0716
26,27	0755	61	0239	106,107	0755	149	0367
28	0716	62	0205	108	0716		
29	0367	63	0239	109	0367	151,152	0846
		65,66	0998			153	0574
31	0375	68	0716	111,112	0846	155-157	0574
32	0846	69	0686	113	0574	159	0370
33	0574			115-117	0574		
34	0608	71	0140	118	0842	162,163	0574
35-37	0574	72	0846	119	0755	164	0239
38	0842	73	0574			165-169	0574
39	0755	75-77	0574	122,123	0574		1033
		78,79	0724	125-129	0574		
41	0375				1033		
42,43	0574	81	0376	131	0574		
44	0608	82,83	0574	132	0282		
45-48 1033	0574	85-88 1033	0574	133	0574		
49	0755	89	0755	135	0620		



CHANGE	...
A	ORIG
B	REDRAWN
C	PPC-D
D	22-1715

...	
A-1233-22	
NO CHANGE	
A-1233-22	
B-1233-22	

(B19) SBUS(0-3)
(C19) UBUS(0-3)
(A9) CLKO
(B44) SFQ1LX
(B44) SFQ2LX
(B44) SFQ3LX
(C29) SBUS(4-7)
(G29) UBUS(4-7)
(B9) CLK1
(D29) SBUS(8-11)
(G29) UBUS(8-11)
(B9) CLK2
(D29) SBUS(12-15)
(G29) UBUS(12-15)
(B9) CLK3
(B44) SFQ0LX

STATUS 0 P1-47
STATUS 1 P1-48
STATUS 2 P1-49
STATUS 3 P1-50
STATUS 4 P1-43
STATUS 5 P1-44
STATUS 6 P1-45
STATUS 7 P1-46

STA6 (D16)
STA7 (D16)

SBUS(0-3)(A41)
UBUS(0-3)(B41)
SBUS(4-7)(B41)
UBUS(4-7)(C41)
SBUS(8-11)(D41)
UBUS(8-11)(D41)
SBUS(12-15)(F41)
UBUS(12-15)(F41)

U37 4-BIT REGISTER Q(0-3) D0D1D2D3
U36 4-BIT REGISTER DB(0-3) D0D1D2D3
U35 4-BIT REGISTER SM(0-3) D0D1D2D3
U33 4-BIT REGISTER DL(0-3) D0D1D2D3
U42 4-BIT REGISTER SP2(0-3) D0D1D2D3
U43 4-BIT REGISTER PB(0-3) D0D1D2D3
U77 4-BIT REGISTER Q(4-7) D0D1D2D3
U76 4-BIT REGISTER DB(4-7) D0D1D2D3
U75 4-BIT REGISTER SM(4-7) D0D1D2D3
U73 4-BIT REGISTER DL(4-7) D0D1D2D3
U82 4-BIT REGISTER SP2(4-7) D0D1D2D3
U83 4-BIT REGISTER PB(4-7) D0D1D2D3
U117 4-BIT REGISTER Q(8-11) D0D1D2D3
U116 4-BIT REGISTER DB(8-11) D0D1D2D3
U115 4-BIT REGISTER SM(8-11) D0D1D2D3
U113 4-BIT REGISTER DL(8-11) D0D1D2D3
U122 4-BIT REGISTER SP2(8-11) D0D1D2D3
U129 4-BIT REGISTER STA(8-11) D0D1D2D3
U123 4-BIT REGISTER PB(8-11) D0D1D2D3
U157 4-BIT REGISTER Q(12-15) D0D1D2D3
U156 4-BIT REGISTER DB(12-15) D0D1D2D3
U155 4-BIT REGISTER SM(12-15) D0D1D2D3
U153 4-BIT REGISTER DL(12-15) D0D1D2D3
U162 4-BIT REGISTER SP2(12-15) D0D1D2D3
U169 4-BIT REGISTER STA(12-15) D0D1D2D3
U163 4-BIT REGISTER PB(12-15) D0D1D2D3

U49 ENABLE
U63A
U103A
U103B
U103C
U103D

(G41) SFQ1L
(C26) STQ1L
(E27) STQ4
(D41) SFQ4
(G41) SFQ2L
(B26) STQ3L
(G41) SFQ3L
(C26) STQ2L
(G41) SFQ0L
(C26) STQ0L
(D41) SFQ7
(F29) STQ7
(E27) STQ5
(D41) SFQ5

30001-60005	TITLE	SHEET 4-5
	S BUS PCA	
ENGINEER	APPROVED	DATE

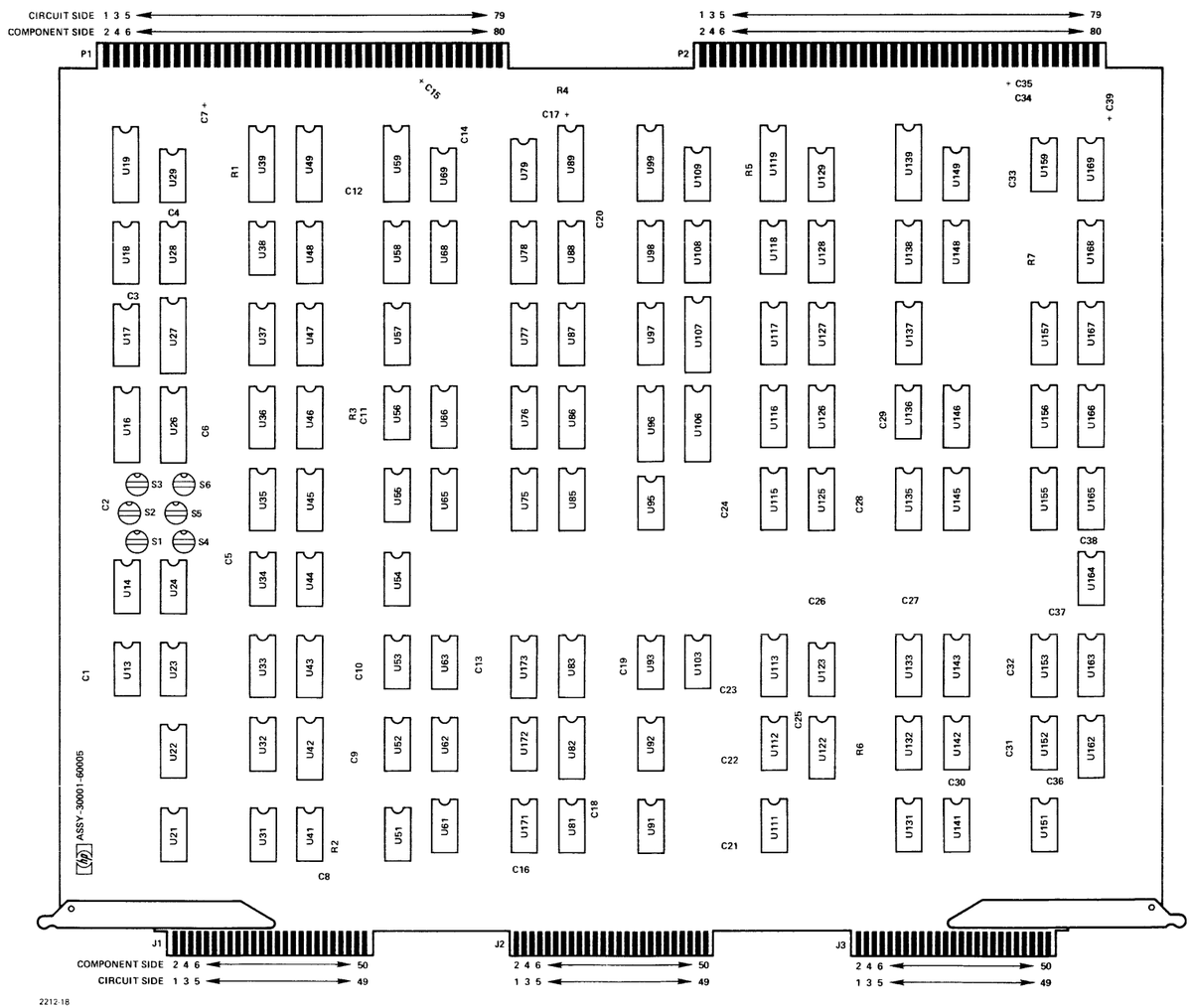
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL
1	ST00	1		1	XXX
2	COM	2	COM	2	XXX
3	S00	3	S08	3	XXX
4	S01	4	S09	4	XXX
5	S02	5	S10	5	XXX
6	S03	6	S11	6	XXX
7	INCP	7	U08	7	XXX
8	SP3IN	8	U09	8	XXX
9	U00	9	U10	9	XXX
10	U01	10	U11	10	XXX
11	U02	11		11	XXX
12	U03	12		12	XXX
13	SF00	13	MDPARITY	13	XXX
14	ST01	14		14	XXX
15	ST02	15	JUMPER01	15	XXX
16	SF01	16	PRTYMODE	16	XXX
17	SFQ0	17	JUMPER02	17	XXX
18	SF02	18		18	XXX
19	PT01	19		19	XXX
20	+5V	20	+5V	20	XXX
21	PT02	21	U12	21	XXX
22	UT02	22	U13	22	XXX
23	UT01	23	U14	23	XXX
24	PSELECT	24	U15	24	XXX
25	JUMPER01	25	COR10	25	XXX
26	JUMPER02	26	COR11	26	XXX
27	COR02	27	COR14	27	XXX
28	COR01	28	COR15	28	XXX
29	COR00	29	COR13	29	XXX
30		30		30	XXX
31	U04	31		31	XXX
32	U05	32		32	XXX
33	U06	33	S12	33	XXX
34	U07	34	S13	34	XXX
35	S04	35	S14	35	XXX
36	S05	36	S15	36	XXX
37	S06	37	CPUSEL	37	XXX
38	S07	38		38	XXX
39	COM	39	COM	39	XXX
40	COM	40	COM	40	XXX
41	RDSWITCH	41		41	XXX
42		42		42	XXX
43	STATUS04	43	MCUD08	43	XXX
44	STATUS05	44	MCUD09	44	XXX
45	STATUS06	45	MCUD10	45	XXX
46	STATUS07	46	MCUD11	46	XXX
47	STATUS00	47	MCUD12	47	XXX
48	STATUS01	48	MCUD13	48	XXX
49	STATUS02	49	MCUD14	49	XXX
50	STATUS03	50	MCUD15	50	XXX
51	TNAME00	51	SP315		
52	TNAME01	52			
53	MCUD01	53	RDCPX1		
54	MCUD00	54	RDCPX2		
55	MCUD03	55	RDMOD		
56	MCUD02	56	RORT16		
57	MCUD05	57	RDIOM		
58	MCUD04	58	RORT17		
59		59	CNTRMAX		
60	+5V	60	+5V		
61	MCUD06	61	INCTR		
62	MCUD07	62	REPN		
63		63	TR3		
64		64	TR2		
65		65	TR1		
66		66	RORT18		
67		67	TR0		
68		68	RORT19		
69		69	ST STATUS		
70	DISPIOP	70	—		
71	ST03	71	RDOPND		
72	ST04	72	RORT15		
73	NOP2	73	NXTDCD		
74		74	SFSAME		
75	SF03	75	QUP		
76	SF04	76	STIOM		
77	—	77	SP3SHIFT		
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0685	51	0375	91	0239	136	0690
14	0608	52	0373	92	0370	137,138	0574
16	0755	53	0205	93	0205	139	0755
17,18	0574	54	0367	95	0239		
19	0755	55	0424	96	0755	141	0141
		56	0690	97,98	0574	142	0282
21	0375	57-58	0574	99	0755	143	0574
22,23	0685	59	0755			145,146	0620
24	0683			103	0141	148	0716
26,27	0755	61	0239	106,107	0755	149	0367
28	0716	62	0205	108	0716		
29	0367	63	0239	109	0367	151,152	0846
		65,66	0998			153	0574
31	0375	68	0716	111,112	0846	155-157	0574
32	0846	69	0686	113	0574	159	0370
33	0574			115-117	0574		
34	0608	71	0140	118	0842	162,163	0574
35-37	0574	72	0846	119	0755	164	0239
38	0842	73	0574			165-169	0574
39	0755	75-77	0574	122,123	0574		1033
		78,79	0724	125-129	~~0574~~ 1033		
41	0375						
42,43	0574	81	0376	131	0374		
44	0608	82,83	0574	132	0282		
45-48 1033	~~0574~~	85-88 1033	~~0574~~	133	0574		
49	0755	89	0755	135	0620		



1209A-2 | 1209B-2 | 1209C-2

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1233-22
D	22-1715	B-1233-22

S'BUS FIELD DECODER

(B40) SBUS(0-3)
(G49) SF4
(G49) SF3
(G5) NXTDCD
2-BIT DECODER U79B
$\overline{SFQ0L}$ X(C35)
$\overline{SFQ1L}$ X(C31)
$\overline{SFQ2L}$ X(C31)
$\overline{SFQ3L}$ X(C31)
(C40) SBUS(4-7)
(B40) UBUS(0-3)
(A9) CLK0
(G48) SF0
(F48) SF1
U52A
U61A
U95A
CC (B21) (C17)
U95C
U← SBUS (C5)
(D40) UBUS(4-7)
(B9) CLK1
(E40) SBUS(8-11)
(H32) $\overline{SFQ4}$
(H36) $\overline{SFQ7}$
(H39) $\overline{SFQ5}$
U61D
U164D
U93C
S(10:15)← CNTR (A21)
S(0:7)← Ø (C6)
U95D
S← SP3 (C15)
$\overline{RDIOM}$ ← P2-57
$\overline{SFQ0}$ ← P1-17
(E40) UBUS(8-11)
(B9) CLK2
(F40) SBUS(12-15)
BINARY-TO-OCTAL DECODER U34
NXTDCD (G5)
U95B
S(8:15)← Ø (G6)
U63C
S(4:9)← CNTR (B22)
(F40) UBUS(12-15)
(B9) CLK3
U24E
$\overline{SF2}$ (F48)
SF1 ← P1-16
U61B
U91B
U91A
U52B
SF2 ← P1-18
SF0 ← P1-13
U91D
U91C
$\overline{SFQ0L}$ (H36)
$\overline{SFQ1L}$ (H32)
$\overline{SFQ2L}$ (H33)
$\overline{SFQ3L}$ (H35)
P2-71 $\overline{RDOPND}$
P1-41 RDSWITCH
P2-54 RDCPX2
P2-55 RDMOD
P2-53 RDCPX1
P2-74 SFSAME
P2-67 $\overline{TRO}$
P2-65 $\overline{TR1}$
P2-64 $\overline{TR2}$

(B29) Ⓑ

U45 4-BIT REGISTER — TROS(0-3) — P1-3 SBUS0, P1-4 SBUS1, P1-5 SBUS2, P1-6 SBUS3
U46 4-BIT REGISTER — TR1S(0-3)
U47 4-BIT REGISTER — TR2S(0-3)
U48 4-BIT REGISTER — TR3S(0-3)
U85 4-BIT REGISTER — TROS(4-7) — P1-35 SBUS4, P1-36 SBUS5, P1-37 SBUS6, P1-38 SBUS7
U86 4-BIT REGISTER — TR1S(4-7)
U87 4-BIT REGISTER — TR2S(4-7)
U88 4-BIT REGISTER — TR3S(4-7)
U125 4-BIT REGISTER — TROS(8-11) — P2-3 SBUS8, P2-4 SBUS9, P2-5 SBUS10, P2-6 SBUS11
U126 4-BIT REGISTER — TR1S(8-11)
U127 4-BIT REGISTER — TR2S(8-11)
U128 4-BIT REGISTER — TR3S(8-11)
U165 4-BIT REGISTER — TROS(12-15) — P2-33 SBUS12, P2-34 SBUS13, P2-35 SBUS14, P2-36 SBUS15, P2-63 TR3
U166 4-BIT REGISTER — TR1S(12-15)
U167 4-BIT REGISTER — TR2S(12-15)
U168 4-BIT REGISTER — TR3S(12-15)

U65 DUAL 4-TO-1 MULTIPLEXER — $\overline{SF(TR1)}$ $\overline{SF(TR0)}$ — STROBE B, STROBE A
U66 DUAL 4-TO-1 MULTIPLEXER — $\overline{SF(TR3)}$ $\overline{SF(TR2)}$ — STROBE B, STROBE A

P1-52 TNAME 1
P1-51 TNAME 0
(C41) SF1
(F44) $\overline{SF2}$
(B41) SF0
U81A
U53D
U55E
+5V
XX 1K
P1-70 $\overline{DISPIOP}$
U79A 2-BIT DECODER
SF4 (B41) → P1-76 SF4
SF3 (B41) → P1-75 SF3
NXTDCD (G5)

30001-60005 S BUS PCA — SHEET 5-5
ENGINEER | APPROVED | DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-205

CURRENT INSTRUCTION REGISTER (CIR) PCA

30001-60006

SERIES 1210

1305

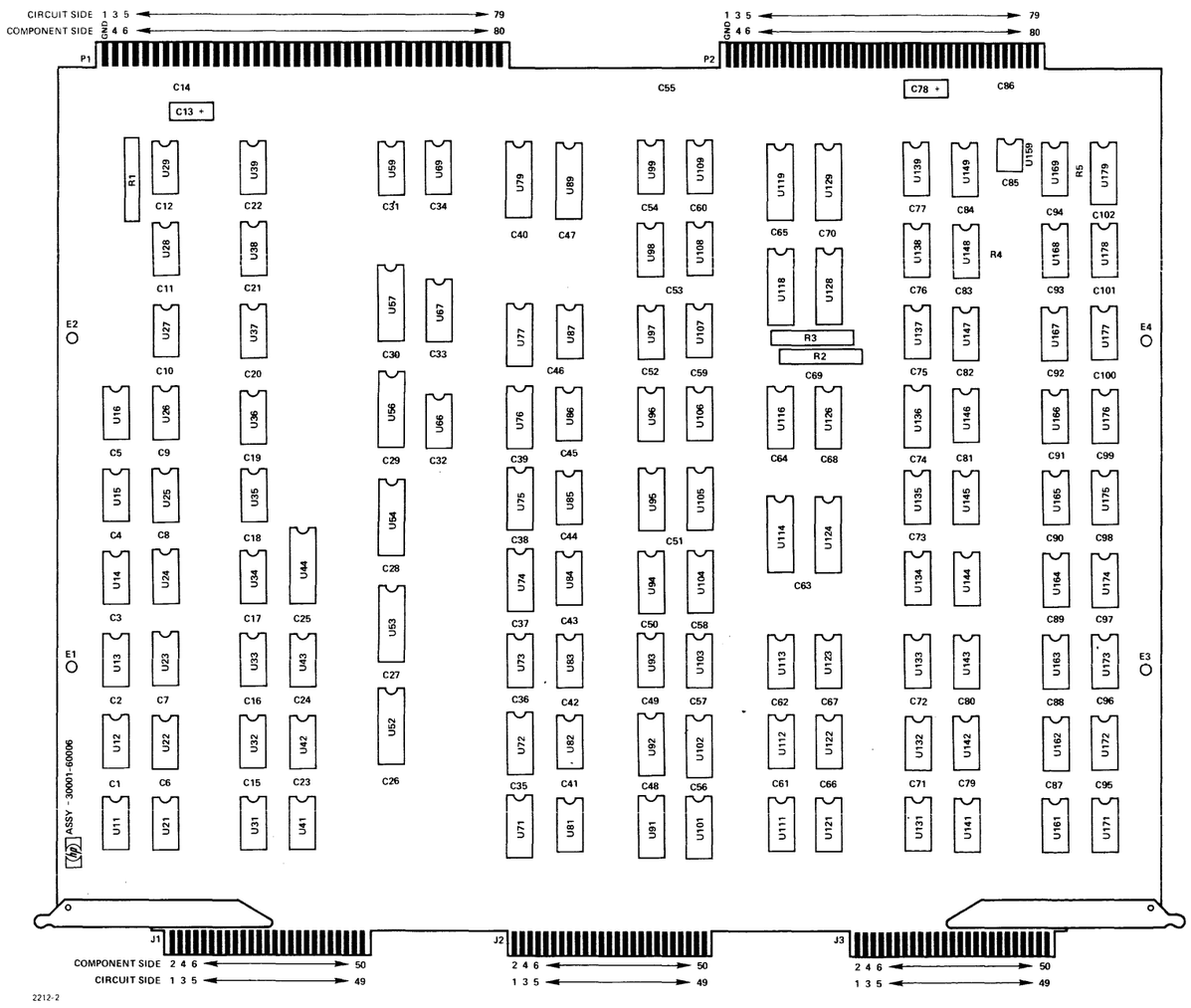
REV C

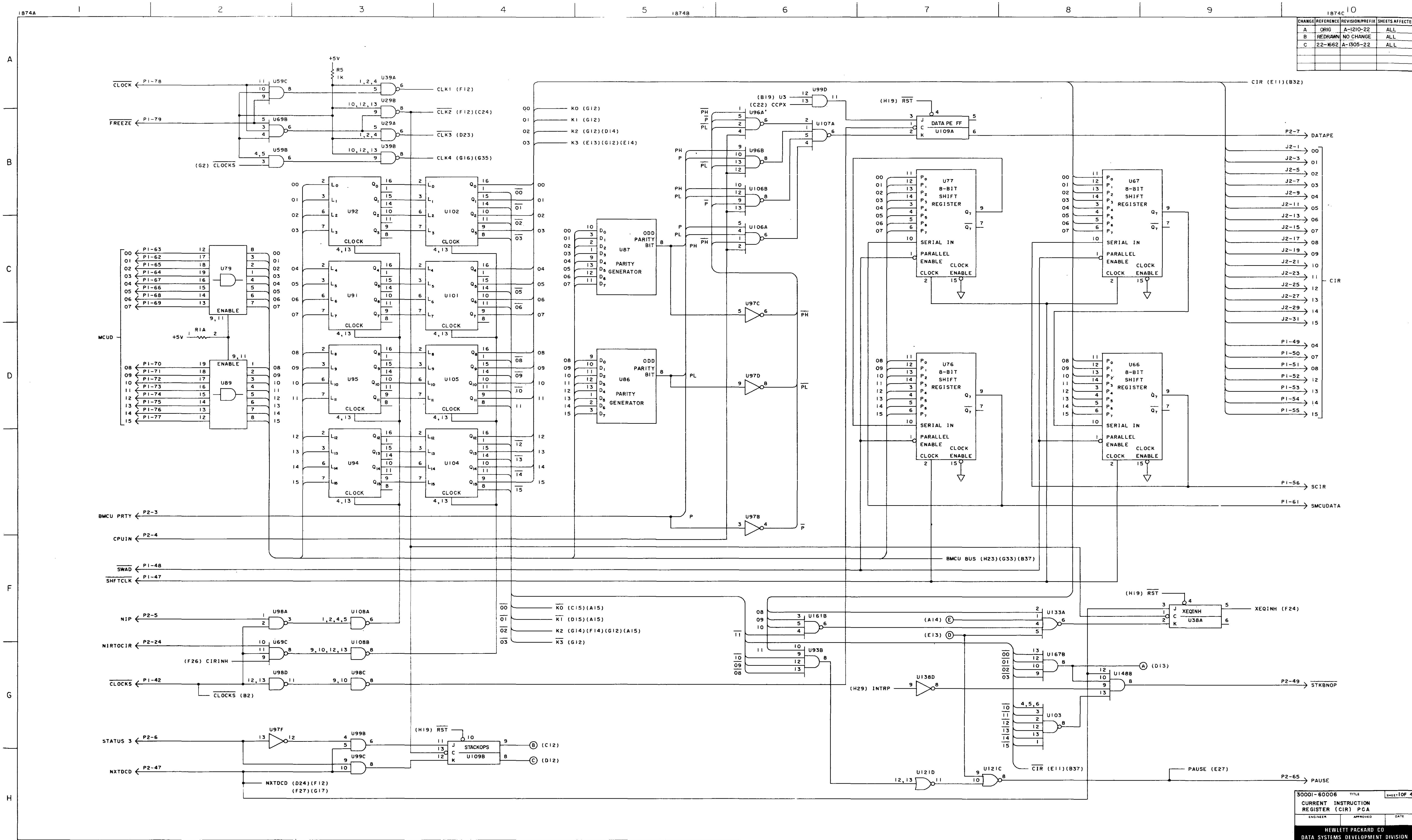
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL
1	DSPFLAG	1	OPINP	1	GND	1	CIR00
2	COM	2	COM	2	SW00	2	—
3	CPURSTS	3	BMCUPRTY	3	SW01	3	CIR01
4	IORSTSW	4	CPUIN	4	GND	4	—
5	MCUHINT	5	NIP	5	SW02	5	CIR02
6	HALT	6	STATUS03	6	SW03	6	—
7	MCUCMP	7	DATAPE	7	GND	7	CIR03
8	CMPRFF	8	V00	8	SW04	8	—
9	EXTINT	9	V01	9	SW05	9	CIR04
10	MCUINT	10	V02	10	GND	10	—
11	PWRFAIL	11	V03	11	SW06	11	CIR05
12	MODINT	12	V04	12	SW07	12	—
13	RUNFF	13	V05	13	GND	13	CIR06
14	INTRP	14	V06	14	SW08	14	—
15	STATUS04	15	V07	15	SW09	15	CIR07
16	STATUS01	16	V08	16	GND	16	—
17	CCPX	17	V09	17	SW10	17	CIR08
18	STATUS02	18	V10	18	SW11	18	—
19	FPNLOS	19	V11	19	GND	19	CIR09
20	+5V	20	+5V	20	SW12	20	—
21	RMCUCPX1	21	STORAR	21	SW13	21	CIR10
22	BNDV	22	SWLDRAR	22	GND	22	—
23	MCUCMPL	23	U00	23	SW14	23	CIR11
24	MCUCMPH	24	NIRTOCIR	24	SW15	24	—
25	RDCPX1	25		25	GND	25	CIR12
26	S00	26	U03	26	RSTSWIO	26	—
27	S01	27	U04	27	RSTSWCP	27	CIR13
28	S02	28	U05	28	GND	28	—
29	S03	29	U06	29	CLDLOAD	29	CIR14
30		30		30	CR UNFF	30	—
31	S04	31	U07	31	GND	31	CIR15
32	S05	32	U08	32	CONSINT	32	—
33	S06	33	U09	33	LOADREG	33	—
34	S07	34	U10	34	GND	34	—
35	S08	35	U11	35	DISPMEM	35	LUTA00
36	S09	36	U12	36	LOADMEM	36	—
37	S10	37	U13	37	GND	37	LUTA01
38	S11	38	U14	38	XEQ SW	38	—
39	COM	39	COM	39	SNGINST	39	LUTA02
40	COM	40	COM	40	GND	40	—
41	S12	41	U15	41	INHINTR	41	LUTA03
42	CLOCKS	42		42	ENBINTH	42	—
43	S13	43		43	BKPT HALT	43	LUTA04
44	S14	44	SPV	44	SYSDUMP	44	—
45	S15	45	NOP	45	RUN	45	LUTA05
46	RDCIR	46		46	INHAR	46	—
47	SHFTCLK	47	NXTDCD	47	INCRADD	47	LUTA06
48	SLOAD	48		48	DECRADD	48	—
49	CIR04	49	STKBNOP	49	SYSHALT	49	LUTA07
50	CIR07	50		50	—	50	—
51	CIR08	51	SR01				
52	CIR12	52					
53	CIR13	53					
54	CIR14	54					
55	CIR15	55	W				
56	SCIR	56					
57	RDCPX2	57	LUTGATE				
58	RDSWITCH	58					
59	RDOPND	59					
60	+5V	60	+5V				
61	SMCUDATA	61	SR00				
62	MCUD01	62					
63	MCUD00	63	JBNDV				
74	MCUD03	64					
65	MCUD02	65	PAUSE				
66	MCUD05	66					
67	MCUD04	67	PADDIN09				
68	MCUD06	68	INDIRECT				
69	MCUD07	69	PWR ONB				
70	MCUD08	70	DS				
71	MCUD09	71	QS				
72	MCUD10	72	PADDIN11				
73	MCUD11	73	PADDIN10				
74	MCUD12	74	PADDIN08				
75	MCUD13	75	PADDXS00				
76	MCUD14	76	PADDXS01				
77	MCUD15	77	PADDSUB				
78	CLOCK	78	CPURST				
79	FREEZE	79	PADDX				
80	COM	80	COM				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0370	41	0375	96	0688	132	0373	168	0376
12	0696	42	0424	97	0683	133	0837	169	0512
13	0688	43	0846	98	0681	134	0375		
14	0371	44	0755	99	0141	135	0379	171	0374
15	0372	52-54	0755			137	0846	172	0373
16	0374	56,57	0755	101,102	0301	138	0424	173	0375
		59	0686	103	0375	139	0837	174	0373
21	0691			104,105	0301			175,176	0371
22	0372	66,67	0262	106,107	0688	141	0371	177	0374
23	0696	69	0685	108	0690	142	0205	178	0370
24	0380	71,72	0574	109	0695	143	0370	179	0574
25	0205	73	0837			144	0371		
26	0370	74,75	0574	111	0282	145	0379		
27,28	0696	76,77	0262	112	0371	146	0370		
29	0690	79	0759	113	0376	147	0239		
				114	0755	148	0274		
31	0239	81,82	0282	118,119	0755	149	0141		
32	0370	83	0837						
33	0239	84,85	0282	121	0239	159	0535		
34	0141	86,87	0842	122	0371	161	0371		
35	0372	89	0759	123	0373	162	0141		
36	0382			124	0755	163	0301		
37	0141	91,92	0301	128,129	0755	164	0371		
38	0695	93	0374			165	0379		
39	0690	94,95	0301	131	0371	166	0372		
						167	0374		





CHANGE | REFERENCE | REVISION/PREFIX | SHEETS AFFECTED
A | ORIG | A-1210-22 | ALL
B | REDRAWN | NO CHANGE | ALL
C | 22-1662 | A-1305-22 | ALL
CLOCK
FREEZE
(G2) CLOCKS
CLK1 (F12)
CLK2 (F12)(C24)
CLK3 (D23)
CLK4 (G16)(G35)
K0 (G12)
K1 (G12)
K2 (G12)(D14)
K3 (E13)(G12)(E14)
MCUD
ENABLE
U87 PARITY GENERATOR
U86 PARITY GENERATOR
DATA PE FF U109A
U77 8-BIT SHIFT REGISTER
U76 8-BIT SHIFT REGISTER
U67 8-BIT SHIFT REGISTER
U66 8-BIT SHIFT REGISTER
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE
CIR (E11)(B32)
DATAPE
CIR
SCIR
SMCUDATA
BMCU PRTY
CPUIN
SWAD
SHFTCLK
BMCU BUS (H23)(G33)(B37)
NIP
NIRTOCIR
(F26) CIRINH
CLOCKS
CLOCKS (B2)
STATUS 3
NXTDCD
NXTDCD (D24)(F12) (F27)(G17)
(H19) RST
STACKOPS U109B
K0 (C15)(A15)
K1 (D15)(A15)
K2 (G14)(F14)(G12)(A15)
K3 (G12)
XEQINH U38A
XEQINH (F24)
(H29) INTRP
STKBNOP
CIR (E11)(B37)
PAUSE (E27)
PAUSE
30001-60006
CURRENT INSTRUCTION REGISTER (CIR) PCA
SHEET 1 OF 4
ENGINEER
APPROVED
DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1

PIN	SIGNAL
1	DSPFLAG
2	COM
3	CPURSTS
4	IORSTSW
5	MCUHINT
6	HALT
7	MCUCMP
8	CMPRFF
9	EXTINT
10	MCUINT
11	PWRFAIL
12	MODINT
13	RUNFF
14	INTRP
15	STATUS04
16	STATUS01
17	CCPX
18	STATUS02
19	FPNLOS
20	+5V
21	RMCUCPX1
22	BNDV
23	MCUCMPL
24	MCUCMPH
25	RDCPX1
26	S00
27	S01
28	S02
29	S03
30	
31	S04
32	S05
33	S06
34	S07
35	S08
36	S09
37	S10
38	S11
39	COM
40	COM
41	S12
42	CLOCKS
43	S13
44	S14
45	S15
46	RDCIR
47	SHFTCLK
48	SLOAD
49	CIR04
50	CIR07
51	CIR08
52	CIR12
53	CIR13
54	CIR14
55	CIR15
56	SCIR
57	RDCPX2
58	RDSWITCH
59	RDOPND
60	+5V
61	SMCUDATA
62	MCUD01
63	MCUD00
74	MCUD03
65	MCUD02
66	MCUD05
67	MCUD04
68	MCUD06
69	MCUD07
70	MCUD08
71	MCUD09
72	MCUD10
73	MCUD11
74	MCUD12
75	MCUD13
76	MCUD14
77	MCUD15
78	CLOCK
79	FREEZE
80	COM

P2

PIN	SIGNAL
1	OPINP
2	COM
3	BMCUPRTY
4	CPUIN
5	NIP
6	STATUS03
7	DATAPE
8	V00
9	V01
10	V02
11	V03
12	V04
13	V05
14	V06
15	V07
16	V08
17	V09
18	V10
19	V11
20	+5V
21	STORAR
22	SWLDRAR
23	U00
24	NIRTOCIR
25	
26	U03
27	U04
28	U05
29	U06
30	
31	U07
32	U08
33	U09
34	U10
35	U11
36	U12
37	U13
38	U14
39	COM
40	COM
41	U15
42	
43	
44	SPV
45	NOP
46	
47	NXTDCD
48	
49	STKBNOP
50	
51	SR01
52	
53	
54	
55	W
56	
57	LUTGATE
58	
59	
60	+5V
61	SR00
62	
63	JBNDV
64	
65	PAUSE
66	
67	PADDIN09
68	INDIRECT
69	PWR ONB
70	DS
71	QS
72	PADDIN11
73	PADDIN10
74	PADDIN08
75	PADDXS00
76	PADDXS01
77	PADDSUB
78	CPURST
79	PADDX
80	COM

J1

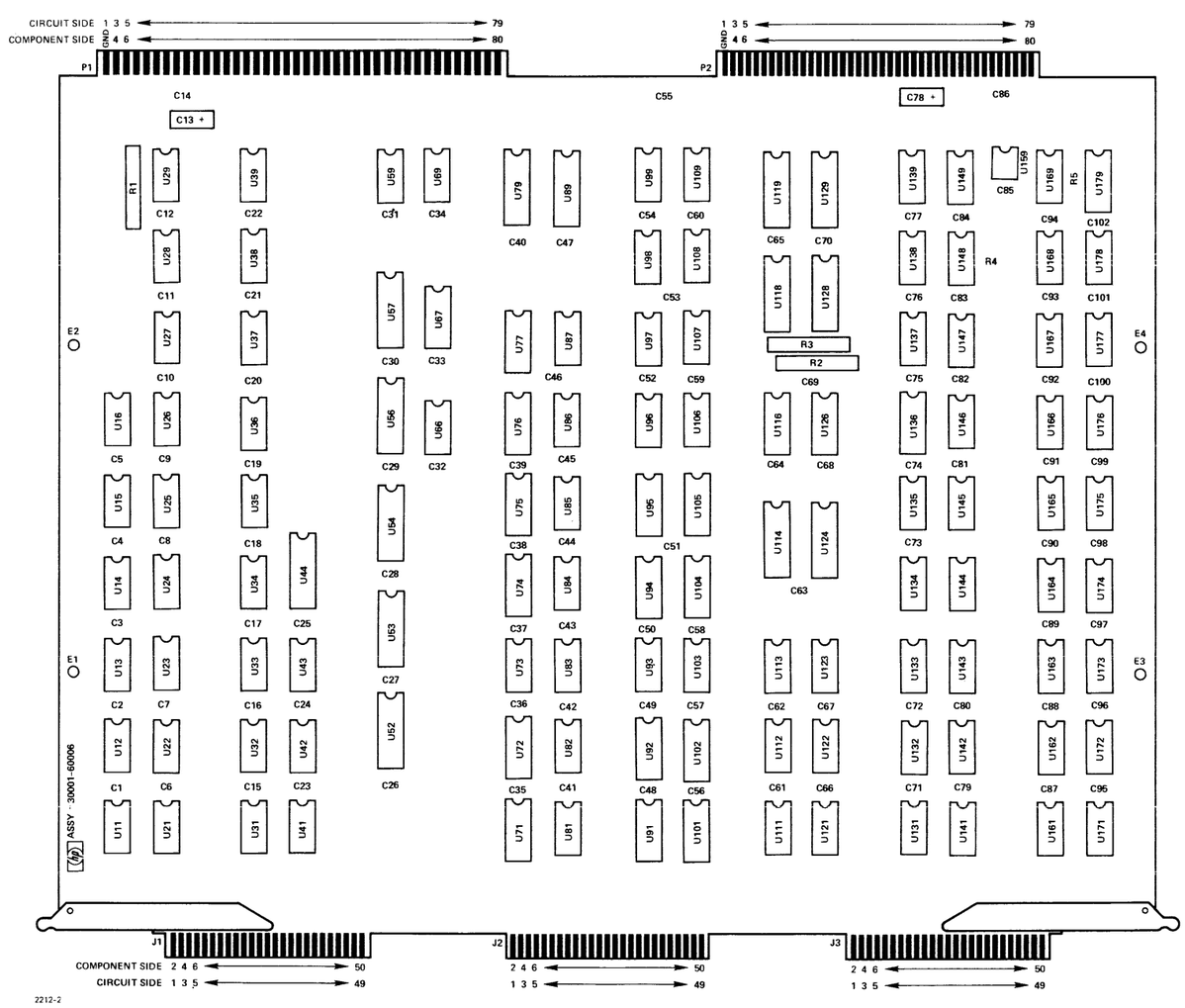
PIN	SIGNAL
1	GND
2	SW00
3	SW01
4	GND
5	SW02
6	SW03
7	GND
8	SW04
9	SW05
10	GND
11	SW06
12	SW07
13	GND
14	SW08
15	SW09
16	GND
17	SW10
18	SW11
19	GND
20	SW12
21	SW13
22	GND
23	SW14
24	SW15
25	GND
26	RSTSWIO
27	RSTSWCP
28	GND
29	CLDLOAD
30	CR UNFF
31	GND
32	CONSINT
33	LOADREG
34	GND
35	DISPMEM
36	LOADMEM
37	GND
38	XEQ SW
39	SNGINST
40	GND
41	INHINTR
42	ENBINTH
43	BKPT HALT
44	SYSDUMP
45	RUN
46	INHAR
47	INCRADD
48	DECRADD
49	SYSHALT
50	—

J2

PIN	SIGNAL
1	CIR00
2	—
3	CIR01
4	—
5	CIR02
6	—
7	CIR03
8	—
9	CIR04
10	—
11	CIR05
12	—
13	CIR06
14	—
15	CIR07
16	—
17	CIR08
18	—
19	CIR09
20	—
21	CIR10
22	—
23	CIR11
24	—
25	CIR12
26	—
27	CIR13
28	—
29	CIR14
30	—
31	CIR15
32	—
33	—
34	—
35	LUTA00
36	—
37	LUTA01
38	—
39	LUTA02
40	—
41	LUTA03
42	—
43	LUTA04
44	—
45	LUTA05
46	—
47	LUTA06
48	—
49	LUTA07
50	—

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0370	41	0375	96	0688	132	0373	168	0376
12	0696	42	0424	97	0683	133	0837	169	0512
13	0688	43	0846	98	0681	134	0375		
14	0371	44	0755	99	0141	135	0379	171	0374
15	0372	52-54	0755			137	0846	172	0373
16	0374	56,57	0755	101,102	0301	138	0424	173	0375
		59	0686	103	0375	139	0837	174	0373
21	0691			104,105	0301			175,176	0371
22	0372	66,67	0262	106,107	0688	141	0371	177	0374
23	0696	69	0685	108	0690	142	0205	178	0370
24	0380	71,72	0574	109	0695	143	0370	179	0574
25	0205	73	0837			144	0371		
26	0370	74,75	0574	111	0282	145	0379		
27,28	0696	76,77	0262	112	0371	146	0370		
29	0690	79	0759	113	0376	147	0239		
				114	0755	148	0274		
31	0239	81,82	0282	118,119	0755	149	0141		
32	0370	83	0837						
33	0239	84,85	0282	121	0239	159	0535		
34	0141	86,87	0842	122	0371	161	0371		
35	0372	89	0759	123	0373	162	0141		
36	0382			124	0755	163	0301		
37	0141	91,92	0301	128,129	0755	164	0371		
38	0695	93	0374			165	0379		
39	0690	94,95	0301	131	0371	166	0372		
						167	0374		



1875A

1875C

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22

LUTGATE P2-57

SR1 P2-51
SRO P2-61

U P2-26 P2-27 P2-28 P2-29 P2-31 P2-32 P2-33 P2-34 P2-35 P2-36 P2-37 P2-38 P2-41

U178A U138F U138A (E) (F7)

U147D U148A U142D SRA 01

U147B U146A U146B U133B SPECOP (C37) K5 (F13)

U124 ENABLE (G4) (B) 9,11

U172B K5

U114 ENABLE (H4) (C) 9,11 K7 K6 (G13)(F14)

U149D (G9) (A) (G13) K7

U166B U166C

(H8) CIR (A9) CIR

U179 W-BIT REGISTER CLOCK CLEAR OUTPUT ENABLE INPUT ENABLE

U149A (A4) CLK1 (B4) CLK2 (H2) NXTDCD

U131B K3 (B5) (F7)

U144C U143B U144A U143A U144B U134 K0 (F4)

U164C U164A U164B U174A K1 (F4)

U135D U135B U135E U135A U135C (B5) K2

U145D U145B U145E U145A U145C (B5) K3

U165A U165B U165E U165D U165C (F4) K2 (D13) K6

U163D U163B

(F39) AA (C13) K5

U177A U177B U174B

U147C U146D K7 (D13) CC (E38)

U176C (B5) K2 (A5) KO (F4) K3

U176B K6 (D13) DD (C37)

U107B (A5) KO (B5) K1 (B5) K3 (F4) K2 BB (E38)

U178B 4,5

U175C U163C U175B U175A (F4) K2

U167A (F4) K0 (F4) K1 (F4) K2

U137A

U136 4X256 ROM ENABLE

U126 4X256 ROM ENABLE

U116 4X256 ROM ENABLE

R4 1K +5V

U118 ENABLE 9,11

U128 ENABLE

U129 ENABLE

U119 ENABLE 9,11

03 U3 (A6)
09 U9 (B22)
10 U10 (C23)
13 U13 (B28)
15 U15 (C27)(B22)

J2-35 J2-37 J2-39 J2-41 J2-43 J2-45 J2-47 J2-49 — LUTA

R3A R3B R2A R2D R3C R3D R2E R3E +5V

P2-8 P2-9 P2-10 P2-11 P2-12 P2-13 P2-14 P2-15

R3G R2G R3F R2F +5V

P2-16 P2-17 P2-18 P2-19 — V

SRA 01

P2-68 INDIRECT
WF (E39)(C38) P2-65 W
P2-70 DS
P2-71 OS

R5 1K +5V

CPU RESET DLY U169A

CLK 4 (B4)

ABC (F27)

PON U169B

(H29) INTRP (H2) NXTDCD

U178D U178C U149C U138B

U147A U138C U139A U139B R1F 1K +5V

P2-44 SPV
P2-45 NOP

R3A 1K +5V

U159B 6,7

SWLDRAR P2-22
JBNDV P2-63

STORAR P2-21
PWR ONB P2-69
CPURST P2-78

RST (A7)(F9)(G4)(A23)

30001-60006 TITLE CURRENT INSTRUCTION REGISTER (CIR) PCA

SHEET 2 OF 4

ENGINEER | APPROVED | DATE

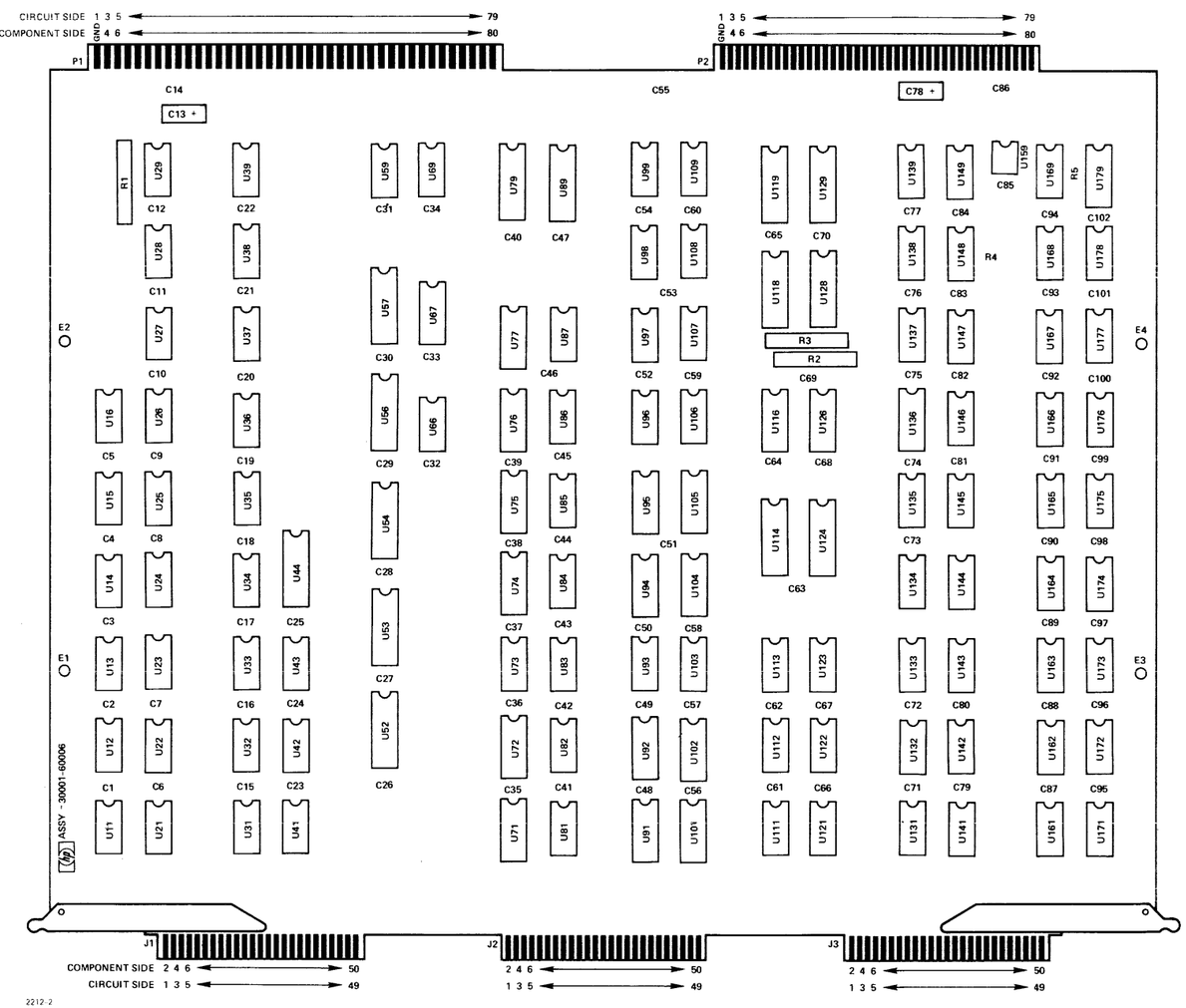
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

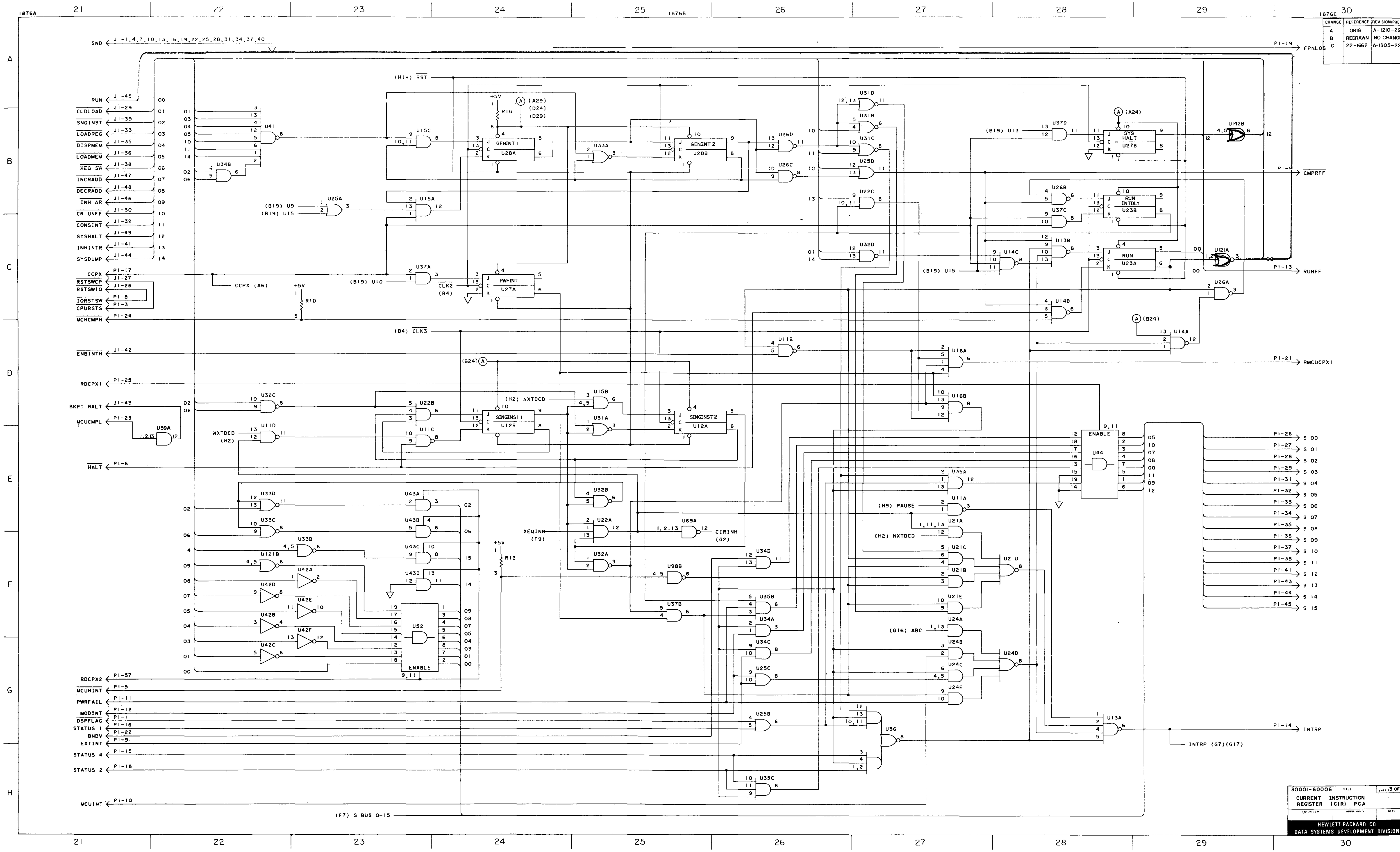
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL
1	DSPFLAG	1	OPINP	1	GND	1	CIR00
2	COM	2	COM	2	SW00	2	—
3	CPURSTS	3	BMCUPRTY	3	SW01	3	CIR01
4	IORSTSW	4	CPUIN	4	GND	4	—
5	MCUHINT	5	NIP	5	SW02	5	CIR02
6	HALT	6	STATUS03	6	SW03	6	—
7	MCUCMP	7	DATAPE	7	GND	7	CIR03
8	CMPRFF	8	V00	8	SW04	8	—
9	EXTINT	9	V01	9	SW05	9	CIR04
10	MCUINT	10	V02	10	GND	10	—
11	PWRFAIL	11	V03	11	SW06	11	CIR05
12	MODINT	12	V04	12	SW07	12	—
13	RUNFF	13	V05	13	GND	13	CIR06
14	INTRP	14	V06	14	SW08	14	—
15	STATUS04	15	V07	15	SW09	15	CIR07
16	STATUS01	16	V08	16	GND	16	—
17	CCPX	17	V09	17	SW10	17	CIR08
18	STATUS02	18	V10	18	SW11	18	—
19	FPNLOS	19	V11	19	GND	19	CIR09
20	+5V	20	+5V	20	SW12	20	—
21	RMCUCPX1	21	STORAR	21	SW13	21	CIR10
22	BNDV	22	SWLDRAR	22	GND	22	—
23	MCUCMPL	23	U00	23	SW14	23	CIR11
24	MCUCMPH	24	NIRTOCIR	24	SW15	24	—
25	RDCPX1	25		25	GND	25	CIR12
26	S00	26	U03	26	RSTSWIO	26	—
27	S01	27	U04	27	RSTSWCP	27	CIR13
28	S02	28	U05	28	GND	28	—
29	S03	29	U06	29	CLDLOAD	29	CIR14
30		30		30	CR UNFF	30	—
31	S04	31	U07	31	GND	31	CIR15
32	S05	32	U08	32	CONSINT	32	—
33	S06	33	U09	33	LOADREG	33	—
34	S07	34	U10	34	GND	34	—
35	S08	35	U11	35	DISPMEM	35	LUTA00
36	S09	36	U12	36	LOADMEM	36	—
37	S10	37	U13	37	GND	37	LUTA01
38	S11	38	U14	38	XEQ SW	38	—
39	COM	39	COM	39	SNGINST	39	LUTA02
40	COM	40	COM	40	GND	40	—
41	S12	41	U15	41	INHINTR	41	LUTA03
42	CLOCKS	42		42	ENBINTH	42	—
43	S13	43		43	BKPT HALT	43	LUTA04
44	S14	44	SPV	44	SYSDUMP	44	—
45	S15	45	NOP	45	RUN	45	LUTA05
46	RDCIR	46		46	INHAR	46	—
47	SHFTCLK	47	NXTDCD	47	INCRADD	47	LUTA06
48	SLOAD	48		48	DECRADD	48	—
49	CIR04	49	STKBNOP	49	SYSHALT	49	LUTA07
50	CIR07	50		50	—	50	—
51	CIR08	51	SR01				
52	CIR12	52					
53	CIR13	53					
54	CIR14	54					
55	CIR15	55	W				
56	SCIR	56					
57	RDCPX2	57	LUTGATE				
58	RDSWITCH	58					
59	RDOPND	59					
60	+5V	60	+5V				
61	SMCUDATA	61	SR00				
62	MCUD01	62					
63	MCUD00	63	JBNDV				
74	MCUD03	64					
65	MCUD02	65	PAUSE				
66	MCUD05	66					
67	MCUD04	67	PADDIN09				
68	MCUD06	68	INDIRECT				
69	MCUD07	69	PWR ONB				
70	MCUD08	70	DS				
71	MCUD09	71	QS				
72	MCUD10	72	PADDIN11				
73	MCUD11	73	PADDIN10				
74	MCUD12	74	PADDIN08				
75	MCUD13	75	PADDXS00				
76	MCUD14	76	PADDXS01				
77	MCUD15	77	PADDSUB				
78	CLOCK	78	CPURST				
79	FREEZE	79	PADDX				
80	COM	80	COM				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0370	41	0375	96	0688	132	0373	168	0376
12	0696	42	0424	97	0683	133	0837	169	0512
13	0688	43	0846	98	0681	134	0375		
14	0371	44	0755	99	0141	135	0379	171	0374
15	0372	52-54	0755			137	0846	172	0373
16	0374	56,57	0755	101,102	0301	138	0424	173	0375
		59	0686	103	0375	139	0837	174	0373
21	0691			104,105	0301			175,176	0371
22	0372	66,67	0262	106,107	0688	141	0371	177	0374
23	0696	69	0685	108	0690	142	0205	178	0370
24	0380	71,72	0574	109	0695	143	0370	179	0574
25	0205	73	0837			144	0371		
26	0370	74,75	0574	111	0282	145	0379		
27,28	0696	76,77	0262	112	0371	146	0370		
29	0690	79	0759	113	0376	147	0239		
				114	0755	148	0274		
31	0239	81,82	0282	118,119	0755	149	0141		
32	0370	83	0837						
33	0239	84,85	0282	121	0239	159	0535		
34	0141	86,87	0842	122	0371	161	0371		
35	0372	89	0759	123	0373	162	0141		
36	0382			124	0755	163	0301		
37	0141	91,92	0301	128,129	0755	164	0371		
38	0695	93	0374			165	0379		
39	0690	94,95	0301	131	0371	166	0372		
						167	0374		





CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22

30001-60006 SHEET 3 OF 4

CURRENT INSTRUCTION REGISTER (CIR) PCA

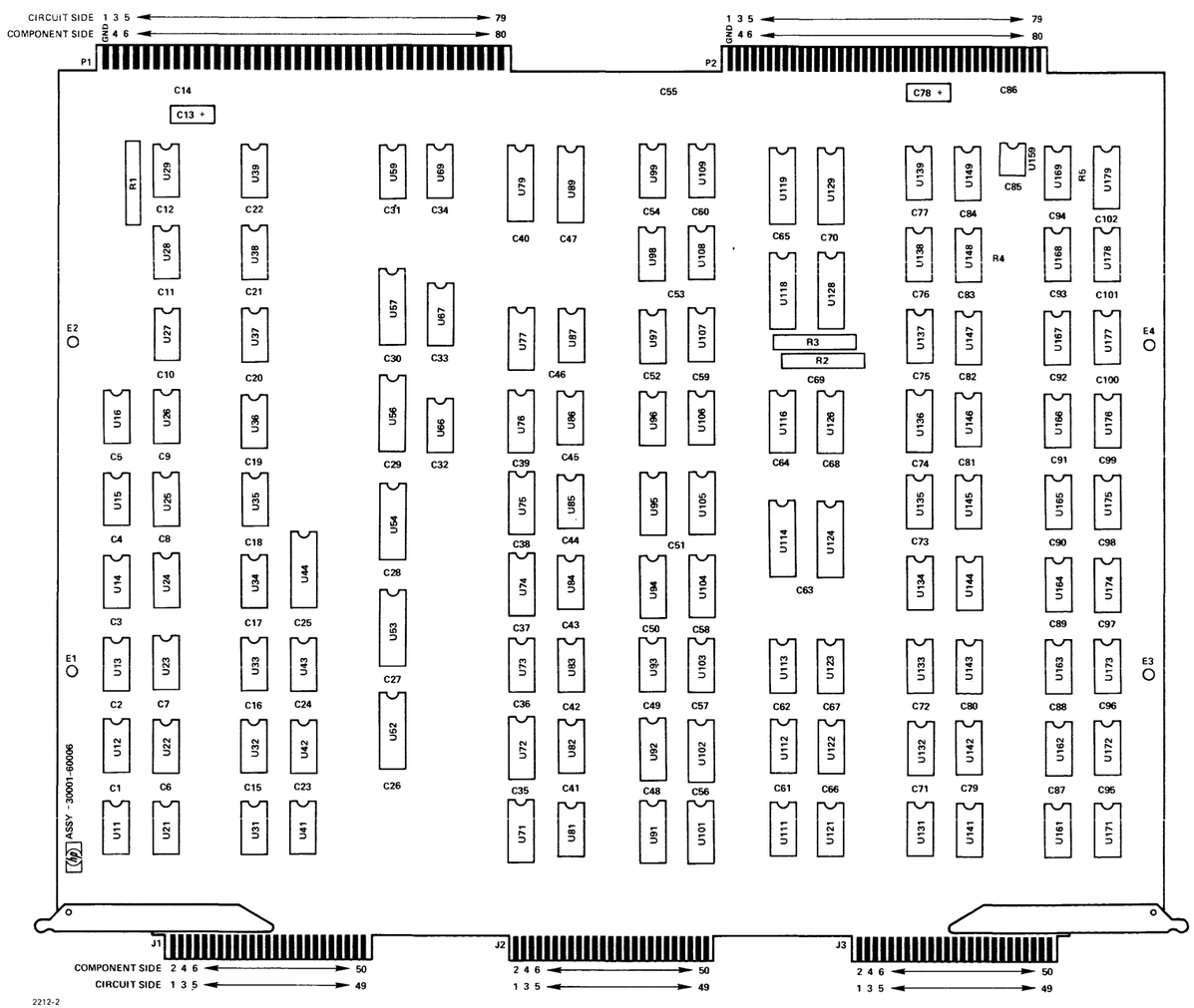
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL
1	DSPFLAG	1	OPINP	1	GND	1	CIR00
2	COM	2	COM	2	SW00	2	—
3	CPURSTS	3	BMCUPRTY	3	SW01	3	CIR01
4	IORSTSW	4	CPUIN	4	GND	4	—
5	MCUHINT	5	NIP	5	SW02	5	CIR02
6	HALT	6	STATUS03	6	SW03	6	—
7	MCUCMP	7	DATAPE	7	GND	7	CIR03
8	CMPRFF	8	V00	8	SW04	8	—
9	EXTINT	9	V01	9	SW05	9	CIR04
10	MCUINT	10	V02	10	GND	10	—
11	PWRFAIL	11	V03	11	SW06	11	CIR05
12	MODINT	12	V04	12	SW07	12	—
13	RUNFF	13	V05	13	GND	13	CIR06
14	INTRP	14	V06	14	SW08	14	—
15	STATUS04	15	V07	15	SW09	15	CIR07
16	STATUS01	16	V08	16	GND	16	—
17	CCPX	17	V09	17	SW10	17	CIR08
18	STATUS02	18	V10	18	SW11	18	—
19	FPNLOS	19	V11	19	GND	19	CIR09
20	+5V	20	+5V	20	SW12	20	—
21	RMCUCPX1	21	STORAR	21	SW13	21	CIR10
22	BNDV	22	SWLDRAR	22	GND	22	—
23	MCUCMPL	23	U00	23	SW14	23	CIR11
24	MCUCMPH	24	NIRTOCIR	24	SW15	24	—
25	RDCPX1	25		25	GND	25	CIR12
26	S00	26	U03	26	RSTSWIO	26	—
27	S01	27	U04	27	RSTSWCP	27	CIR13
28	S02	28	U05	28	GND	28	—
29	S03	29	U06	29	CLDLOAD	29	CIR14
30		30		30	CR UNFF	30	—
31	S04	31	U07	31	GND	31	CIR15
32	S05	32	U08	32	CONSINT	32	—
33	S06	33	U09	33	LOADREG	33	—
34	S07	34	U10	34	GND	34	—
35	S08	35	U11	35	DISPMEM	35	LUTA00
36	S09	36	U12	36	LOADMEM	36	—
37	S10	37	U13	37	GND	37	LUTA01
38	S11	38	U14	38	XEQ SW	38	—
39	COM	39	COM	39	SNGINST	39	LUTA02
40	COM	40	COM	40	GND	40	—
41	S12	41	U15	41	INHINTR	41	LUTA03
42	CLOCKS	42		42	ENBINTH	42	—
43	S13	43		43	BKPT HALT	43	LUTA04
44	S14	44	SPV	44	SYSDUMP	44	—
45	S15	45	NOP	45	RUN	45	LUTA05
46	RDCIR	46		46	INHAR	46	—
47	SHFTCLK	47	NXTDCD	47	INCRADD	47	LUTA06
48	SLOAD	48		48	DECRADD	48	—
49	CIR04	49	STKBNOP	49	SYSHALT	49	LUTA07
50	CIR07	50		50	—	50	—
51	CIR08	51	SR01				
52	CIR12	52					
53	CIR13	53					
54	CIR14	54					
55	CIR15	55	W				
56	SCIR	56					
57	RDCPX2	57	LUTGATE				
58	RDSWITCH	58					
59	RDOPND	59					
60	+5V	60	+5V				
61	SMCUDATA	61	SR00				
62	MCUD01	62					
63	MCUD00	63	JBNDV				
74	MCUD03	64					
65	MCUD02	65	PAUSE				
66	MCUD05	66					
67	MCUD04	67	PADDIN09				
68	MCUD06	68	INDIRECT				
69	MCUD07	69	PWR ONB				
70	MCUD08	70	DS				
71	MCUD09	71	QS				
72	MCUD10	72	PADDIN11				
73	MCUD11	73	PADDIN10				
74	MCUD12	74	PADDIN08				
75	MCUD13	75	PADDXS00				
76	MCUD14	76	PADDXS01				
77	MCUD15	77	PADDSUB				
78	CLOCK	78	CPURST				
79	FREEZE	79	PADDX				
80	COM	80	COM				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0370	41	0375	96	0688	132	0373	168	0376
12	0696	42	0424	97	0683	133	0837	169	0512
13	0688	43	0846	98	0681	134	0375		
14	0371	44	0755	99	0141	135	0379	171	0374
15	0372	52-54	0755			137	0846	172	0373
16	0374	56,57	0755	101,102	0301	138	0424	173	0375
		59	0686	103	0375	139	0837	174	0373
21	0691			104,105	0301			175,176	0371
22	0372	66,67	0262	106,107	0688	141	0371	177	0374
23	0696	69	0685	108	0690	142	0205	178	0370
24	0380	71,72	0574	109	0695	143	0370	179	0574
25	0205	73	0837			144	0371		
26	0370	74,75	0574	111	0282	145	0379		
27,28	0696	76,77	0262	112	0371	146	0370		
29	0690	79	0759	113	0376	147	0239		
				114	0755	148	0274		
31	0239	81,82	0282	118,119	0755	149	0141		
32	0370	83	0837						
33	0239	84,85	0282	121	0239	159	0535		
34	0141	86,87	0842	122	0371	161	0371		
35	0372	89	0759	123	0373	162	0141		
36	0382			124	0755	163	0301		
37	0141	91,92	0301	128,129	0755	164	0371		
38	0695	93	0374			165	0379		
39	0690	94,95	0301	131	0371	166	0372		
						167	0374		



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1505-22

(A9) CIR

RDCIR ← P1-46

RPOPND ← P1-59

RDSWITCH ← P1-58

SW 00 ← J1-2
SW 01 ← J1-3
SW 02 ← J1-5
SW 03 ← J1-6
SW 04 ← J1-8
SW 05 ← J1-9
SW 06 ← J1-11
SW 07 ← J1-12

SW 08 ← J1-14
SW 09 ← J1-15
SW 10 ← J1-17
SW 11 ← J1-18
SW 12 ← J1-20
SW 13 ← J1-21
SW 14 ← J1-23
SW 15 ← J1-24

OPINP ← P2-1

U57, U56, U53, U54 — ENABLE (9,11)

U82A, U82D, U82B, U82C, U83A → 00
U81A, U81D, U81B, U81C, U73A → 01
U85A, U85D, U85B, U85C, U73B → 02
U84A, U84D, U84B, U84C, U83B → 03

U93A → P1-7 MCUCMP

S BUS 0-15 (F7)

U72, U71, U75, U74 — 4-BIT REGISTER
CLOCK
CLEAR
OUTPUT ENABLE (1,2) INPUT ENABLE (9,10)

(B4) CLK 4

(F7) BMCU 0-15

U97A

(H8) $\overline{CIR}$

U173 → $\overline{BCC}$ (G13)

(G13) DD

(C13) SPECOP

(F19) WF

U162C → P2-74 08
U161C
U141C
U131C
U143C
U141B
U161A → P2-67 09
U162B
U141A
U131A
U132B
U171A → P2-73 10
U172A
U162D → P2-72 11
U142A
U143D
U112B
U132A
U113B → P2-77 PADDSUB
U123A
U176A
U16B
U166A
U112A
R5D 1K +5V
U168B
U113A → P2-79 $\overline{PADDX}$
U162A
U122B
AA (F13)
U123B
U122C → P2-76 01
U122A → P2-75 00
U111A
U112C

PADDIN

PADDXS

30001-60006	TITLE	SHEET 4 OF 4
CURRENT INSTRUCTION REGISTER (CIR) PCA		
ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-206

MODULE CONTROL UNIT (MCU) PCA

30001-60007

SERIES 1247

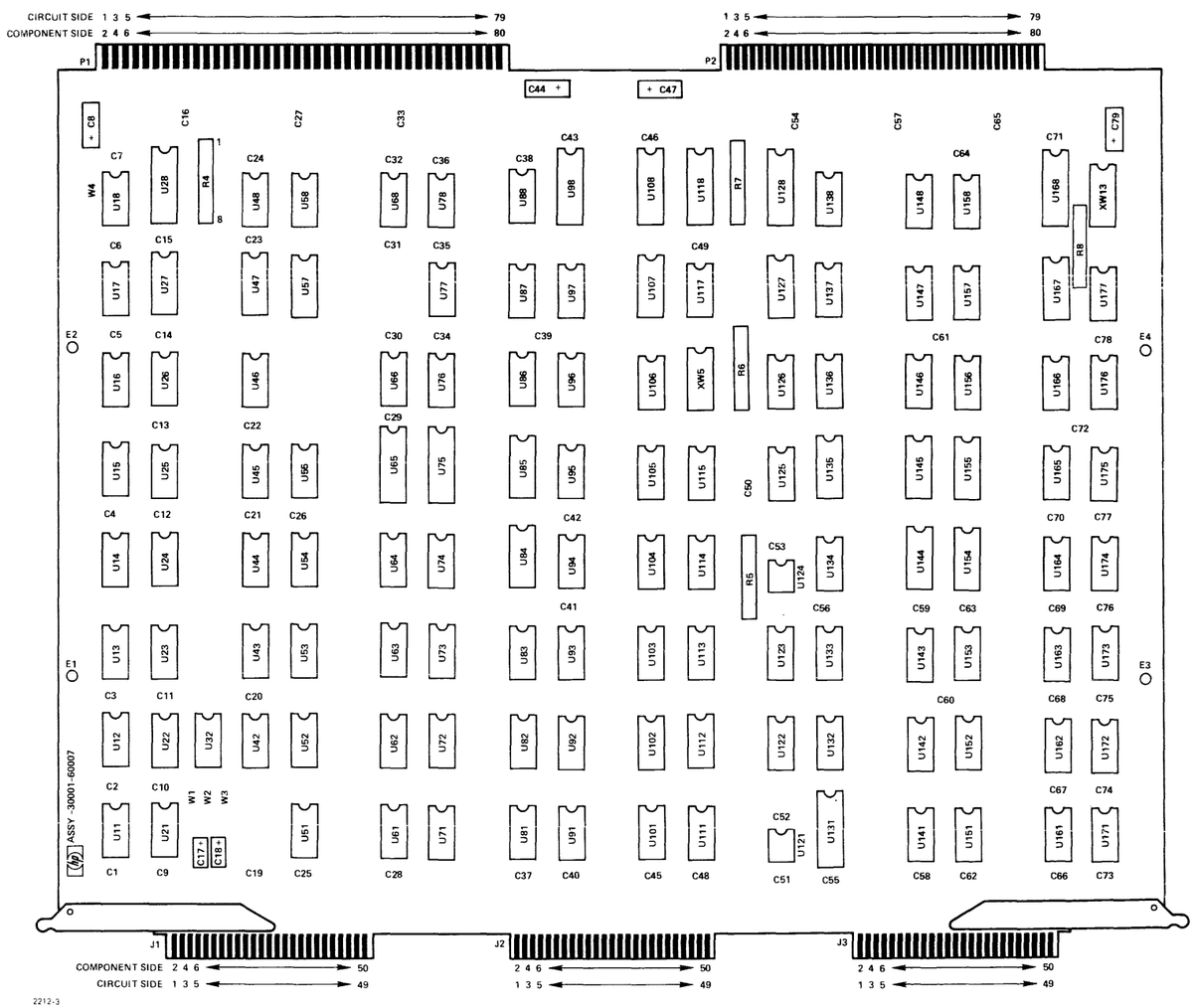
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	S03	1	READY00	1	—
2	COM	2	COM	2	—
3	S01	3	READY02	3	XXX
4	CPUIN	4	FROM00	4	—
5	RDCPX1	5	READY04	5	XXX
6	RMCUCPX1	6	FROM02	6	—
7	S02	7	READY06	7	XXX
8	U02	8	MOP01	8	—
9	S00	9	ENABLE01	9	XXX
10	U06	10	TO02	10	—
11	S10	11	ENABLE03	11	—
12	S08	12	FROM01	12	—
13		13	ENABLE05	13	—
14	S09	14	MOP00	14	—
15	S13	15	MCUD PE	15	—
16	S11	16	TO00	16	—
17	S14	17	MCU RST	17	—
18	S12	18	SYSPRTY	18	—
19	S15	19	READY01	19	—
20	+5V	20	+5V	20	—
21	DATAPE	21	READY03	21	—
22	MCUINT	22	TO01	22	—
23	ERFRZINH	23	READY05	23	—
24	CPUTIMER	24	UT01	24	—
25	RDOPND	25	ENABLE00	25	—
26	NOP1	26	UT02	26	—
27	INTRP	27	ENABLE02	27	—
28	POLLORSO	28	PT01	28	—
29	UNFRZ	29	ENABLE04	29	XXX
30	NXTDCD	30		30	—
31	ENTIMER	31		31	—
32	NXTFINH	32	PT02	32	—
33	JMPFRZ	33	SYS PE	33	XXX
34	STATUS01	34	TENB	34	—
35	MPIFRZ	35	IOLRQFF	35	—
36	U01	36	IOHRQFF	36	—
37	BMCUPRTY	37	SLOAD	37	XXX
38	MODINT	38	SHFTCLK	38	—
39	COM	39	COM	39	XXX
40	COM	40	COM	40	—
41	COR10	41	INSTSEL	41	XXX
42	CLOCKS	42		42	—
43	COR11	43	SRDYENBL	43	XXX
44	COR14	44	RDCPX2	44	—
45	COR15	45	IOHIREQ	45	XXX
46	COR13	46		46	—
47	TMRFRZI	47	IOLOREQ	47	XXX
48	U07	48		48	—
49	DATA	49	IOERROR	49	—
50	ST03	50	SRVOUT1	50	—
51	BUSOP	51	IOSTROBE		
52	NOP2	52	COR00		
53	RORT23	53	IOHSEL		
54	RORT24	54	COR01		
55	RORT27	55	IOLOSEL		
56	CCPX	56	COR02		
57	RORT26	57			
58	STOFROM	58	PSELECT		
59	RORT25	59			
60	+5V	60	+5V		
61	IOFRZ	61	CPULRFF		
62	IOHSREQ	62	CHACT		
63	DRTINH	63	CPULOSEL		
64	IOINP	64	CPUHRFF		
65	IOTIMER	65	ST01		
66	IOMOP00	66	OPNDSEL		
67	IOMOP01	67	ST00		
68	IOTO02	68	MCIOTMR		
69	IOTO01	69	ST02		
70	S04	70	IOCMP		
71	S07	71	IORESET		
72	MCUDPRTY	72	NEXT		
73	S06	73			
74	S05	74	NIP		
75	RDMOD	75			
76	CPUSEL	76	OPINP		
77	MDPARITY	77			
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0685	53	0141	86	0846	114	0424	144,145	0574
13	0371	54,55	0691	87	0842	115	0623	146	0696
14	0686	57	0574	88	0690	117	0617	147	0691
15	0141	58	0686			118	0755	148	0682
16-18	0846			91	0371				
		61	0424	92	0696	121	0535	151	0837
21	0844	62	0512	93	0373	122	0846	152	0693
22,23	0696	63	0696	94	0837	123	0617	153	0141
24	0681	64	0374	95	0424	124	0535	154,155	0574
25	0141	65	0759	96	0685	125	0843	156	0686
26	0739	66	0690	97	0842	126	0691	157,158	0843
27	0574	68	0686	98	0755	127	0262		
28	0755					128	0759	161,162	0837
		71	0608	101	0371			163,164	0696
32	0141	72	0696	102	0696	131	0755	165	0239
		73	0239	103	0617	132	0382	166	0681
42	0371	74	0371	104	0205	133,134	0696	167	0262
43	0696	75	0755	105	0374	135	0574	168	0759
44	0424	76,77	0690	106	0842	136	0682		
45	0696	78	0681	107	0262	137	0691	171,172	0837
46	0837			108	0759	138	0682	173	0205
47	0574	81	0683					174	0370
48	0688	82	0696	111	0372	141	0370	175	0683
		83	0617	112	0696	142	0693	176	0690
51	0239	84	0574	113	0373	143	0374	177	0375
52	0205	85	0262						



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-C	NO CHANGE	ALL
D	PC-22-1549	A-1238-22	ALL
E	PC-22-1566	A-1241-22	ALL
F	22-1587	B-1247-22	ALL
G	ERRATA	NO CHANGE	ALL

ENABLE 00 P2-25
ENABLE 01 P2-9
ENABLE 02 P2-27
ENABLE 03 P2-11
ENABLE 04 P2-29
ENABLE 05 P2-13
U168 ENABLE
U178 ENB X2
W12 W13
R8A 1K +5V
U78A MPIFRZ (G12)
(B33) IOLRQ
(C33) IOHRQ
U167 8-BIT SHIFT REGISTER
U127 8 BIT SHIFT REGISTSTER
SERIAL IN PARALLEL ENABLE CLOCK ENABLE CLOCK
SLOAD P2-37
SHFTCLK P2-38
R7F 1K +5V
U128 ENABLE
READY00 P2-1
READY01 P2-19
READY02 P2-3
READY03 P2-21
READY04 P2-5
READY05 P2-23
READY06 P2-7
RRDY0 (F37)
RRDY1 (F37)
RRDY2 (F37)
RRDY3 (F37)
U165A (D13)(G28) (K)
U156B (D13)(G28) (M)
(D13)(G28) (L)
U157 DATA 2° 2¹ 1-TO-4 MULIPLEXER
READY 0 (E37)
READY 1 (E37)
READY 2 (E37)
READY 3 (E37)
U158 DATA 2° 2¹ 1-TO-4 MULTIPLEXER
U137B U137C U137D U137E U137A U147B U147C U147D U147E U147A U138A U138D U138C U148B U148A U148D U148C
U77A U77B U78C U76A U78D U76B U68A U66B
UFCLK1 (A16)(G38) (B28)(D22)
UFCLK2 (B32)(E22) (G37)
UFCLK1 (B16)(B35)
FCLK1 (C28)
FCLK1 (F26)
IOFRE P1-61
CLOCKS P1-42
INFRZ (G15)
CLOCK P1-78
CPURST P2-78
R5G 1K R5C 1K
U121A U124B U124A R5B 1K +5V
RST1 (C28)(E24)
RST2 (F17)(B16)(E22) (B28)(G38)
U114F RST (E22)
SLOAD (G18)(E38)
SHFTCLK (G18)(E38)
X2=U178 W14 W15
RBE 1K RBF 1K +5V
U177
P2-34 TENB
(B37) HSELINH U132
(C38) LSELINH U114A
(A19) CMCU ERR U141B
U151C U151B U53B
(B24) INFRZ (G15)
U141C (A27) OPINP (D25) UM
U171B (C30) NIPSELENB
(E22)
U171A (D29) ROPND
(E23)
U44D (E) (D16)
U166A
U176A (C39) IOLRDY (B33) IOHRQFF
U176B 9,10,12,13
U138B (D19) MODINT RDY W9 W10 W11
(F17) (F)
LREQFF TENE RDYCMP U161A
U111C (B24) (H)
CPUHRFF (D38)
CPUSEL (G8)(C12)(G16)(D38)
P2-76 CPUSEL
U72B CPUSEL (C27)
R5B 1K
U53B (B24) (G) INFRZ (G15)
CPULRFF (F16)(D38)
P2-3,61,85 CPULRFF
U133B LREQ (J) (D22)
U156C
P2-43 SRDYENBL
LRQFF (F12)
P2-64 CPUHRFF
U133A HREQ HRQFF (F12)(B33)
R4G 1K
U23B OPNDSEL (D) (H26)
OPNDSEL (B27)
J2-11
P2-66 OPNDSEL
U22A CWANOP (G28)
R5G 1K
U72A LOSEL
U166B
R5E 1K
U62A CHECK CYC (B9) CPUSEL (A) (A17)
P2-25
P2-17 MCURST

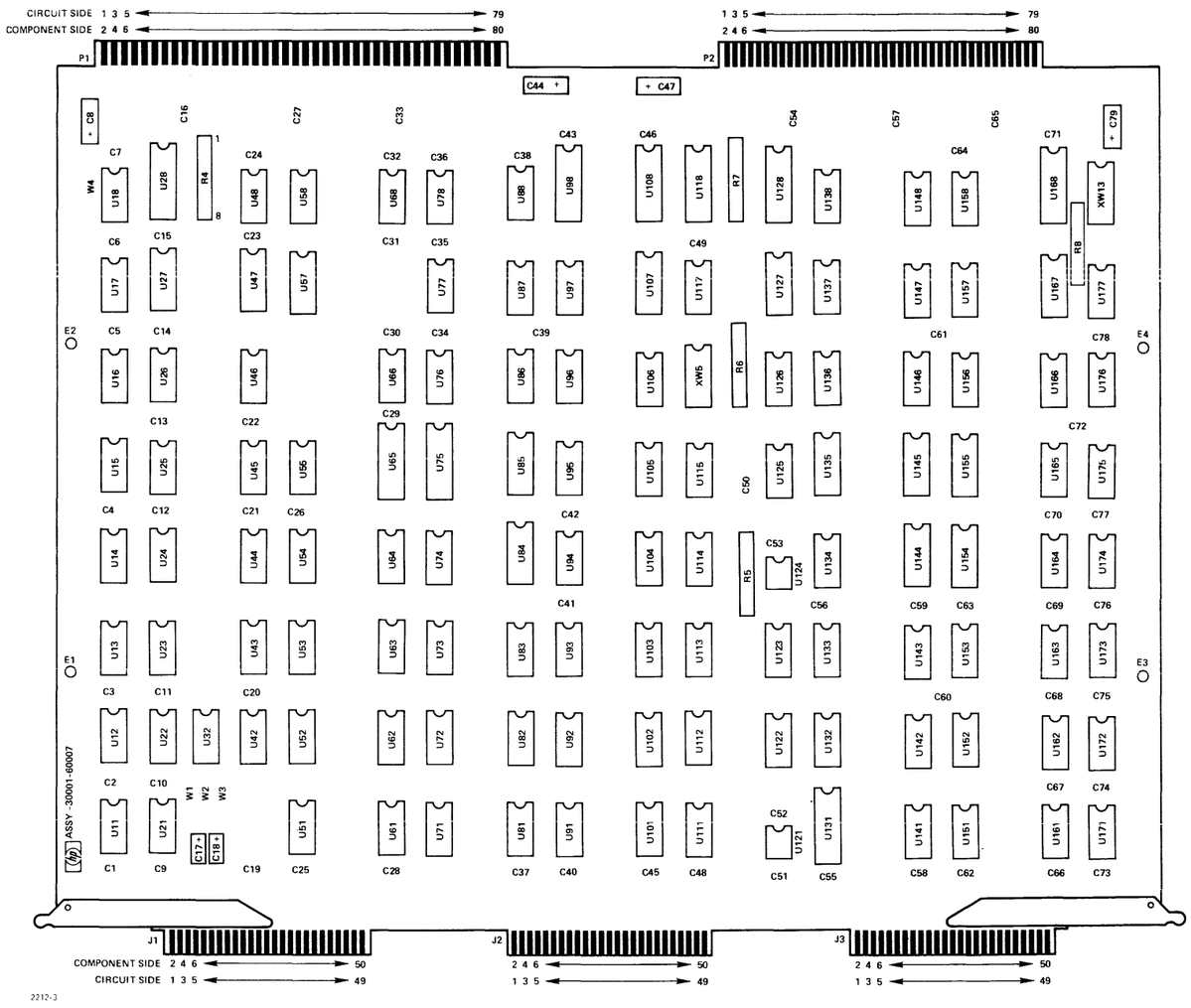
30001-60007 TITLE SHEET 1 OF 4
MODULE CONTROL UNIT (MCU) P.C.A
ENGINEER APPROVED DATE
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	S03	1	READY00	1	—
2	COM	2	COM	2	—
3	S01	3	READY02	3	XXX
4	CPUIN	4	FROM00	4	—
5	RDCPX1	5	READY04	5	XXX
6	RMCUCPX1	6	FROM02	6	—
7	S02	7	READY06	7	XXX
8	U02	8	MOP01	8	—
9	S00	9	ENABLE01	9	XXX
10	U06	10	TO02	10	—
11	S10	11	ENABLE03	11	—
12	S08	12	FROM01	12	—
13		13	ENABLE05	13	—
14	S09	14	MOP00	14	—
15	S13	15	MCUD PE	15	—
16	S11	16	TO00	16	—
17	S14	17	MCU RST	17	—
18	S12	18	SYSPRTY	18	—
19	S15	19	READY01	19	—
20	+5V	20	+5V	20	—
21	DATAPE	21	READY03	21	—
22	MCUINT	22	TO01	22	—
23	ERFRZINH	23	READY05	23	—
24	CPUTIMER	24	UT01	24	—
25	RDOPND	25	ENABLE00	25	—
26	NOP1	26	UT02	26	—
27	INTRP	27	ENABLE02	27	—
28	POLLORSO	28	PT01	28	—
29	UNFRZ	29	ENABLE04	29	XXX
30	NXTDCD	30		30	—
31	ENTIMER	31		31	—
32	NXTFINH	32	PT02	32	—
33	JMPFRZ	33	SYS PE	33	XXX
34	STATUS01	34	TENB	34	—
35	MPIFRZ	35	IOLRQFF	35	—
36	U01	36	IOHRQFF	36	—
37	BMCUPRTY	37	SLOAD	37	XXX
38	MODINT	38	SHFTCLK	38	—
39	COM	39	COM	39	XXX
40	COM	40	COM	40	—
41	COR10	41	INSTSEL	41	XXX
42	CLOCKS	42		42	—
43	COR11	43	SRDYENBL	43	XXX
44	COR14	44	RDCPX2	44	—
45	COR15	45	IOHIREQ	45	XXX
46	COR13	46		46	—
47	TMRFRZI	47	IOLOREQ	47	XXX
48	U07	48		48	—
49	DATA	49	IOERROR	49	—
50	ST03	50	SRVOUT1	50	—
51	BUSOP	51	IOSTROBE		
52	NOP2	52	COR00		
53	RORT23	53	IOHSEL		
54	RORT24	54	COR01		
55	RORT27	55	IOLOSEL		
56	CCPX	56	COR02		
57	RORT26	57			
58	STOFROM	58	PSELECT		
59	RORT25	59			
60	+5V	60	+5V		
61	IOFRZ	61	CPULRFF		
62	IOHSREQ	62	CHACT		
63	DRTINH	63	CPULOSEL		
64	IOINP	64	CPUHRFF		
65	IOTIMER	65	ST01		
66	IOMOP00	66	OPNDSEL		
67	IOMOP01	67	ST00		
78	IOTO02	68	MCIOTMR		
69	IOTO01	69	ST02		
70	S04	70	IOCMP		
71	S07	71	IORESET		
72	MCUDPRTY	72	NEXT		
73	S06	73			
74	S05	74	NIP		
75	RDMOD	75			
76	CPUSEL	76	OPINP		
77	MDPARITY	77			
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0685	53	0141	86	0846	114	0424	144,145	0574
13	0371	54,55	0691	87	0842	115	0623	146	0696
14	0686	57	0574	88	0690	117	0617	147	0691
15	0141	58	0686			118	0755	148	0682
16-18	0846			91	0371				
		61	0424	92	0696	121	0535	151	0837
21	0844	62	0512	93	0373	122	0846	152	0693
22,23	0696	63	0696	94	0837	123	0617	153	0141
24	0681	64	0374	95	0424	124	0535	154,155	0574
25	0141	65	0759	96	0685	125	0843	156	0686
26	0739	66	0690	97	0842	126	0691	157,158	0843
27	0574	68	0686	98	0755	127	0262		
28	0755					128	0759	161,162	0837
		71	0608	101	0371			163,164	0696
32	0141	72	0696	102	0696	131	0755	165	0239
		73	0239	103	0617	132	0382	166	0681
42	0371	74	0371	104	0205	133,134	0696	167	0262
43	0696	75	0755	105	0374	135	0574	168	0759
44	0424	76,77	0690	106	0842	136	0682		
45	0696	78	0681	107	0262	137	0691	171,172	0837
46	0837			108	0759	138	0682	173	0205
47	0574	81	0683					174	0370
48	0688	82	0696	111	0372	141	0370	175	0683
		83	0617	112	0696	142	0693	176	0690
51	0239	84	0574	113	0373	143	0374	177	0375
52	0205	85	0262						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-C	NO CHANGE
D	PC-22-1548	A-1238-22
E	PC-22-1580	A-1241-22
F	22-1587	B-1247-22
G	ERRATA	NO CHANGE

MCUD PE ← P2-15
U1 ← P2-36
MOP1 ← P2-8
MOP0 ← P2-14
FROM2 ← P2-6
FROM1 ← P2-12
FROM0 ← P2-4
T02 ← P2-10
T01 ← P2-22
T00 ← P2-16
U108 ENABLE
BMOP1 (D38)
U106 ODD PARITY BIT, SYS PAR CHECK, PARITY 1, PARITY 2, PARITY ERROR
(G17) SYSTP
R7F 1K
+5V
R7C 1K, R7A 1K, R7B 1K, R6A 1K, R6B 1K, R7E 1K
U118 ENABLE
(D34) MOP1
(E34) MOP0
(E34) FRM2
(E34) FRM1
(E34) FRM0
(D34) T02
(D34) T01
(D34) T00
(B9) CPUSEL
(D27) ME
U86A, U86B, U86D
ME2 (F32)(H27)
ME1 (F32)(G27)
ME0 (E32)(G27)
X1=U116 FRM
W6, W7, W8
RFM0 (H23)
RFM1 (H23)
RFM2 (H23)
U117A, U117D, U117C
U96A
U95F
ME (F36)
U87 ODD PARITY BIT, CNTRL PAR GEN
(K) (G28) (D3)
(L) (G28) (E3)
(M) (G28) (E3)
(G30) MOP1
(H30) MOP0
U95D
(F4) UFCLK1
GSYSPE (G36)
U95C
RDMOD ← P1-75
RDMOD (A37)
U7 ← P1-48
RMCUCPX1 ← P1-6
DATA PE ← P1-21
SYS PE ← P2-33
STATUS 1 ← P1-34
RDCPX1 ← P1-5
U2 ← P1-8
CPUTIMER ← P1-24
COR0 ← P2-52
COR1 ← P2-54
COR2 ← P2-56
ST0 ← P2-67
ST2 ← P2-69
ST1 ← P2-65
U75A, U75B, U56A
BUSOP/DATA
(B33)(D9) HRQFF
(C9) LRQFF
U24D
(B22) NOP2
U55A, U55E, U55C, U55B, U54C, U54E, U54A, U54B, U55D, U54D
(D23) NXTDLD
R4E 1K
ERFRZINH ← P1-23
XTFINH ← P1-32
NXTDCD ← P1-30
INTRP ← P1-27
U44F, U44E
U58B
(A27) S
(D23) NXTDLD
(C26) RWAN
U13A
(B29) NIP
RDOPND ← P1-25
NOP1 ← P1-26
U44A, U44B
(B30) OPINP
(B27) SETOPND
R4F 1K
MP1FRZ (B2)
MP1FRZ ← P1-35
JMPFRZ ← P1-33
U48B, U88B, U24A, U88A, U25C
FRZ
UNFRZ ← P1-29
TMRFRZI ← P1-47
CCPX ← P1-56
U6 ← P1-10
MD PARITY ← P1-77
(T) (G28)
(P) (G24)
(C) (G26)
U73C, U104B, U104C
RCRL (B27)
RNIR (C28)
ROFND (E7)
U44C
CCPX (B17)
(G35) COMP
U64B, U74B
INFRZ (F2)(C7)(A27)
U95E
(C9) CPCLRFF
U105A
(C28) (N)
U61D
U115 4-BIT COMPARATOR ADER CMP, STROBE
MAX MEM
R6E 1K, R6D 1K, R6C 1K, R5E 1K
W3, W4, W5
U84 4-BIT REGISTER
(F4) UFCLK
CLOCK
CLEAR
INPUT ENABLE
OUTPUT ENABLE
U65G
U168H
(D17) CCPX
ADDPE (D37)
(G9) (A)
U73B, U25A
U73A
SYSTPE (D37)
U46B
CPU ERR (B6)
APEFF (E16)
U15A, U16A
U15B, U16B
P2-7 ← S2
S2 (B38)
P2-1 ← S3
S3 (B38)
P2-74 ← S5
P2-73 ← S6
P2-71 ← S7
P2-70 ← S4
U45B CMCU ADDR PE
U25D, U18B
P2-3 ← S1
S1 (B28)
J2-3
R4G 1K
MODINT (G5)
U23A MOD INT
U14B, U24B
P1-38 ← MOD INT
U14C, U25B
U14A
P1-4 ← CPUIN
RDCPXI (B38)
U74A, U24C
P1-22 ← MCUINT
U15C, U16D
U15D, U16C
J2-5
U64A, U13B
(A19) APEFF
TIMER
U46A
ILLARD (F6)
MCUERR (B27)
R5A 1K
U63A CMCU ILL ADD
(G4) RST2
P1-37 ← BMCUPRTY
U107 8-BIT SHIFT REGISTER
(E38)
(D39) STOFROM
SERIAL IN
(C5) SLOAD
PARALLEL ENABLE
CLOCK
CLOCK ENABLE
(C5) SHFTCLK
U65J, U65D, U65A
SYSTP (D38)(B14)
U75J, U75A, U75E
(B9) CPUSEL
SYSPRTY (E35)
P2-18 ← SYSPRTY
P1-72 ← MCUDPRTY
P1-79 ← FREEZE

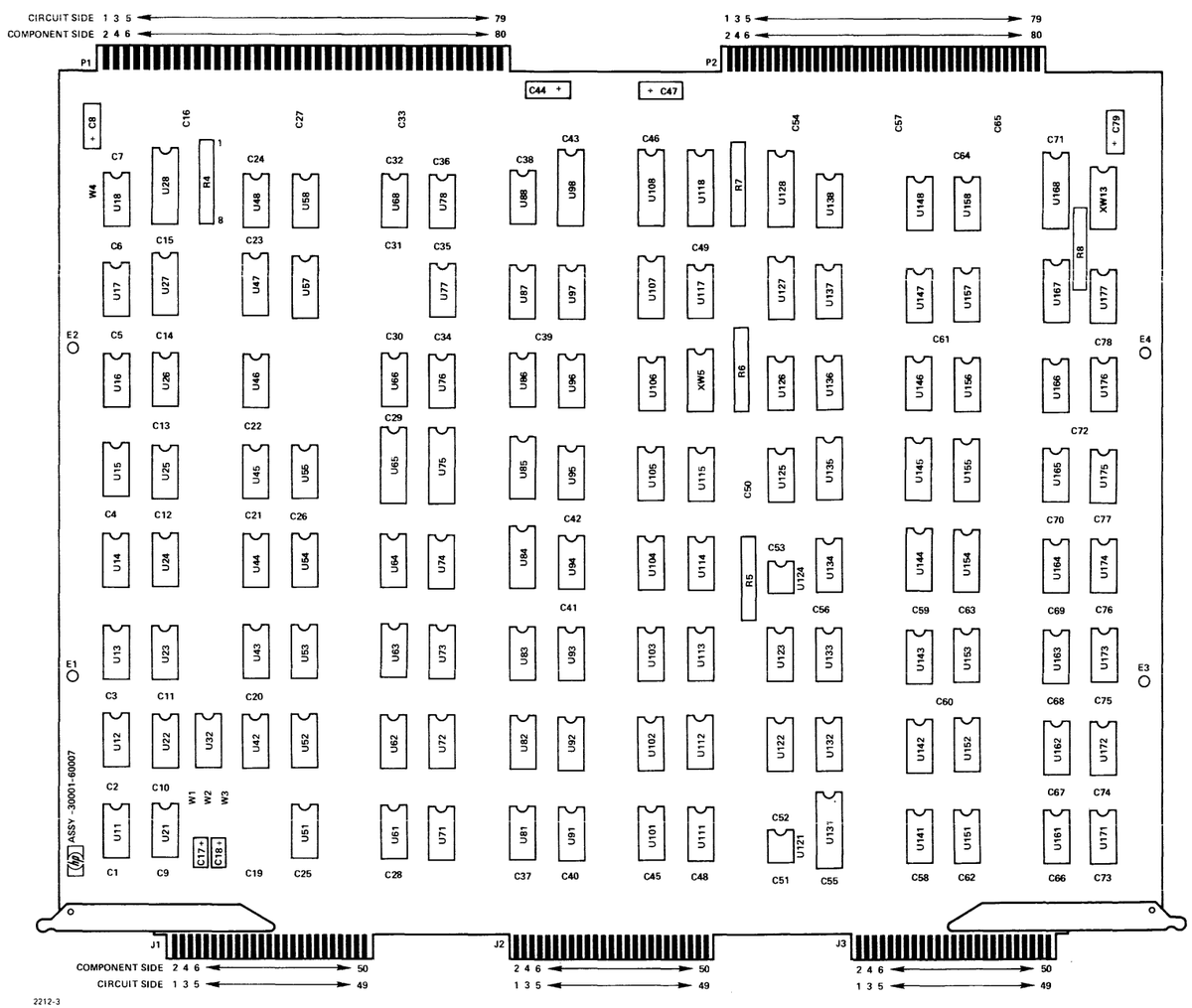
30001-60007 TITLE SHEET 2 OF 4
MODULE CONTROL UNIT (MCU) PCA
DRAWN | APPROVED | DATE
HEWLETT PACKARD CO

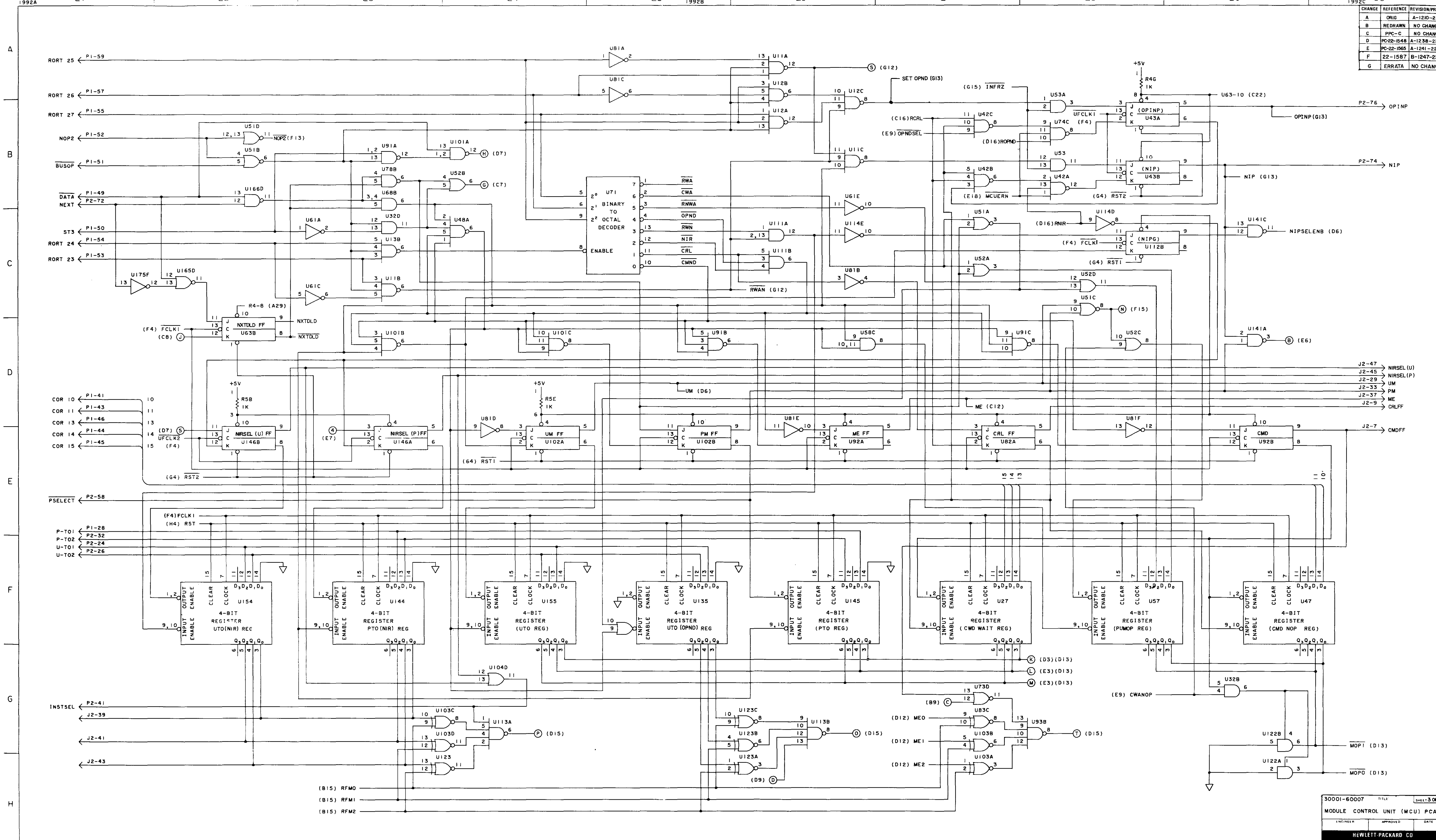
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	S03	1	READY00	1	—
2	COM	2	COM	2	—
3	S01	3	READY02	3	XXX
4	CPUIN	4	FROM00	4	—
5	RDCPX1	5	READY04	5	XXX
6	RMCUCPX1	6	FROM02	6	—
7	S02	7	READY06	7	XXX
8	U02	8	MOP01	8	—
9	S00	9	ENABLE01	9	XXX
10	U06	10	TO02	10	—
11	S10	11	ENABLE03	11	—
12	S08	12	FROM01	12	—
13		13	ENABLE05	13	—
14	S09	14	MOP00	14	—
15	S13	15	MCUD PE	15	—
16	S11	16	TO00	16	—
17	S14	17	MCU RST	17	—
18	S12	18	SYSPRTY	18	—
19	S15	19	READY01	19	—
20	+5V	20	+5V	20	—
21	DATAPE	21	READY03	21	—
22	MCUINT	22	TO01	22	—
23	ERFRZINH	23	READY05	23	—
24	CPUTIMER	24	UT01	24	—
25	RDOPND	25	ENABLE00	25	—
26	NOP1	26	UT02	26	—
27	INTRP	27	ENABLE02	27	—
28	POLLORSO	28	PT01	28	—
29	UNFRZ	29	ENABLE04	29	XXX
30	NXTDCD	30		30	—
31	ENTIMER	31		31	—
32	NXTFINH	32	PT02	32	—
33	JMPFRZ	33	SYS PE	33	XXX
34	STATUS01	34	TENB	34	—
35	MPIFRZ	35	IOLRQFF	35	—
36	U01	36	IOHRQFF	36	—
37	BMCUPRTY	37	SLOAD	37	XXX
38	MODINT	38	SHFTCLK	38	—
39	COM	39	COM	39	XXX
40	COM	40	COM	40	—
41	COR10	41	INSTSEL	41	XXX
42	CLOCKS	42		42	—
43	COR11	43	SRDYENBL	43	XXX
44	COR14	44	RDCPX2	44	—
45	COR15	45	IOHIREQ	45	XXX
46	COR13	46		46	—
47	TMRFRZI	47	IOLOREQ	47	XXX
48	U07	48		48	—
49	DATA	49	IOERROR	49	—
50	ST03	50	SRVOUT1	50	—
51	BUSOP	51	IOSTROBE		
52	NOP2	52	COR00		
53	RORT23	53	IOHSEL		
54	RORT24	54	COR01		
55	RORT27	55	IOLOSEL		
56	CCPX	56	COR02		
57	RORT26	57			
58	STOFROM	58	PSELECT		
59	RORT25	59			
60	+5V	60	+5V		
61	IOFRZ	61	CPULRFF		
62	IOHSREQ	62	CHACT		
63	DRTINH	63	CPULOSEL		
64	IOINP	64	CPUHRFF		
65	IOTIMER	65	ST01		
66	IOMOP00	66	OPNDSEL		
67	IOMOP01	67	ST00		
78	IOTO02	68	MCIOTMR		
69	IOTO001	69	ST02		
70	S04	70	IOCMP		
71	S07	71	IORESET		
72	MCUDPRTY	72	NEXT		
73	S06	73			
74	S05	74	NIP		
75	RDMOD	75			
76	CPUSEL	76	OPINP		
77	MDPARITY	77			
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0685	53	0141	86	0846	114	0424	144,145	0574
13	0371	54,55	0691	87	0842	115	0623	146	0696
14	0686	57	0574	88	0690	117	0617	147	0691
15	0141	58	0686			118	0755	148	0682
16-18	0846			91	0371				
		61	0424	92	0696	121	0535	151	0837
21	0844	62	0512	93	0373	122	0846	152	0693
22,23	0696	63	0696	94	0837	123	0617	153	0141
24	0681	64	0374	95	0424	124	0535	154,155	0574
25	0141	65	0759	96	0685	125	0843	156	0686
26	0739	66	0690	97	0842	126	0691	157,158	0843
27	0574	68	0686	98	0755	127	0262		
28	0755					128	0759	161,162	0837
		71	0608	101	0371			163,164	0696
32	0141	72	0696	102	0696	131	0755	165	0239
		73	0239	103	0617	132	0382	166	0681
42	0371	74	0371	104	0205	133,134	0696	167	0262
43	0696	75	0755	105	0374	135	0574	168	0759
44	0424	76,77	0690	106	0842	136	0682		
45	0696	78	0681	107	0262	137	0691	171,172	0837
46	0837			108	0759	138	0682	173	0205
47	0574	81	0683					174	0370
48	0688	82	0696	111	0372	141	0370	175	0683
		83	0617	112	0696	142	0693	176	0690
51	0239	84	0574	113	0373	143	0374	177	0375
52	0205	85	0262						





CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-C	NO CHANGE
D	PC-22-1548	A-1238-22
E	PC-22-1565	A-1241-22
F	22-1587	B-1247-22
G	ERRATA	NO CHANGE

30001-60007 TITLE SHEET 3 OF 4

MODULE CONTROL UNIT (MCU) PCA

ENGINEER | APPROVED | DATE

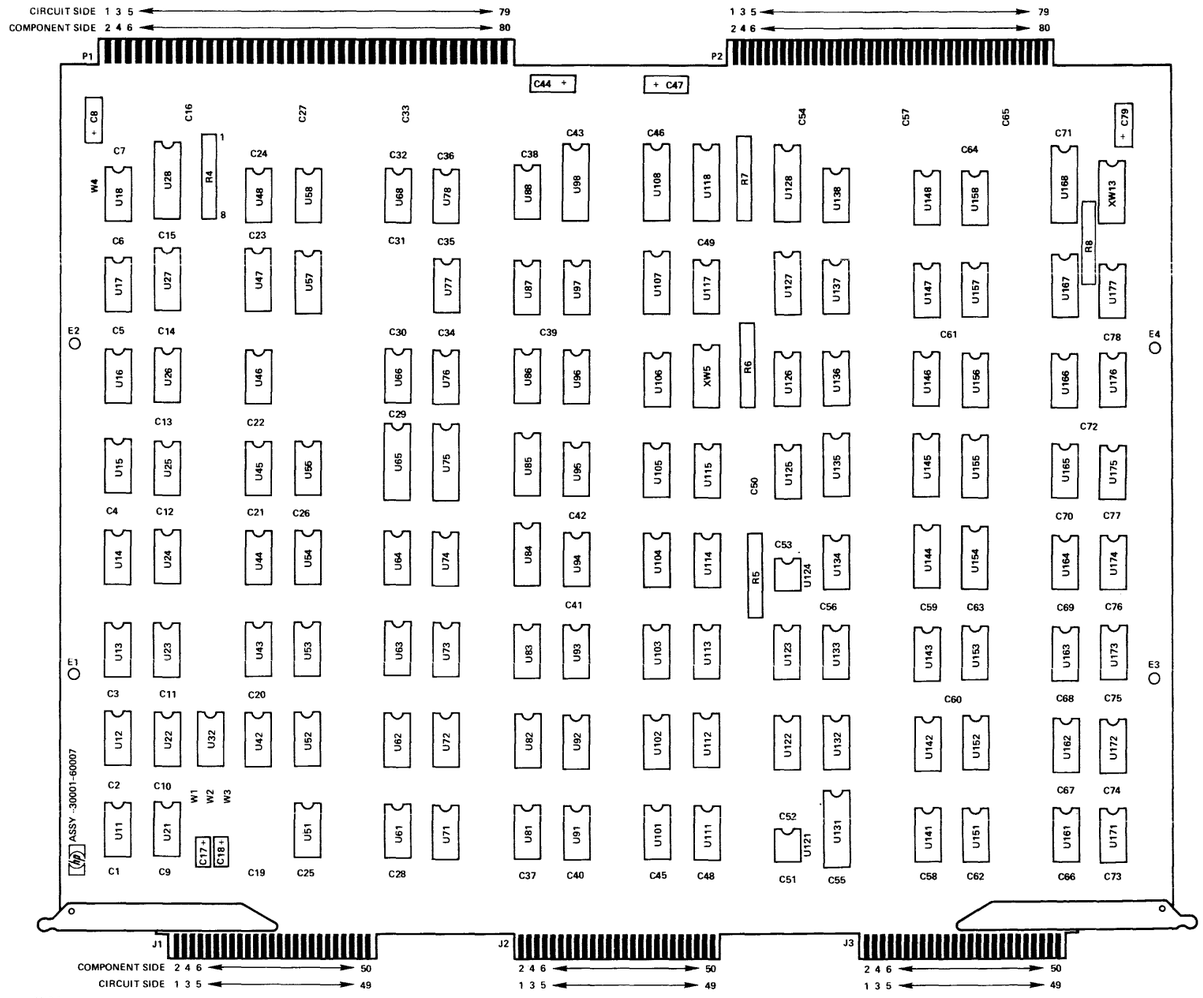
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

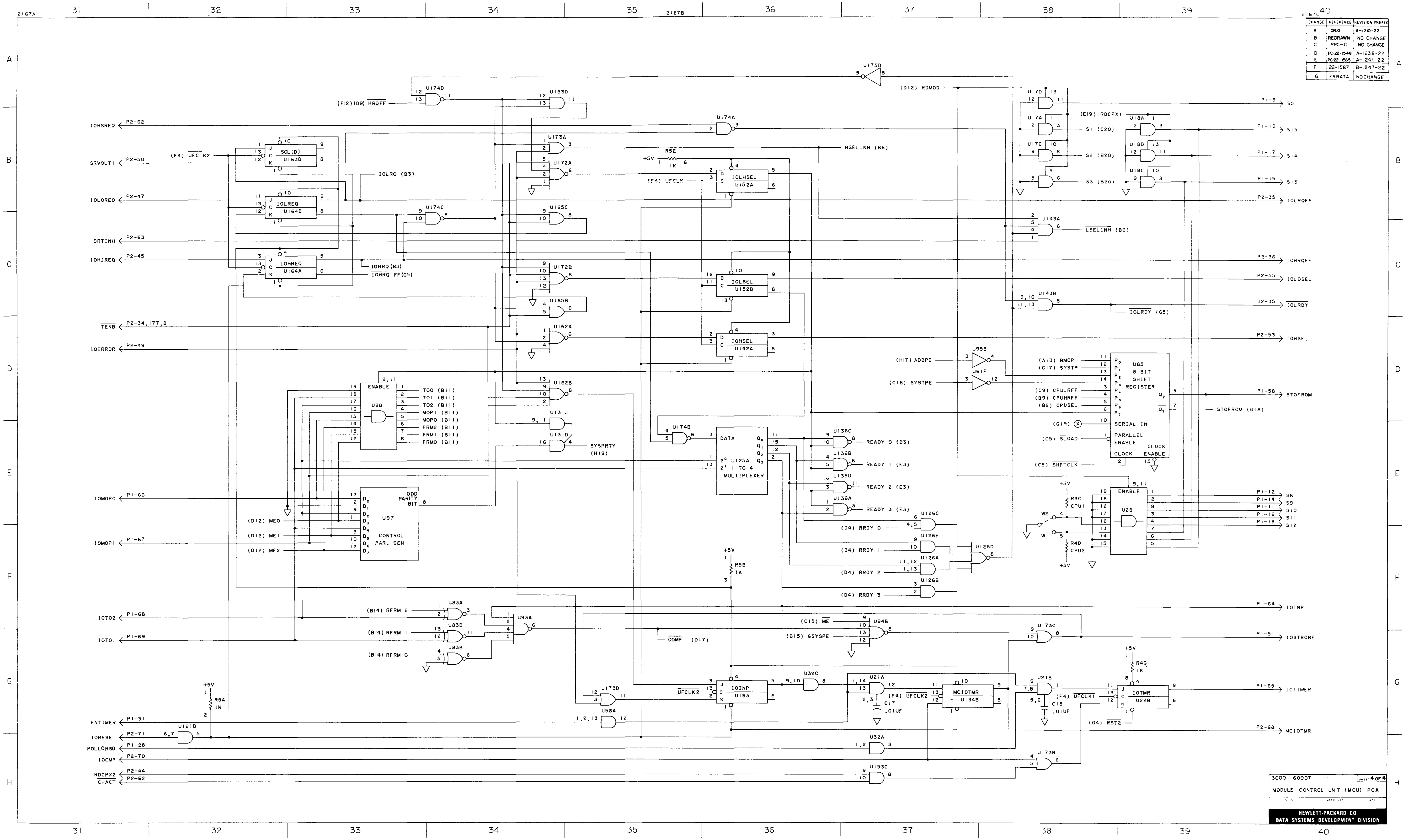
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	S03	1	READY00	1	—
2	COM	2	COM	2	—
3	S01	3	READY02	3	XXX
4	CPUIN	4	FROM00	4	—
5	RDCPX1	5	READY04	5	XXX
6	RMCUCPX1	6	FROM02	6	—
7	S02	7	READY06	7	XXX
8	U02	8	MOP01	8	—
9	S00	9	ENABLE01	9	XXX
10	U06	10	TO02	10	—
11	S10	11	ENABLE03	11	—
12	S08	12	FROM01	12	—
13		13	ENABLE05	13	—
14	S09	14	MOP00	14	—
15	S13	15	MCUD PE	15	—
16	S11	16	TO00	16	—
17	S14	17	MCU RST	17	—
18	S12	18	SYSPRTY	18	—
19	S15	19	READY01	19	—
20	+5V	20	+5V	20	—
21	DATAPE	21	READY03	21	—
22	MCUINT	22	TO01	22	—
23	ERFRZINH	23	READY05	23	—
24	CPUTIMER	24	UT01	24	—
25	RDOPND	25	ENABLE00	25	—
26	NOP1	26	UT02	26	—
27	INTRP	27	ENABLE02	27	—
28	POLLORSO	28	PT01	28	—
29	UNFRZ	29	ENABLE04	29	XXX
30	NXTDCD	30		30	—
31	ENTIMER	31		31	—
32	NXTFINH	32	PT02	32	—
33	JMPFRZ	33	SYS PE	33	XXX
34	STATUS01	34	TENB	34	—
35	MPIFRZ	35	IOLRQFF	35	—
36	U01	36	IOHRQFF	36	—
37	BMCUPRTY	37	SLOAD	37	XXX
38	MODINT	38	SHFTCLK	38	—
39	COM	39	COM	39	XXX
40	COM	40	COM	40	—
41	COR10	41	INSTSEL	41	XXX
42	CLOCKS	42		42	—
43	COR11	43	SRDYENBL	43	XXX
44	COR14	44	RDCPX2	44	—
45	COR15	45	IOHIREQ	45	XXX
46	COR13	46		46	—
47	TMRFRZI	47	IOLOREQ	47	XXX
48	U07	48		48	—
49	DATA	49	IOERROR	49	—
50	ST03	50	SRVOUT1	50	—
51	BUSOP	51	IOSTROBE		
52	NOP2	52	COR00		
53	RORT23	53	IOHSEL		
54	RORT24	54	COR01		
55	RORT27	55	IOLOSEL		
56	CCPX	56	COR02		
57	RORT26	57			
58	STOFROM	58	PSELECT		
59	RORT25	59			
60	+5V	60	+5V		
61	IOFRZ	61	CPULRFF		
62	IOHSREQ	62	CHACT		
63	DRTINH	63	CPULOSEL		
64	IOINP	64	CPUHRFF		
65	IOTIMER	65	ST01		
66	IOMOP00	66	OPNDSEL		
67	IOMOP01	67	ST00		
78	IOTO02	68	MCIOTMR		
69	IOTO01	69	ST02		
70	S04	70	IOCMP		
71	S07	71	IORESET		
72	MCUDPRTY	72	NEXT		
73	S06	73			
74	S05	74	NIP		
75	RDMOD	75			
76	CPUSEL	76	OPINP		
77	MDPARITY	77			
78	CLOCK	78	CPURST		
79	FREEZE	79			
80	COM	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0685	53	0141	86	0846	114	0424	144,145	0574
13	0371	54,55	0691	87	0842	115	0623	146	0696
14	0686	57	0574	88	0690	117	0617	147	0691
15	0141	58	0686			118	0755	148	0682
16-18	0846			91	0371				
		61	0424	92	0696	121	0535	151	0837
21	0844	62	0512	93	0373	122	0846	152	0693
22,23	0696	63	0696	94	0837	123	0617	153	0141
24	0681	64	0374	95	0424	124	0535	154,155	0574
25	0141	65	0759	96	0685	125	0843	156	0686
26	0739	66	0690	97	0842	126	0691	157,158	0843
27	0574	68	0686	98	0755	127	0262		
28	0755					128	0759	161,162	0837
		71	0608	101	0371			163,164	0696
32	0141	72	0696	102	0696	131	0755	165	0239
		73	0239	103	0617	132	0382	166	0681
42	0371	74	0371	104	0205	133,134	0696	167	0262
43	0696	75	0755	105	0374	135	0574	168	0759
44	0424	76,77	0690	106	0842	136	0682		
45	0696	78	0681	107	0262	137	0691	171,172	0837
46	0837			108	0759	138	0682	173	0205
47	0574	81	0683					174	0370
48	0688	82	0696	111	0372	141	0370	175	0683
		83	0617	112	0696	142	0693	176	0690
51	0239	84	0574	113	0373	143	0374	177	0375
52	0205	85	0262						





CHANGE | REFERENCE | REVISION PREFIX
A | ORIG | A-1210-22
B | REDRAWN | NO CHANGE
C | PPC-C | NO CHANGE
D | PC-22-1548 | A-1238-22
E | PC-22-1565 | A-1241-22
F | 22-1587 | B-1247-22
G | ERRATA | NOCHANGE
30001-60007
SHEET 4 OF 4
MODULE CONTROL UNIT (MCU) PCA
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-207

INPUT/OUTPUT PROCESSOR (IOP) PCA

30001-60008

SERIES 1210

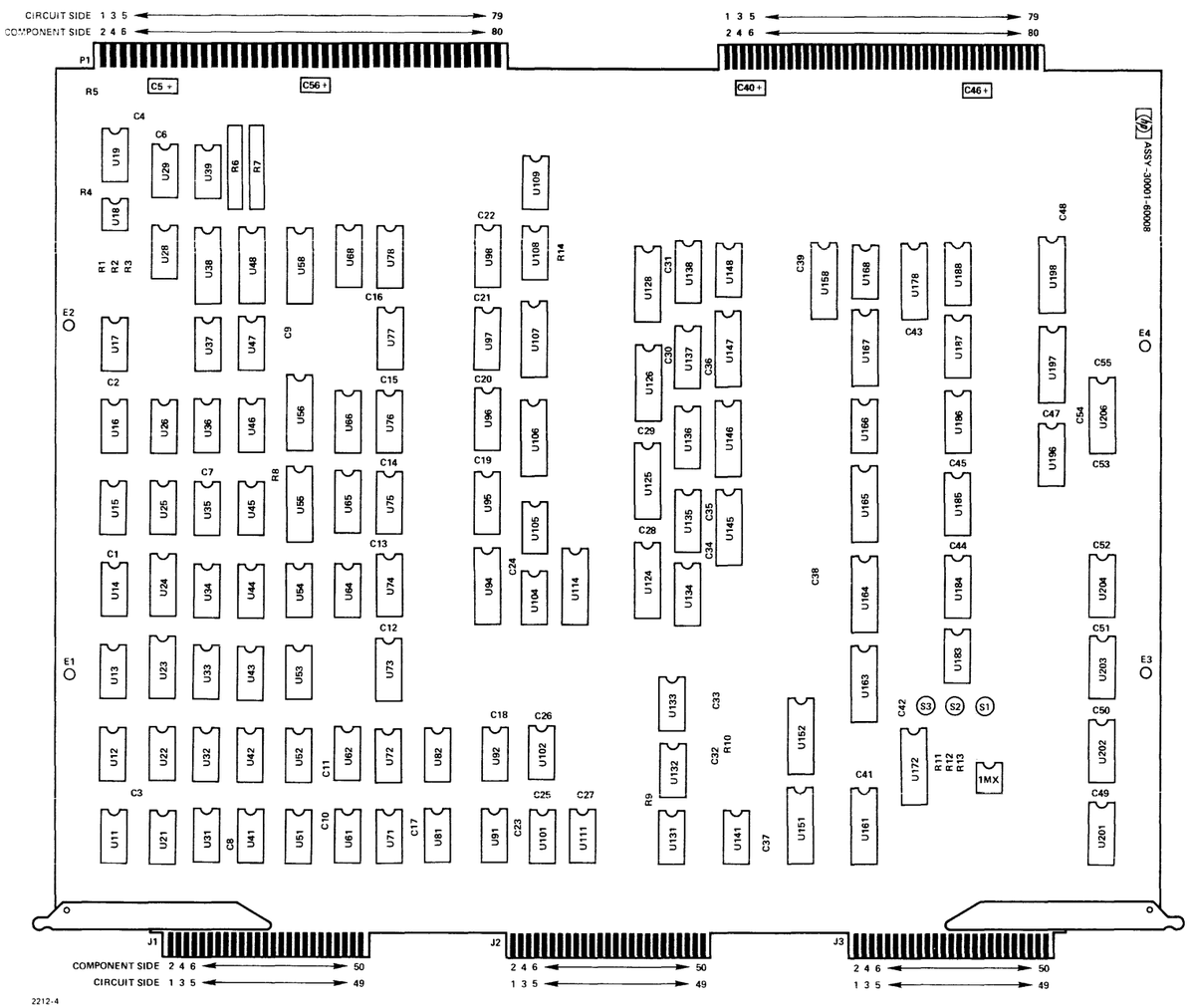
1305

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	DATAPOLL	1		1	XXX
2	DATAPOLR	2	COM	2	XXX
3	IOCMP	3	SYS PE	3	XXX
4	IOHIREQ	4		4	XXX
5	FLAG3	5	IOINP	5	XXX
6	IOMOP01	6	MCUDPE	6	XXX
7	IORESET	7	IOERROR	7	XXX
8	EXTINT	8	IOLRQFF	8	XXX
9	SIOP	9	IOILG	9	XXX
10	IOHSREQ	10	IOHRQFF	10	XXX
11	PFWARNB	11	CCPX	11	XXX
12	IOSTROBE	12	IOAPE	12	XXX
13	STATUS01	13	U08	13	XXX
14	SLOAD	14		14	XXX
15	SHFTCLK	15		15	XXX
16	DRTINH	16		16	XXX
17	OUTBND	17		17	XXX
18	OUTBNDR	18	RDIOM	18	—
19	SRVOUT1	19	IOFLG1	19	XXX
20	+5V	20	+5V	20	—
21	PFWARN	21	IOLOSEL	21	XXX
22	S00	22	DISPLAY	22	—
23	ENTIMER	23	IOTIMER	23	XXX
24	S01	24	IOHSEL	24	—
25	P1-4	25	IOMOP00	25	XXX
26	S02	26	CLFLAG03	26	—
27	P1-3	27	IOLOREQ	27	XXX
28	S03	28		28	—
29	PWR ON	29	MCIOTMR	29	XXX
30	POLLORSO	30		30	—
31		31	IOD PE	31	XXX
32	S04	32	IODPRTY	32	—
33	IORESET	33	IOCMD00	33	—
34	S05	34	IOCMD02	34	—
35	HSREQ	35	IOCMD01	35	—
36	S06	36	DEVNO01	36	—
37	P1-14	37	DEVNO00	37	—
38	S07	38	DEVNO02	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	SI	41	DEVNO03	41	—
42	S08	42	DEVNO05	42	—
43	SO	43	DEVNO04	43	—
44	S09	44	DEVNO06	44	—
45	MSKRTRN	45	DEVNO07	45	—
46	S10	46	IOD01	46	—
47		47	IOD00	47	—
48	S11	48	IOD02	48	—
49	MCUD01	49	IOD03	49	XXX
50	S12	50	IOD05	50	XXX
51	MCUD00	51	IOD04		
52	S13	52	IOD06		
53	MCUD03	53	IOD07		
54	S14	54	IOD09		
55	MCUD02	55	IOD08		
56	S15	56	IOD10		
57	MCUD05	57	IOD11		
58	ST04	58	IOD13		
59	MCUD04	59	IOD12		
60	+5V	60	+5V		
61	MCUD06	61	IOD15		
62	STIOM	62	IOD14		
63	MCUD07	63	INTREQ		
64	ST03	64	P3-45		
65	MCUD08	65	P3-48		
66	SF03	66	P3-47		
67	MCUD09	67	INTACK		
68	SF04	68			
69	MCUD10	69			
70	MCUD15	70			
71	MCUD11	71			
72	MCUDPRTY	72			
73	MCUD12	73			
74		74			
75	MCUD13	75	IOTO01		
76	IOFRZ	76	CHACT		
77	MCUD14	77	IOTO02		
78	CLOCKS	78	CPURST		
79	INTPOLL	79			
80	INTPOLLR	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0141	41	0512	91	0696	151,152,158	0755
12	0696	42	0685	92	0837	161,163-165	0755
13	0205	43	0696	94	0755	166	0842
14	745113	44	0681	95-98	0574	167	0755
15	0681	45	0688			168	0842
16	0685	46	0696	101	0375		
17	0696	47	0141	102	0205	172,178	0755
18	0535	48	0760	104	0683	183	0623
				105	0724	184	0574
19	0376	51,52	0696	106,107	0756	185-188	0716
		53	0685	108	0685		
21	0696	54	0239	109	0686	196	0574
22	0681	55	0760			197,198	0760
23,24	0262	56,58	0756	111	0375		
25	0141			114,124	0756	201-204	0574
26	0374	61	0205			206	0760
28,29	0690	62	0696	125	0755		
		64	0688	126	0756		
31	0683	65,66,68	0574	128	0755		
32	0691						
33	0385	71	0239	131-133	0685		
34	0681	72	0141	134-138	0301		
35	0685	73-78	0574				
36	0696			141	0683		
37	0374	81	0141	145-147	0759		
38	0756	82	0239	148	0690		
39	0512						



2212-4

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1662	A-1305-22	ALL
D	22-1715	B-1305-22	1

(D38) SI(D)
(D44) JMP
(F49) SRVOUT
(E44) IN/OUT BND
(D33) SIO ACK
(D44) DRT REQ
(B37) IOFLG I
(C39) D POLL
U24 8-BIT SHIFT REGISTER
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE
SLOAD ← P1-14
P1-9 → SIOP

(F44) DATA CYC
(E44) XERR
(B46) STO DRT
(B13) ECFF
(D48) CE
(D37) IOBENB
(F35) INT POLL
(G35) IACK
U23 8-BIT SHIFT REGISTER
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE

(E29) WCUD BUS
SHFTCLK ← P1-15
S-BUS (C12)
U98 4-BIT REGISTER
U97 4-BIT REGISTER
U96 4-BIT REGISTER
U95 4-BIT REGISTER
CLOCK
MR
INPUT ENABLE
OUTPUT ENABLE
CLK1 (E36)

U145
U147
U146
R10 1K +5V
U134
U138
U137
U136
U135
L ENABLE
U148A
U148B
U108C
IOINP ← P2-5
STO IOD (D13)
CLOCKS (E31)

IOD PRTY ← P2-32
IOD00 ← P2-47
IOD01 ← P2-46
IOD02 ← P2-48
IOD03 ← P2-49
IOD04 ← P2-51
IOD05 ← P2-50
IOD06 ← P2-52
IOD07 ← P2-53
IOD08 ← P2-55
IOD09 ← P2-54
IOD10 ← P2-56
IOD11 ← P2-57
IOD12 ← P2-59
IOD13 ← P2-58
IOD14 ← P2-62
IOD15 ← P2-61
U206
U198
U197
ENABLE
(E46) IODE
W-BUS (A22)

DRTG (D36)
U114
U126
U124
U107
U106
(B36) DDG

E BUS (D21)
F BUS (D21)
G BUS (B21)
H BUS (B21)

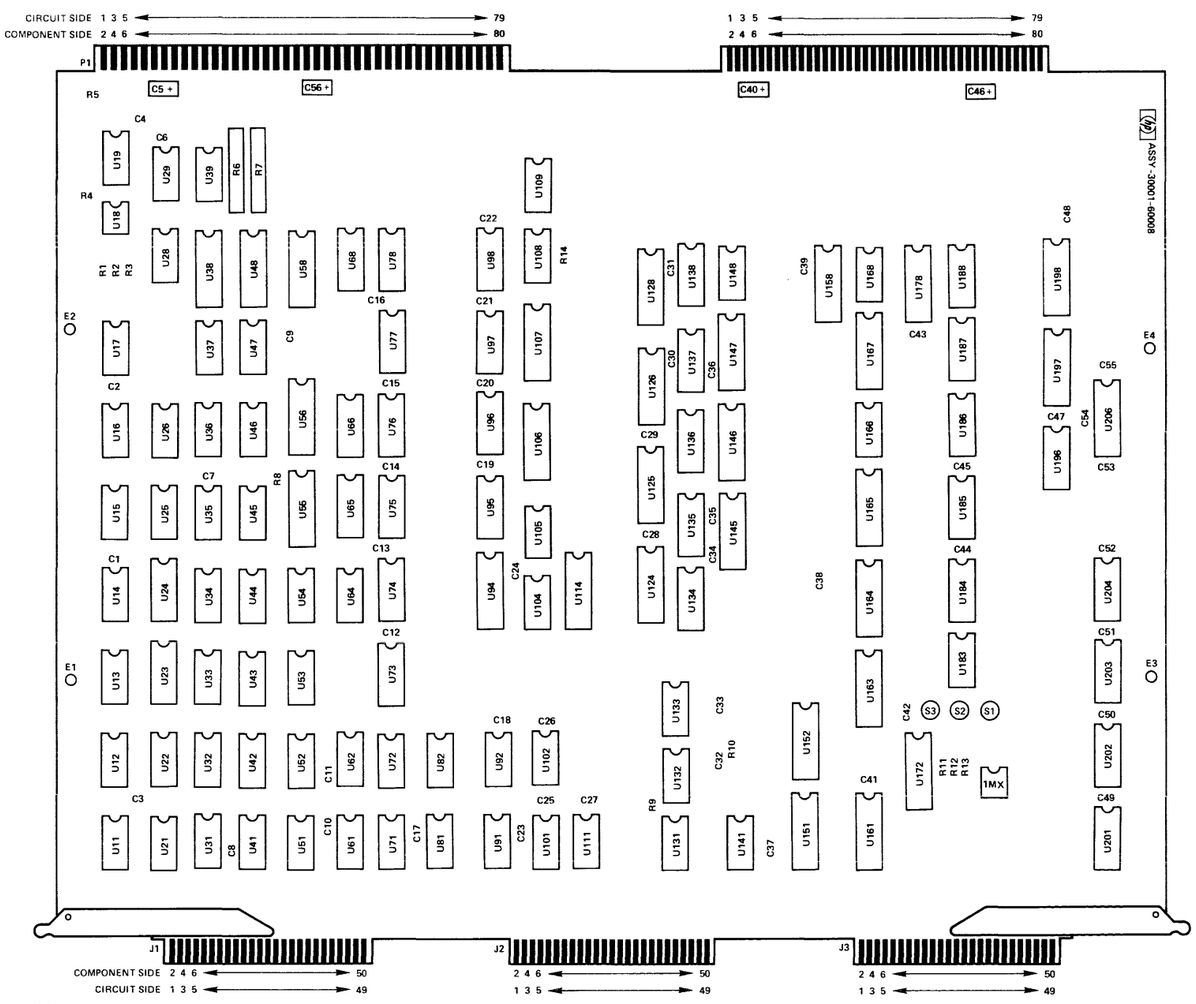
30001-60008-S TITLE	SHEET 1 OF 5
INPUT/OUTPUT PROCESSOR (IOP) CARD	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION	

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	DATAPOLL	1		1	XXX
2	DATAPOLR	2	COM	2	XXX
3	IOCMP	3	SYS PE	3	XXX
4	IOHIREQ	4		4	XXX
5	FLAG3	5	IOINP	5	XXX
6	IOMOP01	6	MCUDPE	6	XXX
7	IORESET	7	IOERROR	7	XXX
8	EXTINT	8	IOLRQFF	8	XXX
9	SIOP	9	IOILG	9	XXX
10	IOHSREQ	10	IOHRQFF	10	XXX
11	PFWARNB	11	CCPX	11	XXX
12	IOSTROBE	12	IOAPE	12	XXX
13	STATUS01	13	U08	13	XXX
14	SLOAD	14		14	XXX
15	SHFTCLK	15		15	XXX
16	DRTINH	16		16	XXX
17	OUTBND	17		17	XXX
18	OUTBNDR	18	RDIOM	18	—
19	SRVOUT1	19	IOFLG1	19	XXX
20	+5V	20	+5V	20	—
21	PFWARN	21	IOLOSEL	21	XXX
22	S00	22	DISPLAY	22	—
23	ENTIMER	23	IOTIMER	23	XXX
24	S01	24	IOHSEL	24	—
25	P1-4	25	IOMOP00	25	XXX
26	S02	26	CLFLAG03	26	—
27	P1-3	27	IOLOREQ	27	XXX
28	S03	28		28	—
29	PWR ON	29	MCIOTMR	29	XXX
30	POLLORSO	30		30	—
31		31	IOD PE	31	XXX
32	S04	32	IODPRTY	32	—
33	IORESET	33	IOCMD00	33	—
34	S05	34	IOCMD02	34	—
35	HSREQ	35	IOCMD01	35	—
36	S06	36	DEVNO01	36	—
37	P1-14	37	DEVNO00	37	—
38	S07	38	DEVNO02	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	SI	41	DEVNO03	41	—
42	S08	42	DEVNO05	42	—
43	SO	43	DEVNO04	43	—
44	S09	44	DEVNO06	44	—
45	MSKRTRN	45	DEVNO07	45	—
46	S10	46	IOD01	46	—
47		47	IOD00	47	—
48	S11	48	IOD02	48	—
49	MCUD01	49	IOD03	49	XXX
50	S12	50	IOD05	50	XXX
51	MCUD00	51	IOD04		
52	S13	52	IOD06		
53	MCUD03	53	IOD07		
54	S14	54	IOD09		
55	MCUD02	55	IOD08		
56	S15	56	IOD10		
57	MCUD05	57	IOD11		
58	ST04	58	IOD13		
59	MCUD04	59	IOD12		
60	+5V	60	+5V		
61	MCUD06	61	IOD15		
62	STIOM	62	IOD14		
63	MCUD07	63	INTREQ		
64	ST03	64	P3-45		
65	MCUD08	65	P3-48		
66	SF03	66	P3-47		
67	MCUD09	67	INTACK		
68	SF04	68			
69	MCUD10	69			
70	MCUD15	70			
71	MCUD11	71			
72	MCUDPRTY	72			
73	MCUD12	73			
74		74			
75	MCUD13	75	IOTO01		
76	IOFRZ	76	CHACT		
77	MCUD14	77	IOTO02		
78	CLOCKS	78	CPURST		
79	INTPOLL	79			
80	INTPOLLR	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0141	41	0512	91	0696	151,152,158	0755
12	0696	42	0685	92	0837	161,163-165	0755
13	0205	43	0696	94	0755	166	0842
14	745113	44	0681	95-98	0574	167	0755
15	0681	45	0688			168	0842
16	0685	46	0696	101	0375		
17	0696	47	0141	102	0205	172,178	0755
18	0535	48	0760	104	0683	183	0623
				105	0724	184	0574
19	0376	51,52	0696	106,107	0756	185-188	0716
		53	0685	108	0685		
21	0696	54	0239	109	0686	196	0574
22	0681	55	0760			197,198	0760
23,24	0262	56,58	0756	111	0375		
25	0141			114,124	0756	201-204	0574
26	0374	61	0205			206	0760
28,29	0690	62	0696	125	0755		
		64	0688	126	0756		
31	0683	65,66,68	0574	128	0755		
32	0691						
33	0385	71	0239	131-133	0685		
34	0681	72	0141	134-138	0301		
35	0685	73-78	0574				
36	0696			141	0683		
37	0374	81	0141	145-147	0759		
38	0756	82	0239	148	0690		
39	0512						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22
D	22-1715	B-1305-22

U71C
(G29)
R10
+5V
1K
U145
SYS PE P2-3
MCUD PE P2-6
U81D
U82D
IOLOSEL(C28)
IOLOSEL P2-21
ERR CYC U41B
(E36)CLK1
(F39)RST1
ECFF (B3) (G42)
ILLEG ADDR U91B
APEFF U91A
(E36)CLK1
(C47)IOCMP
ILG(F42)
APEFF (F44)
U92B
U141A
ERR (D48)
P2-9 IOILG
P2-7 IOERROR
P2-12 IOAPE
S BUS(C1)(E27)
SO0 P1-22
SO1 P1-24
SO2 P1-26
SO3 P1-28
SO4 P1-32
SO5 P1-34
SO6 P1-36
SO7 P1-38
SO8 P1-42
SO9 P1-44
SO10 P1-46
SO11 P1-48
SO12 P1-50
SO13 P1-52
SO14 P1-54
SO15 P1-56
U78 4-BIT REGISTER
U77 4-BIT REGISTER
U76 4-BIT REGISTER
U75 4-BIT REGISTER
U65 4-BIT REGISTER
U66 4-BIT REGISTER
U68 4-BIT REGISTER
U74 4-BIT REGISTER
U73 4-BIT REGISTER
CLK2 (E36)
CLOCK MR
INPUT ENABLE OUTPUT ENABLE
ST 4 P1-58
ST 3 P1-64
STIOM P1-62
U105A 2-BIT DECODER
STO IOA(C32)
STMSK
STO IOD(H2) (B32)
SF 4 P1-68
SF 3 P1-66
RDIOM P2-18
U105B 2-BIT DECODER
RDDAC (G22)
RDIOA
RDIOD (H22)
ROMASR
MSKRTRN P1-45
DEVNO 08 P2-37
DEVNO 01 P2-36
DEVNO 02 P2-38
DEVNO 03 P2-41
DEVNO 04 P2-43
DEVNO 05 P2-42
DEVNO 06 P2-44
DEVNO 07 P2-45
U55 ENABLE
R8 1K +5V
U54D U54C U54A U54B U64A
≠0 (G34)
U56 ENABLE
DAG (C36)
U82A U47 U48 U58 U37B
IOFLG1 (B37)
MSK RTRN (G42)
P2-37 DEVNO 00
P2-36 DEVNO 01
P2-38 DEVNO 02
P2-41 DEVNO 03
P2-43 DEVNO 04
P2-42 DEVNO 05
P2-44 DEVNO 06
P2-45 DEVNO 07
P2-34 IOCMD 02
P2-35 IOCMD 01
P2-33 IOCMD 00
U74 4-BIT REGISTER
U73 4-BIT REGISTER
U94 ENABLE
U104C
(F36)IENB
J2-2 J2-4 J2-6 J2-8 J2-10 J2-12 J2-14 J2-16
J2-17 J2-19 J2-21 J2-23 J2-25 J2-27 J2-29 J2-31
J2-49 J2-50
R9 1K +5V
U101 U111
U119B 4-BIT REGISTER
(E37)CLK2
AENB (B45)
P2-75 IOTO1
P2-77 IOTO2

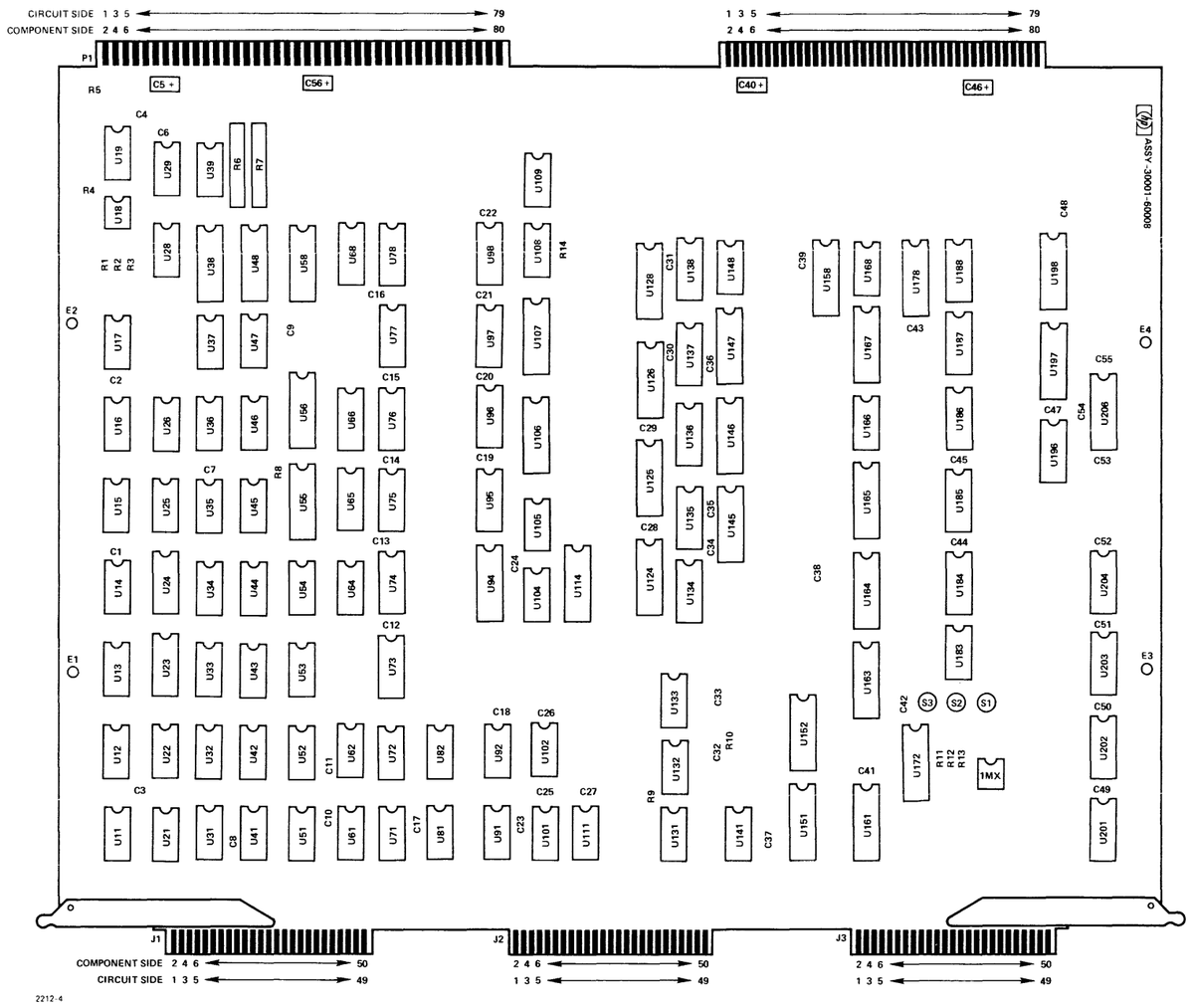
30001-60008—S TITLE SHEET 2 OF 5
INPUT/OUTPUT PROCESSOR (IOP) CARD
ENGINEER APPROVED DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	DATAPOLL	1		1	XXX
2	DATAPOLR	2	COM	2	XXX
3	IOCMP	3	SYS PE	3	XXX
4	IOHIREQ	4		4	XXX
5	FLAG3	5	IOINP	5	XXX
6	IOMOP01	6	MCUDPE	6	XXX
7	IORESET	7	IOERROR	7	XXX
8	EXTINT	8	IOLRQFF	8	XXX
9	SIOP	9	IOILG	9	XXX
10	IOHSREQ	10	IOHRQFF	10	XXX
11	PFWARNB	11	CCPX	11	XXX
12	IOSTROBE	12	IOAPE	12	XXX
13	STATUS01	13	U08	13	XXX
14	SLOAD	14		14	XXX
15	SHFTCLK	15		15	XXX
16	DRTINH	16		16	XXX
17	OUTBND	17		17	XXX
18	OUTBNDR	18	RDIOM	18	—
19	SRVOUT1	19	IOFLG1	19	XXX
20	+5V	20	+5V	20	—
21	PFWARN	21	IOLOSEL	21	XXX
22	S00	22	DISPLAY	22	—
23	ENTIMER	23	IOTIMER	23	XXX
24	S01	24	IOHSEL	24	—
25	P1-4	25	IOMOP00	25	XXX
26	S02	26	CLFLAG03	26	—
27	P1-3	27	IOLOREQ	27	XXX
28	S03	28		28	—
29	PWR ON	29	MCIOTMR	29	XXX
30	POLLORSO	30		30	—
31		31	IOD PE	31	XXX
32	S04	32	IODPRTY	32	—
33	IORESET	33	IOCMD00	33	—
34	S05	34	IOCMD02	34	—
35	HSREQ	35	IOCMD01	35	—
36	S06	36	DEVNO01	36	—
37	P1-14	37	DEVNO00	37	—
38	S07	38	DEVNO02	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	SI	41	DEVNO03	41	—
42	S08	42	DEVNO05	42	—
43	SO	43	DEVNO04	43	—
44	S09	44	DEVNO06	44	—
45	MSKRTRN	45	DEVNO07	45	—
46	S10	46	IOD01	46	—
47		47	IOD00	47	—
48	S11	48	IOD02	48	—
49	MCUD01	49	IOD03	49	XXX
50	S12	50	IOD05	50	XXX
51	MCUD00	51	IOD04		
52	S13	52	IOD06		
53	MCUD03	53	IOD07		
54	S14	54	IOD09		
55	MCUD02	55	IOD08		
56	S15	56	IOD10		
57	MCUD05	57	IOD11		
58	ST04	58	IOD13		
59	MCUD04	59	IOD12		
60	+5V	60	+5V		
61	MCUD06	61	IOD15		
62	STIOM	62	IOD14		
63	MCUD07	63	INTREQ		
64	ST03	64	P3-45		
65	MCUD08	65	P3-48		
66	SF03	66	P3-47		
67	MCUD09	67	INTACK		
68	SF04	68			
69	MCUD10	69			
70	MCUD15	70			
71	MCUD11	71			
72	MCUDPRTY	72			
73	MCUD12	73			
74		74			
75	MCUD13	75	IOTO01		
76	IOFRZ	76	CHACT		
77	MCUD14	77	IOTO02		
78	CLOCKS	78	CPURST		
79	INTPOLL	79			
80	INTPOLLR	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0141	41	0512	91	0696	151,152,158	0755
12	0696	42	0685	92	0837	161,163-165	0755
13	0205	43	0696	94	0755	166	0842
14	745113	44	0681	95-98	0574	167	0755
15	0681	45	0688			168	0842
16	0685	46	0696	101	0375		
17	0696	47	0141	102	0205	172,178	0755
18	0535	48	0760	104	0683	183	0623
				105	0724	184	0574
19	0376	51,52	0696	106,107	0756	185-188	0716
		53	0685	108	0685		
21	0696	54	0239	109	0686	196	0574
22	0681	55	0760			197,198	0760
23,24	0262	56,58	0756	111	0375		
25	0141			114,124	0756	201-204	0574
26	0374	61	0205			206	0760
28,29	0690	62	0696	125	0755		
		64	0688	126	0756		
31	0683	65,66,68	0574	128	0755		
32	0691						
33	0385	71	0239	131-133	0685		
34	0681	72	0141	134-138	0301		
35	0685	73-78	0574				
36	0696			141	0683		
37	0374	81	0141	145-147	0759		
38	0756	82	0239	148	0690		
39	0512						



2212-4

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22
D	22-1715	B-1305-22

IOHSEL ← P2-24

W BUS (B9)

G BUS (H6)

H BUS (H6)

E BUS (G6)

F BUS (G6)

(E46)STODRT

(D48)CE

(E48)LDENB

(E37)CLK 2

DISPLAY ← P2-22

IOLRQFF ← P2-8

(E13) RDDIAG

(E13) RDIOD

CLK2 (E37)

AENB (B45)

IOLOSEL (B12)

S BUS (C13)

MCUD BUS (C2)

U184 4-BIT REGISTER

U185 4-BIT BINARY COUNTER

U186 4-BIT BINARY COUNTER

U187 4-BIT BINARY COUNTER

U188 4-BIT BINARY COUNTER

U125 ENABLE

U128 ENABLE

U166A ODD PARITY BIT GENERATOR

U168 ODD PARITY BIT GENERATOR

U166B

U164 ENABLE

U163 ENABLE

U104D

U104A

U104E

U196 4-BIT REGISTER

U204 4-BIT REGISTER

U203 4-BIT REGISTER

U201 4-BIT REGISTER

U202 4-BIT REGISTER

CCW

S1

S2

S3

U172 ENABLE

U161 ENABLE

U183 4-BIT COMPARATOR

STROBE

W1

W2

W3

+5V

R13

R12

R11

U158

U167 ENABLE

U165 ENABLE

U178

U152 ENABLE

U151 ENABLE

P1-72 MCUD PRTY

P1-51 MCUD00

P1-49 MCUD01

P1-55 MCUD02

P1-53 MCUD03

P1-59 MCUD04

P1-57 MCUD05

P1-61 MCUD06

P1-63 MCUD07

P1-65 MCUD08

P1-67 MCUD09

P1-69 MCUD10

P1-71 MCUD11

P1-73 MCUD12

P1-75 MCUD13

P1-77 MCUD14

P1-70 MCUD15

U141F

U141E

U141D

U131B

U131A

U132C

U132B

U132A

U133C

U133B

U133A

U131C

U141C

J2-9

J2-11

J2-13

J2-15

J2-1

J2-3

J2-5

J2-7

(A13)

30001-60008-S TITLE

SHEET 30F5

INPUT/OUTPUT PROCESSOR (IOP) CARD

ENGINEER | APPROVED | DATE

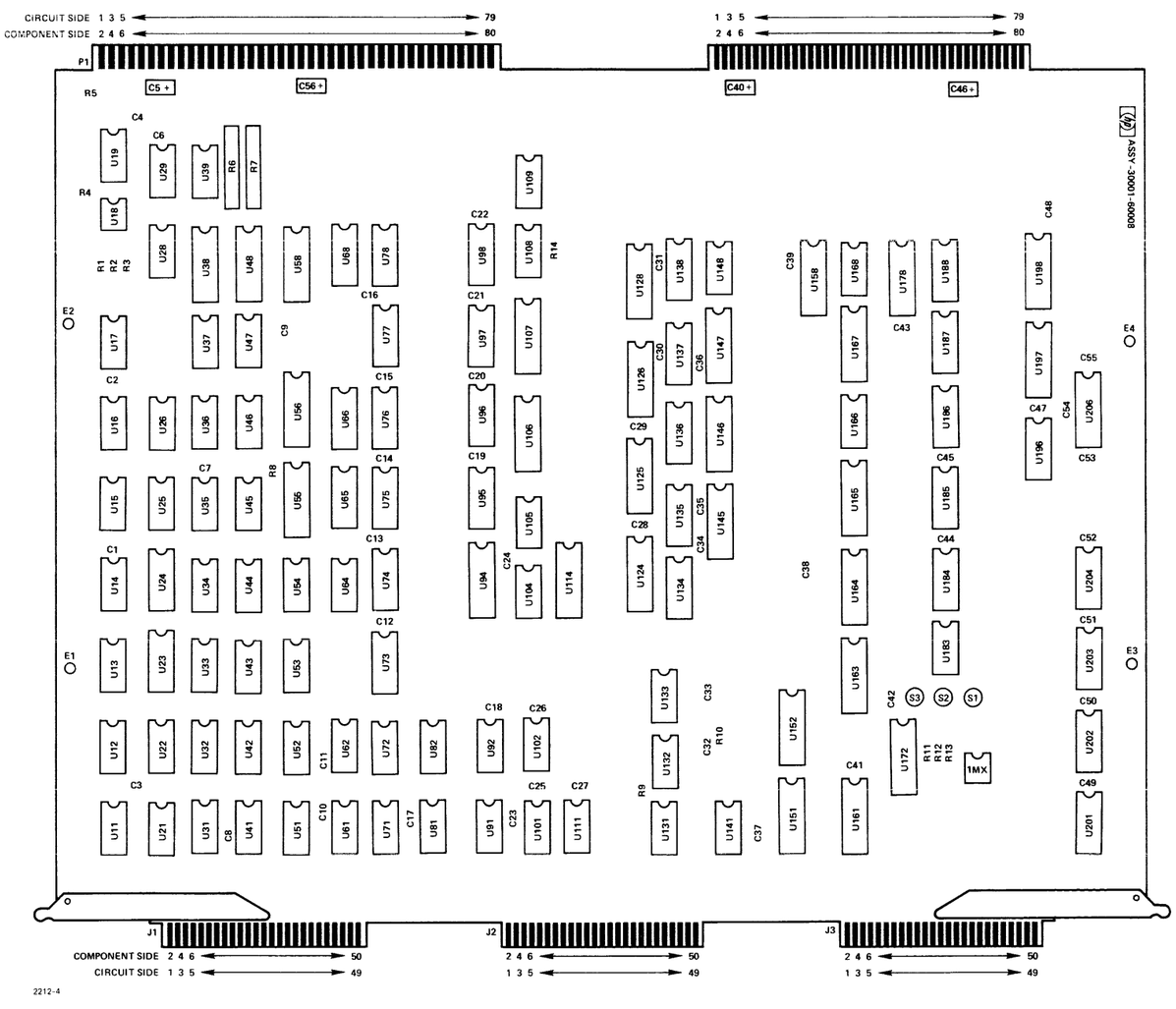
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	DATAPOLL	1		1	XXX
2	DATAPOLR	2	COM	2	XXX
3	IOCMP	3	SYS PE	3	XXX
4	IOHIREQ	4		4	XXX
5	FLAG3	5	IOINP	5	XXX
6	IOMOP01	6	MCUDPE	6	XXX
7	IORESET	7	IOERROR	7	XXX
8	EXTINT	8	IOLRQFF	8	XXX
9	SIOP	9	IOILG	9	XXX
10	IOHSREQ	10	IOHRQFF	10	XXX
11	PFWARNB	11	CCPX	11	XXX
12	IOSTROBE	12	IOAPE	12	XXX
13	STATUS01	13	U08	13	XXX
14	SLOAD	14		14	XXX
15	SHFTCLK	15		15	XXX
16	DRTINH	16		16	XXX
17	OUTBND	17		17	XXX
18	OUTBNDR	18	RDIOM	18	—
19	SRVOUT1	19	IOFLG1	19	XXX
20	+5V	20	+5V	20	—
21	PFWARN	21	IOLOSEL	21	XXX
22	S00	22	DISPLAY	22	—
23	ENTIMER	23	IOTIMER	23	XXX
24	S01	24	IOHSEL	24	—
25	P1-4	25	IOMOP00	25	XXX
26	S02	26	CLFLAG03	26	—
27	P1-3	27	IOLOREQ	27	XXX
28	S03	28		28	—
29	PWR ON	29	MCIOTMR	29	XXX
30	POLLORSO	30		30	—
31		31	IOD PE	31	XXX
32	S04	32	IODPRTY	32	—
33	IORESET	33	IOCMD00	33	—
34	S05	34	IOCMD02	34	—
35	HSREQ	35	IOCMD01	35	—
36	S06	36	DEVNO01	36	—
37	P1-14	37	DEVNO00	37	—
38	S07	38	DEVNO02	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	SI	41	DEVNO03	41	—
42	S08	42	DEVNO05	42	—
43	SO	43	DEVNO04	43	—
44	S09	44	DEVNO06	44	—
45	MSKRTRN	45	DEVNO07	45	—
46	S10	46	IOD01	46	—
47		47	IOD00	47	—
48	S11	48	IOD02	48	—
49	MCUD01	49	IOD03	49	XXX
50	S12	50	IOD05	50	XXX
51	MCUD00	51	IOD04		
52	S13	52	IOD06		
53	MCUD03	53	IOD07		
54	S14	54	IOD09		
55	MCUD02	55	IOD08		
56	S15	56	IOD10		
57	MCUD05	57	IOD11		
58	ST04	58	IOD13		
59	MCUD04	59	IOD12		
60	+5V	60	+5V		
61	MCUD06	61	IOD15		
62	STIOM	62	IOD14		
63	MCUD07	63	INTREQ		
64	ST03	64	P3-45		
65	MCUD08	65	P3-48		
66	SF03	66	P3-47		
67	MCUD09	67	INTACK		
68	SF04	68			
69	MCUD10	69			
70	MCUD15	70			
71	MCUD11	71			
72	MCUDPRTY	72			
73	MCUD12	73			
74		74			
75	MCUD13	75	IOTO01		
76	IOFRZ	76	CHACT		
77	MCUD14	77	IOTO02		
78	CLOCKS	78	CPURST		
79	INTPOLL	79			
80	INTPOLLR	80	COM		

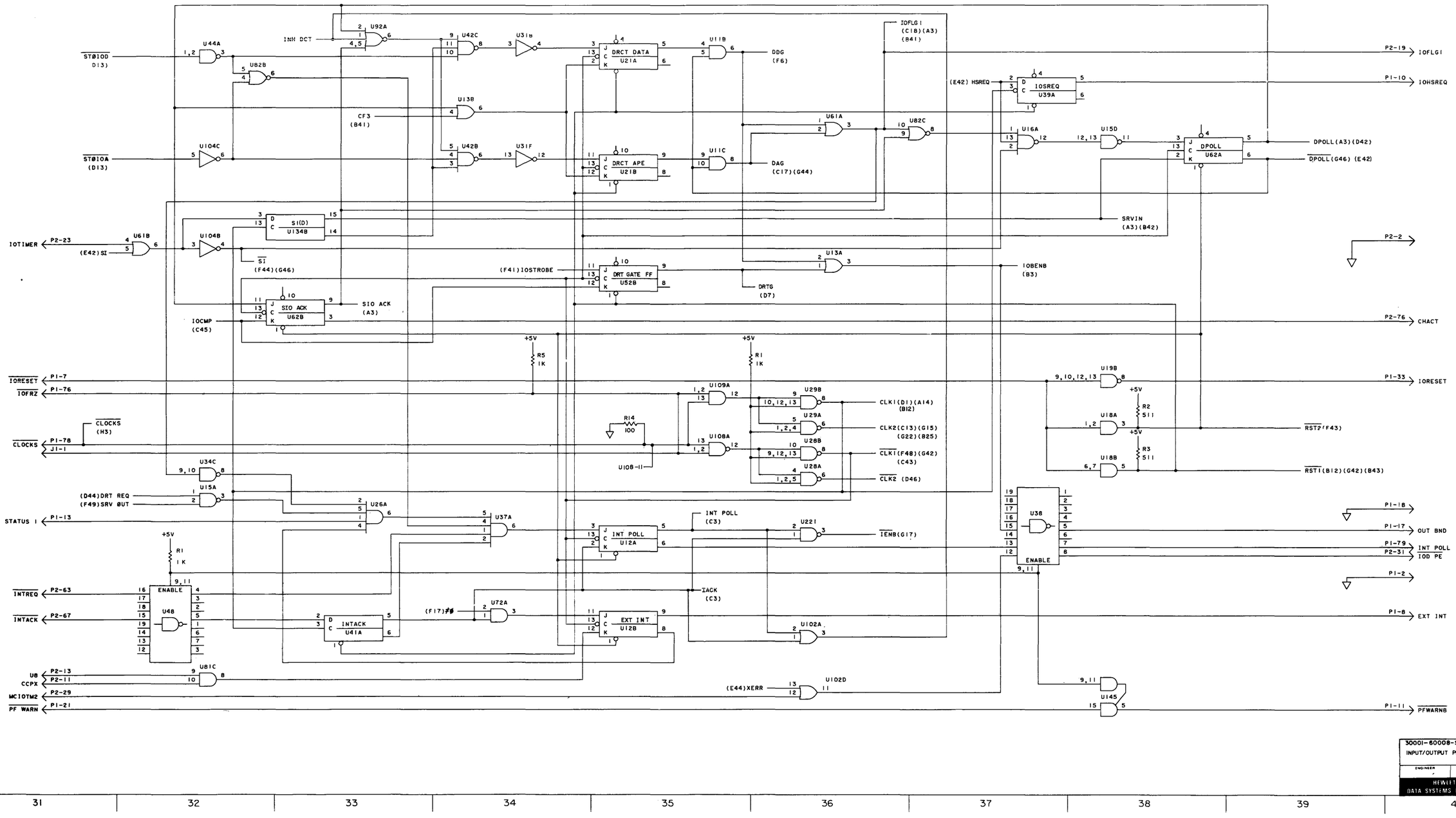
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0141	41	0512	91	0696	151,152,158	0755
12	0696	42	0685	92	0837	161,163-165	0755
13	0205	43	0696	94	0755	166	0842
14	745113	44	0681	95-98	0574	167	0755
15	0681	45	0688			168	0842
16	0685	46	0696	101	0375		
17	0696	47	0141	102	0205	172,178	0755
18	0535	48	0760	104	0683	183	0623
		51,52	0696	105	0724	184	0574
19	0376	53	0685	106,107	0756	185-188	0716
		54	0239	108	0685		
21	0696	55	0760	109	0686	196	0574
22	0681	56,58	0756			197,198	0760
23,24	0262			111	0375		
25	0141	61	0205	114,124	0756	201-204	0574
26	0374	62	0696			206	0760
28,29	0690	64	0688	125	0755		
		65,66,68	0574	126	0756		
31	0683			128	0755		
32	0691	71	0239				
33	0385	72	0141	131-133	0685		
34	0681	73-78	0574	134-138	0301		
35	0685						
36	0696	81	0141	141	0683		
37	0374	82	0239	145-147	0759		
38	0756			148	0690		
39	0512						



2212-4

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22
D	22-1751	B-1305-22



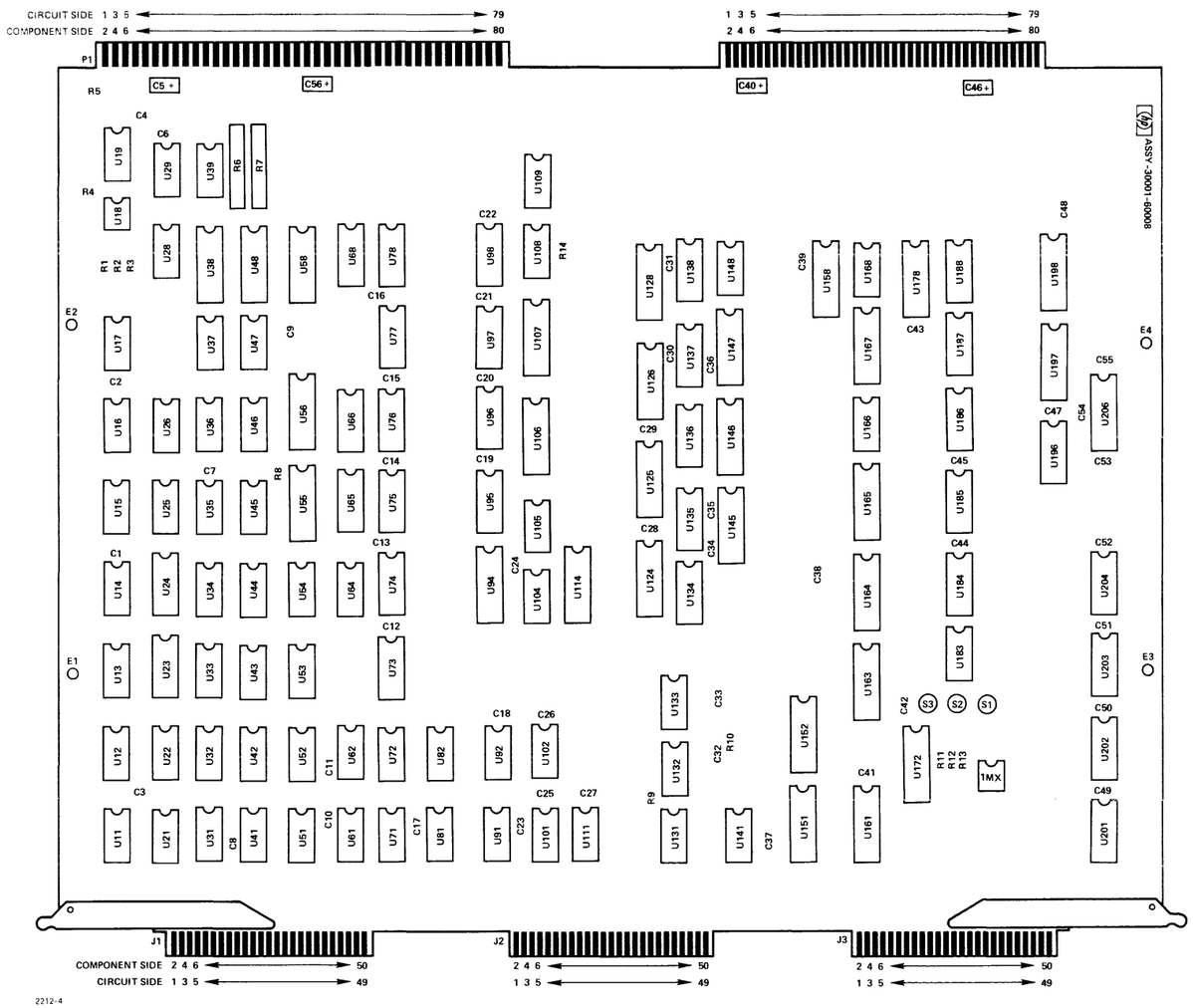
30001-60008-S TITLE	SHEET 4 OF 5
INPUT/OUTPUT PROCESSOR (IOP) CARD	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION	

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	J2 PIN	J2 SIGNAL
1	DATAPOLL	1		1	XXX
2	DATAPOLR	2	COM	2	XXX
3	IOCMP	3	SYS PE	3	XXX
4	IOHIREQ	4		4	XXX
5	FLAG3	5	IOINP	5	XXX
6	IOMOP01	6	MCUDPE	6	XXX
7	IORESET	7	IOERROR	7	XXX
8	EXTINT	8	IOLRQFF	8	XXX
9	SIOP	9	IOILG	9	XXX
10	IOHSREQ	10	IOHRQFF	10	XXX
11	PFWARNB	11	CCPX	11	XXX
12	IOSTROBE	12	IOAPE	12	XXX
13	STATUS01	13	U08	13	XXX
14	SLOAD	14		14	XXX
15	SHFTCLK	15		15	XXX
16	DRTINH	16		16	XXX
17	OUTBND	17		17	XXX
18	OUTBNDR	18	RDIOM	18	—
19	SRVOUT1	19	IOFLG1	19	XXX
20	+5V	20	+5V	20	—
21	PFWARN	21	IOLOSEL	21	XXX
22	S00	22	DISPLAY	22	—
23	ENTIMER	23	IOTIMER	23	XXX
24	S01	24	IOHSEL	24	—
25	P1-4	25	IOMOP00	25	XXX
26	S02	26	CLFLAG03	26	—
27	P1-3	27	IOLOREQ	27	XXX
28	S03	28		28	—
29	PWR ON	29	MCIOTMR	29	XXX
30	POLLORSO	30		30	—
31		31	IOD PE	31	XXX
32	S04	32	IODPRTY	32	—
33	IORESET	33	IOCMD00	33	—
34	S05	34	IOCMD02	34	—
35	HSREQ	35	IOCMD01	35	—
36	S06	36	DEVNO01	36	—
37	P1-14	37	DEVNO00	37	—
38	S07	38	DEVNO02	38	—
39	COM	39	COM	39	—
40	COM	40	COM	40	—
41	SI	41	DEVNO03	41	—
42	S08	42	DEVNO05	42	—
43	SO	43	DEVNO04	43	—
44	S09	44	DEVNO06	44	—
45	MSKRTRN	45	DEVNO07	45	—
46	S10	46	IOD01	46	—
47		47	IOD00	47	—
48	S11	48	IOD02	48	—
49	MCUD01	49	IOD03	49	XXX
50	S12	50	IOD05	50	XXX
51	MCUD00	51	IOD04		
52	S13	52	IOD06		
53	MCUD03	53	IOD07		
54	S14	54	IOD09		
55	MCUD02	55	IOD08		
56	S15	56	IOD10		
57	MCUD05	57	IOD11		
58	ST04	58	IOD13		
59	MCUD04	59	IOD12		
60	+5V	60	+5V		
61	MCUD06	61	IOD15		
62	STIOM	62	IOD14		
63	MCUD07	63	INTREQ		
64	ST03	64	P3-45		
65	MCUD08	65	P3-48		
66	SF03	66	P3-47		
67	MCUD09	67	INTACK		
68	SF04	68			
69	MCUD10	69			
70	MCUD15	70			
71	MCUD11	71			
72	MCUDPRTY	72			
73	MCUD12	73			
74		74			
75	MCUD13	75	IOTO01		
76	IOFRZ	76	CHACT		
77	MCUD14	77	IOTO02		
78	CLOCKS	78	CPURST		
79	INTPOLL	79			
80	INTPOLLR	80	COM		

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0141	41	0512	91	0696	151,152,158	0755
12	0696	42	0685	92	0837	161,163-165	0755
13	0205	43	0696	94	0755	166	0842
14	745113	44	0681	95-98	0574	167	0755
15	0681	45	0688			168	0842
16	0685	46	0696	101	0375		
17	0696	47	0141	102	0205	172,178	0755
18	0535	48	0760	104	0683	183	0623
				105	0724	184	0574
19	0376	51,52	0696	106,107	0756	185-188	0716
		53	0685	108	0685		
21	0696	54	0239	109	0686	196	0574
22	0681	55	0760			197,198	0760
23,24	0262	56,58	0756	111	0375		
25	0141			114,124	0756	201-204	0574
26	0374	61	0205			206	0760
28,29	0690	62	0696	125	0755		
		64	0688	126	0756		
31	0683	65,66,68	0574	128	0755		
32	0691						
33	0385	71	0239	131-133	0685		
34	0681	72	0141	134-138	0301		
35	0685	73-78	0574				
36	0696			141	0683		
37	0374	81	0141	145-147	0759		
38	0756	82	0239	148	0690		
39	0512						



2212-4

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22
D	22-1715	B-1305-22	

CLFLAG 3 ← P2-26 ← CF3 (C33)

(B37) IOFLG I

(D38) SI(D)

IOHROFF ← P2-10

(C39)DPOLL

+5V R1 1K

(C39)$\overline{POLL}$ U38

$\overline{IOCMD2}$ P2-34
$\overline{IOCMD1}$ P2-35
$\overline{IOCMD0}$ P2-33
$\overline{HSREQ}$ ← P1-35
$\overline{SI}$ ← P1-41
ENABLE U48 → JMP, DRT FETCH, MEMENO, HSREQ (B37), SI (D31)

(A15) $\overline{IOILG}$ U22B

IOSTROBE ← P1-12 ← IOSTROBE(D34)

(B13) ECFF
(F37)CLK1
(C47)IOCMP
MCU CMP U51A
(F39)$\overline{RST1}$

(C19)MSK RTRN

U102B → FLAG3 U51B → P1-5 FLAG3

(F39)$\overline{RST1}$

U26B → U71B → $\overline{AENB}$(H15)

U61C → P2-27 IOLOREQ

U72C → U11A → $\overline{CLK1}$ (F37) → IO CMP U52A → P1-3 IOCMP

IOCMP(B14)(D32)(G42) → U72B

U41B

U81B → U47B → JMP U36A

JMP (A3) → U25B → U34B → U44B → CE U14A → CE(B3)(E22)

U35A, U35B, U34A → P1-4 IOHIREQ

(B18)$\overline{ERR}$

U25A

U47C → DRT 1 U36B → DRT REQ (A3)(F31)

U11D → $\overline{CLK2}$ (F37) → LOREQ INIT U43A

U32C 4,5,6

P1-16 $\overline{DRT\ INH}$

P1-1 DATA POLL

STO DRT(B3)(C21) → DRT 2 U43B → IODE (C9)

U13D → P1-6 IOMOP1

U31E → P2-25 IOMOP0

U47A → MEM BND U46A → IN/OUT BND (A3)

XERR(G35)(B3)

U32A, U32B, U32E, U32D → $\overline{LDENB}$ (G22)

U44C → U44D → U45B

(B15)$\overline{APEFF}$

(D32)$\overline{SI}$ → U35C

DATA CYC (B3) → DATA CYC U46B

U64B → SO1 U17B

(E39)$\overline{RST2}$

U61D → U45A

(F37)$\overline{CLK1}$ → SO2 U14B

U13C, U31C → U16C, U15C, U15B → U38 → P1-43 $\overline{SO}$

SRVOUT (F31)(A3)

+5V R8 1K

U34D → P1-30 POLLORSO

(C39)$\overline{POLL}$

U72D → P1-19 SRVOUT1

(D32)$\overline{SI}$

U22D

U53B → (C36)DAG (E17)DSO

U33C, U42A

U71A

30001-60008-S TITLE			SHEET 5 OF 5
INPUT/OUTPUT PROCESSOR (IOP) CARD			
ENGINEER	APPROVED	DATE	
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION			

CPU/IOP DETAILED DIAGRAM SET

DD-208

CENTRAL DATA BUS TERMINATOR PCA

30001-60009

SERIES 1228

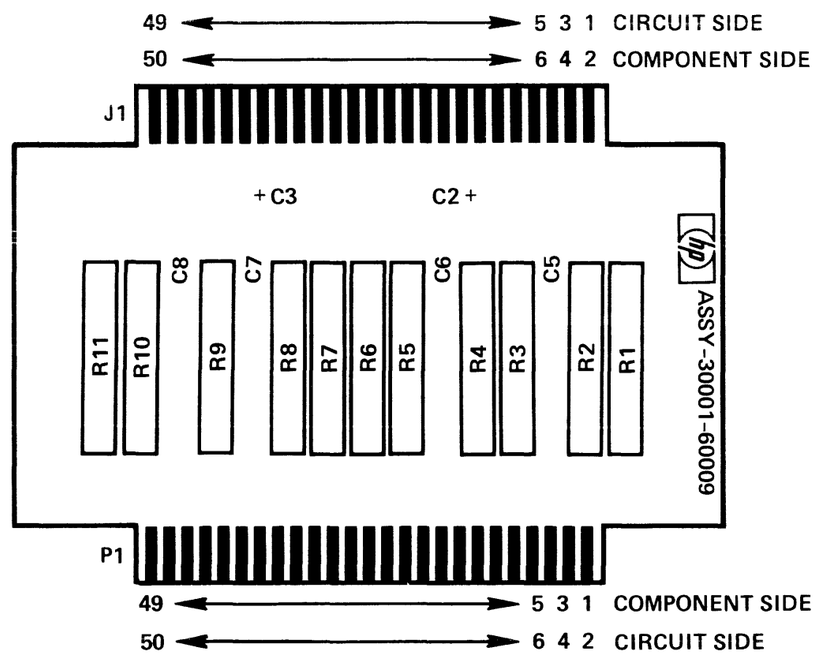
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL
1	COM	1	COM
2	MCUD00	2	+5V
3	MCUD01	3	COM
4	MCUD02	4	+5V
5	MCUD03	5	COM
6	MCUD04	6	+5V
7	MCUD05	7	—
8	XXX	8	—
9	MCUD06	9	—
10	MCUD07	10	—
11	MCUD08	11	—
12	MCUD09	12	—
13	MCUD10	13	—
14	XXX	14	—
15	MCUD11	15	—
16	MCUD12	16	—
17	MCUD13	17	—
18	MCUD14	18	—
19	MCUD15	19	—
20	MCUDPRTY	20	—
21	XXX	21	—
22	TO00	22	—
23	TO01	23	—
24	TO02	24	—
25	FROM00	25	—
26	FROM01	26	—
27	FROM02	27	—
28	MOP00	28	—
29	MOP01	29	—
30	XXX	30	—
31	READY06	31	—
32	SYSPRTY	32	—
33	READY00	33	—
34	READY01	34	—
35	READY02	35	—
36	READY03	36	—
37	READY04	37	—
38	READY05	38	—
39	XXX	39	—
40	ENABLE00	40	—
41	ENABLE01	41	—
42	ENABLE02	42	—
43	ENABLE03	43	—
44	ENABLE04	44	—
45	ENABLE05	45	+5V
46	XXX	46	COM
47	$\overline{\text{MCUDPE}}$	47	+5V
48	$\overline{\text{SYSPE}}$	48	COM
49	$\overline{\text{MCUDRST}}$	49	+5V
50	XXX	50	COM

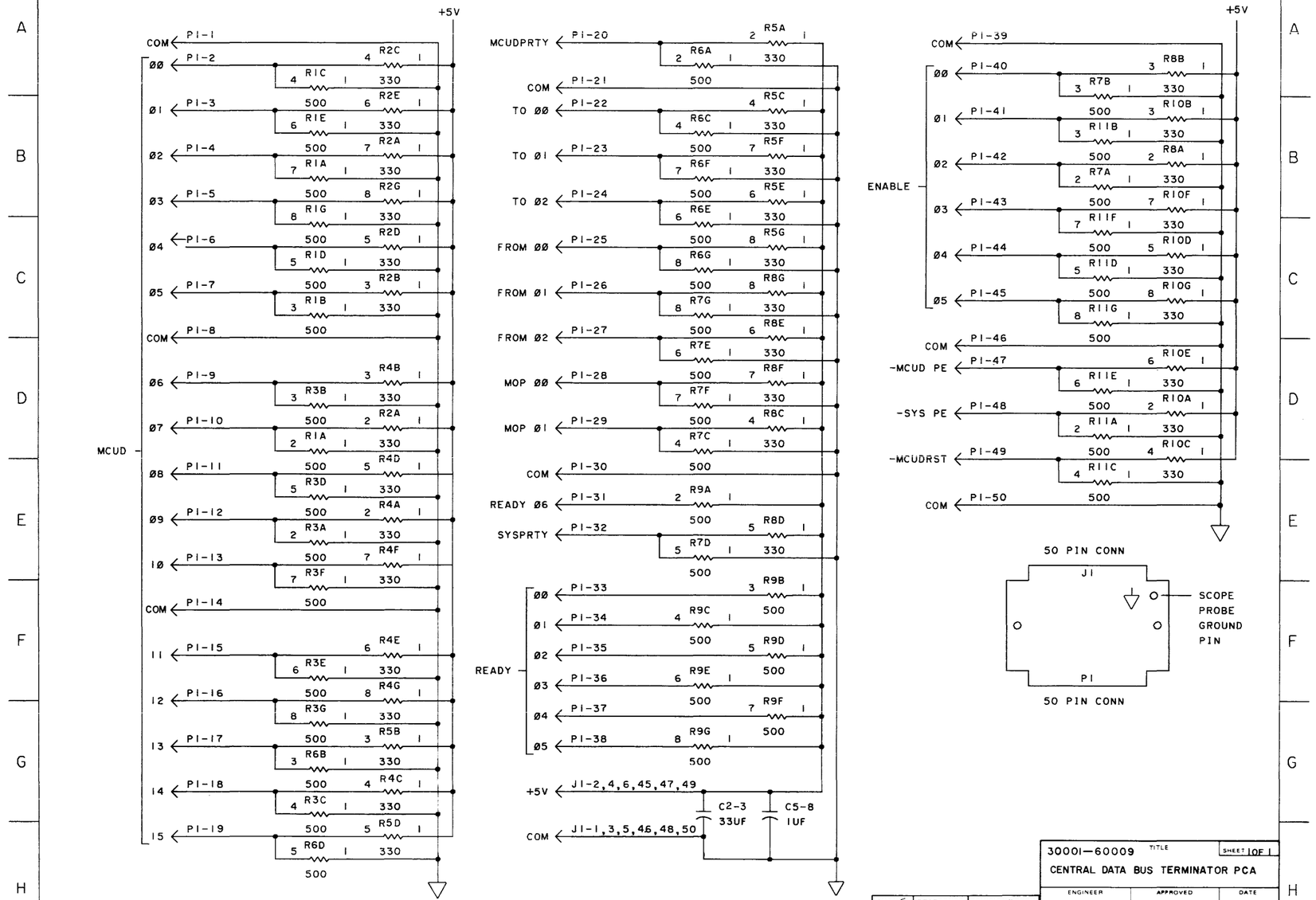
I.C. INDEX

U	1820-
No I.C.s	



2212-19

1867



NOTE ALL RESISTANCE VALUES ARE IN OHMS UNLESS OTHERWISE SPECIFIED

CHANGE	REFERENCE	REVISION/PREFIX

30001-60009 TITLE SHEET 1 OF 1

CENTRAL DATA BUS TERMINATOR PCA

ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-209

I/O PROCESSOR BUS TERMINATOR PCA

30001-60016

SERIES 1305

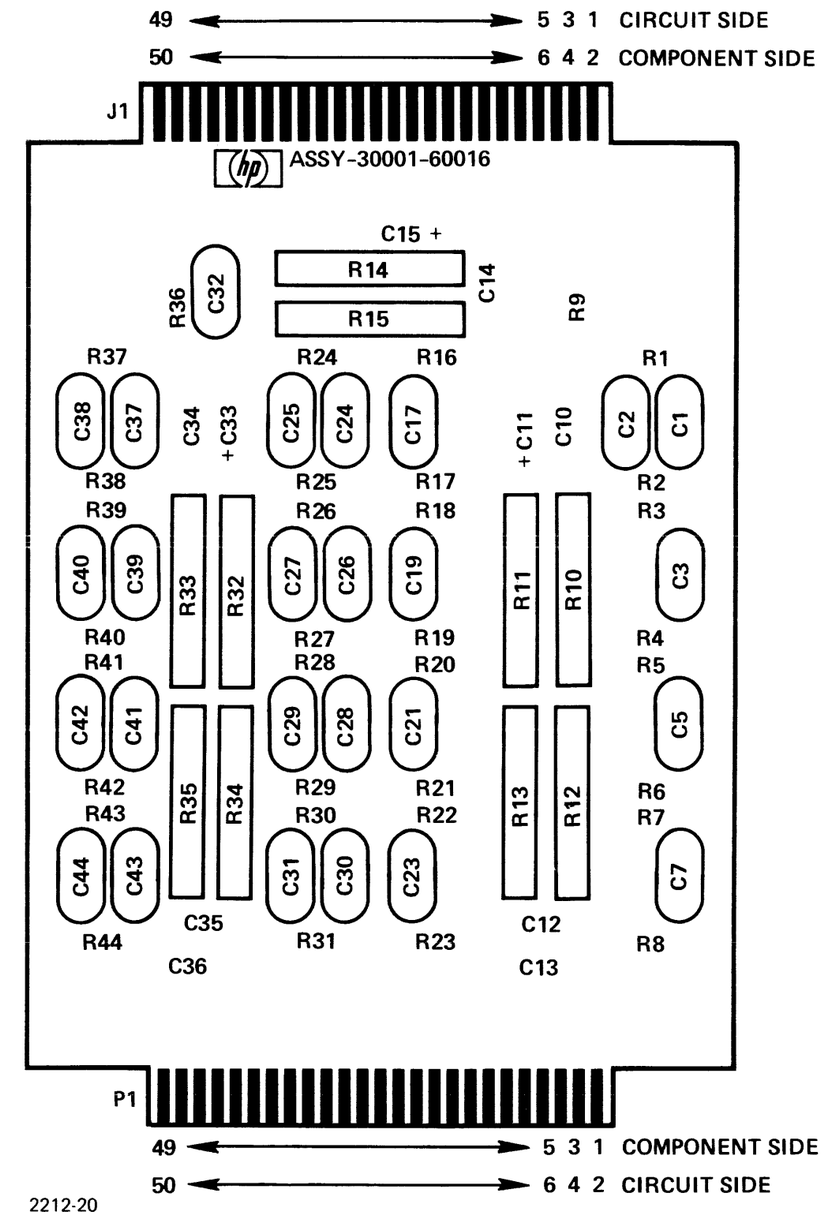
REV B

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL
1	XXX	1	COM
2	XXX	2	+5V
3	COM	3	COM
4	XXX	4	+5V
5	XXX	5	COM
6	XXX	6	+5V
7	COM	7	—
8	XXX	8	—
9	XXX	9	—
10	COM	10	—
11	XXX	11	—
12	XXX	12	—
13	COM	13	—
14	XXX	14	—
15	XXX	15	—
16	COM	16	—
17	XXX	17	—
18	XXX	18	—
19	COM	19	—
20	XXX	20	—
21	XXX	21	—
22	COM	22	—
23	XXX	23	—
24	XXX	24	—
25	COM	25	—
26	XXX	26	—
27	XXX	27	—
28	COM	28	—
29	XXX	29	—
30	XXX	30	—
31	COM	31	—
32	XXX	32	—
33	XXX	33	—
34	COM	34	—
35	XXX	35	—
36	XXX	36	—
37	COM	37	—
38	XXX	38	—
39	XXX	39	—
40	COM	40	—
41	XXX	41	—
42	XXX	42	—
43	COM	43	—
44	XXX	44	—
45	XXX	45	+5V
46	COM	46	COM
47	XXX	47	+5V
48	XXX	48	COM
49	COM	49	+5V
50	XXX	50	COM

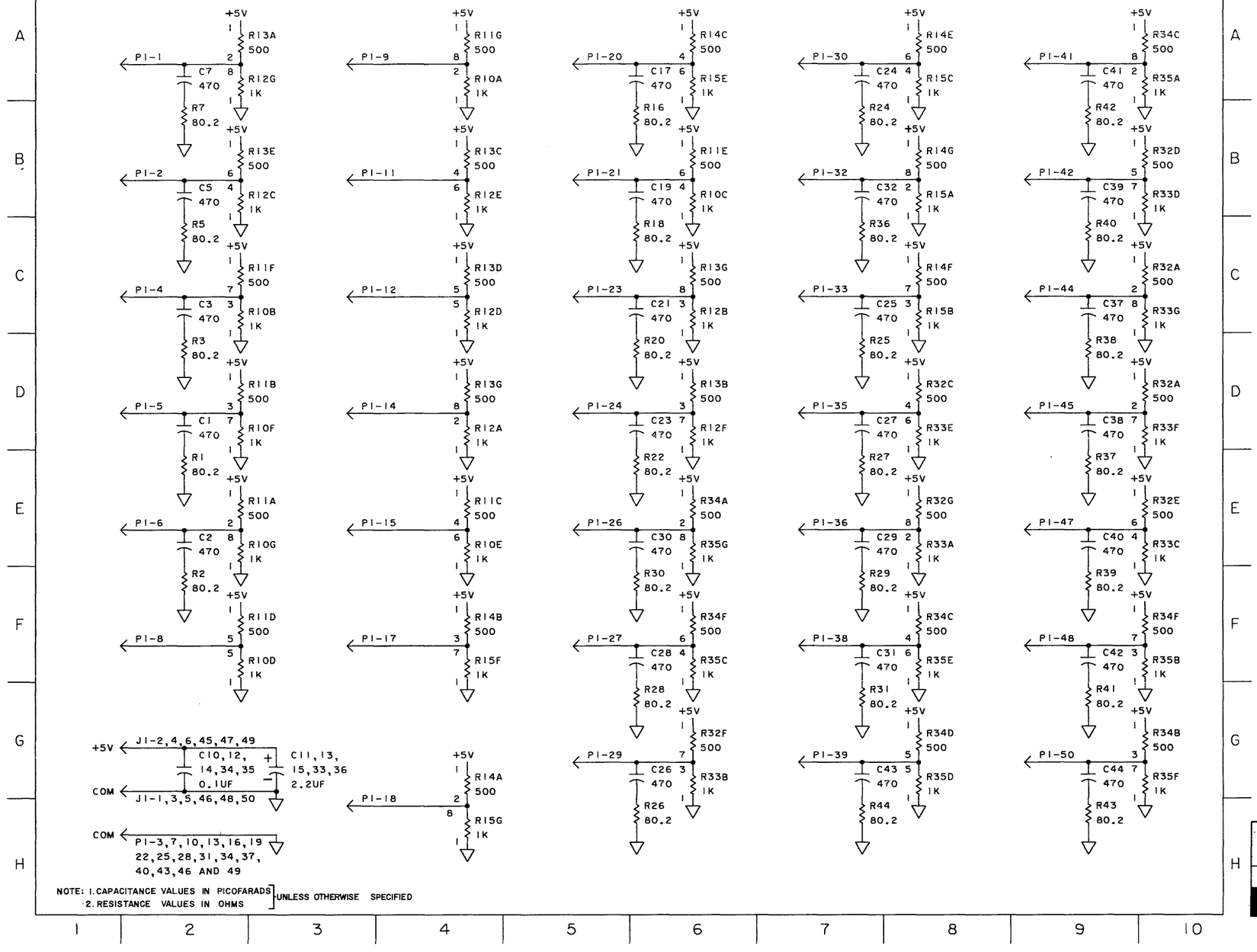
IC INDEX

U	1820-
No I.C.s	



2212-20

1866



NOTE: 1. CAPACITANCE VALUES IN PICOFARADS
2. RESISTANCE VALUES IN OHMS
} UNLESS OTHERWISE SPECIFIED

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1662	A-1305-22

30001-60016 TITLE SHEET 1 OF 1

INPUT/OUTPUT PROCESSOR BUS TERMINATOR PCA

ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-210

POWER BUS TERMINATOR PCA
30001-60021
SERIES 1210

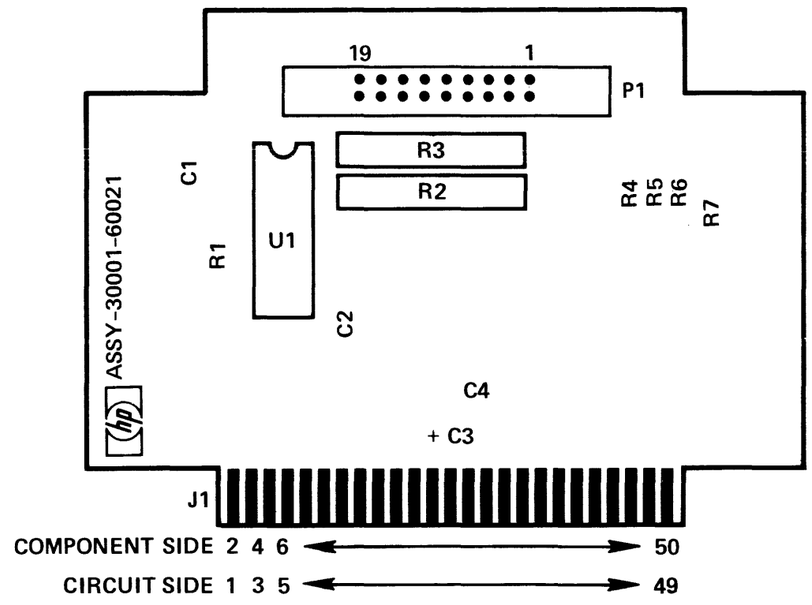
REV B

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL
1	ENTIMER	1	COM
2	$\overline{\text{PF WARN}}$	2	+5V
3	—	3	COM
4	—	4	+5V
5	COM	5	COM
6	PWR ON	6	+5V
7	COM	7	—
8	IORESET	8	—
9	COM	9	—
10	$\overline{\text{MCUCLKS}}$	10	—
11	COM	11	—
12	$\overline{\text{HS REQ}}$	12	—
13	COM	13	—
14	SPARE	14	—
15	COM	15	—
16	$\overline{\text{SI}}$	16	—
17	COM	17	—
18	$\overline{\text{SO}}$	18	—
19	COM	19	—
20	$\overline{\text{MSKRTRN}}$	20	—
21	—	21	—
22	—	22	—
23	—	23	—
24	—	24	—
25	—	25	—
26	—	26	—
27		27	—
28		28	—
29		29	—
30		30	—
31		31	—
32		32	—
33		33	—
34		34	—
35		35	—
36		36	—
37		37	—
38		38	—
39		39	—
40		40	—
41		41	—
42		42	—
43		43	—
44		44	—
45	+5V	45	+5V
46	COM	46	COM
47	+5V	47	+5V
48	COM	48	COM
49	+5V	49	+5V
50	COM	50	COM
51			
52			
53			
54			
55			
56			

I.C. INDEX

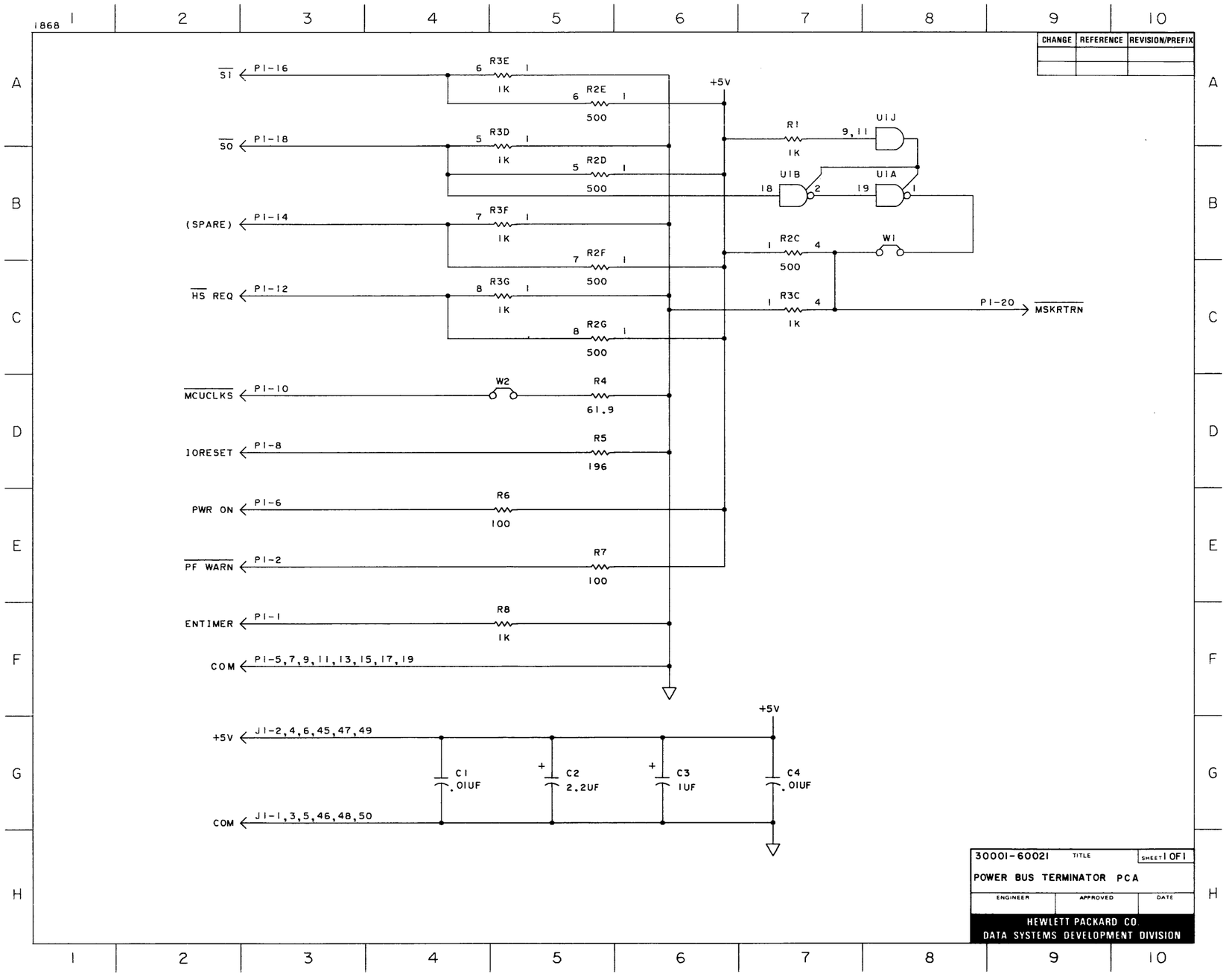
U	1820-
1	0756



2212-21

1868

CHANGE	REFERENCE	REVISION/PREFIX



30001-60021	TITLE	SHEET 1 OF 1
POWER BUS TERMINATOR PCA		
ENGINEER	APPROVED	DATE

HEWLETT PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-211

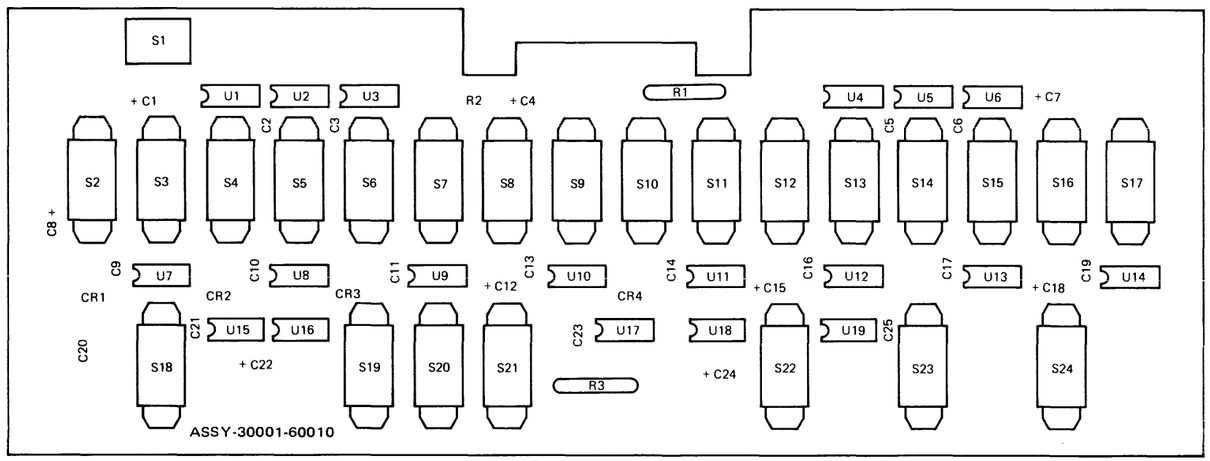
CONTROL BOARD PCA
30001-60010
SERIES 1210

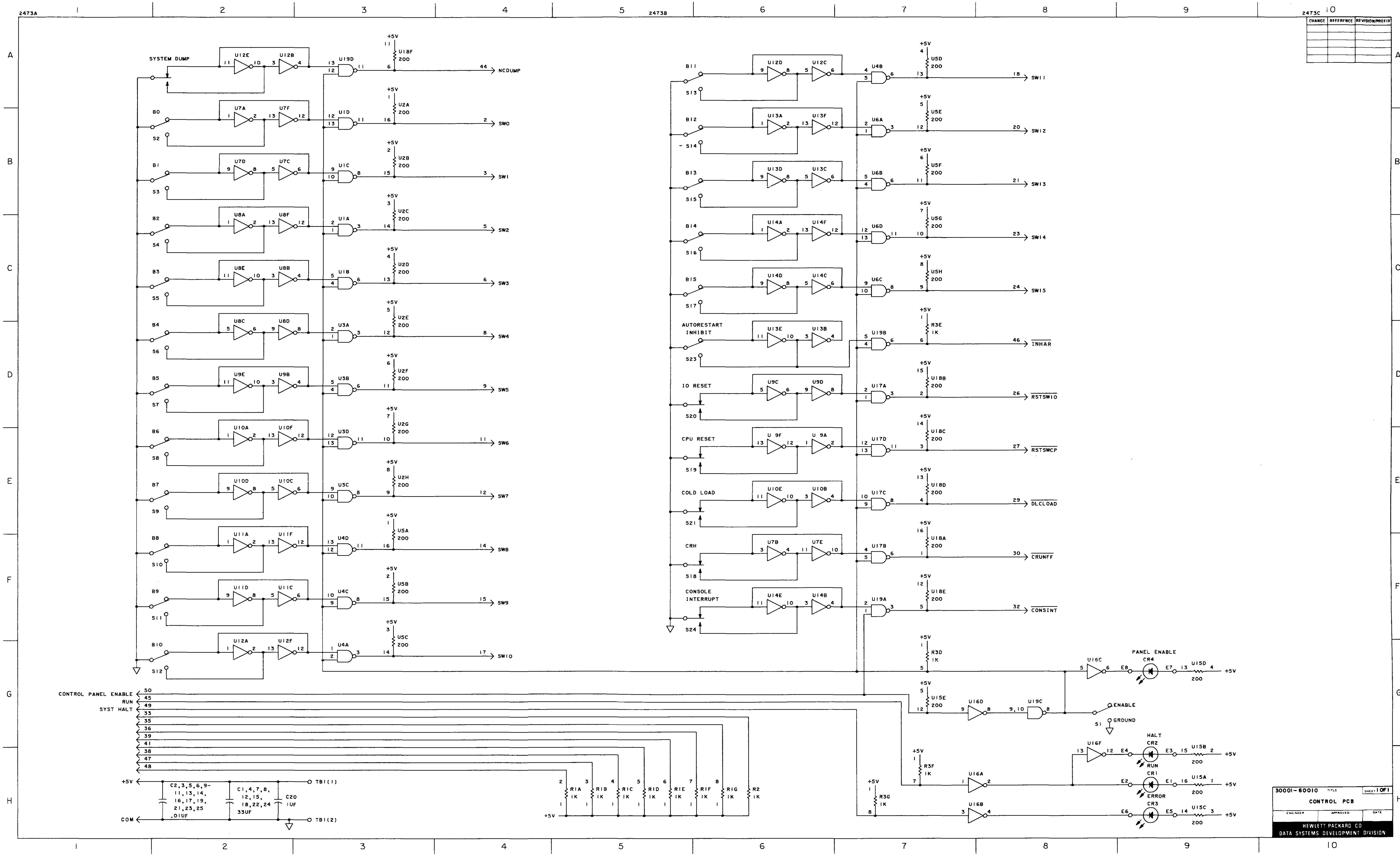
SIGNAL INDEX

PIN	SIGNAL
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	SW11
19	
20	SW12
21	SW13
22	
23	SW14
24	SW15
25	
26	$\overline{\text{RSTSWIO}}$
27	$\overline{\text{RSTSWCP}}$
28	
29	$\overline{\text{DLCLOAD}}$
30	$\overline{\text{CRUNFF}}$
31	
32	$\overline{\text{CONSINT}}$
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	$\overline{\text{RUN}}$
46	$\overline{\text{INHAR}}$
47	
48	
49	SYST HALT
50	CONTROL PANEL ENABLE

I.C. INDEX

U	18xx	U	18xx	U	18xx
1	1820-0621				
2	1810-0124				
3,4	1820-0621				
5	1810-0124				
6	1820-0621				
7 – 14	1820-0307				
15	1810-0124				
16	1820-0424				
17	1820-0621				
18	1810-0124				
19	1820-0621				




SYSTEM DUMP
NCDUMP
CONTROL PANEL ENABLE
RUN
SYST HALT
AUTORESTART INHIBIT
IO RESET
CPU RESET
COLD LOAD
CRH
CONSOLE INTERRUPT
PANEL ENABLE
ENABLE
GROUND
HALT
RUN
ERROR
30001-60010
CONTROL PCB
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

CPU/IOP DETAILED DIAGRAM SET

DD-300

MEMORY LOAD PCA

30005-60001

SERIES 1247

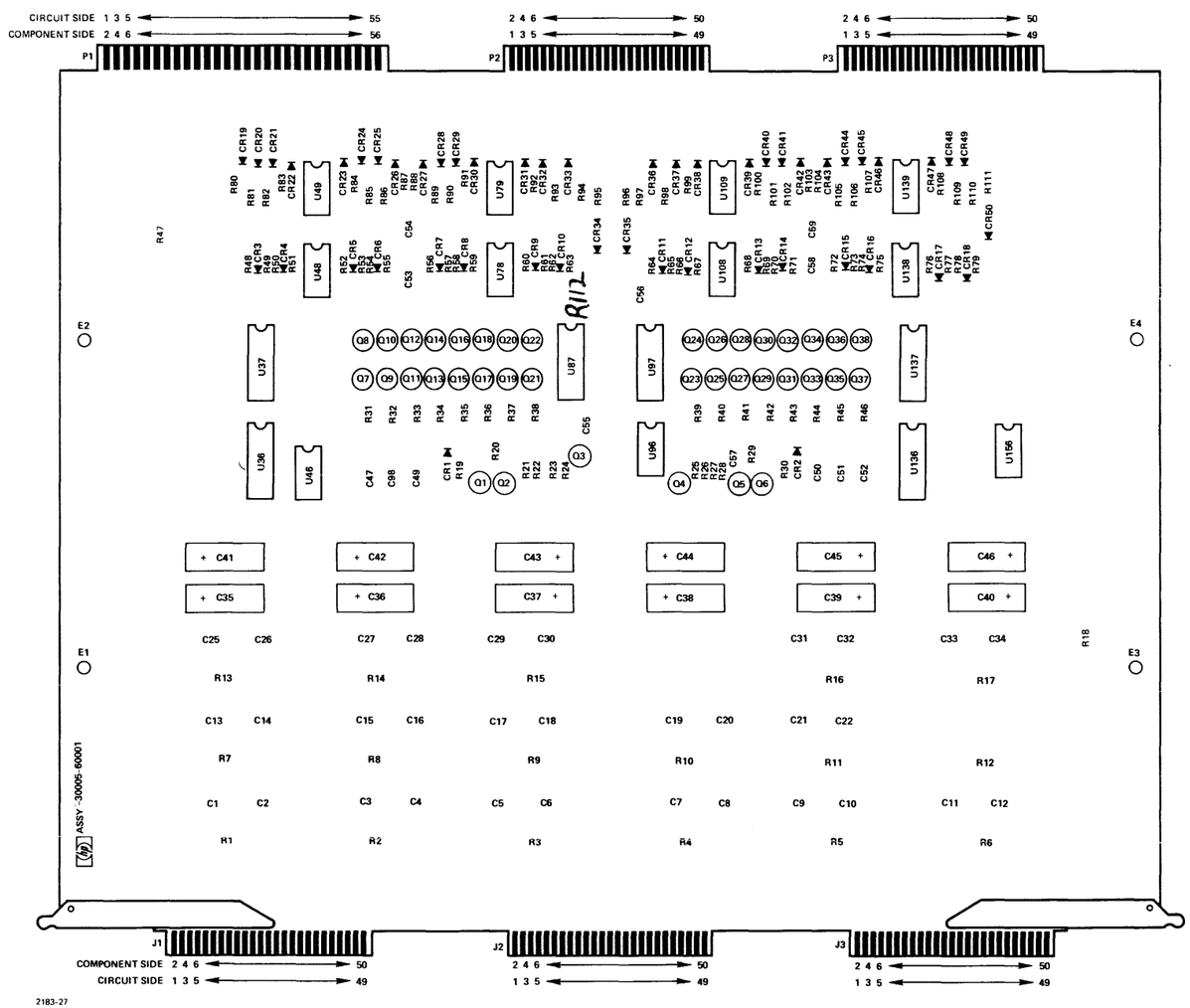
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1		1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2		2		2	
3	+5V	3	COM	3		3	COM	3	COM	3	COM
4	+5V	4	COM	4	$\overline{\text{MRTE}}$	4		4		4	
5		5	COM	5		5	COM	5	COM	5	COM
6		6	COM	6		6		6		6	
7		7	COM	7		7	COM	7	COM	7	COM
8		8	COM	8	COM	8		8		8	
9	PWR ON	9	YCC7	9		9	COM	9	COM	9	COM
10	COM	10	YCA7	10	COM	10		10		10	
11		11	COM	11		11	COM	11	COM	11	COM
12		12	YCC6	12	COM	12		12		12	
13		13	YCA6	13	A7	13	COM	13	COM	13	COM
14		14	YCC3	14	COM	14		14		14	
15	COM	15	COM	15	A9	15	COM	15	COM	15	COM
16	COM	16	YCA3	16	COM	16		16		16	
17	-5V	17	YCC2	17	A8	17	COM	17	COM	17	COM
18	-5V	18	YCA2	18	COM	18		18		18	
19	COM	19	COM	19		19	COM	19	COM	19	COM
20	COM	20	XCC7	20	$\overline{\text{COM}}$	20		20		20	
21		21	XCA7	21	$\overline{\text{MWT}}$	21	COM	21	COM	21	COM
22		22	XCC5	22		22		22		22	
23		23	COM	23	A13	23	COM	23	COM	23	COM
24		24	XCA5	24		24		24		24	
25		25	XCC3	25	A14	25	COM	25	COM	25	COM
26		26	XCA3	26	COM	26		26		26	
27		27	COM	27	A15	27	COM	27	COM	27	COM
28		28	XCC1	28	$\overline{\text{COM}}$	28		28		28	
29	COM	29	XCA1	29	$\overline{\text{MR T}}$	29	COM	29	COM	29	COM
30	COM	30	XCA6	30	$\overline{\text{COM}}$	30		30		30	
31	-20V	31	COM	31	$\overline{\text{MW'TEX}}$	31	COM	31	COM	31	COM
32	-20V	32	XCC6	32	COM	32		32		32	
33	-20V	33	XCA4	33		33	COM	33	COM	33	COM
34	-20V	34	XCC4	34	COM	34	IDR16	34		34	
35	+20V	35	COM	35		35	COM	35	COM	35	COM
36	+20V	36	XCA2	36	COM	36	IDR15	36		36	IDR7
37	+20V	37	XCC2	37		37	COM	37	COM	37	COM
38	+20V	38	XCA0	38	COM	38	IDR14	38		38	IDR6
39	+20V	39	COM	39		39	COM	39	COM	39	COM
40	+20V	40	XCC0	40	COM	40	IDR13	40		40	IDR5
41		41	YCA0	41		41	COM	41	COM	41	COM
42		42	YCC0	42	COM	42	IDR12	42		42	IDR4
43		43	COM	43		43	COM	43	COM	43	COM
44		44	YCA1	44	COM	44	IDR11	44		44	IDR3
45		45	YCC1	45		45	COM	45	COM	45	COM
46		46	YCA4	46	COM	46	IDR10	46		46	IDR2
47		47	COM	47		47	COM	47	COM	47	COM
48		48	YCC4	48	COM	48	IDR9	48		48	IDR1
49		49	YCA5	49		49	COM	49	COM	49	COM
50		50	YCC5	50	COM	50	IDR8	50		50	IDR0
51											
52											
53											
54											
55	TEMP SNS										
56	TEMP SNS										

I.C INDEX

U	1820-	U	1820-
36	0755	97	0755
37	0756	108	0006
46	0608	109	0020
48	0006	136	0759
49	0020	137	0756
78	0006	138	0006
79	0020	139	0020
87	0755	156	0608
96	0424		



2183-27

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1612	B-1247-22	1

XCC7 XCA7 XCC6 XCA6 XCC5 XCA5 XCC4 XCA4 XCC3 XCA3 XCC2 XCA2 XCC1 XCA1 XCC0 XCA0

P2-20 P2-21 P2-32 P2-30 P2-22 P2-24 P2-34 P2-33 P2-25 P2-26 P2-37 P2-36 P2-28 P2-29 P2-40 P2-38

U108C U108A U108D U108B U138C U138A U138D U138B

CR14 CR12 CR13 CR11 CR18 CR16 CR17 CR15

R71 R67 R68 R64 R79 R75 R76 R72 1K

+20V

R72 R66 R69 R65 R78 R74 R77 R73 38.3

MW'TEX • PWR ON

MW'TEX • PWR ON

U137 U97

MR'T

MR'T

CR41 CR40 CR37 CR36 CR49 CR45 CR48 CR44

Q29 Q27 Q25 Q23 Q37 Q33 Q35 Q31

U109 U139

R42 R41 R40 R39 R46 R45 R44 R43 121

R102 R101 R98 R97 R110 R106 R109 R105 68.1

R103 R100 R99 R96 R111 R107 R108 R104 1K

CR42 CR39 CR38 CR35 CR50 CR46 CR47 CR3

-5V -20V

Q30 Q28 Q26 Q24 Q38 Q34 Q36 Q32

U137 9 11 — U96D 8 9

U97 9 11 — P3-31 $\overline{\text{MW'TEX}}$

P3-29 $\overline{\text{MR'T}}$

-5V

C59 27PF

R29

U96F 13 12

U96E 11

R27 196

R28 281

Q6

Q5

$\overline{\text{MR'T}}$ 10

R30 511

CR2

+5V

U136

4	3	2	1	8	7	6	5
16	17	18	19	12	13	14	15

ENABLE 9, 11,

+5V

Q4

PWR ON (F20)

C56 .01CF

R25 196

R26 196

BINARY-TO-OCTAL DECODER U156

1	2	3	4	13	12	11	10
7	6	5	4	3	2	1	0

ENABLE 2^2 2^1 2^0

8 9 6 5

P3-27 → A15

P3-25 → A14

P3-23 → A13

COM ← P1-10,15,16,19,20,29,30

C47,48,51,52 1UF

C49,50 1UF

C53,57 1UF

C54,58 1UF

+5V ← P1-1,2,3,4 → +5V

-5V ← P1-17,18 → -5V

+20V ← P1-35 THRU 40 → +20V

-20V ← P1-31 THRU 34 → -20V

P1-55

R18

P1-56

(TEMP SENSE ELEMENT)

C1,3,6,7,10,12,13,15,18,19,22,24,25,27,30,32,34 1UF

C35,36,37,38,39,40,41,42,43,44,45,46 100UF 25V

1. COMMON RETURNS:
   J1 ALL ODDS 1-49
   J2 ALL ODDS 1-49
   J3 ALL ODDS 1-49,34
   P2 1-8,11,15,19,23,27,31,35,39,43,AND 47
   P3 EVENS ONLY 2,8-20,26-50

NOTE: UNLESS OTHERWISE SPECIFIED

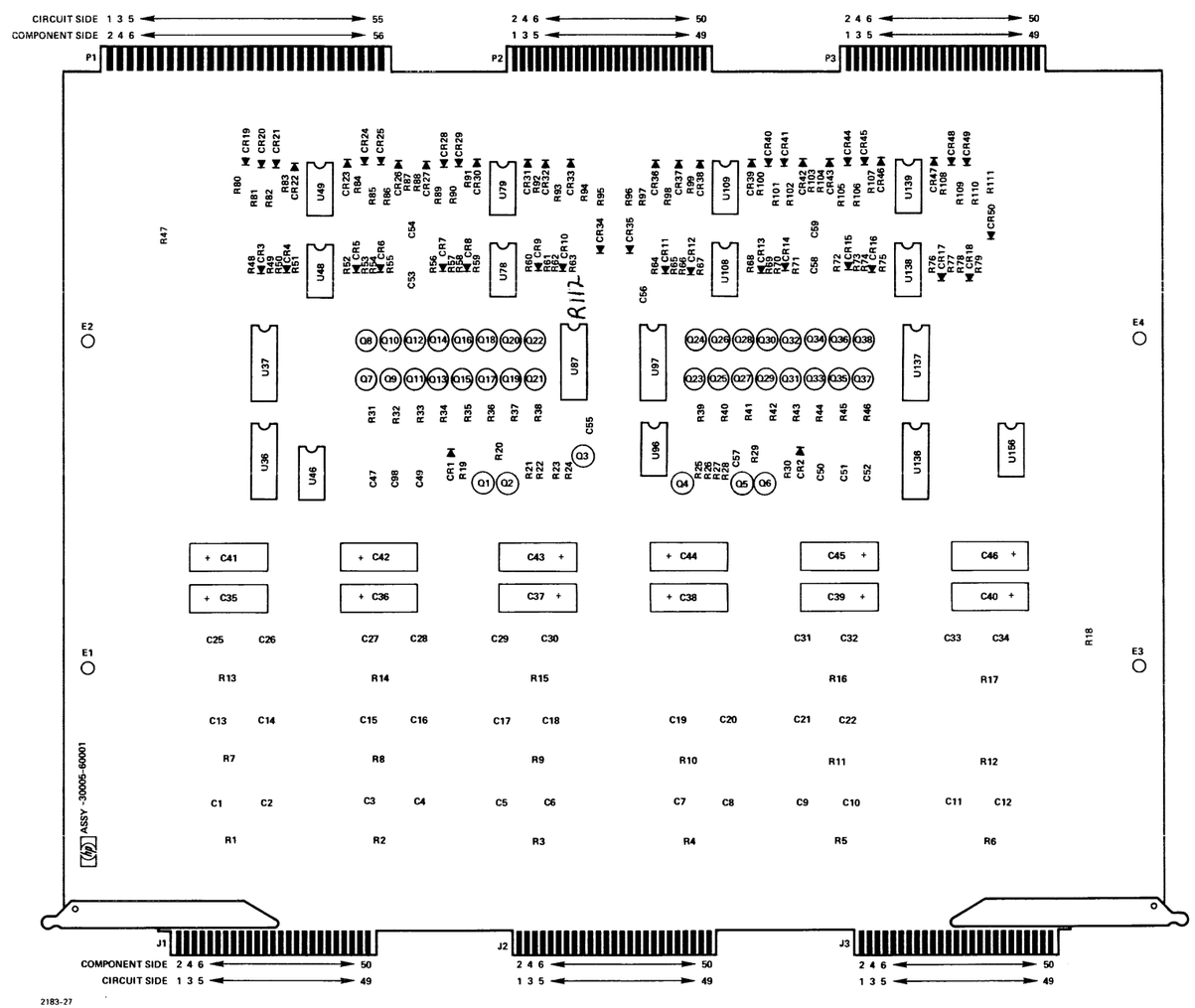
30005-60001	TITLE	SHEET 1 OF 2
MEMORY LOAD PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1		P2		P3		J1		J2		J3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1	COM	1		1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2		2		2	
3	+5V	3	COM	3		3	COM	3	COM	3	COM
4	+5V	4	COM	4	$\overline{\text{MRTE}}$	4		4		4	
5		5	COM	5		5	COM	5	COM	5	COM
6		6	COM	6		6		6		6	
7		7	COM	7		7	COM	7	COM	7	COM
8		8	COM	8	COM	8		8		8	
9	PWR ON	9	YCC7	9		9	COM	9	COM	9	COM
10	COM	10	YCA7	10	COM	10		10		10	
11		11	COM	11		11	COM	11	COM	11	COM
12		12	YCC6	12	COM	12		12		12	
13		13	YCA6	13	A7	13	COM	13	COM	13	COM
14		14	YCC3	14	COM	14		14		14	
15	COM	15	COM	15	A9	15	COM	15	COM	15	COM
16	COM	16	YCA3	16	COM	16		16		16	
17	-5V	17	YCC2	17	A8	17	COM	17	COM	17	COM
18	-5V	18	YCA2	18	COM	18		18		18	
19	COM	19	COM	19		19	COM	19	COM	19	COM
20	COM	20	XCC7	20	$\overline{\text{COM}}$	20		20		20	
21		21	XCA7	21	$\overline{\text{MWT}}$	21	COM	21	COM	21	COM
22		22	XCC5	22		22		22		22	
23		23	COM	23	A13	23	COM	23	COM	23	COM
24		24	XCA5	24		24		24		24	
25		25	XCC3	25	A14	25	COM	25	COM	25	COM
26		26	XCA3	26	COM	26		26		26	
27		27	COM	27	A15	27	COM	27	COM	27	COM
28		28	XCC1	28	$\overline{\text{COM}}$	28		28		28	
29	COM	29	XCA1	29	$\overline{\text{MR'T}}$	29	COM	29	COM	29	COM
30	COM	30	XCA6	30	$\overline{\text{COM}}$	30		30		30	
31	-20V	31	COM	31	$\overline{\text{MW'TEX}}$	31	COM	31	COM	31	COM
32	-20V	32	XCC6	32	COM	32		32		32	
33	-20V	33	XCA4	33		33	COM	33	COM	33	COM
34	-20V	34	XCC4	34	COM	34	IDR16	34		34	
35	+20V	35	COM	35		35	COM	35	COM	35	COM
36	+20V	36	XCA2	36	COM	36	IDR15	36		36	IDR7
37	+20V	37	XCC2	37		37	COM	37	COM	37	COM
38	+20V	38	XCA0	38	COM	38	IDR14	38		38	IDR6
39	+20V	39	COM	39		39	COM	39	COM	39	COM
40	+20V	40	XCC0	40	COM	40	IDR13	40		40	IDR5
41		41	YCA0	41		41	COM	41	COM	41	COM
42		42	YCC0	42	COM	42	IDR12	42		42	IDR4
43		43	COM	43		43	COM	43	COM	43	COM
44		44	YCA1	44	COM	44	IDR11	44		44	IDR3
45		45	YCC1	45		45	COM	45	COM	45	COM
46		46	YCA4	46	COM	46	IDR10	46		46	IDR2
47		47	COM	47		47	COM	47	COM	47	COM
48		48	YCC4	48	COM	48	IDR9	48		48	IDR1
49		49	YCA5	49		49	COM	49	COM	49	COM
50		50	YCC5	50	COM	50	IDR8	50		50	IDR0
51											
52											
53											
54											
55	TEMP SNS										
56	TEMP SNS										

I.C INDEX

U	1820-	U	1820-
36	0755	97	0755
37	0756	108	0006
46	0608	109	0020
48	0006	136	0759
49	0020	137	0756
78	0006	138	0006
79	0020	139	0020
87	0755	156	0608
96	0424		



2183-27

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1612	B-1247-22

YCC7 YCA7 YCC6 YCA6 YCC5 YCA5 YCC4 YCA4 YCC3 YCA3 YCC2 YCA2 YCC1 YCA1 YCC0 YCA0

P2-9 P2-10 P2-12 P2-13 P2-50 P2-49 P2-48 P2-46 P2-14 P2-16 P2-17 P2-18 P2-45 P2-44 P2-42 P2-41

U48B U48A U48D U48C U78B U78A U78D U78C

CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10

R48 1K R51 1K R52 1K R55 1K R56 1K R59 1K R60 1K R63 1K

+20V

R49 38.3 R50 38.3 R53 38.3 R54 38.3 R57 38.3 R58 38.3 R61 38.3 R62 38.3

MWT • PWR ON

$\overline{MWT}$ • PWR ON

U37 U87

U96C

P3-21 $\overline{MWT}$

$\overline{MRTE}$

$\overline{MRTE}$

CR20 CR21 CR24 CR25 CR28 CR29 CR32 CR33

Q7 Q9 Q11 Q13 Q15 Q17 Q19 Q21

U49 U79

R31 121 R81 68.1 R80 1K CR19

R32 121 R82 68.1 R83 1K CR22

R33 121 R85 68.1 R84 1K CR23

R34 121 R86 68.1 R87 1K CR26

R35 121 R89 68.1 R88 1K CR27

R36 121 R90 68.1 R91 1K CR30

R37 121 R93 68.1 R92 1K CR31

R38 121 R94 68.1 R95 1K CR34

-5V -20V

Q8 Q10 Q12 Q14 Q16 Q18 Q20 Q22

-5V

R20 1K

R22 196 R21 261

Q2 Q1

P3-4 $\overline{MRTE}$

R19 2.61K CR1

+5V

U36

ENABLE 9, 11,

+5V

Q3

(F10)

P1-9 PWR ON

R112 147

C55 .01UF

R23 196 R24 196

BINARY-TO-OCTAL DECODER U46

ENABLE 2^2 2^1 2^0

P3-15 A9

P3-17 A8

P3-13 A7

+20V

C2 1600PF R1 22 C4 1600PF R2 22 C5 1600PF R3 22 C8 1600PF R4 22 C9 1600PF R5 22 C11 1600PF R6 22 C14 1600PF R7 22 C16 1600PF R8 22 C17 1600PF R9 22 C20 1600PF R10 22 C21 1600PF R11 22 C23 1600PF R12 22 C26 1600PF R13 22 C28 1600PF R14 22 C29 1600PF R15 22 C31 1600PF R16 22 C33 1600PF R17 22

J1-36 IDR15 J1-42 IDR12 J1-48 IDR9 J3-38 IDR6 J3-40 IDR5 J3-46 IDR2 J1-38 IDR14 J1-44 IDR11 J1-46 IDR10 J3-36 IDR7 J3-42 IDR4 J3-48 IDR1 J1-34 IDR16 J1-40 IDR13 J1-50 IDR8 J3-44 IDR3 J3-50 IDR0

30005-60001	TITLE		SHEET 2 OF 2
MEMORY LOAD PCA			
ENGINEER	APPROVED	DATE	
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION			

CPU/IOP DETAILED DIAGRAM SET

DD-301

MEMORY DATA AND CONTROL PCA

30005-60002

SERIES 1210

1245

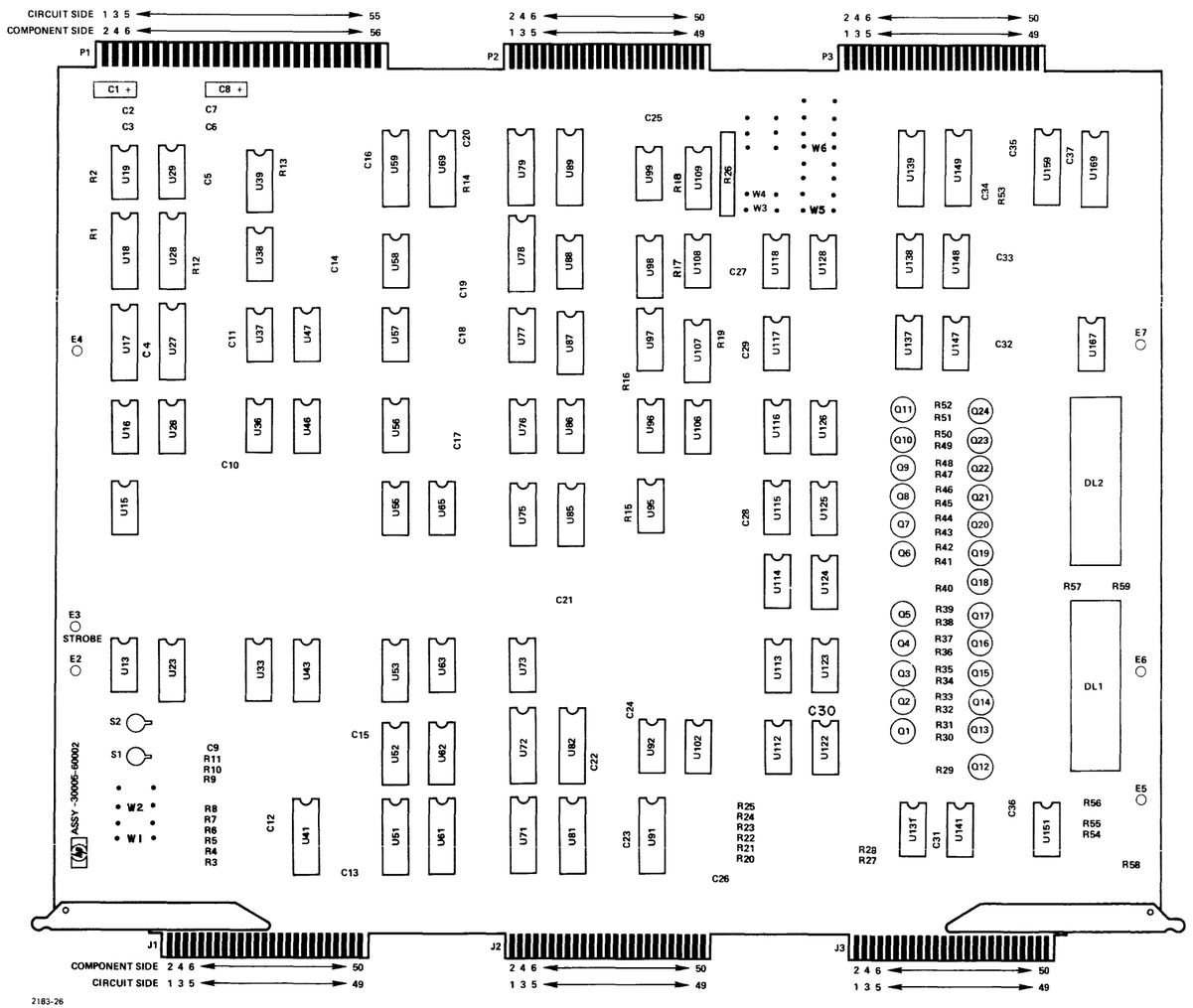
REV C

SIGNAL INDEX

P1		P2		P3		J1		J2		J3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1	COM	1		1		1		1	
2	+5V	2	MCUD 00	2		2	SA16	2	ID16	2	SA7
3	+5V	3	MCUD 01	3		3		3		3	
4	+5V	4	MCUD 02	4	$\overline{\text{MRTE}}$	4	SA15	4	ID15	4	SA6
5		5	MCUD 03	5		5		5		5	
6	ENTIMER	6	MCUD 04	6	$\overline{\text{MWTE}}$	6	SA14	6	ID14	6	SA5
7		7	MCUD 05	7		7		7		7	
8		8	COM	8		8	SA13	8	ID13	8	SA4
9		9	MCUD 06	9		9		9		9	
10		10	MCUD 07	10		10	SA12	10	ID12	10	SA3
11		11	MCUD 08	11		11		11		11	
12	$\overline{\text{\quad\quad}}$	12	MCUD 09	12		12	SA11	12	ID11	12	SA2
13	MCUCLKS	13	MCUD 10	13	AD7	13		13		13	
14	COM	14	COM	14		14	SA10	14	ID10	14	SA1
15	COM	15	MCUD 11	15	AD9	15		15		15	
16	COM	16	MCUD 12	16		16	SA9	16	ID09	16	SA0
17	-5V	17	MCUD 13	17	AD8	17		17		17	
18	-5V	18	MCUD 14	18		18	SA8	18	ID08	18	
19	COM	19	MCUD 15	19	AD4	19		19		19	
20	COM	20	MCUD PRTY	20		20		20	ID07	20	
21		21	COM	21	$\overline{\text{MWT}}$	21		21		21	
22		22	'TO' 00	22	AD5	22		22	ID06	22	
23		23	'TO' 01	23	AD13	23		23	MSG	23	
24		24	'TO' 02	24	AD6	24		24	ID05	24	
25		25	'FROM' 00	25	AD14	25		25		25	
26		26	'FROM' 01	26		26		26	ID04	26	
27		27	'FROM' 02	27	AD15	27		27		27	
28		28	MOP 00	28		28		28	ID03	28	
29	COM	29	MOP 01	29	$\overline{\text{MR'T}}$	29		29		29	
30	COM	30	COM	30		30		30	ID02	30	
31		31		31	MW'TEX	31		31		31	
32		32	SYS PRTY	32		32		32	ID01	32	
33		33	READY 00	33	MR'TE	33		33		33	
34		34	READY 01	34		34		34	ID00	34	
35		35	READY 02	35	AD10	35		35		35	
36		36	READY 03	36		36		36	$\overline{\text{MODE 7}}$	36	
37		37		37	$\overline{\text{MW'TEXE}}$	37		37		37	
38		38		38		38		38	$\overline{\text{MODE 6}}$	38	
39		39	COM	39	AD11	39		39		39	
40		40	ENABLE 00	40		40		40	$\overline{\text{MODE 5}}$	40	
41		41	ENABLE 01	41	AD12	41		41		41	
42		42	ENABLE 02	42		42		42	$\overline{\text{MODE 4}}$	42	
43		43	ENABLE 03	43	$\overline{\text{MODE 1,0}}$	43		43		43	
44		44		44		44		44	$\overline{\text{MODE 3}}$	44	
45		45		45	$\overline{\text{MODE 3,2}}$	45		45		45	
46		46	COM	46		46		46	$\overline{\text{MODE 2}}$	46	
47		47	$\overline{\text{MCUD PE}}$	47	$\overline{\text{MODE 5,4}}$	47		47		47	
48		48	$\overline{\text{SYS PE}}$	48		48		48	$\overline{\text{MODE 1}}$	48	
49		49	$\overline{\text{MCU RST}}$	49	$\overline{\text{MODE 7,6}}$	49		49		49	
50		50	COM	50		50		50	$\overline{\text{MODE 0}}$	50	
51											
52											
53											
54											
55											
56											

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0842	51	0759	86	0239	115-117	0239
15,16	0690	52,53	0301	87	0301	118	0376
17,18	0759	55	0141	88	0370		
19	0140	56	0686	89	0755	122-125	0239
		57	0683			126	0205
23	0301	58	0371	91	0756	128	0686
26	0690	59,61	0755	92	0141		
27	0756	62	0301	95	0690	131	0377
28	0759	63	0842	96	0141	137	0683
29	0424	65	0140	97	0706	138	0424
		69	**0755**	98	0629	139	0759
33	0301	71	0759	99	0842	141	0377
36	0690	72	0301			147,148	0376
37	0371	73	0140	102	0608	149	0755
38	0376	75	0629	106	0370		
39	0629	76	0239	107	0629	151	0207
		77	0842	108	0608	159	0755
41	0756	78	0301	109	0706	167	0376
43	0301	79,81	0759			169	0755
46	0690	82	0301	112	0239		
47	0370	85	0629	113,114	0205		



2183-26

1381A-1 1381B-1 1381C-1

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	ERRATA	NO CHANGE	ALL

CTL DATA BUS

ENABLE ØØ P2-40
ENABLE Ø1 P2-41
ENABLE Ø2 P2-42
ENABLE Ø3 P2-43
MOP Ø1 P2-29

JUMPER	POSITION	MODULE 0	1	2	3	FUNCTION
W3	F2	0 0	0 0	0 0	0–0	ENABLE 02
W4	F1	0 0	0 0	0–0	0 0	ENABLE 01
W5	F0	0 0	0–0	0 0	0 0	ENABLE 00
W4	E1	0–0	0 0	0 0	0 0	TO/FROM
W3	E0	0–0	0 0	0–0	0 0	TO/FROM
W1	D3	0 0	0 0	0 0	0–0	READY 03
	D2	0 0	0 0	0–0	0 0	READY 02
	D1	0 0	0–0	0 0	0 0	READY 01
	D0	0–0	0 0	0 0	0 0	READY 00
W2	C3	0 0	0 0	0 0	0–0	ENABLE 03
	C2	0 0	0 0	0–0	0 0	ENABLE 02
	C1	0 0	0–0	0 0	0 0	ENABLE 01
	C0	0–0	0 0	0 0	0 0	ENABLE 00

MOP DECODER	INPUT MOP Ø1	INPUT MOP Ø0	OUTPUT CW	OUTPUT RNW
NOP	Ø	Ø	1	1
CW	1	Ø	0	1
RR	Ø	1	1	1
RNW	1	1	1	0

NOTE: 1. ALL RESISTANCES ARE 2.37K UNLESS OTHERWISE SPECIFIED.

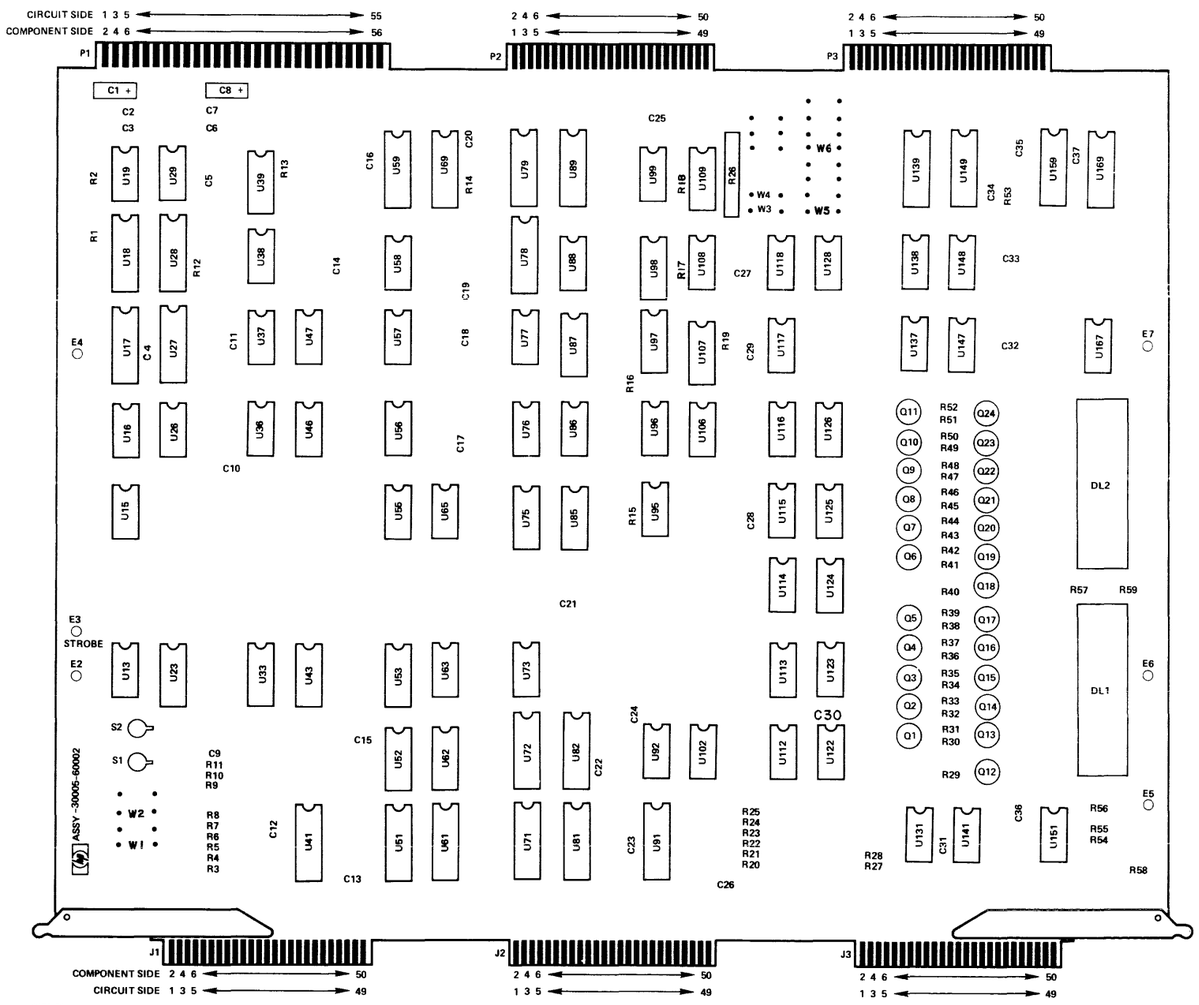
30005-60002 TITLE	SHEET 1 OF 3
MEMORY DATA AND CONTROL PCA	
ENGINEER / APPROVED / DATE	
HEWLETT PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION	

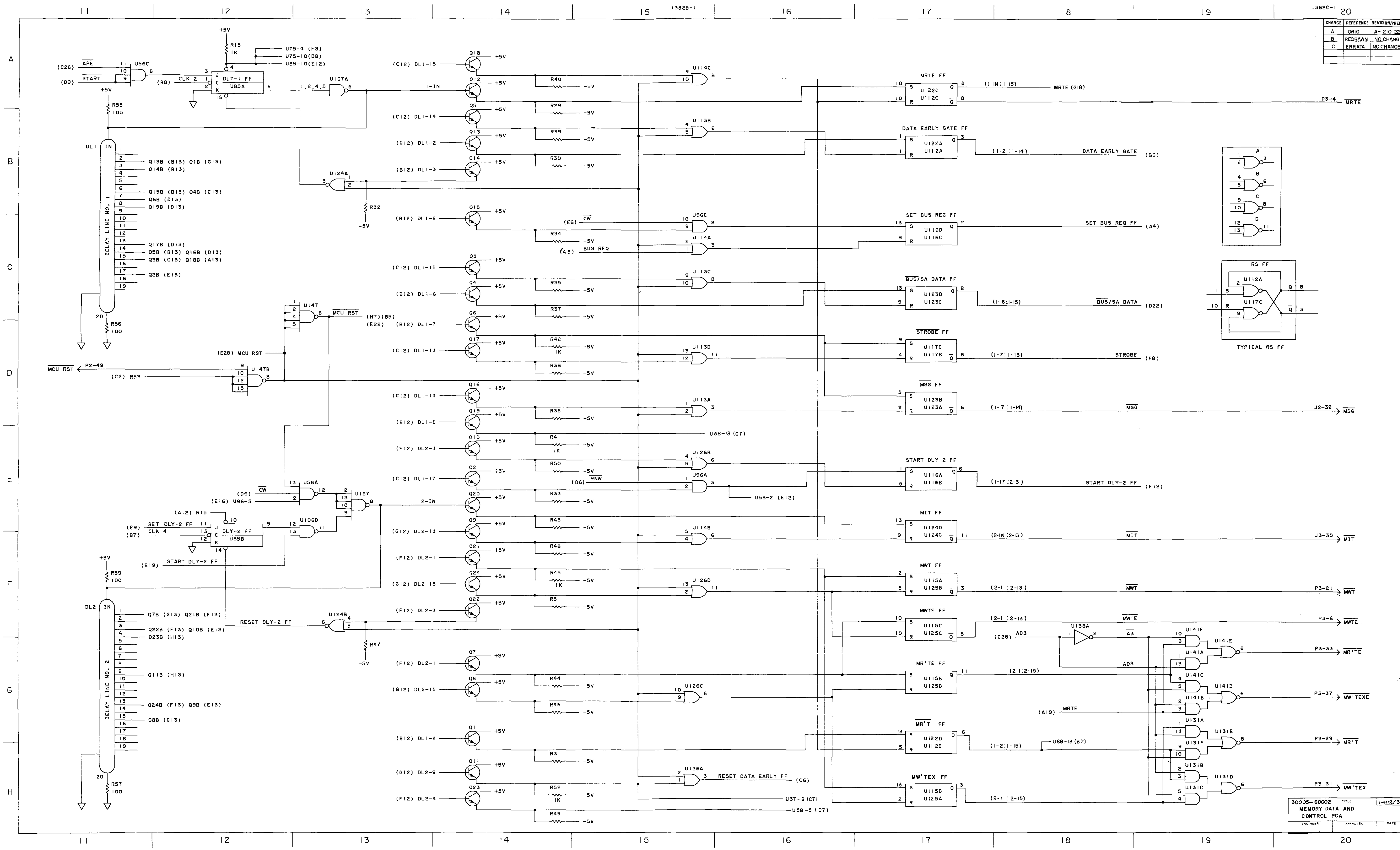
SIGNAL INDEX

P1		P2		P3		J1		J2		J3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1	COM	1		1		1		1	
2	+5V	2	MCUD 00	2		2	SA16	2	ID16	2	SA7
3	+5V	3	MCUD 01	3		3		3		3	
4	+5V	4	MCUD 02	4	$\overline{\text{MRTE}}$	4	SA15	4	ID15	4	SA6
5		5	MCUD 03	5		5		5		5	
6	ENTIMER	6	MCUD 04	6	$\overline{\text{MWTE}}$	6	SA14	6	ID14	6	SA5
7		7	MCUD 05	7		7		7		7	
8		8	COM	8		8	SA13	8	ID13	8	SA4
9		9	MCUD 06	9		9		9		9	
10		10	MCUD 07	10		10	SA12	10	ID12	10	SA3
11		11	MCUD 08	11		11		11		11	
12		12	MCUD 09	12		12	SA11	12	ID11	12	SA2
13	$\overline{\text{MCUCLKS}}$	13	MCUD 10	13	AD7	13		13		13	
14	COM	14	COM	14		14	SA10	14	ID10	14	SA1
15	COM	15	MCUD 11	15	AD9	15		15		15	
16	COM	16	MCUD 12	16		16	SA9	16	ID09	16	SA0
17	-5V	17	MCUD 13	17	AD8	17		17		17	
18	-5V	18	MCUD 14	18		18	SA8	18	ID08	18	
19	COM	19	MCUD 15	19	AD4	19		19		19	
20	COM	20	MCUD PRTY	20		20		20	ID07	20	
21		21	COM	21	$\overline{\text{MWT}}$	21		21		21	
22		22	'TO' 00	22	AD5	22		22	ID06	22	
23		23	'TO' 01	23	AD13	23		23	MSG	23	
24		24	'TO' 02	24	AD6	24		24	ID05	24	
25		25	'FROM' 00	25	AD14	25		25		25	
26		26	'FROM' 01	26		26		26	ID04	26	
27		27	'FROM' 02	27	AD15	27		27		27	
28		28	MOP 00	28		28		28	ID03	28	
29	COM	29	MOP 01	29	$\overline{\text{MR'T}}$	29		29		29	
30	COM	30	COM	30		30		30	ID02	30	
31		31		31	MW'TEX	31		31		31	
32		32	SYS PRTY	32		32		32	ID01	32	
33		33	READY 00	33	MR'TE	33		33		33	
34		34	READY 01	34		34		34	ID00	34	
35		35	READY 02	35	AD10	35		35		35	
36		36	READY 03	36		36		36	$\overline{\text{MODE 7}}$	36	
37		37		37	$\overline{\text{MW'TEXE}}$	37		37		37	
38		38		38		38		38	$\overline{\text{MODE 6}}$	38	
39		39	COM	39	AD11	39		39		39	
40		40	ENABLE 00	40		40		40	$\overline{\text{MODE 5}}$	40	
41		41	ENABLE 01	41	AD12	41		41		41	
42		42	ENABLE 02	42		42		42	$\overline{\text{MODE 4}}$	42	
43		43	ENABLE 03	43	$\overline{\text{MODE 1,0}}$	43		43		43	
44		44		44		44		44	$\overline{\text{MODE 3}}$	44	
45		45		45	$\overline{\text{MODE 3,2}}$	45		45		45	
46		46	COM	46		46		46	$\overline{\text{MODE 2}}$	46	
47		47	$\overline{\text{MCUD PE}}$	47	$\overline{\text{MODE 5,4}}$	47		47		47	
48		48	$\overline{\text{SYS PE}}$	48		48		48	$\overline{\text{MODE 1}}$	48	
49		49	$\overline{\text{MCU RST}}$	49	$\overline{\text{MODE 7,6}}$	49		49		49	
50		50	COM	50		50		50	$\overline{\text{MODE 0}}$	50	
51											
52											
53											
54											
55											
56											

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0842	51	0759	86	0239	115-117	0239
15,16	0690	52,53	0301	87	0301	118	0376
17,18	0759	55	0141	88	0370		
19	0140	56	0686	89	0755	122-125	0239
		57	0683			126	0205
23	0301	58	0371	91	0756	128	0686
26	0690	59,61	0755	92	0141		
27	0756	62	0301	95	0690	131	0377
28	0759	63	0842	96	0141	137	0683
29	0424	65	0140	97	0706	138	0424
		69	**0755**	98	0629	139	0759
33	0301	71	0759	99	0842	141	0377
36	0690	72	0301			147,148	0376
37	0371	73	0140	102	0608	149	0755
38	0376	75	0629	106	0370		
39	0629	76	0239	107	0629	151	0207
		77	0842	108	0608	159	0755
41	0756	78	0301	109	0706	167	0376
43	0301	79,81	0759			169	0755
46	0690	82	0301	112	0239		
47	0370	85	0629	113,114	0205		





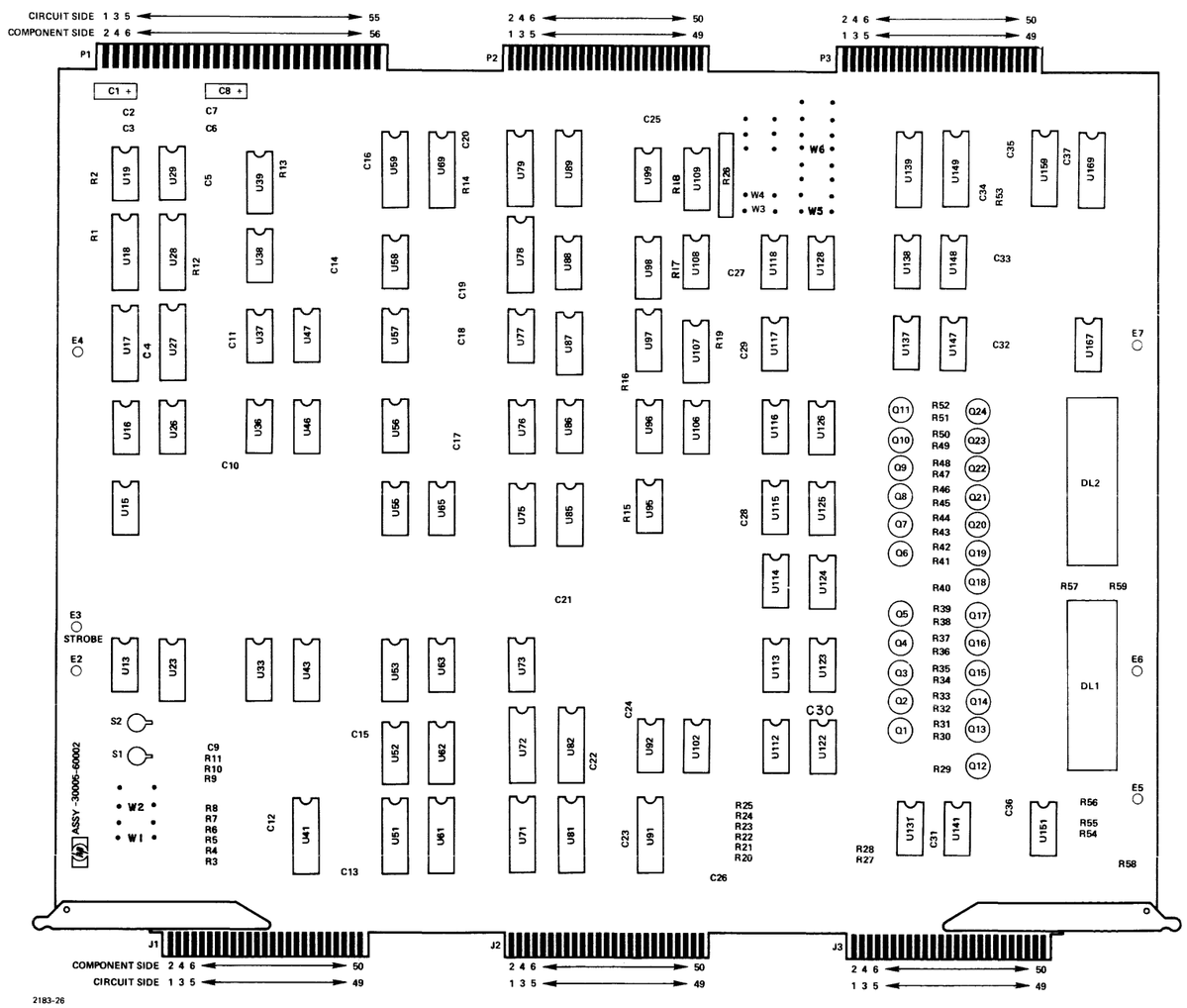
13828-1
1382C-1
CHANGE REFERENCE REVISION/PREFIX
A ORIG A-1210-22
B REDRAWN NO CHANGE
C ERRATA NO CHANGE
DLY-1 FF U85A
DLY-2 FF U85B
DELAY LINE NO. 1
DELAY LINE NO. 2
MRTE FF
DATA EARLY GATE FF
SET BUS REQ FF
BUS/SA DATA FF
STROBE FF
MSG FF
START DLY 2 FF
MIT FF
MWT FF
MWTE FF
MR'TE FF
MR'T FF
MW'TEX FF
TYPICAL RS FF
RESET DLY-2 FF
RESET DATA EARLY FF
MCU RST
DATA EARLY GATE (B6)
SET BUS REQ FF (A4)
BUS/SA DATA (D22)
STROBE (F8)
START DLY-2 FF (F12)
P3-4 MRTE
J2-32 MSG
J3-30 MIT
P3-21 MWT
P3-6 MWTE
P3-33 MR'TE
P3-37 MW'TEXE
P3-29 MR'T
P3-31 MW'TEX
30005-60002
MEMORY DATA AND CONTROL PCA
SHEET 2/3

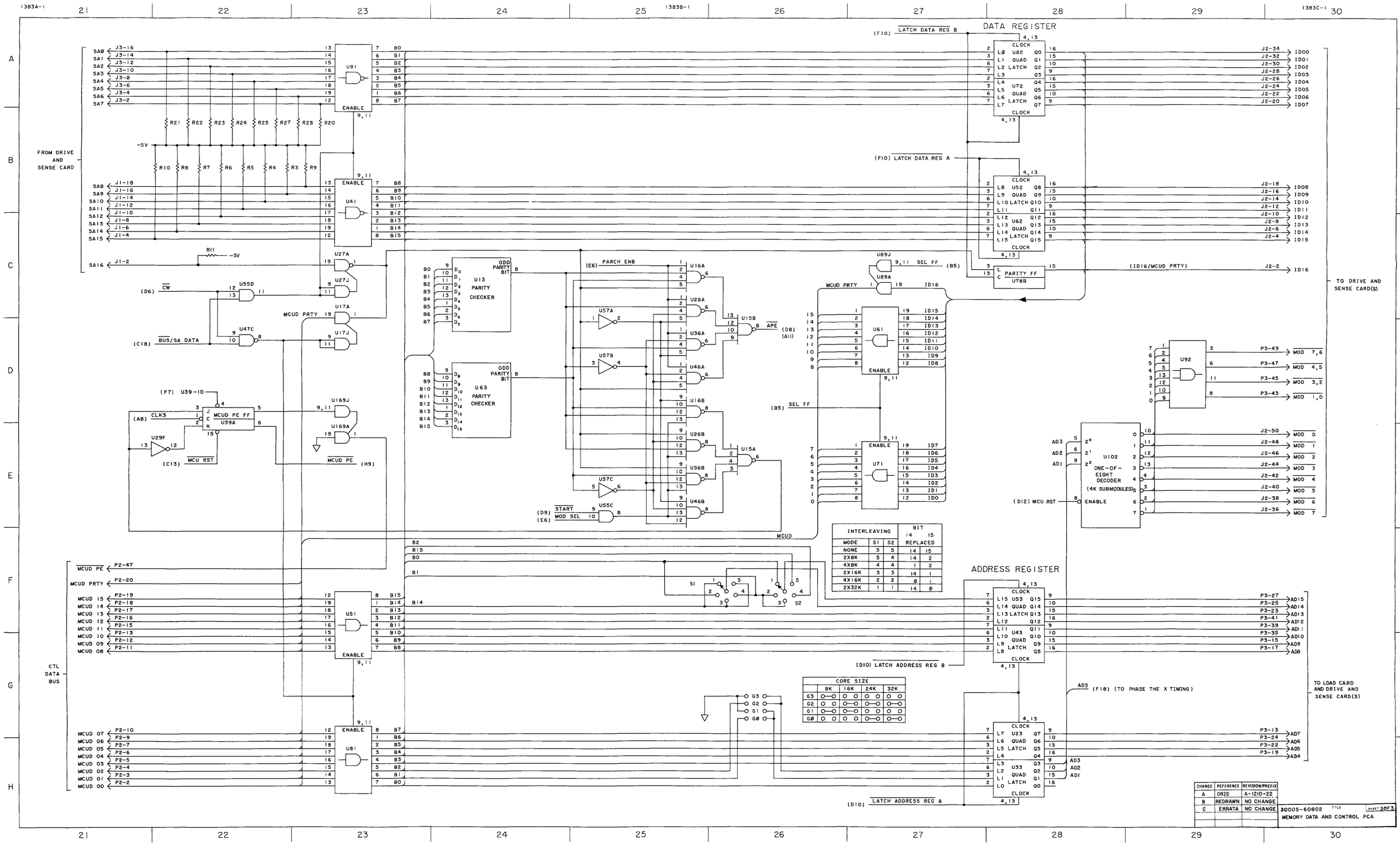
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1		1		1		1	
2	+5V	2	MCUD 00	2		2	SA16	2	ID16	2	SA7
3	+5V	3	MCUD 01	3		3		3		3	
4	+5V	4	MCUD 02	4	$\overline{\text{MRTE}}$	4	SA15	4	ID15	4	SA6
5		5	MCUD 03	5		5		5		5	
6	ENTIMER	6	MCUD 04	6	$\overline{\text{MWTE}}$	6	SA14	6	ID14	6	SA5
7		7	MCUD 05	7		7		7		7	
8		8	COM	8		8	SA13	8	ID13	8	SA4
9		9	MCUD 06	9		9		9		9	
10		10	MCUD 07	10		10	SA12	10	ID12	10	SA3
11		11	MCUD 08	11		11		11		11	
12		12	MCUD 09	12		12	SA11	12	ID11	12	SA2
13	$\overline{\text{MCUCLKS}}$	13	MCUD 10	13	AD7	13		13		13	
14	COM	14	COM	14		14	SA10	14	ID10	14	SA1
15	COM	15	MCUD 11	15	AD9	15		15		15	
16	COM	16	MCUD 12	16		16	SA9	16	ID09	16	SA0
17	-5V	17	MCUD 13	17	AD8	17		17		17	
18	-5V	18	MCUD 14	18		18	SA8	18	ID08	18	
19	COM	19	MCUD 15	19	AD4	19		19		19	
20	COM	20	MCUD PRTY	20		20		20	ID07	20	
21		21	COM	21	$\overline{\text{MWT}}$	21		21		21	
22		22	'TO' 00	22	AD5	22		22	ID06	22	
23		23	'TO' 01	23	AD13	23		23	MSG	23	
24		24	'TO' 02	24	AD6	24		24	ID05	24	
25		25	'FROM' 00	25	AD14	25		25		25	
26		26	'FROM' 01	26		26		26	ID04	26	
27		27	'FROM' 02	27	AD15	27		27		27	
28		28	MOP 00	28		28		28	ID03	28	
29	COM	29	MOP 01	29	$\overline{\text{MR'T}}$	29		29		29	
30	COM	30	COM	30		30		30	ID02	30	
31		31		31	MW'TEX	31		31		31	
32		32	SYS PRTY	32		32		32	ID01	32	
33		33	READY 00	33	MR'TE	33		33		33	
34		34	READY 01	34		34		34	ID00	34	
35		35	READY 02	35	AD10	35		35		35	
36		36	READY 03	36		36		36	$\overline{\text{MODE 7}}$	36	
37		37		37	$\overline{\text{MW'TEXE}}$	37		37		37	
38		38		38		38		38	$\overline{\text{MODE 6}}$	38	
39		39	COM	39	AD11	39		39		39	
40		40	ENABLE 00	40		40		40	$\overline{\text{MODE 5}}$	40	
41		41	ENABLE 01	41	AD12	41		41		41	
42		42	ENABLE 02	42		42		42	$\overline{\text{MODE 4}}$	42	
43		43	ENABLE 03	43	$\overline{\text{MODE 1,0}}$	43		43		43	
44		44		44		44		44	$\overline{\text{MODE 3}}$	44	
45		45		45	$\overline{\text{MODE 3,2}}$	45		45		45	
46		46	COM	46		46		46	$\overline{\text{MODE 2}}$	46	
47		47	MCUD PE	47	$\overline{\text{MODE 5,4}}$	47		47		47	
48		48	$\overline{\text{SYS PE}}$	48		48		48	$\overline{\text{MODE 1}}$	48	
49		49	$\overline{\text{MCU RST}}$	49	$\overline{\text{MODE 7,6}}$	49		49		49	
50		50	COM	50		50		50	$\overline{\text{MODE 0}}$	50	
51											
52											
53											
54											
55											
56											

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
13	0842	51	0759	86	0239	115-117	0239
15,16	0690	52,53	0301	87	0301	118	0376
17,18	0759	55	0141	88	0370		
19	0140	56	0686	89	0755	122-125	0239
		57	0683			126	0205
23	0301	58	0371	91	0756	128	0686
26	0690	59,61	0755	92	0141		
27	0756	62	0301	95	0690	131	0377
28	0759	63	0842	96	0141	137	0683
29	0424	65	0140	97	0706	138	0424
		69	**0755**	98	0629	139	0759
33	0301	71	0759	99	0842	141	0377
36	0690	72	0301			147,148	0376
37	0371	73	0140	102	0608	149	0755
38	0376	75	0629	106	0370		
39	0629	76	0239	107	0629	151	0207
		77	0842	108	0608	159	0755
41	0756	78	0301	109	0706	167	0376
43	0301	79,81	0759			169	0755
46	0690	82	0301	112	0239		
47	0370	85	0629	113,114	0205		





INTERLEAVING			BIT 14	BIT 15
MODE	S1	S2	REPLACED	
NONE	5	5	14	15
2X8K	5	4	14	2
4X8K	4	4	1	2
2X16K	3	3	14	1
4X16K	2	2	0	1
2X32K	1	1	14	0

CORE SIZE	8K	16K	24K	32K
G3	●	○	○	○
G2	○	●	○	○
G1	●	○	●	○
G0	○	○	○	●

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

30005-60902 TITLE SHEET 30F3
MEMORY DATA AND CONTROL PCA

CPU/IOP DETAILED DIAGRAM SET

DD-302

MEMORY DRIVE AND SENSE PCA

30006-60002

SERIES 1247

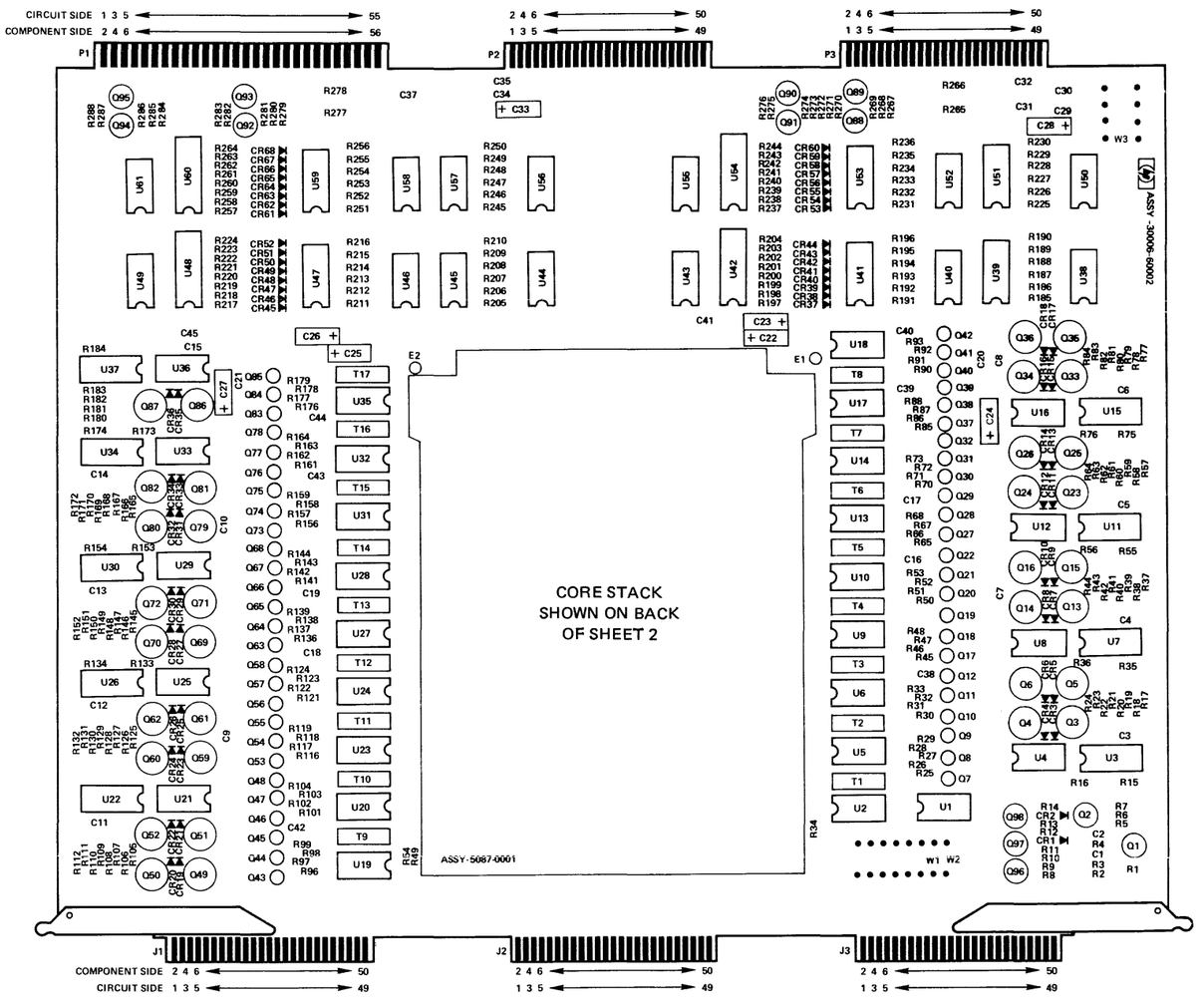
1242

SIGNAL INDEX

P1		P2		P3		J1		J2		J3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1	COM	1		1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	SA16	2	ID16	2	SA7
3	+5V	3	COM	3		3	COM	3	COM	3	COM
4	+5V	4	COM	4	$\overline{\text{MRTE}}$	4	SA15	4	ID15	4	SA6
5	+5V	5	COM	5		5	COM	5	COM	5	COM
6	+5V	6	COM	6	$\overline{\text{MWTE}}$	6	SA14	6	ID14	6	SA5
7	+5V	7	COM	7		7	COM	7	COM	7	COM
8	+5V	8	COM	8	COM	8	SA13	8	ID13	8	SA4
9		9		9	COM	9	COM	9	COM	9	COM
10		10		10	COM	10	SA12	10	ID12	10	SA3
11		11	COM	11		11	COM	11	COM	11	COM
12		12		12	COM	12	SA11	12	ID11	12	SA2
13		13		13		13	COM	13	COM	13	COM
14		14		14	COM	14	SA10	14	ID10	14	SA1
15		15	COM	15		15	COM	15	COM	15	COM
16		16		16	COM	16	SA9	16	ID9	16	SA0
17	−5V	17		17		17	COM	17	COM	17	COM
18	−5V	18		18	COM	18	SA8	18	ID8	18	
19		19	COM	19	AD4	19	COM	19	COM	19	COM
20		20		20	COM	20		20	ID7	20	
21	+15V	21		21		21	COM	21	COM	21	COM
22	+15V	22		22	AD5	22		22	ID6	22	
23	+15V	23	COM	23		23	COM	23	COM	23	COM
24	+15V	24		24	AD6	24		24	ID5	24	
25		25		25		25	COM	25	COM	25	COM
26		26		26	COM	26		26	ID4	26	
27		27	COM	27		27	COM	27	COM	27	COM
28		28		28	COM	28		28	ID3	28	
29		29		29		29	COM	29	COM	29	$\overline{\text{COM}}$
30		30		30	COM	30		30	ID2	30	$\overline{\text{MIT}}$
31	−20V	31	COM	31		31	COM	31	COM	31	$\overline{\text{COM}}$
32	−20V	32		32	$\overline{\text{COM}}$	32		32	ID1	32	$\overline{\text{MSG}}$
33	−20V	33		33	$\overline{\text{MR'TE}}$	33	COM	33	COM	33	COM
34	−20V	34		34	COM	34		34	ID0	34	
35	+20V	35	COM	35	AD10	35	COM	35	$\overline{\text{COM}}$	35	COM
36	+20V	36		36	$\overline{\text{COM}}$	36	IDR15	36	$\overline{\text{MOD 7}}$	36	IDR7
37	+20V	37		37	$\overline{\text{MW'TEXE}}$	37	COM	37	$\overline{\text{COM}}$	37	COM
38	+20V	38		38	COM	38	IDR14	38	$\overline{\text{MOD 6}}$	38	IDR6
39	+20V	39	COM	39	AD11	39	COM	39	$\overline{\text{COM}}$	39	COM
40	+20V	40		40	COM	40	IDR13	40	$\overline{\text{MOD 5}}$	40	IDR5
41		41		41	AD12	41	COM	41	COM	41	COM
42		42		42	$\overline{\text{COM}}$	42	IDR12	42	$\overline{\text{MOD 4}}$	42	IDR4
43		43	COM	43	$\overline{\text{MOD 0,1}}$	43	COM	43	COM	43	COM
44		44		44	$\overline{\text{COM}}$	44	IDR11	44	$\overline{\text{MOD 3}}$	44	IDR3
45		45		45	$\overline{\text{MOD 2,3}}$	45	COM	45	COM	45	COM
46		46		46	$\overline{\text{COM}}$	46	IDR10	46	$\overline{\text{MOD 2}}$	46	IDR2
47		47	COM	47	$\overline{\text{MOD 4,5}}$	47	COM	47	$\overline{\text{COM}}$	47	COM
48		48		48	$\overline{\text{COM}}$	48	IDR9	48	$\overline{\text{MOD 1}}$	48	IDR1
49		49		49	$\overline{\text{MOD 6,7}}$	49	COM	49	$\overline{\text{COM}}$	49	COM
50		50		50	COM	50	IDR8	50	$\overline{\text{MOD 0}}$	50	IDR0
51											
52											
53											
54											
55											
56											

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
1	0205	21	0621	38	0006	52	0006
2	0105	22	3180	39	3130	53	3130
3	3180	23,24	0001	40	0006	54	0756
4	0621	25	0621	41	3100	55	0239
5,6	0001	26	3180	42	0756	56	0006
7	3180	27,28	0001	43	0608	57	3130
8	0621	29	0621	44	0006	58	0006
9,10	0001	30	3180	45	3130	59	3130
11	3180	31,32	0001	46	0006		
12	0621	33	0621	47	3130		
13,14	0001	34	3180	48	0756		
15	3180	35	0001	49	0608		
16	0621	36	0621	50	0006		
17–20	0001	37	3180	51	3130		



1082A-1

SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16

BIT0 BIT1 BIT2 BIT3 BIT4 BIT5 BIT6 BIT7 BIT8 BIT9 BIT10 BIT11 BIT12 BIT13 BIT14 BIT15 BIT16

IDR0 IDR1 IDR2 IDR3 IDR4 IDR5 IDR6 IDR7 IDR8 IDR9 IDR10 IDR11 IDR12 IDR13 IDR14 IDR15 IDR16

ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7 ID8 ID9 ID10 ID11 ID12 ID13 ID14 ID15 ID16

MSG = 4:8K

MSG = 0:4K

0:4K, MIT

0:4K-MIT

4:8K MIT

PLACE PAIR OF JUMPERS AS PER CARD LOCATION

0:4K 4:8K

MOD 0 MOD 1 MOD 2 MOD 3 MOD 4 MOD 5 MOD 6 MOD 7

MSG MIT

3. VALUE OF R1 IS FIXED DURING MANUFACTURE

2. ALL RESISTOR VALUES ARE IN OHMS

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

C3 THRU C6, C11 THRU C15, C20, C21, C41: +5V, P1-1 THRU 8, 4, 1.0, C27 C24 10

C42 C38 200PF, C26 C23 10, C17, C19, C45, 1.0: -5V, P1-17, 18

C16 C18 1.0, C22, C25 10: +15V, P1-21 THRU 24

C30 C35 1.0: +20V, P1-35 THRU 40

C7 THRU C10, C29, C34 1.0, C28 6.8, C33 6.8: -20V, P1-31 THRU 34

THRESHOLD ADJ. CKT

R2 31.6, R1 100, R3 383, C1 1.0, R4 110, C2 1.0, Q1, V_{TH}, +5V, -5V

SENSE AMPLIFIER

TYPICAL U5,6,9,10,13,14,17,18,19,20, 23,24,27,28,31,32 AND 35 (1858-0001)

TYPICAL 81-817 BALUN MODULE

COMMON RETURN

COMMON ← J1 ALL ODD NO.S 1 THRU 49

COMMON ← J2 ALL ODD NO.S 1 THRU 49

COMMON ← J3 ALL ODD NO.S 1 THRU 49,34

P1-15, 16, 19, 20, 29, 30

P2 1-8, 11, 15, 19, 23, 27, 31, 35, 39, 43, AND 47

COMMON ← P3 EVENS 2, 8-20, 26-50

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1565	A-1242-22	1
D	22-1613	B-1247-22	1
E	ERRATA	NO CHANGE	1

30006-60002 TITLE SHEET 1 OF 2

MEMORY DRIVE & SENSE PCA

ENGINEER APPROVED DATE

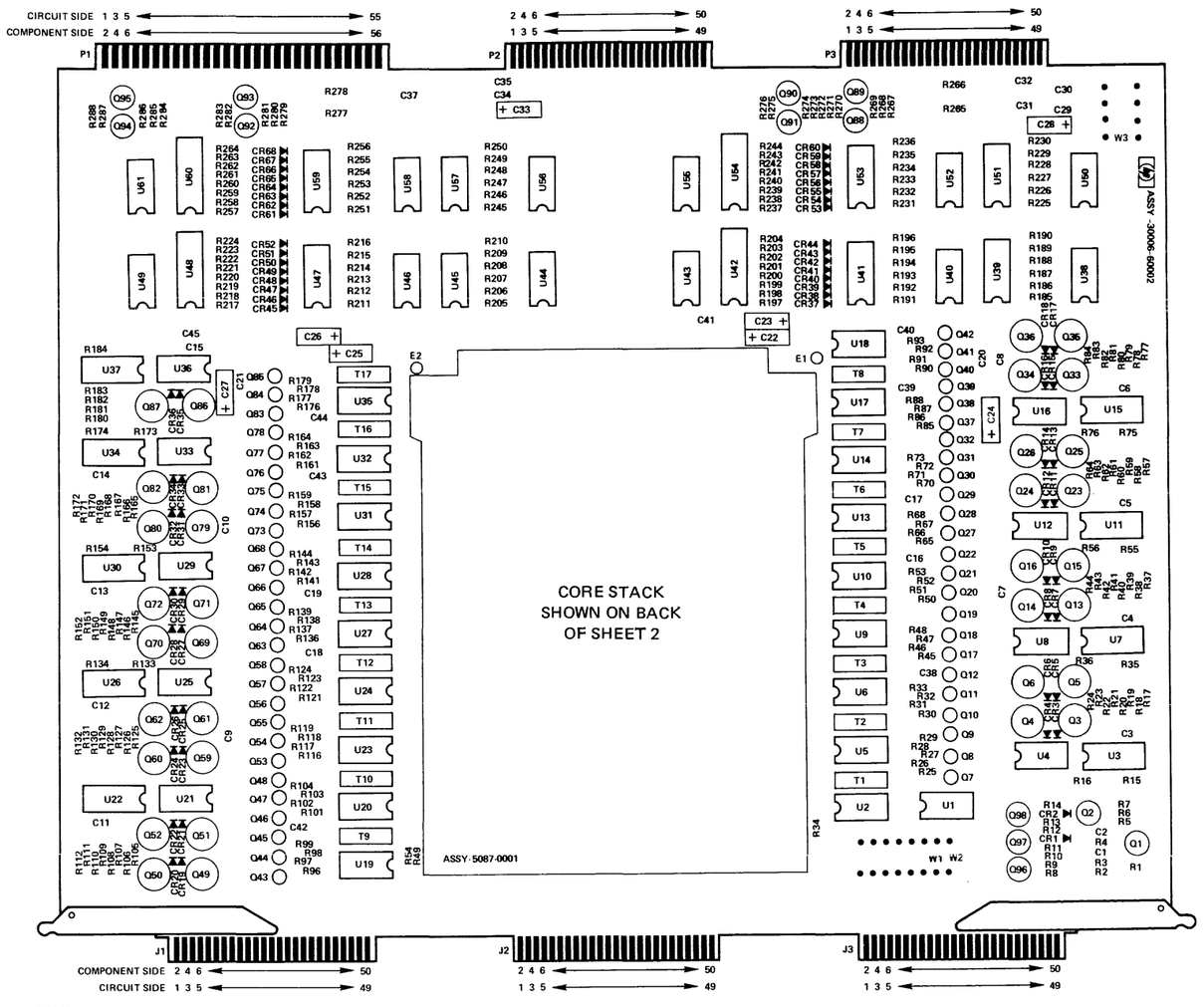
HEWLETT PACKARD CO

SIGNAL INDEX

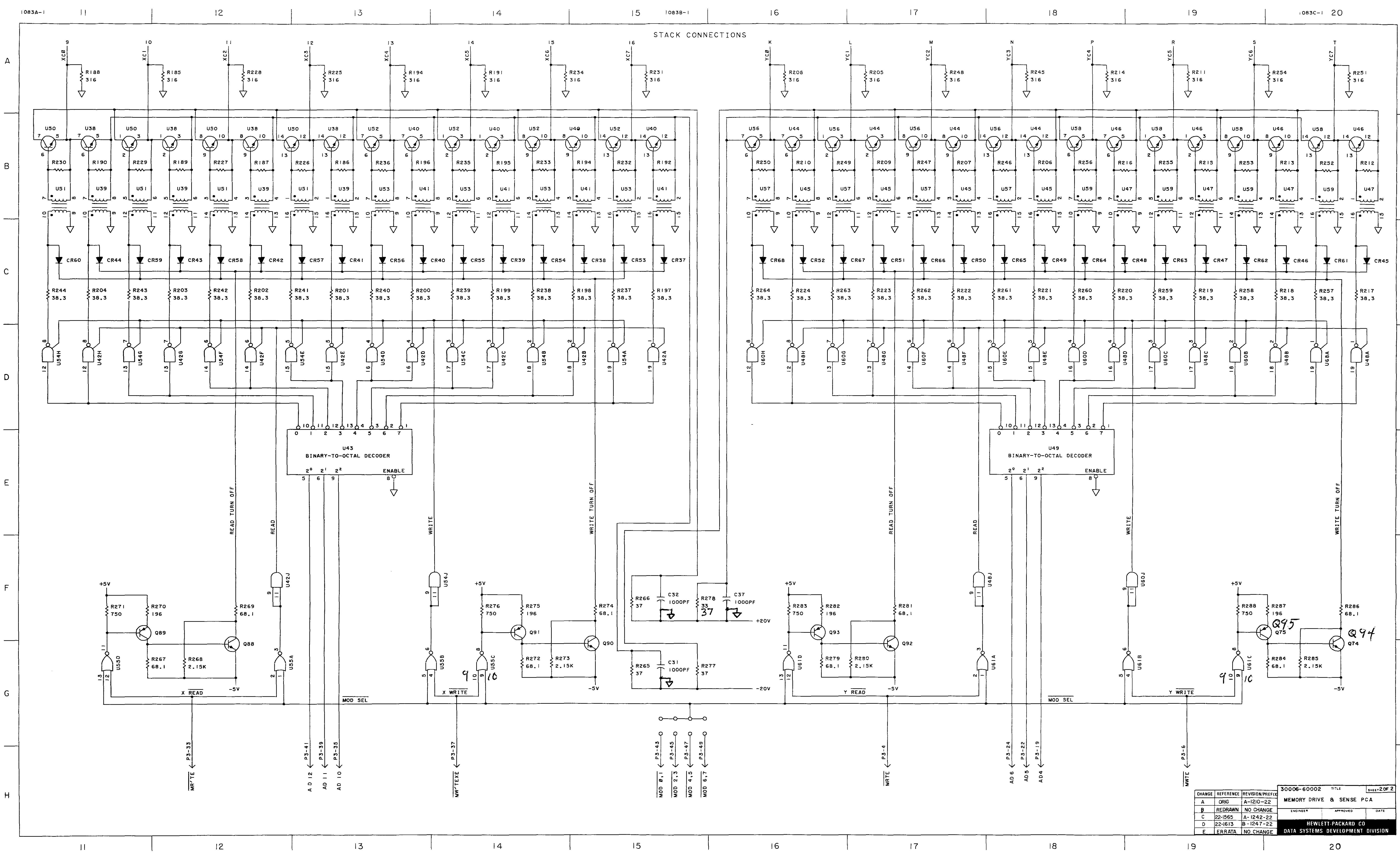
P1		P2		P3		J1		J2		J3	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	1	COM	1		1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	SA16	2	ID16	2	SA7
3	+5V	3	COM	3		3	COM	3	COM	3	COM
4	+5V	4	COM	4	$\overline{\text{MRTE}}$	4	SA15	4	ID15	4	SA6
5	+5V	5	COM	5		5	COM	5	COM	5	COM
6	+5V	6	COM	6	$\overline{\text{MWTE}}$	6	SA14	6	ID14	6	SA5
7	+5V	7	COM	7		7	COM	7	COM	7	COM
8	+5V	8	COM	8	COM	8	SA13	8	ID13	8	SA4
9		9		9		9	COM	9	COM	9	COM
10		10		10	COM	10	SA12	10	ID12	10	SA3
11		11	COM	11		11	COM	11	COM	11	COM
12		12		12	COM	12	SA11	12	ID11	12	SA2
13		13		13		13	COM	13	COM	13	COM
14		14		14	COM	14	SA10	14	ID10	14	SA1
15		15	COM	15		15	COM	15	COM	15	COM
16		16		16	COM	16	SA9	16	ID9	16	SA0
17	−5V	17		17		17	COM	17	COM	17	COM
18	−5V	18		18	COM	18	SA8	18	ID8	18	
19		19	COM	19	AD4	19	COM	19	COM	19	COM
20		20		20	COM	20		20	ID7	20	
21	+15V	21		21		21	COM	21	COM	21	COM
22	+15V	22		22	AD5	22		22	ID6	22	
23	+15V	23	COM	23		23	COM	23	COM	23	COM
24	+15V	24		24	AD6	24		24	ID5	24	
25		25		25		25	COM	25	COM	25	COM
26		26		26	COM	26		26	ID4	26	
27		27	COM	27		27	COM	27	COM	27	COM
28		28		28	COM	28		28	ID3	28	
29		29		29		29	COM	29	COM	29	$\overline{\text{COM}}$
30		30		30	COM	30		30	ID2	30	$\overline{\text{MIT}}$
31	−20V	31	COM	31		31	COM	31	COM	31	$\overline{\text{COM}}$
32	−20V	32		32	$\overline{\text{COM}}$	32		32	ID1	32	$\overline{\text{MSG}}$
33	−20V	33		33	$\overline{\text{MR'TE}}$	33	COM	33	COM	33	COM
34	−20V	34		34	COM	34		34	ID0	34	
35	+20V	35	COM	35	AD10	35	COM	35	COM	35	COM
36	+20V	36		36	$\overline{\text{COM}}$	36	IDR15	36	$\overline{\text{MOD 7}}$	36	IDR7
37	+20V	37		37	$\overline{\text{MW'TEXE}}$	37	COM	37	$\overline{\text{COM}}$	37	COM
38	+20V	38		38	COM	38	IDR14	38	$\overline{\text{MOD 6}}$	38	IDR6
39	+20V	39	COM	39	AD11	39	COM	39	$\overline{\text{COM}}$	39	COM
40	+20V	40		40	COM	40	IDR13	40	$\overline{\text{MOD 5}}$	40	IDR5
41		41		41	AD12	41	COM	41	$\overline{\text{COM}}$	41	COM
42		42		42	$\overline{\text{COM}}$	42	IDR12	42	$\overline{\text{MOD 4}}$	42	IDR4
43		43	COM	43	$\overline{\text{MOD 0,1}}$	43	COM	43	COM	43	COM
44		44		44	$\overline{\text{COM}}$	44	IDR11	44	$\overline{\text{MOD 3}}$	44	IDR3
45		45		45	$\overline{\text{MOD 2,3}}$	45	COM	45	$\overline{\text{COM}}$	45	COM
46		46		46	$\overline{\text{COM}}$	46	IDR10	46	$\overline{\text{MOD 2}}$	46	IDR2
47		47	COM	47	$\overline{\text{MOD 4,5}}$	47	COM	47	$\overline{\text{COM}}$	47	COM
48		48		48	$\overline{\text{COM}}$	48	IDR9	48	$\overline{\text{MOD 1}}$	48	IDR1
49		49		49	$\overline{\text{MOD 6,7}}$	49	COM	49	$\overline{\text{COM}}$	49	COM
50		50		50	COM	50	IDR8	50	$\overline{\text{MOD 0}}$	50	IDR0
51											
52											
53											
54											
55											
56											

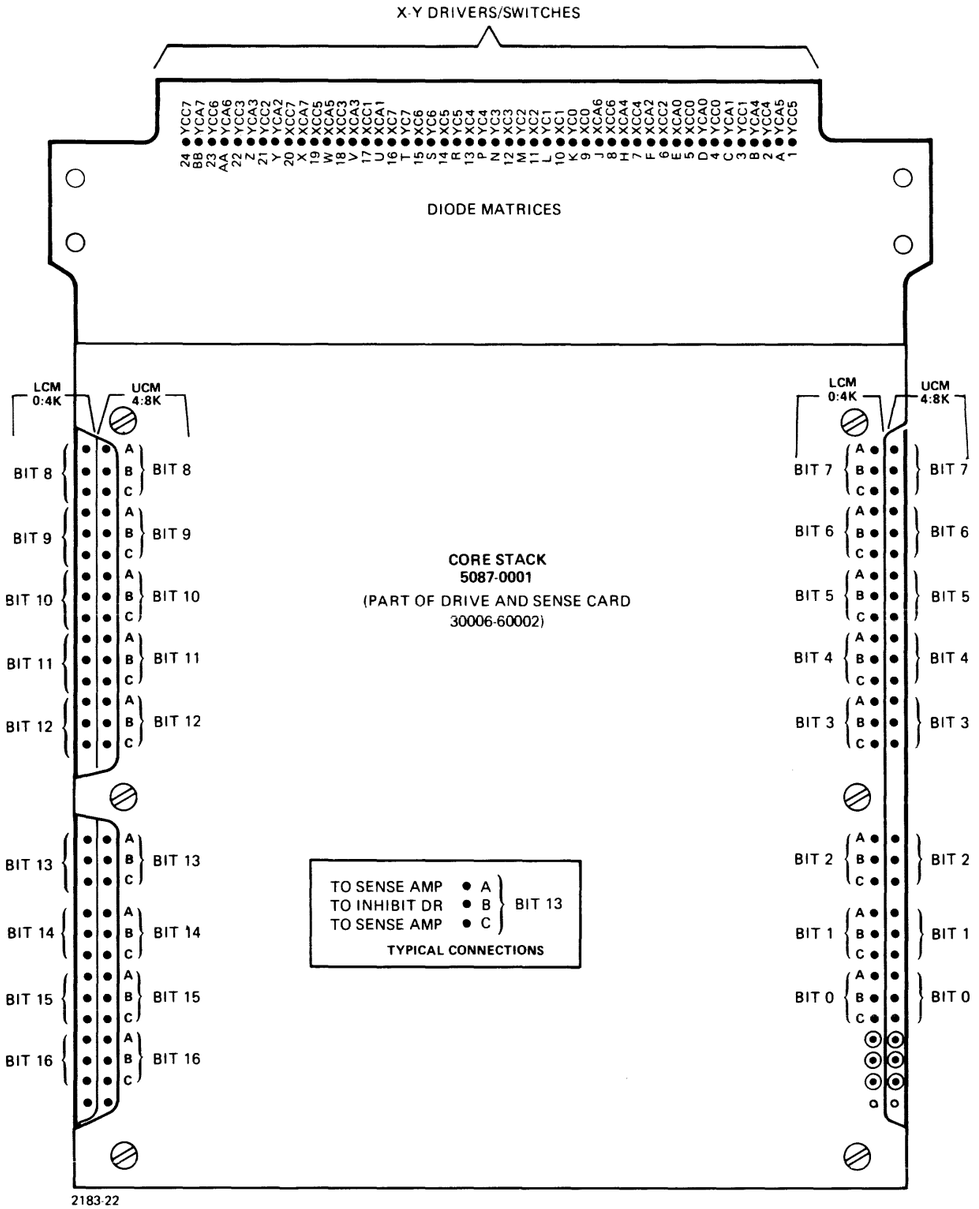
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
1	0205	21	0621	38	0006	52	0006
2	0105	22	3180	39	3130	53	3130
3	3180	23,24	0001	40	0006	54	0756
4	0621	25	0621	41	3100	55	0239
5,6	0001	26	3180	42	0756	56	0006
7	3180	27,28	0001	43	0608	57	3130
8	0621	29	0621	44	0006	58	0006
9,10	0001	30	3180	45	3130	59	3130
11	3180	31,32	0001	46	0006		
12	0621	33	0621	47	3130		
13,14	0001	34	3180	48	0756		
15	3180	35	0001	49	0608		
16	0621	36	0621	50	0006		
17–20	0001	37	3180	51	3130		



2183-28


1083A-1
1083B-1
1083C-1
STACK CONNECTIONS
XC0 XC1 XC2 XC3 XC4 XC5 XC6 XC7
YC0 YC1 YC2 YC3 YC4 YC5 YC6 YC7
U43
BINARY-TO-OCTAL DECODER
ENABLE
U49
BINARY-TO-OCTAL DECODER
ENABLE
READ TURN OFF
READ
WRITE
WRITE TURN OFF
+5V
-5V
+20V
-20V
X READ
MOD SEL
X WRITE
Y READ
Y WRITE
P3-33
P3-41
P3-39
P3-35
P3-37
P3-43
P3-45
P3-47
P3-49
P3-4
P3-24
P3-22
P3-19
P3-6
MRTE
AD 12
AD 11
AD 10
MWTEXE
MOD 0,1
MOD 2,3
MOD 4,5
MOD 6,7
MRTE
AD 6
AD 5
AD 4
MWTE
CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG | A-1210-22
B | REDRAWN | NO CHANGE
C | 22-1565 | A-1242-22
D | 22-1613 | B-1247-22
E | ERRATA | NO CHANGE
30006-60002
SHEET 2 OF 2
MEMORY DRIVE & SENSE PCA
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION


X-Y DRIVERS/SWITCHES
24 YCC7
BB YCA7
23 YCC6
AA YCA6
22 YCC3
Z YCA3
21 YCC2
Y YCA2
20 XCC7
X XCA7
19 XCC5
W XCA5
18 XCC3
V XCA3
17 XCC1
U XCA1
16 XC7
T YC7
15 XC6
S YC6
14 XC5
R YC5
13 XC4
P YC4
N YC3
12 XC3
M YC2
11 XC2
L YC1
10 XC1
K YC0
9 XCA6
J XCC6
8 XCA4
H XCC4
7 XCA2
F XCC2
6 XCA0
E XCC0
5 YCA0
D YCC0
4 YCA1
C YCC1
3 YCA4
B YCC4
2 YCA5
A YCC5
DIODE MATRICES
LCM 0:4K
UCM 4:8K
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
BIT 15
BIT 16
A
B
C
CORE STACK
5087-0001
(PART OF DRIVE AND SENSE CARD
30006-60002)
TO SENSE AMP
TO INHIBIT DR
TO SENSE AMP
TYPICAL CONNECTIONS
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0

2183-22

I/O DETAILED DIAGRAM SET

DD-404

SYSTEM CLOCK/CONSOLE INTERFACE PCA

30031-60001

SERIES 1249

REV C

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARNING
6	
7	
8	
9	PWR ON
10	
11	I/O RESET
12	RESET COM
13	CLK
14	CLK COM
15	COM
16	COM
17	−5V
18	−5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	−15V
26	−15V
27	−15V
28	−15V
29	COM
30	COM
31	−20V
32	−20V
33	−20V
34	−20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSR SIG
42	SIG COM
43	COM
44	INTPOLL OUT
45	
46	
47	COM
48	INTPOLL IN
49	SI
50	COM
51	
52	
53	SO
54	COM
55	
56	

P2

PIN	SIGNAL
1	
2	COM
3	
4	COM
5	
6	COM
7	
8	COM
9	
10	COM
11	
12	
13	
14	COM
15	COM
16	
17	
18	
19	
20	COM
21	
22	
23	COM
24	
25	
26	
27	
28	
29	
30	COM
31	
32	
33	
34	
35	
36	COM
37	
38	
39	
40	
41	
42	COM
43	
44	
45	
46	
47	
48	
49	
50	

P3

PIN	SIGNAL
1	
2	
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	
46	COM
47	
48	
49	COM
50	INTACK

J1

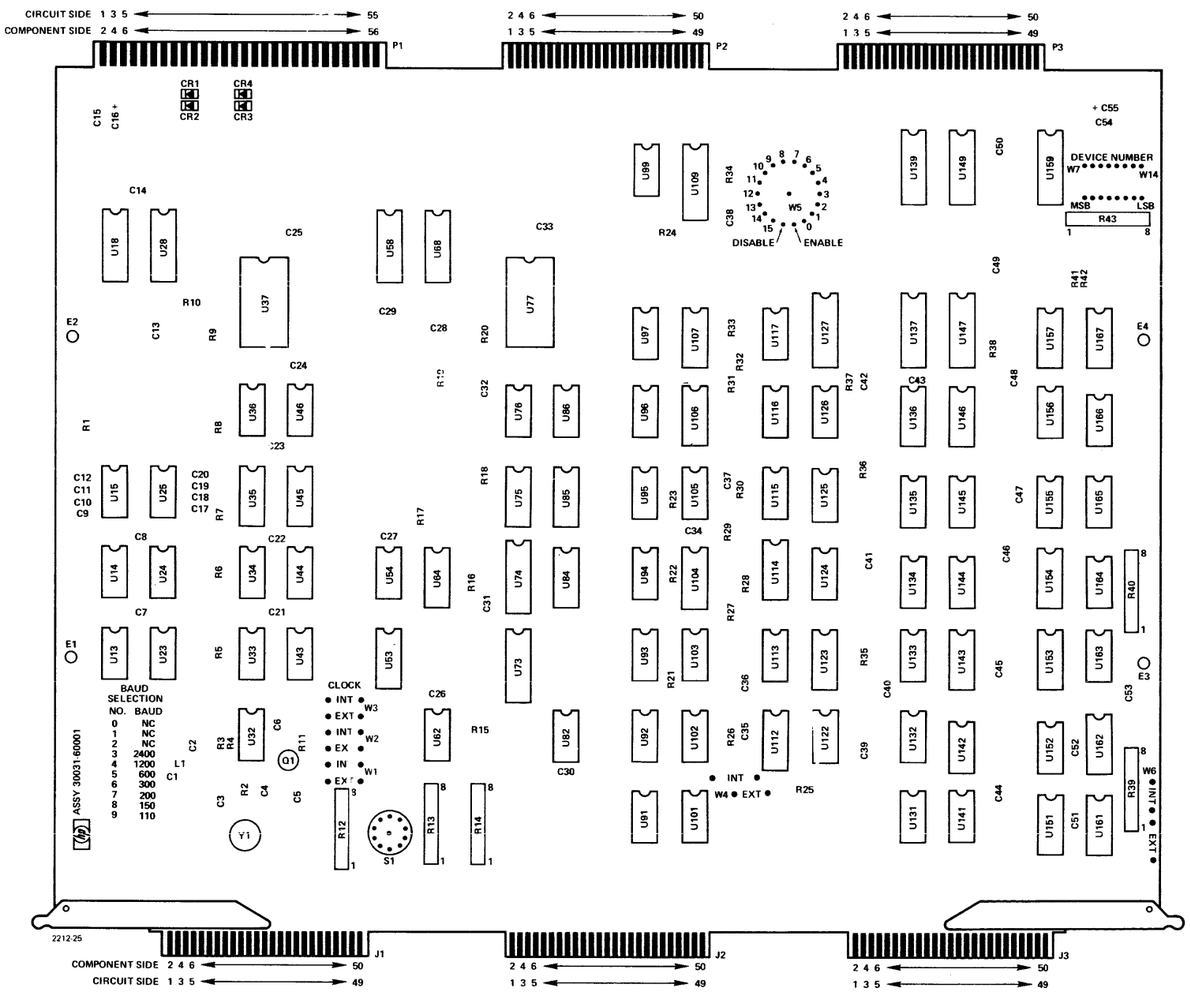
PIN	SIGNAL
1	PROTECTIVE GROUND (AA)
2	SIGNAL GROUND (AB)
3	RECEIVED DATA (BB)
4	RECEIVED DATA (BB)
5	CLEAR TO SEND (CB)
6	CLEAR TO SEND (CB)
7	DATA SET READY (CC)
8	DATA SET READY (CC)
9	TRANSMITTED DATA (BA)
10	TRANSMITTED DATA (BA)
11	DATA TERMINAL READY (CD)
12	DATA TERMINAL READY (CD)
13	CARRIER DETECT (CF)
14	CARRIER DETECT (CF)
15	RINGING INDICATOR(CE)
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	2400 BAUD
36	COM
37	1200 BAUD
38	COM
39	600 BAUD
40	COM
41	300 BAUD
42	COM
43	200 BAUD
44	COM
45	150 BAUD
46	COM
47	110 BAUD
48	COM
49	
50	COM

J2

PIN	SIGNAL
1	COM
2	EXT CLK
3	COM
4	CLK
5	COM
6	CLK
7	COM
8	10S
9	COM
10	1 S
11	COM
12	100 MS
13	COM
14	10 MS
15	COM
16	1 MS
17	COM
18	100 US
19	COM
20	10 US
21	COM
22	1 US
23	COM
24	COUNT PULSE
25	
26	EXT BIT CLOCK
27	
28	BIT CLOCK OUTPUT
29	
30	TEST
31	
32	BIT CLOCK CLEAR
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820	U	1820-
13,14	0751	53	0622	92	0141	115	0471	141	0371	163	0294
15	0609	54	0668	93,94	0512	116	0424	142	0239	164	0512
18	0755	58	0755	95	0077	117	0141	143	0629	165,166	0765
				96	0374	122	0077	144	0141	167	0626
23,24	0751	62	0668	97	0370	113	0372	145	0765		
25	0990	64	0629	99	0686	124	0141	146	0706		
28	0755	68	0755			125	0205	147	0760		
				101	0372	126	0370	149	0756		
32	0142	73,74	0755	102,103	0424	127	0760				
33,34	1715	75	0233	104	0629			151	0231		
35	0233	76	0719	105	0844	131	0370	152	0424		
36	0719	77	0742	106	0301	132	0141	153,154	0574		
37	0742			107	0491	133	0372	155	0512		
		82	0141	109	0760	134,135	0205	156	0424		
43,44	0751	85	0233			136	0706	157	0262		
45	0233	86	0719	112	0515	137	0760	159	0756		
46	0719			113	0370	139	0756				
		91	0370	114	0834			161,162	0231		



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1220-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1618	A-1249-22	1
D	ERRATA	NO CHANGE	1,2

SI POSITION	BAUD RATE
0,1,2	NC
3	2400
4	1200
5	600
6	300
7	200
8	150
9	110

(NOTE 4)

BAUD RATE SELECTION

COMMAND DECODER

DEVICE NUMBER COMPARATOR

DEVICE NUMBER GENERATOR

COMMON

P2-2,4,6,8,10,14,15,20,
23,30,36,42

P3-3,7,10,13,16,19,22,25,28
31,34,37,40,43,46,49

NOTES:

1. ALL LOGIC IS POSITIVE TRUE

2. UNLESS OTHERWISE SPECIFIED ALL DISCRETE RESISTORS ARE 4.64K AND ALL RESISTORS IN PACKS ARE 4.7K

3. SELECT ONE OF 18 MASK POSITIONS.

4. IF BAUD RATE IS SELECTED BY CONNECTION IN J1 SWITCH S1 MUST BE IN POSITION 0,1, OR 2.

5. JUMPER INSTALLED SELECTS LOGIC 0 IN DEVICE NUMBER

30031-60001	TITLE	SHEET 1 OF 3
SYSTEM CLOCK/CONSOLE INTERFACE PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARNING
6	
7	
8	
9	PWR ON
10	
11	I/O RESET
12	RESET COM
13	CLK
14	CLK COM
15	COM
16	COM
17	−5V
18	−5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	−15V
26	−15V
27	−15V
28	−15V
29	COM
30	COM
31	−20V
32	−20V
33	−20V
34	−20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSR SIG
42	SIG COM
43	COM
44	INTPOLL OUT
45	
46	
47	COM
48	INTPOLL IN
49	SI
50	COM
51	
52	
53	SO
54	COM
55	
56	

P2

PIN	SIGNAL
1	
2	COM
3	
4	COM
5	
6	COM
7	
8	COM
9	
10	COM
11	
12	
13	
14	COM
15	COM
16	
17	
18	
19	
20	COM
21	
22	
23	COM
24	
25	
26	
27	
28	
29	
30	COM
31	
32	
33	
34	
35	
36	COM
37	
38	
39	
40	
41	
42	COM
43	
44	
45	
46	
47	
48	
49	
50	

P3

PIN	SIGNAL
1	
2	
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	
46	COM
47	
48	
49	COM
50	INTACK

J1

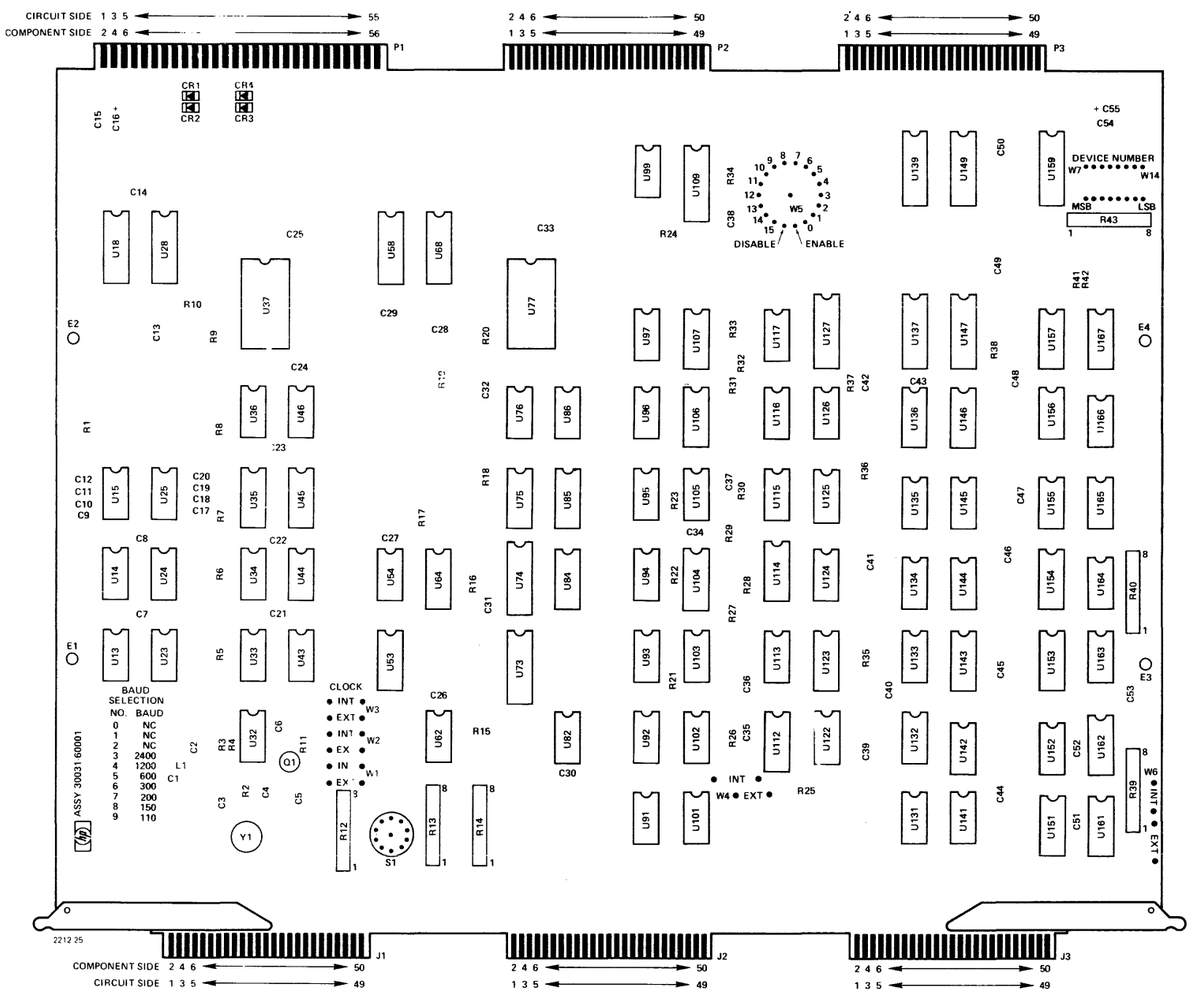
PIN	SIGNAL
1	PROTECTIVE GROUND (AA)
2	SIGNAL GROUND (AB)
3	RECEIVED DATA (BB)
4	RECEIVED DATA (BB)
5	CLEAR TO SEND (CB)
6	CLEAR TO SEND (CB)
7	DATA SET READY (CC)
8	DATA SET READY (CC)
9	TRANSMITTED DATA (BA)
10	TRANSMITTED DATA (BA)
11	DATA TERMINAL READY (CD)
12	DATA TERMINAL READY (CD)
13	CARRIER DETECT (CF)
14	CARRIER DETECT (CF)
15	RINGING INDICATOR(CE)
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	2400 BAUD
36	COM
37	1200 BAUD
38	COM
39	600 BAUD
40	COM
41	300 BAUD
42	COM
43	200 BAUD
44	COM
45	150 BAUD
46	COM
47	110 BAUD
48	COM
49	
50	COM

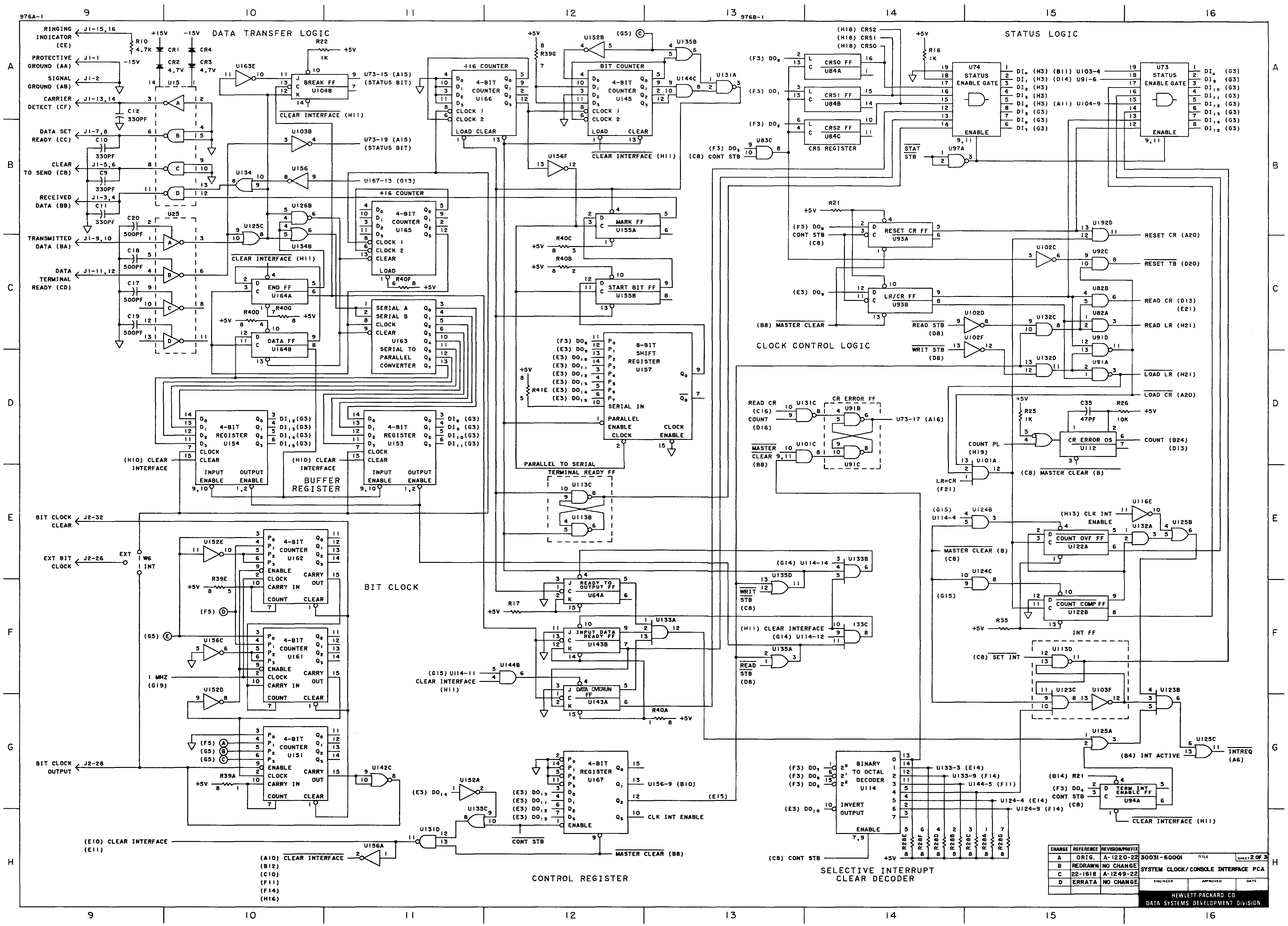
J2

PIN	SIGNAL
1	COM
2	EXT CLK
3	COM
4	CLK
5	COM
6	CLK
7	COM
8	10S
9	COM
10	1 S
11	COM
12	100 MS
13	COM
14	10 MS
15	COM
16	1 MS
17	COM
18	100 US
19	COM
20	10 US
21	COM
22	1 US
23	COM
24	COUNT PULSE
25	
26	EXT BIT CLOCK
27	
28	BIT CLOCK OUTPUT
29	
30	TEST
31	
32	BIT CLOCK CLEAR
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820	U	1820-
13,14	0751	53	0622	92	0141	115	0471	141	0371	163	0294
15	0609	54	0668	93,94	0512	116	0424	142	0239	164	0512
18	0755	58	0755	95	0077	117	0141	143	0629	165,166	0765
				96	0374	122	0077	144	0141	167	0626
23,24	0751	62	0668	97	0370	113	0372	145	0765		
25	0990	64	0629	99	0686	124	0141	146	0706		
28	0755	68	0755			125	0205	147	0760		
				101	0372	126	0370	149	0756		
32	0142	73,74	0755	102,103	0424	127	0760				
33,34	1715	75	0233	104	0629			151	0231		
35	0233	76	0719	105	0844	131	0370	152	0424		
36	0719	77	0742	106	0301	132	0141	153,154	0574		
37	0742			107	0491	133	0372	155	0512		
		82	0141	109	0760	134,135	0205	156	0424		
43,44	0751	85	0233			136	0706	157	0262		
45	0233	86	0719	112	0515	137	0760	159	0756		
46	0719			113	0370	139	0756				
		91	0370	114	0834			161,162	0231		




DATA TRANSFER LOGIC
STATUS LOGIC
CLOCK CONTROL LOGIC
BUFFER REGISTER
BIT CLOCK
PARALLEL TO SERIAL
TERMINAL READY FF
INT FF
CONTROL REGISTER
SELECTIVE INTERRUPT CLEAR DECODER
CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG. | A-1220-22
B | REDRAWN | NO CHANGE
C | 22-1618 | A-1249-22
D | ERRATA | NO CHANGE
30031-60001
SHEET 2 OF 3
SYSTEM CLOCK/CONSOLE INTERFACE PCA
ENGINEER
APPROVED
DATE
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARNING
6	
7	
8	
9	PWR ON
10	
11	I/O RESET
12	RESET COM
13	CLK
14	CLK COM
15	COM
16	COM
17	−5V
18	−5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	−15V
26	−15V
27	−15V
28	−15V
29	COM
30	COM
31	−20V
32	−20V
33	−20V
34	−20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSR SIG
42	SIG COM
43	COM
44	INTPOLL OUT
45	
46	
47	COM
48	INTPOLL IN
49	SI
50	COM
51	
52	
53	SO
54	COM
55	
56	

P2

PIN	SIGNAL
1	
2	COM
3	
4	COM
5	
6	COM
7	
8	COM
9	
10	COM
11	
12	
13	
14	COM
15	COM
16	
17	
18	
19	
20	COM
21	
22	
23	COM
24	
25	
26	
27	
28	
29	
30	COM
31	
32	
33	
34	
35	
36	COM
37	
38	
39	
40	
41	
42	COM
43	
44	
45	
46	
47	
48	
49	
50	

P3

PIN	SIGNAL
1	
2	
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	
46	COM
47	
48	
49	COM
50	INTACK

J1

PIN	SIGNAL
1	PROTECTIVE GROUND (AA)
2	SIGNAL GROUND (AB)
3	RECEIVED DATA (BB)
4	RECEIVED DATA (BB)
5	CLEAR TO SEND (CB)
6	CLEAR TO SEND (CB)
7	DATA SET READY (CC)
8	DATA SET READY (CC)
9	TRANSMITTED DATA (BA)
10	TRANSMITTED DATA (BA)
11	DATA TERMINAL READY (CD)
12	DATA TERMINAL READY (CD)
13	CARRIER DETECT (CF)
14	CARRIER DETECT (CF)
15	RINGING INDICATOR(CE)
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	2400 BAUD
36	COM
37	1200 BAUD
38	COM
39	600 BAUD
40	COM
41	300 BAUD
42	COM
43	200 BAUD
44	COM
45	150 BAUD
46	COM
47	110 BAUD
48	COM
49	
50	COM

J2

PIN	SIGNAL
1	COM
2	EXT CLK
3	COM
4	CLK
5	COM
6	CLK
7	COM
8	10S
9	COM
10	1 S
11	COM
12	100 MS
13	COM
14	10 MS
15	COM
16	1 MS
17	COM
18	100 US
19	COM
20	10 US
21	COM
22	1 US
23	COM
24	COUNT PULSE
25	
26	EXT BIT CLOCK
27	
28	BIT CLOCK OUTPUT
29	
30	TEST
31	
32	BIT CLOCK CLEAR
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820	U	1820-
13,14	0751	53	0622	92	0141	115	0471	141	0371	163	0294
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18	0755	58	0755	95	0077	117	0141	143	0629	165,166	0765
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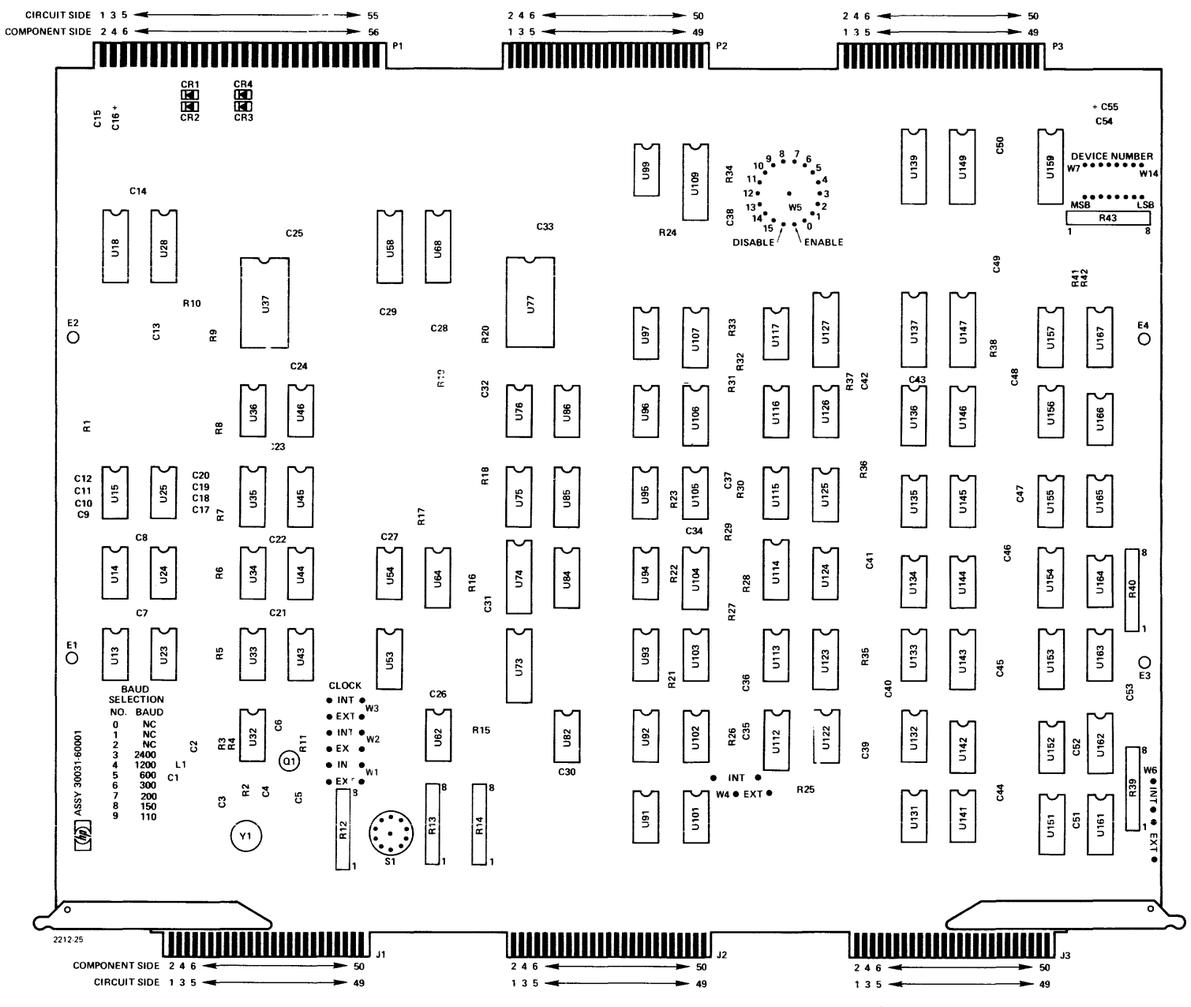
25	0990	64	0629	99	0686	124	0141	146	0706		
28	0755	68	0755			125	0205	147	0760		
				101	0372	126	0370	149	0756		
32	0142	73,74	0755	102,103	0424	127	0760				
33,34	1715	75	0233	104	0629			151	0231		
35	0233	76	0719	105	0844	131	0370	152	0424		
36	0719	77	0742	106	0301	132	0141	153,154	0574		
37	0742			107	0491	133	0372	155	0512		
		82	0141	109	0760	134,135	0205	156	0424		
43,44	0751	85	0233			136	0706	157	0262		
45	0233	86	0719	112	0515	137	0760	159	0756		
46	0719			113	0370	139	0756				
		91	0370	114	0834			161,162	0231		



977A-1 977B-1

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1220-22
B	REDRAWN	NO CHANGE
C	22-1618	A-1249-22
D	ERRATA	NO CHANGE

10 MHZ CLOCK

C5 2-8PF, C4 24PF, Y1 10MHZ, R3 316, R11 200, U62F, U32A, U32B, R2 46.4, R4 1K, C3 .01, L1 100UH, C6 2.2UF, C2 .01, C1 .01, +5V, R15 511, Q1

10MHZ INT, W1 EXT

U103C, U62E, R14F, J2-6 CLK

U82D, U54E, R13C, J2-4 CLK

J2-2 EXT CLK

CLOCK FREQUENCY DIVIDER

EXT | INT W2

+5V R5 1K

U43 4-BIT COUNTER (1US)

U33 4-BIT COUNTER (10US)

U23 4-BIT COUNTER (100US)

U13 4-BIT COUNTER (1MS)

RESET TB (C16)

EXT CLK | INT CLK W3

+5V R6 1K

U44 4-BIT COUNTER (10MS)

U34 4-BIT COUNTER (100MS)

U24 4-BIT COUNTER (1S)

U14 4-BIT COUNTER (10S)

COUNT RATE SELECTION LOGIC

+5V R14E R14D R14C R14B

U62D, U62A, U62B, U62C, U54D, U54C, U54B, U54A

J2-8 10 S, J2-10 1 S, J2-12 100 MS, J2-14 10 MS, J2-16 1 MS, J2-18 100 US, J2-20 10 US, J2-22 1 US

1 MHZ (F9)

+5V R14G 1K, R13D R13E R13F R13G

U53 8-TO-1 MULTIPLEXER, U54F

J2-24 COUNT PULSE

J2-1,3,5,7,9,11, 13,15,17,19,21,23

COUNT PL (D15)

J2-30 TEST

CRS0 (A14), CRS1 (A14), CRS2 (A14)

COUNT REGISTER

(D16) LOAD CR

(B16) RESET CR

U85 4-BIT UP/DOWN COUNTER, LOAD CLEAR, CLOCK UP CARRY, CLOCK DN BORROW

U75 4-BIT UP/DOWN COUNTER

U45 4-BIT UP/DOWN COUNTER

U35 4-BIT UP/DOWN COUNTER

+5V R18 1K

+5V R7 1K (D16) COUNT

CR0 (E21), CR1 (F21), CR2 (E21), CR3 (E21)

(E21) CR4, (F21) CR5, (E21) CR6, (E21) CR7

CR8 (E22), CR9 (F22), CR10 (E22), CR11 (E22)

(E23) CR12, (F23) CR13, (E23) CR14, (E23) CR15

U58 ENABLE, (H3) DI0 DI1 DI2 DI3, DI7 (G3) DI6 (G3) DI5 (G3) DI4 (H3)

U18 ENABLE, (G3) DI8 DI9 DI10 DI11, DI15 (G3) DI14 (G3) DI13 (G3) DI12 (G3)

(C16) READ CR

COUNT COMPARE LOGIC

U86, U76, U46, U36 4-BIT COMPARATOR A0=B0 A1=B1 A2=B2 A3=B3

(B21) CR2 (G22) LR2, (C21) CR3 (G22) LR3, (B21) CR0 (G22) LR0, (B21) CR1 (G22) LR1

(B22) CR4 (G22) LR4, (C22) CR7 (G22) LR7, (B22) CR6 (G22) LR6, (B22) CR5 (G22) LR5

(B23) CR10 (G24) LR10, (C23) CR11 (G24) LR11, (B23) CR8 (G24) LR8, (B23) CR9 (G24) LR9

(B24) CR14 (G24) LR14, (C24) CR13 (G24) LR13, (B24) CR12 (G24) LR12, (B24) CR15 (G24) LR15

(E14) LR=CR

+5V R8 1K

LIMIT REGISTER

U77 8-BIT REGISTER LIMIT REGISTER LR0-LR7

U37 8-BIT REGISTER LIMIT REGISTER LR8-LR15

(F3) DO0 (F3) DO1 (F3) DO2 (F3) DO3 (F3) DO4 (F3) DO5 (F3) DO6 (F3) DO7

(E3) DO12 (E3) DO13 (E3) DO14 (E3) DO15 (F3) DO8 (E3) DO9

LR4 (F21), LR5 (F21), LR7 (E21), LR6 (E21), LR2 (E21), LR3 (E21), LR0 (F21), LR1 (F21)

LR12 (F23), LR13 (F23), LR15 (E23), LR14 (E23), LR10 (E22), LR11 (E22), LR8 (F22), LR9 (F22)

R20 1K, R9 1K, CLEAR 0-3, CLEAR 4-7, LOAD 2,3,14,15

U68 ENABLE, (H3) DI0 DI1 DI2 DI3, DI7 (G3) DI6 (G3) DI5 (G3) DI4 (H3)

U28 ENABLE, (G3) DI8 DI9 DI10 DI11, DI15 (G3) DI14 (G3) DI13 (G3) DI12 (G3)

(D16) LOAD LR

(C16) READ LR

30031-60001	TITLE	SHEET 3 OF 3	
SYSTEM CLOCK/CONSOLE INTERFACE PCA			
ENGINEER	APPROVED	DATE	
HEWLETT-PACKARD CO			

I/O DETAILED DIAGRAM SET

DD-405

MULTIPLEXER CHANNEL PCA

30035-60001

SERIES 1210

1211

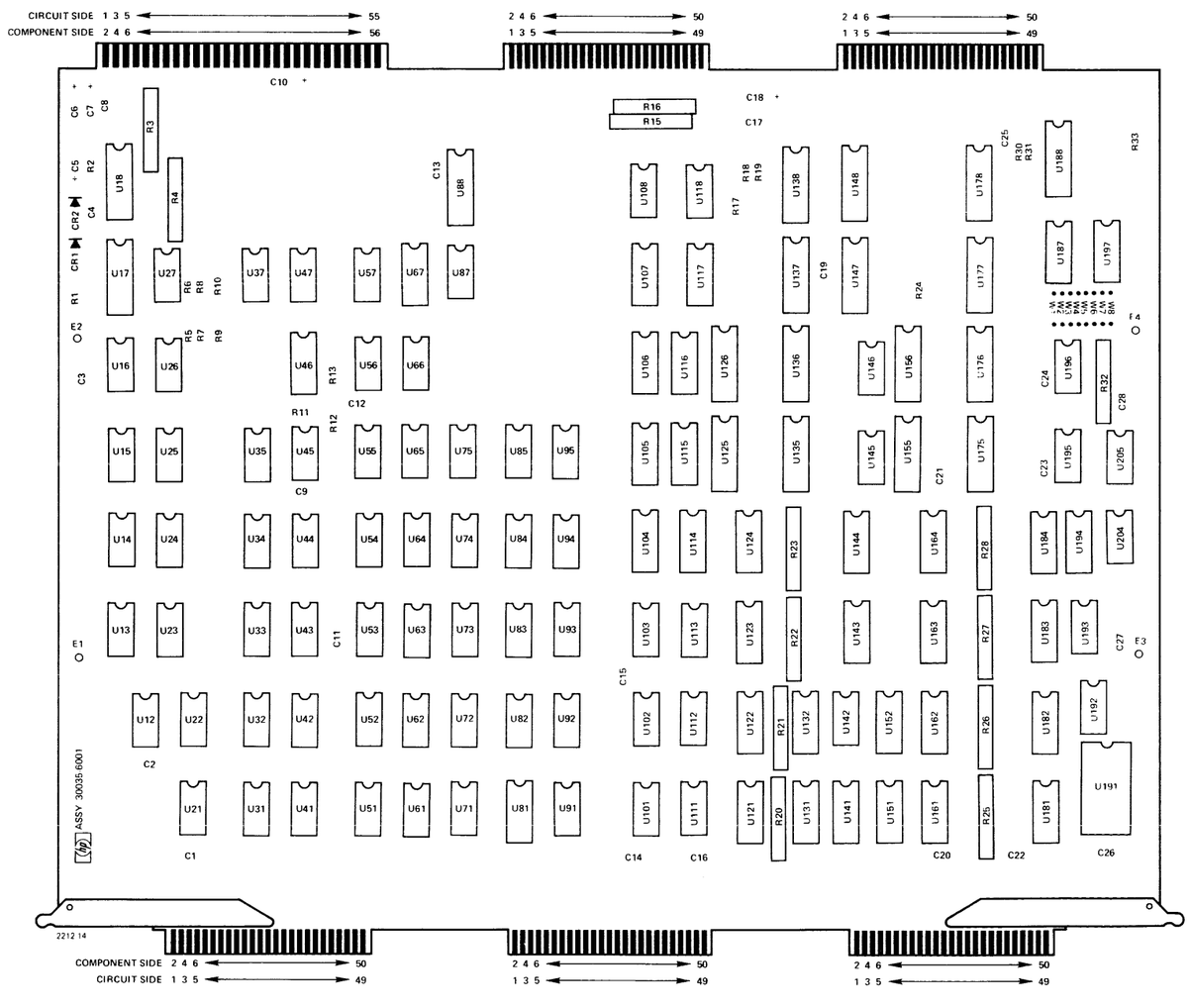
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY
2	+5V	2	COM	2	IOD PE
3	+5V	3	SR CLOCK	3	COM
4	+5V	4	COM	4	IOCMD 00
5	PF WARN	5	DEV END	5	IOCMD 02
6	ENTIMER	6	COM	6	IOCMD 01
7	(SPARE)	7	ACK SR	7	COM
8	(SPARE)	8	COM	8	DEVNO 00
9	PWR ON	9	CHAN ACK	9	DEVNO 01
10	COM	10	COM	10	COM
11	IORESET	11	DEVNO DB	11	DEVNO 02
12	COM	12	SIO ENABLE	12	DEVNO 03
13	MCUCLKS	13	EOT	13	COM
14	COM	14	JMP MET	14	DEVNO 04
15	COM	15	COM	15	DEVNO 05
16	COM	16	TOGGLE INXFER	16	COM
17	-5V	17	CHAN SR	17	DEVNO 06
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07
19	COM	19	TOGGLE SIO OK	19	COM
20	COM	20	COM	20	IOD 00
21	+15V	21	XFER ERROR	21	IOD 01
22	+15V	22	REQ	22	COM
23	+15V	23	COM	23	IOD 02
24	+15V	24	SR 15	24	IOD 03
25	-15V	25	SR 14	25	COM
26	-15V	26	SR 13	26	IOD 04
27	-15V	27	SR 12	27	IOD 05
28	-15V	28	SR 11	28	COM
29	COM	29	SR 10	29	IOD 06
30	COM	30	COM	30	IOD 07
31	-20V	31	SR 9	31	COM
32	-20V	32	SR 8	32	IOD 08
33	-20V	33	SR 7	33	IOD 09
34	-20V	34	SR 6	34	COM
35	+20V	35	SR 5	35	IOD 10
36	+20V	36	COM	36	IOD 11
37	+20V	37	SR 4	37	COM
38	+20V	38	SR 3	38	IOD 12
39	+20V	39	SR 2	39	IOD 13
40	+20V	40	SR 1	40	COM
41	HSREQ	41	SR 0	41	IOD 14
42	COM	42	COM	42	IOD 15
43	COM	43	P CMD 1	43	COM
44	INTPOLLOUT	44	SET JMP	44	INTREQ
45	(SPARE)	45	P STATUS STB	45	(SPARE)
46	COM	46	P CONT STB	46	COM
47	COM	47	RD NEXT WD	47	(SPARE)
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)
49	SI	49	SET INT	49	COM
50	COM	50	P READ STB	50	INTACK
51	COM				
52	DATAPOLL OUT				
53	SO				
54	COM				
55	COM				
56	DATAPOLL IN				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12	0205	35	0141	61	0376	91	0372	118	0655	161–164	0628
13	0377	37	0686	62	0141	92	0371				
14	0380			63	0370	93,94	0205	121–124	0628	175–178	0756
15	0370	41	0377	64	0693	95	0239	125,126	0759		
16	0681	42	0141	65	0141					181–184	0545
17,18	0755	43	0379	66	0371	101	0683	131	0626	187	0706
		44	0686	67	0214	102	0372	132	0233	188	0760
21	0379	45	0684			103	0376	135–138	0756		
22	0424	46	0301	71,72	0370	104	0657			191	0742
23	0205	47	0683	73	0377	105,106	0301	141	0626	192	0424
24	0377			74	0140	107	0491	142	0836	193	0371
25	0685	51	0377	75	0681	108	0655	143,144	0233	194	0628
26	0372	52	0693					145,146	0842	195,196	0842
27	0471	53	0686	81	0214	111	0141	147,148	0756	197	0706
		54	0685	82–84	0424	112	0370				
31	0377	55	0370	85	0681	113	0372	151	0628	204	0693
32	0371	56	0844	87	0424	114	0657	152	0788	205	0141
33	0141	57	0684	88	0760	115,116	0301	155,156	0759		
34	0379					117	0491				



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	ERRATA	NO CHANGE	ALL

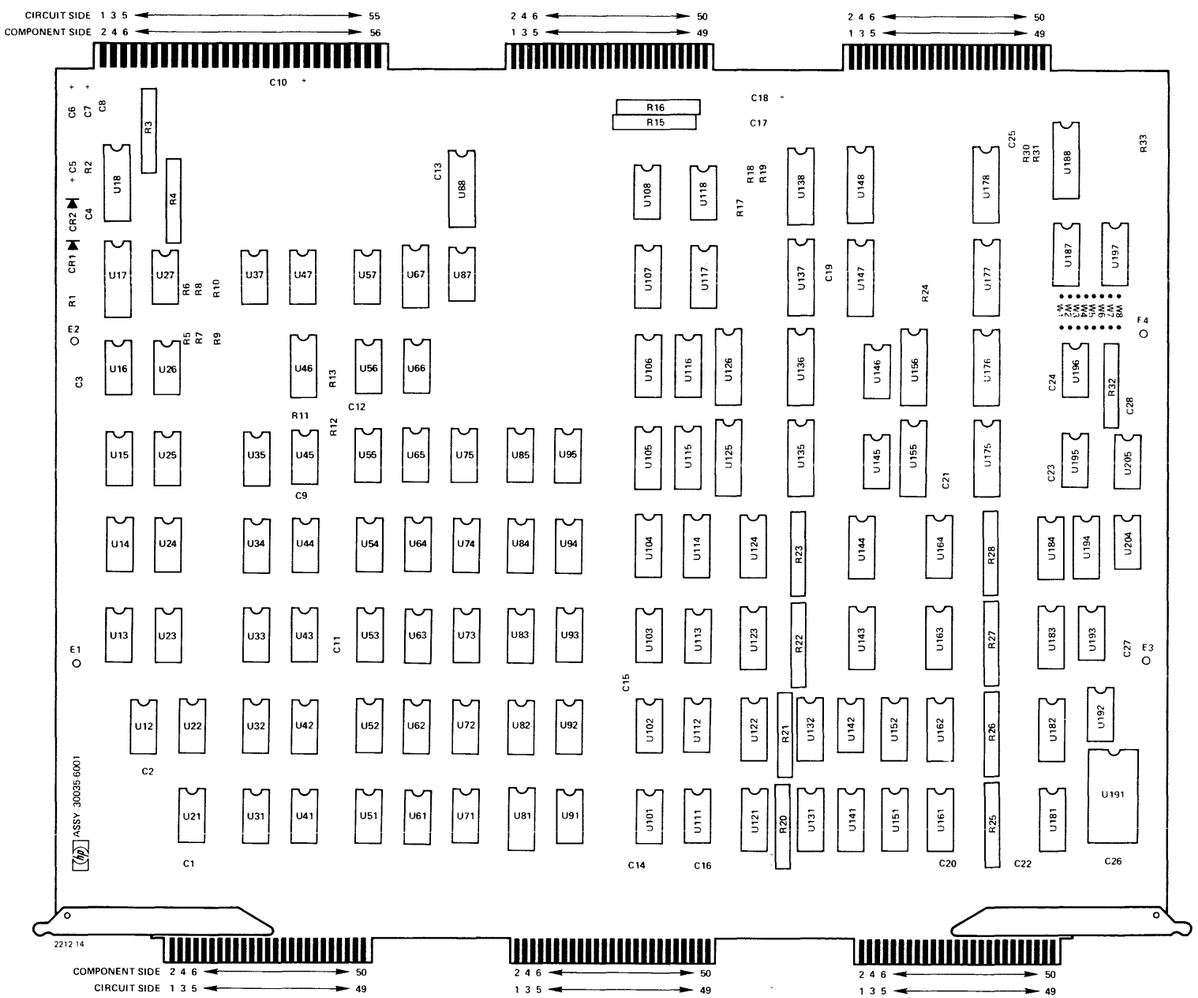
30035-60001	SHEET 1-3
MULTIPLEXER CHANNEL PCA	
ENGINEER	APPROVED / DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION	

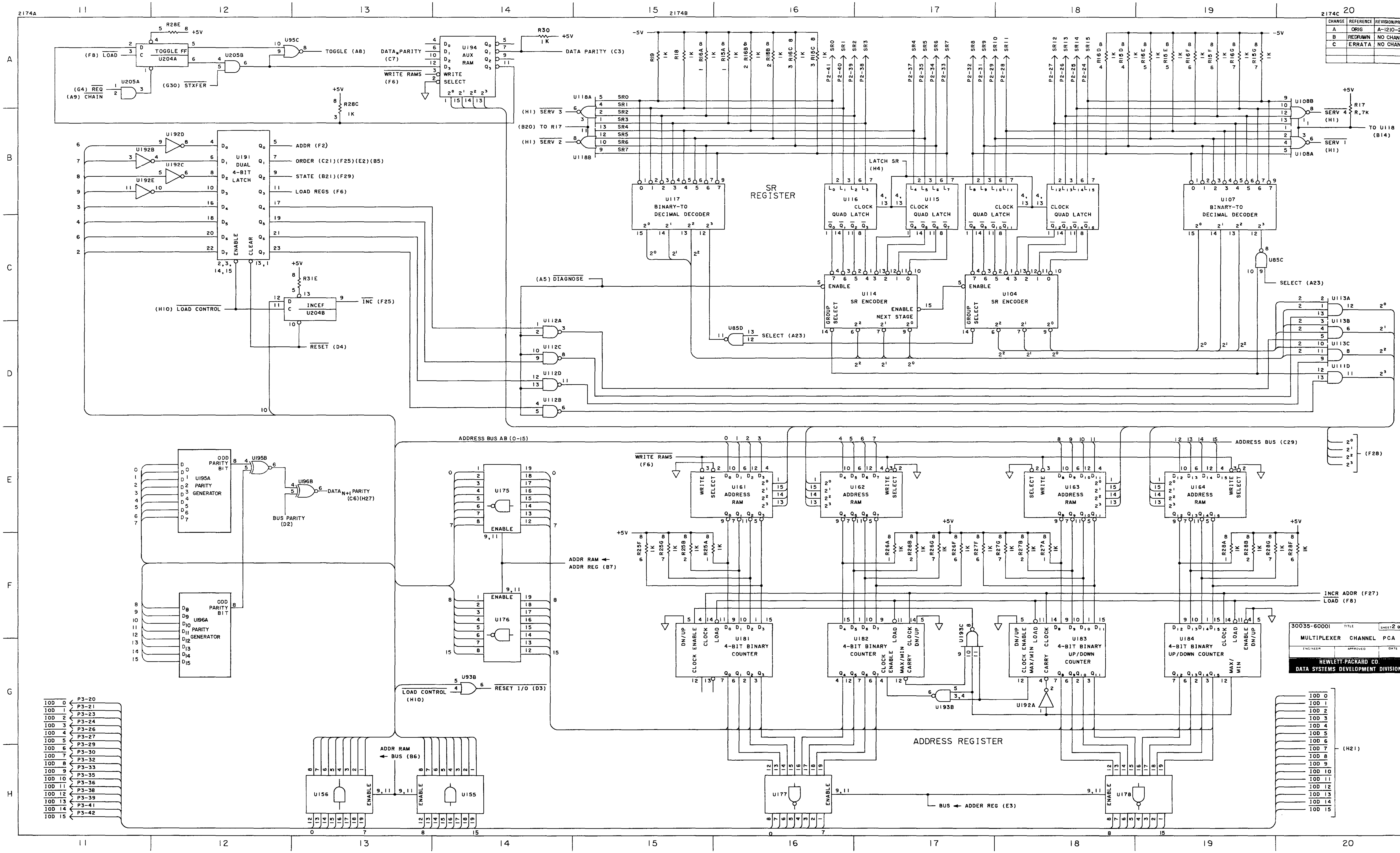
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY
2	+5V	2	COM	2	IOD PE
3	+5V	3	SR CLOCK	3	COM
4	+5V	4	COM	4	IOCMD 00
5	PF WARN	5	DEV END	5	IOCMD 02
6	ENTIMER	6	COM	6	IOCMD 01
7	(SPARE)	7	ACK SR	7	COM
8	(SPARE)	8	COM	8	DEVNO 00
9	PWR ON	9	CHAN ACK	9	DEVNO 01
10	COM	10	COM	10	COM
11	IORESET	11	DEVNO DB	11	DEVNO 02
12	COM	12	SIO ENABLE	12	DEVNO 03
13	MCUCLKS	13	EOT	13	COM
14	COM	14	JMP MET	14	DEVNO 04
15	COM	15	COM	15	DEVNO 05
16	COM	16	TOGGLE INXFER	16	COM
17	-5V	17	CHAN SR	17	DEVNO 06
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07
19	COM	19	TOGGLE SIO OK	19	COM
20	COM	20	COM	20	IOD 00
21	+15V	21	XFER ERROR	21	IOD 01
22	+15V	22	REQ	22	COM
23	+15V	23	COM	23	IOD 02
24	+15V	24	SR 15	24	IOD 03
25	-15V	25	SR 14	25	COM
26	-15V	26	SR 13	26	IOD 04
27	-15V	27	SR 12	27	IOD 05
28	-15V	28	SR 11	28	COM
29	COM	29	SR 10	29	IOD 06
30	COM	30	COM	30	IOD 07
31	-20V	31	SR 9	31	COM
32	-20V	32	SR 8	32	IOD 08
33	-20V	33	SR 7	33	IOD 09
34	-20V	34	SR 6	34	COM
35	+20V	35	SR 5	35	IOD 10
36	+20V	36	COM	36	IOD 11
37	+20V	37	SR 4	37	COM
38	+20V	38	SR 3	38	IOD 12
39	+20V	39	SR 2	39	IOD 13
40	+20V	40	SR 1	40	COM
41	HSREQ	41	SR 0	41	IOD 14
42	COM	42	COM	42	IOD 15
43	COM	43	P CMD 1	43	COM
44	INTPOLLOUT	44	SET JMP	44	INTREQ
45	(SPARE)	45	P STATUS STB	45	(SPARE)
46	COM	46	P CONT STB	46	COM
47	COM	47	RD NEXT WD	47	(SPARE)
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)
49	SI	49	SET INT	49	COM
50	COM	50	P READ STB	50	INTACK
51	COM				
52	DATAPOLL OUT				
53	SO				
54	COM				
55	COM				
56	DATAPOLL IN				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12	0205	35	0141	61	0376	91	0372	118	0655	161–164	0628
13	0377	37	0686	62	0141	92	0371				
14	0380			63	0370	93,94	0205	121–124	0628	175–178	0756
15	0370	41	0377	64	0693	95	0239	125,126	0759		
16	0681	42	0141	65	0141					181–184	0545
17,18	0755	43	0379	66	0371	101	0683	131	0626	187	0706
		44	0686	67	0214	102	0372	132	0233	188	0760
21	0379	45	0684			103	0376	135–138	0756		
22	0424	46	0301	71,72	0370	104	0657			191	0742
23	0205	47	0683	73	0377	105,106	0301	141	0626	192	0424
24	0377			74	0140	107	0491	142	0836	193	0371
25	0685	51	0377	75	0681	108	0655	143,144	0233	194	0628
26	0372	52	0693					145,146	0842	195,196	0842
27	0471	53	0686	81	0214	111	0141	147,148	0756	197	0706
		54	0685	82–84	0424	112	0370				
31	0377	55	0370	85	0681	113	0372	151	0628	204	0693
32	0371	56	0844	87	0424	114	0657	152	0788	205	0141
33	0141	57	0684	88	0760	115,116	0301	155,156	0759		
34	0379					117	0491				





SR REGISTER
U117 BINARY-TO DECIMAL DECODER
U116 CLOCK QUAD LATCH
U115 CLOCK QUAD LATCH
U107 BINARY-TO DECIMAL DECODER
U114 SR ENCODER
U104 SR ENCODER
U191 DUAL 4-BIT LATCH
U194 AUX RAM
TOGGLE FF U204A
INCEF U204B
U195A PARITY GENERATOR
U196A PARITY GENERATOR
U161 ADDRESS RAM
U162 ADDRESS RAM
U163 ADDRESS RAM
U164 ADDRESS RAM
U181 4-BIT BINARY COUNTER
U182 4-BIT BINARY COUNTER
U183 4-BIT BINARY UP/DOWN COUNTER
U184 4-BIT BINARY UP/DOWN COUNTER
ADDRESS REGISTER
ADDRESS BUS AB (0-15)
ADDRESS BUS (C29)
ADDR RAM ← BUS (B6)
BUS ← ADDER REG (E3)
ADDR RAM ← ADDR REG (B7)
INCR ADDR (F27)
LOAD (F8)
30035-60001
MULTIPLEXER CHANNEL PCA
SHEET 2 of 3
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION
A ORIG A-1210-22
B REDRAWN NO CHANGE
C ERRATA NO CHANGE

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY
2	+5V	2	COM	2	IOD PE
3	+5V	3	SR CLOCK	3	COM
4	+5V	4	COM	4	IOCMD 00
5	PF WARN	5	DEV END	5	IOCMD 02
6	ENTIMER	6	COM	6	IOCMD 01
7	(SPARE)	7	ACK SR	7	COM
8	(SPARE)	8	COM	8	DEVNO 00
9	PWR ON	9	CHAN ACK	9	DEVNO 01
10	COM	10	COM	10	COM
11	IORESET	11	DEVNO DB	11	DEVNO 02
12	COM	12	SIO ENABLE	12	DEVNO 03
13	MCUCLKS	13	EOT	13	COM
14	COM	14	JMP MET	14	DEVNO 04
15	COM	15	COM	15	DEVNO 05
16	COM	16	TOGGLE INXFER	16	COM
17	-5V	17	CHAN SR	17	DEVNO 06
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07
19	COM	19	TOGGLE SIO OK	19	COM
20	COM	20	COM	20	IOD 00
21	+15V	21	XFER ERROR	21	IOD 01
22	+15V	22	REQ	22	COM
23	+15V	23	COM	23	IOD 02
24	+15V	24	SR 15	24	IOD 03
25	-15V	25	SR 14	25	COM
26	-15V	26	SR 13	26	IOD 04
27	-15V	27	SR 12	27	IOD 05
28	-15V	28	SR 11	28	COM
29	COM	29	SR 10	29	IOD 06
30	COM	30	COM	30	IOD 07
31	-20V	31	SR 9	31	COM
32	-20V	32	SR 8	32	IOD 08
33	-20V	33	SR 7	33	IOD 09
34	-20V	34	SR 6	34	COM
35	+20V	35	SR 5	35	IOD 10
36	+20V	36	COM	36	IOD 11
37	+20V	37	SR 4	37	COM
38	+20V	38	SR 3	38	IOD 12
39	+20V	39	SR 2	39	IOD 13
40	+20V	40	SR 1	40	COM
41	HSREQ	41	SR 0	41	IOD 14
42	COM	42	COM	42	IOD 15
43	COM	43	P CMD 1	43	COM
44	INTPOLLOUT	44	SET JMP	44	INTREQ
45	(SPARE)	45	P STATUS STB	45	(SPARE)
46	COM	46	P CONT STB	46	COM
47	COM	47	RD NEXT WD	47	(SPARE)
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)
49	SI	49	SET INT	49	COM
50	COM	50	P READ STB	50	INTACK
51	COM				
52	DATAPOLL OUT				
53	SO				
54	COM				
55	COM				
56	DATAPOLL IN				

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
12	0205	35	0141	61	0376	91	0372	118	0655	161–164	0628
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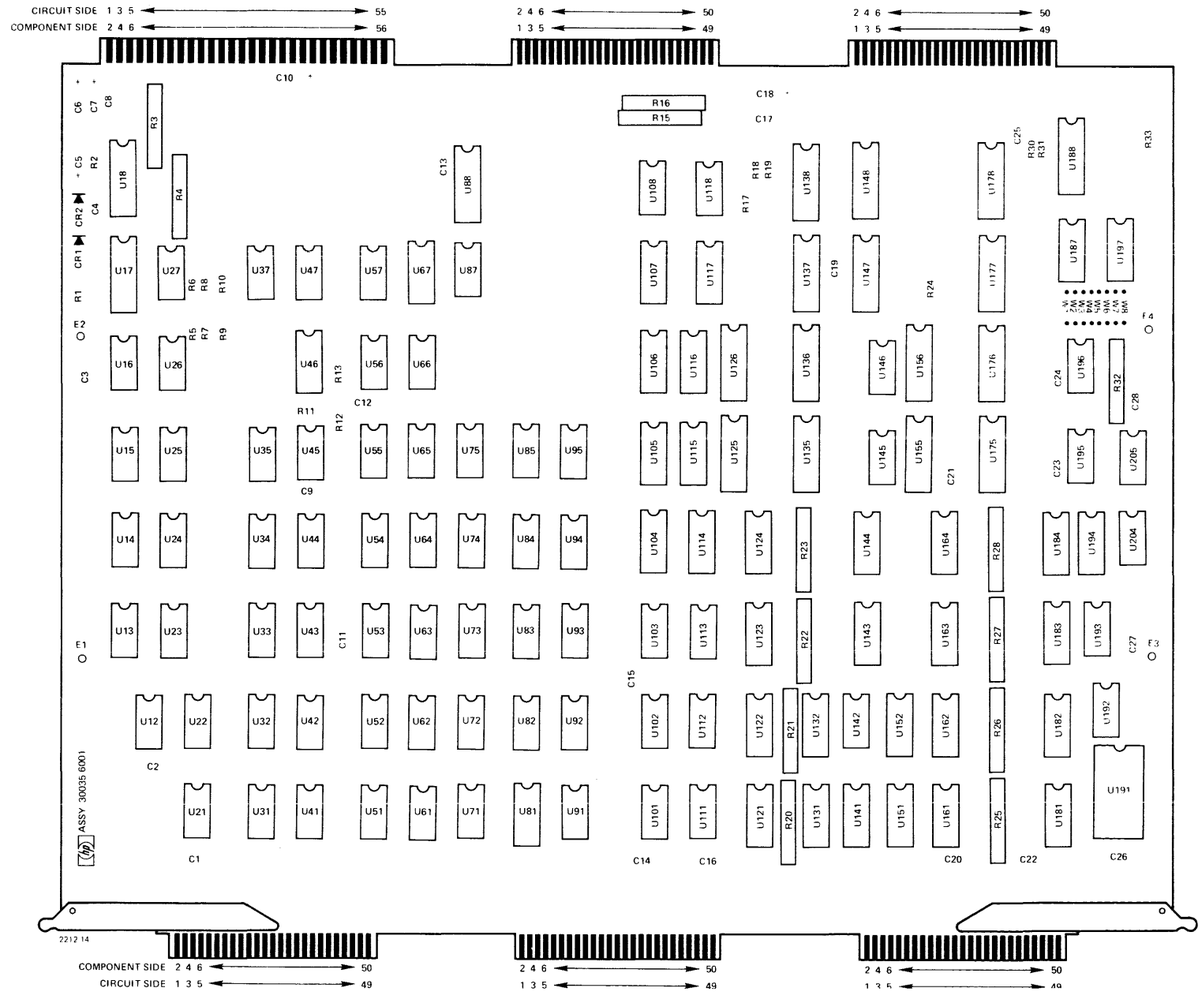
14	0380			63	0370	93,94	0205	121–124	0628	175–178	0756
15	0370	41	0377	64	0693	95	0239	125,126	0759		
16	0681	42	0141	65	0141					181–184	0545
17,18	0755	43	0379	66	0371	101	0683	131	0626	187	0706
		44	0686	67	0214	102	0372	132	0233	188	0760
21	0379	45	0684			103	0376	135–138	0756		
22	0424	46	0301	71,72	0370	104	0657			191	0742
23	0205	47	0683	73	0377	105,106	0301	141	0626	192	0424
24	0377			74	0140	107	0491	142	0836	193	0371
25	0685	51	0377	75	0681	108	0655	143,144	0233	194	0628
26	0372	52	0693					145,146	0842	195,196	0842
27	0471	53	0686	81	0214	111	0141	147,148	0756	197	0706
		54	0685	82–84	0424	112	0370				
31	0377	55	0370	85	0681	113	0372	151	0628	204	0693
32	0371	56	0844	87	0424	114	0657	152	0788	205	0141
33	0141	57	0684	88	0760	115,116	0301	155,156	0759		
34	0379					117	0491				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

(E5) READ — U62C — READ STATE (H26)

(B13) STATE — U83E — (A5) DIAGNOSE, (G4) CHAN SO — U54C — SELECT (D28)(C20)(D16)

(G4) REQ — U111C

U101B — U102A — RETURN RESIDUE

U101A — U44B — CONT (H8)(D8)(B8)

U93D — WRITE RAMS (F6)

ORDER BUS (0-15)

(F6) WRITE RAMS

U121 ORDER 64-BIT RAM

U122 ORDER 64-BIT RAM

U123 ORDER 64-BIT RAM

U124 ORDER 64-BIT RAM

U151 STATE 64-BIT RAM

+5V — R20E, R20D, R20C, R20B, R21A, R21B, R21C, R21F, R22A, R22B, R22G, R22F, R23A, R23B, R23C, R23F, R20G, R20F, R25C, R20A — 1K

(F28) A_N(B) — U51F

(B13) ORDER (D5) WRITE — U51A

U51E — U83C — ORDER RAM ← BUS (C8)

(F8) LOAD

U131 ORDER 4-BIT REGISTER

U132 ORDER REGISTER 4-BIT UP/DOWN COUNTER

U143 ORDER REGISTER 4-BIT UP/DOWN COUNTER

U144 ORDER REGISTER 4-BIT UP/DOWN COUNTER

U141 STATE 4-BIT REGISTER — SELECT (A23)

(E19) ADDRESS BUS

U101F, U101D, U101C, U101E

U22E — (F7)(A8)(B7) DC

R21E 1K — +5V

SET EOT (A8)

(F2)(E6) MSB

ORDER PARITY CHECKER

U145A PARITY GENERATOR — ODD PARITY BIT

U146A PARITY GENERATOR — ODD PARITY BIT — ORDER $_{NH}$ PARITY (C8) — BUS PARITY (D2)

U135, U136 — ENABLE

(B8) DC

(F7)(B7)(G29) O_4 (E5)

(B7)(B8)(F28) O_2 (G29) (D5)

(D5)(C4) O_1

(H6) U65-8 — (B6) DEV END FF — (E2) DEV END — U26C

(B13) ORDER — (C13) INC — (E5) READ — U42

(B13) ADDR

(F28) D_N(B) — (F28) A_N(B) — U93C

U51C, U51B, U41A, U51D, U41F, U41D — INC ADDR (F20)

(D8)(B8)(H9) A_N (E3) (E2)(E7)(B5) B_N (A6)(C5) (B5)(F2)(G8) C_N (F8)(F3) D_N

U35B, U111B, U33A, U111A — A_N(B), B_N(B), C_N(B), D_N(B)(D7) (F25)(A8)(B7)

(E20) — U22A — (H8) U47C-5

(A8) EOT — U32B — (E2) DEV END — U25A — (C5)(B8) (D)

(B7) DEV END FF — D_N(B) — A_N(B) (C21)(F25)

U32A — (D5) WRITE (B13) STATE — U628

(B7) DEV END FF — U32C

(F25) O_2 (D6) INT — U71D — U71C — (G4) REQ

U152 STATUS REGISTER — CLEAR CLOCK — RESET (D4)

U35A — (B) (G5)

B_N(B) — (G8)(B8)(D8)(E8)

C_N(B)(G9)(F7)

U23A — (D8) (C)

(F25) O_2 (E25) O_4 — U42D

U13A, U13E, U13F, U31B, U31D, U31C, U31A, U31E, U31F, U41B, U41D, U41C — A_{N+1}, B_{N+1}, C_{N+1}, D_{N+1}

U71B — STXFER (A12)

(H20) — 10D 00 … 10D 15

U126, U125, U137, U138 — ENABLE — BUS ORDER REG (E3)

(E5) GATE STATUS — U147 — R24 4.64K

U148 — EOT (A8) — DATA PARITY $_{W+1}$ (E11) — CONT PARITY (C8)

U1428 2-BIT A=B COMPARATOR

(A22) READ STATE

NEXT STATE LOGIC

30035-60001 TITLE — SHEET 3 of 3

MULTIPLEXER CHANNEL PCA

ENGINEER | APPROVED | DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

I/O DETAILED DIAGRAM SET

DD-501

UNIVERSAL INTERFACE (DIFFERENTIAL) PCA

30051-60001

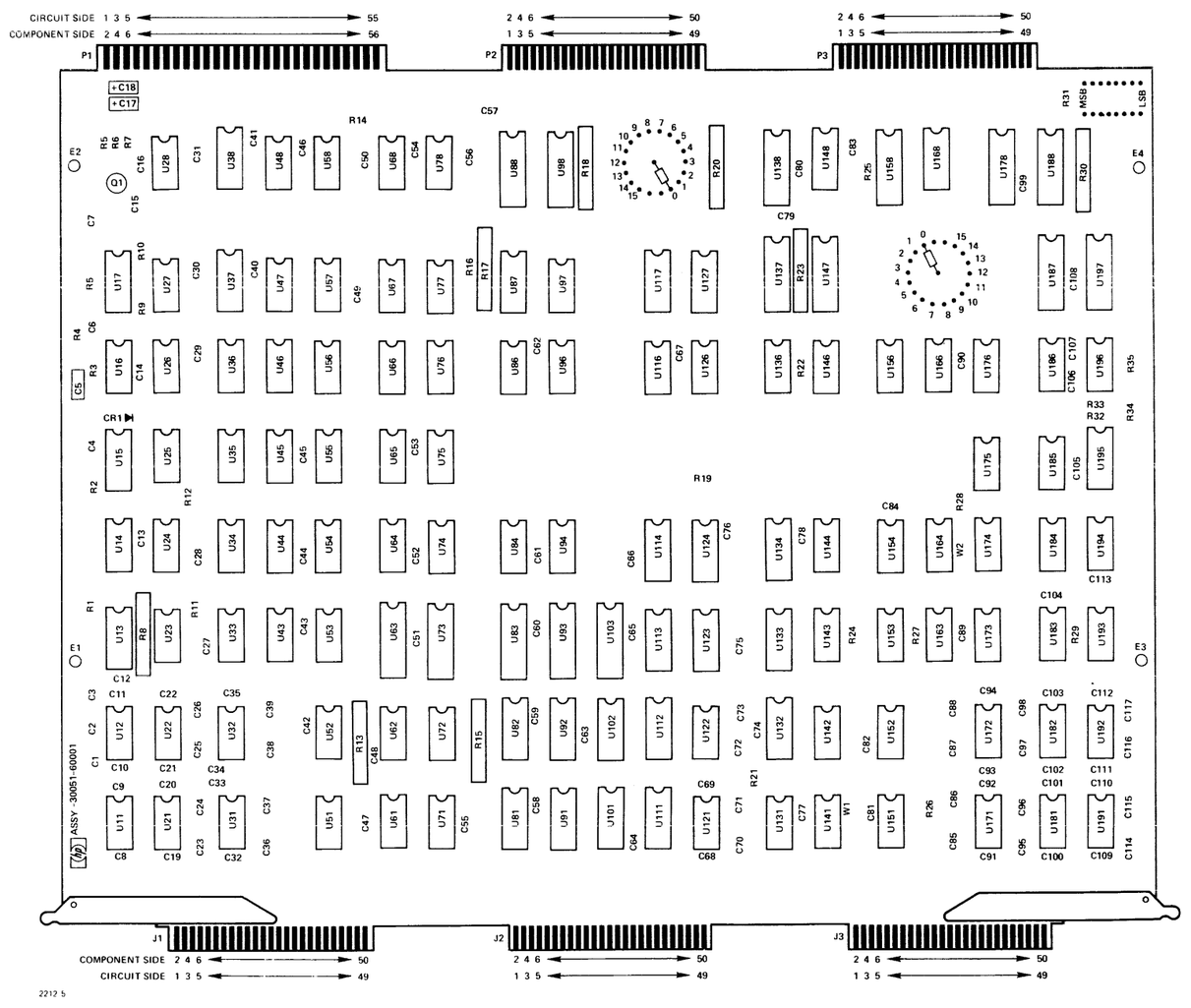
SERIES 1249

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1	BIT 8	1	POWER FAIL	1	BIT 2
2	+5V	2	COM	2	IOD PE	2	BIT 8	2	POWER FAIL	2	BIT 2
3	+5V	3	SR CLOCK	3	COM	3	DEV FLAG	3	PON	3	BIT 4
4	+5V	4	COM	4	IOCMD 00	4	DEV FLAG	4	RET	4	BIT 4
5	PF WARN	5	DEV END	5	IOCMD 02	5		5	CLEAR RELAY	5	BIT 6
6	ENTIMER	6	COM	6	IOCMD 01	6				6	BIT 6
7	(SPARE)	7	ACK SR	7	COM	7	SET TRANS ERROR FF	6	CLEAR RELAY	7	BIT 8
8	(SPARE)	8	COM	8	DEVNO 00	8				8	BIT 8
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	BIT 10	7	J2W1	9	BIT 7
10	COM	10	COM	10	COM	10	BIT 10	8	J2W1	10	BIT 7
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	BIT 9	9	J2W2	11	SELF TEST PWR
12	COM	12	SIO ENABLE	12	DEVNO 03	12	BIT 9	10	J2W2	12	SELF TEST PWR
13	MCUCLKS	13	EOT	13	COM	13	BIT 13	11	J2W3	13	SELF TEST PWR
14	COM	14	JMP MET	14	DEVNO 04	14	BIT 13	12	J2W3	14	SELF TEST PWR
15	COM	15	COM	15	DEVNO 05	15	BIT 12	13	J2W4		
16	COM	16	TOGGLE INXFER	16	COM	16	BIT 12	14	J2W4		
17	-5V			17	DEVNO 06	17	BIT 8	15	J2W5	15	BIT 1
18	-5V	17	TOGGLE SR	18	DEVNO 07	18	BIT 8	16	J2W5	16	BIT 1
19	COM	18	TOGGLE OUTXFER	19	COM	19	BIT 14	17		17	BIT 3
20	COM			20	IOD 00	20	BIT 14	18		18	BIT 3
21	+15V	19	TOGGLE SIO OK	21	IOD 01	21	BIT 15	19		19	BIT 7
22	+15V			22	COM	22	BIT 15	20		20	BIT 7
23	+15V	20	COM	23	IOD 02	23	BIT 12	21	J2W6	21	BIT 5
24	+15V	21	XFER ERROR	24	IOD 03	24	BIT 12	22	J2W6	22	BIT 5
25	-15V	22	REQ	25	COM	25	BIT 13	23		23	BIT 6
26	-15V	23	COM	26	IOD 04	26	BIT 13	24		24	BIT 6
27	-15V	24	SR 15	27	IOD 05	27	BIT 10	25	J2W11	25	BIT 0
28	-15V	25	SR 14	28	COM	28	BIT 10	26	J2W11	26	BIT 0
29	COM	26	SR 13	29	IOD 06	29	BIT 11	27		27	BIT 12
30	COM	27	SR 12	30	IOD 07	30	BIT 11	28		28	BIT 12
31	-20V	28	SR 11	31	COM	31	BIT 9	29		29	BIT 7
32	-20V	29	SR 10	32	IOD 08	32	BIT 9	30		30	BIT 7
33	-20V	30	COM	33	IOD 09	33	BIT 8	31		31	BIT 6
34	-20V	31	SR 9	34	COM	34	BIT 8	32		32	BIT 6
35	+20V	32	SR 8	35	IOD 10	35	SELF TEST LOGIC	33		33	BIT 4
36	+20V	33	SR 7	36	IOD 11			34		34	BIT 4
37	+20V	34	SR 6	37	COM	36		35	J2W8	35	BIT 5
38	+20V	35	SR 5	38	IOD 12	37	BIT 10	36	J2W8	36	BIT 5
39	+20V	36	COM	39	IOD 13	38	BIT 10	37	J2W9	37	BIT 14
40	+20V	37	SR 4	40	COM	39	DEV CMD	38	J2W9	38	BIT 14
41	HSREQ	38	SR 3	41	IOD 14	40	DEV CMD	39	J2W10	39	BIT 1
42	COM	39	SR 2	42	IOD 15	41	BIT 15	40	J2W10	40	BIT 1
43	COM	40	SR 1	43	COM	42	BIT 15	41	BIT 9	41	BIT 0
44	INTPOLLOUT	41	SR 0	44	INTREQ	43	BIT 14	42	BIT 9	42	BIT 0
45	(SPARE)	42	COM	45	(SPARE)	44	BIT 14	43	MASTER CLEAR	43	BIT 15
46	COM	43	P CMD 1	46	COM	45	BIT 9			44	BIT 15
47	COM	44	SET JMP	47	(SPARE)	46	BIT 9	44	MASTER CLEAR	45	BIT 3
48	INTPOLL IN	45	P STATUS STB	48	(SPARE)	47	BIT 10			46	BIT 3
49	SI	46	P CONT STB	49	COM	48	BIT 10	45	BIT 11	47	BIT 2
50	COM	47	RD NEXT WD	50	INTACK	49	BIT 11	46	BIT 11	48	BIT 2
51	COM	48	P WRITE STB			50	BIT 11	47	CLR INF	49	BIT 13
52	DATAPOLL OUT	49	SET INT					48	CLR INF	50	BIT 13
53	SO	50	P READ STB					49	DEV END		
54	COM							50	DEV END		
55	COM										
56	DATAPOLL IN										

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0721	51,52	0720	87	0491	138	0759	181,182	0721
13	0834	53	0512	88	0760			183	0373
14	0239	54	0141			141,142	0720	184	0512
15-17	0515	55	0512	91,92	0616	143,144	0512	185	0686
		56	0282	93	0756	146	0370	186	0512
21,22	0721	57	0141	94,96	0141	147	0760	187	0760
23	0512	58	0512	97	0374	148	0706	188	0756
24	0844			98	0759				
25	0512	61,62	0720			151,152	0720	191,192	0721
26	0205	63	0756	101,102	0626	153	0424	193	0512
27	0370	64	0371	103	0756	154	0377	194	0424
28	0141	65	0512			156	0371	195	0301
		66	0371	111,112	0616	158	0760	196	0844
31,32	0721	67	0377	113,114	0626			197	0755
33	0512	68	0141	116	0424	163	0370		
34	0424	71,72	0720	117	0715	164	0141		
35,36	0141	73	0756			166	0372		
37	0629	74,75	0141	121,122	0721	168	0706		
38	0574	76	0424	123,124	0626				
		77	0377	126	0900	171,172	0721		
43	0512	78	0512	127	0715	173	0141		
44	0375					174	0761		
45	0371	81,82	0626	131,132	0720	175	0141		
46	0370	83	0756	133,134	0626	176	0424		
47	0424	84	0424	136	0141	178	0756		
48	0141	86	0686	137	0755				



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CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO. CHANGE	ALL
C	PPC-A	A-1230-22	1
D	22-1625	A-1249-22	1
E	22-1630	B-1249-22	ALL
F	22-1693	B-1305-22	ALL

SERVICE REQUEST PRIORITY JUMPER

SR0 P2-41
SR1 P2-40
SR2 P2-39
SR3 P2-38
SR4 P2-37
SR5 P2-35
SR6 P2-34
SR7 P2-33
SR8 P2-32
SR9 P2-31
SR10 P2-29
SR11 P2-28
SR12 P2-27
SR13 P2-26
SR14 P2-25
SR15 P2-24

W5

+5V R19 23.7

U146D U174F U194B U185A U176C SR (B) FF U186B

(D39) P I/O RESET

U173C

IOCMD00 P3-4
IOCMD02 P3-5
ICOMD01 P3-6
TOGGLE SR P2-17
CHAN SO P2-1
SO P1-53
MCUCLK P1-13
I/O RESET P1-11

U88 ENABLE R18A

CLK (C22)

DEV END P2-5
JMP MET P2-14

(D25) DEV END

U98 ENABLE

TOGGLE SIO OK P2-19
TOGGLE OUTXFER P2-18
TOGGLE INXFER P2-16
EOT P2-13
DEVNO DB P2-11
ACK SR P2-7

U136 ENABLE

P READ STB P2-50
SET INT P2-49
RD NEXT WD P2-47
P WRITE STB P2-48
P STATUS STB P2-45
P CONT STB P2-46
P CMD 1 P2-43
SET JMP P2-44

COM P2-2,4,6,8,10,15,20,23,30,36,42

COM P3-7,10,13,16,19,22,25,26,31,34,37,40,43,46,49

+5V P1-1,2,3,4

COM P1-10,12,14,15,16,19,20,29,30,43,47,50,54

.01UF C17,18 2.2UF

TRUE COMPARE (D15) (B)

+5V R35 3.16K C107 75

U196A

XFER ERROR P2-21

U116F XFER ERROR (B28)

U156C U97A U166C U176D U146C

CHAN ACK P2-9

U174E U126B U116A

SI P1-49

U96D U194F (A) (C15)

U96C U86C U194A (H) (D15)

U96B

U176B

(D18) (E)

INT MASK FF U184B

R29 +5V

U176E U175A U194E

U116D U116E

U126C U126A DEVICE END BUFFER FF

R16 +5V

U87 BINARY TO DECIMAL DECODER

CLK XFER ERROR (B27)

TODDPRTY P3-1

+5V R28 1K W4

U164D U174C

(D30) INT REQ

U97B

U175B

U175C U164C

INT ACT FF U186A

U194F

INT LATCH FF U195B

U185B U174D

P1-44 INT POLL OUT

P3-44 INTREQ

D CONT STB (D37)
D WRIT STB (B34)
RESET INT (C30)
D STATUS STB (G32)

D READ STB (G45)
ACK 1 (B36)
ACK 2 (G32)
ACK 3 (E38)
ACK 4 (G45)

R17G R17F R17E R17D R17C R17B R17A R18B R18F +5V

INTPOLL IN P1-48

+5V R32 3.16K C106 75

U166B RESET STAT (F33)

U185C U196B U176F (G) (C13)

MASTER RESET (G32)

U166A U174A P3-50 INT ACK

INT ACTIVE (D29)

(F40) DEV SR U156B

EOT (F38)

R18B R18C R18D +5V

+5V R20G R20F R20E R20D R20C R20B R20A R23C R22

P READ STB (G45)(F37)
RD NEXT WD (B34)
P WRITE STB (B34)
P STATUS STB (G32)
P CONT STB (D37)(F37)
P CMD 1 (E38)(F38)

U146A U136B U146B SIO OK (E33) U156A

U116B

ENABLE SR FF U184A

CLR IL (B829)

+5V R18G

SIO ENABLE P2-12

SR FF U127A
SIO OK FF U127B
OUTXFER FF U117A
INXFER FF U117B
U116C

U136A SEL INT (C28)

U136D ACK SR (F38)(D24)

U136C

U194C U174B P2-22 REQ

(A24)(C23)(F38) OUTXFER OUTXFER

(A24)(C23) INXFER (E37) INXFER

4. ALL RESISTANCE VALUES ARE IN OHMS, 1/8W, ±1% FILM
3. ALL RESISTOR PACKS ARE 1K, 1810-0130
2. ALL DISCRETE RESISTORS ARE 1K
1. ALL CAPACITANCE VALUES ARE IN PICOFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

30051-60001	TITLE	SHEET 1 of 5
UNIVERSAL INTERFACE (DIFFERENTIAL) PCA		
ENGINEER	APPROVED	DATE
HEWLETT PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLLOUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	BIT 8
2	BIT 8
3	DEV FLAG
4	DEV FLAG
5	
6	
7	SET TRANS ERROR FF
8	
9	BIT 10
10	BIT 10
11	BIT 9
12	BIT 9
13	BIT 13
14	BIT 13
15	BIT 12
16	BIT 12
17	BIT 8
18	BIT 8
19	BIT 14
20	BIT 14
21	BIT 15
22	BIT 15
23	BIT 12
24	BIT 12
25	BIT 13
26	BIT 13
27	BIT 10
28	BIT 10
29	BIT 11
30	BIT 11
31	BIT 9
32	BIT 9
33	BIT 8
34	BIT 8
35	SELF TEST LOGIC
36	
37	BIT 10
38	BIT 10
39	DEV CMD
40	DEV CMD
41	BIT 15
42	BIT 15
43	BIT 14
44	BIT 14
45	BIT 9
46	BIT 9
47	BIT 10
48	BIT 10
49	BIT 11
50	BIT 11

J2

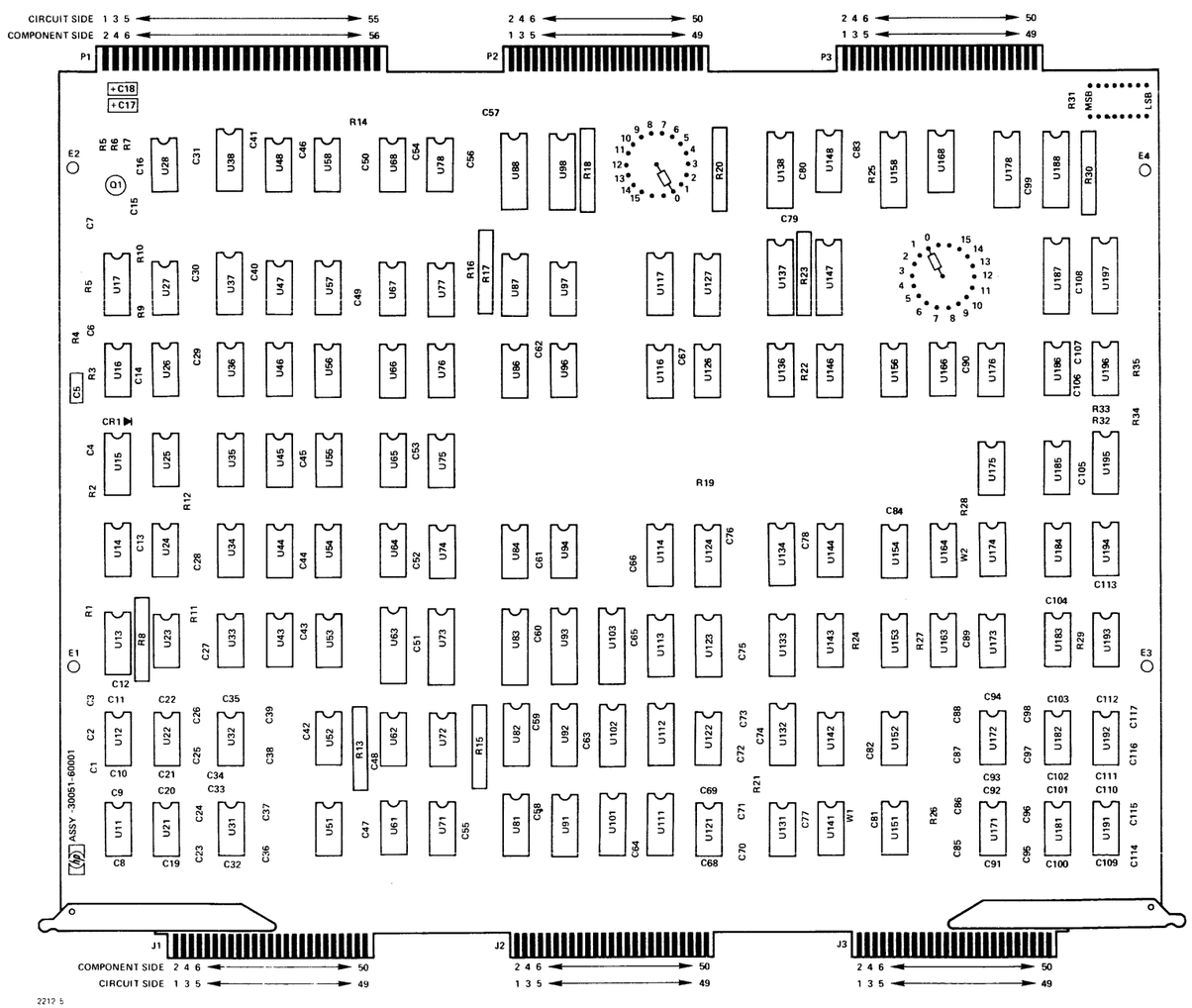
PIN	SIGNAL
1	POWER FAIL
2	POWER FAIL
3	PON
4	RET
5	CLEAR RELAY
6	CLEAR RELAY
7	J2W1
8	J2W1
9	J2W2
10	J2W2
11	J2W3
12	J2W3
13	J2W4
14	J2W4
15	J2W5
16	J2W5
17	
18	
19	
20	
21	J2W6
22	J2W6
23	
24	
25	J2W11
26	J2W11
27	
28	
29	
30	
31	
32	
33	
34	
35	J2W8
36	J2W8
37	J2W9
38	J2W9
39	J2W10
40	J2W10
41	BIT 9
42	BIT 9
43	MASTER CLEAR
44	MASTER CLEAR
45	BIT 11
46	BIT 11
47	CLR INF
48	CLR INF
49	DEV END
50	DEV END

J3

PIN	SIGNAL
1	BIT 2
2	BIT 2
3	BIT 4
4	BIT 4
5	BIT 6
6	BIT 6
7	BIT 8
8	BIT 8
9	BIT 7
10	BIT 7
11	SELF TEST PWR
12	SELF TEST PWR
13	SELF TEST PWR
14	SELF TEST PWR
15	BIT 1
16	BIT 1
17	BIT 3
18	BIT 3
19	BIT 7
20	BIT 7
21	BIT 5
22	BIT 5
23	BIT 6
24	BIT 6
25	BIT 0
26	BIT 0
27	BIT 12
28	BIT 12
29	BIT 7
30	BIT 7
31	BIT 6
32	BIT 6
33	BIT 4
34	BIT 4
35	BIT 5
36	BIT 5
37	BIT 14
38	BIT 14
39	BIT 1
40	BIT 1
41	BIT 0
42	BIT 0
43	BIT 15
44	BIT 15
45	BIT 3
46	BIT 3
47	BIT 2
48	BIT 2
49	BIT 13
50	BIT 13

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0721	51,52	0720	87	0491	138	0759	181,182	0721
13	0834	53	0512	88	0760			183	0373
14	0239	54	0141			141,142	0720	184	0512
15-17	0515	55	0512	91,92	0616	143,144	0512	185	0686
		56	0282	93	0756	146	0370	186	0512
21,22	0721	57	0141	94,96	0141	147	0760	187	0760
23	0512	58	0512	97	0374	148	0706	188	0756
24	0844			98	0759				
25	0512	61,62	0720			151,152	0720	191,192	0721
26	0205	63	0756	101,102	0626	153	0424	193	0512
27	0370	64	0371	103	0756	154	0377	194	0424
28	0141	65	0512			156	0371	195	0301
		66	0371	111,112	0616	158	0760	196	0844
31,32	0721	67	0377	113,114	0626			197	0755
33	0512	68	0141	116	0424	163	0370		
34	0424	71,72	0720	117	0715	164	0141		
35,36	0141	73	0756			166	0372		
37	0629	74,75	0141	121,122	0721	168	0706		
38	0574	76	0424	123,124	0626				
		77	0377	126	0900	171,172	0721		
43	0512	78	0512	127	0715	173	0141		
44	0375					174	0761		
45	0371	81,82	0626	131,132	0720	175	0141		
46	0370	83	0756	133,134	0626	176	0424		
47	0424	84	0424	136	0141	178	0756		
48	0141	86	0686	137	0755				



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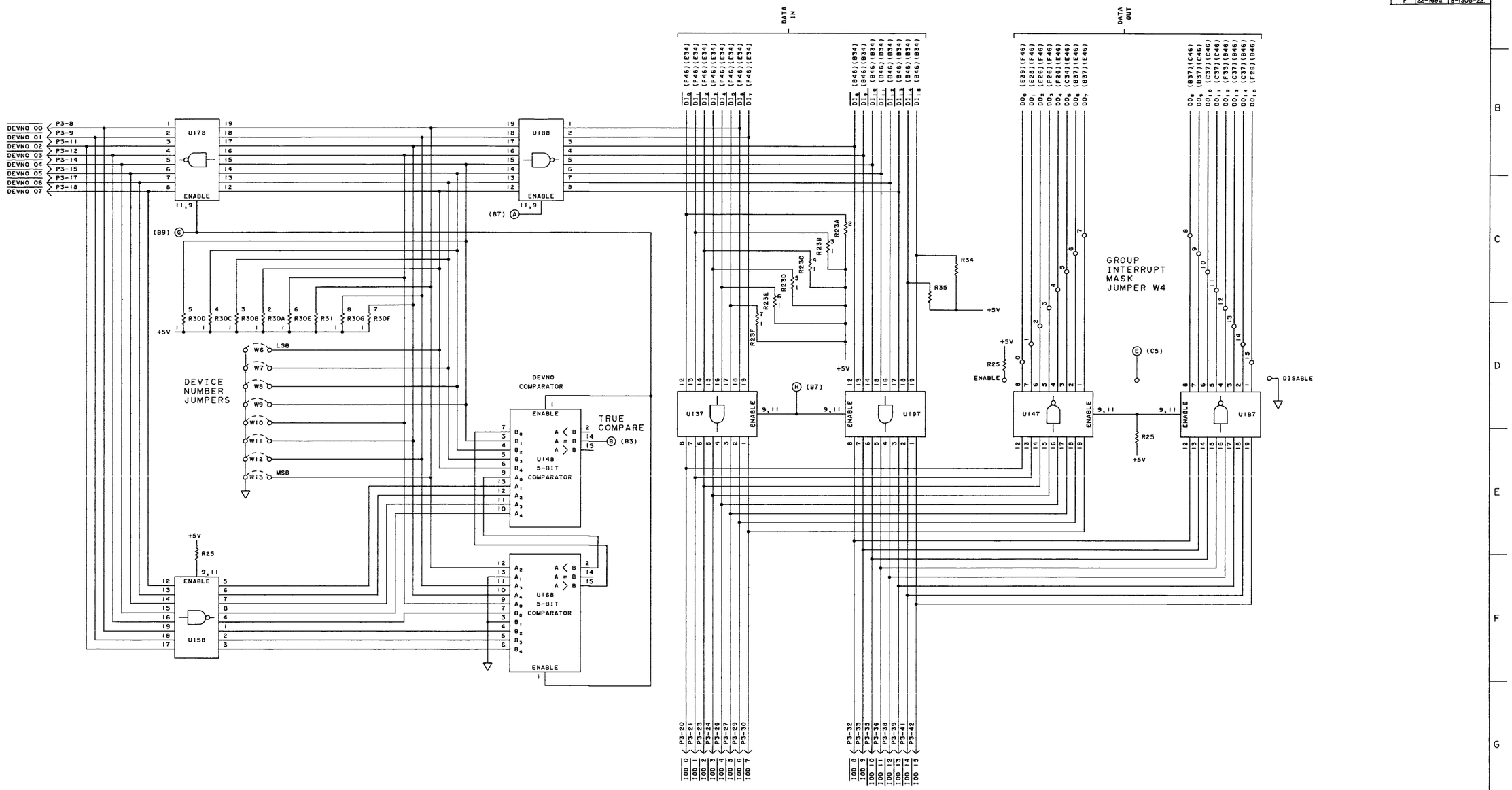
CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1230-22
D	22-1625	A-1249-22
E	22-1630	B-1249-22
F	22-1693	B-1305-22.



30051-60001	TITLE	SHEET 2 OF 5
UNIVERSAL INTERFACE (DIFFERENTIAL) PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLLOUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLLIN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	BIT 8
2	BIT 8
3	DEV FLAG
4	DEV FLAG
5	
6	
7	SET TRANS ERROR FF
8	
9	BIT 10
10	BIT 10
11	BIT 9
12	BIT 9
13	BIT 13
14	BIT 13
15	BIT 12
16	BIT 12
17	BIT 8
18	BIT 8
19	BIT 14
20	BIT 14
21	BIT 15
22	BIT 15
23	BIT 12
24	BIT 12
25	BIT 13
26	BIT 13
27	BIT 10
28	BIT 10
29	BIT 11
30	BIT 11
31	BIT 9
32	BIT 9
33	BIT 8
34	BIT 8
35	SELF TEST LOGIC
36	
37	BIT 10
38	BIT 10
39	DEV CMD
40	DEV CMD
41	BIT 15
42	BIT 15
43	BIT 14
44	BIT 14
45	BIT 9
46	BIT 9
47	BIT 10
48	BIT 10
49	BIT 11
50	BIT 11

J2

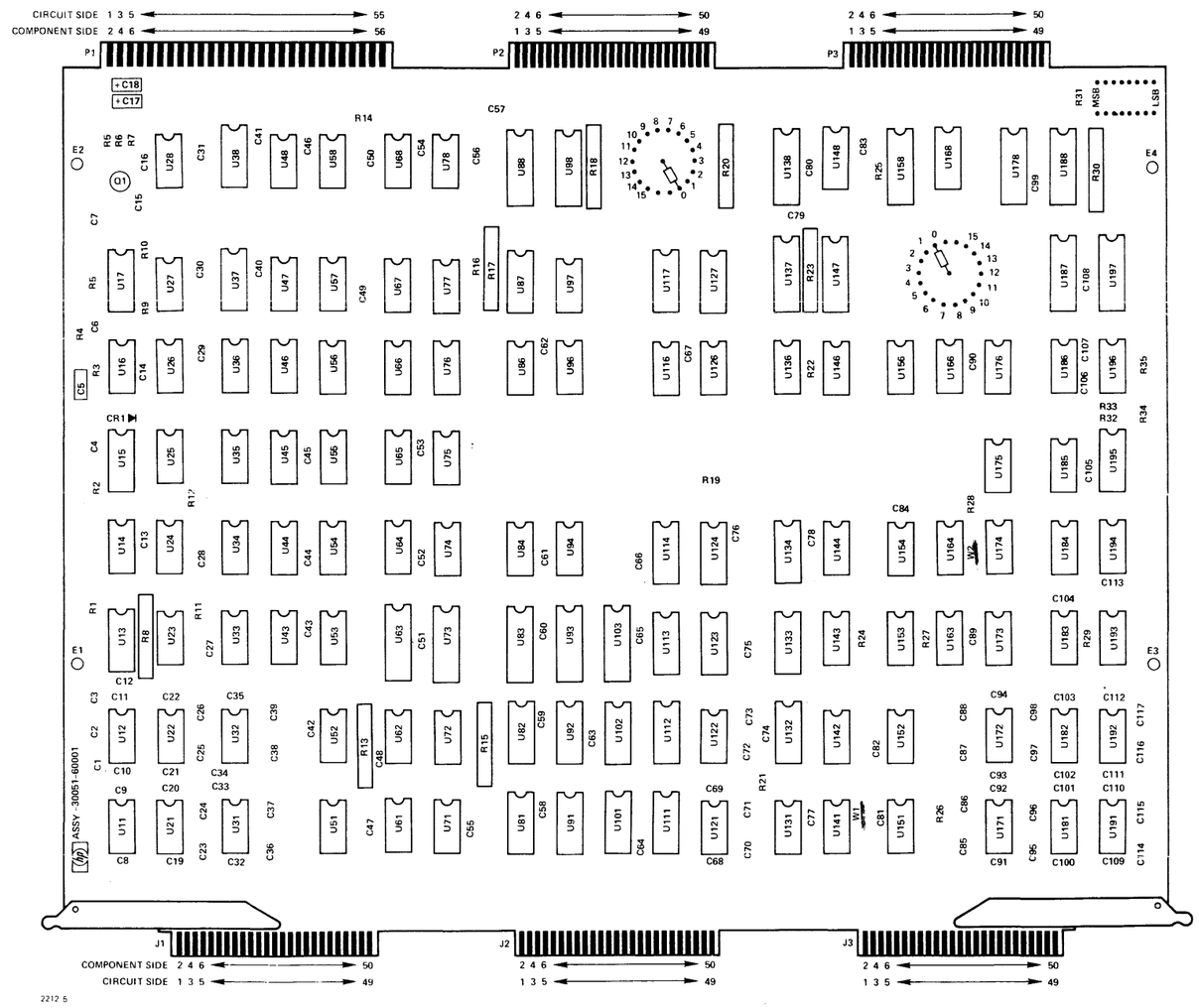
PIN	SIGNAL
1	POWER FAIL
2	POWER FAIL
3	PON
4	RET
5	CLEAR RELAY
6	CLEAR RELAY
7	J2W1
8	J2W1
9	J2W2
10	J2W2
11	J2W3
12	J2W3
13	J2W4
14	J2W4
15	J2W5
16	J2W5
17	
18	
19	
20	
21	J2W6
22	J2W6
23	
24	
25	J2W11
26	J2W11
27	
28	
29	
30	
31	
32	
33	
34	
35	J2W8
36	J2W8
37	J2W9
38	J2W9
39	J2W10
40	J2W10
41	BIT 9
42	BIT 9
43	MASTER CLEAR
44	MASTER CLEAR
45	BIT 11
46	BIT 11
47	CLR INF
48	CLR INF
49	DEV END
50	DEV END

J3

PIN	SIGNAL
1	BIT 2
2	BIT 2
3	BIT 4
4	BIT 4
5	BIT 6
6	BIT 6
7	BIT 8
8	BIT 8
9	BIT 7
10	BIT 7
11	SELF TEST PWR
12	SELF TEST PWR
13	SELF TEST PWR
14	SELF TEST PWR
15	BIT 1
16	BIT 1
17	BIT 3
18	BIT 3
19	BIT 7
20	BIT 7
21	BIT 5
22	BIT 5
23	BIT 6
24	BIT 6
25	BIT 0
26	BIT 0
27	BIT 12
28	BIT 12
29	BIT 7
30	BIT 7
31	BIT 6
32	BIT 6
33	BIT 4
34	BIT 4
35	BIT 5
36	BIT 5
37	BIT 14
38	BIT 14
39	BIT 1
40	BIT 1
41	BIT 0
42	BIT 0
43	BIT 15
44	BIT 15
45	BIT 3
46	BIT 3
47	BIT 2
48	BIT 2
49	BIT 13
50	BIT 13

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0721	51,52	0720	87	0491	138	0759	181,182	0721
13	0834	53	0512	88	0760			183	0373
14	0239	54	0141			141,142	0720	184	0512
15-17	0515	55	0512	91,92	0616	143,144	0512	185	0686
		56	0282	93	0756	146	0370	186	0512
21,22	0721	57	0141	94,96	0141	147	0760	187	0760
23	0512	58	0512	97	0374	148	0706	188	0756
24	0844			98	0759				
25	0512	61,62	0720			151,152	0720	191,192	0721
26	0205	63	0756	101,102	0626	153	0424	193	0512
27	0370	64	0371	103	0756	154	0377	194	0424
28	0141	65	0512			156	0371	195	0301
		66	0371	111,112	0616	158	0760	196	0844
31,32	0721	67	0377	113,114	0626			197	0755
33	0512	68	0141	116	0424	163	0370		
34	0424	71,72	0720	117	0715	164	0141		
35,36	0141	73	0756			166	0372		
37	0629	74,75	0141	121,122	0721	168	0706		
38	0574	76	0424	123,124	0626				
		77	0377	126	0900	171,172	0721		
43	0512	78	0512	127	0715	173	0141		
44	0375					174	0761		
45	0371	81,82	0626	131,132	0720	175	0141		
46	0370	83	0756	133,134	0626	176	0424		
47	0424	84	0424	136	0141	178	0756		
48	0141	86	0686	137	0755				



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CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1230-22
D	22-1625	A-1249-22
E	22-1630	B-1249-22
F	22-1693	B-1305-22

SEQUENCE COUNTER

DEVICE END LOGIC

DEVICE FLAG EDGE DETECTOR LOGIC

INTERRUPT LOGIC

30051-60001	TITLE
UNIVERSAL INTERFACE (DIFFERENTIAL) PCA	SHEET 3 OF 5
ENGINEER / APPROVED / DATE	
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION	

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLLOUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	BIT 8
2	BIT 8
3	DEV FLAG
4	DEV FLAG
5	
6	
7	SET TRANS ERROR FF
8	
9	BIT 10
10	BIT 10
11	BIT 9
12	BIT 9
13	BIT 13
14	BIT 13
15	BIT 12
16	BIT 12
17	BIT 8
18	BIT 8
19	BIT 14
20	BIT 14
21	BIT 15
22	BIT 15
23	BIT 12
24	BIT 12
25	BIT 13
26	BIT 13
27	BIT 10
28	BIT 10
29	BIT 11
30	BIT 11
31	BIT 9
32	BIT 9
33	BIT 8
34	BIT 8
35	SELF TEST LOGIC
36	
37	BIT 10
38	BIT 10
39	DEV CMD
40	DEV CMD
41	BIT 15
42	BIT 15
43	BIT 14
44	BIT 14
45	BIT 9
46	BIT 9
47	BIT 10
48	BIT 10
49	BIT 11
50	BIT 11

J2

PIN	SIGNAL
1	POWER FAIL
2	POWER FAIL
3	PON
4	RET
5	CLEAR RELAY
6	CLEAR RELAY
7	J2W1
8	J2W1
9	J2W2
10	J2W2
11	J2W3
12	J2W3
13	J2W4
14	J2W4
15	J2W5
16	J2W5
17	
18	
19	
20	
21	J2W6
22	J2W6
23	
24	
25	J2W11
26	J2W11
27	
28	
29	
30	
31	
32	
33	
34	
35	J2W8
36	J2W8
37	J2W9
38	J2W9
39	J2W10
40	J2W10
41	BIT 9
42	BIT 9
43	MASTER CLEAR
44	MASTER CLEAR
45	BIT 11
46	BIT 11
47	CLR INF
48	CLR INF
49	DEV END
50	DEV END

J3

PIN	SIGNAL
1	BIT 2
2	BIT 2
3	BIT 4
4	BIT 4
5	BIT 6
6	BIT 6
7	BIT 8
8	BIT 8
9	BIT 7
10	BIT 7
11	SELF TEST PWR
12	SELF TEST PWR
13	SELF TEST PWR
14	SELF TEST PWR
15	BIT 1
16	BIT 1
17	BIT 3
18	BIT 3
19	BIT 7
20	BIT 7
21	BIT 5
22	BIT 5
23	BIT 6
24	BIT 6
25	BIT 0
26	BIT 0
27	BIT 12
28	BIT 12
29	BIT 7
30	BIT 7
31	BIT 6
32	BIT 6
33	BIT 4
34	BIT 4
35	BIT 5
36	BIT 5
37	BIT 14
38	BIT 14
39	BIT 1
40	BIT 1
41	BIT 0
42	BIT 0
43	BIT 15
44	BIT 15
45	BIT 3
46	BIT 3
47	BIT 2
48	BIT 2
49	BIT 13
50	BIT 13

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0721	51,52	0720	87	0491	138	0759	181,182	0721
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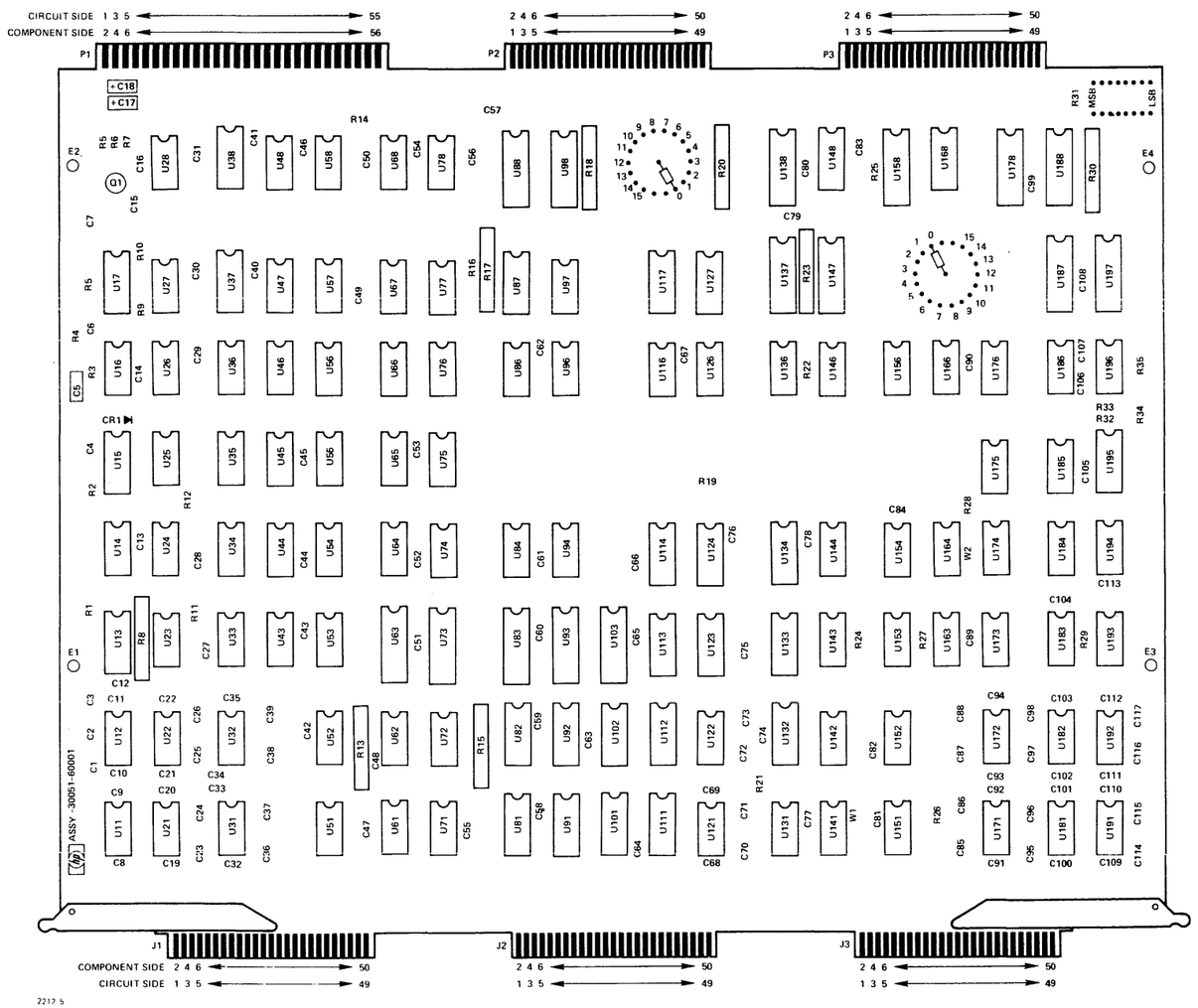


CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1230-22
D	22-1625	A-1249-22
E	22-1630	B-1249-22
F	22-1693	B-1305-22

STATUS FROM DEVICE

BIT 15 J3-44 J3-43 C102 2000 U182B C97 100
BIT 14 J3-38 J3-37 C103 2000 U182A C98 100
BIT 13 J3-50 J3-49 C111 2000 U192B C116 100
BIT 12 J3-28 J3-27 C112 2000 U192A C117 100
BIT 11 J2-46 J2-45 C69 2000 U121A C71 100
BIT 10 J1-10 J1-9 C1 2000 U11A C10 100
BIT 9 J1-12 J1-11 C17 2000 U11B C9 100
BIT 8 J1-2 J1-1 C11 2000 U12A C3 100

(K) (F42)
(C) (C21)
(D) (D42)

B STAT 11 (G38)
B STAT 10 (F28)
B STAT 9 (G28)
B STAT 8 (F28)

R15G +5V

STATUS LOGIC

INTERRUPT

(B29) TIME OUT
(B28) TRANS ERR
(C28) I/O SYS
(D28) CLR INF
(E28) DATA TRANS
(F28) STAT 10
(G28) STAT 9
(F28) STAT 8

U63 ENABLE 9,11 → DI15 DI14 DI13 DI12 DI11 DI10 DI9 DI8 (B17)

DEVICE

U73 ENABLE 9 → DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0

INTERFACE

U93 ENABLE 9,11 → DI7 DI6 DI5 DI4 DI3 DI2 DI1 DI0 (B16)

(E22) DEV FLAG
(B25) SEQ 2
(B25) SEQ 1
(E29) INT PEND
(F8) SIO OK → U84D → U75B

(F26)
(B19) DO12 (D38) LOAD CMD → D C INT/DEV STAT FF U65A

(C35) → D C RIO/WIO OK FF U58B
MR2 (G33)
(D25) OP DONE → U86A 1,2,13 12 → U86B 3,4,5 6 → 11
(F23) COUNT

(B8) RESET STAT → U84A
(D8) D STATUS STB
(F9) P STATUS STB → U75D → ACK 2 (D9)

(B8) MASTER RESET
U94C → MR1 (C37) (D44) (G46)
U36B → MR2 (B35) (E34) (C22) (D26) (F32)
U36C → MR3 (B21) (D24) (G26) (C29)

(F9) P WRITE STB
(C8) D WRITE STB → U68B → ACK 1 (D9)

LD WRT BUF (G46)

(D25) OP DONE → D C WRT XFER FF U78A
(G33) MR2
(F9) RD NEXT WD → U68C
(D38) LOAD CMD
(B18) DO9 → U27D → D C RD XFER FF U78B

(F32) → R14 +5V → D C QO FF U58A → QO (C21)
U68D U68A
(C25) COUNT 0

BYTE TRANS (C38)

U57A BYTE WRITE (G47) U77C U77D U77B → WRT DELAY OS U17A
J1-6 R5 +5V 10K WRITE DELAY CAP J1-5 C7 47

U27A R9 51.1 C14 470 U46B U46C → B DEV CMD (F34)(A26)

U67C U67D U67B
U57B
(B25) COUNT 1
(C25) COUNT 3

R10 23.7K +5V
C15 1000
R13G +5V → CMD PULSE OS U17B

(G33) MR2
EXT DEV END (D24) → U57C U57D
B DEV CMD (E37)

U67A U67E U67F U76A
R15B +5V

DEVICE COMMAND LOGIC

R13B +5V → U56D U51B

J2-11 J2-12 → J2W3
J2-39 J2-40 → J2W10
J1-40 J1-39 → DEV CMD

U133 4-BIT REGISTER ENABLE CLEAR
(B18) DO4
(B18) DO7
(B19) DO8
(B19) DO6

U134 4-BIT REGISTER ENABLE CLEAR
(B19) DO11
(B19) DO14
(B19) DO13
(B19) DO10

(G32) MRI

CW DATA INT (E28)
(NOT USED)
BYTE TRANS (D34) (F22) (G46)

U1328 → J3-5 J3-6 BIT 6
U1418 → J3-9 J3-10 BIT 7
U141A → J3-7 J3-8 BIT 8
U132A → J2-41 J2-40 BIT 9
U51A → J1-37 J1-38 BIT 10

CONTROL WORD TO DEVICE

CONTROL LOGIC

LOAD CMD
(F9) P CONT STB
(C8) D CONT STB → U173A → U153D → LOAD CMD (C29)(C35)(D25)(F35)
(B18) DO0 → U163C → P I/O RESET (C2)
(F9) P CMD I → U173B → ACK 3 (D9)

(C25) DEV END ON I
(F6) INXFER → U154C U154D U153B
U154B
(D25) OP DONE
R24 +5V → D C DATA SR FF U143B

EOT (E7) → U153A
(E9) P READ STB → U153C
(G5) OUTXFER → U163B
(G6) ACK SR → U163A
OUT XFER BUF → OUTXFER (G5)

D C EOT SR U143A
D C XFER SR FF U144A
D C CMD SR FF U144B

U183B U84C → DEV SR (E8)

(F9) P CONT STB → U153E
U163D
(F9) P CMD I → U164B
U153F
(D32) B STAT 11 → U164A
R27 +5V

J2-7 J2-8 → J2W1

DEVICE SR LOGIC

30051-60001	TITLE	SHEET 4 OF 5
UNIVERSAL INTERFACE (DIFFERENTIAL) PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLLOUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	BIT 8
2	BIT 8
3	DEV FLAG
4	DEV FLAG
5	
6	
7	SET TRANS ERROR FF
8	
9	BIT 10
10	BIT 10
11	BIT 9
12	BIT 9
13	BIT 13
14	BIT 13
15	BIT 12
16	BIT 12
17	BIT 8
18	BIT 8
19	BIT 14
20	BIT 14
21	BIT 15
22	BIT 15
23	BIT 12
24	BIT 12
25	BIT 13
26	BIT 13
27	BIT 10
28	BIT 10
29	BIT 11
30	BIT 11
31	BIT 9
32	BIT 9
33	BIT 8
34	BIT 8
35	SELF TEST LOGIC
36	
37	BIT 10
38	BIT 10
39	DEV CMD
40	DEV CMD
41	BIT 15
42	BIT 15
43	BIT 14
44	BIT 14
45	BIT 9
46	BIT 9
47	BIT 10
48	BIT 10
49	BIT 11
50	BIT 11

J2

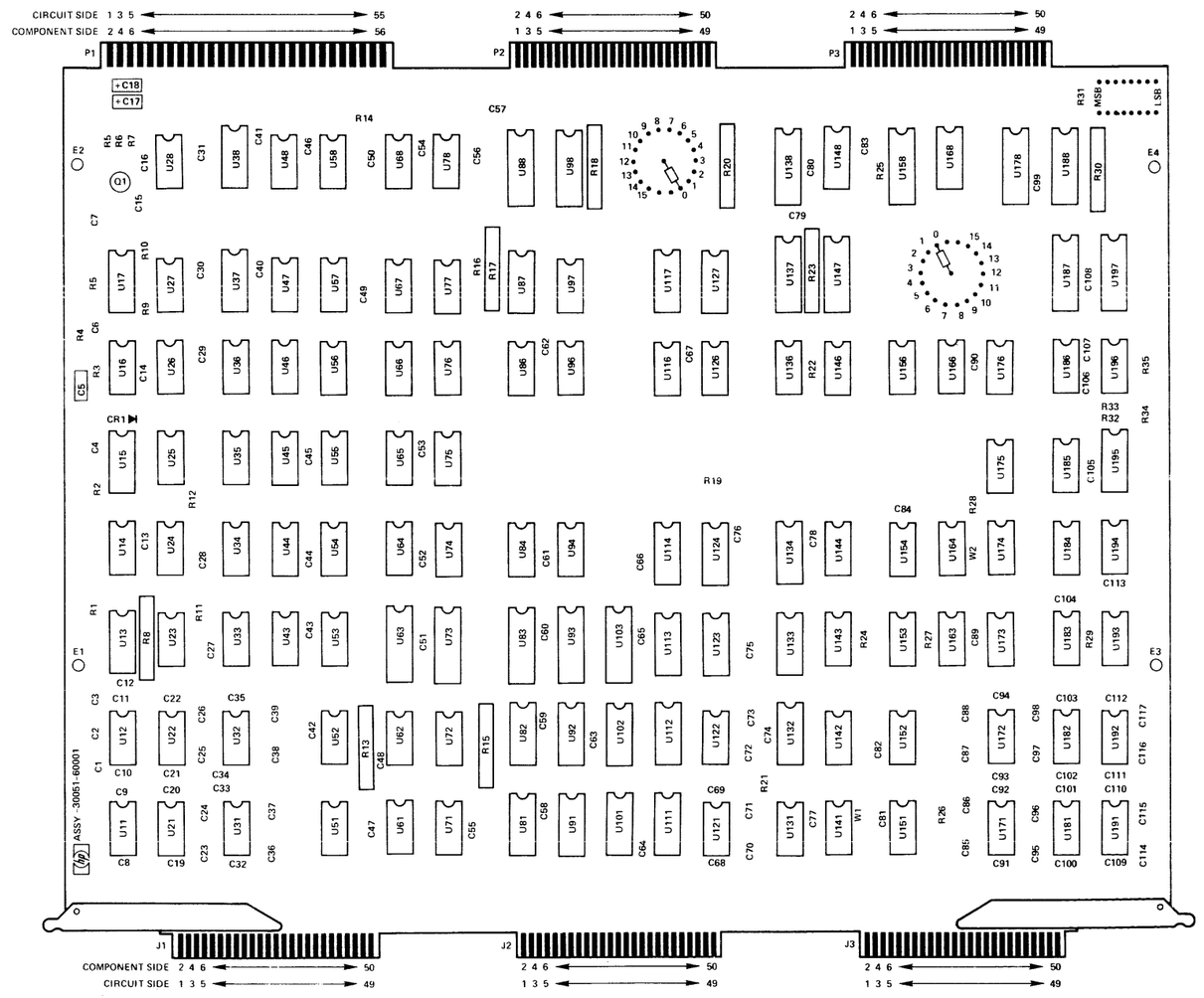
PIN	SIGNAL
1	POWER FAIL
2	POWER FAIL
3	PON
4	RET
5	CLEAR RELAY
6	CLEAR RELAY
7	J2W1
8	J2W1
9	J2W2
10	J2W2
11	J2W3
12	J2W3
13	J2W4
14	J2W4
15	J2W5
16	J2W5
17	
18	
19	
20	
21	J2W6
22	J2W6
23	
24	
25	J2W11
26	J2W11
27	
28	
29	
30	
31	
32	
33	
34	
35	J2W8
36	J2W8
37	J2W9
38	J2W9
39	J2W10
40	J2W10
41	BIT 9
42	BIT 9
43	MASTER CLEAR
44	MASTER CLEAR
45	BIT 11
46	BIT 11
47	CLR INF
48	CLR INF
49	DEV END
50	DEV END

J3

PIN	SIGNAL
1	BIT 2
2	BIT 2
3	BIT 4
4	BIT 4
5	BIT 6
6	BIT 6
7	BIT 8
8	BIT 8
9	BIT 7
10	BIT 7
11	SELF TEST PWR
12	SELF TEST PWR
13	SELF TEST PWR
14	SELF TEST PWR
15	BIT 1
16	BIT 1
17	BIT 3
18	BIT 3
19	BIT 7
20	BIT 7
21	BIT 5
22	BIT 5
23	BIT 6
24	BIT 6
25	BIT 0
26	BIT 0
27	BIT 12
28	BIT 12
29	BIT 7
30	BIT 7
31	BIT 6
32	BIT 6
33	BIT 4
34	BIT 4
35	BIT 5
36	BIT 5
37	BIT 14
38	BIT 14
39	BIT 1
40	BIT 1
41	BIT 0
42	BIT 0
43	BIT 15
44	BIT 15
45	BIT 3
46	BIT 3
47	BIT 2
48	BIT 2
49	BIT 13
50	BIT 13

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11,12	0721	51,52	0720	87	0491	138	0759	181,182	0721
13	0834	53	0512	88	0760			183	0373
14	0239	54	0141			141,142	0720	184	0512
15 17	0515	55	0512	91,92	0616	143,144	0512	185	0686
		56	0282	93	0756	146	0370	186	0512
21,22	0721	57	0141	94,96	0141	147	0760	187	0760
23	0512	58	0512	97	0374	148	0706	188	0756
24	0844			98	0759				
25	0512	61,62	0720			151,152	0720	191,192	0721
26	0205	63	0756	101,102	0626	153	0424	193	0512
27	0370	64	0371	103	0756	154	0377	194	0424
28	0141	65	0512			156	0371	195	0301
		66	0371	111,112	0616	158	0760	196	0844
31,32	0721	67	0377	113,114	0626			197	0755
33	0512	68	0141	116	0424	163	0370		
34	0424	71,72	0720	117	0715	164	0141		
35,36	0141	73	0756			166	0372		
37	0629	74,75	0141	121,122	0721	168	0706		
38	0574	76	0424	123,124	0626				
		77	0377	126	0900	171,172	0721		
43	0512	78	0512	127	0715	173	0141		
44	0375					174	0761		
45	0371	81,82	0626	131,132	0720	175	0141		
46	0370	83	0756	133,134	0626	176	0424		
47	0424	84	0424	136	0141	178	0756		
48	0141	86	0686	137	0755				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1230-22
D	22-1625	A-1249-22
E	22-1630	B-1249-22
F	22-1693	B-1305-22

DATA IN LOGIC

DATA FROM DEVICE

BIT 15 J1-22 J1-21 C19 2000 U21B C23 100
BIT 14 J1-20 J1-19 C20 2000 U21A C24 100
BIT 13 J1-26 J1-25 C32 2000 U31B C36 100
BIT 12 J1-24 J1-23 C33 2000 U31A C37 100
BIT 11 J1-30 J1-29 C35 2000 U32B C38 100
BIT 10 J1-28 J1-27 C34 2000 U32A C39 100
BIT 9 J1-32 J1-31 C21 2000 U22B C25 100
BIT 8 J1-18 J1-17 C22 2000 U22A C26 100
BIT 7 J3-30 J3-29 C94 2000 U172A C87 100
BIT 6 J3-32 J3-31 C92 2000 U171A C86 100
BIT 5 J3-36 J3-35 C91 2000 U171B C85 100
BIT 4 J3-34 J3-33 C93 2000 U172B C88 100
BIT 3 J3-46 J3-45 C110 2000 U191A C115 100
BIT 2 J3-48 J3-47 C109 2000 U191B C114 100
BIT 1 J3-40 J3-39 C101 2000 U181A C96 100
BIT 0 J3-42 J3-41 C100 2000 U181B C95 100

R13G 1 +5V
R13A 1 +5V
R35 +5V

(D) (E32) (E21)
(K) (A32)

U82 4-BIT REGISTER (P_{15} P_{14} P_{13} P_{12} D_{15} D_{14} D_{13} D_{12} Q_{15} Q_{14} Q_{13} Q_{12}) ENABLE CLEAR
U81 4-BIT REGISTER (P_{11} P_{10} P_9 P_8 D_{11} D_{10} D_9 D_8 Q_{11} Q_{10} Q_9 Q_8) ENABLE CLEAR
U83 ENABLE 9,11 → (B17) DI_{15} DI_{14} DI_{13} DI_{12} DI_{11} DI_{10} DI_9 DI_8
U103 ENABLE 9,11 → (B16) DI_7 DI_6 DI_5 DI_4 DI_3 DI_2 DI_1 DI_0

U92 QUAD 2-BIT MULTIPLEXER (A_1 A_2 B_1 B_2 C_1 C_2 D_1 D_2 Q_A Q_B Q_C Q_D) ENABLE SELECT
U102 4-BIT REGISTER (P_7 P_6 P_5 P_4 D_7 D_6 D_5 D_4 Q_7 Q_6 Q_5 Q_4) ENABLE CLEAR
U91 QUAD 2-BIT MULTIPLEXER (A_1 A_2 B_1 B_2 C_1 C_2 D_1 D_2 Q_A Q_B Q_C Q_D) ENABLE SELECT
U101 4-BIT REGISTER (P_3 P_2 P_1 P_0 D_3 D_2 D_1 D_0 Q_3 Q_2 Q_1 Q_0) ENABLE CLEAR

U84F (C25) COUNT 3
U66B
U94A
U34A (B25) COUNT 1
U14D
U94D (D9) D READ STB (F9) P READ STB
U84E ACK 4 (D9)
R15B +5V
J2-16 J2-15 J2-W5

(D24) EXT DEV END
U94B
(G32) MRI

DATA OUT LOGIC

(B19) DO_{15} DO_{14} DO_{13} DO_{12} → U113 4-BIT REGISTER (P_{15} P_{14} P_{13} P_{12} D_{15} D_{14} D_{13} D_{12} Q_{15} Q_{14} Q_{13} Q_{12}) ENABLE CLEAR
(B19) DO_{11} DO_{10} DO_9 DO_8 → U123 4-BIT REGISTER (P_{11} P_{10} P_9 P_8 D_{11} D_{10} D_9 D_8 Q_{11} Q_{10} Q_9 Q_8) ENABLE CLEAR
(B18) DO_7 DO_6 DO_5 DO_4 → U114 4-BIT REGISTER (P_7 P_6 P_5 P_4 D_7 D_6 D_5 D_4 Q_7 Q_6 Q_5 Q_4) ENABLE CLEAR
(B18) DO_3 DO_2 DO_1 DO_0 → U124 4-BIT REGISTER (P_3 P_2 P_1 P_0 D_3 D_2 D_1 D_0 Q_3 Q_2 Q_1 Q_0) ENABLE CLEAR

U112 QUAD 2-BIT MULTIPLEXER (A_1 A_2 B_1 B_2 C_1 C_2 D_1 D_2 Q_A Q_B Q_C Q_D) ENABLE SELECT
U111 QUAD 2-BIT MULTIPLEXER (A_1 A_2 B_1 B_2 C_1 C_2 D_1 D_2 Q_A Q_B Q_C Q_D) ENABLE SELECT

U62A J1-41 J1-42 BIT 15
U62B J1-43 J1-44 BIT 14
U52B J1-13 J1-14 BIT 13
U52A J1-15 J1-16 BIT 12
U71B J1-49 J1-50 BIT 11
U71A J1-47 J1-48 BIT 10
U61B J1-45 J1-46 BIT 9
U61A J1-33 J1-34 BIT 8
U131B J3-19 J3-20 BIT 7
U151B J3-23 J3-24 BIT 6
U151A J3-21 J3-22 BIT 5
U131A J3-3 J3-4 BIT 4
U152A J3-17 J3-18 BIT 3
U152B J3-1 J3-2 BIT 2
U142B J3-15 J3-16 BIT 1
U142B J3-25 J3-26 BIT 0

DATA TO DEVICE

U76D 8 9

(C25) SEQ 2
U66C U66A BYTE WRITE FF
U76
(A36) LD WRT BUF
(G32) MRI
(C37) BYTE TRANS
U76F U77F U77A U77E
(D35) BYTE WRITE
R15F 1 +5V
J2-26 J2-25 J2-W7

30051-60001	TITLE	SHEET 5 of 5
UNIVERSAL INTERFACE (DIFFERENTIAL) PCA		
ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

I/O DETAILED DIAGRAM SET

DD-508

TERMINAL DATA INTERFACE PCA

30060-60001

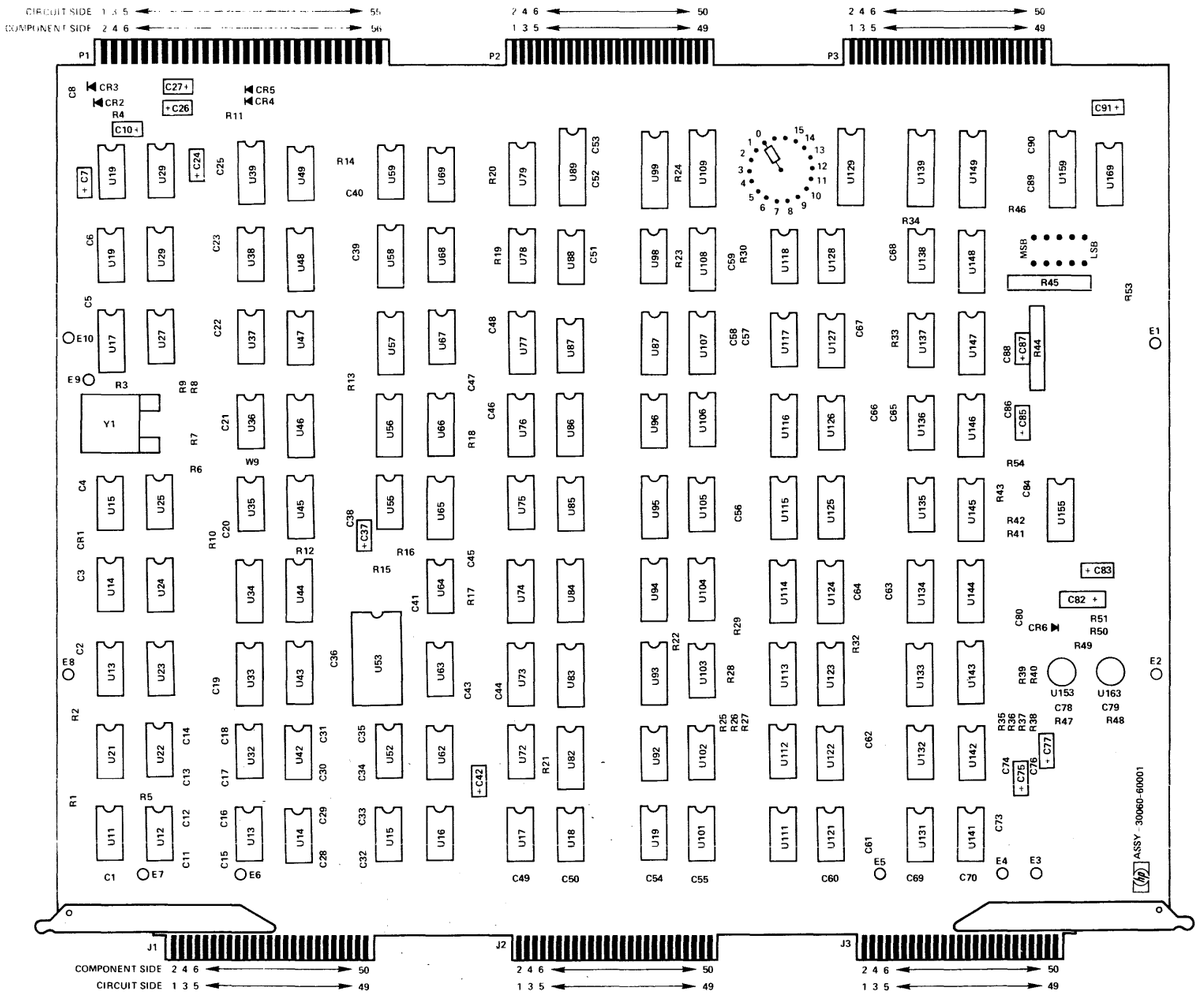
SERIES 1251

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL
1	+5V	1	CHAN SO	1		1	+15V
2	+5V	2	COM	2		2	+15V
3	+5V	3	SR CLOCK	3	COM	3	+15V
4	+5V	4	COM	4	IOCMD 00	4	+15V
5	PF WARN	5	DEV END	5	IOCMD 02	5	OSC TEST
6	ENTIMER	6	COM	6	IOCMD 01	6	—
7	(SPARE)	7	ACK SR	7	COM	7	—
8	(SPARE)	8	COM	8	DEVNO 00	8	—
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	—
10	COM	10	COM	10	COM	10	BA0
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	—
12	COM	12	SIO ENABLE	12	DEVNO 03	12	—
13	MCUCLKS	13	EOT	13	COM	13	BA1
14	COM	14	JMP MET	14	DEVNO 04	14	—
15	COM	15	COM	15	DEVNO 05	15	BA3
16	COM	16	TOGGLE INXFER	16	COM	16	BA2
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	BA4
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	BA5
19	COM	19	TOGGLE SIO OK	19	COM	19	BA7
20	COM	20	COM	20	IOD 00	20	BA6
21	+15V	21	XFER ERROR	21	IOD 01	21	—
22	+15V	22	REQ	22	COM	22	—
23	+15V	23	COM	23	IOD 02	23	BB7
24	+15V	24	SR 15	24	IOD 03	24	—
25	-15V	25	SR 14	25	COM	25	BB0
26	-15V	26	SR 13	26	IOD 04	26	BB5
27	-15V	27	SR 12	27	IOD 05	27	BA8
28	-15V	28	SR 11	28	COM	28	BA9
29	COM	29	SR 10	29	IOD 06	29	BA11
30	COM	30	COM	30	IOD 07	30	BA10
31	-20V	31	SR 9	31	COM	31	BB3
32	-20V	32	SR 8	32	IOD 08	32	BA13
33	-20V	33	SR 7	33	IOD 09	33	BA12
34	-20V	34	SR 6	34	COM	34	BA15
35	+20V	35	SR 5	35	IOD 10	35	BB2
36	+20V	36	COM	36	IOD 11	36	BA14
37	+20V	37	SR 4	37	COM	37	BB4
38	+20V	38	SR 3	38	IOD 12	38	BB1
39	+20V	39	SR 2	39	IOD 13	39	—
40	+20V	40	SR 1	40	COM	40	BB6
41	HSREQ	41	SR 0	41	IOD 14	41	BB8
42	COM	42	COM	42	IOD 15	42	BB9
43	COM	43	P CMD 1	43	COM	43	BB12
44	INTPOLL OUT	44	SET JMP	44	INTREQ	44	BB14
45	(SPARE)	45	P STATUS STB	45		45	BB11
46	COM	46	P CONT STB	46	COM	46	BB10
47	COM	47	RD NEXT WD	47		47	BB13
48	INTPOLL IN	48	P WRITE STB	48		48	BB15
49	SI	49	SET INT	49	COM	49	COM
50	COM	50	P READ STB	50	INTACK	50	COM
51	COM						
52	DATAPOLL OUT						
53	SO						
54	COM						
55	COM						
56	DATAPOLL IN						

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0616	41,42	0509	71	0141	91,92	0370	121	0371	141,142	0376
12	0063	43,44	0301	72	0063	93	0231	122	0141	143	0733
13	0424	45	0076	73	0616	94	0839	123,124	0616	144	0616
14	0371	46	0715	74	0231	95,96	0616	125	0616	145	0839
15	0141	47	0370	75	0063	97	0301	126	0435	146,147	0301
17	0715	48	0301	76	0616	98	0844	127	0140	148	0706
18	0327	49	0327	77	0301	99	0755	128	0370	149	0760
19	0141	51	0990	78	0077			129	0760	153	0832
		53	0640	79	0214	101	0328			155	0715
21	0077	55	0376			102	0424	131	0370	159	0756
22	0376	56	0250	81	0370	103	0328	132	0205		
23,24	0294	57,58	0301	82	0616	104	0616	133,134	0839	163	0832
25	0140	59	0374	83	0839	105,106	0367	135	0367	168	0706
27	0424			84	0616	107,108	0301	136,137	0327		
28,29	0370	61,62	0990	86	0839	109	0760	138	0761		
		63	0376	85	0435			139	0755		
31,32	0509	64	0077	87	0301	111	0424				
33,34	0301	65,66	0231	88	0686	112	0141				
35	0261	67,68	0327	89	0760	113	0733				
36	0217	69	0141			114	0231				
37	0328					115,116	0839				
38	0140					117	0140				
39	0301					118	0424				



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1205-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-A	A-1225-22	ALL
D	PC-22-M22	B-1251-21	ALL
E	ERRATA	NO CHANGE	ALL

INTERRUPT LOGIC

INTPOLL IN ← P1-48

U118A

+5V

R30 3.16K

C59 75PF

U98A

INT LATCH U108A

U38A

U118B

INT ACTIVE FF

U128D

U128A

MASTER RESET (C11)

(F4) DOOO

U28D

U19A

U69A

U69D

RESET INT (F6)

U88A

U69C

U88C

P1-44 → INTPOLL OUT

U138A

P3-50 → INT ACK1

U138B

P3-44 → INTREQ

U98B

R23 3.16K

C51 75PF

U59B

INT MASK FF U78A

R19

U118F

INTREQ

U88B

U128B

U128C

U138C

P1-49 → SI

SERVICE IN GENERATOR

D CONT STB

U118D

U118E

U59A

U27E

SET INT

D CONT STB (B11)

D WRIT STB 1,2,4,5

D STAT STB (A12)

D READ STB (D17)

U55A

WT STB (E21)

U79 BINARY TO DECIMAL DECODER

COMMAND DECODER

U29D

U28C

U19D

(A5) RESET INT

R15 1K

(B13) FLAG

INTERRUPT REQUEST FF U64A

INTREQ (A13)

SO ← P1-53
IO RESET ← P1-11
IO CMDO ← P3-4
IOCMD1 ← P3-6
IO CMD2 ← P3-5

U89 ENABLE

R20

CR3 CR2 +15V → +10V TO LINE DRIVERS

R4 147 1/2W

C10 ±2.2UF

CR5 CR4 -15V → -10V TO LINE DRIVERS

R11 147 1/2W

C26 ±2.2UF

R34

DISABLE

IOD15 ← P3-42
IOD14 ← P3-41
IOD13 ← P3-39
IOD12 ← P3-38
IOD11 ← P3-36
IOD10 ← P3-35
IOD09 ← P3-33
IOD08 ← P3-32

U129

IOD07 ← P3-30
IOD06 ← P3-29
IOD05 ← P3-27
IOD04 ← P3-26
IOD03 ← P3-24
IOD02 ← P3-23
IOD01 ← P3-21
IOD00 ← P3-20

U109

ENABLE

DO15 (B11)(E21)
DO14 (E21)(B12)
DO13 (E21)
DO12 (D21)
DO11 (D21)
DO10 (D21)
DO09 (D21)
DO08 (C21)
DO07 (C21)
DO06 (A14)(C21)
DO05 (A14)(B21)
DO04 (A14)(B21)
DO03 (B14)(B21)
DO02 (B14)(B21)
DO01 (A21)
DO00 (B3)(D11)(A21)

ENABLE

U139

U99

DI15 (G27)
DI14 (G27)
DI13 (F27)
DI12 (F27)
DI11 (G26)
DI10 (G26)
DI09 (F26)
DI08 (F26)
DI07 (B18)
DI06 (B18)
DI05 (C18)
DI04 (B16)
DI03 (C16)
DI02 (A18)
DI01 (A18)
DI00 (B18)

R1 316 1/2W
R2 316 1/2W
C8 .01UF
C27 2.2UF
C79 .01UF
C83 2.2UF
C16,55 2.2UF
C15,54 .01UF
C70 .01UF
C77 2.2UF

J1-3,4 ← -15V
J1-1,2 ← +15V
J1-49,50 ← COM
P1-17,18 ← -5V
P1-1,2,3,4 ← +5V
P1-15,16,19, 20,29,30 ← COM
P1-43,47,50,54 ← COM
P2-2,4,6,8,10,15, 20,23,30,36,42 ← COM
P3-3,7,10,13,16,19,22,25, 28,31,34,37,40,43,46,49 ← COM

R24G 8 1.5K
R24F 7 1.5K
R24E 6 1.5K
R24D 5 1.5K
R24C 4 1.5K
R24B 3 1.5K
R24A 2 1.5K
R14 1.5K
R33
R44G 8 1.5K
R44F 7 1.5K
R44E 6 1.5K
R44D 5 1.5K
R44C 4 1.5K
R44A 2 1.5K
R44B 3 1.5K
+5V

+5V R53
R45A 1.5K
R45B 1.5K
R45C 1.5K
R45D 1.5K
R45E 1.5K
R45F 1.5K
R45G 1.5K

U159

P3-18 → DEVN07
P3-17 → DEVN06
P3-15 → DEVN05
P3-14 → DEVN04
P3-12 → DEVN03
P3-11 → DEVN02
P3-9 → DEVN01
P3-8 → DEVN00

U149

R46 +5V

U148 5-BIT COMPARATOR

W1
W2
W3
W4

ADDRESS GENERATOR / COMPARATOR

U169 5-BIT COMPARATOR

W5
W6
W7
W8

1. ALL RESISTOR VALUES ARE IN OHMS, 1.47K, 1/8W, ±1%

NOTE: UNLESS OTHERWISE SPECIFIED

30060-60001 TITLE SHEET 1 OF 4

TERMINAL DATA INTERFACE PCA

ENGINEER | APPROVED | DATE

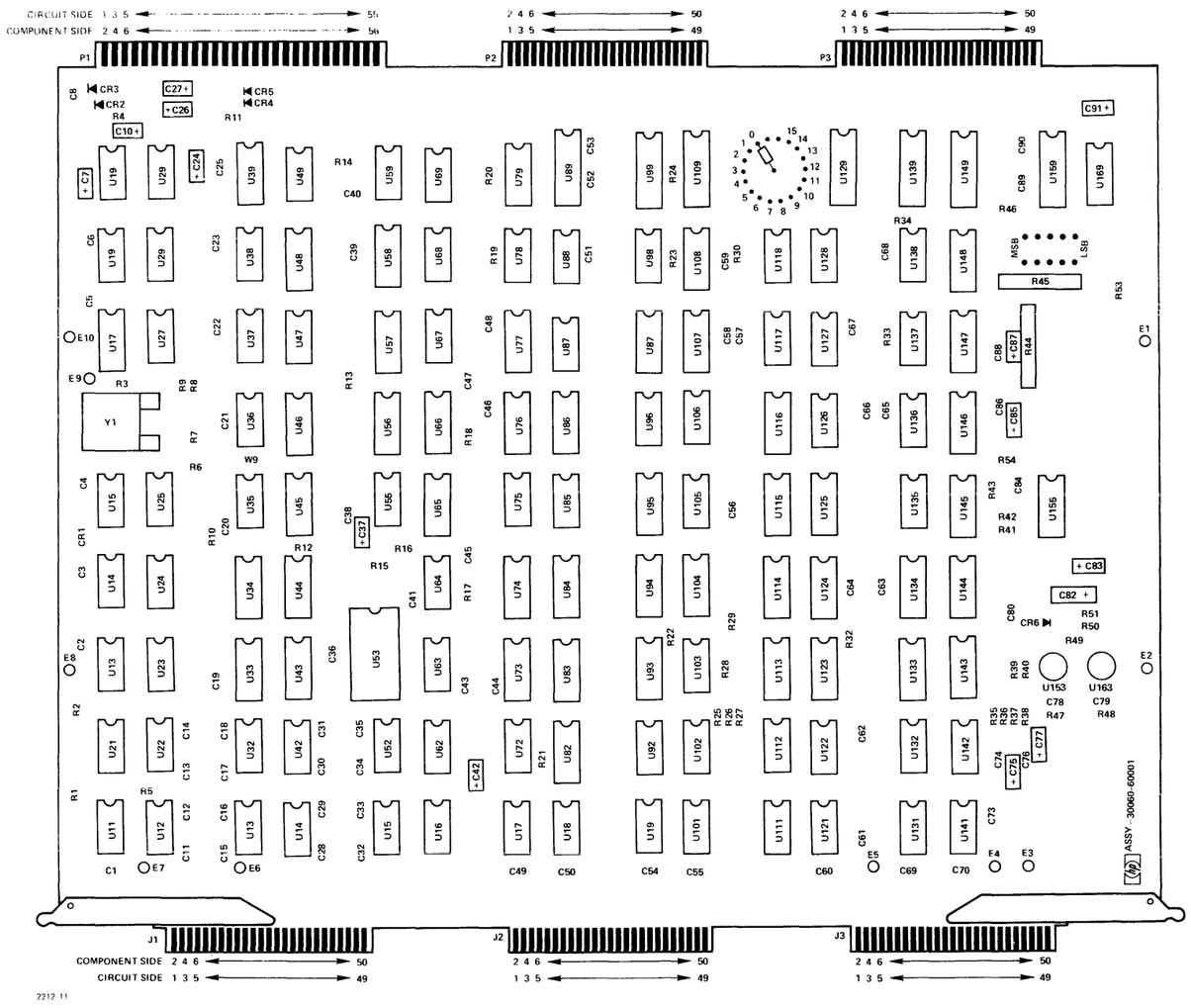
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL
1	+5V	1	CHAN SO	1		1	+15V
2	+5V	2	COM	2		2	+15V
3	+5V	3	SR CLOCK	3	COM	3	+15V
4	+5V	4	COM	4	IOCMD 00	4	+15V
5	PF WARN	5	DEV END	5	IOCMD 02	5	OSC TEST
6	ENTIMER	6	COM	6	IOCMD 01	6	—
7	(SPARE)	7	ACK SR	7	COM	7	—
8	(SPARE)	8	COM	8	DEVNO 00	8	—
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	—
10	COM	10	COM	10	COM	10	BA0
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	—
12	COM	12	SIO ENABLE	12	DEVNO 03	12	—
13	MCUCLKS	13	EOT	13	COM	13	BA1
14	COM	14	JMP MET	14	DEVNO 04	14	—
15	COM	15	COM	15	DEVNO 05	15	BA3
16	COM	16	TOGGLE INXFER	16	COM	16	BA2
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	BA4
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	BA5
19	COM	19	TOGGLE SIO OK	19	COM	19	BA7
20	COM	20	COM	20	IOD 00	20	BA6
21	+15V	21	XFER ERROR	21	IOD 01	21	—
22	+15V	22	REQ	22	COM	22	—
23	+15V	23	COM	23	IOD 02	23	BB7
24	+15V	24	SR 15	24	IOD 03	24	—
25	-15V	25	SR 14	25	COM	25	BB0
26	-15V	26	SR 13	26	IOD 04	26	BB5
27	-15V	27	SR 12	27	IOD 05	27	BA8
28	-15V	28	SR 11	28	COM	28	BA9
29	COM	29	SR 10	29	IOD 06	29	BA11
30	COM	30	COM	30	IOD 07	30	BA10
31	-20V	31	SR 9	31	COM	31	BB3
32	-20V	32	SR 8	32	IOD 08	32	BA13
33	-20V	33	SR 7	33	IOD 09	33	BA12
34	-20V	34	SR 6	34	COM	34	BA15
35	+20V	35	SR 5	35	IOD 10	35	BB2
36	+20V	36	COM	36	IOD 11	36	BA14
37	+20V	37	SR 4	37	COM	37	BB4
38	+20V	38	SR 3	38	IOD 12	38	BB1
39	+20V	39	SR 2	39	IOD 13	39	—
40	+20V	40	SR 1	40	COM	40	BB6
41	HSREQ	41	SR 0	41	IOD 14	41	BB8
42	COM	42	COM	42	IOD 15	42	BB9
43	COM	43	P CMD 1	43	COM	43	BB12
44	INTPOLL OUT	44	SET JMP	44	INTREQ	44	BB14
45	(SPARE)	45	P STATUS STB	45		45	BB11
46	COM	46	P CONT STB	46	COM	46	BB10
47	COM	47	RD NEXT WD	47		47	BB13
48	INTPOLL IN	48	P WRITE STB	48		48	BB15
49	SI	49	SET INT	49	COM	49	COM
50	COM	50	P READ STB	50	INTACK	50	COM
51	COM						
52	DATAPOLL OUT						
53	SO						
54	COM						
55	COM						
56	DATAPOLL IN						

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0616	41,42	0509	71	0141	91,92	0370	121	0371	141,142	0376
12	0063	43,44	0301	72	0063	93	0231	122	0141	143	0733
13	0424	45	0076	73	0616	94	0839	123,124	0616	144	0616
14	0371	46	0715	74	0231	95,96	0616	125	0616	145	0839
15	0141	47	0370	75	0063	97	0301	126	0435	146,147	0301
17	0715	48	0301	76	0616	98	0844	127	0140	148	0706
18	0327	49	0327	77	0301	99	0755	128	0370	149	0760
19	0141	51	0990	78	0077			129	0760	153	0832
		53	0640	79	0214	101	0328			155	0715
21	0077	55	0376			102	0424	131	0370	159	0756
22	0376	56	0250	81	0370	103	0328	132	0205		
23,24	0294	57,58	0301	82	0616	104	0616	133,134	0839	163	0832
25	0140	59	0374	83	0839	105,106	0367	135	0367	168	0706
27	0424			84	0616	107,108	0301	136,137	0327		
28,29	0370	61,62	0990	86	0839	109	0760	138	0761		
		63	0376	85	0435			139	0755		
31,32	0509	64	0077	87	0301	111	0424				
33,34	0301	65,66	0231	88	0686	112	0141				
35	0261	67,68	0327	89	0760	113	0733				
36	0217	69	0141			114	0231				
37	0328					115,116	0839				
38	0140					117	0140				
39	0301					118	0424				



2212-11

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1205-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1225-22
D	22-1621	B-1251-22
E	ERRATA	NO CHANGE

UP/DOWN TRANSFER LOGIC

CLOCK AND TIMING LOGIC

LINE RECEIVERS

P/O STATUS INPUT BUFFER

UP/DOWN ADDRESS BUFFER

P/O STATUS INPUT BUFFER

FIELD COUNTER

ADDRESS COUNTER

MAIN/ DIAGNOSE CHANNEL SELECT LOGIC

OUTPUT REGISTERS

OUTPUT BUFFERS

LINE DRIVERS

30060-60001	SHEET 2 OF 4
TERMINAL DATA INTERFACE PCA	
ENGINEER	APPROVED / DATE
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION	

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLL OUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

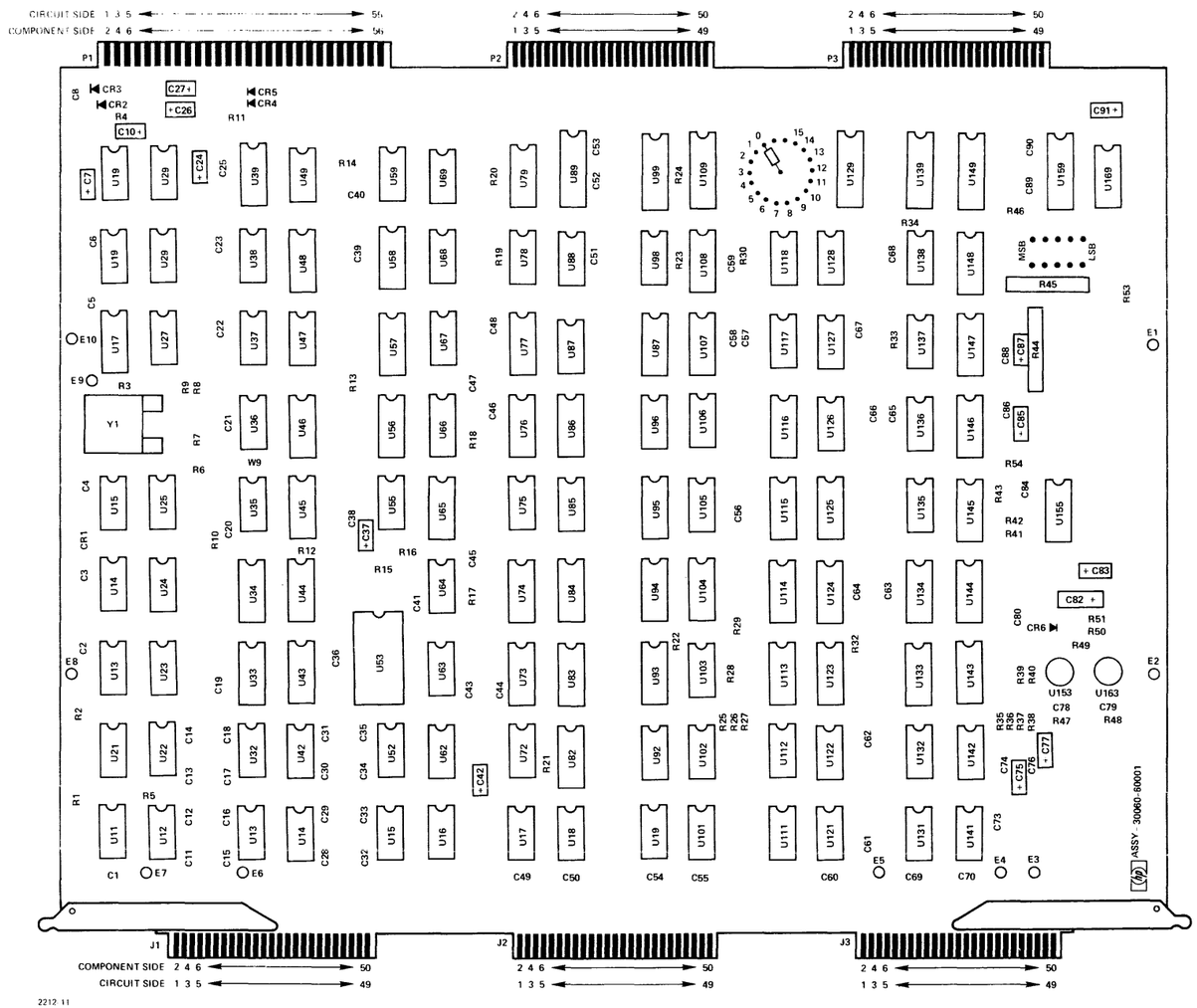
PIN	SIGNAL
1	
2	
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	
46	COM
47	
48	
49	COM
50	INTACK

J1

PIN	SIGNAL
1	+15V
2	+15V
3	+15V
4	+15V
5	OSC TEST
6	—
7	—
8	—
9	—
10	BA0
11	—
12	—
13	BA1
14	—
15	BA3
16	BA2
17	BA4
18	BA5
19	BA7
20	BA6
21	—
22	—
23	BB7
24	—
25	BB0
26	BB5
27	BA8
28	BA9
29	BA11
30	BA10
31	BB3
32	BA13
33	BA12
34	BA15
35	BB2
36	BA14
37	BB4
38	BB1
39	—
40	BB6
41	BB8
42	BB9
43	BB12
44	BB14
45	BB11
46	BB10
47	BB13
48	BB15
49	COM
50	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0616	41,42	0509	71	0141	91,92	0370	121	0371	141,142	0376
12	0063	43,44	0301	72	0063	93	0231	122	0141	143	0733
13	0424	45	0076	73	0616	94	0839	123,124	0616	144	0616
14	0371	46	0715	74	0231	95,96	0616	125	0616	145	0839
15	0141	47	0370	75	0063	97	0301	126	0435	146,147	0301
17	0715	48	0301	76	0616	98	0844	127	0140	148	0706
18	0327	49	0327	77	0301	99	0755	128	0370	149	0760
19	0141	51	0990	78	0077			129	0760	153	0832
		53	0640	79	0214	101	0328			155	0715
21	0077	55	0376			102	0424	131	0370	159	0756
22	0376	56	0250	81	0370	103	0328	132	0205		
23,24	0294	57,58	0301	82	0616	104	0616	133,134	0839	163	0832
25	0140	59	0374	83	0839	105,106	0367	135	0367	168	0706
27	0424			84	0616	107,108	0301	136,137	0327		
28,29	0370	61,62	0990	86	0839	109	0760	138	0761		
		63	0376	85	0435			139	0755		
31,32	0509	64	0077	87	0301	111	0424				
33,34	0301	65,66	0231	88	0686	112	0141				
35	0261	67,68	0327	89	0760	113	0733				
36	0217	69	0141			114	0231				
37	0328					115,116	0839				
38	0140					117	0140				
39	0301					118	0424				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1205-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1225-22
D	22-1621	B-1251-22
E	ERRATA	NO CHANGE

DATA OUT HOLDING REGISTER

(F4) D000 — P/D U77A — D000 — TRANSFER DOWN (B13)
(F4) D001 — S/R U77B — D001 — S/R (E14)
(F4) D002 — ENABLE U77C — D002 — ENABLE
(F4) D003 — PARITY/ECHO U77D — D003 — (D29) F, (D29) E, PARITY/ECHO
(F4) D004 — SYNC/DIAGNOSE U87A — D004 — (D29) D, (D29) C — D004 (D24)
(F4) D005 — CHAR BIT10 U87B — D005 (A38) — D005 (A38)
(E4) D006 — CHAR BIT9 U87C — D006 (A38)
(E4) D007 — CHAR BIT8 U87D — D007
(E4) D008 — BAUD BIT7 U97A — D008
(E4) D009 — BAUD BIT6 U97B — D009
(E4) D010 — BAUD BIT5 U97C — D010
(E4) D011 — BAUD BIT4 U97D — D011
(E4) D012 — BAUD BIT3 U107A — D012
(E4) D013 — BAUD BIT2 U107B — D013
(E4) D014 — BAUD BIT1 U107C — D014
(E4) D015 — (D7) WT STB — BAUD BIT0 U107D — D015

U92B, U91D, U102C, U111F, U92C, U131D, U131A, U141A
PARAMETER, DATA (F35), (G16) DP, E4, E3
(F16) LOGIC CLK — PARAM LATCH CLOCK (D31)
PARAM MUX LOAD (B31)

LOWER CONTROL BUFFER
U76 QUAD 2-BIT MULTIPLEXER
U86 4-BIT REGISTER
ENABLE (D39), ECHO (H34)

DIAGNOSE (E16)
U96 QUAD 2-BIT MULTIPLEXER
LINE (C17)

DATA ACCUMULATOR/ BUFFERS
U106 4-BIT SHIFT REGISTER
U116 4-BIT REGISTER
U95 QUAD 2-BIT MULTIPLEXER
U105 4-BIT SHIFT REGISTER
I9 (B16), I8 (B16)
PARALLEL CLOCK ENABLE
PARALLEL DATA CLOCK
SERIAL DATA CLOCK

DATA MUX LOAD
(B22) D004
U115 4-BIT REGISTER
U125 QUAD 2-BIT MULTIPLEXER
U135 4-BIT SHIFT REGISTER
U145 4-BIT REGISTER
SEND BIT (G35)
PARALLEL DATA CLOCK (F37)
PARALLEL CLOCK ENABLE (F35)
(E32) DATA MUX ENABLE
BUFFER CLK (F40)
BUFFER CLK

LOWER MOS MEMORY
U143 QUAD 256-BIT SHIFT REGISTER
(F34), (G34)
R42 3.16K +5V
R35 3.16K
R36 3.16K
R41 3.16K
R40 3.16K
R37 3.16K
R38 3.16K
R39 3.16K -5V
(F) (B22), (E) (B22), (D) (B22), (C) (B22)

P/O RESET LOGIC
U117B (D12) INITIALIZE → INITIALIZE
U117A → MR1 (B32) (D36)
U127A → MR2 (B34) (D31)

DATA INPUT BUFFER
U147A, U147B, U147C, U147D
U137A, U137D, U137C, U137B
DI08 (G6), DI09 (G6), DI10 (G6), DI11 (G6)
(C14) LOAD PULSE
U146A, U146B, U146C, U146D
U136A, U136D, U136C, U136B
DI12 (F6), DI13 (F6), DI14 (F6), DI15 (F6)
(D18) RD STB

INPUT PARITY CHECKER/GEN
U126 PARITY CHECKER/GENERATOR
ΣEVEN, ΣODD → (B) (C17)
+5V R54 — EVEN IN, ODD IN

OUTPUT PARITY LOGIC
U85 PARITY CHECKER/GENERATOR
D008 (A35), D009 (A35), D010 (A35), D011 (A35), D012 (B31), D013 (A31), D014 (A31), D015 (A31)
PARITY BIT
U102A, U75B → PARITY
+5V R17 — EVEN IN, ODD IN

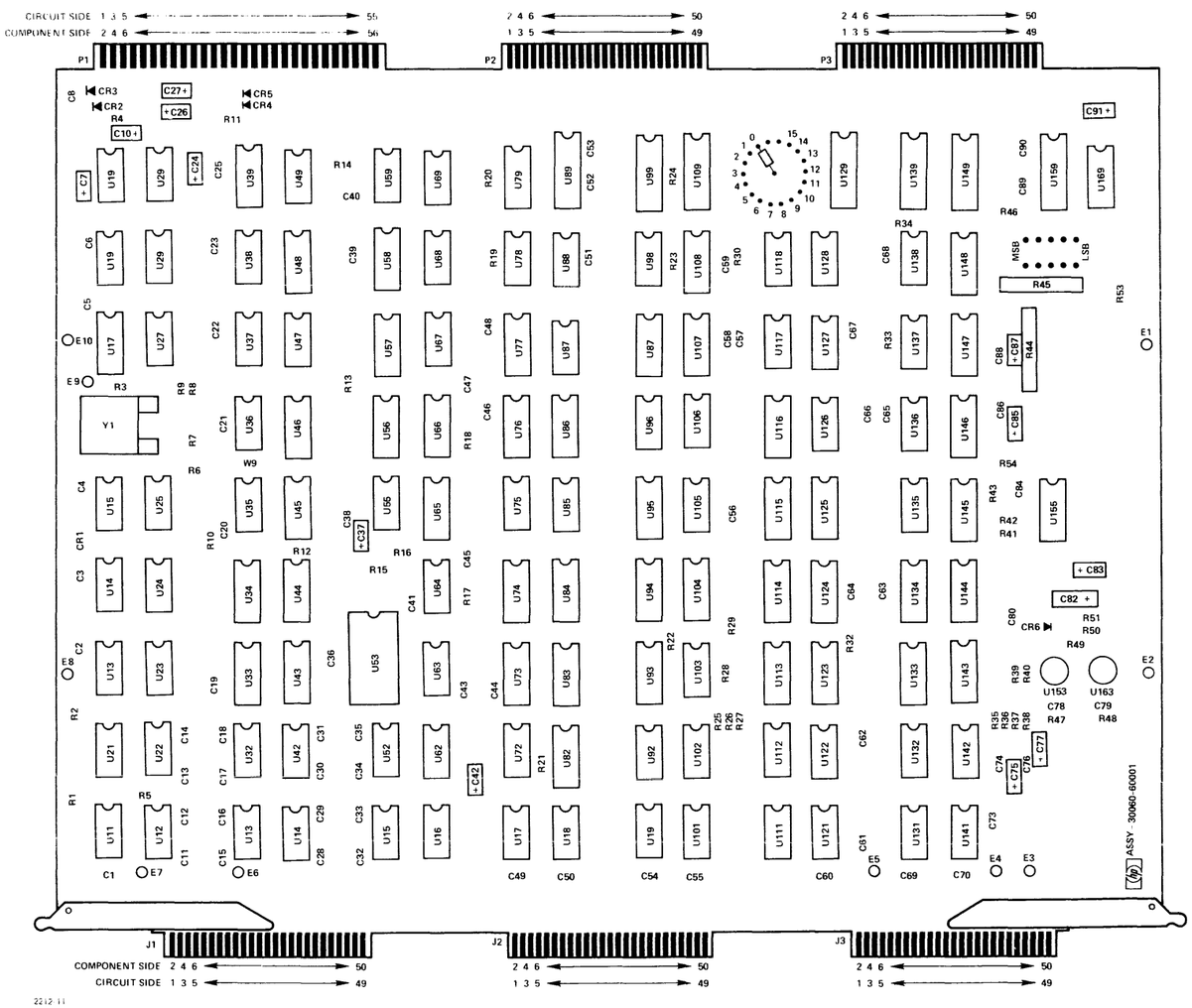
30060-60001	TITLE	SHEET 3 OF 4
TERMINAL DATA INTERFACE PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL
1	+5V	1	CHAN SO	1		1	+15V
2	+5V	2	COM	2		2	+15V
3	+5V	3	SR CLOCK	3	COM	3	+15V
4	+5V	4	COM	4	IOCMD 00	4	+15V
5	PF WARN	5	DEV END	5	IOCMD 02	5	OSC TEST
6	ENTIMER	6	COM	6	IOCMD 01	6	—
7	(SPARE)	7	ACK SR	7	COM	7	—
8	(SPARE)	8	COM	8	DEVNO 00	8	—
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	—
10	COM	10	COM	10	COM	10	BA0
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	—
12	COM	12	SIO ENABLE	12	DEVNO 03	12	—
13	MCUCLKS	13	EOT	13	COM	13	BA1
14	COM	14	JMP MET	14	DEVNO 04	14	—
15	COM	15	COM	15	DEVNO 05	15	BA3
16	COM	16	TOGGLE INXFER	16	COM	16	BA2
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	BA4
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	BA5
19	COM	19	TOGGLE SIO OK	19	COM	19	BA7
20	COM	20	COM	20	IOD 00	20	BA6
21	+15V	21	XFER ERROR	21	IOD 01	21	—
22	+15V	22	REQ	22	COM	22	—
23	+15V	23	COM	23	IOD 02	23	BB7
24	+15V	24	SR 15	24	IOD 03	24	—
25	-15V	25	SR 14	25	COM	25	BB0
26	-15V	26	SR 13	26	IOD 04	26	BB5
27	-15V	27	SR 12	27	IOD 05	27	BA8
28	-15V	28	SR 11	28	COM	28	BA9
29	COM	29	SR 10	29	IOD 06	29	BA11
30	COM	30	COM	30	IOD 07	30	BA10
31	-20V	31	SR 9	31	COM	31	BB3
32	-20V	32	SR 8	32	IOD 08	32	BA13
33	-20V	33	SR 7	33	IOD 09	33	BA12
34	-20V	34	SR 6	34	COM	34	BA15
35	+20V	35	SR 5	35	IOD 10	35	BB2
36	+20V	36	COM	36	IOD 11	36	BA14
37	+20V	37	SR 4	37	COM	37	BB4
38	+20V	38	SR 3	38	IOD 12	38	BB1
39	+20V	39	SR 2	39	IOD 13	39	—
40	+20V	40	SR 1	40	COM	40	BB6
41	HSREQ	41	SR 0	41	IOD 14	41	BB8
42	COM	42	COM	42	IOD 15	42	BB9
43	COM	43	P CMD 1	43	COM	43	BB12
44	INTPOLL OUT	44	SET JMP	44	INTREQ	44	BB14
45	(SPARE)	45	P STATUS STB	45		45	BB11
46	COM	46	P CONT STB	46	COM	46	BB10
47	COM	47	RD NEXT WD	47		47	BB13
48	INTPOLL IN	48	P WRITE STB	48		48	BB15
49	SI	49	SET INT	49	COM	49	COM
50	COM	50	P READ STB	50	INTACK	50	COM
51	COM						
52	DATAPOLL OUT						
53	SO						
54	COM						
55	COM						
56	DATAPOLL IN						

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
11	0616	41,42	0509	71	0141	91,92	0370	121	0371	141,142	0376
12	0063	43,44	0301	72	0063	93	0231	122	0141	143	0733
13	0424	45	0076	73	0616	94	0839	123,124	0616	144	0616
14	0371	46	0715	74	0231	95,96	0616	125	0616	145	0839
15	0141	47	0370	75	0063	97	0301	126	0435	146,147	0301
17	0715	48	0301	76	0616	98	0844	127	0140	148	0706
18	0327	49	0327	77	0301	99	0755	128	0370	149	0760
19	0141	51	0990	78	0077			129	0760	153	0832
		53	0640	79	0214	101	0328			155	0715
21	0077	55	0376			102	0424	131	0370	159	0756
22	0376	56	0250	81	0370	103	0328	132	0205		
23,24	0294	57,58	0301	82	0616	104	0616	133,134	0839	163	0832
25	0140	59	0374	83	0839	105,106	0367	135	0367	168	0706
27	0424			84	0616	107,108	0301	136,137	0327		
28,29	0370	61,62	0990	86	0839	109	0760	138	0761		
		63	0376	85	0435			139	0755		
31,32	0509	64	0077	87	0301	111	0424				
33,34	0301	65,66	0231	88	0686	112	0141				
35	0261	67,68	0327	89	0760	113	0733				
36	0217	69	0141			114	0231				
37	0328					115,116	0839				
38	0140					117	0140				
39	0301					118	0424				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1205-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1225-22
D	22-1621	B-1251-22
E	ERRATA	NO CHANGE

RATE COUNTER

BAUD RATE MUX

BAUD RATE LATCH

÷2

SAMPLE COUNTER

BAUD RATE MUX

BAUD RATE LATCH

+5V

R16

÷2

SAMPLE COUNTER

CHAR SIZE MUX

(F22) D015
(F22) D014
(F22) D013
(E22) D012
PARAM MUX LOAD (A25)
MR1 (F23)
(D22) D011
(D22) D010
(D22) D009
(D22) D008
(F23) MR2
(C22) D007
(C22) D006
(C22) D005
(B22) D005
(C31) I
(C31) J
(C31) K
(C31) L

CHAR SIZE LATCH

BIT COUNTER

UPPER MOS MEMORY

(A39) J
(A39) I
(B39) L
(A39) K
(A26) PARAM LATCH CLK
(F23) MR2
U103C
U103D
U92A
3 ACTIVE

UPPER CONTROL BUFFER

MRI (F23)

FLAG CONTROL LOGIC

BREAK (B16)
CHAR LOST (C16)
BUFFER FLAG (B12)
U112B
U102B
U92D
TRANSFER UP (B13)
ENABLE (B24)
U132A
U132B
U132C
U122D
U122A
LINE
3 SET BREAK FLAG
U122B
6 SET CHAR LOST FLAG
U122C
8 SET START BIT FLAG
U112C
8 SET BUFFER FLAG

(F16) CLOCK • DP
(C17) LINE
U121B
NOISE RESET

R29
R25
R27
R22
R31
R26
R32
R28
3.16K
-5V

(F16) LOGIC CLK
U142A
1,2,4,5
COUNTER CLOCK

U81A
U71A
SAMPLE CNTR PRESET ENABLE
RIGHT JUSTIFY

STOP
U102F
U102D
U102E
RECEIVE START
(C17) LINE
SHIFT

U101A
DATA MUX ENABLE (E27)
SHIFT

MOS CLOCK GENERATOR

+5V
R43
(G15) DP
U81D
U155A
U153
U163
V3
V2
C78
C79
68PF
R47
R48
31.6
R49
R52
1.96K
1/2W
R51
R50
511
C81
10UF
C80
.01UF
CLOCK Ø1
CLOCK Ø2
(E28) G
(E28) H
CR3
3.16V
-15V

U131B
E5
(E25) PARALLEL CLK ENABLE
(G16) DP
U121A
U112A
PARALLEL DATA CLK (E25)
(A23) DATA
(C17) SEND/RECEIVE
ACTIVE
BREAK
U131C
U121C
LOGIC CLK
9,10,12
U141B
BUFFER CLK (D23)

OLD/NEW BIT SELECT LOGIC

LINE
U132D
(C18) OLD BIT
SHIFT
(D27) SEND BIT
U72B
U111D
U71C
(B24) ECHO
U72A
RIGHT JUSTIFY
LOGIC CLK

R21
U82
QUAD 2-BIT MULTI-PLEXER
SELECT
ENABLE
START CONDITION
START BIT DETECT
NEW BIT (D15) (H17)
U103A
U103B
START
U81C
BCCO
U111B
U81B
RIGHT JUSTIFY
U71B
STOP

START, STOP, AND SHIFT CONTROL LOGIC

30060-60001 TITLE		SHEET 40F4
TERMINAL DATA INTERFACE PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		

I/O DETAILED DIAGRAM SET

DD-509

TERMINAL CONTROL INTERFACE PCA

30061-60001

SERIES 1251

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLLOUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

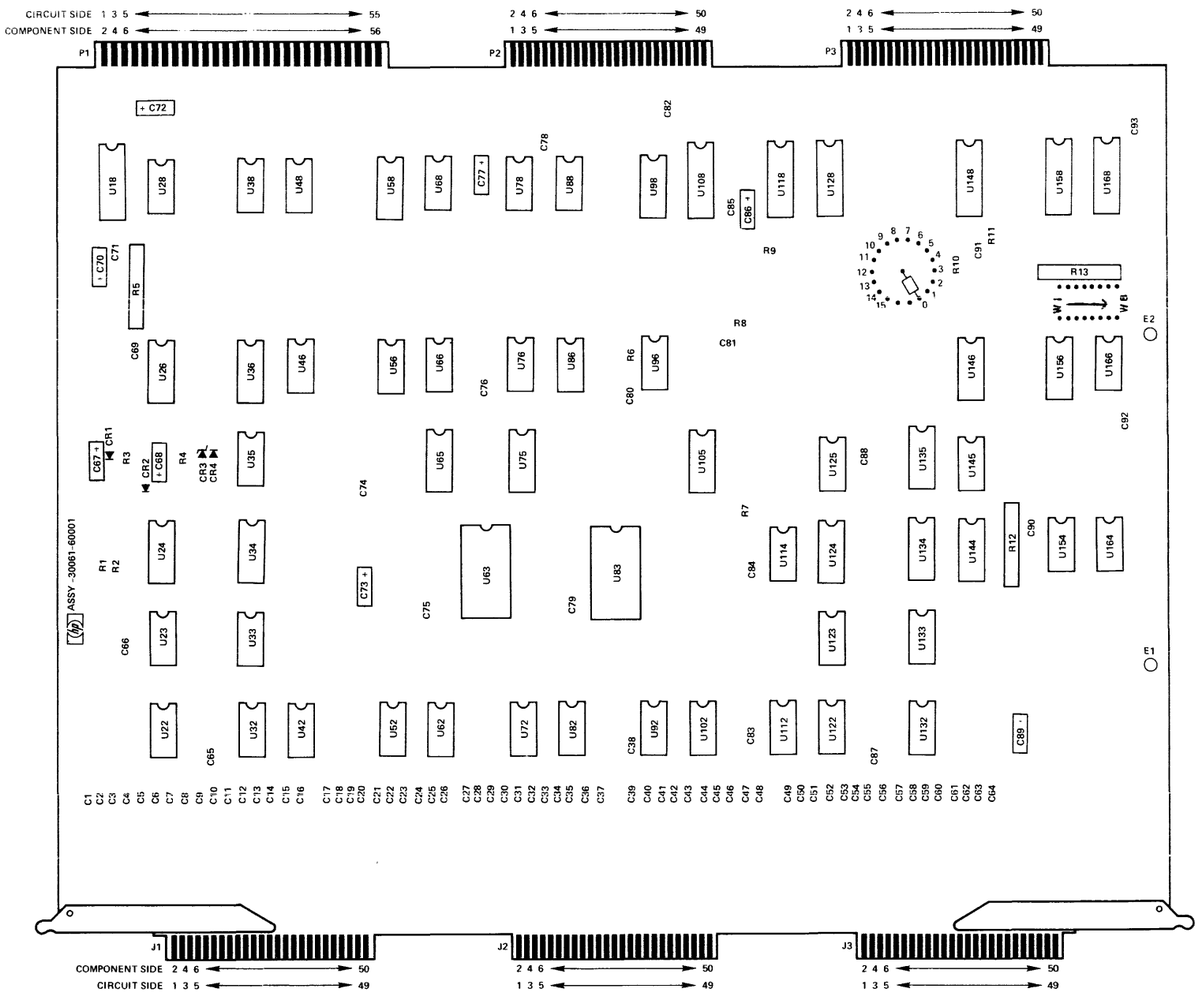
PIN	SIGNAL
1	COM
2	+15V
3	7C2 (CA/CH7)
4	5C1 (CD/SA5)
5	5C2 (CA/CH5)
6	2C1 (CD/SA2)
7	3C2 (CA/CH3)
8	3C1 (CD/SA3)
9	2C2 (CA/CH2)
10	1C1 (CD/SA1)
11	7C1 (CD/SA7)
12	0C1 (CD/SA0)
13	0C2 (CA/CH0)
14	4C1 (CD/SA4)
15	4C2 (CA/CH4)
16	6C1 (CD/SA6)
17	6C2 (CA/CH6)
18	1C2 (CA/CH1)
19	7S1 (CC/SB7)
20	
21	6S1 (CC/SB6)
22	
23	4S1 (CC/SB4)
24	
25	5S1 (CC/SB5)
26	
27	3S1 (CC/SB3)
28	
29	2S1 (CC/SB2)
30	
31	1S1 (CC/SB1)
32	
33	0S1 (CC/SB0)
34	
35	
36	
37	
38	
39	
40	2S2 (CF/CB2)
41	
42	
43	
44	1S2 (CF/CB1)
45	0S2 (CF/CB0)
46	3S2 (CF/CB3)
47	6S2 (CF/CB6)
48	7S2 (CF/CB7)
49	4S2 (CF/CB4)
50	5S2 (CF/CB5)

J2

PIN	SIGNAL
1	11S1 (CF/CB11)
2	10S2 (CF/CB10)
3	14S2 (CF/CB14)
4	15S2 (CF/CB15)
5	
6	
7	
8	
9	9S2 (CF/CB9)
10	8S2 (CF/CB8)
11	
12	12S2 (CF/CB12)
13	13S2 (CF/CB13)
14	
15	
16	
17	15S1 (CC/SB15)
18	
19	14S1 (CC/SB14)
20	
21	13S1 (CC/SB13)
22	
23	12S1 (CC/SB12)
24	
25	10S1 (CC/SB10)
26	
27	11S1 (CC/SB11)
28	
29	9S1 (CC/SB9)
30	
31	8S1 (CC/SB8)
32	
33	15C2 (CA/CH15)
34	10C2 (CA/CH10)
35	13C2 (CA/CH13)
36	15C1 (CD/SA15)
37	11C2 (CA/CH11)
38	13C1 (CD/SA13)
39	14C1 (CD/SA14)
40	11C1 (CD/SA11)
41	9C2 (CA/CH9)
42	10C1 (CD/SA10)
43	8C2 (CA/CH8)
44	8C1 (CD/SA8)
45	12C2 (CA/CH12)
46	9C1 (CD/SA9)
47	14C2 (CA/CH14)
48	12C1 (CD/SA12)
49	COM
50	-15V

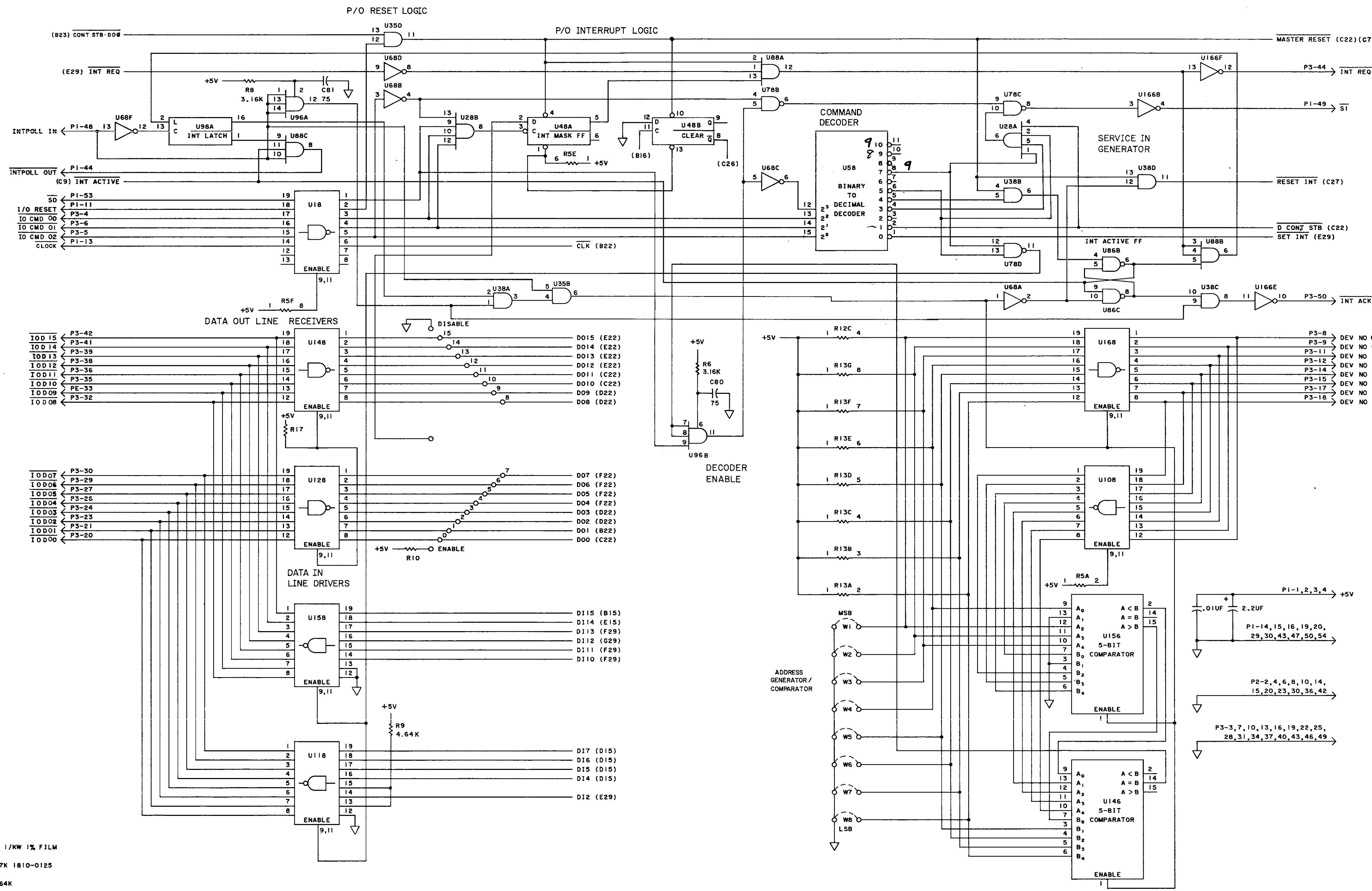
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
18	0760	62	0990	92	0990	144	0628
22,23	0509	63	0640	96	0844	145	0424
24	0833	65	0839	98	0301	146	0706
26	0076	66	0371			148	0760
28	0374	68	0424	102	0990		
				105	0076	154	0617
32,33	0509	72	0990	108	0760	156	0706
34	0833	75	0839	112	0990	158	0756
35	0141	76	0424	114	0205		
36	0715	78	0370	118	0756	164	0239
38	0141					166	0761
		82	0990	122,123	0509	168	0756
42	0990	83	0640	124	0833		
46	0141	86	0370	125	0765		
48	0077	88	0686	128	0760		
52	0990			132,133	0509		
56	0370			134	0833		
58	0214			135	0839		



2212-12

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-A	NO CHANGE	1
D	PPC-B	NO CHANGE	1
E	PPC-C	A-1241-22	1
F	PC-22-1622	A-1251-22	ALL



4. ALL RESISTANCE IS IN OHMS 1/KW 1% FILM
3. ALL RESISTORS IN PACKS 4.7K 1810-0125
2. ALL DISCRETE RESISTORS 4.64K
1. ALL CAPACITORS ARE 470 PICOFARADS.

NOTES: UNLESS OTHERWISE SPECIFIED

30061-60001 TITLE SHEET 1 OF 3

TERMINAL CONTROL INTERFACE PCA

ENGINEER | APPROVED | DATE

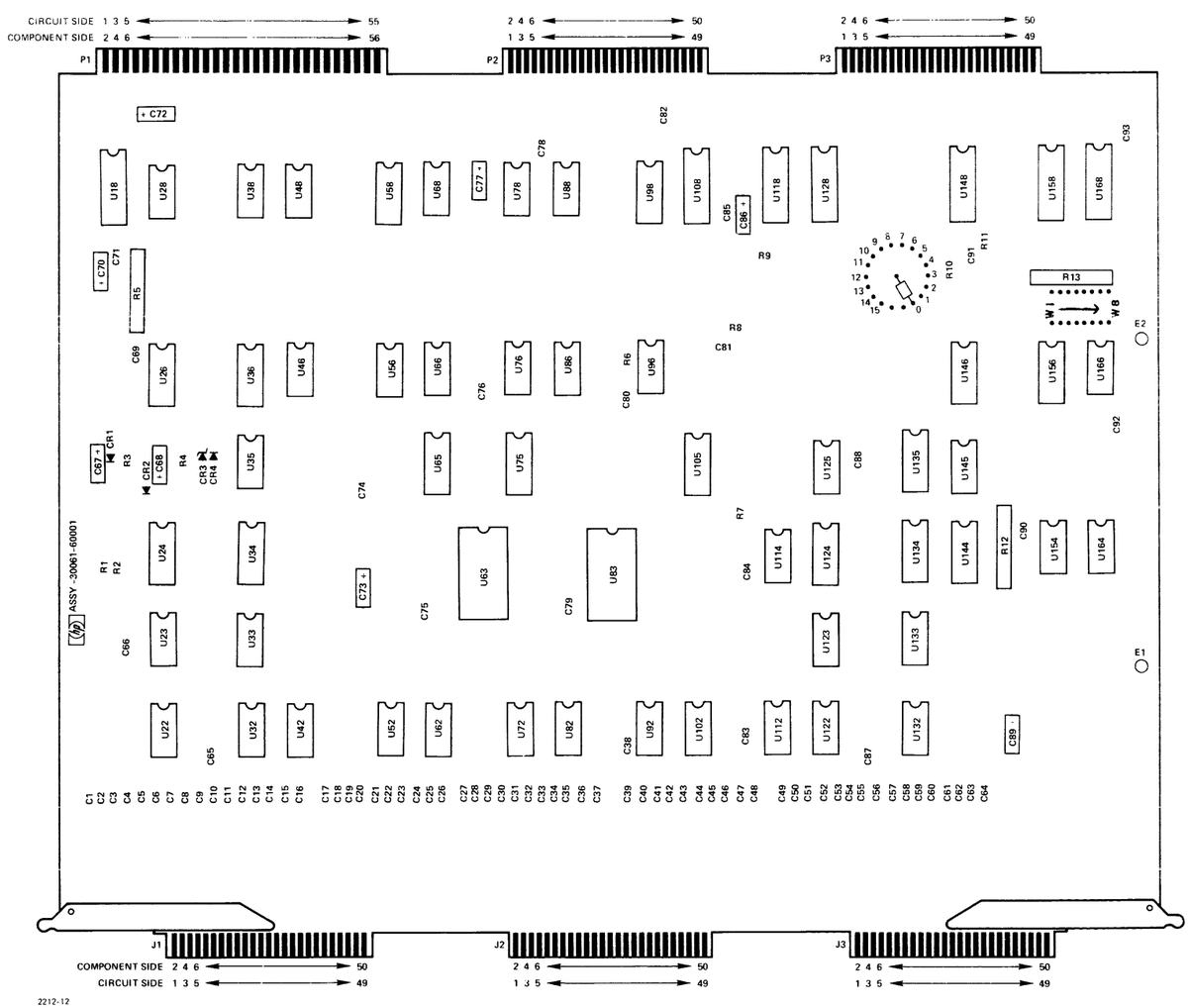
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1	COM	1	11S1 (CF/CB11)
2	+5V	2	COM	2	IOD PE	2	+15V	2	10S2 (CF/CB10)
3	+5V	3	SR CLOCK	3	COM	3	7C2 (CA/CH7)	3	14S2 (CF/CB14)
4	+5V	4	COM	4	IOCMD 00	4	5C1 (CD/SA5)	4	15S2 (CF/CB15)
5	PF WARN	5	DEV END	5	IOCMD 02	5	5C2 (CA/CH5)	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	2C1 (CD/SA2)	6	
7	(SPARE)	7	ACK SR	7	COM	7	3C2 (CA/CH3)	7	
8	(SPARE)	8	COM	8	DEVNO 00	8	3C1 (CD/SA3)	8	
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	2C2 (CA/CH2)	9	9S2 (CF/CB9)
10	COM	10	COM	10	COM	10	1C1 (CD/SA1)	10	8S2 (CF/CB8)
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	7C1 (CD/SA7)	11	
12	COM	12	SIO ENABLE	12	DEVNO 03	12	0C1 (CD/SA0)	12	12S2 (CF/CB12)
13	MCUCLKS	13	EOT	13	COM	13	0C2 (CA/CH0)	13	13S2 (CF/CB13)
14	COM	14	JMP MET	14	DEVNO 04	14	4C1 (CD/SA4)	14	
15	COM	15	COM	15	DEVNO 05	15	4C2 (CA/CH4)	15	
16	COM	16	TOGGLE INXFER	16	COM	16	6C1 (CD/SA6)	16	
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	6C2 (CA/CH6)	17	15S1 (CC/SB15)
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	1C2 (CA/CH1)	18	
19	COM	19	TOGGLE SIO OK	19	COM	19	7S1 (CC/SB7)	19	14S1 (CC/SB14)
20	COM	20	COM	20	IOD 00	20		20	
21	+15V	21	XFER ERROR	21	IOD 01	21	6S1 (CC/SB6)	21	13S1 (CC/SB13)
22	+15V	22	REQ	22	COM	22		22	
23	+15V	23	COM	23	IOD 02	23	4S1 (CC/SB4)	23	12S1 (CC/SB12)
24	+15V	24	SR 15	24	IOD 03	24		24	
25	-15V	25	SR 14	25	COM	25	5S1 (CC/SB5)	25	10S1 (CC/SB10)
26	-15V	26	SR 13	26	IOD 04	26		26	
27	-15V	27	SR 12	27	IOD 05	27	3S1 (CC/SB3)	27	11S1 (CC/SB11)
28	-15V	28	SR 11	28	COM	28		28	
29	COM	29	SR 10	29	IOD 06	29	2S1 (CC/SB2)	29	9S1 (CC/SB9)
30	COM	30	COM	30	IOD 07	30		30	
31	-20V	31	SR 9	31	COM	31	1S1 (CC/SB1)	31	8S1 (CC/SB8)
32	-20V	32	SR 8	32	IOD 08	32		32	
33	-20V	33	SR 7	33	IOD 09	33	0S1 (CC/SB0)	33	15C2 (CA/CH15)
34	-20V	34	SR 6	34	COM	34		34	10C2 (CA/CH10)
35	+20V	35	SR 5	35	IOD 10	35		35	13C2 (CA/CH13)
36	+20V	36	COM	36	IOD 11	36		36	15C1 (CD/SA15)
37	+20V	37	SR 4	37	COM	37		37	11C2 (CA/CH11)
38	+20V	38	SR 3	38	IOD 12	38		38	13C1 (CD/SA13)
39	+20V	39	SR 2	39	IOD 13	39		39	14C1 (CD/SA14)
40	+20V	40	SR 1	40	COM	40	2S2 (CF/CB2)	40	11C1 (CD/SA11)
41	HSREQ	41	SR 0	41	IOD 14	41		41	9C2 (CA/CH9)
42	COM	42	COM	42	IOD 15	42		42	10C1 (CD/SA10)
43	COM	43	P CMD 1	43	COM	43		43	8C2 (CA/CH8)
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44	1S2 (CF/CB1)	44	8C1 (CD/SA8)
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45	0S2 (CF/CB0)	45	12C2 (CA/CH12)
46	COM	46	P CONT STB	46	COM	46	3S2 (CF/CB3)	46	9C1 (CD/SA9)
47	COM	47	RD NEXT WD	47	(SPARE)	47	6S2 (CF/CB6)	47	14C2 (CA/CH14)
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48	7S2 (CF/CB7)	48	12C1 (CD/SA12)
49	SI	49	SET INT	49	COM	49	4S2 (CF/CB4)	49	COM
50	COM	50	P READ STB	50	INTACK	50	5S2 (CF/CB5)	50	-15V
51	COM								
52	DATAPOLL OUT								
53	SO								
54	COM								
55	COM								
56	DATAPOLL IN								

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
18	0760	62	0990	92	0990	144	0628
22,23	0509	63	0640	96	0844	145	0424
24	0833	65	0839	98	0301	146	0706
26	0076	66	0371			148	0760
28	0374	68	0424	102	0990		
				105	0076	154	0617
32,33	0509	72	0990	108	0760	156	0706
34	0833	75	0839	112	0990	158	0756
35	0141	76	0424	114	0205		
36	0715	78	0370	118	0756	164	0239
38	0141					166	0761
		82	0990	122,123	0509	168	0756
42	0990	83	0640	124	0833		
46	0141	86	0370	125	0765		
48	0077	88	0686	128	0760		
52	0990			132,133	0509		
56	0370			134	0833		
58	0214			135	0839		



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	NO CHANGE
D	PPC-B	NO CHANGE
E	PPC-C	A-1241-22
F	PC-22-1622	A-1251-22

(CC/SB0) 0S1 ← J1-33
(CC/SB1) 1S1 ← J1-31
(CC/SB2) 2S1 ← J1-29
(CC/SB3) 3S1 ← J1-27
(CC/SB4) 4S1 ← J1-23
(CC/SB5) 5S1 ← J1-25
(CC/SB6) 6S1 ← J1-21
(CC/SB7) 7S1 ← J1-19
(CC/SB8) 8S1 ← J2-31
(CC/SB9) 9S1 ← J2-29
(CC/SB10) 10S1 ← J2-25
(CC/SB11) 11S1 ← J2-27
(CC/SB12) 12S1 ← J2-23
(CC/SB13) 13S1 ← J2-21
(CC/SB14) 14S1 ← J2-19
(CC/SB15) 15S1 ← J2-17
(CF/CB0) 0S2 ← J1-45
(CF/CB1) 1S2 ← J1-44
(CF/CB2) 2S2 ← J1-40
(CF/CB3) 3S2 ← J1-46
(CF/CB4) 4S2 ← J1-49
(CF/CB5) 5S2 ← J1-50
(CF/CB6) 6S2 ← J1-47
(CF/CB7) 7S2 ← J1-48
(CF/CB8) 8S2 ← J2-10
(CF/CB9) 9S2 ← J2-9
(CF/CB10) 10S2 ← J2-2
(CF/CB11) 11S2 ← J2-1
(CF/CB12) 12S2 ← J2-12
(CF/CB13) 13S2 ← J2-13
(CF/CB14) 14S2 ← J2-3
(CF/CB15) 15S2 ← J2-4

C24 U52D, C23 U52C, C22 U52B, C21 U52A, C19 U42D, C17 U42C, C20 U42A, C18 U42B, C48 U112C, C47 U112D, C45 U112A, C46 U112B, C44 U102C, C43 U102D, C42 U102B, C41 U102A, C28 U62D, C26 U62A, C25 U62B, C27 U62C, C31 U72D, C32 U72C, C29 U72A, C30 U72B, C35 U82D, C36 U82C, C34 U82B, C33 U82A, C39 U92D, C40 U92C, C38 U92B, C37 U92A

U83 16-TO-1 MULTIPLEXER
SI
DI15 (FS)(G22)
DI4 (G5)(G22)
DI5 (G5)(G22)
DI6 (G5)(G22)
DI7 (G5)(G22)

U63 16-TO-1 MULTIPLEXER
S2
DI14 (F5)(G22)

DEVICE CONTROL SIGNAL INPUT SCAN LOGIC

(C29) $\overline{C2}$
(C29) $\overline{C1}$
(D29) A
(D29) B
(A24)
U145C, U114B, U114C, U114D, U114A
U124, U134, U34, U24
DATA IN, LOAD, CLEAR
R12B
+5V
-9.5V +9.5V

J2-43 ← 8C2 (CA/CH8)
J2-41 ← 9C2 (CA/CH9)
J2-34 ← 10C2 (CA/CH10)
J2-37 ← 11C2 (CA/CH11)
J2-45 ← 12C2 (CA/CH12)
J2-35 ← 13C2 (CA/CH13)
J2-47 ← 14C2 (CA/CH14)
J2-33 ← 15C2 (CA/CH15)
J2-44 ← 8C1 (CD/SA8)
J2-46 ← 9C1 (CD/SA9)
J2-42 ← 10C1 (CD/SA10)
J2-40 ← 11C1 (CD/SA11)
J2-48 ← 12C1 (CD/SA12)
J2-38 ← 13C1 (CD/SA13)
J2-39 ← 14C1 (CD/SA14)
J2-36 ← 15C1 (CD/SA15)
J1-13 ← 0C2 (CA/CH0)
J1-18 ← 1C2 (CA/CH1)
J1-9 ← 2C2 (CA/CH2)
J1-7 ← 3C2 (CA/CH3)
J1-15 ← 4C2 (CA/CH4)
J1-5 ← 5C2 (CA/CH5)
J1-17 ← 6C2 (CA/CH6)
J1-3 ← 7C2 (CA/CH7)
J1-12 ← 0C1 (CD/SA0)
J1-10 ← 1C1 (CD/SA1)
J1-6 ← 2C1 (CD/SA2)
J1-8 ← 3C1 (CD/SA3)
J1-14 ← 4C1 (CD/SA4)
J1-4 ← 5C1 (CD/SA5)
J1-16 ← 6C1 (CD/SA6)
J1-11 (CD/SA7) ← 7C1

C54, C53, C51, C52, C55, C50, C56, C49, C62, C63, C61, C59, C64, C58, C60, C57, C13, C16, C11, C10, C8, C7, C9, C6, C5, C4, C2, C3, C14, C1, C15, C12

U122, U123, U132, U133, U32, U22, U23, U33

DEVICE CONTROL SIGNAL OUTPUT LOGIC

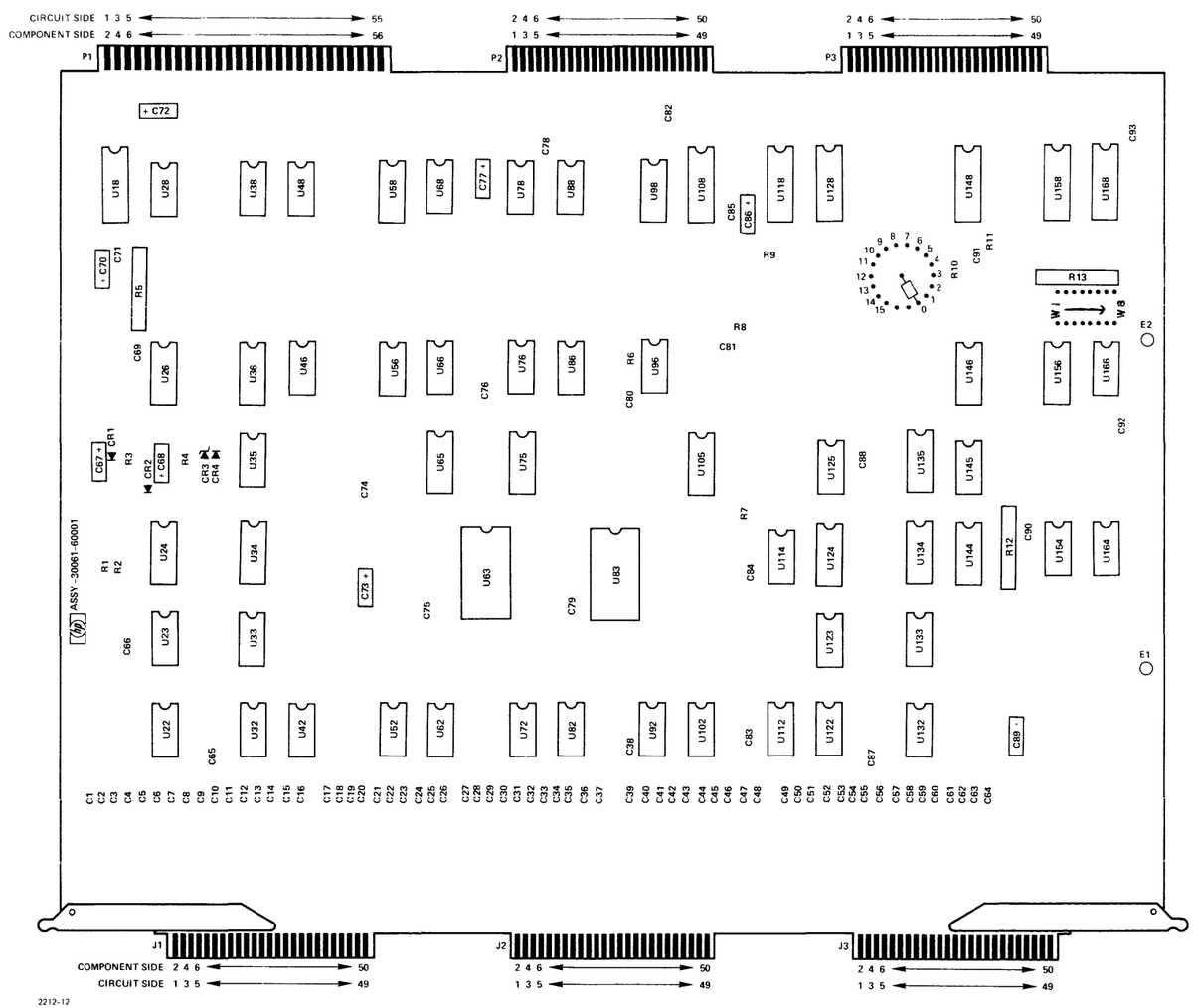
30061-60001	TITLE	SHEET 2 OF 3
TERMINAL CONTROL INTERFACE PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1	COM	1	11S1 (CF/CB11)
2	+5V	2	COM	2	IOD PE	2	+15V	2	10S2 (CF/CB10)
3	+5V	3	SR CLOCK	3	COM	3	7C2 (CA/CH7)	3	14S2 (CF/CB14)
4	+5V	4	COM	4	IOCMD 00	4	5C1 (CD/SA5)	4	15S2 (CF/CB15)
5	PF WARN	5	DEV END	5	IOCMD 02	5	5C2 (CA/CH5)	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	2C1 (CD/SA2)	6	
7	(SPARE)	7	ACK SR	7	COM	7	3C2 (CA/CH3)	7	
8	(SPARE)	8	COM	8	DEVNO 00	8	3C1 (CD/SA3)	8	
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	2C2 (CA/CH2)	9	9S2 (CF/CB9)
10	COM	10	COM	10	COM	10	1C1 (CD/SA1)	10	8S2 (CF/CB8)
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	7C1 (CD/SA7)	11	
12	COM	12	SIO ENABLE	12	DEVNO 03	12	0C1 (CD/SA0)	12	12S2 (CF/CB12)
13	MCUCLKS	13	EOT	13	COM	13	0C2 (CA/CH0)	13	13S2 (CF/CB13)
14	COM	14	JMP MET	14	DEVNO 04	14	4C1 (CD/SA4)	14	
15	COM	15	COM	15	DEVNO 05	15	4C2 (CA/CH4)	15	
16	COM	16	TOGGLE INXFER	16	COM	16	6C1 (CD/SA6)	16	
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	6C2 (CA/CH6)	17	15S1 (CC/SB15)
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	1C2 (CA/CH1)	18	
19	COM	19	TOGGLE SIO OK	19	COM	19	7S1 (CC/SB7)	19	14S1 (CC/SB14)
20	COM	20	COM	20	IOD 00	20		20	
21	+15V	21	XFER ERROR	21	IOD 01	21	6S1 (CC/SB6)	21	13S1 (CC/SB13)
22	+15V	22	REQ	22	COM	22		22	
23	+15V	23	COM	23	IOD 02	23	4S1 (CC/SB4)	23	12S1 (CC/SB12)
24	+15V	24	SR 15	24	IOD 03	24		24	
25	-15V	25	SR 14	25	COM	25	5S1 (CC/SB5)	25	10S1 (CC/SB10)
26	-15V	26	SR 13	26	IOD 04	26		26	
27	-15V	27	SR 12	27	IOD 05	27	3S1 (CC/SB3)	27	11S1 (CC/SB11)
28	-15V	28	SR 11	28	COM	28		28	
29	COM	29	SR 10	29	IOD 06	29	2S1 (CC/SB2)	29	9S1 (CC/SB9)
30	COM	30	COM	30	IOD 07	30		30	
31	-20V	31	SR 9	31	COM	31	1S1 (CC/SB1)	31	8S1 (CC/SB8)
32	-20V	32	SR 8	32	IOD 08	32		32	
33	-20V	33	SR 7	33	IOD 09	33	0S1 (CC/SB0)	33	15C2 (CA/CH15)
34	-20V	34	SR 6	34	COM	34		34	10C2 (CA/CH10)
35	+20V	35	SR 5	35	IOD 10	35		35	13C2 (CA/CH13)
36	+20V	36	COM	36	IOD 11	36		36	15C1 (CD/SA15)
37	+20V	37	SR 4	37	COM	37		37	11C2 (CA/CH11)
38	+20V	38	SR 3	38	IOD 12	38		38	13C1 (CD/SA13)
39	+20V	39	SR 2	39	IOD 13	39		39	14C1 (CD/SA14)
40	+20V	40	SR 1	40	COM	40	2S2 (CF/CB2)	40	11C1 (CD/SA11)
41	HSREQ	41	SR 0	41	IOD 14	41		41	9C2 (CA/CH9)
42	COM	42	COM	42	IOD 15	42		42	10C1 (CD/SA10)
43	COM	43	P CMD 1	43	COM	43		43	8C2 (CA/CH8)
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44	1S2 (CF/CB1)	44	8C1 (CD/SA8)
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45	0S2 (CF/CB0)	45	12C2 (CA/CH12)
46	COM	46	P CONT STB	46	COM	46	3S2 (CF/CB3)	46	9C1 (CD/SA9)
47	COM	47	RD NEXT WD	47	(SPARE)	47	6S2 (CF/CB6)	47	14C2 (CA/CH14)
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48	7S2 (CF/CB7)	48	12C1 (CD/SA12)
49	SI	49	SET INT	49	COM	49	4S2 (CF/CB4)	49	COM
50	COM	50	P READ STB	50	INTACK	50	5S2 (CF/CB5)	50	-15V
51	COM								
52	DATAPOLL OUT								
53	SO								
54	COM								
55	COM								
56	DATAPOLL IN								

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
18	0760	62	0990	92	0990	144	0628
22,23	0509	63	0640	96	0844	145	0424
24	0833	65	0839	98	0301	146	0706
26	0076	66	0371			148	0760
28	0374	68	0424	102	0990		
				105	0076	154	0617
32,33	0509	72	0990	108	0760	156	0706
34	0833	75	0839	112	0990	158	0756
35	0141	76	0424	114	0205		
36	0715	78	0370	118	0756	164	0239
38	0141					166	0761
		82	0990	122,123	0509	168	0756
42	0990	83	0640	124	0833		
46	0141	86	0370	125	0765		
48	0077	88	0686	128	0760		
52	0990			132,133	0509		
56	0370			134	0833		
58	0214			135	0839		



2212-12

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	NO CHANGE
D	PPC-B	NO CHANGE
E	PPC-C	A-1241-22
F	PC-22-1622	A-1251-22

P/O RESET LOGIC

(B16) A
(E5) DO0
U86D
CONT STB-DO0 (A3)
STATUS CLEAR
U48B
+5V

CONTROL DATA HOLDING REGISTER

(C4) CLK
(E5) DO1
(D5) DO11
(D5) DO10
(C7) D CONT STB
(A8) MASTER RESET
U145A
U75
4-BIT REGISTER
CLOCK
CLEAR

(E5) DO3
(E5) DO2
(D5) DO8
(D5) DO9
U76A
U65
4-BIT REGISTER
UPDATE
SCAN
SCAN
EC2
EC1

(D5) DO14
(D5) DO15
(D5) DO12
(D5) DO13
U135
4-BIT REGISTER
S2
S1
ES2
ES1

CHANNEL COUNTER

(E5) DO7
(E5) DO6
(E5) DO5
(E5) DO4
(C29) C
U125
4-BIT COUNTER
CLOCK 1
CLOCK 2
LOAD CLEAR

(D15) DI7
(D15) DI6
(D15) DI5
(D15) DI4
(B15) DI15
(E15) DI14

R7
+5V
U105A
CLOCK ÷2A
U105B
CLOCK ÷2B

CONTROL LOGIC

U56D
U66A
U56A
U56B
U56C
U46A
U46B
U46C
U76B
R3C
+5V
U46D
U26A
SYNC 1
U26B
SYNC 2

STATUS STORAGE

U144
64 BIT RAM
SELECT
WRITE
R11D
R11E
R11G
R12F
+5V

STATUS DECODE LOGIC

U154B
U154C
U164B
U164A
U164C
U164D
U145E
U145F
DI11 (F5)
DI10 (F5)
DI13 (F5)
DI12 (F5)

+15V
CR2
R2
1K 1/4W±5%
J1-2 +15V
R3 120 2W
CR1 5.11V
+9.5V
C67 2.2UF
J1-1 COM
J2-49 COM
C68 2.2UF
-9.5V
R4 120 2W
CR3 5.11V
-15V
CR4
R1
1K 1/4W±5%
J2-50 -15V

C1 (C16)
C2 (B16)
C (F22)
(B9) RESET INT
U35A
B (E16)
A (D16)

A STATUS

R5B
+5V
U36A
CHANGE FF
U36B
INT REQ FF
SET INT (C7)
DI2 (G5)
INT REQ (B5)

P/O INTERRUPT LOGIC

30061-60001	TITLE	SHEET 3 OF 3
TERMINAL CONTROL INTERFACE PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

I/O DETAILED DIAGRAM SET

DD-600

DISC FILE READ/WRITE PCA
30202-60001
SERIES 1251
1324

REV C

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLL OUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

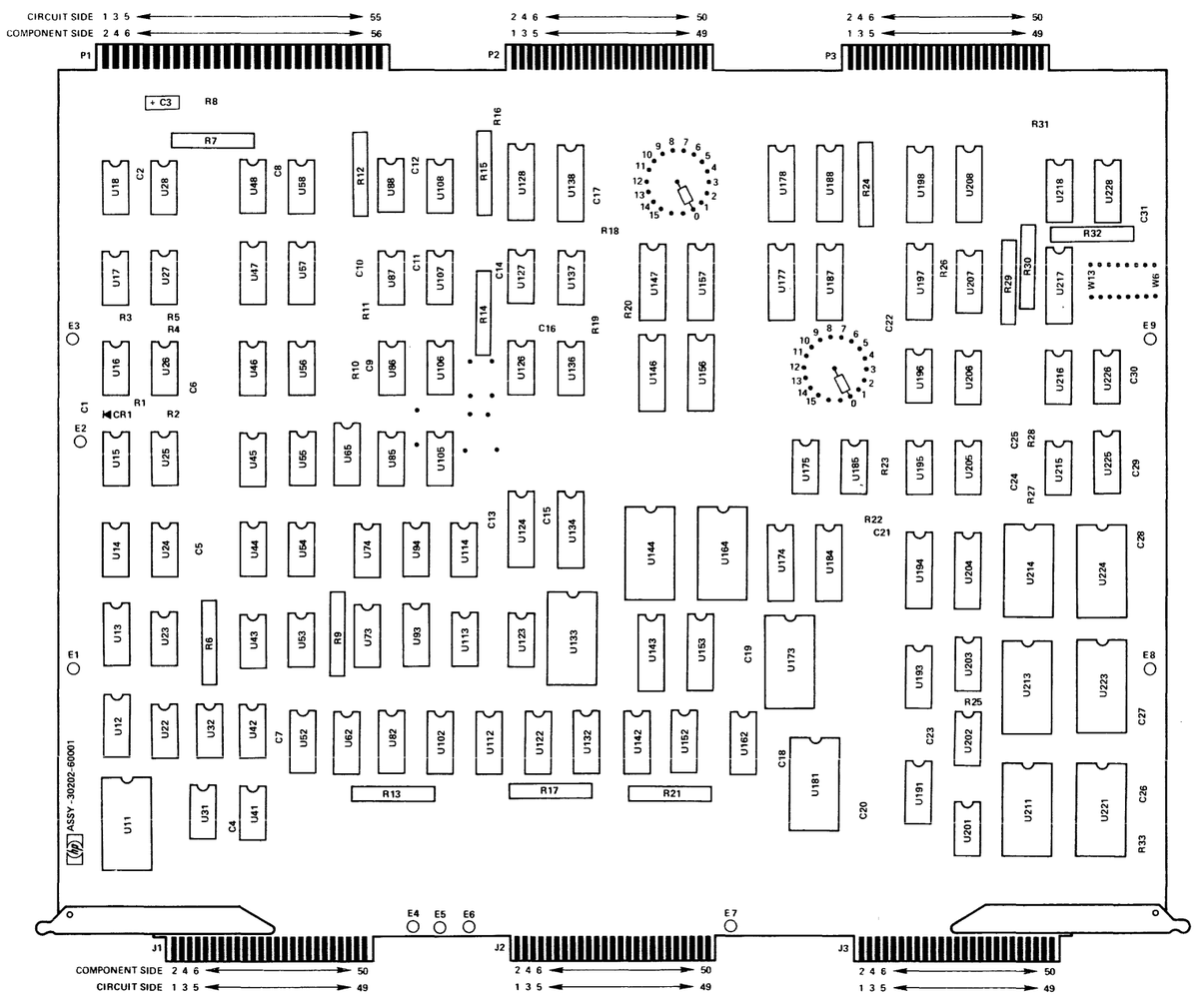
PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	COM
2	COM
3	CLK RST
4	NOT USED
5	ALTCLK
6	DISP
7	A=CKCTL
8	—
9	ERA 7
10	—
11	LD ERA
12	ERA 11
13	ERA 3
14	ERA 2
15	ERA 10
16	ERA 6
17	AT 0
18	CTL 1= ENT012
19	AT 3
20	AT 1
21	AT 2
22	—
23	CTL2= ENT3
24	UB
25	AM
26	LB
27	AS 2
28	AS 3
29	AS 1
30	AS 0
31	V
32	W
33	T
34	U
35	ERA 1
36	—
37	ERA 5
38	ERA 9
39	ERA 4
40	ERA 0
41	ERA 8
42	—
43	NOT USED
44	NOT USED
45	Z
46	LDREG
47	X
48	Y
49	COM
50	COM

IC INDEX

U	18XX	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
	1816-	11	0495	43	0511	86	0239	128	0759	181	0742	216	0371
62	0231	12,13	0715	44	0371	87	0370	133	0742	184	0755	217	0756
82	0232	14	0371	45	0373	88	0424	134	0756	185	0370	218	0706
102	0232	15	0054	46	0371			136	0424	187,188	0755	221,223	0726
112	0234	16	0511	47	0715	93	0715	137	0370			224	0742
122	0235	17	0371	48	0077	94	0370	138	0759	194	0755	225	0301
132	0236	18	0370							195	0077	226	0374
142	0237			53,54	0512	105	0205	143	0756	196	0141	228	0706
152	0238	22	0054	55	0141	106	0141	144	0742	197,198	0760		
162	0239	23	0077	56	0512	107	0370	146,147	0755				
191,193	1810-	24	0424	57	0715	108	0761			201–203	0175		
	0037	25	0141	58	0686			153	0756	204	0755		
		26	0902			113	0205	156	0760	205	0686		
		27,28	0141	65	0231	114	0141	157	0759	206	0424		
										207	0491		
		31,32	0902	73	0715	123	0205	173	0742	208	0756		
				74	0512	124	0755	174	0755	211,213	0742		
		41	0239			126	0371	177	0760	214			
		42	0077	85	0379	127	0141	178	0759	215	0844		



NOTES UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE IS IN OHMS
2. ALL RESISTOR PACKS ARE 4.7K
3. ALL CAPACITANCE IS IN PICOFARADS

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	22-1588	A-1244-22	ALL
D	22-1627	A-1251-22	ALL
E	22-1668	A-1307	ALL
F	22-1713	A-1324	3

30202-60001 TITLE SHEET 1 OF 4
DISC FILE READ/WRITE PCA
ENGINEER | APPROVED | DATE
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLL OUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

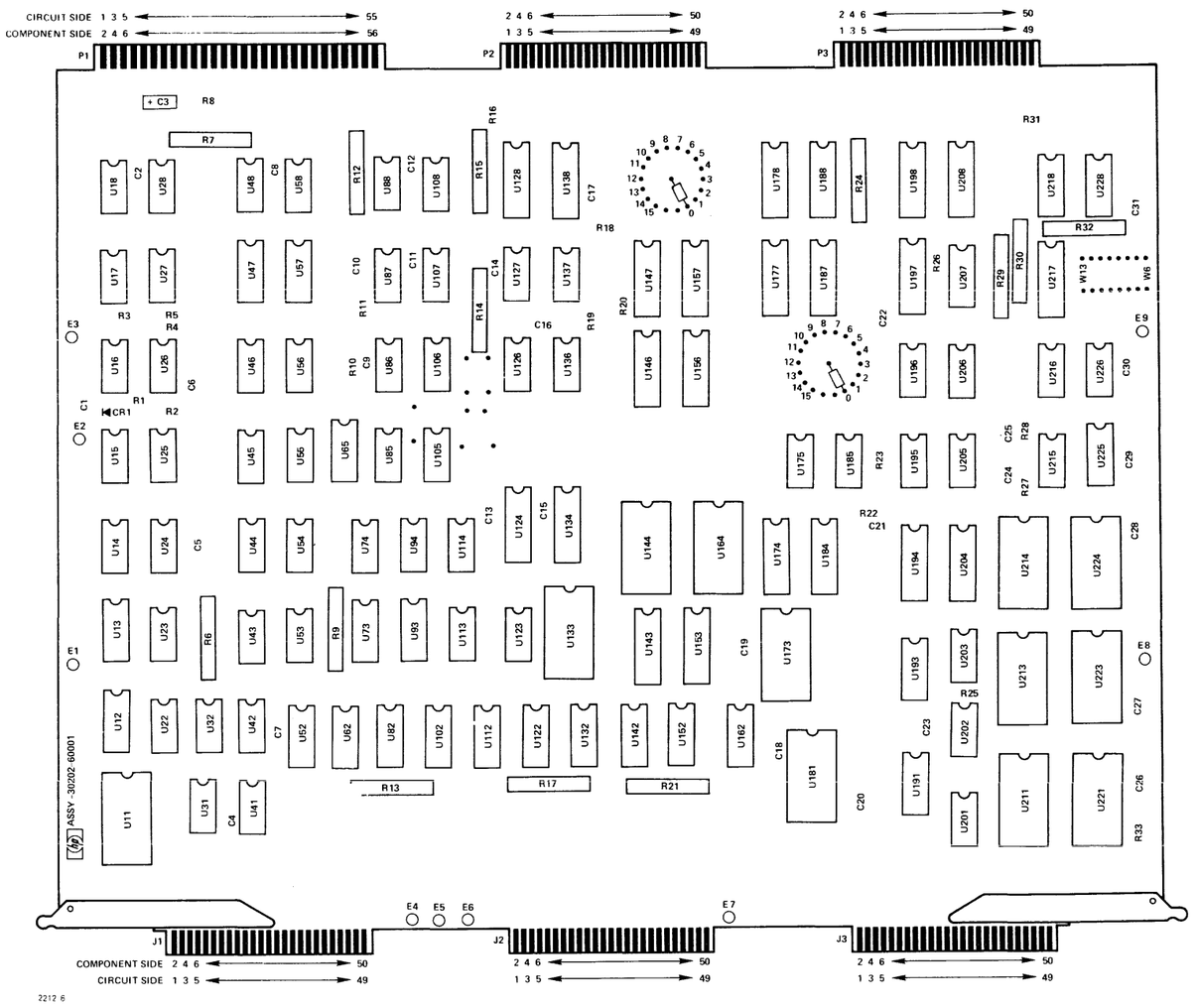
PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

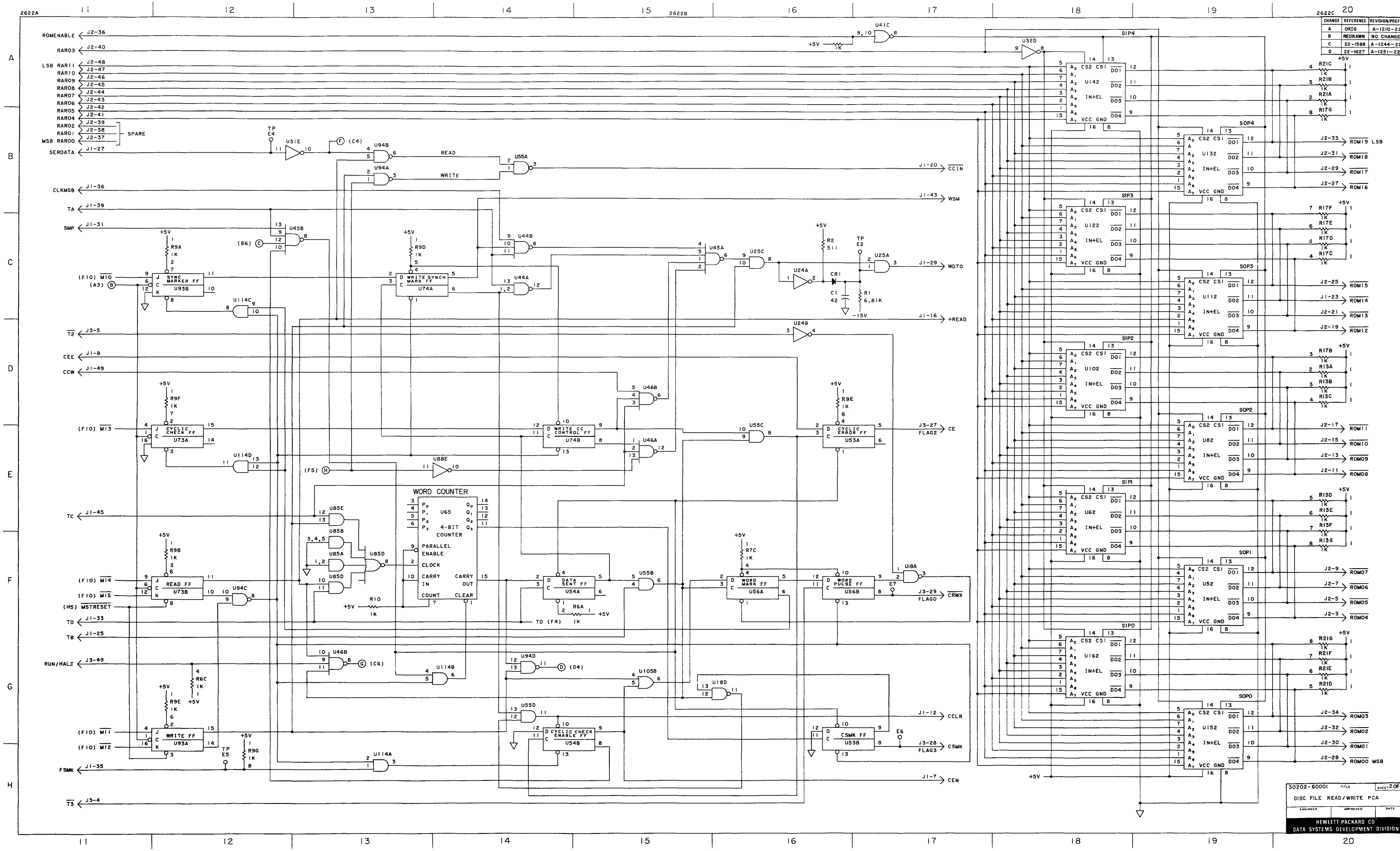
PIN	SIGNAL
1	COM
2	COM
3	CLK RST
4	NOT USED
5	ALTCLK
6	DISP
7	A=CKCTL
8	—
9	ERA 7
10	—
11	LD ERA
12	ERA 11
13	ERA 3
14	ERA 2
15	ERA 10
16	ERA 6
17	AT 0
18	CTL 1= ENT012
19	AT 3
20	AT 1
21	AT 2
22	—
23	CTL2= ENT3
24	UB
25	AM
26	LB
27	AS 2
28	AS 3
29	AS 1
30	AS 0
31	V
32	W
33	T
34	U
35	ERA 1
36	—
37	ERA 5
38	ERA 9
39	ERA 4
40	ERA 0
41	ERA 8
42	—
43	NOT USED
44	NOT USED
45	Z
46	LDREG
47	X
48	Y
49	COM
50	COM

IC INDEX

U	18XX	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
	1816-	11	0495	43	0511	86	0239	128	0759	181	0742	216	0371
62	0231	12,13	0715	44	0371	87	0370	133	0742	184	0755	217	0756
82	0232	14	0371	45	0373	88	0424	134	0756	185	0370	218	0706
102	0232	15	0054	46	0371			136	0424	187,188	0755	221,223	0726
112	0234	16	0511	47	0715	93	0715	137	0370			224	0742
122	0235	17	0371	48	0077	94	0370	138	0759	194	0755	225	0301
132	0236	18	0370							195	0077	226	0374
142	0237			53,54	0512	105	0205	143	0756	196	0141	228	0706
152	0238	22	0054	55	0141	106	0141	144	0742	197,198	0760		
162	0239	23	0077	56	0512	107	0370	146,147	0755				
191,193	1810-	24	0424	57	0715	108	0761			201–203	0175		
	0037	25	0141	58	0686			153	0756	204	0755		
		26	0902			113	0205	156	0760	205	0686		
		27,28	0141	65	0231	114	0141	157	0759	206	0424		
										207	0491		
		31,32	0902	73	0715	123	0205	173	0742	208	0756		
				74	0512	124	0755	174	0755	211,213	0742		
		41	0239			126	0371	177	0760	214			
		42	0077	85	0379	127	0141	178	0759	215	0844		



2212 6



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1588	A-1244-22
D	22-1627	A-1251-22

30202-60001 TITLE SHEET 2 OF 4

DISC FILE READ/WRITE PCA

ENGINEER APPROVED DATE

HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLL OUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

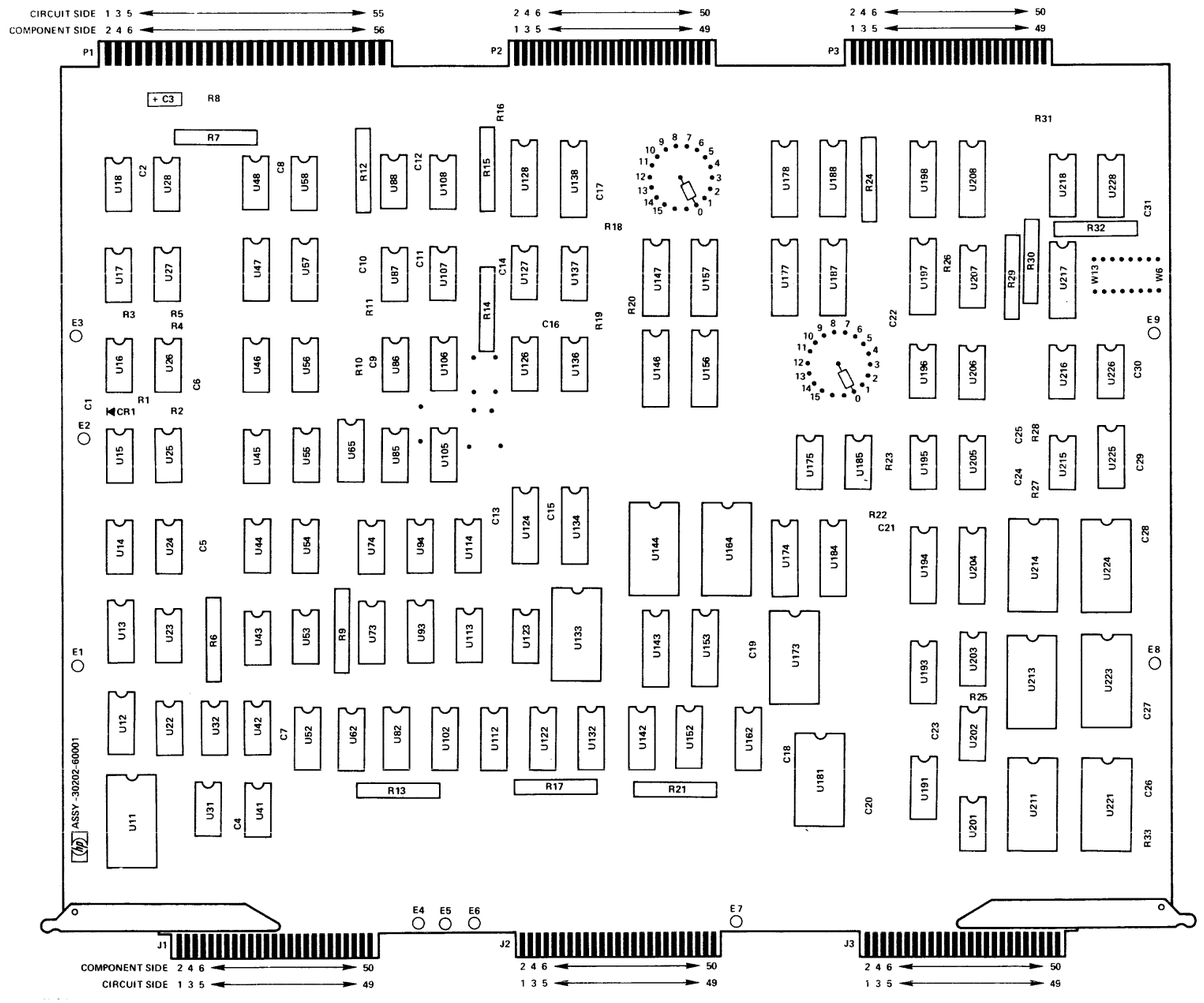
PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	COM
2	COM
3	CLK RST
4	NOT USED
5	ALTCLK
6	DISP
7	A=CKCTL
8	—
9	ERA 7
10	—
11	LD ERA
12	ERA 11
13	ERA 3
14	ERA 2
15	ERA 10
16	ERA 6
17	AT 0
18	CTL 1= ENT012
19	AT 3
20	AT 1
21	AT 2
22	—
23	CTL2= ENT3
24	UB
25	AM
26	LB
27	AS 2
28	AS 3
29	AS 1
30	AS 0
31	V
32	W
33	T
34	U
35	ERA 1
36	—
37	ERA 5
38	ERA 9
39	ERA 4
40	ERA 0
41	ERA 8
42	—
43	NOT USED
44	NOT USED
45	Z
46	LDREG
47	X
48	Y
49	COM
50	COM

IC INDEX

U	18XX	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
	1816-	11	0495	43	0511	86	0239	128	0759	181	0742	216	0371
62	0231	12,13	0715	44	0371	87	0370	133	0742	184	0755	217	0756
82	0232	14	0371	45	0373	88	0424	134	0756	185	0370	218	0706
102	0232	15	0054	46	0371			136	0424	187,188	0755	221,223	0726
112	0234	16	0511	47	0715	93	0715	137	0370			224	0742
122	0235	17	0371	48	0077	94	0370	138	0759	194	0755	225	0301
132	0236	18	0370							195	0077	226	0374
142	0237			53,54	0512	105	0205	143	0756	196	0141	228	0706
152	0238	22	0054	55	0141	106	0141	144	0742	197,198	0760		
162	0239	23	0077	56	0512	107	0370	146,147	0755				
191,193	1810-	24	0424	57	0715	108	0761			201–203	0175		
	0037	25	0141	58	0686			153	0756	204	0755		
		26	0902			113	0205	156	0760	205	0686		
		27,28	0141	65	0231	114	0141	157	0759	206	0424		
										207	0491		
		31,32	0902	73	0715	123	0205	173	0742	208	0756		
				74	0512	124	0755	174	0755	211,213	0742		
		41	0239			126	0371	177	0760	214			
		42	0077	85	0379	127	0141	178	0759	215	0844		



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1588	A-1244-22
D	22-1627	A-1251-22

INPUT RECEIVER

IOP OUTPUT DATA BUFFER

CHANNEL OUTPUT DATA BUFFER

COMMAND DECODER

DEVICE NO. (PREWIRED)

DEVICE NO. DIRECT BUFFER

DEVICE NO. COMPARATOR

PRIORITY

30202-60001 TITLE SHEET 3 OF 4

DISC FILE READ/WRITE PCA

ENGINEER | APPROVED | DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	PF WARN
6	ENTIMER
7	(SPARE)
8	(SPARE)
9	PWR ON
10	COM
11	IORESET
12	COM
13	MCUCLKS
14	COM
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	HSREQ
42	COM
43	COM
44	INTPOLL OUT
45	(SPARE)
46	COM
47	COM
48	INTPOLL IN
49	SI
50	COM
51	COM
52	DATAPOLL OUT
53	SO
54	COM
55	COM
56	DATAPOLL IN

P2

PIN	SIGNAL
1	CHAN SO
2	COM
3	SR CLOCK
4	COM
5	DEV END
6	COM
7	ACK SR
8	COM
9	CHAN ACK
10	COM
11	DEVNO DB
12	SIO ENABLE
13	EOT
14	JMP MET
15	COM
16	TOGGLE INXFER
17	TOGGLE SR
18	TOGGLE OUTXFER
19	TOGGLE SIO OK
20	COM
21	XFER ERROR
22	REQ
23	COM
24	SR 15
25	SR 14
26	SR 13
27	SR 12
28	SR 11
29	SR 10
30	COM
31	SR 9
32	SR 8
33	SR 7
34	SR 6
35	SR 5
36	COM
37	SR 4
38	SR 3
39	SR 2
40	SR 1
41	SR 0
42	COM
43	P CMD 1
44	SET JMP
45	P STATUS STB
46	P CONT STB
47	RD NEXT WD
48	P WRITE STB
49	SET INT
50	P READ STB

P3

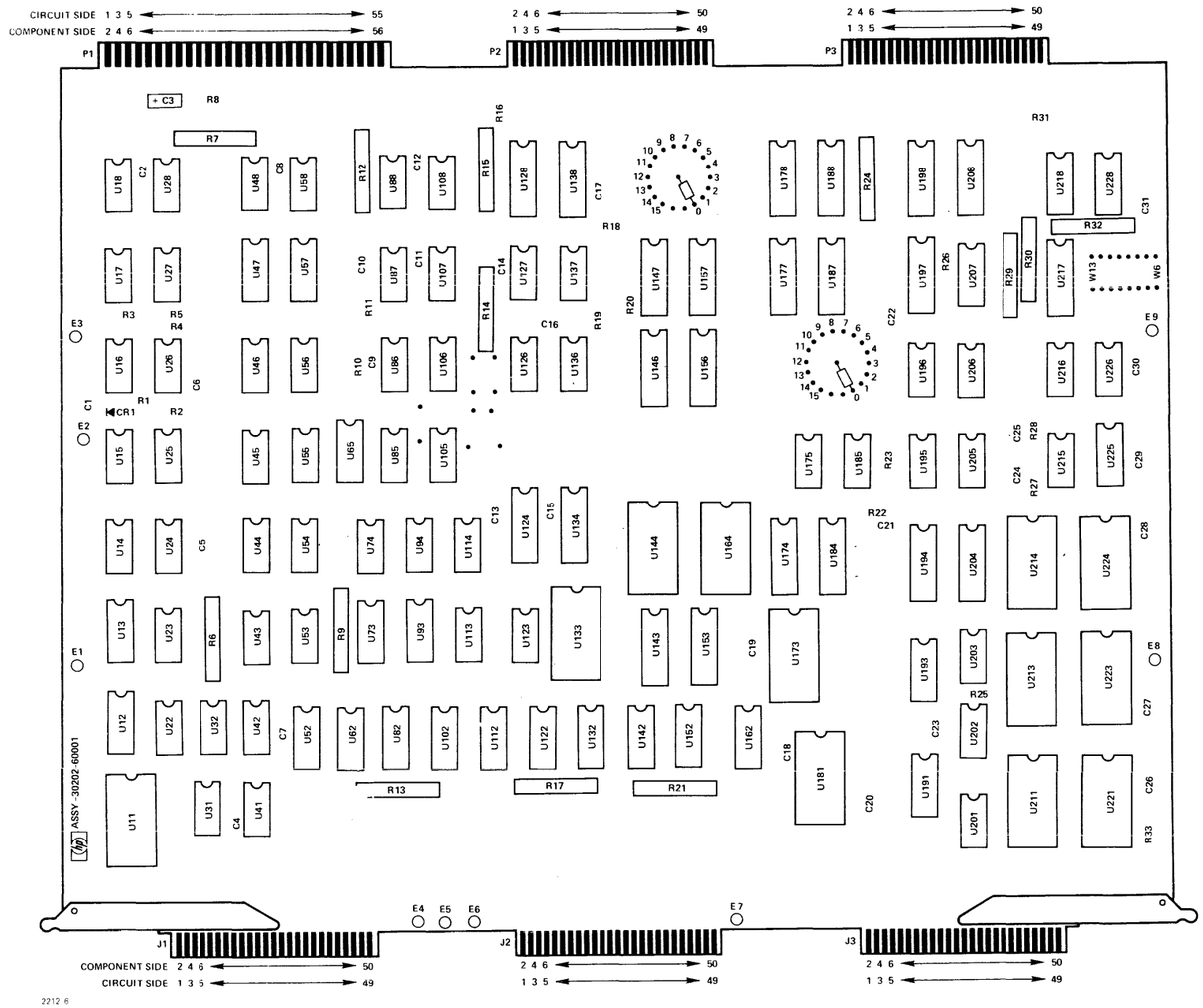
PIN	SIGNAL
1	IODPRTY
2	IOD PE
3	COM
4	IOCMD 00
5	IOCMD 02
6	IOCMD 01
7	COM
8	DEVNO 00
9	DEVNO 01
10	COM
11	DEVNO 02
12	DEVNO 03
13	COM
14	DEVNO 04
15	DEVNO 05
16	COM
17	DEVNO 06
18	DEVNO 07
19	COM
20	IOD 00
21	IOD 01
22	COM
23	IOD 02
24	IOD 03
25	COM
26	IOD 04
27	IOD 05
28	COM
29	IOD 06
30	IOD 07
31	COM
32	IOD 08
33	IOD 09
34	COM
35	IOD 10
36	IOD 11
37	COM
38	IOD 12
39	IOD 13
40	COM
41	IOD 14
42	IOD 15
43	COM
44	INTREQ
45	(SPARE)
46	COM
47	(SPARE)
48	(SPARE)
49	COM
50	INTACK

J1

PIN	SIGNAL
1	COM
2	COM
3	CLK RST
4	NOT USED
5	ALTCLK
6	DISP
7	A=CKCTL
8	—
9	ERA 7
10	—
11	LD ERA
12	ERA 11
13	ERA 3
14	ERA 2
15	ERA 10
16	ERA 6
17	AT 0
18	CTL 1= ENT012
19	AT 3
20	AT 1
21	AT 2
22	—
23	CTL2= ENT3
24	UB
25	AM
26	LB
27	AS 2
28	AS 3
29	AS 1
30	AS 0
31	V
32	W
33	T
34	U
35	ERA 1
36	—
37	ERA 5
38	ERA 9
39	ERA 4
40	ERA 0
41	ERA 8
42	—
43	NOT USED
44	NOT USED
45	Z
46	LDREG
47	X
48	Y
49	COM
50	COM

IC INDEX

U	18XX	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-
	1816-	11	0495	43	0511	86	0239	128	0759	181	0742	216	0371
62	0231	12,13	0715	44	0371	87	0370	133	0742	184	0755	217	0756
82	0232	14	0371	45	0373	88	0424	134	0756	185	0370	218	0706
102	0232	15	0054	46	0371			136	0424	187,188	0755	221,223	0726
112	0234	16	0511	47	0715	93	0715	137	0370			224	0742
122	0235	17	0371	48	0077	94	0370	138	0759	194	0755	225	0301
132	0236	18	0370							195	0077	226	0374
142	0237			53,54	0512	105	0205	143	0756	196	0141	228	0706
152	0238	22	0054	55	0141	106	0141	144	0742	197,198	0760		
162	0239	23	0077	56	0512	107	0370	146,147	0755				
191,193	1810-	24	0424	57	0715	108	0761			201–203	0175		
	0037	25	0141	58	0686			153	0756	204	0755		
		26	0902			113	0205	156	0760	205	0686		
		27,28	0141	65	0231	114	0141	157	0759	206	0424		
										207	0491		
		31,32	0902	73	0715	123	0205	173	0742	208	0756		
				74	0512	124	0755	174	0755	211,213	0742		
		41	0239			126	0371	177	0760	214			
		42	0077	85	0379	127	0141	178	0759	215	0844		



2212 6

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1588	A-1244-22
D	22-1627	A-1251-22

COMMAND RECEIVER

STATUS REGITER

STATUS REGISTER DRIVERS

DEVICE DRT ADDRESS REGISTER

CHANNEL INPUT DATA BUFFER

IOP INPUT DATA BUFFER

30202-60001	SHEET 4 OF 4
DISC FILE READ/WRITE PCA	
ENGINEER / APPROVED / DATE	
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION	

I/O DETAILED DIAGRAM SET

DD-601

DISC FILE BUS PCA
30202-60002
SERIES 1236

REV C

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	—
6	—
7	—
8	—
9	PWR ON
10	—
11	—
12	—
13	—
14	—
15	COM
16	COM
17	—
18	—
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	—
32	—
33	—
34	—
35	—
36	—
37	—
38	—
39	—
40	—
41	—
42	—
43	—
44	—
45	—
46	—
47	—
48	—
49	—
50	—
51	—
52	—
53	—
54	—
55	—
56	—

P2

PIN	SIGNAL
1	MOD SEL (SPARES)
2	COM
3	MOD SEL 7
4	COM
5	MOD SEL 6
6	COM
7	MOD SEL 4
8	COM
9	MOD SEL 5
10	COM
11	MOD SEL 3
12	COM
13	MOD SEL 2
14	COM
15	MOD SEL 0
16	COM
17	MOD SEL 1
18	COM
19	SET HD/DIR
20	COM
21	SET DIFF
22	COM
23	SET CYL
24	COM
25	CONTR
26	COM
27	BUS 256
28	COM
29	BUS 1
30	COM
31	BUS 2
32	COM
33	BUS 8
34	COM
35	BUS 4
36	COM
37	BUS 16
38	COM
39	BUS 128
40	COM
41	BUS 32
42	COM
43	BUS 64
44	COM
45	—
46	COM
47	SEQ PICK
48	CLK OUT
49	TRACE SEQ PICK
50	CPU HLT

P3

PIN	SIGNAL
1	GAT7
2	GAT(SPARE)
3	COM
4	GAT6
5	GAT5
6	COM
7	COM
8	GAT4
9	GAT3
10	COM
11	GAT2
12	COM
13	GAT1
14	COM
15	GAT0
16	COM
17	200TPI
18	COM
19	WRCR SENSE
20	COM
21	PACK CHG
22	COM
23	END OF CYL
24	COM
25	SEEK INCOMPLETE
26	COM
27	FILE UNSAFE
28	COM
29	ONLINE
30	COM
31	BUSY
32	COM
33	INDEX
34	COM
35	CAR 1
36	COM
37	CAR 2
38	COM
39	CAR 4
40	COM
41	CAR 8
42	COM
43	CAR 16
44	COM
45	CAR 32
46	COM
47	CAR 64
48	COM
49	CAR 128
50	CAR 256

J1

PIN	SIGNAL
1	COM
2	UNIR(4)
3	COM
4	UNIR(2)
5	COM
6	UNIR(1)
7	CEN
8	CEE
9	COM
10	FCE
11	COM
12	CCLR
13	COM
14	COM
15	DRIVE BUSY
16	+READ
17	SEEK INCOMPLETE
18	COM
19	UNSAFE
20	CCIN
21	ONLINE
22	COM
23	PACK CHG
24	200TPI
25	TB
26	COM
27	SEP DATA
28	COM
29	WRITE DATA (70)
30	COM
31	SMP
32	COM
33	TD
34	COM
35	—
36	CLK
37	COM
38	D10
39	TA
40	COM
41	D11
42	D12
43	WSM
44	D15
45	TC
46	COM
47	D14
48	D13
49	—
50	COM

J2

PIN	SIGNAL
1	COM
2	WRITE 0
3	COM
4	READ 0
5	COM
6	SEL MOD 0
7	COM
8	WRITE 1
9	COM
10	READ 1
11	COM
12	SEL MOD 1
13	COM
14	WRITE 2
15	COM
16	READ 2
17	COM
18	SEL MOD 2
19	COM
20	WRITE 3
21	COM
22	READ 3
23	COM
24	SEL MOD 3
25	COM
26	WRITE 4
27	COM
28	READ 4
29	COM
30	SEL MOD 4
31	COM
32	WRITE 5
33	COM
34	READ 5
35	COM
36	SEL MOD 5
37	COM
38	WRITE 6
39	COM
40	READ 6
41	COM
42	SEL MOD 6
43	COM
44	WRITE 7
45	COM
46	READ 7
47	COM
48	SEL MOD 7
49	CONTROL GND
50	COM

J3

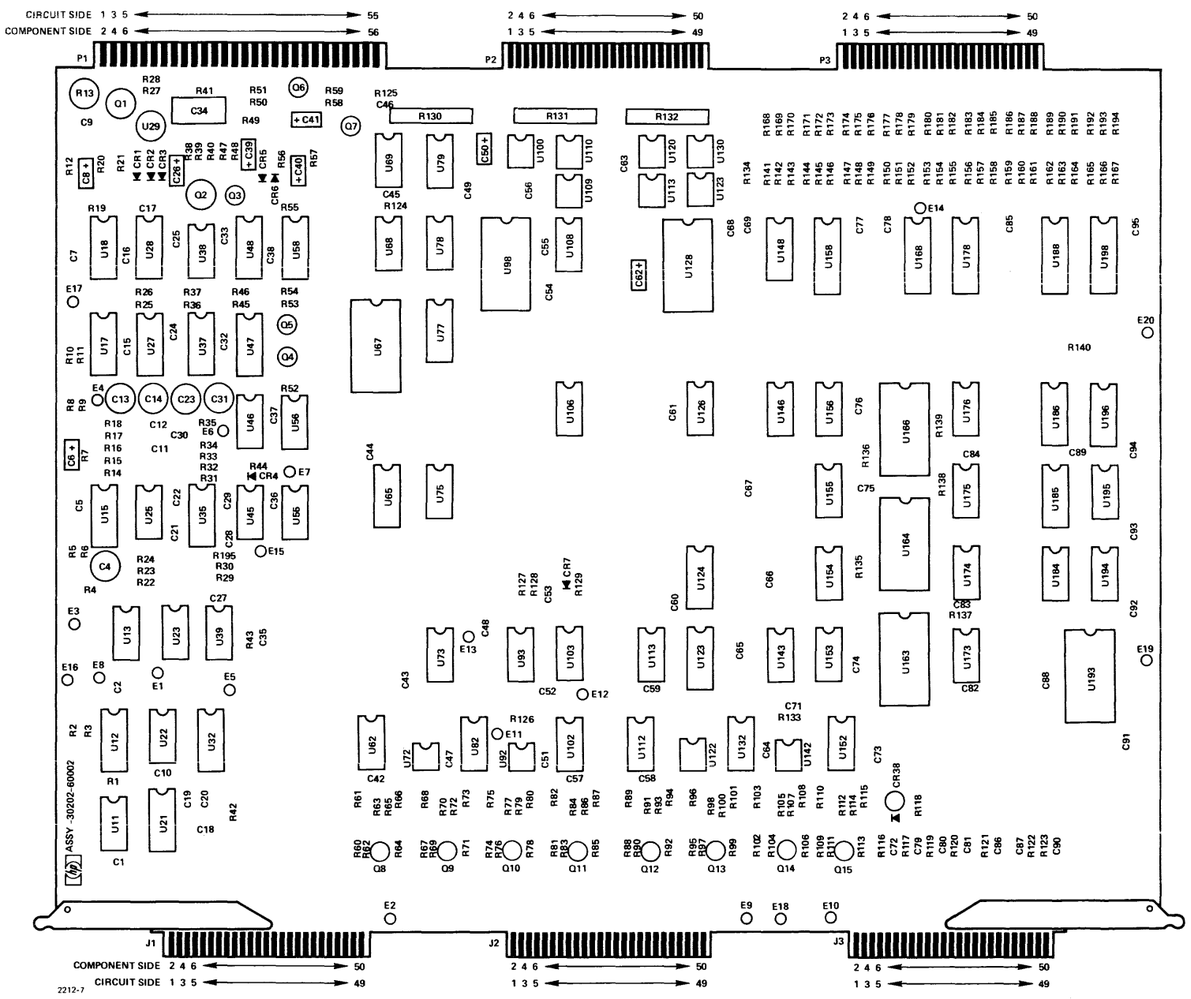
PIN	SIGNAL
1	COM
2	CLR
3	T0
4	T3
5	T2
6	—
7	UOS
8	IS
9	—
10	LOS
11	—
12	—
13	—
14	—
15	—
16	—
17	—
18	—
19	—
20	—
21	—
22	(FLG0)TU
23	—
24	(FLG7)INDEX
25	(FLG4)DIS
26	(FLG5)DRQ
27	—
28	—
29	—
30	—
31	M12
32	—
33	M13
34	M11
35	M14
36	M10
37	M15
38	M09
39	T1
40	M08
41	—
42	M04
43	—
44	M05
45	—
46	M06
47	—
48	M07
49	—
50	COM

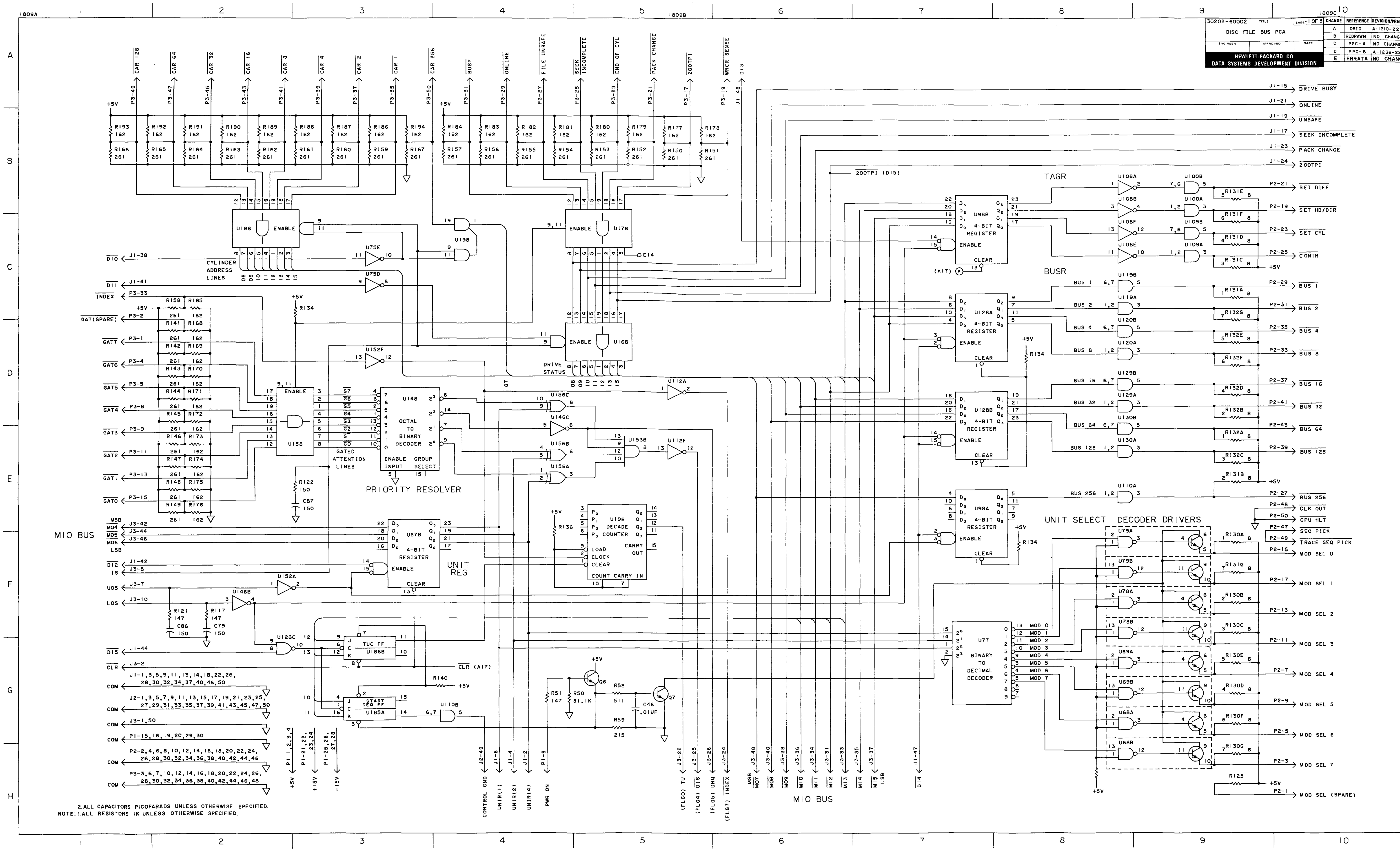
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0424	72	0535	128	0742	184	0282
12	0368	73	0370	129,130	0535	185,186	0715
13	0077	75	0174	132	0605	188	0755
15	0515	77	0111				
21	0231	78,79	0902	142	0535	193	0726
22	0613			143	0282	194	0613
23	0370	82	0605	146	0174	195	0511
25	0077	92	0535	148	0657	196	0705
29	0429	93	0141	152	0174	198	0755
		98	0742	153	0374		
32	0515			154	0372		
33	0619	100	0535	155	0374		
35	0515	102	0174	156	0282		
45	0239	103	0370	158	0755		
46	0205	106	0511				
		108	0174	163,164	0726		
55	0077	109,110	0535	166	0726		
56	0424	112	0174	168	0755		
		113	0370	173,176	0613		
62	0174	119,120	0535	178	0755		
65	0616	122	0535				
67	0742	123,124	0657				
68,69	0902	126	0328				

Note: U17, 18, 27, 28, 37, 47, 48, and 58 are part no. 1858-0021.

U38 is part no. 1858-0001.





30202-60002
DISC FILE BUS PCA
SHEET 1 OF 3
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION
CHANGE REFERENCE REVISION/PREFIX
A ORIG A-1210-22
B REDRAWN NO CHANGE
C PPC-A NO CHANGE
D PPC-B A-1236-22
E ERRATA NO CHANGE
1809A
1809B
1809C
CAR 128
CAR 64
CAR 32
CAR 16
CAR 8
CAR 4
CAR 2
CAR 1
CAR 256
BUSY
ONLINE
FILE UNSAFE
SEEK INCOMPLETE
END OF CYL
PACK CHANGE
200TPI
WRCR SENSE
DI3
DRIVE BUSY
ONLINE
UNSAFE
SEEK INCOMPLETE
PACK CHANGE
200TPI
200TPI (DI5)
CYLINDER ADDRESS LINES
DRIVE STATUS
TAGR
SET DIFF
SET HD/DIR
SET CYL
CONTR
BUSR
BUS 1
BUS 2
BUS 4
BUS 8
BUS 16
BUS 32
BUS 64
BUS 128
BUS 256
CLK OUT
CPU HLT
SEQ PICK
TRACE SEQ PICK
4-BIT REGISTER
ENABLE
CLEAR
GATED ATTENTION LINES
OCTAL TO BINARY DECODER
ENABLE INPUT
GROUP SELECT
PRIORITY RESOLVER
MIO BUS
UNIT REG
DECADE COUNTER
LOAD
CLOCK
CARRY OUT
COUNT CARRY IN
UNIT SELECT DECODER DRIVERS
BINARY TO DECIMAL DECODER
MOD SEL 0
MOD SEL 1
MOD SEL 2
MOD SEL 3
MOD SEL 4
MOD SEL 5
MOD SEL 6
MOD SEL 7
MOD SEL (SPARE)
TUC FF
START SEQ FF
INDEX
GAT(SPARE)
CLR (A17)
CONTROL GND
UNIR(1)
UNIR(2)
UNIR(4)
PWR ON
(FLG0) TU
(FLG4) DI5
(FLG5) DRQ
(FLG7) INDEX
J1-1,3,5,9,11,13,14,18,22,26,28,30,32,34,37,40,46,50
J2-1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,50
J3-1,50
P1-15,16,19,20,29,30
P2-2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46
P3-3,6,7,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46,48
COM
2. ALL CAPACITORS PICOFARADS UNLESS OTHERWISE SPECIFIED.
NOTE: 1. ALL RESISTORS 1K UNLESS OTHERWISE SPECIFIED.

SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	—
6	—
7	—
8	—
9	PWR ON
10	—
11	—
12	—
13	—
14	—
15	COM
16	COM
17	—
18	—
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	—
32	—
33	—
34	—
35	—
36	—
37	—
38	—
39	—
40	—
41	—
42	—
43	—
44	—
45	—
46	—
47	—
48	—
49	—
50	—
51	—
52	—
53	—
54	—
55	—
56	—

P2

PIN	SIGNAL
1	MOD SEL (SPARES)
2	COM
3	MOD SEL 7
4	COM
5	MOD SEL 6
6	COM
7	MOD SEL 4
8	COM
9	MOD SEL 5
10	COM
11	MOD SEL 3
12	COM
13	MOD SEL 2
14	COM
15	MOD SEL 0
16	COM
17	MOD SEL 1
18	COM
19	SET HD/DIR
20	COM
21	SET DIFF
22	COM
23	SET CYL
24	COM
25	CONTR
26	COM
27	BUS 256
28	COM
29	BUS 1
30	COM
31	BUS 2
32	COM
33	BUS 8
34	COM
35	BUS 4
36	COM
37	BUS 16
38	COM
39	BUS 128
40	COM
41	BUS 32
42	COM
43	BUS 64
44	COM
45	—
46	COM
47	SEQ PICK
48	CLK OUT
49	TRACE SEQ PICK
50	CPU HLT

P3

PIN	SIGNAL
1	GAT7
2	GAT(SPARE)
3	COM
4	GAT6
5	GAT5
6	COM
7	COM
8	GAT4
9	GAT3
10	COM
11	GAT2
12	COM
13	GAT1
14	COM
15	GAT0
16	COM
17	200TPI
18	COM
19	WRCR SENSE
20	COM
21	PACK CHG
22	COM
23	END OF CYL
24	COM
25	SEEK INCOMPLETE
26	COM
27	FILE UNSAFE
28	COM
29	ONLINE
30	COM
31	BUSY
32	COM
33	INDEX
34	COM
35	CAR 1
36	COM
37	CAR 2
38	COM
39	CAR 4
40	COM
41	CAR 8
42	COM
43	CAR 16
44	COM
45	CAR 32
46	COM
47	CAR 64
48	COM
49	CAR 128
50	CAR 256

J1

PIN	SIGNAL
1	COM
2	UNIR(4)
3	COM
4	UNIR(2)
5	COM
6	UNIR(1)
7	CEN
8	CEE
9	COM
10	FCE
11	COM
12	CCLR
13	COM
14	COM
15	DRIVE BUSY
16	+READ
17	SEEK INCOMPLETE
18	COM
19	UNSAFE
20	CCIN
21	ONLINE
22	COM
23	PACK CHG
24	200TPI
25	TB
26	COM
27	SEP DATA
28	COM
29	WRITE DATA (70)
30	COM
31	SMP
32	COM
33	TD
34	COM
35	—
36	CLK
37	COM
38	D10
39	TA
40	COM
41	D11
42	D12
43	WSM
44	D15
45	TC
46	COM
47	D14
48	D13
49	—
50	COM

J2

PIN	SIGNAL
1	COM
2	WRITE 0
3	COM
4	READ 0
5	COM
6	SEL MOD 0
7	COM
8	WRITE 1
9	COM
10	READ 1
11	COM
12	SEL MOD 1
13	COM
14	WRITE 2
15	COM
16	READ 2
17	COM
18	SEL MOD 2
19	COM
20	WRITE 3
21	COM
22	READ 3
23	COM
24	SEL MOD 3
25	COM
26	WRITE 4
27	COM
28	READ 4
29	COM
30	SEL MOD 4
31	COM
32	WRITE 5
33	COM
34	READ 5
35	COM
36	SEL MOD 5
37	COM
38	WRITE 6
39	COM
40	READ 6
41	COM
42	SEL MOD 6
43	COM
44	WRITE 7
45	COM
46	READ 7
47	COM
48	SEL MOD 7
49	CONTROL GND
50	COM

J3

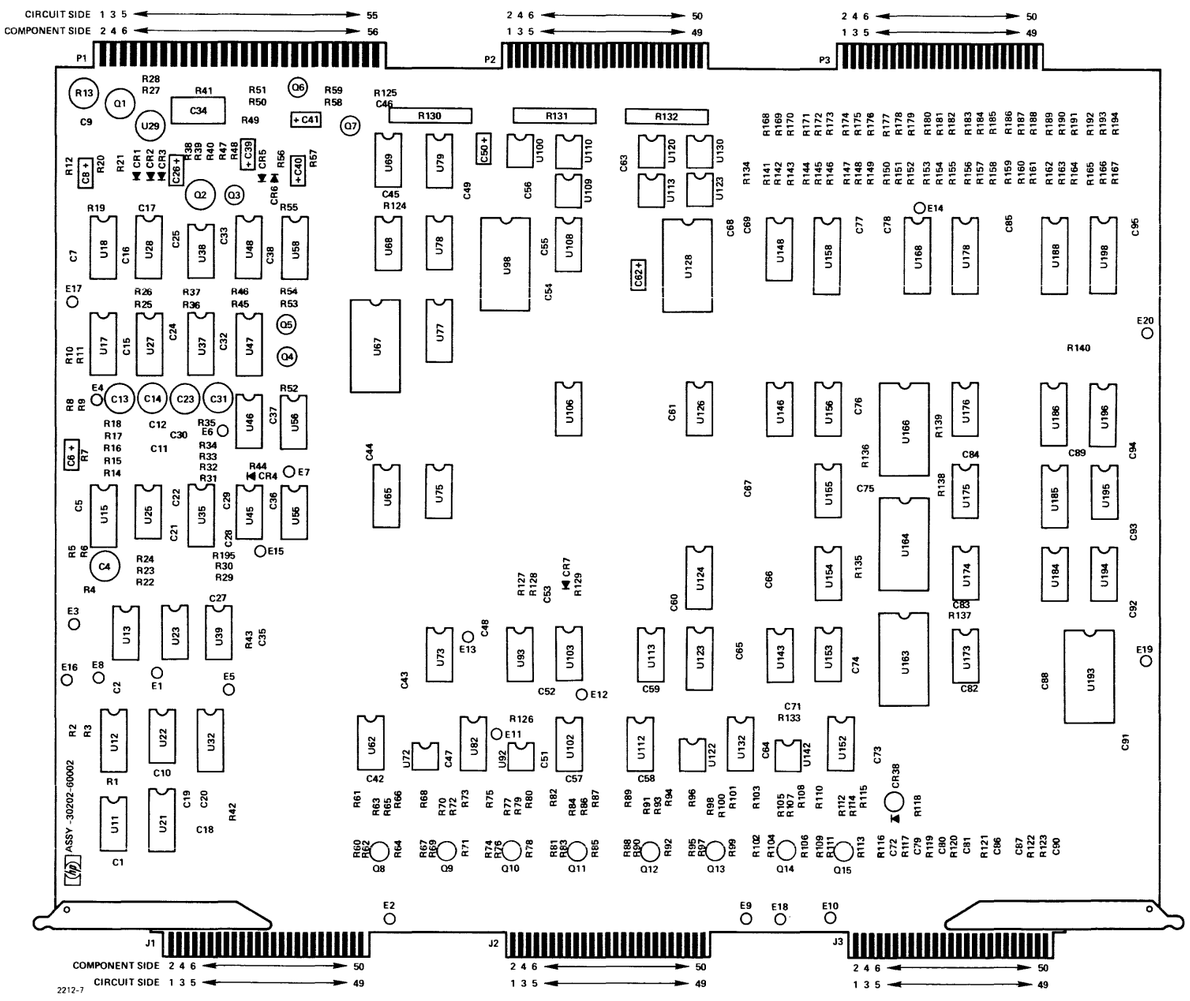
PIN	SIGNAL
1	COM
2	CLR
3	T0
4	T3
5	T2
6	—
7	UOS
8	IS
9	—
10	LOS
11	—
12	—
13	—
14	—
15	—
16	—
17	—
18	—
19	—
20	—
21	—
22	(FLG0)TU
23	—
24	(FLG7)INDEX
25	(FLG4)DIS
26	(FLG5)DRQ
27	—
28	—
29	—
30	—
31	M12
32	—
33	M13
34	M11
35	M14
36	M10
37	M15
38	M09
39	T1
40	M08
41	—
42	M04
43	—
44	M05
45	—
46	M06
47	—
48	M07
49	—
50	COM

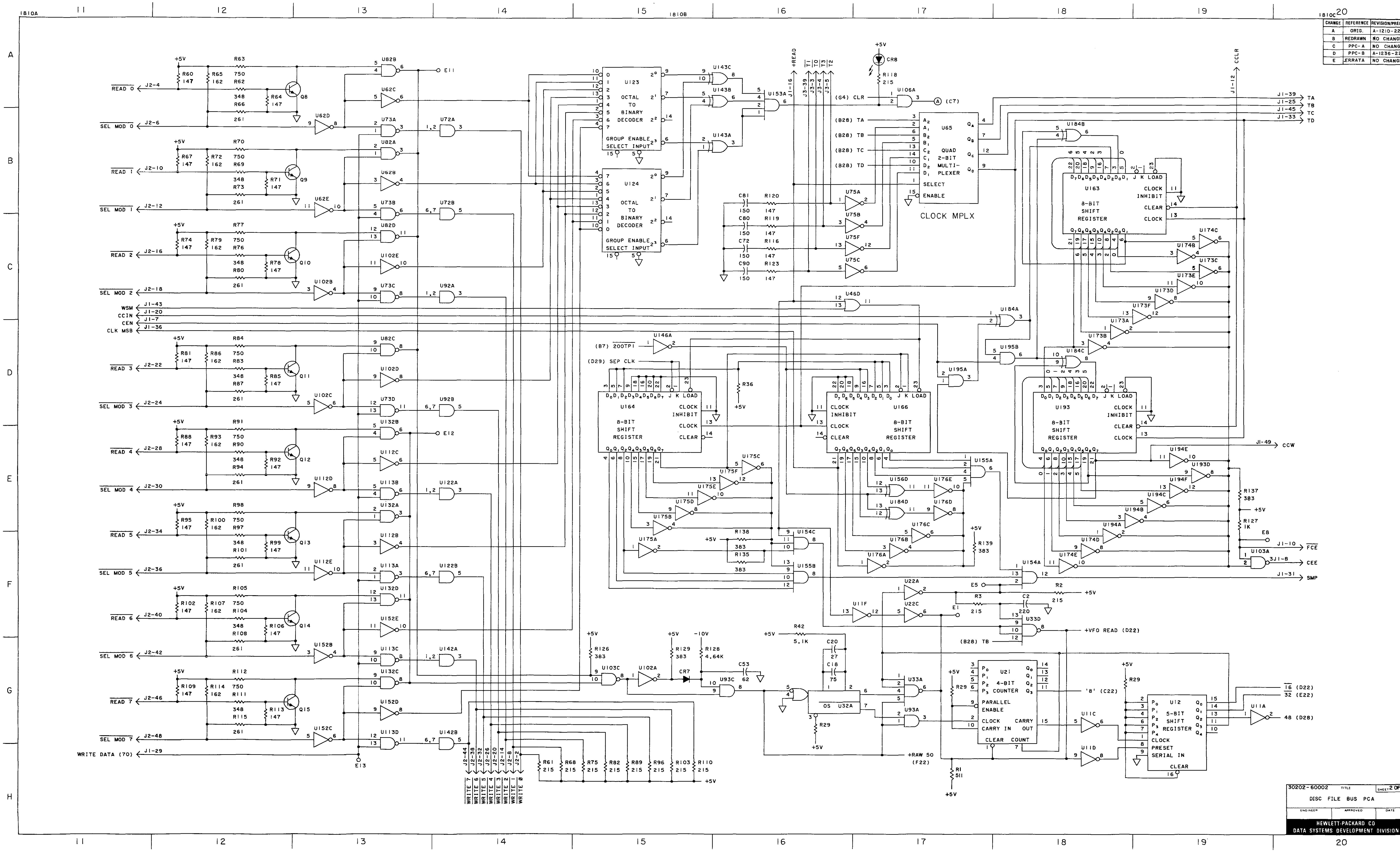
I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0424	72	0535	128	0742	184	0282
12	0368	73	0370	129,130	0535	185,186	0715
13	0077	75	0174	132	0605	188	0755
15	0515	77	0111				
21	0231	78,79	0902	142	0535	193	0726
22	0613			143	0282	194	0613
23	0370	82	0605	146	0174	195	0511
25	0077	92	0535	148	0657	196	0705
29	0429	93	0141	152	0174	198	0755
		98	0742	153	0374		
32	0515			154	0372		
33	0619	100	0535	155	0374		
35	0515	102	0174	156	0282		
45	0239	103	0370	158	0755		
46	0205	106	0511				
		108	0174	163,164	0726		
55	0077	109,110	0535	166	0726		
56	0424	112	0174	168	0755		
		113	0370	173,176	0613		
62	0174	119,120	0535	178	0755		
65	0616	122	0535				
67	0742	123,124	0657				
68,69	0902	126	0328				

Note: U17, 18, 27, 28, 37, 47, 48, and 58 are part no. 1858-0021.

U38 is part no. 1858-0001.





CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	NO CHANGE
D	PPC-B	A-1236-22
E	ERRATA	NO CHANGE

30202-60002 SHEET 2 OF 3

DISC FILE BUS PCA

HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	—
6	—
7	—
8	—
9	PWR ON
10	—
11	—
12	—
13	—
14	—
15	COM
16	COM
17	—
18	—
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	—
32	—
33	—
34	—
35	—
36	—
37	—
38	—
39	—
40	—
41	—
42	—
43	—
44	—
45	—
46	—
47	—
48	—
49	—
50	—
51	—
52	—
53	—
54	—
55	—
56	—

P2 PIN	P2 SIGNAL
1	MOD SEL (SPARES)
2	COM
3	MOD SEL 7
4	COM
5	MOD SEL 6
6	COM
7	MOD SEL 4
8	COM
9	MOD SEL 5
10	COM
11	MOD SEL 3
12	COM
13	MOD SEL 2
14	COM
15	MOD SEL 0
16	COM
17	MOD SEL 1
18	COM
19	SET HD/DIR
20	COM
21	SET DIFF
22	COM
23	SET CYL
24	COM
25	CONTR
26	COM
27	BUS 256
28	COM
29	BUS 1
30	COM
31	BUS 2
32	COM
33	BUS 8
34	COM
35	BUS 4
36	COM
37	BUS 16
38	COM
39	BUS 128
40	COM
41	BUS 32
42	COM
43	BUS 64
44	COM
45	—
46	COM
47	SEQ PICK
48	CLK OUT
49	TRACE SEQ PICK
50	CPU HLT

P3 PIN	P3 SIGNAL
1	GAT7
2	GAT(SPARE)
3	COM
4	GAT6
5	GAT5
6	COM
7	COM
8	GAT4
9	GAT3
10	COM
11	GAT2
12	COM
13	GAT1
14	COM
15	GAT0
16	COM
17	200TPI
18	COM
19	WRCR SENSE
20	COM
21	PACK CHG
22	COM
23	END OF CYL
24	COM
25	SEEK INCOMPLETE
26	COM
27	FILE UNSAFE
28	COM
29	ONLINE
30	COM
31	BUSY
32	COM
33	INDEX
34	COM
35	CAR 1
36	COM
37	CAR 2
38	COM
39	CAR 4
40	COM
41	CAR 8
42	COM
43	CAR 16
44	COM
45	CAR 32
46	COM
47	CAR 64
48	COM
49	CAR 128
50	CAR 256

J1 PIN	J1 SIGNAL
1	COM
2	UNIR(4)
3	COM
4	UNIR(2)
5	COM
6	UNIR(1)
7	CEN
8	CEE
9	COM
10	FCE
11	COM
12	CCLR
13	COM
14	COM
15	DRIVE BUSY
16	+READ
17	SEEK INCOMPLETE
18	COM
19	UNSAFE
20	CCIN
21	ONLINE
22	COM
23	PACK CHG
24	200TPI
25	TB
26	COM
27	SEP DATA
28	COM
29	WRITE DATA (70)
30	COM
31	SMP
32	COM
33	TD
34	COM
35	—
36	CLK
37	COM
38	D10
39	TA
40	COM
41	D11
42	D12
43	WSM
44	D15
45	TC
46	COM
47	D14
48	D13
49	—
50	COM

J2 PIN	J2 SIGNAL
1	COM
2	WRITE 0
3	COM
4	READ 0
5	COM
6	SEL MOD 0
7	COM
8	WRITE 1
9	COM
10	READ 1
11	COM
12	SEL MOD 1
13	COM
14	WRITE 2
15	COM
16	READ 2
17	COM
18	SEL MOD 2
19	COM
20	WRITE 3
21	COM
22	READ 3
23	COM
24	SEL MOD 3
25	COM
26	WRITE 4
27	COM
28	READ 4
29	COM
30	SEL MOD 4
31	COM
32	WRITE 5
33	COM
34	READ 5
35	COM
36	SEL MOD 5
37	COM
38	WRITE 6
39	COM
40	READ 6
41	COM
42	SEL MOD 6
43	COM
44	WRITE 7
45	COM
46	READ 7
47	COM
48	SEL MOD 7
49	CONTROL GND
50	COM

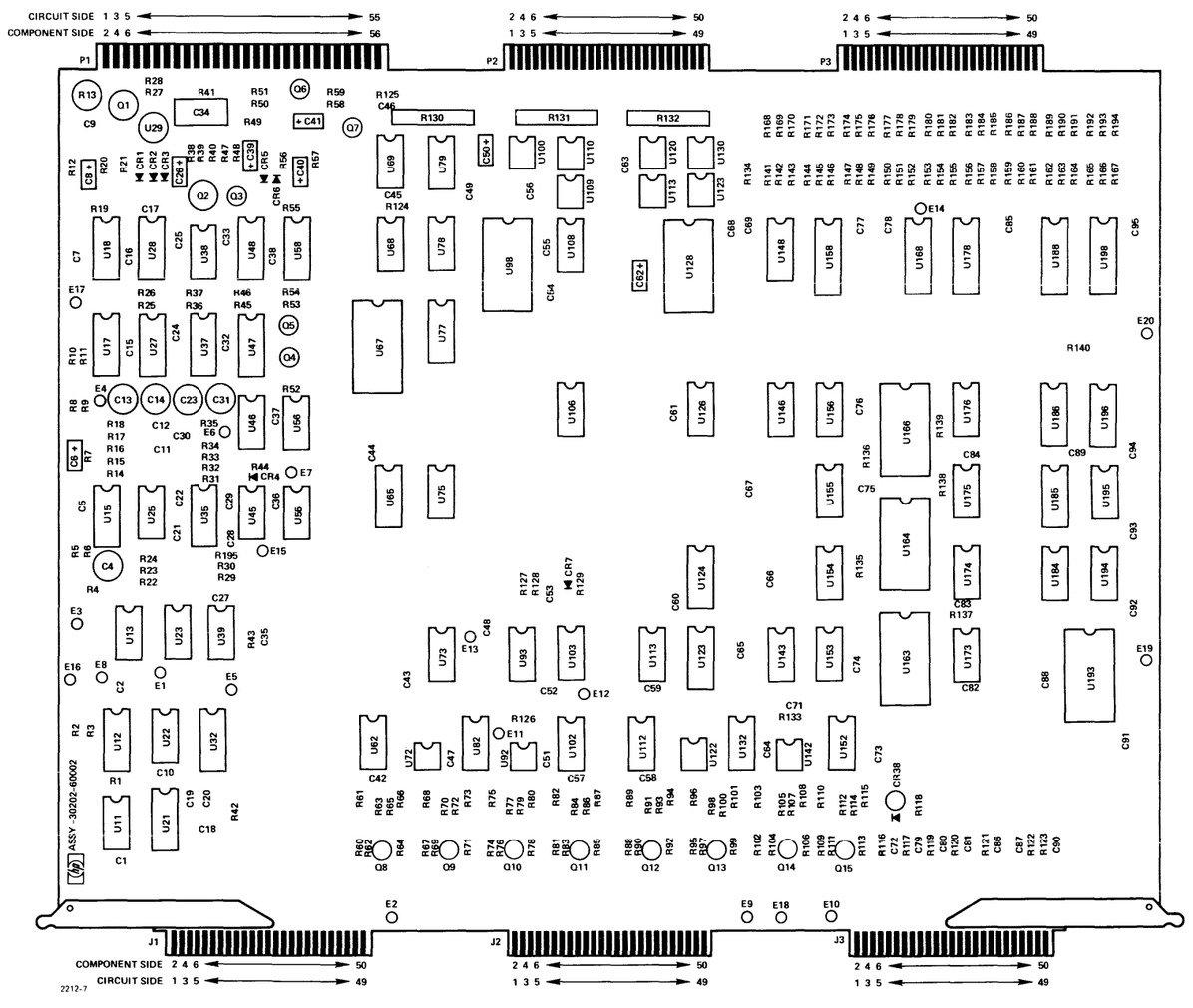
J3 PIN	J3 SIGNAL
1	COM
2	CLR
3	T0
4	T3
5	T2
6	—
7	UOS
8	IS
9	—
10	LOS
11	—
12	—
13	—
14	—
15	—
16	—
17	—
18	—
19	—
20	—
21	—
22	(FLG0)TU
23	—
24	(FLG7)INDEX
25	(FLG4)DIS
26	(FLG5)DRQ
27	—
28	—
29	—
30	—
31	M12
32	—
33	M13
34	M11
35	M14
36	M10
37	M15
38	M09
39	T1
40	M08
41	—
42	M04
43	—
44	M05
45	—
46	M06
47	—
48	M07
49	—
50	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-
11	0424	72	0535	128	0742	184	0282
12	0368	73	0370	129,130	0535	185,186	0715
13	0077	75	0174	132	0605	188	0755
15	0515	77	0111				
21	0231	78,79	0902	142	0535	193	0726
22	0613			143	0282	194	0613
23	0370	82	0605	146	0174	195	0511
25	0077	92	0535	148	0657	196	0705
29	0429	93	0141	152	0174	198	0755
		98	0742	153	0374		
32	0515			154	0372		
33	0619	100	0535	155	0374		
35	0515	102	0174	156	0282		
45	0239	103	0370	158	0755		
46	0205	106	0511				
		108	0174	163,164	0726		
55	0077	109,110	0535	166	0726		
56	0424	112	0174	168	0755		
		113	0370	173,176	0613		
62	0174	119,120	0535	178	0755		
65	0616	122	0535				
67	0742	123,124	0657				
68,69	0902	126	0328				

Note: U17, 18, 27, 28, 37, 47, 48, and 58 are part no. 1858-0021.

U38 is part no. 1858-0001.



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	NO CHANGE
D	PPC-B	A-1236-22
E	ERRATA	NO CHANGE

VOLTAGE CONTROLLED OSCILLATOR (VCO)

DATA/CLOCK SEPARATOR

5VOLT REGULATOR

DC VOLTAGE REFERENCE

VFO TIMING PULSES

AMPLIFIER U38B

50 PIN S OF- U17,U18,U27, U28,U37,U38, U47,U48,U58

30202-60002	TITLE: DISC FILE BUS PCA	SHEET 3 OF 3
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		

I/O DETAILED DIAGRAM SET

DD-602

DISC CONTROLLER PROCESSOR PCA

30202-60003

SERIES 1251

121C

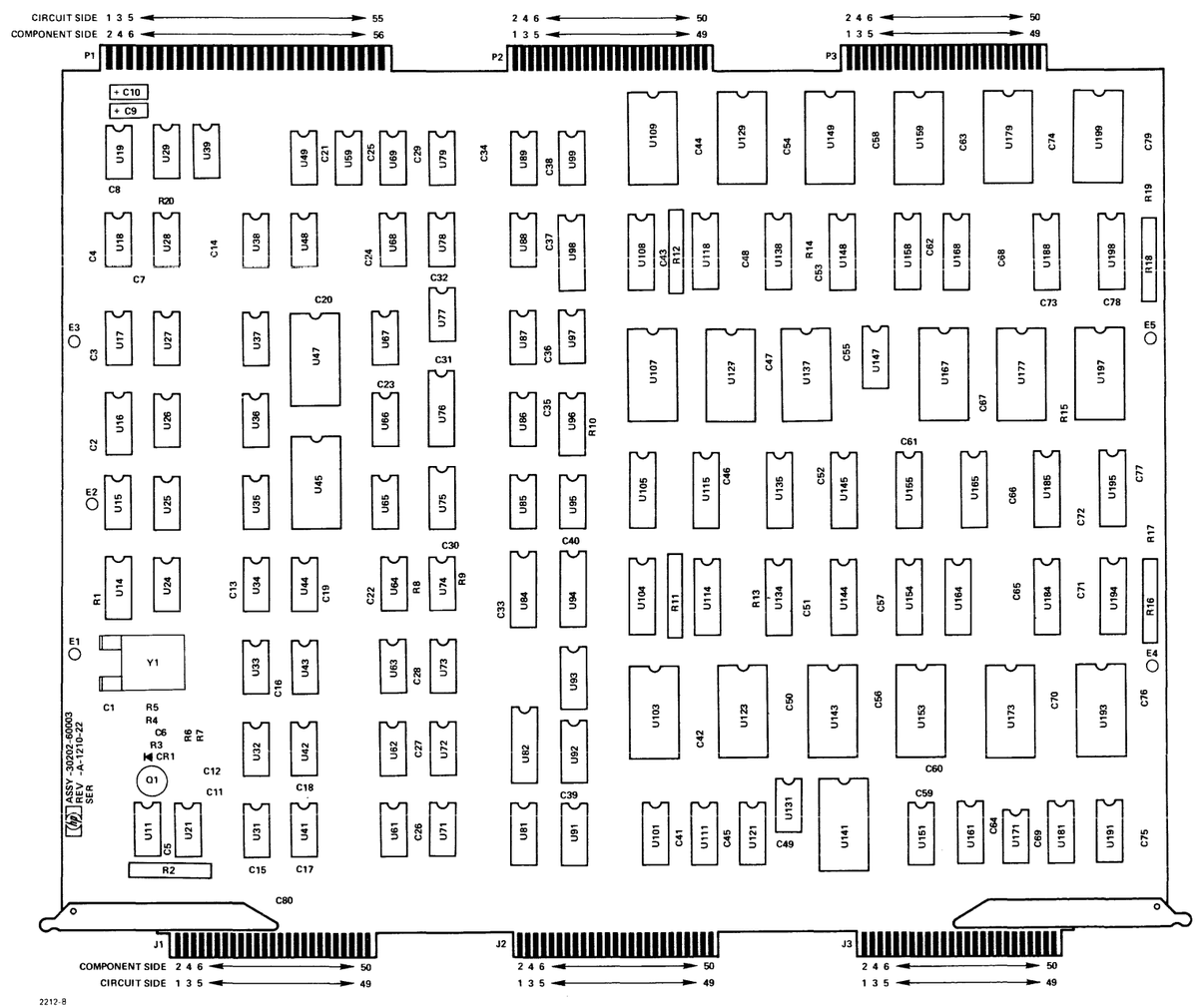
REV C

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	$\overline{\text{COM}}$
2	+5V	2	$\overline{\text{COM}}$	2	COM	2	$\overline{\text{CLEAR}}$
3	+5V	3	$\overline{\text{CLK RST}}$	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	$\overline{\text{ALT CK}}$	5	ROM 5	5	$\overline{T_2}$
6		6	$\overline{\text{DISP}}$	6		6	ROR 9
7		7	$\overline{\text{CK CTL}}$	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8		8	INPUT STROBE
9		9	ERA 7	9	ROM 7		
10		10		10		9	FLAG 10
11		11	LD ERA	11	ROM 8	10	LOWER OUTPUT STROBE
12		12	ERA 11	12			
13		13	ERA 3	13	ROM 9	11	FLAG 14
14		14	ERA 2	14		12	FLAG 12
15	COM	15	ERA 10	15	ROM 10	13	FLAG 16
16	COM	16	ERA 6	16		14	FLAG 15
17		17	AT_0	17	ROM 11	15	ROR 8
18		18	CTL1	18		16	FLAG 17
19	COM	19	AT_3	19	ROM 12	17	ROR 11
20	COM	20	AT_1	20		18	ROR 7
21		21	AT_2	21	ROM 13	19	WORD TYPE ONE
22		22		22			
23		23	CTL2	23	ROM 14	20	ROR 10
24		24	$\overline{\text{UB}}$	24		21	FLAG 13
25		25	$\overline{\text{AM}}$	25	ROM 15	22	FLAG 11
26		26	$\overline{\text{LB}}$	26		23	FLAG 6
27		27	AS2	27	ROM 16	24	FLAG 7
28		28	AS3	28	ROM 0	25	FLAG 4
29	COM	29	AS1	29	ROM 17	26	FLAG 5
30	COM	30	AS0	30	ROM 1	27	FLAG 2
31		31	V	31	ROM 18	28	FLAG 3
32		32	W	32	ROM 2	29	FLAG 0
33		33	T	33	ROM 19	30	FLAG 1
34		34	U	34	ROM 3	31	$\overline{\text{M12}}$
35		35	ERA 1	35		32	EXT SEL
36		36		36		33	$\overline{\text{M13}}$
37		37	ERA 5	37	RAR 0	34	$\overline{\text{M11}}$
38		38	ERA 9	38	RAR 1	35	$\overline{\text{M14}}$
39		39	ERA 4	39	RAR 2	36	$\overline{\text{M10}}$
40		40	ERA 0	40	RAR 3	37	$\overline{\text{M15}}$
41		41	ERA 8	41	RAR 4	38	$\overline{\text{M9}}$
42		42		42	RAR 5	39	$\overline{T_1}$
43		43		43	RAR 6	40	$\overline{\text{M8}}$
44		44		44	RAR 7	41	$\overline{\text{M3}}$
45		45	$\overline{\text{Z}}$	45	RAR 8	42	$\overline{\text{M4}}$
46		46	$\overline{\text{LDRG}}$	46	RAR 9	43	$\overline{\text{M2}}$
47		47	X	47	RAR 10	44	$\overline{\text{M5}}$
48		48	Y	48	RAR 11	45	$\overline{\text{M1}}$
49		49	COM	49	COM	46	$\overline{\text{M6}}$
50		50	COM	50	COM	47	$\overline{\text{M0}}$
51						48	$\overline{\text{M7}}$
52						49	
53						50	COM
54							
55							
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-		1820-	U	1820-
11	0377	47	0495	88	0205	129	0742	167	0606
14	0788	48	0372	89	0372			168	0759
15	0424	49	0377			131	0205		
16	0535			91-93	0788	134	0759	171	0374
17	0512	59	0371	94	0759	135	0755	173	0742
18	0205			95	0843	137	0606	177	0606
19	0239	61-63	0379	96	0788	138	0759	179	0742
		64	0424	97	0205				
21	0142	65	0371	98	0759	141	0640	181	0545
24	0371	66	0372	99	0608	143	0742	184	0759
25	0370	67	0375			144	0759	185	0755
26	0376	68	0205	101	0545	145	0755	188	0759
27	0424	69	0376	103	0742	147	0611		
28	0376			104	0759	148	0759	191	0545
29	0535	71-73	0379	105	0755	149	0742	193	0742
		74	0512	107	0742			194	0759
31-33	0379	75	0788	108	0759	151	0545	195	0755
34	0140	76	0759	109	0742	153	0742	197	0742
35	0384	77	0205			154	0759	198	0759
36	0371	78	0282	111	0545	155	0755	199	0742
37	0141	79	0140	114	0759	158	0759		
38	0140			115	0755	159	0742		
39	0512	81	0788	118	0759				
		82	0759			161	0545		
41-43	0379	84	0759	121	0545				
44	0140	85	0371	123	0742	164	0759		
45	0495	86,87	0843	127	0606	165	0755		



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	ERRATA	NO CHANGE	1,2,3,4

ERA0 J1-40
ERA1 J1-35
ERA2 J1-14
ERA3 J1-13
ERA4 J1-39
ERA5 J1-37
ERA6 J1-16
ERA7 J1-9
ERA8 J1-41
ERA9 J1-38
ERA10 J1-15
ERA11 J1-12

RAR/SAVE REGISTER CONTROL LOGIC

WORD TYPE SIX (D15)

LD ERA J1-11

+5V R2A

(F17) A

(D15) B

(F17) C

CLEAR1 (G9)

(G20) $\overline{T_2}$

(G20) T_1

U65A U35B U35C U26A U26B U34A U34B U44A

JMP CTR RTN

LDERA

$\overline{CT0}$ (E23) ROR 8 (B17)
$\overline{CT1}$ (D23) ROR 9 (B17)
$\overline{CT2}$ (D23) ROR 10 (B17)
$\overline{CT3}$ (D23) ROR 11 (B17)
$\overline{CT4}$ (D23) ROR 12 (B19)
$\overline{CT5}$ (C23) ROR 13 (B19)
$\overline{CT6}$ (C23) ROR 14 (B19)
$\overline{CT7}$ (C23) ROR 15 (B19)
$\overline{CT8}$ (C23) ROR 16 (B19)
$\overline{CT9}$ (B23) ROR 17 (C19)
$\overline{CT10}$ (B23) ROR 18 (B19)
$\overline{CT11}$ (B23) ROR 19 (C19)

C16 .001UF
C80 .001UF

0 1 2 3 4 5 6 7 8 9 10 11

U31E U31D U31B U31A U41E U41D U41B U41A U71E U71D U71B U71A U61E U61D U61B U61A U32E U32D U32B U32A U42E U42D U42B U42A U72E U72D U72B U72A U62E U62D U62B U62A U73E U73D U73B U73A U33E U33D U33B U33A U43E U43D U43B U43A U63E U63D U63B U63A

U31C U41C U71C U61C U32C U42C U72C U62C U73C U33C U43C U63C

RAR

DN/UP CLOCK ENABLE, MAX/MIN, CLOCK, LOAD, CARRY, D_0 D_1 D_2 D_3, Q_0 Q_1 Q_2 Q_3
4-BIT BINARY UP/DOWN COUNTER U101

DN/UP CLOCK ENABLE, MAX/MIN, CLOCK, LOAD, CARRY, D_4 D_5 D_6 D_7, Q_4 Q_5 Q_6 Q_7
4-BIT BINARY UP/DOWN COUNTER U111

(H20) $\overline{T_0}$ U54E

DN/UP CLOCK ENABLE, MAX/MIN, CLOCK, LOAD, CARRY, D_8 D_9 D_{10} D_{11}, Q_8 Q_9 Q_{10} Q_{11}
4-BIT BINARY UP/DOWN COUNTER U121

SAVE REGISTER

MSB
RAR0 J2-37
RAR1 J2-38
RAR2 J2-39
RAR3 J2-40
RAR4 J2-41
RAR5 J2-42

LSB
RAR6 J2-43
RAR7 J2-44
RAR8 J2-45
RAR9 J2-46
RAR10 J2-47
RAR11 J2-48

U81 6-BIT REGISTER: D_0 D_1 D_2 D_3 D_4 D_5, Q_0 Q_1 Q_2 Q_3 Q_4 Q_5, CLOCK, CLEAR

U91 6-BIT REGISTER: D_6 D_7 D_8 D_9 D_{10} D_{11}, Q_6 Q_7 Q_8 Q_9 Q_{10} Q_{11}, CLOCK, CLEAR

(G20) T_1 (E17) D U19D

+5V R20 100Ω U29B

$\overline{CLEAR1}$(D1)(B13)(A18)(B26)(A31)(G31)(F26)

$\overline{CLEAR}$ J3-2

+5V R2C

CLEAR(B) FF U39A
CLEAR 1 FF U39B

(U25-9) AT1

3. ALL LOGIC IS POSITIVE TRUE

2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1K

1. CRYSTAL FREQUENCY MAY VARY WITH DIFFERENT SUBSYSTEMS

NOTES:

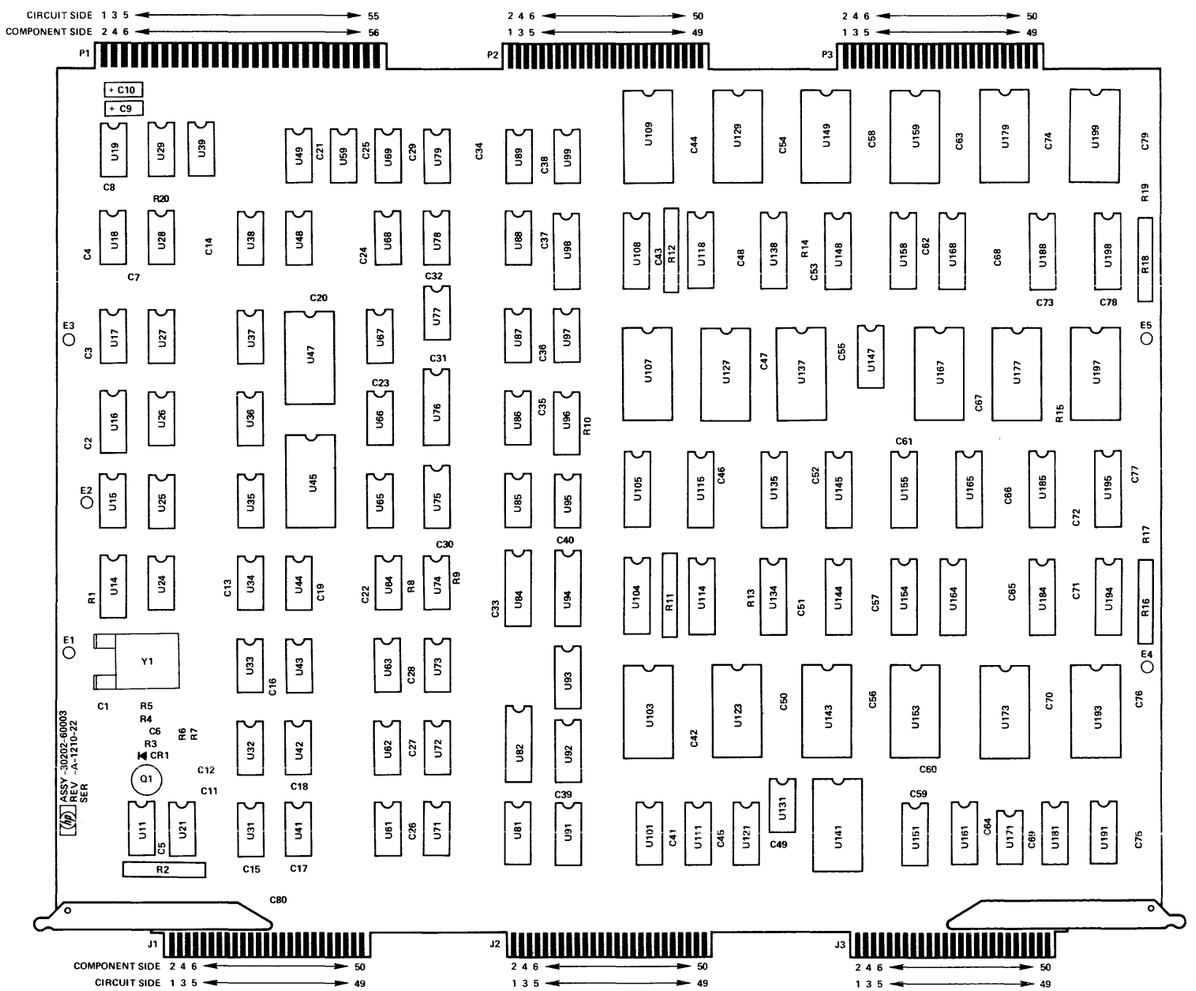
30202-60003 TITLE SHEET 1 OF 4
DISC CONTROLLER PROCESSOR PCA
ENGINEER | APPROVED | DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	CLEAR
3	+5V	3	CLK RST	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	ALT CK	5	ROM 5	5	$\overline{T_2}$
6		6	DISP	6		6	ROR 9
7		7	CK CTL	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8		8	INPUT STROBE
9		9	ERA 7	9	ROM 7	9	FLAG 10
10		10		10		10	LOWER OUTPUT STROBE
11		11	LD ERA	11	ROM 8	11	FLAG 14
12		12	ERA 11	12		12	FLAG 12
13		13	ERA 3	13	ROM 9	13	FLAG 16
14		14	ERA 2	14		14	FLAG 15
15	COM	15	ERA 10	15	ROM 10	15	ROR 8
16	COM	16	ERA 6	16		16	FLAG 17
17		17	AT_0	17	ROM 11	17	ROR 11
18		18	CTL1	18		18	ROR 7
19	COM	19	AT_3	19	ROM 12	19	WORD TYPE ONE
20	COM	20	AT_1	20		20	ROR 10
21		21	AT_2	21	ROM 13	21	FLAG 13
22		22		22		22	FLAG 11
23		23	CTL2	23	ROM 14	23	FLAG 6
24		24	$\overline{UB}$	24		24	FLAG 7
25		25	$\overline{AM}$	25	ROM 15	25	FLAG 4
26		26	$\overline{LB}$	26		26	FLAG 5
27		27	AS2	27	ROM 16	27	FLAG 2
28		28	AS3	28	ROM 0	28	FLAG 3
29	COM	29	AS1	29	ROM 17	29	FLAG 0
30	COM	30	AS0	30	ROM 1	30	$\overline{FLAG\ 1}$
31		31	V	31	ROM 18	31	$\overline{M12}$
32		32	W	32	ROM 2	32	**EXT SEL**
33		33	T	33	ROM 19	33	$\overline{M13}$
34		34	U	34	ROM 3	34	$\overline{M11}$
35		35	ERA 1	35		35	$\overline{M14}$
36		36		36		36	$\overline{M10}$
37		37	ERA 5	37	RAR 0	37	$\overline{M15}$
38		38	ERA 9	38	RAR 1	38	$\overline{M9}$
39		39	ERA 4	39	RAR 2	39	$\overline{T_1}$
40		40	ERA 0	40	RAR 3	40	$\overline{M8}$
41		41	ERA 8	41	RAR 4	41	$\overline{M3}$
42		42		42	RAR 5	42	$\overline{M4}$
43		43		43	RAR 6	43	$\overline{M2}$
44		44		44	RAR 7	44	$\overline{M5}$
45		45	Z	45	RAR 8	45	$\overline{M1}$
46		46	LDRG	46	RAR 9	46	$\overline{M6}$
47		47	X	47	RAR 10	47	$\overline{M0}$
48		48	Y	48	RAR 11	48	$\overline{M7}$
49		49	COM	49	COM	49	
50		50	COM	50	COM	50	COM
51							
52							
53							
54							
55							
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-		1820-	U	1820-
11	0377	47	0495	88	0205	129	0742	167	0606
14	0788	48	0372	89	0372			168	0759
15	0424	49	0377			131	0205		
16	0535			91-93	0788	134	0759	171	0374
17	0512	59	0371	94	0759	135	0755	173	0742
18	0205			95	0843	137	0606	177	0606
19	0239	61-63	0379	96	0788	138	0759	179	0742
		64	0424	97	0205				
21	0142	65	0371	98	0759	141	0640	181	0545
24	0371	66	0372	99	0608	143	0742	184	0759
25	0370	67	0375			144	0759	185	0755
26	0376	68	0205	101	0545	145	0755	188	0759
27	0424	69	0376	103	0742	147	0611		
28	0376			104	0759	148	0759	191	0545
29	0535	71-73	0379	105	0755	149	0742	193	0742
		74	0512	107	0742			194	0759
31-33	0379	75	0788	108	0759	151	0545	195	0755
34	0140	76	0759	109	0742	153	0742	197	0742
35	0384	77	0205			154	0759	198	0759
36	0371	78	0282	111	0545	155	0755	199	0742
37	0141	79	0140	114	0759	158	0759		
38	0140			115	0755	159	0742		
39	0512	81	0788	118	0759				
		82	0759			161	0545		
41-43	0379	84	0759	121	0545				
44	0140	85	0371	123	0742	164	0759		
45	0495	86,87	0843	127	0606	165	0755		



2212-8

1085A-2 1085B-2 1085C-2

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

DESTINATION/SOURCE CODE

ROR

ROR CK (F18)
CLEAR1(G9)

ROR 8 (C2)
ROR 9 (C3)
ROR 10 (C4)
ROR 11 (C4)

ROR 16 (C7)(E18)(G21)
ROR 18 (C9)(G21)
ROR 15 (C7)(E18)(G21)
ROR 14 (C6)(F21)
ROR 13 (C6)(F21)(C27)
ROR 12 (C5)(G21)(D27)
ROR 19 (C9)(G21)
ROR 17 (C8)(G21)

ALU CONTROL DECODE

INSTRUCTION DECODER

CONDITION SENSE LOGIC

COUNTER/ REGISTER SELECT

FLAG LOGIC

WORD DECODE CONTROL

STROBE GENERATOR

DRIVER GATES

TIMING GENERATOR/ CONTROL LOGIC

TIMING GENERATOR

OSCILLATOR

30202-60003 TITLE SHEET 2 OF 4

DISC CONTROLLER PROCESSOR PCA

ENGINEER | APPROVED | DATE

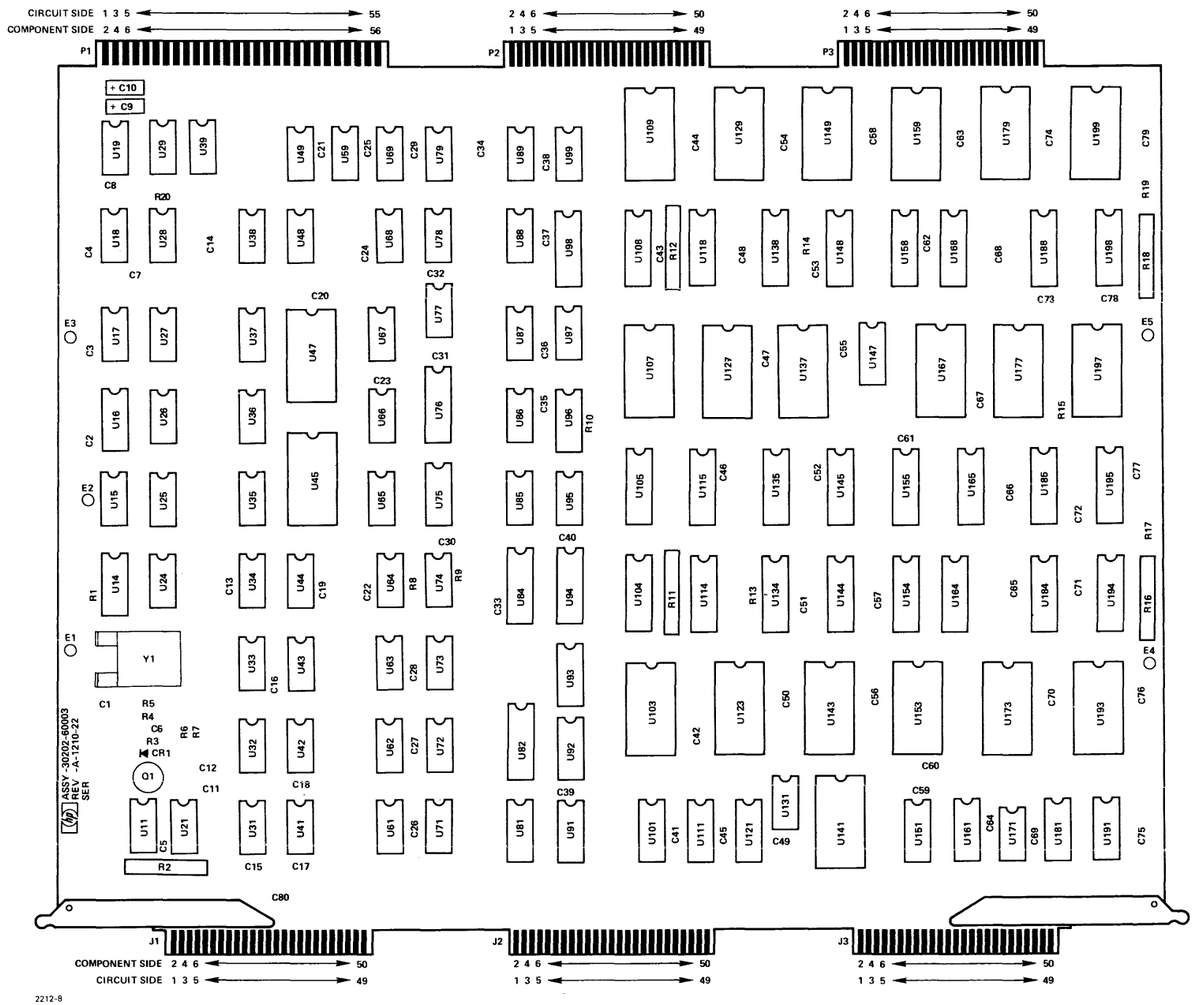
HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	$\overline{\text{COM}}$
2	+5V	2	$\overline{\text{COM}}$	2	COM	2	$\overline{\text{CLEAR}}$
3	+5V	3	$\overline{\text{CLK RST}}$	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	$\overline{\text{ALT CK}}$	5	ROM 5	5	$\overline{T_2}$
6		6	$\overline{\text{DISP}}$	6		6	ROR 9
7		7	$\overline{\text{CK CTL}}$	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8		8	INPUT STROBE
9		9	ERA 7	9	ROM 7		
10		10		10		9	FLAG 10
11		11	LD ERA	11	ROM 8	10	LOWER OUTPUT STROBE
12		12	ERA 11	12			
13		13	ERA 3	13	ROM 9	11	FLAG 14
14		14	ERA 2	14		12	FLAG 12
15	COM	15	ERA 10	15	ROM 10	13	FLAG 16
16	COM	16	ERA 6	16		14	FLAG 15
17		17	AT_0	17	ROM 11	15	ROR 8
18		18	CTL1	18		16	FLAG 17
19	COM	19	AT_3	19	ROM 12	17	ROR 11
20	COM	20	AT_1	20		18	ROR 7
21		21	AT_2	21	ROM 13	19	WORD TYPE ONE
22		22		22			
23		23	$\overline{\text{CTL2}}$	23	ROM 14	20	ROR 10
24		24	$\overline{\text{UB}}$	24		21	FLAG 13
25		25	$\overline{\text{AM}}$	25	ROM 15	22	FLAG 11
26		26	$\overline{\text{LB}}$	26		23	FLAG 6
27		27	AS2	27	ROM 16	24	FLAG 7
28		28	AS3	28	ROM 0	25	FLAG 4
29	COM	29	AS1	29	ROM 17	26	FLAG 5
30	COM	30	AS0	30	ROM 1	27	FLAG 2
31		31	V	31	ROM 18	28	FLAG 3
32		32	W	32	ROM 2	29	FLAG 0
33		33	T	33	ROM 19	30	FLAG 1
34		34	U	34	ROM 3	31	$\overline{\text{M12}}$
35		35	ERA 1	35		32	**EXT SEL**
36		36		36		33	$\overline{\text{M13}}$
37		37	ERA 5	37	RAR 0	34	$\overline{\text{M11}}$
38		38	ERA 9	38	RAR 1	35	$\overline{\text{M14}}$
39		39	ERA 4	39	RAR 2	36	$\overline{\text{M10}}$
40		40	ERA 0	40	RAR 3	37	$\overline{\text{M15}}$
41		41	ERA 8	41	RAR 4	38	$\overline{\text{M9}}$
42		42		42	RAR 5	39	$\overline{T_1}$
43		43		43	RAR 6	40	$\overline{\text{M8}}$
44		44		44	RAR 7	41	$\overline{\text{M3}}$
45		45	$\overline{\text{Z}}$	45	RAR 8	42	$\overline{\text{M4}}$
46		46	$\overline{\text{LDRG}}$	46	RAR 9	43	$\overline{\text{M2}}$
47		47	X	47	RAR 10	44	$\overline{\text{M5}}$
48		48	Y	48	RAR 11	45	$\overline{\text{M1}}$
49		49	COM	49	COM	46	$\overline{\text{M6}}$
50		50	COM	50	COM	47	$\overline{\text{M0}}$
51						48	$\overline{\text{M7}}$
52						49	
53						50	COM
54							
55							
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-		1820-	U	1820-
11	0377	47	0495	88	0205	129	0742	167	0606
14	0788	48	0372	89	0372			168	0759
15	0424	49	0377			131	0205		
16	0535			91-93	0788	134	0759	171	0374
17	0512	59	0371	94	0759	135	0755	173	0742
18	0205			95	0843	137	0606	177	0606
19	0239	61-63	0379	96	0788	138	0759	179	0742
		64	0424	97	0205				
21	0142	65	0371	98	0759	141	0640	181	0545
24	0371	66	0372	99	0608	143	0742	184	0759
25	0370	67	0375			144	0759	185	0755
26	0376	68	0205	101	0545	145	0755	188	0759
27	0424	69	0376	103	0742	147	0611		
28	0376			104	0759	148	0759	191	0545
29	0535	71-73	0379	105	0755	149	0742	193	0742
		74	0512	107	0742			194	0759
31-33	0379	75	0788	108	0759	151	0545	195	0755
34	0140	76	0759	109	0742	153	0742	197	0742
35	0384	77	0205			154	0759	198	0759
36	0371	78	0282	111	0545	155	0755	199	0742
37	0141	79	0140	114	0759	158	0759		
38	0140			115	0755	159	0742		
39	0512	81	0788	118	0759				
		82	0759			161	0545		
41-43	0379	84	0759	121	0545				
44	0140	85	0371	123	0742	164	0759		
45	0495	86,87	0843	127	0606	165	0755		



IMMEDIATE OPERAND GATES

U98

ENABLE

A BUS

A15(C31)(D40)
A14(C31)(D40)
A13(C31)(D40)
A12(C31)(C40)
A11(C31)(C40)
A10(D31)(C40)
A9(D31)(C40)
A8(D31)(C40)

COUNTER CONTROL

COUNTER

(LSB)
(A30) M15
(A30) M14
(A30) M13
(A30) M12

U151 D0 D1 D2 D3 4-BIT BINARY UP/DOWN COUNTER
LOAD
CLOCK
CLOCK ENABLE
DN/UP
CARRY MAX/MIN
Q0 Q1 Q2 Q3

CT11 (C9)
CT10 (C9)
CT9 (C8)
CT8 (C7)

(G20) T1
(B11) ROR 5 (DEC)
U88D

U138
ENABLE

(A30) M11
(A30) M10
(A30) M9
(A30) M8

U161 D0 D1 D2 D3 4-BIT BINARY UP/DOWN COUNTER
LOAD
CLOCK
CLOCK ENABLE
DN/UP
CARRY MAX/MIN
Q0 Q1 Q2 Q3

CT7 (C7)
CT6 (C6)
CT5 (C5)
CT4 (C5)

(F20) LB
(D31) 0
U131D
U131C

U171A
CO (G25)

COUNTER GATES

(E20) UB

(H30) M7
(G30) M6
(G30) M5
(G30) M4

U191 D0 D1 D2 D3 4-BIT BINARY UP/DOWN COUNTER
LOAD
CLOCK
CLOCK ENABLE
DN/UP
CARRY MAX/MIN
Q0 Q1 Q2 Q3

CT3 (C4)
CT2 (C3)
CT1 (C3)
CT0 (C2)

U134
ENABLE

(H30) M3
(H30) M2
(H30) M1
(H30) M0
(MSB)

U181 D0 D1 D2 D3 4-BIT BINARY UP/DOWN COUNTER
LOAD
CLOCK
CLOCK ENABLE
DN/UP
CARRY MAX/MIN
Q0 Q1 Q2 Q3

IMMEDIATE OPERAND GATES

U94
ENABLE

A BUS

(B19) ROR 12
(B19) ROR 13
(B19) ROR 14
(B19) ROR 15
(B19) ROR 16
(C19) ROR 17
(C19) ROR 18
(C19) ROR 19

A7(F31)(F40)
A6(F31)(F40)
A5(F31)(F40)
A4(F31)(F40)
A3(E31)(E40)
A2(E31)(E40)
A1(E31)(E40)

GATE SELECT LOGIC

U64F
B GATES SELECT

(G27) F
(C19) W
(C19) V
DATA 1-TO-4 MULTIPLEXER U87 2^0 2^1 Q0 Q1 Q2 Q3
H (F37)
J (F34)
K (F36)
L (F33)

(G11) ARS
(C19) T
(C19) U
DATA 1-TO-4 MULTIPLEXER U86 2^0 2^1 Q0 Q1 Q2 Q3
M (F40)
N (F39)
P (F32)

A GATES SELECT

ALU

U177 A0 A1 A2 A3 B0 B1 B2 B3 FUNCTION GENERATOR CARRY IN MODE S0 S1 S2 S3 CARRY OUT A=B F0 F1 F2 F3 CP CG

(C37) B15
(C37) B14
(C37) B13
(C37) B12
(D11) C15

U167 A0 A1 A2 A3 B0 B1 B2 B3 FUNCTION GENERATOR CARRY IN MODE S0 S1 S2 S3 CARRY OUT A=B F0 F1 F2 F3 CP CG

(C37) B11
(D37) B10
(D37) B9
(D37) B8

U127 A0 A1 A2 A3 B0 B1 B2 B3 FUNCTION GENERATOR CARRY IN MODE S0 S1 S2 S3 CARRY OUT A=B F0 F1 F2 F3 CP CG

(F37) B7
(F37) B6
(F37) B5
(F37) B4

U137 A0 A1 A2 A3 B0 B1 B2 B3 FUNCTION GENERATOR CARRY IN MODE S0 S1 S2 S3 CARRY OUT A=B F0 F1 F2 F3 CP CG

(E37) B3
(E37) B2
(E37) B1
(E37) B0

(C11) M
(C11) S0
(C11) S1
(B11) S2
(C11) S3

HOLDING (T) REGISTER

LOWER BYTE T REG
U197 D12 D13 D14 D15 8-BIT REGISTER Q12 Q13 Q14 Q15
CLEAR
ENABLE 0-3 ENABLE 4-7

C BUS

CLEAR1,13 (G9)
(G18) TC

U147 P0 P1 P2 P3 G0 G1 G2 G3 CARRY GENERATOR Cn+X Cn+Y Cn+Z Cn IN P G

U127 CP CG A0 A1 A2 A3 B0 B1 B2 B3 CARRY OUT A=B FUNCTION GENERATOR F0 F1 F2 F3

UPPER BYTE T REG
U107 D4 D5 D6 D7 8-BIT REGISTER Q4 Q5 Q6 Q7
CLEAR
ENABLE 0-3 ENABLE 4-7

(MSB) C BUS
CLEAR1,13 (G9)

(D23) CO
+5V
R115
U96 D0 D1 D2 D3 D4 D5 6-BIT REGISTER Q0 Q1 Q2 Q3 Q4 Q5
CLOCK
CLEAR
(G20) T4
(C27) F

COV (A15)
OF (A15)
ZRO (A15)
MSB (A15)

CONDITIONAL JUMP REGISTER

T BUS

ROTATE/SHIFT CONTROL

+5V
R10
(G21) F
(G26) ROR 13
(B19) DISP
(F11) ROR 14
(G11) ARS
U85B
U85C
DATA 1-TO-4 MULTIPLEXER U95 2^0 2^1 Q0 Q1 Q2 Q3
SHIFT DECODER

ROTATE CONTROL GATES

U97A
U97C
U97B
U97D
(B19) ROR 12
U88C

ROTATE/SHIFT LOGIC

RIGHT ONE U195 ENABLE
NO SHIFT U185 ENABLE
LEFT ONE U165 ENABLE
LEFT FOUR U155 ENABLE

M15 (B21)(A31)
M14 (B21)(A31)
M13 (B21)(A31)
M12 (C21)(A31)
M11 (C21)(A31)
M10 (C21)(A31)
M9 (C21)(A31)
M8 (D21)(A31)

J3-37 M15
J3-35 M14
J3-33 M13
J3-31 M12
J3-34 M11
J3-36 M10
J3-38 M9
J3-40 M8

LOWER BYTE MIO BUS

LB (E20)

LEFT FOUR U145 ENABLE
NO SHIFT U105 ENABLE
LEFT ONE U135 ENABLE
RIGHT ONE U115 ENABLE

J3-48 M7
J3-46 M6
J3-44 M5
J3-42 M4
J3-43 M3
J3-41 M2
J3-45 M1
J3-47 M0

UPPER BYTE MIO BUS

UB (E20)

M7 (D21)(H31)
M6 (D21)(H31)
M5 (D21)(H31)
M4 (E21)(H31)
M3 (E21)(H31)
M2 (E21)(H31)
M1 (E21)(H31)
M0 (F21)(H31)

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

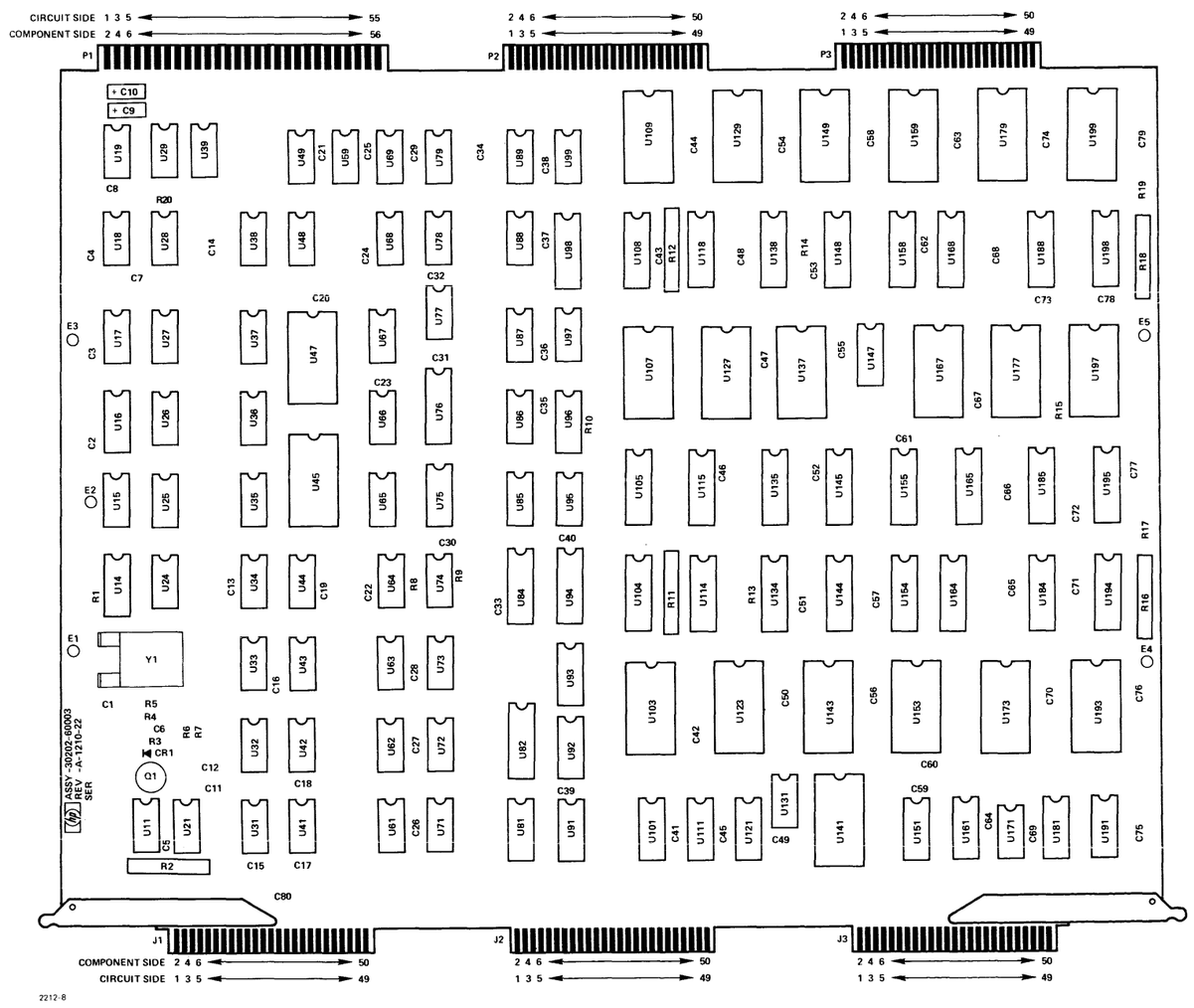
30202-60003 TITLE SHEET 3 OF 4
DISC CONTROLLER PROCESSOR PCA
ENGINEER APPROVED DATE
HEWLETT PACKARD CO

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	$\overline{\text{COM}}$
2	+5V	2	$\overline{\text{COM}}$	2	COM	2	$\overline{\text{CLEAR}}$
3	+5V	3	$\overline{\text{CLK RST}}$	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	$\overline{\text{ALT CK}}$	5	ROM 5	5	$\overline{T_2}$
6		6	$\overline{\text{DISP}}$	6		6	ROR 9
7		7	$\overline{\text{CK CTL}}$	7	ROM 6	7	$\overline{\text{UPPER OUTPUT STROBE}}$
8		8		8		8	$\overline{\text{INPUT STROBE}}$
9		9	ERA 7	9	ROM 7		
10		10		10		9	FLAG 10
11		11	LD ERA	11	ROM 8	10	$\overline{\text{LOWER OUTPUT STROBE}}$
12		12	ERA 11	12			
13		13	ERA 3	13	ROM 9	11	FLAG 14
14		14	ERA 2	14		12	FLAG 12
15	COM	15	ERA 10	15	ROM 10	13	FLAG 16
16	COM	16	ERA 6	16		14	FLAG 15
17		17	AT_0	17	ROM 11	15	ROR 8
18		18	CTL1	18		16	FLAG 17
19	COM	19	AT_3	19	ROM 12	17	ROR 11
20	COM	20	AT_1	20		18	ROR 7
21		21	AT_2	21	ROM 13	19	WORD TYPE ONE
22		22		22			
23		23	CTL2	23	ROM 14	20	ROR 10
24		24	$\overline{\text{UB}}$	24		21	FLAG 13
25		25	$\overline{\text{AM}}$	25	ROM 15	22	FLAG 11
26		26	$\overline{\text{LB}}$	26		23	FLAG 6
27		27	AS2	27	ROM 16	24	FLAG 7
28		28	AS3	28	ROM 0	25	FLAG 4
29	COM	29	AS1	29	ROM 17	26	FLAG 5
30	COM	30	AS0	30	ROM 1	27	FLAG 2
31		31	V	31	ROM 18	28	FLAG 3
32		32	W	32	ROM 2	29	FLAG 0
33		33	T	33	ROM 19	30	FLAG 1
34		34	U	34	ROM 3	31	$\overline{\text{M12}}$
35		35	ERA 1	35		32	**EXT SEL**
36		36		36		33	$\overline{\text{M13}}$
37		37	ERA 5	37	RAR 0	34	$\overline{\text{M11}}$
38		38	ERA 9	38	RAR 1	35	$\overline{\text{M14}}$
39		39	ERA 4	39	RAR 2	36	$\overline{\text{M10}}$
40		40	ERA 0	40	RAR 3	37	$\overline{\text{M15}}$
41		41	ERA 8	41	RAR 4	38	$\overline{\text{M9}}$
42		42		42	RAR 5	39	$\overline{T_1}$
43		43		43	RAR 6	40	$\overline{\text{M8}}$
44		44		44	RAR 7	41	$\overline{\text{M3}}$
45		45	Z	45	RAR 8	42	$\overline{\text{M4}}$
46		46	$\overline{\text{LDRG}}$	46	RAR 9	43	$\overline{\text{M2}}$
47		47	X	47	RAR 10	44	$\overline{\text{M5}}$
48		48	Y	48	RAR 11	45	$\overline{\text{M1}}$
49		49	COM	49	COM	46	$\overline{\text{M6}}$
50		50	COM	50	COM	47	$\overline{\text{M0}}$
51						48	$\overline{\text{M7}}$
52						49	
53						50	COM
54							
55							
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-		1820-	U	1820-
11	0377	47	0495	88	0205	129	0742	167	0606
14	0788	48	0372	89	0372			168	0759
15	0424	49	0377			131	0205		
16	0535			91-93	0788	134	0759	171	0374
17	0512	59	0371	94	0759	135	0755	173	0742
18	0205			95	0843	137	0606	177	0606
19	0239	61-63	0379	96	0788	138	0759	179	0742
		64	0424	97	0205				
21	0142	65	0371	98	0759	141	0640	181	0545
24	0371	66	0372	99	0608	143	0742	184	0759
25	0370	67	0375			144	0759	185	0755
26	0376	68	0205	101	0545	145	0755	188	0759
27	0424	69	0376	103	0742	147	0611		
28	0376			104	0759	148	0759	191	0545
29	0535	71-73	0379	105	0755	149	0742	193	0742
		74	0512	107	0742			194	0759
31-33	0379	75	0788	108	0759	151	0545	195	0755
34	0140	76	0759	109	0742	153	0742	197	0742
35	0384	77	0205			154	0759	198	0759
36	0371	78	0282	111	0545	155	0755	199	0742
37	0141	79	0140	114	0759	158	0759		
38	0140			115	0755	159	0742		
39	0512	81	0788	118	0759				
		82	0759			161	0545		
41-43	0379	84	0759	121	0545				
44	0140	85	0371	123	0742	164	0759		
45	0495	86,87	0843	127	0606	165	0755		



2212-8

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

(A30) M15
(A30) M14
(A30) M13
(A30) M12
(A30) M11
(A30) M10
(A30) M9
(A30) M8
(G9) CLEAR
(F20) LB

OWER BYTE MIO BUS

15V ← P1-1,2,3,4 — C1-5,7-8,11-15, .01UF 79. — +5V — C9,10 2.2UF
COM ← J1-1,2,49,50
COM ← J2-1,2,49,50
COM ← J3-1,50
COM ← P1-15,16,19,20,29,30

8-BIT REGISTER U149 — RG3 — CLEAR — ENABLE 0-3 — ENABLE 4-7
8-BIT REGISTER U159 — RG0
8-BIT REGISTER U179 — RG1
8-BIT REGISTER U199 — RG2
8-BIT REGISTER U109 — RG4
8-BIT REGISTER U129 — RG5

U168 ENABLE
U188 ENABLE
U198 ENABLE
U108 ENABLE
U118 ENABLE

A BUS
(B24) A8
(A24) A9
(A24) A10
(A24) A11
(A24) A12
(A24) A13
(A24) A14
(A24) A15
U148 ENABLE
U158 ENABLE
B BUS
B8 (C25)
B9 (C25)
B10 (C25)
B11 (C25)
B12 (B25)
B13 (B25)
B14 (B25)
B15 (B25)
R18F R19 R18E R18G +5V
R18B R18C R18A R18D +5V
R12F R14 R12C R12B +5V
A BUS
A8 (B24)
A9 (A24)
A10 (A24)
A11 (A24)
A12 (A24)
A13 (A24)
A14 (A24)
A15 (A24)
R12A R12E R12G R12D +5V

(E20) LB
(D21) G
(C19) X
(C19) Y
(C19) Z
(D18) CLD
U99 2¹ 2² BINARY TO OCTAL DECODER ENABLE
EXT SEL ← J3-32

R16C R16E R16F R16D +5V
R16A R16G R16B R17 +5V
R11F R13 R11B R11AG +5V
R11C R11E R11A R11D +5V

(G24) A0
(G24) A1
(G24) A2
(G24) A3
(G24) A4
(G24) A5
(G24) A6
(G24) A7
U144 ENABLE
U154 ENABLE
A BUS
B BUS
(H22) P
L (H22)
U164 ENABLE
U184 ENABLE
U194 ENABLE
U104 ENABLE
U114 ENABLE
J (G22)
K (H22)
H (G22)
N (H22)
M (H22)
B0 (F25)
B1 (F25)
B2 (F25)
B3 (E25)
B4 (E25)
B5 (E25)
B6 (D25)
B7 (D25)
A0 (G24)
A1 (G24)
A2 (G24)
A3 (G24)
A4 (G24)
A5 (G24)
A6 (G24)
A7 (G24)
(E20) B
(E20) UB

8-BIT REGISTER U143 — RG3 — ENABLE 4-7 — ENABLE 0-3 — CLEAR
8-BIT REGISTER U153 — RG0
8-BIT REGISTER U173 — RG1
8-BIT REGISTER U193 — RG2
8-BIT REGISTER U103 — RG4
8-BIT REGISTER U123 — RG5

(G9) CLEAR
(H30) M0
(H30) M1
(H30) M2
(H30) M3
(G30) M4
(G30) M5
(G30) M6
(H30) M7

UPPER BYTE MIO BUS

30202-60003	TITLE	SHEET 4 OF 4
DISC CONTROLLER PROCESSOR PCA		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO		
[illegible] SYSTEMS [illegible] DIVISION		

I/O DETAILED DIAGRAM SET

DD-607

MAGNETIC TAPE (9 TRACK) CONTROLLER PCA

30215-60001

SERIES 1250

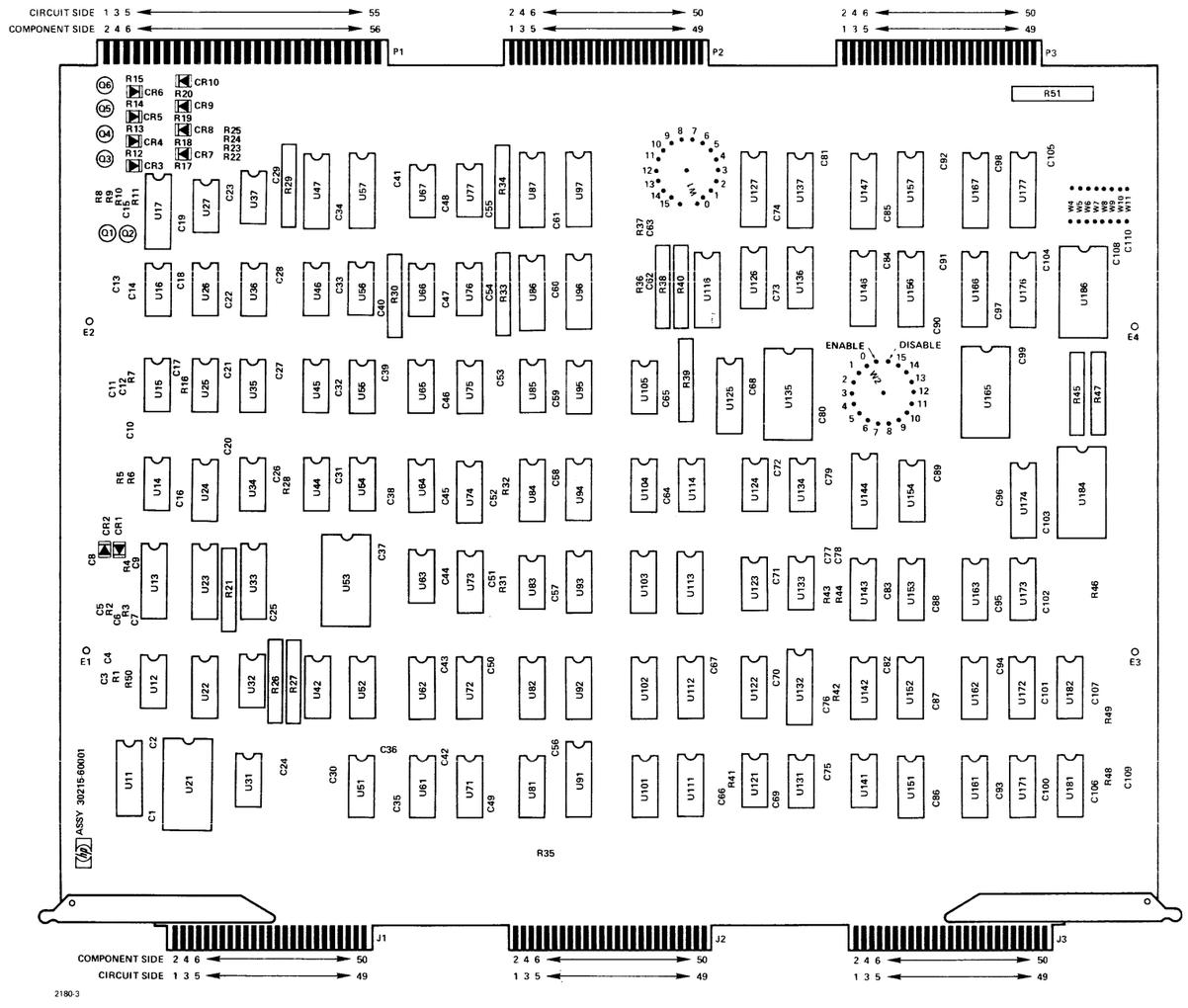
1305

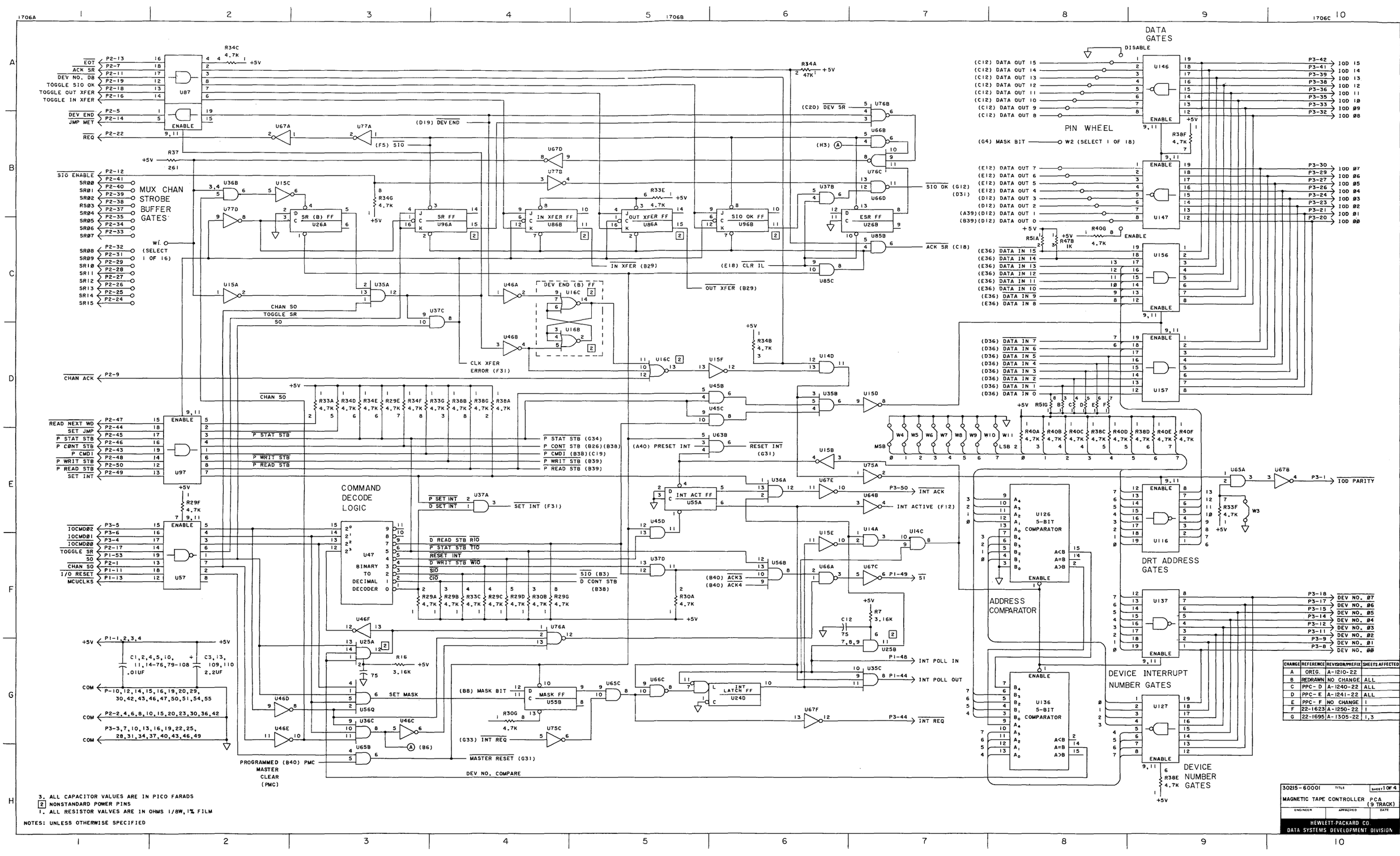
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1		1		1	
2	+5V	2	COM	2	IOD PE	2	SINGLE TRK ERROR	2		2	CLR
3	+5V	3	SR CLOCK	3	COM	3	CS0	3	ROM 04	3	
4	+5V	4	COM	4	IOCMD 00	4	CS1	4		4	
5	PF WARN	5	DEV END	5	IOCMD 02	5	CS2	5	ROM 05	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	CS3	6		6	ROR 09
7	(SPARE)	7	ACK SR	7	COM	7	EOB	7	ROM 06	7	UP STB
8	(SPARE)	8	COM	8	DEVNO 00	8		8		8	INPSTB
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	RDP	9	ROM 07	9	RD CLK
10	COM	10	COM	10	COM	10	WDP	10		10	LOW STB
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	WR STAT	11	ROM 08	11	DATA FF
12	COM	12	SIO ENABLE	12	DEVNO 03	12	800/1600	12		12	OUT-XFER
13	MCUCLKS	13	EOT	13	COM	13	PNT	13	ROM 09	13	IN-XFER
14	COM	14	JMP MET	14	DEVNO 04	14	RDY	14		14	INTER
15	COM	15	COM	15	DEVNO 05	15	FILE PROT	15	ROM 10	15	ROR 08
16	COM	16	TOGGLE INXFER	16	COM	16	EOT	16		16	CMO ENB
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	FWD	17	ROM 11	17	ROR 11
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	REV	18		18	ROR 07
19	COM	19	TOGGLE SIO OK	19	COM	19	WRITE	19	ROM 12	19	
20	COM	20	COM	20	IOD 00	20	OFF-LINE	20		20	ROR 10
21	+15V	21	XFER ERROR	21	IOD 01	21	REWIND	21	ROM 13	21	READY
22	+15V	22	REQ	22	COM	22	WRRST	22		22	TAPE ERR
23	+15V	23	COM	23	IOD 02	23		23	ROM 14	23	R/W PARITY
24	+15V	24	SR 15	24	IOD 03	24		24		24	EOB
25	-15V	25	SR 14	25	COM	25		25	ROM 15	25	800/1600 BPI
26	-15V	26	SR 13	26	IOD 04	26		26		26	WRITE STATUS
27	-15V	27	SR 12	27	IOD 05	27		27	ROM 16	27	FLG 2
28	-15V	28	SR 11	28	COM	28		28	ROM 00	28	BOT
29	COM	29	SR 10	29	IOD 06	29		29	ROM 17	29	FLG 0
30	COM	30	COM	30	IOD 07	30		30	ROM 01	30	FLG 1
31	-20V	31	SR 9	31	COM	31		31	ROM 18	31	M12
32	-20V	32	SR 8	32	IOD 08	32		32	ROM 02	32	
33	-20V	33	SR 7	33	IOD 09	33		33	ROM 19	33	M13
34	-20V	34	SR 6	34	COM	34		34	ROM 03	34	M11
35	+20V	35	SR 5	35	IOD 10	35		35		35	M14
36	+20V	36	COM	36	IOD 11	36		36	ROM ENABLE	36	M10
37	+20V	37	SR 4	37	COM	37		37	A00	37	M15
38	+20V	38	SR 3	38	IOD 12	38		38	A01	38	M09
39	+20V	39	SR 2	39	IOD 13	39		39	A02	39	
40	+20V	40	SR 1	40	COM	40		40	A03	40	M08
41	HSREQ	41	SR 0	41	IOD 14	41		41	A04	41	M03
42	COM	42	COM	42	IOD 15	42		42	A05	42	M04
43	COM	43	P CMD 1	43	COM	43		43	A06	43	M02
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44		44	A07	44	M05
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45		45	A08	45	M01
46	COM	46	P CONT STB	46	COM	46		46	A09	46	M06
47	COM	47	RD NEXT WD	47	(SPARE)	47		47	A10	47	M00
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48		48	A11	48	M07
49	SI	49	SET INT	49	COM	49		49		49	
50	COM	50	P READ STB	50	INTACK	50		50		50	
51	COM										
52	DATAPOLL OUT										
53	SO										
54	COM										
55	COM										
56	DATAPOLL IN										

I.C. INDEX

U	18XX	U	1820-	U	1820-	U	1820-	U	1820-
	1810-	11	0755	45	0141	91	0755	141	0141
73	0037	12	0661	46	0424	94	0715	142	0715
93	0037	13	0756	47	0491	95	0371	143	0515
122	0037	14	0141	53	0742	96	0715	144	0756
		15	0424	54	0141	97	0759	146,147	0760
	1816-	16	0900	55	0077	114	0077	151-153	0715
42	0221	17	0724	56	0374	116	0756	154	0724
51	0220	21	0742	57	0760	121	0424	155,156	0755
52	0206	22	0515	63	0372	123	0370	161,162	0715
61	0222	23	0756	64	0424	124	0424	163	0657
62	0229	24	0626	65	0141	125	0756	165	0742
71	0223	25	0844	66	0370	126	0706	166,167	0756
72	0225	26	0077	67	0761	127	0760	171-173	0715
81	0224	27	0613	74	0715	131	0141	174	0756
82	0212	31,32	0435	75	0424	132	0756	176,177	0755
92	0226	33	0756	76	0371	133	0661	181,182	0715
111	0218	34	0424	77	0424	134	0370	184,186	0742
112	0203	35	0685	83	0077	135	0742		
113	0219	36	0372	84	0715	136	0706		
		37	0141	85	0141	137	0756		
		44	0378	85	0715				
				87	0759				





CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	
B	REDRAWN	NO CHANGE	ALL
C	PPC- D	A-1240-22	ALL
D	PPC- E	A-1241-22	ALL
E	PPC- F	NO CHANGE	1
F	22-1623	A-1250-22	1
G	22-1695	A-1305-22	1,3

3. ALL CAPACITOR VALUES ARE IN PICO FARADS
2 NONSTANDARD POWER PINS
1. ALL RESISTOR VALUES ARE IN OHMS 1/8W, 1% FILM

NOTES: UNLESS OTHERWISE SPECIFIED

30215-60001 TITLE SHEET 1 OF 4

MAGNETIC TAPE CONTROLLER PCA (9 TRACK)

ENGINEER | APPROVED | DATE

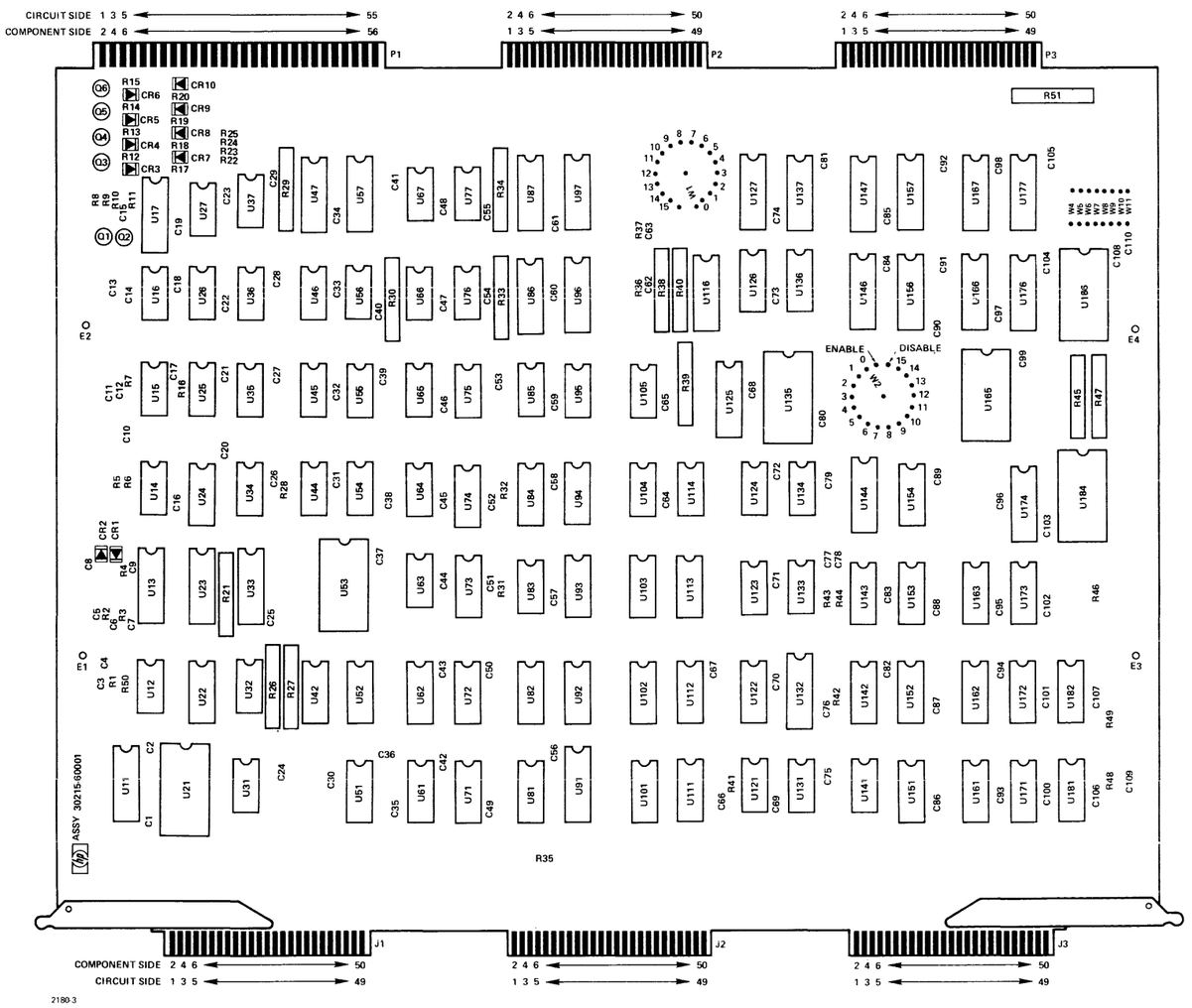
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1		1		1	
2	+5V	2	COM	2	IOD PE	2	SINGLE TRK ERROR	2		2	CLR
3	+5V	3	SR CLOCK	3	COM	3	CS0	3	ROM 04	3	
4	+5V	4	COM	4	IOCMD 00	4	CS1	4		4	
5	PF WARN	5	DEV END	5	IOCMD 02	5	CS2	5	ROM 05	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	CS3	6		6	ROR 09
7	(SPARE)	7	ACK SR	7	COM	7	EOB	7	ROM 06	7	UP STB
8	(SPARE)	8	COM	8	DEVNO 00	8		8		8	INPSTB
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	RDP	9	ROM 07	9	RD CLK
10	COM	10	COM	10	COM	10	WDP	10		10	LOW STB
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	WR STAT	11	ROM 08	11	DATA FF
12	COM	12	SIO ENABLE	12	DEVNO 03	12	800/1600	12		12	OUT-XFER
13	MCUCLKS	13	EOT	13	COM	13	PNT	13	ROM 09	13	IN-XFER
14	COM	14	JMP MET	14	DEVNO 04	14	RDY	14		14	INTER
15	COM	15	COM	15	DEVNO 05	15	FILE PROT	15	ROM 10	15	ROR 08
16	COM	16	TOGGLE INXFER	16	COM	16	EOT	16		16	CMO ENB
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	FWD	17	ROM 11	17	ROR 11
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	REV	18		18	ROR 07
19	COM	19	TOGGLE SIO OK	19	COM	19	WRITE	19	ROM 12	19	
20	COM	20	COM	20	IOD 00	20	OFF-LINE	20		20	ROR 10
21	+15V	21	XFER ERROR	21	IOD 01	21	REWIND	21	ROM 13	21	READY
22	+15V	22	REQ	22	COM	22	WRRST	22		22	TAPE ERR
23	+15V	23	COM	23	IOD 02	23		23	ROM 14	23	R/W PARITY
24	+15V	24	SR 15	24	IOD 03	24		24		24	EOB
25	-15V	25	SR 14	25	COM	25		25	ROM 15	25	800/1600 BPI
26	-15V	26	SR 13	26	IOD 04	26		26		26	WRITE STATUS
27	-15V	27	SR 12	27	IOD 05	27		27	ROM 16	27	FLG 2
28	-15V	28	SR 11	28	COM	28		28	ROM 00	28	BOT
29	COM	29	SR 10	29	IOD 06	29	ID BURST	29	ROM 17	29	FLG 0
30	COM	30	COM	30	IOD 07	30	WRCLK	30	ROM 01	30	FLG 1
31	-20V	31	SR 9	31	COM	31	TAPE ERROR	31	ROM 18	31	M12
32	-20V	32	SR 8	32	IOD 08	32	TAPE MARK	32	ROM 02	32	
33	-20V	33	SR 7	33	IOD 09	33	WRITE DATA 0	33	ROM 19	33	M13
34	-20V	34	SR 6	34	COM	34	WRITE DATA 1	34	ROM 03	34	M11
35	+20V	35	SR 5	35	IOD 10	35	WRITE DATA 6	35		35	M14
36	+20V	36	COM	36	IOD 11	36	WRITE DATA 7	36	ROM ENABLE	36	M10
37	+20V	37	SR 4	37	COM	37	WRITE DATA 4	37	A00	37	M15
38	+20V	38	SR 3	38	IOD 12	38	WRITE DATA 5	38	A01	38	M09
39	+20V	39	SR 2	39	IOD 13	39	WRITE DATA 2	39	A02	39	
40	+20V	40	SR 1	40	COM	40	WRITE DATA 3	40	A03	40	M08
41	HSREQ	41	SR 0	41	IOD 14	41	READ DATA 6	41	A04	41	M03
42	COM	42	COM	42	IOD 15	42	READ DATA 7	42	A05	42	M04
43	COM	43	P CMD 1	43	COM	43	READ DATA 4	43	A06	43	M02
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44	READ DATA 5	44	A07	44	M05
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45	READ DATA 2	45	A08	45	M01
46	COM	46	P CONT STB	46	COM	46	READ DATA 3	46	A09	46	M06
47	COM	47	RD NEXT WD	47	(SPARE)	47	READ DATA 0	47	A10	47	M00
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48	READ DATA 1	48	A11	48	M07
49	SI	49	SET INT	49	COM	49		49		49	
50	COM	50	P READ STB	50	INTACK	50		50		50	
51	COM										
52	DATAPOLL OUT										
53	SO										
54	COM										
55	COM										
56	DATAPOLL IN										

I.C. INDEX

U	18XX-	U	1820-	U	1820-	U	1820-	U	1820-
	1810-	11	0755	45	0141	91	0755	141	0141
73	0037	12	0661	46	0424	94	0715	142	0715
93	0037	13	0756	47	0491	95	0371	143	0515
122	0037	14	0141	53	0742	96	0715	144	0756
		15	0424	54	0141	97	0759	146,147	0760
	1816-	16	0900	55	0077	114	0077	151-153	0715
42	0221	17	0724	56	0374	116	0756	154	0724
51	0220	21	0742	57	0760	121	0424	155,156	0755
52	0206	22	0515	63	0372	123	0370	161,162	0715
61	0222	23	0756	64	0424	124	0424	163	0657
62	0229	24	0626	65	0141	125	0756	165	0742
71	0223	25	0844	66	0370	126	0706	166,167	0756
72	0225	26	0077	67	0761	127	0760	171-173	0715
81	0224	27	0613	74	0715	131	0141	174	0756
82	0212	31,32	0435	75	0424	132	0756	176,177	0755
92	0226	33	0756	76	0371	133	0661	181,182	0715
111	0218	34	0424	77	0424	134	0370	184,186	0742
112	0203	35	0685	83	0077	135	0742		
113	0219	36	0372	84	0715	136	0706		
		37	0141	85	0141	137	0756		
		44	0378	85	0715				
				87	0759				



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1240-22
D	PPC-E	A-1241-22
E	PPC-F	NO CHANGE
F	22-1623	A-1250-22
G	22-1695	A-1305-22

30215-60001 TITLE SHEET 2 OF 4

MAGNETIC TAPE CONTROLLER PCA (9 TRACK)

ENGINEER | APPROVED | DATE

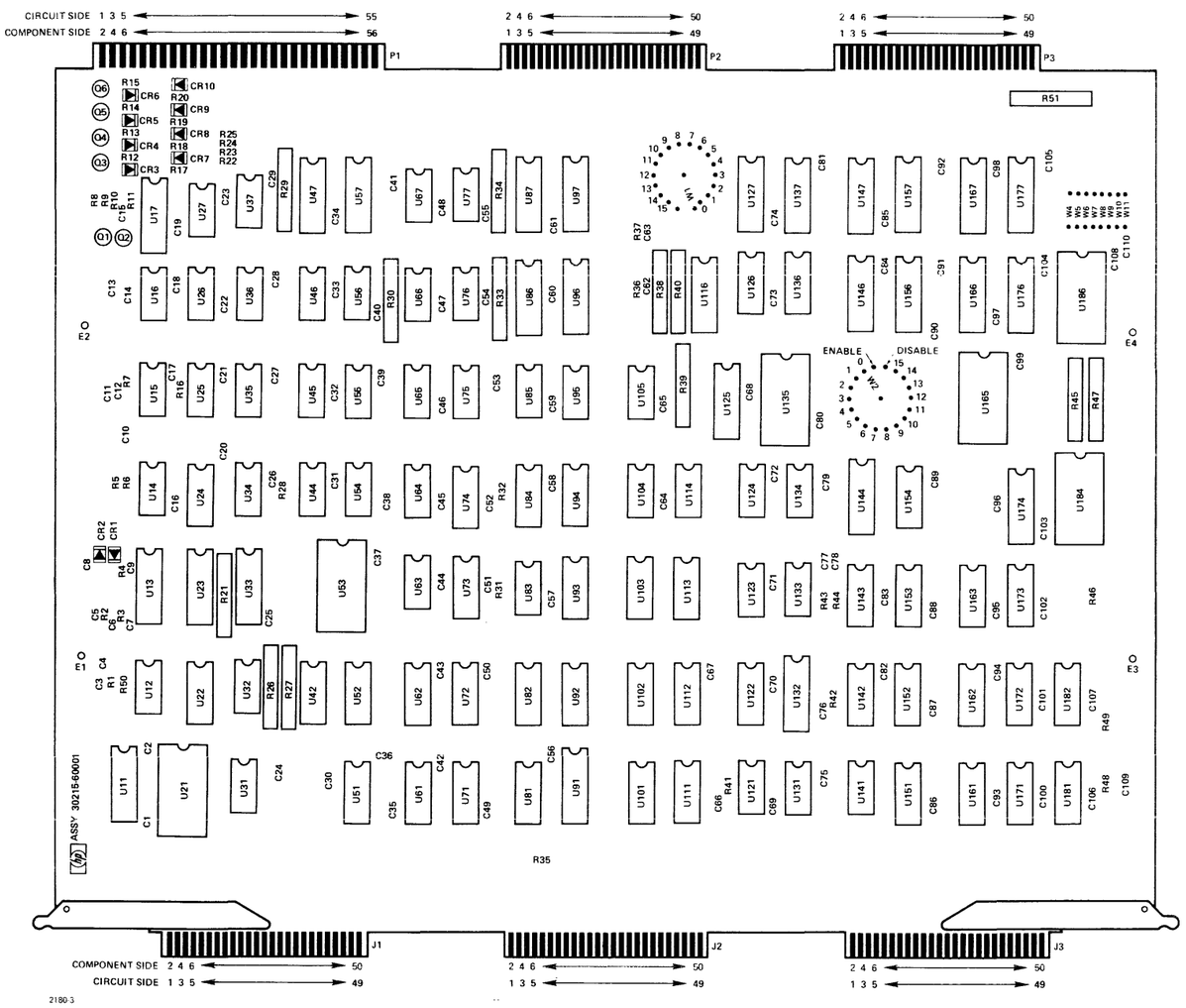
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

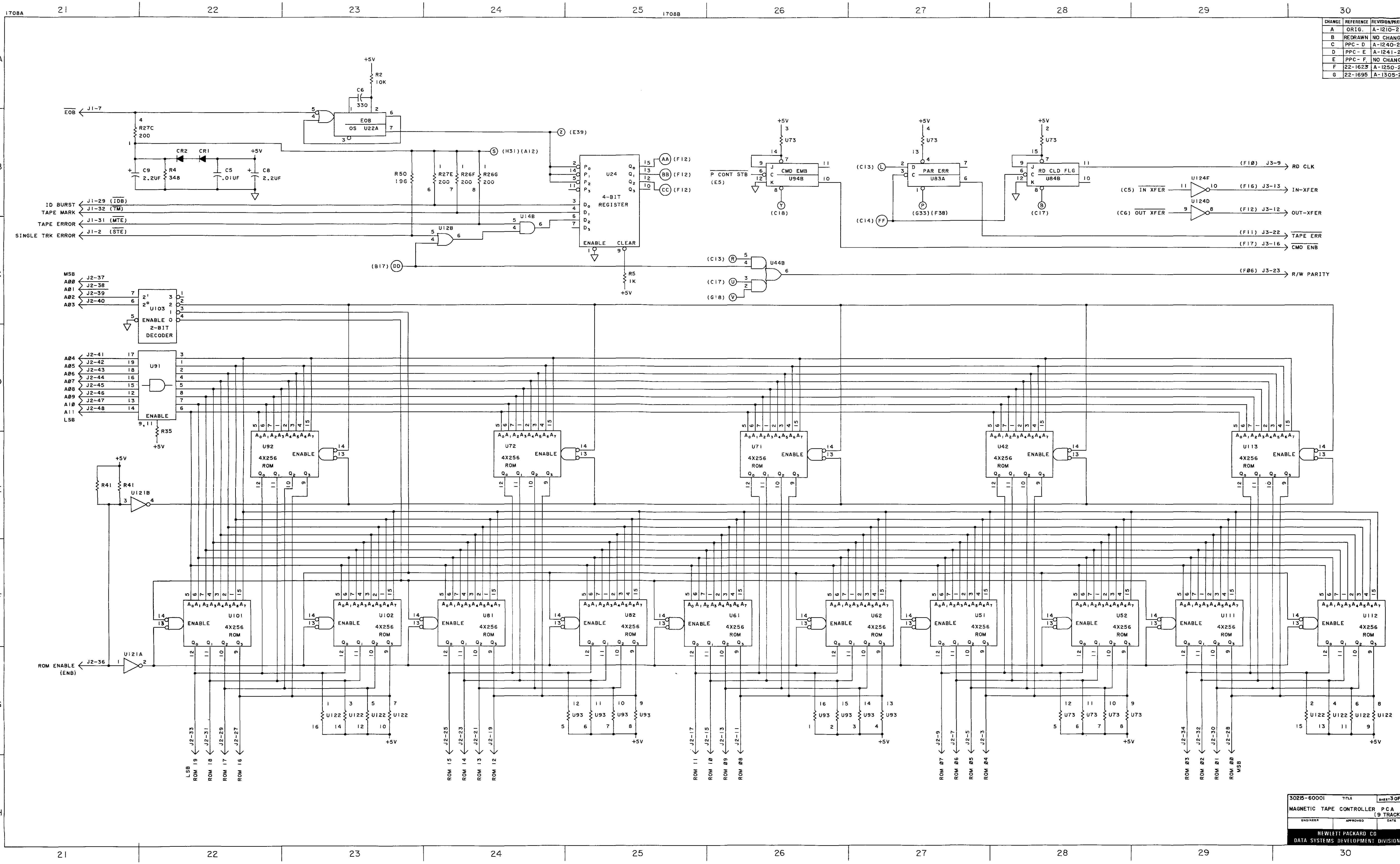
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1		1		1	
2	+5V	2	COM	2	IOD PE	2	SINGLE TRK ERROR	2		2	CLR
3	+5V	3	SR CLOCK	3	COM	3	CS0	3	ROM 04	3	
4	+5V	4	COM	4	IOCMD 00	4	CS1	4		4	
5	PF WARN	5	DEV END	5	IOCMD 02	5	CS2	5	ROM 05	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	CS3	6		6	ROR 09
7	(SPARE)	7	ACK SR	7	COM	7	EOB	7	ROM 06	7	UP STB
8	(SPARE)	8	COM	8	DEVNO 00	8		8		8	INPSTB
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	RDP	9	ROM 07	9	RD CLK
10	COM	10	COM	10	COM	10	WDP	10		10	LOW STB
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	WR STAT	11	ROM 08	11	DATA FF
12	COM	12	SIO ENABLE	12	DEVNO 03	12	800/1600	12		12	OUT-XFER
13	MCUCLKS	13	EOT	13	COM	13	PNT	13	ROM 09	13	IN-XFER
14	COM	14	JMP MET	14	DEVNO 04	14	RDY	14		14	INTER
15	COM	15	COM	15	DEVNO 05	15	FILE PROT	15	ROM 10	15	ROR 08
16	COM	16	TOGGLE INXFER	16	COM	16	EOT	16		16	CMO ENB
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	FWD	17	ROM 11	17	ROR 11
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	REV	18		18	ROR 07
19	COM	19	TOGGLE SIO OK	19	COM	19	WRITE	19	ROM 12	19	
20	COM	20	COM	20	IOD 00	20	OFF-LINE	20		20	ROR 10
21	+15V	21	XFER ERROR	21	IOD 01	21	REWIND	21	ROM 13	21	READY
22	+15V	22	REQ	22	COM	22	WRRST	22		22	TAPE ERR
23	+15V	23	COM	23	IOD 02	23		23	ROM 14	23	R/W PARITY
24	+15V	24	SR 15	24	IOD 03	24		24		24	EOB
25	-15V	25	SR 14	25	COM	25		25	ROM 15	25	800/1600 BPI
26	-15V	26	SR 13	26	IOD 04	26		26		26	WRITE STATUS
27	-15V	27	SR 12	27	IOD 05	27		27	ROM 16	27	FLG 2
28	-15V	28	SR 11	28	COM	28		28	ROM 00	28	BOT
29	COM	29	SR 10	29	IOD 06	29	ID BURST	29	ROM 17	29	FLG 0
30	COM	30	COM	30	IOD 07	30	WRCLK	30	ROM 01	30	FLG 1
31	-20V	31	SR 9	31	COM	31	TAPE ERROR	31	ROM 18	31	M12
32	-20V	32	SR 8	32	IOD 08	32	TAPE MARK	32	ROM 02	32	
33	-20V	33	SR 7	33	IOD 09	33	WRITE DATA 0	33	ROM 19	33	M13
34	-20V	34	SR 6	34	COM	34	WRITE DATA 1	34	ROM 03	34	M11
35	+20V	35	SR 5	35	IOD 10	35	WRITE DATA 6	35		35	M14
36	+20V	36	COM	36	IOD 11	36	WRITE DATA 7	36	ROM ENABLE	36	M10
37	+20V	37	SR 4	37	COM	37	WRITE DATA 4	37	A00	37	M15
38	+20V	38	SR 3	38	IOD 12	38	WRITE DATA 5	38	A01	38	M09
39	+20V	39	SR 2	39	IOD 13	39	WRITE DATA 2	39	A02	39	
40	+20V	40	SR 1	40	COM	40	WRITE DATA 3	40	A03	40	M08
41	HSREQ	41	SR 0	41	IOD 14	41	READ DATA 6	41	A04	41	M03
42	COM	42	COM	42	IOD 15	42	READ DATA 7	42	A05	42	M04
43	COM	43	P CMD 1	43	COM	43	READ DATA 4	43	A06	43	M02
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44	READ DATA 5	44	A07	44	M05
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45	READ DATA 2	45	A08	45	M01
46	COM	46	P CONT STB	46	COM	46	READ DATA 3	46	A09	46	M06
47	COM	47	RD NEXT WD	47	(SPARE)	47	READ DATA 0	47	A10	47	M00
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48	READ DATA 1	48	A11	48	M07
49	SI	49	SET INT	49	COM	49		49		49	
50	COM	50	P READ STB	50	INTACK	50		50		50	
51	COM										
52	DATAPOLL OUT										
53	SO										
54	COM										
55	COM										
56	DATAPOLL IN										

I.C. INDEX

U	18XX-	U	1820-	U	1820-	U	1820-	U	1820-
	1810-	11	0755	45	0141	91	0755	141	0141
73	0037	12	0661	46	0424	94	0715	142	0715
93	0037	13	0756	47	0491	95	0371	143	0515
122	0037	14	0141	53	0742	96	0715	144	0756
		15	0424	54	0141	97	0759	146,147	0760
	1816-	16	0900	55	0077	114	0077	151-153	0715
42	0221	17	0724	56	0374	116	0756	154	0724
51	0220	21	0742	57	0760	121	0424	155,156	0755
52	0206	22	0515	63	0372	123	0370	161,162	0715
61	0222	23	0756	64	0424	124	0424	163	0657
62	0229	24	0626	65	0141	125	0756	165	0742
71	0223	25	0844	66	0370	126	0706	166,167	0756
72	0225	26	0077	67	0761	127	0760	171-173	0715
81	0224	27	0613	74	0715	131	0141	174	0756
82	0212	31,32	0435	75	0424	132	0756	176,177	0755
92	0226	33	0756	76	0371	133	0661	181,182	0715
111	0218	34	0424	77	0424	134	0370	184,186	0742
112	0203	35	0685	83	0077	135	0742		
113	0219	36	0372	84	0715	136	0706		
		37	0141	85	0141	137	0756		
		44	0378	85	0715				
				87	0759				





EOB J1-7
R27C 200
CR2 CR1
C9 2.2UF R4 348 C5 .01UF C8 2.2UF
+5V R2 10K C6 330
EOB OS U22A
(E39)
(H31)(A12)
R50 196 R27E 200 R26F 200 R26G 200
U24 4-BIT REGISTER ENABLE CLEAR
(F12)
ID BURST J1-29 (IDB)
TAPE MARK J1-32 (TM)
TAPE ERROR J1-31 (MTE)
SINGLE TRK ERROR J1-2 (STE)
U12B U14B
(B17)
R5 1K
P CONT STB (E5)
CMD EMB U94B
PAR ERR U83A
RD CLD FLG U84B
U73
(C13) (C14) (C18) (G33)(F38) (C17)
(F10) J3-9 RD CLK
(C5) IN XFER U124F (F16) J3-13 IN-XFER
(C6) OUT XFER U124D (F12) J3-12 OUT-XFER
(F11) J3-22 TAPE ERR
(F17) J3-16 CMO ENB
(C13) (C17) (G18) U44B (F06) J3-23 R/W PARITY
MSB A00 A01 A02 A03 J2-37 J2-38 J2-39 J2-40
U103 ENABLE 2-BIT DECODER
A04 A05 A06 A07 A08 A09 A10 A11 LSB
J2-41 J2-42 J2-43 J2-44 J2-45 J2-46 J2-47 J2-48
U91 ENABLE R35
U92 U72 U71 U42 U113 4X256 ROM ENABLE
R41 U121B
ROM ENABLE (ENB) J2-36 U121A
U101 U102 U81 U82 U61 U62 U51 U52 U111 U112 4X256 ROM ENABLE
U122 U93 U73
J2-33 J2-31 J2-29 J2-27 J2-25 J2-23 J2-21 J2-19 J2-17 J2-15 J2-13 J2-11 J2-9 J2-7 J2-5 J2-3 J2-34 J2-32 J2-30 J2-28
LSB ROM 19 ROM 18 ROM 17 ROM 16 ROM 15 ROM 14 ROM 13 ROM 12 ROM 11 ROM 10 ROM 09 ROM 08 ROM 07 ROM 06 ROM 05 ROM 04 ROM 03 ROM 02 ROM 01 ROM 00 MSB

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1240-22
D	PPC-E	A-1241-22
E	PPC-F	NO CHANGE
F	22-1623	A-1250-22
G	22-1695	A-1305-22

30215-60001 TITLE SHEET 3 OF 4

MAGNETIC TAPE CONTROLLER PCA (9 TRACK)

ENGINEER APPROVED DATE

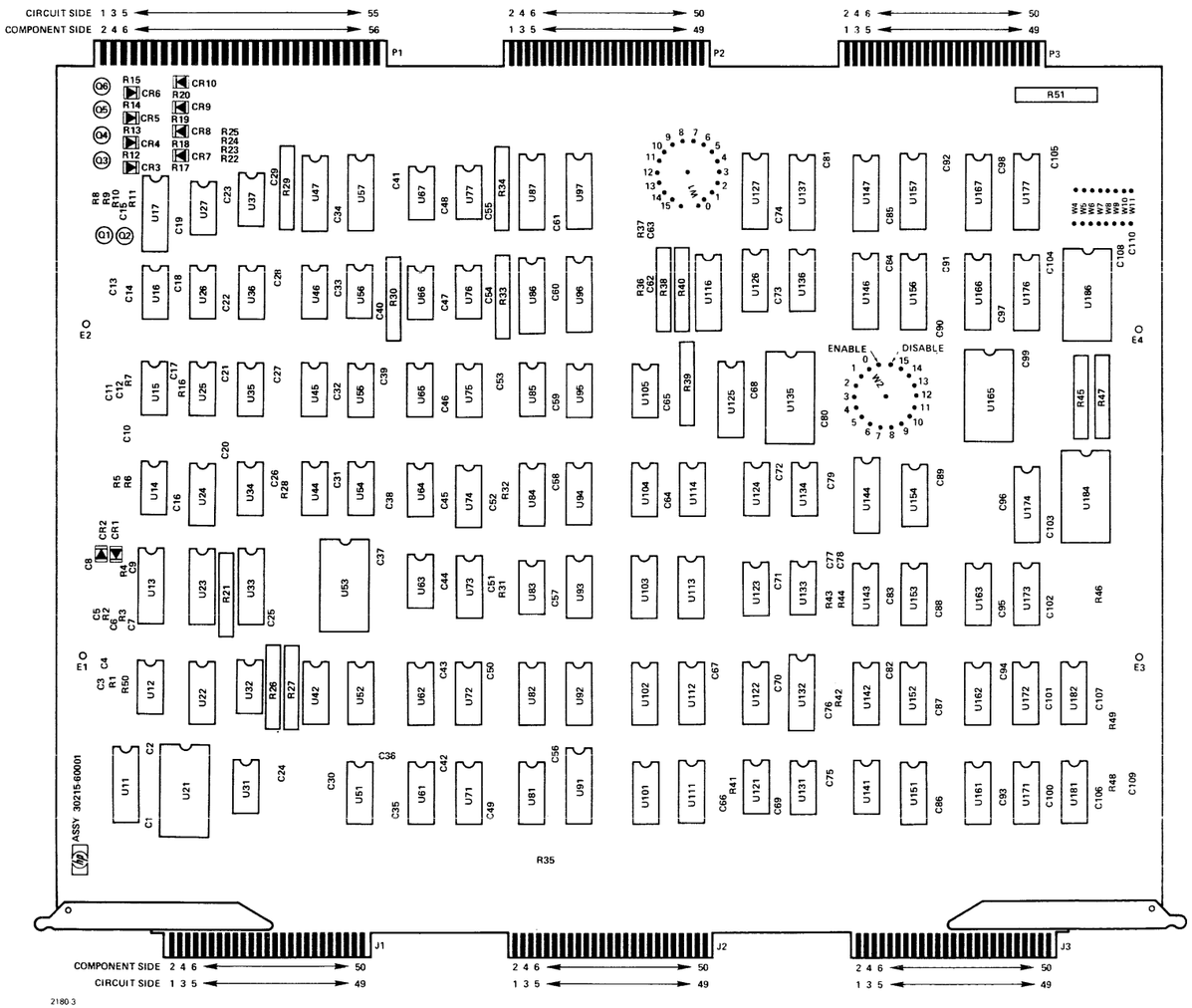
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

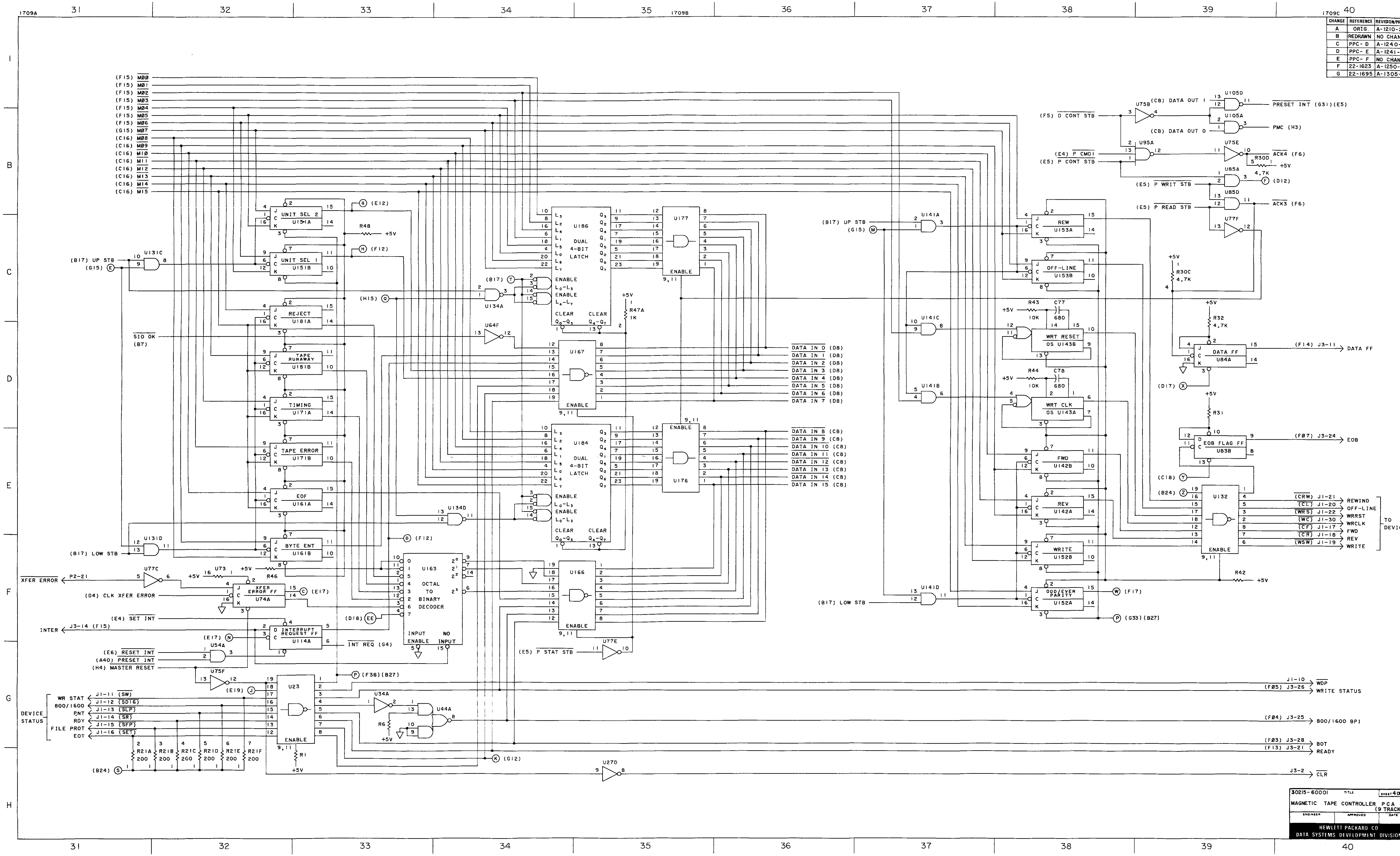
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL	P3 PIN	P3 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	CHAN SO	1	IODPRTY	1		1		1	
2	+5V	2	COM	2	IOD PE	2	SINGLE TRK ERROR	2		2	CLR
3	+5V	3	SR CLOCK	3	COM	3	CS0	3	ROM 04	3	
4	+5V	4	COM	4	IOCMD 00	4	CS1	4		4	
5	PF WARN	5	DEV END	5	IOCMD 02	5	CS2	5	ROM 05	5	
6	ENTIMER	6	COM	6	IOCMD 01	6	CS3	6		6	ROR 09
7	(SPARE)	7	ACK SR	7	COM	7	EOB	7	ROM 06	7	UP STB
8	(SPARE)	8	COM	8	DEVNO 00	8		8		8	INPSTB
9	PWR ON	9	CHAN ACK	9	DEVNO 01	9	RDP	9	ROM 07	9	RD CLK
10	COM	10	COM	10	COM	10	WDP	10		10	LOW STB
11	IORESET	11	DEVNO DB	11	DEVNO 02	11	WR STAT	11	ROM 08	11	DATA FF
12	COM	12	SIO ENABLE	12	DEVNO 03	12	800/1600	12		12	OUT-XFER
13	MCUCLKS	13	EOT	13	COM	13	PNT	13	ROM 09	13	IN-XFER
14	COM	14	JMP MET	14	DEVNO 04	14	RDY	14		14	INTER
15	COM	15	COM	15	DEVNO 05	15	FILE PROT	15	ROM 10	15	ROR 08
16	COM	16	TOGGLE INXFER	16	COM	16	EOT	16		16	CMO ENB
17	-5V	17	TOGGLE SR	17	DEVNO 06	17	FWD	17	ROM 11	17	ROR 11
18	-5V	18	TOGGLE OUTXFER	18	DEVNO 07	18	REV	18		18	ROR 07
19	COM	19	TOGGLE SIO OK	19	COM	19	WRITE	19	ROM 12	19	
20	COM	20	COM	20	IOD 00	20	OFF-LINE	20		20	ROR 10
21	+15V	21	XFER ERROR	21	IOD 01	21	REWIND	21	ROM 13	21	READY
22	+15V	22	REO	22	COM	22	WRRST	22		22	TAPE ERR
23	+15V	23	COM	23	IOD 02	23		23	ROM 14	23	R/W PARITY
24	+15V	24	SR 15	24	IOD 03	24		24		24	EOB
25	-15V	25	SR 14	25	COM	25		25	ROM 15	25	800/1600 BPI
26	-15V	26	SR 13	26	IOD 04	26		26		26	WRITE STATUS
27	-15V	27	SR 12	27	IOD 05	27		27	ROM 16	27	FLG 2
28	-15V	28	SR 11	28	COM	28		28	ROM 00	28	BOT
29	COM	29	SR 10	29	IOD 06	29	ID BURST	29	ROM 17	29	FLG 0
30	COM	30	COM	30	IOD 07	30	WRCLK	30	ROM 01	30	FLG 1
31	-20V	31	SR 9	31	COM	31	TAPE ERROR	31	ROM 18	31	M12
32	-20V	32	SR 8	32	IOD 08	32	TAPE MARK	32	ROM 02	32	
33	-20V	33	SR 7	33	IOD 09	33	WRITE DATA 0	33	ROM 19	33	M13
34	-20V	34	SR 6	34	COM	34	WRITE DATA 1	34	ROM 03	34	M11
35	+20V	35	SR 5	35	IOD 10	35	WRITE DATA 6	35		35	M14
36	+20V	36	COM	36	IOD 11	36	WRITE DATA 7	36	ROM ENABLE	36	M10
37	+20V	37	SR 4	37	COM	37	WRITE DATA 4	37	A00	37	M15
38	+20V	38	SR 3	38	IOD 12	38	WRITE DATA 5	38	A01	38	M09
39	+20V	39	SR 2	39	IOD 13	39	WRITE DATA 2	39	A02	39	
40	+20V	40	SR 1	40	COM	40	WRITE DATA 3	40	A03	40	M08
41	HSREQ	41	SR 0	41	IOD 14	41	READ DATA 6	41	A04	41	M03
42	COM	42	COM	42	IOD 15	42	READ DATA 7	42	A05	42	M04
43	COM	43	P CMD 1	43	COM	43	READ DATA 4	43	A06	43	M02
44	INTPOLLOUT	44	SET JMP	44	INTREQ	44	READ DATA 5	44	A07	44	M05
45	(SPARE)	45	P STATUS STB	45	(SPARE)	45	READ DATA 2	45	A08	45	M01
46	COM	46	P CONT STB	46	COM	46	READ DATA 3	46	A09	46	M06
47	COM	47	RD NEXT WD	47	(SPARE)	47	READ DATA 0	47	A10	47	M00
48	INTPOLL IN	48	P WRITE STB	48	(SPARE)	48	READ DATA 1	48	A11	48	M07
49	SI	49	SET INT	49	COM	49		49		49	
50	COM	50	P READ STB	50	INTACK	50		50		50	
51	COM										
52	DATAPOLL OUT										
53	SO										
54	COM										
55	COM										
56	DATAPOLL IN										

I.C. INDEX

U	18XX-	U	1820-	U	1820-	U	1820-	U	1820-
	1810-	11	0755	45	0141	91	0755	141	0141
73	0037	12	0661	46	0424	94	0715	142	0715
93	0037	13	0756	47	0491	95	0371	143	0515
122	0037	14	0141	53	0742	96	0715	144	0756
		15	0424	54	0141	97	0759	146,147	0760
	1816-	16	0900	55	0077	114	0077	151-153	0715
42	0221	17	0724	56	0374	116	0756	154	0724
51	0220	21	0742	57	0760	121	0424	155,156	0755
52	0206	22	0515	63	0372	123	0370	161,162	0715
61	0222	23	0756	64	0424	124	0424	163	0657
62	0229	24	0626	65	0141	125	0756	165	0742
71	0223	25	0844	66	0370	126	0706	166,167	0756
72	0225	26	0077	67	0761	127	0760	171-173	0715
81	0224	27	0613	74	0715	131	0141	174	0756
82	0212	31,32	0435	75	0424	132	0756	176,177	0755
92	0226	33	0756	76	0371	133	0661	181,182	0715
111	0218	34	0424	77	0424	134	0370	184,186	0742
112	0203	35	0685	83	0077	135	0742		
113	0219	36	0372	84	0715	136	0706		
		37	0141	85	0141	137	0756		
		44	0378	85	0715				
				87	0759				





1709A
1709B
1709C
31 32 33 34 35 36 37 38 39 40
(F15) M00
(F15) M01
(F15) M02
(F15) M03
(F15) M04
(F15) M05
(F15) M06
(G15) M07
(C16) M08
(C16) M09
(C16) M10
(C16) M11
(C16) M12
(C16) M13
(C16) M14
(C16) M15
UNIT SEL 2 U151A
UNIT SEL 1 U151B
REJECT U181A
TAPE RUNAWAY U181B
TIMING U171A
TAPE ERROR U171B
EOF U161A
BYTE ENT U161B
(B17) UP STB
(G15)
U131C
U131D
(B17) LOW STB
SIO OK (B7)
U134A
U64F
U134D
U186 DUAL 4-BIT LATCH
U184 DUAL 4-BIT LATCH
ENABLE L0-L3
ENABLE L4-L7
CLEAR Q0-Q3
CLEAR Q4-Q7
U177
U167
U176
U166
ENABLE
R47A 1K
R48
+5V
(E12)
(F12)
(H15)
U163 OCTAL TO BINARY DECODER
INPUT ENABLE
NO INPUT
XFER ERROR
P2-21
U77C
U73
R46
(D4) CLK XFER ERROR
XFER ERROR FF U74A
(E17)
(E4) SET INT
INTER
J3-14 (F15)
INTERRUPT REQUEST FF U114A
INT REQ (G4)
(D18)
U54A
(E6) RESET INT
(A40) PRESET INT
(H4) MASTER RESET
U75F
(E19)
U23
(F38)(B27)
U34A
U44A
R6
DEVICE STATUS
WR STAT
800/1600
PNT
RDY
FILE PROT
EOT
J1-11 (SW)
J1-12 (SD16)
J1-13 (SLP)
J1-14 (SR)
J1-15 (SFP)
J1-16 (SET)
R21A 200
R21B 200
R21C 200
R21D 200
R21E 200
R21F 200
R1
(B24)
(G12)
U27D
(E5) P STAT STB
U77E
DATA IN 0 (D8)
DATA IN 1 (D8)
DATA IN 2 (D8)
DATA IN 3 (D8)
DATA IN 4 (D8)
DATA IN 5 (D8)
DATA IN 6 (D8)
DATA IN 7 (D8)
DATA IN 8 (C8)
DATA IN 9 (C8)
DATA IN 10 (C8)
DATA IN 11 (C8)
DATA IN 12 (C8)
DATA IN 13 (C8)
DATA IN 14 (C8)
DATA IN 15 (C8)
(B17) UP STB
(G15)
U141A
U141C
U141B
U141D
(B17) LOW STB
REW U153A
OFF-LINE U153B
R43 10K
C77 680
WRT RESET OS U143B
R44 10K
C78 680
WRT CLK OS U143A
FWD U142B
REV U142A
WRITE U152B
ODD/EVEN PARITY U152A
(F17)
(G33)(B27)
(F5) D CONT STB
U75B
(C8) DATA OUT 1
(C8) DATA OUT 0
U105D
U105A
PRESET INT (G31)(E5)
PMC (H3)
(E4) P CMD1
(E5) P CONT STB
U95A
U75E
R30D
ACK4 (F6)
4.7K
U85A
(E5) P WRIT STB
(D12)
U85D
(E5) P READ STB
ACK3 (F6)
U77F
R30C 4.7K
R32 4.7K
DATA FF U84A
(F14) J3-11
DATA FF
(D17)
R31
EOB FLAG FF U83B
(F07) J3-24
EOB
(C18)
(B24)
U132
R42
(CRW) J1-21 REWIND
(CL) J1-20 OFF-LINE
(WRS) J1-22 WRRST
(WC) J1-30 WRCLK
(CF) J1-17 FWD
(CR) J1-18 REV
(WSW) J1-19 WRITE
TO DEVICE
J1-10 WDP
(F05) J3-26 WRITE STATUS
(F04) J3-25 800/1600 BPI
(F03) J3-28 BOT
(F13) J3-21 READY
J3-2 CLR

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	A-1240-22
D	PPC-E	A-1241-22
E	PPC-F	NO CHANGE
F	22-1623	A-1250-22
G	22-1695	A-1305-22

30215-60001 SHEET 4 OF 4

MAGNETIC TAPE CONTROLLER PCA (9 TRACK)

HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

I/O DETAILED DIAGRAM SET

DD-608

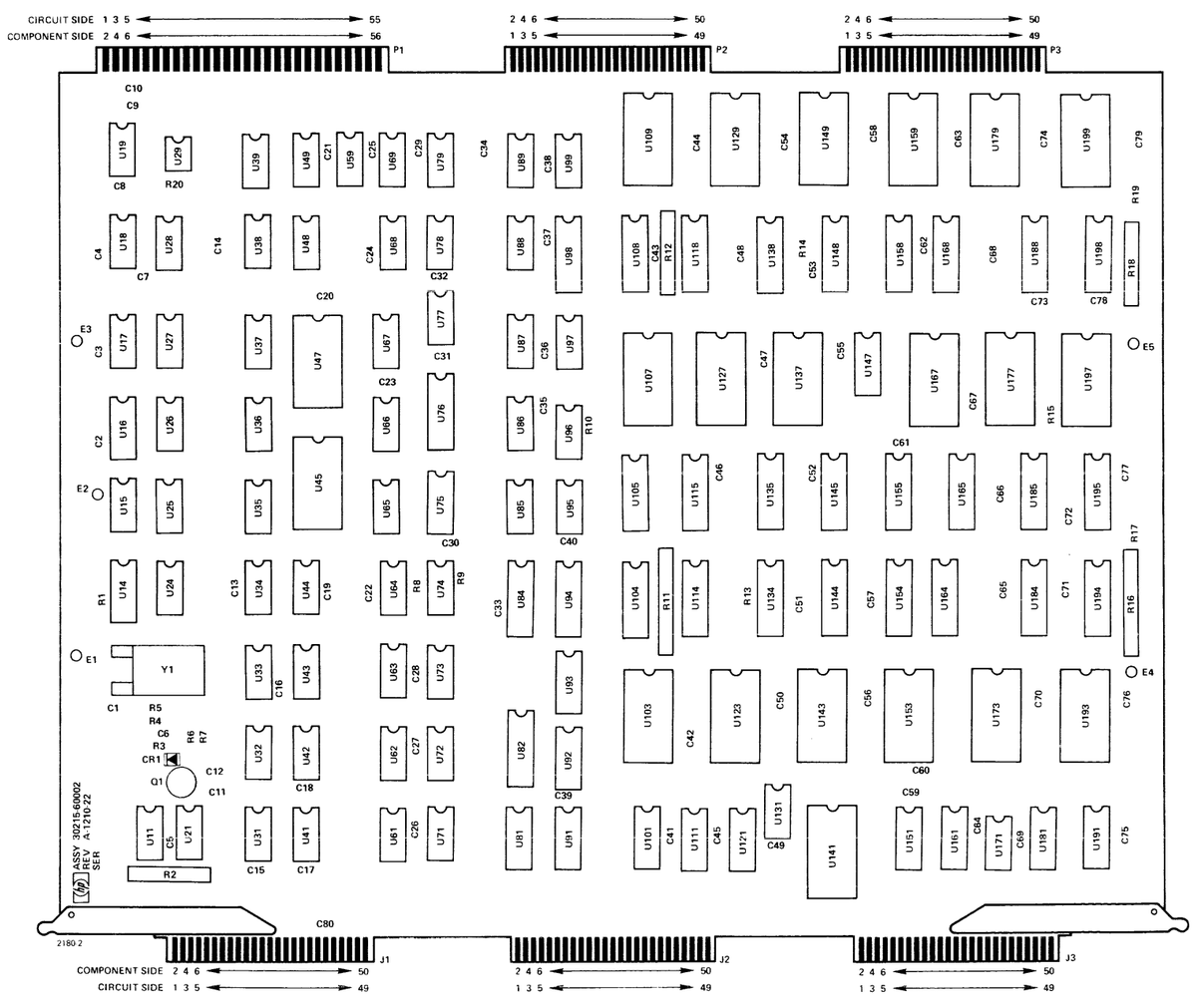
MAGNETIC TAPE CONTROLLER PROCESSOR PCA
30215-60002
SERIES 1210

SIGNAL INDEX

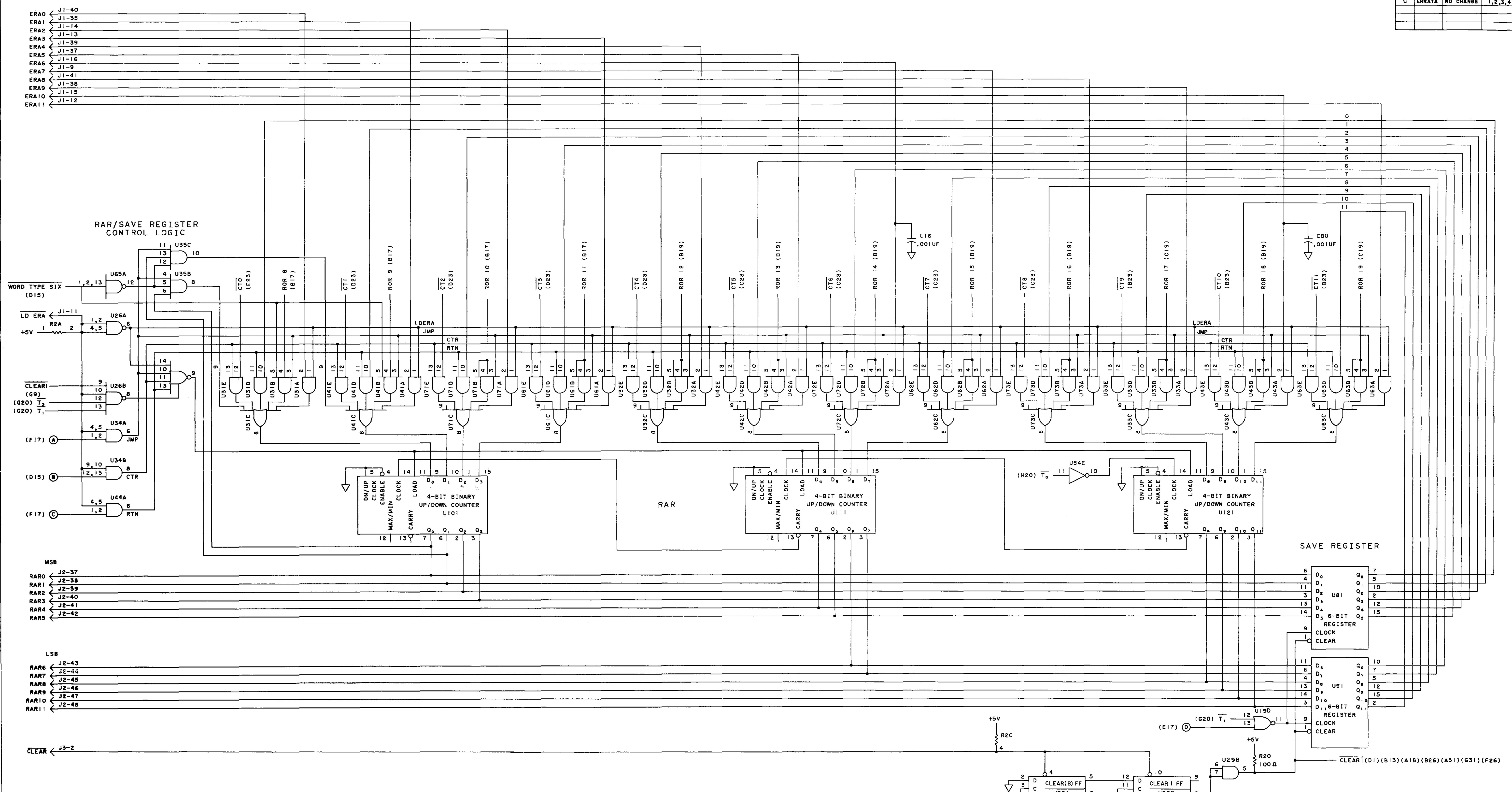
P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	CLEAR
3	+5V	3	CLK RST	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	ALT CK	5	ROM 5	5	$\overline{T_2}$
6		6	DISP	6		6	ROR 9
7		7	CK CTL	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8			
9		9	ERA 7	9	ROM 7	8	INPUT STROBE
10		10		10			
11		11	LD ERA	11	ROM 8	9	FLAG 10
12		12	ERA 11	12		10	LOWER OUTPUT STROBE
13		13	ERA 3	13	ROM 9		
14		14	ERA 2	14			
15	COM	15	ERA 10	15	ROM 10	11	FLAG 14
16	COM	16	ERA 6	16		12	FLAG 12
17		17	AT_0	17	ROM 11	13	FLAG 16
18		18	CTL 1	18		14	FLAG 15
19	COM	19	AT_3	19	ROM 12	15	ROR 8
20	COM	20	AT_1	20		16	FLAG 17
21		21	AT_2	21	ROM 13	17	ROR 11
22		22		22		18	ROR 7
23		23	CTL 2	23	ROM 14	19	WORD TYPE ONE
24		24	$\overline{UB}$	24			
25		25	$\overline{AM}$	25	ROM 15	20	ROR 10
26		26	$\overline{LB}$	26		21	FLAG 13
27		27	AS 2	27	ROM 16	22	FLAG 11
28		28	AS 3	28	ROM 0	23	FLAG 6
29	COM	29	AS 1	29	ROM 17	24	FLAG 7
30	COM	30	AS 0	30	ROM 1	25	FLAG 4
31		31	V	31	ROM 18	26	FLAG 5
32		32	W	32	ROM 2	27	FLAG 2
33		33	T	33	ROM 19	28	FLAG 3
34		34	U	34	ROM 3	29	FLAG 0
35		35	ERA 1	35		30	FLAG 1
36		36		36		31	$\overline{M12}$
37		37	ERA 5	37	RAR 0	32	$\overline{EXT}$ SEL
38		38	ERA 9	38	RAR 1	33	$\overline{M13}$
39		39	ERA 5	39	RAR 2	34	$\overline{M11}$
40		40	ERA 0	40	RAR 3	35	$\overline{M14}$
41		41	ERA 8	41	RAR 4	36	$\overline{M10}$
42		42		42	RAR 5	37	$\overline{M15}$
43		43		43	RAR 6	38	$\overline{M9}$
44		44		44	RAR 7	39	$\overline{T_1}$
45		45	$\overline{Z}$	45	RAR 8	40	$\overline{M8}$
46		46	$\overline{LDRG}$	46	RAR 9	41	$\overline{M3}$
47		47	X	47	RAR 10	42	$\overline{M4}$
48		48	Y	48	RAR 11	43	$\overline{M2}$
49		49	COM	49	COM	44	$\overline{M5}$
50		50	COM	50	COM	45	$\overline{M1}$
51						46	$\overline{M6}$
52						47	$\overline{M0}$
53						48	M7
54						49	
55						50	COM
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1802-
11	0377	36	0371	68	0205	91-93	0788	121	0545	151	0545	181	0545
14	0788	37	0140	69	0376	94	0759	123	0742	153	0742	184	0759
15	0424	38	0140			95	0843	127	0606	154	0759	185	0755
16	0535	39	0512	71-73	0379	96	0788	129	0742	155	0755	188	0759
17	0512			74	0512	97	0205			158	0759		
18	0205	41-43	0379	75	0788	98	0759	131	0205	159	0742	191	0545
19	0239	44	0140	76	0759	99	0608	134	0759			193	0742
		45	0495	77	0205			135	0755	161	0545	194	0759
21	0142	47	0495	78	0282	101	0545	137	0606			195	0755
24	0371	48	0372	79	0140	103	0742	138	0759	164	0759	197	0742
25	0370	49	0377			104	0759			165	0755	198	0759
26	0376			81	0788	105	0755	141	0640	167	0606	199	0742
27	0424	59	0371	82	0759	107	0742	143	0742	168	0759		
28	0376			84	0759	108	0759	144	0759				
29	0535	61-63	0379	85	0371	109	0742	145	0755	171	0374		
		64	0424	86,87	0843			147	0611	173	0742		
31-33	0379	65	0371	88	0205	111	0545	148	0759	177	0606		
34	0140	66	0372	89	0372	114	0759	149	0742	179	0742		
35	0384	67	0375			115	0755						
						118	0759						



CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	ERRATA	NO CHANGE	1,2,3,4



3. ALL LOGIC IS POSITIVE TRUE
2. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1K
1. CRYSTAL FREQUENCY MAY VARY WITH DIFFERENT SUBSYSTEMS
NOTES:

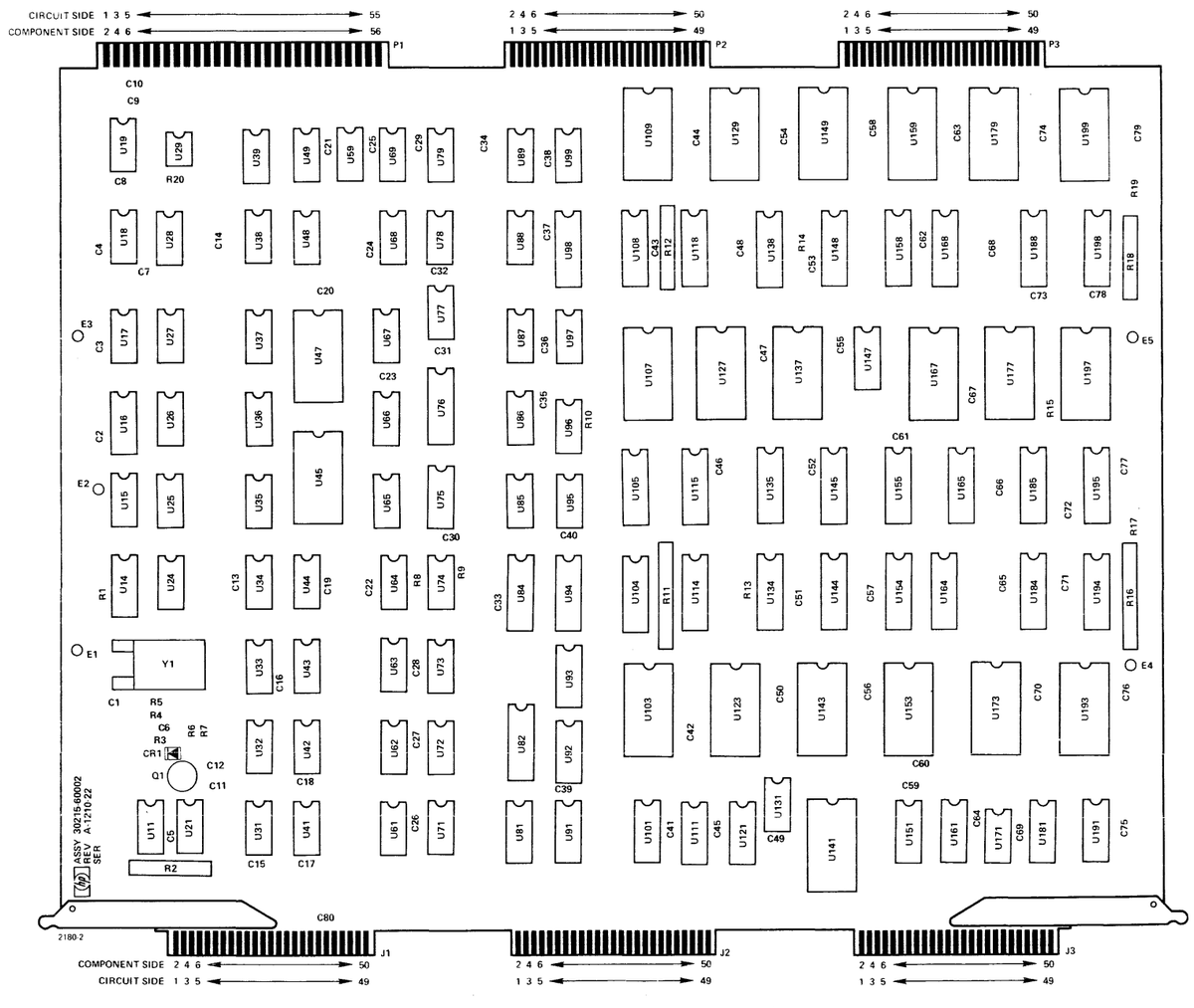
30215-60002 SHEET 1 OF 4
MAGNETIC TAPE CONTROLLER PROCESSOR PCA
ENGINEER APPROVED DATE
HEWLETT PACKARD CO
I/O & SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	CLEAR
3	+5V	3	CLK RST	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	ALT CK	5	ROM 5	5	$\overline{T_2}$
6		6	DISP	6		6	ROR 9
7		7	CK CTL	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8			
9		9	ERA 7	9	ROM 7	8	INPUT STROBE
10		10		10			
11		11	LD ERA	11	ROM 8	9	FLAG 10
12		12	ERA 11	12		10	LOWER OUTPUT STROBE
13		13	ERA 3	13	ROM 9		
14		14	ERA 2	14		11	FLAG 14
15	COM	15	ERA 10	15	ROM 10	12	FLAG 12
16	COM	16	ERA 6	16		13	FLAG 16
17		17	AT_0	17	ROM 11	14	FLAG 15
18		18	CTL 1	18		15	ROR 8
19	COM	19	AT_3	19	ROM 12	16	FLAG 17
20	COM	20	AT_1	20		17	ROR 11
21		21	AT_2	21	ROM 13	18	ROR 7
22		22		22		19	WORD TYPE ONE
23		23	CTL 2	23	ROM 14		
24		24	$\overline{UB}$	24		20	ROR 10
25		25	AM	25	ROM 15	21	FLAG 13
26		26	$\overline{LB}$	26		22	FLAG 11
27		27	AS 2	27	ROM 16	23	FLAG 6
28		28	AS 3	28	ROM 0	24	FLAG 7
29	COM	29	AS 1	29	ROM 17	25	FLAG 4
30	COM	30	AS 0	30	ROM 1	26	FLAG 5
31		31	V	31	ROM 18	27	FLAG 2
32		32	W	32	ROM 2	28	FLAG 3
33		33	T	33	ROM 19	29	FLAG 0
34		34	U	34	ROM 3	30	FLAG 1
35		35	ERA 1	35		31	M12
36		36		36		32	EXT SEL
37		37	ERA 5	37	RAR 0	33	M13
38		38	ERA 9	38	RAR 1	34	M11
39		39	ERA 5	39	RAR 2	35	M14
40		40	ERA 0	40	RAR 3	36	M10
41		41	ERA 8	41	RAR 4	37	M15
42		42		42	RAR 5	38	M9
43		43		43	RAR 6	39	T_1
44		44		44	RAR 7	40	M8
45		45	Z	45	RAR 8	41	M3
46		46	LDRG	46	RAR 9	42	M4
47		47	X	47	RAR 10	43	M2
48		48	Y	48	RAR 11	44	M5
49		49	COM	49	COM	45	M1
50		50	COM	50	COM	46	M6
						47	M0
						48	M7
						49	
						50	COM

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1802-
11	0377	36	0371	68	0205	91-93	0788	121	0545	151	0545	181	0545
14	0788	37	0140	69	0376	94	0759	123	0742	153	0742	184	0759
15	0424	38	0140			95	0843	127	0606	154	0759	185	0755
16	0535	39	0512	71-73	0379	96	0788	129	0742	155	0755	188	0759
17	0512			74	0512	97	0205			158	0759		
18	0205	41-43	0379	75	0788	98	0759	131	0205	159	0742	191	0545
19	0239	44	0140	76	0759	99	0608	134	0759			193	0742
		45	0495	77	0205			135	0755	161	0545	194	0759
21	0142	47	0495	78	0282	101	0545	137	0606			195	0755
24	0371	48	0372	79	0140	103	0742	138	0759	164	0759	197	0742
25	0370	49	0377			104	0759			165	0755	198	0759
26	0376			81	0788	105	0755	141	0640	167	0606	199	0742
27	0424	59	0371	82	0759	107	0742	143	0742	168	0759		
28	0376			84	0759	108	0759	144	0759				
29	0535	61-63	0379	85	0371	109	0742	145	0755	171	0374		
		64	0424	86,87	0843			147	0611	173	0742		
31-33	0379	65	0371	88	0205	111	0545	148	0759	177	0606		
34	0140	66	0372	89	0372	114	0759	149	0742	179	0742		
35	0384	67	0375			115	0755						
						118	0759						



1085A-2 1085B-2 1085C-2

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

30215-60002 TITLE SHEET 2 OF 4

MAGNETIC TAPE CONTROLLER PROCESSOR PCA

ENGINEER | APPROVED | DATE

HEWLETT-PACKARD COMPANY DATA SYSTEMS DIVISION

DESTINATION/SOURCE CODE

ALU CONTROL DECODE

INSTRUCTION DECODER

CONDITION SENSE LOGIC

ROR

COUNTER/ REGISTER SELECT

FLAG LOGIC

WORD DECODE CONTROL

STROBE GENERATOR

DRIVER GATES

TIMING GENERATOR

TIMING GENERATOR/ CONTROL LOGIC

OSCILLATOR

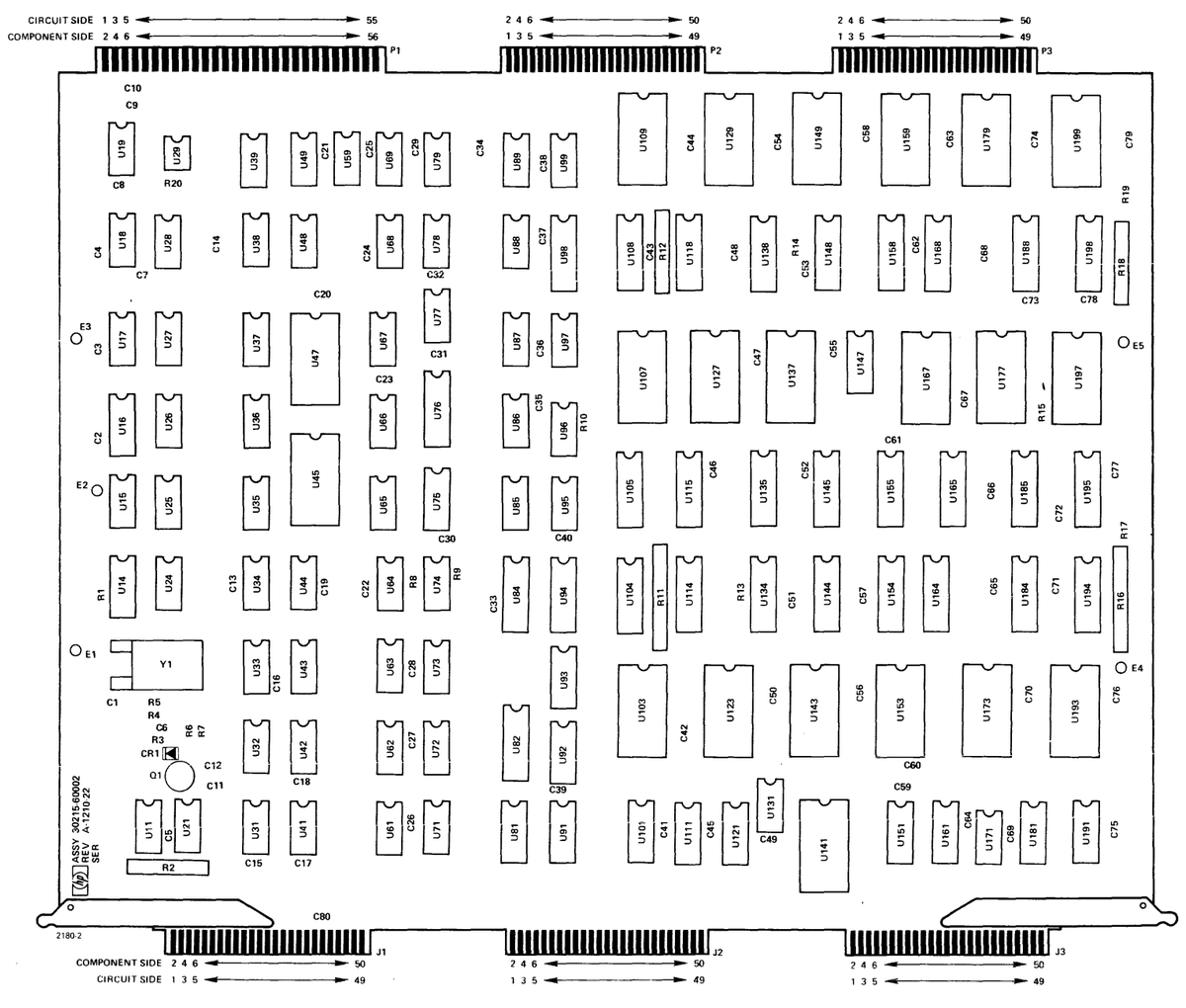
(2060 USE ONLY)

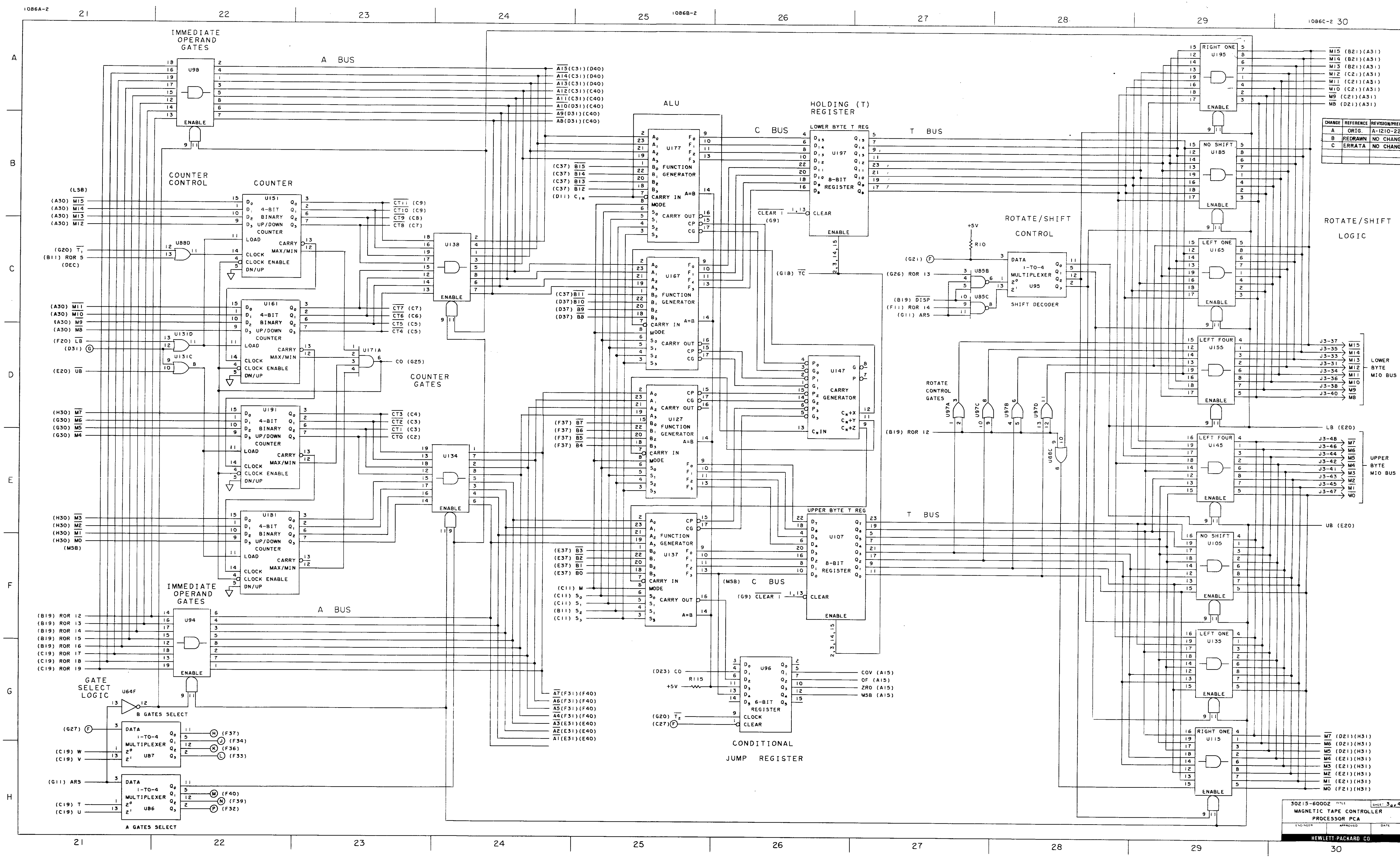
SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	$\overline{\text{COM}}$
2	+5V	2	$\overline{\text{COM}}$	2	COM	2	$\overline{\text{CLEAR}}$
3	+5V	3	$\overline{\text{CLK RST}}$	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	$\overline{\text{ALT CK}}$	5	ROM 5	5	$\overline{T_2}$
6		6	$\overline{\text{DISP}}$	6		6	ROR 9
7		7	$\overline{\text{CK CTL}}$	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8			
9		9	ERA 7	9	ROM 7	8	INPUT STROBE
10		10		10			
11		11	$\overline{\text{LD ERA}}$	11	ROM 8	9	FLAG 10
12		12	ERA 11	12		10	LOWER OUTPUT STROBE
13		13	ERA 3	13	ROM 9		
14		14	ERA 2	14			
15	COM	15	ERA 10	15	ROM 10	11	FLAG 14
16	COM	16	ERA 6	16		12	FLAG 12
17		17	AT_0	17	ROM 11	13	FLAG 16
18		18	CTL 1	18		14	FLAG 15
19	COM	19	AT_3	19	ROM 12	15	ROR 8
20	COM	20	AT_1	20		16	FLAG 17
21		21	AT_2	21	ROM 13	17	ROR 11
22		22		22		18	ROR 7
23		23	$\overline{\text{CTL 2}}$	23	ROM 14	19	WORD TYPE ONE
24		24	$\overline{\text{UB}}$	24			
25		25	$\overline{\text{AM}}$	25	ROM 15	20	ROR 10
26		26	$\overline{\text{LB}}$	26		21	FLAG 13
27		27	AS 2	27	ROM 16	22	FLAG 11
28		28	AS 3	28	ROM 0	23	FLAG 6
29	COM	29	AS 1	29	ROM 17	24	FLAG 7
30	COM	30	AS 0	30	ROM 1	25	FLAG 4
31		31	V	31	ROM 18	26	FLAG 5
32		32	W	32	ROM 2	27	FLAG 2
33		33	T	33	ROM 19	28	FLAG 3
34		34	U	34	ROM 3	29	FLAG 0
35		35	ERA 1	35		30	$\overline{\text{FLAG 1}}$
36		36		36		31	$\overline{\text{M12}}$
37		37	ERA 5	37	RAR 0	32	$\overline{\text{EXT SEL}}$
38		38	ERA 9	38	RAR 1	33	$\overline{\text{M13}}$
39		39	ERA 5	39	RAR 2	34	$\overline{\text{M11}}$
40		40	ERA 0	40	RAR 3	35	$\overline{\text{M14}}$
41		41	ERA 8	41	RAR 4	36	$\overline{\text{M10}}$
42		42		42	RAR 5	37	$\overline{\text{M15}}$
43		43		43	RAR 6	38	$\overline{\text{M9}}$
44		44		44	RAR 7	39	$\overline{T_1}$
45		45	$\overline{Z}$	45	RAR 8	40	$\overline{\text{M8}}$
46		46	$\overline{\text{LDRG}}$	46	RAR 9	41	$\overline{\text{M3}}$
47		47	X	47	RAR 10	42	$\overline{\text{M4}}$
48		48	Y	48	RAR 11	43	$\overline{\text{M2}}$
49		49	COM	49	COM	44	$\overline{\text{M5}}$
50		50	COM	50	COM	45	$\overline{\text{M1}}$
51						46	$\overline{\text{M6}}$
52						47	$\overline{\text{M0}}$
53						48	$\overline{\text{M7}}$
54						49	
55						50	COM
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1802-
11	0377	36	0371	68	0205	91-93	0788	121	0545	151	0545	181	0545
14	0788	37	0140	69	0376	94	0759	123	0742	153	0742	184	0759
15	0424	38	0140			95	0843	127	0606	154	0759	185	0755
16	0535	39	0512	71-73	0379	96	0788	129	0742	155	0755	188	0759
17	0512			74	0512	97	0205			158	0759		
18	0205	41-43	0379	75	0788	98	0759	131	0205	159	0742	191	0545
19	0239	44	0140	76	0759	99	0608	134	0759			193	0742
		45	0495	77	0205			135	0755	161	0545	194	0759
21	0142	47	0495	78	0282	101	0545	137	0606			195	0755
24	0371	48	0372	79	0140	103	0742	138	0759	164	0759	197	0742
25	0370	49	0377			104	0759			165	0755	198	0759
26	0376			81	0788	105	0755	141	0640	167	0606	199	0742
27	0424	59	0371	82	0759	107	0742	143	0742	168	0759		
28	0376			84	0759	108	0759	144	0759				
29	0535	61-63	0379	85	0371	109	0742	145	0755	171	0374		
		64	0424	86,87	0843			147	0611	173	0742		
31-33	0379	65	0371	88	0205	111	0545	148	0759	177	0606		
34	0140	66	0372	89	0372	114	0759	149	0742	179	0742		
35	0384	67	0375			115	0755						
						118	0759						





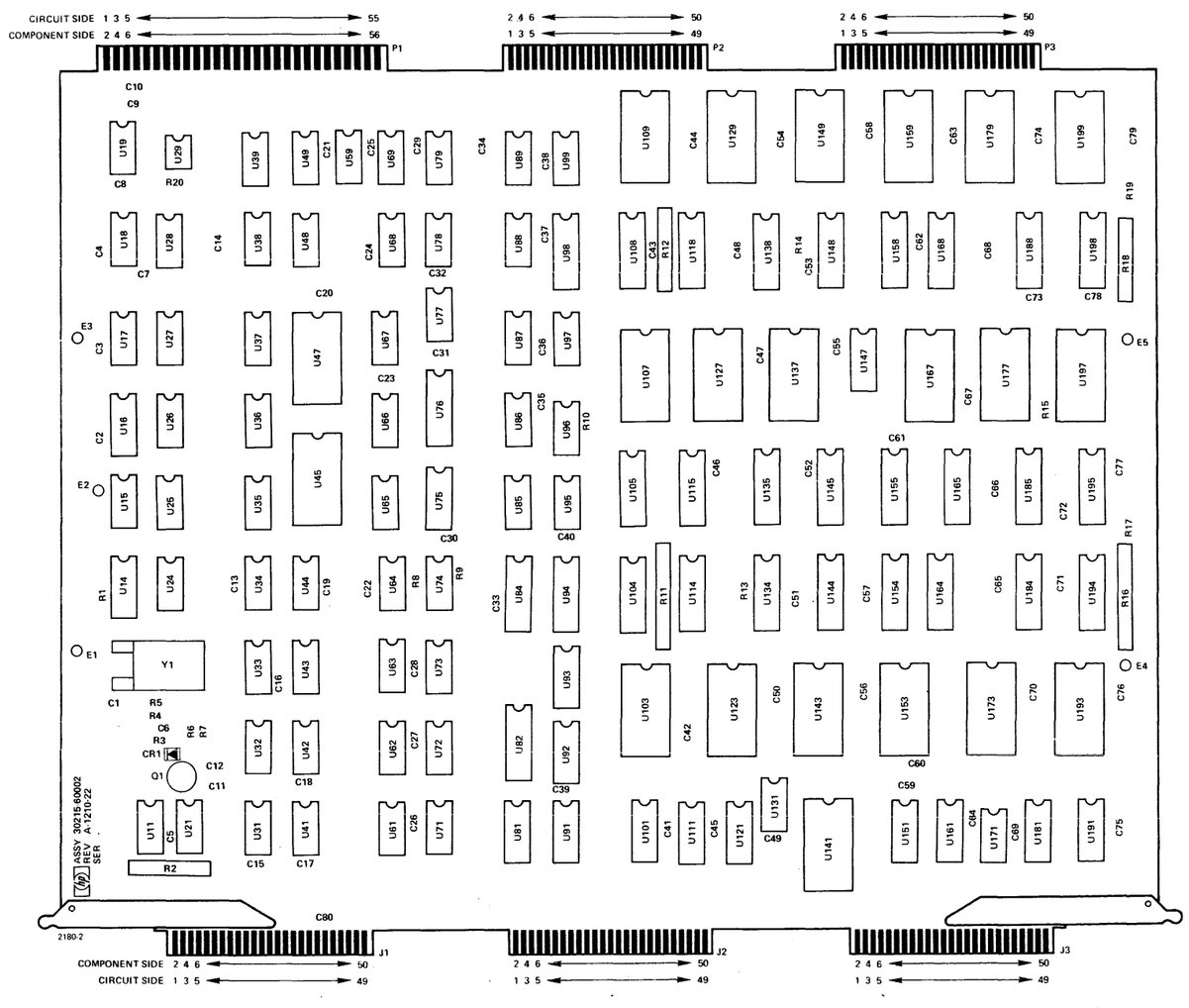
IMMEDIATE OPERAND GATES
A BUS
ALU
HOLDING (T) REGISTER
C BUS
T BUS
LOWER BYTE T REG
8-BIT REGISTER
COUNTER CONTROL
COUNTER
4-BIT BINARY UP/DOWN COUNTER
COUNTER GATES
FUNCTION GENERATOR
CARRY GENERATOR
ROTATE/SHIFT CONTROL
SHIFT DECODER
1-TO-4 MULTIPLEXER
ROTATE/SHIFT LOGIC
RIGHT ONE
NO SHIFT
LEFT ONE
LEFT FOUR
LOWER BYTE MIO BUS
UPPER BYTE MIO BUS
ROTATE CONTROL GATES
UPPER BYTE T REG
CONDITIONAL JUMP REGISTER
6-BIT REGISTER
GATE SELECT LOGIC
B GATES SELECT
A GATES SELECT
CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG. | A-1210-22
B | REDRAWN | NO CHANGE
C | ERRATA | NO CHANGE
30215-60002
MAGNETIC TAPE CONTROLLER PROCESSOR PCA
HEWLETT-PACKARD CO

SIGNAL INDEX

P1 PIN	P1 SIGNAL	J1 PIN	J1 SIGNAL	J2 PIN	J2 SIGNAL	J3 PIN	J3 SIGNAL
1	+5V	1	COM	1	COM	1	COM
2	+5V	2	COM	2	COM	2	CLEAR
3	+5V	3	CLK RST	3	ROM 4	3	$\overline{T_0}$
4	+5V	4		4		4	$\overline{T_3}$
5		5	ALT CK	5	ROM 5	5	$\overline{T_2}$
6		6	DISP	6		6	ROR 9
7		7	CK CTL	7	ROM 6	7	UPPER OUTPUT STROBE
8		8		8			
9		9	ERA 7	9	ROM 7	8	INPUT STROBE
10		10		10			
11		11	LD ERA	11	ROM 8	9	FLAG 10
12		12	ERA 11	12		10	LOWER OUTPUT STROBE
13		13	ERA 3	13	ROM 9		
14		14	ERA 2	14		11	FLAG 14
15	COM	15	ERA 10	15	ROM 10	12	FLAG 12
16	COM	16	ERA 6	16		13	FLAG 16
17		17	AT_0	17	ROM 11	14	FLAG 15
18		18	CTL 1	18		15	ROR 8
19	COM	19	AT_3	19	ROM 12	16	FLAG 17
20	COM	20	AT_1	20		17	ROR 11
21		21	AT_2	21	ROM 13	18	ROR 7
22		22		22		19	WORD TYPE ONE
23		23	$\overline{CTL}$ 2	23	ROM 14		
24		24	$\overline{UB}$	24		20	ROR 10
25		25	$\overline{AM}$	25	ROM 15	21	FLAG 13
26		26	$\overline{LB}$	26		22	FLAG 11
27		27	AS 2	27	ROM 16	23	FLAG 6
28		28	AS 3	28	ROM 0	24	FLAG 7
29	COM	29	AS 1	29	ROM 17	25	FLAG 4
30	COM	30	AS 0	30	ROM 1	26	FLAG 5
31		31	V	31	ROM 18	27	FLAG 2
32		32	W	32	ROM 2	28	FLAG 3
33		33	T	33	ROM 19	29	FLAG 0
34		34	U	34	ROM 3	30	$\overline{FLAG}$ 1
35		35	ERA 1	35		31	$\overline{M12}$
36		36		36		32	$\overline{EXT}$ SEL
37		37	ERA 5	37	RAR 0	33	$\overline{M13}$
38		38	ERA 9	38	RAR 1	34	$\overline{M11}$
39		39	ERA 5	39	RAR 2	35	$\overline{M14}$
40		40	ERA 0	40	RAR 3	36	$\overline{M10}$
41		41	ERA 8	41	RAR 4	37	$\overline{M15}$
42		42		42	RAR 5	38	$\overline{M9}$
43		43		43	RAR 6	39	$\overline{T_1}$
44		44		44	RAR 7	40	$\overline{M8}$
45		45	$\overline{Z}$	45	RAR 8	41	$\overline{M3}$
46		46	LDRG	46	RAR 9	42	$\overline{M4}$
47		47	X	47	RAR 10	43	$\overline{M2}$
48		48	Y	48	RAR 11	44	$\overline{M5}$
49		49	COM	49	COM	45	$\overline{M1}$
50		50	COM	50	COM	46	$\overline{M6}$
51						47	$\overline{M0}$
52						48	$\overline{M7}$
53						49	
54						50	COM
55							
56							

I.C. INDEX

U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1820-	U	1802-
11	0377	36	0371	68	0205	91-93	0788	121	0545	151	0545	181	0545
14	0788	37	0140	69	0376	94	0759	123	0742	153	0742	184	0759
15	0424	38	0140			95	0843	127	0606	154	0759	185	0755
16	0535	39	0512	71-73	0379	96	0788	129	0742	155	0755	188	0759
17	0512			74	0512	97	0205			158	0759		
18	0205	41-43	0379	75	0788	98	0759	131	0205	159	0742	191	0545
19	0239	44	0140	76	0759	99	0608	134	0759			193	0742
		45	0495	77	0205			135	0755	161	0545	194	0759
21	0142	47	0495	78	0282	101	0545	137	0606			195	0755
24	0371	48	0372	79	0140	103	0742	138	0759	164	0759	197	0742
25	0370	49	0377			104	0759			165	0755	198	0759
26	0376			81	0788	105	0755	141	0640	167	0606	199	0742
27	0424	59	0371	82	0759	107	0742	143	0742	168	0759		
28	0376			84	0759	108	0759	144	0759				
29	0535	61-63	0379	85	0371	109	0742	145	0755	171	0374		
		64	0424	86,87	0843			147	0611	173	0742		
31-33	0379	65	0371	88	0205	111	0545	148	0759	177	0606		
34	0140	66	0372	89	0372	114	0759	149	0742	179	0742		
35	0384	67	0375			115	0755						
						118	0759						



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	ERRATA	NO CHANGE

LOWER BYTE MIO BUS

(A30) M15
(A30) M14
(A30) M13
(A30) M12
(A30) M11
(A30) M10
(A30) M9
(A30) M8
(G9) CLEAR
(F20) LB

15V ← P1-1,2,3,4 — C1-5,7-8,11-15, .01UF 79. — C9,10 2.2UF — +5V

COM ← J1-1,2,49,50
COM ← J2-1,2,49,50
COM ← J3-1,50
COM ← P1-15,16,19,20,29,30

RG3 8-BIT REGISTER U149 — RG0 8-BIT REGISTER U159 — RG1 8-BIT REGISTER U179 — RG2 8-BIT REGISTER U199 — RG4 8-BIT REGISTER U109 — RG5 8-BIT REGISTER U129

ENABLE 0-3 / ENABLE 4-7 / CLEAR

A BUS — U148 — U158 — B BUS

(B24) A8
(A24) A9
(A24) A10
(A24) A11
(A24) A12
(A24) A13
(A24) A14
(A24) A15

U168 U188 U198 U108 U118 ENABLE

R18F R19 R18E R18G — R18B R18C R18A R18D — R12F R14 R12C R12B — R12A R12E R12G R12D — +5V

B8 (C25)
B9 (C25)
B10 (C25)
B11 (C25)
B12 (B25)
B13 (B25)
B14 (B25)
B15 (B25)

A8 (B24)
A9 (A24)
A10 (A24)
A11 (A24)
A12 (A24)
A13 (A24)
A14 (A24)
A15 (A24)

(E20) LB
(D21) G

U99 BINARY TO OCTAL DECODER — ENABLE

(C19) X
(C19) Y
(C19) Z
(D18) CLD

EXT SEL ← J3-32

R16C R16E R16F R16D — R16A R16G R16B R17 — R11F R13 R11B R11AG — R11C R11E R11A R11D — +5V

A BUS — U144 — U154 — B BUS

(G24) A0
(G24) A1
(G24) A2
(G24) A3
(G24) A4
(G24) A5
(G24) A6
(G24) A7

U164 U184 U194 U104 U114 ENABLE

(H22) P
(H22) L
(G22) J
(H22) K
(G22) H
(H22) N
(H22) M

B0 (F25)
B1 (F25)
B2 (F25)
B3 (E25)
B4 (E25)
B5 (E25)
B6 (D25)
B7 (D25)

A0 (G24)
A1 (G24)
A2 (G24)
A3 (G24)
A4 (G24)
A5 (G24)
A6 (G24)
A7 (G24)

(E20) B
(E20) UB

RG3 8-BIT REGISTER U143 — RG0 8-BIT REGISTER U153 — RG1 8-BIT REGISTER U173 — RG2 8-BIT REGISTER U193 — RG4 8-BIT REGISTER U103 — RG5 8-BIT REGISTER U123

ENABLE 4-7 / ENABLE 0-3 / CLEAR

(G9) CLEAR
(H30) M0
(H30) M1
(H30) M2
(H30) M3
(G30) M4
(G30) M5
(G30) M6
(H30) M7

UPPER BYTE MIO BUS

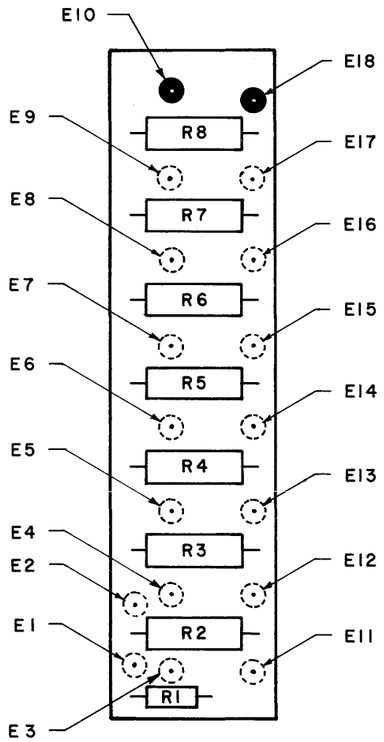
30215-60002	TITLE: MAGNETIC TAPE CONTROLLER PROCESSOR PCA
SHEET 4 OF 6	
ENGINEER	APPROVED / DATE
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION	

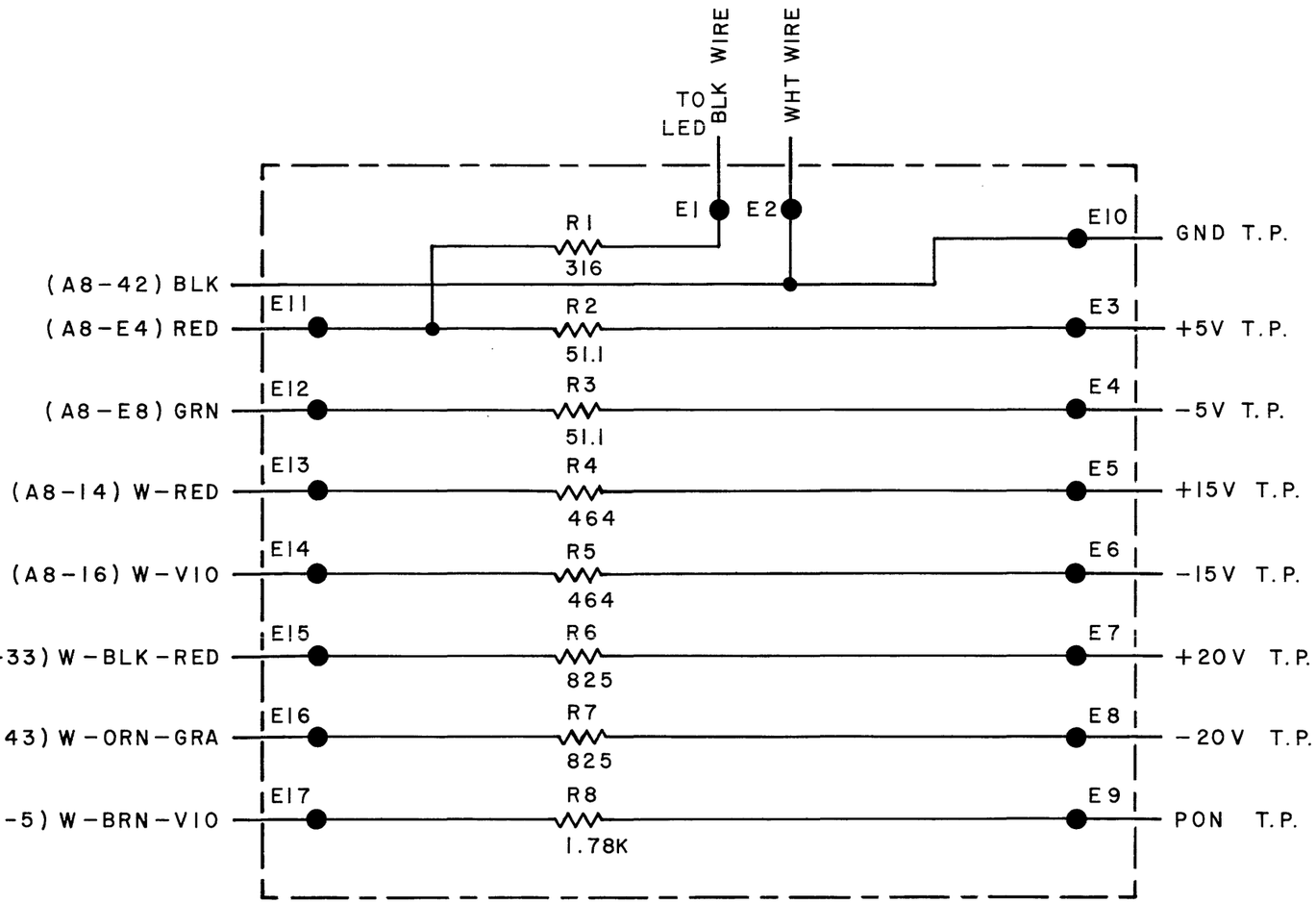
HP 30310A POWER SUPPLY
DETAILED DIAGRAM SET

DD-700

ASSEMBLY	SERIES	SHEET
30310-60001	1209	1
30310-60002	1210	2
30310-60003	1210	3
30310-60004	1303	4
30310-60005	1303	5
30310-60006	1303	6
30310-60007	1210	7
30310-60008	1303	8
30310-60009	1210	8
30310-60010	1210	9
30310-60011	1210	10
30000-93088	—	11
OVERALL	—	12

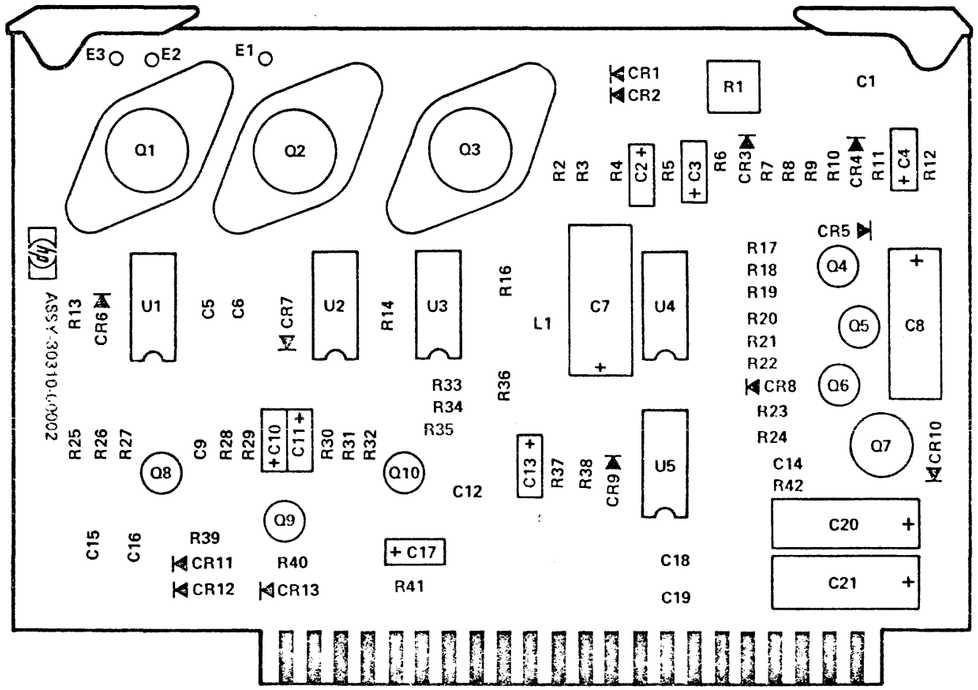
REV D





NOTE: RESISTANCE VALUES ARE IN OHMS

30310-60001 TITLE		SHEET 1 OF 1
TEST POINT BOARD A12A1		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		


E3
E2
E1
Q1
Q2
Q3
CR1
CR2
R1
C1
R2
R3
R4
C2 +
R5
+ C3
R6
CR3
R7
R8
R9
R10
CR4
R11
+ C4
R12
CR5
Q4
Q5
Q6
Q7
C8
R17
R18
R19
R20
R21
R22
CR8
R23
R24
C14
R42
CR10
C20 +
C21 +
ASSY-30310-0002
R13
CR6
U1
C5
C6
CR7
U2
R14
U3
R16
L1
C7 +
U4
R33
R34
R35
R36
R25
R26
R27
Q8
C9
R28
R29
+ C10
C11 +
R30
R31
R32
Q10
C12
C13 +
R37
R38
CR9
U5
C18
C19
Q9
C15
C16
R39
CR11
CR12
R40
CR13
+ C17
R41

2206-30

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE

+5V BIAS
+18,V
+15V BIAS
+4,D
+15V BIAS
9,K
INU
15,S
-30V FEEDBACK
16,T
OVERCURRENT
17,U

+9V 7,H

Q3

R33 2.7
R34 2.7
R35 3.16K
C12 470PF
C13 2.2
R16 4.64K
R36 9.09K

+5 VOLT BIAS REGULATOR

U3

+7.5V REF.

+15 VOLT BIAS REGULATOR

Q2
R32 2.7
R14 4.64K
C6 100PF
CR7 11V
U2
+22V 5,E
Q10
R31 5.11K
R30 4.64K
C11 2.2
+15V BIAS

COMMON 1,A
E1

-15 VOLT BIAS REGULATOR

-22V
CR6 11V
U1
C5 .001
R13 56.2K
+5V
C9 .001
R29 4.64K
R28 4.64K
Q8
Q1
-22V 10,L
R27 2.7
C10 2.2
-15V BIAS

R42 1.96K
R17 16.2K
Q4
Q5
Q6
C8 20
C14 .68
CR5
R18 31.6K
R19 10K
+15V BIAS
R11 7.5K

INU INHIBIT CONTROL

+15V BIAS
±5V, ±15V ADJ.
R1 5K CW
R7 12.1K
R4 11K
L1 10MH
R2 51.1K
R3 511
C2 1.0
C7 47
R38 3.16K
CR3
R5 3.16K
R9 10K
-15V BIAS

ERROR DETECTOR

C1 .0047
R12 147K
C3 .33
R6 5.6M
C4 1.0
+15V BIAS
U4
R8 3.16K
CR2
CR1
R10 100K
-15V BIAS
CR4

AXIS CROSSING DETECTOR

6,F
R26 1.21K
CR11
C16 .1
21.5 VRMS FROM T3 BIAS TRANSFORMER
8,J
C15 .1
2,B
R25 1.21K
CR12
R39 1.96K

RAMP GENERATOR

+15V BIAS
R41 100K
R40 10K
Q9
CR13
C17 .1
E2

+8.8V
+0.8V
WAVEFORM AT E2

FIRING-ANGLE COMPARATOR

+15V BIAS
U5
-15V BIAS
CR9 8.25V
E3

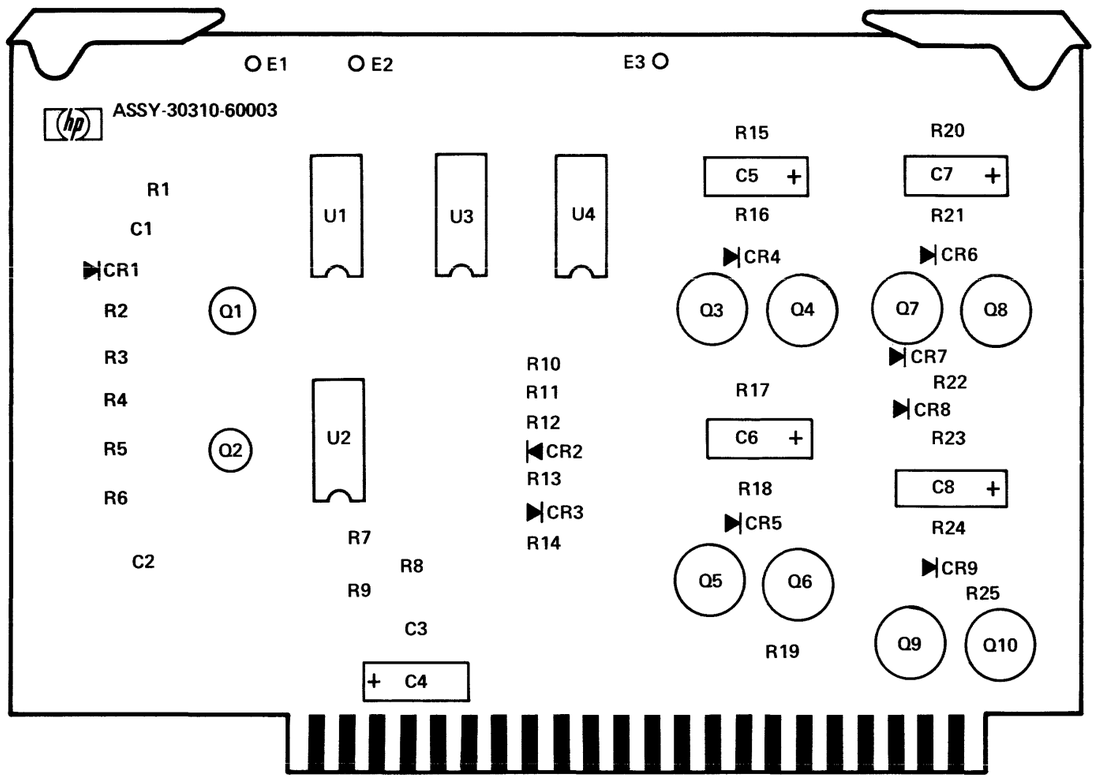
20
19
21,Y
BLOCKING OSCILLATOR OP. TO A9 PREREGULATOR (T1)

R23 51.1
+15V BIAS
R24 100
CR8
C18 .022
R22 100
C20 47
Q7
CR10
R37 10K
C19 .01
R21 3.16K
R20 51.1
-15V BIAS
C21 150

BLOCKING OSCILLATOR

3. ▽ DENOTES SIGNAL COMMON
2. CAPACITANCE VALUES ARE IN MICROFARADS
1. RESISTANCE VALUES ARE IN OHMS
NOTES: UNLESS OTHERWISE SPECIFIED

30310-60002	TITLE	SHEET 1 OF 1
PREREGULATOR CONTROL PCA (A1)		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		


E1
E2
E3
ASSY-30310-60003
R1
C1
CR1
R2
R3
R4
R5
R6
C2
Q1
Q2
U1
U2
U3
U4
R7
R8
R9
C3
C4
R10
R11
R12
CR2
R13
CR3
R14
R15
C5
R16
R17
C6
R18
CR5
Q5
Q6
R19
CR4
Q3
Q4
R20
C7
R21
CR6
Q7
Q8
CR7
R22
CR8
R23
C8
R24
CR9
R25
Q9
Q10

2208-31

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE

+22V 5,E → C4 4.7 → +22V

+22V COMMON 8,J

+5V BIAS 18,V → C3 .01 → +5V BIAS

SIGNAL COMMON 1,A

3.2 KHZ OSCILLATOR

R2 4.64K, R3 2.61K, R4 1K, R5 28.1K, R6 5.11K → +5V BIAS

CR1, C2 .015, Q1, Q2, C1 .015

FREQUENCY DIVIDER

+5V BIAS → U2A, U2B → +5V BIAS

PHASE DIVIDER LOGIC

U1D, U4C, U3C, U1A, U4B, U3B, U1C, U4D, U3D, U1B, U4A, U3A

+5V BIAS → R10 147, R12 147, R11 147, R14 147

R7 1K → E2

R9 68.1, R1 68.1 → E3

R8 1K → E1

INV 15,S

+22V

R23 316, R24 316, R20 316, R21 316

Q9, Q7, C8 15, C7 15, CR9, CR6

20,X

21,Y

→ TO A7 INVERTER (T1) PHASE 1 INVERTER DRIVE

CR8, Q10, Q8

PHASE 1 INVERTER DRIVER

R25 1K, R22 1K

CR7

+22V

R17 316, R15 316, R18 316, R16 316

Q5, Q3, C6 15, C5 15, CR5, CR4

17,U

14,R

→ TO A7 INVERTER (T2) PHASE 2 INVERTER DRIVE

CR3, Q6, Q4

PHASE 2 INVERTER DRIVER

R19 1K, R13 1K

CR2

4. U1, U2, U3, & U4-PIN 7 ▽, PIN 14 +5V BIAS

3. ▽ DENOTES SIGNAL COMMON

2. DENOTES +22 VDC (UNREGULATED) COMMON ▽

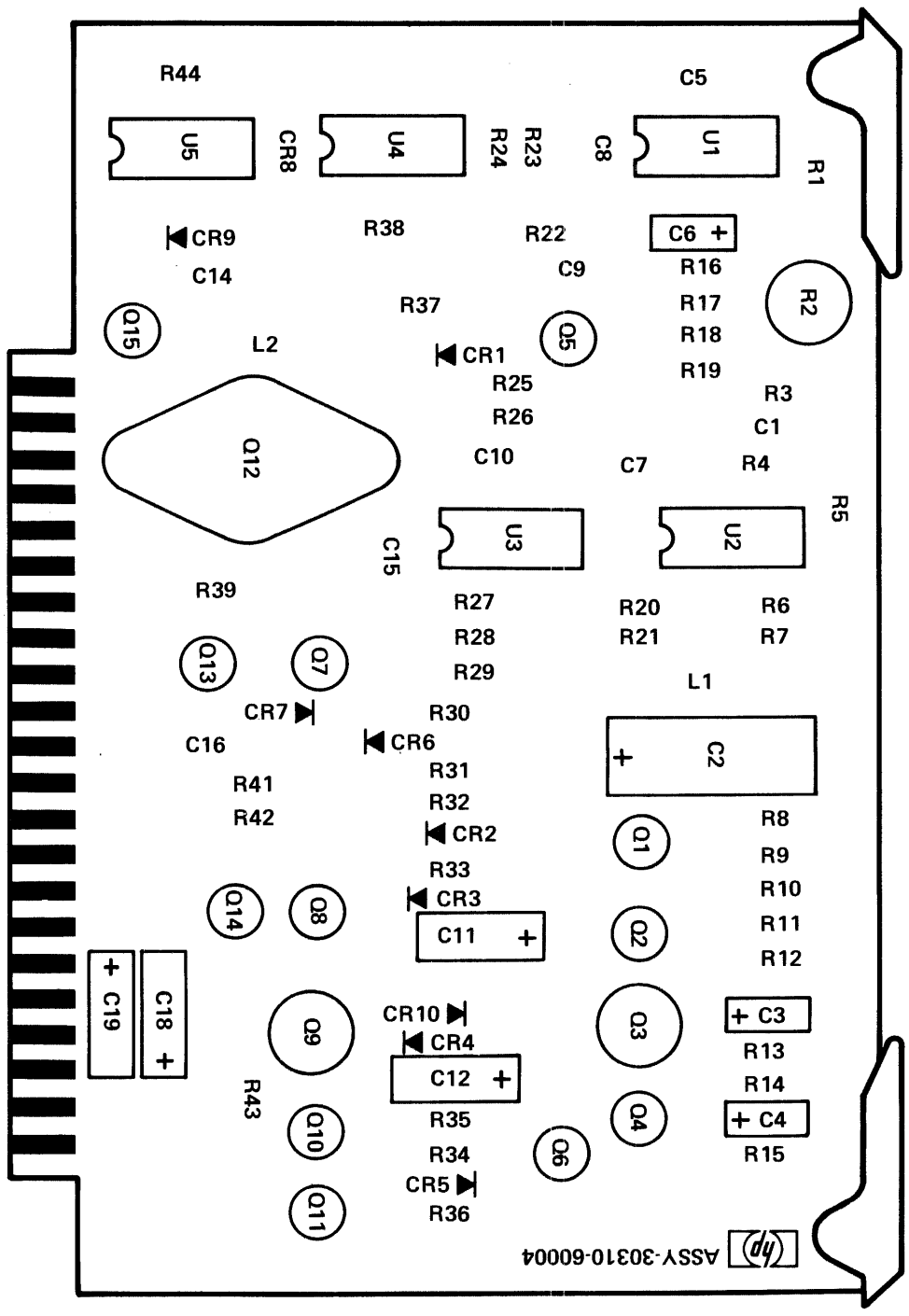
1. RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

30310-60003	TITLE	SHEET 1 OF 1
INVERTER DRIVER PCA (A2)		
ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

2208-32


R44
C5
U5
CR8
U4
R24
R23
C8
U1
R1
CR9
R38
R22
C6 +
C14
C9
R16
R17
R18
R19
R2
R37
Q15
L2
CR1
Q5
R25
R26
R3
C1
Q12
C10
C7
R4
R5
U3
U2
C15
R39
R27
R28
R29
R20
R21
R6
R7
Q13
Q7
L1
CR7
R30
C16
CR6
C2
R31
R41
R32
R42
CR2
R8
Q1
R33
R9
R10
Q14
Q8
CR3
C11 +
Q2
R11
R12
C19 +
C18 +
Q9
CR10
CR4
Q3
+ C3
R13
R43
C12 +
R14
Q10
R35
Q6
Q4
+ C4
R34
R15
CR5
R36
Q11
ASSY-30310-60004

2382

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-B	B-1230-22
D	PPC-C	B-1232-22
E	PPC-I	NO CHANGE
F	22-1655	B-1303-22

+20V SENSE W
+20V SAMPLE 3
+20V DRIVE C
+30V 5
SWITCH SENSE E
TEMP SENSE TB3-10 H
±20VDC COMMON 8,J
-20V 10,L
+20V X
-30V 7
+15V BIAS 4,D
-15V BIAS 9,K
COMMON 1,A

+20V REGULATOR DRIVER
Q7
Q12
Q13
R39 1.5
L2 3.3 mH
CR1
CR7
R41 4.64K
R42 4.64K
C16 .01

DUTY CYCLE COMPARATOR
+15V BIAS
U5
R44 2.15K
CR9
R37 453
Q15
-15V BIAS

20 KHZ OSCILLATOR
C14 .015
R38 1.21K
R24 10K
+15V BIAS
U4
R23 4.64K
-15V BIAS

INHIBIT CONTROL
+15V BIAS
R26 10K
R25 14.7K
R19 4.64K
Q5
R22 6.81K
R3 14.7K
C6 1UF 35V
C9 .01
R16 383

+20V REGULATOR
R18 4.22K
C8 30PF
CR8
+15V BIAS
U1
R17 3.16K
+20V ADJ
R2 500
CW
R1 100K
C5 .001
-15V BIAS

+20V CURRENT LIMITER
+20V(X)
Q11
Q10
R43 261
R36 10M
Q9
CR5
R35 10
C12 4.7
R30 100K
R31 10K
CR6
CR10
CR4
Q8
Q14
CR3
R32 2.15K
CR2 8.25
R34 10K
-15V BIAS
+15V BIAS
R33 6.81K
C11 15 20V

-20V ERROR DETECTOR
-20V
R29 6.124K
R28 6.124K
+20V
+15V BIAS
U3
-15V BIAS
C15 220PF
R27 10K
C10 .015
R21 10K
R7 10K

-20V REGULATOR DRIVER
C7 220PF
U2
R4 100K
R6 10K
L1 1mH
C2 50
Q1
R8 10
C1 .0015
R5 2.15K
R20 10K
R9 1K
R10 200
R11 511
-20V(10,L)
Q2
Q4
Q6
Q3
R12 1.78K
R13 3.83K
R14 3.83K
C3 2.2
R15 11K
C4 2.2

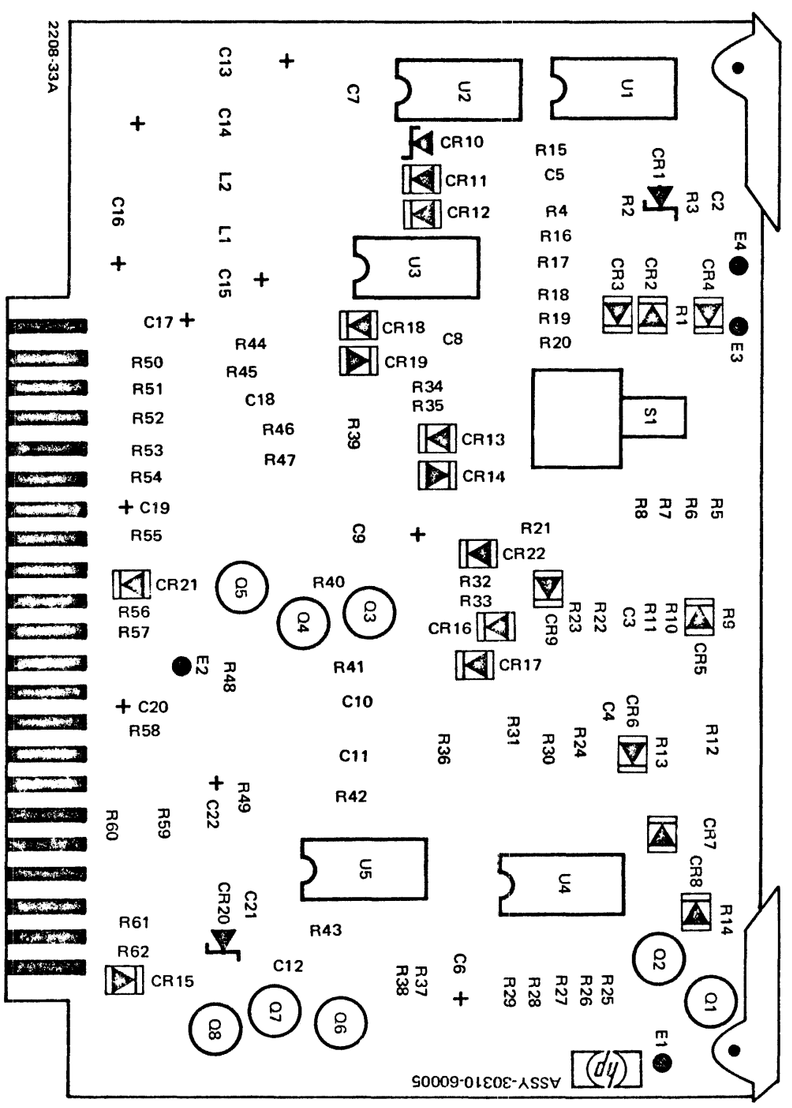
-20V CURRENT LIMITER
+15V BIAS

U -20V SENSE
17 -20V DRIVE

C18 15 20V
C19 15 20V

2. ⟨2⟩ DENOTES ± 20V OUTPUT COMMON
1. ⟨1⟩ DENOTES SIGNAL COMMON
NOTES:

30310-60004 TITLE
SHEET 1 OF 1
20 VOLT SUPPLY PCA (A3)
ENGINEER | APPROVED | DATE
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION


2208-33A
U1
U2
U3
U4
U5
S1
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
CR22
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
E1
E2
E3
E4
R1
R2
R3
R4
R5
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R48
R49
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
L1
L2
ASSY-30310-60005

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-L	B-1232-22
D	22-1655	B-1303-22
E	22-1696	C-1303-22

+30V 5,E — L1 10MH — C13 20 50V

+5V BIAS 18,V

+5V 20,X — R61 383 — R59 815 — C22 .47

+5V SENSE 21,Y — R62 383 — R60 815 — R49 121K

C10 2.2 — R36 90.9K — R42 121K — C11 .01

U5A: +15VBIAS, -15VBIAS

+15V 3,C — R51 2.15K — C17 .47

+15V SENSE 8,Z — R50 2.15K — R44 68.1K

C2 2.2 — R3 90.9K — R2 110K — C1 .01

U1

E3

CR3 — CR2 — CR1 31.6V — R4 2.15K — -15V BIAS

-5V 11,M — R57 1K — C20 .47

-5V SENSE 13,P — R58 1K — R48 61.9K

R43 90.9K — C12 2.2 — R38 133K — C21 .01

U5B

E4

-15V 7 — R54 2.15K — R35 110K — C7 .01

-15V SENSE 14,H — R55 2.15K — R53 68.1K — C19 .47

U2

E1

SIGNAL COMMON 1,A

R15 90.9K — C5 2.2 — R8 46.4K — CR14 — R34 46.4K — CR13

R52 2.15K — +15V BIAS

CR10 31.6V

C16 10 20V — C15 10 20V — CR12 — C14 20 50V — CR11

+15 BIAS 4,D — +15V BIAS

-15V BIAS 9,K — -15V BIAS

-30V 8,J — L2 10MH

R1 10K — CR4

R19 90.9K — R18 681K

R20 100K — R17 133K

-15V BIAS

R39 90.9K — R47 90.9K

R21 90.9K — R46 100K

INU INTERLOCK 15 — 5

CR7 LED

R14 162

+15V BIAS

+5V CURRENT LIMIT THRESHOLD ADJ.

-15V BIAS — R30 1.62K — CR6 7.87V — R12 5K CW — R10 17.8K

U4A

CR5

R26 196K — U4B — R24 3.83K — C3 .01

R11 46.4K — CR16

Q1 — Q2 — CR8 — C6 10UF — R25 14.7K

R37 2.37K — R27 196K

Q6 OVERCURRENT TIMER

CR9

C4 .01

+15V BIAS — R5 2.61K — R6 619 — R7 422 — S-1 +5V CURRENT THRESHOLD INCREMENT

R9 19.6K — R13 287K

R33 10K

+15V BIAS — R28 2.15K — R31 10K — Q8 OVERCURRENT LATCH

Q7 — Q3 — CR20 9.09V — Q4 — R41 10K

R29 2.15K

R23 14.7K — CR17

R22 10K — -15V BIAS

R16 422K — C8 .01

U3B

R45 464K — C18 .01

U3A

CR18 — CR22 — CR15

+15V BIAS — R56 21.5K — E2 — 17,U OVERCURRENT

CR21 — Q5

R32 10K — C9 47 — -15V BIAS

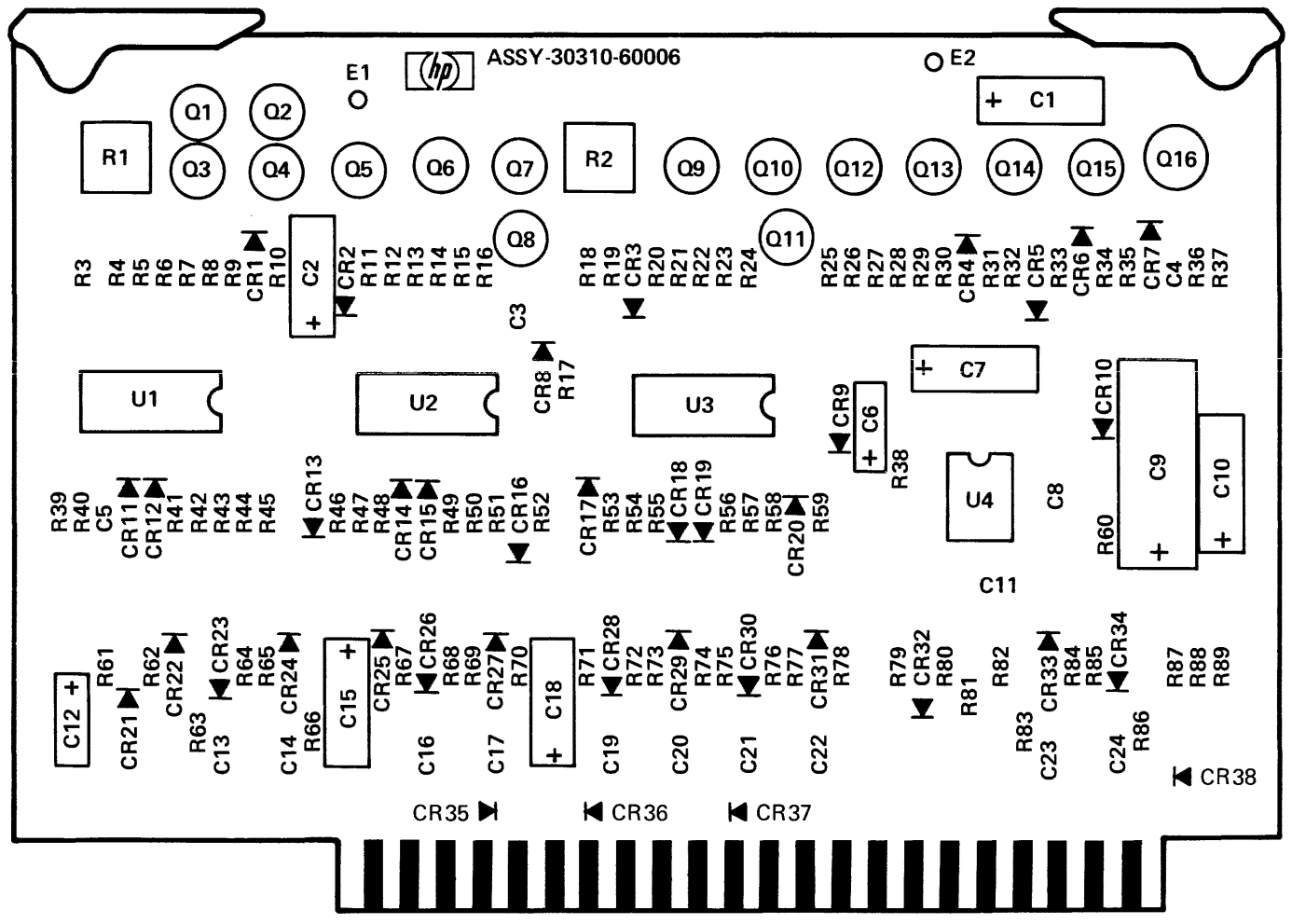
R40 178K

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/4 WATT, 1%

30310-60005	TITLE	SHEET 1 OF 1
CURRENT LIMIT PCA (A4)		
ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION


ASSY-30310-60006
E1
E2
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
R1
R2
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
U1
U2
U3
U4
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
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R76
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R78
R79
R80
R81
R82
R83
R84
R85
R86
R87
R88
R89
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CR15
CR16
CR17
CR18
CR19
CR20
CR21
CR22
CR23
CR24
CR25
CR26
CR27
CR28
CR29
CR30
CR31
CR32
CR33
CR34
CR35
CR36
CR37
CR38

2208-34

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	A-1210-22
B	REDRAWN	NO CHANGE
C	22-1571	A-1244-22
D	22-1655	A-1303-22
E	22-1696	B-1303-22

POSITIVE OVERVOLTAGE COMPARATOR

POSITIVE UNDERVOLTAGE COMPARATOR

NEGATIVE OVERVOLTAGE COMPARATOR

NEGATIVE UNDERVOLTAGE COMPARATOR

DC ENABLE COMPARATOR

LINE VOLTAGE MONITOR

CROWBAR LATCH

TURN ON INHIBIT

LEVEL SHIFTER

INU DRIVER

CROWBAR BLOCKING OSCILLATOR

TO A8 T1 CROWBAR TRIGGER TRANSFORMER

PSU DETECTOR

0.6 SECOND DELAY SCHMITT TRIGGER

PON OUTPUT DRIVER

REFERENCE SUPPLY

PFW DRIVER

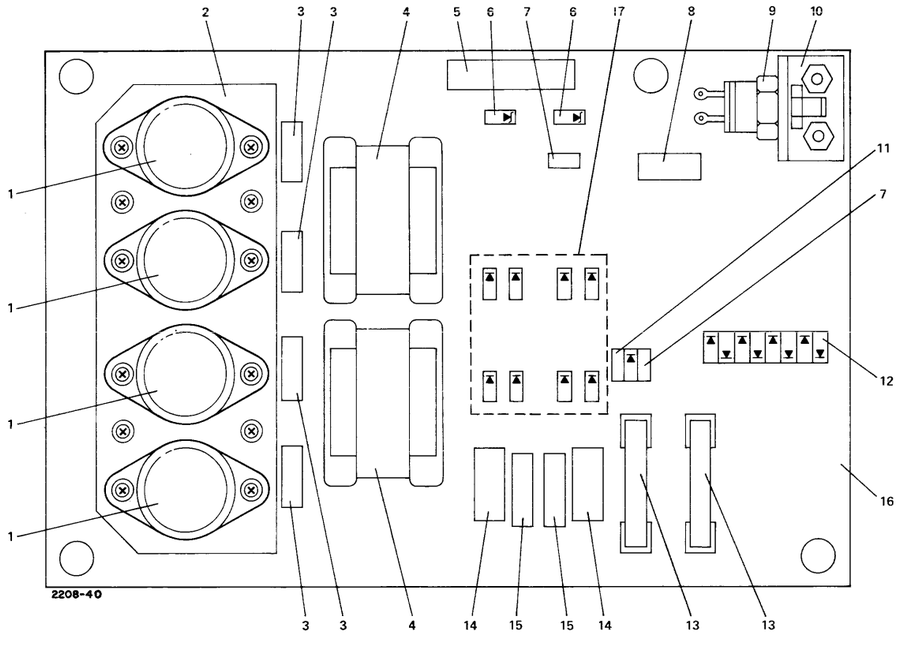
3. CR35 IS A STABISTOR, HP PART NO. 1901-0460.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
1. ALL RESISTANCE VALUES ARE IN OHMS.

NOTE: UNLESS OTHERWISE SPECIFIED

30310-60006	TITLE: VOLTAGE PROTECT PCA (A5)
SHEET 1 OF 1	
ENGINEER	APPROVED
DATE	

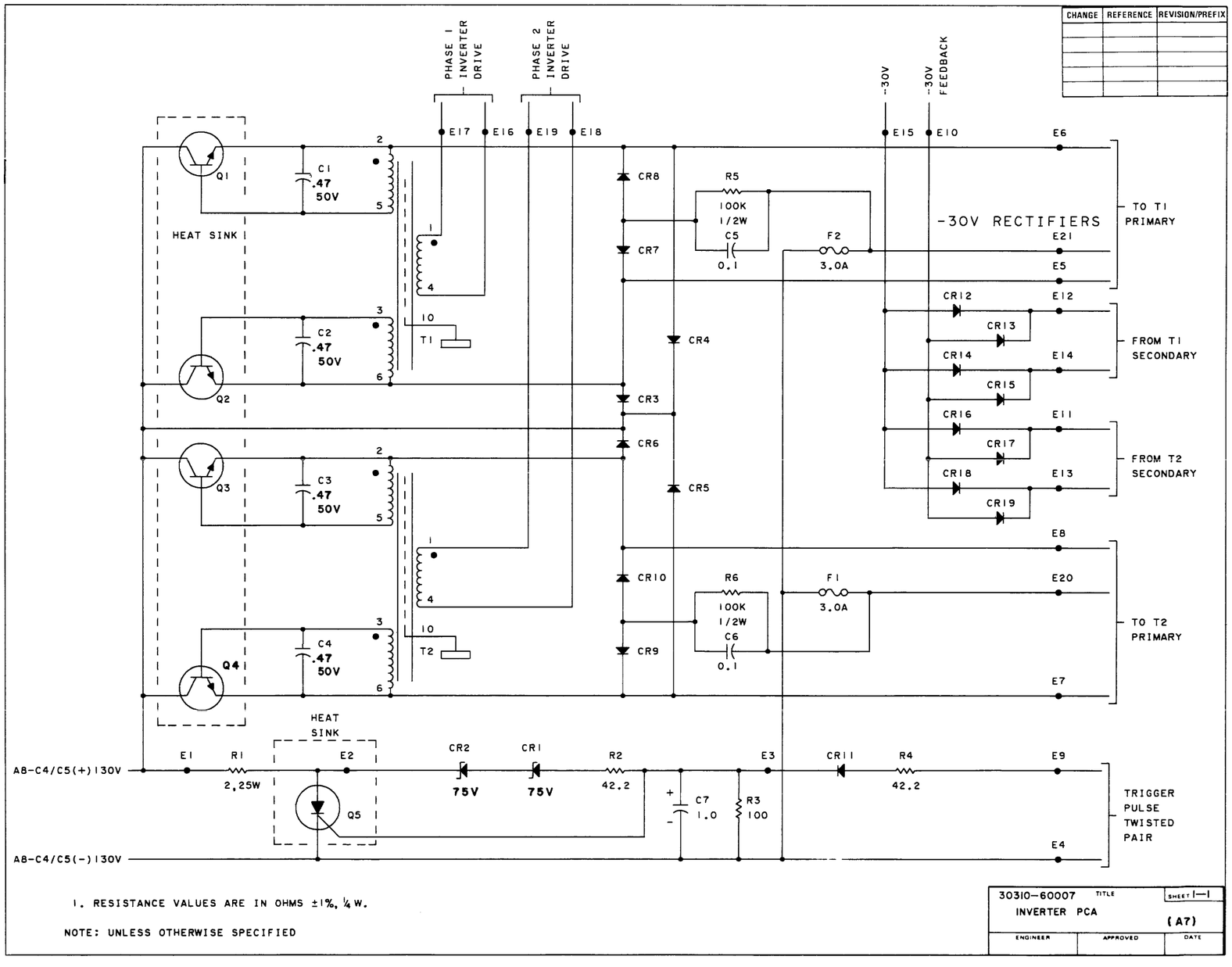
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

1	Q1, Q2, Q3, Q4
3	C1, C2, C3, C4
4	T1, T2
5	R1
6	CR1, CR2
7	R2, R4
8	C7
9	Q5
11	R3
12	CR12 THRU CR19
13	F1, F2
14	C5, C6
15	R5, R6
17	CR3-10



1302-1

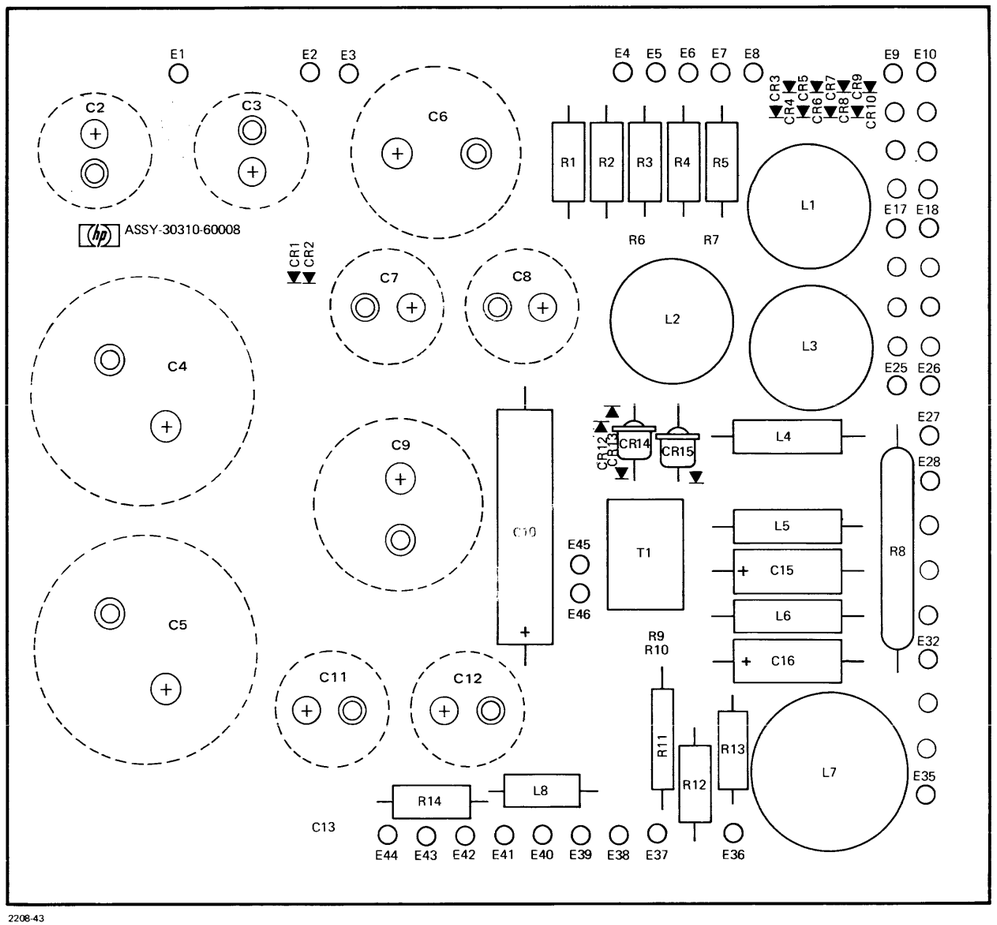
CHANGE	REFERENCE	REVISION/PREFIX



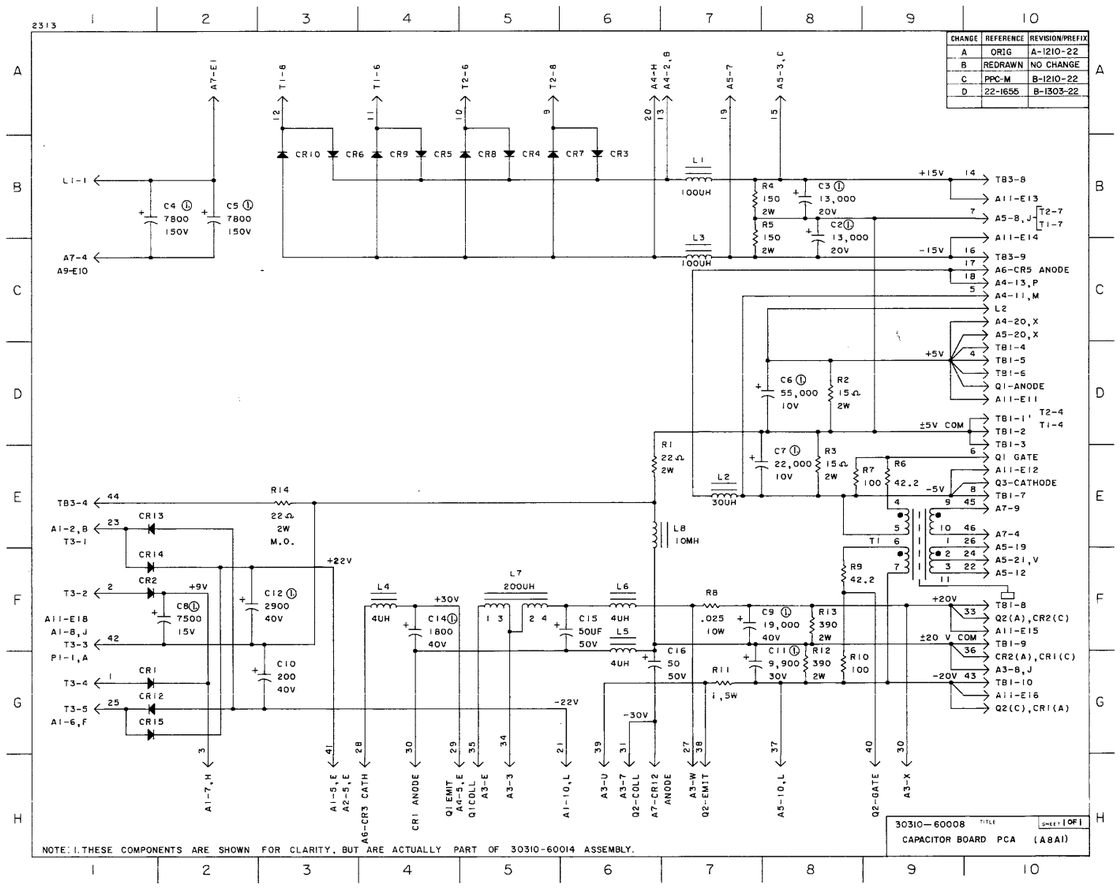
1. RESISTANCE VALUES ARE IN OHMS ±1%, ¼ W.

NOTE: UNLESS OTHERWISE SPECIFIED

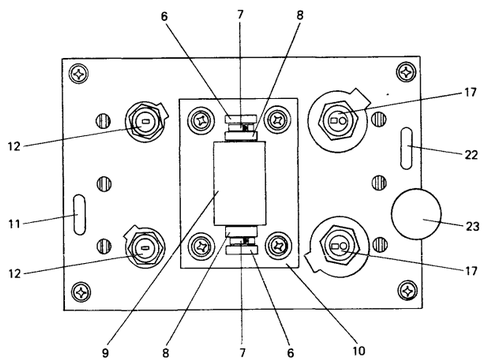
30310-60007 TITLE	SHEET 1—1
INVERTER PCA	(A7)
ENGINEER	APPROVED / DATE


E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E17
E18
E25
E26
E27
E28
E32
E35
E36
E37
E38
E39
E40
E41
E42
E43
E44
E45
E46
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
ASSY-30310-60008
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR12
CR13
CR14
CR15
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
L1
L2
L3
L4
L5
L6
L7
L8
T1
C15
C16

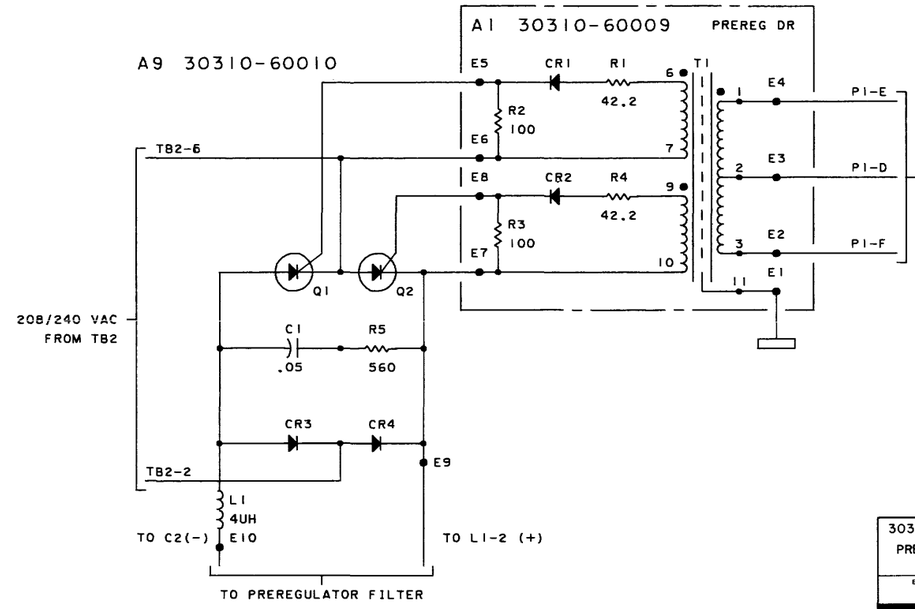
2208-43


2313
CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG | A-1210-22
B | REDRAWN | NO CHANGE
C | PPC-M | B-1210-22
D | 22-1655 | B-1303-22
CR10 CR6 CR9 CR5 CR8 CR4 CR7 CR3
L1 100UH
L3 100UH
L2 30UH
L8 10MH
L4 4UH
L7 200UH
L6 4UH
L5 4UH
C4 7800 150V
C5 7800 150V
C3 13,000 20V
C2 13,000 20V
C6 55,000 10V
C7 22,000 10V
C8 7500 15V
C12 2900 40V
C10 200 40V
C14 1800 40V
C15 50UF 50V
C16 50 50V
C9 19,000 40V
C11 9,900 30V
R1 22Ω 2W
R2 15Ω 2W
R3 15Ω 2W
R4 150 2W
R5 150 2W
R6 42.2
R7 100
R8 .025 10W
R9 42.2
R10 100
R11 1.5W
R12 390 2W
R13 390 2W
R14 22Ω 2W M.O.
T1
T2-7 T1-7
T2-4 T1-4
+15V
-15V
+5V
+5V COM
-5V
+9V
+22V
+30V
-22V
-30V
+20V
±20 V COM
-20V
TB3-8
A11-E13
A5-8,J
A11-E14
TB3-9
A6-CR5 ANODE
A4-13,P
A4-11,M
L2
A4-20,X
A5-20,X
TB1-4
TB1-5
TB1-6
Q1-ANODE
A11-E11
TB1-1
TB1-2
TB1-3
Q1 GATE
A11-E12
Q3-CATHODE
TB1-7
A7-9
A7-4
A5-19
A5-21,V
A5-12
TB1-8
Q2(A),CR2(C)
A11-E15
TB1-9
CR2(A),CR1(C)
A3-8,J
TB1-10
A11-E16
Q2(C),CR1(A)
A7-E1
T1-8
T1-6
T2-6
T2-8
A4-H A4-2,8
A5-7
A5-3,C
L1-1
A7-4 A9-E10
TB3-4
A1-2,B T3-1
T3-2
A11-E18 A1-8,J T3-3 P1-1,A
T3-4
T3-5 A1-6,F
CR13
CR14
CR2
CR1
CR12
CR15
A1-7,H
A1-5,E A2-5,E A6-CR3 CATH
CR1 ANODE
Q1 EMIT A4-5,E Q1 COLL A3-E
A3-3
A1-10,L
A3-U
A3-7 Q2-COLL
A7-CR12 ANODE
A3-W Q2-EMIT
A5-10,L
Q2-GATE
A3-X
NOTE: 1. THESE COMPONENTS ARE SHOWN FOR CLARITY, BUT ARE ACTUALLY PART OF 30310-60014 ASSEMBLY.
30310-60008 TITLE
SHEET 1 OF 1
CAPACITOR BOARD PCA (A8A1)

6	R1, R4
7	CR1, CR2
8	R2, R3
9	T1
10	A1
11	L1
12	CR3, CR4
17	Q1, Q2
22	R5
23	C1

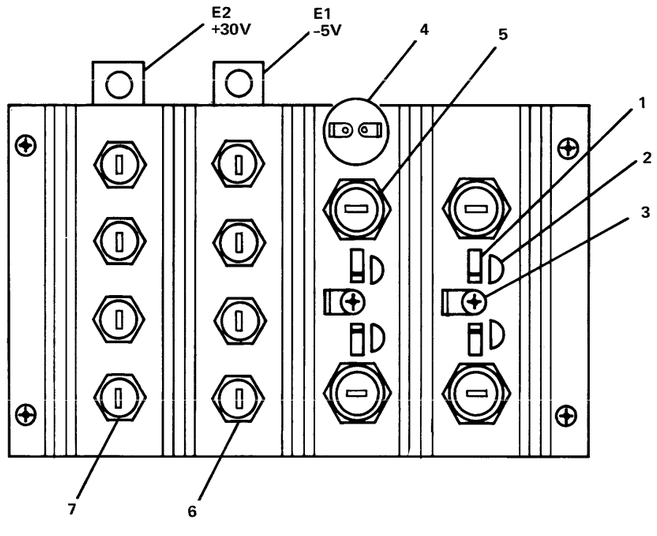


CHANGE	REFERENCE	REVISION/PREFIX

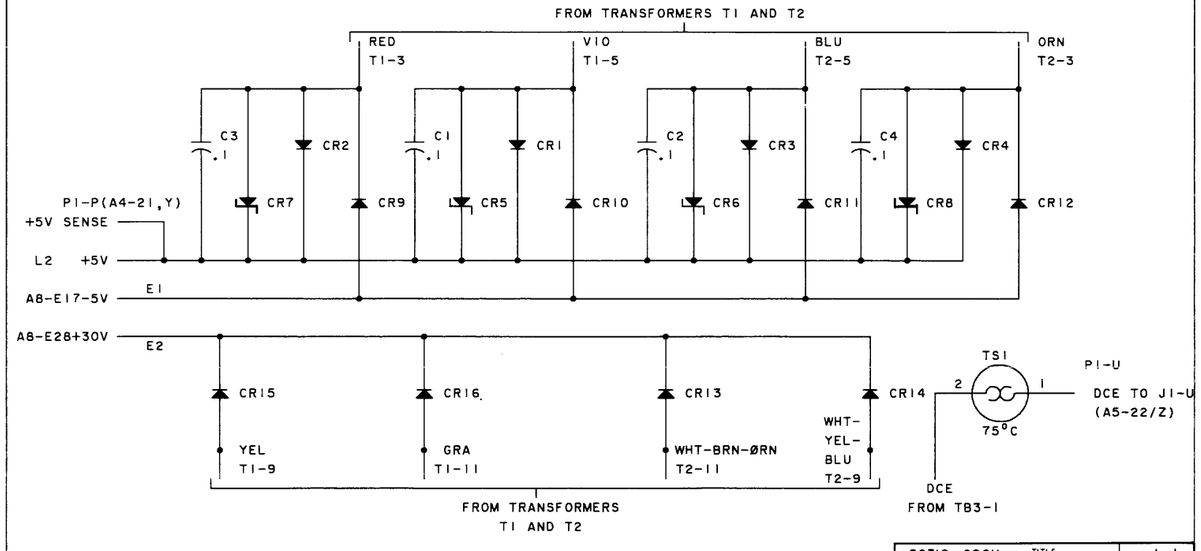


30310-60010 PREREGULATOR ASSEMBLY	TITLE	SHEET 1 — 1
		(A9)
ENGINEER	APPROVED	DATE
HEWLETT PACKARD CO DATA SYSTEMS DEVELOPMENT DIVISION		

1	CR5, 6, 7, 8
2	C1, C2, C3, C4
3	C4, C5
4	TS1
5	CR1, CR2, CR3, CR4
6	CR9, CR10, CR11, CR12
7	CR13, CR14, CR15, CR16



CHANGE	REFERENCE	REVISION/PREFIX



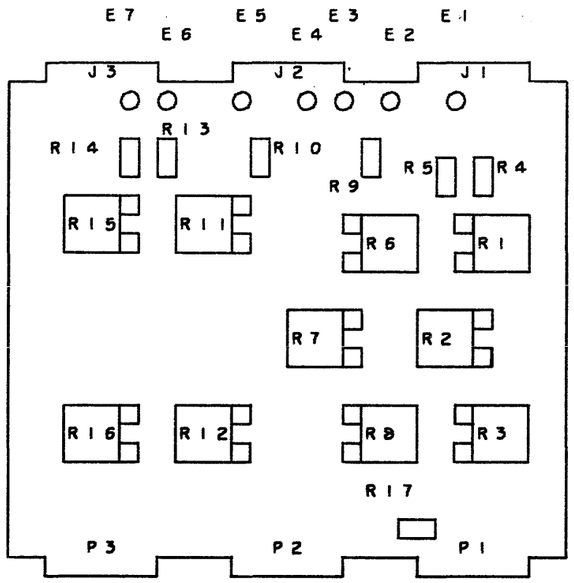
30310-60011 TITLE		SHEET 1—1
5V/30V RECTIFIER ASSEMBLY (A6)		
ENGINEER	APPROVED	DATE

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1239-22
B	REDRAWN	NO CHANGE

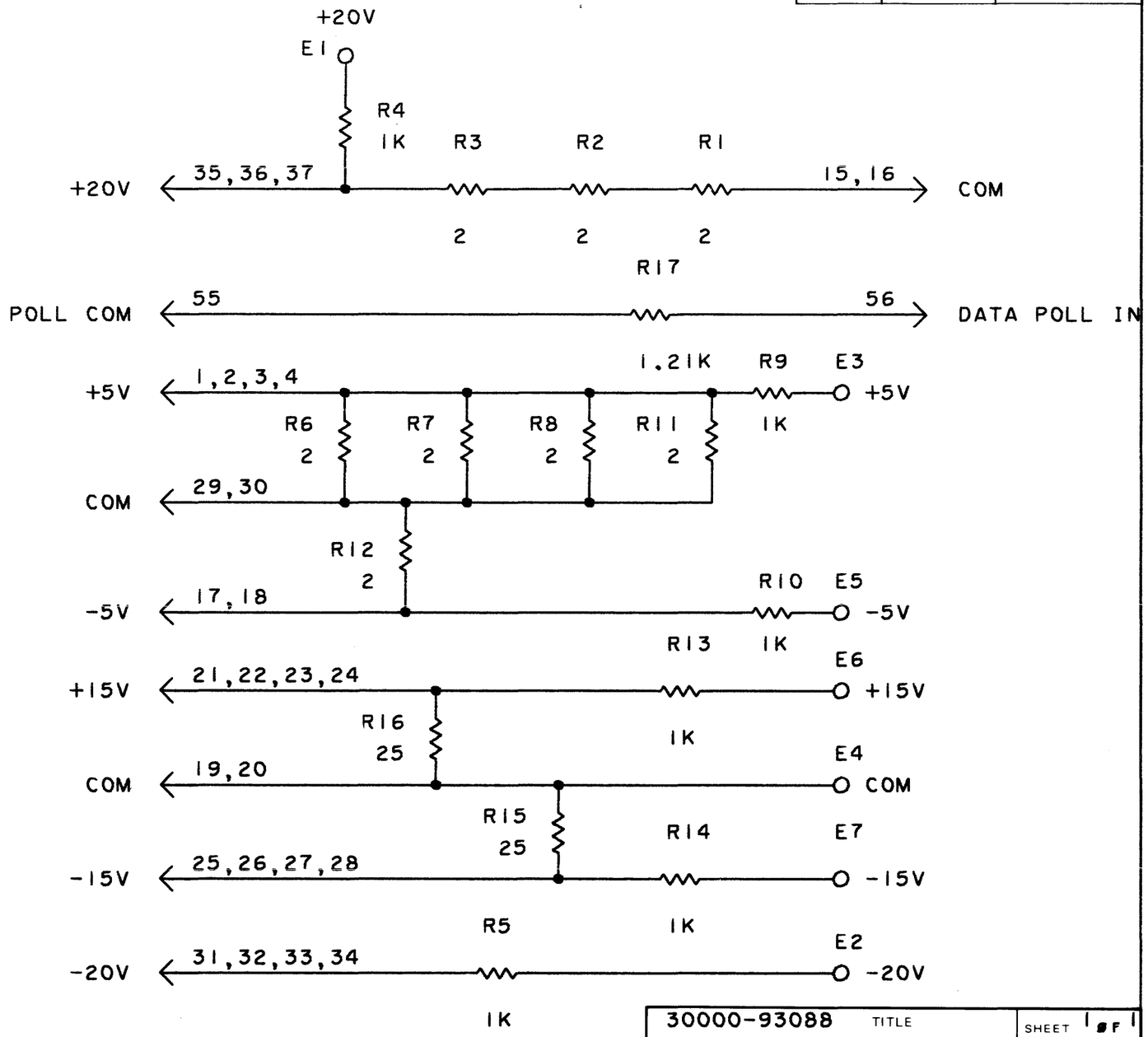
SIGNAL INDEX

P1

PIN	SIGNAL
1	+5V
2	+5V
3	+5V
4	+5V
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	COM
16	COM
17	-5V
18	-5V
19	COM
20	COM
21	+15V
22	+15V
23	+15V
24	+15V
25	-15V
26	-15V
27	-15V
28	-15V
29	COM
30	COM
31	-20V
32	-20V
33	-20V
34	-20V
35	+20V
36	+20V
37	+20V
38	+20V
39	+20V
40	+20V
41	
42	
43	
44	
45	
46	
47	
48	
49	
50	
51	
52	
53	
54	
55	+20V REG TEMP. SENSE
56	

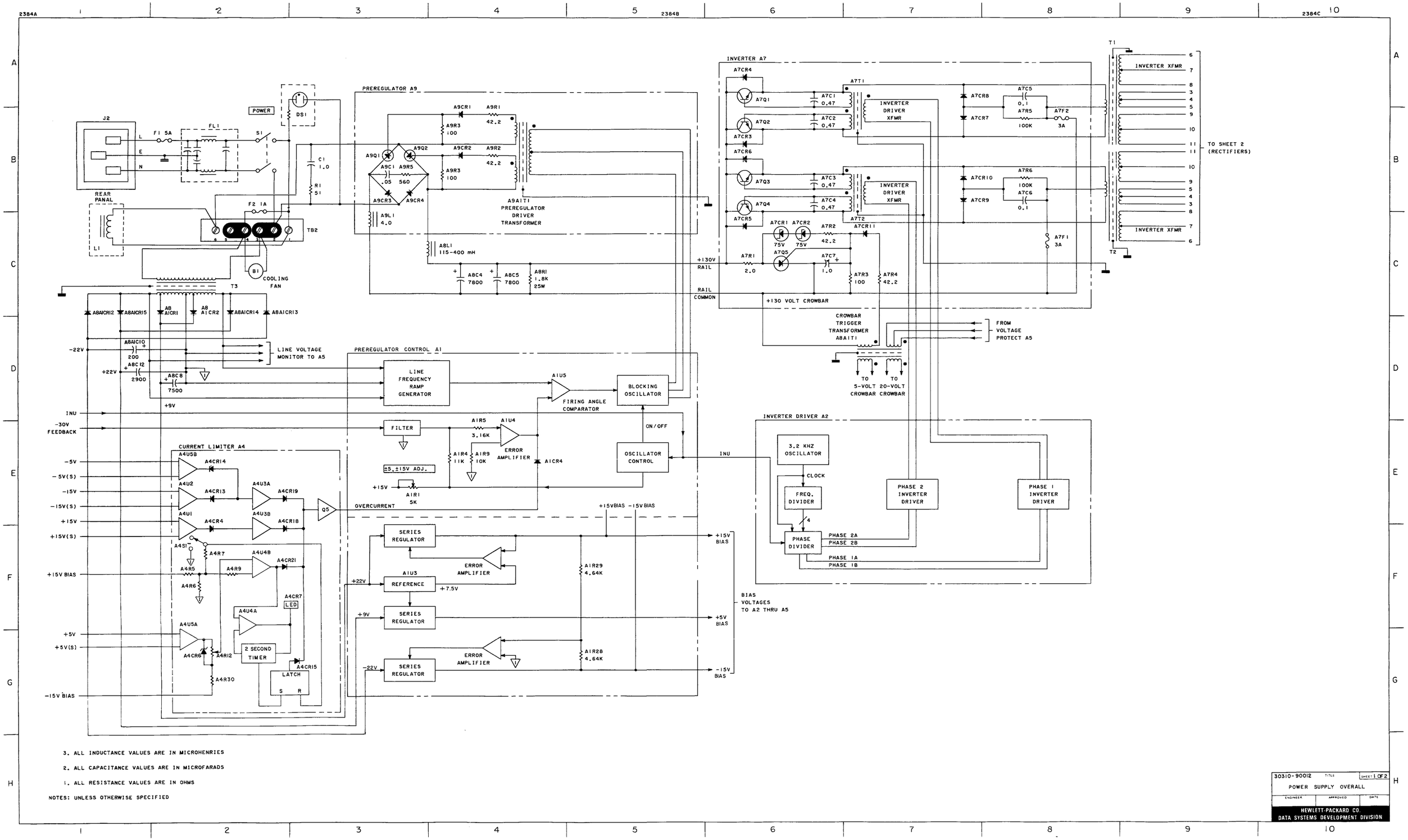


PARTS LOCATION



NOTE: 1. RESISTANCE VALUES ARE IN OHMS.
2. R1,2,3,6,7,8,11,12,15,16 ARE 30 WATT RESISTORS.
3. R4,5,9,10,13,14,17 ARE 1 WATT RESISTORS.

30000-93088 TITLE	SHEET 1 OF 1
I/O CAGE POWER SUPPLY LOAD PCA	
ENGINEER	APPROVED / DATE



3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES

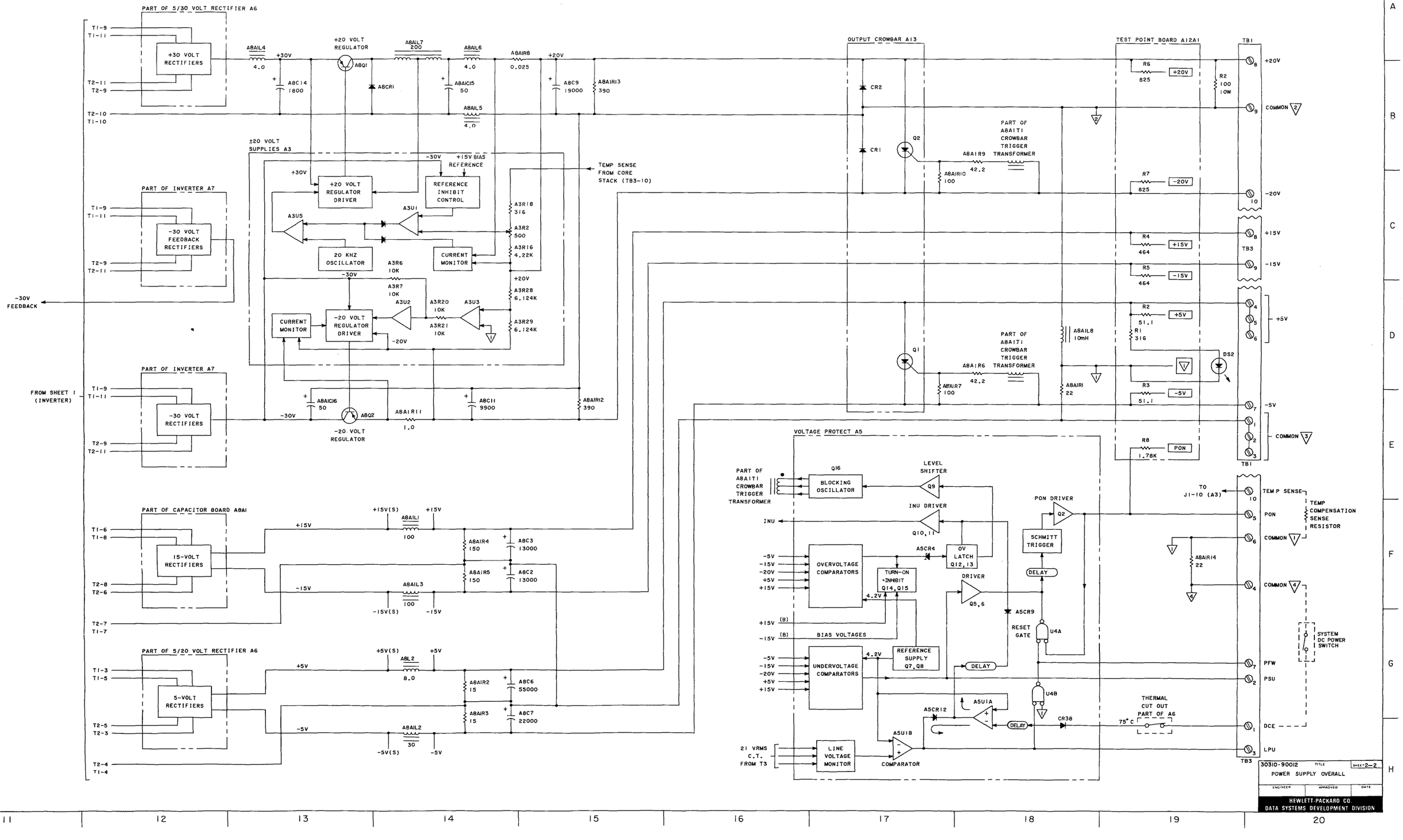
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS

1. ALL RESISTANCE VALUES ARE IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

30310-90012	TITLE	SHEET 1 OF 2
POWER SUPPLY OVERALL		
ENGINEER	APPROVED	DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION


PART OF 5/30 VOLT RECTIFIER A6
T1-9
T1-11
+30 VOLT RECTIFIERS
T2-11
T2-9
T2-10
T1-10
A8AIL4
4.0
+30V
A8C14
1800
+20 VOLT REGULATOR
A8Q1
A8CR1
A8AIL7
200
A8AIL6
4.0
A8AIC15
50
A8AIL5
4.0
A8AIR8
0.025
+20V
A8C9
19000
A8AIR13
390
±20 VOLT SUPPLIES A3
-30V
+15V BIAS REFERENCE
+30V
+20 VOLT REGULATOR DRIVER
REFERENCE INHIBIT CONTROL
TEMP SENSE FROM CORE STACK (TB3-10)
A3U1
A3U5
A3R18
316
A3R2
500
A3R16
4.22K
20 KHZ OSCILLATOR
CURRENT MONITOR
A3R6
10K
A3R7
10K
-30V
+20V
A3R28
6.124K
A3U2
A3U3
A3R20
10K
A3R21
10K
A3R29
6.124K
CURRENT MONITOR
-20 VOLT REGULATOR DRIVER
-20V
PART OF INVERTER A7
T1-9
T1-11
-30 VOLT FEEDBACK RECTIFIERS
T2-9
T2-11
-30V FEEDBACK
PART OF INVERTER A7
FROM SHEET 1 (INVERTER)
T1-9
T1-11
-30 VOLT RECTIFIERS
T2-9
T2-11
A8AIC16
50
-30V
A8Q2
-20 VOLT REGULATOR
A8AIR11
1.0
A8C11
9900
A8AIR12
390
PART OF CAPACITOR BOARD A8AI
T1-6
T1-8
15-VOLT RECTIFIERS
T2-8
T2-6
T2-7
T1-7
+15V(S)
+15V
A8AIL1
100
+15V
A8AIR4
150
A8C3
13000
A8AIR5
150
A8C2
13000
-15V
A8AIL3
100
-15V(S)
-15V
PART OF 5/20 VOLT RECTIFIER A6
T1-3
T1-5
5-VOLT RECTIFIERS
T2-5
T2-3
T2-4
T1-4
+5V(S)
+5V
A8L2
8.0
+5V
A8AIR2
15
A8C6
55000
A8AIR3
15
A8C7
22000
-5V
A8AIL2
30
-5V(S)
-5V
OUTPUT CROWBAR A13
CR2
CR1
Q2
PART OF A8AITI CROWBAR TRIGGER TRANSFORMER
A8AIR9
42.2
A8AIR10
100
Q1
A8AIL8
10mH
A8AIR6
42.2
A8AIR7
100
A8AIR1
22
TEST POINT BOARD A12A1
R6
825
+20V
R7
825
-20V
R4
464
+15V
R5
464
-15V
R2
51.1
+5V
R1
316
DS2
R3
51.1
-5V
R8
1.78K
PON
R2
100
10W
COMMON
TB1
+20V
COMMON
-20V
TB3
+15V
-15V
+5V
-5V
COMMON
TO J1-10 (A3)
TEMP SENSE
PON
COMMON
COMMON
COMMON
PFW
PSU
DCE
LPU
TEMP COMPENSATION SENSE RESISTOR
A8AIR14
22
SYSTEM DC POWER SWITCH
VOLTAGE PROTECT A5
PART OF A8AITI CROWBAR TRIGGER TRANSFORMER
Q16
BLOCKING OSCILLATOR
LEVEL SHIFTER
Q9
INU
INU DRIVER
Q10,11
PON DRIVER
Q2
SCHMITT TRIGGER
-5V
-15V
-20V
+5V
+15V
OVERVOLTAGE COMPARATORS
A5CR4
OV LATCH Q12,13
TURN-ON INHIBIT Q14,Q15
4.2V
DRIVER
Q5,6
DELAY
A5CR9
+15V (B)
-15V (B)
BIAS VOLTAGES
RESET GATE
U4A
-5V
-15V
-20V
+5V
+15V
UNDERVOLTAGE COMPARATORS
4.2V
REFERENCE SUPPLY Q7,Q8
DELAY
U4B
A5U1A
A5CR12
DELAY
CR38
THERMAL CUT OUT PART OF A6
75°C
A5U1B
COMPARATOR
21 VRMS C.T. FROM T3
LINE VOLTAGE MONITOR
30310-90012
TITLE
POWER SUPPLY OVERALL
SHEET 2-2
ENGINEER
APPROVED
DATE
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

DETAILED DIAGRAM SET

DD-800

AUXILIARY CONTROL PANEL INPUT PCB

30350-60001
SERIES 1238

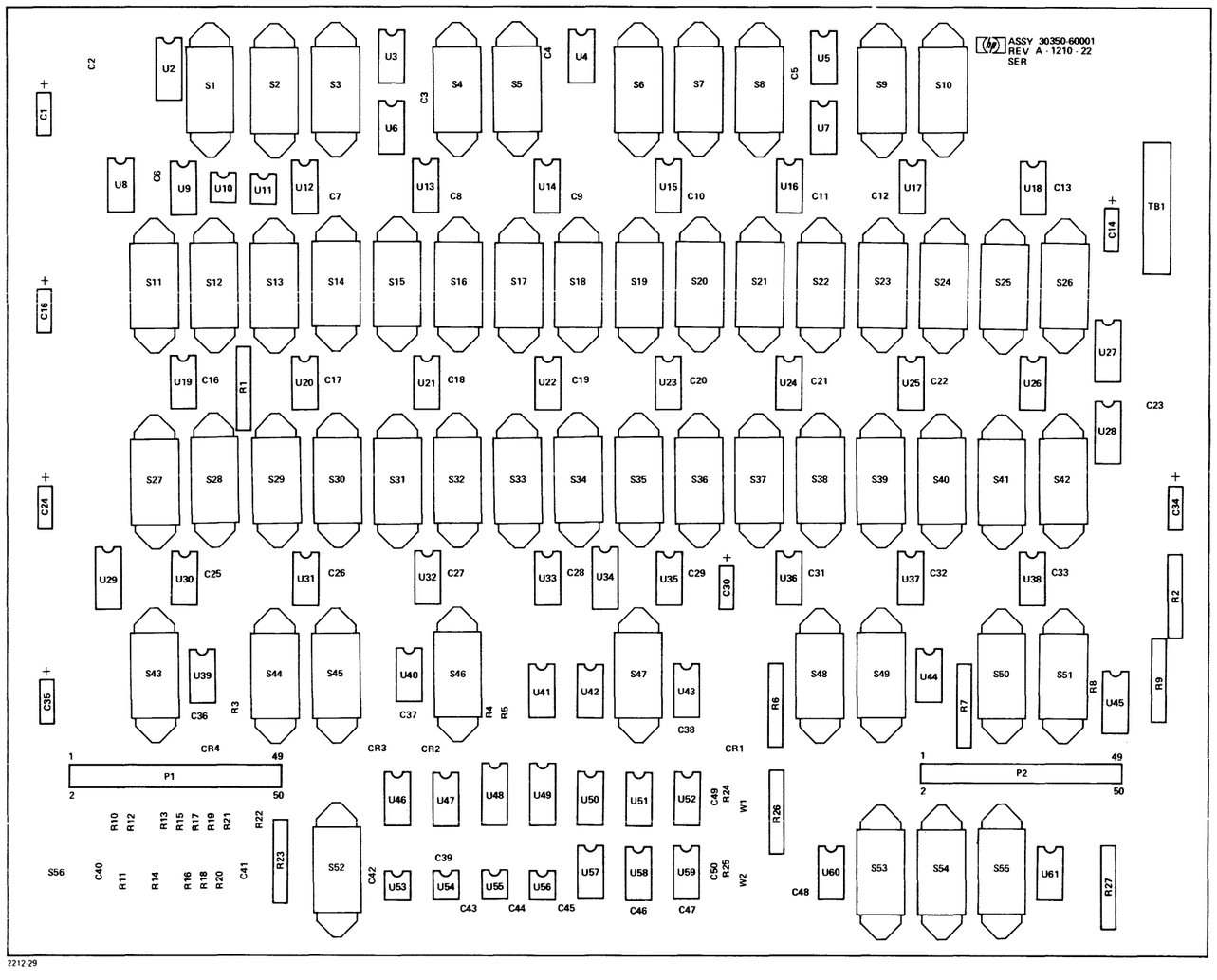
REV C

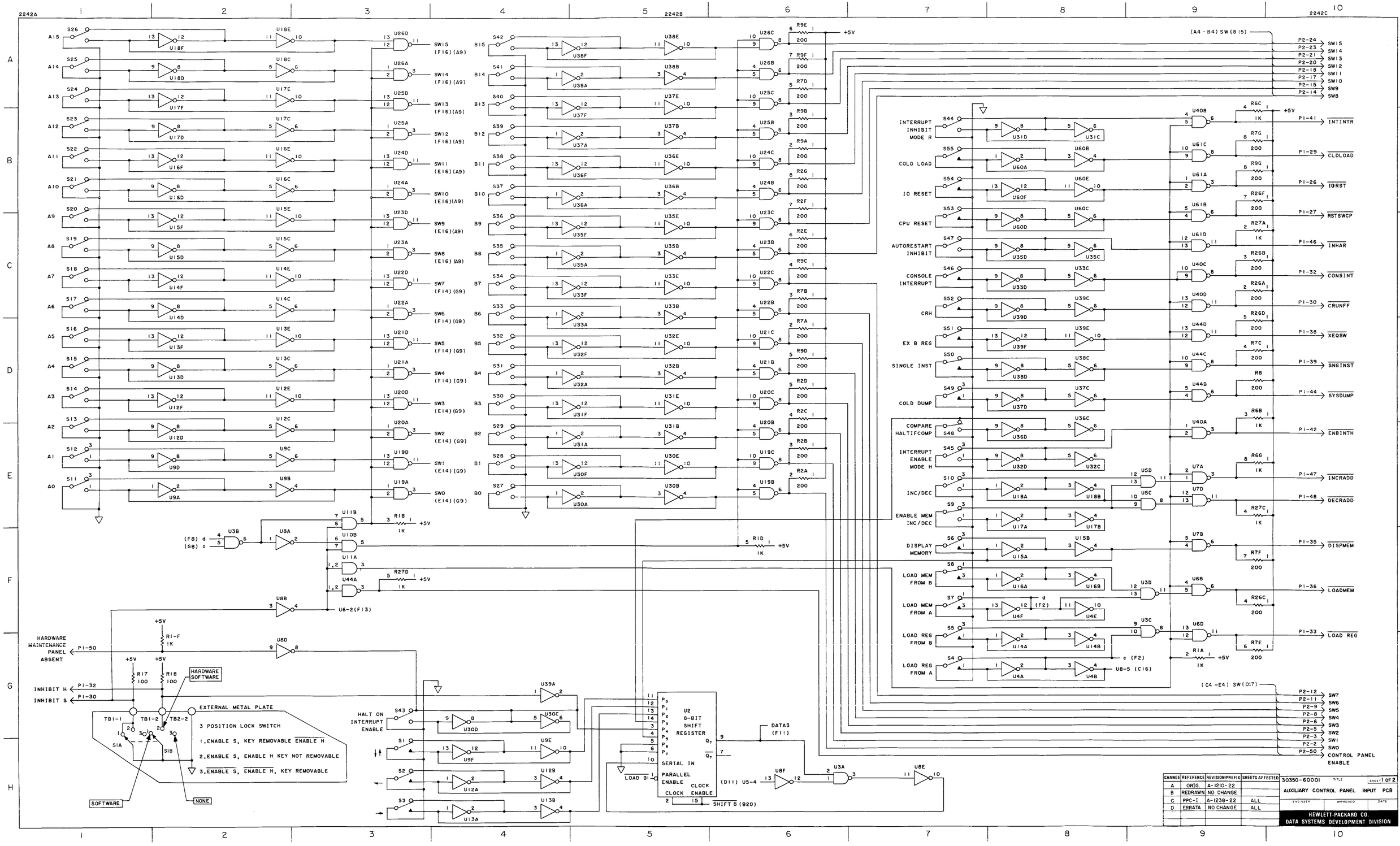
SIGNAL INDEX

P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL
1		1	
2	$\overline{A0}$	2	SW0
3		3	SW1
4	$\overline{A1}$	4	
5		5	SW2
6	$\overline{A2}$	6	SW3
7		7	
8	$\overline{A3}$	8	SW4
9		9	SW5
10	$\overline{\text{LOAD A1}}$	10	
11		11	SW6
12	$\overline{\text{LOAD A2}}$	12	SW7
13		13	
14	$\overline{\text{SHIFT A}}$	14	SW8
15		15	SW9
16	$\overline{B0}$	16	
17		17	SW10
18	$\overline{B1}$	18	SW11
19		19	
20	$\overline{B2}$	20	SW12
21		21	SW13
22	$\overline{\text{LOAD B1}}$	22	
23		23	SW14
24	$\overline{\text{LOAD B2}}$	24	SW15
25		25	
26	$\overline{\text{SHIFT B}}$	26	
27	$\overline{\text{CPURST}}$	27	
28	$\overline{\text{CLOCK}}$	28	
29	$\overline{\text{CLDLOAD}}$	29	
30	$\overline{\text{INHIBIT S}}$	30	
31		31	
32	$\overline{\text{INHIBIT H}}$	32	
33	$\overline{\text{LOAD REG}}$	33	
34	$\overline{\text{RAR COMP}}$	34	
35	$\overline{\text{DISPMEM}}$	35	
36	$\overline{\text{B COMP}}$	36	
37	$\overline{\text{SNGINST}}$	37	
38	$\overline{\text{EXT CLOCK}}$	38	
39		39	
40	$\overline{\text{RESET}}$	40	
41	$\overline{\text{INTINTR}}$	41	
42	$\overline{\text{DATA-A}}$	42	
43		43	BKPTHALT
44	$\overline{\text{DATA-B}}$	44	
45		45	RUN
46	LOCAL MODE	46	
47	$\overline{\text{INCRADD}}$	47	
48	TEST MODE	48	
49		49	SYSHALT
50	HARDWARE ABSENCE	50	CONTROL PANEL ENABLE

I.C. INDEX

U	1820-	U	1820-	U	1820-
2	0262	30-39	0307	50	0512
3	0370			51	0424
4	0370	40	0621	52	0207
5	0141	41	0374	53-56	0535
6,7	0621	42	0512	57	0370
8,9	0307	43	0695	58	0141
10,11	0535	44	0621	59	0207
13-18	0307	45	0262		
19-26	0621	46,47	0621	60	0307
27,28	0262	48,49	0233	61	0621
29	0615				





CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG	A-1210-22	
B	REDRAWN	NO CHANGE	
C	PPC-1	A-1238-22	ALL
D	ERRATA	NO CHANGE	ALL

30350-60001 TITLE SHEET 1 OF 2

AUXILIARY CONTROL PANEL INPUT PCB

ENGINEER APPROVED DATE

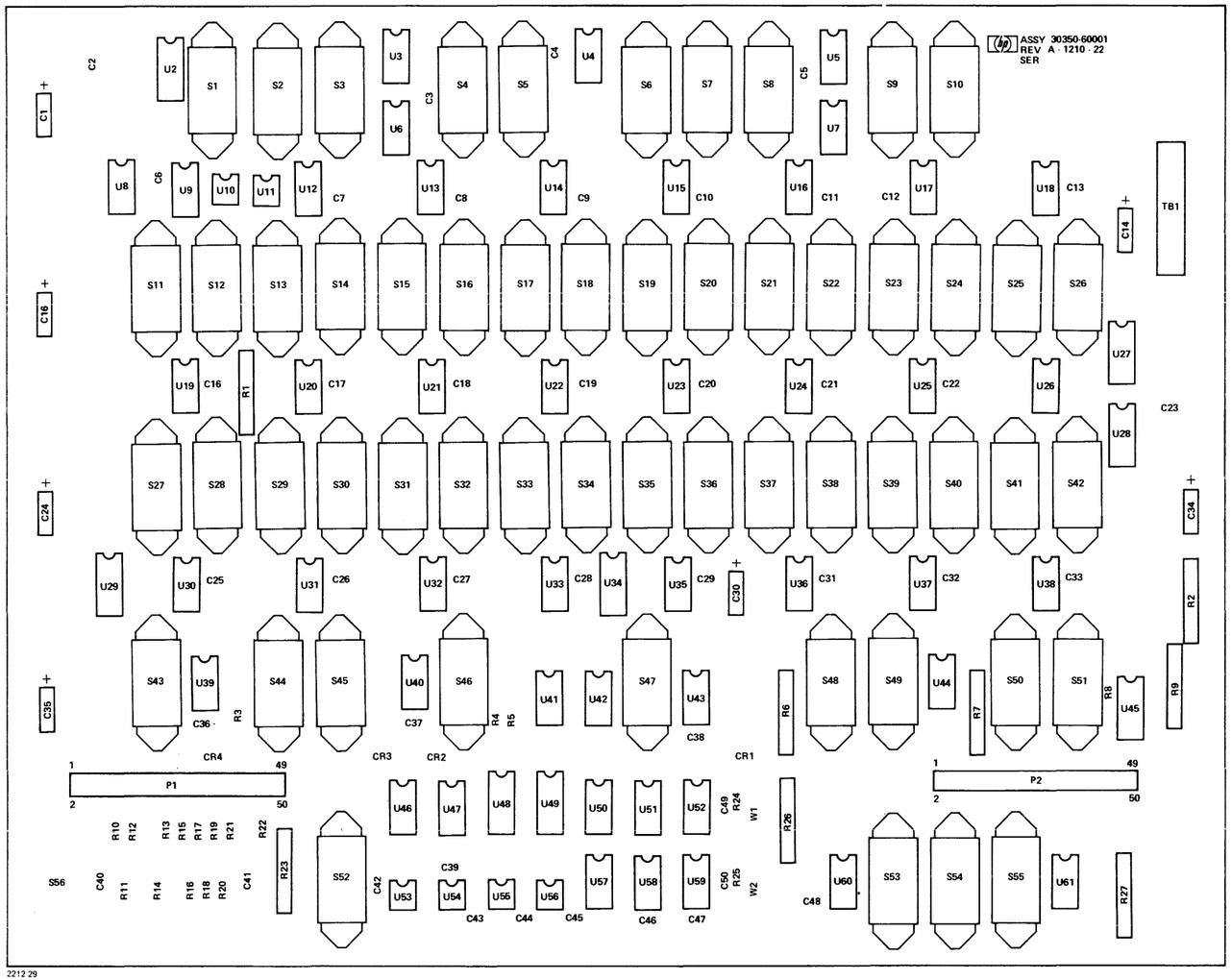
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

SIGNAL INDEX

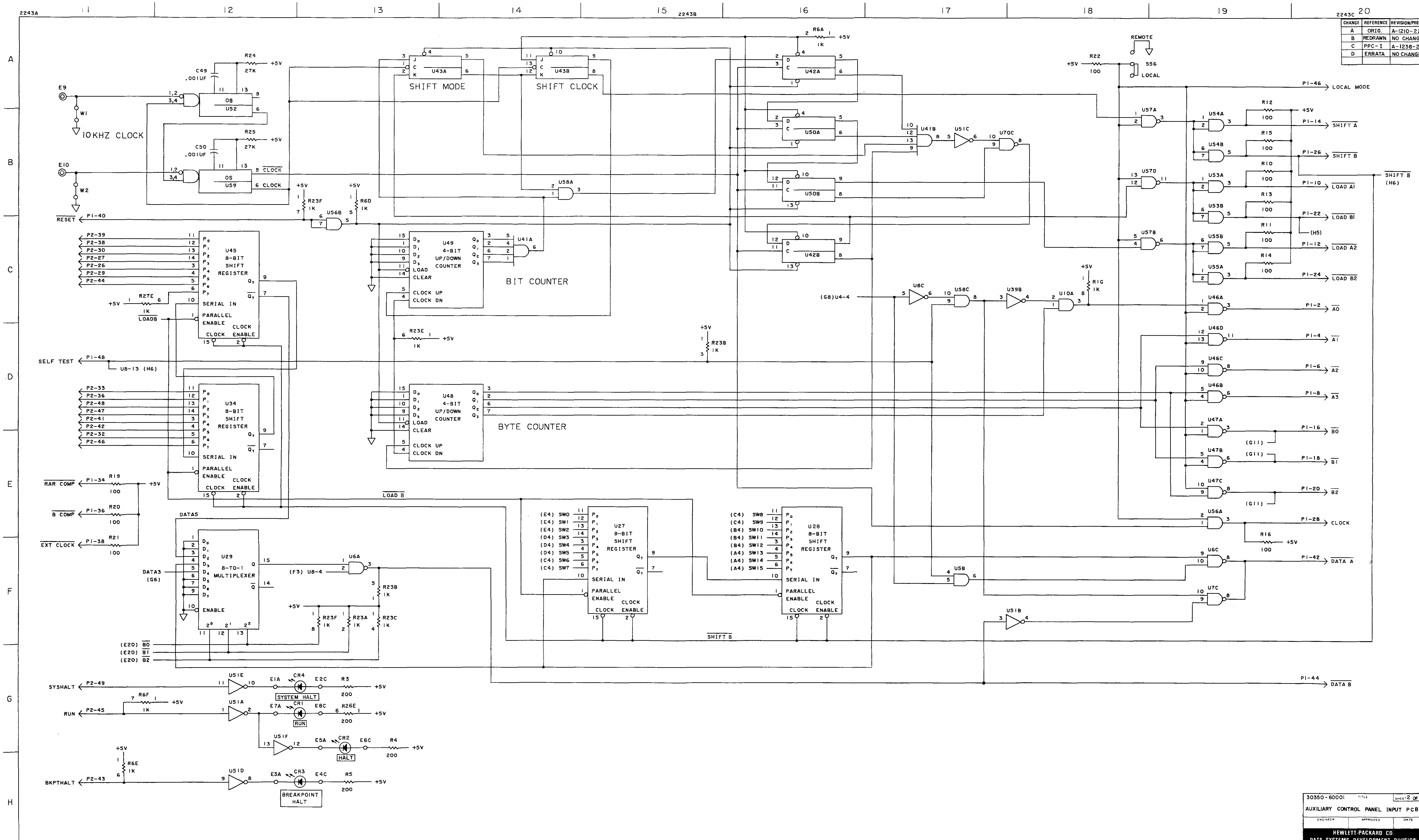
P1 PIN	P1 SIGNAL	P2 PIN	P2 SIGNAL
1		1	
2	$\overline{A0}$	2	SW0
3		3	SW1
4	$\overline{A1}$	4	
5		5	SW2
6	$\overline{A2}$	6	SW3
7		7	
8	$\overline{A3}$	8	SW4
9		9	SW5
10	$\overline{\text{LOAD A1}}$	10	
11		11	SW6
12	$\overline{\text{LOAD A2}}$	12	SW7
13		13	
14	$\overline{\text{SHIFT A}}$	14	SW8
15		15	SW9
16	$\overline{B0}$	16	
17		17	SW10
18	$\overline{B1}$	18	SW11
19		19	
20	$\overline{B2}$	20	SW12
21		21	SW13
22	$\overline{\text{LOAD B1}}$	22	
23		23	SW14
24	$\overline{\text{LOAD B2}}$	24	SW15
25		25	
26	$\overline{\text{SHIFT B}}$	26	
27	$\overline{\text{CPURST}}$	27	
28	$\overline{\text{CLOCK}}$	28	
29	$\overline{\text{CLDLOAD}}$	29	
30	INHIBIT S	30	
31		31	
32	$\overline{\text{INHIBIT H}}$	32	
33	$\overline{\text{LOAD REG}}$	33	
34	$\overline{\text{RAR COMP}}$	34	
35	$\overline{\text{DISPMEM}}$	35	
36	$\overline{\text{B COMP}}$	36	
37	$\overline{\text{SNGINST}}$	37	
38	$\overline{\text{EXT CLOCK}}$	38	
39		39	
40	$\overline{\text{RESET}}$	40	
41	$\overline{\text{INTINTR}}$	41	
42	DATA-A	42	
43		43	BKPTHALT
44	$\overline{\text{DATA-B}}$	44	
45		45	RUN
46	LOCAL MODE	46	
47	$\overline{\text{INCRADD}}$	47	
48	TEST MODE	48	
49		49	SYSHALT
50	HARDWARE ABSENCE	50	CONTROL PANEL ENABLE

I.C. INDEX

U	1820-	U	1820-	U	1820-
2	0262	30-39	0307	50	0512
3	0370			51	0424
4	0370	40	0621	52	0207
5	0141	41	0374	53-56	0535
6,7	0621	42	0512	57	0370
8,9	0307	43	0695	58	0141
10,11	0535	44	0621	59	0207
13-18	0307	45	0262		
19-26	0621	46,47	0621	60	0307
27,28	0262	48,49	0233	61	0621
29	0615				



2212 29



CHANGE | REFERENCE | REVISION/PREFIX
A | ORIG. | A-1210-22
B | REDRAWN | NO CHANGE
C | PPC-I | A-1238-22
D | ERRATA | NO CHANGE
10KHZ CLOCK
SHIFT MODE
SHIFT CLOCK
BIT COUNTER
BYTE COUNTER
U45 8-BIT SHIFT REGISTER
U34 8-BIT SHIFT REGISTER
U49 4-BIT UP/DOWN COUNTER
U48 4-BIT UP/DOWN COUNTER
U29 8-TO-1 MULTIPLEXER
U27 8-BIT SHIFT REGISTER
U28 8-BIT SHIFT REGISTER
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE
CLOCK UP
CLOCK DN
RESET
SELF TEST
RAR COMP
B COMP
EXT CLOCK
SYSHALT
RUN
BKPTHALT
SYSTEM HALT
HALT
BREAKPOINT HALT
REMOTE
LOCAL
LOCAL MODE
SHIFT A
SHIFT B
LOAD A1
LOAD B1
LOAD A2
LOAD B2
CLOCK
DATA A
DATA B
LOAD B
DATA5
DATA3
30350-60001
SHEET 2 OF 2
AUXILIARY CONTROL PANEL INPUT PCB
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

DETAILED DIAGRAM SET

DD-801

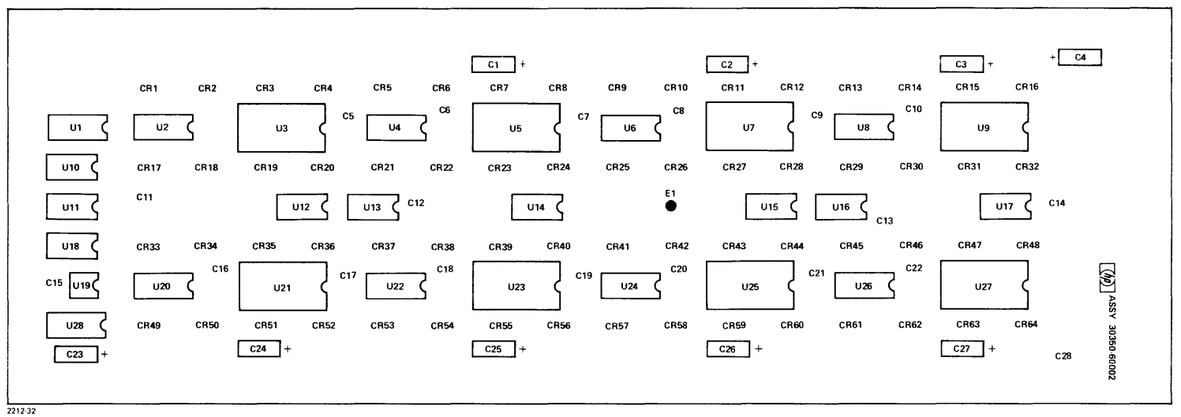
AUXILIARY CONTROL PANEL DISPLAY PCB

30350-60002

SERIES 1210

I.C. INDEX

U	1810-	U	1820-	U	1820-
1	0037	3	0742	17	0141
2	0124	5	0742	18	0373
4	0124	7	0742	19	0535
6	0124	9	0742		
8	0124	10	0424	21	0742
				23	0742
20	0124	11	0373	25	0742
22	0124	12	0141	27	0724
24	0124	13	0294		
26	0124	14,15	0141		
28	0037	16	0294		



2212-32

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-B	B-1210-22

DATA A ← P1-42
SHIFT A ← P1-14
A0 ← P1-2
A1 ← P1-4
A2 ← P1-6
A3 ← P1-8
LOAD A2 ← P1-12
RESET ← P1-40

U13 8-BIT SHIFT REGISTER (DATA IN, CLOCK, CLEAR)
U16 8-BIT SHIFT REGISTER (DATA IN, CLOCK, CLEAR)
U1E 1K, U1G 1K, U1D 1K, U1C 1K, U1B 1K, U1A 1K, U1H 1K, U1F 1K
U12A, U12B, U12C, U12D, U14B, U14A, U14C, U14D
U15A, U15B, U15C, U15D, U17B, U17A, U17C, U17D
U10C, U10B, U10A
U11A, U11B, U18B, U18A
U19A, U19B
U28F 1K, U28E 1K
BYTE8, BYTE9, BYTE10, BYTE11, LOAD, RESET

+5V
.01UF C5-22,28
33UF C1-4,23-27
GROUND ON ALL ODD PINS

1. ALL RESISTOR VALUES ARE 200 OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

U21A 4-BIT REGISTER — CR33 RA, CR34 RB, CR35 RC, CR36 RD
U22A 4-BIT REGISTER — CR37 SP2, CR38 SP3, CR39 OPND, CR40 10A
U25A 4-BIT REGISTER — CR41 10D, CR42 CTRL, CR43 CPX1, CR44 CPX2
U26A 4-BIT REGISTER — CR45 RAR, CR46 MOD, CR47 PADD, CR48
U21B 4-BIT REGISTER — CR49 ADDRESS, CR50 DATA, CR51 STA, CR52 X
U22B 4-BIT REGISTER — CR53 PB, CR54 P, CR55 PL, CR56
U25B 4-BIT REGISTER — CR57 DB, CR58 Q, CR59 S, CR60 Z
U26B 4-BIT REGISTER — CR61 MASK, CR62 SPARE, CR63 SPARE, CR64 SPARE

REG SELECT

U3A 4-BIT REGISTER — CR1, CR2, CR3, CR4
U5A 4-BIT REGISTER — CR5, CR6, CR7, CR8
U7A 4-BIT REGISTER — CR9, CR10, CR11, CR12
U9A 4-BIT REGISTER — CR13, CR14, CR15, CR16
U3B 4-BIT REGISTER — CR17, CR18, CR19, CR20
U5B 4-BIT REGISTER — CR21, CR22, CR23, CR24
U7B 4-BIT REGISTER — CR25, CR26, CR27, CR28
U9B 4-BIT REGISTER — CR29, CR30, CR31, CR32

REG DISPLAY

CURRENT INSTRUCTION REGISTER DISPLAY

SELECTED REGISTER DISPLAY CIRCUITS

30350-60002 TITLE SHEET 1 of 1
AUXILIARY CONTROL PANEL DISPLAY PCB

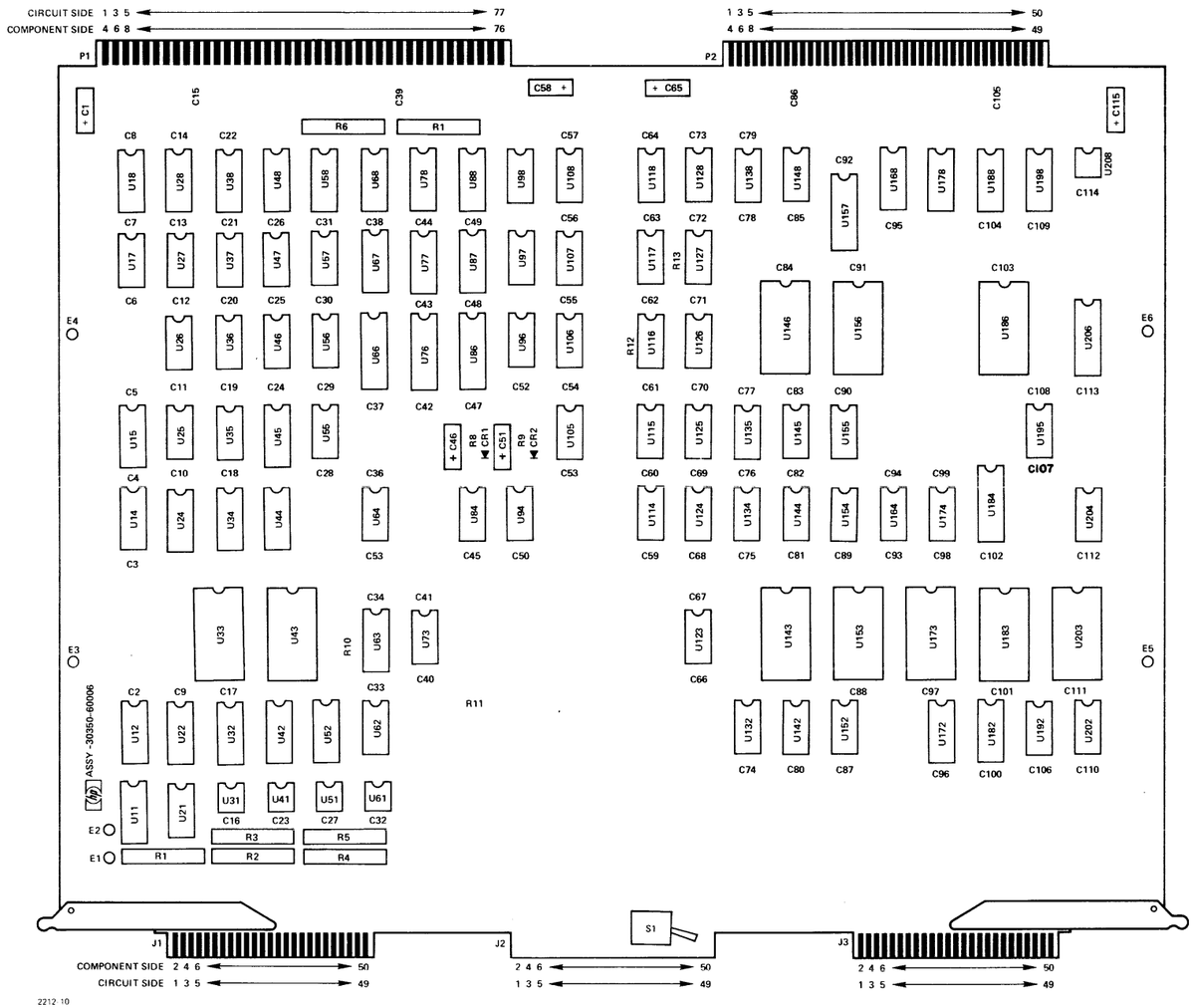
DETAILED DIAGRAM SET

DD-802

AUXILIARY CONTROL PANEL INTERFACE PCA

30350-60006

SERIES 1233


CIRCUIT SIDE 1 3 5
COMPONENT SIDE 4 6 8
77
76
P1
1 3 5
4 6 8
50
49
P2
+ C1
C15
C39
C58 +
+ C65
C86
C105
+ C115
R6
R1
C8
C14
C22
C57
C64
C73
C79
C92
U18
U28
U38
U48
U58
U68
U78
U88
U98
U108
U118
U128
U138
U148
U157
U168
U178
U188
U198
U208
C114
C7
C13
C21
C26
C31
C38
C44
C49
C56
C63
C72
C78
C85
C95
C104
C109
U17
U27
U37
U47
U57
U67
U77
U87
U97
U107
U117
U127
R13
C6
C12
C20
C25
C30
C43
C48
C55
C62
C71
C84
C91
C103
E4
E6
U26
U36
U46
U56
U66
U76
U86
U96
U106
U116
U126
R12
U146
U156
U186
U206
C5
C11
C19
C24
C29
C37
C42
C47
C52
C54
C61
C70
C77
C83
C90
C108
C113
U15
U25
U35
U45
U55
U105
U115
U125
U135
U145
U155
U195
C107
+ C46
R8
CR1
+ C51
R9
CR2
C4
C10
C18
C28
C36
C53
C60
C69
C76
C82
C94
C99
U14
U24
U34
U44
U64
U84
U94
U114
U124
U134
U144
U154
U164
U174
U184
U204
C3
C53
C45
C50
C59
C68
C75
C81
C89
C93
C98
C102
C112
C34
C41
C67
U33
U43
U63
U73
U123
U143
U153
U173
U183
U203
E3
E5
R10
C33
C40
C66
C88
C97
C101
C111
C2
C9
C17
R11
U12
U22
U32
U42
U52
U62
U132
U142
U152
U172
U182
U192
U202
C74
C80
C87
C96
C100
C106
C110
ASSY - 30350-60006
U11
U21
U31
U41
U51
U61
C16
C23
C27
C32
E2
R3
R5
E1
R1
R2
R4
J1
J2
S1
J3
COMPONENT SIDE 2 4 6
CIRCUIT SIDE 1 3 5
50
49
2 4 6
1 3 5
50
49
2 4 6
1 3 5
50
49

2212-10

CHANGE	REFERENCE	REVISION/PREFIX	SHEETS AFFECTED
A	ORIG.	A-1210-22	ALL
B	REDRAWN	NO CHANGE	ALL
C	PPC-A	" " "	1
D	PPC-B	" " "	1
E	PPC-C	A-1233-22	1
F	22,168	B-1233-22	ALL

ROR2DISP (E26)

U57C, U57A, U57D, U57B

RF1 P1-47
RF2 P1-48
RF3 P1-45
RF0 P1-49

U67 4-BIT REGISTER

FREEZE (B7)

FREEZE / CLOCK P1-79 P1-78

U97

INPUT ENABLE, OUTPUT ENABLE, CLOCK, MR

U86 ENABLE 9,11

SF4 P1-62

U77 4-BIT REGISTER

SF3 P1-73
SF2 P1-74
SF1 P1-68
SF0 P1-67

U87 4-BIT REGISTER

ROR24 P1-54
ROR25 P1-57
ROR26 P1-56
ROR27 P1-55

U68 8-BIT SHIFT REGISTER

ROR16 P1-72
ROR17 P1-71
ROR18 P1-70
ROR19 P1-69
ROR20 P1-63
ROR21 P1-64
ROR22 P1-65
ROR23 P1-66

U88 8-BIT SHIFT REGISTER

LOADA1 J1-10

U31A

R2,3G 200

+5V

R10 1K

LOADA1 (B18),(F11)

SMCUDATA P2-13
STOFROM P2-16
SRDYENBL P2-15

ST3 P1-50
ST4 P1-51
ROR10 P1-52
ROR11 P1-53
ROR12 P1-46
ROR13 P1-43
ROR14 P1-44
ROR15 P1-41

U58 8-BIT SHIFT REGISTER

STO P1-61
ST1 P1-59
ST2 P1-58

U78 8-BIT SHIFT REGISTER

SCIR P2-14
SIOP P2-9

QS P1-25
DS P1-26
SKIP P1-28
LUTGATE P1-27
OPNDSEL P1-24
INSTSEL P1-23
RESRUDA P1-22
RESRUDB P1-21

U38 8-BIT SHIFT REGISTER

INTFLAG P1-35
DISPFLAG P1-36
NXT=1 P1-37
NXT=2 P1-38
OPINP P1-34
NIP P1-33
IOINP P1-32
W P1-31

U48 8-BIT SHIFT REGISTER

+5V R11 1K

R2,3E 200

U31B

SHIFTA (G11) (D19)

SHIFTA J1-14

A0 J1-2
A3 J1-8
A2 J1-0
A1 J1-4

A0 TEST POINT

U21D, U21C, U21B

U12 8-TO-1 MULTIPLEXER

U11 8-TO-1 MULTIPLEXER

(H14) A
(A20) DATA10
(C20) DATA11

ENABLE, 2^0 2^1 2^2

R1D 1K
R1A 1K
R1B 1K
R1C 1K

CARRY P1-6
OVFL P1-8
BNDV P1-7
EXTINT P1-9
INTRP P1-5
IOTIMER P1-4
CPUTIMER P1-3

U18 8-BIT SHIFT REGISTER

U96A

FREEZE (C1)

FREEZE-(B) (E29)

U26

XFRZ (D26)

FLAG1 P1-13
FLAG2 P1-15
FLAG3 P1-16
TNAME0 P1-18
TNAME1 P1-14
NOP1 P1-11
NOP2 P1-12
REPEAT P1-10

U28 8-BIT SHIFT REGISTER

RAR0 P2-61
RAR1 P2-62
RAR2 P2-58
RAR3 P2-57
RAR4 P2-54
RAR5 P2-53
RAR6 P2-56
RAR7 P2-55

RAR0 (C29) … RAR7 (E29)

U178 8-BIT SHIFT REGISTER

RAR8 P2-51
RAR9 P2-52
RAR10 P2-49
RAR11 P2-50

RAR8 (A29) … RAR11 (B29)

U168 8-BIT SHIFT REGISTER

U0 P2-77
U1 P2-10
U2 P2-75
U3 P2-76
U4 P2-72
U5 P2-71
U6 P2-74
U7 P2-73

(B24) U0 … (C24) U7

U198 8-BIT SHIFT REGISTER

U8 P2-69
U9 P2-70
U10 P2-68
U11 P2-67
U12 P2-65
U13 P2-66
U14 P2-63
U15 P2-64

(D24) U8 … (D24) U15

U188 8-BIT SHIFT REGISTER

DATA9C (H13)

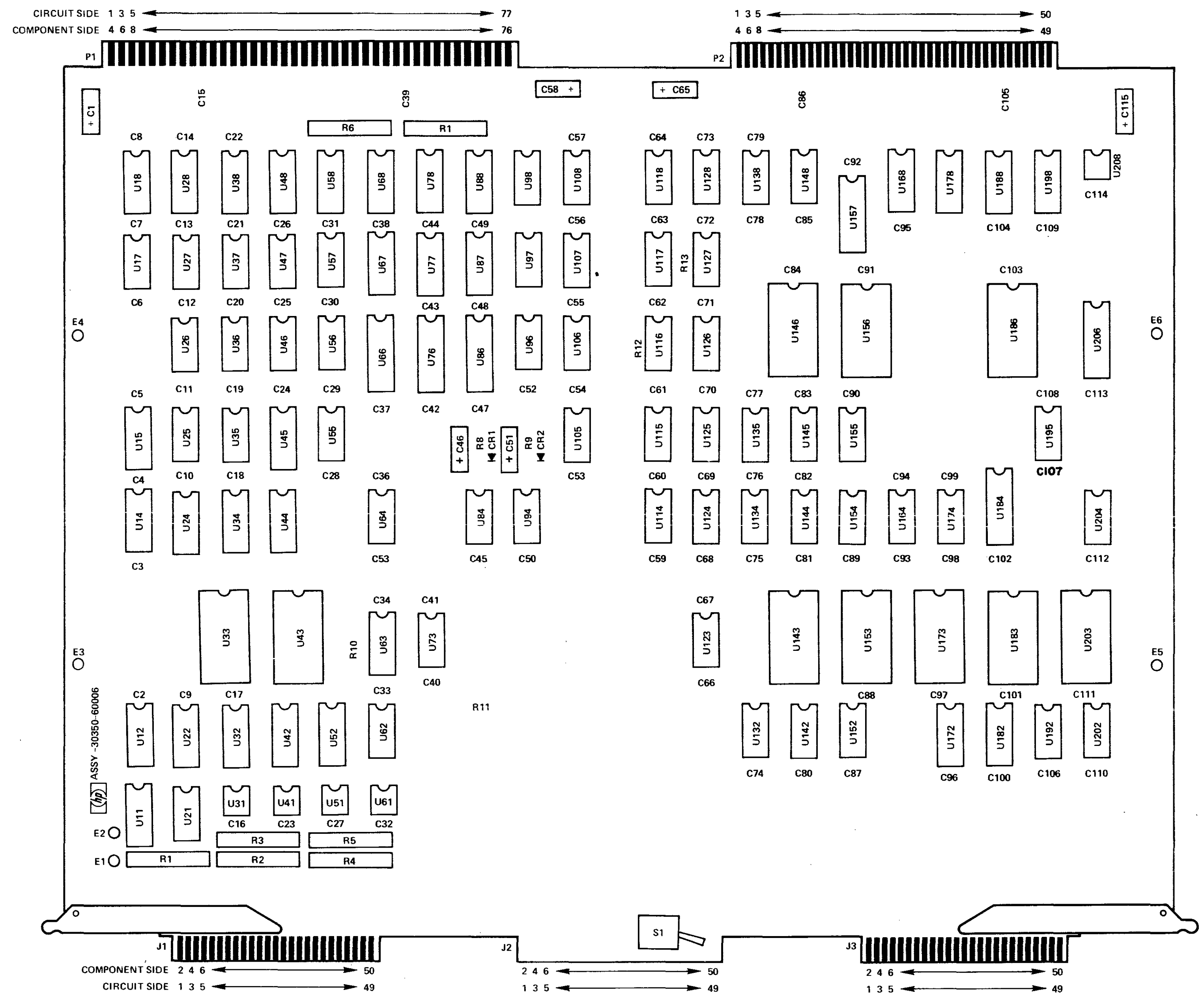
U61A

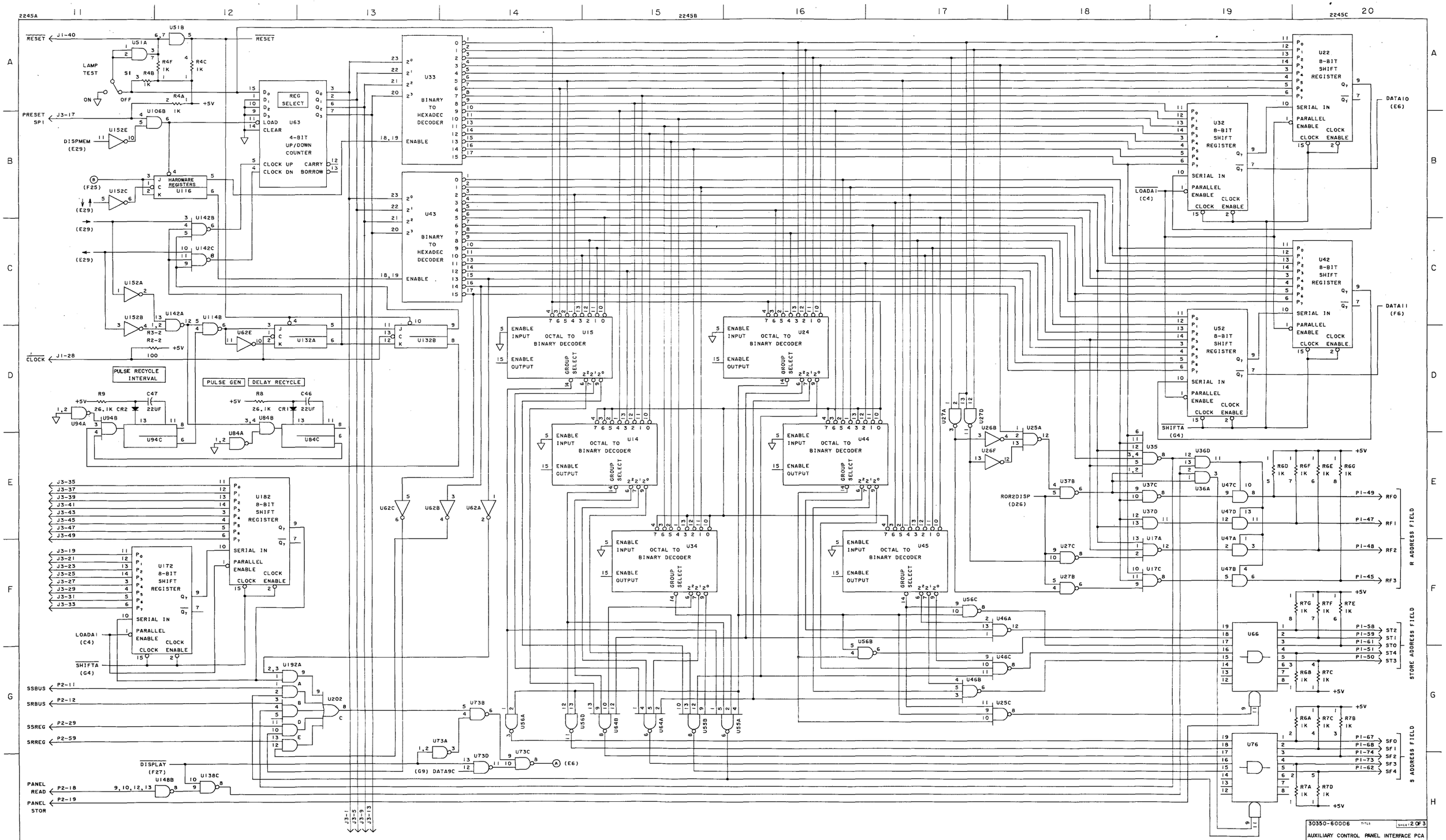
+5V R4D 1K

P1-75 SHIFTA
P1-76 LOADA1
J1-42 DATA A

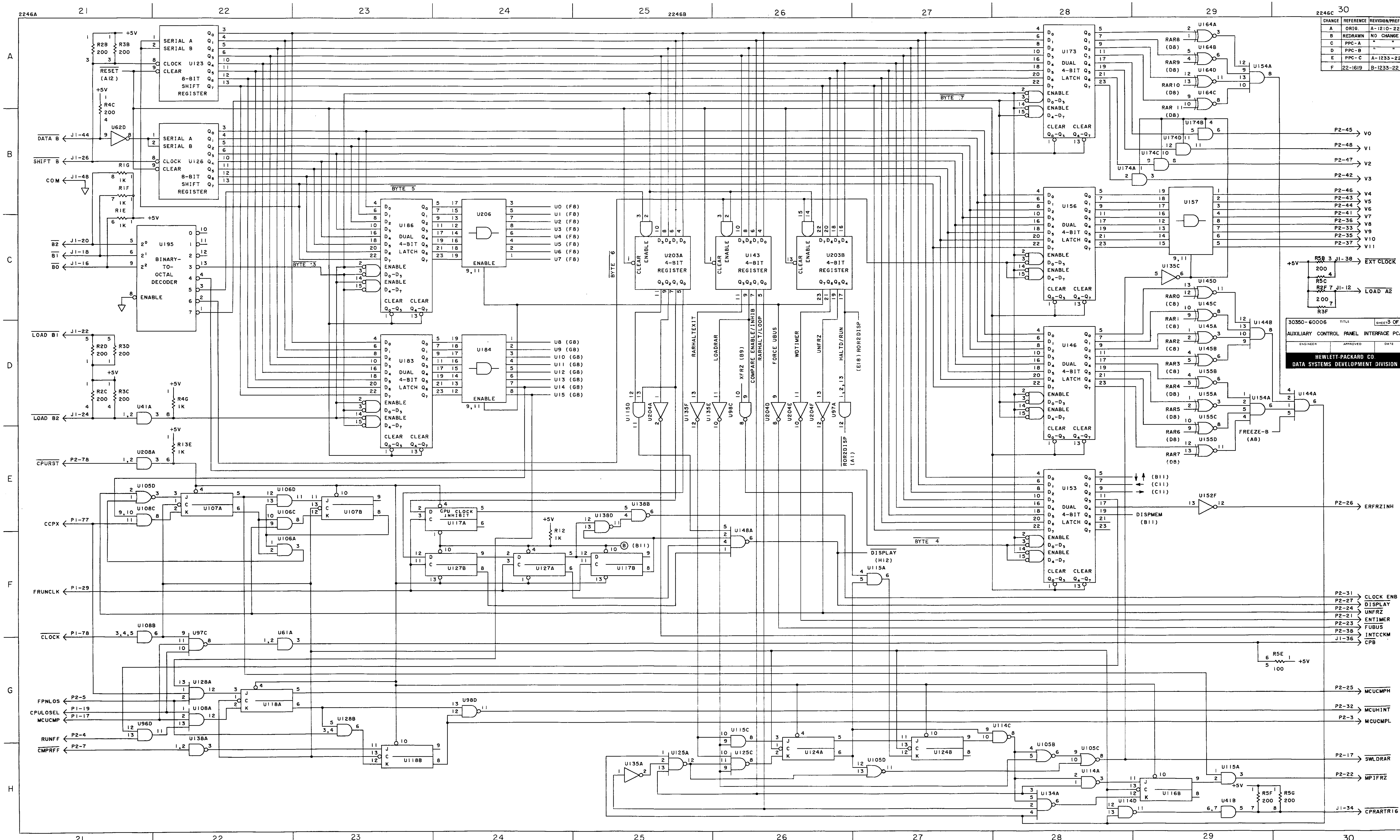
30350-60006 TITLE SHEET 1 OF 3

AUXILIARY CONTROL PANEL INTERFACE PCA


CIRCUIT SIDE 1 3 5 77
COMPONENT SIDE 4 6 8 76
1 3 5 50
4 6 8 49
P1
P2
ASSY -30350-60006
COMPONENT SIDE 2 4 6 50
CIRCUIT SIDE 1 3 5 49
2 4 6 50
1 3 5 49
2 4 6 50
1 3 5 49
J1
J2
J3
S1
E1
E2
E3
E4
E5
E6
2212-10


RESET
J1-40
U51B
U51A
LAMP TEST
S1
R4F 1K
R4B 1K
R4C 1K
ON
OFF
R4A 1K
+5V
PRESET SP1
J3-17
U106B
U152E
DISPMEM (E29)
HARDWARE REGISTERS U116
U63
REG SELECT
4-BIT UP/DOWN COUNTER
CLOCK UP
CLOCK DN
CARRY
BORROW
LOAD
CLEAR
U33
U43
BINARY TO HEXADEC DECODER
ENABLE
(F25)
U152C
(E29)
U142B
U142C
U152A
U152B
U142A
U114B
U62E
U132A
U132B
R3-2
R2-2
100
CLOCK
J1-28
PULSE RECYCLE INTERVAL
PULSE GEN
DELAY RECYCLE
R9 26.1K
C47 22UF
CR2
U94A
U94B
U94C
R8 26.1K
C46 22UF
CR1
U84A
U84B
U84C
U15
U24
U14
U44
U34
U45
ENABLE INPUT
OCTAL TO BINARY DECODER
ENABLE OUTPUT
GROUP SELECT
U62C
U62B
U62A
U182 8-BIT SHIFT REGISTER
U172 8-BIT SHIFT REGISTER
J3-35
J3-37
J3-39
J3-41
J3-43
J3-45
J3-47
J3-49
J3-19
J3-21
J3-23
J3-25
J3-27
J3-29
J3-31
J3-33
SERIAL IN
PARALLEL ENABLE
CLOCK ENABLE
LOADA1 (C4)
SHIFTA (G4)
U192A
U202
SSBUS P2-11
SRBUS P2-12
SSREG P2-29
SRREG P2-59
DISPLAY (F27)
U148B
U138C
PANEL READ P2-18
PANEL STOR P2-19
9,10,12,13
U73A
U73B
U73C
U73D
(G9) DATA9C
(A) (E6)
U56A
U56B
U56C
U56D
U64A
U64B
U55A
U55B
U46A
U46B
U46C
U25C
U27A
U27D
U26B
U26F
U25A
U27B
U27C
U37B
U35
U36D
U36A
U37C
U37D
U17A
U17C
U47C
U47D
U47A
U47B
R6D 1K
R6F 1K
R6E 1K
R6G 1K
ROR2DISP (D26)
P1-49 RF0
P1-47 RF1
P1-48 RF2
P1-45 RF3
R ADDRESS FIELD
U22 8-BIT SHIFT REGISTER
U32 8-BIT SHIFT REGISTER
U42 8-BIT SHIFT REGISTER
U52 8-BIT SHIFT REGISTER
LOADA1 (C4)
SHIFTA (G4)
DATA10 (E6)
DATA11 (F6)
U66
U76
R7G 1K
R7F 1K
R7E 1K
R68 1K
R7C 1K
R6A 1K
R7C 1K
R7B 1K
R7A 1K
R7D 1K
P1-58 ST2
P1-59 ST1
P1-61 ST0
P1-51 ST4
P1-50 ST3
P1-67 SF0
P1-68 SF1
P1-74 SF2
P1-73 SF3
P1-62 SF4
STORE ADDRESS FIELD
S ADDRESS FIELD
30350-60006
AUXILIARY CONTROL PANEL INTERFACE PCA
SHEET 2 OF 3

CIRCUIT SIDE 1 3 5 77
COMPONENT SIDE 4 6 8 76
P1
1 3 5 50
4 6 8 49
P2
+ C1
C15
C39
C58 +
+ C65
C86
C106
+ C115
R6
R1
C8 C14 C22 C57 C64 C73 C79 C92
U18 U28 U38 U48 U58 U68 U78 U88 U98 U108 U118 U128 U138 U148 U157 U168 U178 U188 U198 U208
C7 C13 C21 C26 C31 C38 C44 C49 C56 C63 C72 C78 C85 C95 C104 C109 C114
U17 U27 U37 U47 U57 U67 U77 U87 U97 U107 U117 R13 U127
C6 C12 C20 C25 C30 C43 C48 C55 C62 C71
C84 C91 C103
E4
E6
U26 U36 U46 U56 U66 U76 U86 U96 U106 R12 U116 U126 U146 U156 U186 U206
C5 C11 C19 C24 C29 C37 C42 C47 C52 C54 C61 C70 C77 C83 C90 C108 C113
U15 U25 U35 U45 U55 + C46 R8 CR1 + C51 R9 CR2 U105 U115 U125 U135 U145 U155 U195
C107
C4 C10 C18 C28 C36 C53 C60 C69 C76 C82 C94 C99
U14 U24 U34 U44 U64 U84 U94 U114 U124 U134 U144 U154 U164 U174 U184 U204
C3 C45 C50 C59 C68 C75 C81 C89 C93 C98 C102 C112
C34 C41 C67
U33 U43 R10 U63 U73 U123 U143 U153 U173 U183 U203
E3
E5
C33 C40 C66 C88 C97 C101 C111
C2 C9 C17 R11
U12 U22 U32 U42 U52 U62 U132 U142 U152 U172 U182 U192 U202
C74 C80 C87 C96 C100 C106 C110
ASSY -30350-60006
U11 U21 U31 U41 U51 U61
C16 C23 C27 C32
E2
R3 R5
E1
R1 R2 R4
J1
COMPONENT SIDE 2 4 6 50
CIRCUIT SIDE 1 3 5 49
J2
S1
2 4 6 50
1 3 5 49
J3
2 4 6 50
1 3 5 49
2212-10



2246A
2246B
2246C
U123 8-BIT SHIFT REGISTER
U126 8-BIT SHIFT REGISTER
U195 BINARY-TO-OCTAL DECODER
U186 DUAL 4-BIT LATCH
U183 DUAL 4-BIT LATCH
U206
U184
U203A 4-BIT REGISTER
U143 4-BIT REGISTER
U203B 4-BIT REGISTER
U173 DUAL 4-BIT LATCH
U156 DUAL 4-BIT LATCH
U146 DUAL 4-BIT LATCH
U153 DUAL 4-BIT LATCH
U157
CPU CLOCK INHIBIT U117A
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
DATA B
SHIFT B
COM
B2
B1
B0
LOAD B1
LOAD B2
CPURST
CCPX
FRUNCLK
CLOCK
FPNLOS
CPULOSEL
MCUCMP
RUNFF
CMPRFF
RESET (A12)
RARHALTEXIT
LOADRAR
XFRZ (B9)
COMPARE ENABLE/INHIB
RARHALT/LOOP
FORCE UBUS
WDTIMER
UNFRZ
HALTD/RUN
(E18) ROR2DISP
ROR2DISP (A1)
DISPLAY (H12)
DISPMEM (B11)
FREEZE-B (A8)
U0 (F8)
U1 (F8)
U2 (F8)
U3 (F8)
U4 (F8)
U5 (F8)
U6 (F8)
U7 (F8)
U8 (G8)
U9 (G8)
U10 (G8)
U11 (G8)
U12 (G8)
U13 (G8)
U14 (G8)
U15 (G8)
V0
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
EXT CLOCK
LOAD A2
ERFRZINH
CLOCK ENB
DISPLAY
UNFRZ
ENTIMER
FUBUS
INTCCKM
CPB
MCUCMPH
MCUHINT
MCUCMPL
SWLDRAR
MP1FRZ
CPRARTRIG

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	" "
D	PPC-B	" "
E	PPC-C	A-1233-22
F	22-1619	B-1233-22

30350-60006 TITLE SHEET 3 OF 3

AUXILIARY CONTROL PANEL INTERFACE PCA

ENGINEER | APPROVED | DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

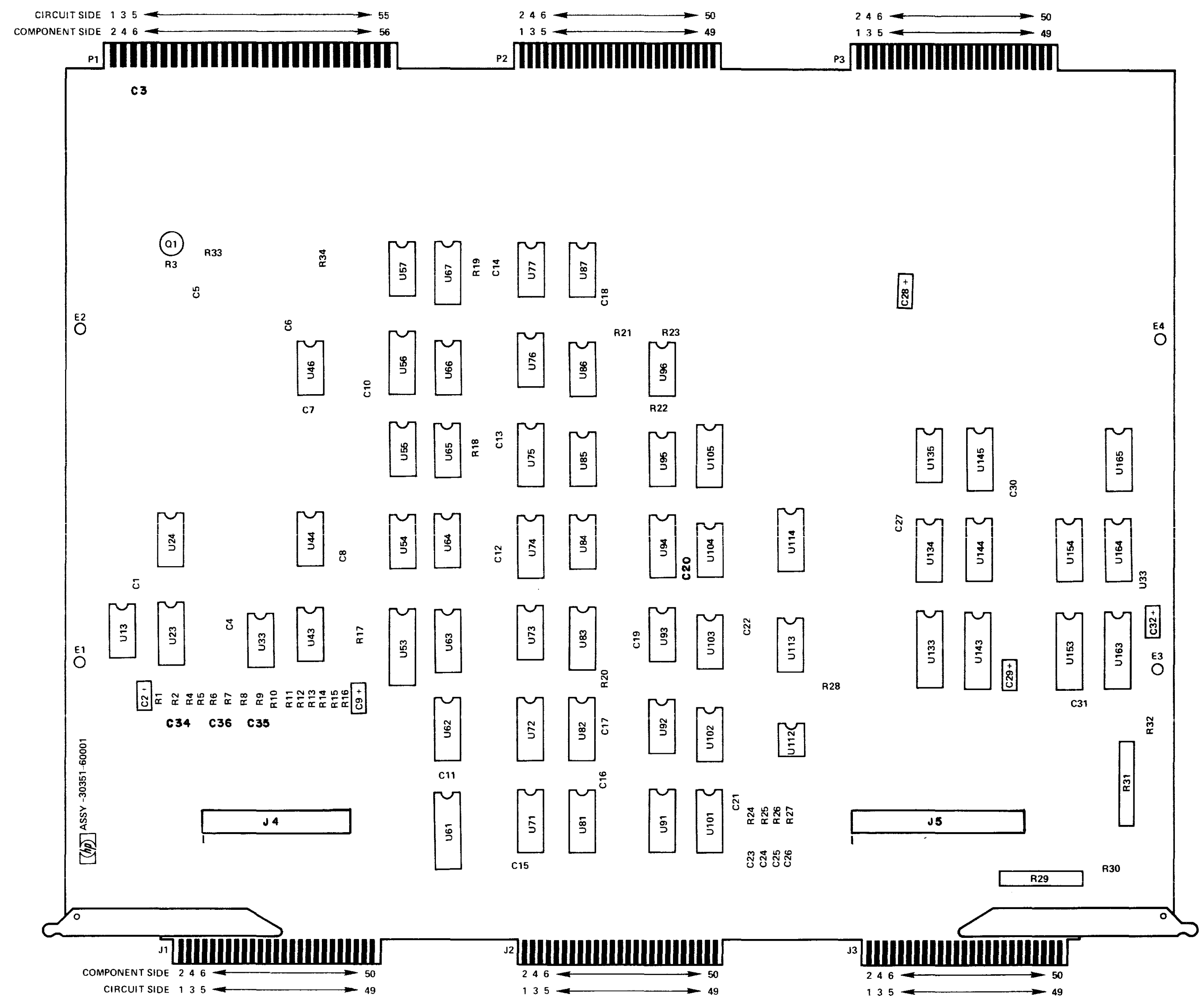
DETAILED DIAGRAM SET

DD-803

INPUT / OUTPUT MAINTENANCE PANEL INTERFACE PCA

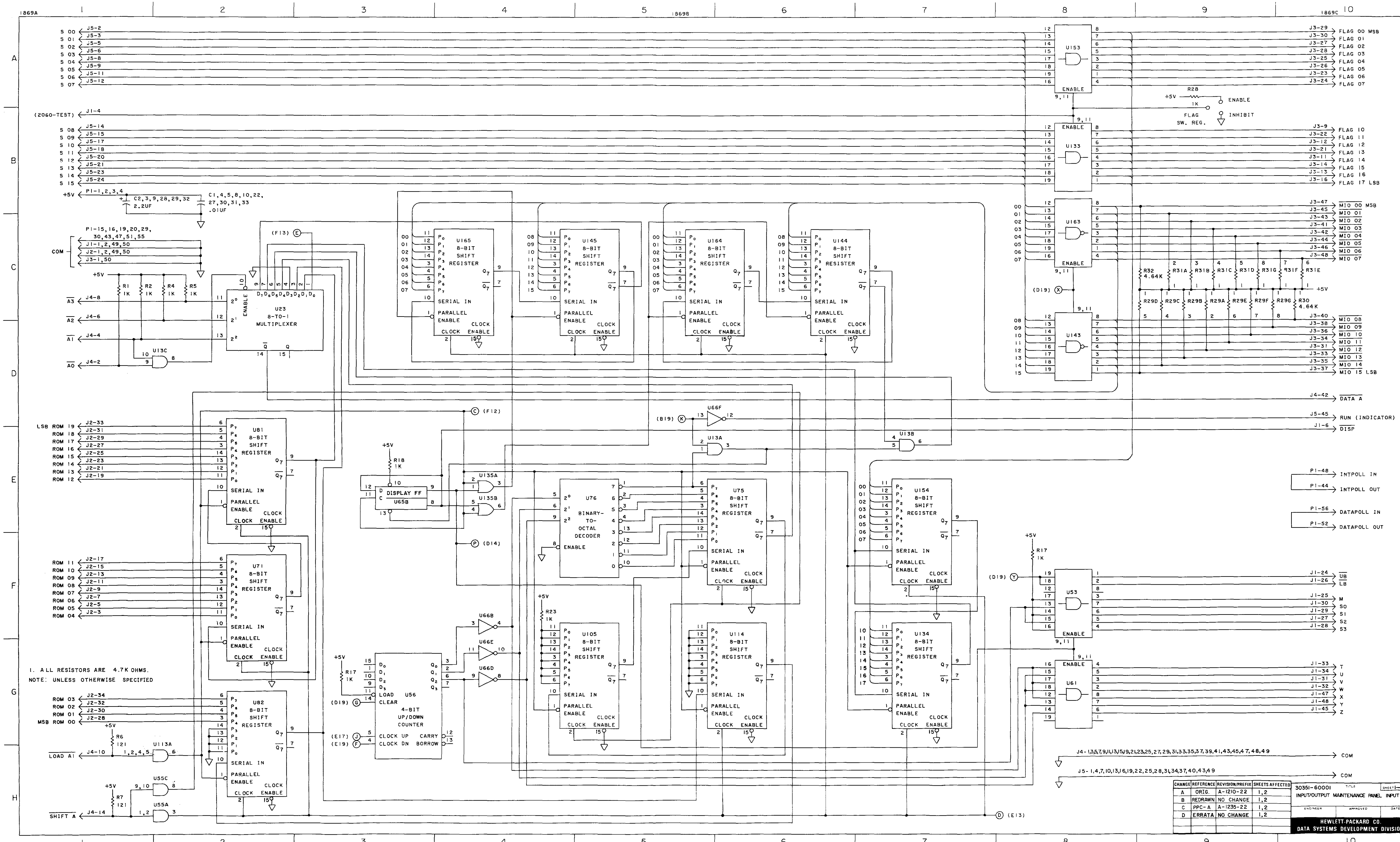
30351-60001

SERIES 1235

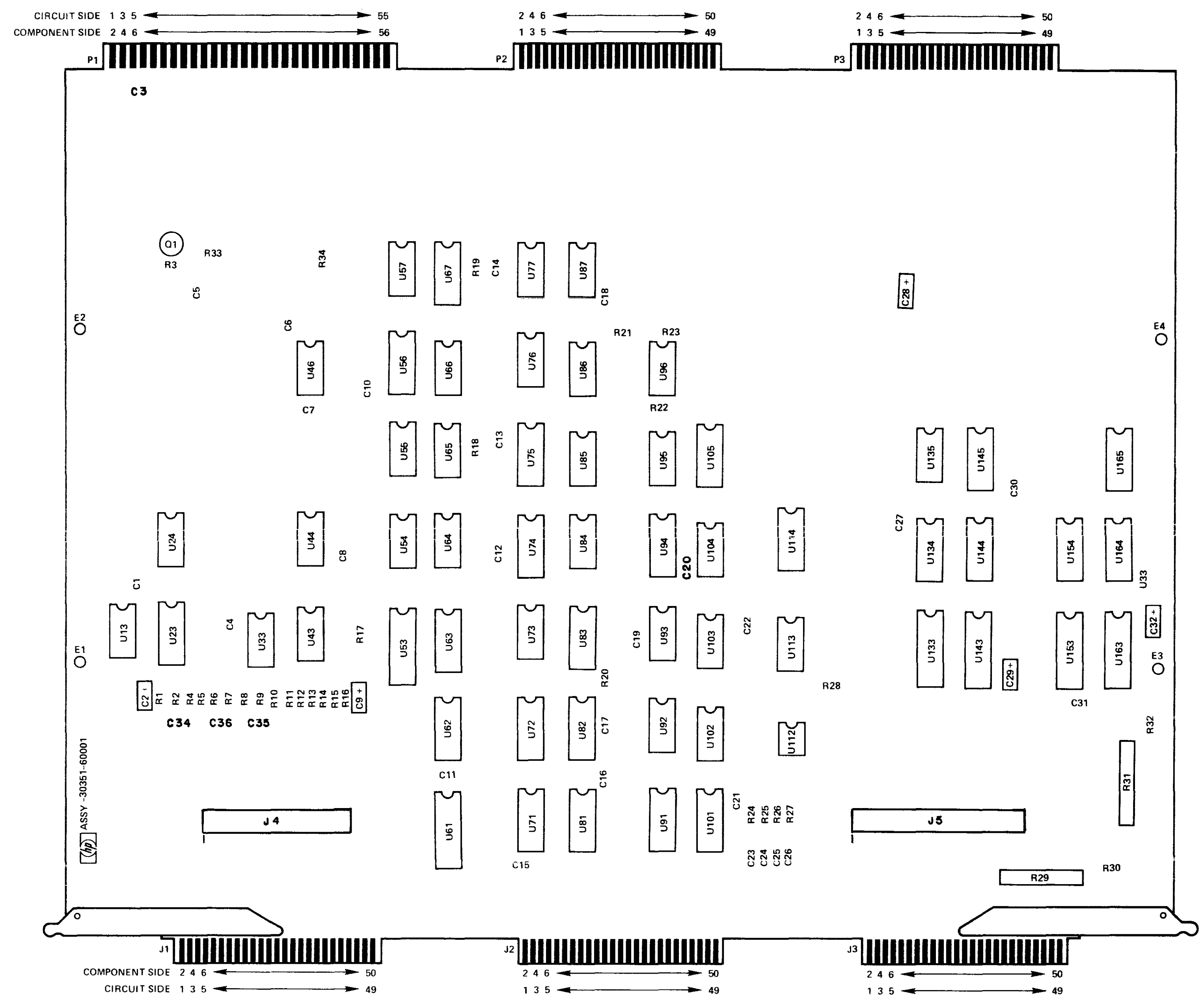


CIRCUIT SIDE 1 3 5 55
COMPONENT SIDE 2 4 6 56
2 4 6 50
1 3 5 49
P1
P2
P3
J1
J2
J3
J4
J5
COMPONENT SIDE 2 4 6 50
CIRCUIT SIDE 1 3 5 49
ASSY -30351-60001

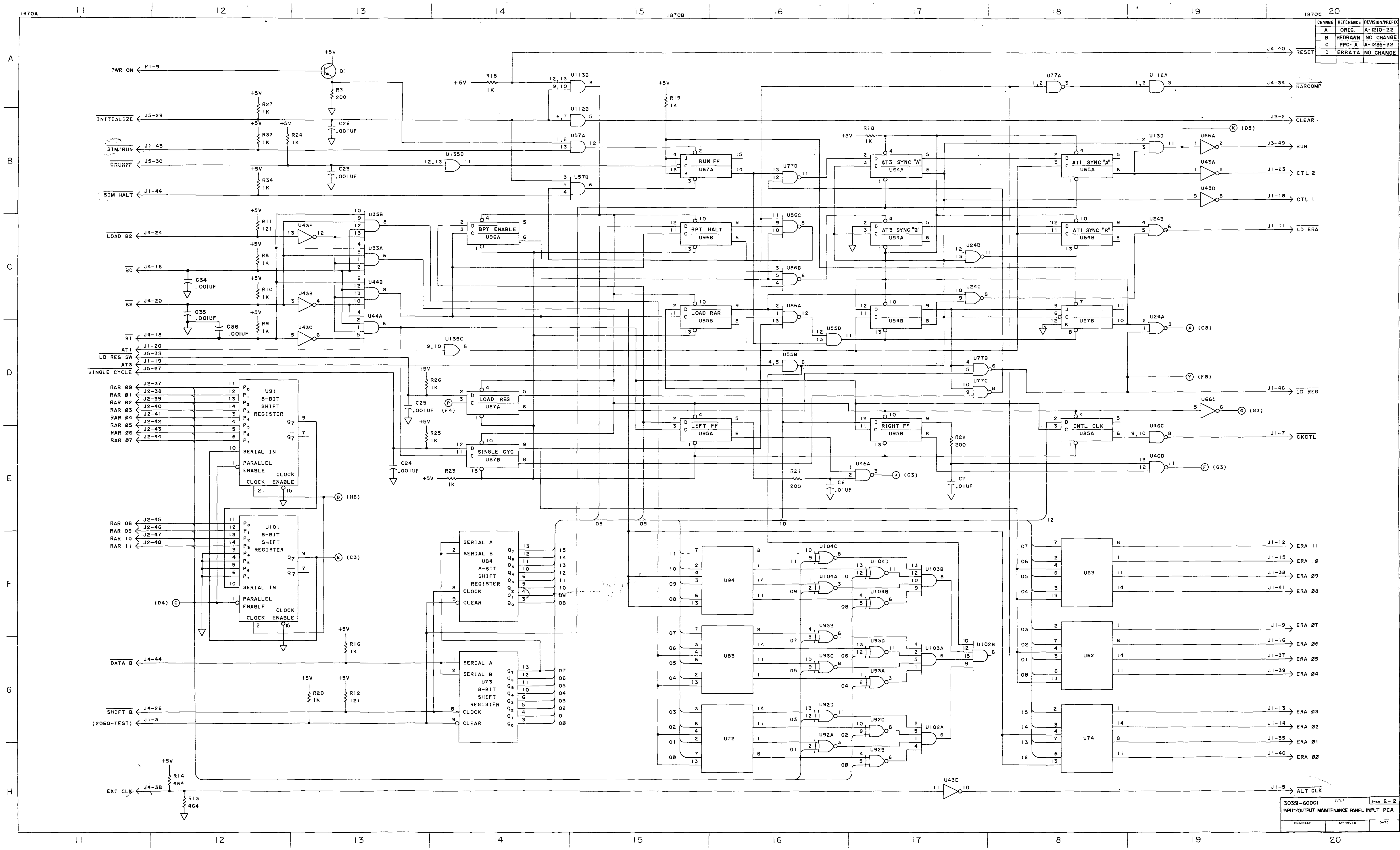
2212 13



1. ALL RESISTORS ARE 4.7K OHMS.
NOTE: UNLESS OTHERWISE SPECIFIED
U23 8-TO-1 MULTIPLEXER
U165 8-BIT SHIFT REGISTER
U145 8-BIT SHIFT REGISTER
U164 8-BIT SHIFT REGISTER
U144 8-BIT SHIFT REGISTER
U81 8-BIT SHIFT REGISTER
U71 8-BIT SHIFT REGISTER
U82 8-BIT SHIFT REGISTER
DISPLAY FF U65B
U76 BINARY-TO-OCTAL DECODER
U75 8-BIT SHIFT REGISTER
U154 8-BIT SHIFT REGISTER
U105 8-BIT SHIFT REGISTER
U114 8-BIT SHIFT REGISTER
U134 8-BIT SHIFT REGISTER
U56 4-BIT UP/DOWN COUNTER
FLAG SW. REG.
ENABLE
INHIBIT
DATA A
RUN (INDICATOR)
DISP
INTPOLL IN
INTPOLL OUT
DATAPOLL IN
DATAPOLL OUT
LOAD A1
SHIFT A
J4-1,3,5,7,9,11,13,15,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,48,49 COM
J5-1,4,7,10,13,16,19,22,25,28,31,34,37,40,43,49 COM
CHANGE | REFERENCE | REVISION/PREFIX | SHEETS AFFECTED
A | ORIG. | A-1210-22 | 1,2
B | REDRAWN | NO CHANGE | 1,2
C | PPC-A | A-1235-22 | 1,2
D | ERRATA | NO CHANGE | 1,2
30351-60001
INPUT/OUTPUT MAINTENANCE PANEL INPUT PCA
SHEET 1 OF 2
HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION


CIRCUIT SIDE 1 3 5 55
COMPONENT SIDE 2 4 6 56
2 4 6 50
1 3 5 49
P1
P2
P3
C3
J4
J5
J1
J2
J3
COMPONENT SIDE 2 4 6 50
CIRCUIT SIDE 1 3 5 49
ASSY -30351-60001

2212 13



CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-A	A-1235-22
D	ERRATA	NO CHANGE

30351-60001
INPUT/OUTPUT MAINTENANCE PANEL INPUT PCA
SHEET 2-2
ENGINEER | APPROVED | DATE

DETAILED DIAGRAM SET

DD-804

HARDWARE MAINTENANCE PANEL INPUT PCB

30352-60001

SERIES 1210

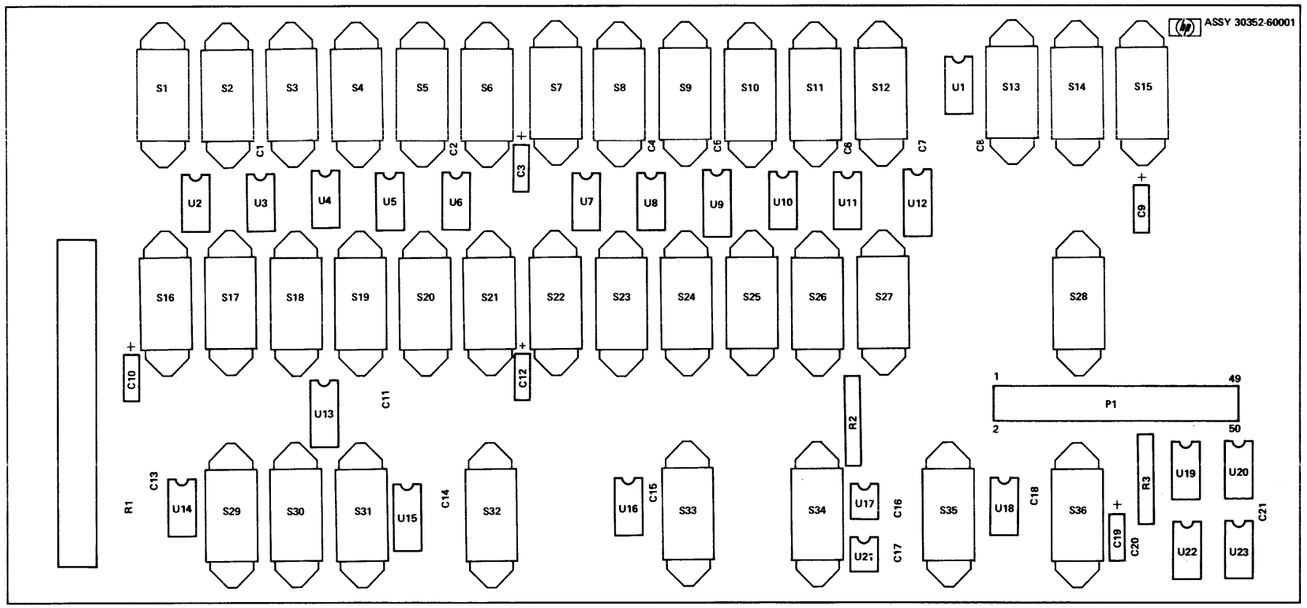
SIGNAL INDEX

P1

PIN	SIGNAL
1	COM
2	
3	COM
4	
5	COM
6	
7	COM
8	
9	COM
10	
11	COM
12	
13	COM
14	
15	COM
16	$\overline{B0}$
17	COM
18	$\overline{B1}$
19	COM
20	$\overline{B2}$
21	COM
22	$\overline{LOAD\ B1}$
23	COM
24	
25	COM
26	$\overline{SHIFT\ B}$
27	COM
28	
29	COM
30	
31	COM
32	INHIBIT H
33	COM
34	$\overline{RAR\ COMP}$
35	COM
36	$\overline{B\ COMP}$
37	COM
38	$\overline{EXT\ CLOCK}$
39	COM
40	
41	COM
42	
43	COM
44	$\overline{DATA\ B}$
45	COM
46	
47	COM
48	TEST MODE
49	COM
50	COM

I.C. INDEX

U	1820-	U	1820-
1-3	0307	16	0307
4	0262	17	0535
5-8	0307	18	0307
9	0262	19	0621
10,11	0307	20	0373
12,13	0262	21	0535
14	0307	22	0424
15	0262	23	0373



2212-30

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	B-1210-22
D	ERRATA	NO CHANGE

TEST MODE ← P1-48

RAR BREAK POINT REGISTER SWITCHES

RAR LOAD REGISTER SWITCHES

RAR LOAD REGISTER SWITCHES

RAR COMPARE

RAR SWITCH REGISTER

U4 8-BIT SHIFT REGISTER

U9 8-BIT SHIFT REGISTER

U13 8-BIT SHIFT REGISTER

U12 8-BIT SHIFT REGISTER

U15 8-BIT SHIFT REGISTER

SERIAL IN

PARALLEL ENABLE

CLOCK

CLOCK ENABLE

LOAD (F7)

SHIFT B (F7)

RAR HALT/JUMP S14

COPARE ENABLE S13

LOAD RAR S28

HALT EXIT S15

HALT D RUN S33

UNFR2 S35

INHIBIT WD TIMER S34

FORCE U-BUS S36

EXECUTE SINGLE CYCLE S31

SINGLE CYCLE MODE S30

EXT/INT CLOCK S29

SINGLE CYCLE REGISTER DISPLAY S32

REAR PANEL

TB-5 TB-6 RAR COMPARE J9

TB-3 TB-4 B COMPARE J8

TB-7 TB-8 EXT CLOCK J7

TB-1 TB-2 LOGIC PROBE J10

R1 50

R2A 1K

R2C 1K

R2D 1K

R2E 1K

R2F 1K

R2G 1K

R3A 1K

R3B 1K

R3C 1K

R3D 1K

R3E 1K

R3F 1K

R3G 1K

+5V

U22D U21B U17B U21A U17A U22C U19A U22B U22A U23A U23B U20B U20A U22E U22F

LOAD (B3)(E3) (B5)(E5)(B7)

SHIFT B (B3)(E3) (B5)(E5)(B7)

P1-38 EXT CLOCK

P1-44 DATA B

DATA 0

DATA 1

RAR COMP P1-34

B COMP P1-36

LOAD BI P1-22

SHIFT B P1-26

INHIBIT H P1-32

B0 P1-16

B2 P1-20

B1 P1-18

COM ← P1-ALL ODD PINS, 50

+5V

C3, C9, C10, C12, C19 33

C1, C2, C4-8, C11, C13-18, C20, C21 .01

COM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1K
2. ALL CAPACITANCE IS IN MICROFARADS
3. TWISTED PAIR.

30352-60001	TITLE	SHEET 1 OF 1
HARDWARE MAINTENANCE PANEL INPUT PCB		
ENGINEER	APPROVED	DATE
HEWLETT-PACKARD CO. DATA SYSTEMS DEVELOPMENT DIVISION		

DETAILED DIAGRAM SET

DD-805

HARDWARE MAINTENANCE PANEL DISPLAY PCB

30352-60002

SERIES 1210

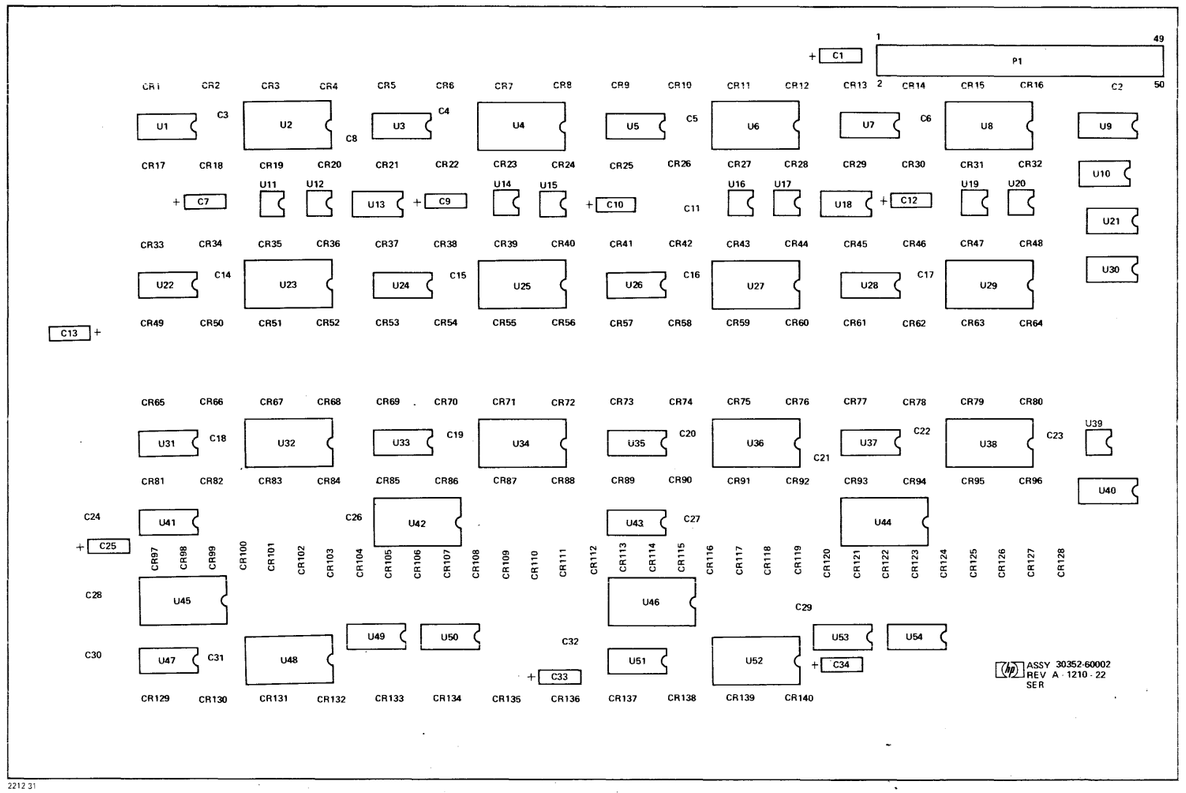
SIGNAL INDEX

P1

PIN	SIGNAL
1	
2	$\overline{A0}$
3	
4	$\overline{A1}$
5	
6	$\overline{A2}$
7	
8	$\overline{A3}$
9	
10	
11	
12	$\overline{LOAD\ A2}$
13	
14	$\overline{SHIFT\ A}$
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	
36	
37	
38	
39	
40	$\overline{RESET}$
41	
42	$\overline{DATA\ A}$
43	
44	
45	
46	
47	
48	
49	
50	

I.C. INDEX

U	1810-	U	1810-	U	1820-	U	1820-
1	0124	35	0124	2	0742	29	0742
3	0124	37	0124	4	0742	30	0608
5	0124	40	0037	6	0742	32	0742
7	0124	41	0124	8	0742	34	0742
9	0037	43	0124	10	0373	36	0742
22	0124	47	0124	11,12	0535	38	0742
24	0124	49	0037	13	0294	39	0535
26	0124	50,51	0124	14-17	0535	42	0742
28	0124	53	0037	18	0294	44-46	0742
31	0124	54	0124	19,20	0535	48	0742
33	0124			21	0373	52	0742
				23	0742		
				25	0742		
				27	0742		



2212 31

2248A 2248B 2248C

30352-60002 TITLE SHEET 1

HARDWARE MAINTENANCE PANEL DISPLAY PCB

ENGINEER | APPROVED | DATE

HEWLETT-PACKARD CO.
DATA SYSTEMS DEVELOPMENT DIVISION

ROM OUTPUT REGISTOR

ROM ADDRESS REGISTER

CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG.	A-1210-22
B	REDRAWN	NO CHANGE
C	PPC-D	B-1210-22
D	ERRATA	NO CHANGE

1. ALL RESISTORS ARE 200 OHM

NOTES: UNLESS OTHERWISE INDICATED