HEWLETT **hp** PACKARD

OPERATING AND SERVICE MANUAL

12597A-002

TAPE READER INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assembly
12597-6001, Rev 832

Note

This manual should be retained with the applicable
computer system documentation.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2.   This manual provides general information, installation instructions, programming instructions, theory of operation, maintenance information, and replaceable parts information for the Hewlett-Packard (HP) 12597A-002 Tape Reader Interface Kit (see figure 1-1).

1-3. DESCRIPTION.

1-4.   GENERAL.

1-5.   The HP 12597A-002 Tape Reader Interface Kit supplies the interfacing requirements for the addition of an HP 2748A Tape Reader or an HP 2758A Tape Reader-Reroller to the user's computer system.

1-6.   INTERFACE KIT CONTENTS.

1-7.   The HP 12597A-002 Tape Reader Interface Kit consists of the following:

    a. Tape reader interface card (part no. 12597-6001).

    b. Interface cable (part no. 12597-6004).

    c. Test connector, 24-pin (part no. 1251-0332).

    d. Operating and service manual (part no. 12597-90022).

1-8. IDENTIFICATION

1-9.   Hewlett-Packard uses five digits and a letter (00000A) to identify standard interface kits and three digits (-000) to identify options to standard interface kits. If the designation of the kit received does not agree with the designation on the title page of this manual, there are differences between the kit received and the kit described in this manual. These differences are explained in manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-10.   In addition to a part number, each plug-in printed-circuit card is identified by a letter, a date code, and a division code (e.g., A-921-22). These are marked on the card beneath the part number. The letter identifies the version of the etched circuit on the card. The date code (three or four digits) refers to the electrical characteristics of the board with components mounted. The division code (one or two digits) identifies the Hewlett-Packard division which manufactured the card. If the date code on a printed-circuit card does not agree with the date code shown on the title page of this manual, the card differs from the one described in this manual. These differences are explained in a manual supplement available at HP Sales and Service Offices.

1-11.   The interface cable is identified by its part number, marked on one of the plugs attached to the cable.
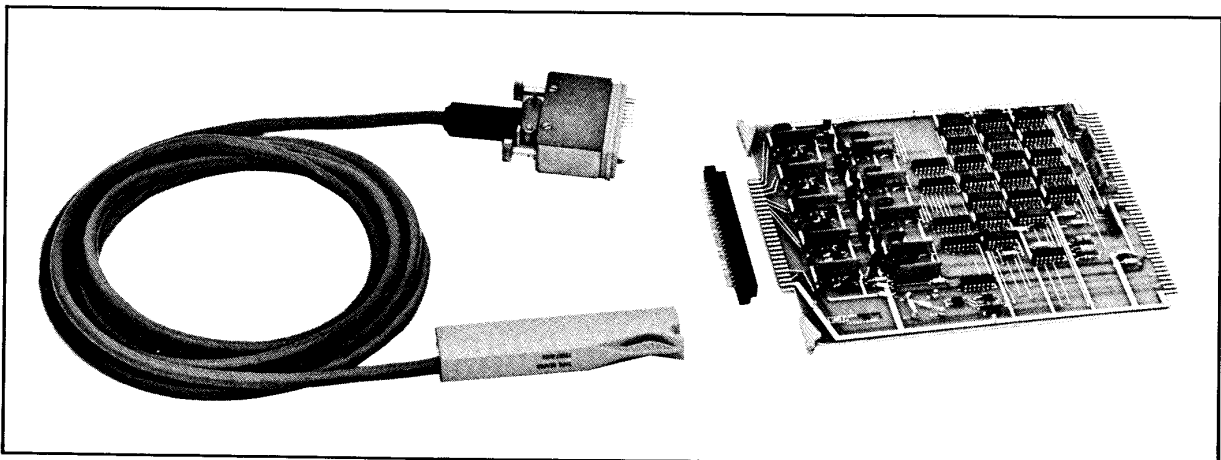
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Figure 1-1. HP 12597A-002 Tape Reader Interface Kit

1-12. The manual and manual supplements are identified by title, part number, and publication date, marked on the title page of the document. Supplements, if required, are bound to the back of the manual.

1-13. SPECIFICATIONS.

1-14. Table 1-1 lists the specifications for the HP 12597A-002 Tape Reader Interface Kit.

Table 1-1. Tape Reader Interface Kit Specifications

CHARACTERISTICS	SPECIFICATIONS
Output Levels	
"1" state	0 to +0.5V, 12 mA sink max.
"0" state	+12V, 10K source
Input Levels	
"1" state	0 to +0.5V, 12 mA sink max.
"0" state	+8V
Computer Power Supply	
Current Requirements	
+12V	0.05A
-12V	0.02A
-2V	0.05A
+4.5V	0.75A
Interface Card	
Dimensions	
Width	7-3/4 inches (196,8 mm)
Height	8-11/16 inches (220,7 mm)
Interface Kit Weight	
Net Weight	18 oz (675 gm)
Shipping Weight	4 lb (1,8 kg)

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2.   This section provides information on unpacking and inspection, reshipment, preparation for installation, and installation of the tape reader interface kit.

2-3. UNPACKING AND INSPECTION.

2-4.   If the tape reader interface kit is received separated from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5.   Inspect each component of the kit as the parts are unpacked. Look for such evidence of damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the kit is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier.

2-6. RESHIPMENT.

2-7.   If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-8.   Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest Hewlett-Packard Sales and Service Office.

2-9.   If standard factory packing material is not used, wrap the item in air cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorn, N.J.) or equivalent and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

2-10. PREPARATION FOR INSTALLATION.

2-11.   CURRENT REQUIREMENTS.

2-12.   The interface card in this kit obtains its operating currents from the computer power supply. Before installing this interface card, determine the sum of the current requirements of this card in combination with any other interface or accessory cards already installed in the computer. Volume Three of the computer system documentation describes the procedure for calculating the total current requirements. If the total current requirements exceed the limitations of the computer power supply, an HP power supply extender unit or I/O extender unit must be used. See table 1-1 for the current requirements of the tape reader interface card.

2-13.   INTERFACE CARD JUMPERS.

2-14.   There are several jumper wires on the tape reader interface card. These jumpers are used to adapt the card for use with I/O devices other than the tape reader. Before installation of the interface card, ensure that the jumpers are positioned as described in table 2-1 (see figure 5-2 for physical location of the jumpers).

Table 2-1. Interface Card Jumper Positions

JUMPER	POSITION
W1	A
W2	A
W3	Connected
W4	Connected
W5	Connected
W6	Connected
W7	Connected
W8	Disconnected
W9	Disconnected

2-15. INSTALLATION.

2-16.   To install the tape reader interface kit, proceed as follows:

   a.   Turn computer and tape reader power off.

   b.   Insert the interface card in the computer I/O card slot corresponding to the desired select code (address).

   c.   Turn on power to the computer and perform diagnostic test procedure (part number 12554-90023 for 2114, 2115, and 2116 Computers, or part number 12554-90026 for 2100 Computers), in the Manual of Diagnostics, to verify proper operation of the tape reader interface card.

   d.   Turn computer power off.

   e.   Connect the 48-pin connector end of the interface cable to the interface card.

   f.   Connect the other end of the interconnecting cable to the tape reader.

   g.   Apply power to the computer and the tape reader and perform diagnostic test procedure (part number 02737-90191 for 2114, 2115, and 2116 Computers, or part number 5951-1363 for 2100 Computers) as described in the Manual of Diagnostics, to verify proper operation of the interface card in conjunction with the tape reader.

SECTION III

PROGRAMMING

3-1.   INTRODUCTION.

3-2.   This section provides programming information for the 12597A-002 Tape Reader Interface Kit.

3-3.   GENERAL.

3-4.   The tape reader interface card provides command logic to start the tape reader and flag logic to signal the computer when the tape reader has data ready for transfer. An input storage register provides buffer storage for transfer of eight bits of data from the tape reader to the computer. The following paragraphs provide information required to program the operation of the command, flag, and input register logic on the tape reader interface card.

3-5.   I/O ADDRESSING.

3-6.   Through the use of the I/O extender options, some HP computers are capable of operating up to 56 I/O devices. To provide orderly I/O operations, each I/O slot is assigned a two digit octal address called a select code. All program instructions calling for action by the tape reader interface card must include the interface card's select code.

3-7.   SAMPLE PROGRAM.

3-8.   Table 3-1 provides a sample program showing the use of the tape reader interface card to operate an HP 2748A or 2758A Tape Reader. The sample is an actual program listing prepared on an HP computer system using the HP Assembler software package.

3-9.   The program will cause 100 characters to be read from a punched tape and stored in 100 consecutive memory locations. To supply the I/O addressing requirements, the tape reader interface card has been arbitrarily assigned a select code of 13 octal.

3-10.   The sample program does not use the computer interrupt system. If the interrupt system has been previously enabled, a CLF 00 instruction must be included at the start of the program to turn off the interrupt system.

Table 3-1. Sample Program

```
    PAGE 0002 #01


    0001                    ASMB,A,B,L,T
    0002*
    0003*   THIS IS A SAMPLE PROGRAM DEMONSTRATING THE USE OF THE
    0004*   HP 12597A-002 INTERFACE TO CONTROL THE OPERATION OF
    0005*   AN HP 2748A OR 2758A TAPE READER.  THIS PROGRAM WILL
    0006*   READ 100, 8-BIT CHARACTERS USING THE TAPE READER AND
    0007*   STORE THEM IN 100 CONSECUTIVE CORE LOCATIONS.  SELECT-
    0008*   CODE ADDRESS OF THE TAPE READER IS 13 OCTAL.
    0009*
    0010  00100              ORG 100B     PROGRAM STARTS AT ADDRESS 100 OCTAL.
    0011*
    0012  00100 060270  START LDA CNT     INITIALIZE A COUNT-BY-100 COUNTER
    0013  00101 070267        STA CNTR      AND STORE IN LOCATION CNTR.
    0014  00102 060121        LDA ITBL    ASSIGN BEGINNING ADDRESS OF STORAGE
    0015  00103 070266        STA PNTR      BLOCK TO ADDRESS POINTER "PNTR".
    0016*
    0017  00104 014113  GO    JSB READ    JUMP TO SUBROUTINE LABLED READ.
    0018*
    0019  00105 170266        STA PNTR,I  STORE NEW CHARACTER IN LOCATION
    0020*                                 SPECIFIED BY POINTER.
    0021  00106 034266        ISZ PNTR    INCREMENT POINTER FOR NEXT STORAGE.
    0022  00107 034267        ISZ CNTR    INCREMENT COUNTER. 100 OPERATIONS?
    0023  00110 024104        JMP GO      NO. READ ANOTHER CHARACTER.
    0024  00111 102077        HLT 77B     YES. HALT PROGRAM.
    0025  00112 024100        JMP START   TO RERUN PROGRAM. PRESS "RUN".
    0026*
    0027*   **SUBROUTINE**
    0028*    THIS PORTION OF THE PROGRAM INSTRUCTS THE INTERFACE
    0029*    TO OPERATE THE TAPE READER.
    0030*
    0031  00113 000000  READ  NOP         ENTRY POINT.
    0032  00114 103713        STC PTR,C   START TAPE READER.
    0033  00115 102313        SFS PTR     HAS READER COMPLETED OPERATION?
    0034  00116 024115        JMP *-1     NO. WAIT.
    0035  00117 102513        LIA PTR     YES. PUT CHARACTER IN "A" REGISTER.
    0036  00120 124113        JMP READ,I  RETURN TO MAIN PROGRAM WITH NEW
    0037*                                 CHARACTER.
    0038*
    0039*
    0040*   CONSTANT AND STORAGE INFORMATION.
    0041*
    0042  00121 000122  ITBL  DEF TBL
    0043  00122 000000  TBL   BSS 100
    0044  00266 000000  PNTR  BSS 1
    0045  00267 000000  CNTR  BSS 1
    0046  00270 177634  CNT   DEC -100
    0047  00013         PTR   EQU 13B
    0048*
    0049                      END START
    **  NO ERRORS*
```

SECTION IV

THEORY OF OPERATION

4-1.   INTRODUCTION.

4-2.   This section provides the theory of operation for the 12597-6001 Tape Reader Interface Card.

4-3.   FUNCTIONAL THEORY OF OPERATION.

4-4.   Figure 4-1 is a flow chart showing the functional theory of operation for the tape reader interface card. The programmed instructions shown on the flowchart are the same as those used in the subroutine portion of the sample program (table 3-1) in section III of this manual.

4-5.   The first programmed instruction (STC,C) sets the Control and Command FFs and clears the flag buffer and Flag FFs. The set side of the Command FF provides a Read signal which starts the operation of the tape reader. When the tape reader has completed its operation, it supplies a Feed Hole signal which sets the Flag Buffer FF, clears the Command FF, and loads the eight bits of data from the tape reader into the interface card's input storage register. The next ENF (T2) signal after the Flag Buffer FF sets will set the Flag FF.

4-6.   Since the tape reader operates at a speed considerably slower than the computer, some means must be provided to signal the computer when the tape reader has completed its operation. Figure 4-1 shows the next instruction to be an SFS instruction. If the Flag FF is not set (tape reader is still busy), the computer executes a JMP *-1 instruction and again executes the SFS instruction. The computer will stay in this wait-for-flag loop until the Flag FF is finally set.

4-7.   When the Flag FF sets, the interface card generates an SKF signal which causes the computer to skip the JMP *-1 instruction and proceed with the next instruction (LIA). The interface card then transfers the 8-bit data word to the computer's A-register.

4-8.   DETAILED THEORY OF OPERATION.

4-9.   GENERAL.

4-10.   Diagrams that support the detailed theory of operation of the tape reader interface include the timing diagram (figure 4-4) in this section and the logic diagram (figure 5-2) in section V of this manual.

4-11.   For an index of signals to and from the 86-pin edge of the interface card, see volume two of the computer system documentation. For interface cable signals, see table 5-2 in section V of this manual.

4-12.   Logic levels between the computer and the interface card and logic levels internal to the interface card are positive-true. The term "true" refers to a signal level of approximately +3.5 volts and "false" refers to a level of approximately ground. These signal levels vary depending on the integrated circuit package involved. Detailed signal level information for the various integrated circuit packages is provided in figure 5-1.

4-13.   Signals to and from the tape reader are ground-true and are detailed in table 1-1.

4-14.   POWER-ON LOGIC.

4-15.   When power is initially applied to the computer or the computer's PRESET switch is pressed, the computer supplies a POPIO and a CRS signal to the interface card. The POPIO signal sets the Flag Buffer FF; the CRS signal clears the Control and Command FFs. The Control FF, in the clear state, disables the interrupt circuitry on the interface card. A cleared Command FF ensures that the tape reader will be receiving a false Read signal. At time T2 the computer generates an ENF signal which is gated with the set-side of the Flag Buffer FF to set the Flag FF. The ENF signal also ensures that the IRQ FF is in the clear state.

4-16.   The initial operating conditions of the tape reader interface card after power on are: Flag Buffer and Flag FFs set and Control, Command, and IRQ FFs cleared.

4-17.   COMMAND LOGIC.

4-18.   The first programmed instruction required for a tape reading operation is an STC xx,C (combined Set Control and Clear Flag) instruction with the select code (xx) of the tape reader interface card. As a result of this instruction, the interface card receives true IOG, SCM, SCL, STC, and CLF signals which set the Control and Command FFs and clear the Flag and Flag Buffer FFs.

4-19.   The set side of the Control FF provides an enable for the interface card interrupt circuitry. Interrupt operation is described in detail in paragraph 4-25. The set side of the Command FF is level amplified and sent to the tape reader as a Read signal. The tape reader reads one 8-bit word and puts the word on the eight data signal lines from the reader to the interface card. In the clear state, the Flag and Flag Buffer FFs provide the initial operating conditions for the following discussion of the interface card flag logic.

4-20.   FLAG LOGIC.

4-21.   When the tape reader completes a read operation, it supplies a Feed Hole signal (so named because it is generated by the feed holes in the tape). The Feed Hole

4-1

signal is converted to a 300-nanosecond pulse which clears the Command FF, sets the Flag Buffer FF, and latches the 8-bit word from the tape reader into the input storage register.

4-22.   The timing of the flag logic at this point is dependent on the timing of the tape reader and is not related to the computer timing. An ENF signal is supplied by the computer every machine cycle at time T2. This signal is gated with the output of the Flag Buffer FF (now in the set state) to set the Flag FF. This action synchronizes the affect of the Feed Hole signal with the computer timing by allowing the Flag FF to be set only at computer time T2.

4-23.   When the Flag FF is in the set state, the interface card flag logic responds by generating either an SKF signal, FLG and IRQ signals, or an SRQ signal. These signals indicate to the computer that an 8-bit word is in the input storage register and is ready to be transferred to the computer. The following paragraphs describe how these signals are generated and how they are used by the computer.

4-24.   SKIP-ON-FLAG SIGNAL. If the computer is programmed to wait for the Flag FF to be set (SFS instruction followed by a JMP *-1 instruction for example), the resulting SFS signal gated with a true signal from the set side of the Flag FF will generate an SKF signal. This causes the computer to skip the next programmed instruction (in this case JMP *-1) and proceed with the program. Figure 4-2 illustrates the generation of an SKF signal by the interface card. Notice that an SKF signal can also be generated when the Flag FF is in the clear state by programming an SFC instruction. Either way, the state of the Flag FF is being tested and the computer must be programmed to respond accordingly.

4-25.   INTERRUPT SIGNALS. If the computer's interrupt system has been enabled by an STF 00 instruction, the computer can be doing work in the main program rather than waiting for the Flag FF to be set. Figure 4-3 illustrates the functions involved in an interrupt operation. To interrupt the main program when the tape reader is ready, the following conditions must be met:

    a.   Control FF set (paragraph 4-18).

    b.   Flag Buffer FF set (paragraph 4-21).

    c.   Flag FF set (paragraph 4-22).

    d.   IEN signal true (interrupt system enabled).

    e.   PRH signal true (no higher priority interrupts).

4-26.   When all of these conditions are established, an SIR signal from the computer at time T5 will set the IRQ FF which generates true FLG and IRQ signals. These signals are used by the computer I/O control and addressing circuits to generate an interrupt request signal.

4-27.   At time T2 after interrupt is initiated, an ENF signal clears the IRQ FF. An SIR signal again sets the IRQ FF if the PRH signal is still true at time T5 during the interrupt phase. The FLG and IRQ signals this time are used by the computer I/O control and addressing circuits to encode the interrupt address.

4-28.   The next machine cycle will be under control of the instruction located at the interrupt address in memory. During this machine cycle, an IAK signal clears the Flag Buffer FF and an ENF signal at time T2 clears the IRQ FF. The Flag FF remains set to inhibit lower priority interrupts by providing a false PRL signal. A CLF instruction must be programmed to clear the Flag FF and enable lower priority interrupts just before returning to the main program.

4-29.   SERVICE REQUEST LOGIC.

4-30.   If the computer is equipped with the Direct Memory Access (DMA) option, and the DMA circuits have been initialized, the 8-bit word from the tape reader can be transferred directly into the computer memory. When the Flag FF on the interface card is set, the interface card supplies a true SRQ signal which enables the DMA circuits. The DMA circuits then suspend the computer program for one machine cycle and provide the necessary signals to transfer the 8-bit word to the computer memory.

4-31.   Refer to the applicable DMA option operating and service manual for detailed information on DMA controlled I/O operations.

4-32.   INPUT REGISTER LOGIC.

4-33.   As described in paragraph 4-21, the Feed Hole signal latches the 8-bit word from the tape reader into the input storage register. An LIA, LIB, MIA, or MIB instruction in the main program or in an interrupt subroutine transfers the word from the input storage register to the computer A- or B-register. Any one of these instructions with the select code of the tape reader interface card supplies true IOG, SCM, SCL, and IOI signals to the interface card. The IOI signal strobes the 8 bits from the input storage register onto the IOBI lines (bits 0-7). With the 8 bits of data in the computer, the operation of the tape reader interface card is complete.
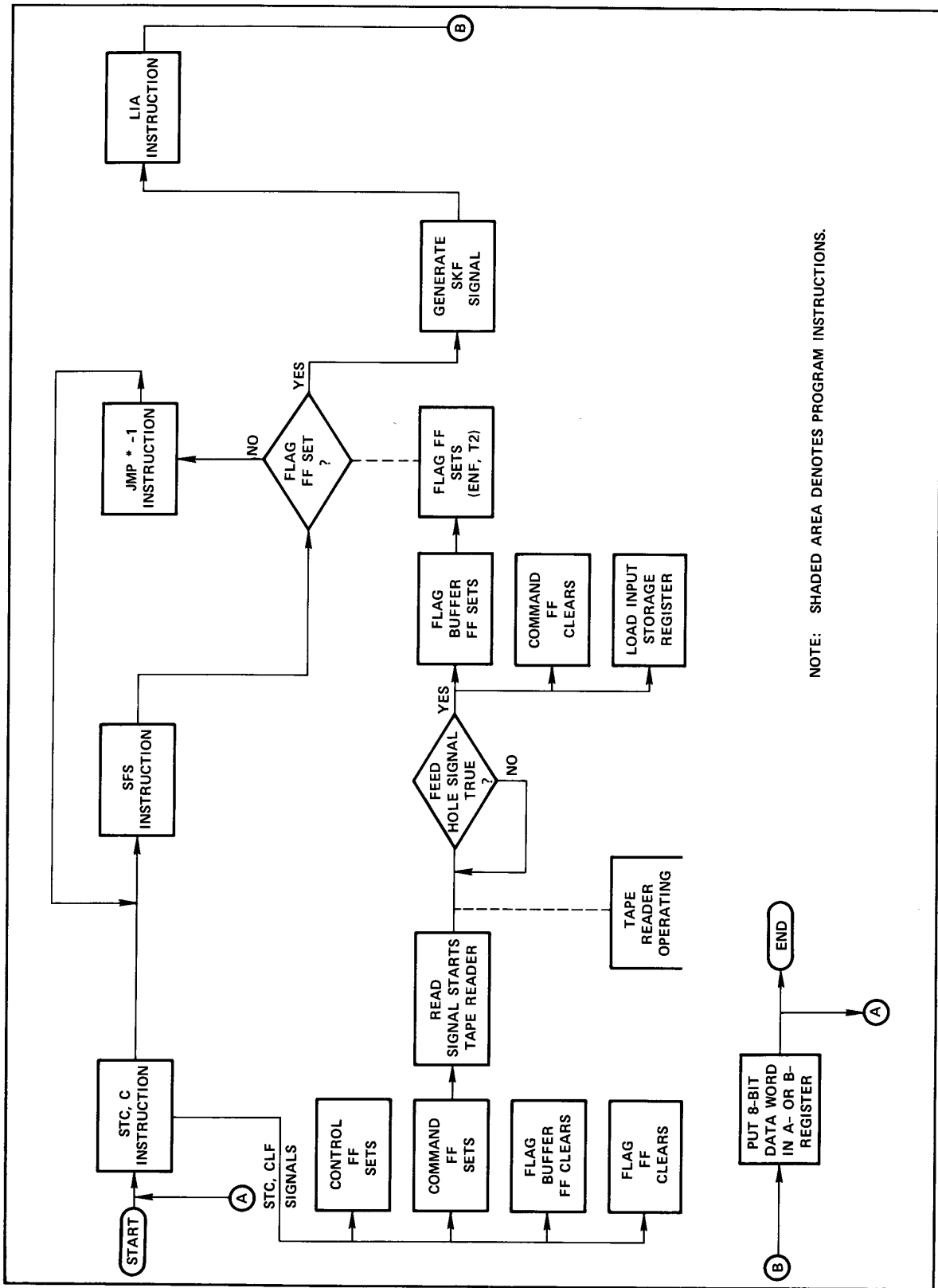
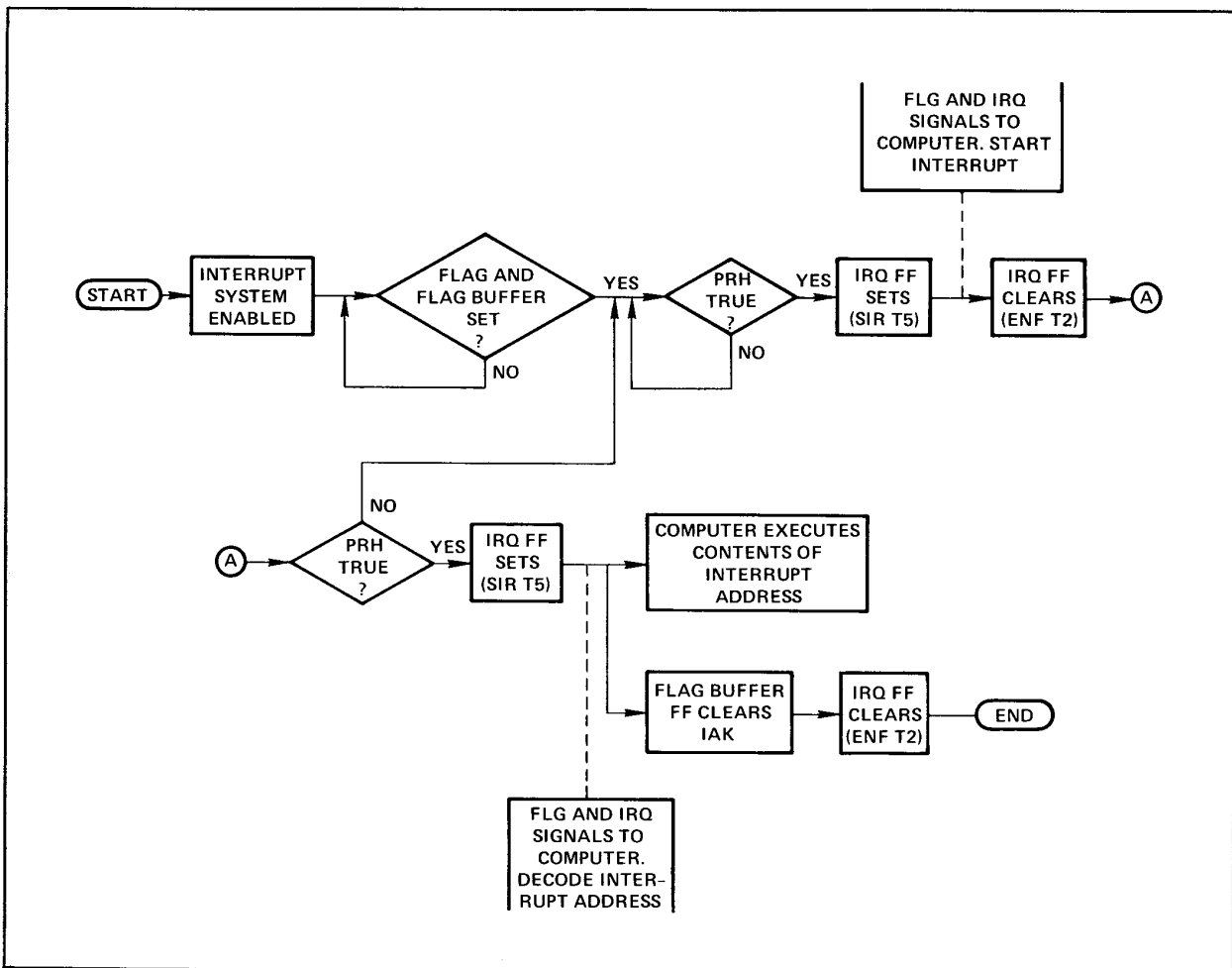Figure 4-1. Tape Reader Interface Card Functional Operation Flow Chart

2118-1
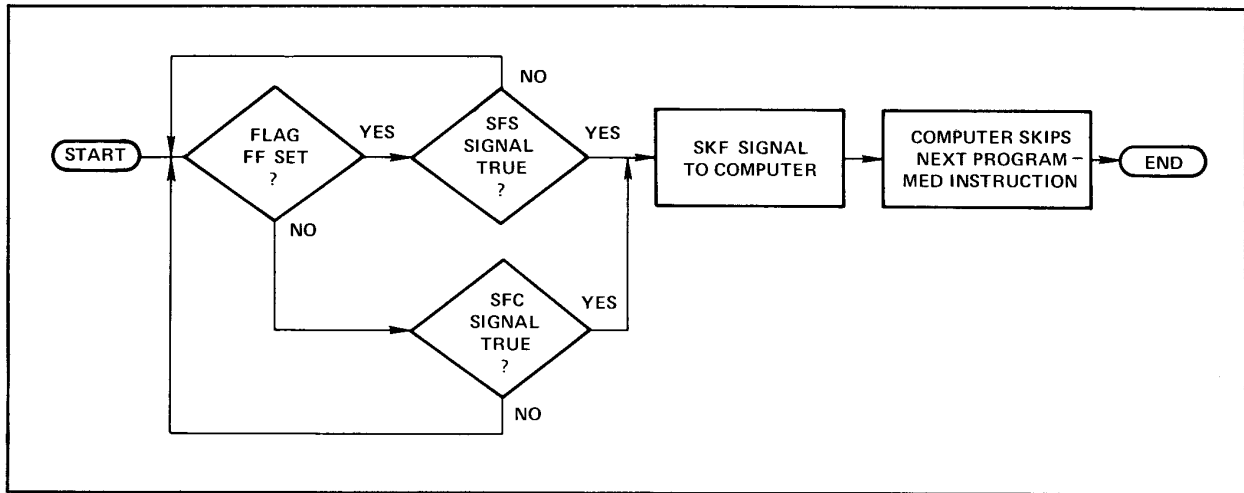
2118-2

Figure 4-2. Skip-On-Flag Signal Generation Flow Chart

2118-3A

Figure 4-3. Interrupt Operation Flow Chart
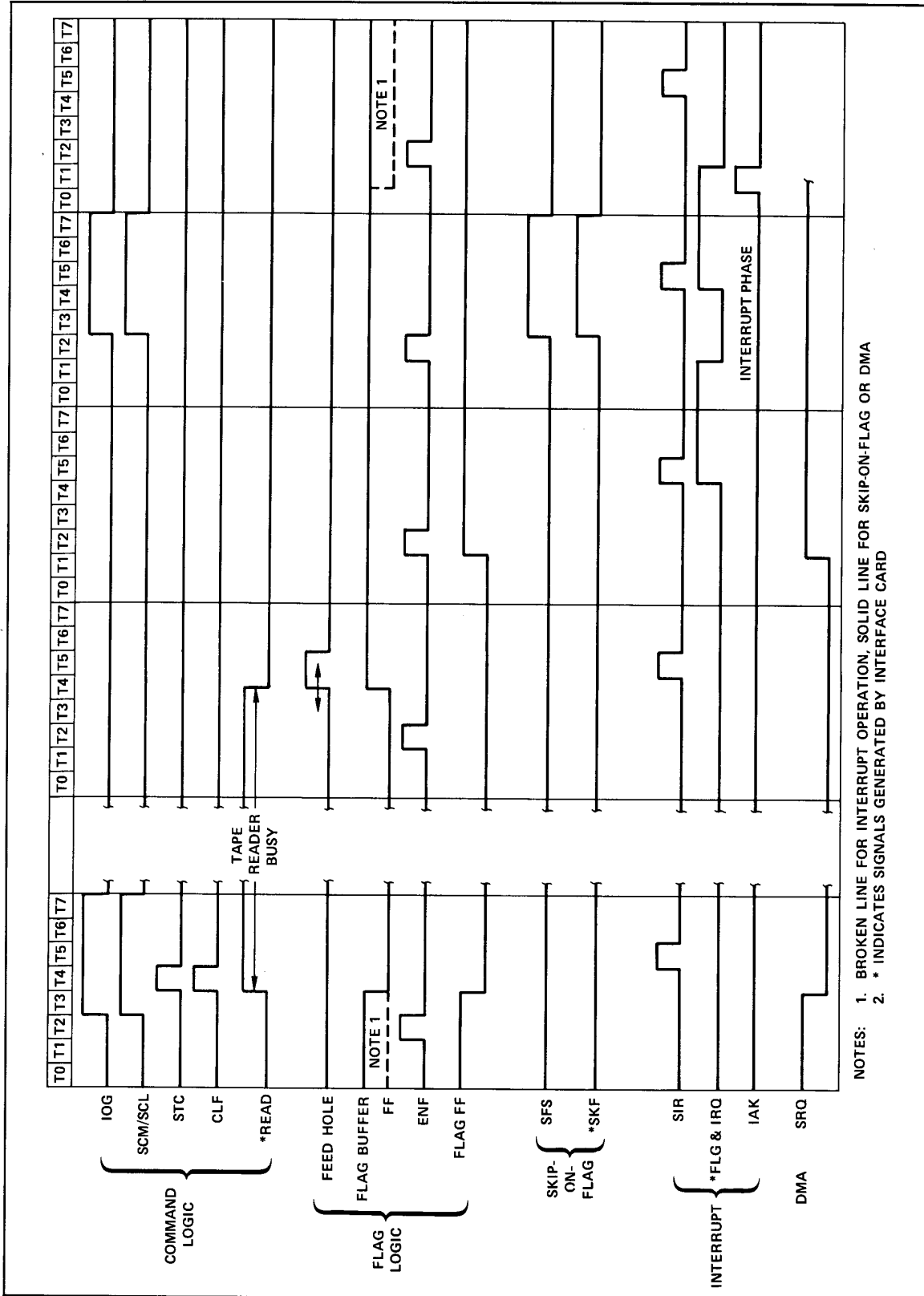
Figure 4-4. Overall Timing Diagram Showing Operation with 2114, 2115, and 2116 Computers

NOTES: 1. BROKEN LINE FOR INTERRUPT OPERATION, SOLID LINE FOR SKIP-ON-FLAG OR DMA
2. * INDICATES SIGNALS GENERATED BY INTERFACE CARD

2118-4
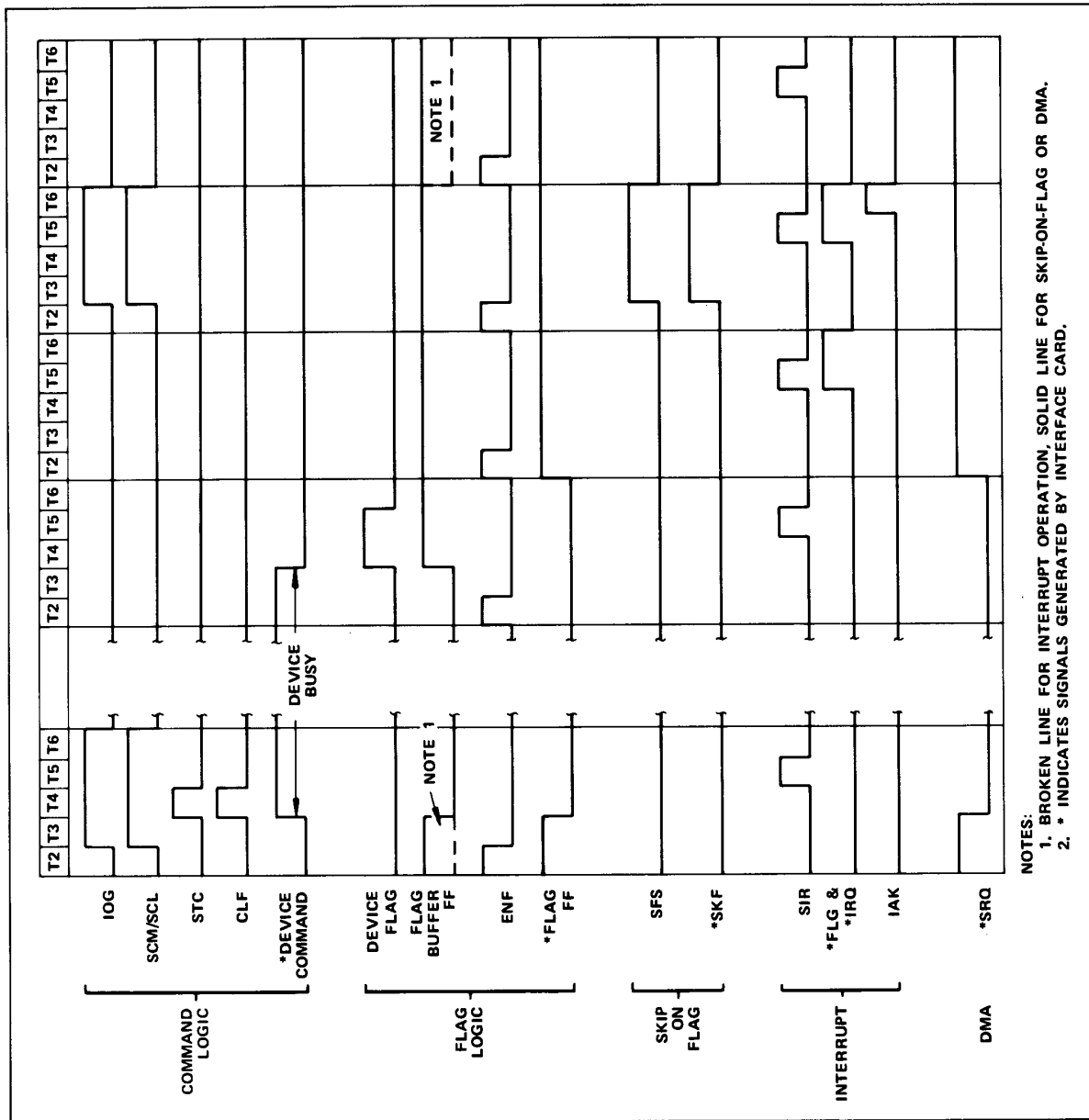
Figure 4-5. Overall Timing Diagram Showing Operation with 2100 Computer

NOTES:
1. BROKEN LINE FOR INTERRUPT OPERATION, SOLID LINE FOR SKIP-ON-FLAG OR DMA.
2. * INDICATES SIGNALS GENERATED BY INTERFACE CARD.

2118-US1

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2.   This section provides maintenance information for
the tape reader interface kit. Included are preventive main-
tenance instructions, troubleshooting instructions, and
maintenance data consisting of an interface card replaceable
parts list (table 5-1), information pertaining to the inte-
grated circuit pin connections and characteristics
(figure 5-1), an interface card parts location diagram and
logic diagram (figure 5-2), and an interface cable signal
index (table 5-2).

5-3. PREVENTIVE MAINTENANCE.

5-4.   Preventive maintenance for the tape reader inter-
face kit should be performed along with the preventive
maintenance routines for the computer system.

5-5.   Preventive maintenance consists of running the
combined tape reader and tape reader interface diagnostic
test procedure (part number 02737-90101 for 2114, 2115,
and 2116 Computers, or part number 5951-1363 for 2100
Computers), as described in the Manual of Diagnostics. Also,
visually inspect the interface card, cable, and connectors for
burned or broken components, connections, and insulation.

5-6. TROUBLESHOOTING.

5-7.   Troubleshooting the tape reader interface card is
accomplished by running the diagnostic test procedure (part
number 12554-90023 for 2114, 2115, and 2116 Computers
and part number 12554-90026 for 2100 Computers), as
described in the Manual of Diagnostics and analyzing error
halts as they occur.

5-8.   Use the maintenance data contained in this section
to further isolate faulty components.

Table 5-1. Tape Reader Interface Card Replaceable Parts List

| REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C8,18	0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	28480	0140-0198
C9 thru C16	0140-0191	Capacitor, Fxd, Mica, 56 pF, 5%	28480	0140-0191
C17	0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192
C19,22	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C20,21	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%	28480	0160-0154
C23 thru C32	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X 9020A2
CR9 thru CR17	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
MC15,36	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC16,26,47	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC17,25,27,37,46,57,86,94	1820-0054	Integrated Circuit, TTL	56289	USN7400A
MC34,44,64,74	1820-0301	Integrated Circuit, TTL	01295	SN7475N
MC35	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC45,55,65,75	1820-0974	Integrated Circuit, CTL	07263	SL4817
MC56,66	1820-0071	Integrated Circuit, TTL	56289	USN7440A
Q1 thru Q18	1854-0215	Transistor, Si, NPN	04713	SPS3611
R1 thru R8,18	0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417
R9 thru R17	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442
R19,22,23	0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R20,30,31	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R21	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R24,25,28,32	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R26,27	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R29	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R101,103,105,107,109, 111,113,115,117,118	1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008
R119 thru R122	1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020
W1 thru W7	8159-0005	Jumper Wire	28480	8159-0005
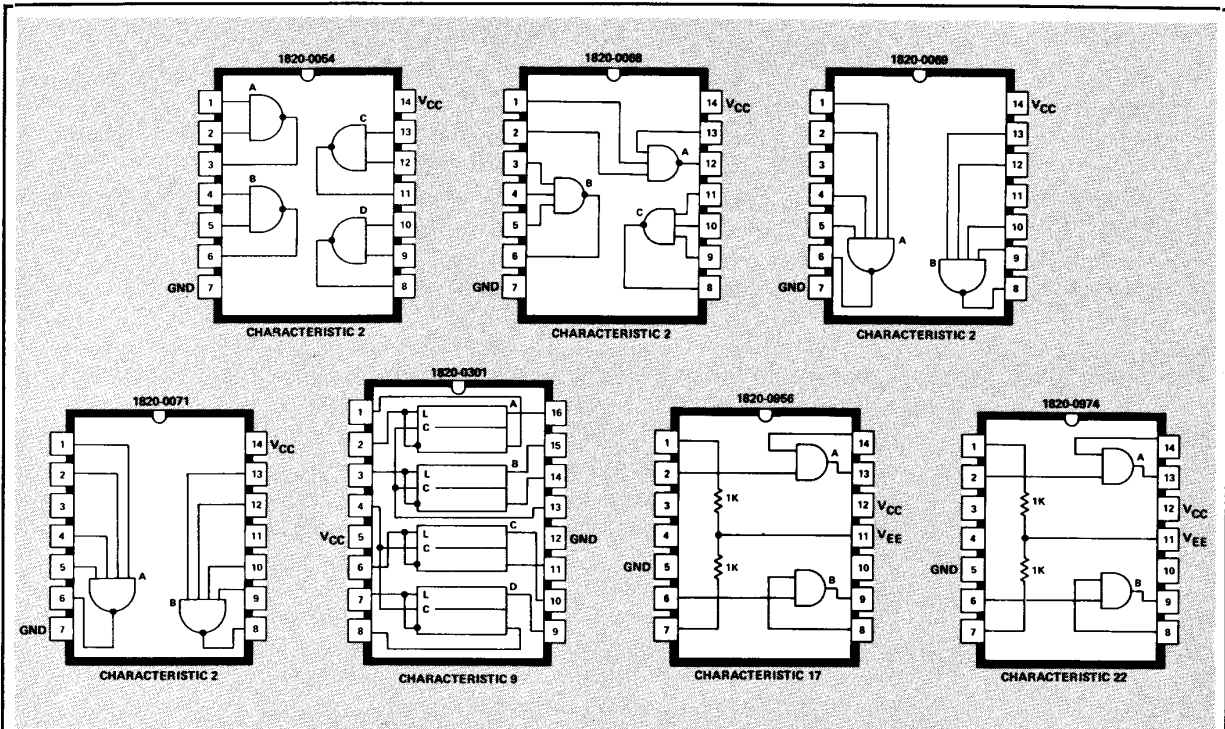
(TOP VIEW)

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECOND)	TO LOGIC 0 (NANOSECOND)
2	+2.0	+0.8	+2.4	+0.4	1	29	15
9	+2.0*	+0.8	+2.4	+0.4	1	40	25
17	+1.25	+0.5	+2.25	-0.36	0	18	18
22	+1.5	+0.4	+2.2	-0.3	0	24	24

*Required pulse widths; clock 30 ns minimum, data 75 ns minimum.

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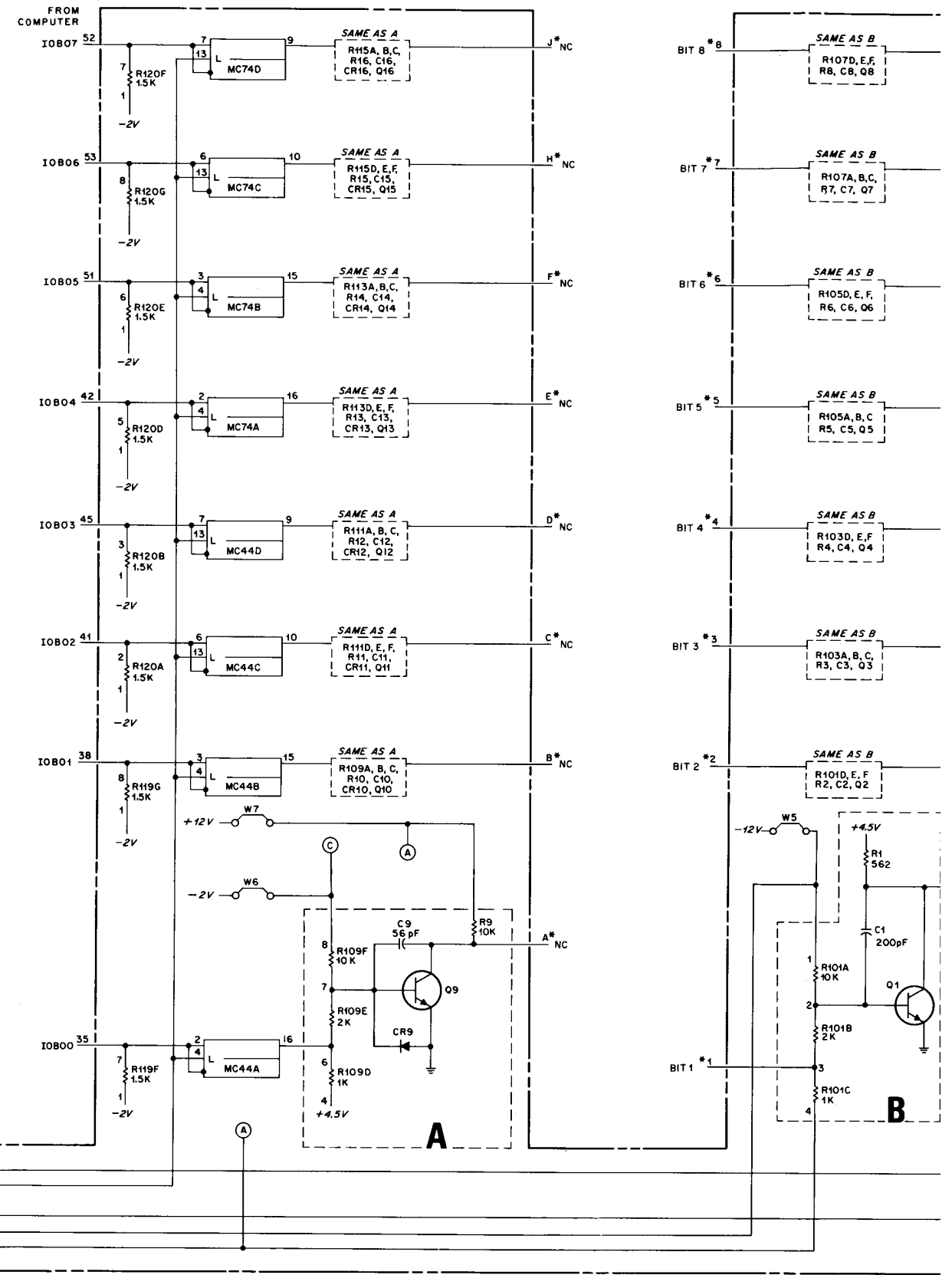Figure 5-1. Integrated Circuit Pin Connections and Characteristics
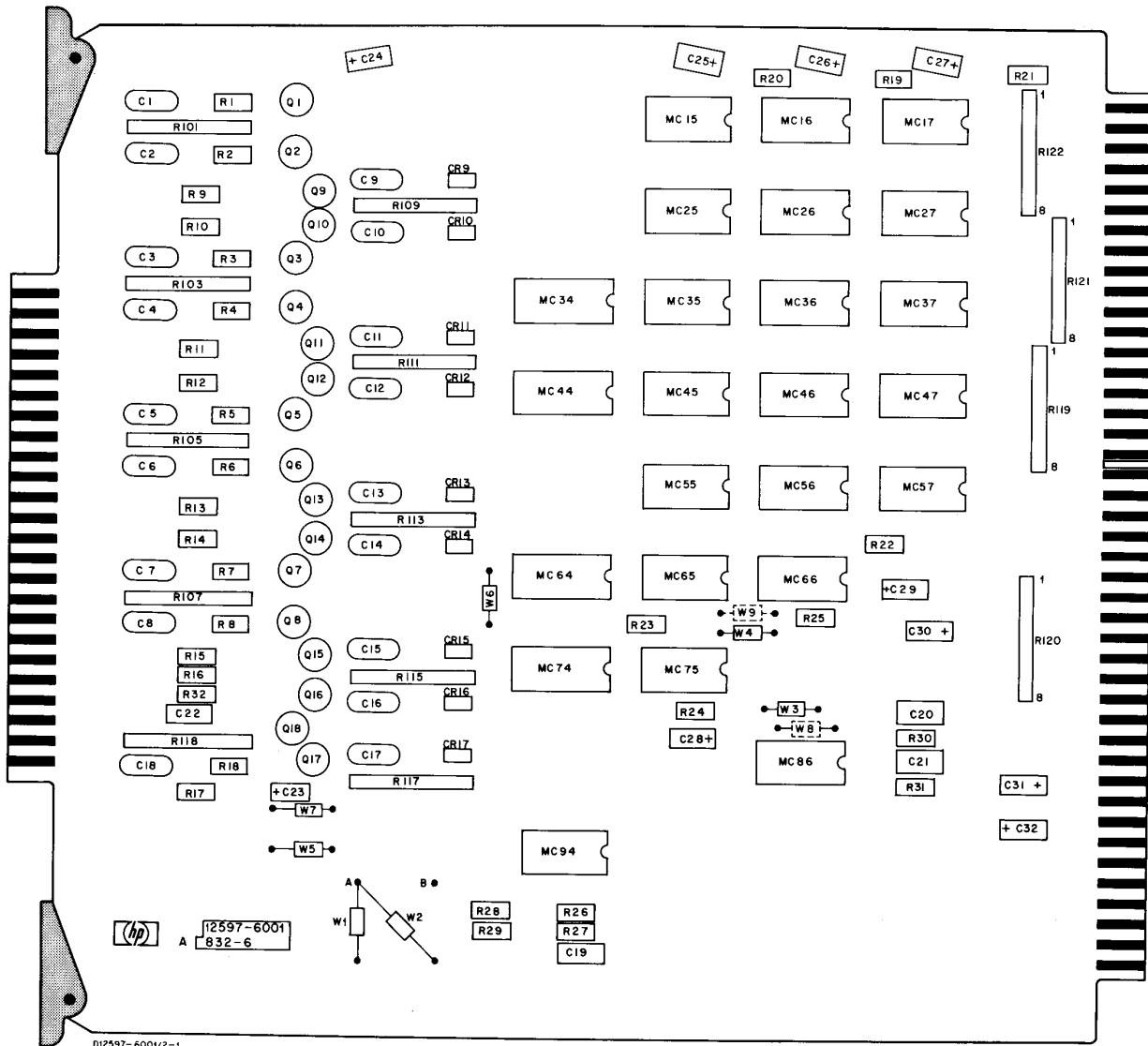
D12597-6001/2-1

Table 5-2. Interface Cable Signal Index

48-PIN CONNECTOR PIN NO.	TAPE READER CONNECTOR PIN NO.	SIGNAL
1	B	Bit 1
2	F	Bit 2
3	L	Bit 3
4	R	Bit 4
5	V	Bit 5
6	Z	Bit 6
7	d	Bit 7
8	j	Bit 8
AA	AA	Read
23	FF	Feed Hole
24,BB	HH	Ground

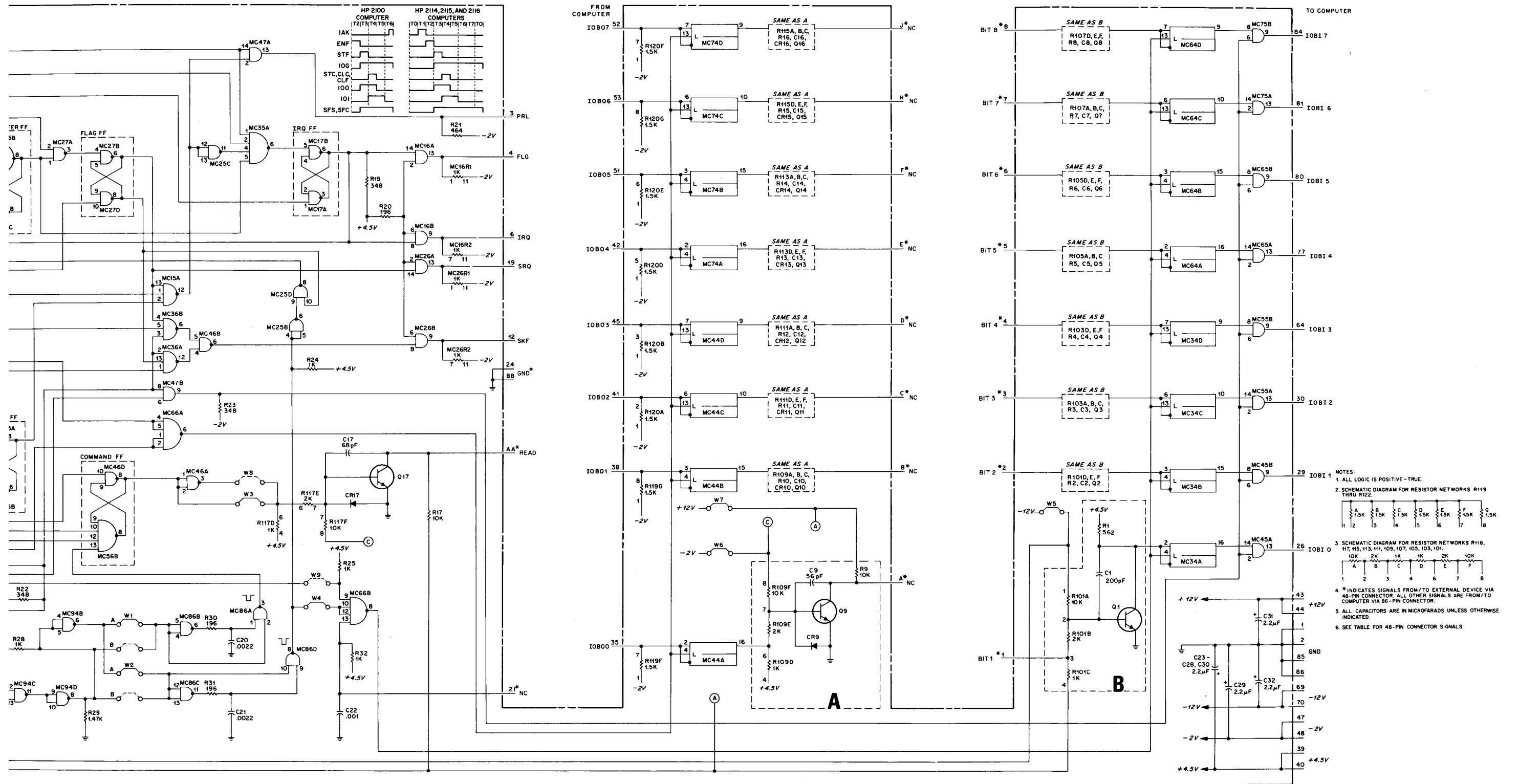TAPE READER INTERFACE CARD (12597-6001, REV. 832)
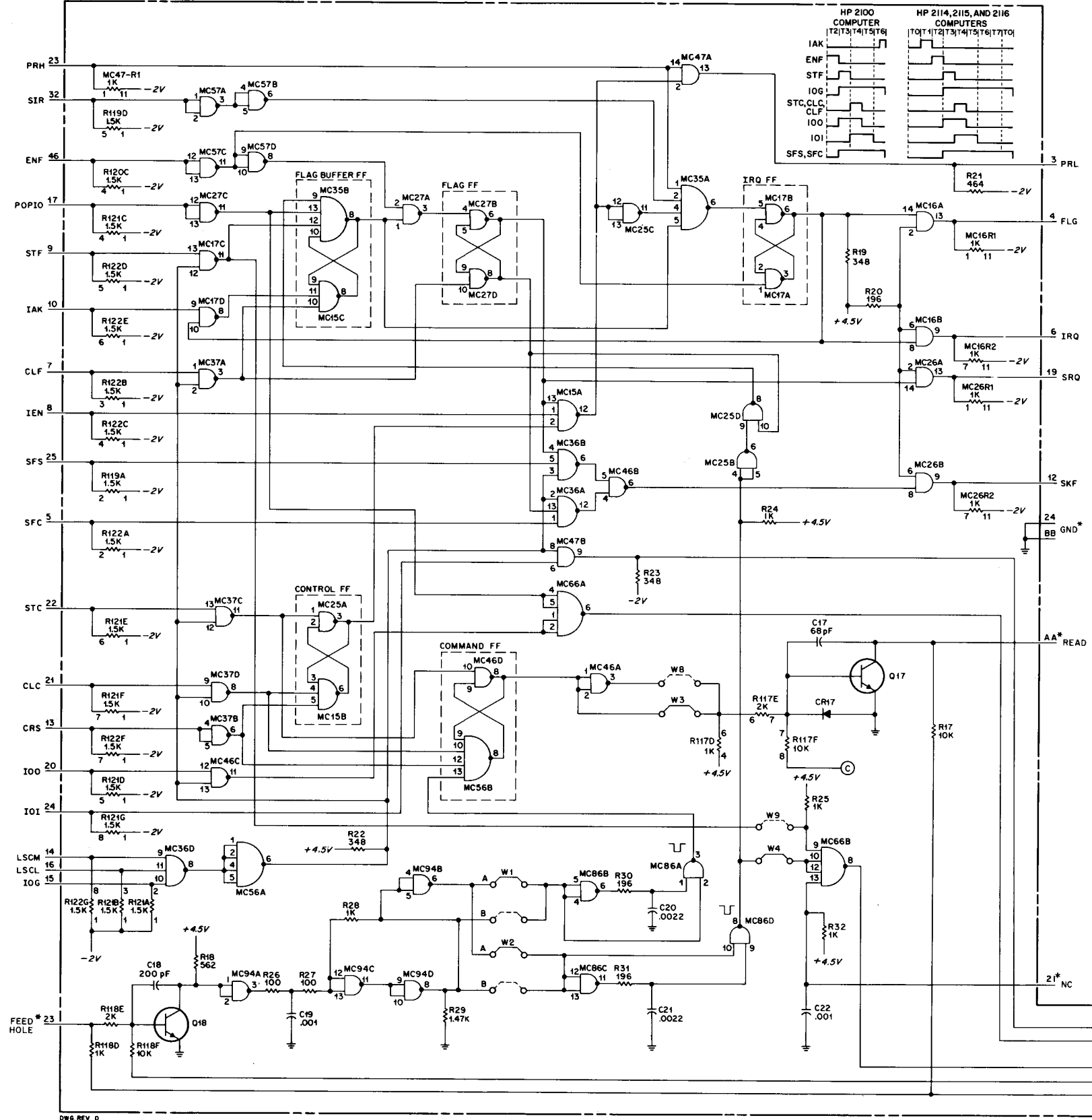
Figure 5-2. Tape Reader Interface Card Parts Location
Diagram and Logic Diagram

SECTION VI

REPLACEABLE PARTS

6-1.   INTRODUCTION.

6-2.   This section provides information for ordering re-
placement parts for the 12597A-002 Tape Reader Interface
Kit. Table 6-1 is a numerical listing of all replaceable parts
in the interface kit.

6-3.   An interface card replaceable parts list (table 5-1)
and parts location diagram (figure 5-2) are provided in
Section V of this manual.

6-4.   Tables 5-1 and 6-1 list the following information
for each replaceable part:

a.   Reference designation of the part (table 5-1 only).
(Refer to table 6-2 for an explanation of the abbreviations
used in the REFERENCE DESIGNATION column.)

b.   Hewlett-Packard part number.

c.   Description of the part. Refer to table 6-2 for an
explanation of the abbreviations used in the
DESCRIPTION column.

d.   A five digit code that corresponds to the manu-
facturer of the part. (Refer to table 6-3 for a code list of
manufacturers.)

e.   Manufacturer's part number.

f.   Total quantity (TQ) of each part used in the kit or
assembly (table 6-1 only).

6-5.   ORDERING INFORMATION.

6-6.   To order replacement parts, address the order or
inquiry to the nearest Hewlett-Packard Sales and Service
Office. Refer to the list at the back of this manual for
addresses. Specify the following information for each part
ordered:

a.   Identification of the instrument, kit, or assembly
containing the part (refer to paragraph 1-8).

b.   Hewlett-Packard part number for each part.

c.   Description of each part.

d.   Circuit reference designation for each part (if
applicable).

Table 6-1. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0191	Capacitor, Fxd, Mica, 56 pF, 5%	28480	0140-0191	8
0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192	1
0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	28480	0140-0198	9
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	2
0160-0154	Capacitor, Fxd, My, 2200 pF, 10%	28480	0160-0154	2
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X 9020A2	10
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	28480	0698-0082	1
0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	3
0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	3
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	4
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1/8W	28480	0757-0401	2
0757-0417	Resistor, Fxd, Flm, 562 ohms, 1%, 1/8W	28480	0757-0417	9
0757-0442	Resistor, Fxd, Flm, 10.0 ohms, 1%, 1/8W	28480	0757-0442	9
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094	1
1251-0332	Connector, PC	13511	143-024-08 (1158)	1
1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008	10
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	4
1820-0054	Integrated Circuit, TTL	56289	USN7400A	8
1820-0068	Integrated Circuit, TTL	56289	USN7410A	2
1820-0069	Integrated Circuit, TTL	56289	USN7420A	1
1820-0071	Integrated Circuit, TTL	56289	USN7440A	2
1820-0301	Integrated Circuit, TTL	01295	SN7475N	4
1820-0956	Integrated Circuit, CTL	07263	SL3459	3
1820-0974	Integrated Circuit, CTL	07263	SL4817	4
1854-0215	Transistor, Si, NPN	04713	SPS3611	18
1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088	9
8159-0005	Jumper Wire	28480	8159-0005	7
12597-6001	Tape Reader Interface Card	28480	12597-6001	1
12597-6004	Cable	28480	12597-6004	1
12597-90022	Operating and Service Manual	28480	12597-90022	1