CHAPTER 4
I/O ADDRESS SUMMARY

The following is a summary of the HORNET I/O addresses.

4.1 PC-Compatible Registers

4.1.1 Programmable Interrupt Controller (8259 Compatible)

I/O Address	R/W Mode	Description
0020h	R	PIC Interrupt Request/In-Service Registers programmed by Operation Command Word 3 (OCW3): Interrupt Request Register, where: bits 7-0 = 0 no active request for the corresponding interrupt line = 1 active request for the corresponding interrupt line Interrupt In-Service Register, where: bits 7-0 = 0 the corresponding interrupt line is not currently being serviced = 1 the corresponding interrupt line is currently being serviced
0020h	W	PIC Initialization Command Word 1 (ICW1) when bit 4 is one: bits 7-5 = 0 not used bit 4 = 1 required to select this command word bit 3 = 0 edge triggered mode bit 2 = 1 not used bit 1 = 1 single mode (no ICW3 needed) bit 0 = 1 ICW4 needed

I/O Address	R/W Mode	Description		
0021h	W	PIC ICW2 and ICW4 in sequential order after ICW1 written to Port 0020h:		
		ICW2, where:		
		bit 7-3	=00001	address lines A7-A3 of base vector address for interrupt controller
		bit 2-0	=0	reserved
		ICW4, where:		
		bits 7-5	=0	not used
		bits 4	=0	no special fully nested mode
		bits 3-2	=11	buffered mode/master
		bit 1	=0	normal EOI
		bit 0	=1	8086/8088 mode
0021h	R/W	PIC interrupt mask register (OCW1), where:		
		bit 7	=0	enable IRQ7 GPIO interrupts
		bit 6	=0	enable IRQ6 GPIO interrupts
		bit 5	=0	enable IRQ5 GPIO interrupts
		bit 4	=0	enable IRQ4 UART interrupts
		bit 3	=0	enable IRQ3 GPIO interrupts
		bit 2	=0	enable IRQ2 miscellaneous interrupts
		bit 1	=0	enable IRQ1 PC compatible keyboard interrupt (checked by BIOS)
		bit 0	=0	enable IRQ0 timer0 interrupt
0020h	W	PIC OCW2 when bit 4 is zero and bit 3 is zero, where:		
		bits 7-5	=000	rotate in automatic EOI mode (clear)
			=001	non-specific EOI
			=010	no operation
			=011	specific EOI
			=100	rotate in automatic EOI command (set)
			=101	rotate on non-specific EOI command
			=110	set priority command
			=111	rotate on specific EOI command
		bits 3-4	=00	required to select this command word
		bits 2-0		interrupt request to which the command applies

I/O Address	R/W Mode	Description		
0020h	W	PIC OCW3 when bit 4 is zero and bit 3 is one, where:		
		bit 7	=0	reserved
		bits 6-5	=00	no operation
			=01	no operation
			=10	reset special mask
			=11	set special mask
		bits 4-3	=01	required to select this command word
		bit 2	=0	no poll command
			=1	poll command
		bits 1-0	=00	no operation
			=01	no operation
			=10	read interrupt request register on next read at Port 20h
		bits 1-0	=11	read interrupt in-service register on next read at Port 20h

4.1.2 HORNET Specific Registers

I/O Address	R/W Mode	Description		
0022h	R/W	HIR - Hornet index register		
0023h	R/W	HDR - Hornet data register		
0028h	R/W	CPU Power Control		
		bits 7-3		undefined when read, must write 0
		bit 1	=1	enter idle mode at next halt cycle
		bit 0	=1	enter powerdown mode at next halt cycle
0029h	R/W	bits 7-0		undefined when read, must write 0
002Ch	R	bits 7-4		reserved
		bits 3-0		Stepping ID (0001 for first parts)
002Dh	-	reserved		

4.1.3 Programmable Interval Timer (8254 Compatible)

I/O Address	R/W Mode	Description
0040h	R/W	PIT counter 0
0041h	R/W	PIT counter 1
0042h	R/W	PIT counter 2
0043h	W	PIT control word, where:

bits 7-6	=00	select Counter 0
	=01	select counter 1
	=10	select counter 2
	=11	read back command
bits 5-4	=00	counter latch command
	=01	read/write counter bits 0-7 only
	=10	read/write counter bits 8-15 only
	=11	read/write counter bits 0-7 first, then bits 8-15
bits 3-1	=000	mode 0 select
	=001	mode 1 select
	=x10	mode 2 select
	=x11	mode 3 select
	=100	mode 4 select
	=101	mode 5 select
bit 0	=0	binary counter 16 bits
	=1	BCD counter

4.1.4 Programmable Peripheral Interface (Emulates 8255)

The HORNET chip does not contain a PPI as such. Instead it contains a group of 3 I/O registers that are configured to behave as the PC's PPI. The definitions of the configuration switch bits should be chosen to be PC compatible.

I/O Address	R/W Mode	Description
0060h	R/W	PPI Input Port A:
		If port 0061h bit7=0:
		bits 7-0 — scratch location for keyboard scan code
		If port 0061h bit7=1:
		bits 7-0 — scratch location for SW1 configuration switch settings
0061h	R/W	PPI Output Port B:
		bit 7 =0 — read/write keyboard scratch byte (0060h)
		bit 7 =1 — read/write SW1 scratch byte (0060h)
		bit 6 =0 — disable keyboard
		bit 5 =0 — ignored, reads 0 (enable I/O check)
		bit 4 =0 — ignored, reads 0 (enable RAM parity check)
		bit 3 =0 — read high switch (0062h)
		bit 3 =1 — read low switch (0062h)
		bit 2 =0 — ignored, always reads 0
		bit 1 =1 — enable speaker data
		bit 0 =1 — enable timer 2 gate (to speaker)
0062h	R/W	PPI Input Port C:
		bits 7-6 =0 — unused (read only)
		bit 5 — timer 2 output (read only)
		bit 4 =0 — unused (read only)
		If port 0061h bit 3=0:
		bits 3-0 — scratch location for 4 MSBs of SW2 configuration switches
		If port 0061h bit 3=1:
		bits 3-0 — scratch location for 4 LSBs of SW2 configuration switches

4.1.5 Standard Display Controller Registers (PC CGA/MDA compatable)

I/O Address	Bits	R/W Mode	Description
03B4h/03D4h	4-0	R/W	CRTCindex - MDA/CGA CTRC index register.
03B5h/03D5h			CRTCdata - Indexed MDA/CGA CTRC data registers.
-0Ah			CurStart - cursor start scan line and blink mode.
	6-5	R/W	CurBlinkBits - cursor blink mode.
	4-0	R/W	CurStartBits - cursor start scan line.
-0Bh	4-0	R/W	CurStop - cursor stop scan line.
-0Ch	5-0	R/W	DspStHi - display start address high.
-0Dh	7-0	R/W	DspStLo - display start address low.
-0Eh	5-0	R/W	CurLocHi - cursor location high.
-0Fh	7-0	R/W	CurLocLo - cursor location low.
-10h	5-0	R	LpenHi - Light pen high. Reads same as Cursor address high.
-11h	7-0	R	LpenLo - Light pen low. Reads same as Cursor address low.
03B8h/03D8h			Mode - MDA/CGA mode control register.
	6	R/W	EnUndl - enable underline character attribute.
	5	R/W	EnBlink - enable blink character attribute.
	4	R/W	HiResGr - enable high resolution graphics.
	3	R/W	Unblank - unblank display.
	2	R/W	AlphaBW - disable alpha color.
	1	R/W	Graphics - 1 = graphics, 0 = alpha.
	0	R/W	HiResText - enable high resolution alpha.
03D9h	-	-	Palette - CGA pallete register (not implimented).
03BAh/03DAh			Status - MDA/CGA status register.
	3	R	Vsync - vertical sync.
	2	R	LPswitch - light pen switch.
	1	R	LPS - light pen status.
	0	R	Hsync - horizontal sync.
03DBh	-	-	ClrLPS - clear LPS bit in status register.
03DCh	-	-	SetLPS - set LPS bit in status register.

4.1.6 Serial Port (16450 Compatible UART)

I/O Address	R/W Mode	Description
03F8h	W	UART transmitter holding register, which contains the character to be sent. Bit 0, the least significant bit, is sent first.
		bits 7-0 — contains data bits 7-0 when Divisor Latch Access Bit (DLAB) = 0 (03FBh)
03F8h	R	UART receiver buffer register, which contains the received character.
		bits 7-0 — contains data bits 7-0 when DLAB=0
03F8h	R/W	UART divisor latch, low byte. Both divisor latch registers store the baud rate divisor.
		bits 7-0 — bits 7-0 of divisor when DLAB=1
03F9h	R/W	UART divisor latch, high byte, where:
		bits 7-0 — bits 15-8 of divisor, when DLAB=1
03F9h	R/W	UART interrupt enable register when DLAB = 0. Allows the four controller interrupts to enable the chip interrupt output signal.

bits 7-4	=0	reserved
bit 3	=1	modem status interrupt enable
bit 2	=1	receiver line status interrupt enable
bit 1	=1	transmitter holding register empty interrupt enable
bit 0	=1	received data available interrupt enable

I/O Address	R/W Mode	Description
03FAh	R	UART interrupt ID register. Information about a pending interrupt is stored here. When ID register is addressed, the highest priority interrupt is held and no other interrupts are acknowledged until the CPU services that interrupt.

bits 7-3 =0 reserved

bits 2-1 Identity of the pending interrupt with the highest priority

=11	receiver line status interrupt: highest priority
=10	received data available: second priority
=01	transmitter holding register: third priority
=00	modem status interrupt: lowest priority

bit 0	=0	interrupt pending, contents of register can be used as a pointer to the appropriate interrupt service routine
	=1	no interrupt pending

03FBh R/W UART Line Control Register, where:

bit 7	=0	Receiver buffer, transmitter holding or interrupt enable register access (DLAB)
bit 7	=1	divisor latch access
bit 6	=1	set break enabled (output = space)
bit 5		stick parity
bit 4	=0	odd parity
	=1	even parity
bit 3	=1	parity enable
bit 2	=0	1 stop bit
	=1	1.5 stop bits if bits 1-0 = 00, else 2 stop bits
bits 1-0	=00	5 bit word length
	=01	6 bit word length
	=10	7 bit word length
	=11	8 bit word length

I/O Address	R/W Mode	Description		
03FCh	R/W	UART Modem Control Register		
		bits 7-4	=0	reserved
		bit 3	=1	enable UART interrupt
		bit 2	=0	reserved
		bit 1	=0	Request to Send inactive
			=1	Request to Send active
		bit 0	=0	Data Terminal Ready inactive
			=1	Data Terminal Ready active
03FDh	R	UART Line Status Register, where:		
		bit 7	=0	reserved
		bit 6	=1	transmitter shift and holding registers empty
		bit 5	=1	transmitter holding register is empty
		bit 4	=1	break interrupt
		bit 3	=1	framing error
		bit 2	=1	parity error
		bit 1	=1	overrun error
		bit 0	=1	data ready
03FEh	R	UART Modem Status Register		
		bit 7	=0	Data Carrier Detect inactive
			=1	Data Carrier Detect active
		bit 6	=0	Ring Indicator inactive
			=1	Ring Indicator active
		bit 5	=0	Data Set Ready inactive
			=1	Data Set Ready active
		bit 4	=0	Clear to Send inactive
			=1	Clear to Send active
		bit 3	=1	Data Carrier Detect changed state
		bit 2	=1	Ring Indicator changed state
		bit 1	=1	Data Set Ready changed state
		bit 0	=1	Clear to Send changed state
03FFh	R/W	UART scratch pad register		

4.2 HORNET Specific Registers

The HORNET chip contains a collection of special purpose hardware that is not found in a PC compatible system. In order to avoid conflicts with the PC IO address mapping, the registers required to interface to this hardware are addressed using an index register and a data register located at 022h and 023h. The following sections describe these registers.

4.2.1 Keyboard

Index	R/W Mode	Description
-00h	W	Low byte of keyboard output register (KB[0-7]) A write to this location starts keyboard precharge.
-01h	W	Middle byte of keyboard output register (KB[8-15])
-02h	W	High 6 bits of keyboard output register (KB[16-21]) bits 0-5 KB[16-21] bits 6-7 unused
-03h	W	A write to this location ends keyboard precharge.
-00h	R	Low byte of keyboard input register (KB[0-7])
-01h	R	Middle byte of keyboard input register (KB[8-15])
-02h	R	High byte of keyboard input register (KB[16-21], KBI[22-23])) bits 0-5 KB[16-21] bits 6-7 KBI[22-23]
-03h	R	bit 0 ONKEY pressed flag bits 1-7 unused Note: bit 0 will be set while the ONKEY is pressed and after it is released, reading this register after the ON key is released clears bit 0.

4.2.2 Real-Time-Clock

Index	R/W Mode	Description	
-08h	R/W	bits 7-0	bits 7-0 of the 26-bit counter value
-09h	R/W	bits 7-0	bits 15-8 of the 26-bit counter value
-0Ah	R/W	bits 7-0	bits 23-16 of the 26-bit counter value
-0Bh	R/W	bits 1-0	bits 25-24 of the 26-bit counter value
		bit 2	F16HZ signal (read only)
		bit 3	F8HZ signal (read only)
		bit 4	F4HZ signal (read only)

bit 5	F2HZ signal (read only)
bit 6	F1HZ, Anticipates the state of the RTC clock by 1mS (read only)
bit 7	Shows the state of the RTC clock (read only)

4.2.3 Miscellaneous Registers

Index	R/W Mode	Description		
-10h	R/W	IR Format Register (IRFMAT)		
		bit 7	=1	invert sense of LED signal
			=0	normal sense of LED signal
		bit 6	=1	enable LED buffer empty interrupt
		bit 5	=1	LED buffer full (read only)
		bit 4	=0	single pulse transmission mode
			=1	multiple pulse transmission mode
		bit 3	=0	modulate using 32.768KHz
			=1	modulate using baud rate generator
		bit 2	=1	IR UART communication mode
		bit 1	=1	modulated communication mode
		bit 0	=1	REDEYE transmit mode
-11h	R/W	IR Transmit / Receive Register		
		bit 7		state of the IRI pin (read only)
		bit 6	=1	enable IR interrupt on IRI = 1
		bit 5	=1	IR event has occurred, must be cleared by software
		bits 4-3		unused
		bit 2	=1	gate output when in modulated communication mode
		bit 1	=0	transmit "off" half-bit in REDEYE format
			=1	transmit "on" half-bit in REDEYE format
		bit 0	=1	turn on LED driver, used for software controlled transmissions
-12h	R/W	ADC Control Register		
		bits 7-5		unused except for testing
		bit 4	=1	ADC is busy doing a conversion; read only
		bit 3	=1	DAC value above analog input; read only (comparitor output)
		bits 2-1	Input Voltage Channel Select, where:	
			=00	system batteries
			=01	backup battery
			=10	reference voltage
			=11	VSS
		bit 0	=1	enable ADC
-13h	R/W	ADC Value Register		
		bits 5-0		ADC value
		bits 7-6		unused (read zero)

Index	R/W Mode	Description		
-18h	R/W	First Byte of Interrupt Enable Register		
		bits 7-2		unused
		bit 1	=1	force PC Keyboard interrupt (IRQ1)
		bit 0	=1	enable timer 0 interrupt/wakeup (IRQ0)
-19h	R/W	Second Byte of Interrupt Enable Register		
		bit 7	=1	IR interrupt/wakeup (IRQ2)
		bit 6	=1	keyboard interrupt/wakeup (IRQ2)
		bit 5	=1	ring detect interrupt/wakeup (IRQ2)
		bit 4	=1	RX pad interrupt/wakeup (IRQ2)
		bit 3	=1	timer 1 interrupt/wakeup (IRQ2)
		bit 2	=1	RTC interrupt/wakeup (IRQ2)
		bit 1	=1	display cursor interrupt (IRQ2)
		bit 0	=1	low power interrupt (NMI)
-1Ah	R/W	Interrupt Source Register		
		bit 7	=1	IR interrupt (IRQ2)
		bit 6	=1	keyboard interrupt (IRQ2)
		bit 5	=1	ring detect interrupt (IRQ2)
		bit 4	=1	RX pad interrupt (IRQ2)
		bit 3	=1	timer 1 interrupt (IRQ2)
		bit 2	=1	RTC underflow (IRQ2)
		bit 1	=1	display cursor interrupt (IRQ2)
		bit 0	=1	low power interrupt (NMI)
-1Eh	R/W	System Control Register		
		bits 7-6	speaker volume	
			=00	off (0V)
			=01	soft (3V)
			=10	medium (5V)
			=11	loud (8V)
		bits 5-4	crystal speed selection	
			=00	10.738636 MHz
			=01	15.836773 MHz
			=10	21.477272 MHz
			=11	31.673550 MHz
		bit 3		unused
		bit 2	=1	display on
		bit 1	=1	unit has been in backup mode
		bit 0	=1	CPU shutdown (set only)

Index	R/W Mode	Description
-1Fh	R/W	System Status Register
		bit 7 =0 reset has occured; this bit will be cleared by a system reset; it is initialized to a one by the warmstart code
		bit 6 unused
		bit 5 unused
		bit 4 =1 Internal 8254, 8259, or 8255 has been accessed
		bit 3 =1 External IO device has been accessed
		bit 2 =1 PC compatible MDA/CGA register has been accessed
		bit 1 =1 Video RAM has been accessed
		bit 0 =1 UART has been accessed

4.2.4 Non-Standard Display Controller Registers

Index	Bits	R/W Mode	Description
-20h			DspSetUp - display setup register.
	7-5	R/W	DspTest - display test mode selection.
	4	R/W	NoRTLmode - disable row-then-line mode.
	3	R/W	UCmode - enable update on change mode.
	2	R/W	JagGrMode - select jaguar compatible graphics.
	1	R/W	CGAMode - select CGA registers.
	0	R/W	DspEnable - enable MDA/CGA registers and memory.
-21h			DspSpd - clock speed selection.
	3-2		DotClk - dot clock to display module.
	1-0		DspClk - display DRAM access speed.
-22h	7-0	R/W	RowTime - row timer.
-23h	4-0	R/W	Contrast - contrast control.
-24h	6-0	R/W	HorzDsp - horizontal displayed.
-25h			ChrWidth - character width
	2	R/W	DoubDot - enable dot doubler.
	1-0	R/W	CellWid - character cell width.
-26h	5-0	R/W	RowOff - window row size offset.
-27h	4-0	R/W	FontOff - font offset.
-28h	7-0	R/W	VertDsp - vertical displayed.
-29h	4-0	R/W	MaxScan - maximum scan line.
-2Ah	5-0	R/W	VertAdj - vertical adjust.
-2Bh	4-0	R/W	Underline - underline scan line.
-2Ch			ShadeReg - shading and color mapping.
	3-2	R/W	ShadeMode - shading technique selection.
	1	R/W	EnFRS - enable frame-rate shading.
	0	R/W	Invert - invert shades.

4.2.5 BITBLT Registers

Index	Bits	Mode	Description
-30h	7-0	R/W	SrcPtrLow - source pointer low byte.
-31h	4-0	R/W	SrcPtrHi - source pointer high byte.
-32h	7-0	R/W	DstPtrLow - destination pointer low byte.
-33h	4-0	R/W	DstPtrHi - destination pointer high byte.
-34h	2-0	R/W	DstBitOff - destination bit offset.
-35h	2-0	R/W	ChrW - character width.
-36h	4-0	R/W	ChrH - character height.
-37h			BitBltMode - bitblt mode and status register.
	5	R	BitBltBusy - bitblt busy flag.
	4	R/W	InsaneFTF - select insane font table format.
	3-0	R/W	XferMode - transfer mode selection.

4.3 GPIO

4.3.1 Configuration Registers

Index	R/W Mode	Description		
-40h	R/W	bit 7	=1	enable pulldown on GPIO[1]
		bit 6	=1	enable pullup on GPIO[1]
		bits 5-4	=00	GPIO[1] is general purpose input
			=01	GPIO[1] is general purpose output
			=10	GPIO[1] is control pin
			=11	illegal
		bit 3	=1	enable pulldown on GPIO[0]
		bit 2	=1	enable pullup on GPIO[0]
		bits 1-0	=00	GPIO[0] is general purpose input
			=01	GPIO[0] is general purpose output
			=10	GPIO[0] is control pin
			=11	illegal
-41h	R/W	bits 7-4		GPIO[3] configuration (see -40h)
		bits 3-0		GPIO[2] configuration (see -40h)
-42h	R/W	bits 7-4		GPIO[5] configuration (see -40h)
		bits 3-0		GPIO[4] configuration (see -40h)
-43h	R/W	bits 7-4		GPIO[7] configuration (see -40h)
		bits 3-0		GPIO[6] configuration (see -40h)
-44h	R/W	bits 7-4		GPIO[9] configuration (see -40h)
		bits 3-0		GPIO[8] configuration (see -40h)
-45h	R/W	bits 7-4		GPIO[11] configuration (see -40h)
		bits 3-0		GPIO[10] configuration (see -40h)
-46h	R/W	bits 7-4		GPIO[13] configuration (see -40h)
		bits 3-0		GPIO[12] configuration (see -40h)
-47h	R/W	bits 7-4		GPIO[15] configuration (see -40h)
		bits 3-0		GPIO[14] configuration (see -40h)
-48h	R/W	bits 7-4		GPIO[17] configuration (see -40h)
		bits 3-0		GPIO[16] configuration (see -40h)
-49h	R/W	bits 7-4		GPIO[19] configuration (see -40h)
		bits 3-0		GPIO[18] configuration (see -40h)
-4Ah	R/W	bits 7-4		GPIO[21] configuration (see -40h)
		bits 3-0		GPIO[20] configuration (see -40h)
-4Bh	R/W	bits 7-4		GPIO[23] configuration (see -40h)
		bits 3-0		GPIO[22] configuration (see -40h)

Index	R/W Mode		Description
-4D	R/W	bit 7	unused
		bits 6-4 = 001	select NMI interrupt for GPIO[24]
		= nnn	select IRQ[nnn] interrupt for GPIO[24] (nnn = 2-3,5-7)
		bit 3 = 1	enable pulldown on GPIO[24]
		bit 2 = 1	enable pullup on GPIO[24]
		bit 1	unused
		bit 0 = 0	GPIO[24] is general purpose input
		= 1	GPIO[24] is general purpose output
-4E	R/W	bits 7-0	GPIO[25] configuration (see -4D)
-4F	R/W	bits 7-0	GPIO[26] configuration (see -4D)

4.3.2 Operational Registers

Index	R/W Mode	Description		
-50	-	bits 7-0		optional off chip I/O register
-51	R/W	bits 7-0		GPIO[0:7] data
-52	R/W	bits 7-0		GPIO[8:15] data
-53	R/W	bits 7-0		GPIO[16:23] data
-54	R/W	bit 7	=1	enable GPIO[7] interrupt
		bit 6	=1	enable GPIO[6] interrupt
		bit 5	=1	enable GPIO[13] interrupt
		bit 4	=1	enable GPIO[12] interrupt
		bit 3	=1	enable GPIO[11] interrupt
		bit 2	=1	enable GPIO[10] interrupt
		bit 1	=1	enable GPIO[9] interrupt
		bit 0	=1	enable GPIO[8] interrupt
-55	R/W	bits 7-0	=0	the corresponding GPIO[8:12,5:7] pin set to interrupt on low level, see index -54 for bit mapping
-56	R	bits 7-0	=1	interrupt has occurred on the corresponding GPIO[8:13,6:7] pin, see index -54 for bit mapping
	W	bits 7-0	=0	clear interrupt for corresponding GPIO[8:13,6:7] pin
			=1	no effect
-57	R/W	bits 7-0		reserved
-58	R/W	bits 7-3		unused
		bits 2-0		GPIO[24:26] data
-59	R/W	bits 7-3		unused
		bits 2-0	=1	enable interrupts for the corresponding GPIO[24:26] pin
-5A	R/W	bits 7-3		unused
		bits 2-0	=0	the corresponding GPIO[24:26] pin set to interrupt on low level
			=1	the corresponding GPIO[24:26] pin set to interrupt on high level
-5B	R/W	bits 7-3		unused
	R	bits 2-0	=1	interrupt has occurred on the corresponding GPIO[24:26] pin
	W	bits 2-0	=0	clear interrupt for corresponding GPIO[24:26] pin
			=1	no effect

4.3.3 Programmable I/O Chip Select

Index	R/W Mode	Description		
-60	R/W	IOCS mask register LSB		
		bit 7	=0	A[7] ignored
		bit 6	=0	A[6] ignored
		bit 5	=0	A[5] ignored
		bit 4	=0	A[4] ignored
		bit 3	=0	A[3] ignored
		bit 2	=0	A[2] ignored
		bit 1	=0	A[1] ignored
		bit 0	=0	A[0] ignored
-61	R/W	IOCS mask register MSB		
		bit 7	=0	A[15] ignored
		bit 6	=0	A[14] ignored
		bit 5	=0	A[13] ignored
		bit 4	=0	A[12] ignored
		bit 3	=0	A[11] ignored
		bit 2	=0	A[10] ignored
		bit 1	=0	A[9] ignored
		bit 0	=0	A[8] ignored
-62	R/W	bits 7-0		IOCS match value LSB
-63	R/W	bits 7-0		IOCS match value MSB

4.4 Memory Configuration and Bank Switching

Index	R/W Mode	Description		
-80h	R/W	bit 7		unused
		bits 6-4	=111b	3-bit NRCE 1st half wait state value (default)
		bit 3		unused
		bits 2-0	=111b	3-bit NRCE 2nd half wait state value (default)
-81h	R/W	bit 7	=0b	512 cycles/8mS DRAM refresh rate (default)
		bits 6-2		unused
		bits 1-0	=11b	2-bit NRAS[3:0] wait state value (default)
-82h	R/W	bits 7-4	=1111b	4-bit NCS[1] wait state value (default)
		bits 3-0	=1111b	4-bit NCS[0] wait state value (default)
-83h	R/W	bits 7-4	unused	
		bits 3-0	=1111b	4-bit ISA wait state value (default)
-84h	R/W	bits 7-3		unused
		bits 2-0	=001b	Size of NRAS[0] RAM mapped into CPU address space
-85h	R/W	bits 7-3		unused
		bits 2-0	=001b	Size of NRAS[1:0] RAM mapped into CPU address space
-86h	R/W	bit 7		unused
		bit 6	=0	NCS[1] write disabled (default)
		bit 5	=0	NCS[0] write disabled (default)
		bit 4	=1	NRAS[3] write enabled (default)
		bit 3	=1	NRAS[2] write enabled (default)
		bit 2	=1	NRAS[1] write enabled (default)
		bit 1	=1	NRAS[0] write enabled (default)
		bit 0	=0	NRCE write disabled (default)
-87h	R/W	bits 7-0	=A0h	Write protect register (CPU address bits [19:12])

Index	R/W Mode	Description		
-88h	R/W	bits 7-0		Bank D0 frame select (device address bits [25:18])
-89h	R/W	bits 7-4		Bank D0 frame select (device address bits [17:14])
		bit 3	=0	Bank D0 not enabled (default)
		bits 2-0	=000 NRCE	Bank D0 device select code
			=001 NRAS[0]	
			=010 NRAS[1]	
			=011 NRAS[2]	
			=100 NRAS[3]	
			=101 NCS[0]	
			=110 NCS[1]	
			=111 unused	
-8Ah	R/W	bits 7-0		Bank D1 frame select (device address bits [25:18])
-8Bh	R/W	bits 7-4		Bank D1 frame select (device address bits [17:14])
		bit 3	=0	Bank D1 not enabled (default)
		bits 2-0		Bank D1 device select code (see -89h)
-8Ch	R/W	bits 7-0		Bank D2 frame select (device address bits [25:18])
-8Dh	R/W	bits 7-4		Bank D2 frame select (device address bits [17:14])
		bit 3	=0	Bank D2 not enabled (default)
		bits 2-0		Bank D2 device select code (see -89h)
-8Eh	R/W	bits 7-0		Bank D3 frame select (device address bits [25:18])
-8Fh		bits 7-4		Bank D3 frame select (device address bits [17:14])
		bit 3	=0	Bank D3 not enabled (default)
		bits 2-0		Bank D3 device select code (see -89h)
-90h	R/W	bits 7-0		Bank E0 frame select (device address bits [25:18])
-91h	R/W	bits 7-4		Bank E0 frame select (device address bits [17:14])
		bit 3	=0	Bank E0 not enabled (default)
		bits 2-0		Bank E0 device select code (see -89h)
-92h	R/W	bits 7-0		Bank E1 frame select (device address bits [25:18])
-93h	R/W	bits 7-4		Bank E1 frame select (device address bits [17:14])
		bit 3	=0	Bank E1 not enabled (default)
		bits 2-0		Bank E1 device select code (see -89h)
-94h	R/W	bits 7-0		Bank E2 frame select (device address bits [25:18])
-95h	R/W	bits 7-4		Bank E2 frame select (device address bits [17:14])
		bit 3	=0	Bank E2 not enabled (default)
		bits 2-0		Bank E2 device select code (see -89h)
-96h	R/W	bits 7-0		Bank E3 frame select (device address bits [25:18])

-97h	R/W	bits 7-4		Bank E3 frame select (device address bits [17:14])
		bit 3	=0	Bank E3 not enabled (default)
		bits 2-0		Bank E3 device select code (see -89h)
-98h	R/W	bits 7-0		Bank C frame select (device address bits [25:18])
-99h	R/W	bits 7-6		Bank C frame select (device address bits [17:16])
		bit 5		unused
		bit 4	=0	Bank C Attribute Memory Select
		bit 3	=0	Bank C not enabled (default)
		bits 2-0		Bank C device select code (see -89h)
-9Ah	R/W	bits 7-0		Disp Memory frame select (device address bits [25:18])
-9Bh	R/W	bits 7-4		Disp Memory frame select (device address bits [17:14])
		bit 3		unused
		bits 2-0		Disp Memory device select code (NRAS[3:0] only)
-9Ch	R/W	bits 7-0		Font Table frame select (device address bits [25:18])
-9Dh	R/W	bits 7-4		Font Table frame select (device address bits [17:14])
		bit 3		unused
		bits 2-0		Font Table device select code (see -89h)
-9Eh	R/W	bit 7	=0	Bank E3 Attribute Memory Select
		bit 6	=0	Bank E2 Attribute Memory Select
		bit 5	=0	Bank E1 Attribute Memory Select
		bit 4	=0	Bank E0 Attribute Memory Select
		bit 3	=0	Bank D3 Attribute Memory Select
		bit 2	=0	Bank D2 Attribute Memory Select
		bit 1	=0	Bank D1 Attribute Memory Select
		bit 0	=0	Bank D0 Attribute Memory Select
-9Fh	R/W	bits 7-0		unused
-A0h	R/W	bits 7-0		I/O Window 0 start address upper byte (I/O address bits [15:8])
-A1h	R/W	bits 7-0		I/O Window 0 start address lower byte (I/O address bits [7:0])
-A2h	R/W	bits 7-0		I/O Window 0 size register (must be power of 2)
-A3h	R/W	bits 7-5		unused
		bit 4	=0	Overlapping I/O-Address Window 0 not enabled (default)
		bit 3	=0	I/O Window 0 not enabled (default)
		bits 2-0	=101 NCS[0] =110 NCS[1]	I/O Window 0 device select code
-A4h	R/W	bits 7-0		I/O Window 1 start address upper byte (I/O address bits [15:8])

-A5h	R/W	bits 7-0		I/O Window 1 start address lower byte (I/O address bits [7:0])
-A6h	R/W	bits 7-0		I/O Window 1 size register (must be power of 2)
-A7h	R/W	bits 7-5		unused
		bit 4	=0	Overlapping I/O-Address Window 1 not enabled (default)
		bit 3	=0	I/O Window 1 not enabled (default)
		bits 2-0	=101 NCS[0]	I/O Window 1 device select code
			=110 NCS[1]	

CHAPTER 11
SERIAL COMMUNICATION

The serial communication portion of the HORNET IC contains both wired Serial and IR transmit and receive capabilities. The Serial UART port uses a 16450 cell to control transmit and receive. The IRO output port can be used for two types of communication, IR transmit and REDEYE. REDEYE is used to transmit data to an infrared REDEYE printer port. The IR communications portion uses both the IRO output to transmit and the IRI input pin to receive data. These ports are used for wireless communication using infrared light. The 16450 and the IR ports can be used simultaneously to implement a wireless infrared UART mode.

11.1 UART

The serial UART block is implemented using a 16450 compatible macro cell. A 1.84 MHz clock will be supplied for operation of this block. The UART is addressed from 3F8h to 3FFh. Serial drive and receive circuits are provided off chip.

The 1.84 MHz UART clock is available in operating and light sleep modes. The UART clock should be disabled to save power when the UART is not in use. This is done by setting the 16450 baud rate divisor to zero.

The UART supports the following data, control and status lines:

* Transmit Data
* Data Terminal Ready
* Request to Send
* Receive Data
* Data Set Ready
* Clear to Send
* Data Carrier Detect
* Ring Indicator

11.2 IR Communication

The IR communication block enables the HORNET IC to have wireless communication using an external infrared LED and IR receive circuit. The IR communication block supports 5 seperate communication formats. These formats are REDEYE, Software controlled communication, Modulated communication, IR UART with both single pulse and multiple pulse communication. To control the IR transmission of these formats, the hardware uses 2 control registers, the IRCNT register and the IRFMAT register. The IRFMAT register which is addressed at indexed -10h contains control bits that choose which format is chosen for IR communication. These bits are as follows:

Bit	Name	Description
0	RED	This bit when set activates REDEYE transmit mode. It turns on the REDEYE transmit hardware and sets it to a state where it is waiting for input from software.
1	MDLTE	This bit when set activates Modulated communication mode. It turns on the modulation source and allows the MDLD bit in the IRCNT register to control the output of a modulated waveform.
2	IRURT	This bit when set activates IR UART communication mode. This bit disconnects the 16450 from the Serial interface pins and connects it to the IR communication block. Software after setting the PMOD and MDSEL bits in this register, just transmits and receives using the 16450 as though it were connected to the Serial port. CTS, DSR and DCD inputs to the 16450 are held active and IR is held inactive in this mode. NOTE: Altering this bit can cause spurious UART interrupts if modem status interrupts are enabled in the UART at the time the bit is changed.
3	MDSEL	This bit is used to select the modulation source for both IR UART mode and Modulation communication mode. If this bit is 0, the 32kHz low frequency clock is chosen as the modulation source. If it is set to 1, the 16450 baud rate generator 16x clock is used for the modulation source. This allows the modulation source to be set a 38kHz to be remote control compatible.
4	PMOD	This bit is used in IR UART mode to select between single pulse transmission and multiple pulse transmittion. If it is set to 0, a single pulse of duration equal to a half cycle time of the modulation source will be transmitted for a 0 output bit. If it is set to 1, a pulse train of the modulation frequency will be used to transmit a 0.
5	LBF	Led Buffer Full. This bit is used in REDEYE mode to indicate that the contents of the LBR bit have not yet been transmitted and should not be written at this time. Writing to the LBR automatically sets this bit. This bit is cleared when the LBR is transferred to the REDEYE formatter.
6	ELBE	Enable Interrupt on LBR bit Empty (LBF clear). If this bit is set and LBF is clear, an IR interrupt will occur.
7	-	When set, this bit inverts the sense of the IR LED signal. Used to allow use of either inverting or non-inverting drivers for the LED.

The IRCNT register which is addressed at indexed -11h contains bits that are used to transmit a bit or waveform out on the IRO pad. The IRCNT register also allows software to receive IR data in any of the formats that can be transmitted. The contents are as follows:

Bit	Name	Description
0	LED	This bit is used to turn on the IR LED connected to the HPIRO pad. It is used for software controlled IR transmission. When it is set to a 1, the IR LED is turned on.

1	LBR	This bit contains the half-bit to be transmitted in REDEYE format. Write a one to send an "on" half-bit or write a zero to send an "off" half-bit.
2	MDLD	This bit is used for software to output a serial waveform to be modulated by the chosen modulation source. This allows compatibility with remote control format.
5	IRE	IR Event. This bit is set by a logic low voltage on the IRI pin. It is set to indicate that an IR event has occurred. Once set, software must reset this bit.
6	EIRI	Enable IR interrupt. An IR interrupt will occur if this bit and the IRE bit are both set.
7	IRI	IR Input pin. This bit allows software to monitor the state of the IRI pin. It is a read only bit.

Using the last three bits, software can receive each of the transmission formats described later. Also, if IR UART mode is set, software can receive data using the 16450 the same as it would in Serial mode.

11.2.1 REDEYE format

The REDEYE portion consists of the RED, LBF, and ELBE bits in the IRFMAT register, the LBR bit in the IRCNT register, the REDEYE formatter, and the IRO LED pin. The LED pin has an open drain device and thus may be driven low or tristated only. When driven low the drain current is somewhat regulated by a feedback circuit. The LBF and LBR bits form a double buffered handshake mechanism that allow automatic REDEYE half-bit formatting and pacing. An interrupt mechanism is provided to indicate completion of each half-bit.

The REDEYE printer requires 15-bit frames of a precise format. Each bit of the frame consists of two half-bits. The duration of each half-bit is 14 cycles of the 32768 kHz crystal oscillator. The half-bit is considered to be "on" if the LED is pulsed 6-8 times (out of the 14 possible) at the 32768 kHz rate. HORNET's REDEYE port uses 8 pulses. The format of a complete REDEYE frame is shown below:

Start-bits	Three half-bits "on-on-on".
Hamming-bits	Four pairs of half-bits.
Data-bits	Eight pairs of half-bits. Each of the four hamming and eight data bits are encoded with two half-bits. A "one" data or hamming bit is encoded by "on-off" and a zero is encoded by "off-on".
Stop-bits	Three half-bits "off-off-off". This is the minimum idle time required between frames.

The ELBE, RED, LBF, and LBR bits are cleared at reset. The REDEYE port also uses a formatter which is turned off whenever RED is cleared. Software initiates a half-bit transmission by writing a bit to LBR. This automatically sets the LBF flags in IRFMAT register and starts the state machine. The state machine transfers the bit from LBR into the formatter and clears LBF. If ELBE is set, this will cause an IR interrupt indicating that it is safe to write the next half-bit to LBR. The state machine then times the half-bit for 14 counts of the 32768 Hz crystal oscillator. If the bit

in the formatter is a one, the LED is pulsed for the first eight of the 14 counts. Otherwise the LED is left off. If after the 14 counts LBF is clear, the state machine will return to its idle state of waiting for LBF. Otherwise it will immediately transfer the next half-bit and start timing it.

When LBF is clear and ELBE is set, an IR interrupt will occur. When the state machine clears LBF, software has 13 counts of the oscillator to write the next bit to LBR. Otherwise the length of the half-bits will not be correct.

Through-put:
32768 /14 = 2340.6 baud (half-bits/sec)
32768 /28 = 1170.3 bps (bits/sec)
REDEYE Frame Length:
1.5 start + 4 Hamming + 8 data + 1.5 stop = 15 bits
REDEYE Thru-put:
1170.3 /15 = 78.02 cps

11.2.2 Software Controlled Mode

The LED bit in IRCNT register is provided for software generated IR formats. This bit is OR-ed with the output of the REDEYE formatter, and the other IR format outputs. Therefore, two IR formats may not be used simultaneously.

Due to LED current limitations, the LED output driver duty cycle must be limited to a time average of 29%. The duty cycle is automatically limited to 1/2 x 8/14 or 28.6% by the REDEYE formatter. The format of a full REDEYE frame yields a duty-cycle of only 14.3%. If a different format is used (by using the LED bit) software must limit the duty-cycle.

11.2.3 Modulated Mode

The MDLD bit in the IRCNT register can be used by software to output any custom modulated waveform desired. To output a waveform, software must first set the MDLTE bit in the IRFMAT register and choose the modulation source using the MDSEL bit. If the 16450 baud rate 16x clock is chosen, its frequency must be set to the desired modulation frequency. Once this has been accomplished, software can set and clear the MDLD bit at desired to emulate the envelope of the output waveform. Whenever MDLD is one, pulses will be output of a 50% duty cycle for the given modulation source. As before, care must be taken not to exceed the 29% communication duty cycle.

11.2.4 IR UART Modes

The 16450 may be used for half duplex IR communication of limited baud rate. To use this mode the IRURT bit must be set in the IRFMAT register. When this bit is set, the 16450 is disconnected from the Serial port and connected to the IR communication block. When using this mode, software must first choose the transmission format. The two possible formats are single pulse mode and multiple pulse mode. If the PMOD bit is 0, single pulse mode is chosen. In this mode, a single pulse of one half cycle of the modulation source is transmitted for a 0. In multiple pulse mode, a train of pulses of the modulation source is transmitted for a 0. In both modes, a 1 is transmitted as no pulses. As in Modulated mode, the modulation source again must be chosen. If the baud rate of 2400 baud is chosen, choosing the 16450 16x clock will give you a modulation rate of 38 kHz.

After this is set up, software can use the 16450 to communicate as though it were still connected to the Serial port.