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	HSDC			

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(EMD - III version)

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1 INTRODUCTION

1.1 Scope

This Engineering Product Specification (EPS) defines the High Speed Disk Controller (HSDC), which is a DPS-6 High Priority Megabus Interface (16 bit data bus and 24 bit address bus) Printed Circuit Assembly (PWA) with logic providing control over the Storage Module Drive (9.67 MHz. SMD-0 and 14.52 MHz. SMD-E) interface and connected either up to four Fixed Storage Drives (FSD's) or up to four Eight Inch Module Drives (EMD's). In addition the HSDC can connect to other devices (minidiskette or streamer tape) through unique adapters mountable on the HSDC.

The HSDC consists of one Printed Circuit Assembly (PWA) which can reside in any of the Megabus I/O positions as defined by the 1975 EPS# 60126298 and is also intended to be used on MRX systems on selectable basis.

1.2 Objective

To provide a subassembly enabling communication between a DPS-6 Megabus and the HSDC with associated peripherals. The subsystem consists of five parts:

- High Speed Disk Controller motherboard assembly
- Disk Drive(s) with interface cables
- Minidiskette and/or Streamer Tape adapters
- Interface cables for the above
- AC (FSD and EMD with power supply) and DC (Minidiskette and Streamer) power cables to the system Power Distribution Unit and DC power supply

Only the HSDC is described in this EPS with references to other documents describing the remaining components.

1.3 Documentation

1.3.1 Related documents

60126298, EPS-1, Level 6 Bus (Megabus)
60149832, EPS-1, MRX Megabus

60149778, PFS, High Speed Disk Controller
60166413, EPS, High Performance Disk Controller - Enhanced (HPDC_E)

60149612, EPS-1, L6 Quarter Daughter Board Subsystem Attachment

60149781, EPS, 1/4-Inch Larkette Streamer Adapter
60149988, EPS, Small Computer System Interface (SCSI) Adapters (WangTek)

64717900, MPI Rev.C, Product Specification for the 9715 Fixed Storage Drive, 160 MB with the SMD-0 Interface.

64400400, MPI Rev.A, Product Specification for the 9716 Fixed Storage Drive, 515 MB with SMD-E Interface.

64401200, MPI Rev.5, Product Specification for the 9720 Eight Inch Module Drive, 368 MB with SMD-E Interface.

64712402, MPI Rev.A, SMD-E Interface Specification For 15 MHz & 24 MHz Devices

1.3.2 Reference documents

Q4.1, PWA/PWB Testability Design Rules

MG1, Component Availability
MTG2, PWA Test Documentation Requirements
MTG4, PWA Test Monitor/Test Box Design
MTG5, PWA Quality Logic Test Creation
MTG6, PWA Test and Verification Program Creation
MTG7, PWA IC Socket Utilization
MTG8, Design for Producibility, Installability, Maintainability and Replaceability

MPDG1, PWA/PWB Producibility Guidelines

58035052, Worldwide Maintainance Requirements

1.4 Standards

1.4.1 General Design, Honeywell Bull Standards

B01.08, Environment, Operating
B01.09, Equipment Safety
B01.10, Environment, Transportation, Storage & Installation
B01.48, Primary Power-Utility Supplied

B03.07, Reliability - Standard Failure Rate Data Base
B03.08, Reliability Failure Rate & MTBF Predictions

B04.06, System Grounding

1.4.2 Product Maintainability, Honeywell Bull Standards

B07.11, Logic Nomenclature
B07.12, Location Reference Designation
B07.13, Identification Nomenclature for IC's, Printed Cards and Card Cages

B07.38, Logic Symbology
B07.39, Logic Block Diagrams

G02.01, FE Tools and Test Equipment Catalog
G02.05, FE Product Tools & Test Equipment

G07.01, Field Product Maintenance Documentation
G07.02, Product Manual Content Guide
G07.03, Product Style Guide for Manuals
G07.08, Major and Intermediate Block Diagrams
G07.09, Repair Documentation, Draft

1.4.3 Manufacturing Testability Guidelines

D.002.01, PWA/PWB Testability Design Rules
MTG1, PWA Test Equipment Connection Requirements
MTG3, PWA Microdiagnostic Creation
60129949, Application Rules for Minicomputer & Terminal Products

1.5 Definitions

CRC Cyclic Redundancy Check
CPU Central Processor Unit

DMA Direct Memory Access

EDAC Error Detection and Correction

HDA Head Assembly (Disk)
HSDC High Speed Disk Controller

LSA Larkette Streamer Adapter

MBZ Must be Zero

ORU Optimum Replaceable Unit

PWA Printed Wire Assembly

RPS Rotational Position Sensing, on SMD-E only.

QDM Quarter Daughter Board Diskette Adapter
QLT Quick Logic Test

SPM Scratch Pad Memory

RFU Reserved for Future Use

TCD Tape Cartridge Device
T&V Test and Verification

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2 ARCHITECTURE

2.1 Overview

The High Speed Disk Controller Subsystem (HSDCS), Figure 2.1, provides the Megabus systems with facility to store and retrieve data from mass storage media mounted on a disk drive. Up to four Disk Drives (FSD's or EMD's, not mixed types) can be cabled to one HSDC which can process one data transfer and several seek commands simultaneously. The HSDC interfaces with other devices through adapters mountable on the HSDC motherboard; all devices can function independently and interface asynchronously with the Megabus.

2.2 Major components

2.2.1 High Speed Disk Controller

The HSDC is a microprogrammed peripheral control unit which can interface up to four disks cabled via connectors mounted on the edge of the printed circuit board (PWB). The HSDC firmware is generalized to facilitate its application as a control element for other devices interfaced through Adapters. The HSDC performs the following functions:

- Execution of DPS-6 command sequences such as ACK, NAK, WAIT, etc...; status and control register storage in dedicated, per channel, random access memory accessible by both the HSDC and the CPU.
- Direct Memory Access (DMA) data transfer control with data buffer for intermediate storage.
- Multi-sector data transfers overlapping track and cylinder boundaries.
- SMD-0 and SMD-E interface dialog control with serial-parallel and parallel-serial data conversion and associated error detection and correction.
- Self-diagnostic, QLT, functions with an LED go/no-go indicator.
- Media defect handling using the prerecorded error logs on each track "home address" (first sector) and new error log recorded on the last cylinder; this cylinder is also used for reallocated error sectors.
- Adapter Interface for up to two additional channels.

o Direct disk to streamer and streamer to disk data transfers are <u>not</u> supported.

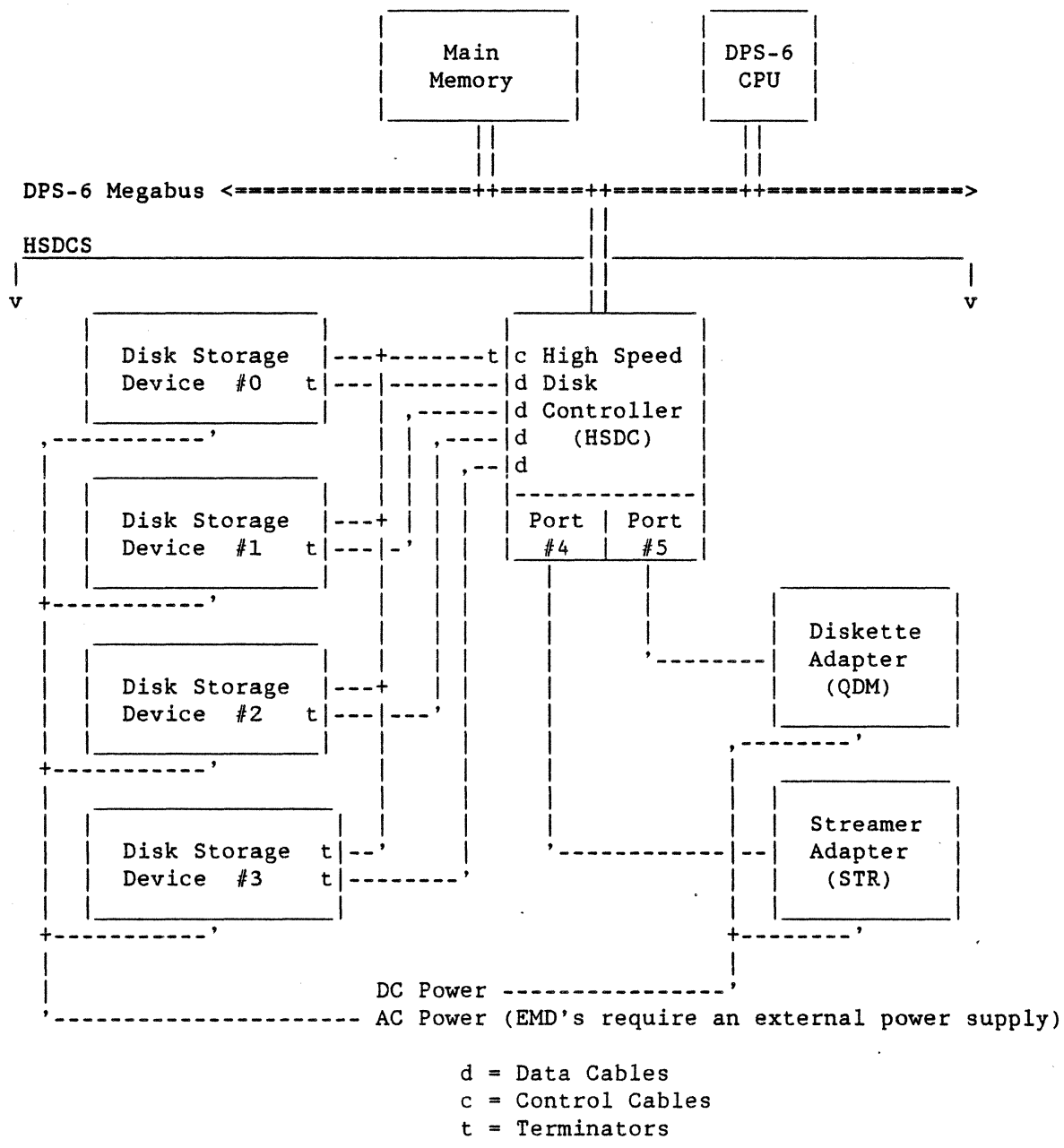


Figure 2-1 High Speed Disk Controller Subsystem

2.2.2 Fixed Storage Drive

The FSD is a small, random access, rotating 9.0" disk, mass memory device with rigid disk media storage and 9.67 MHz. SMD-0 or 14.52 MHz. SMD-E interface. Components of the FSD are: a box casting, integral switching type power supply, direct coupled DC brushless spindle drive motor with digital speed control brake, Disk Module with composite or thin film heads,logic package with read/write (phase-locked data separation and NRZ to 2,7 RLL code conversion), fault detection, transmitters, receiver and microprocessor controlled servo electronics. The Disk Module is an environmentally sealed unit containing the disks, heads, actuator, DC motor and air filter. Disk Logic Address is selectable by a plug on the front panel.

FSD Configurations:

- o 9615-515 414 MB formatted (516 MBytes unformatted)
- o 9615-160 132 MB formatted (166 MBytes unformatted)

Each FSD interfaces with the HSDC via two cables: one radial to each drive D (data) and one daisy-chainable C (command) cable; external termination is required on the last device on the C cable. Terminator is supplied with each device.

FSD Power:

Each drive requires AC power which can be internally set to the following nominal input voltage/frequency combinations:

100v through 120v @ 3.40 Amps in either 50 or 60Hz, nominal values
208v through 240v @ 2.10 Amps in either 50 or 60Hz, nominal values

2.2.3 Eight Inch Module Drive (EMD II & III)

The EMD is a small, random access, rotating 8.0" disk, mass memory device with rigid disk media storage and 14.52 MHz SMD-E interface. Components of the EMD are: a box casting, integral switching type power supply, closed loop positioner using a dedicated servo surface for both coarse and fine positioning activity, Disk Module which is an environmentally sealed unit containing the oxide disks, thin film heads, balanced rotary actuator, brushless DC motor and air filter. CMOS and ECL technology with extensive use of LSI in all functions logic package, read/write (phase-locked data separation and NRZ to 2,7 RLL code conversion), fault detection, transmitters, receiver and microprocessor controlled servo electronics. The Disk Logic Address is selectable by a plug on the front panel.

FMD Configurations:

- o 9720-368 295 MB formatted (368 MBytes unformatted)
- o 9720-741 595 MB formatted (741 MBytes unformatted)

Each EMD interfaces with the HSDC via two cables: one radial to each drive D (data) and one daisy-chainable C (command) cable; external termination is required on the last device on the C cable. Terminator is supplied with each device.

Each EMD drive (DC power required, only) with separate power supply requires AC power which can be internally set to the following nominal input voltage/frequency combinations:

100v through 120v @ 2.20 Amps in either 50 or 60Hz, nominal values
208v through 240v @ 1.30 Amps in either 50 or 60Hz, nominal values

2.2.4 Minidiskette Adapter, QDM

The Quarter Daughter Board Diskette Adapter (QDM), reference EPS-1 #60149612, provides an interface to the 5 1/4 inch minidiskette. The HSDC emulates the MDC III (BDC8) firmware in controlling one minidiskette device attached to the QDM. Adapter functions are as follows:

- Performs device interface dialog control and data recovery and transmission.
- Address Mark generation and detection.
- Control of Seek and Seek overlap; multi-sector data transfers overlapping track and cylinder boundries.
- CRC generation and verification.
- Device status monitoring.

Minidiskette Power.

Minidiskette device requires DC power from the system power supply at +5v. and +12v, nominal.

2.2.5 Streamer Adapter

The Streamer Adapter (STR) quarter sized daughter board is a microprogrammed peripheral control unit that can interface with one Tape Cartridge Device (TCD) cabled via a connector mounted on the STR printed circuit board. On one side, the STR, provides an interface to the common MDC-4 internal bus and on the other it controls access to the TCD. The STR contains the following functionality:

- Device interface dialog control
- Device read/write data buffers control; one 16 K byte buffer on the adapter and one disk track buffer on the HSDC.
- STR to HSDC, MDC-4 interface control

TCD Power.

The TCD requires DC power from the system power supply. Frame ground and signal grounds are isolated in the TCD and are brought out separately to an external, system level, tie point. The following DC voltages are required: +5v., +12v. and -12v..

3 FUNCTIONAL REQUIREMENTS

3.1 Configuration and Simultaneity

Devices attached to the HSDC are software addressable via channel numbers. Each individual device has two channel numbers assigned, differing from each other only in the low order bit value (the direction bit). When an IOLD instruction is issued to the HSDC, the direction bit of the output address channel number specifies whether it is going to be an input or an output data transfer; for all other commands, the direction bit is ignored. Bits 8 through 13 (reference figure 3-1) are assigned at system installation and must conform to constraints defined in the Megabus EPS-1. Software visibility of the devices attached to the HSDC is such that the devices are independent of each other; except that initiation of a command sequence addressed to one device may be stalled while the HSDC is busy servicing another device.

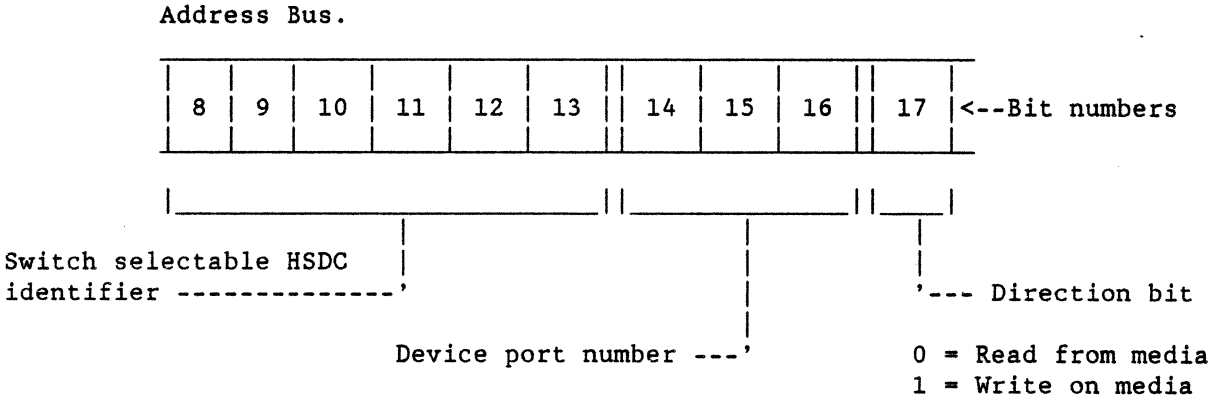
The HSDC provides a single level of simultaneity (only one data transfer can be active in the subsystem) and supports the following:

- A not busy channel must accept instructions directed to it over the Megabus even though a data transfer may be active over another channel. An instruction may be "waited" for a period not exceeding 100 microseconds; longer delays can affect performance of the entire system.
- Any seek orders received during a data transfer must be initiated prior to the start of any another data transfer.
- Channels are serviced on an alternating priority basis so that no channel can dominate controller usage.
- Controller accepts a data read/write command to channel B while channel A is in the process of moving data but does not initiate a data transfer on B until A's data transfer is complete
- If the HSDC is configured with less then six devices, it responds to channel numbers associated with the installed devices only.

3.2 Megabus Control

3.2.1 Command Transfer

The HSDC recognizes a command transfer request on the Megabus when a valid channel number is decoded in bits 8 through 17 of the address bus. If the addressed



Device assignments:

Disk #0	=	Channel n
Disk #1	=	" n + 080
Disk #2	=	" n + 100
Disk #3	=	" n + 180
Streamer Adapter	=	" n + 200
Diskette Adapter	=	" n + 280

Figure 3-1 Channel Numbers.

channel is not busy, the contents of the data and address buses are stored in the HSDC interface hardware and the HSDC issues an ACK to the CPU to complete the bus cycle; now the HSDC can process the information contained in the registers. If the addressed channel is busy executing a previously received command, the HSDC completes the bus cycle by issuing a NAK (except for the Output Control Word command; reference section 5.). If, however, the HSDC is temporarily busy, processing a not interruptible function, it completes the bus cycle with a WAIT response which must be followed by either an ACK or a NAK response when the function in process terminates. WAIT response must be as short as possible ($\leq$ 100us.) to avoid performance degradation and if too long system hardware or software timeout may occur (1ms on 6/9X CPU's).

3.2.2 Data Transfer

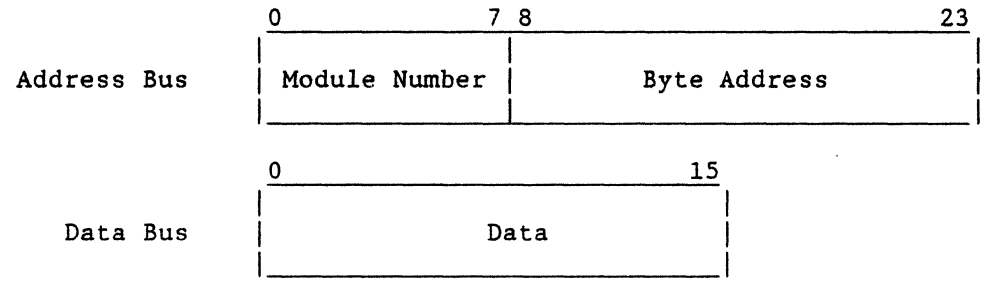
All data transfers associated with the HSDC are executed in Direct Memory Access (DMA) mode; transfers are normally word wide but byte wide operation may occur on the first and/or last memory cycle of a particular data transfer if the memory buffer begins or ends on an odd byte boundary.

If, during memory read/write request cycle on the Megabus, a NAK response is received at the HSDC, data transfer is aborted with a nonexistent resource error posted in Status Word 1 (reference section 5.). A WAIT response to a memory read/write request cycle results in the HSDC retry of the Megabus request cycle; retries continue until an ACK or a NAK response is received. While either this Megabus cycle or the second half read cycle is pending in the HSDC

interface it is not accessible to the CPU including the Output Control Word command. Once the HSDC is conditioned to do a memory access all other Megabus cycles addressed to the HSDC are completed with either a NAK or a WAIT until the memory reference is terminated.

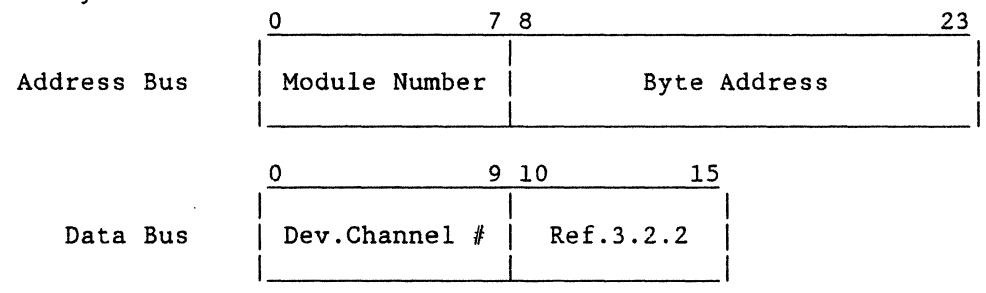
Memory read and write data accesses are illustrated in figure 3-2. During the memory read request cycles, bits 10 through 15 of the data bus may contain an address of a register in the HSDC into which the returned memory data is delivered. Memory responds in the second half of the read cycle by placing on the address bus, bits 8 through 23, the contents of the entire data bus as received, by the memory, during the request cycle.

HSDC Memory Write Request



HSDC Memory Read Request

Request Cycle.



Response Cycle.

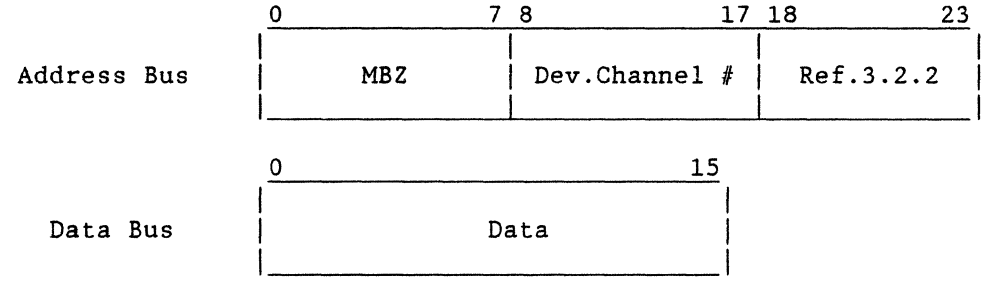


Figure 3-2 Address and Data Bus Configuration for Read and Write Memory Access.

3.2.3 Interrupts

Whenever the channel interrupt level is not zero, either an operation initiated by an Output Task Word or an Output Control Word command is completed or the attention bit in the Status Word 1 is set, an interrupt on the Megabus is attempted. If a NAK response is received to an interrupt request, the HSDC saves the interrupt status until it detects the BSRINT pulse on the Megabus; interrupt is then retried. When an interrupt is saved the channel with the pending interrupt is busy and does not accept commands (except Output Control Word), however, other channels on the HSDC are free to function normally.

Channel zero interrupt level (initialized or set to zero) inhibits Megabus interrupts for that channel. If a condition or an event occurs which would normally cause an interrupt, the appropriate bits in a status word are set but no interrupt is attempted on the Megabus nor is the interrupt request saved; specifically, interrupts that would be generated as a result of either Output Control Word Initialize or Master Clear.

Address and data bus configuration for interrupt sequences is illustrated in Figure 3-3. The channel number supplied on the data bus during an interrupt is the one used in the most recent Output Address instruction to that HSDC channel; if the instruction has not been received the low order bit of the channel number is zero.

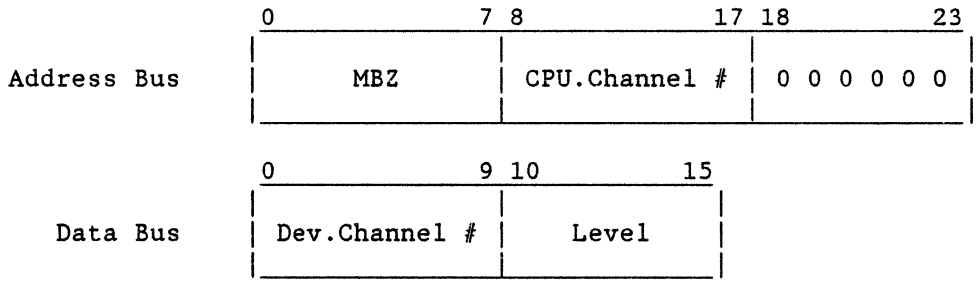


Figure 3-3 Address and Data Bus Configuration for Interrupt Sequences

3.3 Overview of HSDC Access

Associated with each channel is a set of registers which are loaded by software and specify parameters required for attached device operation. In addition to the range and the address registers, used for DMA operation, there are configuration registers which contain record location and identification information and a task register for command codes. To perform a specific operation software first loads the address, range and configuration registers. The task register is loaded last with a command to be performed which also triggers the HSDC channel operation. Commands addressed to a not busy channel are always accepted, but execution may be delayed because another channel is in the process of data transfer. All commands addressed to a busy channel are rejected (NAK response) except Output Control Word.

3.3.1 Memory Addressability

The Megabus interface is 16 bits wide for the data path and 24 bits wide for the address path with provision for the MRX Z01, Z02 and Z03 connectors and its impedance matching components. Memory burst mode of operation is not included in the HSDC design.

3.3.2 Scatter/Gather

The Scatter/Gather DMA data transfer is not supported by the HSDC in either hardware or firmware.

3.3.3 Dual Ported Drives

The Dual Ported FSD's or EMD's are not supported, presently. However, hardware to provide for dual ported devices is incorporated in the design except (lock/unlock) firmware to control these is not in place. FSD's and EMD's require an additional PWA in their controllers to accommodate this functionality; only EMD III is purchased as a dual ported device.

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4 INTERFACES

No specific user action is required to load or initialize the HSDC other than during subsystem installation and subsystem configuration identification. Actions required to load/unload removable media devices (minidiskette or tape cartridge) are described in an appropriate EPS; see references in 1.3.1.

4.1 HSDC to Megabus Interface

The HSDC attaches to the Megabus as a standard DPS-6 (see Megabus EPS-1) controller with provision for the MRX Z01, Z02 and Z03 connectors and their impedance matching components.

4.2 Device Level Interface (DLI)

Refer to the FSD and EMD specifications for information more detailed than that presented in this section which is concerned with the physical interface only. The FSD and EMD specifications (references section 1.3.1) also represents the governing document for device functionalities.

Disk Devices require two cables for attachment to the HSDC. The "A" cable provides the daisy chain linkage between all drives on the DLI while the "B" cable provides a radial connection from each drive to the HSDC. Figure 4-1 shows signals present on each cable. Address and control functions are transferred on ten lines. The significance of the information on these lines is indicated by the three tag lines (refer to figure 4-2).

4.2.1 Address and Control Functions ("A" cable)

Three tag lines are used to send information to all connected drives on the "A" cable; only the selected drive responds to the encoded information. The ten control lines are strobed by the individual tag lines when the control data is valid.

4.2.1.1 Low Cylinder Address (Tag 1)

The SMD-E is a direct cylinder addressing interface which only needs the new cylinder address on the control lines and strobe Tag 1. The drive must be "On Cylinder" before Tag 1 is issued. To provide for more cylinder addressing than the ten tag lines permit two additional bits are available within Tag 2, reference figure

HSDC	"A" CABLE	DRIVE LO	DRIVE HI
	------- Unit Select Tag ---------->	22	52
	------- Unit Select 2^0 ---------->	23	53
	------- Unit Select 2^1 ---------->	24	54
	------- Unit Select 2^2 ---------->	26	56
	------- Unit Select 2^3/Tag 5-* ------->	27	57
	------- Tag 1-* ---------->	1	31
	------- Tag 2-* ---------->	2	32
	------- Tag 3-* ---------->	3	33
	------- Bus Out-Bit 0-* ---------->	4	34
	------- Bus Out-Bit 1-* ---------->	5	35
	------- Bus Out-Bit 2-* ---------->	6	36
	------- Bus Out-Bit 3-* ---------->	7	37
	------- Bus Out-Bit 4-* ---------->	8	38
	------- Bus Out-Bit 5-* ---------->	9	39
	------- Bus.Out-Bit 6-* ---------->	10	40
	------- Bus Out-Bit 7-* ---------->	11	41
	------- Bus Out-Bit 8-* ---------->	12	42
	------- Bus Out-Bit 9-* ---------->	13	43
	------- Open Cable Detector ---------->	14	44
	<------ Bus In-Bit 0-* ----------	19	49
	<------ Bus In-Bit 1-* ----------	17	47
	<------ Bus In-Bit 2-* ----------	16	46
	<------ Bus In-Bit 3-* ----------	15	45
	<------ Bus In-Bit 4-* ----------	28	58
	<------ Bus In-Bit 5-* ----------	20	50
	<------ Bus In-Bit 6-* ----------	18	48
	<------ Bus In-Bit 7-* ----------	25	55
	------- Power Sequence Pick(Power On)->		29
	------- Power Sequence Hold(Power On)->		59
A	<------ Busy-*-# ----------	21	51
CONNECTOR	------- Tag 4-(Ground on SMD-0) ------>	30	60

	"B" CABLE	LO	HI
	--------Write Data---------->	8	20
	--------Ground----------	7	
	--------Write Clock---------->	6	19
	--------Ground----------	18	
	<-------Servo Clock----------	2	14
	--------Ground----------	1	
	<-------Read Data----------	3	16
	--------Ground----------	15	
	<-------Read Clock----------	5	17
	--------Ground----------	4	
	<-------Seek End----------	10	23
	<-------Unit Selected----------	22	9
	--------Ground----------	21	
	--------Reserved for Index----------	12	24
	--------Ground----------	11	
	--------Reserved for Sector----------	13	26
B	--------Ground----------	25	
CONNECTOR	* Gated by Unit Selected	CONNECTOR	
	# Dual channel units only		

Figure 4-1 "A" & "B" Interface Cables

4-2. The High Order Cylinder Address bits (2^{10} and 2^{11}, Tag 2) must be set before Tag 1 since carriage motion begins with Tag 1. Valid Head Select Address must be sent with each Tag 2 to prevent Head Select Fault.

4.2.1.2 Head and High Cylinder Select (Tag 2)

The control lines 0 through 4 and 7 through 8 determine the Head Address and High Order Cylinder Address respectively together with the Tag 2 strobe.

4.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation.

4.2.1.3.1 Write Gate (Bus Out Bit 0)

The Write Gate line enables the Write Data driver circuit during a Write operation.

4.2.1.3.2 Read Gate (Bus Out Bit 1)

The Read Gate line enables the digital Read Data transmission lines.

4.2.1.3.3 Servo Offset Plus (Bus Out Bit 2)

When this signal is true, the actuator is offset from the nominal "On Cylinder" (the "On Cylinder" signal becomes not true for 2.75 ms, approximately) position towards the spindle. Write gate must not be made true by the HSDC while in the Offset mode. The time for the carriage to move + to - or - to + offset is 4 ms.

4.2.1.3.4 Servo Offset Minus (Bus Out Bit 3)

When this signal is true, the actuator is offset from the nominal "On Cylinder" (the "ON Cylinder" signal becomes not true for 2.75 ms, approximately) position away from the spindle. Write gate must not be made true by the HSDC while in the Offset mode. The "ON Cylinder" signal goes false for 2.75 ms. after the offset + or - goes false.

4.2.1.3.5 Fault Clear (Bus Out Bit 4)

A 100 ns (minimum) pulse sent to a selected device clears the fault flip-flop if the fault condition no longer exists. A Seek Error is cleared by a Return-to-zero.

4.2.1.3.6 Address Mark Enable (Bus Out Bit 5)

The address Mark (AM) Enable signal, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks:

- When AM Enable is true together with Write Gate, the writer stops toggling and erases the data creating an AM. The HSDC ensures that the written AM is greater than 22 bits and less then 32 bits in length. Write Fault detection is inhibited by the AM Enable signal.

- When AM Enable is true together with Read Gate, an analog voltage comparator detects the absence of a Read signal. If the duration of the erased area on the medium is 3 bytes long, an AM Found signal is asserted.

- If AM is not used , Bit 5 must be held inactive during Control Select (Tag 3) functions. AM must be three bytes long with no transitions.

4.2.1.3.7 Return To Zero (Bus Out Bit 6)

A 500 ns to 1 ms pulse sent to the device causes the actuator to seek track zero and reset both the head register and Seek Error flip-flop. This seek is significantly longer (1 second, maximum) than normal seek to track zero and should only be used for recalibration, not data aquisition.

4.2.1.3.8 Data Strobe Early (Bus Out Bit 7)

When this signal is true, the drive Phase Locked Oscillator (PLO) data separator strobes the data at a time earlier than nominal; when false nominal timing is returned.

4.2.1.3.9 Data Strobe Late (Bus Out Bit 8)

When this signal is true, the drive PLO data separator strobes the data at a time later than nominal; when false nominal timing is returned.

4.2.1.3.10 Release, Dual Channel only (Bus Out Bit 9)

Enabling this signal releases Channel Reserve and Channel Priority Select Reserve in the device making alternate channel access possible after selection by the other channel ceases. Reference the Interface specification for more details, 1.3.1.

4.2.1.3.11 Unit Select

Priority Select, Dual Channel only (Bus Out Bit 9 and Unit Select Tag)

When this signal is true during Unit Select Tag (strobe) the device is unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Reference the Interface specification for more details, 1.3.1.

4.2.1.4 EMD/SMD-E Extended Drive Dependent Status

The EMD provides the following extended functions (Figore 4-4) when in the SMD-E mode, reference the interface specification for timing considerations:

4.2.1.5 Current Sector Status (Tag 4)

Tag 4 allows the current sector address (4 - 128) to be transmitted to the HSDC on BUS IN lines bit - 0 through bit - 7. The sector counter is free running and the count is valid 200ns, maximum, after the leading edge of the Sector or the Index pulse.

4.2.1.6 Device Extended Status (Tag 5)

Tag 5 in conjunction with BUS OUT bits 0 and 1 allows the Fault Status, Operating Status, Diagnostic Status or Execute Command/Status to be presented over the BUS IN lines.

4.2.1.6.1 Fault Status

When all the BUS OUT bits are equal to zero and Tag 5 equals to one, the following fault status is available:

Read and Write fault, BUS IN Bit 0

When true, this bit indicates that Read and Write conditions existed simultaneously.

Read or Write and Off Cylinder, BUS IN Bit 1

When true, this bit indicates that a Read or a Write condition existed during a Seek (Off Cylinder) condition.

First Seek fault, BUS IN Bit 2

When true, this bit indicates that the drive has failed a first seek/load attempt.

Write fault, BUS IN Bit 3

When true, this bit indicates that a write fault has occurred.

Write and Write Protected, BUS IN Bit 4

When true, this bit indicates that a write function was attempted while the drive is in a write protected condition.

Head Select fault, BUS IN Bit 5

When true, this bit indicates that no heads are selected or that multiple heads are selected.

Voltage fault, BUS IN Bit 6

When true, this bit indicates a below normal voltage exists within the drive.

Valid status, BUS IN Bit 7

When true, this bit indicates that a valid fault status exists on BUS IN Bits 0 through 6.

4.2.1.6.2 Operating Status

When BUS OUT bit 0 = 1 and bit 1 = 0, all others are equal to zero, and Tag 5 equals to one, the following operating status, in BUS IN Bits 0 through 7, is available:

Valid status, BUS IN Bit 7

When true, this bit indicates that a valid operating status exists on BUS IN Bits 0 through 6.

Interface Status Code	Diagnostic Display Code	Status Description
00	00	Ready and On Cylinder
01	01	Carriage parked
02	02	Motor stopping
03	03	Motor stopped
04	04	First load/calbrate
05	05	Sequence delay
06	06	Waiting for, hold + local
07	07	Starting motor
08	08	Motor up to speed
46	46	Seek timeout
4B	4B	Off-track seek error
4D	4D	Illegal cylinder address
4F	4F	Seek error on settle-in
50	50	Low Vcc glitch
51	51	Control MPU reset
54	54	First seek fault on retract
55	55	First seek fault on load
56	56	First seek fault on RTZ
57	57	First seek fault on Calibrate
58	58	Speed loss
59	59	Motor can not start
5A	5A	Emergency retract
60	60	Motor MPU failure
61	61	Servo MPU failure

4.2.1.6.3 Diagnostic Status

When BUS OUT bit 0 = 0 and bit 1 = 1, all others are equal to zero, and Tag 5 equals to one, the following diagnostic status, in BUS IN Bits 0 through 7, is available:

Valid status, BUS IN Bit 7

When true, this bit indicates that a valid diagnostic status exists on BUS IN Bits 0 through 6 for the one most likely Field Replaceable Unit (FRU).

Status	FRU
01	Control board
02	Module, HDA
03	Power supply
04	I/O board
05	Read/Write board
06	Carriage lock electromagnet
07	Cooling fan
08	Status/Control panel
09	Not used
0A	Not used
0B	Not used

4.2.1.6.4 Execute Status

When BUS OUT bit 0 = 1 and bit 1 = 1, all others are equal to zero, and Tag 5 equals to one, the following execution status, in BUS IN Bits 0 through 7, is transmitted to the HSDC:

Valid status, BUS IN Bit 7

When true, this bit indicates that the diagnostic test has began and that BUS IN Bits 0 through 6 are all zero.

4.2.1.7 Device Type Status (Tag 6)

The logical AND of Tag 4 AND Tag 5 (Tag 4 before Tag 5, for timing reasons) causes the device type status to be transmitted to the HSDC. These status BUS IN Bits 0 through 7 may be configured by the user.

4.2.1.8 SMD Status Lines

The following paragraphs define Bus In Bit lines and individual status lines as they appear during normal, non-extended, SMD functions. Extended SMD functions are those in which Tag 4 and/or Tag 5 have control of the Bus In Bit lines.

4.2.1.8.1 Unit Ready (Bus In Bit 0)

When true, this signal indicates that the device is up to speed, the heads are loaded and a fault condition does not exist. First seek fault is indicated if, during a load sequence, servo bits are not sensed.

Bus Out Bit	Tag 1 Low Cyl. Address	Tag 2 Head Sel+ High Cyl. Address	Tag 3 Control Select	Unit Select Tag
		H.S.		
0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	+ Servo Offset	
3	2^3	2^3	- Servo Offset	
4	2^4	2^4	Fault Clear	
5	2^5	H.C.A.	AM Enable	
6	2^6		Return To Zero	
7	2^7	* 2^{10}	Data Strobe Early	
8	2^8	* 2^{11}	Data Strobe Late	
9	2^9		Release **	Priority Select **

Bus In Bit	Drive Status
0	Unit Ready
1	On Cylinder
2	Seek Error
3	Fault
4	Write Protect
5	Address Mark
6	Index Mark
7	Sector Mark

* Cylinder numbers above 1024 ** Dual Channel Only.

Figure 4-2 Tag and Control Lines.

4.2.1.8.2 On Cylinder (Bus In Bit 1)

Status signal indicates, when true, that the servo has positioned the heads over a track successfully. This status line is cleared by any seek instruction causing carriage movement or a zero track seek. A carriage Offset results in the loss of On Cylinder for a nominal 2.75 ms.

4.2.1.8.3 Seek Error (Bus In Bit 2)

This signal indicates that the device is unable to complete a move or that the carriage has moved to a position outside of the recording field or that an address greater than the maximum number of tracks available on the device has been selected. Return To Zero command clears this error and returns the heads to track zero with On Cylinder true.

4.2.1.8.4 Fault (Bus In Bit 3)

When this signal is true a fault condition exists in the device. Conditions that set this line true are:

- o First seek load error.
- o One of the DC voltages is out of limits.
- o Read or Write with "ON Cylinder" signal false.
- o When Write Gate is active:
  - Low or not present Write current.
  - Write Protected.
  - Head circuit open (Bad head).
  - Absence of write data.
  - Invalid head address.
  - Absence of write clock when the Write Gate is activated.
- o Multiple heads selected.
- o Read and Write Gates active simultaneously.

The fault signal can be cleared by either the Clear Fault command or by depressing the Fault Clear Switch on the device operator panel providing the fault condition no longer exists.

4.2.1.8.5 Write Protect (Bus In Bit 4)

Enabling the Write Protect signal, by a front panel switch, inhibits the writer circuit under all conditions, illuminates the front panel indicator and sends the Write Protect signal to the HSDC. Attempting to write while in this state results in a Fault signal.

4.2.1.8.6 Address Mark Found (Bus In Bit 5)

Address Mark Found is a 6 us pulse sent to the controller following recognition of at least 22 but less than 32 missing transitions and the first zero of the zeros pattern. Upon receipt of that signal the HSDC drops the Address Mark Enable (Bit 9) signal and valid data is presented on the I/O lines. False Address Mark Found processing must be provided in the HSDC or the software driver; however, if fixed sector format is selected this problem can be avoided since Address Mark Enable and Address Mark Found signals are not used.

4.2.1.8.7 Index Mark (Bus In Bit 6)

Leading edge of sector zero, on each track, occurs once per revolution; marked by a pulse 2.5 us long, nominal.

4.2.1.8.8 Sector Mark (Bus In Bit 7)

The Sector Mark is derived from the servo track and the number of sectors per track is switch selectable in the device; for the FSD 9616 and EMD 9720 the number should be 96 and for the FSD 9615 the number should be 64.

4.2.1.9 Unit Select Tag

The device is selected 600 ns after the leading edge of the Unit Select Tag which gates the Unit Select lines to the logic number compare circuit. The device is deselected 600 ns after the trailing edge of the Unit Select Tag. Both actions are edge triggered.

4.2.1.10 Unit Select Bits, 2^0, 2^1, 2^2 & 2^3

These four signals are binary coded to select the logic unit number for one of sixteen drives. The unit number, 0 through 15, is selectable by means of a logic plug or switch in each drive; care must be taken not to duplicate logic numbers in the subsystem.

4.2.1.11 Open Cable Detect

The signal, when true, disables the interface in the event that the "A" interface cable is disconnected or the controller power is lost. Reference the Interface specification for further design details, 1.3.1.

4.2.1.12 Power Sequencing (Power On)

Power sequencing requires the AC power On, Start Indicator and switch On and the Remote Sequence switch to be in the Remote position. The HSDC provides the ground return to the Sequence Pick In and the Sequence Hold signals to cause connected drives to begin to power up in order starting with the device closest to the HSDC. Drivers on these lines must be able to sink 11 ma per device.

4.2.1.13 Busy, Dual Channel Only

If the device is already reserved and/or selected, Busy signal is issued, within 600 ns, to the "A" cable and Unit Selected is issued on the "B" cable to the channel attempting to select. This signal is reset by either when the Unit Select Tag is dropped or the device is no longer Busy; Unit Select should be used to enable Busy in the HSDC.

4.2.2 Data and Clock Lines ("B" cable)

4.2.2.1 Unit Selected

When four Unit Select Bits compare with the drive address on the leading edge of the Unit Select Tag signal, the Unit Selected signal is sent to the HSDC on the "B" cable.

4.2.2.2 Seek End

Seek End is a combination signal of On Cylinder or Seek Error indicating that a seek operation has terminated. Seek End and On Cylinder signals pulse for 30 us, nominal, when an address greater than the device can accommodate is received. In dual channel devices, the Seek End signal sent to the unselected channel is normally constant true. However, while the device is selected on a channel and the opposite receives a Select, this action is remembered within the device. When the selected channel's Select and Reserve latches are cleared, the Seek End signal for the waiting channel goes false for 30 us.

4.2.2.3 Write Data

This signal carries NRZ data, synchronized with the Servo Clock at the HSDC, which is to be recorded on the selected disk drive.

4.2.2.4 Servo Clock

The Servo Clock is a phase-locked 14.52 MHz clock on the SMD-E or 9.67 MHz on the SMD-0 generated from the servo track bits; it is available at all times.

4.2.2.5 Read Data

Recovered NRZ data is transmitted on this line from the device to the HSDC.

4.2.2.6 Read Clock

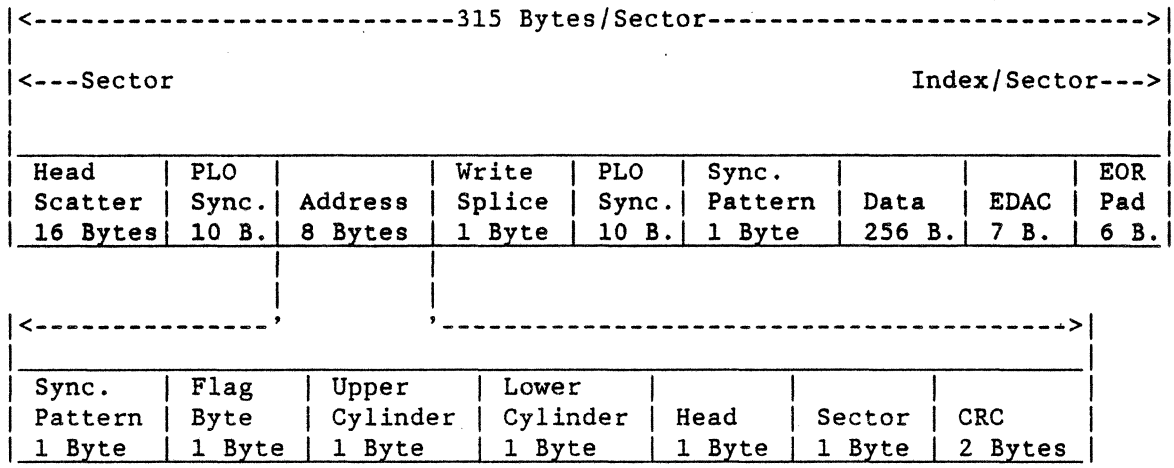
The Read Clock defines the data cell; it is transmitted continuously and is in phase synchronizm with Read Data within 5 us after Read Gate.

4.2.2.7 Write Clock

This signal transmits the Write Clock which is synchronized to the NRZ Write Data in the HSDC. The Write Clock is the Servo Clock retransmitted to the device by the HSDC during a write operation; it need not be transmitted continuously but it must be present at least 250 ns before the Write Gate.

4.2.3 Data Format

Fixed sector format is used by the HSDC which defines 96 equal sectors per track for the 414 MB FSD and the 295 MB EMD and 64 equal sectors per track for the 132 MB FSD. However, because a list of defects occupies the space reserved for the first sector (home address) only 95 or 63 sectors are available for user space. Reference Figure 4-3 for details.



Efficiency $\frac{256 * 95}{30,240} = 80.4\%$ for 414 MB FSD and 295 MB EMD.

$\frac{256 * 63}{20,160} = 80\ \%$ for 132 MB FSD.

Head Scatter & Skew = 16 Bytes of Zeros

PLO Synchronization = 6 us of Zeros, minimum

Synchronization Pattern = #19

Write Driver Turn On = 552 ns (within the Write Splice byte)

Figure 4-3 Fixed Sector Format.

4.3 EMD Options

I/O card selections, reference the device specification for more details:

Switch	Open	Closed
Local/Remote disk spin up mode	Remote	--
SMD-0/SMD-E interface	SMD-E	--
Normal/Extended cylinder address	Extended	--
Index and sector select	1A, 1B	--

Switch		Open	Closed
Channel disable		--	2A, 2B
Tag 2/Tag 1		Tag 2	--
Ready/Power OK		Ready	--
Absolute Reserve/Reserve timer		Abs.Res.	--
Device ID	Sw 0	--	Closed
	Sw 1	--	Closed
	Sw 2	Open	--
	Sw 3	Open	--
	Sw 4	Open	--
	Sw 5	Open	--
	Sw 6	Open	--
	Sw 7	Open	--

Control card selections:

Switch		Open	Closed
Set clock select 0.8/1.6		0.8	--
Write Protect/Normal		--	Normal
Sector select (Set to 96)	Sw 0	--	Closed
	Sw 1	--	Closed
	Sw 2	Open	--
	Sw 3	--	Closed
	Sw 4	Open	--
	Sw 5	Open	--
	Sw 6	Open	--
	Sw 7	--	Closed
	Sw 8	Open	--
	Sw 9	Open	--
	Sw 10	Open	--
	Sw 11	Open	--
Unit select (Logical Add)	Sw 0	--	Closed
	Sw 1	--	Closed
	Sw 2	--	Closed
	Sw 3	--	Closed

Jumper	Name	Configuration
6430-6431	WE Delay	Jumpered
B167-168	EM Control	Jumpered
B446-546	EM Servo	Jumpered
J061-161	2-7 Data	Jumpered

Blank

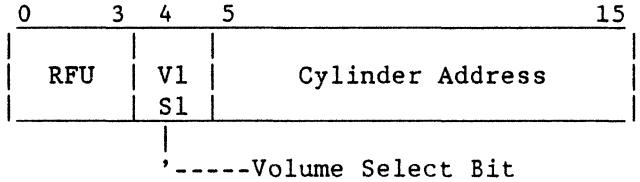
5 INSTRUCTIONS

5.1 General

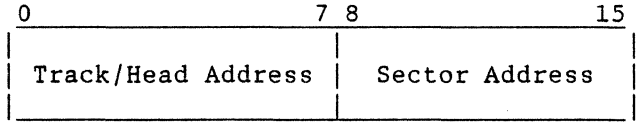
Two configuration words are required to define data access on a disk device. Configuration Words A and B contain the image of the ID field of the sector on which a particular operation is initiated. Data access is defined via four hierarchical elements split between the two Configuration Words. In order to provide for the potential growth of disk type devices, the following guidelines are established for the distribution of the four elements in the two Configuration Words.

- Bits 0 through 4 of Configuration Word A are reserved for use as a magazine address. Magazine selection applies to a device which has more than one physically identifiable media. For example, a cartridge disk device may have a fixed media and a removable media. These bits may also be used to indicate track condition and/or sector size.
- Bits 5 through 15 of Configuration Word A are reserved for use as a cylinder address.
- Bits 0 through 7 of Configuration Word B are reserved for use as a track/head address.
- Bits 8 through 15 of Configuration Word B are reserved for use as a sector address.

Configuration Word A.



Configuration Word B.



In multisector data transfer operations (Read or Write), the controller enables an automatic track and cylinder switching function. Track switching occurs whenever

the last logical sector on the track has been completed and the range has not expired. Note that track switching is not associated with Index Mark but with equality with the last sector number. When the last track of the cylinder has been completed and track switching is attempted, the HSDC initiates a seek to the next consecutive cylinder number, selects track number zero, and initiates a search for sector number zero. Note that activities on another channels (including data transfer) may occur during the seek latency period.

Additional considerations are:

- RPS is implemented for all Read and Write functions on disk drives with SMD-E interface.

- Data transfer continues until the range expires, an error is encountered, an unsuccessful search occurs or the end of the last cylinder is detected (setting bit 5 of the status word).

- Automatic track switching does not occur for any format operation or any unsuccessful search; detection of two Index Marks without a successful compare on both the addressed track and all tracks on the Error Log cylinder. When track completion is detected without an error, the Configuration Words are modified to reflect the next consecutive track and sector zero. In addition, if cylinder completion is also detected, the Configuration Words are modified to reflect the next consecutive cylinder, track and sector zero. Note that this update occurs only if the range is nonzero at the end of the last sector of the previous track.

- An attempt to automatically switch off the last track of the last cylinder results in status bit 5 being set (except in the case where the range has been decremented to zero).

- Both track and cylinder switching occur within the fixed disk selected by the Configuration Words provided that Range has not expired. A multisector operation takes place only within the selected media and does not link to another drive media.

The functionality described above enables software to access records in sequential order without having to reload the sector ID argument for every operation on a particular track. Extended reads or writes operate on sequential records and can therefore be used to advantage on files that are formatted with interleaved sectors.

5.2 Instructions

The DPS-6 instructions supported by the HSDC are listed in Table 5-1 with detailed instruction description following.

5.2.1 IOLD

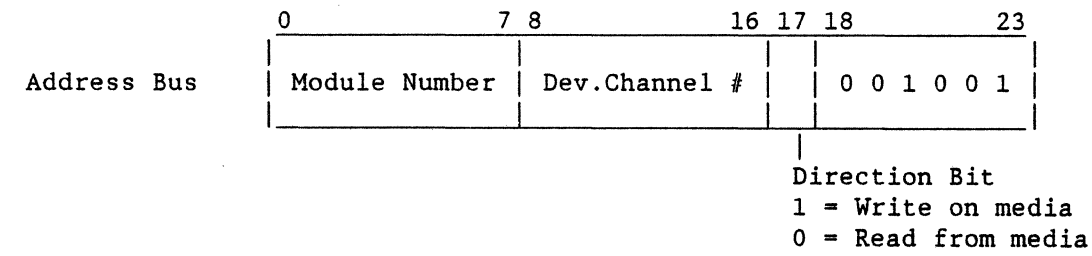
The I/O Load (IOLD) instruction is transformed by the CPU into the Output Address and Output Range instructions on the Megabus. Each IOLD instruction results in an Output Address instruction followed by an Output Range instruction.

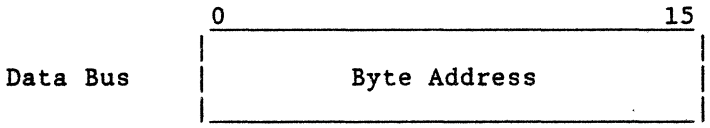
Type	Function Code Hex.	Instruction	Ref. Section
	*		
Output		IOLD:	5.2.1
	09	Address	5.2.1.1
	0D	Range	5.2.1.2
	0F	Offset Range (not used)	5.2.2
	11	Configuration Word A	5.2.3
	13	Configuration Word B	5.2.4
	15	Configuration Word C	5.2.5
	03	Interrupt Control	5.2.6
	07	Task Word	5.2.7
	01	Control Word	5.2.8
Input	08	Memory Byte Address	5.2.9
	0A	Memory Module Address/QLTI	5.2.10/19
	0C	Range	5.2.11
	0E	Offset Range (not used)	5.2.12
	10	Configuration Word A	5.2.13
	12	Configuration Word B	5.2.13
	14	Configuration Word C	5.2.13
	02	Interrupt Control	5.2.14
	26	Identification Code	5.2.15
	06	Task Word	5.2.16
	18	Status Word 1	5.2.17
	1A	Status Word 2	5.2.18
	3C	Firmware Revision	5.2.20
	20	Retry Counter	5.2.21
Diag - nostic	Any Even Code	Read HSDC Registers	5.2.22
	Any Odd Code	Write HSDC Registers	5.2.22

* All other Function Codes are RFU.

Table 5-1 Instructions.

5.2.1.1 Output Address

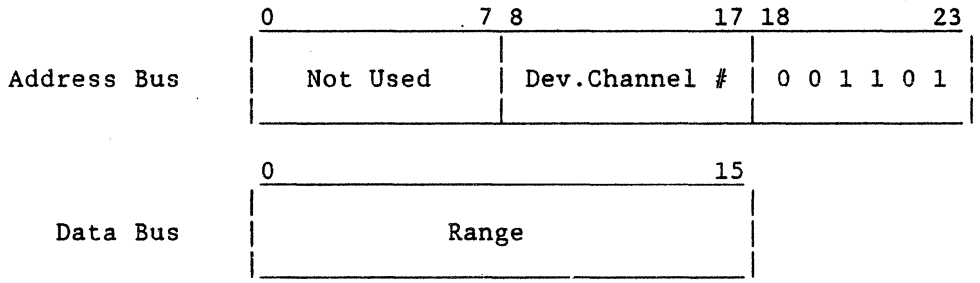




This instruction loads a 24 bit address into the address register associated with the referenced channel (device). The address refers to the starting (byte) location in the main memory where the HSDC commences input or output data transfers. Bits 0 through 7 of the address bus (module number) are the most significant bits. Data transfers to or from memory are normally on a word basis, but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

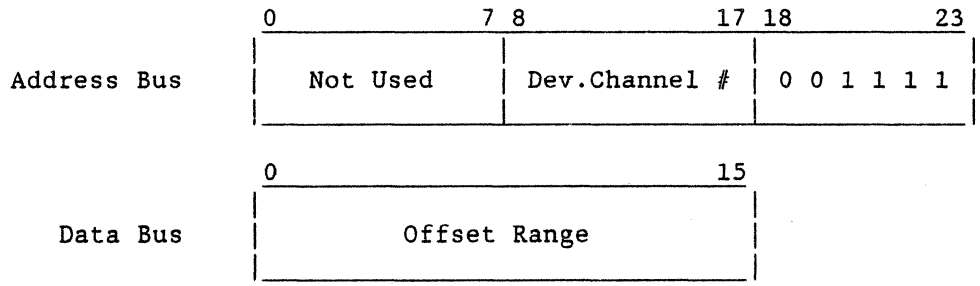
Bit 17 of the address bus the direction bit of the channel number, determines the direction of any subsequent data transfer operation. A logical One specifies an output operation (writing on media) while a logical Zero specifies an input operation (reading from media).

5.2.1.2 Output Range



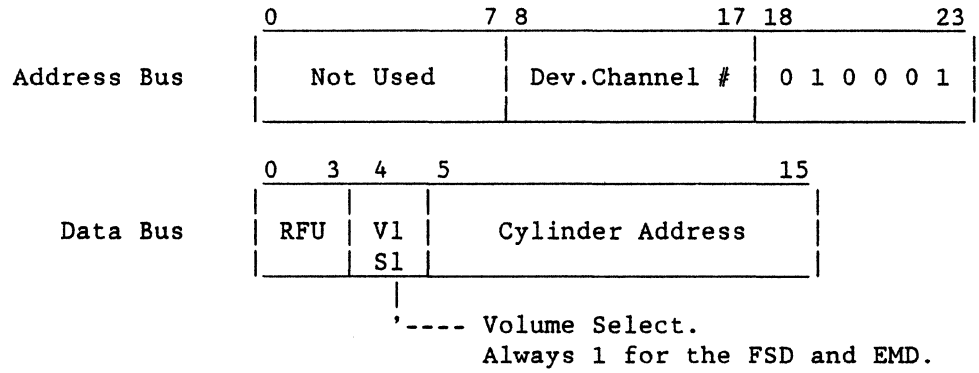
This instruction loads the range register associated with the referenced channel. The (16 bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity and is decremented by the HSDC after each memory transfer. A range of zero results in a premature End-of-Operation termination for any Read or Write command that may be subsequently issued (refer to subsections 5.2.7.3 through 5.2.7.9). Any range register residue is applied to the next command unless reset by another IOLD instruction.

5.2.2 Output Offset Range



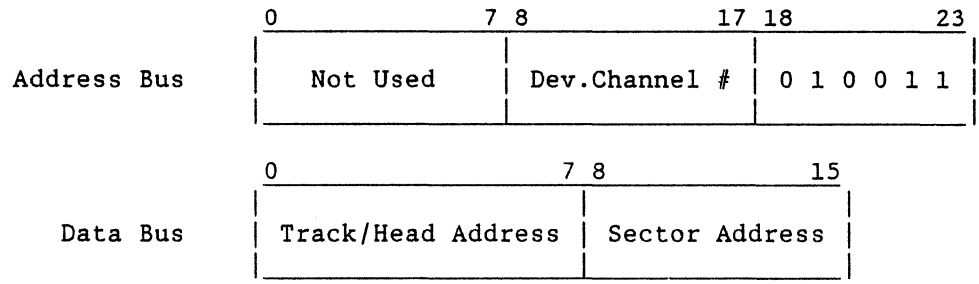
This instruction, implemented partially for compatibility reasons, loads the Offset Range register associated with the referenced channel and no other action takes place, except the normal instruction termination.

5.2.3 Output Configuration Word A



This instruction loads Configuration Word A for the device corresponding to the referenced channel. The cylinder address (bits 5 through 15) is used as the seek argument during Seek operations. The complete word is used as the two high order bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0 through 3 are reserved for future use (RFU). The highest cylinder address permissible for a disk is a maximum cylinder # - 2 (reserved for T&V cylinder and alternate 'Error Sector' cylinder). Bit 4, the volume select bit, is defined as: 0 = removable volume, 1 = fixed volume.

5.2.4 Output Configuration Word B



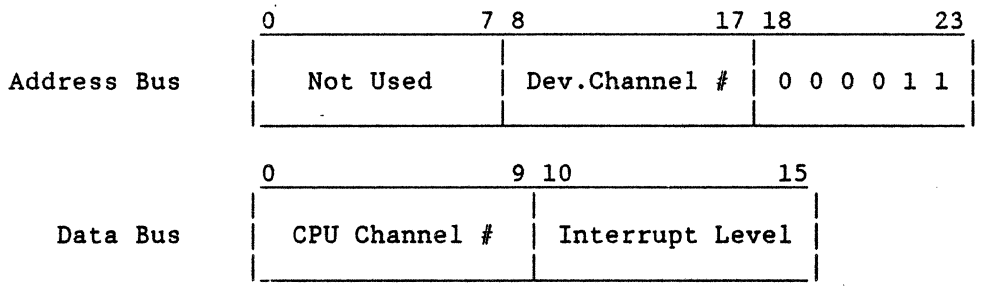
This instruction loads Configuration Word B for the device corresponding to the referenced channel. This word is used as the low order two bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0 through 7 provide the track address for any Read or Write operations: even = upper surface address, odd = lower surface address.

The subsystem treats bits 8 through 15 of Configuration Word B as a sector number. This number is incremented after operating on a data field during a data field Read or Write operation (see subsection 5.2.7).

5.2.5 Output Configuration Word C

This instruction is not implemented on the HSDC for filling the data field during a Format Write procedure, but the controller defaults to a 6D bit pattern.

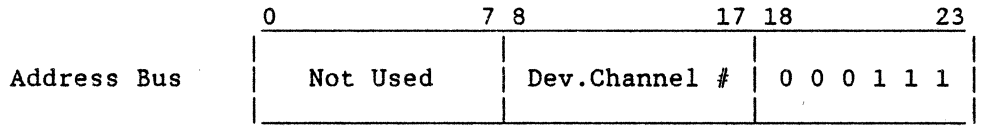
5.2.6 Output Interrupt Control



This instruction loads, for the referenced channel, the interrupt level and the channel number of the CPU. The interrupt level number is a 6-bit quantity and is positioned on the data bus as illustrated above. Bits 0 through 9 of the data bus contain the CPU channel number to which subsequent interrupts are to be directed.

If an interrupt level of Zero is loaded, the subsystem does not generate or save interrupts for any events that occur while the interrupt level is Zero. The interrupt level is set to Zero whenever the subsystem is initialized.

5.2.7 Output Task Word



Data Bus — Command Code

0 1 2 3	4 5 6 7	8	9		12	13	14	15	
0 0 0 0	0 0 0 0	0	0	MBZ	0	0	0	0	Recalibrate
0 0 0 0	0 0 0 1	0	0	"	0	0	0	0	Seek
1 0 A R	R 0 0 0	0	0	"	0	0	0	0	Format Write
1 0 A R	R 0 0 1	0	X	"	0	0	C	X	Read/Write Data
1 0 A R	R 1 0 0	B	D	"	0	0	0	E	Format Read/Write
1 0 A R	R 0 1 0	0	0	"	0	0	0	0	Diagnostic Format Read/Write
1 0 A R	R 0 1 1	0	0	"	0	0	0	0	Diagnostic Read/Write Data
1 1 0 0	0 0 0 0	0	0	"	0	0	0	0	Wraparound Read/Write Buffer
1 1 0 0	0 0 1 0	0	0	"	0	0	0	0	Read SPM
1 1 0 1	0 0 0 0	0	0		T4	T5	B1	B0	Diagnostic Detail Status

See page 46

Where:

A = Automatic Seek Bit
B through E & T = Specific meaning for the command
R = Reserved for Future Use (RFU). These must be "don't care" bits when not implemented.
MBZ = Must Be Zero

This instruction outputs a Task Word to the referenced channel. The coding of bits 0 through 7, illustrated above, represents operations that are to be performed (modified by bits defined in 8 through 15). When this instruction is accepted, the channel enters the "busy" state and the indicated task is initiated or stacked. All address, range, and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low order bit of the most recent output address instruction (refer to subsection 5.2.1.1). For example, if the data field encoding of the Task Word is received when a read channel number is indicated, than a Read Data command is executed. Note that track selection is performed for each media data transfer command prior to initiation of the data transfer and is based on the current contents of the Configuration Word B.

Bits 2 through 4 of the command code have specific meaning for all media data transfers as follows:

- Bit 2 - Automatic Seek

  If this bit is logical Zero, the data transfer is initiated based on the current cylinder position of the drive.

  If this bit is a logical One, a Seek Cylinder operation, based on the current contents of Configuration Word A, is initiation to the drive. Another channel may be serviced by the HSDC during the Seek latency period. At Seek completion, no Seek complete interrupt is generated to the bus channel and the specified data transfer operation is initiated.

- Bits 3 and 4

  Reserved for future use (RFU) and must be don't care bits in the HSDC.

5.2.7.1 Recalibrate

The Recalibrate command causes the channel to move the device's positioner to cylinder Zero, select track Zero, and send a Fault Clear command to the device. This instruction is intended as an Initialization command to guarantee that the position location information in the HSDC is correct and that all device faults are cleared. Completion of the Return To Zero operation by the device results in an On Cylinder status and Seek End.

5.2.7.2 Seek

The Seek command in the Task Word causes the channel to move the device's positioner to the cylinder indicated in Configuration Word A. If the cylinder specified is greater than the innermost cylinder or an error occurs during positioner

movement, than an error bit is set in the Status Word (refer to subsection 5.2.20 or 5.2.21). Completion of a positioning operation (whether or not any physical movement occurred) by the device results in the generation of an interrupt. Note that Seek completion as a result of an automatic Seek (see subsection 5.2.7) does not result in an interrupt.

5.2.7.3 Format Read

This command is redundant and is not implemented. Refer to subsection 5.2.7.4.

5.2.7.4 Format Read ID

The Format Read ID command causes the channel to read all Identifiers (IDs) on a track beginning with the first user sector after index and in the order in which they are recorded. IDs are transferred to memory beginning at the memory location specified in the subsystem's memory address register. This address is the address loaded by the most recent Output Address (IOLD) instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations have been executed since the last Output Address IOLD instruction, then the starting memory address used for this operation is the byte address immediately following the end of the most recent data transfer executed for this device (either read or write).

If Bit 8 (B) of the Command code is a One, then the CRC bytes of any sector identifier read are ignored. If bit 8 of the Command code is a Zero, then the CRC bytes of any sector identifier read are checked.

Data is transferred until an uncorrectable read error occurs (except as noted for bit 8), the range is satisfied, or the entire track is read (index is detected).

Normal range for this command (to read one complete track) is:

Range = 4 x N

Where: N = number of user sectors per track; 63 or 95, see section 7.

If this command is terminated due to end of track before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). An uncorrectable read error in any field (except as previously noted for bit 8 of the Command code = 1) causes the operation to be terminated with the read error bit set in the Status Word 1, bit 4. The field in error can be determined through examination of the residual range. If a read error is detected in an ID field the range is decremented for the ID field only.

If the range register is zero when this command is received, the task is terminated. No data is read or transferred. Track selection of the operation is based on the current contents of the track address of Configuration Word B.

If bit E of the Task Word Command is true, the 21 bytes of the Home Address are read starting with the (see Figure 5-2) Cylinder Address bytes and ending with the F0 byte; the Defect Log bytes are used by the firmware in reallocating bad sectors to the Error Log Cylinder. This command is used for diagnostic purposes only.

5.2.7.5 Format Write

The Format Write command causes the channel to format the track which is positioned under the read/write head specified by Configuration Words A and B when this command is received. 63 or 95, dependent on the device, equal length sectors are written starting at index excluding the invisible to software "home address" sixty fourth or ninety sixth sector. The sector ID fields are read from memory, beginning with the memory location specified in the subsystem's memory address register. Bit 8 is Zero for this command.

The data fields are filled by the HSDC with the 6D filler byte. The range to format one complete track is 380 or 252 bytes for 414/295/595 MB or 132 MB drive, respectively.

NOTES

1. Format Write ID and Format Write codes have the same functionality.

2. Read errors can occur on reallocated sectors which were found to contain uncorrectable errors.

3. Error sector reallocation is performed at this time. Identified error sector ID field CRC bytes are written incorrectly, ie, complemented CRC (see subsection 5.3.3.3).

If a range other than 380/252 is specified, Program Error Bit 5 is set to One in Status Word 1. Error Sector cylinder Format Write is described in subsection 5.3.4. If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation) and no data is written.

If bit E of the Task Word Command is set to one, the 21 bytes of the Home Address are written starting with the (Reference figure 5-2) Cylinder Address bytes and ending with the F0 byte; the Defect Log bytes are used by the firmware in reallocating bad sectors to the Error Log Cylinder. This command is used for diagnostic purposes only. In addition, if bit D is set to one, the Home Address extended gap is written.

5.2.7.6 Read Data

The Read Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to begin transfer of the data field of (at least) that sector to buffer memory. Data is transferred to the main memory from the HSDC buffer memory when the range is satisfied or the buffer is full, beginning with the memory location specified in the subsystem's memory address register. When the buffer is full and the range is not zero the next data transfer to main memory occurs when the buffer is full again or the range decrements to zero.

When the transfer, from the disk to the buffer memory, of the first specified sector data field is completed (without error), the sector number field of

Configuration Word B is incremented. If the initial range was greater than 256, then the sector on that track represented by the updated contents of Configuration Words A and B is located and data transfer continues with the new sector's data field. This operation continues until either the range is satisfied, an uncorrectable read error occurs, or the record specified by Configuration Words A and B cannot be located on the track or the reallocated track as indicated by the detection of two Index Marks without a successful compare (Reference section 5.3.4). If the specified record cannot be located, an unsuccessful search is posted in the status word (bit 7). Note that track and cylinder switching may occur as described in subsection 5.1.

Track selection for the operation is based on the current contents of the track address of Configuration Word B. If an uncorrectable read error (Reference section 5.3.2) is found in a data field, the operation is terminated and the read error bit in the status word is set (bit 4). The sector number field of Configuration Word B contains the address of the record in error.

If a read error is encountered in an ID field (Reference section 5.3.4), a miscompare result is assumed and the search continues. In this case the read error bit is posted in the status word so that, if the desired record is never located, the operation is terminated with both the unsuccessful search bit and read error bit posted in the status word, indicating that the reason for the miscompare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset.

If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation). No data is read or transferred.

Bit C (bit 14 of the Task Word), when set, inhibits read retries; conversely, retries are enabled when reset. This bit is intended to be used by diagnostics only for identification of bad spots on the media.

Bit F (bit ~~15~~ 9 of the Task Word), when set, enables data transfers between the controller data buffer and the disk device only; conversely, normal operation resumes when reset. This bit is intended to be used by diagnostics only.

5.2.7.7 Write Data

The Write Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data is read from main memory, beginning with the memory location specified in the subsystem's memory address register into the HSDC's buffer memory until either the buffer is full or the range becomes zero; then the data is written on the disk one sector at a time. Rewritten data fields are preceded by PLO sync bytes and data field sync byte (see Figure 4-3). When the transfer of a sector is completed, the sector number field of Configuration Word B is incremented. When the buffer is full and the range is not zero data transfer to the buffer memory resumes when the buffer is empty again.

If the range is less than 256, the remainder of the data field is zero filled. If the range is greater than 256, the sector represented by the updated contents of Configuration Words A and B are located and the data field rewritten. This operation continues until either the range is satisfied or the record specified by

Configuration Words A and B cannot be located on the track or the reallocated track, as indicated by the detection of two index marks without a successful ID field compare (Reference section 5.3.4). If the latter event occurs, the unsuccessful search bit is posted in the status word (bit 7). Note that track and cylinder switching may occur as described in subsection 5.1.

If a read error is encountered in an ID field (Reference section 5.3.4), the ID contents are ignored and the search continues. In this case the read error bit is posted in the status word so that, if the desired record is not located, the operation is terminated with both the unsuccessful search bit and the read error bit posted in the status word, indicating that the reason for the miscompare is a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset.

If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.12). If the range register is zero when this command is received, the task is immediately terminated (End-of-Operation) and no data is written.

5.2.7.8 Diagnostic Write Data

The Diagnostic Write Data command causes the channel to perform as if the Write Data command is specified, except that EDAC characters are written at the end of the data field updated as read from memory (not hardware generated). Only one sector can be updated by this command so that the range must equal 263 (256 + 7) bytes.

Track selection for the operation is based on the current contents of the track address of Configuration Words A and B.

5.2.7.9 Diagnostic Read Data

The Diagnostic Read Data command causes the channel to perform as if the Read Data command is specified, except that the seven-byte EDAC field attached to the data field is also transferred to memory (error detection/correction of the data field is not performed). Only one sector can be read by this command so that the range must equal 263 (256 + 7) bytes. Track selection for the operation is based on the current contents of the track address of Configuration Words A and B.

5.2.7.10 Diagnostic Format Write

The Diagnostic Format Write command causes the channel to perform as if the Format Write command is specified, except that invalid CRC characters (true CRC one's complemented) are written at the end of each ID field. Note that the data written in the data field is a pattern of bytes derived from the filler byte of Configuration Word C.

5.2.7.11 Diagnostic Format Read

The Diagnostic Format Read command is not implemented but the same functionality can be obtained by the Format Read ID with bit 8 set (Section 5.2.7.4).

5.2.7.12 Wraparound Read/Write

Only one Wraparound level of command is available on the HSDC. When a Wraparound Write command is received the channel writes into the specified buffer starting from the main memory address indicated by the memory address register. Care must be taken not to exceed the buffer memory size.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified buffer by the previous Wraparound Write command are returned to the main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by software in the preceding Wraparound Write command. The range supplied for the Wraparound Write must be the same as the range supplied for the Wraparound Read or the results are unpredictable.

A range smaller than or equal to 128 bytes should be specified for these commands. If a range of zero is specified, the command is immediately terminated (without being executed nor with any status indications). If a range greater than a buffer size is specified, the results are uncertain and the Program Error bit (bit 5) of the Status Word 1 is set and the command is terminated immediately. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word). Execution of a Task instruction on another channel during a Wraparound sequence is unpredictable.

5.2.7.13 Read SPM

This command is used for diagnostic purposes only; 256 bytes of random access memory (Scratch Pad Memory, SPM) are sent to the main memory. Contents are meaningful to the firmware only with the first 64 bytes corresponding to the Function Codes; consult the firmware listing for more details.

5.2.7.14 Diagnostic Detail Status

When SMD-E functions are enabled Tag 4 and Tag 5 with Tag 6 (logical, Tag 4 AND Tag 5) performance is as shown in Table 5-2; reference section 4.2.1.4 for more details. Appropriate one status (data) byte is sent on the Megabus by the HSDC in response to an IOLD with Range set to 1 and one of the following Task Word commands:

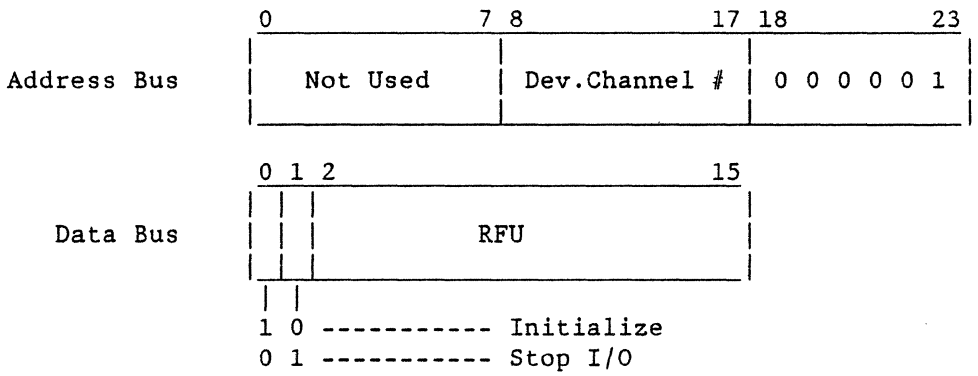
Data Bus 0 1 2 3	Command Code 4 11	12 13 14 15	
1 1 0 1	MBZ	T4 T5 B1 B0	Diagnostic Detail Status
1 1 0 1	MBZ	1 0 0 0	Read Current Sector
1 1 0 1	MBZ	0 1 0 0	Read Fault Status
1 1 0 1	MBZ	0 1 0 1	Read Operating Status
1 1 0 1	MBZ	0 1 1 0	Read Diagnostic Status
1 1 0 1	MBZ	0 1 1 1	Read Execute Start Status
1 1 0 1	MBZ	1 1 0 0	Read Device Type

	Tag 4 $ RPS T4	Tag 5 Extended Status T5				Tag 6 Device Type T6
Bus Out Bit 0	N/A	B0 = 0	= 1	= 0	= 1	N/A
1		B1 = 0	= 0	= 1	= 1	
	Current Sector Status	Fault Status	Opera - ting Status	Diag - nostic Status	Execute Status	Device Type Status
Bus In Bit 0	Megabus Bit 7	Read ^ Write			^	
1	6	(R+W) ^ On Cyl.			|	
2	5	1st Seek			All	User
3	4	Write	*	**	Zeroes	Defined
4	3	Write ^ Write Prot			|	
5	2	Head Select			|	
6	1	Voltage			v	
7	0	Valid Status	Valid Status	Valid Status	Test Started	

* Reference 4.2.1.6.2 ** Reference 4.2.1.6.3
$ RPS = Rotational Position Sensing N/A Not Applicable

Table 5-2 SMD-E Tag 4, Tag 5 and Tag 6 Functions

5.2.8 Output Control Word



This instruction loads a Control Word into the referenced channel. This command is unconditionally accepted by the channel regardless of its busy status, except as noted in subsection ~~3.1.2.~~ 3.2.1 Note that execution of this command may result in invalid

data on the media (if a Write operation is in progress) or a device fault (if a Seek operation is initiated and not completed prior to a subsequent operation).

5.2.8.1 Initialize

This command causes the HSDC to reset to the same state that it enters after power-up. When an Initialize command is received by the HSDC, all of its channels are initialized regardless of which channel the command is received over. A Recalibrate is executed on all connected devices.

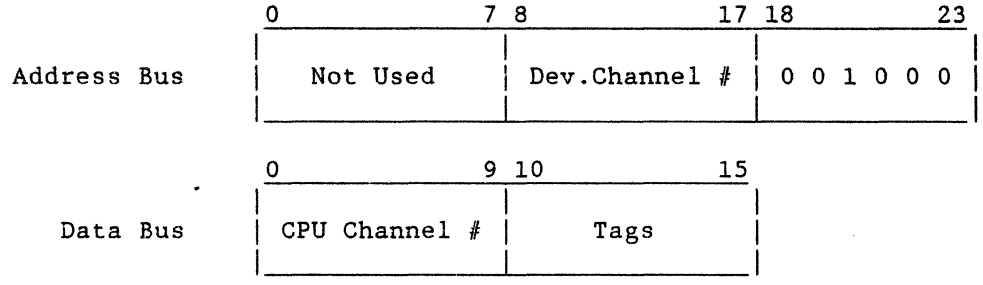
Operations that are in progress in the HSDC at the time of the initialization are abruptly terminated and all software addressable registers are initialized. No information about the terminated operations are retained and no interrupts for the operation are generated. The interrupt level for all channels is set to zero (interrupts blocked).

5.2.8.2 Stop I/O

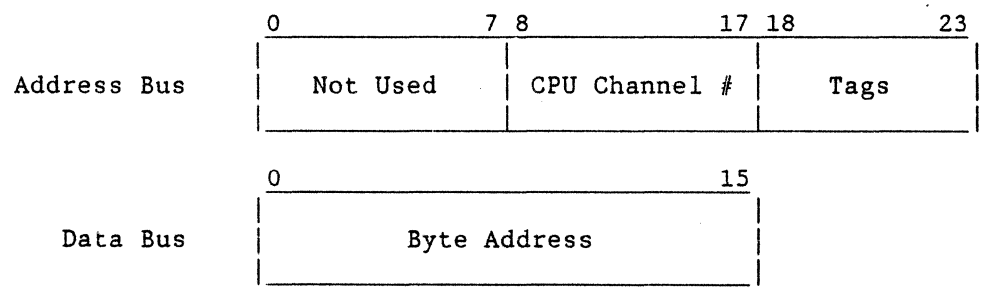
This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it is not completed and no error checking is done. An interrupt is generated for the operation terminated by this command as if the operation comes to a normal ending point. Status, address and range information, present in the HSDC when this command is received, is retained.

5.2.9 Input Memory Byte Address

Request Cycle



Response Cycle



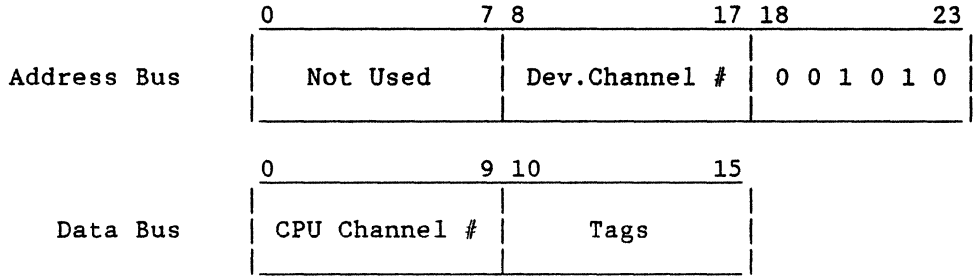
This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting CPU channel.

During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the low order 16 bits of the Memory Byte address currently stored for the specified channel in the HSDC. Note that if a Write command ended at a byte boundary (high order 8 bits of word), the memory address reflects the next word (not the low order 8 bits of the previous word). This command is used for diagnostic purposes only.

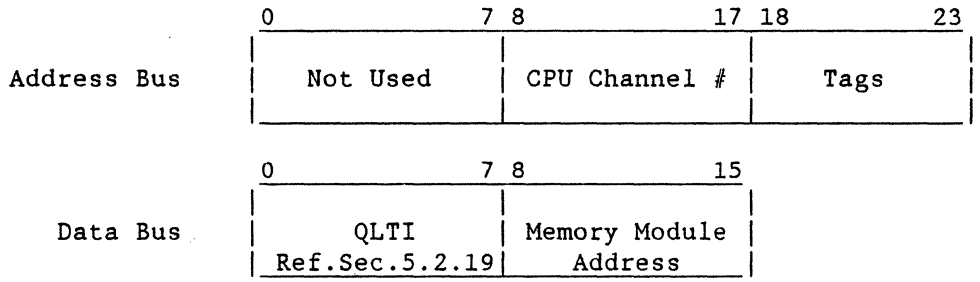
5.2.10 Input Memory Module Address

This instruction causes the current contents of the referenced channel's memory module address to be transferred to the requesting CPU channel.

Request Cycle



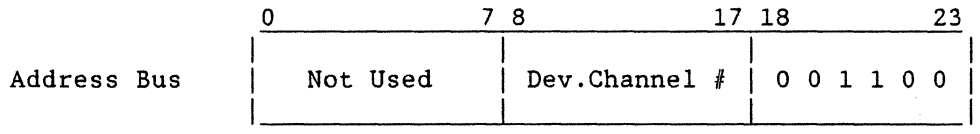
Response Cycle

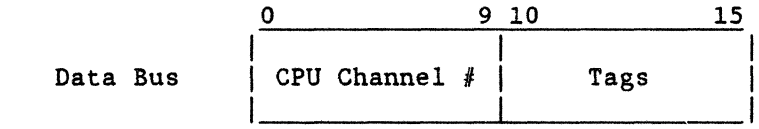


During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the high order 8 bits of the memory word address currently stored for the specified channel in the HSDC. This command is used for diagnostic purposes only.

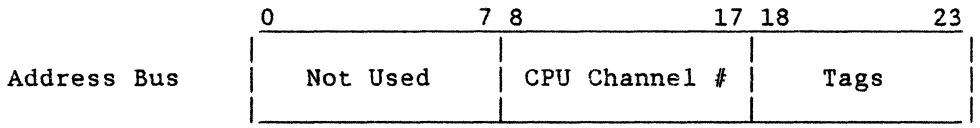
5.2.11 Input Range

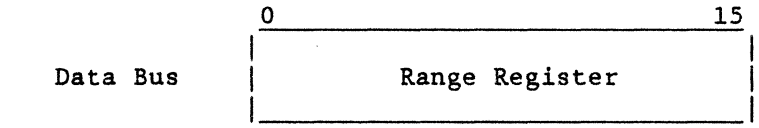
Request Cycle





Response Cycle





This instruction causes the current contents of the referenced channel's range register to be transferred to the requesting CPU channel.

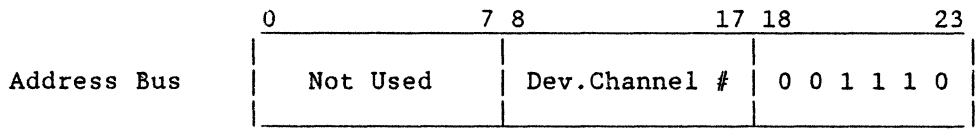
During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

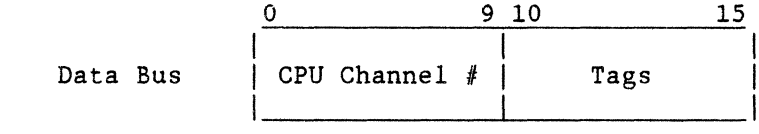
After completion of a data transfer operation, the contents of the range register reflect the byte count of the data transferred:

- o If the content value is greater than zero, the length of the physical sector(s) was less than the original range.
- o If the content is zero, the length of the physical sectors(s) was equal to or greater than the original range.

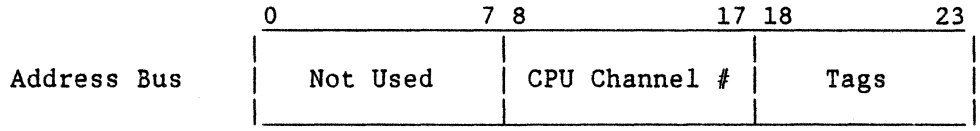
5.2.12 Input Offset Range

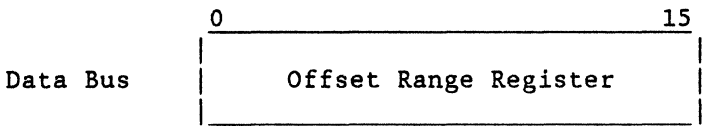
Request Cycle





Response Cycle



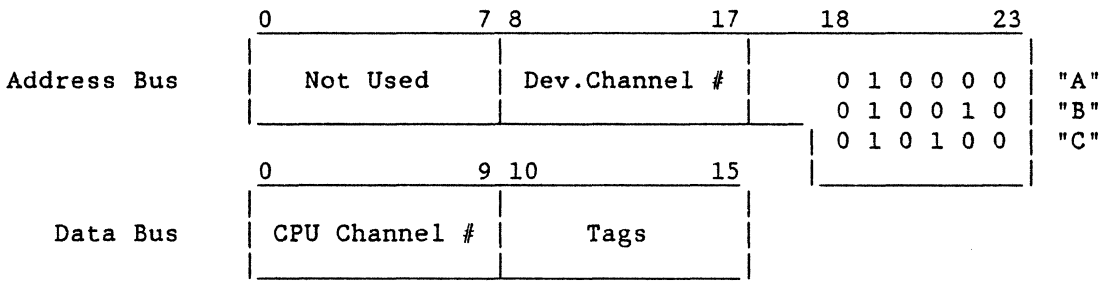


This instruction causes the current contents of the referenced channel's offset range register to be transferred to the requesting CPU channel.

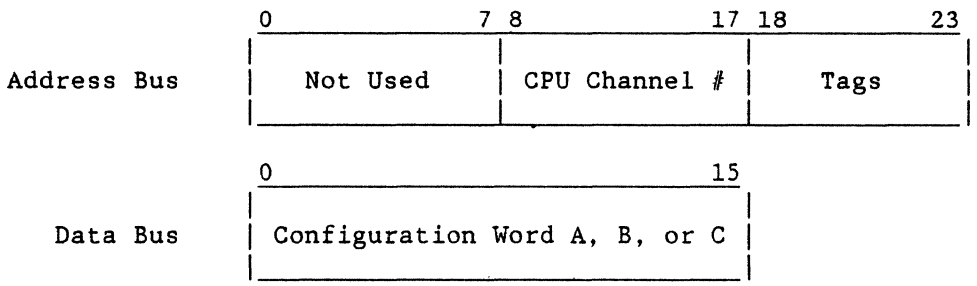
During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle. This instruction, implemented partially for compatibility reasons, reads the contents of the offset range register which was previously loaded by the Output Offset Range command and no other action takes place except the normal instruction termination.

5.2.13 Input Configuration Word A, B or C

Request Cycle



Response Cycle

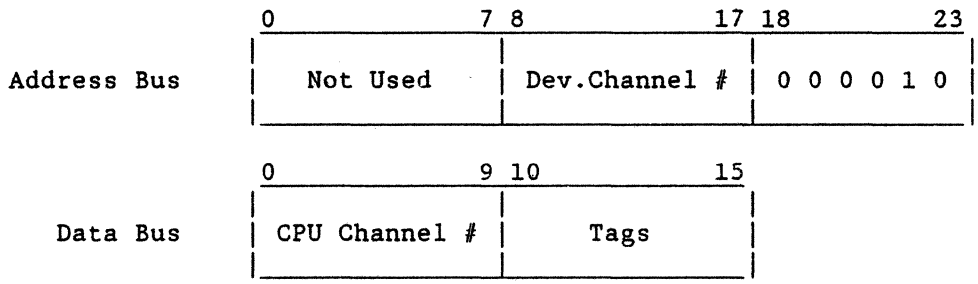


This instruction causes the current contents of the channel's Configuration Word A, B or C to be transferred to the requesting CPU channel.

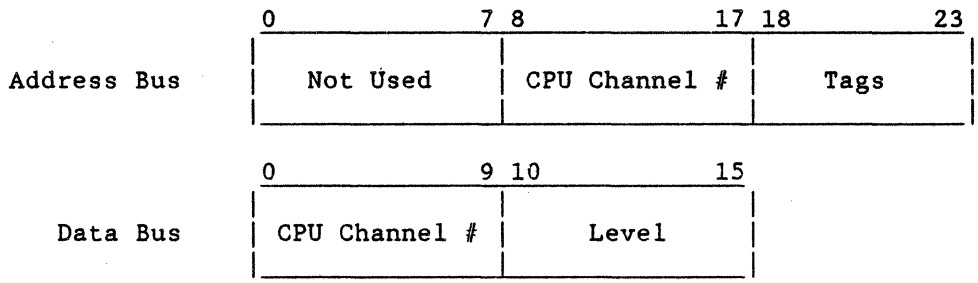
During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.14 Input Interrupt Control

Request Cycle



Response Cycle

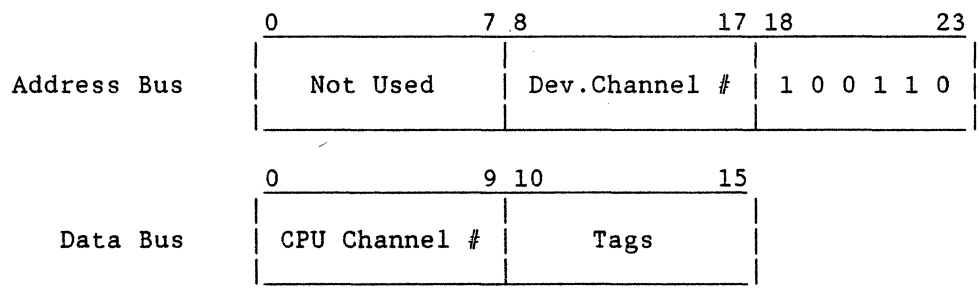


This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value is placed on data bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction, or a default value of 00. The default value is the interrupt level assumed by the channel when initialized. Note that the channel number returned in bits 0 through 9 of the data bus might be different than the channel number of the CPU executing this instruction if more than one CPU is attached to the Megabus.

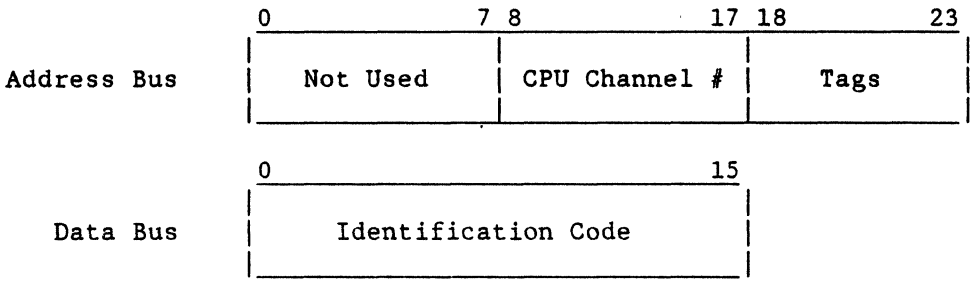
During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.15 Input Identification Code

Request Cycle



Response Cycle



This instruction causes the referenced channel to transfer its Identification Code to the requesting CPU channel. Depending on the device accessed, one of the following codes is returned:

The 201F, 230F and 331E codes represent the ID code received when an device is physically attached but is not accessible to the system because the mainframe has been powered-up but the drive on the channel is not. The HSDC generates the correct ID code when the device becomes available (i.e., when the drive is cycled up).

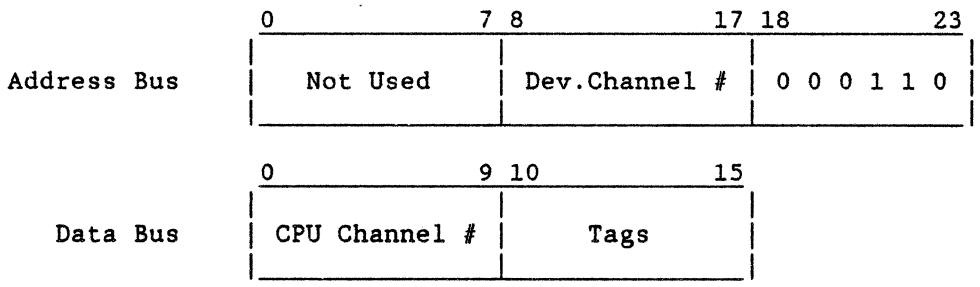
MODEL	ID	CAPACITY
FSD	2300	RFU
"	2301	132 MBytes
"	2305	413 MBytes
EMD	2303	295 MBytes
"	2307	597 MBytes
"	230F	See description above
HW250	2347	266 MBytes Northern Telrcom 8" Disk.
STR	207E	65 MB Sentinel
"	207F	See description above
"	3312	60 MB WangTek
"	331E	See description above
QDM	2017	5 1/4" Diskette
"	201F	See description above

It should be noted that this updated ID code becomes visible to software via the issuance of another Input Identification Code instruction.

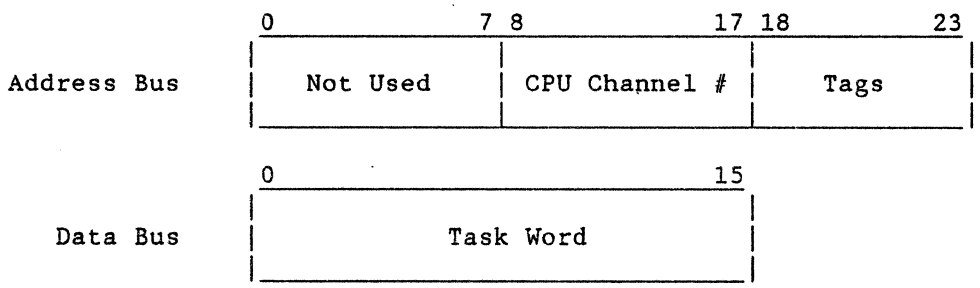
During the response cycle (second half read) the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.16 Input Task Word

Request Cycle



Response Cycle

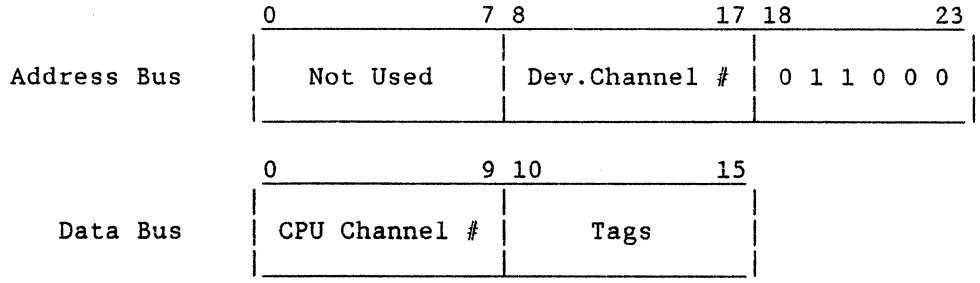


This instruction causes the Task Word of the referenced channel to be transferred to the requesting CPU channel. The Task Word transferred contains the code for the last operation executed by the channel (unless an initialize has occurred).

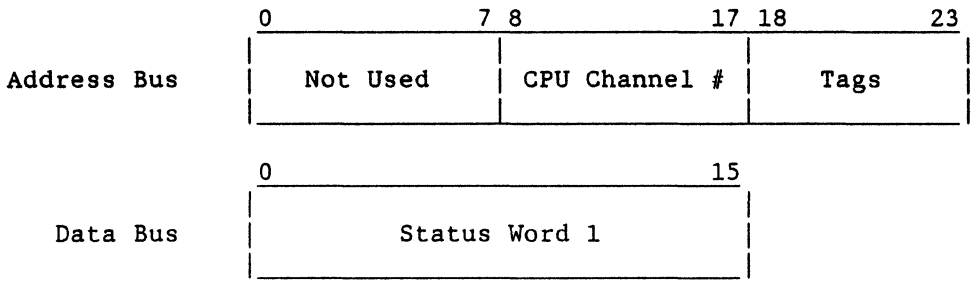
During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.17 Input Status Word 1

Request Cycle



Response Cycle



This instruction causes the referenced channel's Status Word 1 to be transferred to the requesting CPU channel.

During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

Data Bus bit assignment:

Data Bit		Description
0	----------	Device Ready
1	----------	Attention
2	----------	Controller Parity Error
3	----------	Device Fault
4	----------	Read Error
5	----------	Program Error
6	----------	QLT Fault
7	----------	Unsuccessful Search/Format Error
8	----------	Error Log Overflow
9	----------	Successful Recovery
10	----------	RFU-MBZ
11	----------	" "
12	----------	Corrected Memory Error
13	----------	Nonexistent Resource
14	----------	Bus Parity Error
15	----------	Uncorrected Memory Error

5.2.17.1 Device Ready (Bit 0)

This bit indicates that the device is on line with the medium loaded and that no further manual intervention is required to place it under program control. Note that a change of state of this bit causes the attention bit (bit 1) to be set, resulting in an interrupt (if the interrupt level is nonzero). This bit reflects the current condition of the device.

NOTE

When the device is cycled down, spindle motor off, or Device Fault is detected (i.e. write command to a protected device) the Ready Status indication becomes not true.

5.2.17.2 Attention (Bit 1)

This indicator is set whenever the device ready bit (Bit 0 of the status word) changes state. Any change of operational status of the device (e.g., load/unload of media) is indicated to software in this way.

Whenever the attention bit is set, an interrupt is attempted (if the interrupt level is nonzero). If a previously initiated operation is in progress when a device status change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word command or Master Clear on the Megabus.

5.2.17.3 Controller Parity Error (Bit 2)

When transferring data through the controller parity is verified and if found in error this bit is set.

This bit is reset by an Initialize command, an output Task Word command, an input Status Word Command or a Master Clear on the Megabus.

5.2.17.4 Device Fault (Bit 3)

This bit is set if the HSDC status bit 0 is set indicating a device fault; bits 08 through 15 of Status Word 2 reflect more specific faults.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus. Note that operator intervention is required to reset the write protect condition of the device. Also note that this bit is reset if the condition causing it to set is removed by the device.

5.2.17.5 Read Error (Bit 4)

This bit is set during any Read operation if either the EDAC word at the end of a field indicates that an uncorrectable data error has occurred within the field or the CRC Error bit appears within the ID field provided it is a new error not logged in the New Error Log on the highest number cylinder.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.17.6 Program Error (Bit 5)

This bit is set if any of the available Megabus commands are executed erroneously, e.g.:

- o Seek to a nonexistent cylinder,
- o Format Write range is not = 380 or 252 bytes dependent on the drive type.
- o Wraparound buffer range is incorrect
- o Attempt to select a non-existent head

This bit is reset by an Initialize command, an Output Task Word command, or a Master Clear on the Megabus.

5.2.17.7 QLT Fault (Bit 6)

This bit indicates that the controller or an adapter QLT has failed and that the QLT status buffer contains the fault identification. The Device Ready bit is also reset in Status Word 1.

This bit is reset by an Initialize command or a Master Clear on the Megabus.

5.2.17.8 Unsuccessful Search/Format Error (Bit 7)

This bit is set during a nonformat Read or Write operation for which the sector ID specified in Configuration Words A and B cannot be located on the track or on the innermost cylinder. It is also set if Index Mark is detected during a format Write operation; in this case, memory address and range registers are invalid.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.17.9 Error Log Overflow (Bit 8)

This bit is set whenever the HSDC detects that the New Error Log, on either the fixed or removable (if present) medium of the maximum cylinder sectors 1 through 4, on the drive has exceeded error sector space; either bit 5 or bit 6 of Status Word 2 is set.

5.2.17.10 Successful Recovery (Bit 9)

This bit is set when an error condition was successfully recovered during previous operation; Status Word 2 specifies the error condition which has occurred.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.17.11 RFU (Bit 10)

This bit is reserved for future use and must be zero.

5.2.17.12 RFU (Bit 11)

This bit is reserved for future use and must be zero.

5.2.17.13 Corrected Memory Error (Bit 12)

This bit indicates that, during the previous Disk Write operation, main memory detected and corrected a memory read error. The data that was delivered to the HSDC was assumed to be correct.

This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.17.14 Nonexistent Resource (Bit 13)

This bit is set whenever the HSDC attempts any bus cycle (except interrupt) and receives a NAK response from memory.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word 1 command, or Master Clear on the Megabus.

5.2.17.15 Bus Parity Error (Bit 14)

This bit is set whenever the HSDC detects a parity error on either byte of the data bus during any bus cycle, or when a parity error is detected in bits 0 through 7 of the address bus.

This bit is reset by an Input Status Word command or an Initialize (via Master Clear or an Output Control Word command).

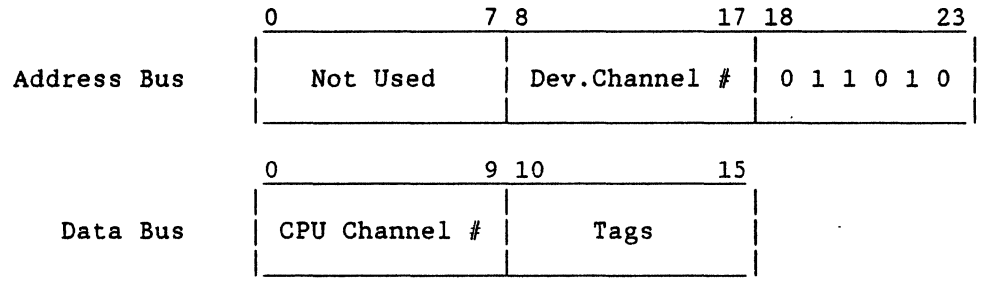
5.2.17.16 Uncorrectable Memory Error (Bit 15)

This bit indicates that, during the previous Disk Write operation, main memory detected a memory read error which the EDAC algorithm could not correct. The data that was delivered to the HSDC may have been incorrect. Occurrence of this condition does not cause termination of the operation in progress but may result in bad data on the medium.

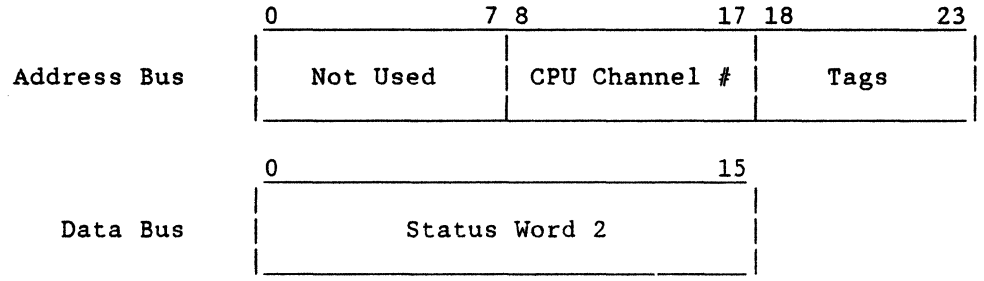
This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18 Input Status Word 2

Request Cycle



Response Cycle



This instruction causes the referenced channel's Status Word 2 to be transferred to the requesting CPU channel.

During the response cycle (second half read), the HSDC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

Data Bus bit assignments:

Data Bit	Description
0	Corrected Read Error
1	Successful Retry
2 thru' 5	RFU-MBZ — Alternate sector link cache hit
6	Error Log Overflow - Fixed Medium
7 thru' 12	RFU-MBZ
13	Hardware Fault
14	Seek Error
15	Write Protected

NOTE

If bit 13 or 14 is set, bit 3
of the Status Word 1 is also set.

5.2.18.1 Corrected Read Error(Bit 0)

This bit is set when a correctable read error occurred during the previous Read operation. Correction was performed by the HSDC in buffer memory. When this bit is set, it causes bit 9 of Status Word 1 to be set. See subsection 5.3.1 for EDAC functionality.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.2 Successful Retry (Bit 1)

This bit is set when a data read error has been successfully retried during the previous operation. Data stored in main memory is correct. When this bit is set, it causes bit 9 of Status Word 1 to be set. See subsection 5.3.2 for retry algorithm.

This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

5.2.18.3 RFU-MBZ (Bits 2 through 5)

These bit are reserved for future use and must be zero.

5.2.18.4 Error Log Overflow - Fixed Medium (Bit 6)

This bit is set whenever the HSDC detects that the New Error Log (on the fixed medium maximum cylinder sectors 1 through 4) on the FSD, has exceeded 255 error sectors count; it is also set on a failure to format the error log cylinder.

5.2.18.5 RFU-MBZ (Bits 7 through 12)

These bit are reserved for future use and must be zero.

5.2.18.6 Hardware Fault (Bit 13)

When this bit is set a device fault has occurred as listed in the interface specification, reference section 4.2.1.8.4.

5.2.18.7 Seek Error (Bit 14)

When this bit is set a seek error has occurred. This signal indicates that the device is unable to complete the actuator move or that it has moved to a position outside the recording area or that the address greater than the maximum number of tracks available has been selected. Read error is also set in Status Word 1 bit 4.

The Return To Zero command is required to clear this error and return the heads to track zero with the On Cylinder and Seek End true.

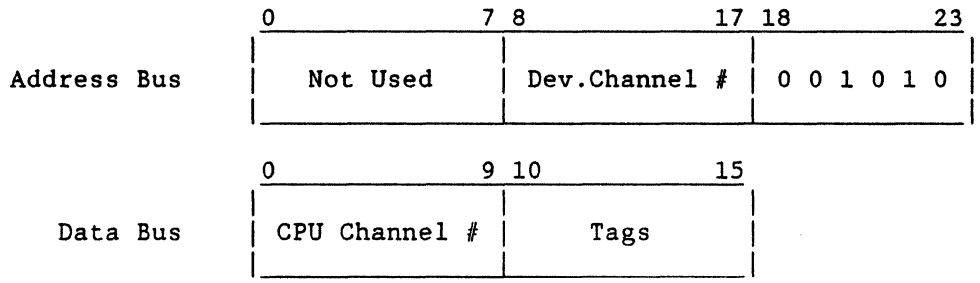
5.2.18.8 Write Protected (Bit 15)

When this bit is set it indicates that the device medium is protected from being written on by a front panel switch which inhibits the writer circuit, illuminates the front panel indicator and sets the Write Protect signal true. Attempting to write while in this state results in the set Fault signal from the device.

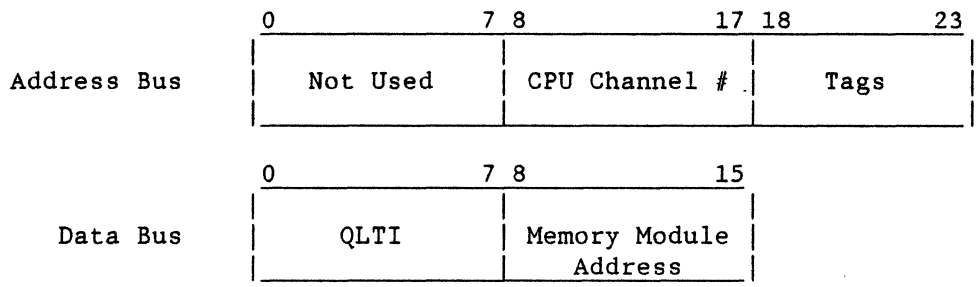
This condition can be reset by depressing the front panel Write Protect switch again which extinguishes the indicator.

5.2.19 Input Quick Logic Test Indicators (QLTI's)

Request Cycle



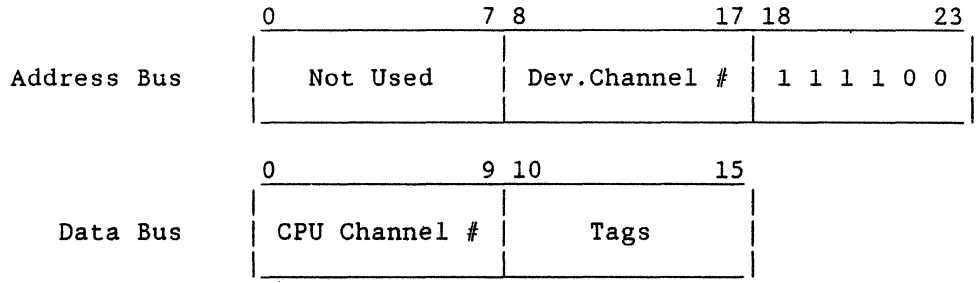
Response Cycle



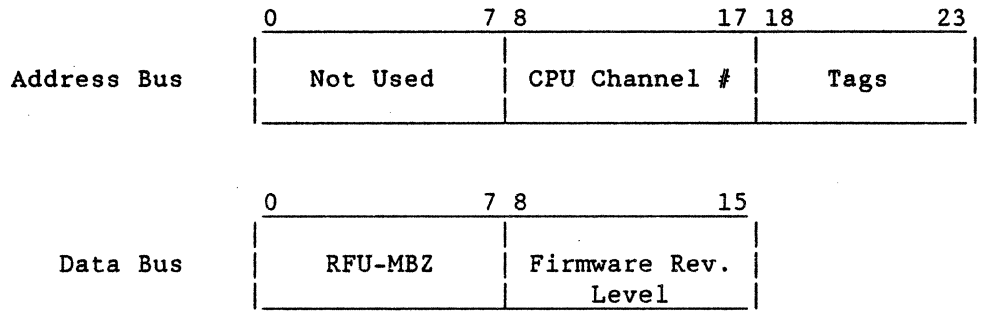
The QLTI's are stored in the Scratch Pad Memory (SPM) buffer during the QLT. If the edge indicator remains lit, the QLTI buffer contains the code of a test which had failed on either the HSDC or on an adapter. (Reference subsection 8.3.2).

5.2.20 Input Firmware Revision

Request Cycle



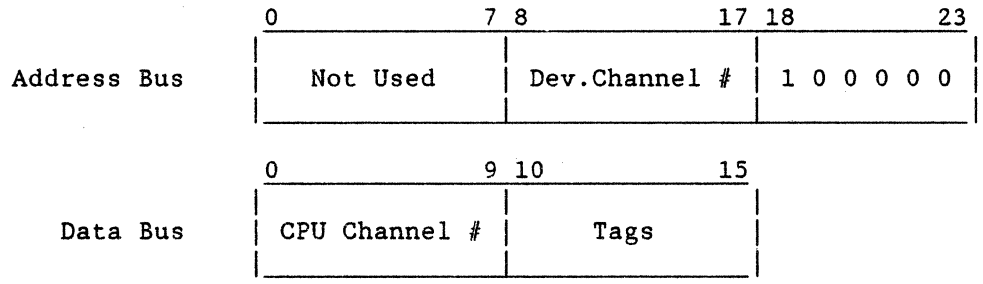
Response Cycle



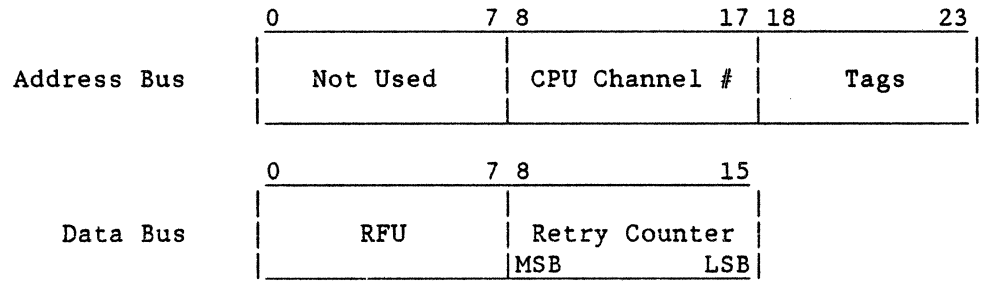
The firmware revision level is represented by a hex number, e.g., 23, which is the sequential control number.

5.2.21 Input Retry Counter

Request Cycle



Response Cycle



This instruction causes the referenced channel's Retry Counter to be transferred to the requesting CPU channel.

The Retry Counter contains the count of the number of times Read Error Retries were performed; reference subsection 5.3.2. This count is provided for error logging purposes.

The Retry Counter is reset by an Output Task Word, Initialize or a Master Clear on the Megabus.

5.2.22 Read/Write HSDC Registers

The HSDC maintains 32 registers (16 bits per register) for each channel. The address of each of the various registers in the HSDC is a combination of 2 bits of the Channel Number and the high order five bits of the Function Code used to write into or read from a particular register (see Table 5-1). For example, Configuration Word A for HSDC channel 2 is HSDC register 48 (hex):

- Function code for configuration word A = 01000X (X = read/write bit)
- Channel number = 010Z (Z = direction bit)
- Register number = 0100, 1000 = 48 (hex)

Complete software visibility to the HSDC registers is provided for diagnostic purposes. An output bus sequence addressed to one of the devices causes the information on the data bus (16 bits) to be loaded into the device specific register specified by the device port number and the high order 5 bits of the function code. (Reference Figure 5-1).

The Output Address command is a special case. When an Output Address command is executed (on port 0, for example) the HSDC register 04 (hex) is loaded with the low order 16 bits of the address. The high order 8 bits of the HSDC register 05 are loaded with the high order 8 bits of the address.

Any input bus sequence addressed to a device causes the register specified by the Port Number and the high order 5 bits of the Function Code to be returned via the data bus (during the second half read cycle). A detailed register map for each device type is available in the HSDC manual.

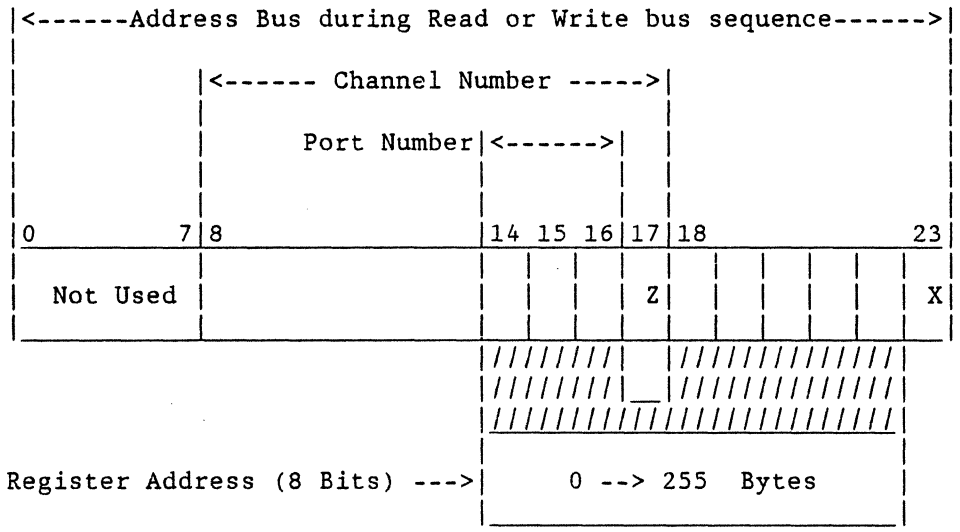


Figure 5-1 HSDC Device Specific Registers and Addressing

Blank

5.3 Defect Management

5.3.1 EDAC Functionality

The 7-byte EDAC field appended to the data field provides the correction of error bursts of up to 11 bits and detection of an error burst of up to 22 bits. Any bit errors separated by more than 10 bits are not correctable. The write polynomial generator used for the creation of a 7-byte EDAC field is as follows:

$$\text{Write Polynomial} = 1 + x^i$$

where: i = 1, 5, 9, 11, 12, 15, 16, 17, 19, 22, 31, 36, 37, 38, 39, 41, 45, 49, 55 and 56.

During Update Read and Write operations, the detection of any read error in an ID field causes bit 4 of the Status Word 1 to be set. The search (update read or write) continues. If a successful search is not made prior to detection of two Index Marks, the operation is terminated with bit 4 set. If a successful search is made prior to detection of two Index Marks, bit 4 is reset and the operation continues normally. In either case, no error correction is performed on the ID field.

If a read error is detected following the transfer of a sector data field to buffer memory, one of two situations is possible:

- The HSDC automatically performs the required correction in buffer memory, sets bit 9 of Status Word 1 and bit 0 of Status Word 2, and continues the data transfer operation. Note that a loss of revolutions of the media occurs during the retry period.

- If the error is not correctable by the retry procedure, EDAC is attempted only once after the retry procedure is unsuccessful in removing an error.

5.3.2 Read Error Retry

If a read error is detected following transfer of a sector data field to the buffer memory, the following retry procedure is invoked automatically by the HSDC:

1. Three retries.
2. Three retries with clock advanced.
3. Three retries with clock retarded.

4. Three retries with offset in.
5. Three retries with offset in, clock advanced.
6. Three retries with offset in, clock retarded.

7. Three retries with offset out.
8. Three retries with offset out, clock advanced.
9. Three retries with offset out, clock retarded.

10. Normal, followed by EDAC.

Note that:

- The read error retry is applied to data field errors only during Read Data

commands (does not apply to format or diagnostic commands - bit 4 of Status Word 1 is set in these cases as applicable).

- o A latency period is entered between retries, i.e., no other channel on the HSDC can be serviced except Seek and Implied Seek.
- o A loss of at least one revolution occurs for each retry.
- o Any clock change or any offset condition is automatically restored after retry (successful or unsuccessful).

The read error retry has one of two results:

- o If the error is not recoverable, bit 4 of Status Word 1 is set and the operation is terminated.
- o If the error is recoverable, bit 9 of Status Word 1 and bit 1 of Status Word 2 are set and the data transfer operation is continued.

5.3.3 Media Defect Handling

Definitions:

- o An error burst of 11 bits or less is a correctable error. An uncorrectable error is one greater than 11 bits in length.
- c Acceptable criteria, CDC specification 64400400, section 4.4.3 through 4.4.5 for the FSD and CDC specification 64401200 (Rev. 7), section 4.4 through 4.4.7 for the EMD:
  - a Have no media defects on cylinder 0, head 0 and 1, and logging areas to the extent defined in the CDC specification.
  - b Have no more than four defective sectors logged per track in the "home address" area on each track.
  - c Have no more than 500 defects per 414 & 595 MB volumes or no more than 250 defects per 295 MB and 132 MB volume.
  - d Have no more than 50 tracks per 414 & 595 MB volumes, no more than 25 tracks per 132 MB volume or no more than 10 tracks per 295 MB volume with two or more defects per track.

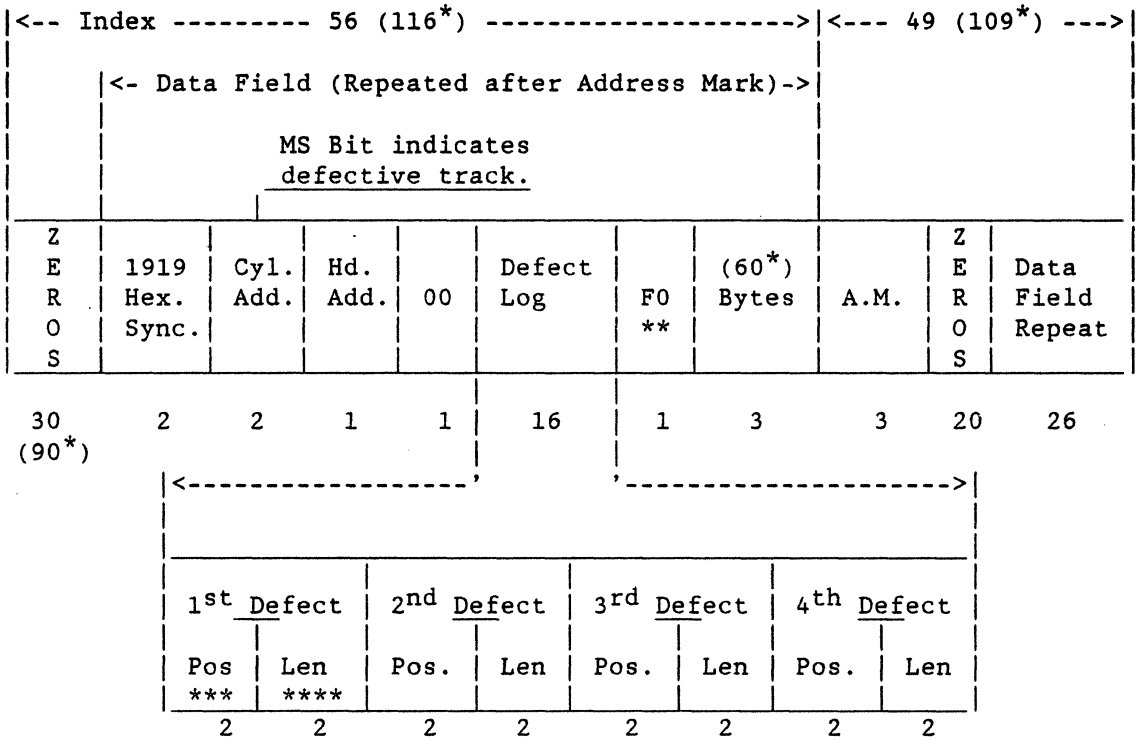
5.3.3.1 Vendor Error Log

Each track is analyzed, during media certification by MPI , for correctable and uncorrectable error conditions. If either defect exists, it is logged in the "home address" area (first sector after Index Mark) of each track. Provision is made to identify only four defective areas per track with a flag byte to signify defect overflow. A list of all the media defects is also available with each device (Reference 5.2.7.5 for reconstruction procedure of the "home address" area).

5.3.3.2 New Error Log

The New Error Log is constructed during Create Volume (CV) procedure when a new volume is formatted for the first time or when a volume is reformatted and the error log is recreated. The New Error Log resides on the Error Log cylinder (the highest number cylinder), head 0, sectors 1 through 4; it can contain identities of up to 255 new defective sectors for the entire volume. The remainder of the Error Log cylinder is used, by the HSDC firmware, for reallocation of error sectors identified by both the Vendor Error Log and the New Error Log.

Additionally, if during the life of the medium a new error should develop, software identifies the erroneous sector and appends its parameters to the New Error Log. This triggers the firmware in the HSDC to reallocate that new error sector.



Numbers are in bytes.

* Defect skipped (byte count).

** If more than 4 defects, Hex. FF is written. Honeywell devices have no more than 4 defects.

*** Position of defect is in bytes after index, ± 1 byte.

**** Length of defect is in bits, ± 1 bit.

Figure 5-2 FSD Home Address Format.

5.3.3.3 Error Log Management

To ascertain that a device has been previously formatted by the HSDC, it is necessary to attempt to read the Error Log cylinder, head 0 and sector 0, first:

- New or unformatted media.

  Attempt to read sector 0 results in either a CRC error or an unsuccessful search or both. The Error Log cylinder must be formatted.

- Formatted media.

  If the Error Log cylinder has been formatted before, reading head 0,sector 0 produces an ID of maximum cylinder # + head 0 + sector 0. The New Error Log sector ID's are maximum cylinder # + head 0 + sector 1 thro' 4; remaining sector ID and data spaces on that track are FF filled. Remaining tracks on the Error Log cylinder are formatted with true sector ID for the zero sector and all other sector ID's and data fields are FF filled. It is optional to format this cylinder when part or the entire volume is reformatted. All vendor identified bad sectors (home address on each track) on the Error Log cylinder are identified by an ID of BADD and an incorrect CRC; when reallocating error sectors, firmware skips over these sectors.

  The Format Write Task to the Error Log cylinder, head 0, is interpreted by the HSDC firmware as a command to format that cylinder, all heads; data fields of all sectors (and all ID fields except ID fields of all sector zero's and the New Error Log) are FF filled. The New Error Log parameters, if present, and reallocated sectors are lost in this process.

  The entire volume should be reformatted before proceeding to use it for data storage.

  Reformatting a volume without altering the error logs requires identification of defective sectors already in the error logs.

5.3.3.3.1 Vendor Error Log Management

The Format Write Task to any other track (not the Error Log cylinder) results in the following:

- The HSDC firmware reads the "home address" information (Reference Figure 5-2) and correlates it with the four byte ID field parameters sent by software during the Format Write operation. ID fields composition is as follows:
  - High Cylinder Address byte with the volume bit (bit 4) set to 1.
  - Low Cylinder Address byte.
  - Head/Track Number byte.
  - Sector Number byte.

- All the identified bad sectors have bad CRC's written in the ID fields when the track is formatted.

- The HSDC firmware then searches for the error sectors' ID's on the Error Log cylinder beginning on the surface on which the original track is being formatted. The search continues until that sector ID is found or an ID of FF's is encountered on this or on following surfaces.

  If error sector ID is found data field is written with 6D pattern, sectors have been already reallocated and no further action is required.

  If an ID of FF's is found that sector has not been reallocated. This error sector ID is then written, beginning on this surface, with replacement of the first ID of FF's.

- If the New Error Log exists on the Error Log cylinder (head 0, sectors 1 through 4) it is read into the main memory, by software, where it remains until a command other than a Format Write is in process. Subsequent Format Write commands to other tracks need only to refer to the New Error Log saved in the main memory to identify associated error sectors. The above is necessary to identify error sectors already recorded in the New Error Log for the track being formatted. Bad CRC's are written in ID fields of sectors identified as in error on the formatted track.

5.3.3.3.2 New Error Log Management

After formatting part or the entire volume the Format Write operation has to be verified by reading, not more than a track at a time, the formatted section of the volume. If a new error sector is found it is reallocated as described in the "New Error Procedure" below after which verification of the remaining sectors on that track resumes.

New Error Procedure:

- If a new error is found the HSDC stops the disk data transfer on the error sector and sends an interrupt to the CPU.

- Software responds to the interrupt then reads Status Word 1 and both Configuration Words A and B to determine which sector on the track is in error.

- The New Error Log is then read, by software, and the error sector parameters are appended (in place of the first four bytes of FF's in the data field) to the log.

- The New Error Log is written back on the Error Log cylinder which triggers the HSDC firmware to reallocate the last error log entry.

- The firmware records bad CRC in the ID field of the error sector and then reallocates that sectors' ID to the Error Log cylinder searching to replace the first ID field (from Index Mark) of FF's starting on the same surface as the bad sector; search continues sequentially to other surfaces until an ID field of FF's is found - if not found Status Word 1 bit 8, Error Log Overflow, is set and search terminates.

5.3.3.3.3 New Error Management

If, during the life of media, a new error develops the sector in error is reallocated in the same way as described in section 5.3.3.3.2 "New Error Procedure".

5.3.3.4 New Error Log Format

The New Error Log is 1024 bytes long, residing on the highest number cylinder, head 0, sectors 1 through 4. The four sectors of the log are initialized, by firmware, to all FF's when the Format Write Task is issued, by software, to the Error Log cylinder. The first four bytes of the log are reserved for software use and the rest of the log is used for new error sector parameters. Each error sector log consists of four bytes corresponding to the error sector ID; thus 255 [(1024-4)/4] new error sectors can be accommodated in the New Error Log.

6 PHYSICAL STRUCTURE

6.1 General

The High Speed Disk Controller Subsystem consists of an HSDC and from one to four drives which are connected to the controller board via cables in a combination daisy chain/radial fashion. The controller, a mother (M) board, is etched and has five connectors and electrical attachments to drives; one daisy chain "A" cable connector and four "B" connectors.

The HSDC mother board has provision for connecting two adapters; one to interface to the Minidiskette (QDM) and one to interface to the Streamer Tape (STA).

6.1.1 Physical Specifications

6.1.1.1 Mechanical

- Dimensions: 15 in. (38.1cm) wide by 16 in. (40.64 cm) long by 0.062 in. (0.157 cm) thick
- Weight: Approximately 28 oz. (0.794 kg)
- Cabling: Three connectors connect between the M-board and the FSD's. There is one daisy-chained control "A" cable and two ("Y") radial data "B" cables between the M-board, and from one to four disk drives connected. The maximum cable length from the controller to the most distant device shall not exceed 50 feet (15.24cm). Device connectors have 56 pins on cable "A" and 44 pins on cable "B".
- Cooling: Forced, unfiltered air at 125^{o}F (51.7^{o}C) maximum ambient at 110 CFM (51.9 liters per second).

6.1.1.2 Environmental

- Per HIS standards, B01.08 - Class 2 (contamination requirements are waived).
- Meet all U/L requirements, CSA approval.

6.1.1.3 Electrical

- Primary power - B01.48, Group I, II, III and VI
- Power module to share a common chassis with the printed circuit boards.
- Further definition given in NML Power Spec (60126325).

6.1.1.4 Physical Specifications, FSD

6.1.1.4.1 Mechanical, FSD's

- Dimensions: 8.5 in. (21.6 cm) width, 10.2 in. (25.9 cm) height (including the front face panel), 30.0 in. (76.2 cm) depth (including the integral power supply).
- Weight: 66 lb. (30.1 kg) - 132 MB FSD with integral power supply, and
  82 lb. (37.4 kg) - 414 MB FSD's with integral power supply.
- Rear panel: Location of cable connectors
- Cabling: Cabling connecting the HSDC with the FSD device in a daisy-chain/radial fashion should not exceed 50 feet (15.2 m.) for the "B" cable and 100 feet (30.4 m.) for the "A" cable in total length. Cable connectors at rear of each device accept cables.
- Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.1.4.2 Environmental, FSD's

The FSD device withstands the following environmental extremes without adverse effects (reference HIS standards B01.08 and B01.10).

Operational environment:

Temperature: 50°F (10.0°C) to 114°F (45°C) with a maximum change of 18°F (10°C)/hour maximum

Humidity: 20% to 80%, relative non-condensing, 79°F Max. wet bulb with a maximum change of 10% per hour

Barometric Pressure: 105 kPa to 69 kPa, -983 ft. (-300 m) to 10,000 ft (3,000 m).

Shock: 2 g's for 10 ms, no more than 2 shocks per second, any axis.

Vibration: Sinusoidal, 0.2 g's from 5 to 50 Hz. and 1 g from 50 to 500 Hz.

Storage environment, packaged:

The FSD packaged in its shipping container, can withstand, without damage, the following conditions:

Temperature: $14^{o}F$ ($-10.0^{o}C$) to $122^{o}F$ ($50^{o}C$) with a maximum change of $27^{o}F$ ($15^{o}C$)/hour maximum

Humidity: 10% to 90% relative, for 90 days maximum

Barometric Pressure: 105 kPa to 69 kPa, -983 ft. (-305 m) to 40,000 ft (12,000 m).

Shock: 24 in drop to a concrete surface

Vibration: Resonance, 4 Hz. to 100 Hz. at 0.5 g's

Transit environment, packaged:

The FSD packaged in its shipping container, can withstand, without damage, the following conditions while in transit in common carrier:

Temperature: $-40^{o}F$ ($-40.0^{o}C$) to $140^{o}F$ ($60^{o}C$) with a maximum change of $36^{o}F$ ($20^{o}C$)/hour maximum

Humidity: 5% to 95% relative, 7 days maximum

Barometric Pressure: 105 kPa to 19 kPa, -983 ft. (-305 m) to 40,000 ft (12,000 m).

Shock: 24 in drop to a concrete surface

Vibration: Resonance, 4 Hz. to 100 Hz. at 0.5 g's

6.1.1.5 Physical Specifications, EMD's

6.1.1.5.1 Mechanical, EMD II

- EMD dimensions: 8.5 in. (21.6 cm) width, 4.75 in. (12.1 cm) height and 14.7 in. (37.3 cm) depth + 1.74 in. (4.42 cm) for a fan and back panel when assembled without a power supply.
- Power Supply dimensions: 8.5 in. (21.6 cm) width, 4.75 in. (12.1 cm) height and 7.0 in. (17.8 cm) depth, includes integral fan.
- Weight: 25 lb. (11.4 kg) - 295 MB EMD without power supply, and 7 lb. (3.2 kg), approximately, for the power supply.
- Rear panel: Location of I/O cable connectors
- Status/Control panel: Location of numeric status display and control switches.

- Cabling: Cabling connecting the HSDC with the EMD device in a daisy-chain/radial fashion should not exceed 50 feet (15.2 m.) for the "B" cable and 100 feet (30.4 m.) for the "A" cable in total length. Cable connectors at rear of each device accept cables.

- Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.1.5.2 Mechanical, EMD III

- EMD III dimensions: 8.5 in. (21.6 cm) width, 4.75 in. (12.1 cm) height and 14.7 in. (37.3 cm) depth + 1.74 in. (4.42 cm) for a fan and back panel when assembled without a power supply.

- Power Supply dimensions: 8.25 in. (21 cm) width, 4.75 in. (12.1 cm) height and 7.2 in. (18.3 cm) depth, includes integral fan.

- Weight: 32.8 lb. (15 kg) - 595 MB EMD with fan but without power supply, 8.0 lb. (3.7 kg), approximately, for the power supply.

- Rear panel: Location of I/O cable connectors

- Status/Control panel: Location of numeric status display and control switches.

- Cabling: Cabling connecting the SMD-0/EA with the EMD device in a daisy-chain/radial fashion should not exceed 50 feet (15.2 m.) for the "B" cable and 100 feet (30.4 m.) for the "A" cable in total length. Cable connectors at rear of each device accept cables.

- Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.1.5.3 Environmental, EMD's

The EMD device withstands the following environmental extremes without adverse effects (reference HIS standards B01.08 and B01.10).

Operational environment:

Temperature: 50°F (10.0°C) to 113°F (45°C) with a maximum change of 27°F (15°C)/hour maximum

Humidity: 20% to 80%, relative non-condensing, 79°F Max. wet bulb with a maximum change of 10% per hour

Barometric Pressure: 104 kPa to 69 kPa, -1000 ft. (-305 m) to 10,000 ft (3,000 m).

Shock: 3 g's for 10 ms, no more than 2 shocks per second, any axis.

Vibration: Sinusoidal, 0.2 g's from 5 to 50 Hz. and 1 g from 50 to 500 Hz.

Non - operating environment, unpackaged:

The EMD in the unpackaged state and with power switched off, can withstand, without damage, the following shock and vibration input through the shock mount isolators:

Shock: 25 g's for 10 ms, any axis, with no less than 5 seconds between shocks

Vibration: Sinusoidal, 0.5 g's from 5 to 50 Hz. and 1 g from 50 to 500 Hz.

Storage environment, packaged:

The EMD packaged in its shipping container for a period of up to 3 years, can withstand, without damage, the following conditions:

Temperature: 14°F (-10.0°C) to 122°F (50°C) with a maximum change of 27°F (15°C)/hour maximum

Humidity: 5% to 95% relative

Barometric Pressure: 104 kPa to 69 kPa, -1000 ft. (-305 m) to 10,000 ft (3,000 m).

Vibration: Resonance, 4 Hz. to 100 Hz. at 0.5 g's

Transit environment, packaged:

The EMD packaged in its shipping container, can withstand, without damage, the following conditions while in transit in common carrier:

Temperature: -40°F (-40.0°C) to 140°F (60°C) with a maximum change of 36°F (20°C)/hour maximum

Humidity: 5% to 95% relative

Barometric Pressure: 104 kPa to 19 kPa, -1000 ft. (-305 m) to 40,000 ft (12,000 m).

Shock: 36 in drop to a concrete surface

Vibration: Resonance, 4 Hz. to 100 Hz. at 0.5 g's

6.1.2 Electrical

414 MB FSD; primary ac power, nominal:

100 - 120 Vac., single phase @ 3.4 Amps. and 0.712 PF
50 - 60 Hz.
260 W. power consumption (886 BTU/hr.).

208 - 240 Vac., single phase @ 2.1 Amps. and 0.66 PF
50 - 60 Hz.
252 W. power consumption (860 BTU/hr.).

295 MB EMD; primary ac power, nominal:

100 - 120 Vac., single phase @ 2.1 Amps. and 0.598 PF
50 - 60 Hz.
137.5 W. power consumption (468.8 BTU/hr.).

208 - 240 Vac., single phase @ 1.25 Amps. and 0.493 PF
50 - 60 Hz.
137.5 W. power consumption (468.8 BTU/hr.).

595 MB EMD; primary ac power, nominal:

100 - 120 Vac., single phase @ 2.1 Amps. and 0.598 PF
50 - 60 Hz.
137.5 W. power consumption (468.8 BTU/hr.).

208 - 240 Vac., single phase @ 1.25 Amps. and 0.493 PF
50 - 60 Hz.
137.5 W. power consumption (468.8 BTU/hr.).

132 MB FSD; primary ac power, nominal:

100 - 120 Vac., single phase @ 2.8 Amps. and 0.726 PF
50 - 60 Hz.
244 W. power consumption (832 BTU/hr.).

208 - 240 Vac., single phase @ 1.6 Amps. and 0.688 PF
50 - 60 Hz.
236 W. power consumption (805 BTU/hr.).

There is isolation of dc ground and frame ground in the disk device. The two grounds are brought out separately for external connection at a system level tie point.

7 PERFORMANCE

7.1 General

The HSDC accommodates a maximum data throughput of 14.52 MHz bits per second to/from the 414 MB FSD/295 & 595 MB EMD disks (1.8 M bytes) and 9.677 MHz bits per second to/from 132 MB FSD disk (1.2 M bytes), with an average Megabus data rate of 833 K bytes per second. The controller provides a one track buffer memory (24,320 bytes for the 414 MB FSD/295 MB EMD and 16,128 bytes for 132 MB FSD); if a range of equal to or less then the buffer memory is specified the range decrements to zero filling the buffer memory before transfer on the Megabus or to the disk, can begin. If a range greater then the buffer memory is specified, the controller fills the buffer, as before, then transfers the data to the Megabus or the disk. However, now disk latency delay of 8.3 ms is encountered in addition to the delay in filling the buffer memory again; this continues until range is satisfied.

The HSDC provides only one level of simultaneity. Only one data transfer can be active at any time but control functions, like seek, are processed simultaneously. One data transfer and any number of control functions can be processed at the same time. For comparison, the HSDC performance is better than that of the HPDC/SMD for range values less than 12 K. bytes, approximately.

7.2 Performance Characteristics

7.2.1 Performance characteristics of the HSDC

Disk Capacity	295/414/595 MB.	132 MB.
Sectors/Track	95	63
Bytes/Track	24,320	16,128
Transfer time/sector:		
Disk to HSDC	174 us	260 us
HSDC to Megabus	307 us	307 us
Transfer time/track:		
Disk to HSDC	16.7 ms	16.7 ms
HSDC to Megabus	29.2 ms	19.3 ms

7.2.2 Performance Characteristics

Performance characteristics of all disks are summarised in Tables 7-1 and 7-2 below.

Device Model #	9715 - 160 FSD	9720 - 368 EMD II	9715 - 515 FSD	9720 - 741 EMD III
Capacity (Unformatted):				
Bytes per track	20,160	30,240	30,240	30,240
Bytes per cylinder	201,600	302,400	725,760	453,600
Bytes per Spindle	165,916,800	368,020,800	516,015,360	740,728,800
Capacity (Formatted):				
Bytes per track *	16,128	24,320	24,320	24,320
Bytes per cylinder *	161,280	243,200	583,680	364,800
Bytes per spindle *	132,410,880	295,488,000	413,829,120	595,718,400
Sectors per track	63	95	95	95
Bytes per sector	256	256	256	256
Number of user cylinders **	821	1215	709	1633
Number of heads	10	10	24	15
Number of user tracks	8,210	12,150	17,016	24,495
Recording mode	2,7 Code	2,7 Code	2,7 Code	2,7 Code
Density,in bits per inch:				
inner track	9,492	15,185	15,040	14,981
outer track	6,117	10,132	9,167	10,032
Tracks per inch	551	960	960	1280
Spindle speed, $\pm$ 1%	3,600	3,600	3,600	3,600
Data transfer rate, nominal	9.67 MHz.	14.52 MHz.	14.52 MHz.	14.52 MHz.
Weight (with power supply)	66 lb.	32 lb.	82 lb.	41 lb.

* Calculations are based on the number of user cylinders.

** In addition, two cylinders are reserved: one for T. & V. use and one for New Error Log & reallocated error sectors.

Table 7-1 FSD/EMD Device Characteristics.

Device Model #	9715 - 160 FSD	9720 - 368 EMD II	9715 - 515 FSD	9720 - 741 EMD III
Data transfer rate, nominal	9.67 MHz.	14.52 MHz.	14.52 MHz.	14.52 MHz.
Positioning times in ms.:				
maximum	55	< 35	< 45	< 30
maximum single track	7	< 5	< 5	< 5
average	30	18	20	16
Latency, in ms.:				
maximum	16.83	16.83	16.83	16.83
average	8.33	8.33	8.33	8.33
Spindle timing, in sec.:				
start time	< 30	< 30	< 30	< 90
stop time	< 15	< 45	< 45	< 60
Head timing, in us.:				
select time	5	5	5	4
settling time (with PLO lock)	19	17	12	11.4
Write to Read recovery, us:	10	7	7	7
Read to Write recovery, us:	0.3	0.3	0.3	0.3
Return To Zero (RTZ), sec.:	< 1	< 1	< 1	< 1
Line Voltage @ 48 to 62Hz:				
low (max.)	85 - 132	85 - 132	85 - 132	85 - 132
high (max.)	177 - 264	177 - 264	177 - 264	177 - 264

Table 7-2 FSD/EMD Performance Characteristics.

Note. The special (Northern Telecom Winchester, 8", HW250) rigid disk drive required for the Navy SNAP program, replacement for the RD60, has the following characteristics:

Unformated Capacity	350.2 MBytes
Formated Capacity	265.6 MBytes
User Cylinders per Volume	1330
Tracks per Cylinder	12
Sectors per Track	65
Bytes per Sector	256

Blank

8 AVAILABILITY

8.1 Integrity

Data integrity is checked in the subsystem by the Error Detection and Correction code described in subsection 5.3.1. All data written on the media has a seven byte code (EDAC) appended such that when the data is subsequently read, the accuracy of the recovered data is guaranteed within limits. Parity is checked from the Megabus through the internal bus structure including buffer memory. Whenever the subsystem is initialized, QLTs are executed by the HSDC to provide a basic level of confidence that the microprocessor is fault free (see subsection 8.3). All subsystem detected errors are reported or displayed (refer to subsections 5.3 and 8.4).

8.2 Security.

Required protection of data on media from being destroyed by unauthorized writing over or erasing the data is provided at the device level by the setting of the Write Protect switch on the desired disk. The detection of a Write command issued to a protected medium is reported in the status register of the HSDC.

8.3 Maintainability

8.3.1 Maintainability Requirements

The following design goals, measured in hours, are specified as a minimum to be achieved during the first year after initial shipment or the 100th unit shipped, whichever comes first. References to "repair" normally imply ORU replacement.

8.3.1.1 Mean Time to Repair (MTTR)

MTTR represents the average repair time for a service engineer to diagnose, isolate, repair or replace, and verify the fix using the maintenance procedure described in 8.3.2. MTTR does not include response time, travel time, or idle time at the site waiting for the system or needed spare parts. These MTTR times are given for each unit that comprises the HSDC subsystem.

UNIT	AFTER FIRST YEAR
HSDC	0.9 hour
FSD	0.9 hour
EMD	0.5 hour

8.3.1.2 Mean Time Between Preventive Maintenance (MTBPM)

This goal, the period of operational time between required or recommended preventive maintenance (PM), is given for each unit.

UNIT	MTBPM
HSDC	no PM
EMD	no PM
FSD	Coarse filter replacement every six months.

8.3.1.3 Diagnostic Facility Localization Effectiveness (DFLE)

This represents the probability that a hard failure can be localized to a unit. The DFLE given takes into consideration the comprehensiveness, the resolution, and the accuracy of the diagnostic facility provided. The goals are stated for the SCPO designed components of the HSDCS and apply when the complete set of mintainability tools (section 8.3.2) are used to detect and isolate faults.

DFLE	First Ship
Comprehensiveness	95%
Isolation to an ORU	85%

- Comprehensiveness is the ratio, in percent, of the number of faults detected to the total number of faults that can occur.
- Isolation to an ORU is the ratio, in percent, of the number of faults correctly resolved to the ORU, to the total number of faults that can occur.

NOTE:

SCPO does not do fault insertion internal to a device and relays on fault isolation information, if any, supplied by the vendor.

8.3.2 Maintenance Strategy

The maintenance strategy for the HSDC subsystem is in accordance with the governing EPS-1 specification on the MRX System. The subsystem is partitioned into ORU's which can be effectively diagnosed for a faulty condition via a combination of firmware controlled tests, software tests, and visual indicators. Available diagnostic aids are to be executable by the customer as well as a service engineer.

Simple repairs such as the replacement of a defective ORU with an operational one should be able to be carried out by trained customer personnel or service engineers. Faulty ORU's are not serviced on the customer site.

8.3.2.1 Maintainability Features

The ORU's for the HSDC Subsystem are:

HSDC ORU's:

- o HSDC with/without adapters
- o HSDC to FSD or EMD cables

FSD/EMD ORU's:

- o HDA Assembly
- o PWA's
- o Power Supply

The goals are stated for the SCPO designed components of the HSDCS and apply when the complete set of maintainability tools, e.g. the QLT's, T & V's and Trouble Shooting and Repair Procedure, T & R.P., are used to detect and isolate faults:

The first step.

The Quick Logic Test (QLT) supplies a go/no-go visual identification of a HSDCS hardware failures. The QLT is invoked by one of the following: the power-on sequence, Master Clear or by the Output Control Word initialize command on any of the HSDC channels. QLT LED's conform to the following rules:

"ON" on the HSDC = HSDC failure
"ON" on an adapter = Adapter failure
"ON" on the HSDC and an adapter = Don't know which

The QLT verifies operation of each of the HSDCS ORU's. If a failure is detected during any of the tests, an LED is illuminated on the edge of the failed ORU (the BSQLT0 line is asserted) and a QLT indicator register is loaded associating tests performed with deviations from expected results for the HSDCS; the results are made available for interrogation at the end of the QLT in the QLTI register. QLTI contains the failing firmware routine code; firmware listing must be consulted for further clarification.

The QLT should conform to the following:

- o The QLT provides a means of isolating a fault to a ORU when combined with an appropriate T&V software routine.
- o No test must be allowed to stop the clock; i.e., no halt condition can exist in the firmware unless, if permitted to run, the controller would affect the Megabus operation. The QLT light stays ON for catastrophic failures only; normally it is extinguished to enable software interrogation of the QLTI register.

- The controller must issue NAK, not WAIT, during the QLT.
- Cables can be tested by substitution or by a continuity meter only.

Major QLT functions performed are:

- Read/Write a data pattern into all Scratch Pad Memory locations and verify
- Set and Reset control flops and test both states
- Wraparound data with bad address parity on the Megabus to test the data paths of the controller

The second step.

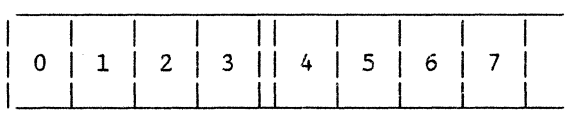
Software T&Vs are provided to verify all operational aspects of the HSDCS and to isolate failures to a ORU. Operator interface with these routines is via the CPU console or any TTY compatible console. The routines are run stand alone. Diagnostic functionality has been included in the subsystem to support software diagnostic routines, and the T&V cylinder can be used at any time for this purpose.

The third step:

Each FSD-414 and EMD-295 are equipped with a test panel mounted behind the front bezel, for running local diagnostics on the device (reference the MPI specification). Control switches and a two digit display enable to identify a faulty assembly within the device. This panel is intended for use by trained field engineering personnel, at a local or at a factory repair center. The FSD-132 does not have this test panel facility.

The designated ORU's are easily removable and replaceable. The only tool required is a screwdriver. System power must be off to remove or replace an ORU. Power for attachable devices is independent of system power to facilitate the powering down and replacement of failed devices without affecting system operation, except where a specific device uses system dc power. The attachable devices are powered individually such that any one device can be powered down without affecting any other.

CSD trained repair personnel utilizes a combination of trouble shooting repair guide and service kit to detect and isolate filing ORU's within a device.



00 HSDC and adapters are all good
XX Error condition, reference HSDC firmware listing for error condition isolation.

Figure 8-1 QLT Indicator Register Codes.

8.3.2.2 Installation

All HSDCS equipment installations or expansions to a basic system are Field Engineering responsibility. Replacement of faulty units is also CSD's responsibility for the initial shipments; subsequent maintenance can be performed by customer personnel, except for the HSDC which resides in the main cabinet assembly.

8.4 Reliability

8.4.1 Product Life

Product life is defined as the period of time within which the equipment performs within established reliability goals.

HSDC	10 years
FSD	5 years
EMD	5 years

The above estimates are made assuming 100% duty factor.

8.4.2 Mean Time Between Failures (MTBF)

MTBF is expressed in "power on" hours of the component or ORU and is concerned only with hardware failures. It is a minimum to be achieved after First Customer Ship (FCS).

	FCS	12th MONTH
HSDC	50,000	65,000
FSD-132	8,200	17,500
FSD-414	8,200	19,250
EMD-295	17,000	24,000
EMD-595	18,000	26,000

8.4.3 Mean Time Between Calls (MTBC)

MTBC is expressed in usage hours of the component or ORU between unscheduled or scheduled demand or emergency calls caused by hardware, operator, or media malfunctions which cannot be corrected by the operator (this includes installation of required FCOs). A "call" is a visit to the customer site by a field engineer. MTBC does not include calls for preventive maintenance.

	FCS	12th MONTH
HSDC	40,000	55,000
FSD	6,000	15,000
EMD	14,000	19,000

8.4.4 Transient Error Rate $\leq$ 1 in 10^9

The transient error rate is the total number of errors encountered as a function of the number of bits read before any recovery techniques are attempted.

8.4.5 Recoverable Error Rate $\leq$ 1 in 10^{11}

The recoverable error rate is the number of errors encountered which are recovered within 27 subsystem retries as a function of the number of bits read.

8.4.6 Unrecoverable Error Rate $\leq$ 1 in 10^{13}

The unrecoverable error rate is the number of errors encountered which cannot be recovered within 27 subsystem retries as a function of the number of bits read.

8.4.7 Recoverable Seek Error Rate $\leq$ 1 in 10^7

A recoverable seek error is one in which the Seek operation fails to position the device read/write head on the proper cylinder. However, upon the issuance of a Recalibrate command followed by a Seek command to the same cylinder, the Seek is executed correctly.

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