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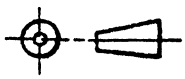
LOC. Billerica, MA		PROJECTION 	CODE	
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NOTE

This EPS-1, if not revised within one year, should be considered obsolete and therefore reference should be made to the appropriate product manual.

Honeywell HONEYWELL INFORMATION SYSTEMS		SPEC. NO. 60149777	SHEET 1.1	REV. B

HONEYWELL INFORMATION SYSTEMS
SYSTEMS ENGINEERING - BOSTON

ENGINEERING PRODUCT SPECIFICATION (EPS - 1)

SUBSYSTEM LEVEL

TITLE: Wren Disk Controller

VERSION: Approval DATE: 2/14/84

PRODUCT CALENDAR REFERENCE:

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SECTION 1 INTRODUCTION

1.1 SCOPE

This Engineering Product Specification defines the Wren Device Controller (WDC), which is a Hercules bus-mounted printed circuit board with logic providing control over the Wren Device Interface (WDI) and, connected, up to two Wren Disk Devices (WDDs). Functionally, the WDC emulates the command structure designed for Storage Module Drives (SMDs) and Cartridge Module Drives (CMDs) with a unique feature of providing a fixed media storage only on two or three platters. The WDC also performs medium defect reallocation for the complete volume with the same software visibility of sector 1 as on Lark.

The WDC is coresident on the same printed circuit assembly with the Sentinel streamer tape controller (STC, EPS-1 60149737) and shares some of the IOP logic with the STC. There is only one level of simultaneity for both WDDs and one STC.

1.2 OBJECTIVES

Four major components comprise the Wren Disk Subsystem (WDS):

- o Wren Device Controller
- o Up to two Wren Disk Drives with interface cables
- o Dc power cables to the power supply
- o Power supply.

Only the WDC functionality is described in this EPS-1. The FDI utilizes two cables: a command cable and a data cable. The command (C) cable is a daisy-chain command/status cable. The data (D) cable is a radial cable for the data and clocks plus some control. The third cable is for the dc power only delivered from the separate power supply.

1.3 DOCUMENTATION

1.3.1 Related Documents

NUMBER	TITLE	RESPONSIBILITY
60126298	EPS-1 Level 6 Bus (Megabus)	Systems Engineering
60144453	EPS-1 Hercules	Systems Engineering
60149661	PFS 8" Fixed Disk Subsystem - Hercules/Helios-0	Product Planning
60149674	Finch Device Controller - Hercules	Peripheral Systems
MTG1	PWA Test Equipment Connection Requirements	AMDXT-TE
MTG3	PWA Microdiagnostic Creation	AMDXT-TE.

1.3.2 Reference Documents

60129949	Application Rules for Minicomputer and Terminals Products	Circuit Design
Q4.1	PWA/PWB Testability Design Rules	PAE-TEE
MG1	Component Availability	AMDXT-TE
MTG2	PWA Test Documentation Requirements	AMDXT-TE
MTG4	PWA Test Monitor/Test Box Design	AMDXT-TE
MTG5	PWA Quality Logic Test Creation	AMDXT-TE
MTG6	PWA Test and Verification Program Creation	AMDXT-TE
MTG7	PWA IC Socket Utilization	AMDXT-TE
MTG8	Design for Producibility, Installability, Maintainability & Replaceability	AMDXT-TE
MPTG1	PWB/PWA Producibility Guidelines	AMDXT-TE
58035052	Worldwide Maintenance Requirements	FED
77653332 Rev. B	Product Specification for Finch Disk Drive - Model 9410-3F	MPI. OKC.

77653374	Application Notes - Diagnostics for Model 9410 Finch Disk Drive	MPI. OKC.
77653461	Application Notes - Interfacing a 9406 Flexible Disk Drive with a 9410 Finch Disk Drive	MPI. OKC.
77711078	Product Specification for Wren Disk Drive Model 9415-3	MPI. OKC.
77711098	Specification for Finch Device Interface	MPI. OKC.

1.4 DEFINITIONS

CMD - Cartridge Module Drive
CRC - Cyclic Redundancy Check
CPU - Central Processor Unit, LSI-6

DMC - Direct Multiplex Control
DS - Disk Subsystem

EDAC - Error Detection and Correction
EOT - End of Track (Record)

FDI - Finch Device Interface

IOP - Input/Output Processor (6809)
IOPB - IOP Bus

LED - Light Emitting Diode

MBZ - Must Be Zero

ORU - Optimum Replaceable Unit

PWA - Printed Wire Assembly
PWB - Printed Wire Board

QLT - Quick Logic Test

RFU - Reserved for Future Use
RPS - Rotational Position Sensing

SMD - Storage Module Drive

T&V - Test and Verification

WDD - Wren Disk Drive.
WDS - Wren Disk Subsystem

SECTION 2 ARCHITECTURE

2.1 OVERVIEW

The Disk Subsystem (DS) provides the Hercules computer systems with facility to store and retrieve data from mass storage media mounted on a disk device. Up to two WDDs can be cabled up to one WDC which can process simultaneously a single data transfer and one Seek command; all Hercules commands are accepted by the WDC in its nonbusy state. The WDC interfaces with other Hercules systems via the 6809 bus which can be Communications Adapter, Memory, IOP, etc. All controllers on the 6809 bus can function independently and concurrently utilizing the 6809 bus asynchronously.

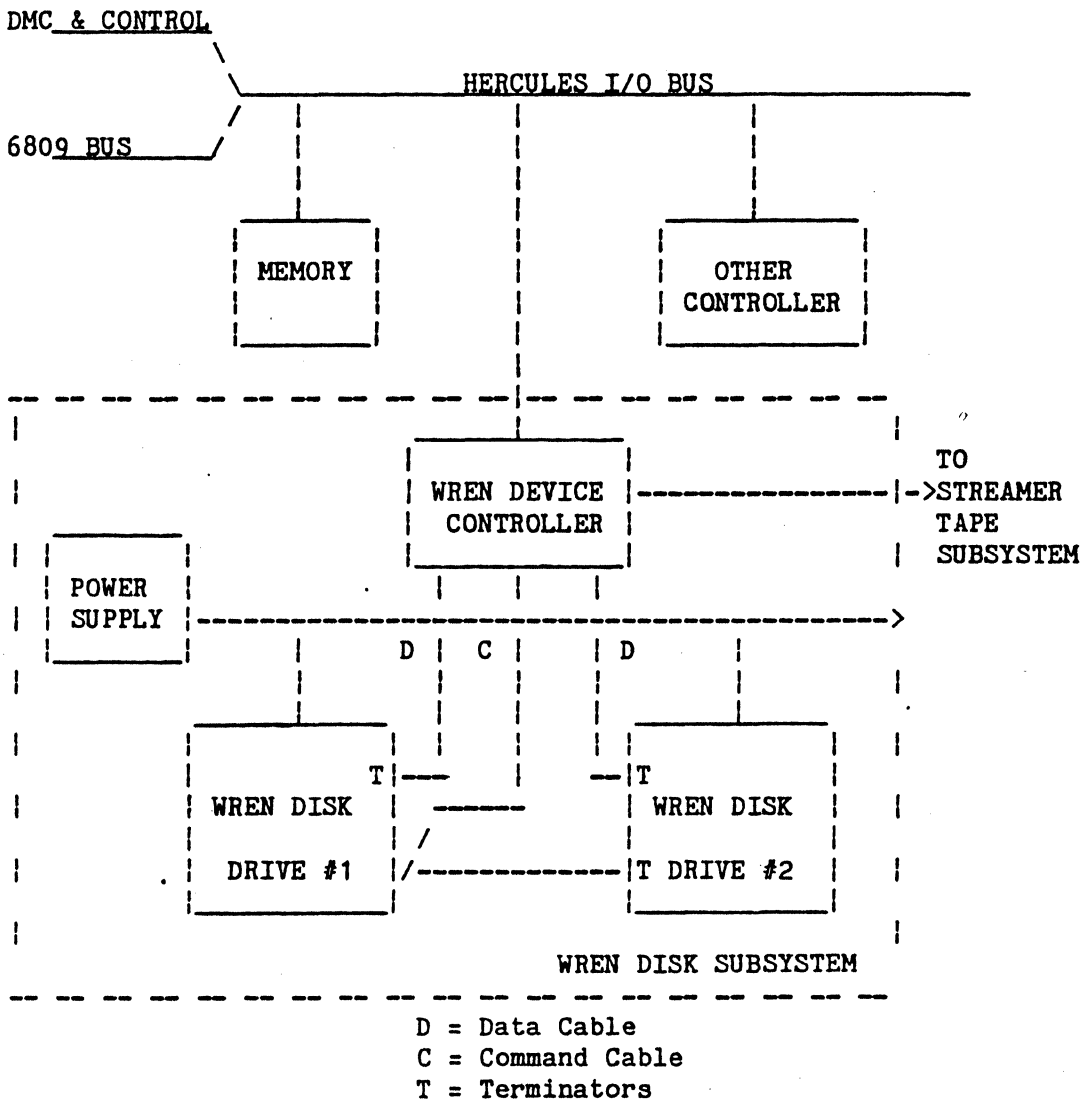
2.2 MAJOR COMPONENTS

2.2.1 Wren Device Controller

The WDC is a microprogrammed peripheral control unit which can interface with up to two WDDs (see Figure 2-1) cabled via connectors mounted on the device printed circuit board. The microprocessor portion of the WDC is generalized to facilitate its application as a control element for higher capacity devices. In addition to providing the IOP Bus command protocol supervision for three independent channels' combinatorial logic, the WDC interfaces with the IOP Bus as well as with the WDD connectors. The WDC performs the following functions:

- Execution of IOP Bus sequences
- Status and control register storage in dedicated, per channel, random access memory

- o DMC data transfers
- o FDI dialog control with serial-parallel and parallel-serial data conversion and associated error detection and correction
- o Medium defect handling using the prerecorded error logs in the highest numbered cylinder.



Wren Device Configuration

Figure 2-1 Disk Subsystem

2.2.2 Wren Disk Drive

The WDD is a small, random access, rotating 5.25-inch disk, mass memory device with fixed disk media storage. It employs rigid disk technology with a servo surface and low mass flying read/write heads attached to a rotary voice coil positioner. The unformatted storage capacity of the WDD is:

WDD Configuration 9415-32-3

- o 35 Mbytes - five surfaces of three disks
- o One servo control surface.

Basic components of the WDD are base casting and spindle, spindle drive motor, spindle and disk assembly, rotary voice coil actuator assembly with read/write heads, base Printed Wire Assembly (PWA) with LSI circuitry, motor control PWA, and read/write preamp PWA.

The WDD interface with the WDC comprises two cables: one radial D (data) cable and one daisy-chainable C (command) cable.

2.2.3 WDD Power Supply

The WDD power provides dc voltages required to operate the WDD. The voltages are +5 V and +12 vdc.

SECTION 3 FUNCTIONAL REQUIREMENTS

3.1 BASIC FUNCTIONS

3.1.1 Configuration and Simultaneity

Devices attached to the WDC are software addressable via a channel number. Each device has two channel numbers assigned, differing from each other only in the low-order bit position (the direction bit). When an IOLD instruction is issued to an WDC, the direction bit of the output address channel number specifies whether this is an input or an output data transfer. For all other commands, the direction bit is ignored by the hardware. Figure 3-1 outlines the composition of the channel number. Bits 0 through 9 are assigned at system installation and must conform to constraints defined in the L6 Bus EPS-1. Software visibility of the devices attached to the WDC is such that the device is, in general, independent of all others on the bus.

The WDC and the IOP provide a single level of simultaneity (only one data transfer can be active in the subsystem consisting of two WDC channels and one streamer channel) and supports the following:

- o A nonbusy device must accept all instructions directed to it, (i.e., IOLD, Configuration Words A and B, Task Word, etc.) even though a data transfer may be active over another device. An instruction may be "waited" for a period not exceeding 350 microseconds (Ref. 5.3.2.3).

- o Following completion of a data transfer operation, any Seek orders received should be initiated prior to the start of any data transfer operations.

- o The Channel Number for the Wren Disk Drive in the Hercules CPU/IOP is fixed as 0500_{16}.
- o Channel Numbers for the Wren Disk Drives are 500_{16} for device #1 and 580_{16} for device #2.
- o WDD ID Number is assigned $333X_{16}$(X = 1, 3, 5 or F; see subsection 5.2.13).

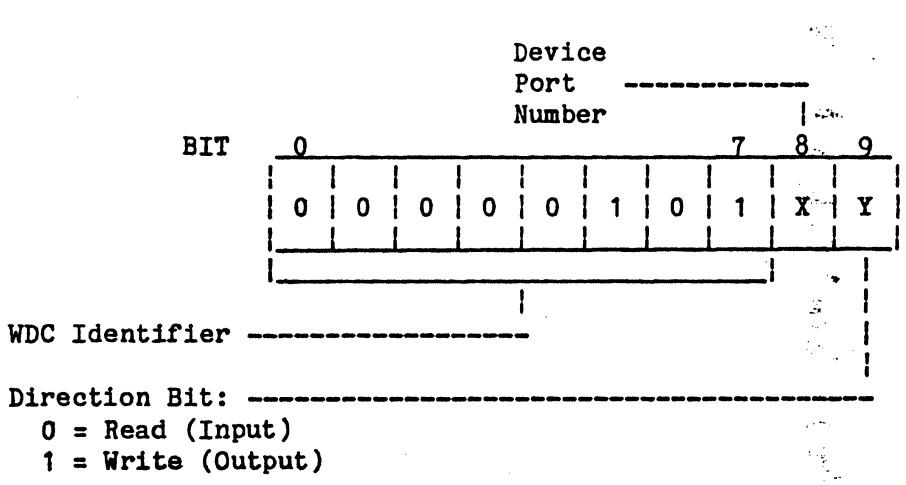
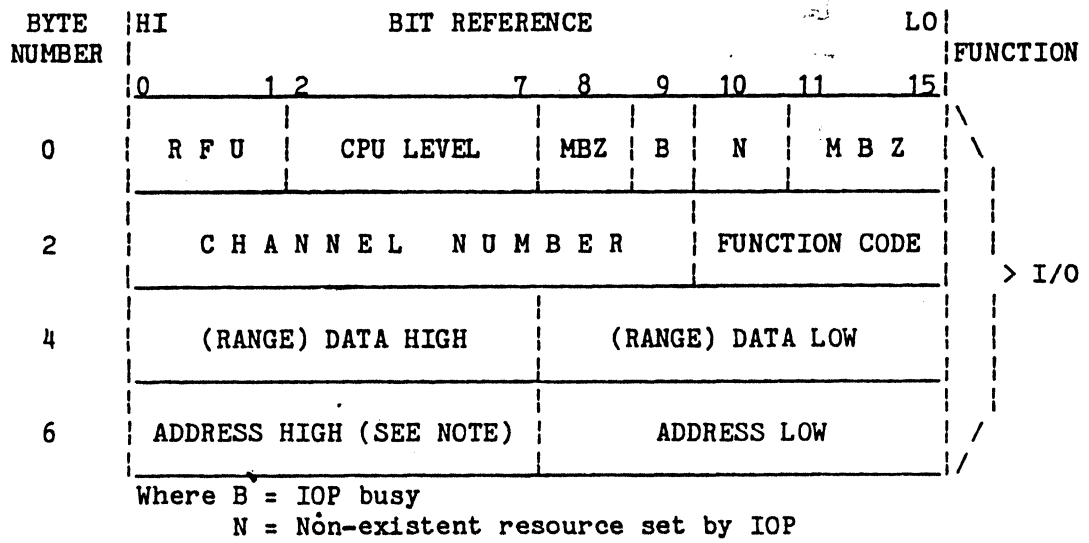


Figure 3-1 Channel Numbers (see Figure 3-2)



NOTE

The four highest order address bits are passed to the IOP through a hardware register.

Figure 3-2 Hercules I/O Mailbox Map

3.1.2 WDC Control

3.1.2.1 COMMAND TRANSFER

The IOP recognizes a command transfer request when the 6809 (IOP) recognizes a Non-maskable Interrupt (NMI) from the LSI-6 (CPU) and the content of the IOP's Mail Box is ready for interrogation. The IOP firmware is then invoked to process the information. For the not-busy case, the IOP completes the transaction by issuing an ACK (B = 0) to the CPU. If, however, the IOP is busy executing a previously received command, the IOP interface hardware completes the transaction by issuing a NAK (B = 1) to the CPU. When complete, the IOP resets the interrupt flop.

On receipt of a command, the IOP stores it in an appropriate table corresponding to the device Channel Number (bits 0 through 9) and depending on the Function Code (bits 10 through 15) of that command, either stores it in a queue to wait for a Task command or executes it immediately (i.e., Read Status command, etc.).

When an input from the IOP is requested by the CPU, the IOP responds to the NMI from the LSI-6 which now can read the data word contained in bytes 4 and 5. The NMI flip-flop is reset by the IOP when this is accomplished.

The address and data bus configurations of the CPU for the various commands are detailed in subsection 5.2.

3.1.2.2 INTERRUPTS

The current CPU Interrupt Level (byte 0, bits 2 through 7) is maintained by the CPU firmware. If the CPU Interrupt Level is lower than or equal to that of the interrupting channel, no interrupt from the IOP to the CPU is attempted, and, as long as this is true, the channel shall continue requesting an interrupt until it is accepted or the condition causing the interrupt is reset.

When an interrupt is serviced, the IOP loads the interrupt Mail Box (see Figure 3-3) bytes A and B and sets bit 8 (F) of byte 9 to a One then interrupt the LSI-6. The CPU reads both bytes A and B, clears the F bit and either sets bit B (bit 9 of byte (9) to a One if the interrupt is not accepted (NAKed) or a Zero if the interrupt is accepted.

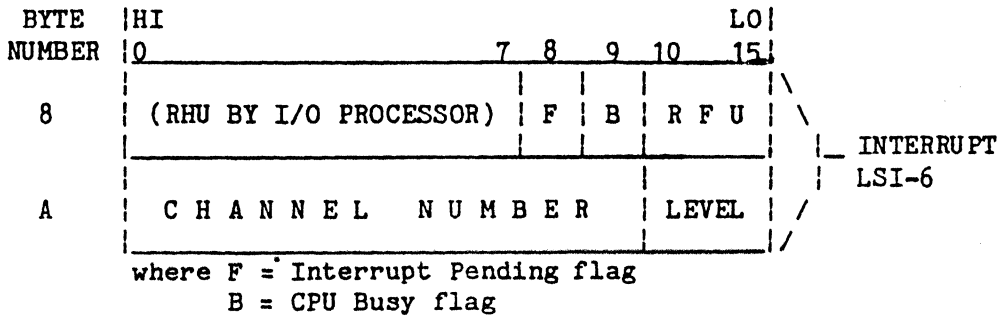


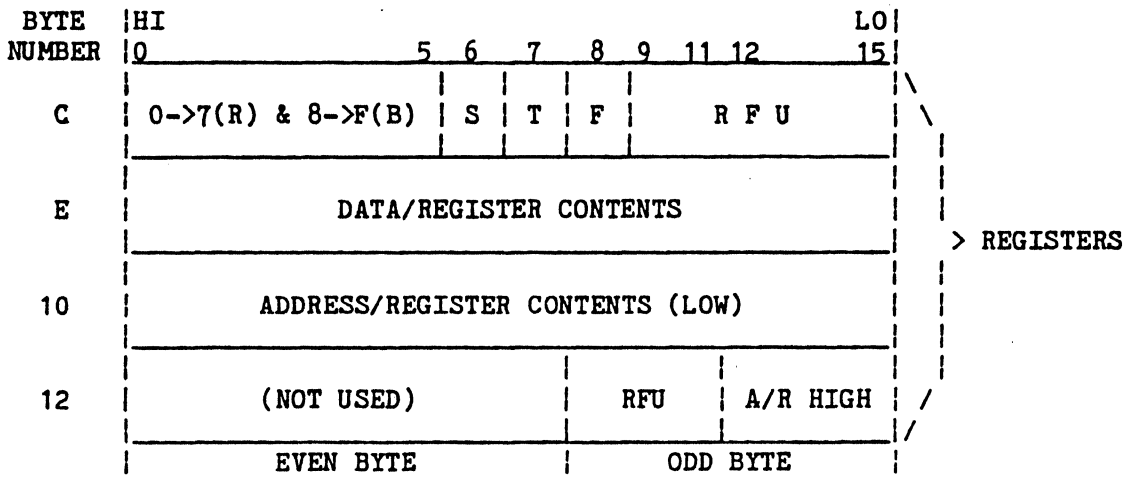
Figure 3-3 Hercules Interrupt Mail Box

3.1.2.3 DATA TRANSFER

All data transfers associated with the WDC are executed in the Direct Multiplex Control (DMC) mode and in the byte format on the IOP bus.

Data transfer procedure is initiated by the CPU loading the IOP with the set up commands, i.e., Configuration Word A, etc., through the I/O Mail Box (see Figure 3-2) and then issuing the Task command which triggers the IOP sequence. The IOP loads the address and range data into the Hercules Register Mail Box (Figure 3-4) for subssequent transfer to the CPU for DMC operation. Standard L6 disk commands are translated by the IOP into the IOP Protocol format (see subsection 5.3) which are then sent to the WDC. When the WDC is ready for data transfer, it makes a DMC request (an interrupt to the CPU) and the data proceeds to the CPU memory without the IOP's direct involvement. The CPU (under DMC control) provides the memory address and the WDC supplies the data to the main CPU memory for each byte of data.

This exchange continues until the end-of-range is indicated by the DMC to the WDC on the last byte of transfer.



where Byte C, bits 0 trough 3:
value 0 to 7 - CPU R register transfer in bytes E and F
value 8 to F - CPU B register transfer in bytes 10, 11, and 13

S = Direction flag:
0 is into the mail box
1 is into the CPU

T = Information type flag for bytes E through 11 and 13:
0 is DMC
1 is Register

F = Register operation in progress when set.

Figure 3-4 Hercules Register Mail Box

3.1.3 Overview of WDC Access

The WDC interface to the 6809 IOP bus emulates a general purpose bi-directional 8-bit wide bus using command and status protocol for communicating with peripheral controllers. Associated with a controller is a set of two registers which can be accessed by the IOP: a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the WDC and may be accessed at any time. The 8-bit Data Register (which actually consists of several bytes in a stack with only one byte presented to the IOP bus at a time) stores data, commands, parameters and WDC status information. Data bytes are read out of or written into the Data Register in order to program or obtain the results after a particular command. The main Status Register may only be read and is used to facilitate the transfer of data.

Commands are initiated by a multi-byte transfer from the IOP, and the result after execution of that command may also be a multi- byte transfer back to the IOP. Each command, therefore, consists of three phases:

- Command Phase - The WDC receives all pertinent information to execute a command
- Execution Phase - The WDC performs the required task.
- Result Phase - After completion of the operation, status and other housekeeping information are made available to the IOP.

SECTION 4 DEVICE INTERFACE

4.1 USER INTERFACES

No specific user action is required to load or initialize the WDC other than those required during subsystem installation for the identification of subsystem configuration. User actions required to load and unload devices are described in appropriate operating guidelines.

4.2 EXTERNAL INTERFACES

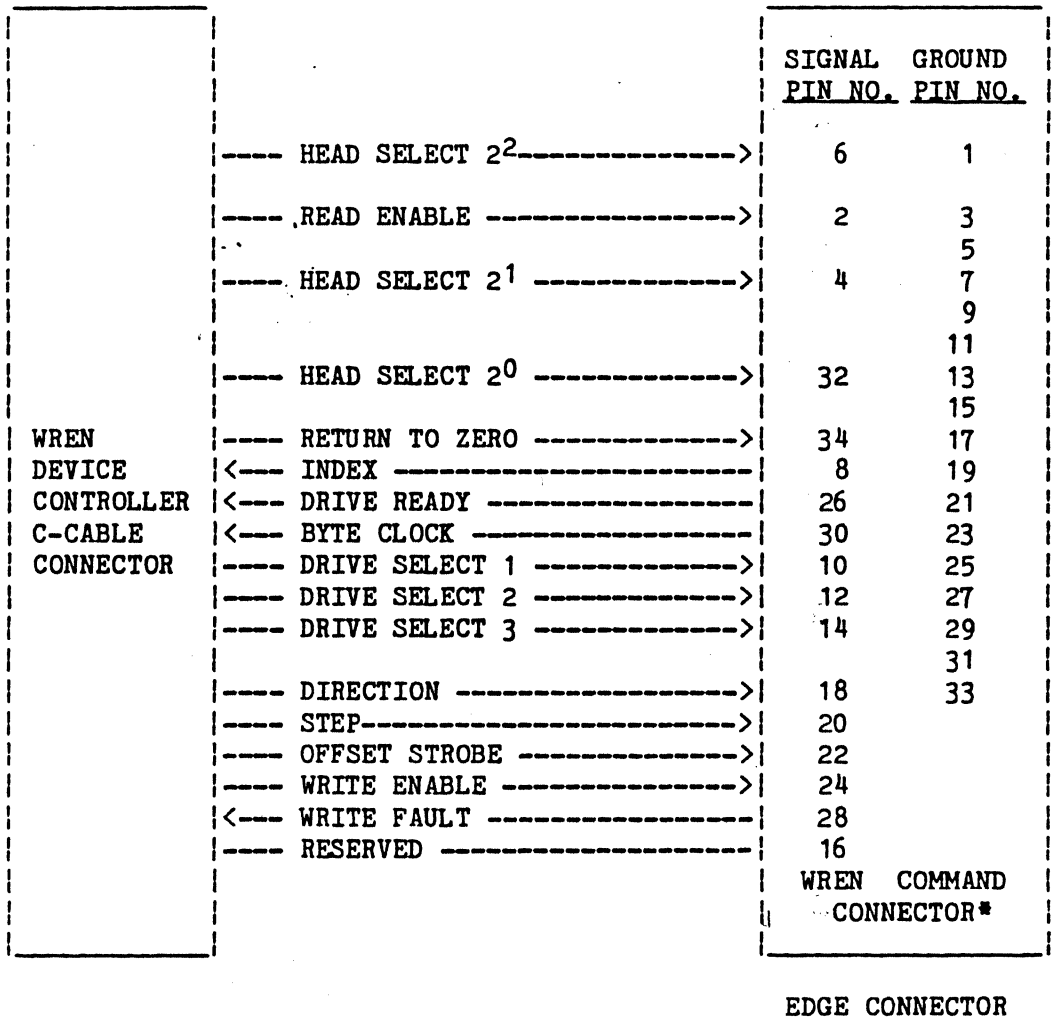
4.2.1 Controller-IOP Interface

The WDC attaches to the IOP bus as a standard Hercules controller. See the Hercules EPS-1 (60144453) subsection 4.6 for more details or refer to section 5.3 of this EPS-1 for specific information.

4.2.2 Wren Device Interface

The appropriate drive specification should be referenced for information more detailed than that presented in this subsection. The drive specification also represents the governing document in terms of drive functionality (see subsection 1.3.2).

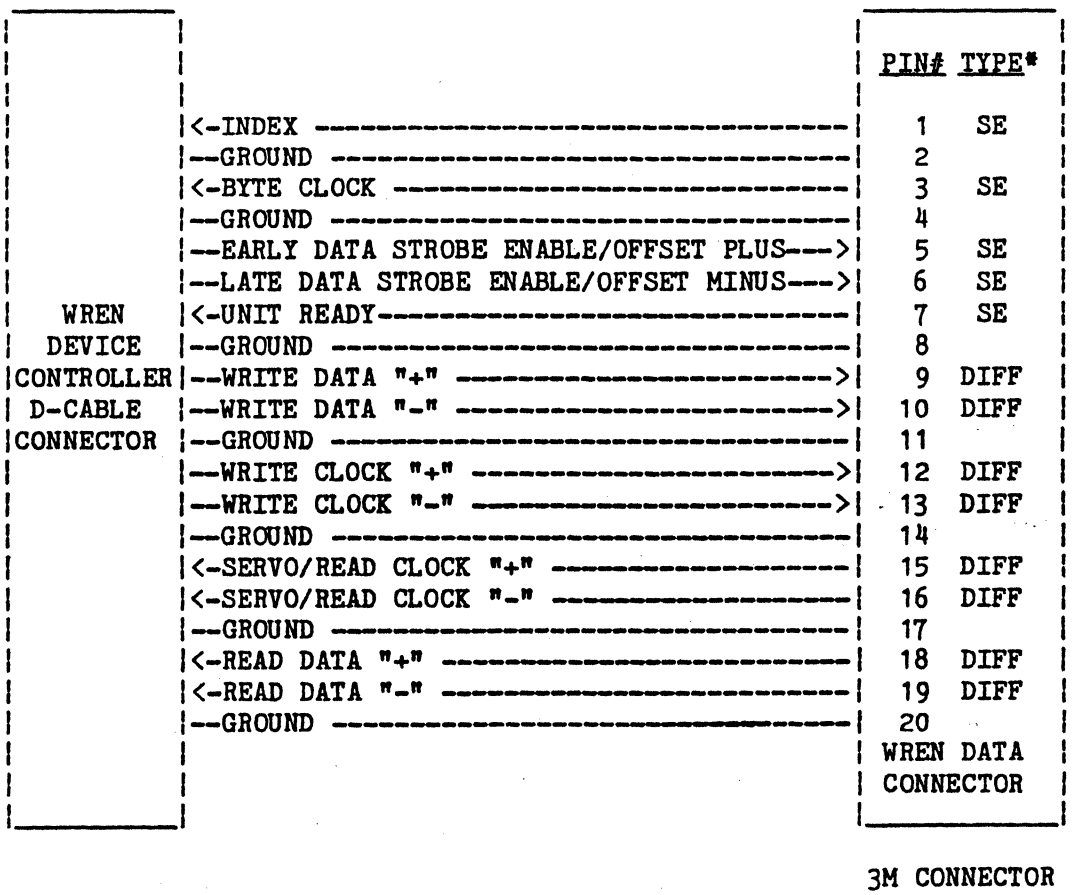
The WDD requires two separate cables for attachment to the WDC. The C-cable and the D-cable provide a radial connection from the drive to the WDC. Figure 4-1 outlines the signals on each cable. Address and control functions are transferred on C-cable lines. The significance of the information on these lines is indicated by the description that follows.



*All signals in the Command cable are single-ended.

a. Command C-Cable (34-pin connector).

Figure 4-1 Wren Device Controller Interface Cables (Sheet 1 of 2)



*SE = Single-ended signal; DIFF = Differential signal.

(D-Cable = Data Cable)

Figure 4-1 Wren Device Controller Interface Cables (Sheet 2 of 2)

4.3 CONTROLLER OUTPUT LINES

4.3.1 Drive Select (1, 2 & 3)

Since only two devices are interfaced to the WDC, Drive Select 1 & 2 are used and the remaining one line can be left unpowered. These input lines are used to gate all command lines to the WDD.

The Unit Select plug located on the base board assembly of the WDD must be set to 1 for drive 1 and 2 for drive two.

Figure 4-2 shows the drive selection timing.

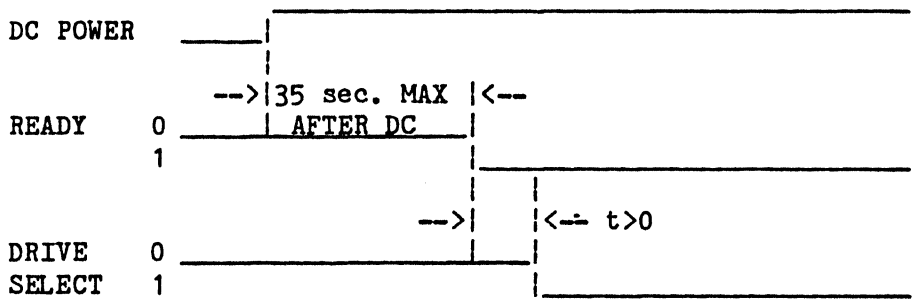
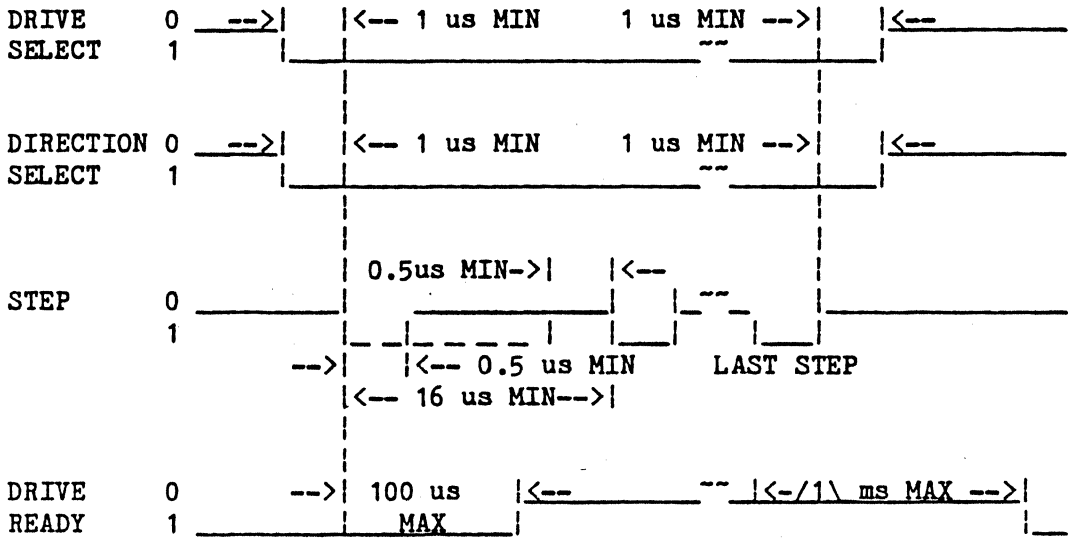


Figure 4-2 Power Turn On and Drive Select

4.3.2 Direction

Direction determines the source of movement of the head-carriage: a logical 1 signifies head-carriage movement toward the higher-numbered cylinders; a logical 0 signifies head-carriage movement toward the low-numbered cylinders (see Figure 4-3).



/1\ - 10 ms for a single track seek (i.e., 1 Step pulse. dependent on Step rate input.

Figure 4-3 Track Access Timing

4.3.3 Step

Step is used with Direction to cause head-carriage movement. Each pulse on the Step line causes the head-carriage to be moved one cylinder in the direction determined by the state of the Direction line.

The rate of head movement is determined by the rate of the in- coming Step pulses; however, the Step pulse rate may exceed the head movement rate. The Drive Ready false indication signifies that a seek is in progress (see Figure 4-3).

4.3.4 Head Select: 2^0, 2^1 x 2^2

These lines are used to select the media and head for data transfer.

HEAD SELECT 2^2	HEAD SELECT 2^1	HEAD SELECT 2^0	HEAD #	FUNCTION	MEDIA
0	0	0	0	Top Head	1st Disk nearest deck casting
0	0	1	1	Bottom Head	2nd
0	1	0	2	Top Head	2nd
0	1	1	3*	Bottom Head	3rd
1	0	0	4*	Top Head	3rd
Remaining Codes are Illegal					

*Invalid for two disk devices.

Drive head line is not affected by any head change (see Figure 4-4).

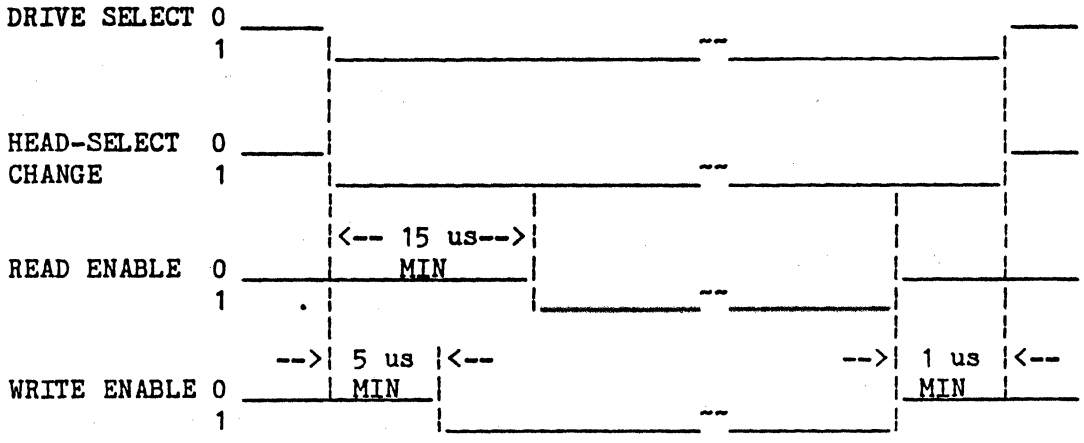


Figure 4-4 Head Select Timing

4.3.5 Return To Zero

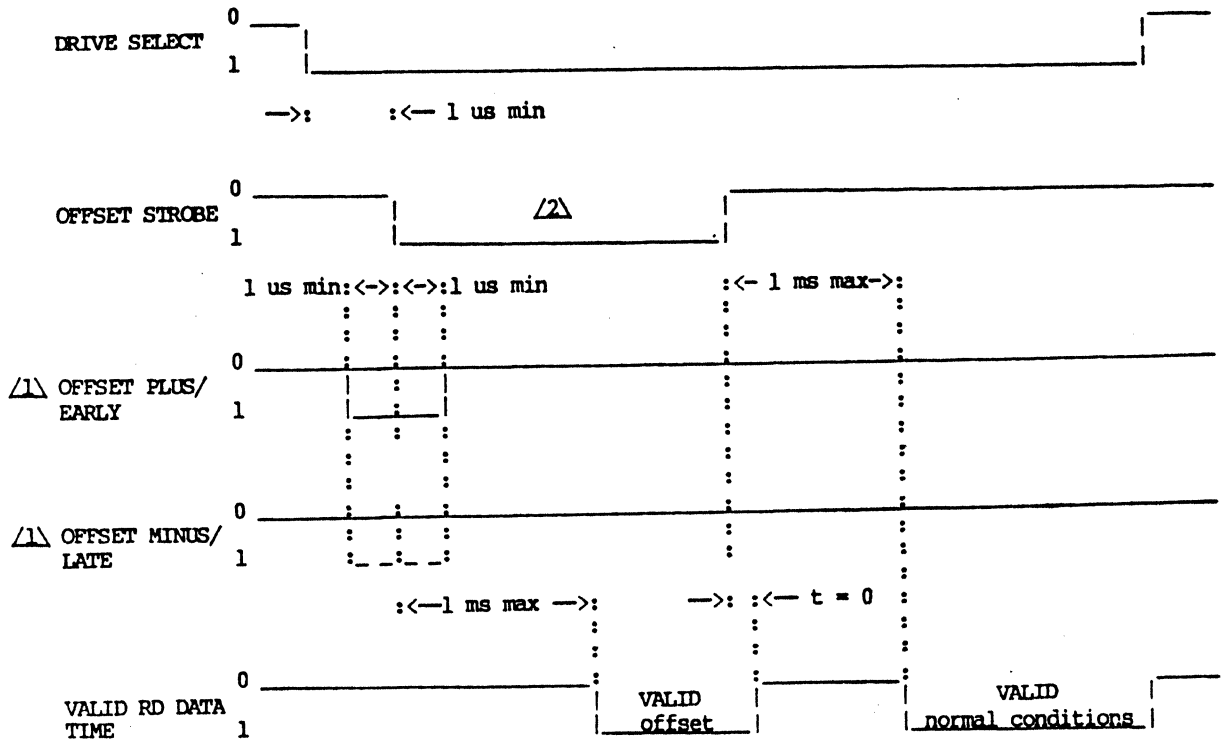
RTZ causes the actuator to return to Zero and resets the "Write Fault" lach. This seek is significantly longer than a seek to track 0 and should only be used for recalibration.

4.3.6 Read Enable

This signal enables the Read Data and Real Clock on the Read/ Servo clock lines.

4.3.7 Write Enable

This signal enables the write drive and initiates recording of the contents of the Write Data lines onto the media (see Figure 4-5 for timing).



/1\ Only one signal line may be inactivated at a time.

/2\ Offset strobe not sllowed during Seek, RTZ or write.

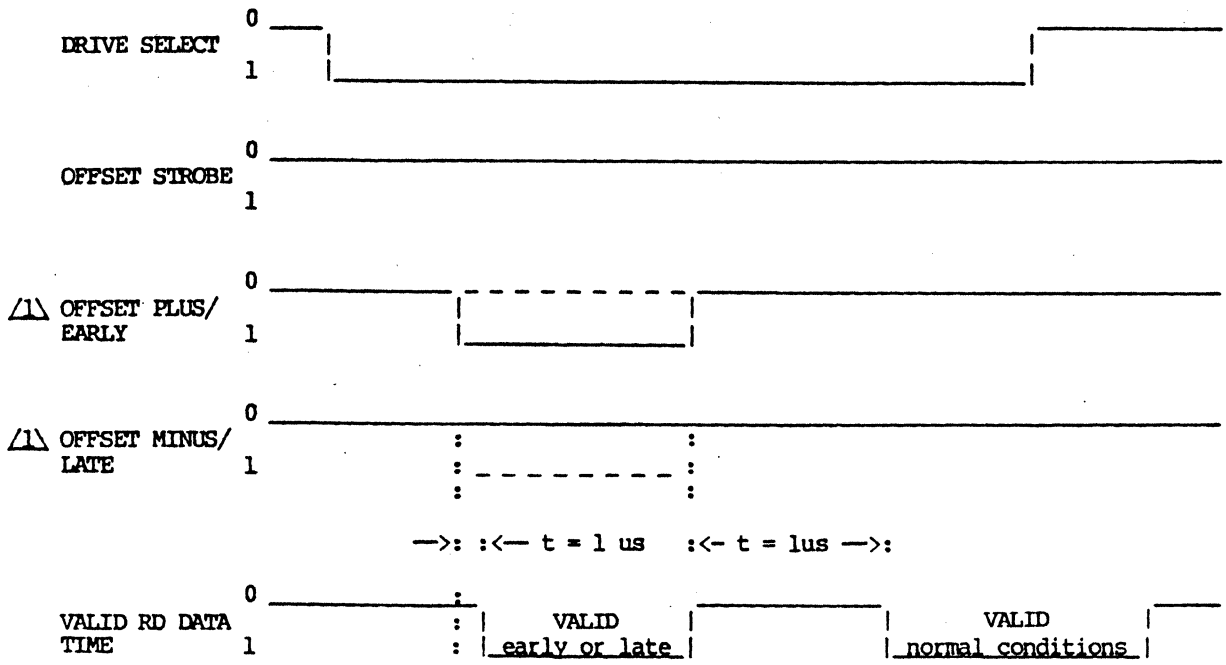
Figure 4-5 Offset Plus/Minus Timing

4.3.8 Early Data Strobe Enable/Offset Plus

This line, when used in conjunction with the Offset Strobe Signal, can be used to obtain three combinations of Plus Offset, Early Data Strobe Enable or both during a Read operation (see Figures 4-5, 4-6 and 4-7).

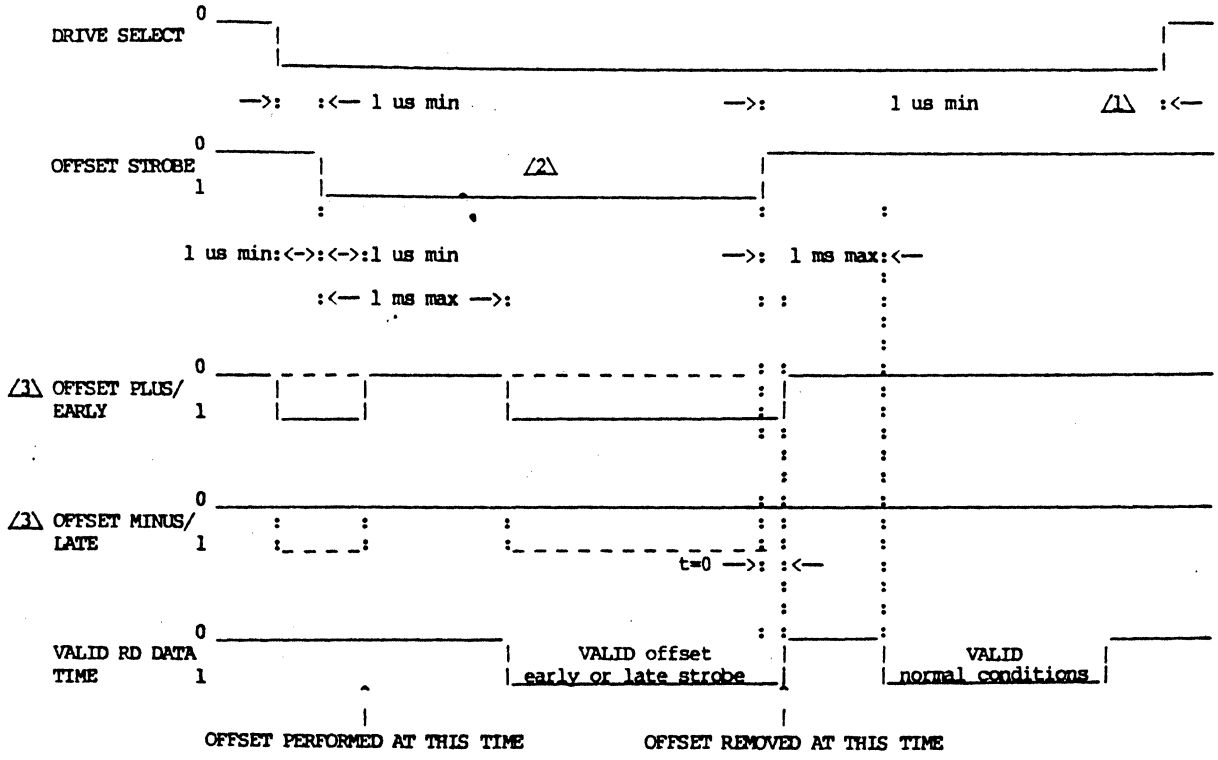
4.3.9 Late Data Strobe Enable/Offset Minus

This line, when used in conjunction with the Offset Strobe Signal can be used to obtain three combinations of the Minus Offset, Late Data Strobe or both during a Read operation (see Figures 4-5, 4-6 and 4-7).



/1\ Only one signal line may be inactivated at a time.

Figure 4-6 Early/Late Strobe Enable Timing



/1\ Offset strobe must be deactivated 1 us prior to selection.

/2\ Offset strobe not allowed during Seek, RTZ or Write.

/3\ Only one signal line can be activated at a time.

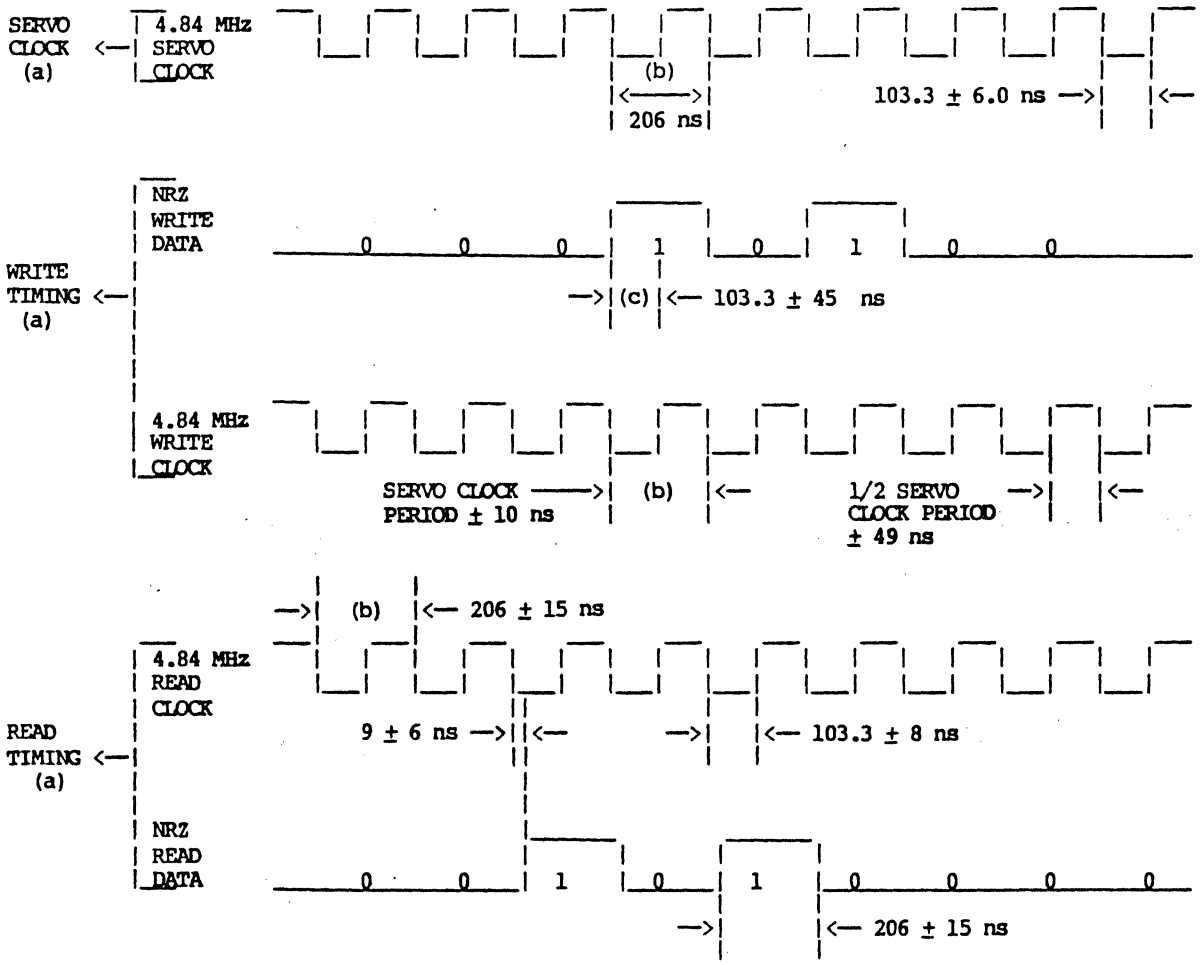
Figure 4-7 Offset Plus/Minus, Early/Late Strobe Timing

4.3.10 Write Data "+" and "-"

These lines carry the balanced differential data to be recorded on the media. The NRZ data is in phase synchronization with the Write Clock signal (see Figure 4-8).

4.3.11 Write Clock "+" and "-"

These lines carry the balanced differential Write Clock signal. The Write Clock is the Servo Clock retransmitted to the drive by the WDC during a write operation (see Figure 4-8).



NOTES

(a) All times in nanoseconds measured at drive I/O connector.

(b) Similar period symmetry shall be ± 3 ns between any two adjacent cycles during reading or writing.

(c) This time (103.3 ± 45 ns) is measured from the activation (or deactivation) of NRZ write data line and rising edge of the write clock line.

All clocks are nominal. A combined spindle speed and clock circuit timing tolerance not exceeding 3% must be taken into account.

Servo clocks are valid when not reading. Other timing is applicable during reading or writing.

Figure 4-8 NRZ Data and Clock Timing

4.3.12 Offset Strobe

This line is used to indicate an actuator offset for the nominal On Cylinder position. The Offset function is intended to be used to aid in the recovery of marginal data that has been previously recorded on the disk media and should only be utilized after rereads without actuator offset have been attempted. This line is available on the 34-pin interface only.

4.3.13 Reserved

This is not used by the Wren Disk Drive.

4.4 CONTROLLER INPUT LINES

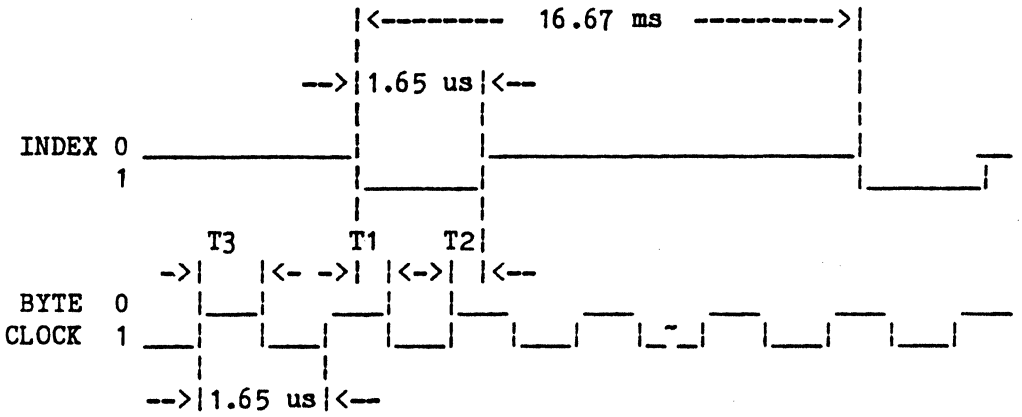
4.4.1 Drive Ready

When true, this line indicates that the disk is up-to-speed and the actuator is on cylinder and not executing a seek or an RTZ function. This line is generated with Drive Select and it also is available as Unit Ready on the D-cable where it is not gated with Drive Select.

4.4.2 Index

Index, which occurs once per revolution, indicates the physical beginning of a cylinder (see Figure 4-8).

This signal is contained in the C-cable gated with Drive Select; it is also available in the D-cable not gated with Drive Select. The relationship of Index and Byte Clock timing is shown in Figure 4-9.



where T1 = 0.2 microsecond to 0.41 microsecond
T2 = 0.41 microsecond to 0.53 microsecond
T3 = 0.83 microsecond

Figure 4-9 Index and Byte Clock Relationship

4.4.3 Byte Clock

Byte Clock occurs once per eight Servo Colck periods. There are 10,080 byte clocks per disk revolution at a minimal rate of 605 KHz. Interrelationship of Index and Byte Clock are shown in Figure 4-9.

4.4.4 Write Fault

Write Fault conditions detected by the Wren disk drive activate the Write Fault signal. It remains active until it is deactivated by either the Fault Reset signal or by power sequencing of the drive.

The Write Fault condition occurs when:

- o Write current is absent
- o Write data is absent
- o The disk is not ready
- o Invalid head or internal multiple heads are selected
- o Read Enable is true
- o Offset Strobe is true.

4.4.5 Unit Ready

This signal is the same as Drive Ready but without being gated by Drive Select.

4.4.6 Servo/Read Clock "+" and "-"

These balanced differential lines contain the device-generated Read Clocks if the Read Enable signal is true; or, the drive generated Servo Clocks, when the Read Enable is false. These lines are not gated with the Drive Select signal.

4.4.7 Read Data "+" and "-"

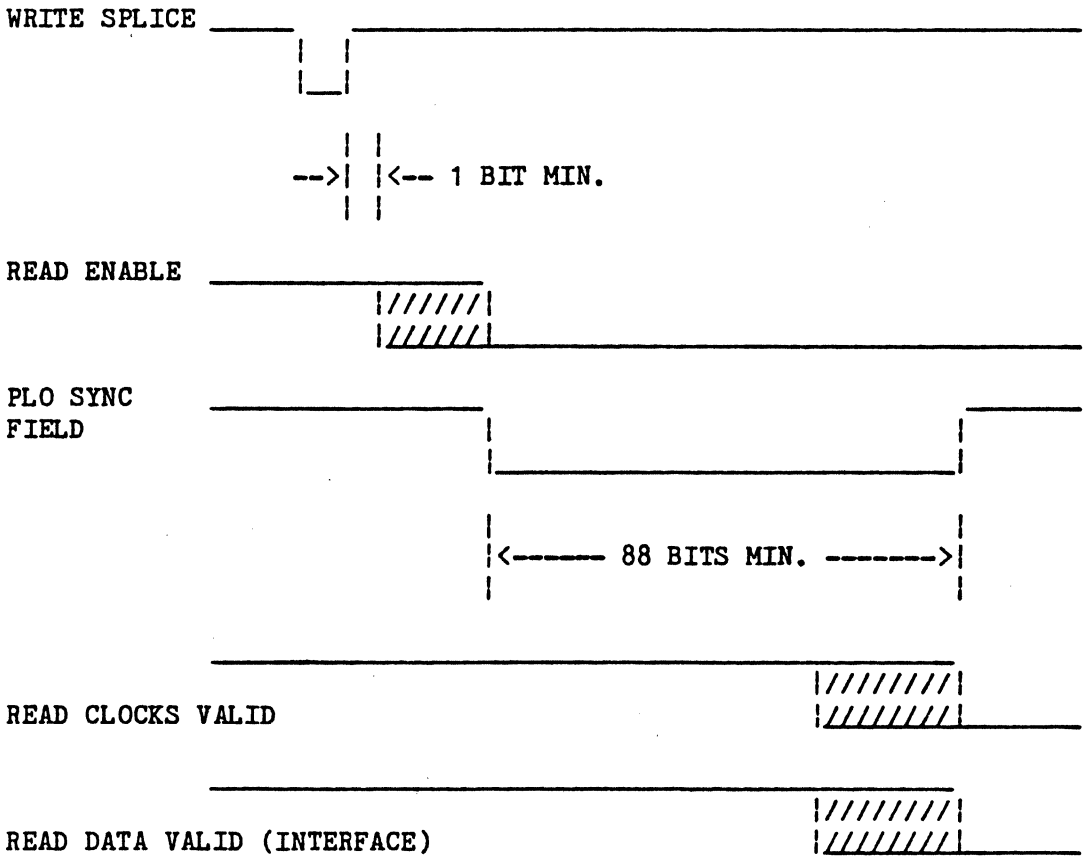
These balanced differential lines transmit the recovered data from the media in the NRZ form from the FDD to the FDC. This data is in frequency and pulse synchronization with the Read Clock as specified in Figures 4-8 and 4-10.

4.5 DATA FORMAT

4.5.1 Format Definition

The record format on the disk is under control of the control- ler. The Index pulse and byte clocks are available for use by the controller to indicate the beginning of a track and to allow the controller to define the beginning of a sector. A suggested format for fixed-length data records is shown in Figure 4-11.

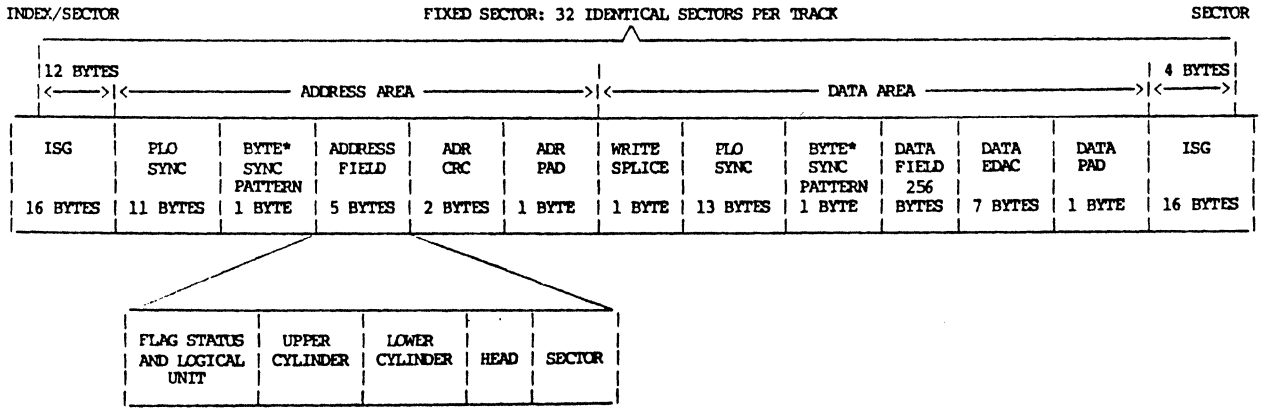
The format presented in Figure 4-11 consists of three functional areas: Intersector Gap, Address and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the disk where the Data areas are to be recorded. This section refers to a Sector pulse which is generated internally to the controller from the Byte clock to ease the format description.



NOTE

Read Enable must be deactivated prior to the Write Splice. Read Enable may be reinitiated at least one bit after the Write Splice and with at least 11 bytes of PLO SYNC remaining in the sync field.

Figure 4-10 Read Timing



DATA FIELD LENGTH USING 32 SECTORS

DATA FIELD = $\frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}}$ = (SYNC FIELDS, TOLERANCE GAPS, AND ADDRESSES

DATA FIELD = $\frac{10080}{32}$ = 315

DATA = 256 BYTES/SECTOR

EFFICIENCY = $\frac{256 \times 32}{10080}$ = 81%

*Byte Sync pattern = FE

Figure 4-11 Sector Format

4.5.2 Intersector Gap, ISG

The Intersector Gap is 16 bytes long for the WDD, and is oriented to begin before Index (Sector) pulse and end after Index (Sector) pulse (see Figure 4-11).

4.5.3 Address Area

The Address area is used to provide positive indication of the track and sector locations. The Address area is normally read by the controller and the address field bytes verified prior to a data area read or write. The Address area is normally only written by the controller during a format function, and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The Address area consists of the following bytes:

1. PLO Sync (11 bytes minimum) - These 11 bytes of Zeros are required by the drive to allow the drive's read-data-phase- locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

2. Byte Sync Pattern (1 byte) - Standard format - FE; it indi- cates to the controller the beginning of the address field information, and it establishes byte synchronization (ability to partition serial bit stream into meaningful groupings, such as bytes).

3. Address Field - These bytes are as shown and interpreted by the controller. The format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address, and one byte to define the sector address.

4. ADR CRC (Address Field Check Codes) - Selection of an appropriate error-detection mechanism, such as a cyclic redundancy check (CRC) code, is made by the hardware and applied to the address for file integrity purposes. These codes are generated by the controller and written on the media when the address is written. Data integrity is maintained by the controller recalculating and verifying the address field check codes when the address field is read.

5. ADR Pad - (Address Field Pad) - The Address Field Pad bytes must be written by the controller and are required by the drive to ensure proper recording and recovery of the last bits of the address field check codes.

4.5.4 Data Area

The data area is used to record the data fields. The contents of the data fields within the data area are specified by the CPU, DMC and memory. The remaining parets of the data area are specified and interpreted by the controller to recover the data fields and ensure their integrity. The data area consists of the following:

1. Write Splice (one byte) - This byte area is required by the drive to allow time for the write drivers to turn on and reach a recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format.

2. PLO Sync (13 bytes) - These 13 bytes of Zeros are required when reading to allow the drive's phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

3. Byte Sync Pattern (one byte) - Standard format - FE. This byte indicates to the controller the beginning of the data field bytes and establishes byte synchronization for the data field.

4. Data Field - The data field contains the 256 bytes of CPU defined data.

5. Data EDAC - (Data-Field Check Codes) - These codes are generated by the controller and written on the mdeia with the data field. The controller maintains data integrity by recalculating and verifying the data field check codes when the data field is read.

6. Data Pad - (Data Field Pad) - The Data Field Pad bytes must be written by the controller and are required by the drive to ensure proper recodring and recovery of the last bits of data field check codes.

SECTION 5 INSTRUCTIONS

5.1 GENERAL

Two configuration words are required to define data access on a disk device. Configuration words A and B contain the image of the ID field of the sector on which a particular operation is initiated. Data access is defined via four hierarchical elements split between the two configuration words. In order to provide for the potential growth of WDD disk type devices, the following guidelines are established for the distribution of the four hierarchical elements in the two configuration words.

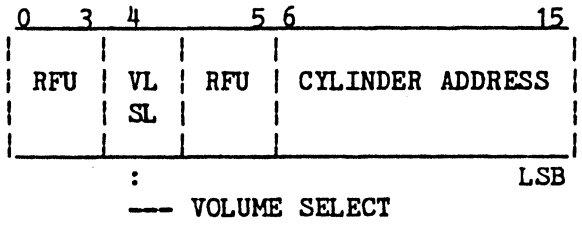
1. Bits 0 through 5 of configuration word A are reserved for use as a magazine address. Magazine selection applies to a device which has more than one physically identifiable media. For example, a cartridge disk device may have a fixed media and a removable media.

2. Bits 6 through 15 of configuration word A are reserved for use as a cylinder address.

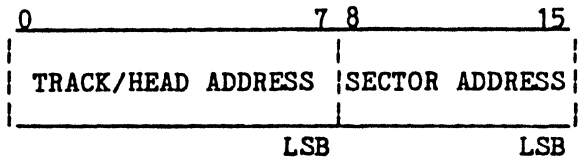
3. Bits 0 through 7 of configuration word B are reserved for use as a track/head address.

4. Bits 8 through 15 of configuration word B are reserved for use as a sector address.

Configuration Word A:



Configuration Word B:



In multisector data transfer operations (Read or Write), the controller enables an automatic track and cylinder function. Track switching occurs whenever the last logical sector on the track has been completed and the range has not expired. Note that track switching is not associated with index mark but with equality with the last sector number. When the last track of the cylinder has been completed and track switching is attempted, the WDC initiates a seek to the next consecutive cylinder number, selects track number Zero, and initiates a search for sector number Zero.

Additional considerations are:

- Data transfer continues until the DMC range expires, an error is encountered, an unsuccessful search occurs, or the end of the last cylinder is detected (setting bit 5 of the status word).
- Automatic track switching does not occur for any format operation or any unsuccessful search (detection of two index marks without a successful compare).
- When track completion is detected without an error and the range has not expired, the configuration words are modified to reflect the next consecutive track and sector Zero. In addition, if cylinder completion is also detected, the configuration words are modified to reflect the next consecutive cylinder, and track and sector Zero. Note that this update occurs only if the EOT sector number has been reached and end of range has not been reached.
- An attempt to automatically switch off the last track of the last cylinder results in status bit 5 being set (except in the case where the range has been decremented to Zero).
- Both track and cylinder switching occurs within the fixed disks selected by the configuration words.

The functionality described above enables software to access records in sequential order without having to reload the sector ID argument for every operation on a particular track or cylinder.

5.1.1 I/O Commands

All I/O commands are addressed by the CPU into the IOP I/O Mail- box (see Figure 3-2) which are shown in subsection 5.2 for each in- struction.

The IOP communicates with the WDG by means of a protocol de- scribed in subsection 5.3.

Figure 5-1 is a representation of a command flow chart.

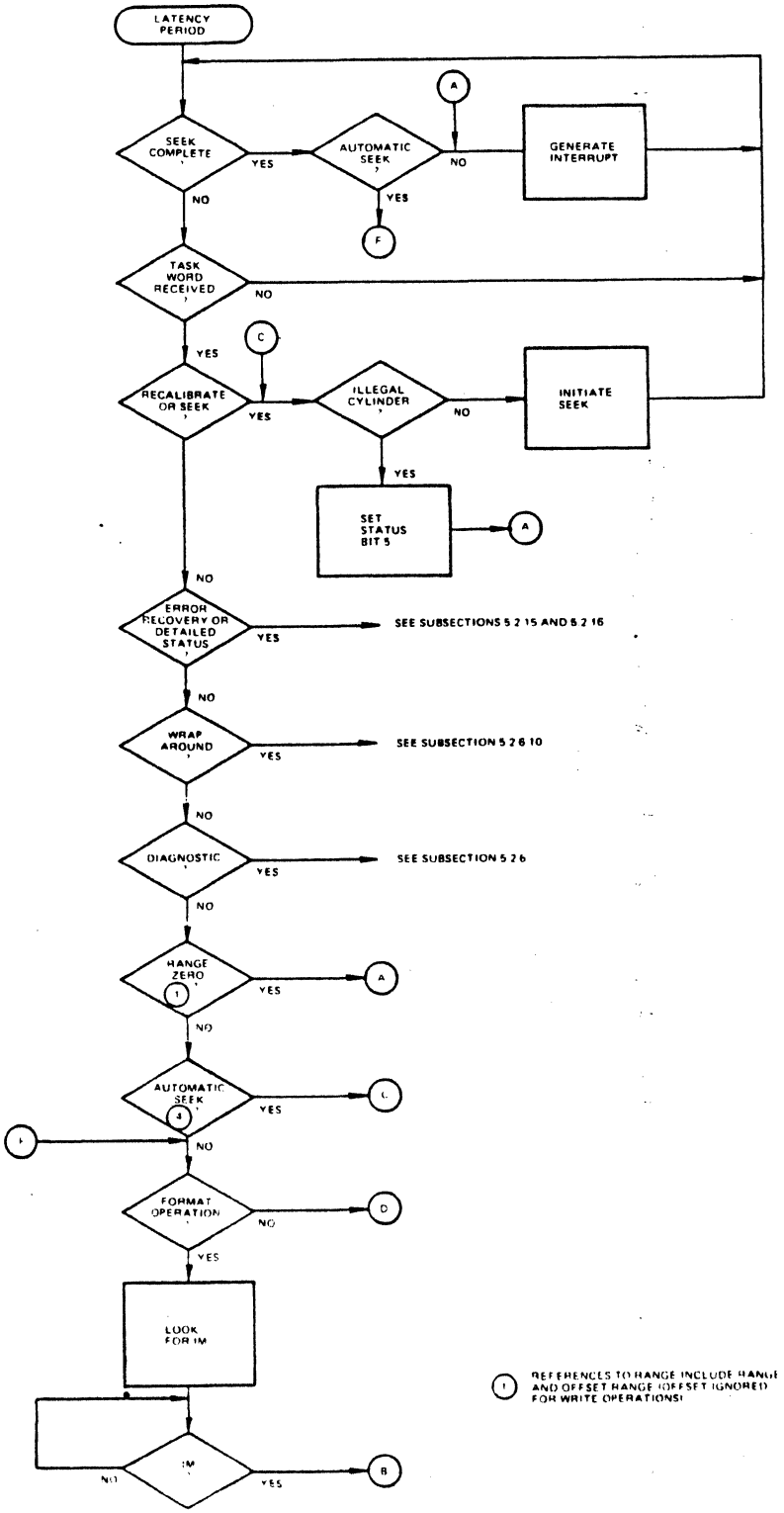


Figure 5-1 Command Flow Chart (Sheet 1 of 2)

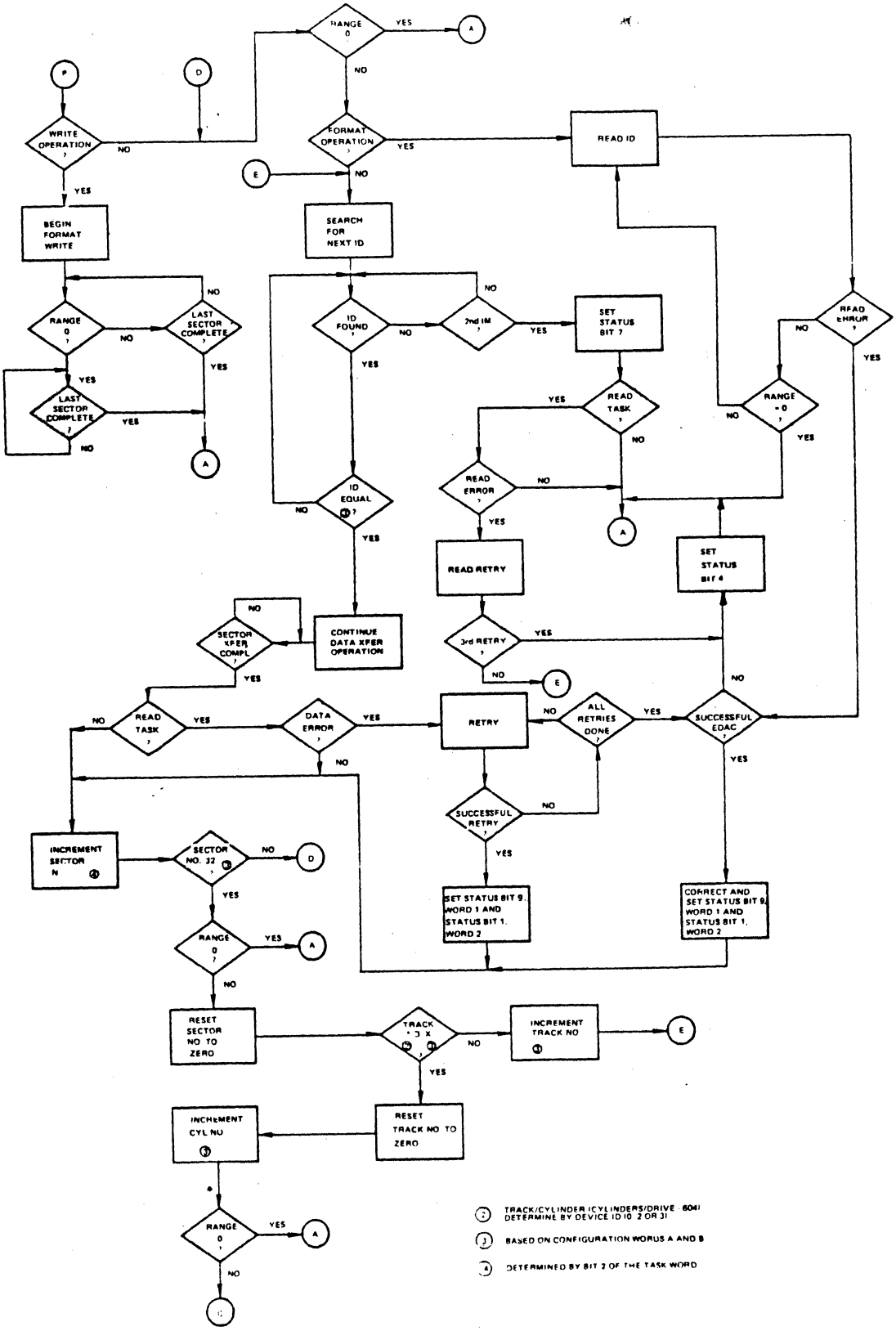


Figure 5-1 Command Flow Chart (Sheet 2 of 2)

5.2 INSTRUCTIONS

The Level 6 instructions supported by the IOP are listed in Table 5-1 with detailed instruction description following.

Table 5-1 Instructions

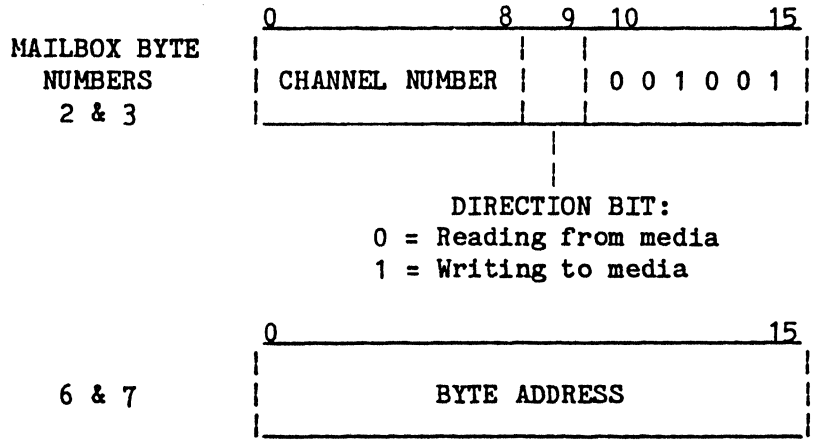
TYPE	FUNCTION CODE (HEX)*	INSTRUCTION	SUBSECTION REFERENCE
Output	09	IOLD	5.2.1
		Address (09)	
		Range (0D)	
	11	Configuration Word A	5.2.2
	13	Configuration Word B	5.2.3
	15	Configuration Word C	5.2.4
	03	Interrupt Control	5.2.5
	07	Task Word	5.2.6
	01	Control Word	5.2.7
Input	08	Memory Byte Address	5.2.8
	0A	Memory Module Address	5.2 9
	0C	Range	5.2.10
	10	Configuration Word A	5.2.11
	12	Configuration Word B	5.2.11
	14	Configuration Word C	5.2.11
	02	Interrupt Control	5.2.12
	26	Identification Code	5.2.13
	06	Task Word	5.2.14
	18	Status Word 1	5.2.15
	1A	Status Word 2	5.2.16
	0A	QLTIs	5.2.17
	04	Firmware Revision (LSB)0	5.2.18
	20	Retry Count	5.2.20
Diagnostic	Any Even Code	Read IOP Registers	5.2.21
	Any Odd Code	Write IOP Registers	5.2.21
	00 to 27 Hex Only		

*All other function codes are RFU.

5.2.1 IOLD

The I/O Load (IOLD) instruction is transformed by the CPU into the Output Address and Output Range instructions on the CPU bus. Each IOLD instruction results in an Output Address instruction followed by an Output Range instruction.

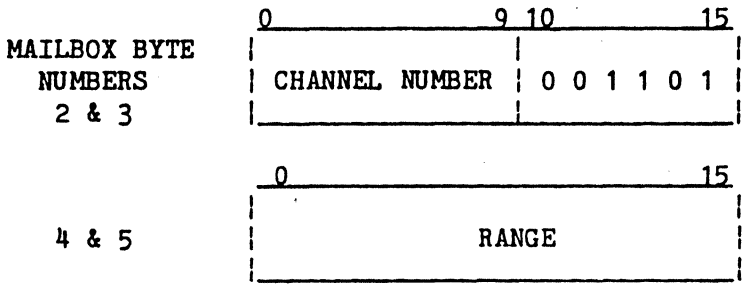
5.2.1.1 OUTPUT ADDRESS



This instruction loads a 16-bit address into the address register of the I/O Mailbox for the referenced channel. The address refers to the starting (byte) location in main memory where the DMC commences input or output data transfers. The most significant four bits of the Address are passed on to the IOP via a hardware register and the data bus contains the 16 least significant bits. Data transfers to or from memory are normally on a word basis, but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

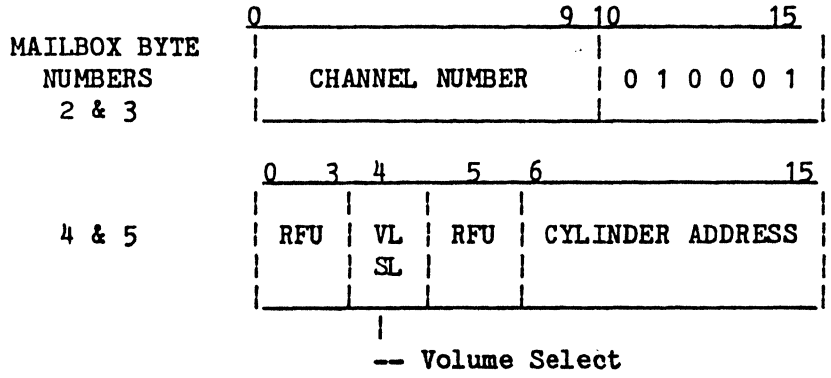
Bit 9 of the address bus (direction bit of the channel number) determines the direction of any subsequent data transfer operation. A logical One specifies an output operation (writing on media) while a logical Zero specifies an input operation (reading from media).

5.2.1.2 OUTPUT RANGE



This instruction loads the range register associated with the referenced channel. The (16-bit) quantity loaded (data bus) is the number of bytes to be transferred during the DMC data transfer that is being set up. The number is a positive binary quantity and is decremented by the DMC after each memory transfer. A range of Zero results in a premature End-of-Operation termination for any Read or Write command that may be subsequently issued (refer to subsections 5.2.6.3 through 5.2.6.9). The DMC operation is described in subsection 3.1.2.3.

5.2.2 Output Configuration Word A

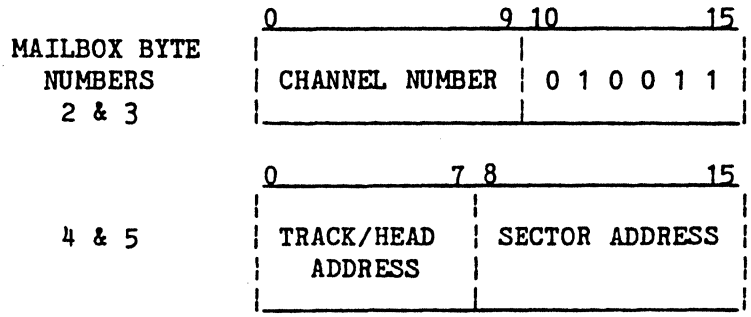


This instruction loads configuration word A for the device corresponding to the referenced channel. The cylinder address (bits 6 through 15) is used as the seek argument during Seek operations. The complete word is used as the two high-order bytes of a sector ID field to be searched for during a search and Read or Write operation. Bits 0 through 3, and bit 5 are reserved for future use (RFU). Bit 4, the volume select bit, is defined as:

- o 0 = Removable volume
- o 1 = Fixed volume.

For the Wren drive, bit 4 = 1 always.

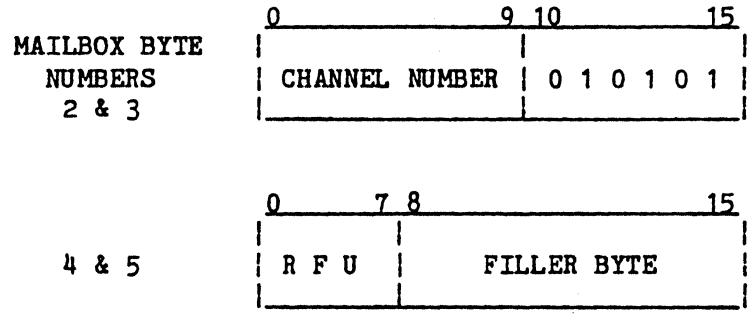
5.2.3 Output Configuration Word B



This instruction loads configuration word B for the device corresponding to the referenced channel. This word is used as the low-order two bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0 through 7 provide the track address for any Read or Write operations.

The subsystem treats bits 8 through 15 of configuration word B as a sector number. This number is incremented after operating on a data field during a data field Read or Write operation (see subsection 5.2.6).

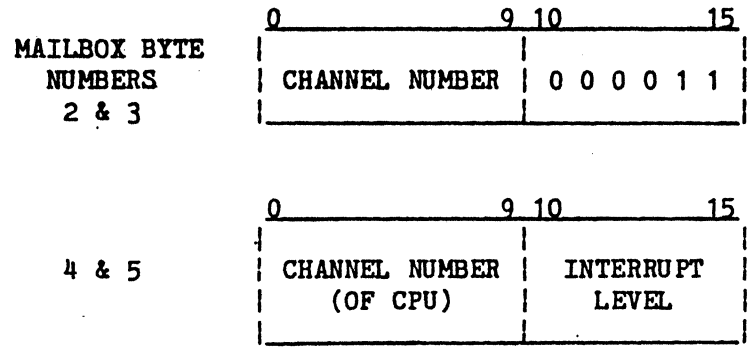
5.2.4 Output Configuration Word C



This instruction loads Configuration Word C of the referenced channel. The low order byte of Configuration Word C is used for filling the data field during the execution of a Format Write instruction. The filler byte is initialized to 00.

5.2.5 Output Interrupt Control

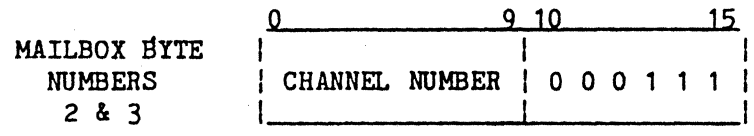
NOT USED
ALWAYS WRITES 3



This instruction loads the interrupt level of the CPU to which subsequent interrupts should be sent. The level number is a 6-bit quantity and is positioned on the data bus as illustrated above.

If an interrupt level of Zero is loaded, the subsystem does not generate or save interrupts for any events that occur while the interrupt level is Zero. The interrupt level is set to Zero whenever the subsystem is initialized.

5.2.6 Output Task Word



4 & 5

	0 1 2 3 4 5 6 7	8	9 10 11 12 13 14	15
	COMMAND CODE		AS DEFINED	
Recalibrate	0 0 0 0 0 0 0 0	0	MBZ	0
Seek	0 0 0 0 0 0 0 1	0	MBZ	0
Format Write	1 0 A R R 0 0 0	0	MBZ	0
Read/Write Data	1 0 A R R 0 0 1	0	MBZ	0
Diagnoctic Read/Write Data	1 0 A R R 0 1 1	0	MBZ	0
Format Read ID	1 0 A R R 1 0 0	B	MBZ	0
Wraparound Read/Write Buffer	1 1 0 0 0 0 0 0	0	MBZ	B
Diagnostic Error Log Buffer Read/Write	1 1 0 0 0 0 1 0	0	MBZ	0

where: A = Automatic Seek Bit
B = Specific meaning for the command
R = RFU (Reserved for Future Use)

This instruction outputs a task word to the referenced channel. The coding of bits 0 through 7, illustrated above, represent the operations that are to be performed. When this instruction is accepted, the channel enters the busy state and the indicated task is initiated or stacked. All address, range, and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low-order bit of the most recent output address instruction (refer to subsection 5.2.1.1). For example, if the data field encoding of the task word is received when a read channel number is indicated, then a Read Data command is executed. Note that track selection is performed for each media data transfer command prior to initiation of the data transfer and is based on the current contents of the configuration word B.

Bits 2 through 4 of the command code have specific meaning for all media data transfers as follows:

1. Bit 2 - Automatic Seek - If this bit is a logical Zero, the data transfer is initiated based on the current cylinder position of the drive.

   If this bit is a logical One, a Seek Cylinder operation, based on the current contents of configuration word A, is initiated to the drive. At Seek completion, no Seek complete interrupt is generated to the CPU and the specified data transfer operation is initited.

   If a seek is initiated to the current cylinder a delay of, approximately, 250 microseconds is entered before data transfer can be initiated.

2. Bits 3 and 4 - Reserved for future use and must be Zero.

NOTE

Bits 3 & 4 of the Output Task Word, for rigid disks, are "don't care" bits on controllers that do not have these options:

- o Bit 3 - Sector size bit
- o Bit 4 - Automatic RPS

An additional function of the task word is that it causes device-detailed status to be reset.

The IOP utilizes the Task Word commands and translates them into the WDC type commands (see subsection 5.3) which are multi-byte transfers from the IOP during the Command Phase. After the Execution Phase in the WDC, the Result Phase can also be a multi-byte transfer back to the IOP (see subsection 3.1.3 for Overview of Disk Accesses).

5.2.6.1 RECALIBRATE

The Recalibrate command causes the channel to move the device's positioner to cylinder Zero, select track Zero. This instruction is intended as an Initialization command to guarantee that the positioner location information in the WDC is correct and that all device faults are cleared. Completion of the recalibration operation by the device results in a Device Ready transmission to the WDC.

5.2.6.2 SEEK

The Seek command in the task word causes the channel to move the device's positioner to the cylinder indicated in configuration word A. If the cylinder specified is greater than the largest available cylinder or an error occurs during positioner movement, then an error bit is set in the status word (refer to subsection 5.2.16). Completion of a positioning operation (whether or not any physical movement occurred) by the device results in the generation of an interrupt. Note that Seek completion as a result of an automatic Seek (see subsection 5.2.6) does not result in an interrupt.

5.2.6.3 FORMAT READ ID

The Format Read ID command causes the channel to read all Identifiers (IDs) on a track beginning with the first sector after index and in the order in which they are recorded. IDs are transferred to memory beginning at the memory location specified in the subsystem's memory address register.

This address is the address loaded by the most recent Output Address IOLD instruction if no data transfer has occurred since that instruction was executed. If one or more data transfer operations have been executed since the last Output Address IOLD instruction, then the starting memory address used for this operation is the byte address immediately following the end of the most recent data transfer executed for this device (either read or write).

If Bit 8 of the Command code is a One, then the CRC bytes of any sector identifier read are ignored. If bit 8 of the Command code is a Zero, then the CRC bytes of any sector identifier read are checked.

Data is transferred until an uncorrectable read error occurs (except as noted for bit 8), the range is satisfied, or the entire track is read (index is detected).

Normal range for this command (to read one complete track) is:

$$R = 4 \times 32 = 128 \text{ bytes},$$

where 4 = number of bytes in ID and 32 = number of sectors per track.

If this command is terminated due to end of track before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.10). An uncorrectable read error in any field (except as previously noted for bit 8 of the Command code = 1) causes the operation to be terminated with the read error bit set in the status word (bit 4). The field in error can be determined through examination of the residual range. (If a read error is detected in an ID field the range is decremented for the ID field only.) The controller spaces the data field without verifying the EDAC.

NOTE

Format Write ID codes 000 and 100 have the same functionality (see Table 5-2).

Read errors can occur on re-allocated sectors which were found to contain uncorrectable errors.

If the range register is Zero when this command is received, the task is immediately terminated (End-of-Operation). No data is read or transferred. Track selection for the operation is based on the current contents of the track address of configuration word B.

Table 5-2 Data Transfer Commands

COMMAND	SUBSECTION	TRANSFERS ID	VALID ID EDC	TRANSFERS DATA	VALID DATA EDAC	MULTITRACK	COMMENTS
Format Write	5.2.6.4	Yes	Yes	No	Yes	No	
Read Data	5.2.6.5	No	Yes	Yes	Yes	Yes	Begins at first
Write Data	5.2.6.6	No	Yes	Yes	Yes	Yes	AM, includes EDAC
Diagnostic Read Data	5.2.6.8	No	Yes	Yes	No	No	
Diagnostic Write Data	5.2.6.7	No	Yes	Yes	No	No	
Format Read ID	5.2.6.3	Yes	*	No	No	No	
Format Write	5.2.6.4	Yes	Yes	No	Yes	No	

*The EDC bytes will not be checked if bit 8 of the Task Word equals One.

5.2.6.4 FORMAT WRITE

The Format Write command causes the channel to format the track which is positioned under the read/write head specified by Configuration Words A and B when this command is received. Thirty-two equal length sectors are written starting at index. The sector ID fields are read from memory, beginning with the memory location specified in the subsystem's DMC address register (refer to subsection 5.2.6.3). Bit 8 is Zero for this command.

The data fields are filled by the WDC with a Configuration C pattern consisting of the repetative filler byte (see subsection 5.2.4).

The range to format one complete track is:

$$R = 4 \times 32 = 128 \text{ bytes.}$$

If a range other than 128_{10} is specified, Program Error Bit 5 is set to One in Status Word 1. *Error Log cylinder Format Write is described in subsection 5.3.4.2.

If the range register is Zero when this command is received, the task is immediately terminated (End-of-Operation). No data is written.

5.2.6.5 READ DATA

The Read Data command causes the channel to locate the sector defined by the sector ID image loaded in configuration words A and B and to begin transfer of the data field of (at least) that sector to main memory. Data is transferred to memory beginning with the memory location specified in the subsystem's DMC address register and continues until the range is satisfied. When the transfer of the first specified sector data field is completed (without error), the sector number field of configuration word B is incremented. If the initial range was greater than 256, then the sector on that track represented by the updated contents of configuration words A and B is located and data transfer continues with the new sector's data field. This operation continues until either the range is satisfied, an uncorrectable read error occurs, or the record specified by configuration words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful compare*). If the specified record cannot be located, an unsuccessful search is posted in the status word (bit 7). Note that track and cylinder switching may occur as described in subsection 5.1.

Track selection for the operation is based on the current contents of the track address of configuration word B.

If an uncorrectable read error is encountered (reread 27 times and check EDAC once, subsection 5.3.2) in a data field, the operation is terminated and the read error bit in the status word is set (bit 4). The sector number field of configuration word B contains the address of the record in error.

If a CRC error is encountered in an ID field*, a miscompare result is assumed and the search continues. In this case the read error bit is posted in the status word so that, if the desired record is never located, the operation is terminated with both the unsuccessful search bit and read error bit posted in the status word, indicating that the reason for the miscompare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset.

If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.10). If the range register is Zero when this command is received, the task is immediately terminated (End-of-Operation). No data is read or transferred.

5.2.6.6 WRITE DATA

EACH WRITE TO ERROR LOG ONLY REALLOCATES LAST SECR ENTERED IN L

The Write Data command causes the channel to locate the sector defined by the sector ID image loaded in configuration words A and B and to rewrite the data field of at least that sector. The data is read from memory, beginning with the memory location specified in the subsystem's DMC address register. Rewritten data fields are preceded by data field sync words (see Figure 4-8). When the transfer of the specified sector is completed, the sector number field of configuration word B is incremented.

If the range is less than 256, the remainder of the data field is Zero filled. If the range is greater than 256, the sector represented by the updated contents of configuration words A and B are located and the data field rewritten. This operation continues until either the range is satisfied or the record specified by configuration words A and B cannot be located on the track (as indicated by the detection of two index marks without a successful ID field compare*). If the latter event occurs, the unsuccessful search bit is posted in the status word (bit 7). Note that track and cylinder switching may occur as described in subsection 5.1.

If a CRC error is encountered in an ID field*, the ID value is ignored and the search continues. In this case the read error bit is posted in the status word so that, if the desired record is not located, the operation is terminated with both the unsuccessful search bit and the read error bit posted in the status word, indicating that the reason for the miscompare is a read error in the sector ID. If the search is eventually successful, the read error bit in the status word is reset with Status Word 1 bit 9 set and Status Word 2 bit 9 set.

If this command is terminated before the range is satisfied, the residual range is available via the Input Range command (refer to subsection 5.2.10). If the range register is Zero when this command is received, the task is immediately terminated (End-of-Operation). No data is written.

Track selection for the operation is based on the current contents of the track address of configuration words A and B.

*See Sector Reallocation, subsection 5.3.4.2, Additional Observations.

5.2.6.7 DIAGNOSTIC WRITE DATA

The Diagnostic Write Data command causes the channel to perform as if the Write Data command is specified, except that EDAC characters are written at the end of the data field updated as read from memory (not hardware generated). Only one sector can be updated by this command so that the range must equal 263 (256 + 7) bytes.

Track selection for the operation is based on the current contents of the track address of configuration word B.

5.2.6.8 DIAGNOSTIC READ DATA

The Diagnostic Read Data command causes the channel to perform as if the Read Data command is specified, except that the seven-byte EDAC field attached to the data field is also transferred to memory (error detection/correction of the data field is not performed). Only one sector can be read by this command so that the range must equal 263 (256 + 7) bytes.

Track selection for the operation is based on the current contents of the track address of configuration word B.

5.2.6.9 WRAPAROUND READ/WRITE

Two wraparound levels are available in the WDC and are controlled by bit 15 of the Task Word. If bit 15 is a logical Zero, the wraparound is at the data buffer B level. If bit 15 is a logical One, the wraparound is at the data buffer A level. In either case, functionality is as described in the following paragraphs.

During a Wraparound Write command, the channel reads from 1 to 4K bytes of memory (at the address specified in the subsystem's memory address register) and transfers the bytes to the appropriate WDC buffer.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified WDC buffer by the previous Wraparound Write command are returned to main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by the software in the preceding Wraparound command.

A range of 1 to 4K bytes should be specified for these commands. If a range greater than 4K bytes or Zero is specified, the command is immediately terminated (without being executed and with Status Word 1, bit 11, set). If bit 15 is a logical Zero, buffer A data us read and then buffer B.

Execution of a task instruction to any other channel during a wraparound sequence results in unspecified results.

5.2.6.10 DIAGNOSTIC ERROR LOG BUFFER READ/WRITE

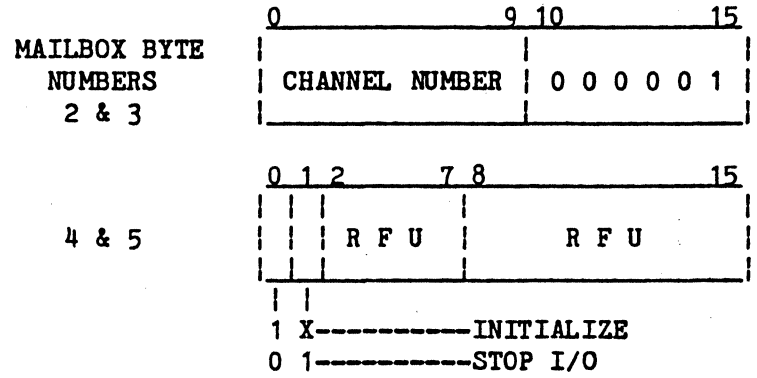
On initialization, this buffer is filled with error sectors IDs read from the Error Log and New Error Log on the Error Log cylinder sectors 00 and 01. This Error Log Buffer is used during a Format Write routine in reallocating bad sectors to the highest numbered cylinder spare sectors.

The Error Log Buffer, derived from the Error Log cylinder logs, is a list of error sectors used by the firmware in reallocating those bad sectors during the Format Write procedure invoked by the Create Volume. The error sectors are reallocated to the Error Log cylinder. This diagnostic procedure allows the addition of temporary error logs to Error Log Buffer without affecting the source of error logs on the Error Log cylinder, which results in:

- o the temporary error sector being reformatted;
- o addition of the complemented CRC to the ID field; and
- o verification that the ID field now has an error.

After the diagnostic procedure is complete, the WDC must be reinitialized in order to remove all the temporary Error Logs from the Buffer.

5.2.7 Output Control Word



This instruction loads a control word into the referenced channel. This command is unconditionally accepted by the channel regardless of its busy status.

5.2.7.1 INITIALIZE

This command causes the WDC to reset to the same state that it enters after power-up. When an Initialize command is received by the WDC, both the channel and the device are initialized and recalibrated respectively.

Operations that are in progress in the WDC at the time of the initialization are abruptly terminated and all software addressable registers are initialized. No information about the terminated operations are retained and no interrupts for the operations are generated. The interrupt level for the channel is set to Zero (interrupts blocked). Note that execution of this command may result in either invalid data on the media (if a Write command is in progress) or a device fault (if a Seek is in progress at a drive).

5.2.7.2 STOP I/O

This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it is not completed and no error checking is done. An interrupt is generated for the operation terminated by this command as if the operation comes to a normal ending point. Status, address and range information, present in the WDC when this command is received, is retained. Note that execution of this command may result in invalid data on the media (if a Write operation is in progress) or a device fault (if a Seek operation is initiated and not completed prior to a subsequent operation).

5.2.8 Input Memory Byte Address

	MAILBOX BYTE NUMBERS	0 ... 9	10 ... 15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE)	0 0 1 0 0 0

		0 ... 7	8 ... 15
RESPONSE CYCLE	4 & 5	BYTE ADDRESS	

This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting CPU.

During the response cycle the WDC returns The data word containing the low order 16 bits of the memory byte address currently stored for the specified channel in the IOP. Note that if a Write command ended at a byte boundary (high-order 8 bits of word), the memory address reflects the next word (not the low-order 8 bits of the previous word). This command is used for diagnostic purposes only.

5.2.9 Input Memory Module Address

	MAILBOX BYTE NUMBERS	0 ... 9	10 ... 15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE)	0 0 1 0 1 0

		0 ... 7	8 ... 15
RESPONSE CYCLE	4 & 5	QLTI (see subsection 5.2.17)	MEMORY MODULE ADDRESS

This instruction causes the current contents of the referenced channel's memory module address to be transferred to the requesting CPU.

During the response cycle the WDC returns the data bus containing the high-order 4 bits of the memory word address currently stored for the specified channel in the IOP. This command is used for diagnostic purposes only.

5.2.10 Input Range

	MAILBOX BYTE NUMBERS	0 ... 9	10 ... 15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE)	0 0 1 1 0 0

		0 ... 15
RESPONSE CYCLE	4 & 5	RANGE REGISTER

This instruction causes the current contents of the active DMC channel's range register to be transferred to the requesting CPU.

After the completion of a data transfer operation, the contents of the range register reflect the status of the transfer with respect to the physical sector(s) read.

- o If the contents are a value greater than Zero, the length of the physical sector(s) was less than the original range.
- o If the contents are Zero, the length of the physical sec- tor(s) was equal to or greater than the original range.

5.2.11 Input Configuration Word A, B, or C

	MAILBOX BYTE NUMBERS	0 ... 9 | 10 ... 15	
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE) | 0 1 0 0 0 0	A
		0 1 0 0 1 0	B
		0 1 0 1 0 0	C

		0 ... 15
RESPONSE CYCLE	4 & 5	CONFIGURATION WORD A, B or C

This instruction causes the current contents of the channel's configuration word A, B or C to be transferred to the requesting CPU.

5.2.12 Input Interrupt Control

	MAILBOX BYTE NUMBERS	0 ... 9 | 10 ... 15	
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE) | 0 0 0 0 1 0	

		0 ... 9 | 10 ... 15	
RESPONSE CYCLE	4 & 5	M B Z	LEVEL

This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value is placed on data bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction, or, a default value of 00. The default value is the interrupt level assumed by the channel when initialized.

5.2.13 Input Identification Code

	MAILBOX BYTE NUMBERS	0 ... 9	10 ... 15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER	1 0 0 1 1 0

		0 ... 15
RESPONSE CYCLE	4 & 5	IDENTIFICATION CODE

This instruction causes the referenced channel to transfer its Identification code to the requesting CPU. Depending on the device accessed, one of the following codes will be returned:

CODE (HEX)	MODEL (Unformatted)
3339	21 MByte Wren Disk Device
333B	35 MByte Wren Disk Device
333F	(See below for explanation)

333D WREN 2 70MB

The 333F code represents the ID code received when an WDD is not physically attached or it is powered down. The WDC generates the correct ID code when the device becomes available (i.e., when the drive is cycled-up.)

It should be noted that this updated ID code becomes visible to software via the issuance of another Input Identification Code instruction.

5.2.14 Input Task Word

	MAILBOX BYTE NUMBERS	0 ... 9	10 ... 15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE)	0 0 0 1 1 0

		0 ... 15
RESPONSE CYCLE	4 & 5	TASK WORD

This instruction causes the task word of the referenced channel to be transferred to the requesting CPU. The task word transferred contains the code for the last operation executed by the channel (unless an initialize has occurred).

5.2.15 Input Status Word 1

		0 ... 9	10 ... 15
REQUEST CYCLE	MAILBOX BYTE NUMBERS 2 & 3	CHANNEL NUMBER (DEVICE)	0 1 1 0 0 0

RESPONSE CYCLE 4 & 5

0	Device Ready
1	Attention
2	RFU/MBZ
3	Device Fault
4	Read Error
5	Program Error
6	QLT Fault
7	Unsuccessful Search
8	Error Log Overflow
9	Successful Recovery
10	WDC Timeout
11	IOP Bus Failure (See bit 5 description)
12	RFU/MBZ
13	Non-Existent Resource
14	RFU/MBZ
15	RFU/MBZ

This instruction causes the referenced channel's status word 1 to be transferred to the requesting CPU. The condition of the status word reflects the state of the device after the last Command and Result phases (see subsection 3.1.3).

5.2.15.1 DEVICE READY (BIT 0)

This bit indicates that the device is online with the actuator loaded and that no further manual intervention is required to place it under program control. Note that a change of state of this bit causes the attention bit (bit 1) to be set, resulting in an interrupt (if the interrupt level is nonZero). The bit reflects the current condition of the device.

5.2.15.2 ATTENTION (BIT 1)

This indicator is set whenever the device ready bit (Bit 0 of the status word) changes state. Any change of operational status of the device is indicated to software in this way.

Whenever the attention bit is set, an interrupt is attempted (if the interrupt level is nonzero). If a previously initiated operation is in progress when a device state change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change.

This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word command or Master Clear on the IOP bus.

5.2.15.3 DEVICE FAULT (BIT 3)

This bit is set if the WDD status Write Fault is set indicating a device fault. Bits 13 through 15 of status word 2 reflect more specific faults. This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus. Note that this bit is reset if the condition causing it to set is removed by the WDD.

5.2.15.4 READ ERROR (BIT 4)

This bit is set during any Read operation if either the EDAC word at the end of a field indicates that an uncorrectable data error has occurred within the field or the CRC Error bit appears within the ID field provided it is a new error not logged in the New Error Log on cylinder 696. This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus.

5.2.15.5 PROGRAM ERROR (BIT 5)

This bit is set if any of the available CPU commands are executed erroneously, e.g.:

- o Select illegal head address
- o Seek to a nonexistent cylinder,
- o Fixed Volume bit = 0
- o Format Write is ≠ 128 bytes
- o In conjunction with bit 11 indicates IOP bus dialog failure.

This bit is reset by an Initialize command, an Output Task Word command, or a Master Clear on the IOP bus.

5.2.15.6 QLT FAULT (BIT 6)

This bit indicates that the controller QLT has failed and that the QLTI status buffer contains the fault identification. The device ready bit is also reset in status word 1. This bit will be reset by an Initialize command, Output Task Word, or a Master Clear.

5.2.15.7 UNSUCCESSFUL SEARCH/FORMAT ERROR (BIT 7)

This bit is set during a nonformat Read or Write operation for which the sector ID specified in configuration words A and B cannot be located on the track or on the alternate cylinder. It is also set if the Index Mark is detected during a format write operation; in this case, memory address and range are invalid. This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus.

5.2.15.8 ERROR LOG OVERFLOW (BIT 8)

This bit is set whenever the WDC detects that the new error log (on the highest numbered cylinder) has exceeded 112 error sectors per volume count. If reformatting does not reduce the error count, the media or the device needs further attention. This bit is reset when the error count is less than 112.

5.2.15.9 SUCCESSFUL RECOVERY (BIT 9)

This bit is set when a recoverable error condition was successfully recovered during the previous operation. Status word 2 specifies the error condition which had occurred. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus.

5.2.15.10 WDC TIMEOUT (BIT 10)

If the WDC decides to terminate a dialog sequence by not responding with Request for Master with Input or Output and Not Busy, the IOP waits for approximately 300 to 500 milliseconds and then closes the dialog sequence by posting a Termination Status (reference subsection 5.3.3.2).

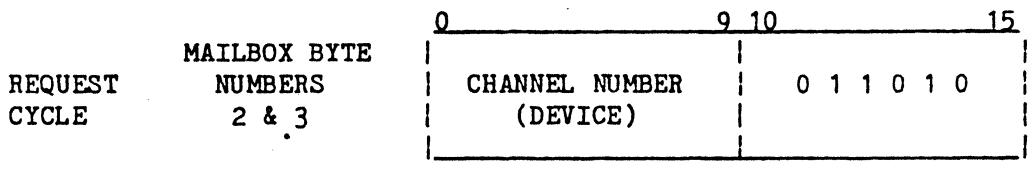
5.2.15.11 RFU-MBZ (BITs 11, 12, 14, 15)

Reserved for future use and must be Zero.

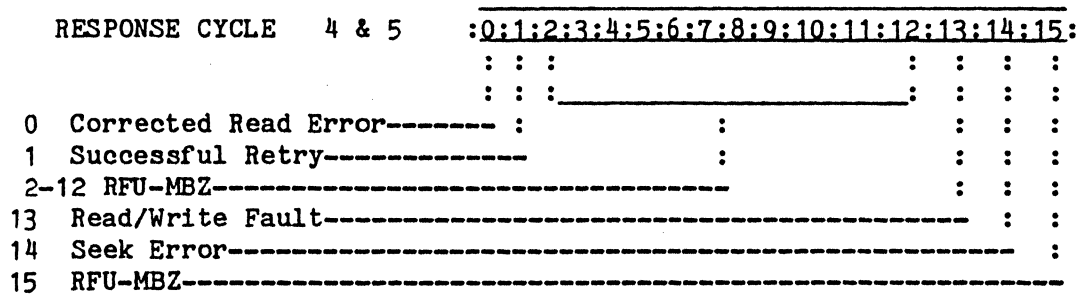
5.2.15.12 NON-EXISTENT RESOURCE (BIT 13)

This bit is set whenever the WDC attempts a Write or Read Request Bus cycle and receives a NAK response. This bit is reset by an Initialize command (Output Control Word), an Output Task Word command, an Input Status command or by a Master Clear on the IOP bus.

5.2.16 Input Status Word 2



RESPONSE CYCLE 4 & 5



This instruction causes the referenced channel's status word 2 to be transferred to the requesting CPU. The condition of the status word reflects the state of the device after the last Command and Result phases (see subsection 3.1.3).

5.2.16.1 CORRECTED READ ERROR (BIT 0)

This bit is set when a correctable read error occurred during the previous Read operation. Correction was performed by the WDC in buffer memory. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus. When this bit is set, it causes bit 9 of status word 1 to be set. See subsection 5.3.1 for EDAC functionality.

5.2.16.2 SUCCESSFUL RETRY (BIT 1)

This bit is set when a data read error has been successfully retried during the previous operation. When this bit is set, it causes bit 9 of status word 1 to be set. See subsection 5.3.2 for retry algorithm. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the IOP bus.

5.2.16.3 READ/WRITE FAULT (BIT 13)

When this bit is true, the Write Enable is on at the same time as the Read Enable. Detection of this fault inhibits the writer.

5.2.16.4 SEEK ERROR (BIT 14)

When this bit is true, the seek error has occurred. The error bit may be deactivated only by performing an RTZ. This bit, when true, indicates that the WDD is unable to perform a Seek within 500 ms, that the carriage has moved to a position outside of the recording field, that the WDD is unable to maintain the track lock, or that the WDC has received an illegal track address. If an illegal track address is received, the seek error bit is One in the status byte and no positioner motion takes place.

5.2.17 Input Quick Logic Test Indicators (QLTIs)

REQUEST CYCLE	MAILBOX BYTE NUMBERS 2 & 3	0 ... 9	10 ... 15
		CHANNEL NUMBER (DEVICE)	0 0 1 0 1 0

		0	15
RESPONSE CYCLE	4 & 5	QLTI	MEMORY MODULE ADDRESS (see subsection 5.2.9)

The QLTIs are stored in the Scratch Pad Memory (SPM) buffer during the QLT. If the edge indicator remains lit, the QLTI buffer contains the code of a test which had failed on either the WDC or one of the WDD. (Reference subsection 8.3.2).

5.2.18 Input Firmware Revision

	MAILBOX BYTE NUMBERS	0	9 10	15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER (DEVICE)	0 0 0 1 0 0	

		0	7 8	15
RESPONSE CYCLE	4 & 5	HARDWARE REL. LEVEL	FIRMWARE REL. LEVEL	

The firmware revision level is represented by a hex number, e.g., 23, which is the sequential control number. Hardware revision level is obtained from a PROM which is updated with every hardware change.

5.2.19 Invalid Code

If an invalid Function Code Read command is received, the IOP responds normally by presenting the contents of its mail box with the unspecified data.

5.2.20 Input Retry Count

INSTRUCTION CYCLE:

	MAILBOX NUMBERS	0	9 10	15
REQUEST CYCLE	2 & 3	CHANNEL NUMBER	1 0 0 0 0 0	

		0	7 8	15
RESPONSE CYCLE	4 & 5	RFU - MBZ	RETRY COUNT	

This instruction causes the referenced channel's Retry Count to be transferred to the requesting channel.

Bits 0 through 7 of the word are reserved for hardware use. Bits 8 through 15 contain the read retry count. This count contains the number of retries executed due to read errors. During a read, if an error is encountered the WDC controller attempts to reinitiate the order. This is counted as one retry.

The retry count is reset during an Initialize, Master Clear or new Output Task Word instructions.

5.2.21 Read/Write WDC IOP Registers

The IOP maintains 32 registers (16 bits per register) for each device. The address of each of the various registers in the IOP is a combination of 2 bits of the channel number and the high-order five bits of the function code used to write into or read from a particular register (see Table 5-1). For example, configuration word A for WDC device 1 is WDC register 08 (hex):

- Function code for configuration word A = 01000X (X = read/write bit)
- Device number = 000Z (Z = direction bit)
- Register number = 0000, 1000 = 08 (hex)

Complete software visibility to the WDC registers is provided for diagnostic purposes. An output bus sequence addressed to one of the devices will cause the information in the IOP Mailbox (16 bits) to be loaded into the device-specific register specified by the device port number and the high-order 5 bits of the function code. (Reference Figure 5-2).

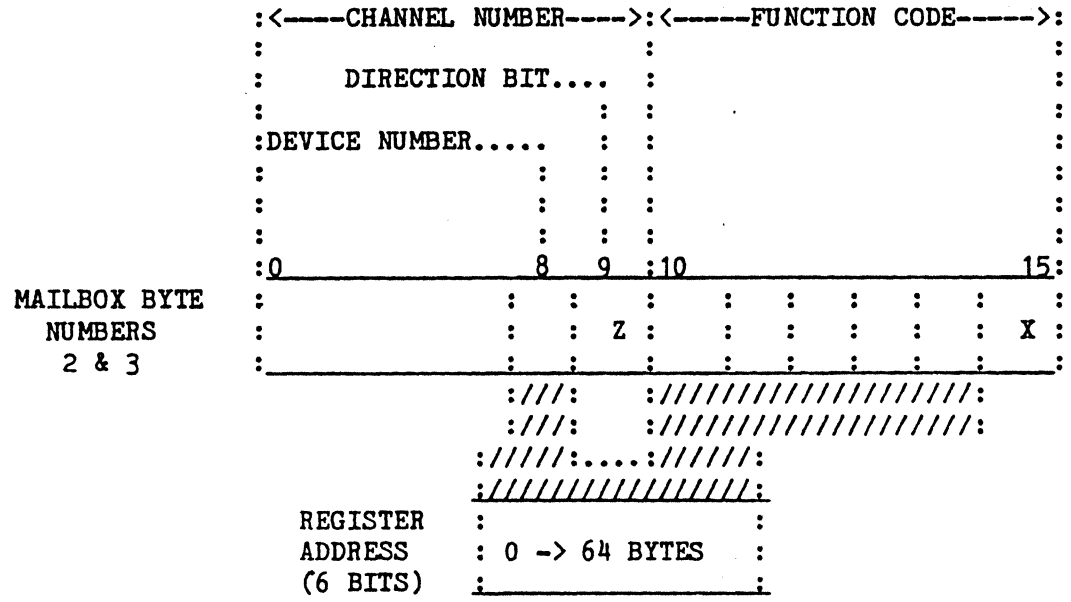


Figure 5-2 WDC Device-Specific Registers and Addressing

The Output Address command is a special case. When an Output Address command is executed (on port 0, for example) the WDC register 04 (hex) will be loaded with the low-order 16 bits of the address. The high-order 4 bits of WDC register 05 is loaded with the high-order 4 bits of the address.

NOTE

Output to some registers may result in an unspecified device operation.

Any input bus sequence addressed to a device causes the register specified by the port number and the high-order 5 bits of the function code to be returned via the IOP Mailbox. A detailed register map for each device type is available in the IOP manual.

5.3 IOP-WDC COMMAND PROTOCOL

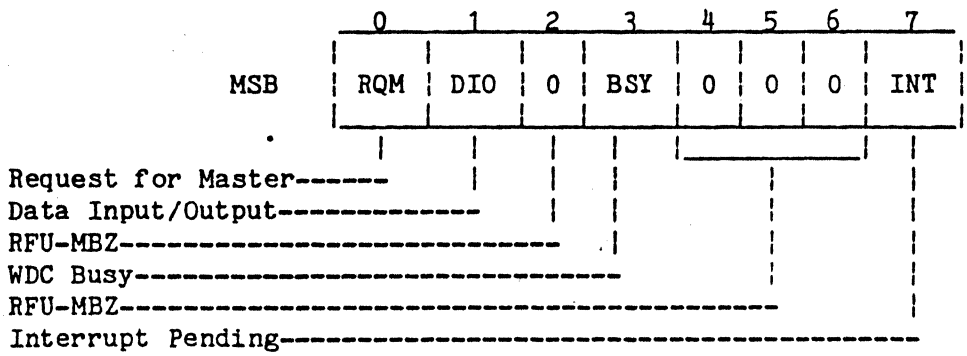
5.3.1 Command Sequence

Each command to the WDC is initiated by a multi-byte command stack transfer and the result, after execution of the command, may also be a multi-byte status stack transfer back to the IOP. Command sequence consists of three phases:

- Command phase - The WDC receives all information required to perform a particular operation.
- Execution phase - The WDC performs the operation.
- Result phase - Status and other housekeeping information are sent to the IOP.

The WDC appears to the IOP as a set of registers in its memory address space; a block of eight addresses is assigned, at design time, with 0 through 6 access Data registers and 7 accesses the Main Status register. There are two redundantly coded Data registers, one for imput functions and one for output functions. Each register consists of a stack of registers accessible to the IOP one at a time. The IOP interrogates the Main Status register before any data transfer to or from the WDC Data registers during both the command and Result phases. During execution phase if any data transfers take place the IOP is not involved except for the initial DMC control setup; data exchange is directly between the main memory and the WDC.

5.3.2 Main Status Register



This register can be read by the IOP at any time and the interpretation of each bit is given below.

5.3.2.1 REQUEST FOR MASTER - RQM (BIT 0)

This bit when set indicates that the WDC Data register is ready to exchange one byte with the IOP. Every time the Main Status register is read the IOP waits 12 microseconds between request to read and then reading the Data register. This bit must be reset within 12 s or the IOP interprets it as another request.

During the QLT, the ROM bit is clamped to Zero; at the end of diagnostics, the INT bit is set and the interrupt line on the IOP Bus is pulled low before raleasing the RQM clamp.

5.3.2.2 DATA INPUT/OUTOUT - DIO (BIT 1)

This bit indicates the direction of the next one byte data transfer between the WDC and the IOP:

- o 0 = Output data, IOP to WDC
- o 1 = Input data, WDC to IOP.

NOTES

Both the RQM "ready" and DIO "direction" bits are used for hand-shaking functions.

The Output Control Word. Step I/O, ((5.2.7) can be sent at any time; to avoid a race condition between the WDC and the I/O, the WDC should set the DIO 25 s before asserting both the RQM and INT. The WDC must be receptive to the Stop I/O command during that delay.

5.3.2.3 WDC BUSY - BSY (BIT 3)

1. On detection of RQM = 0 and BSY = 0, for >350 microseconds the IOP attempts a PIO. This causes an error termination, Status Word 1 bits 0, 5 and 11 set to ones (see bit 5 description).

2. WDC Busy (BSY=1) the IOP restacks the order. Busy must only be set when the current operation terminates in on interrupt.

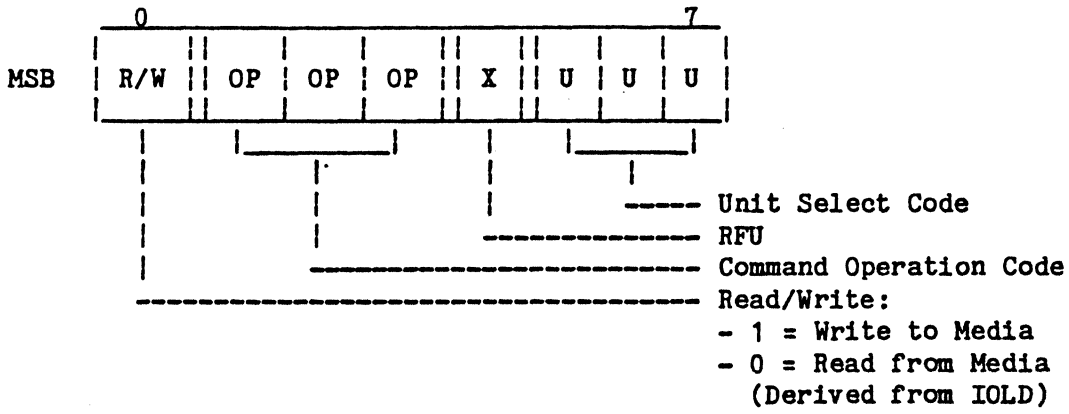
5.3.2.4 INTERRUPT PENDING - INT (BIT 7)

This bit, when set, indicates that an interrupt on one or more ports of the controller is pending and that the interrupt lead is pulled low. The IOP responds with the Request Status command in order to determine what condition caused the interupt on which port. The Request Status command resets the Interupt Pending bit and Interrupt lead if there are no other interrupts requiring attention.

5.3.3 Command Phase

The IOP outputs (DIO = 0), in compliance with the RQM bit, a variable length command string consisting of a command header byte (see below) followed by a string of Level 6 IO command words in a fixed order. The number of bytes in the command byte string is determined by the WDC on examination of the Task word which is sent immediately after the command header. The command string is terminated by the WDC switching to imput mode, DIO = 1 (DIO must change during the RQM = 0), and the IOP then imputs the Command Acknowledge byte whose condition indicates the next IOP procedure (see Initial Response below).

5.3.3.1 COMMAND HEADER BYTE



Command Operation Codes

0 - Output Task
1 - DMC Proceed
2 - Request Status (Result phase)
3 - Request QLT Status
4 - Stop IO (Derived from FC = 01)

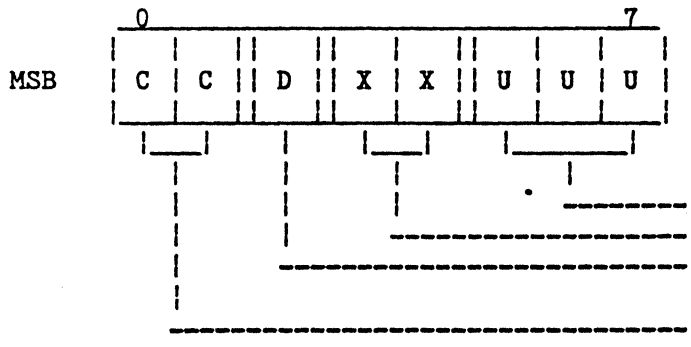
All of the above commands are one byte long except the Output Task command, which is followed by the fixed Level 6 instruction word sequence (two bytes for each instruction):

1 - Task Word, FC = 07
2 - Configuration Word A, FC = 11
3 - Configuration Word B, FC = 13
4 - Range, FC = 0D (From IOLD)
5 - Configuration Word C, FC = 15
6 - Configuration Word D, FC = 17.

5.3.3.2 INITIAL RESPONSE

The Initial WDC Response to a command is either a one byte data transfer if the command is accepted (Command Acknowledge) or it is followed by the Status Response Stack in the event of an error detected during a command phase.

Initial Response Header Byte



Response Type Codes

0 - Command Acknowledge - DMC facility request (Bit D)
1 - QLT Status
2 - Task Termination Status - DMC facility release (Bit D)
3 - Attention Status

- o Response Type 1 (Sent in Response to Request QLT Status Command) Sequence (Two Bytes Each):
  1 - Device ID Word, FC = 26
  2 - Revision Word, FC = 04
  3 - QLT Indicators, FC = 0A (MSB).

- o Response Type 2 is a result of a normal Task command termination with normal status.

- o Response Type 3 is a result of the WDC requesting the IOP to read its QLT status.

In both response types 2 and 3 the Status Response Stack follows the header byte; it is sent in a fixed sequence:

Status Response Stack (Two Bytes Each)

1 - Status Word 1, FC = 18
2 - Configuration Word A, FC = 10
3 - Configuration Word B, FC = 12
4 - Status Word 2, FC = 1A
5 - Retry Count, FC = 20
6 - Range, FC = 0C
7 - Configuration Word C, FC = 14
8 - Configuration Word D, FC = 16

The length of the Status Response Stack is controlled by the WDC by switching the DIO bit from input to output during RQM = 0, then switching the RQM = 1, indicating ready for a new command.

5.3.4 Execution Phase

If no DMC is required (or if it is a two-part operation and the first part requires no DMC), then the WDC proceeds to the Execution phase. If, however, the DMC is required for this operation, the WDC waits for the IOP (RQM = 1, DIO = 0) to output the DMC Proceed command and then executes the Execution phase. The execution phase is terminated by the WDC when the DMC end-of-range is detected, setting the INT bit in the Main Status Register and pulling the interface INT lead low.

For the sake of the IOP performance efficiency, each command to the WDC should be divided into a non-DMC and a DMC portion wherever possible. This is required so that the single DMC channel of the IOP is not tied up for the duration of the non-DMC portion of a command, e.g., during implied seek and latency (if buffered) to a disk. Hence, the protocol sequence between the IOP and an WDC should be as shown in Figure 5-3.

5.3.5 Result Phase

The Result phase starts when the Execution phase ends with an interrupt to the IOP, signifing that either a DMC end-of-range has been reached on data transfers or a control function has terminated. The WDC responds with Response Type 2 for normal Task Command terminations or with Response Type 3 for error or abnormal WDC or device conditions (see subsection 5.3.3.2).

At the completion of the Result Phase, the condition RQM=1, DIO=0 must persist for a minimum of 15 us to allow enough time for the IOP to sense that condition and terminate the Result Phase.

Whenever the WDC must drop the RQM (=0) asynchronously (i.e. on its own and not in direct response to a PIO), it must be able to accept a command byte from the IOP up to 25 us after RQM 0 and DIO=0. If BSY is to be set it must not be set until after the 25 us interval.

5.4 DEFECT MANAGEMENT

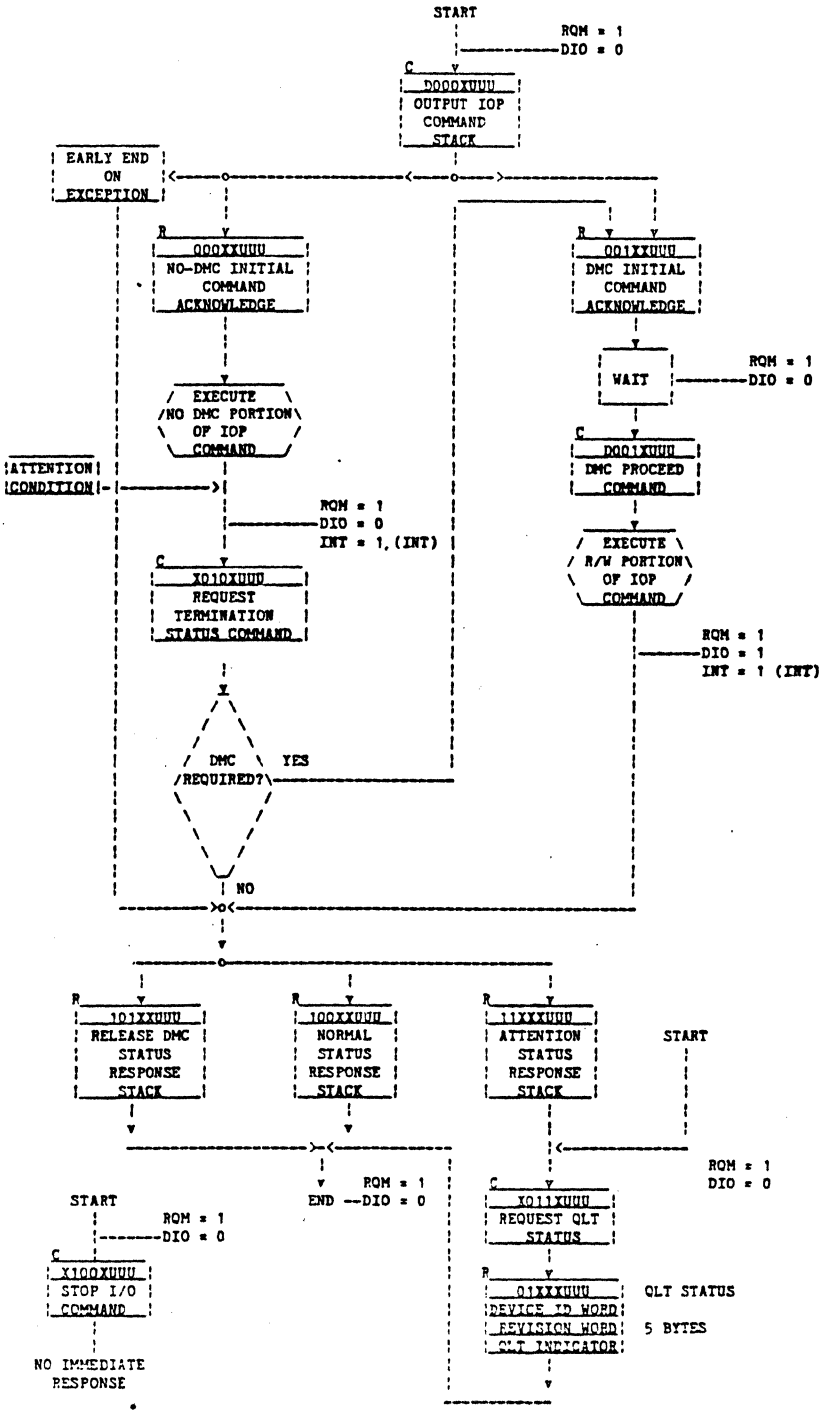
5.4.1 EDAC Functionality

The 7-byte EDAC field appended to the data field provides the correction of error bursts of up to 11 bits and detection of an error burst of up to 22 bits. Any bit errors separated by more than ten bits are not correctable. The write polynomial generator used for the creation of a 7-byte EDAC field is as follows:

Write Polynomial:

$$(X^{21} + 1)(X^{11} + X^7 + X^6 + X + 1)(X^{12} + X^{11} \ldots X^2 + X + 1)$$

During Update Read and Write operations, the detection of any read error in an ID field causes bit 4 of the status word to be set. The search (update read or write) continues. If a successful search is not made prior to detection of two index marks, the operation is terminated with bit 4 set. If a successful search is made prior to detection of two index marks, bit 4 is reset and the operation continues in a more normal fashion. In either case, no error correction is performed on the ID field.



Where C = IOP command; R = WDC response; D = Direction bit; U = Unit Select Code; I = Don't care bit; and INT = Interrupt lead assertion.

Figure 5-3 IOP Interface Protocol Sequence

If a read error is detected following the transfer of a sector data field to buffer memory, one of two situations is possible:

- o If the error is not correctable, retry is initiated as described below.
- o If the error is correctable after a number of retries, then the WDC automatically performs the required correction in buffer memory, sets bit 9 of status word 1 and bit 0 of status word 2, and continues the data transfer operation. Note that a loss of revolutions of the media occurs during the correction period.

5.4.2 Read Error Retry

If a Data Field read error is detected following transfer of a sector data field to the WDCmemory, the following retry procedure is invoked automatically by the WDC:

1. Three retries,
2. Three retries with early data strobe,
3. Three retries with late data strobe,
4. Three retries with offset plus,
5. Three retries with offset plus, early data strobe,
6. Three retries with offset plus, late data strobe,
7. Three retries with offset minus,
8. Three retries with offset minus, early data strobe,
9. Three retries with offset minus, late data strobe.

If an ID Field Read Error is detected, the WDC does 3 retries before reporting Unsuccessful Search (Status Word 2, bit 7) during Read/Write doctor commands.

Note that:

- o EDAC is attempted only once after the above procedure is unsuccessful in removing an error.
- o The read error retry is applied to the data field errors only during Read Data commands (does not apply to format or diagnostic commands - bit 4 of status word 1 is set in these cases as applicable).
- o A latency period is entered between retries.
- o A loss of at least one revolution occurs for each retry.
- o Any clock change condition is automatically restored after retry (successful or unsuccessful).

The read error retry has one of two results:

- o If the error is not recoverable, bit 4 of status word 2 is set and the operation is terminated.
- o If the error is recoverable, bit 9 of status word 1 and bit 1 of status word 2 are set and the data transfer operation is continued.

5.4.3 Media Defect Handling

Definitions:

- o An error burst of 11 bits or less is a correctable error.
- o An uncorrectable error is one greater than 11 bits in length.
- o Only one correctable error may occur in each sector or that sector must be classified as uncorrectable.

For WDD only:

- o Acceptable criteria (CDC specification 77711078, subsection 8.1) for the Wren fixed media:
  - a. Have no media defects on cylinder 0 and 696.
  - b. Have no more than 18 uncorrectable tracks per surface.
  - c. Four additional uncorrectable tracks per surface can occur over the life of the medium.
  - d. Track is flagged as uncorrectable when one or more sectors are found to be uncorrectable.

5.4.3.1 ERROR LOGGING PROCEDURE

Each track is analyzed during medium certification at the vendor factory for correctable and uncorrectable error conditions. If either error condition exists, it is entered in the Vendor Error Log located on the highest number cylinder sector 0 of each surface corresponding to the error sector surface. For format details, see Figure 5-4. The WDC does not re-write this log in Honeywell format.

In addition to the above, an error flag track label is supplied with each unit to provide a second source of error information.

If during the life of a medium an uncorrectable error should develop, software identifies the erroneous sector and records its parameters on the highest number cylinder, surface 0, sector 1, New Error Log, and the firmware in the WDC utilizes this information for sector reallocation. (See Detailed Create Volume Procedure, further on in this Section.)

Because the Wren is a soft sectored unit, the WDC firmware must calculate where the defective sector is located using the Vendor Error Log Byte Count (see Figure 5-3) information.

Using the formula L = N*D/210 (210 = 10080/48) where:

N = the number of sectors;
*D = the Byte Count divided by 48. The BCD number is in the format log at the highest number track and also on the flag track label supplied with the unit; then
L = the actual defective sector.

For example, if the number of sectors in the selected format is 32 and the Byte Count in factory format log is 150, then:

L = 32*150/210, or

L = 22 (rounded down).

Sector 22 is the defective sector.

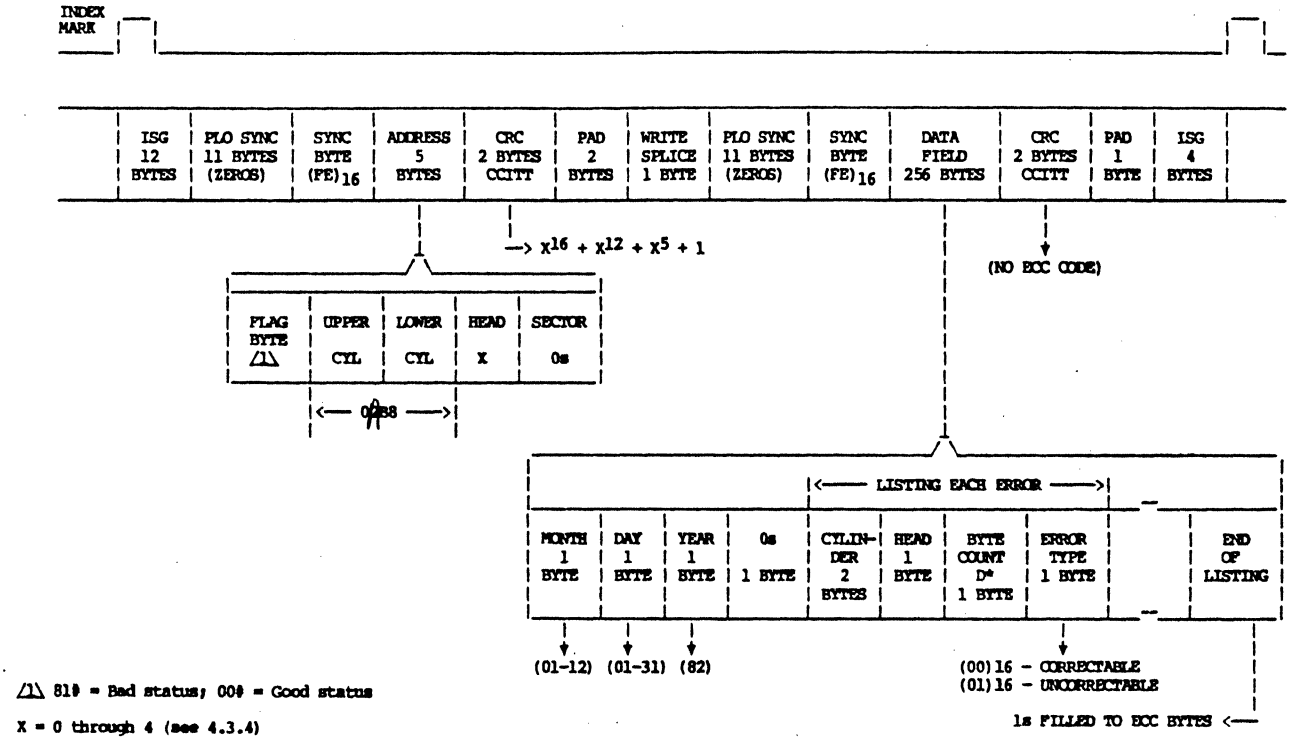


Figure 5-4 Format for Surface 0, Sector 0, Highest Number Cylinder Factory Flagged Data Track

5.4.3.2 SECTOR REALLOCATION

Create Volume Procedure Outline

- Format cylinder 696 first (optional)
- Format user area, cylinders 0 --> 694 and/or cylinder 696 (S)
- Verify read, cylinders 0 --> 694
- If a new error sector is found, append the new error to the New Error Log, highest number cylinder, sector 01 (S)
- Reallocate error sector to highest number cylinder and store the address in controller memory (F)

- Continue verification (S)

where S = Software
F = Firmware on the WDC

Assumption:

- Software formats a volume, one track at a time, using physical addressing only (e.g., no interleaving of sector IDs).

Vendor Error Log Sector ID

In sector 00, 0 on highest number cylinder, the ID fields of medium vendor logs are:

Flag byte:	00# or 81# (Visible to Firmware only),see note /1\, Figure 5-4
Upper Cylinder Byte:	02 (CDC format)
Lower Cylinder Byte:	B8
Head Address Byte:	00 through 04
Sector Address Byte:	00

NOTE

To access either sector 0 or sector 1 on the highest number cylinder; standard Honeywellformat using Configuration Words A and B can be used.

New Error Log Sector ID

In sector 01, surface 0, on highest number cylinder, head address 00, ID fields of the new error log are:

Flag byte:	00 (Visible to firmware only)
Upper Cylinder Byte:	0A (Honeywell format, see NOTE above)
Lower Cylinder Byte:	B8
Head Address Byte:	00
Sector Address Byte:	01

If the ID field is not as shown, then sector 01 on the highest number cylinder has not been formatted before and the New Error Log does not exist.

Detailed Create Volume Procedure

1. Format

If the highest number cylinder has been formatted (identified by a flag in the ID field), it is not nebessary to reformat it whenever the user area is reformatted. This option is desirable for obtaining a cumulative New Error Log on removable media or for avoiding marginal areas on a surface. Software, in Create Volume, attempts to format the highest number cylinder head 0 only. Firmware, triggered by this command, ignores the ID data and formats the highest number cylinder in any manner that is compatible with the implemented algorithm for sector reallocation. It then formats the remainder of the media in a normal manner under software control.

2. Format Verify

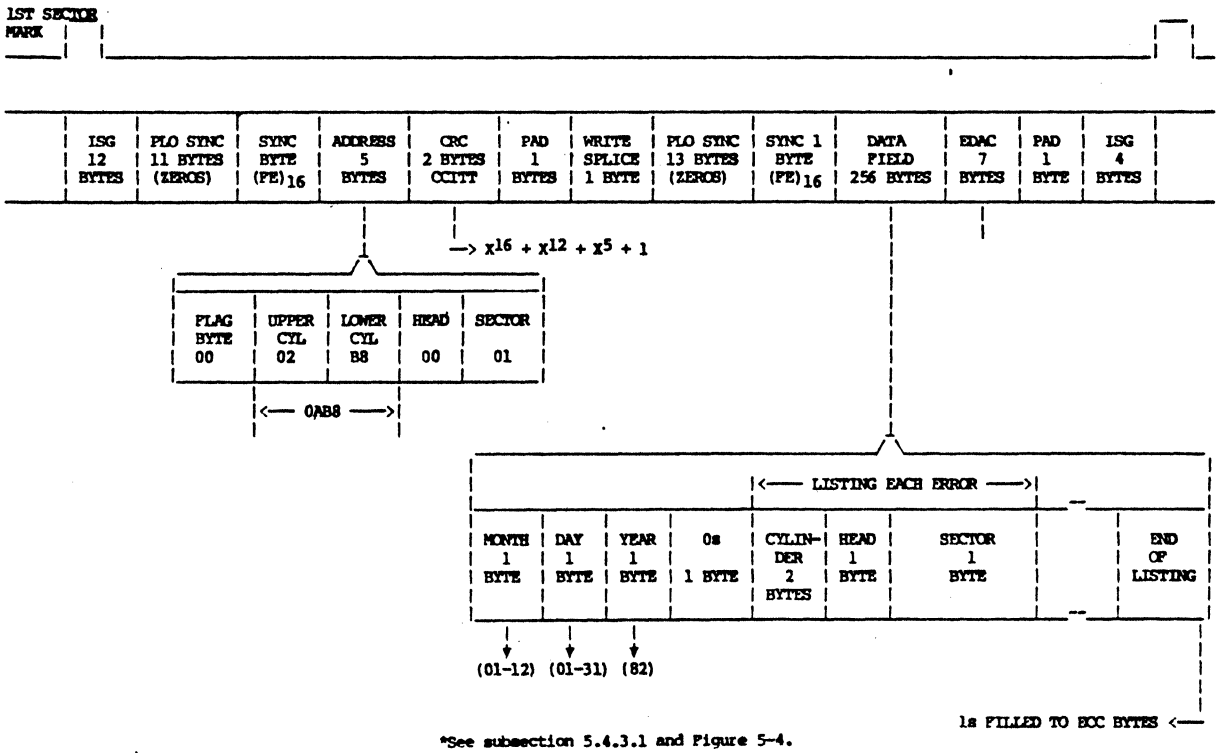
   All user cylinders are verified by reading the formatted tracks.

3. New Error Identification

   If an error is found, software appends the new error parameters to the New Error Log on the highest number cylinder located on sector 1.

   Firmware on the WDC, triggered by the Write to the New Error Log, remaps or reallocates the sector in which the error was found, according to its reallocation algorithm. Reallocated sectors start from sector 2 on the highest number cylinder and surface zero. Refer to Figure 5-5.

   The remainder of the data field on sector 1 is FF filled.



*See subsection 5.4.3.1 and Figure 5-4.

Figure 5-5 New Error Log Format on Cylinder ~~514~~ 696

4. Continue

   Continue the software verification from the error track found during step 3 until the whole volume is verified.

5. Error Development

   If during the life of a medium an error should develop, invoke the procedure described in 3, above only.

Additional Observations

Sector IDs are remapped and reallocated to the highest number cylinder. During Read/Write commands, remapped sectors are detected, or as indicated by a detection of two index marks without compare, resulting in a seek to the highest number cylinder, and a normal search for reallocated sector ID.

Performance considerations are as follows:

- o At least one seek period and one latency period are encountered for each reallocated sector.
- o After that sector is read, another seek period and another latency period are entered in order to read the next sequential sector.
- o The above has less than 3% impact on performance over the life of a medium.

NOTE

If sector 01 exists (see New Error Log Sector ID, above), then the highest number cylinder has been formatted before. However, if the highest number cylinder is being formatted, data contained in sector 01 is lost: medium must be reformatted to locate possible new bad spots.

Diagnostic cylinder 696 is not formatted and is reserved for exclusive use of T&Vs.

Boot Load Procedure

For the sake of compatability with the LARK disk subsystem, the Wren subsystem Boot Load firmware should be different to that used for SMD/CMD devices. The default Boot Load procedure remains unchanged for even I D numbers, i.e., read the Boot Load sector and the Intermediate Loader then load the Operating System from the removable volume. For odd I D numbers, the current procedure reads both the Boot Load with Intermediate Loader and the Operating System from the fixed volume.

SECTION 6 PHYSICAL AND LOGICAL STRUCTURES

6.1 PHYSICAL STRUCTURE

The Wren Disk Subsystem consists of a WDC and up to two Wren devices (WDDs) that are connected to the controller via two radial cables and one daisy-chain cable. The controller board is etched and has three connectors for connection of WDDs.

6.1.1 Physical Specifications - WDC

6.1.1.1 MECHANICAL

- Dimensions: 12.45 in. (31.62 cm) wide by 15.00 in. (38.1 cm) long by 0.062 in. (0.157 cm) thick
- Weight: Approximately 22 oz. (0.618 kg)
- Cabling: Three connectors connect between the M-board and the WDDs; two D-data cables (one to each of two possible devices) and one C-command cable daisy-chained to the second device where it is terminated. Maximum length between the controller and the furthest device is not to exceed 20 feet. Device connectors have 20 pins for the D-cable and 34 pins for the C-cable at the controller.
- Cooling: Forced, unfiltered air at 125°F (51.7°C) maximum ambient at 110 CFM (51.9 liters per second).

6.1.1.2 ENVIRONMENTAL

- Per HIS standards, B01.08 - Class 2 (contamination requirements are waived).
- Meet all U/L requirements, CSA approval.

6.1.1.3 ELECTRICAL

- Primary power - B01.08, Group I, II, III
- Power module to share a common chassis with the printed circuit boards.
- Further definition given in NPL Power Spec (60126325).

6.1.2 Physical Specifications - Wren Disk Drive

6.1.2.1 MECHANICAL

- Dimensions: 5.75 in. (14.60 cm) width, 8.00 in. (20.32 cm) rack depth, 3.25 in. (8.26 cm) height
- Weight: 6.5 lb. (2.94 kg)
- Face panel: 5.88 in. (14.94 cm) width, 3.38 in. (8.59 cm) height. Location of two switches and two indicators.
- Cabling: Cabling connecting the FDC with one disk device in a radial fashion should not exceed 20 feet (6.10 m) in total length. Cable connectors at rear of each device accept cables.
- The Wren Disk Drive dissipates 38 watts of dc power average or 133 BTUs per hour.

6.1.2.2 ENVIRONMENTAL

The disk device will withstand the following environmental extremes without adverse effects (reference HIS standards B01.08 and B01.10).

- Operational temperature: 50°F (10.0°C) to 114.8°F (46°C)
- Storage temperature: 14°F (-10.0°C) to 122°F (50.0°C)
- Operating humidity: 20% to 80% RH (noncondensing)
- Humidity gradient: 10% per hour maximum
- Storage humidity: 10% to 90% RH (noncondensing)
- Operating temperature gradient: 18°F (10°C)/hour maximum
- Storage temperature gradient: 27°F (15.0°C)/hour maximum
- Transit temperature: -40°F (-40°C) to 158°F (70.0°C)
- Transit temperature gradient: 36°F (20°C)/hour maximum
- Effective Altitude (Sea Level Reference):
  - Operating:
  - Transit: -893 to +9830 feet (-300 to 3000 meters)
  - Storage:

6.1.2.3 ELECTRICAL

There is isolation of dc ground and frame ground in the disk device. The two grounds are brought out separately for external connection at a system level tie point.

The Wren Disk Drive dc power requirements are listed below:

Voltage	+5 VDC	+ 12 VDC
Regulation	±3 %	±5 %
Ripple	50 mV	100 mV
Average Operating Current (Worst Case)	1.5 A	2.5 A
Operating Current (Typical)	1.2 A	1.8 A
Operating Current (Peak)	2.0 A	4.0 A
Absolute Maximum Voltage Without Physical Damage to Disk Drive	+6.8 VDC	+ 14 VDC

SECTION 7 PERFORMANCE

7.1 GENERAL

The performance of the WDC is expressed in terms of its maximum throughput requirements and the performance characteristics of attached devices.

The WDC accommodates a maximum data throughput of 604,788 bytes per second for the Wren Disk Drive, with a peak IOP Bus data rate of 190,476 bytes per second. This throttled down IOP Bus data rate is required to allow other events to take place in the Hercules system, during data transfers.

The WDC accepts one input/output sequence for the attached device or devices.

7.2 PERFORMANCE CHARACTERISTICS

Performance characteristics of the WDD are shown in Table 7-1.

Table 7-1 Operational Characteristics Summary (Sheet 1 of 2)

DESCRIPTION	WREN
Data Capacity* (unformatted):	
Bytes per track	10,080
Double disk - Mbytes	21.08
Triple disk - Mbytes	35.13

Table 7-1 Operational Characteristics Summary (Sheet 2 of 2)

DESCRIPTION	WREN
Data Capacity* (formatted):	
Bytes per track	8,192
Double disk - Mbytes	17.08
Triple disk - Mbytes	28.47
Sectors per track	32
Bytes per sector	256
Number of cylinders (total)	697
Number of hrads: (one servo head)	
Double disk	4
Triple disk	6
Recording Mode	MFM
Data Transfer Rate - MHz	4.84 ± 3%
Data Interface	NRZ Data + Clock
Spindle Speed - rpm	3600 ± 1.0%
Step rate** - maximum	8 us
minimum	200 us
Average latency	8.33 us
Average Seek	50.0 ms - 45 ms (typ)
Maximum Seek	100.0 ms - 90 ms (typ)
Single Track Seek	10.0 ms - 9 ms (typ)

*WDD calculations based on 695 tracks per surface with 696 used for T&Vs only and 697 used for error sectors.

**Step pulse rate of slower than 80 us may degrade seek performance.

SECTION 8 AVAILABILITY

8.1 INTEGRITY

Data integrity is checked in the subsystem by the Error Detection and Correction code described in subsection 5.3.1. All data written on the media has the code (EDAC) appended such that when the data is subsequently read, the accuracy of the recovered data is guaranteed within limits.

Whenever the subsystem is initialized, QLTs are executed by the WDC to provide a basic level of confidence that the Wren Disk Subsystem fault-free (see subsection 8.3).

All subsystem-detected errors (recoverable and nonrecoverable) are reported or displayed (refer to subsections 5.3 and 8.4).

8.2 MAINTAINABILITY

8.2.1 Maintainability Requirements

The following design goals, measured in hours, are specified as a minimum to be achieved during the first year after initial ship and during the third year after unlimited production is authorized. References to "repair" normally imply ORU replacement.

8.2.1.1 MEAN TIME TO REPAIR (MTTR)

MTTR represents the average repair time for a service engineer to diagnose, isolate, repair or replace, and verify the fix. MTTR does not include response

time, travel time, or idle time at the site waiting for the system or needed spare parts. These MTTR times are given for each unit that comprises the storage module subsystem.

UNIT	FIRST YEAR	THIRD YEAR
WDD	0.75 hour	0.75 hour
WDC	1.00 hour	0.75 hour
Power Supply	TBD	TBD

8.2.1.2 MEAN TIME BETWEEN PREVENTIVE MAINTENANCE (MTBPM)

This goal, the period of operational time between required or recommended preventive maintenance (PM), is given for each unit.

UNIT	MTBPM
WDD	no PM
WDC	no PM
Power Supply	no PM

8.2.1.3 DIAGNOSTIC FACILITY LOCALIZATION EFFECTIVENESS (DFLE)

This represents the probability that a hard failure is localized to a unit. The DFLE given takes into consideration the comprehensiveness, the resolution, and the accuracy of the diagnostic facility provided.

	DFLE	
	FIRST SHIP	18 MONTHS AFTER FIRST SHIP
Comprehensiveness	95%	98%
Isolation to an ORU	85%	93%
QLT Isolation	70%	70%

- Comprehensiveness is the ratio, in percent, of the number of faults detected to the total number of faults that can occur.
- Isolation to an ORU is the ratio, in percent, of the number of faults correctly resolved to the ORU, to the total number of faults that can occur.
- QLT Isolation is the ability to detect ground insertion errors.

8.2.2 Maintenance Strategy

The maintenance strategy for the WDC subsystem is in accordance with the governing EPS-1 specification on the L6 System. The subsystem is partitioned into ORUs which can be effectively diagnosed for a faulty condition via a combination of

firmware-controlled tests, software tests, and visual indicators. Available diagnostic aids provided are executable by the customer as well as a service engineer. Simple repairs such as the replacement of a defective ORU with an operational one should be able to be carried out by trained customer personnel or service engineers. Faulty ORUs are not serviced on the customer site.

8.2.2.1 MAINTAINABILITY FEATURES

The ORUs for the Disk Subsystem are:

- o WDD Assembly
- o WDC
- o Power Supply
- o Cable Assembly (QLT cannot test continuity on the cable).

Isolation of a failure to an ORU is achieved via a two-step procedure. The first step is a hardware verification routine called a Quick Logic Test (QLT). This test supplies a go/no-go visual identification of a Disk Subsystem hardware failure.

The QLT verifies operation of each of the Disk Subsystem ORUs. In addition, if a failure is detected during any of the tests, a QLTI indicator register is loaded associating tests performed with deviations from expected results for the Wren subsystem; the results are made available for interrogation at the end of the QLT in the QLTI register. QLTI contains the failing firmware indicator - firmware listing must be consulted for further clarification (Refer to Figure 8-1).

QLTI Byte

0 (MSB)	1	2	3	4	5	6	7 (LSB)	
0	0	0	0	0	0	0	0	ALL GOOD
1	0	0	0	0	0	0	0	DEVICE #1 FAULT
1	0	0	0	0	0	0	1	DEVICE #2 FAULT
1	0	0	0	0	0	1	0	DEVICE #3 FAULT
1	0	0	1	0	0	0	0	CHANNEL/ADAPTER #1 FAULT
1	0	0	1	0	0	0	1	CHANNEL/ADAPTER #2 FAULT
1	0	0	1	0	0	1	0	CHANNEL/ADAPTER #3 FAULT
1	0	1	0	0	0	0	0	CONTROLLER FAULT
1	0	1	1	0	0	0	0	CONTROLLER TO BUS INTERFACE FAULT

Figure 8-1 QLT Indicators

The QLT should conform to the following:

- The QLT provides a means of isolating a fault to an ORU when combined with an appropriate T&V software routine.
- No test must be allowed to stop the clock; i.e., no halt condition can exist in the WDC firmware unless continued faulty operation can affect other controllers on the common bus.
- The controller must issue "busy" during the QLT.

Major QLT functions performed are:

- Read/Write a data pattern into all Scratch Pad Memory locations and verify
- Set and Reset control flops and test both states
- Data Wrap on the device interface side to the FDC receivers/drivers.

The QLT is invoked in the WDC in response to Master Clear on the IOP bus or an Initialize command (output control word) received on the WDC channel. Results of the QLT appear as a visual indication on the virtual control panel and on the front edge of the board. The indicator turns on during execution of the QLT and turns off only if the QLT completes successfully. The QLT indicator register is available for inspection in the event of the Disk Subsystem failure.

Software T&Vs are provided to verify all operational aspects of the Disk Subsystem and to isolate failures to an ORU. Operator interface with these routines is via the CPU control panel or a TTY compatible console. The routines are run stand-alone. Diagnostic functionality has been included in the subsystem to support software diagnostic routines, and cylinder 695 on the Wren can be used at any time for this purpose.

The designated ORUs are easily removable and replaceable. The only tool required is a screwdriver. System power must be off to remove or replace the WDC. Power for attachable devices is not independent of system power.

A test procedure for execution by nontechnical trained customer personnel, field engineering personnel, or by others isolating faults to the ORU is supplied to support the QLT and the appropriate device ORU isolation test routines.

8.2.2.2 INSTALLATION

All Disk Subsystem equipment installations or expansions to a basic system are Field Engineering responsibility. Replacement of faulty units is also FED's responsibility for the initial shipments; subsequent maintenance can be performed by customer personnel, except for the WDC which resides in the main floor cabinet assembly.

8.3 RELIABILITY

8.3.1 Product Life

Product life is defined as the period of time within which the equipment performs within established reliability goals:

WDC 10 Years
WDD 5 Years (30,000 hours)

The above estimates are made assuming 100% duty factor.

8.3.2 Mean Time Between Failures (MTBF)

MTBF is expressed in power on hours of the component or ORU and is concerned only with hardware failures. It is a minimum to be achieved after First Customer Ship (FCS):

	FIRST YEAR	18TH MONTH
WDD	5,000	10,000
WDC	70,000	100,000
Power Supply	TBD	TBD

8.3.3 Transient Error Rate - 1 in 10^9

The transient error rate is the total number of errors encountered as a function of the number of bits read before any recovery techniques are attempted.

8.3.4 Recoverable Error Rate - 1 in 10^{10}

The recoverable error rate is the number of errors encountered which are recoverable within 12 subsystem retries as a function of the number of bits read.

8.3.5 Unrecoverable Error Rate - 1 in 10^{12}

The unrecoverable error rate is the number of errors encountered which cannot be recovered within 12 subsystem retries as a function of the number of bits read.

Example:

Assume the WDD passes 1×10^{11} bits of information. Using the transient error rate figure, no more than 100 errors (maximum) are encountered.

Within 12 retries under the conditions described above, at least 99 are recovered, and no more than one is unrecoverable.

8.3.6 Recoverable Seek Error Rate Requirement

A recoverable seek error is one in which the Seek operation fails to position the device read/write head on the proper cylinder. However, upon the issuance of a Recalibrate command followed by a Seek command to the same cylinder, the Seek is executed correctly.

Recoverable Seek Errors - 1 in 10^6 seeks.

SECTION 9 CONFIGURABILITY

9.1 GENERAL

Configurability requirements, restrictions, options, etc., are described in this section for a Finch Device Subsystem. The following paragraphs specify configurational characteristics of relevant units. Performance parameters, instructions and interfaces are described in previous subsections.

9.2 WREN DEVICE SUBSYSTEM

The following points are pertinent to a WDD:

- The Wren Disk Device is mounted in the floor-mount enclosure only.
- Cabling each of two possible WDDs:
  - One 34-pin cable - C cable from the adapter to the first device
  - One 34-conductor cable from the first device to the optional second device
  - One or two (for two WDDs) 20-conductor cable with ground plane and drain wire - d cable
  - One or two (for two WDDs) dc power cables originating in the common power supply.
- Grounding strap (19 mm braid) must be attached between the WDDs and the system ground. Logic and chassis grounds are tied together in the WDD.

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