HONEYWELL

66/DPS, 68/DPS & DPS 8 DATANET 6641/6651/6661/6678 OPERATION

HARDWARE

66/DPS, 68/DPS & DPS 8

DATANET 6641/6651/6661/6678 OPERATION ADDENDUM B

SUBJECT

Changes and Corrections to the Manual

SPECIAL INSTRUCTIONS

This is the second addendum to AY34, Revision 2, dated May 1980. Insert the attached pages according to the collating instructions on the back of this cover. Change bars in the margins indicate technical changes and additions. These changes will be incorporated into the next revision of the manual.

Note:

Insert this cover behind the manual cover to indicate the updating of the manual with Addendum B.

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COLLATING INSTRUCTIONS

To update this manual, remove old pages and insert new pages as follows:

Remove	Insert
1-1, 1-2	1-1, 1-2
1-3, 1-4	1-3, 1-4
3-17, 3-18	3-17, 3-18
C-5, C-6	C-5, C-6

File No.: 1P03, 1L03, 1U03

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Contents

Figures

Tables

Section 1
System Description

The DATANET Network Processor encompasses a whole family of compact, powerful network processors which can provide Honeywell 66/DPS, 68/DPS and DPS 8 systems with large-volume network communications power. Based on Honeywell's minicomputer technology for reduced space, greater reliability, and easier serviceability, the DATANET is logically compatible with the system software and user-generated programs of the DATANET 6600 family of network processors (see Figure 1-1).

The DATANET provides the variety of interfaces required by the elements and protocols of a distributed system, as well as a facility for dialog with the central system. By performing the tasks of message management and message handling, the processor relieves the central system for other processing functions. The resources of the central system are called upon only when the message is submitted for information processing. However, some networking functions (e.g., a message switch) can be accommodated by the processor without any involvement of the host processor.

SYSTEM COMPONENTS

The DATANET consists of combinations of the following major components (see Figure 1-2):

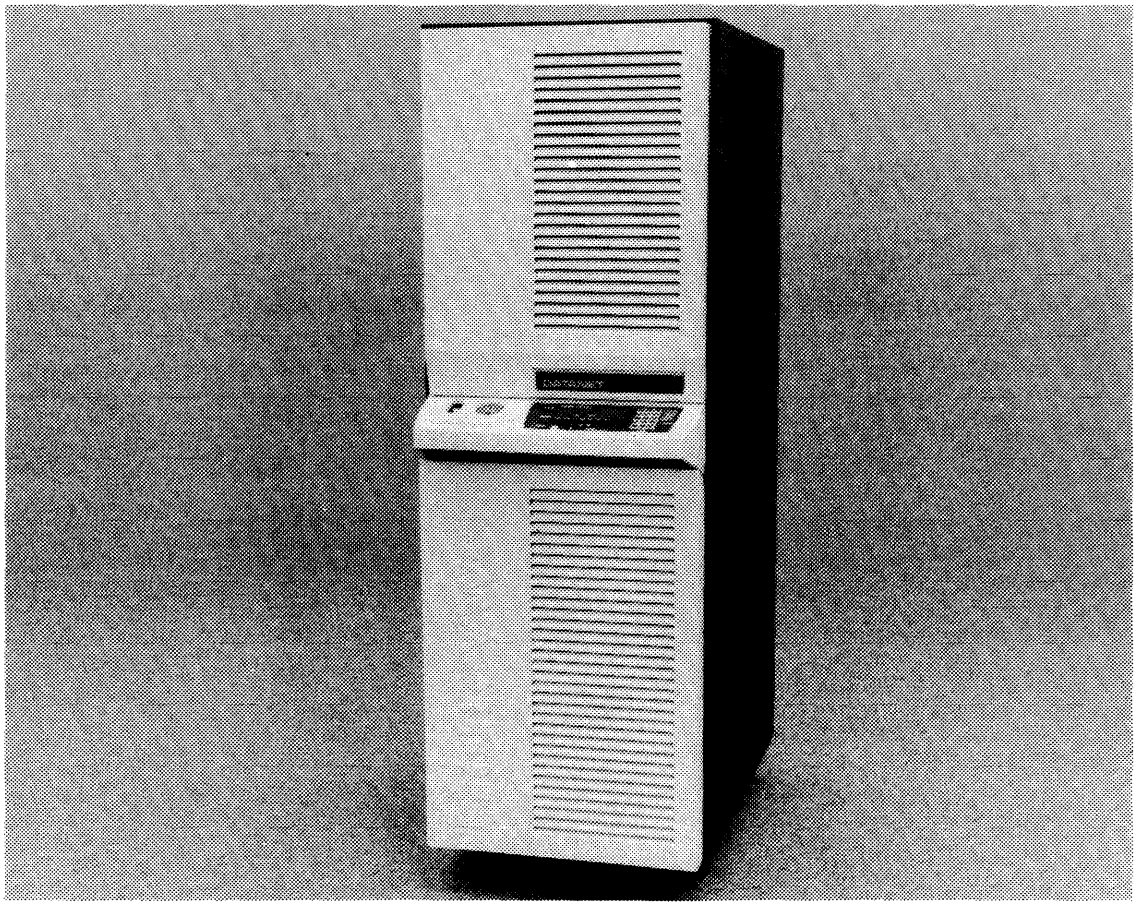


Figure 1-1. DATANET Network Processor

- Central Processor
- Memory
- Cache Memory (if present)
- Page Unit (if present)
- System Bus
- Input/Output Multiplexer
- I/O Bus
- Peripheral Interface Adapter (if present)
- System Support Controller
- Direct Interface Adapter
- Channel Interface Base (CIB)/General Purpose Communication Base (GPCB)

CENTRAL PROCESSOR

The central processing unit is a solid-state, interrupt-driven, 18-bit machine operating asynchronously under firmware control. Its instruction repertoire is designed for efficient processing of a wide variety of communication network applications and is fully upward-compatible with the instruction sets of other Level 66 or Level 68 network processors. The processor design accommodates a high-speed cache memory which, together with the appropriate configuration and optimum instruction mix, provides an execution rate of up to 1,000,000 instructions per second — nearly double that of other DATANETs.

Standard features include a flexible bus structure, power failure/automatic restart, EDAC (Error Detection and Correction) memory, processor faults (internal interrupts), program interrupts (external interrupts), a real-time clock, and a watchdog timer.

MEMORY

The high-speed, random access, semiconductor memory subsystem performs all storage functions without restrictions on address sequences, data patterns, or repetition rates. Memory features include single- and double-fetch, self-contained initialize and refresh logic, and standard EDAC functionality. The DATANET may be configured with up to 256K words maximum.

CACHE MEMORY

The cache memory (if present) provides intermediate high-speed storage, which improves the performance of the central processor unit by decreasing the time required to receive (i.e., fetch) instructions and data from main memory. This decrease in time is achieved both by anticipatory main memory reads and by storage of previously used data and instructions for future iterations of the currently executing program.

The cache memory contains copies of selected (recently referenced) memory locations. It has a system bus interface which allows it to make memory read references on behalf of the central processor unit and to monitor the system bus, copying main memory write data if it currently contains a copy of the location addressed. The cache memory also has a private interface allowing it to communicate with the central processor unit to which it is dedicated. It receives memory read requests across this interface, thereby becoming committed to locate the data for the central processor unit in its local cache array or in main memory. In either case, the requested data is delivered to the CP for processing. The cache memory overlaps its read requests to main memory and is invisible to software.

PAGE CONTROL LOGIC UNIT (PCLU)

The PCLU (if present) enhances the DATANET system by providing a mechanism for memory protection and for accessing over 64K bytes of memory. The PCLU uses software-generated page address tables to expand a 15-bit (16K-byte) CP program address into an 18-bit 512K-byte) absolute address. The tables are also used to determine the access rights assigned each 256-location (page) of memory.

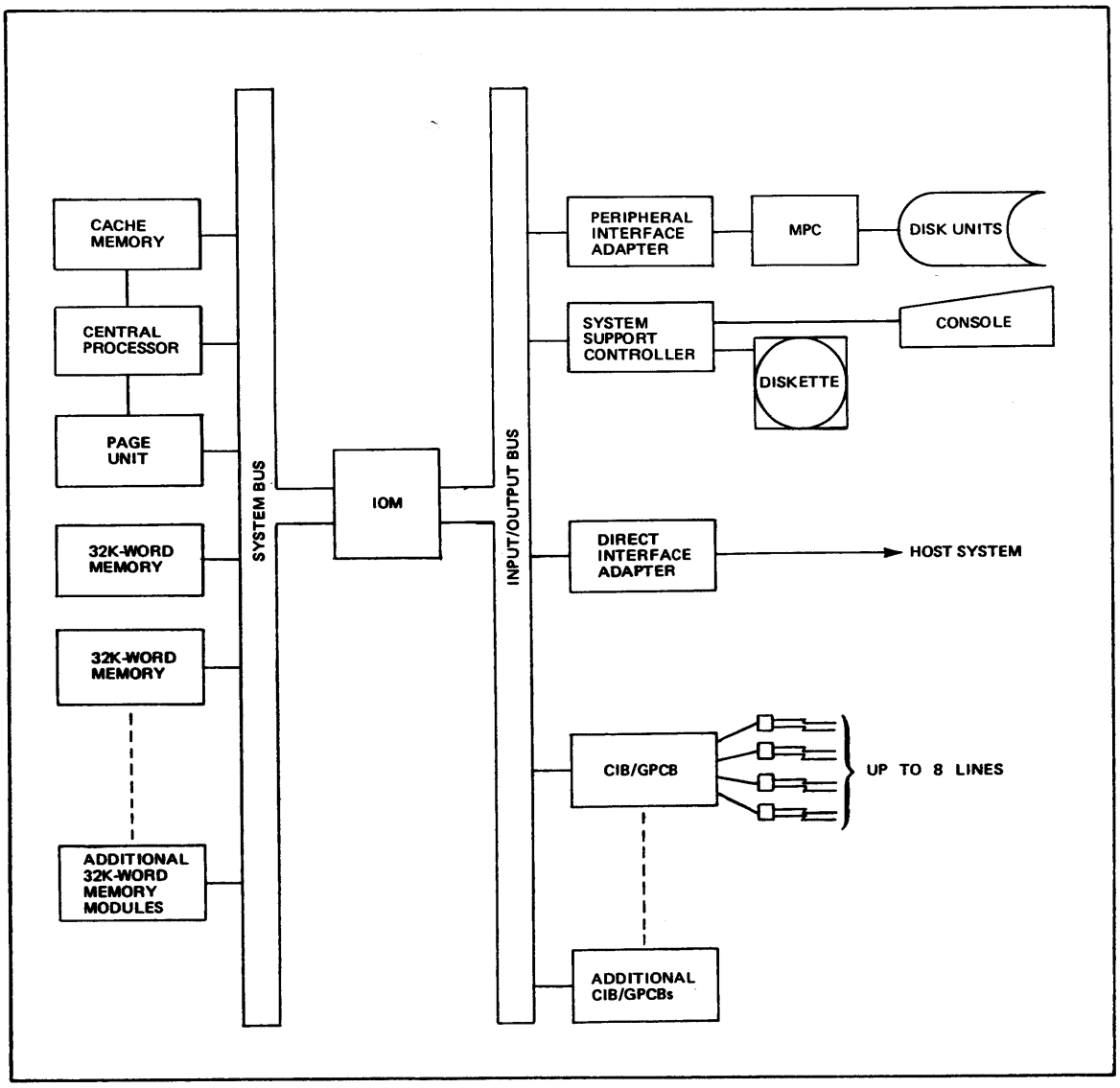


Figure 1-2. DATANET System Components

SYSTEM BUS

The system bus allows communication between the CP, memory, and the input/output multiplexer. The system bus is bidirectional, permitting any two units to communicate with each other at a given time. The transfer of information between units forms a master/slave relationship (i.e., the unit requesting and receiving access to the bus becomes the master; the unit being addresed by the master becomes the slave). If the communication requires a response, the responding slave unit assumes the role of master and the requesting unit (previous master) becomes the slave.

All information transfers are from master to slave and each transfer is referred to as a bus cycle. This cycle is the period of time in which the requester (master) asks for use of the bus. If no other unit of a higher priority is making a bus request, use of the bus is granted to the requester (master). The master then transmits its information to the slave and the slave acknowledges the communication.

Communication between a master and slave requires a response from the slave when the slave is transferring data (e.g., a memory read command). In this case, the request for information requires one bus cycle and the transmission of information back to the requester requires an additional bus cycle to complete the task.

The granting of time on the bus is done on a priority basis. If two components on the bus simultaneously request time, the one with the higher priority will be granted the time. This priority is determined by the physical position of the component on the bus. On the system bus, the lower the physical position, the higher the priority. The priority is established relative to the rate at which the components transfer and/or receive data.

INPUT/OUTPUT MULTIPLEXER (IOM)

The IOM performs all operations required for the transfer of data between input/output devices and the DATANET memory. The advanced technology of the DATANET gives it a transfer rate of 2,000,000 bytes per second. The IOM is the interface between the system bus (to processor and memory) and the I/O bus (to which the various I/O devices are connected). Attached to the I/O bus are the System Support Controller for the console and diskette; the Direct Interface Adapter (DIA), which provides connection to the central system; the Channel Interface Bases/General Purpose Communication Bases, through which the network devices enter the system; and the Peripheral Interface Adapter (PIA), which provides connection to the central system's mass storage processor. Internally, the IOM operates asynchronously in an interrupt-driven fashion.

I/O BUS

The I/O bus is basically the same as the system bus, differing only in the units that interface on the bus and the operations that take place between the units.

The I/O bus allows communication between the I/O controllers and adapters to the system through the IOM. Operations on the I/O bus are initiated by the IOM or DIA, depending on the activity that is required.

The components on the bus are positioned relative to their priority. The highest priority component is placed at the bottom of the I/O bus next to the IOM; the lowest priority component is placed at the top of the I/O bus farthest from the IOM. The I/O bus is at the top of the chassis; the system bus is at the bottom of the chassis.

PERIPHERAL INTERFACE ADAPTER (PIA)

The PIA, which is an option, provides the interface between the DATANET input/output bus and the central system's mass storage processor. Up to two PIAs can be installed in a system; however, the software will utilize only one PIA. The PIA provides the disk access required by the NPS (Network Processing Supervisor) software.

SYSTEM SUPPORT CONTROLLER (SSC)

The SSC is a peripheral controller for the console and diskette. The console is used to control and monitor DATANET activity. The diskette unit is used to load the system offline test and diagnostics (T&Ds).

DIRECT INTERFACE ADAPTER (DIA)

The DIA provides the interface between the DATANET input/output bus and the Level 66 or 68 host system for the transfer of data and control information. The DATANET controls all transactions and normal data transfer activities through the DIA except for "initiate bootload" or program interrupts from the central system. A second DIA can be installed in a system; however, the software will utilize only one DIA.

CHANNEL INTERFACE BASE (CIB)/GENERAL PURPOSE COMMUNICATION BASE (GPCB)

The CIB/GPCB enables low-, medium-, and high-speed data communications terminals and subsystems operating at data transfer rates of up to 72,000 bits per second to be connected to the system. Combinations of half-duplex and full-duplex transmission modes, as well as synchronous and asynchronous transmissions, are supported. The CIB/GPCB provides the line interfacing arrangements necessary to accommodate terminals with various transfer rates, bit orders, bits per character, information codes, character sets, message formats, and communica-

tions control procedures. The CIB/GPCB enables the connection of up to eight communications lines depending upon the functions required. Additional CIB/GPCBs can be configured.

The CIB/GPCB accepts up to 4 (or up to 2 double-size) communications adapters in any combination. A dual channel can connect two lines. The various communications adapters are as follows:

- 20 mA Current Loop — dual
- RS-232-C Synchronous — dual
- RS-232-C Asynchronous — dual
- Automatic Call Unit — dual
- MIL-STD-188C — broadband
- MIL-STD-188C — synchronous
- MIL-STD-188C — asynchronous, dual
- MIL-STD-188C — HDLC
- Bisynchronous — dual
- Broadband
- Broadband CCITT-V.35
- HDLC — voicegrade
- Bisynchronous — broadband
- Broadband — HDLC
- HDLC CCITT-V.35
- Direct Connect — asynchronous
- Direct Connect — synchronous

Note:

Direct connect capability is via cable.

SYSTEM SOFTWARE

Either the Remote Terminal Supervisor (GRTS I/3I; GRTS II Rel. 1) or the Network Processing Supervisor (NPS), Release NT2 (or greater), depending upon network requirements, can control the operation of the DATANET Network Processor and provide a software interface to the central system. GRTS I/II is a high-performance, low-overhead system for users who do not need the full networking capabilities of NPS. Both systems support remote job entry, message concentration, transaction processing, and time sharing dimensions. NPS offers completely unique device control parameterization facilities and other outstanding customization features. By utilizing a DATANET Network Processor channel to the central system's mass storage processor, NPS can provide journalization and message switching capabilities.

BUILT-IN TESTS

A portion of the firmware on the CP, memories, IOM, Channel Interface Bases, and System Support Controller boards is reserved for two types of hardware verification routines called Quality Logic Tests (QLTs) and Extended QLTs (E-QLTs). Their purpose is to verify basic data paths and to provide a go/no-go visual identification of a hardware failure.

The QLTs are automatically executed as part of the normal system initialization procedure. Unsuccessful completion of any QLT turns on the CHECK indicator on the CP control panel and an LED (light-emitting diode) indicator on the specific board failing the QLT. (Access to QLT indicators on the boards is described in Section 3.) The QLTs do not affect memory or programmable registers. The QLTs will truncate the most significant bit of the Instruction Counter (A0); however, its true value will be shown in the hex display before truncation. The operator should make note of A0 after the QLTs. In addition, on the

Channel Interface Base boards, each of the eight lines has program-usable loop-back of data transmit to data receive to facilitate diagnosis.

The Extended QLTs are executed under the guidelines described in Section 3. The E-QLTs provide greater checking capability than the QLTs in that the E-QLTs allow communications between various system components in their testing scheme. However, since E-QLTs destroy memory and register contents, a dump should be taken first. Instead of an LED lighting on a specific board (as with the QLTs), the control panel display is used. Its interpretation dictates the action to be taken.

Section 2
System Operation

DATANET Network Processor operation is controlled by the software except for occasional operator interventions. The operator duties and responsibilities in regard to the DATANET system are normally governed by the rules and regulations in effect for the Series 60 Level 66 or Level 68 system on the site. All subsystem maintenance required on the equipment is performed by the Honeywell Field Engineer, except routine site cleaning which is the responsibility of the operating personnel. The operator is also required to execute the E-QLTs and to load and run the system test and diagnostic programs. These procedures are explained in Section 3.

To operate the DATANET, the operator must know how to operate the following controls and equipment (see Figure 2-1):

- Power Distribution Unit
- Central Processor Control Panel
- Console (Basic or Heavy-Duty)
- Diskette Unit

It is also the operator's responsibility to routinely do the following:

- Power up the system
- Initialize the system
- Power down the system

POWER DISTRIBUTION UNIT

For the system to operate, all power supplies and the Power Distribution Unit (PDU) must be turned on.

Power is applied to the system in the following order:

1. Power Distribution Unit
2. Central Processor Unit
3. Peripherals (Console and Diskette Unit)

The PDU is located in the bottom of the rack (see Figure 2-1).

CONTROL

ON/OFF Switch	The operator must set the PDU ON/OFF switch to the ON position. This action must be taken before power is applied to the central processor.

CENTRAL PROCESSOR CONTROL PANEL

The DATANET has a control panel that provides for the following (see Figures 2-1 and 2-2):

- Powering up and initializing the system
- Starting and stopping the CP
- Entering and displaying registers/memory information
- Single stepping a program
- Bootloading a program
- Master clearing the system
- Indicating CP status

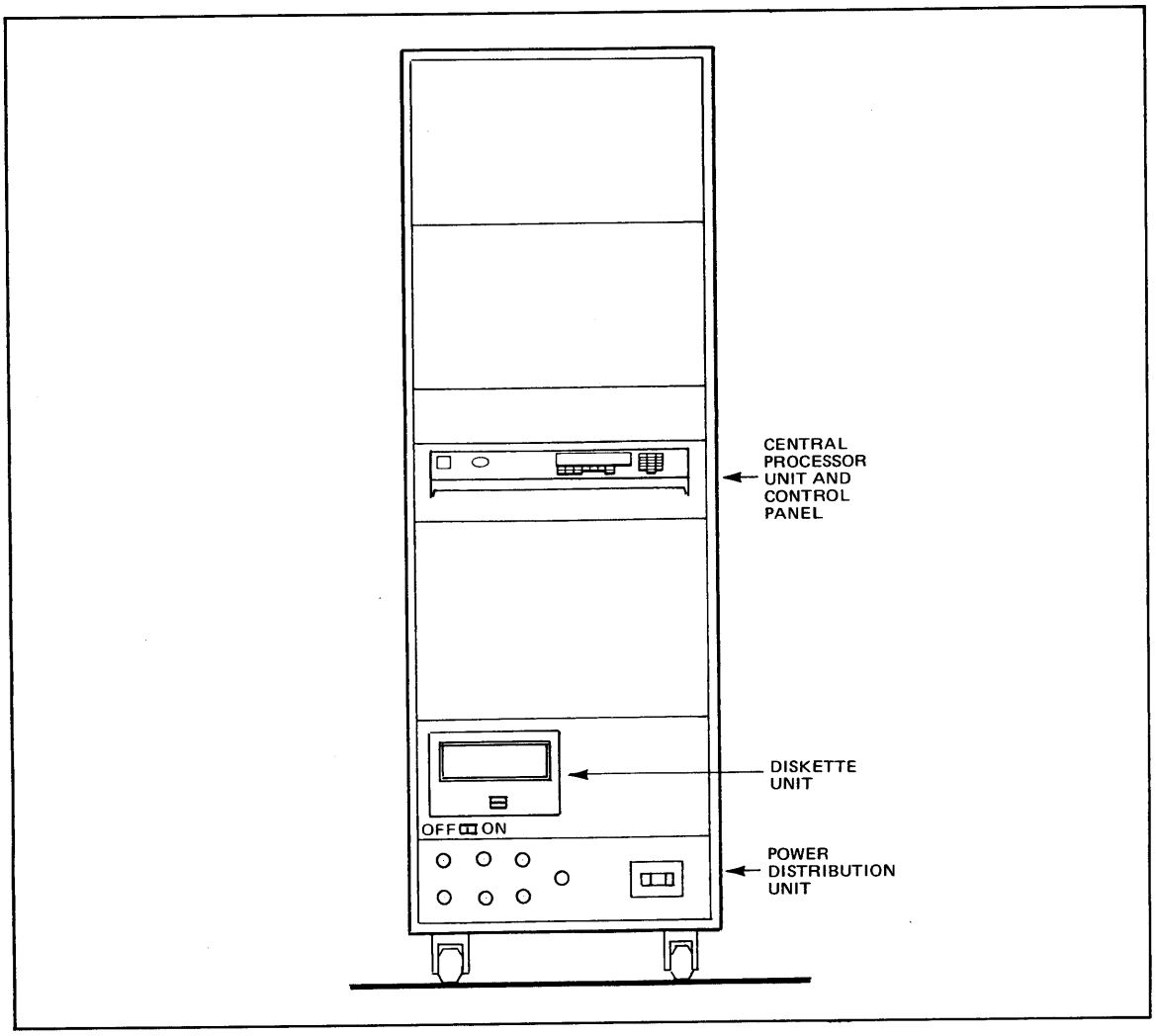


Figure 2-1. DATANET Rack Layout

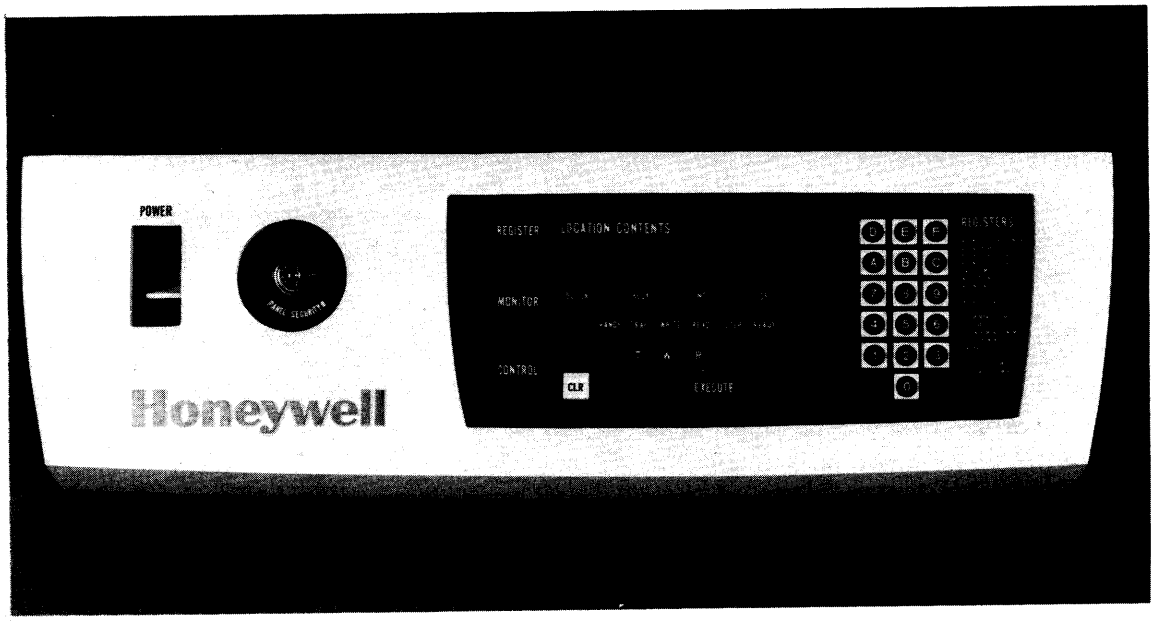


Figure 2-2. DATANET Control Panel

REGISTER DISPLAY

The register display is divided into two sections — one labeled LOCATION and the other CONTENTS.

- LOCATION — A 2-digit display which indicates the specific CP register selected. The display consists of a left hexadecimal digit indicator and a right octal digit indicator.
- CONTENTS — A 6-digit octal display which indicates the contents of the selected register.

OCTAL/HEX KEYPAD

The octal/hex keypad consists of 16 keys and is divided into two groups — an octal digit key cluster and a hex alphabetic key cluster.

- Octal Digit Key Cluster — The digits 0-7 are used to enter address or data into the CONTENTS and LOCATION displays.
- Hex Alphabetic Key Cluster — The digits 8-F are used to enter digits into the LOCATION display.

POWER SWITCH

The power switch is used to apply or remove ac power to or from the system. In the up position, power is on; in the down position, power is off.

PANEL SECURITY KEYLOCK SWITCH

The left (locked) position disables panel switches and push-buttons except for POWER. The right (unlocked) position enables panel switches and push buttons.

INDICATORS

The indicators are long-life, light-emitting diodes (LEDs).

DC ON	Indicates that dc power is applied to the system.
CHECK	Indicates that the system is performing or has been unable to successfully complete its QLTs after a system initialization.
INT	Indicates that the control panel interrupt is active. If indicator stays lit, the system is in a "hung" or non-interruptible "fault" state. (Refer to "System Initialization Procedure").
CP	Indicates that the CP is executing instructions.
CHANGE	Indicates that key cluster information may be entered into the CONTENTS display.
TRAP	Indicates that the CP is in the trap mode.
WRITE	Indicates that the CP is in the write mode.
READ	Indicates that the CP is in the read mode.
STOP/STEP	Indicates that the CP is in the stop mode.
READY	Indicates that the CP is in the ready mode.

PUSH BUTTONS

CLR (Master Clear)	Press to initialize the system.
S (Select)	Press to allow key cluster information to be entered into the LOCATION display.
C (Change)	Press to allow key cluster information to be entered into the CONTENTS display.

T (Trap)	Press to place the CP in a constant panel interrupt mode after every interruptible instruction to allow the CP to stop for a variety of predetermined comparisons. **Note:** Not for normal operator use; for reference purposes only.
W (Write)	Press to place the CP in the write mode so that CONTENTS information is written into CP registers or into main memory.
R (Read)	Press to place the CP in the read mode so that the contents of the CP registers or main memory are read and displayed in the CONTENTS display.
S (Stop/Step)	Press to remove the CP from the run, ready, write, or read mode and place it into the stop mode.
R (Run)	Press to place the CP in the ready mode.
E (Execute)	Press to place the CP in the run mode, allowing it to execute instructions and interrupts according to its internal state.

OPERATION

The functions that can be performed from the control panel are: displaying/changing memory, displaying/changing registers, executing single instructions, restarting programs, and master clearing the processor. Before any operation is performed from the control panel (except for powering up/down), it must first be unlocked using the panel security key.

Table 2-1 lists the various operations that can be performed via the operator control panel. The table lists the five operating modes, all the DATANET registers that an operator can select, and the resulting operation that can be performed.

TRAP MODE

Trap mode is a special mode which enables the field engineer or a programmer to stop on an address or a data pattern.

It is possible to trap on a special value of the instruction counter, index register 1, 2, or 3, A register, Q register, indicator register or a given value at location "X" in memory.

When the specified condition is met the CP will go into stop mode. However, if an interrupt occurs, the CP (if not in inhibited mode) will continue operation.

CAUTION

Trap mode causes the DATANET system to run 10 times slower, and heavily loaded systems may cause other unknown problems.

Examples:

Instruction Counter: stop if IC=001000
Select A0, change, 001000, trap, execute.

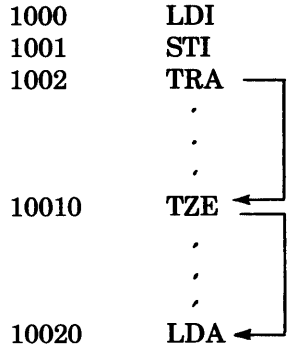
Index Register: stop if X = 001000
Select A1 (respectively A2, A3), change, 001000, trap, execute.

A Register, Q Register, Indicator Register: stop if_____ =001000
Select A4 (respectively A5, A6) change, 001000, trap, execute.

Main Memory: stop if location 000100=123456
Select C0, change, 000100, write, execute.
Select C1, change, 123456, trap, execute.

Notes:

1. If running a program and compare is made the STOP/STEP LED will come on.
2. When the CP is in stop mode, if an interrupt comes along it could send the CP into run mode again.
3. CP can only compare addresses between interruptible instruction. For example:



Any attempt to trap on instruction counter=10010 will fail because all the above instructions except LDA are non-interruptible. Conversely, if the LDI was loading the indictors with the "compared" value, the CP would stop only at the end of the LDA at 10020 and the instruction counter would indicate 10021 because it would be the first interruptible instrution where the condition is met.

DISPLAY MEMORY

Any memory location may be accessed and displayed from the control panel by entering the memory address to be accessed into register C0 (actually memory location 000634) and then reading or writing that location by selecting C1. Sequential memory locations can be read or written by selecting C2 instead of C1 for incrementing memory locations, or C3 for decrementing memory locations.

1. Press Select.
2. Press octal/hex-pad keys C0. This enters the 2-digit selection code for the memory address register.
3. Press Change. This places the processor in change mode preparatory to keying in the address of the memory location to be displayed. The CHANGE indicator lights when the Change control key is pressed.
4. Key in, via the octal hex-pad keys, the 6-digit octal value representing the address of the memory location to be read. This address appears in the CONTENTS field of the REGISTER display.
5. Press Write.
6. Press Execute.
7. Press Select.
8. Key in, via the octal/hex-pad keys, the 2-digit selection code for the desired memory data register (C1, C2, C3, C4, C5, C6, or C7).
9. Press Read.

TABLE 2-1. SUMMARY OF CONTROL PANEL OPERATIONS

Mode	Register (hex)	(octal)	Operation
STOP	B	0	Bootstrap with timer on
		1	Bootstrap with timer off
	A, C, or D		Step submode — executes single instructions with subsequent pressings of Stop key
RUN			Run mode
READ	A	0	Read Instruction Counter
		1	Read Index Register 1
		2	Read Index Register 2
		3	Read Index Register 3
		4	Read Accumulator
		5	Read Quotient Register
		6	Read Indicator/Select Register
		7	Display parity error
	C	0	Read "AOR" unpaged
		1	Read MM
		2	Read MM unpaged AOR + 1
		3	Read MM unpaged AOR − 1
		4	Read "AOR" paged
		5	Read MM paged
		6	Read MM paged AOR + 1
		7	Read MM paged AOR − 1
WRITE	A	0	Write Instruction Counter[a]
		1	Write Index Register 1
		2	Write Index Register 2
		3	Write Index Register 3
		4	Write Accumulator
		5	Write Quotient Register
		6	Write Indicator/Select Register
	C	0	Write "AOR" unpaged
		1	Write MM unpaged
		2	Write MM unpaged AOR + 1
		3	Write MM unpaged AOR − 1
		4	Write "AOR" paged
		5	Write MM paged
		6	Write MM paged AOR + 1
		7	Write MM paged AOR − 1
	D	0	Turn timer on
		1	Turn timer off[a]
		2	Run Extended QLTs[a]
		3	Turn Cache off[a,b]
TRAP			Trap mode

[a]Do not perform this operation while running system software.
[b]This operation will also light the CHECK LED.

Notes:

1. The operator should never write into register C4 and then read/write into any of the following registers: C1, C2, C3, C5, C6, or C7. Rather, write into C0, then read C4 for the correspondence between paged and unpaged addresses.
2. Memory address register C0 is at times loaded with an invalid memory address by the T&Ds; therefore, never perform a read operation of C0 before writing in a valid memory address; otherwise, an illegal memory operation fault will occur.
3. A Master Clear resets the Pager to zero and it is not possible to page again.

10. Press Execute. This loads the data contents of the selected memory location into the selected register and displays it in the CONTENTS field of the REGISTER display.

    Note:

    If an increment or decrement memory data register code was entered in step 8, subsequent pressings of the Execute key will increment or decrement the display as appropriate.

CHANGE MEMORY

Any memory location may be accessed and changed from the control panel. As mentioned previously, the memory address register (C0) is the only visible register that can be used to access memory locations from the control panel.

The following procedure describes a method for changing the contents of one memory location and, as an option, changing the contents of subsequent memory locations.

1. Press Write. This places the processor in write mode and instructs that the contents of the memory location addressed by the memory address register (C0) are to be changed. The WRITE indicator lights when the Write control key is pressed.
2. Press Select. This places the processor in select mode as a necessary preliminary to selecting the memory address register. This step is not necessary unless the CHANGE indicator is lit.
3. Press octal/hex keys C0. This enters the 2-digit selection code for the memory address register. Digits C0 appear in the LOCATION field of the REGISTER display.
4. Press Change. This places the processor in change mode preparatory to keying in the address of the memory location to be changed. The CHANGE indicator lights when the Change control key is pressed.
5. Key in, via the octal/hex keys, the 6-digit octal value representing the address of the memory location to be changed. This address appears in the CONTENTS field of the REGISTER display.
6. Press Execute.
7. Press Select. This returns the processor to select mode as a necessary preliminary to selecting the memory data register. The CHANGE indicator turns off when the Select control key is pressed.
8. Press octal/hex keys. This enters the 2-digit selection code for the memory data register. The digits appear in the LOCATION field of the REGISTER display.
9. Press Change. This places the processor in change mode preparatory to keying in the data for the memory location that is to be changed. The CHANGE indicator lights when the Change control key is pressed.
10. Key in, via the octal/hex keys, the 6-digit octal value representing the new data that is to be entered into the memory location to be changed. The data entered appears in the CONTENTS field of the REGISTER display.
11. Press Execute. This loads the new data contents into the selected memory location.
12. If successive memory locations are to be changed, repeat steps 10 and 11 for each sequential memory location to be changed.

DISPLAY REGISTERS

The contents of any of the visible registers may be displayed on the control panel. A register may be displayed when the processor is in any mode.

The following procedure describes a method for displaying the contents of a register. The same procedure applies regardless of the processor mode.

1. Press Select. This places the processor in select mode as a necessary preliminary to selecting the register to be displayed.

2. Key in, via the octal/hex keys, the 2-digit selection code for the desired register to be displayed. The selection code appears in the LOCATION field of the register display.
3. Press Read.
4. Press Execute. This displays the data contents of the selected register in the CONTENTS field of the REGISTER display.

CHANGE REGISTERS

The contents of software-visible registers may be changed from the control panel. The following procedure describes a method for changing the contents of a register.

1. Press Write. The WRITE indicator lights when the Write control key is pressed.
2. Press Select. This places the processor in the select mode as a necessary preliminary to selecting the register to be changed.
3. Key in, via the octal/hex keys, the 2-digit selection code for the desired register to be changed. The selection code appears in the LOCATION field of the REGISTER display.
4. Press Change. This places the processor in change mode preparatory to keying in the data to the register that is to be changed. The CHANGE indicator lights when the Change control key is pressed.
5. Key in, via the octal/hex keys, the octal value representing the new data that is to be entered into the selected register. The data entered appears in the CONTENTS field of the REGISTER display.
6. Press Write.
7. Press Execute.

STOP PROGRAM EXECUTION

While a program is running, program execution can be stopped at any time by pressing Stop and Execute. The STOP/STEP indicator lights and the RUN, READY, and CP indicators turn off. When this action is initiated, the processor completes the execution of the current instruction and enters the stop mode. After this mode is achieved, the following conditions exist.

1. The processor is automatically placed in a step mode (i.e., ready to execute one instruction at a time).
2. The instruction counter (A0) contains the instruction to be executed next.

Note that when a program is running and a DIS instruction is encountered (RUN indicator remains lit, but the CP indicator turns off), the processor does *not* enter the stop mode, but rather enters an idle condition. In this condition, the DIS instruction is continuously re-executing and the processor is subject to external interrupts, etc. The Stop control key must be pressed in order to set the processor into a stop mode.

EXECUTE SINGLE INSTRUCTION(S)

When running a program, it may be desirable to stop processing and step through the execution of one or more instructions. This procedure is accomplished from the control panel, as follows:

1. Press Stop and Execute. (Refer to the previous procedure, "Stop Program Execution," for relevant information concerning processor/panel status after a stop mode is achieved.)
2. Determine whether the processor has stopped at a point (address) from which you wish to begin executing single instructions. Display and view the contents of the instruction counter (A0) using the procedure previously described for displaying registers.

   At this point memory address register (C0) contains an address incremented by 1 from the address of the instruction to be executed next.

TURN ON ELAPSED TIMER

1. Press Select.
2. Key-in, D0.
3. Press Write.
4. Press Execute. (Timer is now turned on.)

TURN OFF ELAPSED TIMER

1. Press Select.
2. Key-in, D1.
3. Press Write.
4. Press Execute. (Timer is now turned off.)

CHECK TIMER OPERATION

1. Press Select.
2. Key-in, C0.
3. Press Change.
4. Key-in, 000451.
5. Press Select.
6. Press Write.
7. Press Execute
8. Key-in, C1.
9. Press Read.
10. Press Execute several times. Note that the display should change each time Execute is pressed. If not, timer is turned off. However, if the timer is not running and has not been turned off (assuming the control panel is operational), either the IOM is hung or a breakdown in communication between the IOM and CP has occurred since the last Master Clear. To determine if the IOM is hung, attempt to turn the timer on *twice* from the control panel. If the INT indicator does *not* light after the second Execute, the IOM is *not* hung.

BASIC CONSOLE

The basic console (see Figure 2-3) has a 64-character ASCII code set, prints at 10 characters per second and has 72 print positions. It uses a paper roll 8.5 in. (21.6 cm) wide and 5 in. (12.7 cm) in diameter. The basic console is also equipped with an automatic shutdown feature which can extend console life and reduce maintenance costs.

CONTROLS

Console controls are described below.

KEYBOARD

The teleprinter keyboard (see Figure 2-4) is similar to a standard typewriter keyboard. The keys are interlocked so that only correct combinations may be pressed simultaneously. Some of the ASCII keys are inscribed with words such as FORM and EOT for control functions. When a key is pressed, it generates a printable ASCII character.

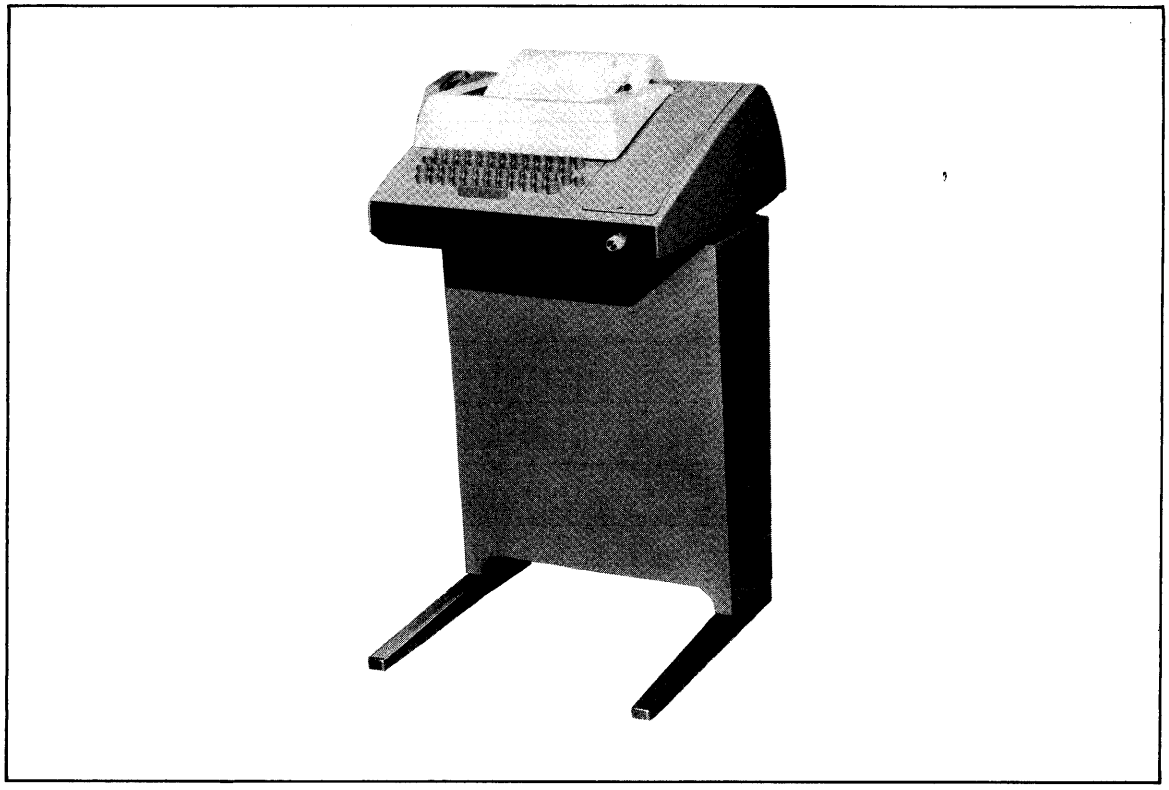


Figure 2-3. Basic Console

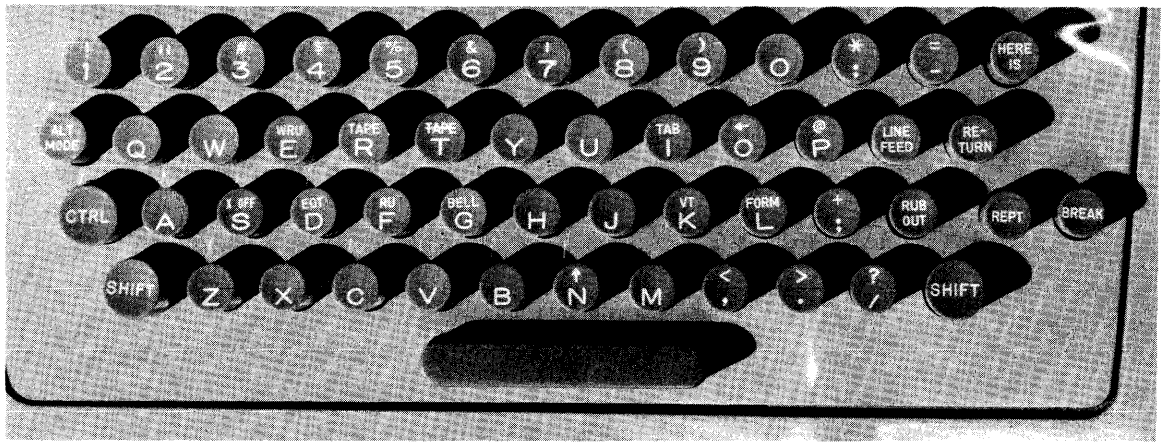


Figure 2-4. Keyboard Layout

CONTROL KEYS

The control keys used for normal teleprinter operation include the following:

LINE/OFF/LOCAL — This switch, located on the right side of the front panel, is the main power switch for the device.

- In the OFF position, the device is disabled.
- In the LINE position, the device is enabled to send to or receive from the central processor in the full-duplex mode.
- In the LOCAL position, the device is offline in the half-duplex mode.

CTRL (Control)	Pressing the control key does not generate any code, but allows some of the keys to generate nonprintable function characters. When CTRL is pressed, inappropriate keys (mostly those having uppercase characters) are locked out.
SHIFT	Pressing the SHIFT key causes all the ASCII keys to generate their associated uppercase characters.
LINE FEED	Pressing the LINE FEED key causes the paper to advance vertically. The carriage does not return to the left margin (see RETURN).
RETURN	Pressing the RETURN key generates a carriage return character. The type unit returns to the left margin but the paper does not advance vertically. The RETURN key should be used with the LINE FEED key to advance the paper vertically.
RUB OUT	Pressing the RUB OUT key generates an octal code 377 each time. For example, by backspacing a paper tape and punching RUB OUT over an error, the error is converted to octal code 377 and is ignored upon subsequent reading.
REPT (Repeat)	Pressing the repeat key simultaneously with another key causes the normal action of the other key to be repeated as long as the two keys are pressed.
ALT MODE	Pressing the ALT MODE key produces an octal code of 375. When ALT MODE is pressed simultaneously with the CTRL key, an octal code of 275 is produced.
BREAK	Pressing the BREAK key interrupts output on the console from the system.

AUTOSHUTDOWN

The basic console is equipped with an automatic shutdown feature which turns the device off in the absence of activity from the central processor for a 1-minute period (when operating with the control switch set to the LINE position).

The central processor activates the console whenever activity is awaiting transmittal. The operator can also activate the device by pressing the BREAK key.

OPERATION

Operating procedures for the teleprinters are described below.

APPLYING POWER

Set LINE/OFF/LOCAL switch to LINE or LOCAL position.

REMOVING POWER

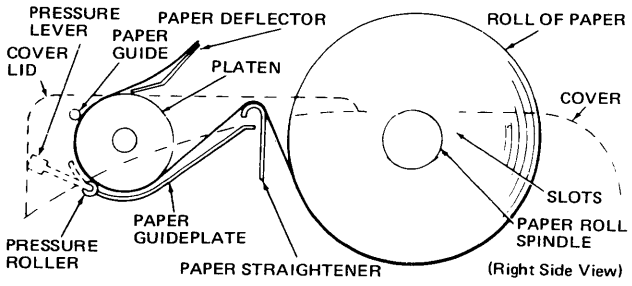
Set LINE/OFF/LOCAL switch to OFF position.

PAPER LOADING

To install a new paper roll, follow these directions. Figure 2-5 illustrates the components discussed in the text.

1. Set LINE/OFF/LOCAL switch to OFF position.
2. Install a new paper roll in the unit by inserting the spindle into the new paper roll.
3. Place the roll in the recess provided at the rear of the cover. The ends of the spindle extending from both ends of the roll should rest in the associated slots (see Figure 2-5 for paper feed direction).

4. Raise the clear plastic lid over the typing unit.
5. Fold and crease the leading edge of the paper to present a smooth threading edge for feeding.
6. Release the tension of the typing unit platen by moving the pressure lever.
7. Push the paper under the platen roller as far as possible and move the pressure lever backwards to reapply roller tension.
8. Push the platen knob to feed the paper forward until it can be passed under the unit paper guide.
9. If necessary, again release the tension on the pressure rollers and straighten the paper.
10. Reapply roller tension.
11. Close the cover.
12. Set LINE/OFF/LOCAL switch to LINE or LOCAL position.



This illustration from Technical Manual Models 32 and 33 Teletypewriter Sets Keyboard Send-Receive (KSR) Receive-Only (RO) Automatic Send-Receive (ASR), Copyrighted by Teletype Corporation; used with permission.

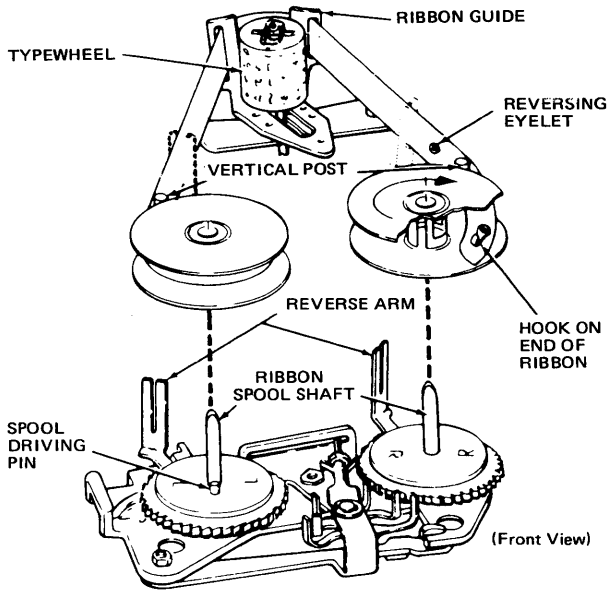
Figure 2-5. Installation of Paper Roll

RIBBON REPLACEMENT

To install a new ribbon, follow these directions. Figure 2-6 illustrates the components discussed in the procedures.

1. Set LINE/OFF/LOCAL switch to OFF.
2. Raise the cover lid.
3. Pull both spools off the friction spindles.
4. Wind the ribbon onto one of the spools.
5. Discard the old ribbon.
6. Unwrap a new ribbon and engage the hook at the end of the ribbon in the hub of the empty spool.
7. Wind a few turns of ribbon onto the empty spool in the direction indicated by the arrow in the hub. Be sure that the reversing eyelet has been wound onto the empty spool.
8. Place the spools on the shafts so that the ribbon feeds to the rear from the right side of the right spool and from the left side of the left spool.
9. Turn each spool slightly until the spool driving pin engages the hole in the spool.
10. Guide the ribbon around the right vertical post and through the slot in the reverse arm.
11. Place the ribbon in the ribbon guide behind the typewheel.
12. Guide the ribbon through the left side of the reverse arm and around the vertical post.

13. Rotate the spool to take up any slack.
14. Set LINE/OFF/LOCAL switch to LINE.



This illustration from Technical Manual Models 32 and 33 Teletypewriter Sets Keyboard Send-Receive (KSR) Receive-Only (RO) Automatic Send-Receive (ASR), Copyrighted by Teletype Corporation; used with permission.

Figure 2-6. Ribbon Installation

OPERATOR MAINTENANCE

Operator maintenance includes such preventive maintenance as normal checking and cleaning performed periodically on a routinely scheduled basis. This maintenance will keep the teleprinter in the best operating condition.

The following list is a general guide to operator maintenance:

- Always plug the device into a 3-wire grounded outlet.
- Ensure that all covers are secured and closed during operation.
- Never operate the teleprinter without paper.
- Avoid leaning on or placing objects on any part of the teleprinter.
- Turn the power OFF before replacing paper or ribbons.
- Never put food or beverages on or near the device.
- Keep the outside covers clean and free of debris.
- Clean and dust the inside areas of the print, punch, and reader mechanisms.

HEAVY-DUTY CONSOLE

The heavy-duty console (see Figure 2-7), which is required for NPS operation, has a 64-character ASCII code set and prints at 120 characters per second. It also has 132 print positions. It uses a paper stock with standard continuous fanfold paper forms with feed holes on each edge with or without margin perforations. The accepted forms length is 3.0 in. to 17 in. (7.63 cm to 43.2 cm). The accepted forms width is 4.0 in. to 15 in. (10.16 cm to 38.1 cm).

CONTROLS AND INDICATORS

Console controls and indicators are described in the following paragraphs.

KEYBOARD

The 64-character keyboard is shown on Figure 2-8.

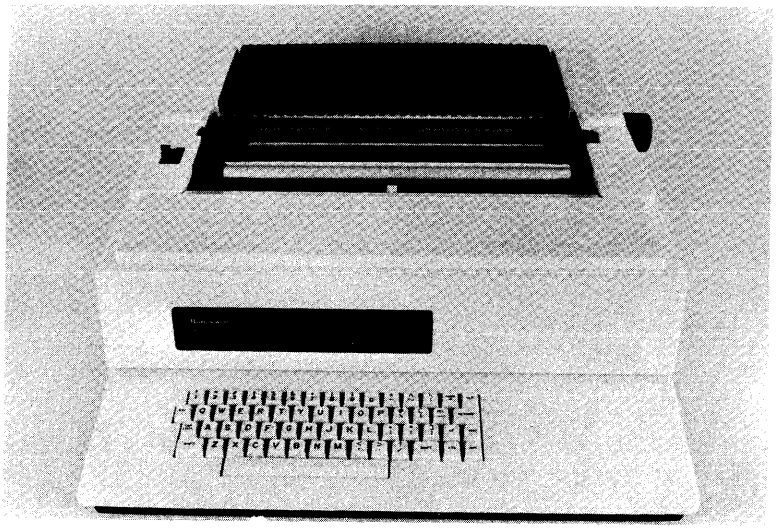


Figure 2-7. Heavy-Duty Console

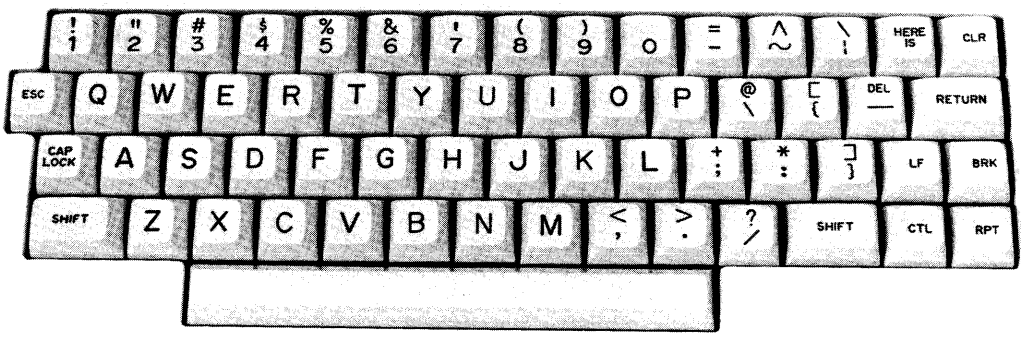


Figure 2-8. Keyboard Layout

CONTROL KEYS

The control keys used for normal operation include the following:

CTL	Pressing the CTL (control) key generates the control function codes of the ASCII code set.
RPT	Pressing the RPT (repeat) key simultaneously with another key causes repeated generation of the other key as long as both are pressed.

LF	Pressing the LF (line feed) key advances the last line upwards one line position.
BRK	Pressing the BRK (break) key allows the operator to generate an interrupt to the system.
RETURN	Pressing the RETURN key causes the carriage to return to the first character position of the same line that it is positioned on.
DEL	Pressing the DEL (delete) key together with the SHIFT key generates an ASCII hex code of 1F.
CLR	Pressing the CLR (clear) key generates an ASCII hex code of 0C. The same code can also be generated by pressing the CTL key together with the L key.
HERE IS	This key is not used.
ESC	Pressing the ESC (escape code) key generates an ASCII hex code of 1B. The same code can also be generated by simultaneously pressing the CTL, SHIFT, and [(left bracket) keys.
CAP LOCK	Pressing the CAP LOCK key locks the keyboard in an uppercase-only operating mode.

CONTROL PANEL

The console control panel is shown in Figure 2-9. The controls and indicators include the following:

MAIN POWER	Pressing this switch (located on the rear of the console) applies or removes power to or from the device.
START	Pressing the START button causes a transition from the standby state to ready state and enables communication with the system.
STOP	Pressing the STOP button causes a transition from the ready state to standby state. It is also used to reset to local condition.
LOCAL	Pressing the LOCAL button allows the console to be used independently from the system (STANDBY lights).
TEST	Pressing the TEST button (preceded by LOCAL) causes a printout of the complete (uppercase and lowercase) character set. Refer to PRINT TEST procedures.
READY	Indicates that the console is in ready state, logically connected to the system, and ready to communicate with the system.
STANDBY	Indicates that the device is powered up, physically connected to the system, but not ready to communicate with the system.
LOCAL	Indicates that the console is in the local mode and can be operated independently of the system.
OFFLINE	Indicates that the console is powered up but not physically connected to the system.
SHIFT	Pressing the SHIFT key with an applicable key generates its associated uppercase character.
Paper-Out Sensor	A sensor, placed on the left tractor, is provided to detect depletion of the forms supply. Upon detection of a paper-out condition, printing is stopped and STANDBY lights.

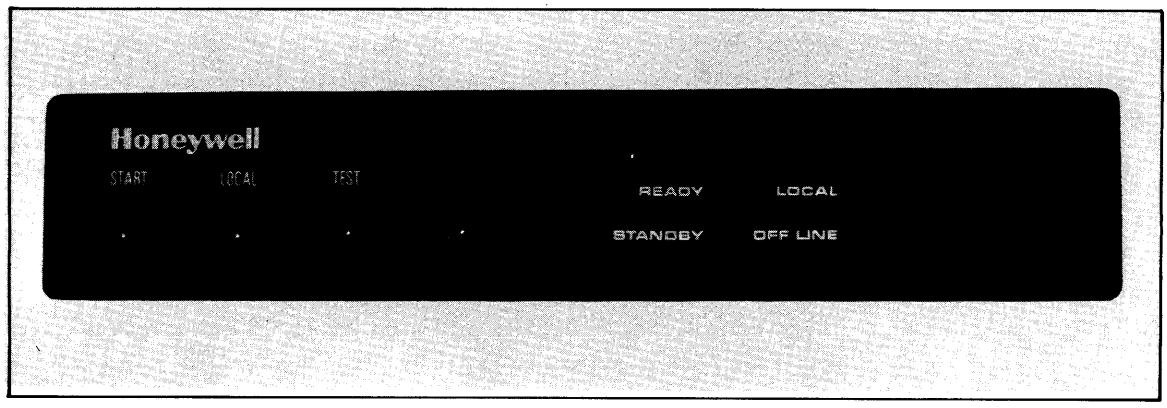


Figure 2-9. Control Panel

MECHANICAL ADJUSTMENTS

There are several mechanical adjustments located in the printer mechanism (Figure 2-10) for the control of printing and paper feeding.

Paper Width Knob	Used to lock/unlock the right tractor so it may be adjusted to accommodate the paper width.
Paper Advance Knob	Used to manually advance paper one or more lines.
Multicopy Adjustment Lever	Used for manual adjustment of the platen in relationship to the print head. The lever is designed with five individual settings (1 through 5) which correspond to the thickness of the applicable form (single through 4-ply). The lever should be checked whenever forms are changed or when the device is turned on to ensure the proper setting. See Table 2-2.

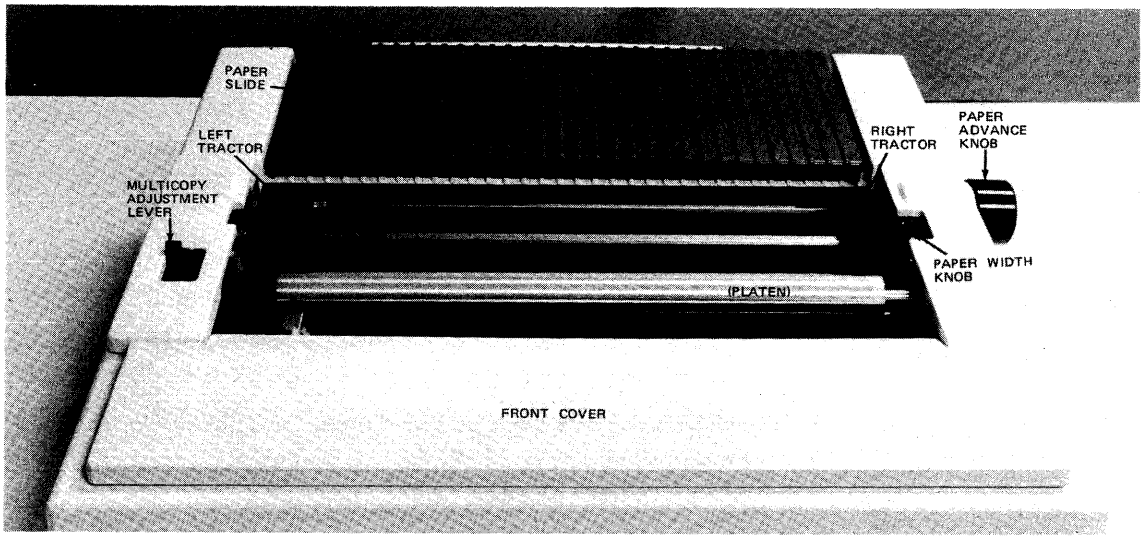


Figure 2-10. Paper Positioning Controls

TABLE 2-2. MULTICOPY ADJUSTMENT LEVEL

Media Thickness	Lever Position
0.07 mm to 0.11 mm (0.003 in. to 0.0043 in.)	1
0.12 mm to 0.22mm (0.0051 in. to 0.0087 in.)	2
0.23 mm to 0.32 mm (0.0091 in. to 0.0126 in.)	3
0.33 mm to 0.42 mm (0.0130 in. to 0.0165 in.)	4
0.43 mm to 0.52 mm (0.0169 in. to 0.0205 in.)	5

OPERATION

Operating procedures for the heavy-duty console are described below.

APPLYING POWER

1. Set power switch on rear of console to ON (STANDBY lights).
2. Refer to "Forms Loading" procedure; otherwise press the START button (READY lights).

REMOVING POWER

1. Press the STOP button.
2. Set power switch on rear of console to OFF (STANDBY turns off).

FORMS LOADING

1. Press the STOP button (if not already stopped).
2. Remove the paper slide.
3. Move the right tractor to accommodate the paper being used by adjusting the paper width knob.
4. Swing the tractor assembly upwards and open the bottom pressure plates (Figure 2-11A).

Note:

The following procedures are best performed from the rear of the console.

5. Feed the paper under the tractor assembly, fit it on the tractors (the leading edge of the paper should not extend beyond the tractors at this point), and close the pressure plates (Figure 2-11B).
6. Lower the tractor assembly.
7. Adjust the Multicopy Adjustment Lever to position 5.
8. Open the top pressure plates.
9. Turn the platen knob and feed the paper under the platen. Enough paper should be fed to attach the paper on the top tractors.
10. Position the paper in the top tractors (Figure 2-11C) and close the top pressure plates.
11. Position the form on the upper tractors and flip down the left and right tractor face plates to secure the form.
12. Replace the paper slide to its original position.
13. Adjust the Multicopy Lever to a setting that corresponds to the form just loaded (Figure 2-11D).

14. Press the START button.

Note:

If the paper is not properly positioned, the initial loading under the lower tractors may be difficult. If the form does not catch under the tractor properly, begin form loading again with the paper repositioned under the tractors. It may be necessary to apply some pressure to multipart forms as they have a tendency to separate while being introduced.

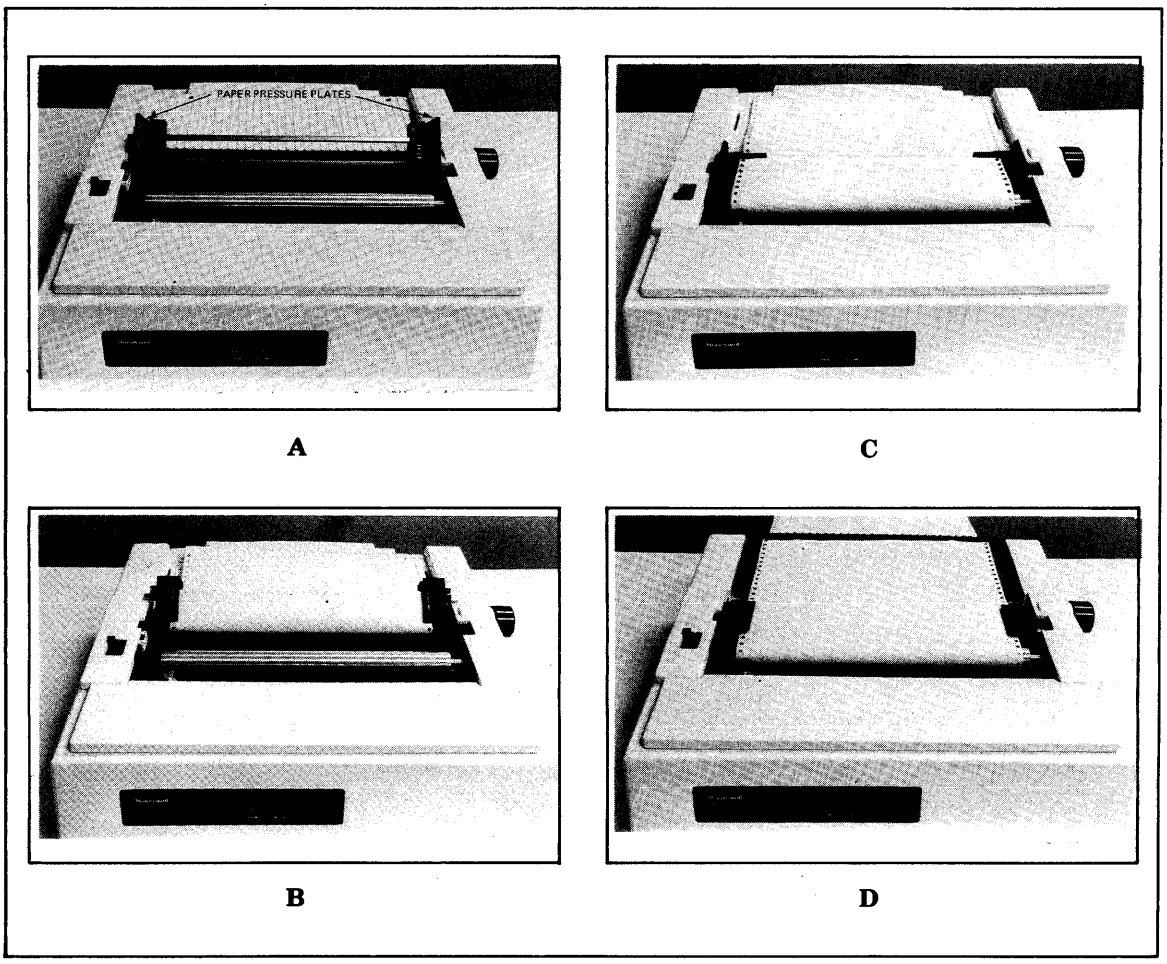


Figure 2-11. Paper Loading

RIBBON CARTRIDGE REPLACEMENT

Ribbons are supplied as operator-replaceable cartridges. The cartridge (M3918—1/4" or M3917—3/8") is positioned on the print mechanism (see Figure 2-12) by the operator, on a reference pin which ensures proper positioning and plastic clips which ensure locking.

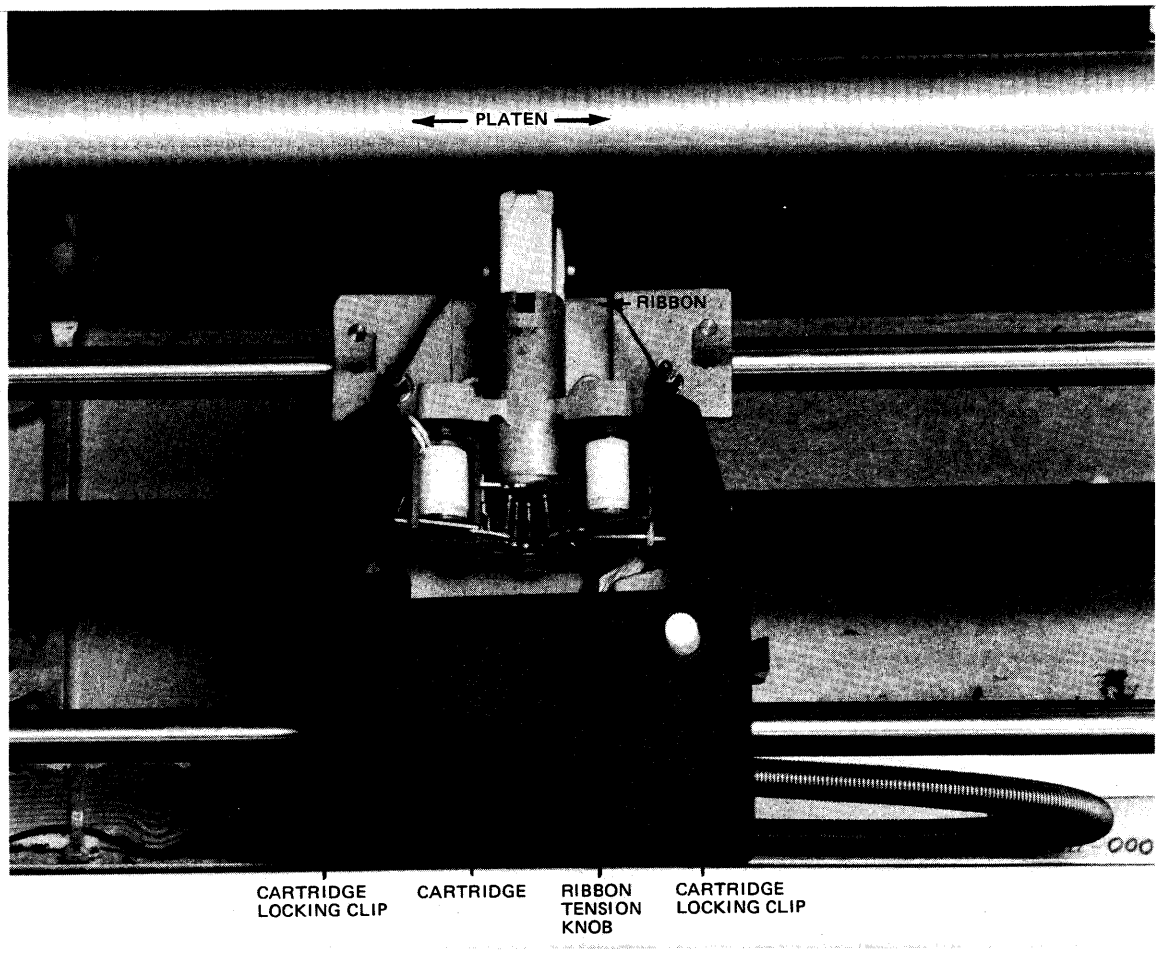


Figure 2-12. Ribbon Cartridge Replacement

The operator replaces the cartridge as necessary to ensure high-quality printing. Cartridge loading includes the following steps:

1. Remove power from the console.
2. Lift off the cover over the print mechanism.
3. Slacken ribbon tension via the ribbon tension knob.
4. Remove worn ribbon cartridge.
5. Slacken ribbon tension on new ribbon cartridge.
6. Position the ribbon between the platen and the print head mechanism.
7. Gently draw the cartridge away from the print mechanism.
8. Carefully position the cartridge on the reference pin and plastic locking clips.
9. Adjust ribbon tension.
10. Replace cover.
11. Apply power to the console.

PRINT TEST

To check print quality and print the entire character set, do the following:

1. Press the STOP button.
2. Press the LOCAL button.

3. Press the TEST button.
4. Press the START button (printing begins).
5. Press the STOP button to terminate the print test.

OPERATOR MAINTENANCE

Operator maintenance includes such preventive maintenance as normal checking and cleaning performed periodically on a routinely scheduled basis. This maintenance will keep the console in the best operating condition thereby reducing the possibility of downtime.

The following list is a general guide to operator maintenance:

- Always plug the console into a 3-wire grounded outlet.
- Ensure that all covers are closed and secured during operation.
- Never operate the console without paper.
- Avoid leaning on or placing objects on any part of the console.
- Turn power OFF before replacing paper or ribbon cartridge.
- Never put food or beverage on or near the console.
- Keep outside covers clean and free of debris.
- Clean and dust the inside areas of the print mechanism.

DISKETTE UNIT

The single, rackmounted diskette unit is used by the operator solely to load the system offline test and diagnostic (T&D) programs which are recorded on the magnetic oxide coated surface of the Mylar disk (or diskette). The T&D programs for the DATANET are contained on three separate diskettes.

The flexible disk is packaged in an 8-inch-square protective nonremovable jacket. Both diskette and jacket contain a center hole with an access slit that extends from the center to the outer edge. When loaded and operative, the magnetic heads on the diskette unit come into physical contact with the recording surface of the diskette. The jacket becomes immobile and is held stationary while the diskette unit spindle automatically engages the diskette and rotates it at a speed of 360 rpm.

CONTROLS

Diskette unit controls include the following:

POWER ON/OFF	This two-position switch is used to either apply or remove power. In non-tabletop configurations, power is applied from the control panel of the central processor.
Access Cover Button	Pressing this button opens the diskette unit access cover to enable either the insertion or removal of the diskette. The access cover is closed manually.

OPERATION

Operating procedures for the diskette units are described below.

APPLYING POWER

Set POWER switch to ON position.

REMOVING POWER

Set POWER switch to OFF position.

Note:

Remove diskette before powering on/off or its programs may be erased.

DISKETTE UNIT LOADING

Prior to loading, visually check the condition of the flexible disk. It should not be torn, folded, or creased. Do not use a damaged diskette.

1. Remove the diskette from its protective envelope (Figure 2-13).
   Note:
   Diskette remains inside its nonremovable jacket.
2. Press the access cover button on the diskette unit.
3. Carefully insert the diskette squarely and completely into the diskette unit.
4. Close the access cover. (The diskette unit spindle automatically engages the diskette and the device is ready for operation.)

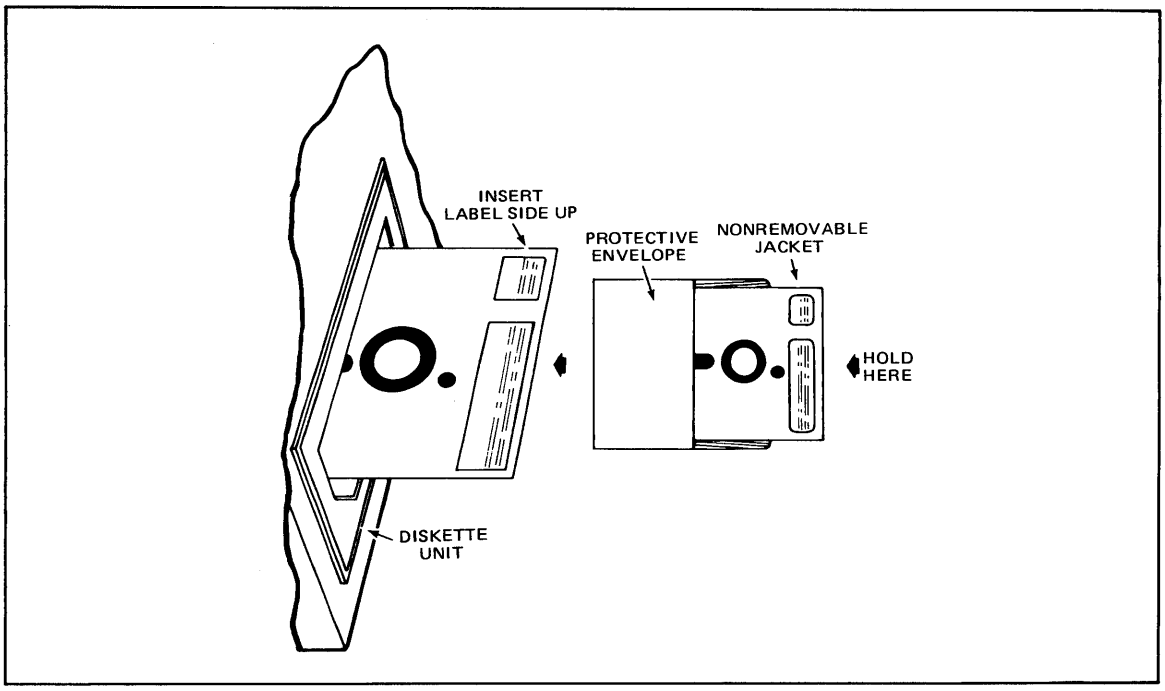


Figure 2-13. Diskette Media Handling

DISKETTE UNIT UNLOADING

1. Press the access cover button on the diskette unit.
2. Grasp the diskette jacket and remove it from the diskette unit.
3. Close the access cover if no other diskette is to be inserted.
4. Return the diskette back into its envelope.

OPERATOR MAINTENANCE

Preventive maintenance includes the checks and cleaning done periodically on a scheduled basis, even though diskette unit operation may be satisfactory and not in need of attention.

CARE AND HANDLING OF DISKETTE

Proper handling and storage of a diskette will increase its life expectancy and reduce the possibility of errors. Observe the following rules for proper media handling and storage.

- Keep the diskette clean. Handle with care since dust and dirt smudges, especially on the recording surfaces, can reduce the intensity and accuracy of reading or recording signals.

- Write on labels *before* adhering them to the nonremovable jacket since writing pressure from a pencil or pen on the jacket may damage the diskette. It is preferable to use felt-tipped pens to minimize contamination.
- Place labels so that they do not obstruct the index sensing hole or adhere the diskette to its jacket.
- It is best not to smoke in the computer room or near the device but, if you must, be extremely careful as smoke and ashes are dirt. Hot ashes are destructive to disks. Food and drink should not be placed on or near the device.
- To reduce the problem of damaged or defective diskettes, never bundle them during storage. Avoid the use of elastic bands or paper clips and store each in its envelope when not in use. Do not stack diskettes on top of other packages.
- Store diskettes in an environment that is the same as the diskette unit operating environment. The recommended environment is from 50°F to 115°F (10°C to 46°C) with a relative humidity of 5% to 90%. Abrupt changes in relative humidity must be avoided.
- Do not expose diskettes to direct sunlight or intense heat.

POWER UP/POWER DOWN/SYSTEM INITIALIZATION PROCEDURES

INITIAL POWER UP PROCEDURE

Note:

Diskette media should not be inserted in unit until after step 5.

1. Open lower front cabinet door.
2. Set Power Distribution Unit ON/OFF switch to the ON position.
3. Close lower front cabinet door.
4. Insert key into panel security keylock switch and turn key to the maximum clockwise position to unlock the control panel.
5. Set control panel POWER switch to the on position (up). DC ON indicator lights. System is now powered up.

Note:

Power up console next.

COMPLETE POWER DOWN PROCEDURE

1. Power down console and diskette (diskette media should be removed first).
2. Set control panel POWER switch to the off (down) position. DC ON indicator turns off.
3. Open lower front cabinet door.
4. Set Power Distribution Unit ON/OFF switch to the OFF position.
5. Close lower front cabinet door. System is now completely powered down.

NORMAL POWER UP PROCEDURE

Note:

Diskette media should not be inserted in unit until after step 2.

1. Insert key into panel security keylock switch and turn key to maximum clockwise position to unlock the control panel.
2. Set control panel POWER switch to the on position (up). DC ON indicator lights. System is now powered up.

Note:

Power up console next.

NORMAL POWER DOWN PROCEDURE

1. Power down console and diskette (diskette media should be removed first).
2. Set control panel POWER switch to the off (down) position. DC ON indicator turns off. System is now powered down.

SYSTEM INITIALIZATION PROCEDURE

1. Be sure STOP/STEP indicator is lit. If it isn't, press the S (Stop/Step) key.
2. Press CLR (Master Clear) key. This initiates running of QLTs (approximately 10-20 seconds).
3. Wait for CHECK indicator to turn off. If it doesn't, refer to "Quality Logic Test" description in Section 3. System is now initialized and ready for operation.

Section 3
Fault Isolation and Diagnostics

This section describes the fault isolation process and the operation of the various test and diagnostics (T&Ds) that an operator must be familiar with. Figure 3-1 shows the proper path to follow.

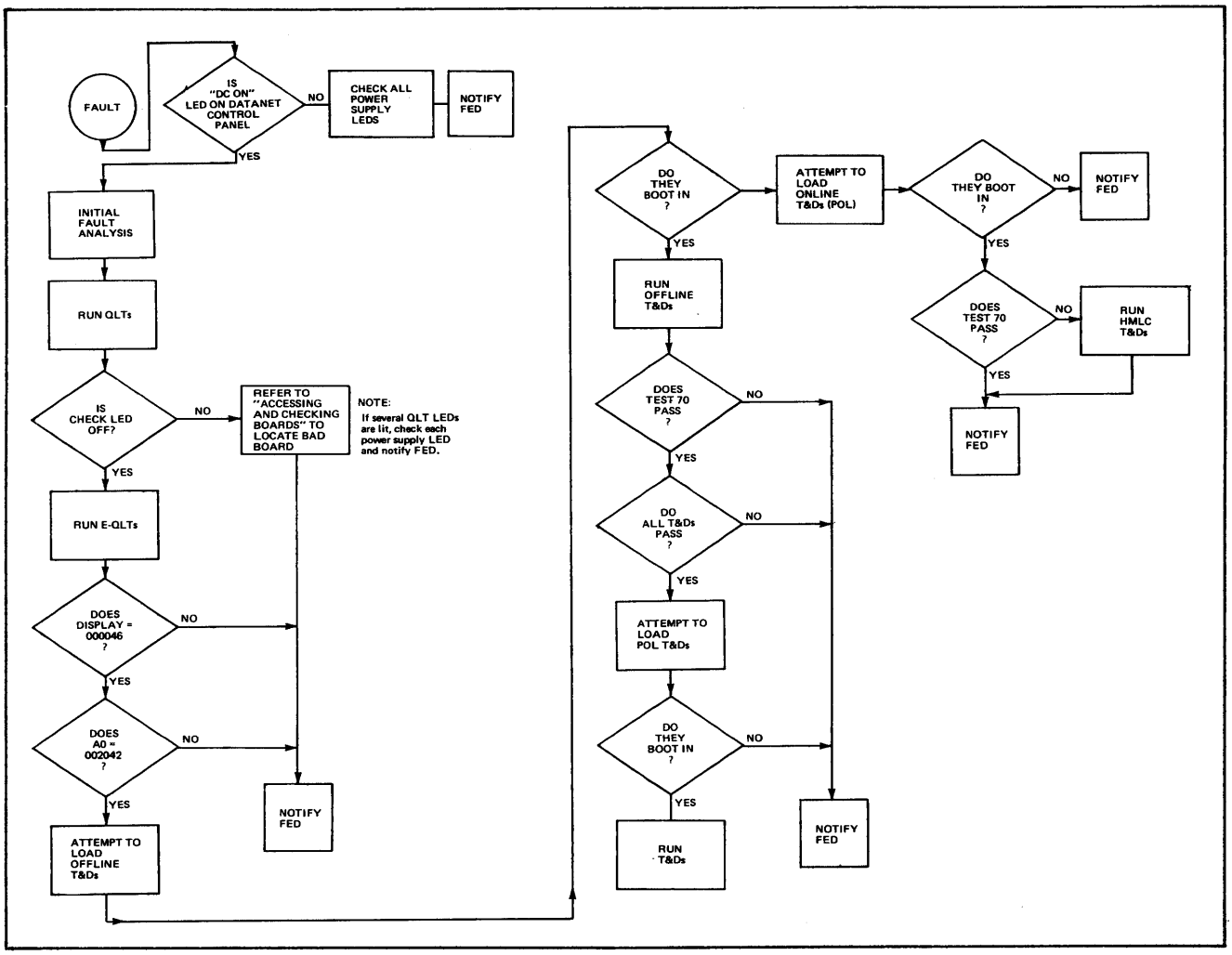


Figure 3-1. Fault Isolation Overview

INITIAL FAULT ANALYSIS

On the occurrence of any failure, the first step is to determine the resultant state of the subsystem via the DATANET operator's control panel.

1. Check whether the DC ON LED is lit. If it is lit, proceed to step 2; otherwise open the rear DATANET cabinet door and check the power supply LED indicators (located in the lower right-hand corner). Note which power supply LED indicators are unlit and notify FED.
2. Check that the control panel is operational by displaying and recording the contents of the following registers:
   - Instruction Counter (A0)
   - Index Register 1 (A1)

- Index Register 2 (A2)
- Index Register 3 (A3)
- A-Register (A4)
- Q-Register (A5)
- Indicator Register (A6)

3. Check that the elapsed timer is running (refer to "Check Timer Operation" in Section 2).
4. Display the level zero interrupt location (000400) from the DATANET control panel and take appropriate action:
   - If the location = 000000, go to step 5.
   - If the location ≠ 000000, display and record the channel fault status words in locations 000420-00437.

     Note:

     Status bit interpretation of the channel fault status words is given in Appendix B.
5. Perform a memory dump and have the results, along with the register information from step 2, analyzed by the appropriate personnel.

   Note:

   If memory parity errors are indicated in the memory dump, the actual memory location of the fault can be determined by selecting register A7 and pressing Read and Execute. The location displayed will be that of the first memory fault encountered and memory location 000000 will be overwritten with the channel fault status word associated with the fault. This test involves memory only, not the pager or cache. If this test does not indicate a memory parity error, then either it is an intermittent error or one caused by the CPU, pager, or cache.
6. Run Quality Logic Tests next.

   Note:

   If at any time the INT LED indicator remains lit after pressing the Execute button, the CP is either in a "hung" or non-interruptible "fault" state. Press the CLR key. Display and record A0 and the type of instruction at and before that location.

QUALITY LOGIC TESTS

After the Initial Fault Analysis, the QLTs must be run. The QLTs are firmware-resident test programs residing on all the boards in the DATANET (except memory and DIA). Although the memory and DIA boards do not have QLT functions, they do accept the QLT signal and pass it onto the bus. QLTs are initiated on each board by the receipt of a Master Clear signal from the bus. The Master Clear signal can be initiated from the DATANET operator's control panel via the CLR (Clear) button, from the Host system via the DIA, or from the Power Valid signal sent by the DATANET power supplies to the operator's control panel.

When initiated, the QLTs light a red LED (light-emitting diode) indicator on the edge of each board and also light the CHECK LED on the operator's control panel. Neither Master Clear nor QLTs affect software or operator-visible registers, other than the interrupt enable register. The Master Clear from the operator's control panel affects every primary board and causes it to start its QLT, turn off its QLT indicator, and pass a "QLT done" signal to the bus. Until a "QLT done" status is achieved by every board on the bus, the CHECK LED on the control panel remains lit and communication between the DATANET and the host will not be allowed.

QLT OPERATING PROCEDURES

QLT operating procedures are as follows:

1. Press CLR (Master Clear) key. The QLT indicators on all applicable boards light and QLTs are running.

   Note:

   A diskette device with its media inserted and the door closed will reset to track zero, which results in a noticeable click that indicates the diskette device is powered up. If the diskette door is open, the SSC QLT light may remain on until the second execution of QLTs.

2. Note that the CHECK LED on the control panel stays lit for the duration of the test (a few seconds).
3. Note that the CP LED extinguishes (if it was lit) and after a few seconds lights and then goes off.
4. Note that the INT LED should not be lit.
5. Note that the register display shows the 18-bit contents of the Instruction Counter (A0); however, the CPU resets the upper three bits of the IC after Master Clear.
6. Refer to the QLT Fault Table (Table 3-1) if the CHECK or CP LED stays lit after a few seconds; otherwise, run the Extended QLTs next.
7. The panel should end up in select, step, and A0.

TABLE 3-1. QLT FAULT TABLE

Control Panel Indication	Explanation and Action
CHECK LED lit	Look for board(s) with QLT indicator(s) and/or error light combinations lit. Refer to "Accessing and Checking Boards." Notify FED of results.
CP LED lit (and control panel unusable)	Memory may have been destroyed and an interrupt may have occurred. Parity error may be pointed to by displaying A0. Attempt to Master Clear again and if unsuccessful, power down and up. Consider memory and CP suspect. Run mainframe and memory T&Ds.

ACCESSING AND CHECKING BOARDS

The operator is required to check and identify malfunctioning boards inside the DATANET Network Processor. The accessing and checking procedures are performed with the power on; therefore, observe the warning note.

WARNING

Do not touch or permit tools to make contact with the logic cards; to do so may cause serious bodily injury. Note also that jewelry, neckties, or other articles of loose clothing should not be worn when performing these procedures.

To open the control panel, proceed as follows:

1. Swing open the top and bottom cabinet doors.
2. Locate the release latch assembly on the right-hand side of the system control panel (see Figure 3-2).
3. Insert≈ 4-mm Allen key (provided) into hexagonal fittings on latch and press inward. The control panel release latch will disengage and the panel will open.
4. Remove Allen key and swing out the control panel from right to left until all of the logic cards are visible.

5. Check the boards in the cabinet for any lit LED indicators. If there are no LED indicators lit, proceed to step 6; otherwise refer to Figures 3-3 and 3-4, and Tables 3-2, 3-3, or 3-4 as appropriate. Notify FED which board is defective.

Note:

If several LED indicators are lit, check each power supply LED. Notify FED if any are not lit.

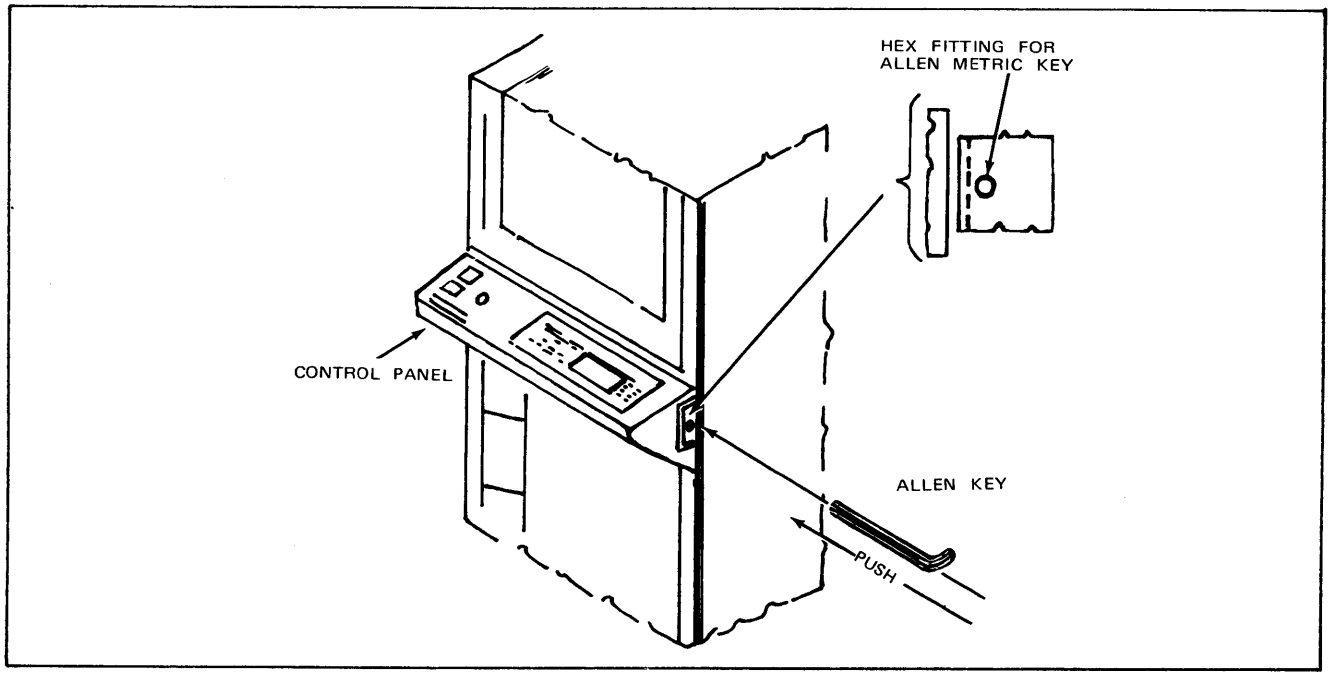


Figure 3-2. Opening Control Panel

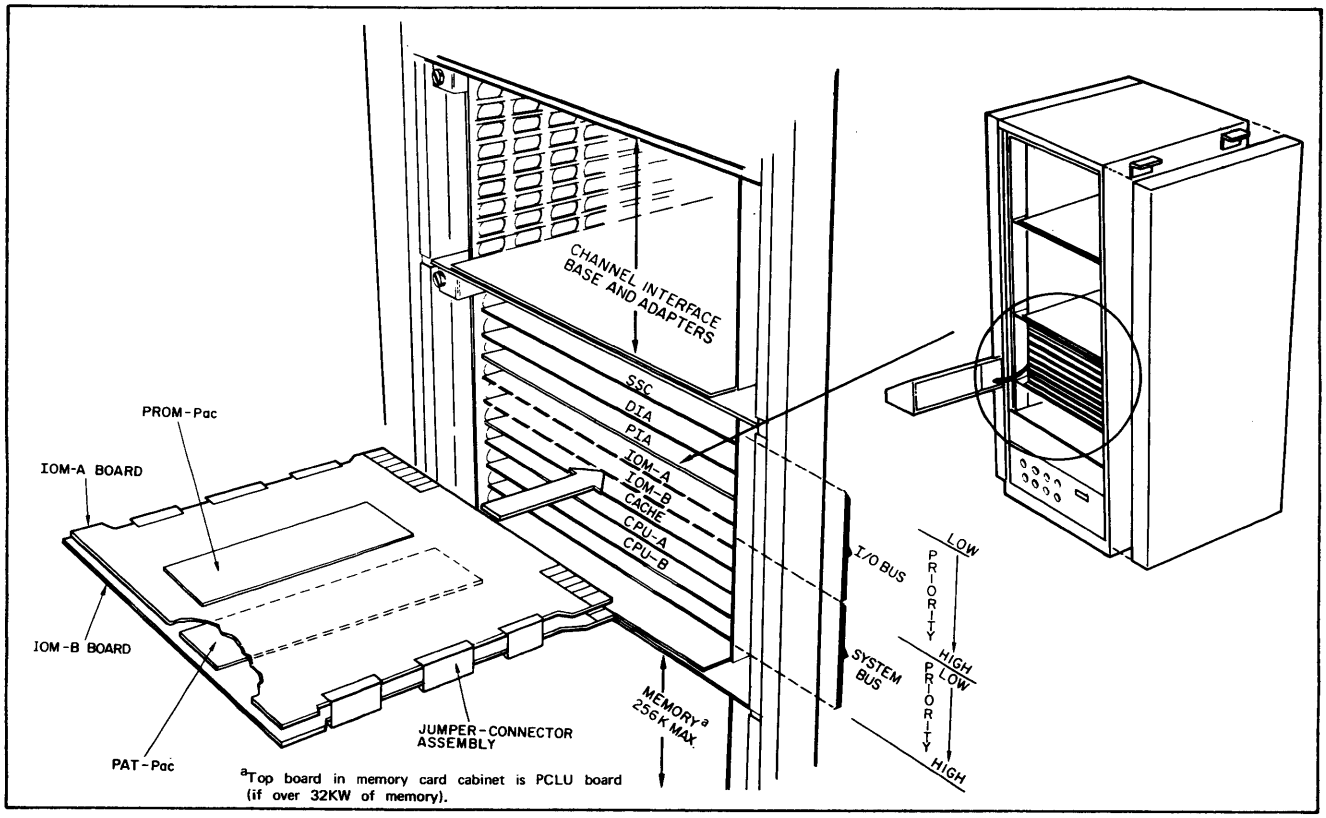


Figure 3-3. Board Locations

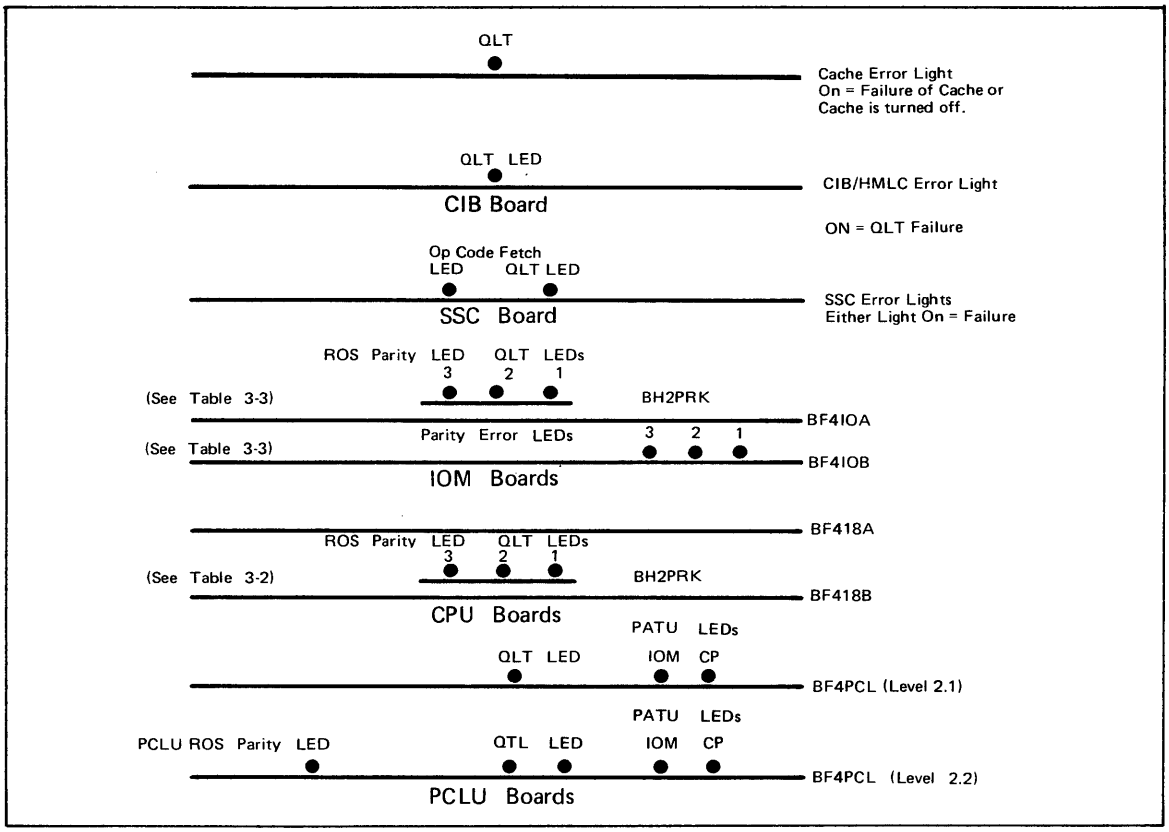


Figure 3-4. QLT and Error LED Locations

TABLE 3-2. CP ERROR LIGHT COMBINATIONS

	Definitions	Error Lights 3	2	1
BF418B Board	QLT Successful	OFF	OFF	OFF
	ROS Parity (PROM board BH2PRK defective)	ON	*	*
	BF418A Board Defective	OFF	OFF	ON
	BF418B Board Defective	OFF	ON	OFF
	CP or Control Panel Failure (cannot determine defective board)	OFF	ON	ON

*Indication irrelevant

TABLE 3-3. IOM ERROR LIGHT COMBINATIONS

	Definitions	Error Lights 3	2	1
BF4IOA Board	QLT Successful	OFF	OFF	OFF
	ROS Parity (PROM board BH2PRK defective)	ON	*	*
	BF4IOA Board Defective	OFF	OFF	ON
	BF4IOB Board Defective	OFF	ON	OFF
	IOM Failure (cannot determine defective board)	OFF	ON	ON
BF4IOB Board	Address Parity on I/O Bus	*	*	ON
	Data Parity Byte 0 on I/O Bus	*	ON	*
	Data Parity Byte 1 on I/O Bus	ON	*	*

*Indication irrelevant

Note:

IOB board LEDs indicate parity errors on memory writes from I/O bus units.

TABLE 3-4. PCLU ERROR LIGHT COMBINATIONS

	Error Lights			
	ROS		PATU	
Definitions	Parity	QLT	CP	IOM
No Errors	OFF	OFF	OFF	OFF
PATU CP board failed	OFF	OFF	ON	OFF
PATU IOM board failed	OFF	OFF	OFF	ON
PCLU failed	OFF	OFF	ON	ON
PCLU QLT test failed	OFF	ON	OFF	OFF
PATU failed QLT test	OFF	ON	ON	OFF
PATU failed QLT test	OFF	ON	OFF	ON
PCLU failed QLT test	OFF	ON	ON	ON
PCLU ROS Parity	ON	*	*	*

*Indication irrelevant

Note:

PATU QLT failures can cause corresponding unit (CP or IOM) to fail QLTs.

6. Check for an empty bus slot between the low and high terminator boards. Notify FED if you find an empty slot; otherwise go to step 7.
7. Check for a QLT LED indicator by performing the following:
   a. Press the CLR button.
   b. Observe that the two QLT LEDs on the CPU board light for approximately 7 seconds.
   c. Observe that the two QLT LEDs on the IOM board light for approximately 1.5 seconds.
   d. Observe that all other QLT LEDs blink.
   e. Notify FED which board does not follow the above sequence.
8. To close system control panel, swing panel from left to right until release latch engages.

EXTENDED QLTS

The Extended QLTs (E-QLTs) are capable of detecting a high percentage of those failures which cannot be caught by the QLTs (bus- or dialog-oriented logic), but which might preclude bootloading. The principal units involved are: memory (1st 16K words), CP, IOM, and SSC (wrap-around channel) and I/O channels.

Note:

The E-QLTs will destroy memory and register contents. The E-QLTs diagnose failures in the various system components by performing the following tests in the order listed:

- Tests CP internal logic
- Tests the 1st 16K words of memory using the CP
- Tests the 1st 16K words of memory using the IOM
- Tests the CP — IOM interaction
- Tests the I/O bus
- Tests the I/O units' bus response logic [1]
- Writes a print buffer containing the channel number of each unit on the I/O bus in order of priority [1]
- Writes a software program in memory
- Executes the program in three parts:
  — CP internal
  — Outputs print buffer on DATANET console [1]
  — I/O and data wrap-around test with CP/IOM/SSC

[1]Test omitted unless CPU PRK board at Rev. BPRK003A-002 (for DN6058s only) or BPRK001A-004 (for all others) and IOM PRK board at Rev. BPRK002A-004.

OPERATING PROCEDURES

The E-QLTs are initiated from the DATANET operator's control panel as follows:

1. Press Select.
2. Key in, D2.
3. Press Write.
4. Press Execute.
5. Wait approximately 20 seconds for message to be printed out on the DATANET console. The message contains one entry for each unit on the I/O bus. These entries should be the channel numbers of each of the units on the I/O bus in order. Communications units, printed with subchannel and major channel number, are four digits long. Non-communications units are printed as a two-digit channel number.

   Example:

HMLC/CIB Number			Channel Number
00	06		(channel 6, subchannels 0-7) = HMLC 0
01	06		(channel 6, subchannels 8-15) = HMLC 1
02	06		(channel 6, subchannels 16-23) = HMLC 2
03	06		(channel 6, subchannels 24-32) = HMLC 3
00	07	Follows same format as channel #6	(channel 7, subchannels 0-7) = HMLC 0
03	10		(channel 10, subchannels 24-32) = HMLC 3
	00		(console (SSC)
	01		(PIA on channel 5)
	03		(unit on channel 3)
	04		(DIA on channel 4)

   Space between HMLC/CIB Number is shown for clarity only. Actual printout has no space.

   Note:

   PIAs return only the two low-order bits of their channel number.

6. Check printout against actual configuration.
7. Wait for CP LED indicator to go off (approximately 15 seconds later), then check control panel display and take appropriate action:

   If display=000046, display register A0 and take appropriate action:
   — If A0 = 002042, the E-QLTs ran successfully. Run mainframe T&Ds next.
   — If A0 ≠ 002042, proceed to step 8.
8. Record display value for interpretation by FED.
9. Display and record the values of the following registers for FED: A0, A1, A2, A3, A4, and A5.
10. Notify the FED Response Center.

T&D GUIDELINES

Figure 3-5 provides an overview of the various T&Ds and their loading points.

- COLTS — Use for minor malfunctions when the problem is suspected to be with a subchannel or remote device. COLTS runs completely online.
- POL — Use for minor or major malfunctions when the problem is suspected to be with a subchannel, DATANET mainframe, or memory. If POL loads and runs successfully, the DIA is all right. If POL cannot be loaded, run the offline T&D programs. If the DIA is suspected, run the offline T&D programs DA and DI, or it may also be tested when the Host is offline and under control of the Monitor by running the ON2 program.

- Offline — Use for minor or major malfunctions when the problem is suspected to be with the DIA, mainframe, or subchannels.

  Note:

  The T&D Program listings (on microfiche) contain detailed descriptions for each test. Refer to these listings for further test functions, methods of testing, and restrictions.

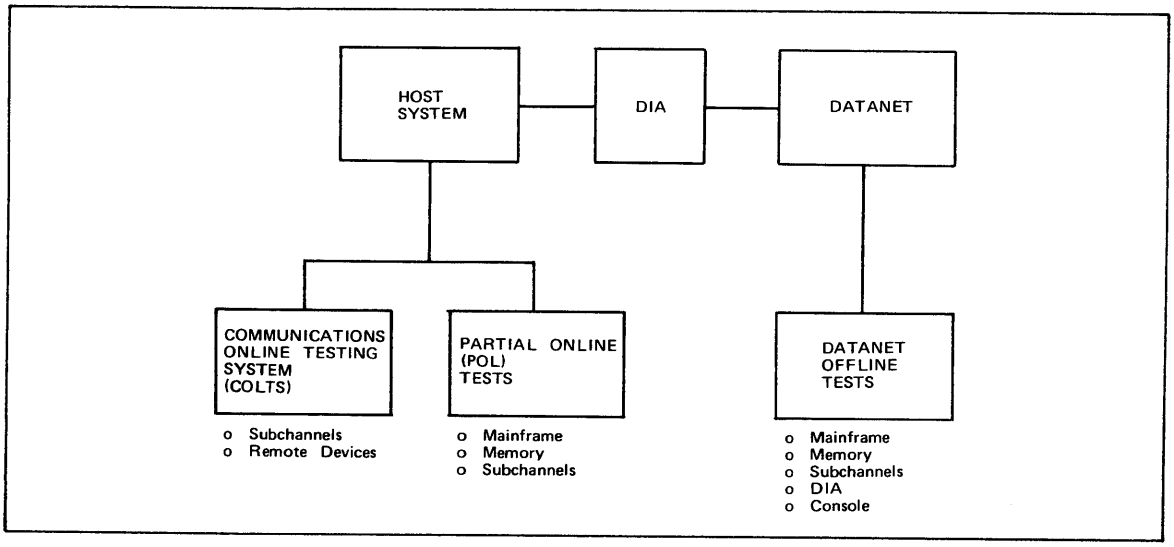


Figure 3-5. T&D Overview

DATANET OFFLINE TESTS

These tests include mainframe, memory, and I/O routines that should be run first in order to verify memory, IOM, and CP basic integrity. The basic bootload path (diskette-SSC-IOM-memory) can be considered verified by the first few diskette records if a console printout occurs (see Figure 3-5). If all of the mainframe tests run without error, the next step is to run the memory test. Up to this point, the tests were concerned with only the first 16K words of memory.

Following the successful completion of the mainframe and memory tests, the cache and pager tests should be run if these units are present on the system. Following these tests, run the I/O tests.

The offline T&Ds are currently distributed on three diskettes. For T&D release A.4, they are as follows:

Part Number	Title	T&Ds
58011799-031	Mainframe (PAS)	25-80
58011799-032	I/O #1	CO, DA, DI, H1-H9, HA, HB
58011799-034	I/O #2	EA, KD, M2, MI
58011799-036	Memory #2	86

A complete list of all offline T&Ds is provided on the first microfiche card of the T&D microfiche package. This list also identifies which diskette the T&D is located on. A detailed description of the various T&Ds is provided by Table 3-5.

The number of the subtest being executed for each T&D is stored in location 20003_8 for BOS T&Ds and in 27003_8 for IOS T&Ds.

As additional programs are released or existing programs are improved, they will be distributed. Your Honeywell FED representative should complete the form provided in Appendix A.

TABLE 3-5. DATANET OFFLINE TEST & DIAGNOSTIC PROGRAMS

T&D Diskette	Program Name	Call	Run Time	Figure Number	Description
	Character Addressing	25	1.0 s	3-6	Tests all types of addressing not covered by the Primitive Function program. Includes character addressing and indirect strings. The functions tested are IACXN and ADCXN.
	Data Movement & Fixed Address — P1	30	1.0 s	3-6	Tests logic related to the following instructions: CX1A, CX2A, CX3A, CAX1, CAX2, CAX3, LDQ, STQ, ADQ, SBQ, CQA, CAQ, STZ, ORA, ERA, LDAQ, STAQ, ADAQ, SBAQ, IERA, ILQ, IAQ, INA, IORA.
	Data Movement & Fixed Address — P2	31	1.0 s	3-6	Tests logic related to the ADQ instruction.
	Data Movement & Fixed Address — P3	32	1.0 s	3-6	Tests logic related to the ADAQ instruction.
	Fixed Address To Store	35	30 ms	3-6	Tests logic related to the following instructions: AOS, SSA, ANSA, ORSA, ERSA
	Compare	40	30 ms	3-6	Tests logic related to the SZN instruction.
	Shift	45	50 ms	3-6	Tests logic related to the shift and normalize instructions.
	Multiply & Divide	50	10.0 s	3-6	Tests logic related to the multiply and divide fraction functions.
PAS[a]	System Controller — P2	56	0.5 s	3-6	Tests the following hardware: inhibit indicator logic in processor, interrupt vector address generator, interrupt cell rewrite generator.
	System Controller — P3	57	0.5 s	3-6	Tests the following hardware: interrupt cell zero detector, interrupt inhibit, interrupt cell priority generator, request interrupt.
	Illegal Operations	60	1.0 s	3-6	Tests the ability of the DATANET processor to reject undefined operation codes.
	Register Interaction	65	1.0 min	3-6	Verifies that certain register-oriented instructions affect only applicable registers. Hardware functions: decode of instructions, data bus to and from store, register strobes, A, Q, S and index registers.

TABLE 3-5 (CONT). DATANET OFFLINE TEST & DIAGNOSTIC PROGRAMS

T&D Diskette	Program Name	Call	Run Time	Figure Number	Description
	Input/Output Multiplexer	70	25 s	3-6	Tests the functional performance of the IOM in a direct and indirect mode. In addition, exercises the instructions SEL, LDEX, and STEX along with the wraparound channel.
	IOM Timer	71	10 ms	3-6	Tests the functional performance of the IOM elapsed and interval timers.
	Instruction Sequence	75	Until Operator Interrupts	3-6	Tests execution of random sequences of instructions using random data.
	Cache	80	—	3-6	Tests the functional performance of the cache/CP to memory.
MEM-2	MOS memory	86	5.0 min	3-7	Tests all of the memory above 8K (A.3 Release)
	Console	CO	Variable	3-8	Tests the transfer of data and control signals between the I/O bus and the console.
	Direct Interface Adapter — P1	DA	3.0 min	3-9	Tests DIA wraparound functionality without being connected to the host IOM.
	Direct Interface Adapter — P2	DI	15 s	3-9	Tests the DIA using the host IOM in the T&D mode. Data is transferred between the DATANET and the host IOM.
	HMLC Central Logic — P1	H1	10.0 s	3-10 3-11	Tests part of the functions of the HMLC central logic using all available subchannels except HDLC and BSC.
	HMLC Central Logic — P2	H2	1.5 to 6 min. for an HMLC with 8 synchronous channels	3-10	Tests the rest of the functions of the HMLC central logic using all subchannels except HDLC and BSC.
	HMLC Subchannels	H3	15 s per line adapter	3-10	All subchannels in the internal wraparound mode except HDLC & BSC.
I/O #1	HMLC Manual Wraparound	H4	15 s per line adapter	3-10	Tests individual subchannels in the external wraparound mode except HDLC and BSC. Requires an external wraparound plug.
	HMLC P1 & P2 with BSC	HA and HB		3-12	Tests HMLC central logic using BSC subchannels.
	HMLC w/BSC Subchannels	H5 and H6	15 s per line adapter	3-12	Tests BSC subchannels in the internal wraparound mode.

TABLE 3-5 (CONT). DATANET OFFLINE TEST & DIAGNOSTIC PROGRAMS

T&D Diskette	Program Name	Call	Run Time	Figure Number	Description
	HMLC w/HDLC	H7 and H8	15 s per line adapter	3-13	Tests HDLC subchannels on the internal wraparound mode.
	HMLC w/HDLC Subchannels	H9	15 s per line adapter	3-13	Tests individual HDLC subchannels in the external wraparound mode. Requires an external wraparound plug.
I/O #2	Pager-Extended Address	EA	—	3-13	Tests the paging mechanism using extended memory (over 32K words). Note: This is not a memory test.
	Diskette Device Test	KD	Variable	3-15	Tests the ability of the diskette and adapter to seek and read any and all tracks on disk.
	Peripheral Interface Adapter (PIA)	M2	30 s	3-16	Tests the PIA channel and the interface with the MPC. Includes the functionality of M1. Option: Test 8 interfaces to the disk. It writes, reads, and compares data. The device must be unused. Channels 3 and 5 are the only valid channels for T&D (A.2).
Multi I/O		MI	Indefinite	3-17	Tests the loading of the I/O T&Ds to execute at the same time. Operating instructions are contained in the M1 listing.

[a]PAS T&Ds will sequence 25-75 by typing a carriage return or "SEQ". Cache T&Ds (80) must be called in separately, e.g., "PRG 80".

LOADING PROCEDURES

This procedure is performed from the diskette unit of the DATANET system.

1. Open lower front cabinet door.
2. Set diskette POWER switch to the ON position.
3. Press the access cover button.
4. Insert the T&D diskette.
5. Close the access cover.
6. Press CLR (Master Clear). This initiates the QLTs (approximately 10 seconds).
7. Wait for CHECK indicator to turn off. If it doesn't, refer to the "Accessing and Checking Boards" procedure.
8. Check that the console is powered up, online, and ready for operation.
9. Press Select.
10. Key in, via the octal/hex pad keys, B0.

11. Press Execute. This will cause the following to happen:

```
Clear first 600₈ memory locations.
Load the following Control Words:
464 = 101000 }
465 = 010001 }   STATUS ICW
466 = 400000 }
467 = 000000 }   DATA ICW
Issue CIOC (Connect) under F/W control to Channel # 1-
  Diskette
PCW data = 000001 (Odd Word)  for READ
Channel No. = 01
```

MEMORY MAP OF BOOTLOAD:

LOCATION	CONTENTS								
00000	00000	000002	000000	000000	000000	000000	000000	000000	000000
00010	00010	000000	000000	000000	000000	000000	000000	000000	000000
00400*	00400	000000	000000	000003	000000	000000	000000	000000	000000
00410	00410	000000	000000	000000	000000	000000	000000	000000	000000
00450*	00450	000000	026252	000000	000000	000000	000000	000000	000000
00460	00460	000000	000000	000000	000000	101000	010001	400000	000000
00470	00470	000000	000000	000000	000000	000000	000000	000000	000000
00600*	00600	252525	252525	252525	252525	252525	252525	252525	252525
00630*	00630	252525	252525	252525	252525	000612	252525	252525	252525
00640	00640	252525	252525	252525	252525	252525	252525	252525	252525
40000*	40000	000000	000000	000000	000000	000000	000000	000000	000000
		ELAPSED TIMER VALUE		CONTROL PANEL DATA (AOR)		STATUS ICW		DATA ICW	

After the read command is issued (CIOC), the diskette head will step-out until track 00 is detected and then go to track 01. Track 00 has title and ownership information. The bootload program will start at Track 01, sector 0 and read four sectors. At this point, the channel unloads the read head and stores status with bit 2 on and interrupts (terminates — cell 1, Level 2). The program already read in will execute the remaining bootload read until a TRO occurs, indicating ICW exhaust. Loading of the bootload will be complete at this point.

Primitive Function Tests (PFTs) will be read and executed, and the Executive will be read and a console message typed on the console. If the diskette does not halt, or no console message is printed, carefully repeat the above steps. If unsuccessful again, run E-QLTs.

OPERATING PROCEDURES

The operating procedures for the various T&Ds are illustrated in Figures 3-6 through 3-17, which are sample T&D console printouts. Operator key-ins are underscored where necessary. The operator will note that the T&Ds are not only very simple to run, but take just a few minutes at most. Figure 3-18 shows the DN66 T&D Memory Map. Table 3-6 explains DN66 configuration.

Notes:

1. When finished running the T&Ds, remove the diskette media and power down the diskette unit.
2. If the program selected is not present on the diskette, the following console message will print out: PRG NOT ON DISK __ __ WRNG CRD FORMAT (CR).
3. These are sample T&D console printouts. The actual console printout may change depending upon the T&D revision and sequence of events. However, these sample printouts should allow the operator to determine if the T&D executed correctly or if it had an error.

```
* DATANET BOS  REV. B 121479
"WARNING" USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE?CENTER Y OR N
BOS OPT      (CR)  <-------------- DEPRESS CARRIAGE RETURN (CR)
25H REV. 00A  CHAR & IND. ADDR.      ON TYPE IN SEQ, THEN (CR).
30H REV. 00A  DATA MOV&FIXED ADD
31H REV. 00A  DATA MOV&FIXED ADD
32H REV. 00A  DATA MOV&FIXED ADD
35H REV. 00A  FIXED ADD TO STORE
40H REV. 00A      COMPARISON
45H REV. 00A  HNP SHIFT TESTS
50H REV. 00A  MULTIPLY & DIVIDE
55H REV. 00B  HNP IOM INTR PART1
MAXIMUM USEABLE CORE IS 32K FOR THIS TEST.
56H REV. 00A  HNP IOM INTR PART2
57H REV. 00A  HNP IOM INTR PART3
60H REV. 00A   ILLEGAL OP TEST
65H REV. 00A  HNP REGISTER INTER
70H REV. 00B  DN-6670 IOM TEST          -> AFTER APPROXIMATELY 4 MINUTES
71H REV. 00A  HNP IOM TIMER TEST           DEPRESS THE BREAK BUTTON
75H REV. 00A   INST. SEQ. PROG. ---------
BOS OPT  PRG80 ------------------------> FOR CACHE T&D IF CACHE IS INSTALLED
BOS OPT  (CR)
80H REV. 00C  HNP CACHE MEMORY

MAXIMUM AVAILABLE CORE IS   177777

DOUBLE WORD PULL INDICATED-NONENTERLEAVE.

TEST INDICATES CACHE CONFIGURED WITH 4K CACHE ARRAY.
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
BOS OPT
```

All BOS T&Ds have now been executed.

Note:

Program 75 will run until interrupted by an error or by manually depressing the break key on the console. To check that program 75 is executing, display memory location $20776_{(8)}$; it should be continually incrementing.

Figure 3-6. BOS Console Typeout Including Cache PRG 80

```
86  REV. 00C  HNP MOS MEMORY
MAXIMUM AVAILABLE MEMORY IS   177777
MOS OPTS?
NORMAL TESTING-Y OR N??Y
  TESTING 020000 THRU 037777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 040000 THRU 057777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 060000 THRU 077777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 100000 THRU 117777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 120000 THRU 137777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 140000 THRU 157777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
  TESTING 160000 THRU 177777.
ADDRESSING SINGLE
6-BIT CHARA.ADDR.
9-BIT CHARA.ADDR.
DATA INTEGRITY
WRITE DISTURB
 ** NO CORRECTIBLE ERRORS DETECTED
END OF PROGRAM.
MOS OPTS?
```

Note:

32K-memory takes about 3.5 minutes.
64K-memory takes about 7.5 minutes

Figure 3-7. Memory T&D 86 Testing 64K Memory

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? CENTER Y OR N]
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY-
IOS OPT
 CONAD REV.   B  CONSOLE ADAPTER
END TEST 01A
0000000000000000000000000000000000000000
0000000000000000000000000000000000000000
0000000000000000000000000000000000000000
0000000000000000000000000000000000000000
0000000000000000000000000000000000000000
END TEST 03A
MM
MMMMMM
MMMMMMMMMM
MMMMMMMMMMMMMM
MMMMMMMMMMMMMMMMMM
MMMMMMMMMMMMMMM
MMMMMMMMMM
MMMMMM
MM

END TEST 03B
1
END TEST 04A
abcdefghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.
bcdefghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.1
cdefghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.12
defghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.123
efghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.1234
fghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.12345
ghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.123456
hijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.123456M
ijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.123456MM
jklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.123456MMM
END TEST 04B

START TYPING IN NON-CONTROL CHARS;
   THIS TEST SHOULD TERMINATE ITSELF AFTER TWO CHARS -
 TT
END TEST 05A

PLEASE TYPE IN UP TO 72 PRINTABLE CHARACTERS, FOLLOWED
BY A CARRIAGE RTN; THE CHARACTERS WILL BE CHECKED AND
OUTPUT ON THE LINE FOLLOWING.
TTTTYYY77788MMMMM,,,
TTTTYYY77788MMMMM,,,
END TEST 05B

PLEASE WAIT 30 SECONDS FOR TIMER RUN-OUT TEST

END OF TIMER RUN-OUT TEST
END TEST 06A

PLEASE DEPRESS THE "LINE BREAK" KEY
(DEPRESS "LINE BREAK" KEY)
AGAIN, PLEASE...WHILE CONSOLE IS TYPING NEXT 2 LINES
abcdefghijklmnopqrstuvwxyz 0123456789 <>()[] / ~_#`&$ *%+-="'       ;,.
abcd
(AGAIN DEPRESS LINE BREAK KEY)
END OF TEST; THANK YOU
END TEST 06B

TYPE A CARRIAGE RETURN   (CR)

TYPE A CONTROL-X  (DEPRESS CONTROL AND X)
END TEST 07
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

Type any characters.

Figure 3-8. Console Typeout for Console T&D CO

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N] N
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY- D
IOS OPT DGDA
DA      REV. B     DIA PT-1 [W/O 645]

ENTER 355 TEST CHAN [2 OCT DIGITS]   04
COM REGION ADDRESS-  00454

     * NOTE-BITS 00-17 OF THE PCW WILL CONTAIN *
     * THE CURRENT DATA OF THE TEST IN EACH OF *
     * THE ERROR MESSAGES IN TESTS 01 THRU 09. *

CONFIGURATION DATA WILL BE GATED DIRECTLY INTO THE
HNP CORE.  THIS DATA WILL BE USED AS TEST DATA FOR
TEST 02A.

 CONFIGURATION     >>>>>>6000/645<<<<<<<
   RAW DATA        MB ADDR. TERM. EMERG.

 003100000077       003100   007    007

HNP "SPECIAL" INTERRUPT WORD IS = 400003.

THE CHANNEL NUMBER AND TERMINATE LEVEL WORD IS = 001002.
   BITS 6,7,8,10,11 = CHANNEL NUMBER
   BITS 15-17 = TERMINATE LEVEL

6000 MB ADDR./INTERRUPT WORD IS = 003177.


ASSIGNED DIA CHANNEL NUMBER  04

       <<<<<< INTERRUPTS >>>>>>     MAILBOX
        TERM.    EMERG.    SPEC.     ADDRESS

645       7         7       NONE      003100

HNP      02       NONE       03       454

  ** PROGRAM WILL NOW GO INTO NORMAL  **
  ** FUNCTIONAL TEST MODE-"HNP" ONLY  **
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT DGDI
DI      REV. A     DIA PT-2[WITH 645]


** INITIALIZE THE 6000 **
** IOM BEFORE STARTING **
** DIA TESTING.        **


ENTER 355 TEST CHAN [2 OCT DIGITS]   04
COM REGION ADDRESS-  00454
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

Variable depending upon site configuration

Figure 3-9. Console Typeout for DIA T&D, DA and DI

```
* DATANET IOS REV B RELS    A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N]
ENTER SUBSYSTEM TYPE:
C=COMMUNICATIONS,D=DOC. ENTRY-
IOS OPT
   H1H REV. D    HMLC CENTRAL PART1

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]

RUN COMPLETED
SHOULD I DUMP ACTIVE CHANNEL TABLE [Y OR N]
LOAD HMLC CENTRAL TEST PART 2
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
   H2H REV. C    HMLC CENTRAL PART2

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]
LOAD HMLC SUBC TST
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
   H3H REV. D    HMLC INT SUBC WRAP
EUROPEAN BAUD RATES [ Y OR N ]

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
   H4H REV. C    HMLC EXT SUBC WRAP

INSTALL SUBCHANNEL WRAPAROUND CONNECTOR
                                          DEPRESS CARRIAGE RETURN (CR)
                                          AFTER INSTALL
                                          WRAPAROUND CONNECTOR.
ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]  00
ENTER SUBCHANNEL NUMBER,[TWO DECIMAL DIGITS]
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

See Figure 3-11 for example of Y response.

Can also type Y; print out will not change.

Notes:

1. H-4 for ASYNC S/Cs require that the direct connect clock switch be turned off.
2. H-4 will test BSC S/Cs but not using BSC-protocol.
3. H-3 and H-4 require the direct connect baud rate switch to be set to 9600 baud, position 6.

Figure 3-10. Console Typeout for EIA-HMLC T&Ds H1-H4

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N]
ENTER SUBSYSTEM TYPE:
C=COMMUNICATIONS,D=DOC. ENTRY-
IOS OPT
   H1H REV. D     HMLC CENTRAL PART1

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]

RUN COMPLETED
SHOULD I DUMP ACTIVE CHANNEL TABLE [Y OR N]  Y
37440                          053000 053000 043000 043000 053000
37450  053000 777777 777777 000000 000000 000000 000000 000000
      LOCATIONS 37460 THROUGH 37477 ALL CONTAIN 000000
37500  000000 000000 000000

LOAD HMLC CENTRAL TEST PART 2
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

Notes:

1. Bits 2-8 = subchannel ID code (see chart.)
2. Bits 0-17 = all ones for non-existent sub-channels
3. First word is for S/C #0
4. Second word is for S/C #1 etc.

Figure 3-11. Console Typeout for T&D H1 with Active Channel Table Printed Out

TABLE 3-6. DN66 CONFIGURATION CHART

IPI No.	Board Type	Board Size	ID Code	No. of CHs	Async Sync	Baud Rate	Comments
BMLFCLAA	BD2CLA	1/4	42	2	A	9600	20/60 MA
BMLF103A	BD2LAS	1/4	53	2	S	9600	EIA
BMLF101B	BD2ASC	1/4	43	2	A	9600	EIA
BMLFDACA	BD2DAC	1/4	64	2	—	10	ACU
BMLF188A	BD2188	1/4	54	1	S	9600	MIL188
BMLFA88A	BD2A88	1/4	40	2	A	9600	MIL188
BMLF616A	BD2B8D	1/4	51	1	S	72000	MIL188BB
BMLFH88A	BD2H88	1/4	—	1	S	9600	MIL188 HDLC
BMLF103A	BD2LAS	Replaced by BMLF618A					
BMLF618A	BD2LAS	1/4	52	2	S	9600	BSC
BMLF619A	BD2CMD	1/4	47/46	1	S	72000	Current Mode/BSC
BMLFCMSA	BD2CMS	Replaced by BMLF619A					
BMLFDLCA	BD2DLC	1/4	50	1	S	9600	EIA, HDLC
BMLFDLDA	BH4DLD	1/2	146	1	S	72000	EIA, HDLC, BB
BMLFDLEA	BH4DLE	1/2	147	1	S	72000	CCITT-V.35, HDLC
BMLFBLSA	BD2BLS	Replaced by BMLF627A					
BMLF627A	BD2BLD	1/4	55	2	S	9600	CCITT-V.35, B.B.

**The ID code is stored in configuration status bits 2-8. If subchannel is attached to an ACU, an octal 20 is added to the ID code.

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N]
ENTER SUBSYSTEM TYPE:
C=COMMUNICATIONS,D=DOC. ENTRY-
IOS OPT
    HA REV. A     HMLC BSC CENTRAL 1

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3[2 DIGITS]
LOAD BSC CENTRAL TEST PART 2
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
    HB REV. A     HSLA BSC CENTRAL 2

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3[2 DIGITS]
LOAD BI-SYNC SUBCHAN TEST
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
 H5H    REV. D     BSC P1 FOR 6670

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]
END PART 1; TO CONTINUE TEST, LOAD
BSC PART 2
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
 H6H    REV. D     BSC P2 FOR 6670

ENTER 355 TEST CHAN [2 OCT DIGITS]

ENTER HMLC NO. 0-3 [2 DIGITS]
END PART 2
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

Note:
Can run H4, manual wrap test, on BSC boards — use the same wrap plug.

Figure 3-12. Console Typeout for BSC-HMLC T&Ds HA, HB, H5, H6

```
* DATANET IOS REV B RELS    A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N] N
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY- C
IOS OPT [illegible]
H7H    REV. D    H7H-HMLC/HDLC PT-1

ENTER 355 TEST CHAN [2 OCT DIGITS]  07

ENTER HMLC NO. 0-3 [2 DIGITS]  02
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT [illegible]
H8H    REV. B    H8H-HDLC PT-2

ENTER 355 TEST CHAN [2 OCT DIGITS]  07

ENTER HMLC NO. 0-3 [2 DIGITS]  02
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT [illegible]
H9     REV. C    H9-HMLC/HDLC PT-3

ENTER 355 TEST CHAN [2 OCT DIGITS]  07

ENTER HMLC NO. 0-3 [2 DIGITS]  02

CALL THE FOLLOWING VIA THE "TEST XX"
OPTION ONLY-
 TEST 07 - "DO-IT-YOURSELF" TEST ROUTINE
 TEST 08 - "CRC" CALCULATION ROUTINE
 TEST 09 - "EXTERNAL-WRAP" TEST
USE THE "SLOOP" OR "LOOP" OPTIONS.
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT TEST 07

ENTER 355 TEST CHAN [2 OCT DIGITS]  07

ENTER HMLC NO. 0-3 [2 DIGITS]  02

 ENTER A SUBCHANNEL NUMBER [2 OCTAL DIGIT]-06


 >> CONNECT "EXTERNAL" WRAP PLUG <<
     [CR WHEN READY]
                        (CR)
ANY MORE SUBCHANNELS
 [ENTER Y OR N]-  N
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

For more information on these tests, see T&D documentation on fiche.

HMLC baud rate switch should be a position #6 and the direct connect switch for the subchannel has to be 'on'.

Figure 3-13. Console Printouts for HMLC-HDLC T&Ds H7-H9

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N] N
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY- C
IOS OPT EAH
   EAH REV. C     HNP PAGER PROGRAM

MAXIMUM AVAILABLE CORE IS    177777
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000003
IOS OPT
```

Figure 3-14. Console Typeout for Extended Addressing T&D EA

```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? [ENTER Y OR N] N
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY- C
IOS OPT KD
KD      REV. B     KD-355 DISC DEVICE

ENTER 355 TEST CHAN [2 OCT DIGITS]   01

INSERT THE FLEXIBLE DISC. ──────────────►
 [CR WHEN READY]
                    (CR)

ENTER A 2 DIGIT DECIMAL VALUE TO
  REPRESENT A SECTOR [01 THRU 26]
  OR [A] FOR ALL SECTORS ON EACH
  TRACK TO BE READ.

  SECTOR ADDRESS 01
END OF PROGRAM

EDAC YELLOW LINE COUNT.
    000000
IOS OPT
```

Note:
Can use any diskette, T&D only reads it. Takes about 2.5 minutes if only one sector is specified.

Figure 3-15. Console Typeout for Diskette T&D KD

```
* DATANET IOS REV G
IS A PRINTER AVAILABLE? [ENTER Y OR N]
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,M=MASS STORE,D=DOC. ENTRY-C
IOS OPT PPR
 ER- PRG M2
PSIM2H REV. 00A  MSL-DN-PIA/MPC

ENTER 355 TEST CHAN [2 OCT DIGITS]  05
COM REGION ADDRESS- 02000

WHAT LOGICAL CHANNEL CONFIGURATION ARE YOU TESTING
[TYPE 1,2,4 OR 8 ].1

PART 2- THIS GROUP OF TESTS CHECK OUT THE INTERFACE
BETWEEN THE PSIC CHANNEL AND THE MPC CONTROLLER.

TEST INDICATES THE CHAN. IS CONFIGURED FOR 001  LC (Earlier revision will print "001000"
                                                      instead of "001 LC.")
TEST-07 THE DEVICE CONTROL REGISTER WILL BE USED
FOR DATA WRAPAROUND. TYPE IN THE OCTAL NUMBER [XX]
OF AN UNUSED DISK DEVICE.
    15
END OF PROGRAM
IOS OPT
TEST 08
```

Figure 3-16. I/O T&D (PRG M2) Console Printout

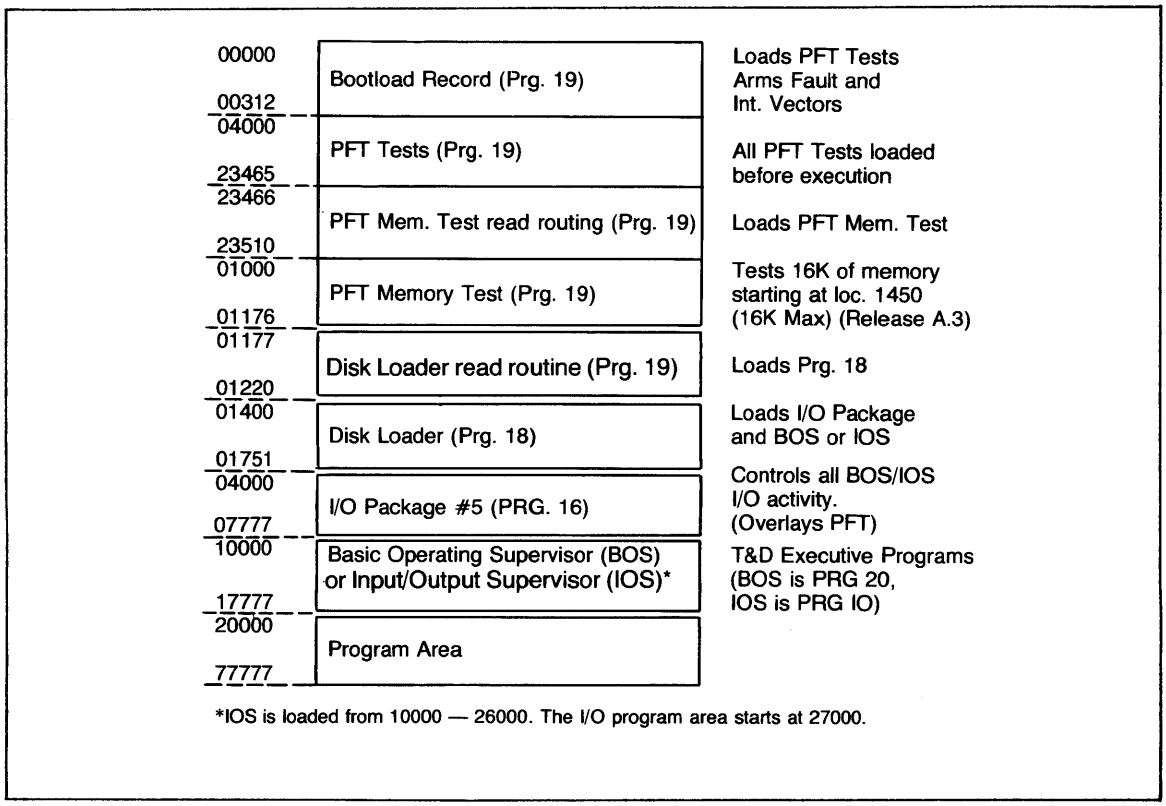
```
* DATANET IOS REV B RELS     A.4
*USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE? CENTER Y OR N]
ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY-
IOS OPT
MULTIO REV.    A    6670   MULTIO TEST
INPUT CHANNEL MODULE REQUESTS-
HSLA,WACH,CON,DIA
     WHEN INPUTS COMPLETE, TYPE GO
 IF ABORT DESIRED, TYPE OPT

MODULE - DIA
DEVICE#- 0

ENTER 355 TEST CHAN [2 OCT DIGITS]    04
COM REGION ADDRESS-  00454
MODULE - CON
DEVICE#- 0

ENTER 355 TEST CHAN [2 OCT DIGITS]    00
MODULE - WACH
DEVICE#- 0
MODULE - HSLA
DEVICE#- 1
HMLC SC# [2 DIGIT DEC]- 00
MODULE - HSLA
DEVICE#- 1
HMLC SC# [2 DIGIT DEC]- 02
MODULE - GO
***
IOS OPT     DEPRESS CARRIAGE RETURN (CR)
            THE PROGRAM WILL NOW RUN INDEFINITELY
            OR UNTIL INTERRUPTED BY AN ERROR OR BY
            DEPRESSING BREAK ON THE CONSOLE.
```

Notes:

Special instructions for MI.

1. When console types out "MODULE —", enter HSLA, WACH, CON, or DIA.
2. When console types out "DEVICE —", enter 0 for all modules except HSLA which should be as follows:
   1 for channel #6
   2 for channel #7
   3 for channel #10.
3. If a DIA is specified, the console will request channel number and com region address. Enter the same information as for DIA T&Ds, DA and DI; shown here is usual response. Note: DIA has to be connected to Host IOM.
4. If an HSLA is specified, the console will request a S/C #. The response has to be two digits and for even numbered subchannels only.
5. If console is specified, the logic will be tested but the console device will not be exercised.
6. Note: Multiple modules can be specified and they can be in any order, i.e., 2-DIAs and 3-HSLAs. More than one even number S/C can be specified.
7. Multi-I/O (MI) is designed as a bus or system exerciser. In this mode, any error situation will be very hard to diagnose. However, if it runs it should increase the confidence of system operation.

Figure 3-17. Console Typeout for Multi I/O T&D MI



*IOS is loaded from 10000 — 26000. The I/O program area starts at 27000.

Figure 3-18. DN66 T&D Memory Map

T&D OPTIONS

In response to the IOS OPT or BOS OPT message there are many options that can be entered. Several options may be entered in response to any option message. Each option should be separated from the previous option by one space. Whenever a number is entered, all leading and trailing zeros should be entered.

In the following descriptions all double-underlined options are standard options. The standard options are assumed when BOS/IOS is loaded.

If the user discovers he has made an error while entering options, he should push the Operator Input Error switch (CTRL and "X" on the teleprinter). This will cause the entire entry to be ignored. "ER-" will be typed, and the option can be re-entered.

At any point during execution the operator may depress the Request switch (BREAK on the teleprinter) and cause the option routine to be entered, producing the IOS OPT or BOS OPT message and causing a Console Read command to be issued, enabling input of options. The Option routine will also be entered following an error message if the standard HALT option is in effect.

All options can be abbreviated to the first three characters.

END OF MESSAGE (CARRIAGE RETURN ON TELEPRINTER)

This response to the BOS OPT message typed out when BOS is loaded will cause all programs to be executed sequentially. At any other time, the current test program will continue at the point where it left off.

ATYPE, APRINT

ATYPE and APRINT are similar to TYPE and PRINT options except that only an abbreviated form of the error message is output. This abbreviated error message contains only the program number, the test instruction, and the items in error.

If a printer is available the "PRINT" option is chosen as the standard. Otherwise, "TYPE" is selected as the standard option.

ALTER xxxxx

This entry allows an operator to make octal changes to a T&D program where xxxxx is the first address to be changed.

The Operating Supervisor will respond with the address and the current contents of that cell. A Read command is then issued to the console to allow the operator to enter the new contents of the cell. When the END OF MESSAGE switch is pushed (or CR), the next address and contents are output, etc. The format is:

IOS or BOS OPT: *ALTER 00401*

```
00401 - 004070
        004057
00402 - 004103
        004013
00403 - etc.
```

(The underlined portions are those entered by the operator.)

If no information is entered and the END OF MESSAGE switch is pushed, zeros will be stored in the cell. If an "N" is entered, no change will be made to the contents of the cell. To exit from the routine, "OPT" must be entered. This will cause a return to the options typeout.

There is one additional entry which can be made while in the ALTER routine. If during the Read command an "A" followed by a five-digit address is entered, BOS/IOS will output that address and its contents and continue the ALTER routine from that point.

BYPASS

If the BYPASS option is chosen, all error messages except unexpected fault messages will not be output. Errors will be output if the option is not chosen. The BYPASS option is reset by TYPE, PRINT, ATYPE, or APRINT options.

CONFIG

This option allows the operator to change the IOS System Configuration. The response to the CONFIG entry will be the following:

1. IOS will type "CHAN" and expect a two-digit octal channel to be output. Currently, only 00 to 16 octal are valid.
2. IOS will type "TYPE CODE" and expect a two-digit octal type code to be input. The following type codes are presently valid.

Device	*Type Code (Octal)*
HSLA	01
ICA	02
LSLA	03
PRINTEM	04
CIA	05
DCA	06
Card Reader	07
Mag Tapes	10
Console 10CPS	11
Console 15CPS	12
Console 30CPS	13
LFA	14
Wraparound Channel	15
Document Handler	16
Tape Cassette	17
DRD 236	20
DIA	21
PIA	22
CMA	23

IOS will type "COMM REGION ADDRESS" and expect a five-digit octal communications area address to be input. This communications area will contain control words (DATA and STATUS ICWS) pertinent to the channel utilized.

IOS will use the information from steps 1 through 3 to set up a new configuration table entry and establish a new set of interrupt vectors.

Repeat steps 1 through 3 until all desired configuration changes have been made.

If IOS detects an invalid input, "ER" will be typed. The input should be reentered in valid format.

The operator can exit from the "CONFIG" routine by an "OPT" in response to any of the messages in steps 1 through 3.

Console Log Example:

```
OPT: CONFIG
CHAN- 06
TYPE CODE- 01
COMM REGION ADDRESS 01000
CHAN- OPT
OPT: (Any option can now be entered)
```

Note:

_ = Operator Response

DELETE

The DELETE option allows the operator to remove a device from the IOS System Configuration table. DELETE differs from CONFIG in that it removes rather than replaces an entry. The response to the "DELETE" entry will be the following:

1. IOS will type "CHAN" and expect a two-digit octal channel number in reply. Only 00 to 16 octal are valid.

The specified channel will be designated inactive in the IOS System Configuration table. Interrupt vectors and status ICWs will be realigned.

Step 1 will be repeated until all necessary deletions have been made.

Console Log Example:

```
OPT: DELETE
CHAN- 05
CHAN- OPT
OPT: (Any legal option can now be entered)
```

Note:

__ = Operator Response

DUMP

DUMP causes all of memory to be output in octal format. To stop, depress BREAK key and enter new option.

HALT

When the HALT option is chosen, the program will halt after each error message. Refer to RUN option description.

HOLD xx

The HOLD option will cause the test program to be executed xx times. xx must be two characters. If not otherwise specified, the program will be executed 262,144 times.

LOOP/NOLOOP

The LOOP option causes the program to loop on a test until the BREAK key is depressed. *NOLOOP* resets the LOOP option.

ODUMP (BOS Only)

ODUMP displays the Op Code table, indicating those instructions that have been checked.

PDUMP (BOS Only)

PDUMP causes the current program to be dumped in octal to the current output device, console or printer.

PRG xx

PRG xx causes program xx to be loaded and executed.

PRINT

See the TYPE/PRINT option description.

PTAL/RTAL

PTAL causes an error tally message to be output. This message has the following format:

```
CURRENT ERROR TALLY = xxxxxx
```

The tally count is reset by the RTAL option. The main use for PTAL and RTAL is to count the number of errors which occur when looping in a test with the BYPASS option set.

RESET

This entry returns all of the options to the "standard" options that prevailed at the time of the initial Option Request typeout. The standard options are double underlined in these descriptions.

RUN

When the RUN option is chosen, the program will continue without stopping after each error message. See the HALT option description.

SEQ (BOS Only)

The normal sequence of events is for each program to be called in automatically upon completion of the previous program. SEQ allows the user to again enter this mode after calling in a program individually, such as with the PRG xx option. When SEQ is entered, normal sequencing will commence, starting with the next program.

SKIP/NOSKIP

If the program is in the RUN mode, the SKIP option is chosen, and an error message is output, the Executive will branch to the next test, as found in the test table. If the program is in the HALT mode and an error message is output, the message will be followed by the Options typeout. The Executive System will branch to the next test if SKIP is then entered. In the HALT mode, the SKIP option is reset after each use. NOSKIP will reset the SKIP option in the RUN mode. In the HALT mode, SKIP will be ignored if an initialized program is not in memory.

SLOOP/NSLOOP

When SLOOP is encountered, the Operating Supervisor will cause the test program to take the smallest possible loop (subtest loop) on the last error that occurred.

NSLOOP (No Subtest Loop) negates the SLOOP option and restores the program to its normal execution.

SNAP/NOSNAP

This option turns on and off the dump provided by the snapshot DUMP macro. This option is valid only if the program has coded the SNAP macro. It is usually a PROGRAMMER DEBUG option.

START

This entry will restart the program currently in execution. START must be used to restart a program after the "End of Program" typeout. START does not reset the LOOP or SLOOP options. START is ignored if an initialized program is not in memory.

TEST xx

TEST xx causes a subtest of the loaded T&D to be executed only. This option can be used if a program is already in execution or in conjunction with the PRG xx option. If only the TEST xx option is attempted and a program is not in execution, the Executive Program will type out ER- and wait for a valid entry. When accepted, the TEST xx option will cause the current program to start at TEST xx.

TRA xxxxx

This entry will cause a transfer to location xxxxx.

TYPE/PRINT

When the TYPE option is chosen, all messages will appear on the system console. When the PRINT option is chosen, all messages except those specified for the system console only will appear on the printer, if available.

DUMPS

XDUMP XXXXX YYYYY

Dumps area starting with address XXXXX and ending with address YYYYY.

The first line of each of these dumps will contain the sequential dump number followed by the dump type. The register contents will be output below this. The register contents shown are those at the time that 355 IOS was entered via a fault, an error message, or by depressing the REQUEST switch on the console. The following register abbreviations are used:

IC	=	Instruction counter
A	=	A register
Q	=	Q register
X1, X2 & X3	=	Index registers 1, 2 and 3
I	=	Indicator register
S	=	Input/output enable select register
IF	=	Interrupt enable register

Any parity errors encountered during the dump will be indicated by an arrow pointing to the cell in which the error occurred.

ERRORS

PAS STANDARD ERROR MESSAGE

If the results or the faults are not as expected, a standard error message will be output under control of the standard operator options.

Error Message Example:

```
LINE 1 **************FIXED ADD-A REG.**************
LINE 2 PS700 TEST-12A S-ADDR TEST BAR-060004
LINE 3 TEST START 000412 PATCH 000467 SUBTEST LOOP POINT 000432
LINE 4 S-ADDER OUTPUTS ARE TESTED FOR ALL LOGICAL INPUT COMBINATIONS FOR
       THE ADD FUNCTION.
LINE 5 LOCATION 000453 000150075400 INSTRUCTION IS ADA
        C(Y)          = 000000000001
LINE 6 PRIME RESULTS              A              E
                    S/B  070707070707        000
                    WAS  070717070707        001
LINE 7 SECONDARY RESULTS        X1          IR
                   S/B     000000        400000
                   WAS     000001        000000
LINE 8 FAULTS       S/B             WAS
                NONE            PARITY (000440)
LINE 9 FUNCTION IN ERROR - S-ADDER INPUTS . . . . . .
              EXPLANATION OF PAS ERROR MESSAGE
       LINE 1                      PROGRAM NAME
       LINE 2 - PS700              TEST TYPE AND IDENTIFIER
              - 12A                TEST NUMBER AND SUBTEST LETTER
              - S-ADDER            TEST NAME
       LINE 3 - TEST START 000412
                                   LOCATION TO TRANSFER FOR LOOP ON TEST
              - PATCH 000467
                                   CHANGE LOCATION TO LOOP ON TEST
       LINE 4 -                    DESCRIPTION OF TEST
       LINE 5 -                    AFFECTED LOCATIONS BEFORE EXECUTION
       LINE 6 -                    PRIME REGISTERS AND AFFECTED LOCATIONS
       LINE 7 -                    SECONDARY REGISTERS AND AFFECTED
                                   LOCATIONS
       LINE 8 -                    EXPECTED AND ACTUAL FAULTS
       LINE 9 -                    TELLS WHAT FUNCTION FAILED
```

Note:

This is an example to show all parts of the error message. It does not represent an actual case.

PAS UNEXPECTED FAULT ERROR MESSAGE:

An unexpected fault will cause an error message to be output, regardless of the options selected by the operator, if there is a printer or a console available.

```
        ERROR MESSAGE EXAMPLE
**********6000 FAULT LOGIC**********
PS720    TEST-01A              BAR-06004
UNEXPECTED ILL PROCED'R FAULT AT 062642 ABSOLUTE
C(062641) = 000000000000 FAULT REG = 400000000000
```

PAS ABBREVIATED ERROR MESSAGE:

The standard error message can be reduced to a minimum error message at the operator's option. The abbreviated error message is called in through the "ATYPE" option for the console or the "APRINT" option for the printer. The abbreviated error message contains only the program number, test number, and the items found to be in error.

```
ERROR MESSAGE EXAMPLE
PS720         TEST-01A
SECONDARY RESULTS
        S/B   777777777777
        WAS   000000000000
```

IOS STANDARD ERROR MESSAGE

Whenever an error occurs in a test program, the appropriate information is supplied to IOS, which then outputs the standard error message shown below:

```
 1. **ERROR** HSLA SUBCHAN. TEST *TST 24A (035106)
 2. SWITCH PRIMARY SEND ICW BY PCW0
 3. OCT CHN 06 SUBCHN 00 PCW 200000 000760
 4. DATA ICWS
 5. PRE  240672 000020    240702 010000    RCV
 6. POST 240702 010000    240702 010000
 7. S/B  240702 010000    240702 010000
 8. PRE  240632 000022    240645 000010    SND
    POST 340637 010010    240647 010000
    S/B  240637 010010    240647 010000
 9. INTERRUPTS: 2/1
10. STATUS: 2/1
11. EXPECTED  400200    700760    424000    700160
12. ACTUAL    400200    700760       MISSING
13. MASK BITS 000000    000000    000000    000000
14. DATA ERRORS    1/16
15. ADDR 240767
16. IS       020
17. S/B      040
18. MISSING STATUS STORE(S)
    ICW IN ERROR
    CHECK SUBCHANNEL *000 BOARD

    *********
```

EXPLANATION OF IOS STANDARD ERROR PRINTOUT

LINE 1: "**ERROR**" INDICATES START OF STANDARD ERROR OUTPUT. ALSO CONTAINED IN THIS LINE ARE:

- --- PROGRAM NAME ("HSLA SUBCHAN. TEST")
- --- TEST AND SUBTEST ("24 AND A")
- --- ABSOLUTE OCTAL ADDRESS OF I/O CALL SEQUENCE ("035106")

LINE 2: DESCRIPTION OF THE TEST

LINE 3: GIVES IOM CHANNEL NUMBER IN OCTAL, SUBCHAN NUMBER IN OCTAL (HSLA AND LSLA ONLY), AND THE PCW ISSUED TO THE CHANNEL. IF THE ACTION ON THIS CHANNEL WAS CAUSED WITHOUT ISSUING A PCW TO THE CHANNEL (FOR EXAMPLE, A LDEX INSTRUCTION), THEN THE MSG. "NO COMMAND ISSUED" WILL APPEAR IN PLACE OF THE PCW.

LINE 4: LINES 4–7 GIVE THE DATA CONTROL WORD INFORMATION ASSOCIATED WITH THE ERROR, IF APPLICABLE.

LINE 5: THE "PRE" LINE GIVES THE ICW BEFORE THE CONNECT WAS ISSUED THE "RCV" NOTATION IS USED WITH LSALA AND HSLA ONLY TO INDICATE RECEIVE ICW'S. THE ICW'S ARE ALWAYS SHOWN SEQUENTIALLY FROM LEFT TO RIGHT.

LINE 6: THE "POST" LINE GIVES THE ICW RESIDUES AFTER COMPLETION OF THE I/O.

LINE 7: THE "S/B" SHOWS WHAT THE EXPECTED ICW RESIDUE WAS. THIS LINE IS OUTPUT AT THE DISCRETION OF THE TEXT PROGRAM AND THEREFORE THE "PRE" AND "POST" LINES MAY APPEAR WITHOUT THE "S/B" LINE.

LINE 8: IF ALL CONTROL WORDS CANNOT BE LISTED IN ONE LINE, LINES 5–7 ARE CONTINUED HERE. THE "SND" NOTATION SHOWN HERE IS USED FOR LSLA AND HSLA ICW'S ONLY TO INDICATE ICWS.

LINE 9: GIVES INTERRUPTS EXPECTED AND RECEIVED. EXPECTED INTERRUPTS ARE ON THE LEFT–HAND SIDE OF THE SLASH, RECEIVED INTERRUPTS ARE ON THE RIGHT.

NOTE: ACTUAL INTERRUPTS CAN NEVER BE GREATER THAN THE NUMBER OF EXPECTED INTERRUPTS. INTERRUPTS OVER THE EXPECTED NUMBER ARE REPORTED AS "EXTRA INTERRUPTS" EXPLAINED LATER.

LINE 10: GIVES THE NUMBER OF EXPECTED AND ACTUAL STATUS RETURNS. NOTE THAT THE NUMBER OF STATUS RETURNS MAY NOT BE THE SAME AS THE NUMBER OF INTERRUPTS, SINCE SOME TYPES OF INTERRUPTS DO NOT STORE STATUS. THE EXPECTED NUMBER OF STATUS RETURNS IS ON THE LEFT–HAND SIDE OF THE SLASH, THE ACTUAL NUMBER ON THE RIGHT.

LINE 11: GIVES THE EXPECTED STATUS RETURNS IN THE EXPECTED ORDER OF OCCURRENCE FROM LEFT TO RIGHT. STATUS RETURNS ARE ALWAYS SHOWN AS 36–BIT DATA. IF A DEVICE STORES STATUS OF LESS THAN 36 BITS, THE STATUS WILL BE RIGHT–JUSTIFIED AND PADDED WITH LEADING ZEROS TO FORM 36 BITS OF DATA.

LINE 12: GIVES THE ACTUAL STATUS RETURNS IN THE ORDER IN WHICH THEY OCCURRED. IF THE NUMBER OF ACTUAL RETURNS DOES NOT EQUAL THE NUMBER OF EXPECTED RETURNS, IOS WILL INSERT "MISSING" IN THE ACTUAL STATUS MESSAGE SLOT.

LINE 13: GIVES THE 36–BIT STATUS MASK FOR EACH STATUS RETURN. BITS WHICH ARE ONES IN THE STATUS MASK INDICATE THAT THE CORRESPONDING ACTUAL STATUS BITS WERE NOT CHECKED BY THIS TEST. THIS LINE WILL BE OMITTED IF THE STATUS MASKS ARE ALL ZERO, MEANING ALL STATUS BITS WERE CHECKED.

LINE 14: GIVES A SUMMARY OF THE DATA ERRORS DETECTED, E.G., "1/16." THE LEFT-HAND NUMBER IS THE NUMBER OF DATA CHARACTERS IN ERROR, AND THE RIGHT-HAND NUMBER IS THE TOTAL NUMBER OF DATA CHARACTERS WHICH WERE TO BE TRANSFERRED. THIS LINE ALSO GIVES THE DATA CHARACTER SIZE. IF NO DATA ERRORS OCCURRED THIS LINE WILL BE OUTPUT TO SO INDICATE, BUT LINES 15 TO 17 WILL BE OMITTED.

LINES 15-17: GIVES EXAMPLES OF THE DATA CHARACTERS IN ERROR. A MAXIMUM OF 12 ERROR EXAMPLES WILL BE OUTPUT. LINE 15 GIVES THE ADDRESS (CELL AND CHARACTER POSITION) OF THE ERRONEOUS CHARACTER, THE ACTUAL CHARACTER RECEIVED IS IN LINE 16. IF NO DATA WAS RECEIVED, THIS CHARACTER WILL BE THE PAD CHARACTER FOR THE TEST PROGRAM DATA BUFFER. REFER TO INDIVIDUAL TEST PROGRAM DOCUMENTATION. FOR PAD CHARACTER DEFINITION. LINE 17 SHOWS WHAT THE DATA CHARACTER SHOULD HAVE BEEN.

NOTE: BECAUSE OF THE DATA TRANSFER CHARACTERISTICS OF THE LSLA, LSLA TEST ERROR MSGS WILL NOT HAVE LINES 14-17 BUT WILL HAVE A SEPARATE DATA ANALYSIS FOLLOWING THE STANDARD ERROR MSG. BODY.

LINE 18: THIS PORTION IS A VARIABLE LENGTH FREE FORM MSG SET UP BY THE TEST PROGRAM WHICH WILL PINPOINT THE CHARACTERS IN ERROR AND INDICATE PROBABLE BOARDS IN ERROR. THIS MESSAGE IS EXPLAINED MORE FULLY IN THE DOCUMENTATION FOR INDIVIDUAL TEST PROGRAMS.

NOTE: CERTAIN ERRORS WHICH ARE NOT THE DIRECT RESULT OF I/O STIMULUS WILL BE REPORTED BY SOME TEST PROGRAMS IN A FORMAT RESEMBLING THE STANDARD ERROR MESSAGE BUT WITH LINES 3 TO 17 OMITTED.

ADDITIONAL IOS ERROR MESSAGES

NONSTANDARD ERRORS

When peripheral errors, extra interrupts, operator errors, etc., occur, 355 IOS and the I/O package will output messages to indicate the error conditions. All of these are listed below. Any other nonstandard error messages are output by the individual test programs. Refer to individual program documentation for descriptions of these messages.

```
UNEXPECTED XXXXXXXXXX FAULT AT YYYYY
```

This message is output whenever a fault other than an IOM channel fault occurs (IOM channel faults are handled as extra interrupts). The first field (XXX-XX) specifies the type of fault. The second field (YYYYY) specifies the address at which the fault occurred.

EXTRA INTERRUPT

```
VECTOR/CHN/SUBCHN/        STATUS       /TEST/LAST I-O
004     06  00      412000 700760       18J   032352
004     06  00      002000 700760       18J   032352
```

The extra interrupt message is output following receipt of one or more interrupts which are not expected by any active I/O call sequences. The English header lines are output once, followed by a line of data for each of the extra interrupts received. Any data which was indeterminate or not applicable to the type of interrupt received is indicated by dashes. The "VECTOR" column gives the octal address of the interrupt vector. "CHN" gives the IOM channel number in octal. "SUBCHN" gives the octal subchannel number (LSLA and HSLA only). "STATUS" gives the status word pair associated with the interrupt (if any) in the same format as line 11 of the

standard error message. "TEST" gives the test and subtest which were executing at the time of the interrupt, and "LAST I/O" gives the address of the last standard I/O request issued by the test program before the interrupt occurred.

```
ER- XXXXXXXXXX
```

If an invalid option is entered in response to "IOS OPT or BOS OPT": the above message is output, where the X's are replaced by the invalid option.

TOO MANY OPTIONS

IOS has a fixed buffer area that is used for option input. The above message is output when this area is exceeded. None of the options specified will be executed, and the option request message and console read command will be re-issued.

HALTS IN DIS INSTRUCTION

Some errors occur from which no normal recovery can be made. When this happens, IOS will halt in a DIS instruction. The least significant six bits will be a code indicating the type of error.

If the code is A 1, a fault occurred while the program was processing a previous fault.

If the code is A 2, the test program made an illegal request of IOS. This error should never be seen by the user.

L/P TROUBLE

When a printer reports status error, this message is output. To continue, the error condition should be corrected and the end of message switch pushed. The print routine will retry the line on which status error occurred.

```
UNEXPECTED INTERRUPT AT LOC XXXXXX
```

This message is output whenever an interrupt that is not expected by the I/O package or the test program occurs. The location indicated will be the last instruction executed before the interrupt was answered.

PARTIAL ONLINE (POL) TESTS

The POL tests provide an alternate method of loading and running the DATANET T&Ds from the host system via the direct interface adapter (DIA). The input source is the binary deck tape which contains the DATANET T&Ds. The console printouts are on the host system except for memory T&D PRG 86, which prints out on the DATANET console. The operating procedures for each of the DATANET T&Ds remain the same as illustrated in Figures 3-6 through 3-17. Programs DA/DI cannot be run on the device interface adapter and program CO cannot be run on the console.

POL tests can be run under either GCOS/TOLTS/COLTS control or under Monitor-4 (PRG 3BT). If GCOS is resident in the host, the POL loader is called in under TOLTS/COLTS control. The POL loader program runs primitive function tests on the DATANET, then gives the option of loading either the BOS Executive (for processors and memory tests) or IOS Executive (for I/O program control). The operator further has the option, when the BOS Executive is in control of the DATANET, of running all programs through PRG 75 automatically and sequentially, or of calling each desired program individually.

If Monitor-4 is resident in the host, program 3BT must be called in by the operator. The same testing procedure and options apply under 3BT control as were described above.

LOADING PROCEDURES

These procedures are performed from the host console. The DATANET system should be initialized before loading the POL tests.

1. Key in TEST BCx (where x = the logical DATANET number:0,1,2, or 3).
2. Mount DATANET T&D binary deck tape (in protect).

3. When requested, key in track/density and reel number of T&D tape.
4. Key in TCALL CSS-x (where x = DATANET number).
5. At option request, if possible, key in .PRT (allows messages on host allocated printer).
6. At request to release DATANET, key in TEST BOCxRLSE (where x = DATANET number).
7. At request to load BOS to IOS, key in B (for BOS) or I (for IOS).

Note:

The Mainframe and Memory T&Ds run under BOS; the I/O T&Ds run under IOS. To switch from BOS to IOS, or from IOS to BOS, requires terminating and starting again. To terminate POL, key in TEST BECx (where x = the logical DATANET number).

OPERATING PROCEDURES

The procedures for each program are identical to the offline T&D operating procedures except that the host console is used. See Figures 3-6 through 3-7, 3-9, 3-20, and 3-21.

RESTRICTIONS/LIMITATIONS

The Executive (COLTS, MONITOR) will test one Front-end Network Processor (FNP) at a time due to internal/memory restraints.

The DIA should be configured on channel 4 on the FNP IOM. If the DIA is configured on another channel, it must be reconfigured to channel 4 before initiating this particular T&D function.

The COLTS On-Line Interface program will not perform any I/O operation to DATANET peripherals; i.e., it will be limited to the 6000 console and the printer. Refer to Figures 3-19, 3-20, and 3-21.

```
???test bc1

***COLTS EXECUTIVE VERSION 781027 ON 020880 AT 06.87
**ISSUE TCALL ON CSS#1 BEFORE TESTING BEGINS

***(COLTS EXECUTIVE)
ENTER TRACK/DENSITY OF T&D TAPE (7-9)/(5-8-16)?9/8
     *MNT TAPE S#$COLT0 0-12-02   REEL#99999


**0(355P1)PAS355 START TD7/BA-POL3, TTLDAT 781207, PHY./LOG. ID /T/04

**0(355P1)PAS355 START PPAS REV 1
*VERIFY THAT ICC MBX IS 002300, ICC INTERRUPT CELL IS 03
*AND RELEASE DN355 ON CSS # 1 BY ENTERING THE OPTION ".RLSE"

**0(355P1)PAS355 WAITING

???test boc1.rlse

**0(355P1)PAS355
PLEASE DEDCAT PR2 IF POSSIBLE
**LOAD BOS OR IOS EXEC FIRST-(B OR I)?i

**0(355P1)PAS355

* DN-6670 10H REV A RELS FW927
*USE UPPER CASE CHARS.

**0(355P1)PAS355
 IS A PRINTER AVAILABLE?.(ENTER Y OR N)  n
```

Figure 3-19. Example of Host Console Typeout for POL T&D IOS

```
**0(355P1)PAS355
 ENTER SUBSYSTEM TYPE;
C=COMMUNICATIONS,D=DOC. ENTRY- c

**0(355P1)PAS355
 IOS OPT  prgh1

**0(355P1)PAS355
    H1H REV. C     HMLC CENTRAL PART1

**0(355P1)PAS355

ENTER 355 TEST CHAN (2 OCT DIGITS)   06

**0(355P1)PAS355

ENTER HMLC NO. 0-3 (2 DIGITS)  00

**0(355P1)PAS355

RUN COMPLETED
SHOULD I DUMP ACTIVE CHANNEL TABLE (Y OR N)  n

**0(355P1)PAS355
 LOAD HMLC CENTRAL TEST PART 2

**0(355P1)PAS355
 END OF PROGRAM

**0(355P1)PAS355

EDAC YELLOW LINE COUNT.
    000000

**0(355P1)PAS355
 IOS OPT


      prgh2

**0(355P1)PAS355
    H2H REV. C     HMLC CENTRAL PART2

**0(355P1)PAS355

;ENTER 355 TEST CHAN (2 OCT DIGITS)   06

**0(355P1)PAS355

ENTER HMLC NO. 0-3 (2 DIGITS)  00

???test bec1 ──────────────────► To terminate IOS; or could
                                 continue running IOS T&Ds.
**0(355P1)PAS355

*FORCED TEST TERMINATION

**0(355P1)PAS355 FORCED TERM 1: 0 STATUS AND 0 DATA ERRORS
TEST E REQUEST RECEIVED
     *DMT--S#$COLT0000 0-12-02 [TD] #99999


***COLTS EXECUTIVE VERSION 781027 OFF 020880 AT 06.96 P.T. 56736

***TOLT TESTING NORMAL-TERM P.T. 000000000768
```

Figure 3-19 (cont). Example of Host Console Typeout for POL T&D IOS

```
???test bc1

***COLTS EXECUTIVE VERSION 781027 ON 020880 AT 06.74
**ISSUE TCALL ON CSS#1 BEFORE TESTING BEGINS

***(COLTS EXECUTIVE)
ENTER TRACK/DENSITY OF T&D TAPE (7-9)/(5-8-16)?9/8
     *MNT TAPE S#$COLTO 0-12-02   REEL#99999


*TS1 020880 06.75   1 USERS    45K


**0(355P1)PAS355 START TD77BA-POL3, TTLDAT 781207, PHY./LOG. ID 1//04

**0(355P1)PAS355 START PPAS REV 1
*VERIFY THAT ICC MBX IS 002300, ICC INTERRUPT CELL IS 03
*AND RELEASE DN355 ON CSS # 1 BY ENTERING THE OPTION ".RLSE"

**0(355P1)PAS355 WAITING

???test boc1.rlse

**0(355P1)PAS355
PLEASE DEDCAT PR2 IF POSSIBLE
**LOAD BOS OR IOS EXEC FIRST-(B OR I)?b

**0(355P1)PAS355

* DN-6670 20H REV A RELS FW927
"WARNING" USE UPPER CASE CHARS.
IS A PRINTER AVAILABLE?(ENTER Y OR N)   n

**0(355P1)PAS355
 BOS OPT
          (CR)

**0(355P1)PAS355
 25H REV. 00A  CHAR & IND. ADDR.

**0(355P1)PAS355
 30H REV. 00A  DATA MOV&FIXED ADD

**0(355P1)PAS355
 31H REV. 00A  DATA MOV&FIXED ADD

**0(355P1)PAS355
 32H REV. 00A  DATA MOV&FIXED ADD

**0(355P1)PAS355
 35H REV. 00A  FIXED ADD TO STORE

**0(355P1)PAS355
 40H REV. 00A      COMPARISON

**0(355P1)PAS355
 45H REV. 00A  HNP SHIFT TESTS

**0(355P1)PAS355
 50H REV. 00A  MULTIPLY & DIVIDE

**0(355P1)PAS355
 55H REV. 00B  HNP IOM INTR PART1

**0(355P1)PAS355
 MAXIMUM USEABLE CORE IS 32K FOR THIS TEST.

**0(355P1)PAS355
 56H REV. 00A  HNP IOM INTR PART2
```

Figure 3-20. Example of Host Console Typeout for POL T&D BOS

```
**0(355P1)PAS355
 57H REV. 00A  HNP IOM INTR PART3

**0(355P1)PAS355
 60H REV. 00A   ILLEGAL OP TEST

**0(355P1)PAS355
 65H REV. 00A  HNP REGISTER INTER

**0(355P1)PAS355
 70H REV. 00B  DN-6670 IOM TEST

**0(355P1)PAS355
 71H REV. 00A  HNP IOM TIMER TEST ──► At this point, PRG 75 is executing
                                      even though it has not typed out.
```

Figure 3-20 (Cont). Example of Host Console Typeout for POL T&D BOS

```
???test boc1.com ──────────────────► Same procedure as for POL BOS up to this point.

**0(355P1)PAS355
 75H REV. 00A   INST. SEQ. PROG.──► To communicate with POL EXEC, causes it to
                                    print out that it was executing PRG 75.
**0(355P1)PAS355

UNEXPECTED  IOP  FAULT AT  077651. ► Glitch in the program that does not cause any problems.

**0(355P1)PAS355
 BOS OPT  prg80 ──────────────────► Call for PRG 80 (cache).

**0(355P1)PAS355
 BOS OPT     (CR)

**0(355P1)PAS355
 80H REV. 00B  HNP CACHE MEMORY

**0(355P1)PAS355

MAXIMUM AVAILABLE CORE IS   777777

**0(355P1)PAS355

TWO WORD TRANSFER INDICATES TYPE 100 MEMORY BOARD.

**0(355P1)PAS355

TEST INDICATES CACHE CONFIGURED WITH 4K CACHE ARRAY.

**0(355P1)PAS355
 END OF PROGRAM

**0(355P1)PAS355

EDAC YELLOW LINE COUNT.
    000000

**0(355P1)PAS355
 BOS OPT  prg86 ──────────────────► Call for PRG 86 memory.

**0(355P1)PAS355
355 CORE PRG CALLED, PPAS WILL REFINI

**0(355P1)PAS355 NORMAL TERM 1: 0 STATUS AND 0 DATA ERRORS
     *DMT-- S#$COLT0000 0-12-02 ETD] #99999


***COLTS EXECUTIVE VERSION 781027 OFF 020880 AT 06.86 P.T. 171337

***TOLT TESTING NORMAL-TERM P.T. 000000001325

*FY1 MPC CH NOT SAMPLED ON 02601, STATUS: 600000000100
```

PRG 86 is now executing in DN66 and control is transferred to DN66 console. Use offline procedures at the DN66 console.

POL now terminates.

Figure 3-21. Example of Host Console Typeout for POL T&Ds 80 (Cache) and 86 (Memory)

BOOTLOADING

The FNP Primitive Function Tests (PFTs) will be segmented (due to space) and booted to the FNP for execution. This will verify the basic 20 instructions for the I/O package and Executive. After completion of the PFTs, the L66 Resident Program will send a "loader" program to the FNP which in turn will process the FNPs I/O package and Executive program. The I/O package and Executive is sent to the FNP in card image format.

NORMAL EXECUTION

Once the I/O package and Executive programs are in the FNP, requests outside the system will be via the four-word information blocks. The FNP will initiate all requests by interrupting the L66. The L66 will, upon receiving an interrupt, read the four-word information block to determine if the FNP requires output to the console or printer, input from the console or input of a program. The four-word information block will contain all the necessary data for the L66 to perform its task.

PROGRAM INPUT

The Binary Deck Tape is a multi-file tape, where each file represents a T&D program (e.g., Bootloader, Primitive Function Test, Executive, etc.).

Note:

The seven-track tape will be 556 bpi. The nine-track tape will be 800 bpi.

COMMUNICATION WITH THE FNP

The FNP will interrupt the L66 when an operation is required. the L66 will then fetch a four-word block of data from the FNP at location 4004 and interpret the request.

POL OFFLINE T&D (MONITOR)

3BT OPERATOR INTERFACE

3BT will be called in under monitor control. If the FNP contains a DIA, the CONFIGURE statement will be standard; i.e.,

```
CONFIG  DIA 10^PRG3BT^
CONFIG  DIA 10^SYSTEM B355^
```

When 3BT is in memory and running, and if there is only one tape subchannel configured, the program will not have to request IOM and channel numbers from the operator. If more than one tape is configured, the operator will be requested to input this information in the form I/cc. In either case the operator will be requested to input the tape device number that contains the binary deck tape.

3BT will then access this tape, read in the PFTs one at a time, process them (deleting non-data), and boot the PFTs over to the FNP.

3BT will then boot over a boot program which will allow the FNP to accept card image data from the L66, strip the non-FNP data from it, and store the program in the appropriate location in its (FNP) memory.

At this point the operator is asked whether he wants to load IOS or BOS. The appropriate Executive, along with with I/O package, is read from tape and sent to the FNP in card image format.

When loaded and initialized, the FNP Executive will cause a special interrupt to be issued to the L66. From this time on, any time a special interrupt occurs, 3BT will read a four-word block in the FNP memory which will indicate to the L66 what service the FNP Executive wants performed or what the status of a program load is. Requests for a specific program will be passed to 3BT via this four-word block. 3BT will then search the tape for the desired program, read it into memory, and send it to the FNP. When data transmission is completed, the FNP executive will cause a special interrupt to be sent to the L66. 3BT will then inspect the four-word block in FNP memory to determine if the program load was successful.

If the operator wishes to reboot the FNP or load a new Executive, he will key in Request on the console which will cause the Monitor to go to "*OPTIONS?". The operator may then input "355" and press EOM. Monitor will then transfer to an address in the header of 3BT (word 17), which in turn will transfer to the 355 options routine in 3BT. At this time the operator can elect to reboot or request that a different Executive be loaded.

EXECUTION SEQUENCE OF PRIMITIVE, LOADER, I/O PACKAGE AND EXECUTIVE

L66 Side	**FNP Side**
(1) *Send interrupt vectors, fault vectors and vector processor to FNP.	
*With T&D "Write" command send Primitive Function Tests (PFTs) to FNP.	
*Set interrupt in FNP to cause PFTs to execute.	(2) *Interrupt received, transfer is made to the start of the Primitive.
*Wait in 10 second loop; if no Level 3 is received, then Primitive "Has Halted in DIS."	*Execute Primitive.
	*If no error, interrupt L66 Level 3 to indicate O.K.
(3) *Level 3 received, thus O.K. *Send core Primitive to FNP and set up a vector in the FNP pointing to the start of the Core Primitive.	(4) *Interrupt received, transfer is made to start Core Primitive.
*Set Interrupt to FNP to cause execution.	*Core Primitive executes.
*Wait in 10-second loop for level 3 from FNP.	*Set level 3 to interrupt.
(5) *Set up level 7 for "Request from-FNP" module. *Send "Card-Image" loader to the FNP.	(6) *Send interrupt level 3.
*Wait for interrupt Level 3 to indicate the "Loader" is in place.	
(7) *Send the I/O package x and Executive to the FNP in blocks of card image format.	(8) *Process the card image data, move into place and, if O.K., send interrupt Level 3.
*Wait for a Level 7 interrupt to indicate a "Request From FNP" and examine the Interface Data Block (IDB).	*Send interrupt level 7 to L66 for "Console-Write". Normally at this point, output "3550PT":
(9) *Receive Level 3 to indicate everything is ready for normal operations.	
*Receive level 7 to indicate "Request From FNP."	

INTERFACE SEQUENCE (FNP INITIATED)

WRITE TO/READ FROM L66 CONSOLE AND PRINT OPERATIONS

L66 Side

(2) *Request received from FNP (Level 7)

*Read IDB from FNP and go to appropriate processing module for Read, Write, or Print.

*Do your thing

*Interrupt FNP with level 3 to indicate done and for the FNP to go on.

*Wait for next happening

FNP Side

(1) *Set up Interface Data Block (IDB) for desired operation.

*Point FNP interrupt Level 3 to "Self-After-DIS."

*Send interrupt level 7 to 6000 to indicate a "Request From FNP."

*Wait in DIS

(3) *Interrupt Level 3 received to indicate L66 is finished and to continue.

INTERFACE SEQUENCE (L66 INITIATED)

OPTIONS REQUEST AT L66 CONSOLE

L66 Side

(1) *Special from L66 console causes Control Executive to user.

(2) *User inputs "xx355" to get control of FNP.

(3) *6000 Driver sends interrupt (Cell #7) to FNP.

(8) *Interrupt received, check IDB for type of action.

(9) *Sequence will be the same as that of the "Write To/Read From L66 console."

FNP Side

(4) *Receives Cell #17 interrupt which indicates "Request-From-L66."

(5) *Saves last IC.

(6) *Set up IDB to output. Send "Interrupt L66 (Cell #7)."

(7) *Wait.

Level 3 (Terminate)

*Always send a Cell #3 interrupt to the FNP to acknowledge the completion of an action.

*The only time the L66 will receive a level 3 is while it is in the process of sending a test program to the FNP. It will indicate to the L66 that the transfer card was detected and the last data transfer was good.

Interrupt Cell #3

*The FNP will receive an interrupt Cell #3 each time after it has requested the L66 to perform an action. This received "Cell 3" interrupt will indicate the "action" was performed and for the FNP to continue with execution.

COMMUNICATIONS ONLINE TESTING SYSTEM (COLTS)

COLTS, a subsystem of the Total Online Testing System (TOLTS), enables the testing of DATANET subchannels or remote devices concurrently with the operating system. COLTS is run from the host system when GCOS is resident in the host and NPS or GRTS is resident in the DATANET. Testing is controlled by TOLTS/COLTS. COLTS obtains the subchannel type by querying the appropriate test page. No processor or memory tests can be run under TOLTS when NPS or GRTS is resident in the DATANET. Only HMLC/CIB subchannels can be tested.

LOADING PROCEDURES

COLTS is always loaded and ready to perform subchannel or remote-device testing.

OPERATING PROCEDURES

The procedures to test the DATANET subchannels or remote devices are described below.

HMLC SUBCHANNEL WRAPAROUND

TEST Cxccssooooo

where

x	= Logical DATANET number (0, 1, 2, or 3)
cc	= DATANET IOM channel number in decimal (6, 7, or 8)
ss	= Subchannel number in decimal (00-31)
ooooo	= Option characters or a control mnemonic

IOM CHANNEL ADAPTERS

CAA Adapter Only Includes Console Test:

TEST Cxccssooooo

where:

x	= Logical DATANET number (0, 1, 2, or 3)
cc	= DATANET IOM channel number in decimal (6, 7, or 8)
ss	= Subchannel which must be zero
ooooo	= Option characters or a control mnemonic

KEYBOARD TYPE DEVICES

VIP/TTY Devices

Test initiation is dependent upon the GRTS direct access log-on procedure for each remote device. While test initiation is originated from the device to be tested, COLTS does not honor the call unless the operator has previously specified a console to be used for testing control and output device.

TEST CRMTx

where:

RMT	= Controlling remote entry
x	= Logical DATANET number from which to expect remote device test calls

VIP Direct Access Log-On Procedure

$*$id PASSWD,xx,.MCOLT

where:

id	= Any two-letter ID
xx	= Terminal type
.MCOLT	= COLTS testing

Possible terminal types include:

4	= DATANET 760, 4 lines
8	= DATANET 760, 8 lines
16	= DATANET 760, 16 lines
26	= DATANET 760, 26 lines
22	= VIP 765/775, 22 lines
22L	= VIP 785, 22 lines (92 characters)
12	= VIP 7700, 12 lines
22N	= VIP 7700, 22 lines
24	= VIP 7700, 24 lines

TTY Direct Access Log-On Procedure

If the TTY line is configured in NPS Startup as a TSS Line, it is necessary to do a logical disconnect and a logical connect to NPS to change line status to a direct access to a direct access (DAC) line.

- If TSS line: Press "CTL C" keys. Wait for host disconnect message. Press "CTL A" keys. Continue as DAC line.
- If DAC line: NPS outputs program name. User types program name,. MCOLT.

When COLTS honors a Test request from a remote device, it is still necessary to ask the operator at the controlling console (the input console of TEST CRMTn) if testing should be started for each new test request.

***REMOTE ID xx(yyyy)zzz REQUESTS COLTS TESTING, TEST? (YES OR NO)

where:

xx	= NPS DAC ID assigned
yyy	= Octal value of the NPS ID
zzz	= Hardware identifier mnemonic

The operator must respond YES or NO. YES starts device testing; NO disconnects the remote device.

For device testing the operator is asked for any initial options desired by an Enter Options message before testing is begun.

The exact DAC log-on procedure for each remote device for test initiation is outlined in the appropriate test page documentation.

NON-KEYBOARD TYPE DEVICES

RC/RLP Devices Only

TEST Cxccssvoooo

where:

x	= Logical DATANET number (0, 1, 2, or 3)
cc	= DATANET IOM channel number in decimal (6, 7, or 8)
ss	= Subchannel number in decimal (00-31)
v	= Device test wanted
oooo	= Option characters or a control mnemonic

RLPs are private line devices connected to a dedicated HMLC subchannel. Therefore, a test request specifying that subchannel with the "v" option starts the test.

Remote computers may be configured as private line or dial line. If dial line, the user must know which HMLC subchannel is being called in order to make the remote connection.

Test Initiation Procedure

1. Load RC with normal NPS operational deck.
2. Dial into DATANET HMLC subchannel.
3. Place printer in OPERATE.
4. Initiate TEST call from control console. A logical disconnect will be made at test completion.

TEST COMMUNICATION REQUEST

To communicate with a test, follow the executive designator (C) with the O character followed by the test and the communications desired.

CHANNEL OR REMOTE DEVICE TEST

TEST COxccssoooo

where:

oooo = New options or control mnemonic (use the option O if you want to interrupt the test).

TEST END REQUEST

To terminate an active test, follow the executive designator with the character E followed by the test.

CHANNEL OR REMOTE DEVICE TEST

TEST CEnccss

STANDARD TEST OPTIONS

The following error control options are the same for all COLTS tests and can be entered in response to an Enter Options message or designated in the options string of a new test request.

A — Accumulate the error messages on the statistical collection file; Test Start and Term messages unconditionally go there.

B — By-pass error message output. By-pass overrides a Pass or Cycle message unless Halt is set; Halt forces these messages out over By-pass.

H — Halt for input of options following error messages, Test End messages, Pass End messages, and Cycle End messages.

I — Inform operator of each normal Test End. If H is also set then an Enter Options is apended to the End Test message. If the next segment is being called, if an End Pass message is being output, or if a cycle ends, the End Test message is overridden.

L — Loop on current test (cannot loop on test 0).

N — Negate the following option character (valid preceding A-B-E-H-I-L-P-R-T options only).

O — Go to Enter Options following processing of the complete option string containing the O.

P — Issue an End Pass message any time a back jump is detected by next test sequencing. If H is also set then an Enter Options is appended to the End Pass message. The error tallies for the current pass are reset when End Pass or End Cycle is reported or when P is being turned ON.

R — Issue an End Cycle message any time a normal test page termination would occur and cycle back to the first test in the current sequence again. If H is also set then an Enter Options is appended to the End Cycle message. The error tallies for both the current pass and current cycle are reset when End Cycle is reported. The error tallies for the cycle are reset whenever R is being turned ON.

S — Unconditionally skip to the next test.

T — If turn ON (no preceding N), then unconditionally jump to the first occurrence of the test in the current sequence; the test number must follow and must be nonzero, and can consist of 1, 2, or 3 digits. For segmented tests, a value outside of the current segment causes a jump to the corresponding segment without further processing of the current option string. If turn OFF (NTxx) then the test number must be in the current segment and sequence and not the forced term test number.

V — Specifies device test instead of subchannel test. Can be used only on initial TEST call and must be the first character following subchannel number. Not used for Communication request.

A control mnemonic follows (see "Control Mnemonics") and is valid only if it is the first character in the string.

SPECIAL TEST OPTIONS

The following options are valid only in a Test End or Test Communication request (not in response to Enter Options) and only when they are the first character(s). These options were implemented to allow ending and communicating with multiple-called (either deliberately or accidentally) test pages for the same device. The test page number (or queue designator) is found as the third character (x) of the standard header which is output with every message for that page and also in the LSTAL messages [**(nccss)id].

0-7 — The command applies only to active tests 0-7 and only if the rest of the header matches. The character is deleted before passing the rest of the string to the option processor.

QA-QP — The command applies only to queued test A-P and only if the rest of the header matches. The characters are deleted before passing the rest of the string to the option processor.

COMMON CONTROL MNEMONICS

The following control mnemonics (.OPTIONS) are processed only if found at the beginning of the option string:

.GO — Return to the test page where interrupted. If S or Txx, or .RSEQ or .SEQT has been specified, the next test sequencing will be performed.

.OPT — An Enter Options message is output.

.PR2 — Future test page error messages will be output on dedicated printer PR2.

.PRT — Future test page error messages will be output on an allocated printer.

.RSEQ — Resequence tests to their initial (at page call) order.

.SEQT — Sequence tests in special order; a message is output:
**X(header) INPUT UP TO zz TEST #'S FROM xxx to yyy IN THE SEQUENCE DESIRED

where:

**x(header)	=	Test page header
zz	=	Number of tests allowed
xxx	=	Lowest test number allowed
yyyy	=	Highest test number allowed

Test numbers are intput in the sequence desired separated by commas. A "-" in front of a test number indicates a jump either forward or backward to the first occurrence of that test number in the new sequence, i.e., 1, 2, 3, 4, -1 indicates running tests in the sequence 1, 2, 3, 4, 1, etc., with a back jump indicated at test 4 (affects the Pass option).

.TAL — A message with a tally of errors in output. P or R must be set and the message includes the information for the current pass or cycle or both depending on the state of P or R or both. The error tallies are reset for the pass cycle or both when reported.

.TEST E — The test page is force terminated.

.TEST W — COLTS is wrapped up.

.TYP — Future test page error messages will be output on the console again.

.WAIT — The test page is put in a Wait condition.

SPECIAL CONTROL MNEMONICS

If a control mnemonic cannot be recognized by the COLTS Executive, the mnemonic will be passed to the indicated Test for processing. If not recognized by the Test, an Invalid Input message will result.

The following control mnemonics are valid for HMLC tests:

.ELOOP — Loop on subtest in error.

.NELOOP — Turn off above option.

.SLOOPxx — Restart current test and loop on subtest xx.

.NSLOOP — Turn OFF above option.

The following control mnemonics are valid for test page HSLA only:

.ASYNC — Configure and test a general prupose subchannel as an asynchronous subchannel.

.SYNCH — Configure and test a general purpose subchannel as a TLPK synchronous subchannel.

.GP — Resets the two options above.

NOTIFYING THE RESPONSE CENTER

To request assistance when a problem cannot be isolated or corrected, call the Honeywell Response Center and supply the following information:

1. Your name
2. Company name and address
3. Your telephone number and extension
4. Type of machine (Series 60 Level 66 or 68 system)
5. DATANET Model
6. System number
7. Symptom of malfunction

Note:

When FED returns your initial call, report the symptom in detail, including which T&Ds were run and their results (console messages, register contents recorded, etc.).

Appendix A
System Configuration Form

This information is to be filled in by Honeywell FED at installation time and referenced when notifying the Response Center.

COMPANY NAME AND ADDRESS: _____

_____

_____

TELEPHONE NUMBER AND EXTENSION: _____

TYPE OF MACHINE: SERIES 60 LEVEL ____ SYSTEM

DATANET MARKETING IDENTIFIER: _____

SYSTEM NUMBER: _____

SYSTEM OPTIONS:

Quantity	*Option Number*	*Description*
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____

COMMUNICATIONS OPTIONS:

Quantity	*Option Number*	*Description*

HMLCs:

HMLC #: _____ (e.g.,00) Channel #: _____ (e.g., 06) Board Slot #: _____ (e.g., 7)

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Subchannel #: _____ (e.g., 01)

Subchannel Type: _____ (e.g., TTY Dual Asynchronous)

T&Ds: _____ (e.g., H6)

Comments: _____ (e.g., TTY 110-300 Baud)

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

HMLC #: _____ Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

HMLC #: _____ Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

HMLC #: _____ Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

Subchannel #: _____

Subchannel Type: _____

T&Ds: _____

Comments: _____

UNIT: _____ (e.g., Direct Interface Adapter)

Channel #: _____ (e.g., 04) Board Slot #: _____ (e.g., 6)

Applicable T&Ds and Run Time: _____

T&D Parameters: _____ (e.g., 0454)

Comments: _____ (e.g., Connects to IOM #2 CH #7)

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

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Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

UNIT: _____

Channel #: _____ Board Slot #: _____

Applicable T&Ds and Run Time: _____

T&D Parameters: _____

Comments: _____

Appendix B

Channel Fault Status Bit Definitions

Interpretation of the various bits composing the channel fault status word is provided in Table B-1.

TABLE B-1. CHANNEL FAULT STATUS BIT DEFINITIONS

Bit	Fault
	System Bus Faults
0	Red from MM
1	Illegal function code
2	Upper data bus parity
3	Lower data bus parity
4	Parity error address bits 5-7
5	Illegal NAK on system bus
6	Bus continuity error
7	ROS parity
8	PAT error
9	Channel-specific channel fault
	I/O Bus Faults
10	Illegal function code
11	Upper data bus parity
12	Lower data bus parity
13	Parity error address bits 0-7
14	Illegal NAK
15	Bus continuity error
16-17	11 — IOM detected the fault and originated status word 10 — Channel detected the fault

If the fault status word location is 426,427, or 430 and if the channel detected the fault, the meaning of bits 0-8 is:

Channel #6 Y01000XX0
Channel #7 Y01001XX0
Channel #10 Y01010XX0

Where:

Y = Memory Red Indicator
XX = HMLC # (0-3)

If the I/O fault status word corresponds to the DIA (normally location 424 if the DIA is on channel 4), then the format is the following:

000 000 00U XY0 00Z 100

DIA Detected Fault
- U = OR to storage
- X = OR to storage or write to storage
- Y = Red from MM
- Z = Error damage report (IOM detected fault)

Appendix C
Programming Considerations

The purpose of this appendix is to point out the differences between the DN6600 (DN355/DN6616-24-32) and the DN66 that require special programming attention.

CPU-I/O CONFLICT ON DN66

If an I/O device is updating a word or word pair at the same time that software is accessing (reading or writing) the same word or word pair, the resultant data may be incorrect. This is particularly true if the cache is installed. Programmers should ensure that software is not accessing the same memory word(s) at the same time as an I/O device.

INSTRUCTION COUNTER DURING FAULTS

When the DN66 has a fault, IC +1 is saved if the fault is divide check, overflow, or illegal op code. For other faults, IC + 0 to IC + 3 could be saved and, if non-interruptable instructions follow the fault, IC would be incremented more.

NEW INSTRUCTIONS

The DN66 has some new instructions that are generally used for T&Ds but could be helpful for debug purposes.

DN66 T&D INSTRUCTIONS

Special T&D instructions are provided to aid in resolving failures in the processor or in other components. The instructions are:

- CAQC — Copy AQ to Channel (533200_8)
- CCQ — Copy Channel to Q (533300_8)
- CRA — Copy Register to A ($7332XX_8$)
- CAR — Copy A to Register ($1332XX_8$)

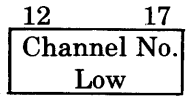
The CAQC and CCQ allow T&D access to registers and control in components which are completely external to the processor (e.g., the IOM, Page Common Logic Unit, I/O channels). The definitions of these T&D orders are contained in the appropriate component specification manuals.

CAQC – COPY ACCUMULATOR AND QUOTIENT TO CHANNEL 533200_8

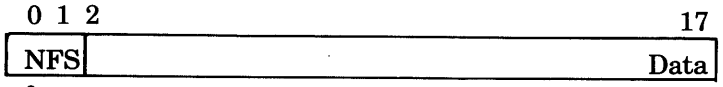
SUMMARY

Data and control information are delivered to the controller, which is connected to the channel specified by the SEL register and bits 8 through 11 of the A register. The software visible format is shown as follows:

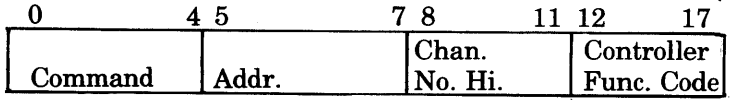
SEL:



Q:



A:



Note:

The K field (Y_{12-17}) must be octal 00.

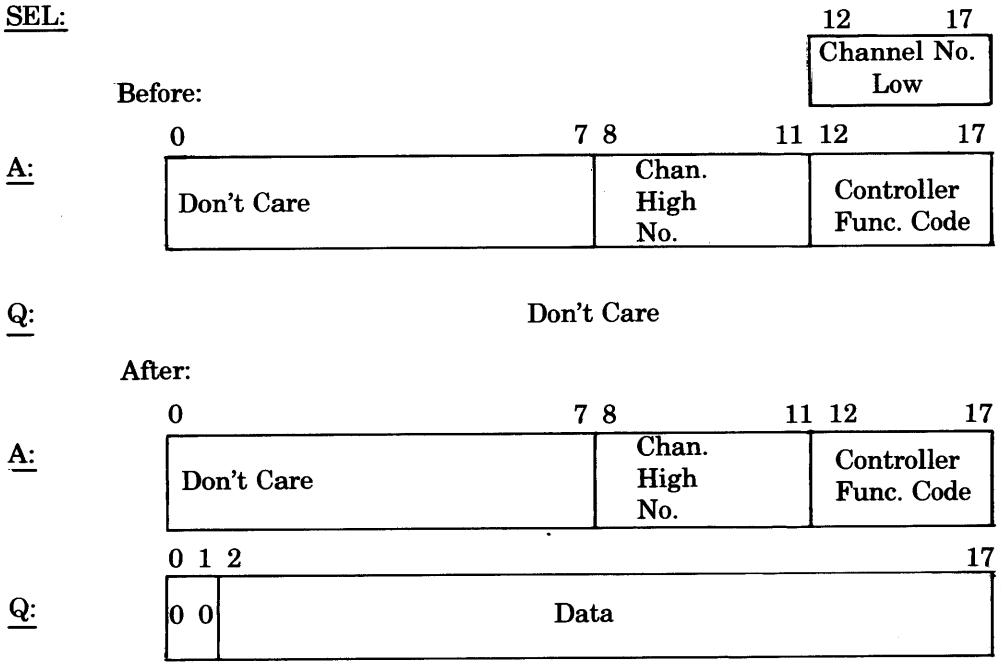
INDICATORS

The indicators are not affected.

CCQ – COPY CHANNEL TO QUOTIENT (533300_8)

SUMMARY

Control information is delivered from the accumulator to the controller, which is connected to the channel specified by the SEL register and bits 8 through 11 of the accumulator. Then, 16 bits of data are returned to the quotient register. The software visible formats before and after the instruction are shown as follows:



Note:

The K field (Y_{12-17}) must be octal 00.

INDICATORS

The indicators are not affected.

CRA – COPY REGISTER TO A ($7332XX_8$)

CAR – COPY A TO REGISTER ($1332XX_8$)

SUMMARY

The CRA and CAR instructions allow Test and Diagnostic (T&D) access to registers and control associated with the CPU, including the Page Address Table Unit (PATU) and the Cache Memory Unit. The K field of the instruction word (i.e., the six low-order bits) specifies the register or function. The K field values are assigned as follows:

- Octal 0xxxxx — CPU
- Octal 10xxxx — PATU
- Octal 11xxxx — Cache Memory Unit

The PATU and Cache CRA/CAR orders (i.e., K field assignments) are defined in their specific option manual. A list is included here.

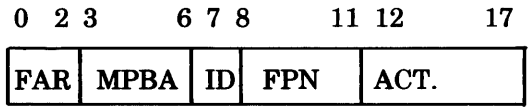
The CPU CRA/CAR orders (i.e., K field assignments) are defined as follows:

CRA K Field (Octal)	Register/Function
00	Processor Number, AR = CP's ID (bit7)
01	Panel Register, AR = Panel Data
02	Hardware QR, AR = (QR) live
03	Hardware ICR, AR = (ICR) live
04	*Combination Register, AR = contents Comb. Reg.
05	Read Sys. Bus, AR = Addr. Bus & QR = Read Data Bus LSB of F.C. = "0".
06-57	RFU
60	Load Cache
61	Store Cache

CAR K Field (Octal)	Register/Function
00	RFU
01	Panel Register, AR = Panel Data
02	Put CP in Stop Mode
03	Panel Register Data to AR and Stop
04	Write Sys. Bus, AR = Addr. Bus & QR = Write Data Bus LSB of F.C. = "1".
05-57	RFU

CAR K Field (Octal)	Register/Function
60	Initialize Cache (Will leave Cache in offline Mode)
61	Cache Off
62	Cache On
63	Set Hit Fault Mode
64	Reset Hit Fault Mode
65	RFU
66	Disable Timers
67	Enable Timers

*The layout of the Combination Register is:



where:

FAR = Fractional Address Register
MPBA = Microprogram Branch Analysis
ID = Processor Identification
FPN = Fault Priority Net
ACT = Activity Counter

PAGE ADDRESS TABLE UPDATE

The page address tables in the DN66 can be updated by single word updates only; double word upates such as STAQ do not work.

PIA BASE ADDRESS

When configuring a PIA on the DN66, the software must specify a base address of Modulo 32 for the hardware communication region.

PIA TRANSFER TIMING ERRORS

The PIA on the DN66 can get Transfer Timing Errors (TTEs) if a large number of short records are being journalized on disk.

Note:

Paper tape mode is automatically journalized.

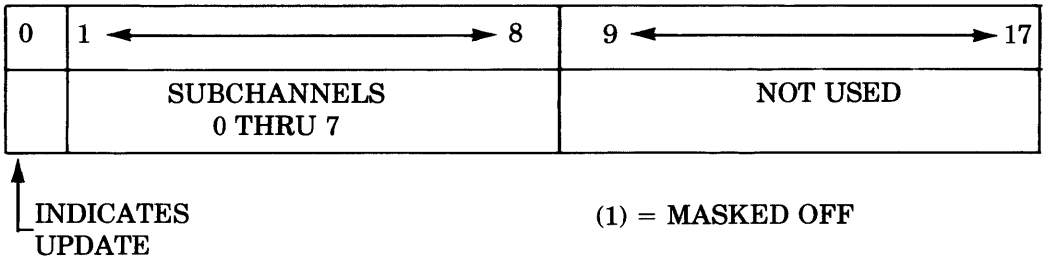
ABSOLUTE ADDRESSING

The DN66 has provision for absolute addressing of upper memory (32K to 256K) for I/O channels only. This capability can be achieved from the HDIA, HPIA, HMLC and the console channel.

- To accomplish absolute addressing with the HPIA, the three-bit character addressing tags cannot be used with the LPWs and DCWs, thus giving a full 18-bit address field. Bit 18 of the PCW must now be set to indicate that all 18 bits are valid as an absolute address.
- To accomplish absolute addressing with the HDIA, the three-bit character addressing tags normally in bits 0-2 of the DN66 DCW are not used, thus giving a full 18-bit address field in word zero. Bit 18 of the DN66 DCW (bit 0 of word 1 of the DN66 DCW) must be set to a "1" to indicate unpaged mode and that the 18-bit address field contains an absolute address.
- To accomplish absolute addressing with the HMLC or console channel, the three-bit character address must be placed in bits 20-22 of the ICW (bits 2-4 of word 1 of the ICW) thus allowing a full 18-bit addressing field in word 0. Bit 18 of the ICW (Bit 1 of word 1 of the ICW) must be set to "1" to indicate all 18 bits are valid as an absolute address.

STORE MASK REGISTER

The DN66 stores mask registers on a per-HMLC basis (8 subchannels per group) in locations X012, X212, X412, X612, where X=1 for channel #6, 2 for channel #7, and 3 for channel #10, and the format is as follows:



INITIALIZING HMLC

Each HMLC has to be initialized separately by issuing a PCW to the first subchannel on the HMLC.

OPTIONAL ASYNC BAUD RATES AND EUROPEAN BAUD RATES

The standardized ASYNC baud rates are supported the same on both the DN66 and DN6600 as follows:

PCW 2

Bits 28	29	30	31	32	33	34	35	Speed (Baud Rate)
1	0	0	0	0	0	0	0	110
0	1	0	0	0	0	0	0	134.5
0	0	1	0	0	0	0	0	150
0	0	0	1	0	0	0	0	300
0	0	0	0	1	0	0	0	1050
0	0	0	0	0	1	0	0	1200
0	0	0	0	0	0	1	0	1800

On the DN66, the optional ASYNC baud rates and the European baud rates are supported as follows:

Bits (PCW2)								Speed (bps)
28	29	30	31	32	33	34	35	
0	0	0	0	0	0	0	1	50
0	0	0	1	0	0	0	1	75
0	0	1	0	0	0	0	1	110
0	0	1	1	0	0	0	1	134.5
0	1	0	0	0	0	0	1	150
0	1	0	1	0	0	0	1	200
0	1	1	0	0	0	0	1	300
0	1	1	1	1	0	0	1	600
1	0	0	0	0	0	0	1	1050
1	0	0	1	0	0	0	1	1200
1	0	1	0	0	0	0	1	1800
1	0	1	1	0	0	0	1	2000
1	1	0	0	0	0	0	1	2400
1	1	0	1	0	0	0	1	4800
1	1	1	0	0	0	0	1	9600
1	1	1	1	0	0	0	1	

PARITY GENERATION FOR COMMUNICATION SUBCHANNELS

The DN66 generates parity on all eight bits in a character buffer. Therefore, if character parity is carried internally in the machine, the parity bit should be "ANDed" to zero to ensure that any bits which are not data are zero in a character before being given to the hardware for transmission.

CURRENT LOOP ADAPTER

The Current Loop Adapter Board, BMLFCLAA, available in four-wire mode only, keeps the ring signal on at all times.

BREAK FROM ASYNC TERMINALS

When a line break request is received from an ASYNC terminal, its status is stored (bit 25). This is normal; however, if the break is still in progress (key still depressed), and a Request Status command is issued, break status will not be stored. Software should delay before responding to the break, but there is no guarantee that the break has stopped since it is dependent upon the type of terminal and the length of time the BREAK key is held down.

LAST COMMUNICATIONS CHARACTER TRANSMISSION

After the last character has been read from memory, software usually issues a PCW to turn off RTS. The hardware may be transmitting the last character when it receives the command to turn off RTS. The hardware does not delay, but turns off RTS immediately. If the terminal is in direct connect mode and gates on RTS, it might not recognize the last character transmitted.

SUBCHANNEL ID CODES

The DN66 stores the subchannel ID code in bits 2-8 of the configuration status. Figure C-1 identifies the I/D codes for the various subchannel options.

AUTO BAUD DETECTION (134.5 BAUD)

The DN66 uses a different timing chip which causes the automatic baud detection feature for 134.5-baud terminals to use a different algorithm.

Mkt. Option No. For:	Mkt. Option No. For:	IPI No.	Board Type	Board Size	ID Code	No. of CHs	Async Sync	Baud Rate	Comments
CPS6058*	DCP6616	—	—	—	—	—	—	—	—
CPS6650*	DCP6624	—	—	—	—	—	—	—	—
CPS8802*	DCP6632	—	—	—	—	—	—	—	—
DCU6641	—	—	—	—	—	—	—	—	—
DCU6651	—	—	—	—	—	—	—	—	—
DCP6678	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—
DCF6610	DCF6011	BMLFCLAA	BD2CLA	1/4	42	2	A	9600	20/60 MA
DCF6611	DCF6013, 6014, 6060	BMLF103A	BD2LAS	1/4	53	2	S	9600	EIA
DCF6612	DCF6010	BMLF101B	BD2ASC	1/4	43	2	A	9600	EIA
DCF6613	DCF6014, 6062	BMLFDACA	BD2DAC	1/4	64	2	—	10	ACU
DCF6614	DCF6012, 6053	BMLF188A	BD2188	1/4	54	1	S	9600	MIL188
DCF6615	DCF6039	BMLFA88A	BD2A88	1/4	40	2	A	9600	MIL188
DCF6616	—	—	—	—	—	—	—	—	—
DCF6616	DCF6048	BMLF616A	BD2B8D	1/4	51	1	S	72000	MIL188BB
DCF6617	DCF6050	BMLFH88A	BD2H88	1/4	—	1	S	9600	MIL188 HDLC
DCF6618	—	BMLF103A	BD2LAS	Replaced by BMLF618A		—	—	—	—
DCF6618	DCF6015, 6062	BMLF618A	BD2LAS	1/4	52	2	S	9600	BSC
DCF6619/21	DCF6016, 6055	BMLF619A	BD2CMD	1/4	47/46	1	S	72000	Current Mode/BSC
DCF6619/21	—	BMLFCMSA	BD2CMS	Replaced by BMLF619A		—	—	—	—
DCF6620	DCF6019, 6053	BMLFDLCA	BD2DLC	1/4	50	1	S	9600	EIA HDLC
DCF6622	DCF6054	BMLFDLDA	BH4DLD	1/2	146	1	S	72000	EIA HDLC BB
DCF6623	DCF6058	BMLFDLEA	BH4DLE	1/2	147	1	S	72000	CCITT V.35 HDLC
DCF6627	—	BMLFBLSA	BD2BLS	Replaced by BMLF627A		—	—	—	—
DCF6627	DCF6060	BMLF627A	BD2BLD	1/4	55	2	S	9600	CCITT V. 35 B.B.

*The ID code is stored in configuration status bits 2-8. If subchannel is attached to an ACU, an octal 20 is added to the ID code.

Figure C-1. Subchannel ID Codes

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