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TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
GE-655 COMMON PERIPHERAL CHANNEL

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1.0 GENERAL DESCRIPTION

The IOM Common Peripheral Channel provides interfaces to a Common Peripheral Subsystem and to the GE-655 Input/Output Multiplexor (IOM) Central (see Figure 1.0). This EPS-1 defines the requirements placed on the channel to bring about appropriate interaction between the two interfaces.

The channel receives instructions in a Peripheral Control Word (PCW) from the software, or in an instruction DCW from user programs, and where appropriate, transmits these instructions to the Peripheral Subsystem. The channel interacts with the Peripheral Subsystem and IOM Central to accomplish I/O data and instruction transactions. This will include both the monitoring of the Peripheral Subsystem status and the use of a list of the Data Control Words (DCW's) in core. After initiation through receipt of a PCW, the channel generates the necessary List, Status, Interrupt, and Indirect Data service requests to the IOM Central which are necessary to perform the function of executing the DCW list in core.

A description of a typical sequence of such services by the IOM Central and a Common Peripheral Channel follows in Section 2.3.

In the remainder of this EPS, the assumption is made that the reader understands the various services performed by IOM Central.

The phrase "IOM" and "IOM Central" are used interchangeably with the same meaning intended.

All references within this specification to GE-655 will apply across the 6000 line.

This specification also defines the requirements for the 6000B Common Peripheral Channel. The 6000 and the 6000B channels are identical except for the 6000B requirement for address extension as noted in Sections 3.3.2 and 3.4.3.

1.1 INTERFACE REQUIREMENTS

The channel operates with the peripheral subsystem in conformance with the Product Performance Specification for Common Peripheral Interface, 43A130524. The GE-655 Common Peripheral Channel shall interface with all GE-615/635 Common Peripheral Subsystems listed in paragraph 2.4 of GE-655 System EPS-1 (43A219600), the CPZ100 card punch subsystem excepted.

The channel operates with IOM Central in conformance with the EPS for the IOM Central referenced in Section 1.5.

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1.2 COMPATIBILITY REQUIREMENTS

The design goal of the Common Peripheral Channel shall be to require no rework of an existing User Program. Insofar as it is possible, the channel will utilize the formats and conventions established for the IOC-C. System software (GECOS) must accommodate any departures from these formats and conventions. Some such departures must be expected in order to utilize the additional features and capabilities of the IOM Central.

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1.3 PACKAGING REQUIREMENTS

It is a requirement that a Common Peripheral Channel reside on no more than two GE-655 (MQX) type circuit boards.

1.4 APPLICABLE DOCUMENTS

Common Peripheral Interface Specification - 43A130524
IOM Central Engineering Product Specification, I - 43A219604
IOC-C Engineering Product Specification, I - M50EB00163
6000B IOM Engineering Product Specification, I - 43A239854.

1.5 DEFINITIONS

- (a) Conclusion (of peripheral operation): An End-Data-Transfer is sent to a peripheral which is operating in a Busy status condition, in accordance with the procedure in the Common Peripheral Interface specification. Peripheral operation is brought to an orderly halt. If the channel is not masked, a Terminate status will be stored when the peripheral indicates that the operation has terminated.
- (b) Abort: Any situation indicating improper operation, such as a fault during List service, which arises during a Common Peripheral Instruction sequence prior to the Release pulse, will cause an Abort condition as defined in the Common Peripheral Interface Specification. If the abort occurs as a result of a user fault, a terminate status will be stored.
- (c) Channel Busy: Receipt of a Peripheral Control Word (PCW) with valid codes in all its fields, when the channel is not busy, will place the channel in a busy condition. The channel will remain busy until all action with the peripheral device named in the PCW has terminated or concluded, including any appropriate status responses.
- (d) Peripheral Busy: A Common peripheral is considered busy anytime the major status Busy line is true, regardless of the state of the other major status lines.

2.0 FUNCTIONAL CAPABILITIES

2.1 TRANSFER RATES

The Common Peripheral Channel must be capable of operating at speeds consistent with the IOM and the common peripherals. The required maximum data rate for Common Peripheral Channels is 650,000 characters (6 bits) per second with the peripherals, or 108,000 words (36 bits) per second with the IOM Central. To achieve this, the peripheral must have a maximum turnaround time of 400 nanoseconds.

2.2 BUFFERING

Each Common Peripheral Channel will be capable of transferring and buffering two 36-bit words per access to the IOM Central, and provide two additional such words of buffering for character/word assembly and disassembly.

2.3 DESCRIPTION OF OPERATION

The following is a description of a typical operation of IOM Central and a Common Peripheral Channel. Exceptions to this description arise at many places but discussion of these are held for the detailed description further into the EPS.

For the 6000B channel only it should be noted that the channel is required to store the address extension as presented by the IOM in the PCW or the IDCW where applicable. The channel will return the address extension on the D Bus (Ref: 6000B IOM EPS-1) when requesting service from the IOM. The formats for address extension are listed in Sections 3.3.2 and 3.4.3.

The software must prepare several control words, in addition to a buffer area for data to be transferred. Data Control Words indicating the locations of each data area must be placed in a DCW list. A List Pointer Word (LPW) indicating the location of the DCW list must then be placed in the core LPW mailbox for the channel to be used.

For the purpose of this discussion, assume that channel 010₈, the lowest-numbered payload channel, is to be issued an instruction to transfer data (Write) to the peripheral attached to its interface. A Status Control Word placed in the same channels SCW mailbox area points to an area of core set aside to receive the status words resulting from the peripheral instructions to be issued. A Peripheral Control Word containing the necessary channel and peripheral instruction codes is placed in another area of core, with a second word containing the channel number (010) of our channel under discussion. The LPW mailbox for the connect channel is provided with a pointer to a list of such PCW's, allowing several payload channels to be initiated with a single connect instruction. As described later, the entire mailbox area is a contiguous block of words, four per channel, relocatable by means of switches on the IOM Configuration Panel.

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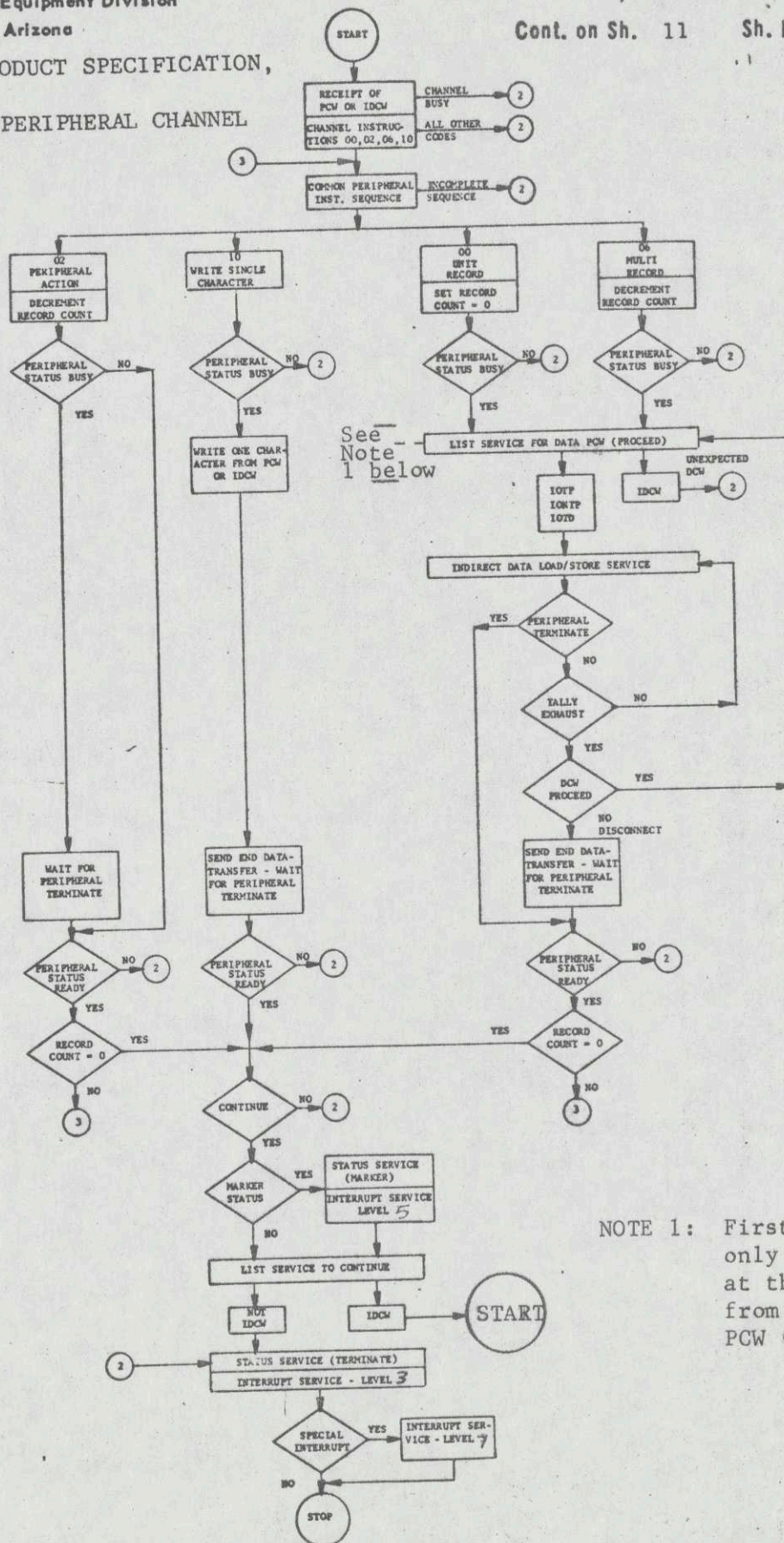
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3.2 DCW LIST



NOTE 1: First list only if arrived at this point from START and PCW (not IDCW).

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3.3.2 PCW Format

The Peripheral Control Word (PCW) and the Instruction DCW (IDCW) both use the same format. The PCW is distinguished by being obtained as the end result of a connect; the IDCW has been conceived to allow the software and unrestricted user programs to place instructions for peripheral devices at appropriate places in a DCW list accessed only by List Services. Any distinction in interpretation of the fields is given in the description of that field.

0	5,6	11,12	17,18	20,21,22,23,24	29,30	35
DEVICE INSTRUC- TION	DEVICE ADDRESS	ADDRESS EXTENSION *	111	M A S K C O N T M A R K	CHANNEL INSTRUC- TION	CHAR. OR RECORD TALLY

The interpretation of these fields is as follows:

Device Instruction (Op Code) (bits 0-5) - This instruction is transmitted directly to the peripheral during the instruction sequence, whether from a PCW or an IDCW. On multiple record and peripheral action type channel instructions, this field is retransmitted to the peripheral. This field is interpreted by the channel to the extent necessary to determine whether a READ or a WRITE operation is to take place.

Device Address (Device Code) (bits 6-11) - This code is transmitted directly to the peripheral during the instruction sequence and is not interpreted by the channel. This field is stored in the channel only from a PCW. This field is reused by subsequent IDCW's but never changed by them. This will make it impossible for a slave program to switch devices within a DCW list.

Address Extension* (bits 12-17) - This field contains the 6-bit address extension which will be stored by the channel for subsequent use by the IOM in preparing a 24-bit address for the 6000B.

Bits 18-20 must be 111 to identify the PCW and distinguish the IDCW from other Data Control Words.

Mask (bit 21) - This bit is ignored in an IDCW. When set to zero in a PCW, the channel responds normally. When set to one in a PCW, the channel will conclude any current peripheral operation, and will cease all communication with IOM Central until a PCW with bit 21=0 is received.

*Applies to 6000B only. This field in 6000 must be zero.

3.4.2 Data Service (Continued)

The channel shall interpret the output data and input data as shown below during the data cycle. A 72-bit transfer will be two successive 36-bit transfers. The character position codes for the 6-bit characters are shown.

36-Bit Data Transfer

0							35
M S B	000	001	010	011	100	101	L S B

Not shown are data formats for nonzero character positions in the initial DCW and for the "early" terminate condition. Specifically, during Read operations, software will see leading zeros in the unused character positions (if the initial DCW has a nonzero CP field) or will see trailing zeros in the unused character positions (if the peripheral terminates before six characters of a word are buffered). The important point to realize is that the IOM will not store partial words in core!

3.4.3 List Service to Continue

The channel will request IOM Central to do a List Service for the purpose of obtaining an Instruction DCW under the following conditions:

- (1) The channel has had a previous PCW or IDCW which indicated the DCW list should continue, and
- (2) The record count indicated in that PCW or IDCW has been reduced to zero, and
- (3) If the preceding instruction was a record transfer DCW, then the preceding DCW was an IOTD, and its tally has exhausted, and
- (4) The peripheral previously in use has terminated with a Ready status, and
- (5) Any marker status called for has been stored, and the corresponding interrupt used.

Since the IOM Central intercepts Transfer DCW's, any DCW sent to the channel at this time which is not an IDCW will cause a Termination with a "User Fault: Incorrect DCW" status.

The format of the IDCW is basically the same as the PCW, except that some fields are ignored.

0	5,6	11,12	17,18	20,21,22,23,24	29,30	35	
DEVICE INSTRUC- TION	IGNORED	ADDRESS EXTEN- SION*	111	E C*	C O N T M A R K	CHANNEL INSTRUC- TION	RECORD TALLY OR CHARACTER

*Applies to 6000B only. These fields in 6000 must be zero.

3.4.3 List Service to Continue (Continued)

The interpretation of these fields is as follows:

Device Instruction (Op Code) (bits 0-5) - This instruction is transmitted directly to the peripheral during the instruction sequence, whether from a PCW or an IDCW. On multiple record and peripheral action type channel instructions, this field is retransmitted.

Ignored (bits 6-11) - The channel must retain the device code or address from the PCW, and ignore this field in an IDCW. Similarly, only a PCW may mask a channel's operation. This will make it impossible for a slave program operating under GECOS to switch devices within a DCW list, or to prevent storing status and causing an interrupt.

Address Extension* (bits 12-17) - This field represents a new address extension with which the channel will replace the present address extension depending on the state of EC (Bit 21).

Bits 18-20 must be 111 to distinguish an IDCW from other Data Control Words.

EC* (bit 21) - This bit indicates whether or not the channel will replace the present address extension with the new address extension as given in Bits 12-17. If EC = 1 the new address extension will apply. If EC = 0 the old address extension will be unaltered.

Bits 22-35 are interpreted the same as in the PCW, and are described in Section 3.3.2.

3.4.4 Status Service (Termination)

Termination status is stored by requesting a Status Service and presenting the IOM Central the status word in the format shown below. As described in the chart in Section 3.2, Termination status is stored whenever any User Fault or peripheral status of not-busy and not-ready occurs, or whenever a PCW or IDCW is terminated which does not indicate that continuation of the DCW list is desired. Terminate Status storage must always be followed by an Interrupt service request, level 3.

Common Peripheral Channels will return the character position residue and a Read/Write indication to the IOM as part of the Service Request to IOM Central. The CP residue is the character number into which or from which the next data character would have been transmitted if the transaction had continued. The channels will always transfer 36-bit words, but will indicate the last actual character +1 as the character position residue. The channel will similarly indicate whether the next transfer would have been a Read or a Write operation, by indicating a one for a Read.

*Applies to 600B only. These fields in 6000 must be zero.

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3.4.4 Status Service (Termination) (Continued)

The channel must recognize user faults reported to it by IOM Central, and store this together with Peripheral subsystem status, as shown in the description of the status word as follows:

0, 1, 2		5, 6	11, 12	15, 16, 17, 18		23, 24	29, 30	35	
T	P	MAJOR STATUS	SUBSTATUS	SOFTWARE STATUS	I	A	IOM/CHAN. STATUS	MBZ	RECORD RESIDUE

The status word format generated by the channels is compatible with the IOC-C format. The content of the IOM/Chan. Status field is encoded differently. The fields have the following definitions:

Entry Present Bit (0) - Stored as a one by the channel hardware; software presently resets this bit to zero to indicate that the status has been examined.

Power Bit (1) - A one if peripheral does not have its power on, or if there is no peripheral attached.

Major Status (2-5) - The major status from the peripheral. Zero when the power bit is one.

Substatus (6-11) - The substatus from the peripheral. Zero when the power bit is one.

Software Status (12-15) - Stored as zero by channel hardware; is presently used by GECOS to indicate software detected errors to the slave program after the hardware has stored the status word.

* Initiation Interrupt (16) - A one if the Peripheral Subsystem did not go busy as a result of this instruction; i.e., this status occurred during an instruction sequence.

Abort Bit (17) - Stored as zero by channel hardware. It is set to one by software if this transaction caused the program to be aborted.

IOM/Channel Status (18-23) - The IOM Status field is divided into 2 independent 3-bit segments: bits 18-20 represent channel detected User Faults and bits 21-23 represent IOM Central detected User Faults reported to the channel. The faults and their codes are described in Section 3.6.

*NOTE: Present hardware implementation sets this bit to zero as a result of a terminate from the peripheral; thus, a one remains if power off occurs during data transfer.

3.4.4 Status Service (Termination) (Continued)

MBZ (24-29) - Unused at present; must be zero (MBZ).

Record Count Residue (30-35) - Residue record count for a peripheral action or multiple record instruction; stored as zero in all other cases. The record count shall be decremented each time the instruction is issued or reissued to the peripheral whether the instruction is accepted or rejected by the peripheral. (For example, a backspace record of 5 issued 3 records off of load point will cause the count to be decremented once for each of the three records and then once when the instruction is issued at load point and rejected. Thus, the record count residue will be 1 when status is stored.)

3.4.5 Status Service (Marker)

The Marker Status is stored by requesting a Status Service, using the same status word format as used in a termination status. Marker Status is stored only when no user or system faults have occurred, the peripheral has terminated with a Ready status, the record count in the PCW/IDCW has been exhausted, and the PCW or IDCW indicated both marker status storage and list continuation. Marker status storage is followed by Program Interrupt, level 5.

3.4.6 Program Interrupt Service

The Common Peripheral Channel is restricted to use of three of the eight levels available in IOM Central. These levels are specified as part of the Interrupt Service request, and are:

- (1) Level 3: Terminate Interrupt
- (2) Level 5: Marker Interrupt
- (3) Level 7: Special Interrupt

Terminate and marker interrupts always follow the respective status storage. A special interrupt may be received from the peripheral subsystem at any time. If the channel is not masked and is not busy, the Interrupt service for special interrupt will be requested immediately; however, the channel must not declare itself busy to do so. If the channel is not masked and is busy, the Interrupt service for special interrupt is requested after the next marker or terminate interrupt. There is no associated status storage with a special interrupt request.

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3.6 USER FAULTS

User faults are defined as faults caused by user or slave programs operating under GECOS. Because of their nature or timing relationship, certain hardware malfunctions also must be reported as user faults.

The Common Peripheral Channel must recognize the user fault indications from the IOM and those detected by the channel, and on their occurrence must conclude any peripheral operation in progress, leaving the channel unmasked. The channel must go through its normal termination procedure; i.e., store status with the appropriate user fault code and program interrupt with a terminate interrupt. Thus, user faults will be indicated in the status queue that is normally used by the Common Peripheral Channel.

3.6.1 IOM Central Detected User Faults

When the IOM Central detects a User Fault, it will indicate a fault and the fault type to the channel at the end of the service. The IOM detected user faults are reported in bits 21-23 of the Status Word. The faults and their codes are as follows:

<u>Code</u> <u>21,22,23</u>	<u>Fault</u>
000	None
001	LPW tally run-out (not connect channel)
010	2 TDCW's in succession
011	Boundary error
100	Address Extension Change Restricted
101	IDCW in restricted mode
110	Character Position/size discrepancy, list service (detected by Common Peripheral Channel)
111	Parity Error, I/O bus, data from channel

All of the IOM Central detected faults are defined in the IOM Central EPS-1. The Common Peripheral Channel, being a word channel to the IOM Central, must detect a character position code of 110 as being a fault. If no other IOM Central detected fault is indicated, the channel will encode 110 into the Central detected fault field, bits 21-23.