Honeywell

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INFORMATION
SYSTEMS INC.

TITLE: 645X IOM EPS-I
DRAFT

No. 43A219604

REVISION RECORD

REVISION LETTER	DATE	PAGES AFFECTED	APPROVALS	AUTHORITY
0	June 23, 1971	ISSUED		
1	July 21, 1971			
2	July 29, 1971	Changes to definition of LPW 20 and transfer DCW 33 for Extended GECOS mode. Use of an IDCW to change the address extension is dropped.		
3	Aug. 17, 1971	Changes for VMM Mode. Change definition of bounds error for Size = 0. Pages 1-13, 15, & 16		

645X IOM EPS-I (Draft)

NOTE: Until such time that the requirements for the extended address 645X IOM can be incorporated into the existing 655 IOM EPS-I to produce an all inclusive IOM EPS-I, the unique requirements for the 645X IOM will initially be distributed as Appendix B to the 655 IOM EPS-I, 43A219604, Revision E.

Where conflicts exist between the present EPS-I and Appendix B, this appendix shall apply.

TABLE OF CONTENTS

B.1.0 GENERAL

B.1.1 Scope

This appendix shall apply as a performance requirement of the Input/Output Multiplexer when used as a subsystem of the 645 system.

B.1.2 Description

The 645X IOM will have the following characteristics:

- The ability to operate in a GECOS III 655 mode with no Operating System or Slave software programming interface difference over the present IOM design.

- The capability of operating in an Extended GECOS, MULTICS, or VMM mode where addressable memory space to 2^{24} locations is possible.

- The ability to change MODE by a manually operated configuration switch.

- The capability of interfacing up to eight (8) 645X System Controllers. There shall be one three position switch for each pair of ports. The following pairs of ports may be interlaced:

  Ports A and B
  Ports C and D
  Ports E and F
  Ports G and H

The interlace mode may either be two (address bit 22) or four (address bit 21) word blocks.

- Provision for control word scratchpad storage for at least 24 payload channels.

- The ability to indicate with a configuration switch per port, that either all or half of the address range assigned to a memory port is available.

- The ability to support word or 9 bit character channels.

B.1.3 Relationship to 655 IOM

The following variations from the 655 IOM are required for address extension to 2^{24} locations.

- Control word formats and fields will remain as presently defined for the IOM insofar as possible. Certain bit definitions within the fields will be changed where necessary.

- Control word mailboxes, interrupt multiplex words, PCW lists, system fault word lists, and status queues will reside in the first 256K core. DCW lists will also reside in the first 256K core in MULTICS MODE; in Extended GECOS or VMM Mode, IDCW's must reside in the first 256K of core and user DCW's may reside in the same 256K block as the data.

- Transactions which cause addresses to be incremented will not be allowed to occur across modulo 256K (absolute) boundaries. That is, overflow past 2^{18} is not allowed.

- The "address extension" (i.e., the 6 most significant bits of a 24-bit address field) will be obtained from two sources:

1) From bits (12-17) of a PCW directed to a data channel in the Extended GECOS or VMM Mode. This extension will be used for data transfers if DCW 21 = 0 and, depending on LPW 20, may also be used when fetching a DCW during a list service.

Restrictions: None. MULTICS will make this field zero.

2) During a list service from bits 0-5 of a data type DCW, provided DCW 21 = 1 and the address mode is absolute (LPW 23 = 0). In this case, the information from DCW 0-5 will replace the former extension. The IOM Central will then modify the DCW such that it is placed in the 18 bit address field of the DCW mailbox with bits 0-11 of the data address equal to bits 6-17 of the "original" DCW, and bits 12-17 of the data address equal to zero. That is, the IOM Central will strip off the address extension and place a 2^{18} modulo 64 address in the DCW mailbox.

Restrictions: MULTICS or VMM Mode only.

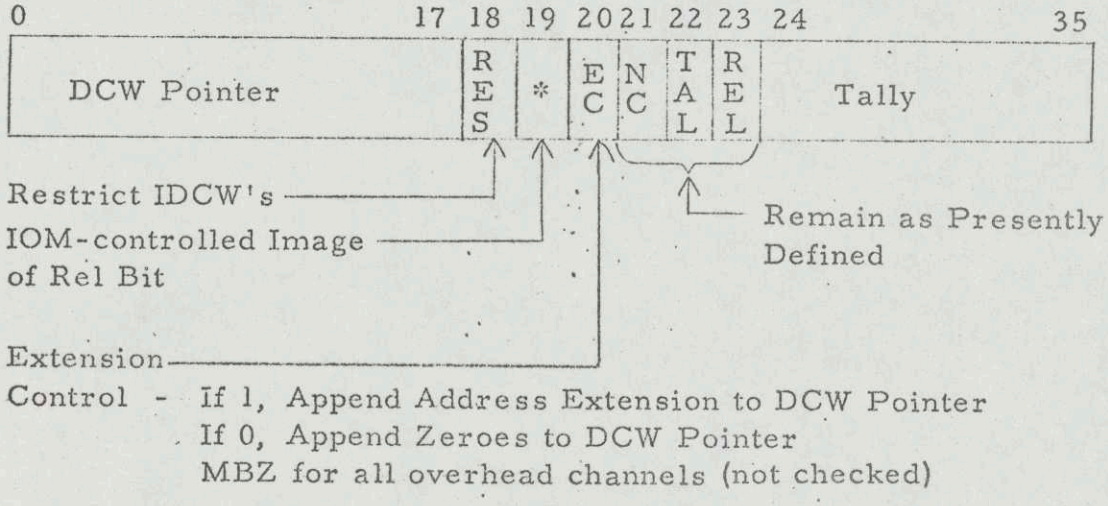
B.2.0 WORD FORMATS

The following control word formats, definitions, and machine actions will allow maximum use of existing IOM organization. The only changes to the existing "non-extended" operation are

the definition of the unused LPW bit 20, redefinition of bit 21 of data type DCW's, and definition of bit 33 of a transfer DCW.

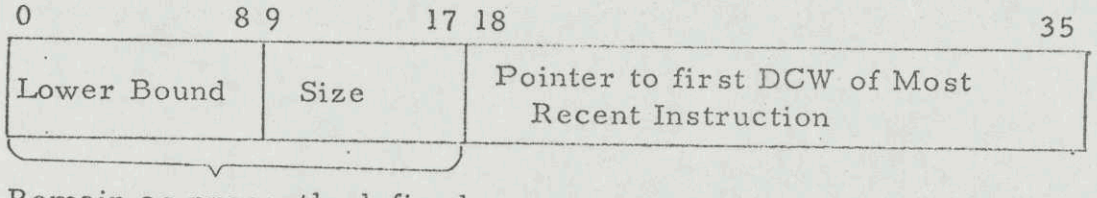
B.2.1 LPW and LPW Extension

Extended GECOS or VMM LPW



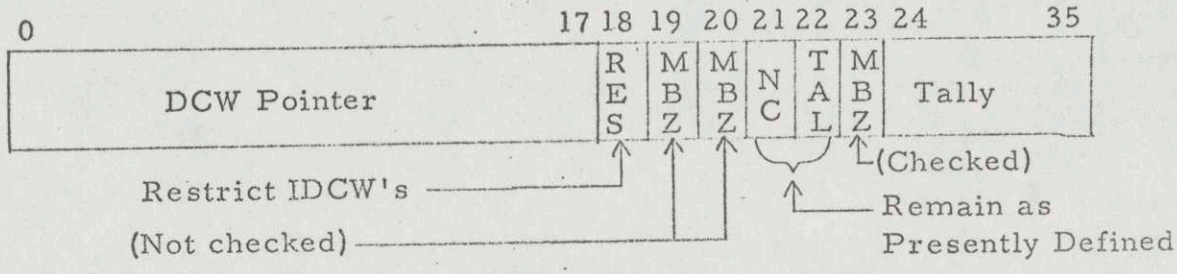
Extension Control - If 1, Append Address Extension to DCW Pointer
If 0, Append Zeroes to DCW Pointer
MBZ for all overhead channels (not checked)

Extended GECOS or VMM LPWX

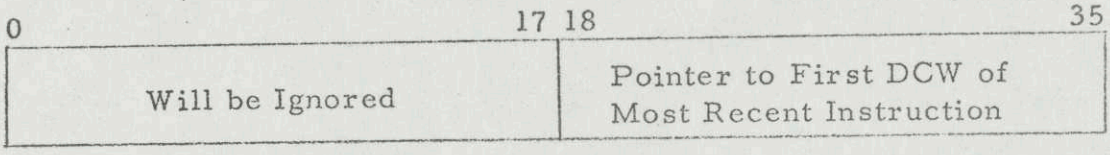


Remain as presently defined, i.e., these are based on 256K and Address Extension is not involved in the Absolutizing Process.

MULTICS LPW



MULTICS LPWX



DCW (or PCW) Pointer (LPW0-17) - Provides the least significant 18 bits of a 24 bit address of the DCW or PCW list. In MULTICS Mode, or for the address of a PCW in any mode, the most significant six address bits will be zero. In Extended GECOS or VMM Mode, the most significant six address bits depend on the state of LPW 20 (see below).

Restricted Bit (LPW 18) - Remains the same as presently specified.

REL' (LPW 19) - Remains the same as presently specified.

EC (LPW 20) - Was previously undefined and is now defined as the Extension Control bit. In the Extended GECOS or VMM Mode this bit defines when a DCW list address should be appended with zeroes (LPW 20 = 0), or should be appended with the current

address extension (LPW 20 = 1). This bit may be changed from a zero to a one via a transfer type DCW, and will be reset to zero during a Reverse List Service. MBZ in MULTICS. A system fault will be reported if LPW 20 = 1 in GECOS Mode.

NC - No Change (LPW 21) - Remains the same as presently specified.

TAL (LPW 22) - Remains the same as presently specified.

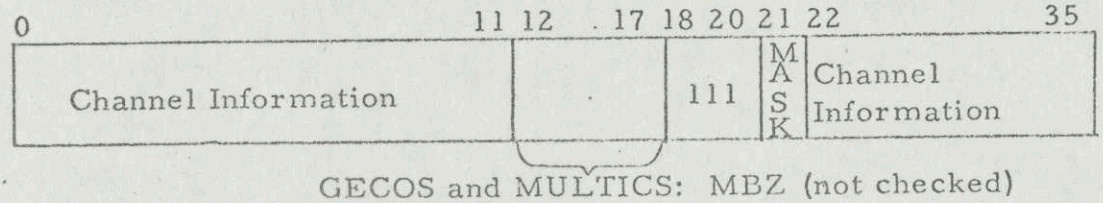
REL (LPW 23) - Remains the same as presently specified for GECOS, Extended GECOS or VMM Modes of operation. In MULTICS Mode operation, since all addressing is absolute, the occurrence of an LPW accessed with bit 23 = 1 will result in a system fault being reported.

Tally (LPW 24-35) - Remains the same as presently specified.

Lower Bound (LPW Ext. 0-8) and Size (LPW Ext. 9-17) - Remains as presently specified for GECOS, Extended GECOS or VMM Modes of operation, except that size = 0 is valid. Contents of these fields will be ignored during MULTICS Mode operation.

Pointer to First DCW to Most Recent Instruction (LPW Ext. 18-25) - Remains the same as presently specified. Note that this pointer is the least significant 18-bits of address.

B.2.2 Peripheral Control Words



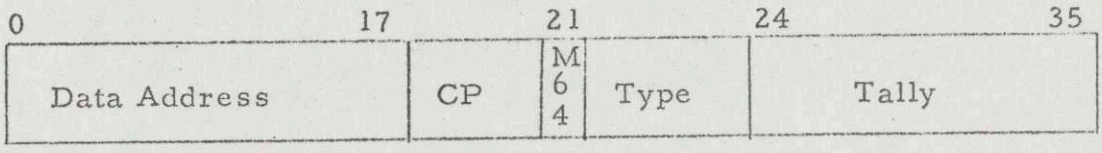
GECOS and MULTICS: MBZ (not checked)
Extended GECOS or VMM: Address Extension

Definition of PCW's remain as presently specified with the exception of bits 12-17. This field was previously undefined; it will now be used for the address extension in Extended GECOS or VMM Mode.

B.2.3 Data Control Words

B.2.3.1 Data type DCW's

For type IOTD, IOTP, IONTP -



The only change to the existing 655 IOM definition of a data DCW will be the interpretation of DCW 21. Data DCW 21 was formerly intended to be used, if a sub-word (character) channel were defined, to specify the manner of DCW tally update. That is, tally updating would be done once per word or once per character. For the 645X IOM, tally will be on a word basis if a 9-bit character channel is ever defined.

In Extended GECOS or VMM, data DCW 21 = 0 will cause the data address DCW 0-17 (absolutized if called for by LPW 23) to be appended with the 6-bit address extension from the PCW for each data transfer; DCW 21 = 1 is a system fault in Extended GECOS.

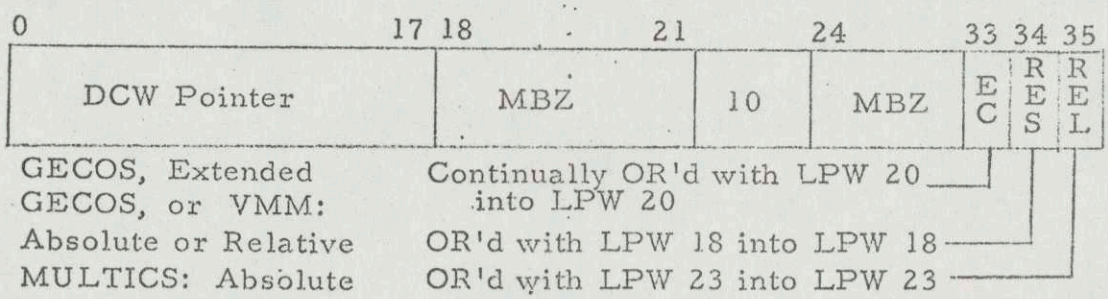
In VMM Mode, DCW 21 = 1 and LPW 23 = 0 (absolute) will result in the formation of a 24 bit modulo 64 address from DCW (0-17) DCW 21 = 1 and LPW 23 = 1 (relative) is a system fault in VMM.

In the MULTICS Mode, data DCW 21 = 0 will cause the absolute data address DCW 0-17 to be appended with 6 leading zeroes for each data transfer; DCW 21 = 1 will initially cause the data address DCW 0-17 to be left justified 6 bits to form a 24 bit modulo 64 address to be used for data transfer. Subsequent data transfers will use DCW (0-5) as the address extension.

B.2.3.2 Instruction DCW

The IDCW remains as formerly defined in the 655 IOM.

B.2.3.3 Transfer DCW



The Transfer DCW remains as presently specified except for bit 33 in Extended GECOS and VMM. The DCW Pointer (0-17) is, depending on the mode and the present state of LPW 23, the low order 18-bits of the relative or absolute address for the next DCW. The most significant six bits (address extension) of the next DCW address are either implied to be zero (MULTICS Mode or [Extended GECOS or VMM Mode · LPW 20 = 0]) or will be the present address extension (Extended GECOS or VMM) and (LPW 20 = 1). The REL bit (bit 35) has no meaning in MULTICS Mode, but the process or ORing it into LPW bit 23 will be followed the same as in the GECOS modes. The end result in MULTICS Mode will be a system fault if bit 35 = 1. Bits (18-21) and (24-32) MBZ and are not checked.

In Extended GECOS or VMM, bit 33 may be used to conditionally change LPW 20 from a zero to a one. That is, if TDCW 33 = 1 and if bit 18 of the present LPW is zero (unrestricted), LPW 20 will be set to a one. This will allow (system) software to control when the address extension bits from the PCW will be used for accessing the users DCW list. Transfer DCW 33 = 1 and LPW 18 = 1 (restricted) is a system fault in Extended GECOS or VMM. DCW 33 MBZ for GECOS and MULTICS (not checked).

B.2.4 Status Control Word

Definition of the fields and format of SCW's remains as presently specified. The Status Queue Address represents the least significant 18-bits of address with the upper six bits implied as zero. The IOM will append zeroes in the six most significant address bits when status storage occurs.

B.2.5 Channel and Device Status Words

Status word storage will be as presently specified, with the exception that the unused bits of the even status word (bits 24-29) will be used to store bits 0-5 of the address extension from a channel and bit 13 = 1 will indicate status was stored due to a "Marker" condition.

Even Word

0	1	2 5	6 11	12	13	14 15	16	17	18 23	24 29	30 35
T	P	Major Status	Sub Status	E O	M R K	Sft.	I	A	IOM Chan Status	IOM Cent Status	Adrs Ext (0-5)	Record Residue

Odd Word

0 17	18 20	21	22 23	24 35
Next Absolute Address bits (6-23) of Data	Char Pos	R	A. C.	DCW Tally Residue

Note that the odd status word is essentially an image of the DCW residue, with the exception of bits 18-21 which are supplied by the channel. Specifically, bit 21 in an odd status word does not indicate Mod 64 transfers; it indicates the direction of data transfer (Read/Write).

The IOM Central will obtain the address extension bits from the channel's Transaction Command (for status service), and will "OR" them into bits 24-29 of the status word supplied by the channel; therefore, the channel must insure that bits 24-29 of the even status word are zero.

B.3.0 SOFTWARE OPERATING SYSTEM CONTROL

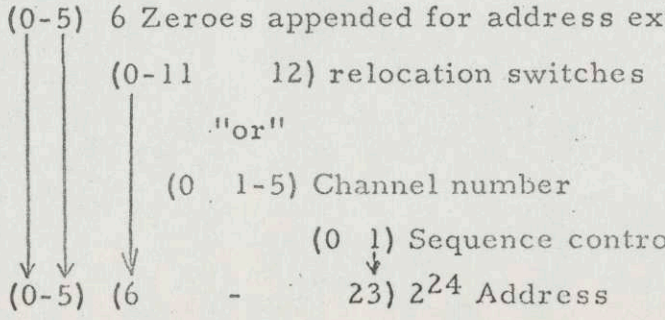
A manually-operated four-position configuration switch will be provided to place restrictions on the allowable operating system:

Position 1 - "Standard GECOS"
Position 2 - "Extended GECOS"
Position 3 - "MULTICS Mode"
Position 4 - "VMM"

A set of system and user faults will be reported (formats to be defined) if the operating system attempts to exceed mode constraints.

B.4.0 2^{24} ADDRESS DEVELOPMENT SUMMARY

B.4.1 Mailbox Addresses - Any Mode



B.4.2 PCW List Addresses - Any Mode

(0-5) 6 Zeroes appended for address extension
(0- -17) Contents of Connect channel LPW 0-7
(0-5) (6- -23) 2^{24} Address

B.4.3 DCW List Addresses

(0-5) 6 Zeroes if Extended GECOS or VMM Mode "and" LPW 20 = 0 "or" if MULTICS Mode,
"or"
(12-17) PCW 12-17 if Extended GECOS or VMM mode "and" LPW 20 = 1
(0 -- 17) Contents of payload channel LPW 0-17
0--5) (6 -- 23) 2^{24} Address

B.4.4 Data Addresses

a) Extended GECOS

. DCW 21 = 0

(12-17) Extension from PCW 12-17
(0-17) Absolutized contents of DCW 0-17
(0--5) (6-23) 2^{24} Address

. DCW 21 = 1 is a system fault.

b) MULTICS

. DCW 21 = 0

(0-5) 6 Zeroes of address extension
(0-17) contents of data DCW 0-17
(0-5) (6-23) 2^{24} Address

· DCW 21 = 1

(0-5) Contents of bits 0-5 of the data DCW become the address extension

(6-17) contents of bits 6-17 of the data DCW

(18-23) initial zero fill of 6 bits

(0-5)(6-17)(18-23) 2^{24} Address

c) VMM

· DCW 21 = 0

Same as Extended GECOS with DCW 21 = 0

· DCW 21 = 1 "and" Absolute (LPW 23 = 0)

Same as MULTICS WITH DCW 21 = 1

· DCW 21 = 1 "and" Relative (LPW 23 = 1)

System fault

B.4.5 Status Lists, Interrupt Multiplex Words, and System Fault Word Addresses - Any Mode

(0-5) 6 Zeroes appended for address extension

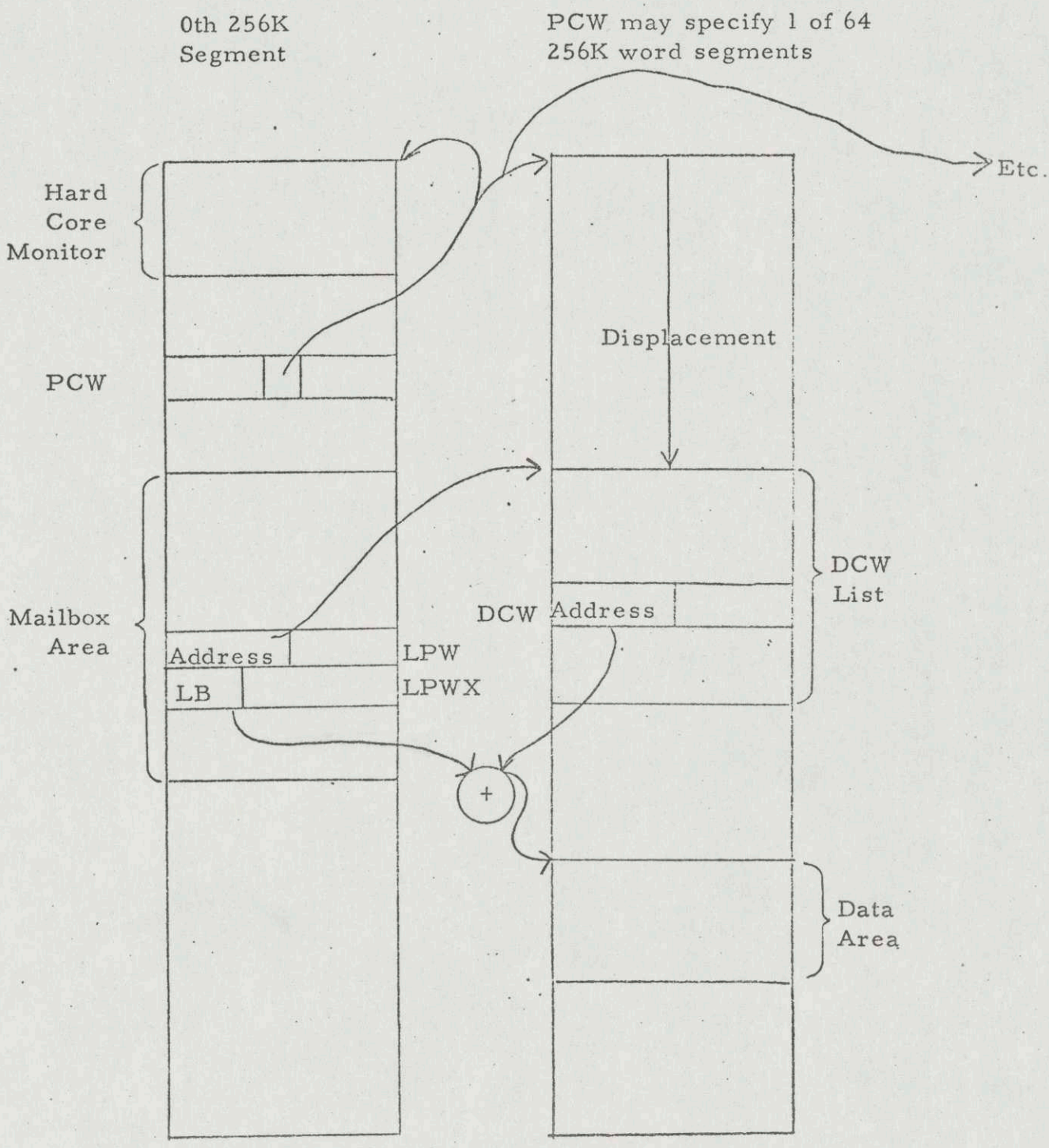
(0-17) 18 bit address as defined in the 655 IOM

(0-5) (6-23) 2^{24} Address

B.4.6 Summary of New Major Control Word Actions

	GECOS	Extended GECOS	MULTICS	VMM
DCW List Address If LPW 20 = 0 = 1	(0-0)(LPW0-17) System Fault	(0-0)(LPW0-17) (EXT-PCW) (LPW0-17)	(0-0)(LPW0-17) NA-MBZ	(0-0)(LPW0-17) (EXT-PCW)(LPW0-17)
Data Address If DCW 21 = 0 = 1	(0-0)(DCW0-17) System Fault	(EXT-PCW)(DCW0-17) System Fault	(0-0)(DCW0-17) (DCW0-17)(0-0)	(EXT-PCW)(DCW0-17) "and" Absolute: (DCW0-17)(0-0) "and" Relative: System Fault
Control of LPW 20 via TDCW 33 = 1	NA-MBZ	"and not restricted:" LPW 20 ⇒ 1 "and restricted:" User Fault	NA-MBZ	"and not restricted:" LPW 20 ⇒ 1 "and restricted:" User Fault
DCW List Address for Reverse List	(0-0)(LPWX0-17)	(0-0)(LPWX0-17)	(0-0)(LPWX0-17)	(0-0)(LPWX0-17)

B.4.7 2^{24} Memory Map - Extended GECOS Example



B.4.8 Fault Summary

In addition to the system and user faults defined in the existing IOM EPS-I specifiecation which will apply to all modes of operation, the following mode dependent errors are defined.

a) Relative error, MULTICS Mode -
Detected during a list service if LPW 23 = 1. Note that LPW 23 could have been set to a 1 by a TDCW with bit 35 = 1.

Result: System Fault

b) Illegal data DCW, Extended GECOS or GECOS Mode -
Detected during a list service if Data DCW 21 = 1.

Result: System Fault

c) Illegal LPW, GECOS Mode -
Detected during a list service if LPW 20 = 1.

Result: System Fault

d) Boundary error, GECOS, Extended GECOS, or VMM Mode -
Detected during a list service when address absolutizing is required and the boundary conditions are not met.

Result: User Fault

e) Illegal Modulo 64 data DCW, VMM Mode -
Detected during a list service if Data DCW 21 = 1 "and" LPW 23 = 1 (relative).

Result: System Fault

f) Illegal control of Address Extension by a Restricted User, Extended GECOS or VMM Mode -
Detected during a list service if TDCW 33 = 1 "and" LPW 18 = 1.

Result: User Fault

B.4.9 Boundary Check

The 655 IOM is defined such that the specifier of the core size for a relative mode program (LPWX 9-17) cannot be zero. That is, the size field of zero is defined as a boundary error.

The 645X IOM will not interpret a size of zero as an error, but will interpret size = 0 as the specifier for 256K (i.e., 512 consecutive blocks of 512 words each). All of the remaining 655 IOM bounds checks will apply.

NOTE: The only valid LB (lower bound) when the size = 0 is a lower bound of zero.

B.5.0 IOM CENTRAL/CHANNEL INTERFACE

This bus structured interface described in Appendix A of the 655 IOM EPS-I is transparent to software but not the logic of IOM Central and the channels.

Because indirect type payload channels are required to accept and buffer the 6 bits of address extension, and because all payload channels must supply the address extension to the Central, the information transfer on this interface must be specified.

During a connect (PCW), or a list service (DCW) sequence with DCW 21 = 1, the Central will place the 6 bits of address extension on bits (12-17) of the U-Bus to the channel. Indirect type payload channels are required to accept and buffer this extension in addition to the other control information extracted by the channel from a PCW or DCW. This is the only change of information placed on the U-Bus to the channel.

A change in the definition of the transaction command information placed on the D-Bus to the Central during a data, list or status service sequence is required in order for the channel to supply the address extension bits to be used in forming 24 bit addresses. During any one of these sequences, the channel will be required to place address extension data on the D-Bus as follows:

Address Extension (0-3)	D-Bus (18-20)
Address Extension (4-6)	D-Bus (33-35)

D-Bus bits (18-20) and (34, 35) were formerly unused in all transactions. D-Bus bits 32 and 33 were defined to indicate, to the IOM Central during a data or list service, the channel interface size to the Central as 6, 9, 18, or 36 bits. D-Bus bit 32 is redefined to specify 9 bits (32=0) or 36 bits (32=1) and D-Bus bit 33 is freed to carry address extension bit 4.