gri-909

THE NEW BREED

maintenance manual

volume I

GRI Computer Corporation
320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

Price: $15.00

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volume I

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320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

March 1972

This manual is for informational purposes only. The technical information is not to be construed as engineering specifications.

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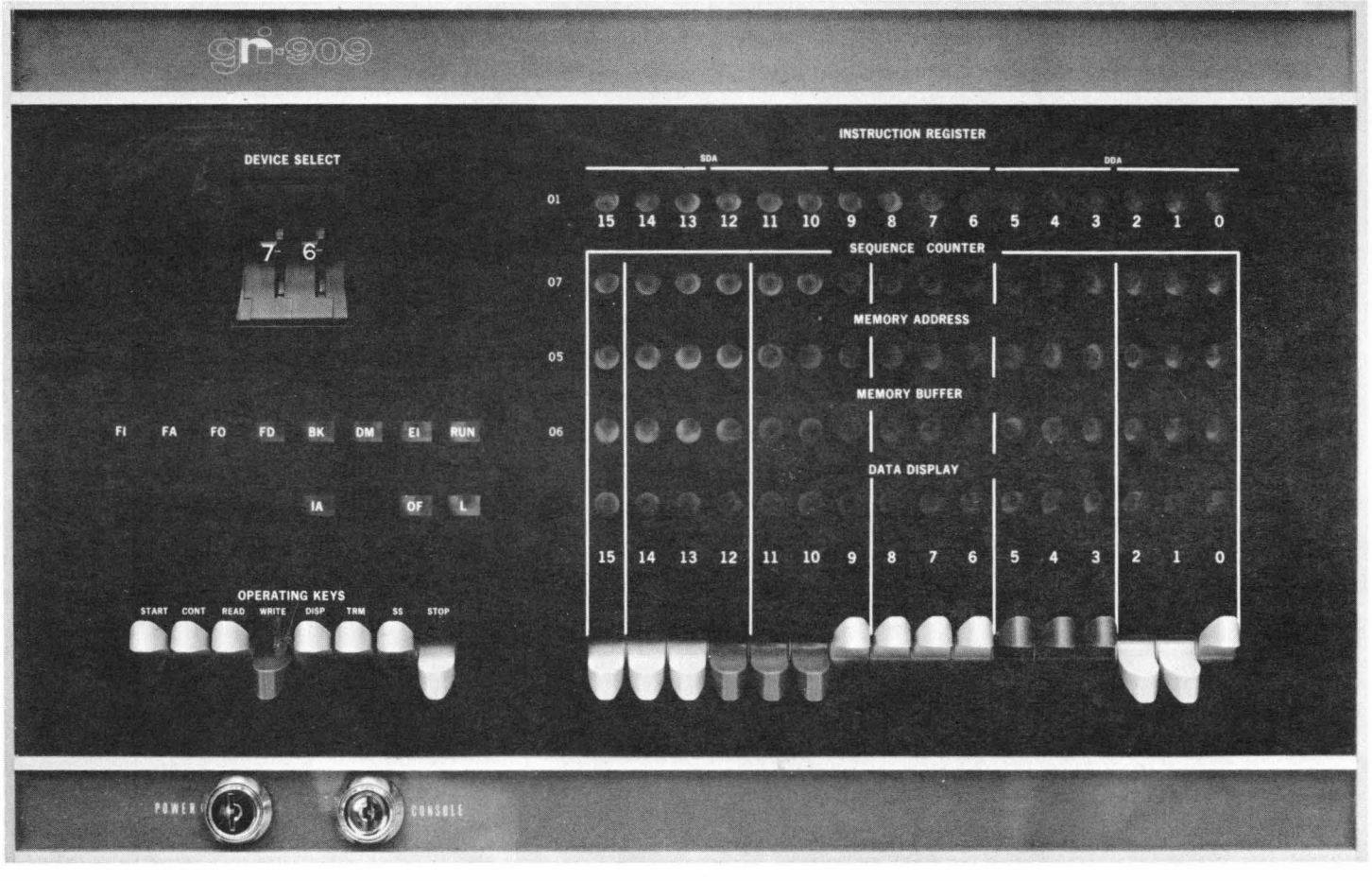
gri-909
DEVICE SELECT
7 6
FI FA FO FD BK DM EI RUN
IA OF L
OPERATING KEYS
START CONT READ WRITE DISP TRM SS STOP
POWER
CONSOLE
INSTRUCTION REGISTER
SDA
DDA
01
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SEQUENCE COUNTER
07
MEMORY ADDRESS
05
MEMORY BUFFER
06
DATA DISPLAY
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

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THE GRI-909

CHAPTER 1
GRI-909
GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

The GRI-909 Computer (available in Models 10, 20, 30, 40) is a compact 16-bit machine, especially designed to be an economical powerful part of larger dedicated systems. The GRI-909 is easily interfaced to a wide variety of system devices. Data handling is fast and efficient, and data can be transferred between all system registers (including memory) and external devices. Programming is directed to specific functions for the system designer, rather than being strictly limited to complex arithmetic or mathematical expressions; the assembly language is easy to understand and highly systems oriented. Section 1.4 contains specifications for the GRI-909 Computer.

1.2 FEATURES

The features listed below make the GRI-909 an especially flexible and expandable computer for system control:

- Processor – 16 bit fully parallel processor, 1.76 μs cycle time
- Memory – Maximum of 32,768 words of random-access core memory, directly addressable (not page oriented). Minimum core size is 1024 words.
- Programming – Simple programming in a higher level, functional language, without sacrificing the efficiencies and economies of an assembly language.
- Direct Memory Access – Any device can transfer data directly to memory. Direct memory access (DMA) channel is available on the same data and control lines as the programmed input/output (I/O) channel (I/O rate: 9.1 Mbits per second). No DMA multiplexer is required for multiple DMA devices.
- Direct Data Transfer – Every device in the system is directly addressable by programmed instructions. Data can be transferred between devices without special accumulators or temporary storage. Many computer instructions normally required for data manipulation are eliminated.
- Firmware – Firmware options can take the form of microprogrammable read only memories (ROMs) or hardware logic to expand the instruction set and provide system flexibility unequalled by more conventional computer designs, e.g., multiple arithmetic units, extended arithmetic options, byte manipulation hardware, general-purpose registers.
- Priority Interrupt System – Priority interrupt system has full capability to be used as a single-channel interrupt or as an automatic hardware interrupt at the option of the system designer. Most GRI standard I/O operators have full auto-hardware interrupt.
- Expansion – Power and space are available for 8192 words of memory, 3 major firmware operators and 16 firmware or device interface operators.
- Protection – Memory power fail protection and automatic restart are standard in the Model 10 and optional in Models 20, 30, 40. Also, remote start and stop are available for use in system interface.
- Versatility – Core memory and ROM are interchangeable.
- Reliability – TTL integrated circuit and medium scale integrated (MSI) circuit modules are used for maximum reliability and economy.
- Displays – All system registers, both internal and external to the computer, can be displayed on the console. Data can be transferred to all system devices using console switches.
- Photo-optical switches – Console switches are photo-optical for long, bounce-free life.
- Peripherals – Peripheral options include: mass memory media, I/O devices, communication interfaces, display, and digital system devices.

1.3 DESIGN CONCEPT

The GRI-909 Computer is a *direct function processor* (see Figure 1-1). Direct function processing, a unique concept in computer-controller design, enables each system element to communicate directly with any other element using shared high-speed data buses. Thus, such peripheral devices as a Teletype® or CRT are connected across the same bus structure as the arithmetic unit and memory of the computer, as well as the other processor elements. Data transfer between external devices and computer devices is accomplished directly, in a single operation, with no temporary storage of data in special I/O registers or accumulators. As a result, data flow between devices increases, and no special complicated command repertoire is necessary to process and translate information transmitted between the computer and the device controlled.

A vital block of logic called the *bus modifier* (see Figure 1-1) provides a programmable path between the source and destination buses. The bus modifier is designed to accept data from any input device and move the data to any output device, as well as perform operations "on-the-fly" as the data pass from one device to the other. Operations that can be performed on the data include: increment, left shift, right shift, one's complement, no modification, and two's complement.

The modular design inherent in direct function processing encourages many machine configurations, ranging from highly economical minimal processors (for systems requiring simple data manipulations) to large systems with powerful computing instructions and a variety of peripheral devices. Hardwired firmware operators can be added in the form of plug-in modules to provide virtually thousands of computer instructions. The modules, or firmware operators, add flexibility and expandability unequalled by conventional computer designs.

The direct function processing technique, used exclusively in the GRI-909, is the culmination of many years of experience in both the design of computers and the use of computers in systems. The GRI-909 is a tested, proven system control computer. Its flexibility, modularity, and ease of programming provide the original equipment or system manufacturer with a system control center that minimizes many of the problems inherent in conventional computer designs. The modular firmware capability of the GRI-909 provides the system designer with flexibility to meet changing system requirements, the ability to incorporate proprietary and unique control features, and a solid hedge against obsolescence caused by the introduction of new system devices or circuitry.

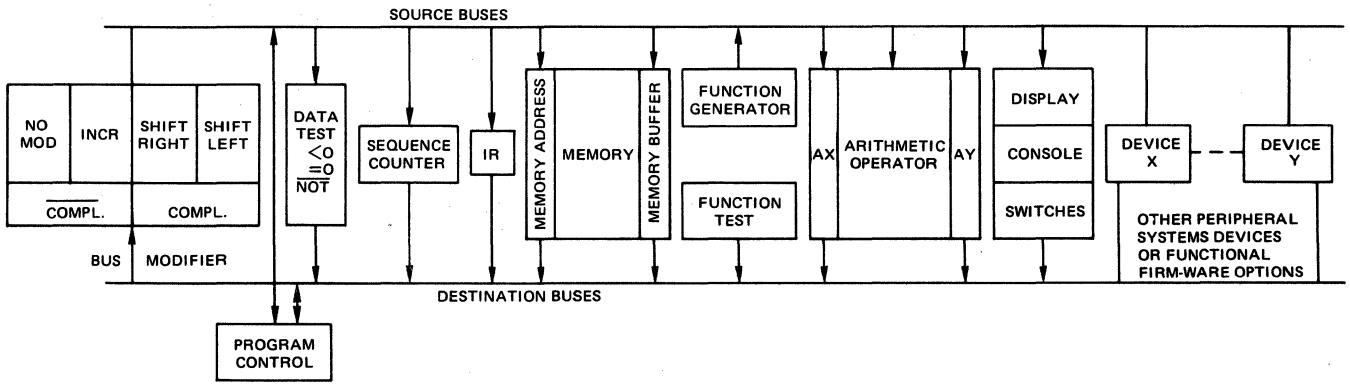


Figure 1-1 Direct Function Processor. Typical Configuration

® Teletype is a registered trademark of Teletype Corp.

1.4 SPECIFICATIONS

1.4.1 Physical (See Figure 1-2)

Size: 10-1/2 in. high, 19 in. wide, 20 in. deep

Weight: 50 lb.

The GRI-909 mounts from the front in a standard EIA 19-in. cabinet with provision for rack slides. Space is provided in the basic frame for up to 3 major functional firmware options and up to 16 firmware or interface modules. Memory capacity of the basic frame is 8192 16-bit words. Extender frames can be provided for an additional 24,576 words of core memory and/or additional firmware or interface modules. ROM modules can be interchanged with core memory modules.

1.4.2 Electrical

Power:	100 Vac - 130 Vac, 60 Hz ± 3%, 8A or 200 Vac - 240 Vac, 50 Hz ± 3%, 4A, single phase.
Power Dissipation:	150W - 250W.
Logic Levels:	Ground and +4 Vdc, DTL and TTL compatible.

1.4.3 Functional

Word Length:	16 bits
Core Memory Size:	1024 words, expandable to 32,768 words, direct addressing.
Machine Cycle Time:	1.76 μs when executing instructions from main memory; 880 ns in External Instruction (EIR) mode.
Instructions:	The number of machine instructions is modular and depends on the firmware and device options used. A basic processor with arithmetic operator has over 100 instructions.

1.4.4 Environmental

Temperature:	0 °C to 50 °C, ambient
Relative Humidity: (non-condensing)	to 90% (operating)
Cooling:	Convection, no fans required for operation over ambient temperature range.
Switches:	All console data and control switches are photo-optical. There are no mechanical contacts subject to wear or arcing.
Rate of Temperature Change:	Not more than 10 °C per hr. for optimum memory tracking.

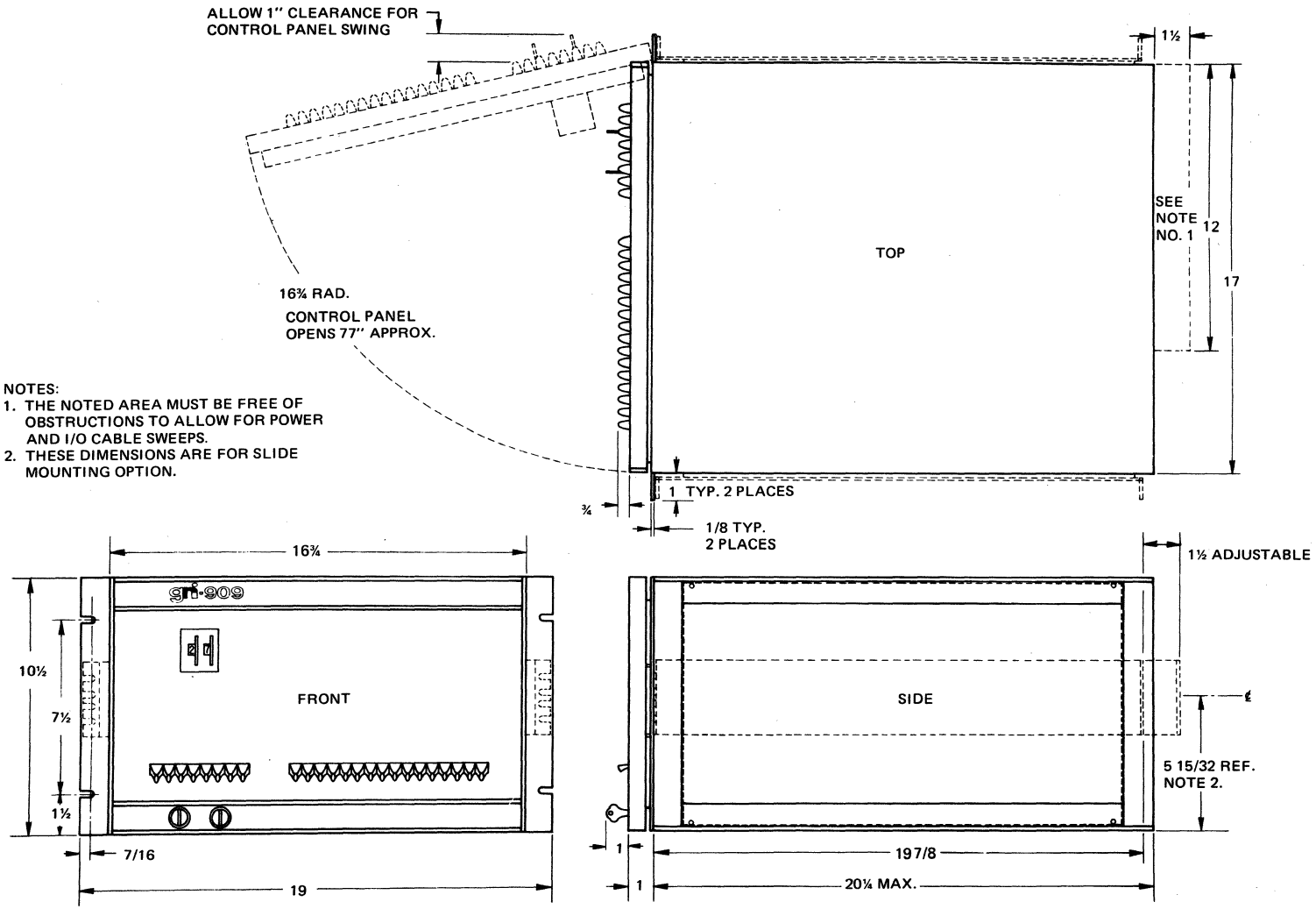


Figure 1-2 GRI-909 Dimensional Drawing

CHAPTER 2
OPERATION AND PROGRAMMING

Chapter 2 describes GRI-909 operations, controls, indicators, and turn-on and shut-down procedures. The I/O and internal processing command repertoire is also fully described.

2.1 CONSOLE DESCRIPTION

Figure 2-1 shows the GRI-909 console. The controls (OPERATING KEYS on the lower left of the console and Data Switch Register toggle switches on the lower right) are used to input data to any device in the system. The indicators on the left (FI, FA, FO, etc.) display internal computer conditions. The indicators on the right display the contents of the various processor registers, INSTRUCTION REGISTER (IR), SEQUENCE COUNTER (SC), MEMORY ADDRESS (MA), MEMORY BUFFER (MB), and DATA DISPLAY (DD). When any indicator is lit, the associated flip-flop is in the 1 state (or true state). When an indicator is out, the associated flip-flop is in the 0 state (false).

2.1.1 Controls

2.1.1.1 Power – The key operated POWER switch on the lower left-hand side of the console supplies primary power to the computer. The key is inserted and turned clockwise.

2.1.1.2 Console – The CONSOLE switch on the lower left-hand side of the console disables the OPERATING KEYS to prevent unauthorized tampering with the operation of the processor. The key is inserted and turned clockwise. The operator can continue to use the data switches to supply information to the program.

2.1.1.3 Operating Keys – The OPERATING KEYS are located at the bottom left of the console. All keys (except SS and STOP) are momentary contact switches. Table 2-1 lists the keys and their associated functions.

Table 2-1

GRI-909 OPERATING KEYS AND FUNCTIONS

Key	Function
START	Sets all Output Ready flags, clears all other flags and control flip-flops, lights FI and RUN, and begins normal operation by executing the instruction at the location specified by SEQUENCE COUNTER.
CONT	Lights RUN and begins normal operation in the state shown by the indicators.
READ	Displays the contents of the memory location addressed by SEQUENCE COUNTER in the MEMORY BUFFER indicators and in the DATA DISPLAY indicators if the thumbwheels are set to 06. Then adds 1 to SEQUENCE COUNTER. At completion, FI is lit.
WRITE	Stores the contents of the Data Switch Register in the memory location specified by SEQUENCE COUNTER. Then adds 1 to SEQUENCE COUNTER. At completion, FI is lit and the MEMORY BUFFER indicators display the word stored; the DATA DISPLAY indicators also display the word if the thumbwheels are set to 06.
DISP	Displays the contents of the source register addressed by the thumbwheels in the DATA DISPLAY. At completion, FI is lit.

Table 2-1

GRI-909 OPERATING KEYS AND FUNCTIONS (Cont.)

Key	Function
TRM	Transmits the contents of the Data Switch Register to the destination register specified by the thumbwheels. At completion, FI is lit and the DATA DISPLAY shows the word transmitted.
SS	Allows the operator to run diagnostic routines or other programs one major state at a time for maintenance purposes. This key is an alternate-action key. While it is down, the processor stops at the end of every cycle it executes. Operations are begun by pressing START, and each succeeding cycle is initiated by pressing CONT.
STOP	Stops at the completion of the current instruction with the INSTRUCTION REGISTER indicators displaying the instruction and SEQUENCE COUNTER pointing to the next instruction. The control lights at the left indicate the type of cycle the processor is to execute when operation is resumed. This key is an alternate-action key; the operator can run a program one instruction at a time by leaving STOP on, executing the first instruction by pressing START, and executing each succeeding instruction by pressing CONT.

2.1.1.4 Data Switch Register – The Data Switch Register is located at the bottom right of the console. The computer operator manipulates these switches to supply addresses, instructions, or data to the destination bus of the computer. A switch that is depressed (down) represents a binary 1; a switch that is not depressed represents a binary 0. The Data Switch Register can be used as follows:

a. As sense switches in real time under program control.
b. To write into memory.
c. To transmit data to a device selected on the thumbwheels.

The contents of the Data Switch Register can be read by the program using source code 10.

2.1.1.5 DEVICE SELECT Switch – Two octal thumbwheels are located at the upper left of the console. The thumbwheels are used to select operator addresses that are used in conjunction with the Data Switch Register and DATA DISPLAY indicators.

2.1.2 Indicators

Most indicators on the GRI-909 console change state too frequently or too quickly to display useful, readable information when the processor is running. For this reason, the description of many of the indicators is limited to information displayed when the processor is not running.

NOTE

The top four rows of indicators at the right of the GRI-909 console are installed only on the programmer's console.

2.1.2.1 Processor Registers – The indicators that display the contents and status of the various processor registers are listed in Table 2-2, accompanied by a brief description of the function of each display.

2.1.2.2 Cycle Indicators – These indicators are located on the left side of the GRI-909 console. Table 2-3 lists the indicators and gives a brief description of the function of each indicator.

Table 2-2

PROCESSOR REGISTER DISPLAYS

Display	Function
INSTRUCTION REGISTER (IR)	Displays the instruction being executed or the last instruction completed. The six indicators on each end represent the source and destination addresses. The middle four indicators represent the control bits.
SEQUENCE COUNTER (SC)	Displays, in the low-order 15 bits, the address in memory of the next instruction to be executed (except in the case of READ and WRITE OPERATING KEYS, where the SEQUENCE COUNTER points to the next location to be read from or written into.)
MEMORY ADDRESS (MA)	Displays the address to which the last memory access was made.
MEMORY BUFFER (MB)	Displays the last data transmitted to the MEMORY BUFFER.
DATA DISPLAY (DD)	Displays information used in conjunction with the OPERATING KEYS. When the program is running, DD displays information sent to the destination selected by the thumbwheels. Thus, the operator can monitor any destination or, by selecting an unused system address (non-existent device), the program can supply information to the operator without affecting any internal register.

Table 2-3

PROCESSOR CYCLE INDICATORS

Indicator	Function
FI	The next processor cycle will be used to fetch an instruction from memory.
FA	The next processor cycle will be used to fetch the address or process an immediate operand in a memory reference instruction.
FO	The next processor cycle will be used to process the operand in a memory reference data transmission instruction, to fetch the second address in a deferred memory reference instruction of any type, or to process the operand in an immediate deferred memory reference.
FD	The next processor cycle will be used to process the operand in a deferred memory reference data transmission instruction.
BK	The next processor cycle will be used to start an interrupt (break) by storing SC in the location addressed by the interrupting device.
DM	The next processor cycle will be used for direct memory access (DMA).
EI	The next processor cycle will be used to execute a pair of external instructions.
RUN	The processor is in normal operation with one instruction following another. When the indicator goes out, the computer stops.
IA	The interrupt control is active (on).
OF	The last data transmission instruction that incremented the word being transmitted increased its value to 2^{16} (causing Bus Overflow flag to set).
L	This indicator displays the state of the 1-bit link register.

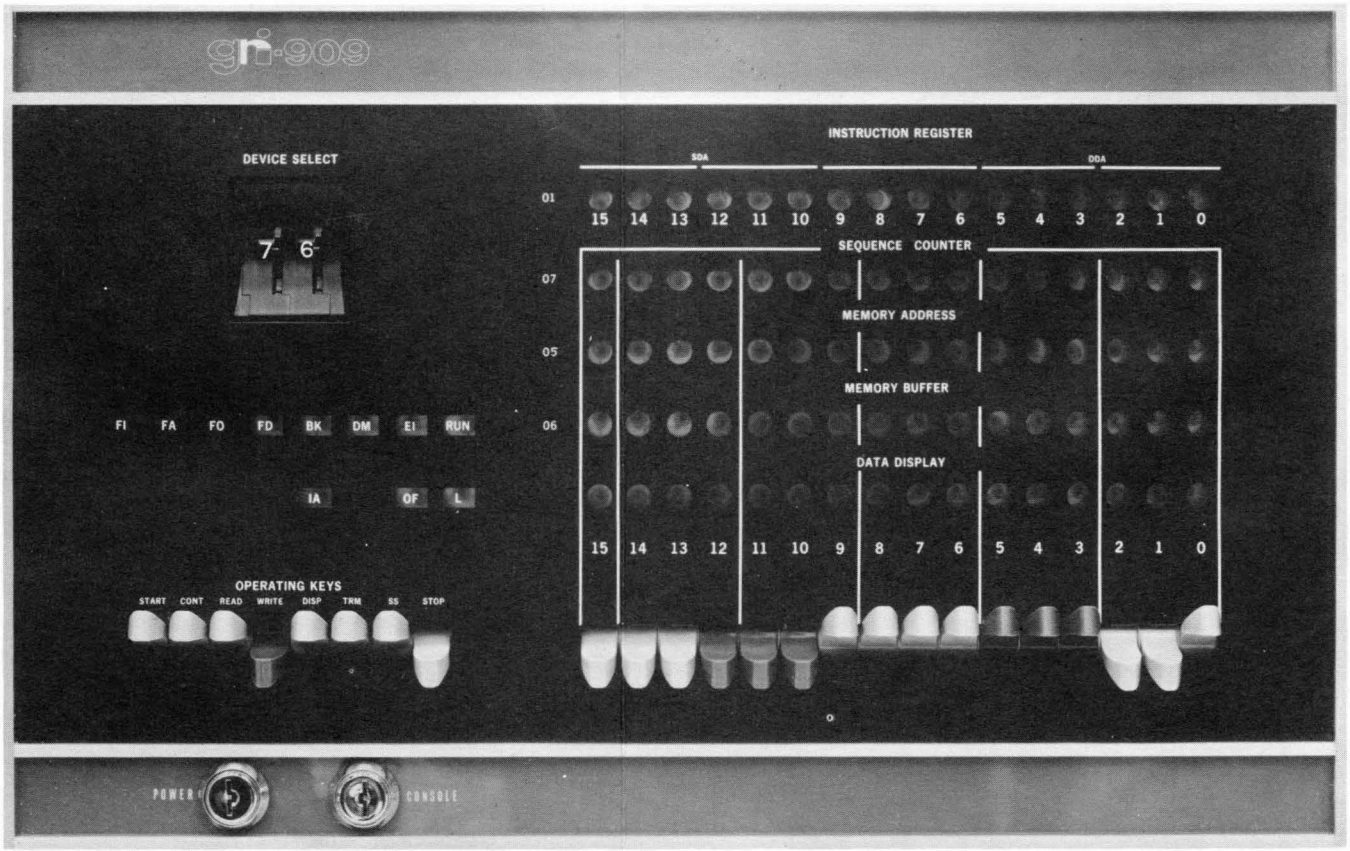


Figure 2-1 GRI-909 Front Panel With Programmer's Console

2.1.3 Start-Up Procedure

When ac power is applied to the computer, it is important to note the following conditions:

a. The register indicators do *not* represent the actual contents of the registers until the operator initializes them by performing an operation.

b. All Output Ready flags are set.

c. If the autorestart switch (located behind the console on the power supply front panel) is *off,* the SC is set to location 6 and the computer is stopped.

d. If the autorestart switch is *on,* the processor begins normal operation at location 6.

e. If the autorestart switch is on, it is recommended that the operator depress the STOP switch before applying ac power. *The computer then performs one instruction and stops.* thereby initializing the register indicators. The contents of the SEQUENCE COUNTER depend upon the instruction.

The following procedure is used to start the GRI-909 Computer:

Step	Procedure
1.	Depress the STOP switch before applying primary ac power.
2.	Set the starting address of the program using the Data Switch Register.
3.	Set the octal thumbwheel switches to 07 (SEQUENCE COUNTER).
4.	Depress the TRM key to load the starting address into the SEQUENCE COUNTER (SC).
5.	Depress the START key to start the program at the SC value.

To continue operation in the current computer state, but at *any* desired location, proceed as follows:

CAUTION

Do not use the SS mode in the following procedures. Any operation in the SS mode may destroy the machine state and, as a result, the instruction being executed if it is not completed.

Step	Procedure
1.	Depress the STOP switch.
2.	Set the new address on the Data Switch Register.
3.	Set the thumbwheel switches to 07 (SC).
4.	Depress the TRM Key to transmit the new address to the SC.
5.	Depress CONT to continue the program.

NOTE

Use of the TRM key affects only the register selected by the thumbwheels and, in some cases, a device connected to that register. For example, transmitting the contents of the Data Switch Register to the teleprinter causes the 8-bit character in switches 0-7 to be printed. thus affecting the Output Ready flag and possibly its interrupt request bit.

To examine the contents of any register, proceed as follows:

Step	Procedure
1.	Depress the STOP key.
2.	Set the octal thumbwheels to the code of the desired register (refer to Table 2-4 at the end of this chapter).
3.	Depress the DISP key.
4.	Read the contents of the selected register in the DATA DISPLAY.
5.	Depress CONT to continue operation.

NOTE

Use of the DISP key does not affect the machine state. However, the DISP key can affect the state of an output device that may share the same system address as an input device. For example, TTI and TTO share 77; displaying 77 also causes the contents of TTI to echo.

2.1.4 Shut-Down Procedure

The following procedure is used to shut down the GRI-909 Computer.

Step	Procedure
1.	Turn the key operated POWER switch counterclockwise.
2.	When ac power is turned off, it is important to note the following conditions:

a. The processor shuts down after a 140-μs delay.

b. The previous contents of memory are unaltered.

c. All flags and control flip-flops are cleared after 140 μs.

2.2 PROGRAMMING

The basic processor (see Figure 2-2) comprises:

a. Back panel bus with bus modifier
b. Controller
c. Four functional operators connected to the bus.

A core memory operator to hold a program and data is also shown in Figure 2-2. The Sequence Counter (SC), Instruction Register (IR), Data Test Operator, and Function Generate/Function Test Operator are required operators using fixed addresses in the bus address scheme. In conjunction with the control logic, these operators select instructions from the program stored in memory, interpret the instruction type as being one of four classes of instructions, and then perform the decoded instruction. Tables 2-4 through 2-7 in the back of this chapter contain reference data pertaining to the four classes of instructions.

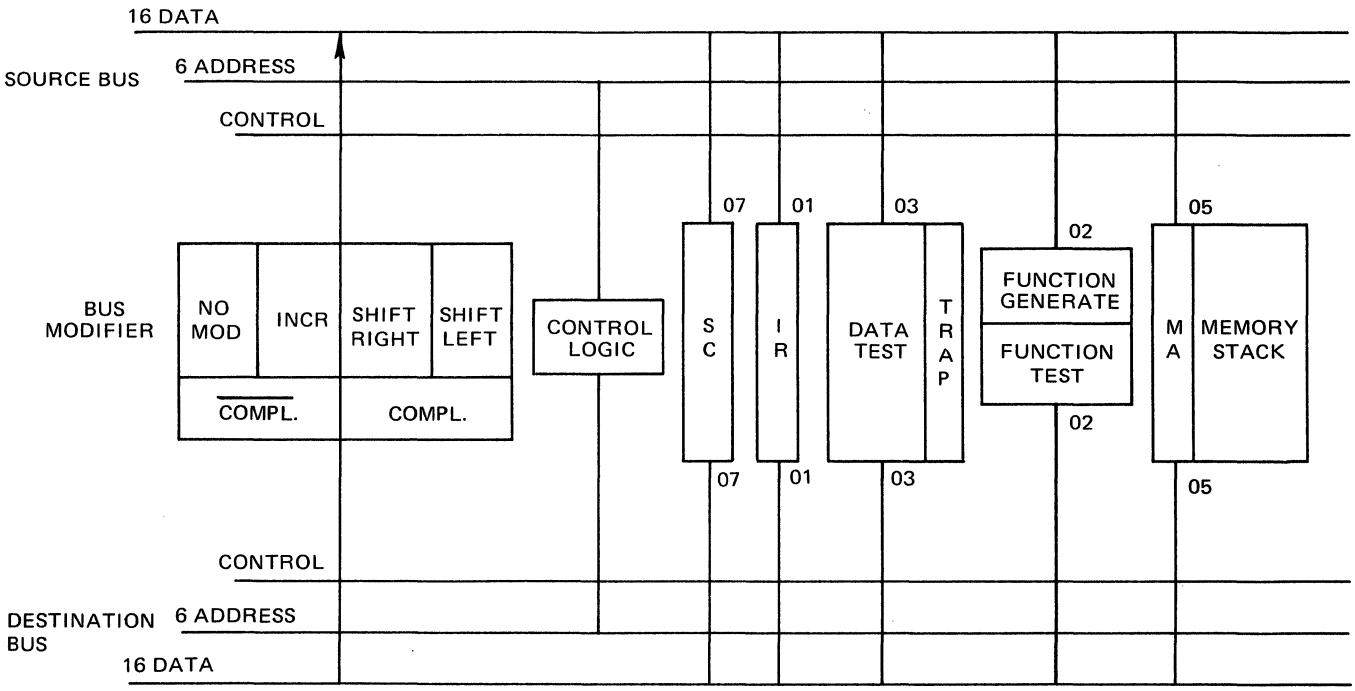
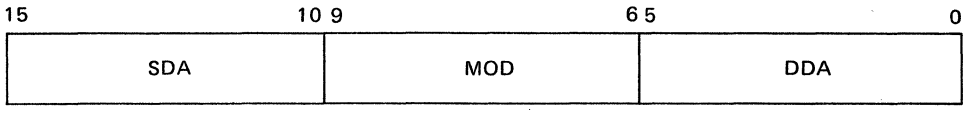


Figure 2-2 Basic Processor

A machine command for the GRI-909 consists of either a one-word instruction or a one-word instruction followed by a second word that contains an address or data. In either case, the one-word instruction is of the general form DEVICE X TO DEVICE Y and is described by the format:

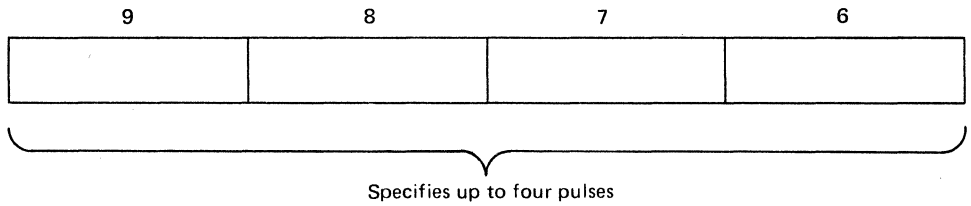


where:

SDA	=	Source Device Address
MOD	=	Modifier
DDA	=	Destination Device Address

2.2.1 Function Generation

The Function Generator, specified by a Source Device Address of 02 (represented as SDA = 02), causes control signals (rather than data) to be transmitted to the device at DDA. The MOD format is:



The unique combination of MOD and DDA defines the function to be performed. Pulses are transmitted in parallel; therefore, up to 16 unique commands can be issued to the device at DDA. The receiving device must, of course, be capable of decoding the pulse pattern.

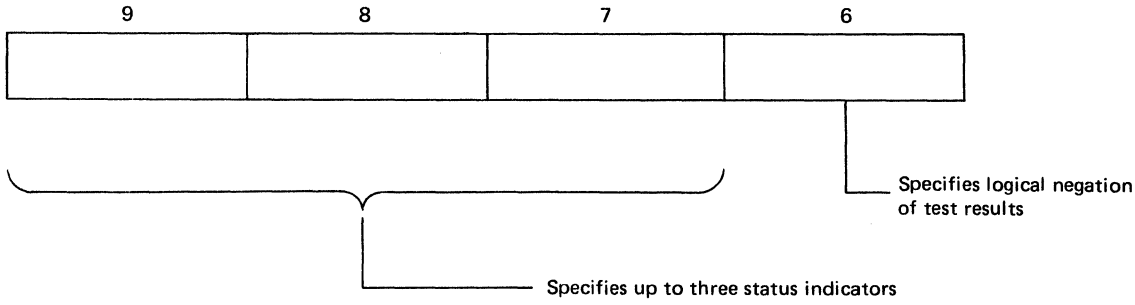
Examples:

Machine Instruction	Description
02 0001 76	Start the high-speed reader.
02 1100 13	Set the arithmetic operator to the OR state.
02 1001 77	Clear input flag and start the Teletype reader.
02 0001 00	Clear the link.
02 0010 00	Set the link.
02 0011 00	Complement the link (combines clear and set).

Refer to Tables 2-4 through 2-7.

2.2.2 Function Testing

The Function Tester, specified by Destination Device Address 02 (represented as DDA = 02), senses status indicators associated with the device at SDA. If the indicators satisfy the test specified by MOD, the control logic of the machine causes a skip of the next two locations to be performed. In other words, the next instruction to be executed is in the third location following the function testing instruction. If the indicators do not satisfy the test specified by MOD, then the instruction in the location following the function test is executed next. The MOD format is:



Any bit in MOD (9-7) = 1 selects the testing of the corresponding status indicator at SDA. If MOD (6) = 0, the test will be true if *any* of the selected indicators is on (true). If MOD (6) = 1, the test will be true only if *all* of the selected indicators are off (false).

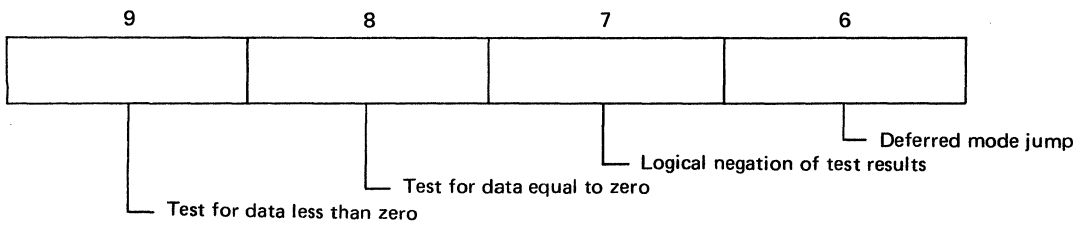
Examples:

Machine Instruction	Description
76 1000 02	Skip if high-speed reader flag on.
76 1001 02	Skip if high-speed reader flag not on.
00 0100 02	Skip if link set (= 1).
00 0110 02	Skip if link *or* bus overflow set.
00 0111 02	Skip if *neither* link *nor* bus overflow set.

Refer to Tables 2-4 through 2-7.

2.2.3 Data Testing

The Data Tester, specified by DDA = 03, tests data at SDA relative to zero. If the data test specified by MOD is true, the contents of the next location is used as a jump address. If the test is not true, the control logic of the machine skips this next location. The MOD format is:



The bits in MOD (9-7) specify the precise test that the data at SDA must satisfy in order for a jump to occur. The combinations are:

100	less than zero
101	not less than zero (greater than or equal to zero)
010	equal to zero
011	not equal to zero
110	less than or equal to zero
111	not less than *and* not equal to zero (greater than zero)

If a jump occurs, the address of the second word of the data test instruction is placed in the trap register (system address = 03) before the jump address is transmitted to the sequence counter. The contents of the trap provide a link back to the calling program if the jump was to a subroutine.

In the direct mode jump (MOD 6 = 0), the contents of the second word of the instruction is transmitted to the sequence counter (which always points to the next instruction to be executed). In the deferred mode (MOD 6 = 1), the contents of the second word is used as a memory address to fetch the jump address – this jump address is incremented, replaced in memory, and the incremented value is transmitted to the sequence counter.

Examples:

Machine Instruction	Description
11 1000 03 000125	If AX less than zero, jump to location 125.
77 0101 03 000200	If Teletype input equal to zero, jump deferred through location 200.
03 1110 03 004150	If the trap register is greater than zero, jump to location 4150.
00 0100 03 000500	Jump to location 500 (00 is as source of a zero word).

Refer to Tables 2-4 through 2-7.

Note that the trap register can be used as a source of data to be tested. This register approximates a general-purpose register because it can be loaded from memory and its contents can be transmitted to any device in the system. However, the trap register cannot be loaded from another register because *register*-to-03 is always interpreted as a data test instruction.

NOTE

If the trap is subjected to data test, remember that the contents are changed if a jump occurs.

2.2.4 Data Transmission

A Data Transmission Instruction causes the transmission of data from a source device, through the bus modifier, to a destination device. The source data is not altered unless SDA = DDA. The leftmost two modifier bits

MOD(9-8) specify simple modifications to data during transmission (see bit maps in Sections 2.2.4.1 and 2.2.4.2).

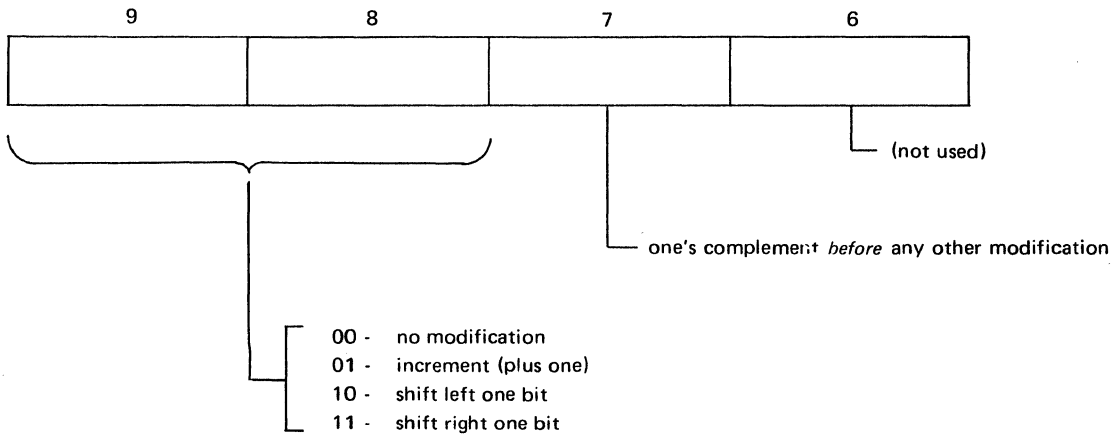
NOTE

Only one such modification may be selected in a transmission instruction.

When data are incremented, the overflow indicator associated with the bus modifier is set (true) if, *and only if,* the data being transmitted was equal to -1 (all 1's), i.e., the last increment caused an overflow into the OF bit. Otherwise, the overflow indicator is cleared. This indicator can be sensed with a Function Test instruction or a Data Test of the machine status register (BOV = MSR 15).

Data shifting in the bus modifier is *circular* through a one-bit link. For example, if data is shifted left, bit 15 (sign) of the source word goes into the link, and the initial content of the link goes into bit 0 of the data word. After a shift, the new status of the link can be sensed with a Function Test instruction. Before a shift the link can be set to 1 or 0 or complemented with a Function Generation instruction.

2.2.4.1 Non-Memory Reference Transmission – These instructions enable the transmission of data directly between system devices. The MOD format is:

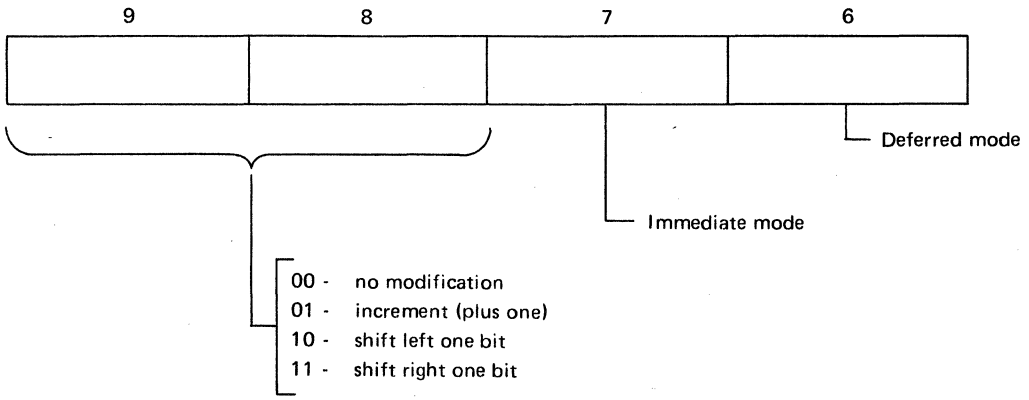


Examples:

Machine Instruction	Description
11 0000 76	Transmit contents of register AX to high-speed punch.
77 0000 77	Transmit Teletype input to Teletype output.
11 0100 11	Increment register AX.
00 0000 12	Clear register AY (00 is source of zeros).
76 0110 12	Two's complement of high-speed reader to register AY (one's complement followed by increment).
11 1000 11	Shift AX left one bit (rotate left one bit through link).
11 1100 11	Shift AX right one bit (rotate right one bit through link).

Refer to Tables 2-4 through 2-7.

2.2.4.2 **Memory Reference Transmission** – These instructions enable the transmission of data to and from memory. If SDA = 06, data is transmitted from memory. If DDA = 06, data is transmitted to memory. If SDA = DDA = 06, data is transmitted from a memory location back to itself. The MOD format is:



All Memory Reference Data Transmission Instructions are two words in length. The first word is the actual instruction. The second word is either an address of another memory location or it is a source or destination for data. The address of the memory location into which data is transmitted or from which data is transmitted is called the *effective address.* The effective address is determined by the addressing mode as specified by MOD (7-6):

Bits 7-6	Description
00	Direct mode – the contents of the second word is the effective address.
01	Deferred mode – the contents of the second word is used to fetch another address which is incremented and replaced. The incremented value is the effective address.
10	Immediate mode – the effective address is the address of the second word of the instruction.
11	Immediate and deferred mode – the contents of the second word is incremented and replaced. The incremented value is the effective address.

Examples (assume location 500 contains 1000):

Machine Instruction	Description
11 0000 06 000200	Transmit contents of AX to location 200.
06 0010 03 177776	Transmit contents of second word (-2) to the trap register – only instance of DDA = 03 that is not a data test instruction.
03 0010 06 000000	Transmit contents of Trap Register to second word – sometimes used to save subroutine linkage.
06 0110 06 000100	Increment second word.

Machine Instruction	Description
06 0001 11 000500	Transmit contents of location 1001 to register AX.
13 0011 06 001000	Transmit arithmetic output to location 1001.

Refer to Tables 2-4 through 2-7.

The deferred mode is sometimes called *one level indirect with auto-indexing.* The term *indirect* in this sense means that the address in the instruction is not the effective address but is the *address* of the effective address. The term *auto-indexing* means that the effective address is incremented before the data transmission takes place.

Table 2-4

ASSIGNED DEVICE ADDRESSES*

Device Address	Device	Device Address	Device
00	Machine Null	13	Arithmetic Operator
01	Instruction Register	14	Ext. Arithmetic Operator
02	Function Generator	17	Machine Status Register
03	Trap Register – Data Test	24	Byte Swap
04	Interrupt Status Register	25	Byte Pack
05	Memory Address	30-35	General Registers
06	Memory Buffer	57	GRI-sette
07	Sequence Counter	62	Interval Timer
10	Console Switch Register	75	Real-Time Clock
11	AX Register	76	High-Speed Reader/Punch
12	AY Register	77	Teletype I/O

*For a complete list of device addresses refer to Appendix B.

Table 2-5

GRI-909 INSTRUCTION SUMMARY

Class	Devices		MOD Bits				Effect
	SDA	DDA	9	8	7	6	
Register Transfers	Any Except 06	Any Except 06	0	0	0	0	None
			0	–	–	0	Increment
			1	0	–	0	Left One Bit
			1	1	–	0	Right One Bit
			–	–	1	0	1's Compl. Before Bits 8,9
Memory Transfers	06 to Any Any to 06, 06 to 06		Same As Reg. Xfer		0	0	Direct
					1	0	Immediate
					0	1	Deferred
					1	1	Immediate-Deferred
Jumps (Data Tests)	Any Except 06	03	0	0	1	–	Always Jump
			0	1	0	–	ETZ
			0	1	1	–	NEZ
			1	0	0	–	LTZ
			1	0	1	–	GEZ
			1	1	0	–	LEZ
			1	1	1	–	GTZ
			–	–	–	1	Deferred
Skips (Function Tests)	00	02	0	0	1	–	BOV (Bus Overflow)
			0	1	0	–	LNK
			1	0	0	–	POK (Power OK)
	13		0	0	1	–	AOV (Arith. Overflow)
			0	1	0	–	SOV (Sum Overflow)
	76 or 77		1	0	0	–	IRDY
			0	0	1	–	ORDY
	Any		–	–	–	–	Depends on Device
			–	–	–	0	Skip if Any Tests True
			–	–	–	1	Skip if No Tests True
Control Signals (Function Generation)	02	00	0	0	0	1	CLL (Clear Link)
			0	0	1	0	STL (Set Link)
			0	1	0	0	HLT
		13	0	0	1	1	CML (Complement Link)
			0	0	0	0	ADD
			0	1	0	0	AND
		14	1	0	0	0	XOR
			1	1	0	0	OR
			0	0	0	1	Multiply
			0	0	1	0	Divide
		04	0	0	1	1	Arithmetic Rt. Shift
			0	1	0	0	Normalize
			0	0	0	1	ICF (Int Control off)
			0	0	1	0	ICO (Int Control on)
		76 or 77	0	0	0	1	STRT
			1	0	0	0	CLIF (Clear IRDY)
			0	0	1	0	CLOF (Clear ORDY)
		Any	–	–	–	–	Any Control Function

Table 2-6

GRI-909 INSTRUCTION EXAMPLES

Class	Sample Machine Instruction	Description
Function Generate	02 0001 77	Start Teletype paper-tape input.
	02 1100 13	Select Arithmetic Operator OR function.
Function Test	77 0011 02	Skip if Teletype input not ready.
	13 0010 02	Skip if arithmetic operation caused overflow.
Data Test	77 0100 03 jump address DONE	If Teletype input equal to zero go to DONE
	13 1110 03 jump address ALARM	If arithmetic result greater than zero, go to ALARM.
Data Transmission		
Non-Memory Reference	35 0100 35	Increment the multiplexer address register.
	77 0000 76	Transmit Teletype input character to the high-speed punch.
	51 0110 12	Transmit the two's complement of the analog/digital converter register to the Y register for a comparison with a limit value in the X register.
Memory Reference	06 0000 11 address UPLIM	Transmit upper limit value to X register.
	03 0010 06 destination	Store trap register immediately.
	06 0100 06 address COUNT	Increment value of counter.
	06 0010 35 operand 12	Transmit an immediate constant (12) to the multiplexer.

Table 2-7

INSTRUCTION TIMES

Class	Length (words)	Memory Cycles	Time (μs)
Function Generate	1	1	1.76
Function Test			
Skip	1	1	1.76
No Skip	1	1	1.76
Data Test			
No Jump	2	1	1.76
Jump Direct	2	2	3.52
Jump Deferred*	2	3	5.28
Data Transmission			
Non-Memory Reference	1	1	1.76
Memory Reference			
direct	2	3	5.28
immediate	2	2	3.52
deferred*	2	4	7.04
immediate – deferred*	2	3	5.28

* The deferred mode selects one level of indirect addressing with auto-indexing; the indirect address is incremented prior to instruction execution.

CHAPTER 3
THEORY OF OPERATION

Chapter 3 contains the Theory of Operation for the GRI-909 Computer. The basic computer elements and the power supply are explained in detail, as well as in relation to the total system.

3.1 PHYSICAL ARCHITECTURE

The physical organization of the basic GRI-909 package is shown in Figure 3-1. The framework is of extruded anodized aluminum and serves both as a caged grounding scheme and as guides for the printed circuit cards in the system. The console is enclosed by the hinged door on the front of the cabinet. All the console switches and indicators with associated driving and sensing circuits are mounted on the door.

All back panel wiring inside the frame is on printed circuit (PC) cards with PC card sockets soldered onto them. As a result. one card is plugged directly to another card. *No wire wrapping or point-to-point wiring is used anywhere in the system.* The processor bus has connectors for nine 9-in. by 13-in. plug-in cards, three of which are available for large firmware operators, such as the arithmetic operator. The I/O bus has sixteen positions for 9-in. by 4-in. cards for smaller firmware or device operators. The memory bus is used for core memory modules.

3.2 BUS SYSTEM

To achieve functional modularity, the machine architecture is designed around a dual bus arrangement (see Figure 3-2). All functional operators in the system are interfaced to these buses, which provide communication and control paths from one operator to another. As shown in Figure 3-2 when a 16-bit data word is to be transmitted from Device X to Y, Device X places the data onto the lower bus, the Destination Bus. These data are then passed to the upper bus, the Source Bus, through a short circuit path between the buses, and then sent to Device Y. A 16-bit data transmission as just described is the most basic operation performed in the machine and is referred to as a *microinstruction* Data are transmitted by the stored program and also by the built-in machine control to perform various bookkeeping tasks. Each of these transfers requires 440 ns.

The Source Bus and the Destination Bus each contain 44 conductors that can be grouped into three major categories:

a. 16 lines are used for the data paths
b. 6 lines for selection of the operator
c. 22 lines provide control

The format of the 16-bit data transmission instruction word is also shown in Figure 3-2. The left-most six bits of this instruction word select a Source Device Address (SDA). These six bits are impressed upon the six address lines of the Destination Bus to select one operator as a data source. The right-most 6 bits of the instruction word appear on the six address lines of the Source Bus to select the Destination Device Address (DDA).

3.2.1 Busing Scheme

The busing scheme and connections internal to the main chassis are shown in Figure 3-3. All PC cards shown in the lower row are of the larger size (9-in. by 13-in.). The processor is contained on three large cards, labeled PC1, PC2, and PC3. The PD buffer board provides the buffering and cable connection to the console. The MR board contains the MA and MB registers, memory timing and controls, and a connection, via flat cable and the MR connector card, to the memory bus. Core memory cards are the largest cards used and contain the core planes, and all read, write, inhibit and sense circuitry. Three connectors are available in the processor bus for the addition of firmware operators.

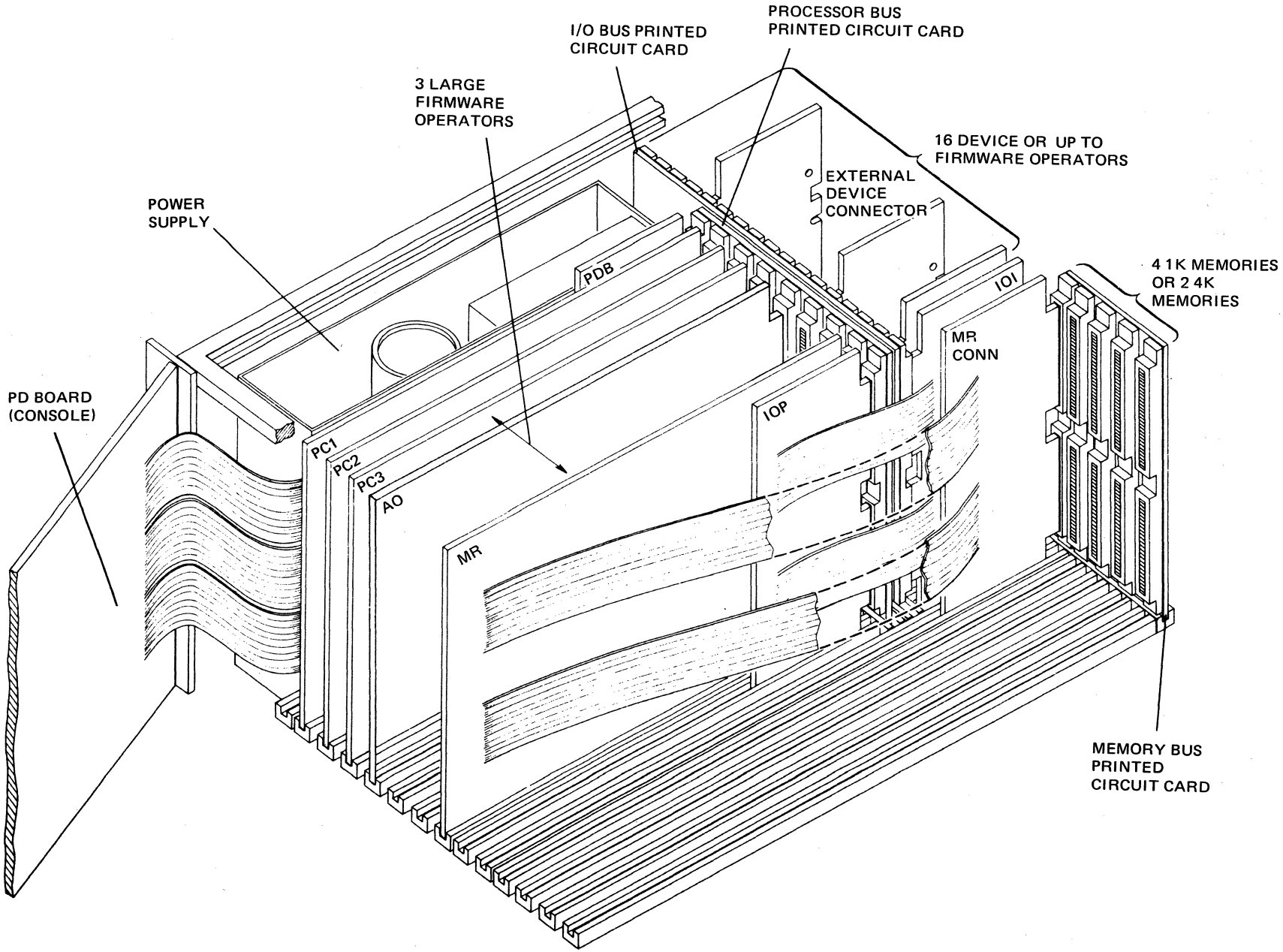


Figure 3-1 Physical Organization of the Basic GRI-909 Package

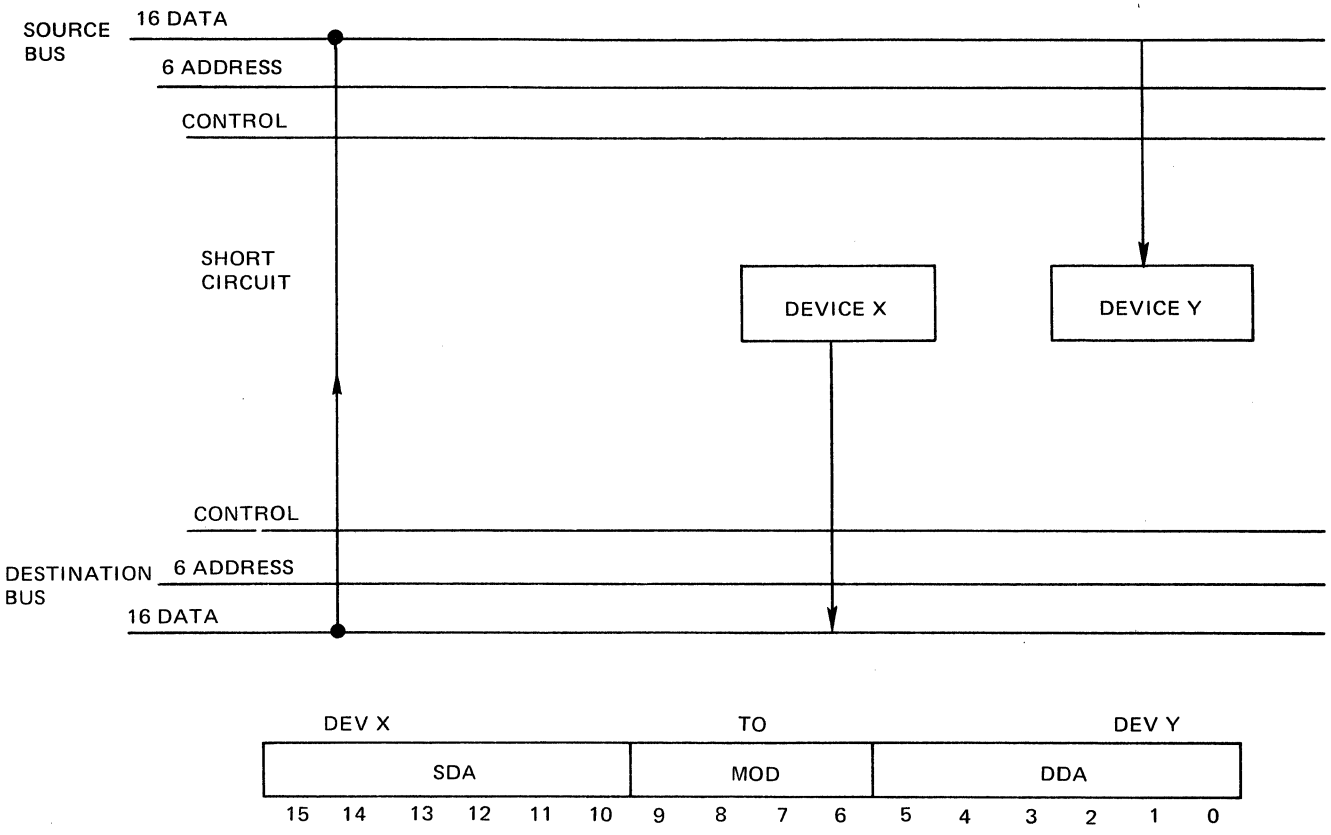


Figure 3-2 Basic Machine Microinstruction

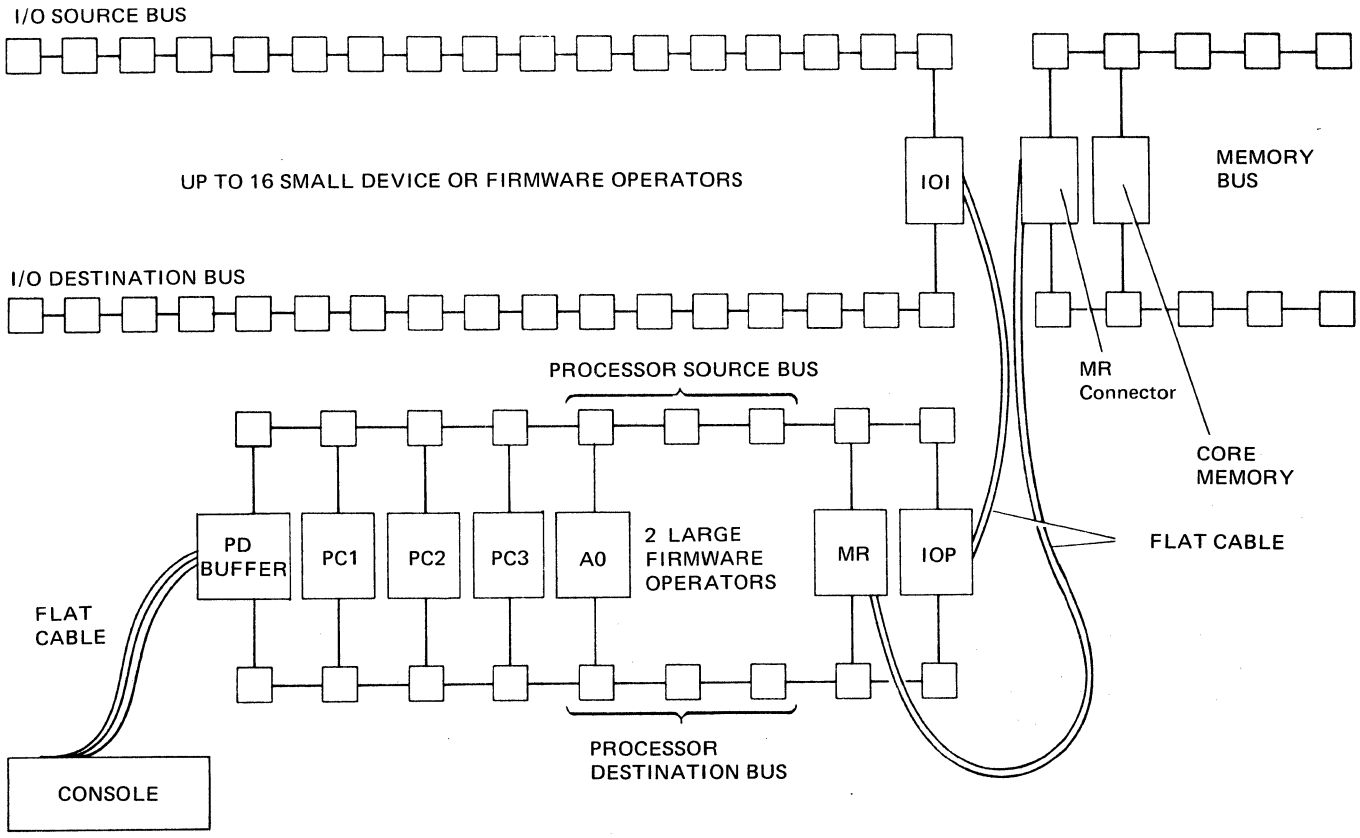


Figure 3-3 System Busing

The IOP and IOI cards have flat cable between them to connect the processor bus to the I/O bus. Drive circuits on these cards provide signal isolation between the two buses, and decoders provide special operator code signals to the I/O bus that are not available on the processor bus. These signals are used for interrupt, direct memory access (DMA) control and external instruction processing. Space for decoding these signals directly from source address lines (SAB) and destination address lines (DAB) is more readily obtained on the large firmware cards than the small I/O cards.

Both the processor bus and the I/O bus are actually each two buses: source and destination. In general, the destination bus is associated with output from system operators, whereas the source bus is the source of data and control information for input to system operators.

All connections between the buses and the console are made with multiconductor flat cable attached at both ends to PC cards. Expansion chassis to extend the memory bus and the I/O bus are of the same type of construction as the mainframe. These expanders are placed either above or below. Flat cable connects the buses.

3.2.2 Bus Schematic

Figure 3-4 is a bus schematic of the basic GRI-909 configuration. Except for most of the power wiring, all system signals are distributed via the printed bus board. Some of the signals and signal groups shown in the schematic are private communications signals between the three major control assemblies (PC1, PC2 and PC3) that make up the basic processor. There are also private communications signals that go between the PD board, via the PDB cable buffer card, specifically to operate the console control switches and state indicators. The power supply delivers voltages and control signals to the bus via wired fast-tab connections that are made to the main processor bus. From PC3 through the last slot on the main processor bus, the signals become the system signals that are distributed in parallel through the entire system, including the I/O bus section in the rear of the machine. These signals are distributed to the I/O bus section via a cable and buffer card assembly called the IOP/IOI *processor bus buffer.* Note that the majority of signals that arrive at the back panel bus of the processor via this card are still identical to the processor signals used internally and, therefore, facilitate the use of internal options plugged into these slots, as well as I/O options.

All connections to the main processor bus or the I/O bus assembly are made by 44-pin connectors. Signal Origin drawings are connector lists that describe all the bus signals that appear on the connectors at the various slots in the main processor. These drawings, located in a separate volume titled *GRI-909 Engineering Drawings,* in addition to showing the connector pin number and the signal name, also contain:

a. Brief descriptions of the signal functions

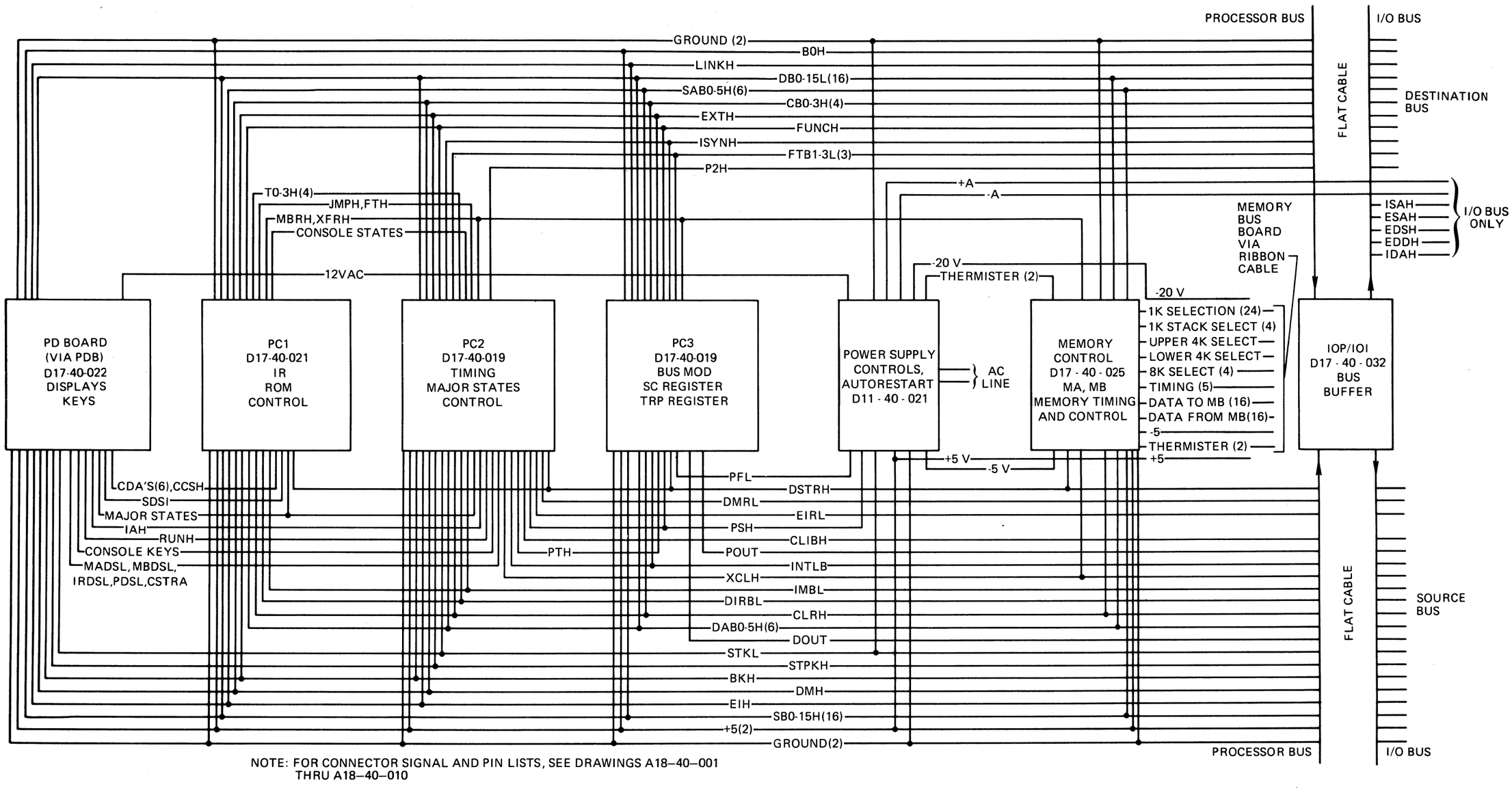
b. Whether the signal is originated on the board described on the drawing.

c. Whether the signal is simply used on that board, or whether the signal contains bus drivers that are ORed onto one of the common buses that runs through the system.

In general, all signals with the suffix *L* are bus type signals that are driven from many points throughout the system by open collector gates. Exceptions to this rule can be found by observing whether the signal is marked in the *Origin* column or the *Used* column. A bus-type signal has more than one origin. If the signal is a bus-type and the *Used* column is marked, this notation indicates a point of termination of the signal.

3.2.3 Source and Destination Bus Signals

Usually, the Source and Destination Bus signals are treated of in block diagram discussions of GRI-909 architecture. This treatment excludes communication paths between PC1, PC2, PC3, MR, PDB, and the power supply. The signals discussed in this section are found on the Source Bus connectors and Destination Bus connectors in the three large card-option slots on the processor bus and the 16 small card-option slots on the I/O bus.



NOTE: FOR CONNECTOR SIGNAL AND PIN LISTS, SEE DRAWINGS A18–40–001 THRU A18–40–010

Figure 3-4 Bus Schematic

Figures 3-5 and 3-6 are diagrams of the two connectors, showing pin numbers and signals as they would appear looking into the processor at the bus board. Those signals marked by an asterisk (*) appear only on the I/O bus connectors. A short explanation of the signals is given in Table 3-1.

SOURCE BUS CONNECTOR

Ground	1	A	Ground
+5V	2	B	+5V
CLRH	3	C	EIH
DMH	4	D	BKH
PINL	5	E	POUTL
DINL	6	F	DOUTL
DAB1H	7	H	DAB0H
DAB3H	8	J	DAB2H
DAB5H	9	K	DAB4H
DSTRH	10	L	XCLL
CL1BH	11	M	INTBL
IMBL	12	N	DIRBL
STPKL	13	P	STKL
EIRL	14	R	DMRL
SB01H	15	S	SB00H
SB03H	16	T	SB02H
SB05H	17	U	SB04H
SB07H	18	V	SB06H
SB09H	19	W	SB08H
SB11H	20	X	SB10H
SB13H	21	Y	SB12H
SB15H	22	Z	SB14H

Figure 3-5 Source Bus Connector

DESTINATION BUS CONNECTOR

DB01L	1	A	DB00L
DB03L	2	B	DB02L
DB05L	3	C	DB04L
DB07L	4	D	DB06L
DB09L	5	E	DB08L
DB11L	6	F	DB10L
DB13L	7	H	DB12L
DB15L	8	J	DB14L
SAB0H	9	K	ISYNH
SAB1H	10	L	FTB1L
SAB2H	11	M	FTB2L
SAB3H	12	N	FTB3L
SAB4H	13	P	LINKH
SAB5H	14	R	B0H
IDAH*	15	S	P2H
EASH*	16	T	ISAH*
EDDH*	17	U	EDSH*
EXTH	18	V	FUNCH
CB3H	19	W	CB2H
DB1H	20	X	CH0H
-A	21	Y	+A
Ground	22	Z	Ground

* APPEAR ONLY ON I/O BUS CONNECTORS

Figure 3-6 Destination Bus Connector

Table 3-1

SOURCE AND DESTINATION BUS CONNECTOR SIGNALS

Signal	Direction	Description
Source Bus		
EIH	Out	External Instruction: the processor external instruction cycle.
CLRH	Out	Clear: system clear level generated by the START key or power on or off.
BKH	Out	Break: the processor interrupt cycle.
DMH	Out	Direct Memory: the processor direct memory access (DMA) cycle.
POUTL	Out	Priority Out: the serial interrupt priority determining level out of an operator.
PINL	Out	Priority In: the serial interrupt priority determining level into an operator.
DOUTL	Out	DMA Out: the serial DMA priority-determining level out of operator.
DINL	Out	DMA In: the serial DMA priority-determining level into an operator.
DAB0H-DAB5H	Out	Destination Address Bus: the 6-bit address of the destination operator.
XCLL	Out	Crystal Clock: a square wave with a 110 ns period.
DSTRH	Out	Data Strobe: used by an operator to gate in data from the Source Bus.
INTBL	In	Interrupt Bus: a common line for all operators to request an interrupt.
CLIBH	Out	Clear Interrupt Bus: clears the DMA device service flip-flop in the requesting device.
DIRBL	In	Direction Bus: indicates data transfer direction for DMA (0V = in, +4V = out)
IMBL	In	Increment Memory Bus: increment the memory location during a DMA cycle.
STKL	In	Start Key: external START request.
STPKL	In	Stop Key: external STOP request.
DMRL	In	Direct Memory Access Request: a common line for all operators to request DMA.
EIRL	In	External Instruction Request: a common line for all operators to request an external instruction cycle.
SB00H-SB15H	Out	Source Bus Data: the 16 data lines in the Source Bus.
Destination Bus		
DB00L-DB15L	In	Destination Bus: the 16 data lines in the Destination Bus.
ISYNH	Out	Interrupt Sync: generated in each cycle to synchronize interrupt and DMA requests by operators.
SAB0H-SA511	Out	Source Address Bus: the 6-bit address of the Source operator.
FTB1L-FTB3L	In	Function Test Bus: operators use these lines for status input during an SF instruction.
LINKH	Out	Link: the link bit associated with the bus modifier.
BOH	Out	Bus Overflow: the Bus Overflow flag associated with the bus modifier.

Table 3-1

SOURCE AND DESTINATION BUS CONNECTOR SIGNALS (Cont.)

Signal	Direction	Description
P2H	Out	Time 2 Pulse: strobe that gates FO commands into an operator or T1 and T3 during EI operation.
IDAH	Out	Interrupt Destination Address: the destination address is 04, the interrupt status register.
EASH	Out	External Address, Source: the source address is 16, the DMA address register or interrupt address generator.
ISAH	Out	Interrupt Source Address: the source address is 04, the interrupt status register.
EDSH	Out	External Data, Source: the source address is 15, the DMA data register or logic that supplies an external instruction from a ROM.
EDDH	Out	External Data, Destination: the destination address is 15, the DMA data register.
FUNCH	Out	Function: the current processor instruction is an SF or an FO.
EXTH	Out	Execute Time: T2, during which the programmed transfer occurs or T1 and T3 during EI operation.
CBOH-CB3H	Out	Control Bus: lines that transmit control bits in an FO instruction.
+A,-A	Out	Unregulated voltage (26V-35V) for use in local regulators.

3.3 PROCESSOR ELEMENT DESCRIPTION

3.3.1 Bus Modifier

The four center bits of the instruction word are used to specify data modification as data are passed from the Destination Bus to the Source Bus, as shown in Figure 3-7. The short circuit path contains an arithmetic unit called the *bus modifier.* During data transmission, the data can be complemented, incremented, shifted left 1 bit, or shifted right 1 bit. An overflow (OV) flip-flop stores a binary carry out of the sixteenth bit caused by incrementing a data word of all 1's. Both right and left shifts are done in a circular fashion through the link (L) flip-flop. Following a shift during data transmission, one bit of the source data is retained in the link, and the bit initially in the link is passed on as part of the data word to the destination device. Path control through the bus modifier, as well as the Bus Overflow (BOV) and Link Bit (L), is located on PC3.

3.3.2 Sequence Counter (SC)

A device is provided to keep track of the program information. This Sequence Counter (or program counter) is common to all computers and indicates the address of the next instruction.

In the GRI-909, the Sequence Counter is connected across the buses, as are all other elements in the system, providing direct access from device to device.

The system address of the SC is 07. The SC is always preset to a value of 6_8 when power is first applied to the processor by the signal PSH. All logic associated with the SC is located on PC3.

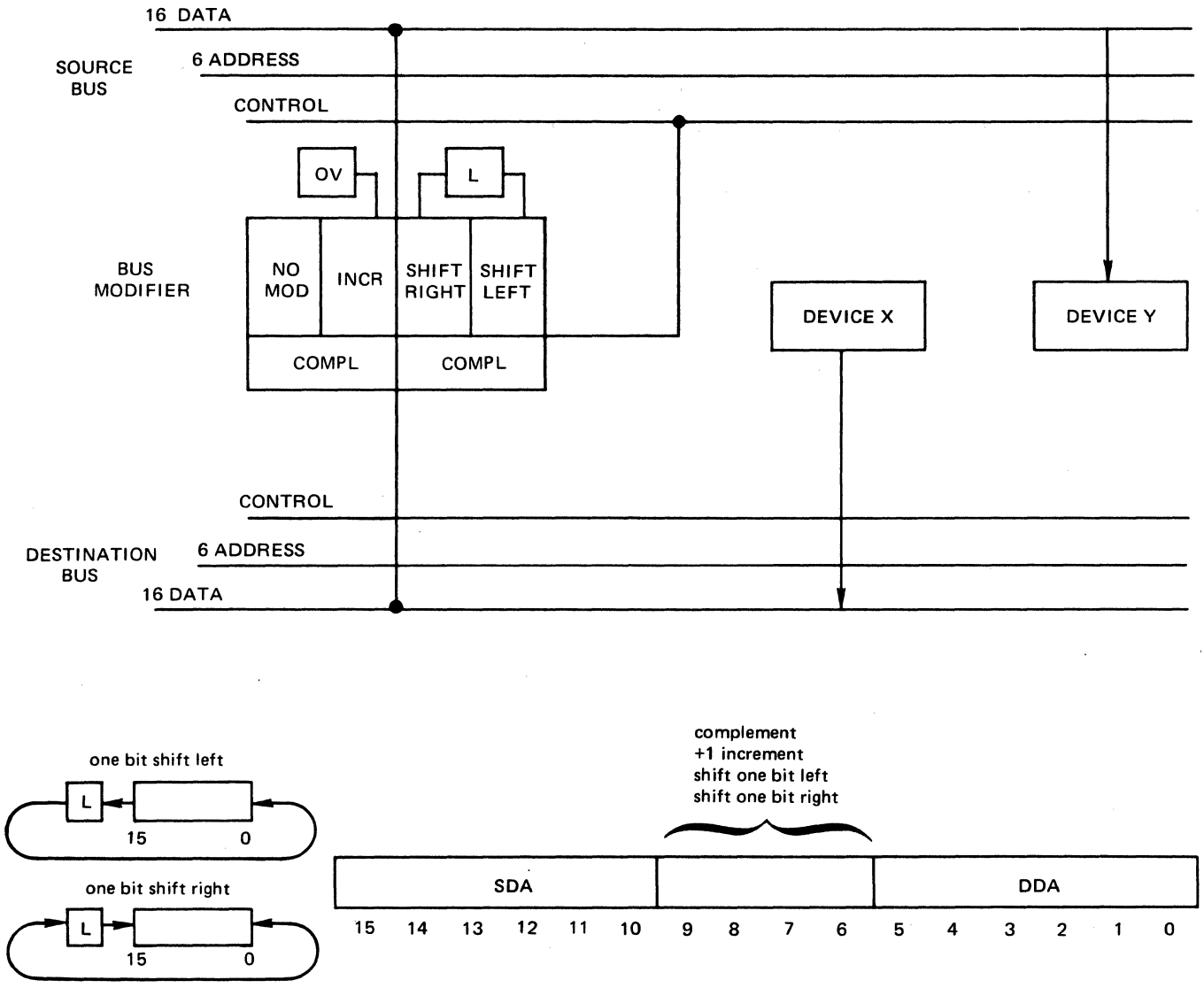


Figure 3-7 Data Modification During a Microinstruction

3.3.3 Instruction Register (IR)

The Instruction Register contains the current instruction in the computer to be executed. As the other elements in this system organization, the IR is connected across the Source and Destination Buses.

The system address of the IR is 01. All logic associated with the IR and decoding the IR is located on PC1.

3.3.4 Data Tester

A computer must decide on the paths that it will follow, based on the value of the data that it receives. In the GRI-909, the Data Tester uses the modifier code bits to determine the value of the information it receives, i.e., less

than zero, equal to zero, or any combination thereof. This tester is connected between the Source and Destination Buses and is programmed to accept data directly from any source. A positive response to a data test results in a jump instruction. The contents of the Sequence Counter are automatically stored in a trap register associated with the Data Tester when a jump is executed.

The system address of the Data Tester is 03. The trap register associated with the Data Tester can be utilized for transfers from memory and carries the same address of (03). The logic associated with the testing of data is located on PC2 and the trap register is located on PC3.

3.3.5 Function Tester

Peripheral devices produce status signals that indicate particular conditions to the computer. The GRI-909 contains a Function Test Operator that compares status signals to the modifier bits and acts on the result.

Three control lines are provided for this purpose, plus a fourth line, which provides logical negation of the other three. A positive response by the Function Test Operator to the sense lines results in a skip instruction.

The system address of the Function Tester is 02. All logic associated with the Function Tester is located on PC2.

3.3.6 Function Generator

The Function Generator is used by the program to perform specific tasks in the destination operator. The function generation process is accomplished by pulsing certain control lines selected by bits 6 through 9 of the instruction word. An example of the use of the function generator is:

02 1000 76

This instruction causes the high-speed reader to read the next character on tape. Another example of function generation is shown in Section 3.3.7.

The source device address of the Function Generator is 02. The logic for the Function Generator is located on PC1.

3.3.7 Arithmetic Operator (AO)

The arithmetic and logical manipulations that can be performed in the functional Arithmetic Operator are ADD, AND, OR, and EXCLUSIVE OR (XOR). The arithmetic operator of the GRI-909 operates somewhat differently from from that of a typical computer. In the GRI-909, no instructions are issued that say "ADD". A conventional computer ADD instruction translates as, "one number is in the accumulator and the other number is in memory. Pull the number out of memory, add the number in the accumulator to the number in memory, and put the sum back into the accumulator."

In the GRI-909, the Function Generator is used to generate the ADD function. The instruction can be shown as:

Function Output ADD ——————→AO

This element always performs the ADD function between the current value of the X and Y registers until the user issues another command changing the state. When either of those registers is changed, a new sum appears, immediately available for transfer to any point in the system. New values can be presented from a system register, and a new result can be obtained in a single cycle time, 1.76 μs. The result, contained in a separate accumulator register (AO), always reflects the instantaneous output generated by the contents of the X and Y registers as controlled

by the function selected. It can be stored in memory by a single instruction. The introduction of new values to one register does not alter the contents of the other register. The AO is considered a firmware operator; consequently, all logic concerned with the implementation of the functions is located on the AO module.

3.3.8 Machine Status Register (MSR)

Certain flag and control flip-flops in the computer are connected to the Source and Destination Buses in such a way that their states can be saved and then restored as though they were bits in a full-word register. This register is referred to as the MSR, which can be addressed as device address 17. The logic associated with the MSR is on PC3 and the AO.

3.3.9 Interrupt Status Register

Priorities of interrupts are determined by a combination of the program-controlled interrupt status register (ISR), which is a mask register, and hardware position on the bus processor.

Each operator with interrupt capability contains an Interrupt Allow flip-flop, which can be set and cleared under program control. When this flip-flop is set, the operator can interrupt, if desired. However, if the Interrupt Allow flip-flop is clear, the operator cannot interrupt under any circumstances These Interrupt Status flip-flops, although distributed throughout the system, are collectively called the Interrupt Status Register. The device address is 04. This register is both a source and destination of data; thus the programmer can save the current interrupt status in memory with one instruction and set new priorities with another instruction.

3.3.10 Memory Address (MA)

This register holds the address of the word being read from or written into memory. Unlike the SC, the MA is used as a pointer during the different modes of addressing. All logic for decoding the MA is located on the MR module.

3.3.11 Memory Buffer (MB)

The MB holds the data being written into and read out of memory. All logic pertaining to the MB is located on the MR module.

3.4 PROCESSOR TIMING

The basic clock frequency in the GRI-909 is provided by a 9.09 MHz crystal clock (Y1). This clock produces a signal (XCLL) that is distributed throughout the system on source bus pin L. The origin of the clock is on PC2. The basic clock period is 110 ns. This period is counted and expanded by four to produce the 440 ns microcycle timing (T0, T1, T2, T3). A timing chart demonstrating this relationship is shown in Figure 3-8. The four micro-cycles within the basic memory cycle are shown with a 110 ns strobe occuring during the last 110 ns of each microcycle, except T0, which occurs 110 ns earlier , and T1, which occurs 60 ns earlier. All clocking of flip-flop registers is done with these strobe pulses. DC flip-flops change state on the leading edge and J K flip-flops on the trailing edge. The 330 ns between the trailing edge of one strobe and the leading edge of the next is used for propagation and settling time through gates.

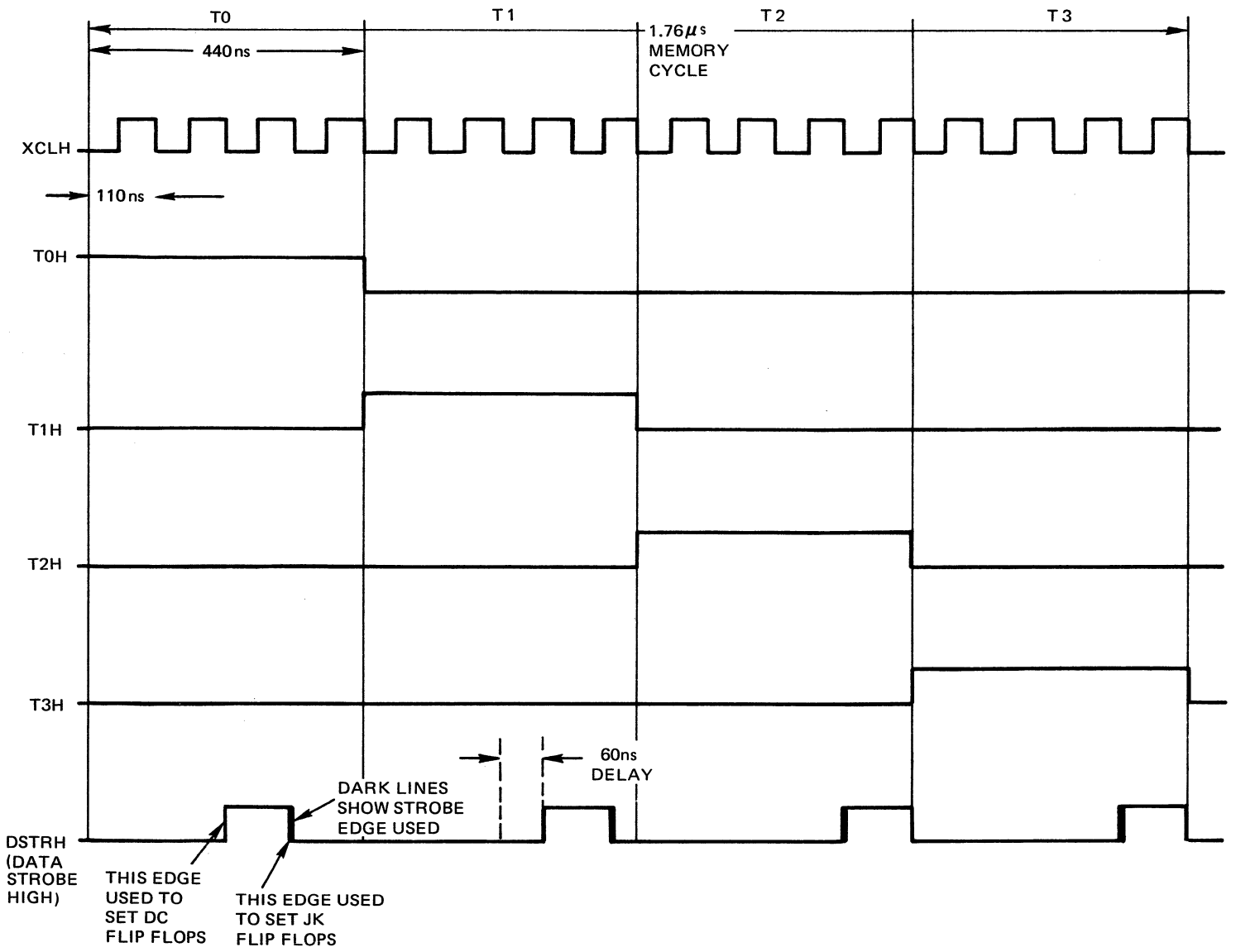


Figure 3-8 Nominal Processor Timing

3.5 MEMORY OPERATION

3.5.1 READ

When the destination of data is device address 05 (DDA = 05) during the execution of a microinstruction, the following occurs:

a. MSTRL is generated.

b. 60 ns later, the memory address is decoded and the MA sets up the sinks, drives and MEM SELECT signals.

The signal MSTRL starts the memory timing chain, which is synchronized with processor timing but runs independently. When the memory timing chain starts, the MB is cleared. After MSTRL is no longer present, SSRH is generated. SSRH in conjunction with the sinks and drives senses memory.

At this time, the DATA STROBE pulse gates the sense lines into the memory buffer register. The MB is used for intermediate storage in this case, because the contents of memory have been destroyed by the sense operation.

3.5.2 Write

On completion of the read operation, the memory timing chain sets the RD flip-flop, which generates the signal WRH. Prior to this time, the data word could have been changed in the MB and the new word written into memory if the instruction warranted.

WRH then enables the Z strobe signal ZSTRH and the signal SSWH. ZSTRH enables the inhibit lines and gates the contents of the MB register to the inhibit drivers. The signal SSWH in conjunction with the sinks and drivers actually performs the write function into core memory at the specified address. At the end of this sequence, the RD flip-flop is cleared to prepare for another operation. Figure 3-9 shows the 1K memory for the GRI-909. Figure 3-10 shows the 4K memory.

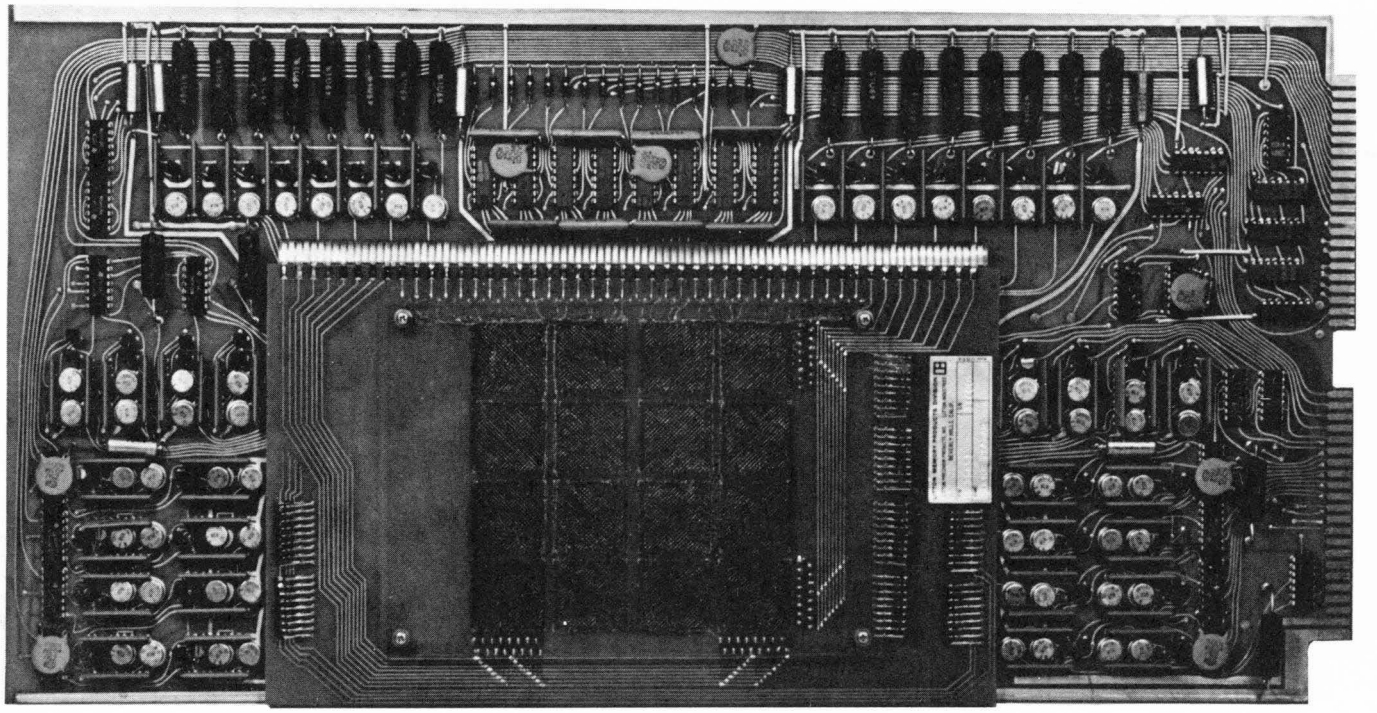


Figure 3-9 1K Memory

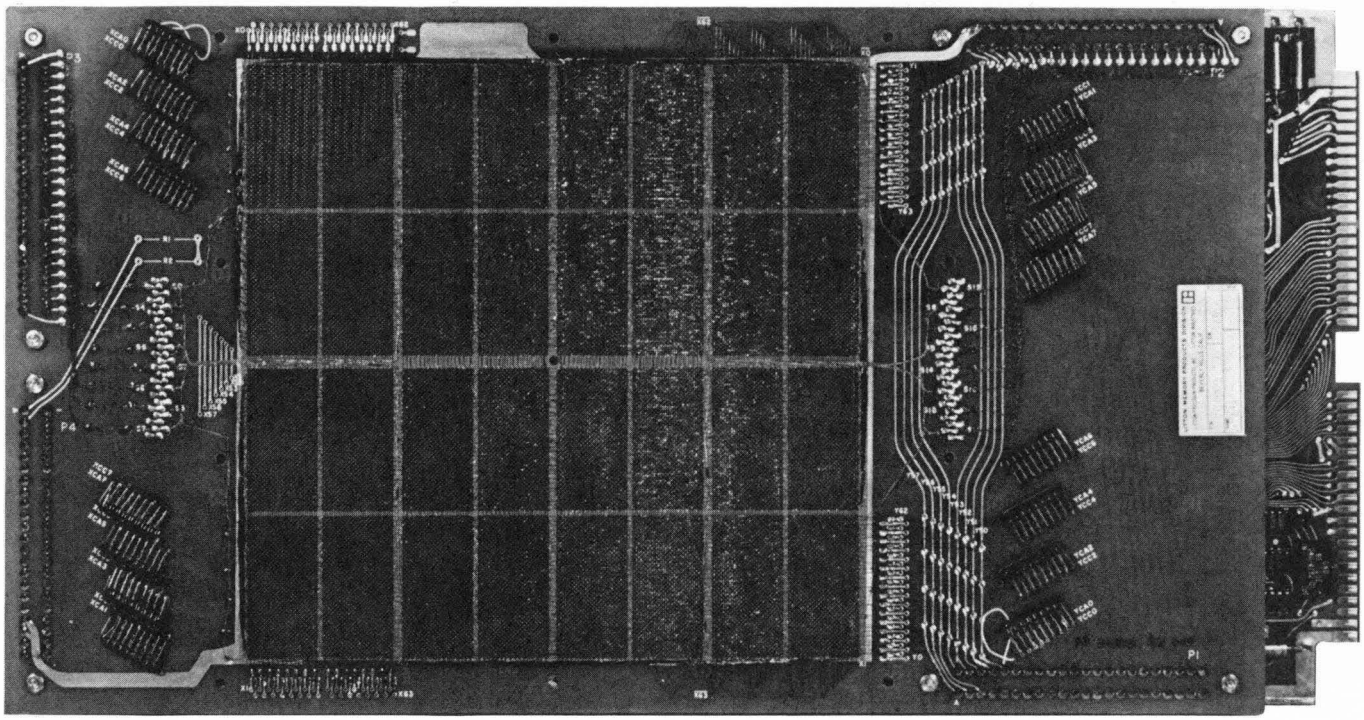


Figure 3-10 4K Memory

3.5.3 Sinks and Drives

As shown in Figure 3-11, one drive is serviced by eight sinks. The sink is selected through the MA register. In the grid portion of the illustration, the intersection of lines represents coordinates of the actual core locations in memory. Each intersection specified 16 discrete core locations. There are four X-drive lines and four Y-drive lines; the upper part of the illustration shows the X-Y selection, as determined by the bits in the memory address.

3.6 MEMORY TIMING

The memory system has its own timing that is run off the processor clock (XCLL), appearing on the processor bus. Thus, memory timing is synchronized with the processor timing but is run as an independent timing chain. Initialization of the timing chain in memory occurs when the processor transmits a request for a memory cycle. The memory decodes this request when it recognizes the MA addressed as a destination of data. This condition always occurs during time slot zero (T0), the first of the four 440 ns time slots that constitute a memory cycle (1.76 μs).

This decoded signal starts the memory timing chain, which subsequently results in one complete memory cycle. Figure 3-12 is a timing diagram showing the occurrence of memory read and write times relative to the processor timing.

3.7 INSTRUCTION EXECUTION

Chapter 2 discussed the instructions used by programmers to perform a task within a program. Those instructions are referred to as *macroinstructions.* In the GRI-909, it is necessary to execute a group of microinstructions to complete a macroinstruction. The microinstructions are in the same format as macroinstructions; the only difference between the two instructions is the source of the microinstruction and the speed at which it is executed.

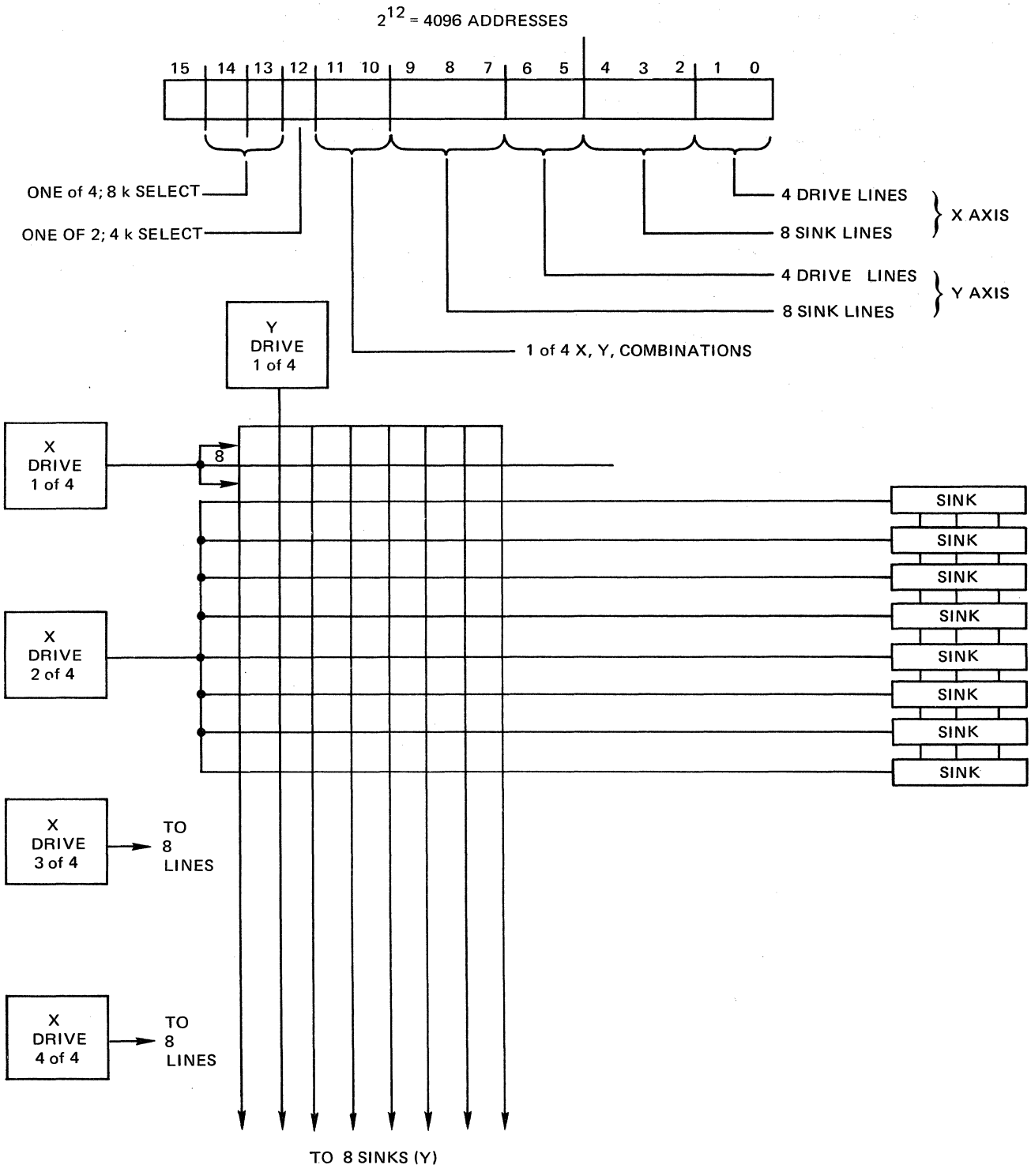


Figure 3-11 Memory Address Selection

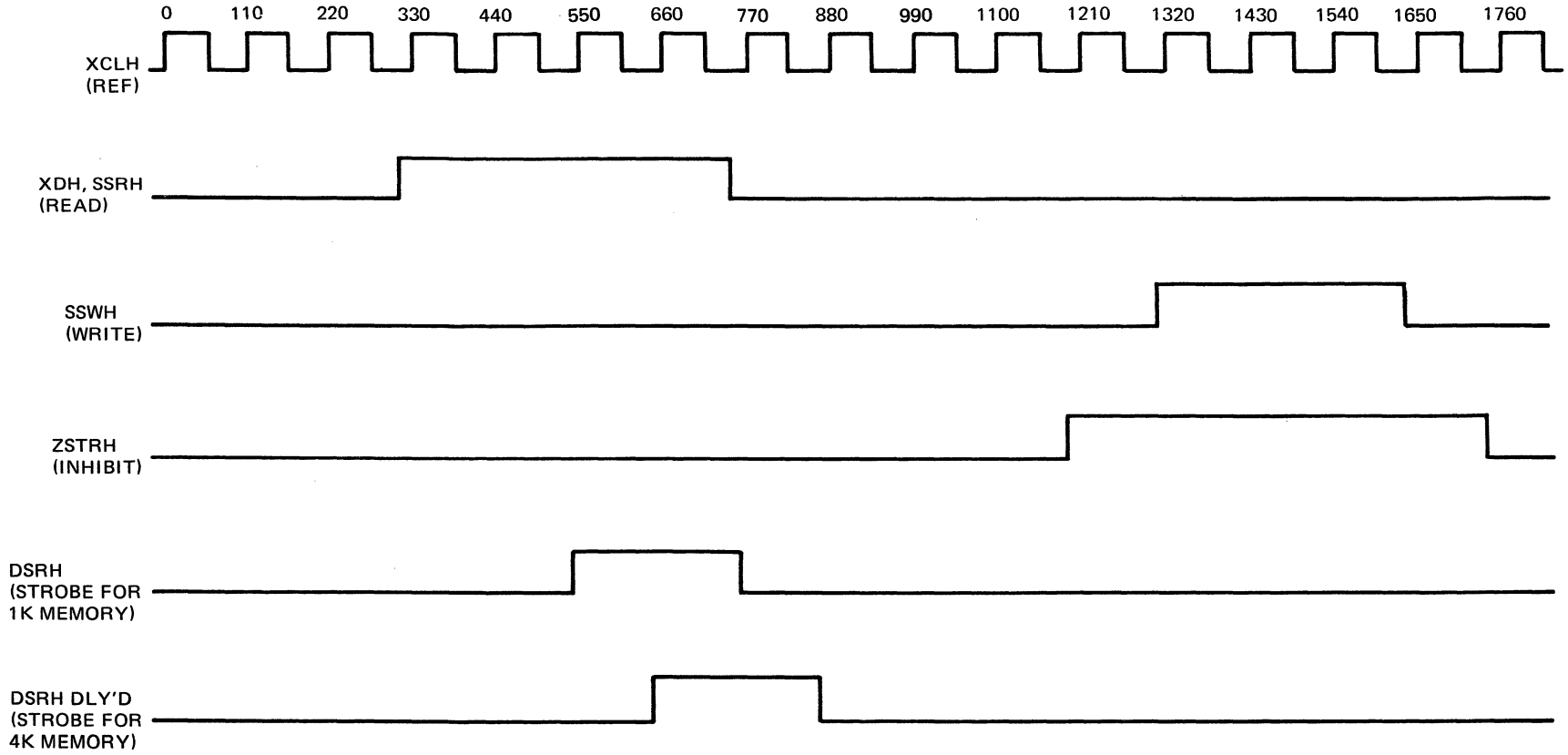


Figure 3-12 Nominal Memory Timing

The GRI-909 macroinstruction set includes the instructions that require 1, 2, 3, or 4 major states to complete. In addition, the interrupt, direct memory access, and external instruction states are three more major states. When power is applied to the processor, it is in the F1 state. During each state, one memory cycle is executed. Each state is given a two-letter designator, as follows:

FI	Instruction cycle 1
FA	Instruction cycle 2
FO	Instruction cycle 3
FD	Instruction cycle 4
BK	Break cycle
DM	Direct memory access cycle
EI	External instruction cycle

Figure 3-13 is a state flow diagram showing priorities and all possible paths between machine cycles.

The mnemonics INTB, EIR, and DMR are used to represent the request signals for the Break, External Instruction, and Direct Memory Access cycles respectively. The End State, Halt State and Console Stop State are not separate machine states but merely conditions that exist within the processor, while the processor is in the state. Note that these states represent stop states for the machine, and no new memory cycle is initiated.

During each memory cycle, up to four microinstructions can be performed using either the instruction register or the processor's ROM as a microinstruction source. The technique of transferring 16 bits of data from a source to a destination was discussed in detail in Chapter 2.

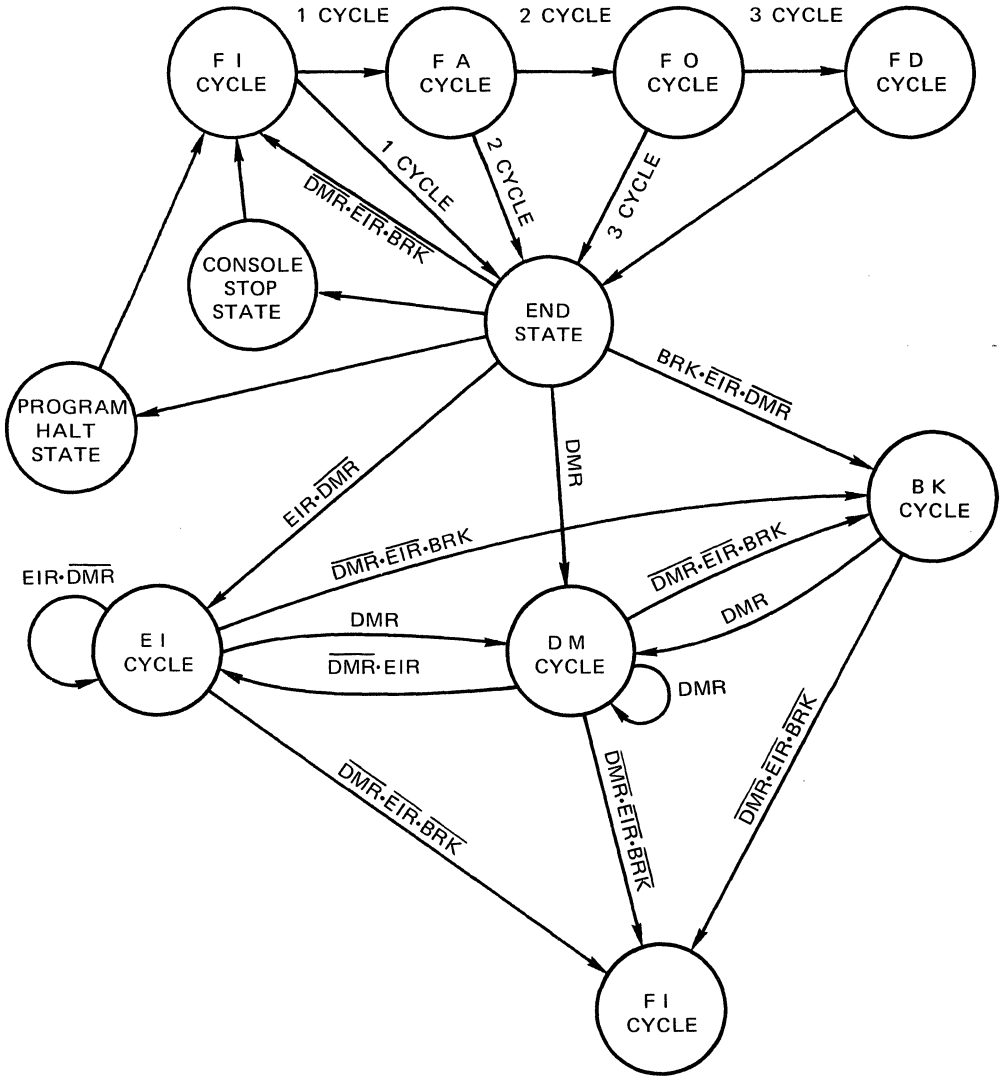
At the start of the memory cycle (T0), the instruction word is in memory and the control logic has no indication of what the macroinstruction will be. A data transfer of SC to the memory address (MA) register is made to read the macroinstruction from memory. During the next period (T1),the instruction word read from memory into the MB is transferred through the bus modifier unaltered to the instruction register (IR). At the end of T1, the control logic receives the macroinstruction the programmer wishes to perform (e.g., a data transfer from SDA to DDA). During T2, the transfer is performed. To prepare for the next instruction, the SC must be incremented. During T3, the SC is transferred to itself and incremented as it passes through the bus modifier.

Every macroinstruction is implemented in this manner with 1, 2, 3, or 4 memory cycles and various microinstruction sequences. These sequences are stored in a read only memory (ROM), which is part of the basic machine control logic. The arrangement shown in Figure 3-14 is used to derive microinstructions from either the IR or the ROM. In the sequence previously discussed, during T0, T1, and T3, microinstructions were taken from the ROM. During T2, the IR supplied the instruction to be executed.

NOTE

When the programmer is manipulating data within the control registers of the machine (such as the trap or SC), it is quite important to know the event sequence of microinstructions relative to macroinstruction execution. Figures 3-15 through 3-17 show the event sequence of the instructions.

Figure 3-15 describes all single-cycle instructions. Figure 3-16 describes the Data Test class of instructions, and Figure 3-17 covers memory reference data transmission. In each case, the hexagonal boxes indicate a transfer of information to ro from memory. Tables 3-2 through 3-7 are provided to supplement the figures with exact sequence information.



PRIORITIES

1. DM DIRECT MEMORY ACCESS
2. EI EXTERNAL INSTRUCTION
3. BK INTERRUPT (BREAK)
4. MACHINE CYCLES (FI, FA, FO, FD)

NOTE:

FI CYCLE IS DRAWN TWICE FOR SIMPLICITY.

Figure 3-13 State Flow Diagram

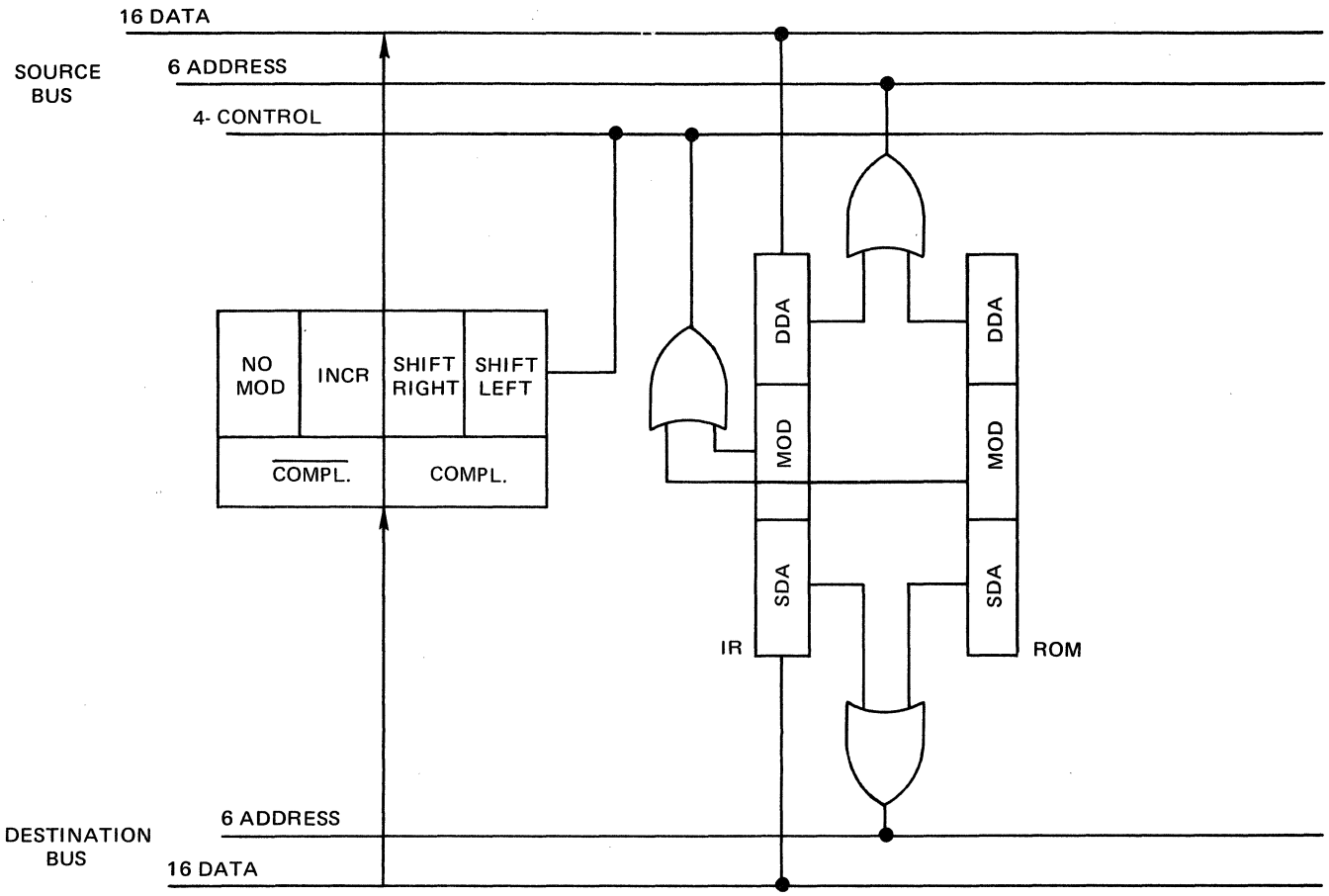


Figure 3-14 Derivation of Addresses and Control Signals from Either the IR or ROM

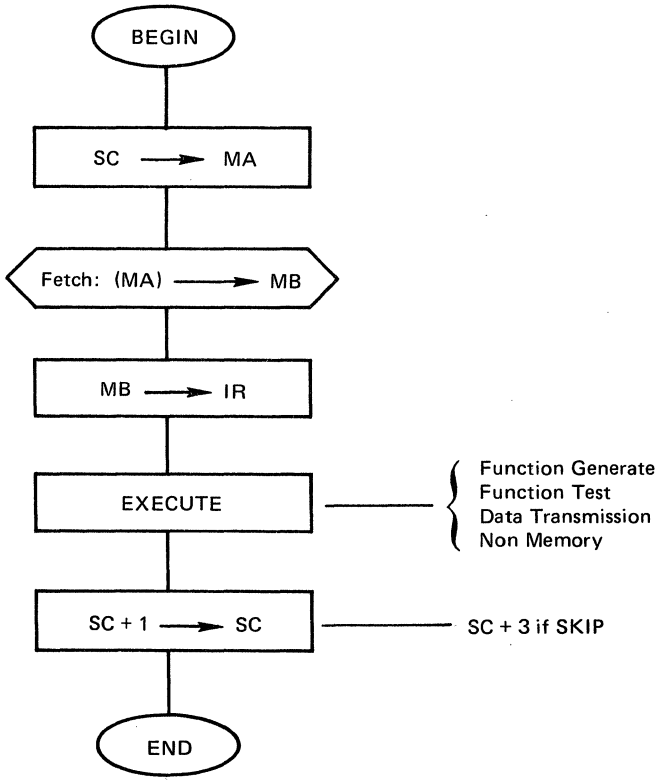


Figure 3-15 Event Sequence for Single-Cycle Instructions

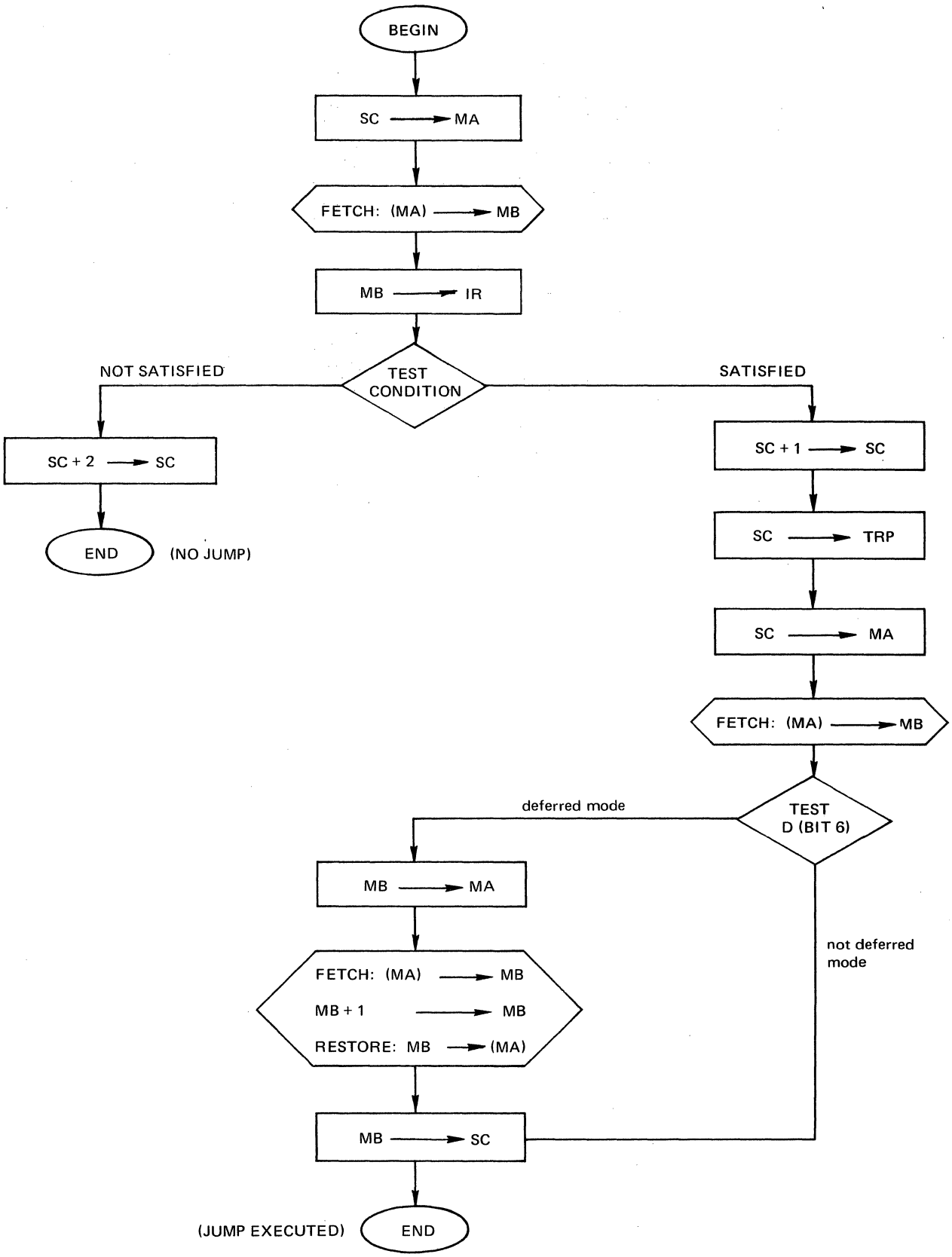


Figure 3-16 Event Sequence for Data Test Instructions

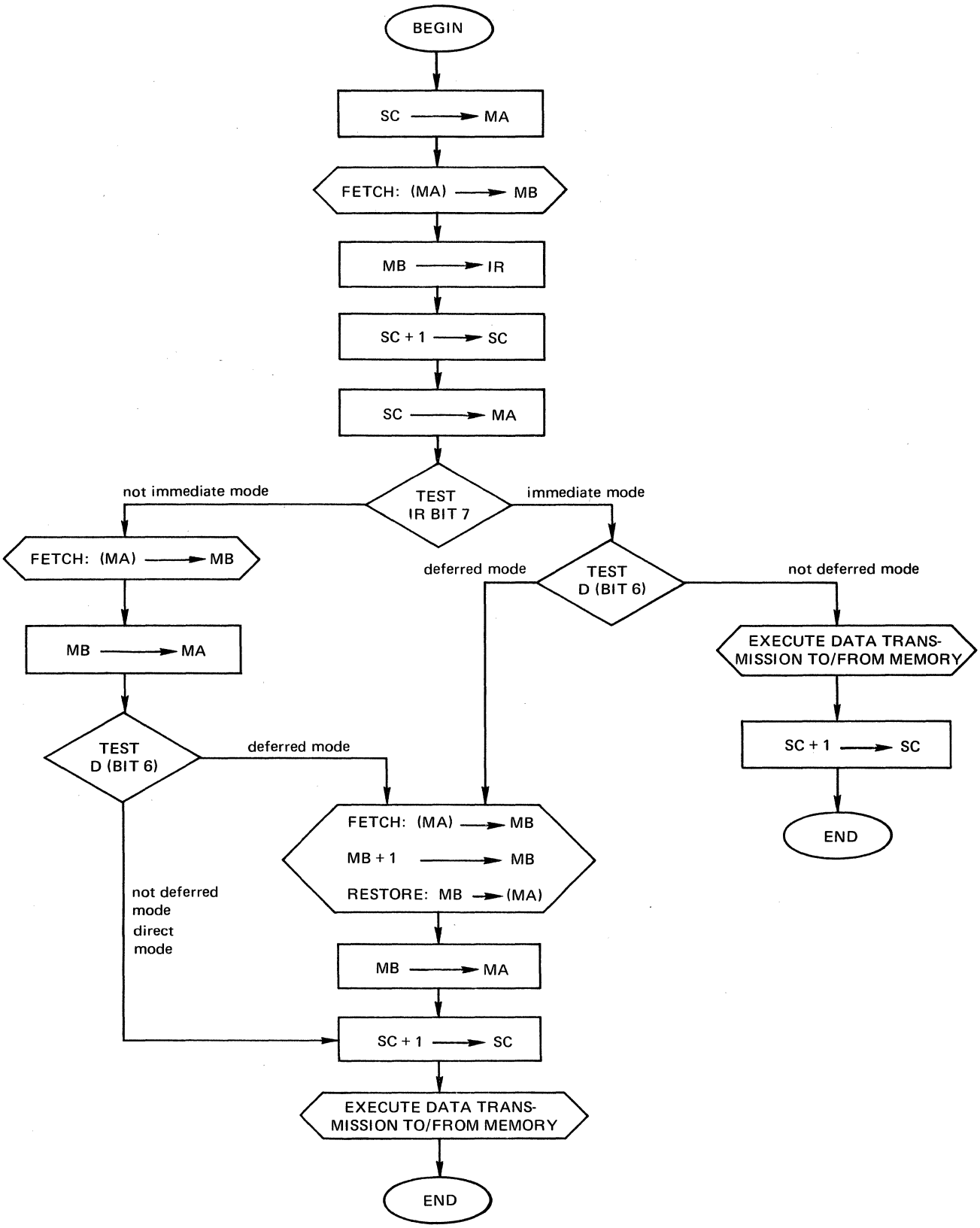


Figure 3-17 Event Sequence for Memory Reference Data Transmission Instructions

Table 3-2

FUNCTION GENERATE (NON-MEMORY DATA TRANSMISSION)

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begins memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
Fetch Instruction	T2	Execute (IR)	Macroinstruction now executed as a micro-instruction
	T3	SC + 1 to SC	The SC now points to next instruction in memory.

Table 3-3

FUNCTION TEST (SKIP)

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begins memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
Fetch Instruction	T2	Execute (IR)	Macroinstruction executed as micro.
	T3	SC + 1 to SC SC + 3 to SC	Test condition true. Test condition not true.

Table 3-4

DATA TEST (JUMP)

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begin memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
Fetch Instruction	T2	Execute (IR)	Perform test.
	T3	SC + 1 to SC	Test condition true; SC now points to jump address; another memory reference required.
		SC + 2 to SC	Test condition not true; SC now points to next instruction.

Table 3-4

DATA TEST (JUMP) (Cont.)

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begin memory reference.
FA	T1	SC to TRP	SC now in trap register.
Fetch Address	T2	No op	No operation
	T3	MB to SC*	Address is now in SC.
	T0	MB to MA	Begin memory reference.
FO	T1	No op	No operation
Fetch Operand	T2	MB + 1 to MB	Increment the address.
	T3	MB to SC	Incremented address now in SC.

* If jump is deferred, this operation is not executed because SC is changed during the next major state.

Table 3-5

MEMORY DATA TRANSMISSION
IMMEDIATE ADDRESS AND DIRECT ADDRESS

Major State	Time Slot	Microinstruction	Comments
Immediate Address			
	T0	SC to MA	Begin memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to address.
FA	T0	SC to MA	Begin memory reference.
	T1	No op	No operation.
	T2	Execute (IR)	Macroinstruction executed as micro-instruction.
	T3	SC + 1 to SC	SC now points to next instruction.
Direct Address			
	T0	SC to MA	Begin memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to address.

Table 3-5

MEMORY DATA TRANSMISSION
IMMEDIATE ADDRESS AND DIRECT ADDRESS
(Cont.)

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begin memory reference.
FA	T1	No op	No operation.
	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to next instruction.
	T0	MB to MA	MA points to referenced location.
FO	T1	No op	No operation.
	T2	Execute (IR)	Execute macroinstruction as micro.
	T3	No op	No operation.

Table 3-6

MEMORY DATA TRANSMISSION IMMEDIATE DEFERRED

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begin memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
Fetch Instruction	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to address.
	T0	SC to MA	Begin memory reference.
FA	T1	No op	No operation.
Fetch Address	T2	MB + 1 to MB	Increment address and store.
	T3	SC + 1 to SC	SC now points to next instruction.
	T0	MB to MA	MA now contains incremented address.
FO	T1	No op	No operation.
Fetch Operand	T2	Execute (IR)	Execute macroinstruction.
	T3	No op	No operation.

Table 3-7

MEMORY DATA TRANSMISSION DEFERRED

Major State	Time Slot	Microinstruction	Comments
	T0	SC to MA	Begin memory reference.
FI	T1	MB to IR	Macroinstruction in IR and decoded.
Fetch Instruction	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to address.
	T0	SC to MA	Begin memory reference.
FA	T1	No op	No operation.
Fetch Address	T2	No op	No operation.
	T3	SC + 1 to SC	SC now points to next instruction.
	T0	MB to MA	Begin memory reference.
FO	T1	No op	No operation.
Fetch Operand	T2	MB+1 to MB	Increment address and store.
	T3	No op	No operation.
	T0	MB to MA	Begin memory reference.
FD	T1	No op	No operation.
Fetch Deferred	T2	Execute (IR)	Execute macroinstruction.
	T3	No op	No operation.

3.7.1 DMA Execution

A DM request is initiated synchronously within a system operator by that operator grounding the DM request line through an open collector gate at ISYN time. A DMA is granted if the following conditions are met:

1. DMRL is true (Request for DMA).
2. The processor has completed a BK, DM, or EI state.
3. The processor is at the end of an instruction.

When the DMA is granted the processor goes into the DM state. The DM state is a cycle consisting of four microstate conditions: T0, T1, T2, T3 (refer to Table 3-7).

a. During T0, the external address is sent to the MA, resulting in a memory reference.

b. T1 is dependent on signal DIRB, which indicates the direction of the DMA transfer. If DIRB is high, the contents of the MB is transmitted to the external device. If DIRB is low a no operation occurs in this microstate time.

c. During T2, if DIRB is low, the data from the external device go to the MB and are written into memory. If IMB is low, the contents of the MB is incremented and sent back to itself; therefore, the incremented value is

stored in memory. If either of the two conditions are not met, this microstate becomes a no operation.

d. T3 is a no operation to allow time for the requesting device to disconnect itself or request the next cycle for a DM.

DMA control is located on PC 2, but decision as to type of DMA is on PC 1.

Table 3-8

DMA EXECUTION

Major State	Time Slot	Microinstruction	Comments
DM	T0	EAS to MA	External address is sent to MA.
	T1	MB to EDD	If DIRB is high, contents of MB go to external device; if DIRB is low, no op.
	T2	EDS to MB MB + 1 to MB	If DIRB is low, data from external device go to MB; if IMB is low, MB is incremented and sent to itself.
	T3	No op	No operation.

3.7.2 Interrupt Execution

An interrupt request is initiated synchronously within a system operator by that operator grounding the interrupt request line through an open collector gate at ISYN time (P1 time, except during a BK cycle). At the completion of the current program instruction, the processor grants one cycle, during which the SC contents are saved in memory and the SC is set to a new address as per the interface design.

An interrupt cycle is granted when the following conditions are met:

a. INTBL is true (interrupt request);

b. The processor is not in a DM or EI state;

c. The processor is finished processing a macroinstruction.

When the interrupt cycle is granted, the processor acknowledges this fact by going into the BK state. A signal POUT (orginated on PC3) is sent down the bus serially away from the processor. Each device not interrupting propagates the signal. The interrupting device terminates the signal and accepts the interrupt acknowledge. When more than one device requests interrupt at the same time, the operator physically closest to the processor on the bus has the highest priority.

When the processor goes into the BK state, four microstate conditions are generated: T0, T1, T2, and T3 (refer to Table 3-9).

a. During T0, the External Address is sent to the MA. This function causes a memory reference.

b. T1 is no operation time slot (the contents of memory is being read).

c. During T2, the contents of the SC is sent to the MB. This action causes the contents of the SC to be stored in memory during the write phase of the memory reference.

d. During T3, the external address is incremented by one and sent to the SC. The SC is now pointing at the first instruction in the interrupt handling routine.

All the interrupt control logic is located on PC 2. Microstate control is on PC 1.

Table 3-9

INTERRUPT EXECUTION

Major State	Time Slot	Microinstruction	Comments
BK	T0	EAS to MA	External address sent to MA.
	T1	No op	No operation
	T2	SC to MB	Contents of SC sent to MB.
	T3	EAS + 1 to SC	External address incremented by 1 and sent to SC.

3.7.3 External Instruction (EIR) Execution

In EIR mode, a system operator takes control of the bus and temporarily suspends operation of the stored program until the operator is finished. Instructions are presented directly to the IR in 16-bit words to be executed. The instructions do not reference memory; however, each instruction requires only 880 ns (half the normal instruction cycle) to be executed. In a sense, the EIR device *borrows* registers (such as the AO) from other devices and, thereby, performs certain operations more efficiently than hardware modules.

An EI is granted if the following conditions are met:

1. EIRL is in a true condition (Request for EI).
2. Processor is not in a BK, DM, or EI state.
3. The processor is at the end of an instruction.

The EIR mode is generally initiated by an FO control pulse that sets an EIR flip-flop in an operator. The EIR flip-flop is gated onto the EIRL bus, causing an EI request to be present when the processor completes execution of the FO instruction. The request is then granted, and the processor enters the EI major state (refer to Table 3-10).

During T0, the processor executes the microinstruction EDSH → IR. Then, the EIR device gates the next instruction from its ROM onto the Destination Bus lines, via the bus modifier to the IR. During T1, the instruction is executed. In the EI state the operator must supply an instruction to the Destination Bus on every even time period. In each odd time period the instruction is performed. During T2, the processor fetches another instruction, and in T3 executes the instruction. The EI mode forces EXT signals to occur during T1 and T3. A P2H is generated during T1 and T3 also to ensure proper operation of FO and SF class instructions.

When the EIR completes its last ROM access, the EIR flip-flop is reset The EI request is terminated and the processor terminates the EI state. The T1 strobe pulse is reinstated at the 330 ns to 440 ns segment of T1.

Table 3-10

EXTERNAL INSTRUCTION

Major State	Time Slot	Microinstruction	Comments
EI	T0	EDS to IR	External data is sent to the instruction register
	T1	EXT C(IR)	Execute the external data as an instruction.
	T2	EDS to IR	See T0.
	T3	EXT C(IR)	See T1.

3.8 CONSOLE OPERATION

The front panel of the programmer's console contains five rows of 16-bit registers and associated indicators and control logic. The Data Switch Register and the Function/Instruction switches are photo-optical: depressing a switch focuses a light, present in the plexiglas rod behind the switch, on the respective photocell that corresponds to the bit or function selected.

The clock or gating term for each register buffered by F0-F4 (8H90) is IRDSL, PDSL, MADSL, MBDSL, and SDSL. These signals are the control signals for each 16-bit register on the panel. The other input to each flip-flop is tied directly to its respective source bus bit (SB00H-SB15H). When a bit is set, its common indicator is lit, via a lamp driver gate (8H90).

The data bits SB00H through SB15H and the gating signals are sent through flat cable to the PD buffer. In the PD buffer, additional buffering is provided and the signals are mated into the processor bus via the PD connector.

The gating signal originates on PC 2. A Type 7430 8-input NAND gate is decoded during a microinstruction and sends the proper gating signal to the front panel, thereby enabling the selected register. This action occurs during the 440 ns T time of the particular major state being executed. Note that the switches on the front panel decode as CDA1H - CDA40H and these are gated into the ROM on PC 1, which decodes the proper microinstruction to be executed.

When the OPERATING KEYS READ, WRITE, TRM, and DISP are actuated on the console, the signals sent by the discrete drivers on the panel (RDKL, SRKL, TRKL, DISKL) are gated into E1(8H90) on PC 2. The signals enable the flip-flops E2 and E3, referred to as DISP, TRM, DEP (WRITE) and EXM (READ). After the flip-flop is set, the high side is gated into a large-wired OR gate, designated E4 and E5. T3H provides the microtime during which these signals are gated into the RUN flip-flop. The single-step signal (SSKL) is also available from the console in a similar manner. Note also that each key is given additional gating into an 8-input NAND gate (EO), which enables SWL and SWH to be generated. SWL and SWH initiate a one-shot timing chain shown at the top of the PC2 drawing. The signals combine to act as the main gating function for the RUN flip-flop, which causes the processor to enter RUN mode.

G5 is enabled by H4 and is gated by the counter (CC0 and CC1). The main timing for F4 is XCLH, which is double-buffered by A1.

The signal PSH is generated from the power supply when both logic power (+5V) and memory power (-20V) are up. In this case, PSH goes low. PSH is used in several places: F5, input of the RUN flip-flop to inhibit the RUN flip-flop if STEH is high; also, PSH is used with the low side of the RUN flip-flop to input D5 and, thereby, disable the one-shot counter circuitry.

The counter (CC0 and CC1) enable CLH and PCLH, a clocking term that is used for another counter (TC0, TC1). This counter enables a series of NAND gates (K3), which generate the sequential timing (T0H through T3H and their complements).

The PC2 drawing (Sheets 2 through 4) shows the major state gating. The signals EXTH and EXTL are gated from four NAND gates (K6). Note that each major state is used with a timing signal (1CH through 4CH). These signals specify the number of cycles that the processor must execute in the indicated major state. The signals 1CH through 4CH are originated on Sheet 3. The enabling term is buffered CB bits BCB0H, CB0L, CB1L, etc. The major states are timed by P times to enable the clock inputs with the proper FI, FA, and FO through D7 at their J input. The signal ENDH, generated by J6, is used as a gating term for the BK, EI, and DM flip-flops according to the respective requests that may be present on the bus lines.

3.9 POWER SUPPLY

The GRI Model S49 Power Supply furnishes the multiple power requirements of the GRI-909 Computer. The power supply protects the computer from both hardware and software damage during powerup, powerdown, and fault conditions (such as line failure or regulator malfunction). Internal circuitry provides sequenced powerup and power-down, fault sensing and protection, automatic restart, and software signaling of power status. Figure 3-18 shows the power supply.

3.9.1 Specifications

The two models of the power supply differ only in input characteristics.

3.9.1.1 Input – The input specifications for the two power supply models are as follows:

GRI Model S49-001

Voltage (1 phase):	99V - 132V
Voltage Surge (1 cycle):	200V
Current at Full Load:	3A nominal
Starting Peak Inrush (1/2 cycle):	14A
Frequency:	58.2 Hz - 61.8 Hz
Fuse (MDL)	5A

GRI Model S49-002

	Parallel Connection	**Series Connection**
Voltage (1 phase):	93V - 132V	186V - 264V
Voltage Surge (1 cycle):	200V	400V
Storage at full load:	20 ms	20 ms
Current at full load:	3A nominal	1.5A nominal
Starting Peak Inrush (1/2 cycle):	14A	14A
Frequency:	48.5 Hz to 51.5 Hz	48.5 Hz to 51.5 Hz
Fuse (MDL):	5A	3A

3.9.1.2 Output – The output specifications are as follows:

Logic Power Output

Output 1:	+5 Vdc, 0A-13A
Output 2:	-5 Vdc, 0A-0.5A
Adjustment:	Each, ±7% minimum at no load
Regulation (all causes):	± 1.5% at output terminals
Ripple and noise	10 mV pp

Lamp Power Output

Rating:	12V rms, 0A-1A, line frequency
Tolerance:	10V - 14V rms due to all causes
Protection:	Current limited, Constant voltage (CV) type transformer; short circuit shuts down dc supplies

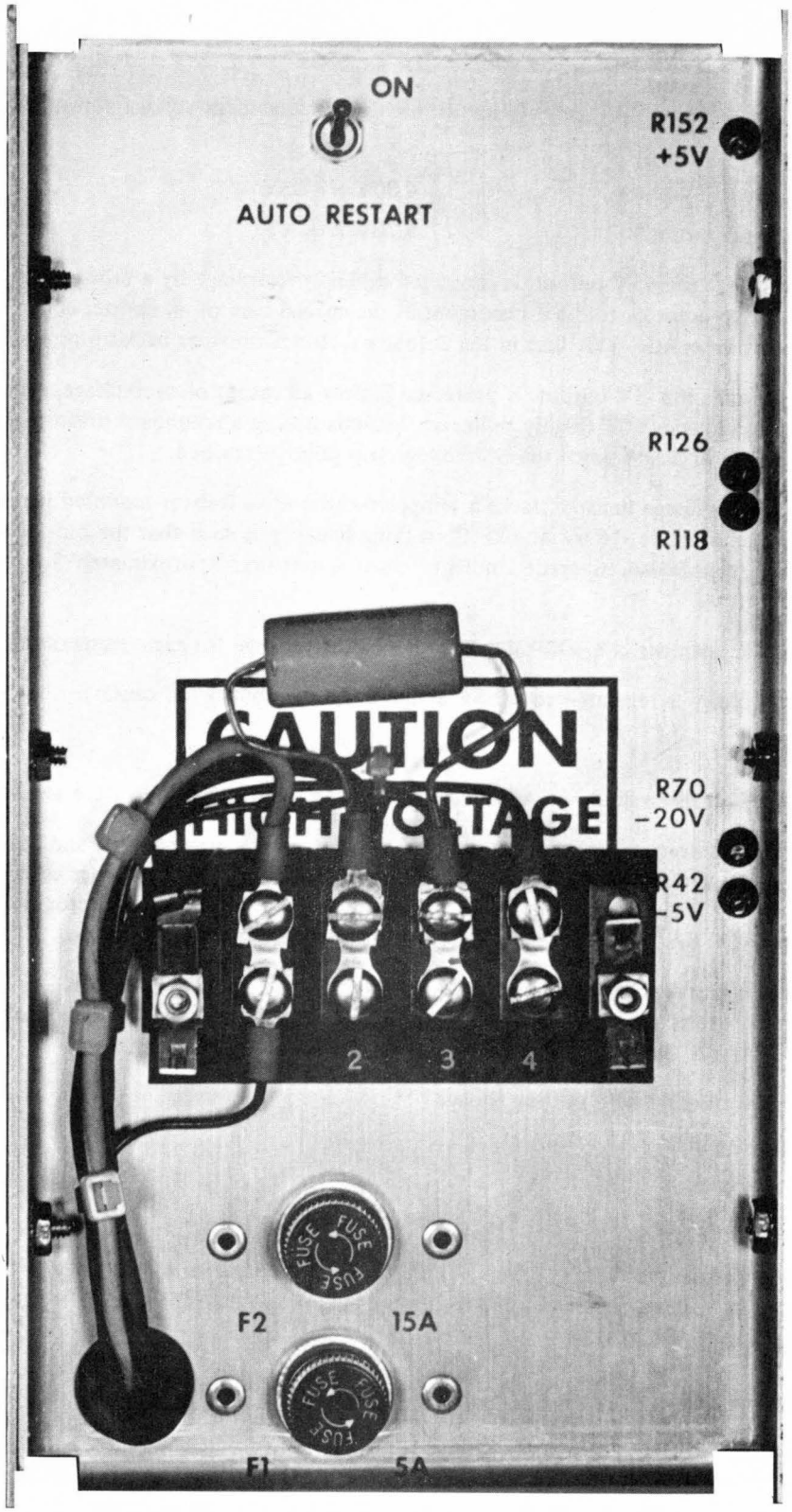


Figure 3-18 GRI-909 Power Supply

Note that the +5V output tracks the -5V in absolute magnitude. An independent voltage adjustment is provided for the +5V output.

Undervoltage (each output):	4.80V ± 0.05V
Overvoltage (each output):	5.20V ± 0.05V

A series regulator, which provides the +5V output, is protected against overvoltage by a crowbar circuit. The output is limited to the overvoltage trip point or to 5.5V maximum in the special case of an emitter-collector short of a pass transistor. In this case, a type AGC 15A fuse in the secondary circuit provides back-up protection.

A shunt regulator, which provides the -5V output, is protected against all causes of overvoltage, except the open circuit failure of the shunt power transistor (highly unlikely), by substituting a redundant preamplifier and error detector for the low-level regulator stages when the overvoltage trip point is reached.

Output Voltage – The output voltage linearly tracks a temperature-sensitive resistor mounted in the memory ambient. Assuming that the output is adjusted to -15.6V at +55 °C, tracking linearity is such that the output will be 21.3V ± 0.8V at 0 °C . The temperature is in degrees Centigrade ambient, which is measured approximately 5 in. below the computer chassis. Cooling is by convection.

Adjustment – The voltage adjustment is ± 10% minimum of nominal voltage for each temperature under all conditions.

Regulation – The output voltage is regulated to ±2.5% at the output terminals (all causes).

Ripple and Noise:	15 mV pp

Undervoltage (92% to 96% of correct value) – An undervoltage detector tracks temperature and potentiometer setting.

Overvoltage (104% to 108% of correct value) – An overvoltage detector tracks temperature and potentiometer setting. The memory supply, which is a series regulator, is protected against overvoltage by a crowbar circuit. The output is limited to the overvoltage trip point under all conditions, including the case of emitter-collector short of a pass transistor. In this event, a type AGC 8A fuse in the secondary circuit provides back-up protection.

Overcurrent and Short-Circuit Protection – Each output is protected against continuous overload or short circuit to common. The +5V output is protected by an overload detector that limits the fault and folds back to approximately 10% of full load current. The -5V output is limited to 2.5A maximum by a series resistor.

The overload trip point varies directly with output voltage.

at 21.3V, trip point is 5.3A - 5.9A

at 18.5V, trip point is 4.6A - 5.2A

at 15.6V, trip point is 3.9A - 4.4A

Auxiliary Power – Two additional voltages (+A and -A) are provided as input to local regulator for reference use. The voltages are unregulated dc voltages specified to be within the range +24V to +35V and -24V to -35V (28V nominal) and can be loaded to a maxium of 100 mA each.

3.9.2 Power Status Logic Signals

The power supply generates three logic signals to communicate power status to the computer. PSH (Power Shutdown) informs the processor logic that the power is down and that no run state should be attempted. STKL (START Key), an extension of the START key switch line, enables the auto-restart circuit to start the computer. PFL (Power Fail) is the signal that causes an interrupt, notifying the processor of an impending power shutdown. A minimum delay of 100 μs is allowed for the program to save all pertinent registers in memory before power is turned off.

3.9.3 Power-Up Sequence

The power-up sequence (see Figure 3-19) is as follows:

1. When the input power is applied, the three dc regulators are inhibited, the ac lamp output rises, and the power status logic signals attain their initial status.
2. After a 2.5s to 6s delay, the inhibit is removed from the ±5V regulators.
3. With ±5V within ratings for 2s, the memory supply is enabled. The memory voltage must attain the correct value faster than a 17 ms to 23 ms time-out or a fault shutdown ensues.
4. As soon as the memory voltage is within ratings, the logic signals communicate to the computer that power is ready.

3.9.4 Power-Down Sequence

3.9.4.1 Normal Turn-Off – The normal turn-off sequence (see Figure 3-19) is as follows:

1. When the input power is removed, the input dc filter capacitors provide the load requirements for 20 ms.
2. Approximately 800 μs later, a fault is detected for an undervoltage condition, causing the logic signal PFL to communicate to the processor that power is about to go down.
3. 100 μs - 140 μs after the fault, the logic signal PSH communicates to the processor that power is unavailable. (This time is used for software to save the status of the processor. The memory voltage is immediately crowbarred.)
4. Approximately 400 μs later, the logic signals attain their initial states and the ±5V supplies are set to the inhibit state.

3.9.4.2 Fault Shutdown During Operation – Line failure or an undervoltage causes a normal turnoff, however, a normal recycle is attempted (Refer to Section 3.9.3). Overvoltages in any of the supplies cause a crowbar to fire. After the crowbar fires, the normal shut-down sequence is started, and a recycle is initiated after the inhibits are placed on the regulators.

3.9.5 Description of Circuitry

The GRI-909 power supply may be divided logically into five major circuits:

a. Input power and bias supplies
b. Voltage regulators
c. Protective circuitry
d. Regulator inhibit and crowbar circuits
e. Sequencing and computer signalling logic.

3.9.5.1 Input Power and Bias Supplies – When the computer POWER switch is turned on, power is applied, via a protective fuse, to the primary of a constant voltage transformer preregulator. The secondary voltages of this transformer are rectified and filtered to provide the following voltages: (see Figure 3-18)

+24V to 35V:	Auxiliary output
+8V:	+5V regulator input
-8V:	-5V regulator input
-24V:	-20V regulator input and auxiliary output

A tap on the secondary is brought out to provide 12 Vac at 1A for the light pipe lamps.

The ±24V and ±8V supplies are also used as internal bias and control supplies. Four other bias voltages are derived for internal use, as follows:

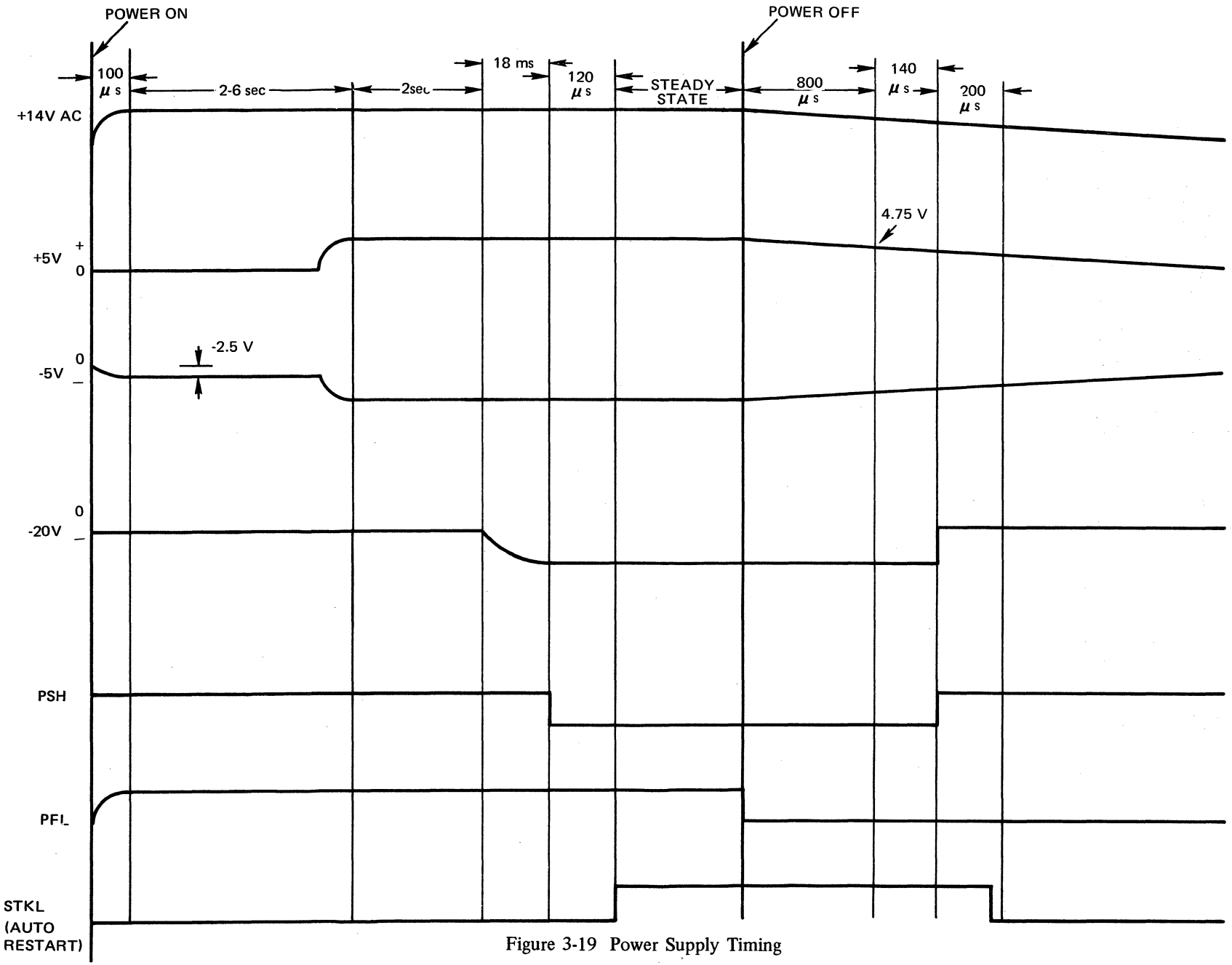


Figure 3-19 Power Supply Timing

a. +8V Stored - derived from +8V across C2. This voltage is used for the power logic and the over- and under-voltage detectors.

b. +6.2V Reference - derived from +24V across constant current fed zener diode D22. This voltage is used as a reference by the -20V regulator and the over- and under-voltage detectors.

c. -5.6V Bias - derived from -24V across resistor-fed zener diode D30. This voltage is used for general bias purposes.

d. +5.6V Reference - derived from ±5V outputs across resistor-fed zener diode D18. This voltage is used as the ±5V regulator reference.

NOTE

All voltages have ample storage capacitors to maintain the computer in operation during ac line drops of 20 ms or more. Also, all critical biases are maintained for an even longer amount of time to maintain the integrity of the logic signal interface between the computer and the power supply.

3.9.5.2 **Voltage Regulators** – The ±5V logic power and -20V memory power are controlled by transistorized regulators.

-5V Supply – Transistor Q14, which is current limited by R6, is utilized as a shunt regulator directly across the -5V supply output. Q14 is controlled by preamplifiers Q15 and differential amplifier Q16, Q17. The latter serves as an error detector, comparing the +5V reference voltage on Q17 base-collector with the -5V output. A change in line or load that causes the output voltage to deviate from -5V results in a change in the current through Q16 and, therefore, a revised current through Q14 and R6, which returns the voltage to normal. For instance, decreased load current causes a small increase in the magnitude of the output voltage, which decreases the current through Q14 equal in magnitude to the load change.

Resistor R6 limits the current in the shunt regulator and also provides current limiting when the output is accidently shorted. R42 is the -5V adjustment rheostat.

+5V Supply – The +5V supply is controlled by parallelled series regulator transistors Q5, Q6, R13,14 and R15,16 are used to improve current sharing of these devices. Q4 and Q9 constitute the preamplifier, and Q10 and Q11 constitute the error detector. In this regulator, the -5V output is used as a reference voltage. The base of Q10 is at ground potential. The detector is balanced when Q11 base is also at ground potential. With R28 = R27 + R152 (+5V adjustment), the +5V output is equal in magnitude to the -5V output voltage.

As an example of the regulatory action, assume a small increase in +5V. The current in Q11 decreases and the current in Q10 increases. This condition causes Q9 to conduct more heavily and shunt on-bias away from Q4. Thus, Q5 and Q6 cut off slightly, and the output voltage increase is opposed. The over-current protection circuit also takes advantage of the fact that turning on Q9 inhibits the +5 output. The overcurrent detector transistors, Q7 and Q8, are normally biased so that Q7 is on and Q8 is nonconducting. This task is accomplished by bias resistors R15, R18, R21, R22. The output current is measured by the resistors which are also used for current sharing: R13, R14, R16, R17. If the +5V output is accidentally overloaded, the voltage across these resistors overcomes the off-bias on Q8. The resulting current in Q8 turns on Q9, thereby inhibiting the +5V output and limiting the fault. Note that the off-bias decreases with the +5V, causing the output current to fold back (decrease) as the resistance of the fault decreases.

-20V Supply – The -20V supply is a series regulator, very similar in operation to the +5V regulator. Q24 and Q25 are the pass transistors. R60 and R61 are the current-sharing and over-current detection resistors. Q19 and Q20 are the preamplifiers, and Q15 – 1 through 5 are the error detector transistors. D22 is the reference zener.

A remotely mounted temperature compensating thermistor is connected across the terminals marked TH1, TH2. The regulatory action is such as to keep Q15 pin 4 at ground potential to match the voltage on Q15 pin 2. As an example, assume a small increase in the magnitude of the -20V output voltage. The detector unbalances in the direction to turn Q19 on harder. This condition biases Q20 further and causes a compensatory decrease in the Q24 and Q25 output. R70 is the voltage adjustment rheostat.

The -20V is used to power the memory core drivers. For optimum memory performance, this output is caused to decrease as ambient temperature increases. The temperature compensating thermistor is mounted near the memory and has a positive temperature coefficient. As the ambient temperature varies, the resistance varies with it and automatically causes the output voltage to vary inversely with the temperature.

As mentioned above, R60 and R61 are used to improve the current sharing of Q24 and Q25 and also for over-current detection. The over-current circuit is a foldback circuit similar to the one used in the +5V regulator. Q21 and Q23 constitute the over-current detector. Q23 is normally on, and Q2 nonconducting. An overload on the -20V output causes Q21 to conduct and, thus, turn on Q22, which then shunts the drive around the pass transistors and limits the fault.

3.9.5.3 **Protective Circuitry** – The GRI-909 is protected from over-current and over- and under-voltage conditions.

Overcurrent – Three fuses are provided: one on the input and two on the high-power outputs. The constant voltage transformer inherently current limits at about 150% of full load and, as previously described, the transistor regulated outputs self-protect against overloads. Thus, these fuses are really back-up protection.

Overvoltage and Undervoltage – The three regulated outputs are monitored by over- and under-voltage detectors. An out-of-tolerance voltage on any output causes a sequenced shutdown and an automatic restart. This process continues until the voltage is correct. To ensure that no hardware damage results, +5V and -20V overvoltages are immediately crowbarred, and -5V overvoltage is limited by overriding the low-level regulator stages with a redundant regulator.

3.9.5.4 **Regulator Inhibit and Crowbar Circuits** – The following paragraphs describe the regulator inhibit and crowbar circuits.

+5V Inhibit – As previously described (+5V over-current circuit), current through Q8 inhibits the +5V regulator. As a result, a positive voltage applied to Q7 base turns off the +5V. The associated signal is +5I.

-5V Inhibit – With the +5V inhibited, reference diode D18 and detector Q16, Q17 are starved. Thus, Q15 (6, 7, 8) is fully conducting, and the shunt transistor also conducts heavily. This situation inhibits the -5V output to about -2.5V.

-20V Inhibit With no current applied to ENT (Enable Negative Twenty) Q54 is saturated. This condition biases off Q20 and inhibits the -20V.

+5V Crowbar To shut down the +5V in the event of overvoltage, a positive signal is applied to +5CB, turning on Q28 and, therefore, Q27. A firing pulse is applied to silicon controlled rectifier Q50, which immediately shorts the output through R77. The +5V regulator then goes into the over-current mode. In the event that the overvoltage was caused by a shorted pass transistor, the backup 15A fuse blows.

-5V Z-bar The probable failure mode for shunt transistor Q14 is a short. Hence, the source of overvoltage is in the low-level circuitry. In the event of overvoltage, current amplifiers Q12, Q13 are turned on by the over-voltage detector. These current amplifiers act as a substitute regulator at about 5.25V.

-20V Crowbar – This circuitry includes Q29, Q30 and Q31. A 1 applied to -20VCB turns Q29 off. Q30 then delivers a firing pulse to Q31 and shorts the -20V output. The -20V regulator then reverts to the current-limit mode or, in the event of a shorted pass transistor, blows the 8A fuse.

3.9.5.5 **Sequencing and Computer Signalling Logic** This section describes how the regulators are sequenced on and off in normal and failure modes. Also, the definition and origin of the computer signalling logic is given.

Over- and Under-Voltage Detectors – These detectors comprise straightforward IC matched transistor differential amplifiers and associated resistor viewing chassis. The +6.2V is used as a common reference for all detectors.

+5V Undervoltage – Q41 pin 6 senses +5V and pin 9 is set at 4.75V. An undervoltage results in a +5UV signal, and Q36 turns on.

+5V Overvoltage – Q41 pin 2 senses+5V and pin 4 is set at 5.25V. An overvoltage results in a +5V signal, which turns on Q34.

-5V Overvoltage and Undervoltage – The principles of operation differ as follows: Q48 pins 4 and 9 are at 0V; Q48 pin 2 is slightly positive; and Q48 pin 12 is slightly negative. If the magnitude of -5V decreases, -5UV turns on Q36. If the magnitude increases, -50V turns on Q35.

-20V Overvoltage and Undervoltage – This circuit is identical to the above and utilizes 4 transistors from Q47. In this case, it is necessary to detect excessive errors on the input to a temperature compensated regulator. Note that Q47 pins 2 and 12 monitor the error at the base of regulator detector transistor Q16. An excessive undervoltage causes -200UV to turn on Q32, an overvoltage causes -200V to turn on Q38.

Normal Turn-On Sequence – The +5V and -5V are sequenced up after an initial delay. When the voltages are within tolerance, the -20V is enabled. When -20V is within tolerance, the processor is signalled that power is ready. The circuit operation is as follows:

1. The POWER switch is turned on, and all bias and power supplies rise to rated values.
2. The +5I signal is applied through R7 and, thus, the ±5V regulators are inhibited, as previously described. Because ENT = 0, the -20V is also inhibited.
3. Capacitor C8 charges through R1 and, after about three seconds, UJT Q1 fires and turns on SCR Q2. This removes +5I and the ±5V regulators are turned on. Also, the voltage across C8 is charged by Q2, R3, D10 to prevent recharging at this time.
4. While ±5 are in the under-voltage state, LVL = 1. This condition is removed when ±5V achieve their rated voltages (assuming no -50V).
5. With LVL = 0, Q55 is turned off and C41 starts to charge. After 80 ms, Q56 fires, clamping C41 and turning on Q58. At this time, ENT = 1 and the -20V rises. When -20V is within ratings, Q38 is turned off and FLT = 0 ($\overline{FLT}$ = 1).
6. The regulators are now in operation. The remaining task is to signal the processor. Assume for a moment that an initialize pulse has sent STKL = 0 ($\overline{STKL}$ = 1).
7. FLT → 0 causes Q41 (12, 13, 14) to turn off and flop Q42, Q48 is set. Immediately PSH → 0. Also, C20 discharges through R110. About 120 μs later, STKL→ 1 and the flop set pulse is removed.

Normal Turn-Off Sequence – Power is turned off. The first regulator that reaches undervoltage causes $\overline{FLT}$ → 0. Because $\overline{STKL}$ = 0, $\overline{PFL}$ → 1. This is latched via D54, and PFL → 0. C21 charges for 100 μs and then turns on $\overline{\Delta PFL}$. This turns on Q33, generating SET PSH.

The signal -20VCB is now generated, and the memory drive voltage decays rapidly. Also a 350 μs one-shot Q52, Q53 is fired, and RCYC is generated. This signal turns on Q3 and Q60, allowing the SCRs Q2 and Q57 to turn off. At the trailing edge of RCTC, +5I is applied and ENT is removed. All voltages decay at this time.

Setting PSH also turns on Q47 (6,7,8), which resets the flop. Then PSH → 1. Also, C20 charges through R111 and, about 250 μs later, STKL → 0 ($\overline{\text{STKL}}$ → 1). This action breaks the D54 latch and PFL → 1. The power supply logic voltages finally decay with the +8V stored, but the decay occurs long after -20V and +5V have disappeared.

Initialize Pulse – It is assumed in the preceding discussion that $\overline{\text{STKL}}$ = 1 initializes automatically on turnon, if it is not already true.

Assume that $\overline{\text{STKL}}$ = 0 on turnon. The outputs are undervoltage; thus, $\overline{\text{FLT}}$ = 0. Consequently, $\overline{\text{PFL}}$ = 1 and C21 charges, giving rise to $\overline{\text{PFL}}$. This generates SET PSH, which resets the flop and about 100 μs later generates $\overline{\text{STKL}}$ as stated.

Fault Shutdowns – An undervoltage on any output causes a normal shutdown. However, since the transformer voltages are still available in this case, C8 recharges and initiates another on-sequence. If the undervoltage persists, the sequence hangs up as described below under Turn-on into Fault Conditions.

Application of +50V or -200V immediately actuates a crowbar of the defective output. A shutdown as described in the previous paragraph is also actuated. Note that the +5V crowbar is slow enough to preserve the required off-sequence; thus, memory contents are protected in this case. A ±50V or -20V overload results in an undervoltage and the accompanying shutdown, as in the case of persistent low-line voltage.

NOTE

In general, only a dead short circuit on one of the outputs causes contents of memory to be destroyed.

Turnon into Fault Conditions – If the fault circuitry detects a ±5V undervoltage during turnon, the sequence holds until the problem is removed and LVL → 0.

The -5V and -20V over-voltage crowbar circuitry is always active to protect hardware. If the fault circuitry detects a -5V overvoltage or intermittently low ±5V during turnon, the sequence also holds. The reason is that LVL = 0 must be valid for about 80 ms to allow C41 to charge to the point where ENT can be enabled.

If -20V does not rise to its rated value within about 20 ms, MVL is generated, and the -20V is crowbarred. Then, the system tries to come up again. The MVL circuit is enabled by ENT. If PLT persists for more than 20 ms, C42 charges to the point where Q59 can be turned on.

NOTE

In none of the above conditions is the processor signalled on.

CHAPTER 4
INSTALLATION AND CHECKOUT

This chapter contains installation information for the GRI-909 Computer. References to the appropriate Teletype manual are included as an aid to Teletype installation.

4.1 UNPACKING AND INSTALLATION

4.1.1 GRI-909

No special procedures are necessary for installation of the GRI-909. The computer is protected by sturdy cardboard cartons and arrives ready for immediate use. Make a cursory inspection to determine that there is no shipping damage. If there is shipping damage, notify the carrier immediately.

NOTE

When a computer is brought into a warm room from a colder area, allow the computer to reach room temperature before using.

4.1.2 Teletype

When an ASR-33 Teletype is included, refer to the Teletype *Technical Manual, 33 Teletypewriter Sets, Bulletin 310B, Volume 1* for unpacking and installation procedures. During packing at GRI, two tiedowns are installed before packing. These tiedowns must be removed before use.

CAUTION

The Teletype unit, when mounted on the fiberboard shipping base, contains special hold-down bolts. When these bolts are removed and when the tie-downs are removed, keep the Teletype as level as possible. If the Teletype is turned on its side or upside down, parts and levers may fall out of place.

4.2 INSTALLATION CONSIDERATIONS

The GRI-909 Computer is built to be rack mounted as shown in Figure 4-1. The operating temperature range is 0 °C to 50 °C ambient, which is the temperature measured at a point 5 in. below the computer in the rack. For proper operation, allow an open area with a minimum height of 5 in. below the computer and several inches of open space above to permit heat to escape. If the computer is to be bench-tested or used initially on a table top, the bottom must be elevated a few inches for convection cooling.

CAUTION

Proper operation is highly dependent on a constant temperature in the ambient region. Hot spots or temperature transients are likely to cause memory failures.

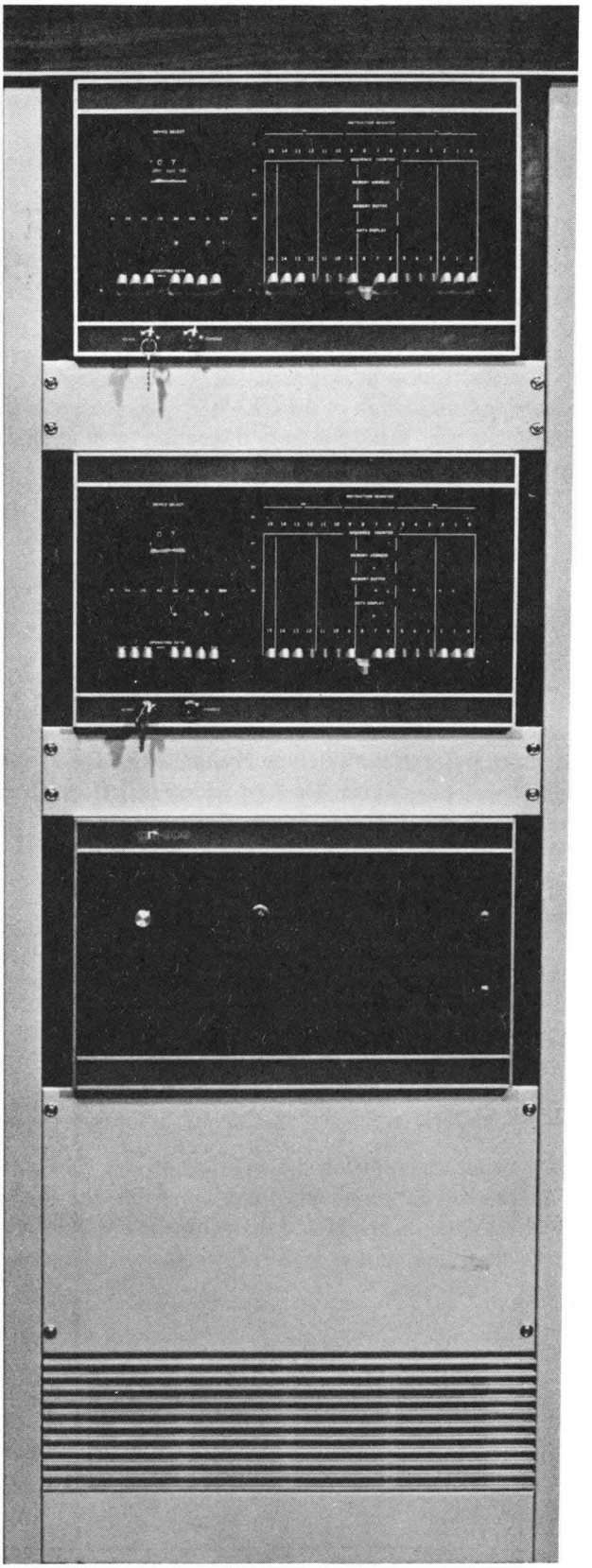


Figure 4-1 Rack Mounted GRI-909

4.3 CHECKOUT

No special check-out procedure is necessary for the GRI-909. Before ac power is applied ensure that all PC cards are securely seated in the connector. When ac power is applied to machines with the autorestart feature, the computer comes up running if the autorestart switch is on. All machines are equipped with a special pre-loaded version of the memory diagnostic. Refer to the directions shipped with the GRI-909.

4.4 CUSTOMER SUPPLIED TELETYPES

The Teletype Corporation Model ASR-33 Teletype is available in a variety of model numbers. These model numbers are designated by the ending two or three character codes on the name plate of the Teletype. The three most common Teletypes being used, all of which may be easily used with the GRI-909 with minor modifications, are the ASR-33 *TC*, the ASR-33 *TU*, and the ASR-33 *TZ*. The models *TC* and *TU* are identical except that the numeral zero on the *TU* has a slash through it (O), whereas the numeral zero on the *TC* printwheel looks like the letter O. The *TC* and *TU* are both what is known as no-parity units; that is, they always produce a 1 in channel 8. The model *TZ* is an even-parity model that produces a 1 in channel 8 in order to make the total number of ones in the 8-bit character an even number. All three of these models are equipped with "answer back," which means that transmission of the "who are you" code (WRU) to the printer mechanism causes the "here is" drum to be tripped and a string of characters to be transmitted. This feature must be disabled before using the Teletype with the GRI-909 software packages. Disabling of the answer back feature is a relatively simple modification which can be performed by any teletype serviceman. All three of these Teletypes are the most common Teletypes available, and they all have friction-feed typing units, where a sprocket-feed typing unit (for pin-feed paper) is desired. The Model ASR-33 *TY* is identical to the Model *TZ*, except for the sprocket-feed typing unit. The common 50-cycle versions of the ASR-33 are the ASR-33 *TAC* or *TAJ*, which are identical to the *TZ* unit (the *TAC* comes without stand and chad box). The model ASR-33 *TBM* is identical to the *TAC* unit with the exception of a sprocket-feed typing unit for pin-feed paper.

None of the Model 33 Teletypes are capable of running in a remote reader/run mode, where the reader may be selected by *external command pulses.* This feature is essential to the operation of the assemblers. This modification is installed via the GRI-909 Teletype mod kit (Model number S40-212). Teletypes which are equipped with an automatic reader control function are not recommended for use with the GRI-909. If a Teletype utilizing this option is to be used with the GRI-909, the X-ON and X-OFF remote reader control functions must be disabled; otherwise, generation of a binary tape by the assembler may cause the reader to turn on or off overriding the remote reader/run control, which is installed with the teletype mod.

There is a model ASR-33 *TBE* that has an even-parity feature, which has been disabled. Disabling of the even-parity, although it apparently produces a no-parity tape, does not produce proper code when reading binary tape with the reader. If this Teletype is to be used with the computer, then the disabling of even-parity must be removed and the unit converted back to an even parity unit. The model *TBE* has a momentary reader/run manual select switch on it and is often equipped with the remote reader control functions X-ON and X-OFF.

Before any of the Teletypes can be used with the GRI TTI and TTO option cards, the teletypes must be converted according to the standard Teletype instructions to a 20-mA current loop operation and to full-duplex operation. New Teletypes generally come wired for 60-mA loop current and simplex operation. Instructions for making this conversion are included in the instructions that come with the Teletype mod kit. If the GRI Teletype mod kit is not used with the Teletype and the user desires to make up his own cables and add his own reader/run relay control, it is recommended that at least the instructions for making the GRI mod be followed explicitly, because the proper grounding of the Teletype and the proper usage of thyrector supressors on 110V switches is required to ensure safe system operation.

CHAPTER 5
MAINTENANCE AIDS

Chapter 5 contains detailed explanations of circuits and logic symbology used in the GRI-909. A troubleshooting guide is included to aid in fault isolation, and step-by-step replacement procedures are given.

5.1 CIRCUITS

The prime building blocks used in the GRI-909 are TTL integrated circuits (ICs). The types of circuits are listed below by category and a close-up drawing of an IC pack is shown in Figure 5-1. Note the pin numbering scheme.

Gates

JK Flip-Flops

D-type Flip-Flops

2-Bit Binary Adder

Memory Sense Amplifier

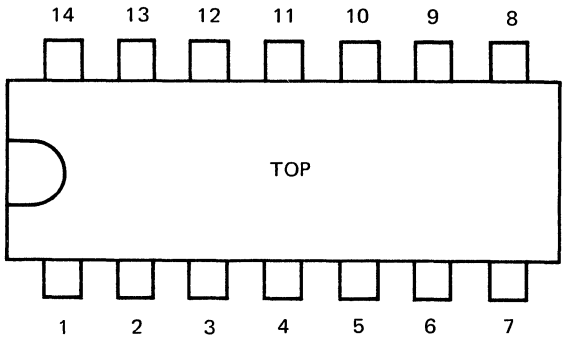


Figure 5-1 IC Pack Pin Numbering

The IC chips are positioned on either small or large printed circuit (PC) cards to build the various system operators. The layout of all cards is identical to facilitate location of a particular IC chip. This layout is shown in Figures 5-2 and 5-3 with a sample callout (J7) shown in Figure 5-3.

A definition of voltage levels for circuit inputs and outputs is included in Figures 5-4 and 5-5.

Figure 5-6 defines the operation and timing characteristics of the D-type flip-flop; the JK flip-flop is shown in Figure 5-7.

5.1.1 Logic-Symbology

The basic gates of the 7400 series logic are NAND gates (negative AND). The logic symbology used is based on widely accepted standards. Figure 5-8 shows signal labeling conventions. The logic symbols and truth table for the NAND gate are shown in Figure 5-9.

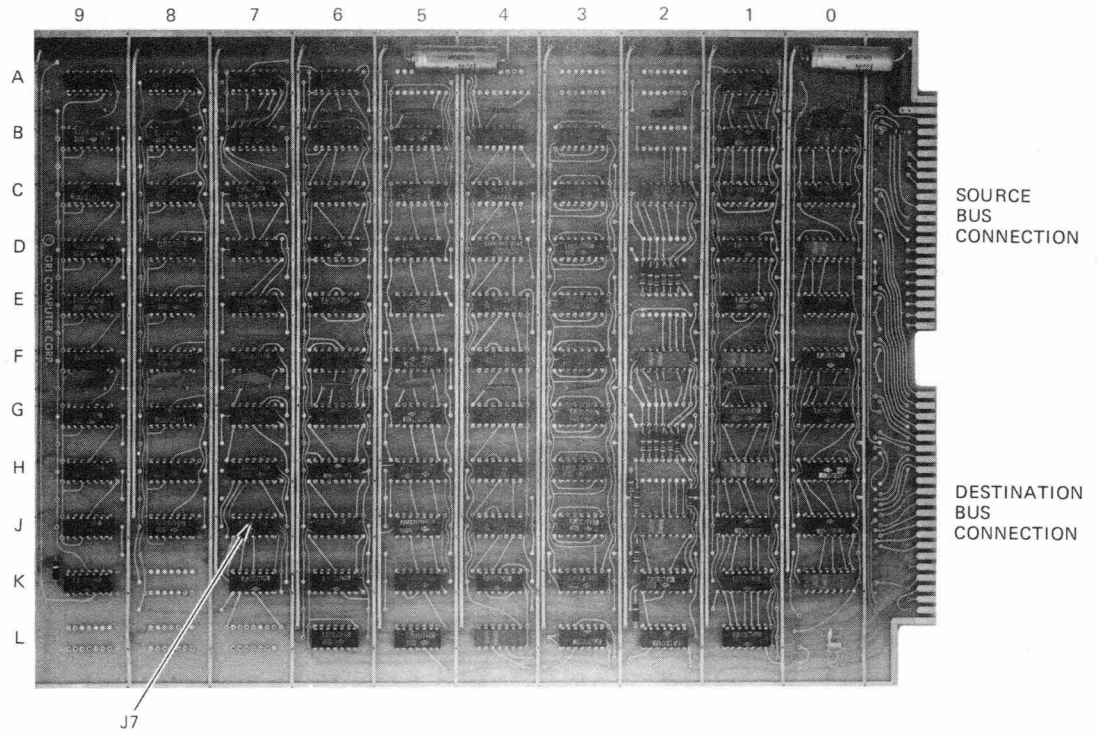


Figure 5-2 Small Firmware/Device Operator PC Card (Component Side)

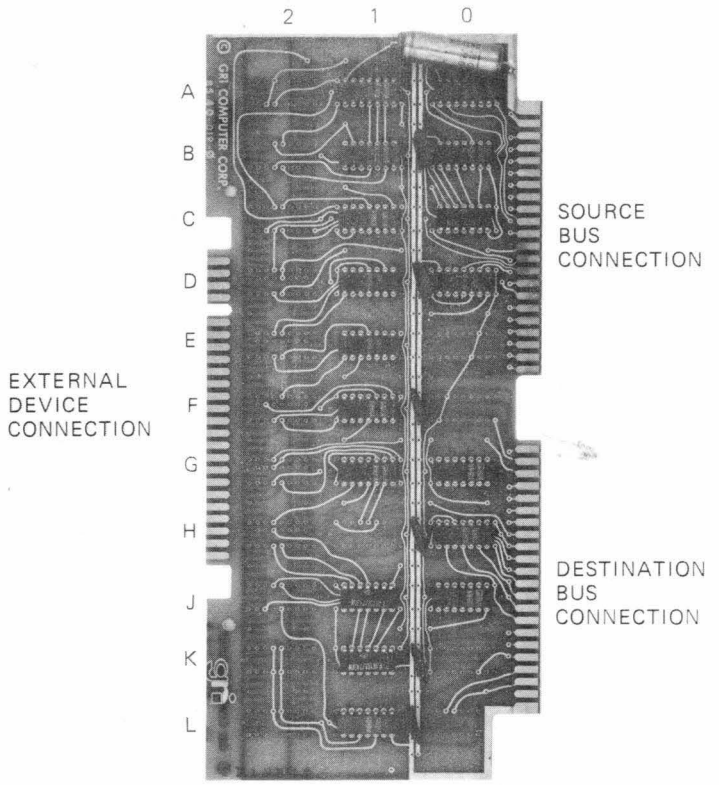


Figure 5-3 Large Firmware/Device Operator PC Card (Component Side)

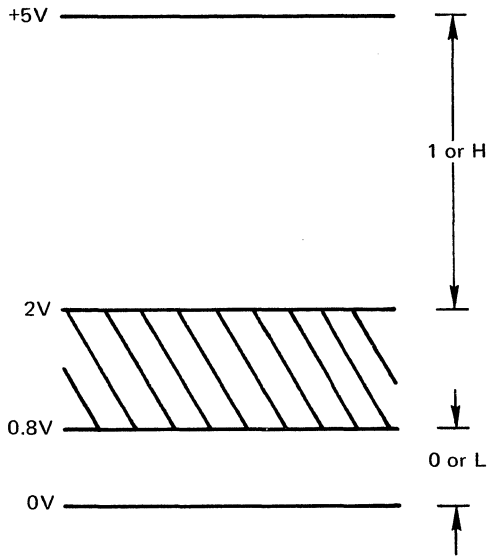


Figure 5-4 Definition of Voltage Levels for Circuit Inputs

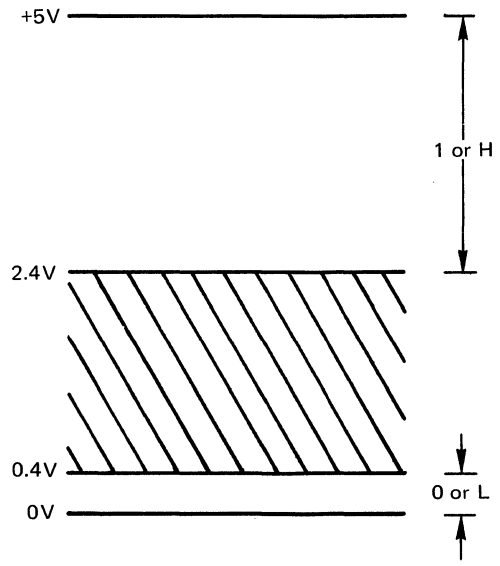


Figure 5-5 Definition of Voltage Levels for Circuit Outputs

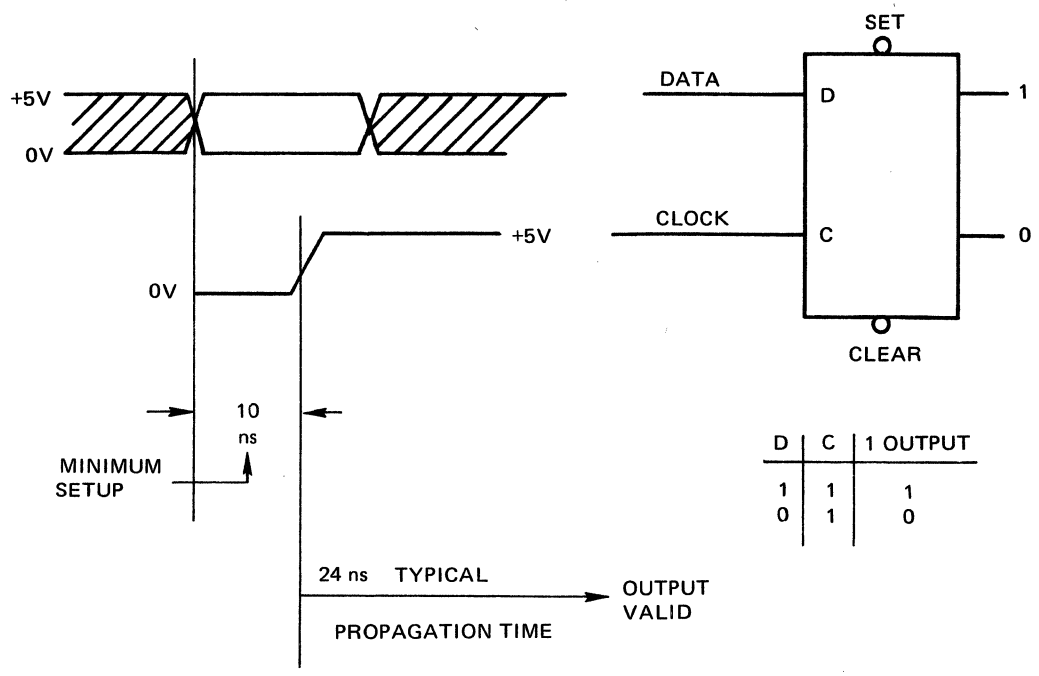


Figure 5-6 D-type Flip-Flop Characteristics

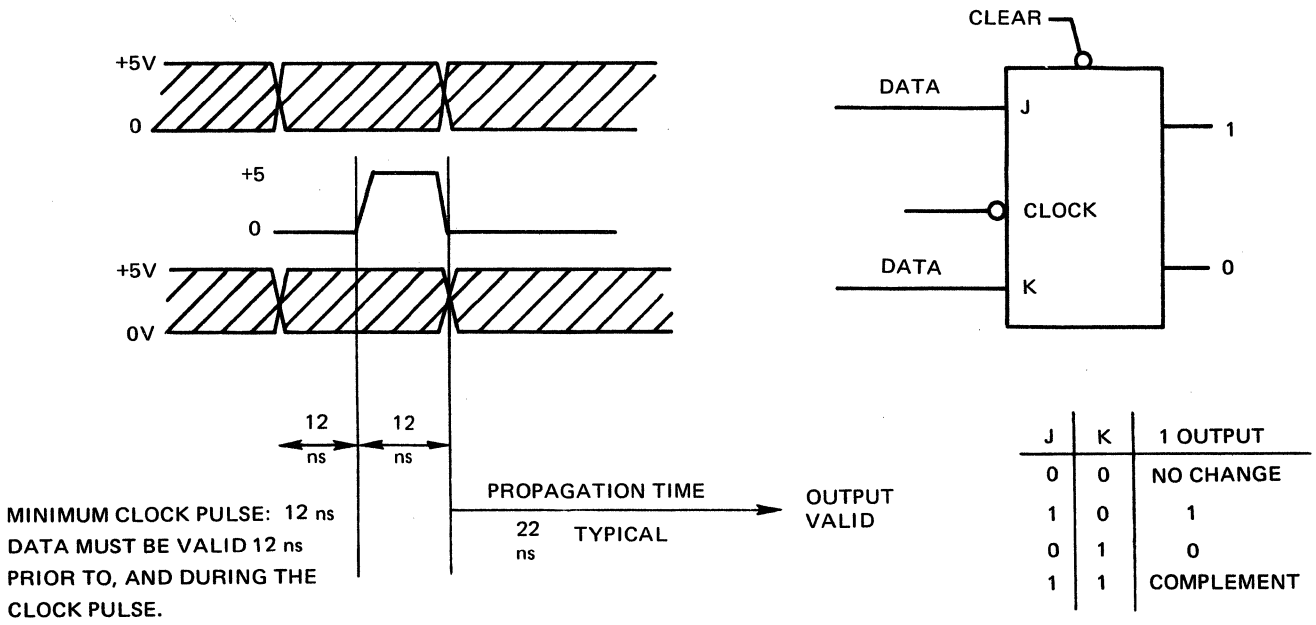


Figure 5-7 JK Flip-Flop Characteristics

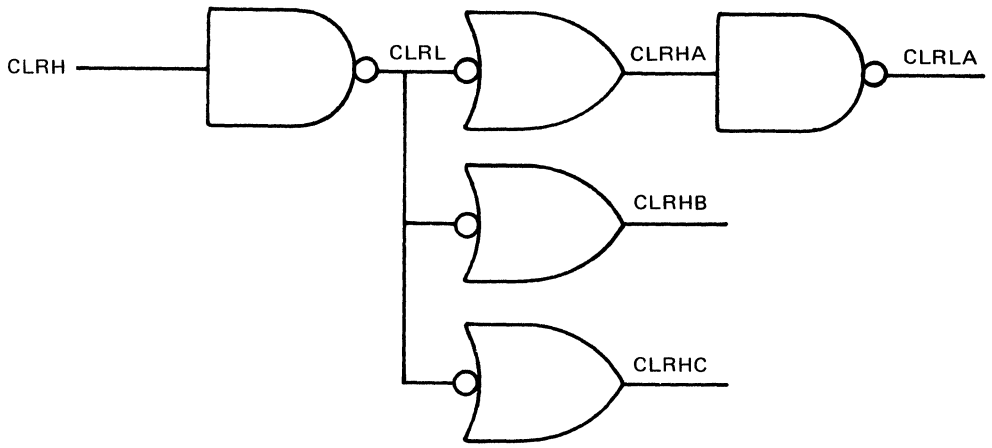
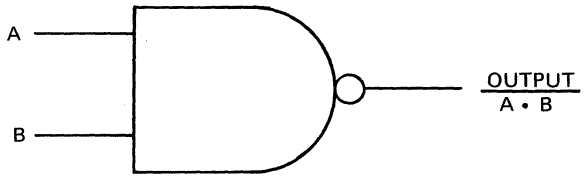


Figure 5-8 Signal Labeling



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

TRUTH TABLE

Figure 5-9 NAND Gate Symbology and Truth Table

As shown in Figure 5-10, signals coming from, or going to, the Source and Destination Buses are denoted by an open arrow with the bus signal name written over the connector pin designation. The signal BKH is coming from the Source Bus, pin D (SD). The output example shows a gate driving the line DB02L, which is pin B of the Destination Bus (DB).

Figure 5-10 Source and Destination Bus Symbology

For small size I/O cards, which have the additional connector on the rear of the board, the same conventions are used (see Figure 5-11). In the case of the small I/O cards, the arrowheads are solid.

Figure 5-11 Small I/O Card Symbology

5.2 TROUBLESHOOTING GUIDE

This section provides troubleshooting guidelines for the GRI-909 Computer and associated power supply. Typical failure symptoms are described, accompanied by appropriate fault isolation techniques.

The ultimate goal of troubleshooting is to isolate a problem to a faulty PC card. The PC card is then replaced, and the faulty card is sent to GRI for repair. Due to the architecture of the GRI-909, problems can be isolated quickly in many cases by a few simple tests from the operator's console. Large size PC cards are used, and very few exist in a complete machine; thus, troubleshooting time can be reduced greatly by simply replacing suspected boards with boards known to be operable.

In this manual, the basic philosophy of fault isolation is to start with a test of a small part, prove the part normal or replace it, and then use that part to test a larger segment of the system. This technique, by necessity, begins with slow tedious tests but proceeds rapidly. The following step-procedure sequence is a general guideline for trouble-shooting.

Step	Procedure
1.	Test for power problems.
2.	Test TRM key, DISP key, and basic processor functions.
3.	Test memory and READ and WRITE keys.
4.	Run short test loops.
5.	Load a diagnostic program.

NOTE

It is tempting to begin with a more advanced step in this sequence and then work either forward or backward as necessary; however, this approach does contain pitfalls. A problem that can be solved easily by a basic test may be further complicated and confused by starting with an advanced test. Many costly hours of troubleshooting can be wasted in these situations.

With sufficient spare parts, a good approach used by experienced troubleshooters is to spend a few minutes in the beginning to change suspected PC boards. If the trouble is not readily apparent, and sufficient spares are not available, proceed to the basic outline. In all cases, experience with the system speeds troubleshooting and reduces downtime.

5.2.1 Power Problems

When several unrelated problems appear to exist, good practice dictates voltage measurements. The GRI-909 Computer is protected for both over- and under-voltage conditions, providing the power supply sensing circuits are working properly. Figure 5-12 shows the power supply and the locations of the various adjustments.

In most cases, a power problem is detected by the fault-sensing circuits. The supply continually cycles down and attempts to come up again. Refer to the power supply specifications in Chapter 3 for adjustment specifications. If a short circuit is apparent, the power buses are easily disconnected by the fast tab connections from the power supply output wiring.

This same recycling symptom occurs if the ac line voltage is too high or there are low-voltage transients. Transients are not unusual in early morning or late afternoon when large industrial machinery is turned on and off. If a low line- voltage condition persists, the power supply attempts to come back by first enabling the ±5V supplies. In this case, these supplies do not reach full voltage; thus, the -20V supply is not enabled. The system stalls in this condition, as evidenced by the dim console indicators. A low ±5V and no -20V output confirms this condition.

The ac line fuse and +5V fuse are easily accessible on the front panel of the power supply. The +5V fuse is merely a backup to the voltage protection circuits. The same is true for the -20V fuse inside the supply. If either of these fuses blows, a power supply failure has occurred, and the supply should be changed.

WARNING

It is strongly recommended that all power supplies be sent to GRI for repair, because hazardous voltages exist in the supplies. Also, special set-up and re-alignment procedures are necessary after a supply has been repaired.

5.2.2 Logic Failures

To isolate system failures, the system must first be logically divided into sections that can be tested individually. The basic processor can be separated into two parts:

a. The processor (PC1, PC2, PC3) and the console;

b. The memory controller (MR) and core memory boards.

The processor and console are used to test themselves; consequently, the results are not always meaningful. The processor can, however, be used to test memory, the arithmetic operator, Teletype, or any other functional part of the system.

Those functional parts of the system internal to the basic processor are listed according to PC card, as follows:

PC1	Instruction Register Read Only Memory
PC2	Basic Timing Major States
PC3	Bus Modifier Sequence Counter Trap Register

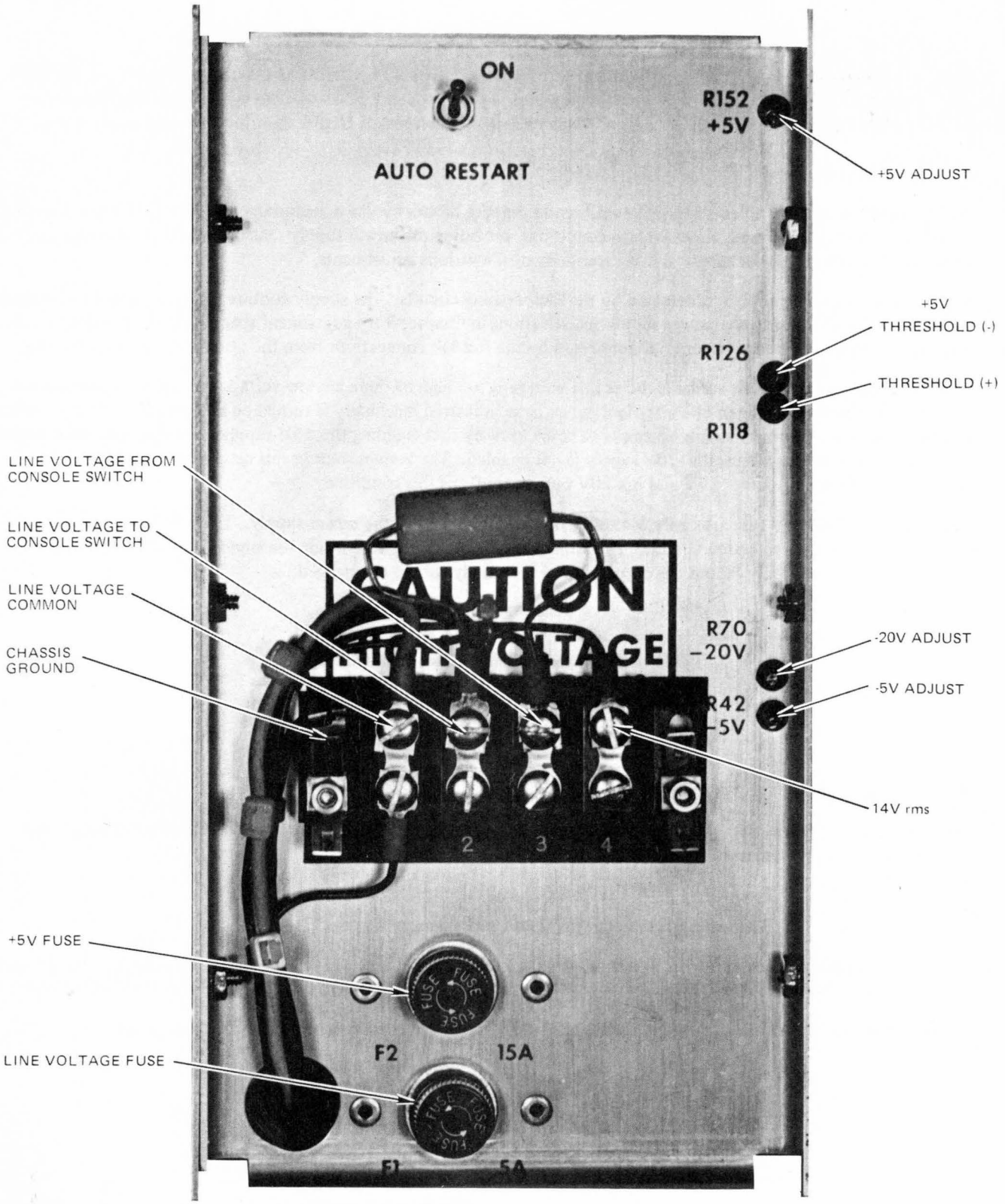


Figure 5-12 Power Supply

It is possible for one system operator to continually fault the buses and disable the entire system; therefore, unplug all PC cards except those under test and those that have been successfully tested. The basic processor cards (PC1, PC2, and PC3) must always remain plugged in.

5.2.2.1 Testing the Processor and Console Within the basic processor, the instruction register, sequence counter register, and trap register can be used in conjunction with the console transmit and display features to check a significant amount of the processor and console logic.

NOTE

It is most important to be thoroughly familiar with the event sequences following transmit and display in order to analyze results correctly. Refer to Section 3.7.

To test the processor and console, proceed as follows:

Step	Procedure
1.	Transmit a bit pattern to the instruction register (IR) (device address 01). Note that the action shown in Figure 5-13 occurs.

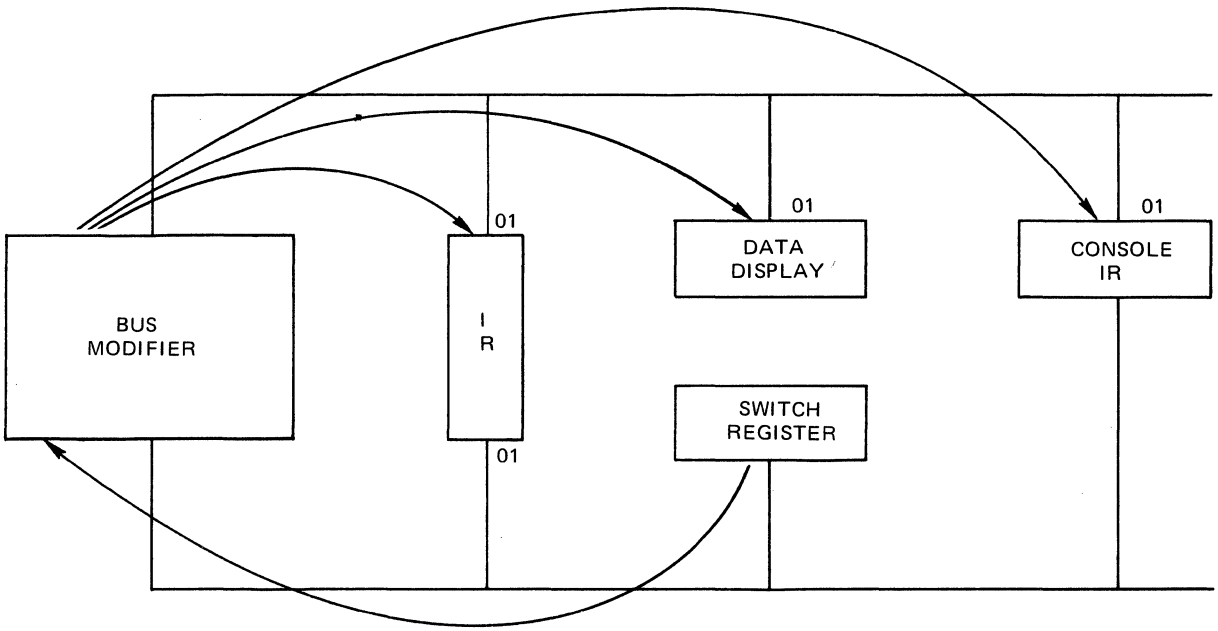


Figure 5-13 Transmit to Device 01

Step	Procedure
2.	The Data Switch Register setting is transmitted to the IR, DATA DISPLAY register, and the console IR indicator buffer, *providing a programmer's console is in use.*
3.	Observe the DATA DISPLAY and console IR indicators. These indicators should match the Data Switch Register.
4.	If several different bit patterns can be transmitted successfully, the data paths on the Source and Destination Buses are working properly. Also, the ROM logic on PC1 is functioning well enough to generate the register-to-register transfer just observed.
5.	Change the console DEVICE SELECT switch to 07 for the sequence counter. Repeat the transmit test.
6.	Set the DEVICE SELECT switch to 03 for the trap register. Repeat the transmit test.
7.	It is important to note that, thus far, no registers have been tested. The Data Switch Register was transmitted to the DATA DISPLAY register and the console IR buffer. However, this action does not ensure that the data reached the instruction register or was stored properly.
8.	To verify these conditions set the DEVICE SELECT switch to 01 and depress the DISP key. The action in Figure 5-14 occurs.
9.	The DATA DISPLAY and console IR indicators do not change unless the IR contained the wrong number. Depress the DISP key several times to ensure proper operation, then repeat for the sequence counter and trap registers.

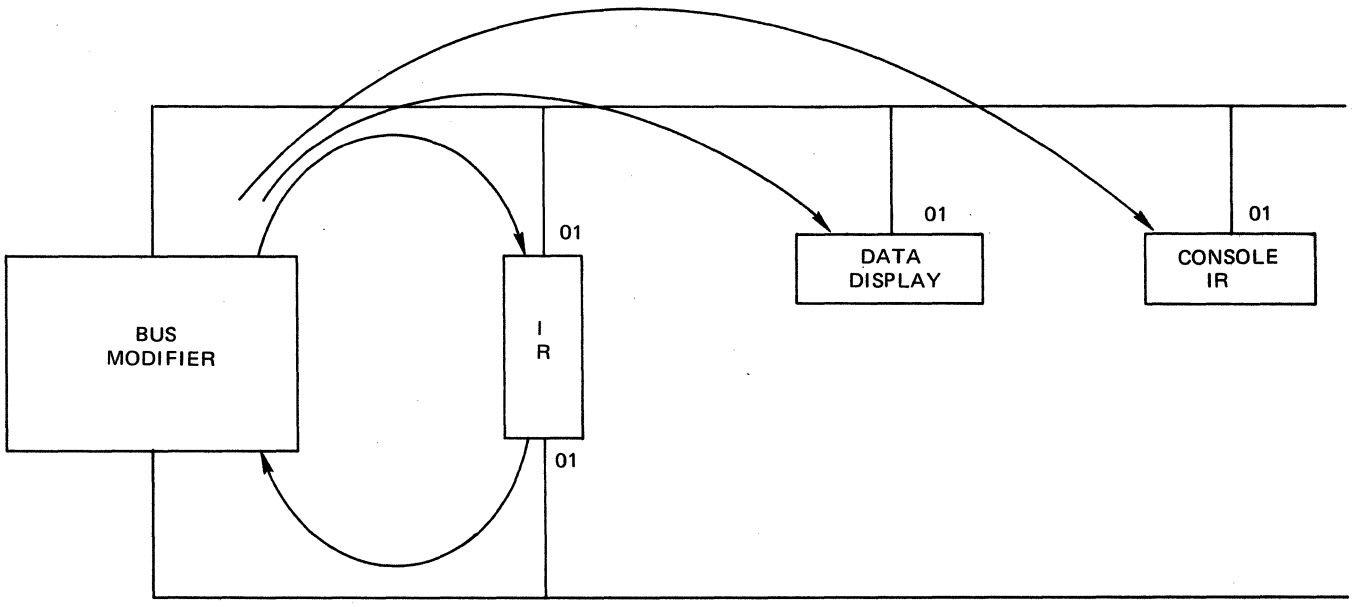


Figure 5-14 Display Device 01

5.2.2.2 Testing Memory – The READ and WRITE switches are used at this point to make minimal tests on memory and at the same time test the processor and console more thoroughly. To test a memory location, proceed as follows:

NOTE

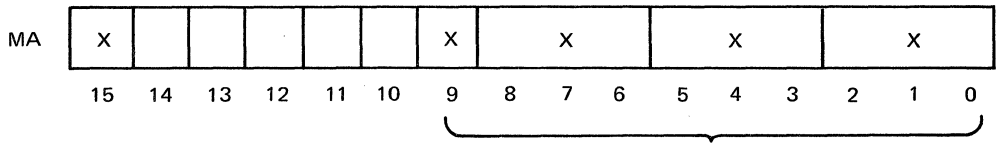
Keep a record of the data words and memory locations used in the following procedure. These words and locations can be used again in Step 8.

Step	Procedure
1.	Transmit the address from the console switches to the sequence counter (07).
2.	Depress DISP to verify that the correct address is indeed in the sequence counter.
3.	Push the WRITE switch to cause the following microinstructions to occur during one memory cycle. T0 SC → MA T1 NULL T2 Switches → MB T3 SC + 1 → SC
4.	Increment the sequence counter by 1; the MA register should hold the address of the memory location just cycled, and the MB should contain the Data Switch Register configuration. Irregularities here could be due to the processor or the MR board.
5.	Again observe the contents of each register using the DISP key to verify the register contents. If the register contents are not correct, possible faults are: ROM on PC1, the MA and MB registers on the MR. At this point, it is not known if the MR communicated with the core memory and wrote the word into memory.
6.	Repeat Step 5 for several memory addresses and several data words to ensure that the MA and MB registers are working satisfactorily.
7.	Exercise the WRITE switch repeatedly to verify that the sequence counter is incrementing.
8.	Use the data words and memory locations exercised in the preceding steps to test the READ switch. The READ switch initiates one memory cycle as did the WRITE, and the following microinstructions occur: T0 SC → MA T1 NOP T2 MB → MB T3 SC + 1 → SC

Step	Procedure
9.	As with the WRITE sequence, verify proper operation of the SC, MA, MB, and SC + 1. The most significant test here is the data word retrieved from core memory. Correct results verify proper writing into and reading from memory. It is important to note that a failure here could be due to either the read or write functions, because the write function produced no feedback prior to this step to indicate that it worked properly.
10.	If the system contains more than one core memory board, a faulty board can be quickly isolated by testing various memory locations in each of the boards. If all failures occur in one board, change the board.

NOTE

Each board can contain either 1024 words or 4096 words. Up to four 1024-word boards can be used or up to eight 4096-word boards. These boards cannot be mixed within one system.* Figure 5-15 specifies memory address stack selection.



						1K	4K
0	0	0	0	0		1	1
0	0	0	0	1		2	1
0	0	0	1	0		3	1
0	0	0	1	1		4	1
0	0	1	0	0			2
0	1	0	X	X			3
0	1	1	X	X			4
1	0	0	X	X			5
1	0	1	X	X			6
1	1	0	X	X			7
1	1	1	X	X			8

Figure 5-15 Memory Address Stack Selection

*Beginning with Serial No. 209, 1K and 4K boards can be intermixed.

5.2.3 Second Level Tests for Basic Processor

If the preceding tests yielded correct results, the core memory, memory control, instruction register, ROM, basic timing, and sequence counter are all performing limited functions correctly. At this point, short instruction test loops can be keyed into core memory and executed. The objective of these short tests is to confirm that the bootstrap loader is operating properly. This procedure allows a diagnostic to be loaded and used as a troubleshooting aid.

NOTE

The bootstrap loader itself can be used at this point. However, it contains no self-checking and error halts as do these short tests

5.2.3.1 Test 1 – Proceed as follows:

Step	Procedure
1.	Key the instructions in Table 5-1 into the memory area to be used by the bootstrap loader.
2.	Start the program at XX727. The program should halt with the SC = XX730 and the MA = XX727.
3.	Depress CONT and the program should halt again with SC and MA advanced by 1. Depressing CONT again should cause another advance by 1. The HLT instruction is used to stop the program when an error is encountered; thus, it is tested first, three times.
4.	Depressing CONT causes the execution of a Jump instruction to itself. The processor should run continuously. Depress STOP and CONT several times. After each STOP, the SC = XX732 and the MA = XX733.
5.	To continue testing, start the SC at location XX734 with the Data Switch Register set to zero. This portion of the test loops continuously and halts only if an error is encountered.
6.	Stop the program while it is looping to ensure that the SC is still within the test loop. It is possible for a failure to send the SC to some unknown area of memory.

5.2.3.2 Test 2 – Proceed as follows:

Step	Procedure
1.	Key in Test 2 and start the SC at 00001 as shown in Table 5-2. This program loops indefinitely and halts only if an error is encountered.
2.	Again, stop the program occasionally to ensure that the SC is still within the test program.

Table 5-1

TEST 1 INSTRUCTIONS

XX727	02 0100 00		FOM HLT	; Test HALT instruction
730	02 0100 00		FOM HLT	; Test HALT instruction
731	02 0100 00		FOM HLT	; Test HALT instruction
732	00 0100 03		JU	; Test Unconditional Jump
733	XX732			
734	02 0010 00	Begin:	FOM STL	; Set link
735	00 0100 02		SFM LNK	; Skip 2 on link
736	02 0100 00		FOM HLT	; Error
737	02 0100 00		FOM HLT	; Should never stop here
740	02 0001 00		FOM CLL	; Clear link
741	00 0101 02		SFM Not LNK	; Skip 2 on not link
742	02 0100 00		FOM HLT	; Error
743	02 0100 00		FOM HLT	; Should never stop here
744	06 1110 06		MSI 1, R1	; Set link
745	1		WORD 1 = .-1	
746	00 0100 02		SFM LNK	; Skip 2 on link
747	02 0100 00		FOM HLT	; Error
750	02 0100 00		FOM HLT	; Should never stop here
751	06 1000 06		MS Word 1, L1	; Restore Word 1, clear link
752	XX745			
753	00 0101 02		SFM Not LNK	; Skip 2 on not link
754	02 0100 00		FOM HLT	; Error
755	02 0100 00		FOM HLT	; Should never stop here
756	06 1010 06		MSI 100000, L1	; Set link
757	100000		WORD 2 = .-1	
760	00 0100 02		SFM LNK	; Skip 2 on link
761	02 0100 00		FOM HLT	; Error
762	02 0100 00		FOM HLT	; Should never stop here
763	06 1100 06		MS Word 2, R1	; Restore word 2, clear link
764	XX757			
765	00 0101 02		SFM Not LNK	; skip 2 on not link
766	02 0100 00		FOM HLT	; Error
767	02 0100 00		FOM HLT	; Should never stop here
770	07 0100 03		JC SC, ETZ, ERR	; Test JC
771	XX777			; Should never jump
772	10 0100 03		JC SWR, ETZ, Begin:	; Test JC
773	XX734			; Should jump if SWR = 0
774	02 0100 00		FOM HLT	; HLT, Error
775				
XX776	02 0100 00	ERR:	FOM HLT	; Error at XX770

Table 5-2

TEST 2 INSTRUCTIONS

0001	06 0010 03	MRI 1, TRP	; 1 to Trap
2	1		
3	03 0000 06	RM TRP, Word 3	; Instruction being tested
4	14		
5	06 1100 06	MS Word 3, R1	; Set link, zero word 3
6	14		
7	00 0100 02	SFM LNK	; Check link
10	02 0100 02	FOM HLT	; Error
11	02 0100 00	FOM HLT	; Should never stop here
12	02 0001 00	FOM CLL	; Clear link
13	06 0010 07	MRI 14, SC	; Word 3 to SC
14	14	Word 3 = -1	
15	02 0100 00	FOM HLT	; Error

5.2.3.3 Test 3 – Proceed as follows:

Step	Procedure

1. Use the Teletype and the TRM key to create a paper tape in the following format:

	.	Blank leader	
	.		
	.		
Control word 1	200_8	frame	1
Data left half	000		2
Data right half	000		3
Control word 2	200		4
Data left half	377		5
Data right half	377		6
Control word 3	200		7
Data left half	377		8
Data right half	000		9
Control word 4	200		10
Data left half	000		11
Data right half	377		12
	.		
	.	Blank Trailer	
	.		

This is a bootstrap format tape consisting of four data words:

000000
177777
177400
000377

Step	Procedure
2.	Using Appendix A as a reference, key in the basic processor bootstrap loader.
3.	Load the test tape (Step 1) using the bootstrap loader and verify that data have been loaded properly by examining memory using the READ switch. Note that this is the first use made of the TTO interface, TTI interface, I/O bus board, and IOI-IOP bus buffer. If trouble is encountered, the problem may lie in one of these areas.
4.	At this point, load the basic processor diagnostic program. If the program does not run and meaningful error reports are not made, attempt to load the Absolute Loader (refer to Section A.2).
5.	If the diagnostic program can then be loaded without errors, it may be executed in the single instruction mode or in short segments marked off by manually inserted HLT codes.
6.	If the diagnostic program cannot be loaded properly and the problem must be pursued (i.e., if module swapping does not clear up the problem), ensure that the Absolute Loader was loaded properly into memory.
7.	If the Absolute Loader is not in memory correctly, the bootstrap loader is malfunctioning and must be used as a tool in troubleshooting.
8.	If the Absolute Loader is in memory correctly, this program must then be used to locate the error. In using a loader program to find a problem, single-step through the program visually verifying each step by the console indicators.
9.	If it is a dynamic problem and stepping does not reveal the trouble, program traps can be set into the loader or test loops can be keyed in.
10.	If the problem appears to be memory and not the processor at all, load the Memory Exerciser program instead of the basic processor diagnostic. For many marginal problems, the program can be loaded but not executed at full speed. The Memory Exerciser may provide more meaningful diagnostics in these cases.

5.3 TESTING SYSTEM OPERATORS

When the basic processor and memory are functioning properly, and a failure is suspected in a system operator, trouble-shooting is greatly simplified. Tests can be made directly from the console, or a diagnostic program for the suspected operator can be loaded and run.

5.3.1 Testing From The Console

The TRM and DISP keys can be used to send data to and receive data from any system operator by placing that operator's address in the DEVICE SELECT switch. This feature is a powerful tool in system debugging. By setting 77 on the

DEVICE SELECT switch, the rightmost 8 bits of the switch register can be sent to the Teletype output interface by depressing TRM. This 8-bit character is then printed automatically if the operator and device are working properly. All ASCII characters can be printed in this manner from the console.

By striking a Teletype key and then depressing DISP, the 8-bit code for the key is displayed in the DATA DISPLAY register. Thus, a high degree of confidence can be established for the TTI interface, TTO interface, and the Teletype by manipulating switches at the console.

An operator such as the Arithmetic Operator can be tested in the same manner. Various operands can be transmitted to the AX and AY registers, and the AO register can be displayed to verify proper operation. The AO functions can be changed manually by transmitting SWR bits 8 and 9 to the MSR (device address 17).

5.3.2 Diagnostic Programs

Each system operator is provided with a diagnostic program that is designed to make an exhaustive test on that device. It is assumed that test verification is done using only those parts of the system that are known to be good. Consult each diagnostic program writeup before using the program to ensure that the minimum functional hardware is available to test the suspected operator.

5.4 TYPICAL FAILURE SYMPTOMS

5.4.1 Input Bus Lines

Bus lines that provide input to the basic processor, such as the Destination Data Bus, are shared by all the operators in a common collector line. This scheme is depicted in Figure 5-16.

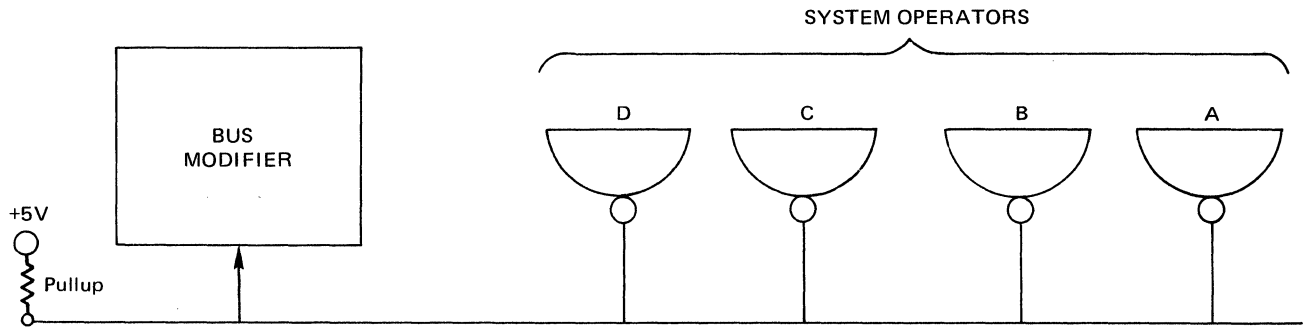


Figure 5-16 Common Collector Bus Line

The gates driving these lines are open collector gates and appear as an open to the line when the gate input is low. Thus, when all gates are off, the line is free and is pulled up to +5V by the pull-up resistor in the processor. If a gate is on, it grounds the line. If two gates are on, the line is still grounded with no indication that two gates are on instead of one. Several conclusions can be drawn as follows:

a. A bit pickup on the line can be caused by a bad gate within the active operator, a bad gate within any other operator gated onto the line, or by any ground path to the line.

b. A bit drop on the line can be caused by a bad gate within the active operator, but cannot be caused by failures anywhere else in the system.

Note that failing input gates in the processor can give the appearance of a failing input bus line.

5.4.2 Output Bus Lines

Bus lines that provide output to the system operators are driven by circuits in the basic processor.

Bit pickups on the line can be caused only by a bad driver gate in the processor. Bit drops can be caused by a bad driver gate or may be the result of a grounded bus line. In neither case is the fault due to system operator gates. See Figure 5-17.

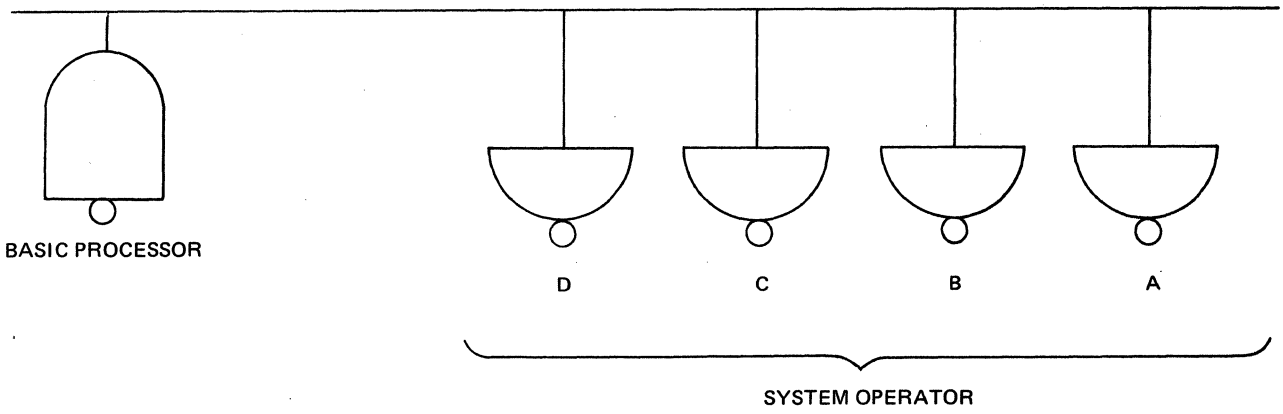


Figure 5-17 Processor Driven Bus Line

5.4.3 Memory Failures

Proper memory operation is highly dependent upon the proper level of the -20V supply at the current operating temperature. In analyzing voltage vs. operating temperature, refer to the Memory Margin Procedure and accompanying plot shipped with the machine. The temperature referenced is ambient as measured in the area 5 inches below the computer chassis. The memory system should operate at a voltage ±0.5 of that shown on the graph.

Bit pickups in memory indicate a high memory voltage, whereas bit drops indicate a low memory voltage. Memory operation is such that, during the read cycle, all cores are driven to 0. Cores that change state were then 1's and the change produces a sense amplifier output to set the MB register. Dropped bits are often caused by a low gain or pattern-sensitive sense amplifier. An oversensitive sense amplifier could produce an erroneous output (and thus a bit pickup), but this situation is very rare.

During the write cycle, all cores are driven to 1's except those that are inhibited by the inhibit driver circuits. Inhibit driver circuits are enabled by the 0 state of an MB bit. The inhibit driver circuits typically fail in the off condition, rather than on, causing a bit pickup. Thus, as a general rule, if a single bit failure is common to one core memory board, a bit drop is likely caused by a faulty sense amplifier and a bit pickup by an inhibit driver.

Other memory failures are due to read-write driver and selection switch circuits. These failures are common to certain groups of addresses within one memory board.

5.5 MAJOR SUBASSEMBLY REPLACEMENT PROCEDURES

5.5.1 Console

Use the following procedure to replace the console.

Step	Procedure
1.	Turn off the computer and disconnect the external ac line voltage. If this is not done, ac line voltage is present on the console POWER switch.
2.	Remove PC1, PC2, and PC3.
3.	Gently remove the PDB card. Do not place any strain on the flat cables between the console and the card. To remove the card, insert the tip of the index finger between the upper corner of the PDB board and the processor bus, then gently pull the card loose at the top. The card can be pulled loose at the bottom in the same manner.
4.	Fasten the PDB card to the back side of the console with rubber bands or masking tape. Do not allow the card to dangle and thereby strain the flat cable.
5.	Disconnect the console wiring from the power supply terminal strip.
6.	Remove the console and leaf hinge from the computer frame. Support the console while it is being removed.
7.	To reinstall the console, simply reverse the above procedure.

5.5.2 Power Supply

To remove the power supply, proceed as follows:

Step	Procedure
1.	Remove the console as described in paragraph 5.5.1.
2.	Remove all external wiring from the terminal strip on the front of the power supply.
3.	Remove the power supply retaining rod. This rod runs vertically through the chassis, connecting the top and bottom and passing through the right-hand power supply supply guide channels. This rod is located in front of the supply and prevents the supply from sliding forward.
4.	Pull the supply forward far enough to disconnect the power supply wiring from the bus boards.
5.	Slide the power supply forward and remove it.
6.	To install a new supply, reverse the above procedure. When installing a new supply, the power leads must be properly connected to prevent damage to the computer. Power and signal names are clearly etched onto the bus boards next to the fast tab terminal connectors. Wiring runs to the same type connectors on the power supply printed circuit card inside the supply. After installing a new supply and before connecting power, check the wiring between the power supply PC board (see Figure 5-18) and the bus boards to ensure proper connection.

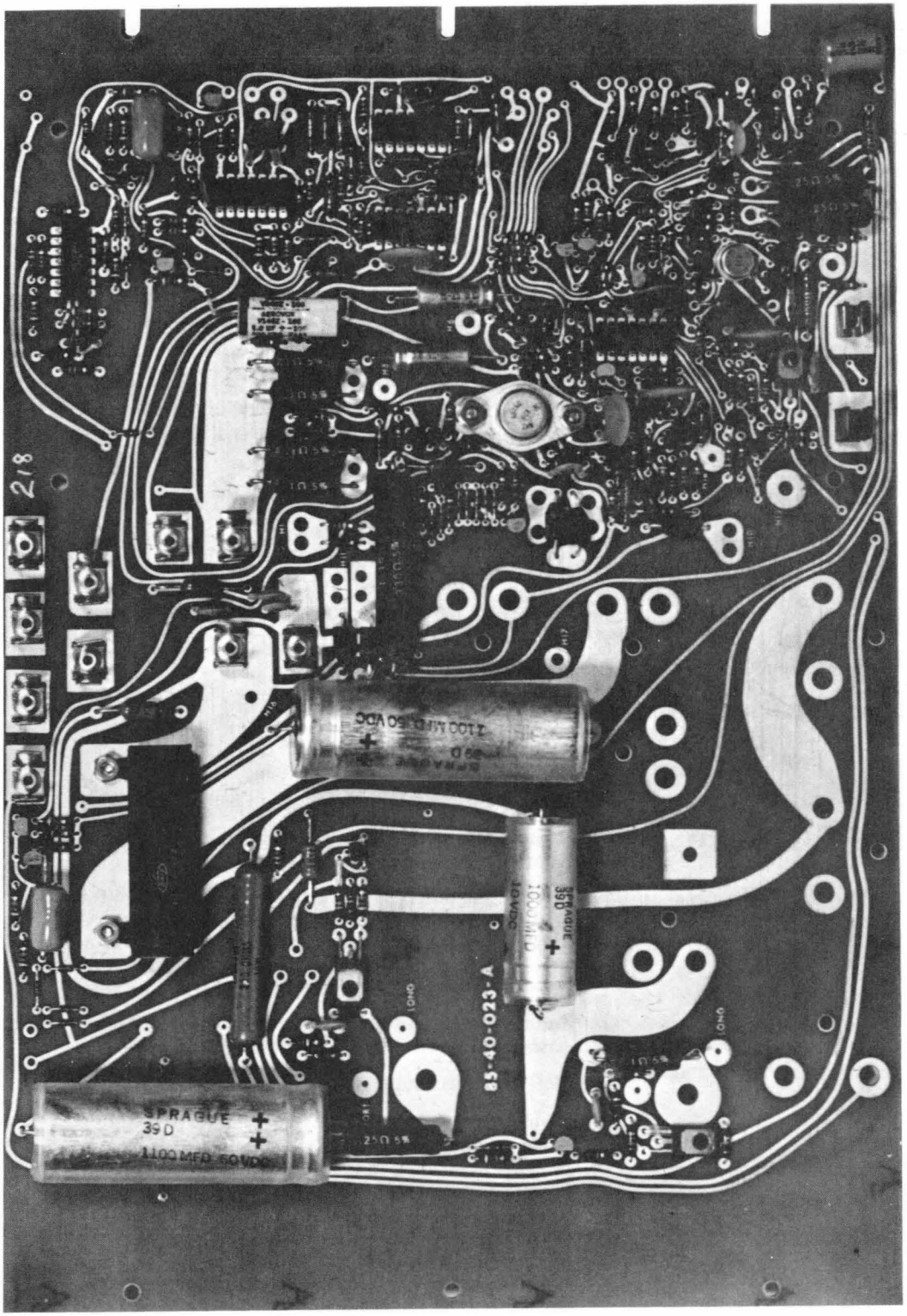


Figure 5-18 Power Supply Printed Circuit Card

5.5.3 Console Bulb Replacement

When electrical measurements on the console PC card indicate that a bulb is burned out, replace it in the following manner:

Step	Procedure
1.	Remove the console as outlined in Section 5.5.1.
2.	Place the console face down on a table with the flat cables and PDB card extending out to the left.
3.	Remove the eight screws holding the printed circuit card to the frame (four along the top and four along the bottom).
4.	Lift the PC card out of the console frame. Some pressure is required to draw the spring-loaded switches through the horizontal slot in the front cover panel.
5.	Remove the light guide that directs lamp illumination onto the display panel. The guide is held by three screws through the PC board into the guide from the rear.
6.	Remove and replace lamps by soldering. Use a heat sink to prevent excessive heat on the lamp leads from damaging the lamp filaments.
7.	Replace the light guide.
8.	Using 2 in. masking tape, fasten the eight console control switches together as shown in Figure 5-19.

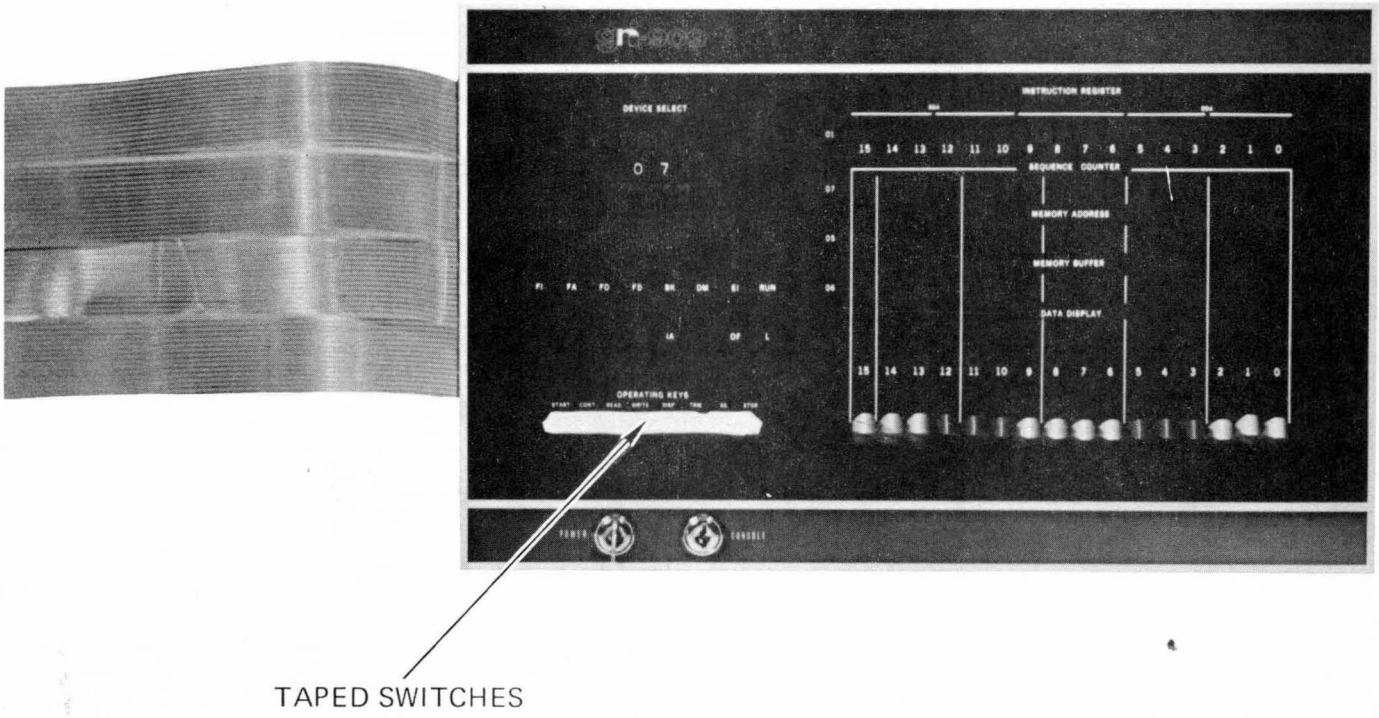


Figure 5-19 Taped Control Switches

9.	Reassemble the console and printed circuit frames. The taped switches greatly simplify this procedure.
10.	Ensure that the DEVICE SELECT switch is seated through the square hole in the display panel. Then install the eight screws removed in Step 3.
11.	Install the console as described in paragraph 5.5.1.

5.5.4 Bus Boards

When it is necessary to remove or replace a bus board, remove the entire top of the computer chassis and lift out the bus board. Proceed as follows:

Step	Procedure
1.	Disconnect power and set the computer chassis on a flat table.
2.	Remove all PC cards.
3.	Remove the frame top section by removing the machine screws and sheet metal screws at the top of the front vertical corner flanges and the rear vertical frame corners. The front vertical corner flanges are each secured with two machine screws and nuts; the rear corners are secured by sheet metal screws.
4.	After disconnecting all bus wiring, lift the memory bus out of the frame.
5.	After disconnecting all wires, lift the processor and I/O bus boards out as an assembly.
6.	To separate the processor and I/O buses, remove the machine screws holding the standoff between the boards.
7.	Reverse the procedure to install a new bus board.

APPENDIX A
LOADERS

Before a program can be executed, it must be brought into memory. To bring a program into memory, a loading program must already reside in core. If the memory is empty, the console switches are used to load in a bootstrap loader, which is ordinarily used only to bring in a more extensive block loader. This block loader program is then used to read the object tapes of all other programs. Both the bootstrap and the block loader usually reside in high core where they are not disturbed by any of the standard GRI-909 software. If an undebugged user routine accidentally destroys either loader, the loaders can be restored by first reloading the bootstrap manually.

There are several bootstrap loaders, depending on which functional operators are included in the system. For each loader, there are two versions: one for the Teletype reader, the other for the high-speed reader.

For a complete description of all loaders, refer to the *GRI-909 Loaders Manual.*

NOTE

In the loader descriptions, the letters XX designate the portion of the address that varies according to the core size of the individual machine. The digits that replace the X's are determined by the highest locations in core. For example: if the machine has 4K of core memory and a load address of XX555 is specified, the actual load address is 07555. (The highest location is 07777 for a 4K machine.)

Specific addresses are assigned for using the boostrap and absolute loader tapes. The tape number specifies the tape format. The tape number is in the following form:

7n - nn - nnnY-Z

where:

7 = Software engineering

n = numeric designations as to category and release order

Y = letter designating tape format

- A = Absolute
- B = Bootstrap
- D = Directory
- R = Relocatable
- X = Relocatable Source

Z = Letter or number designating revision level

A.1 BOOTSTRAP LOADER (%BLD)

The primary purpose of the bootstrap loader is to load the absolute loader (%ALH); however, for the purposes of this manual the basic processor bootstrap loader, which cannot be used to load %ALH, is described first. Section A.1.3 describes the version of %BLD that is used to load %ALH.

A.1.1 Basic Processor Bootstrap Loader

The bootstrap loader reads a bootstrap format object from paper tape and loads it into memory. No tests are performed on the data from the reader to verify that the data have been read correctly.

The basic processor bootstrap loader does not use the AO registers or functions. As a result, this loader is useful for troubleshooting if the AO is faulty (or is suspected) and the AO diagnostic must be loaded.

To load the basic processor bootstrap loader, proceed as follows:

NOTE

If the loader is to be used with a reader other than the Teletype reader, all reference to device address 77 must be changed to the new device address (e.g., for the high-speed reader, change 77 to 76).

Step	Procedure
1.	Key in the following sequence of instructions:

Location	Instruction
XX727	02 0100 00
XX730	02 1001 77
XX731	77 1000 02
XX732	00 0100 03
XX733	0XX731
XX734	77 0100 03
XX735	0XX727
XX736	77 0000 06
XX737	0XX761
XX740	77 0000 06
XX741	0XX772
XX742	02 1001 77
XX743	77 1000 02
XX744	00 0100 03
XX745	0XX743
XX746	77 0001 06
XX747	0XX770
XX750	02 1001 77
XX751	77 1000 02
XX752	00 0100 03
XX753	0XX751
XX754	77 0000 06
XX755	0XX757
XX756	06 1010 06
XX757	0
XX760	06 1110 06
XX761	0
XX762	00 0100 02
XX763	00 0100 03

Location	Instruction
XX764	0XX756
XX765	06 1000 06
XX766	0XX757
XX767	06 1000 06
XX770	
XX771	06 1110 06
XX772	0
XX773	00 0100 02
XX774	00 0100 03
XX775	0XX765
XX776	00 0100 03
XX777	0XX730

Key load address -1 into XX770. Start at XX730.

Step	Procedure
2.	Set XX770 in the Data Switch Register
3.	Set the DEVICE SELECT switches to 07 and depress TRM.
4.	Set the first address -1 of the program to be loaded in the Data Switch Register.
5.	Push the WRITE key up.
6.	Set XX730 in the Data Switch Register.
7.	Depress TRM.
8.	Mount the bootstrap tape in the reader and turn the reader on.
9.	Depress START. The loader halts each time it reads a zero word until it reads a non-zero word.
10.	Depress CONT as many times as necessary.

NOTE

This version of the bootstrap loader is for basic diagnostics purposes only and cannot be used to load the absolute loader. Use the version detailed in Section A.1.2

A.1.2 %BLD to Load %ALH

It is assumed that after the absolute loader has been loaded, the bootstrap loader is no longer necessary; therefore, location zero has been chosen as the starting address. In this location, the bootstrap will most likely be destroyed by other programs loaded later. To locate the loader in a different core area, simply increase all addresses by the value of the address that is chosen to start keying in the program (e.g., to key in at 7000, add 7000 to all internal addresses).

To load the version of %BLD that is used to load %ALH proceed as follows:

NOTE

If the loader is to be used with a reader other than the Teletype reader, all references to device address 77 must be changed to the new device address (e.g., for the high-speed reader, change 77 to 76).

Step	Procedure

1. Key in the following:

```
00000 00 0100 03        JU      GET0
00001 000023
00002 11 1000 12        RR      AX, L1, AY
00003 12 1000 12        RS      AY, L1
00004 12 1000 12        RS      AY, L1
00005 12 1000 12        RS      AY, L1
00006 12 1000 12        RS      AY, L1
00007 12 1000 12        RS      AY, L1
00010 12 1000 12        RS      AY, L1
00011 12 1000 12        RS      AY, L1
00012 00 0100 03        JU      GET0
00013 000023
                ; FOR OTHER THAN %ALH SET
                ; SECOND WORD OF NEXT INSTRUCTION
                ; TO ADDRESS -1 OF LOAD ADDRESS
00014 13 0011 06        RMID    AO , .
00015 000014
00016 00 0100 03 START: JU      GET0    ; START PROGRAM HERE
00017 000023
00020 11 0110 03        JO      AX, NEZ, .-20; PRESS CONTINUE
00021
00022 02 0100 00        FOM     HLT     ; UNTIL NON 0 READ
00023 02 1001 77  GET0: F0      CLIF STRT, TTI; OR HSR
00024 77 1000 02        SF      TTI, IRDY
00025 06 0010 07        MRI     .-2, SC
00026 000023
00027 77 0000 11        RR      TTI, AX
00030 03 0000 07        RR      TRP, SC
```

2. Set 16 on the Data Switch Register.
3. Depress TRM.
4. Depress START once. The loader halts each time, it reads a zero word until it reads a non-zero word.

A.1.4 Bootstrap Tape Format

The bootstrap tape format is:

Blank Tape

.

.

.

Space

Control Code (200_8)

Bits 15-8 of Data Word 1

Bits 7-0 of Data Word 1

Control Code (200_8)

Bits 15-8 of Data Word 2

Bits 7-0 of Data Word 2

.

.

.

Space

A.2 ABSOLUTE LOADER (%ALH)

The absolute loader loads the user's object program into memory. It differs from the bootstrap loader in that it loads a tape of a different format, checks to ensure correct loading , and is capable of loading data into non-sequential areas of memory.

An object tape in absolute format consists of a series of data blocks as follows:

Space	
Control Code	(001)
Checksum	(2 frames)
Block Start Address	(2 frames)
Data Word Count	(2 frames)
Data Word	(2 frames per word)
.	
.	
.	
.	
.	
Data Word	
Block Trailer	(20_8 null frames)

The Control Code indicates the beginning of a block. The checksum is the 16-bit sum, ignoring overflows, of the Block Start Address, the Data Word Count, and the Data Words. The Block Start Address is the first location into which this block of data is to be loaded sequentially. The Data Word Count is the number of data words contained in the block.

A.2.1 Using %ALH

The following procedure is used to read a tape in absolute format:

Step	Procedure
1.	Using the key-in bootstrap loader, load %ALH into memory.
2.	Set 07 on the DEVICE SELECT switches.
3.	Set XX661 on the Data Switch Register.
4.	Depress TRM.
5.	Position bit 15 of the Data Switch register to select a reader, 0 = high-speed reader 1 = Teletype reader
6.	Mount the object tape in the reader. Ensure a null frame preceding the first block is under the head.
7.	Depress START.
8.	If the SC = XX661, the program has loaded correctly, and %ALH is ready to load another. Begin at Step 3.
9.	If execution is halted at another location, there is an error: *a.* SC = XX676 indicates a control code error. Reposition to beginning of block and go to Step 8. *b.* SC = XX733 indicates a checksum error. Reposition to beginning of block and depress START.

NOTE

The last location loaded is XX720.

The absolute loader (block loader) is available in many versions, depending on the available firmware and amount of memory. Refer to the *GRI-909 Loaders Manual* for a complete description.

APPENDIX B
CODES

B.1 DEVICE SELECTION CODES

The GRI-909 architecture allows 6 bits for addressing source and destination operators. This provides a range of $00_8 - 77_8$ or 64_{10} addresses of each type. Several of these addresses are used in conjunction with the basic machine and others are assigned to some of the most popular options. Those addresses currently assigned are included in the Table B-1.

Table B-1

DEVICE SELECT CODES

DEVICE SELECT Code	Abbreviation	Description	Source or Destination of Data
00	–	Null	S
00	–	Null	D
01	IR	Instruction Register	S
01	IR	Instruction Register	D
02	FO	Function Output	S
02	SF	Sense Function	D
03	TRP	Trap	S
03	–	Data Tests and Memory to Trap Register	D
04	ISR	Interrupt Status Register	S
04	ISR	Interrupt Status Register	D
05	MA	Memory Address	S
05	MA	Memory Address	D
06	MB	Memory Buffer	S
06	MB	Memory Buffer	D
07	SC	Sequence Counter	S
07	SC	Sequence Counter	D
10	SWR	Data Switch Register	S
11	AX	AX Register	S
11	AX	AX Register	D
12	AY	AY Register	S
12	AY	AY Register	D
13	AO	Arithmetic Operator	S
13	AO	Arithmetic Operator	D
14	–	Unused	–
14	EAO	Extended Arithmetic Operator	D
15	ED	External Data	S
15	ED	External Data	D
16	EAS	External Address	S
16	EAS	External Address	D
17	MSR	Machine Status	S
17	MSR	Machine Status	D

Table B-1

DEVICE SELECT CODES (Cont.)

DEVICE SELECT Code	Abbreviation	Description	Source or Destination of Data
20	–	Unused	S
20	–	Unused	D
21	–	Unused	–
21	–	Unused	–
22	–	Unused	–
22	–	Unused	D
23	–	Unused	S
23	–	Unused	D
24	BSW	Byte Swap	S
24	BSW	Byte Swap	D
25	BPK	Byte Pack	S
25	BPK	Byte Pack	D
26	BCA	Byte Comparator A	S
26	BCA	Byte Comparator A	D
27	BCB	Byte Comparator B	S
27	BCB	Byte Comparator B	D
30	GP1	General Purpose Register 1	S
30	GP1	General Purpose Register 1	D
31	GP2	General Purpose Register 2	S
31	GP2	General Purpose Register 2	D
32	GP3	General Purpose Register 3	S
32	GP3	General Purpose Register 3	D
33	GP4	General Purpose Register 4	S
33	GP4	General Purpose Register 4	D
34	GP5	General Purpose Register 5	S
34	GP5	General Purpose Register 5	D
35	GP6	General Purpose Register 6	S
35	GP6	General Purpose Register 6	D
36	–	Unused	S
36	–	Unused	D
37	–	Unused	S
37	–	Unused	D
40	–	Unused	S
40	–	Unused	D
41	–	Unused	S
41	–	Unused	D
42	–	Unused	S
42	–	Unused	D
43	–	Unused	S
43	–	Unused	D
44	–	Unused	S
44	–	Unused	D
45	–	Unused	S
45	–	Unused	D

Table B-1

DEVICE SELECT CODES (Cont.)

DEVICE SELECT Code	Abbreviation	Description	Source or Destination of Data
46	–	Unused	S
46	–	Unused	D
47	–	Unused	S
47	–	Unused	D
50	BIM	Binary Input Mux	S
51	BOM	Binary Output Mux	D
52	–	Unused	S
52	–	Unused	D
53	–	Unused	S
53	–	Unused	D
54	–	Unused	S
54	–	Unused	D
55	–	Unused	S
55	–	Unused	D
56	–	Unused	S
56	–	Unused	D
57	GRI	GRI-sette	S
57	GRI	GRI-sette	D
60	WIT	Watchdog Interval Timer	S
60	WIT	Watchdog Interval Timer	D
61	DAC	D/A Converter	D
62	GOR	General Output Register	S
62	GOR	General Output Register	D
63	GI	Gate Input Register	S
64	MUX	Multiplexer	S
64	MUX	Multiplexer	D
65	ADC	A/D Converter	S
65	–	Unused	D
66	WCT	Disk Word Count	S
66	WCT	Disk Word Count	D
67	CAD	Disk Core Address	S
67	CAD	Disk Core Address	D
70	DISK	Disk Controller	S
70	DISK	Disk Controller	D
71	LPR	Line Printer	D
72	–	Unused	S
72	–	Unused	D
73	CRD	Card Reader	S
73	CRD	Card Reader	D
74	–	Unused	S
74	–	Unused	D
75	RTC	Real-Time Clock	DMA
75	RTC	Real-Time Clock	Only

Table B-1

DEVICE SELECT CODES (Cont.)

DEVICE SELECT Code	Abbreviation	Description	Source or Destination of Data
76	HSP	High-speed Reader	S
76	HSP	High-speed Punch	D
77	TTI	Teletype Input	S
77	TTO	Teletype Output	D
NA	PID	Pulse Input Detector	

B.2 INTERRUPT STATUS AND TRAPS

Interrupt devices can interrupt (TRAP) to locate 0 or to a memory location of choice. These devices utilize one bit of the interrupt status register (ISR) for ease of program interrupt control. Those trap locations and status bits currently assigned and considered standard are included in Table B-2.

Table B-2

TRAP LOCATIONS

Interrupt		Device	Abbreviation	Operator Code
Status Bit	Trap Location			
	0	Power Failure		00
	0	Breakpoint		01
0	11	Teletype Output	TTO	77
1	14	Teletype Input	TTI	77
2	17	High-speed Punch	HSP	76
3	22	High-speed Reader	HSR	76
4	25	Card Reader	CRD	73
5	30	Line Printer	LPR	71
6	36*	General Output Register	GOR	62
	44*	Gate Input Card	GI	63
7	–	Unused	–	–
8	104-124	Pulse Input Detector	PID	NA
9	–	Unused	–	–
10	–	Unused	–	–
11	100	Real-time Clock	RTC	75
12	52	A/D Converter	ADC	65
13	–	Unused	–	–
14	53-55	Disk	Disk	66-70
15	25	Watchdog Interval Timer	WIT	61

*For test purposes only.

B.3 TELETYPE CODES

Table B-3 lists the complete Teletype code set. Codes generated by the keyboard may have a 1 or 0 in the most significant bit depending on the Teletype model. For no parity Teletypes, the eighth channel is always punched 1's. In the case of even parity, the eighth channel is either punched or not punched, depending on the number of bits in the particular frame.

The lower-case character set (codes 340-376) is not available on the Model 33. Specifying one of the lower-case codes causes the Teletype to print the corresponding upper case character. Definitions of control codes are those given by the ASCII code set. Most control codes, however, have no effect on the Teletype and their definitions bear no necessary relation to the use of the codes in conjunction with the GRI-909 software.

Table B-3

TELETYPE CODES (No Parity TTY)

8-Bit Octal Code	Character	Remarks
200	NUL	Null, tape feed. Control shift P.
201	SOH	Start of heading; also start of message (SOM). Control A.
202	STX	Start of text; also end of address (EOA). Control B.
203	ETX	End of text; also end of message (EOM). Control C.
204	EOT	End of transmission; shuts off TWX machines. Control D.
205	ENQ	Inquiry; also WRU, "Who are you?" Triggers identification ("Here is .....".)
206	ACK	Acknowledge; also RU, "Are you ...?" Control F.
207	BEL	Rings the bell. Control G.
210	BS	Backspace; also format effector (FEO). Backspaces some machines. Control H.
211	HT	Horizontal tab. Control I.
212	LF	Line feed or line space; advances paper to next line. Duplicated by Control J.
213	VT	Vertical tab. Control K.
214	FF	Form feed to top of next page. Control L.
215	CR	Carriage return to beginning of line. Control M.
216	SO	Shift out; changes ribbon color to red. Control N.
217	SI	Shift in; changes ribbon color to black. Control O.
220	DLE	Data link escape. Control P (DCO).
221	DC1	Device control 1, turns transmitter (reader) on. Control Q (X ON).
222	DC2	Device control 2, turns punch or auxiliary on. Control R (TAPE, AUX ON).
223	DC3	Device control 3, turns transmitter (reader) off. Control S (X OFF).
224	DC4	Device control 4, turns punch or auxiliary off. Control T (AUX OFF).
225	NAK	Negative acknowledge; also error (ERR). Control U.
226	SYN	Synchronous idle. Control V.
227	ETB	End of transmission block; also logical end of medium (LEM). Control W.

Table B-3

TELETYPE CODES (Cont.)

8-Bit Octal Code	Character	Remarks
230	CAN	Cancel. Control X.
231	EM	End of medium. Control Y.
232	SUB	Substitute. Control Z.
233	ESC	Escape, prefix. This code is also generated by control shift K.
234	FS	File separator. Control shift L.
235	GS	Group separator. Control shift M.
236	RS	Record separator. Control shift N.
237	US	Unit separator. Control shift O.
240	SP	Space
241	!	
242	"	
243	#	
244	$	
245	%	
246	&	
247	'	Accent acute or apostrophe.
250	(	
251	)	
252	*	
253	+	
254	,	Comma.
255	–	
256	.	
257	/	
260	0	
261	1	
262	2	
263	3	
264	4	
265	5	
266	6	
267	7	
270	8	
271	9	
272	:	
273	;	
274	<	
275	=	
276	>	
277	?	
300	@	
301	A	
302	B	
303	C	

Table B-3

TELETYPE CODES (Cont.)

8-Bit Octal Code	Character	Remarks
304	D	
305	E	
306	F	
307	G	
310	H	
311	I	
312	J	
313	K	
314	L	
315	M	
316	N	
317	O	
320	P	
321	Q	
322	R	
323	S	
324	T	
325	U	
326	V	
327	W	
330	X	
331	Y	
332	Z	
333	[	Shift K.
334	/	Shift L.
335	]	Shift M.
336	↑	
337	←	
340	'	Accent grave.
341	a	
342	b	
343	c	
344	d	
345	e	
346	f	
347	g	
350	h	
351	i	
352	j	
353	k	
354	l	
355	m	
356	n	
357	o	

Table B-3

TELETYPE CODES (Cont.)

8-Bit Octal Code	Character	Remarks
360	p	
361	q	
362	r	
363	s	
364	t	
365	u	
366	v	
367	w	
370	x	
371	y	
372	z	
373		
374		
375		On early versions, either of these codes may be generated by either the ALT MODE or ESC key.
376		
377	DEL	Delete, rub out.

Teletype Keys That Generate No Codes

REPT	Causes any other key that is struck to repeat continuously until REPT is released.
LOC LF	Local line feed.
LOC CR	Local carriage return.
BREAK	Opens the line (machine sends a continuous string of null characters).
BRK RLS	Break release (not applicable).
HERE IS	Transmits predetermined 20-character message.

APPENDIX C
NUMERICAL TABLES

POWERS OF TWO IN DECIMAL

2^{η}	η	$2^{-\eta}$
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25

POWERS OF TEN IN OCTAL

10^{η}	η	$10^{-\eta}$
1	0	1.000 000 000 000 000 00
12	1	0.063 146 314 631 463 146 31
144	2	0.005 075 341 217 270 243 66
1 750	3	0.000 406 111 564 570 651 77
23 420	4	0.000 032 155 613 530 704 15
303 240	5	0.000 002 476 132 610 706 64
3 641 100	6	0.000 000 206 157 364 055 37
46 113 200	7	0.000 000 015 327 745 152 75
575 360 400	8	0.000 000 001 257 143 561 06
7 346 545 000	9	0.000 000 000 104 560 276 41
112 402 762 000	10	0.000 000 000 006 676 337 66
1 351 035 564 000	11	0.000 000 000 000 537 657 77
16 432 451 210 000	12	0.000 000 000 000 043 136 32
221 411 634 520 000	13	0.000 000 000 000 003 411 35
2 657 142 036 440 000	14	0.000 000 000 000 000 264 11
34 327 724 461 500 000	15	0.000 000 000 000 000 022 01
434 157 115 760 200 000	16	0.000 000 000 000 000 001 63
5 432 127 413 542 400 000	17	0.000 000 000 000 000 000 14
67 405 553 164 731 000 000	18	0.000 000 000 000 000 000 01

OCTAL TO DECIMAL CONVERSION, INTEGERS

Octal 0000-0777
Decimal 0000-0511

Octal	*Decimal*
10000	4096
20000	8192
30000	12288
40000	16384
50000	20480
60000	24576
70000	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

Octal 1000-1777
Decimal 0512-1023

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL TO DECIMAL CONVERSION, INTEGERS

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

Octal	2000-2777
Decimal	1024-1535

Octal	*Decimal*
10000	*4096*
20000	*8192*
30000	*12288*
40000	16384
50000	20480
60000	24576
70000	28672

Octal 3000-3777
Decimal 1536-2047

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

OCTAL TO DECIMAL CONVERSION, INTEGERS

Octal 4000-4777
Decimal 2048-2559

Octal	*Decimal*
10000	4096
20000	8192
30000	12288
40000	16384
50000	20480
60000	24576
70000	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	25
4720	2512	2513	2514	2515	2516	2517	2518	25
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

Octal 5000-5777
Decimal 2560-3071

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL TO DECIMAL CONVERSION, INTEGERS

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

Octal 6000-6777
Decimal 3072-3583

Octal	*Decimal*
10000	4096
20000	8192
30000	12288
40000	16384
50000	20480
60000	24576
70000	28672

Octal 7000-7777
Decimal 3584-4095

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3859
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	2963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

OCTAL TO DECIMAL CONVERSION, FRACTIONS

Octal	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*
.00000	.000000	.10000	.125000	.20000	.250000	.30000	.375000	.40000	.500000
.00100	.001953	.10100	.126953	.20100	.251953	.30100	.376953	.40100	.501953
.00200	.003906	.10200	.128906	.20200	.253906	.30200	.378906	.40200	.503906
.00300	.005859	.10300	.130859	.20300	.255859	.30300	.380859	.40300	.505859
.00400	.007812	.10400	.132812	.20400	.257812	.30400	.382812	.40400	.507812
.00500	.009765	.10500	.134765	.20500	.259765	.30500	.384765	.40500	.509765
.00600	.011718	.10600	.136718	.20600	.261718	.30600	.386718	.40600	.511718
.00700	.013671	.10700	.138671	.20700	.263671	.30700	.388671	.40700	.513671
.01000	.015625	.11000	.140625	.21000	.265625	.31000	.390625	.41000	.515625
.01100	.017578	.11100	.142578	.21100	.267578	.31100	.392578	.41100	.517578
.01200	.019531	.11200	.144531	.21200	.269531	.31200	.394531	.41200	.519531
.01300	.021484	.11300	.146484	.21300	.271484	.31300	.396484	.41300	.521484
.01400	.023437	.11400	.148437	.21400	.273437	.31400	.398437	.41400	.523437
.01500	.025390	.11500	.150390	.21500	.275390	.31500	.400390	.41500	.525390
.01600	.027343	.11600	.152343	.21600	.277343	.31600	.402343	.41600	.527343
.01700	.029296	.11700	.154296	.21700	.279296	.31700	.404296	.41700	.529296
.02000	.031250	.12000	.156250	.22000	.281250	.32000	.406250	.42000	.531250
.02100	.033203	.12100	.158203	.22100	.283203	.32100	.408203	.42100	.533203
.02200	.035156	.12200	.160156	.22200	.285156	.32200	.410156	.42200	.535156
.02300	.037109	.12300	.162109	.22300	.287109	.32300	.412109	.42300	.537109
.02400	.039062	.12400	.164062	.22400	.289062	.32400	.414062	.42400	.539062
.02500	.041015	.12500	.166015	.22500	.291015	.32500	.416015	.42500	.541015
.02600	.042968	.12600	.167968	.22600	.292968	.32600	.417968	.42600	.542968
.02700	.044921	.12700	.169921	.22700	.294921	.32700	.419921	.42700	.544921
.03000	.046875	.13000	.171875	.23000	.296875	.33000	.421875	.43000	.546875
.03100	.048828	.13100	.173828	.23100	.298828	.33100	.423828	.43100	.548828
.03200	.050781	.13200	.175781	.23200	.300781	.33200	.425781	.43200	.550781
.03300	.052734	.13300	.177734	.23300	.302734	.33300	.427734	.43300	.552734
.03400	.054687	.13400	.179687	.23400	.304687	.33400	.429687	.43400	.554687
.03500	.056640	.13500	.181640	.23500	.306640	.33500	.431640	.43500	.556640
.03600	.058593	.13600	.183593	.23600	.308593	.33600	.433593	.43600	.558593
.03700	.060546	.13700	.185546	.23700	.310546	.33700	.435546	.43700	.560546
.04000	.062500	.14000	.187500	.24000	.312500	.34000	.437500	.44000	.562500
.04100	.064453	.14100	.189453	.24100	.314453	.34100	.439453	.44100	.564453
.04200	.066406	.14200	.191406	.24200	.316406	.34200	.441406	.44200	.566406
.04300	.068359	.14300	.193359	.24300	.318359	.34300	.443359	.44300	.568359
.04400	.070312	.14400	.195312	.24400	.320312	.34400	.445312	.44400	.570312
.04500	.072265	.14500	.197265	.24500	.322265	.34500	.447265	.44500	.572265
.04600	.074218	.14600	.199218	.24600	.324218	.34600	.449218	.44600	.574218
.04700	.076171	.14700	.201171	.24700	.326171	.34700	.451171	.44700	.576171
.05000	.078125	.15000	.203125	.25000	.328125	.35000	.453125	.45000	.578125
.05100	.080078	.15100	.205078	.25100	.330078	.35100	.455078	.45100	.580078
.05200	.082031	.15200	.207031	.25200	.332031	.35200	.457031	.45200	.582031
.05300	.083984	.15300	.208984	.25300	.333984	.35300	.458984	.45300	.583984
.05400	.085937	.15400	.210937	.25400	.335937	.35400	.460937	.45400	.585937
.05500	.087890	.15500	.212890	.25500	.337890	.35500	.462890	.45500	.587890
.05600	.089843	.15600	.214843	.25600	.339843	.35600	.464843	.45600	.589843
.05700	.091796	.15700	.216796	.25700	.341796	.35700	.466796	.45700	.591796
.06000	.093750	.16000	.218750	.26000	.343750	.36000	.468750	.46000	.593750
.06100	.095703	.16100	.220703	.26100	.345703	.36100	.470703	.46100	.595703
.06200	.097656	.16200	.222656	.26200	.347656	.36200	.472656	.46200	.597656
.06300	.099609	.16300	.224609	.26300	.349609	.36300	.474609	.46300	.599609
.06400	.101562	.16400	.226562	.26400	.351562	.36400	.476562	.46400	.601562
.06500	.103515	.16500	.228515	.26500	.353515	.36500	.478515	.46500	.603515
.06600	.105468	.16600	.230468	.26600	.355468	.36600	.480468	.46600	.605468

OCTAL TO DECIMAL CONVERSION, FRACTIONS

Octal	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*
.06700	.107421	.16700	.232421	.26700	.357421	.36700	.482421	.46700	.607421
.07000	.109375	.17000	.234375	.27000	.359375	.37000	.484375	.47000	.609375
.07100	.111328	.17100	.236328	.27100	.361328	.37100	.486328	.47100	.611328
.07200	.113281	.17200	.238281	.27200	.363281	.37200	.488281	.47200	.613281
.07300	.115234	.17300	.240234	.27300	.365234	.37300	.490234	.47300	.615234
.07400	.117187	.17400	.242187	.27400	.367187	.37400	.492187	.47400	.617187
.07500	.119140	.17500	.244140	.27500	.369140	.37500	.494140	.47500	.619140
.07600	.121093	.17600	.246093	.27600	.371093	.37600	.496093	.47600	.621093
.07700	.123046	.17700	.248046	.27700	.373046	.37700	.498046	.47700	.623046

OCTAL TO DECIMAL CONVERSION, FRACTIONS

Octal	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*
.50000	.625000	.60000	.750000	.70000	.875000	.00000	.000000
.50100	.626953	.60100	.751953	.70100	.876953	.00001	.000030
.50200	.628906	.60200	.753906	.70200	.878906	.00002	.000061
.50300	.630859	.60300	.755859	.70300	.880859	.00003	.000091
.50400	.632812	.60400	.757812	.70400	.882812	.00004	.000122
.50500	.634765	.60500	.759765	.70500	.884765	.00005	.000152
.50600	.636718	.60600	.761718	.70600	.886718	.00006	.000183
.50700	.638671	.60700	.763671	.70700	.888671	.00007	.000213
.51000	.640625	.61000	.765625	.71000	.890625	.00010	.000244
.51100	.642578	.61100	.767578	.71100	.892578	.00011	.000274
.51200	.644531	.61200	.769531	.71200	.894531	.00012	.000305
.51300	.646484	.61300	.771484	.71300	.896484	.00013	.000335
.51400	.648437	.61400	.773437	.71400	.898437	.00014	.000366
.51500	.650390	.61500	.775390	.71500	.900390	.00015	.000396
.51600	.652343	.61600	.777343	.71600	.902343	.00016	.000427
.51700	.654296	.61700	.779296	.71700	.904296	.00017	.000457
.52000	.656250	.62000	.781250	.72000	.906250	.00020	.000488
.52100	.658203	.62100	.783203	.72100	.908203	.00021	.000518
.52200	.660156	.62200	.785156	.72200	.910156	.00022	.000549
.52300	.662109	.62300	.787109	.72300	.912109	.00023	.000579
.52400	.664062	.62400	.789062	.72400	.914062	.00024	.000610
.52500	.666015	.62500	.791015	.72500	.916015	.00025	.000640
.52600	.667968	.62600	.792968	.72600	.917968	.00026	.000671
.52700	.669921	.62700	.794921	.72700	.919921	.00027	.000701
.53000	.671875	.63000	.796875	.73000	.921875	.00030	.000732
.53100	.673828	.63100	.798828	.73100	.923828	.00031	.000762
.53200	.675781	.63200	.800781	.73200	.925781	.00032	.000793
.53300	.677734	.63300	.802734	.73300	.927734	.00033	.000823
.53400	.679687	.63400	.804687	.73400	.929687	.00034	.000854
.53500	.681640	.63500	.806640	.73500	.931640	.00035	.000885
.53600	.683593	.63600	.808593	.73600	.933593	.00036	.000915
.53700	.685546	.63700	.810546	.73700	.935546	.00037	.000946
.54000	.687500	.64000	.812500	.74000	.937500	.00040	.000976
.54100	.689453	.64100	.814453	.74100	.939453	.00041	.001007
.54200	.691406	.64200	.816406	.74200	.941406	.00042	.001037
.54300	.693359	.64300	.818359	.74300	.943359	.00043	.001068
.54400	.695312	.64400	.820312	.74400	.945312	.00044	.001098
.54500	.697265	.64500	.822265	.74500	.947265	.00045	.001129
.54600	.699218	.64600	.824218	.74600	.949218	.00046	.001159
.54700	.701171	.64700	.826171	.74700	.951171	.00047	.001190
.55000	.703125	.65000	.828125	.75000	.953125	.00050	.001220
.55100	.705078	.65100	.830078	.75100	.955078	.00051	.001251
.55200	.707031	.65200	.832031	.75200	.957031	.00052	.001281
.55300	.708984	.65300	.833984	.75300	.958984	.00053	.001312
.55400	.710937	.65400	.835937	.75400	.960937	.00054	.001342
.55500	.712890	.65500	.837890	.75500	.962890	.00055	.001373
.55600	.714843	.65600	.839843	.75600	.964843	.00056	.001403
.55700	.716796	.65700	.841796	.75700	.966796	.00057	.001434
.56000	.781750	.66000	.843750	.76000	.968750	.00060	.001464
.56100	.720703	.66100	.845703	.76100	.970703	.00061	.001495
.56200	.722656	.66200	.847656	.76200	.972656	.00062	.001525
.56300	.724609	.66300	.849609	.76300	.974609	.00063	.001556
.56400	.726562	.66400	.851562	.76400	.976562	.00064	.001586
.56500	.728515	.66500	.853515	.76500	.978515	.00065	.001617
.56600	.730468	.66600	.855468	.76600	.980468	.00066	.001647

OCTAL TO DECIMAL CONVERSION, FRACTIONS

Octal	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*	*Octal*	*Decimal*
.56700	.732421	.66700	.857421	.76700	.982421	.00067	.001678
.57000	.734375	.67000	.859375	.77000	.984375	.00070	.001708
.57100	.736328	.67100	.861328	.77100	.986328	.00071	.001739
.57200	.738281	.67200	.863281	.77200	.988281	.00072	.001770
.57300	.740234	.67300	.865234	.77300	.990234	.00073	.001800
.57400	.742187	.67400	.867187	.77400	.992187	.00074	.001831
.57500	.744140	.67500	.869140	.77500	.994140	.00075	.001861
.57600	.746093	.67600	.871093	.77600	.996093	.00076	.001892
.57700	.748046	.67700	.873046	.77700	.998046	.00077	.001922