gri-909

gate input card

GRI Computer Corporation
320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

Price $3.00

GRI-909

GATE INPUT CARD

GRI Computer Corporation, 320 Needham Street, Newton, Massachusetts 02164

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1071-500

GATE INPUT CARD

CHAPTER ONE

CHAPTER TWO

APPENDICES

CHAPTER I

GATE INPUT CARD

1.0 Introduction:

The Gate Input Card is one of a series of general operators used to interface most parallel data producing devices that require function control and testing operations. The operator also provides a complete interrupt system interface.

1.1 Specifications:

External Data Inputs	I15 through IØ. 16 inputs corresponding to computer word bits 15-0. Logic "0" = 0 to +0.4v Logic "1" = +2.5 to +12v 1 TTL unit load (+12v from source R $\geq$ 1K ohm)
External Status Inputs	EF1 and EF2, staples permit choice of positive or negative logic input conventions. Logic low = 0 to +0.4 Logic high = +2.5v to +12v 2.5 TTL unit loads (+12v from source R $\geq$ 1K ohm)
External Flag Input	FSP, staple permits choice of positive or negative logic input conventions. Logic low = 0 to +0.4v Logic high = +2.5v to +12v 5.5 TTL unit loads (+12v from source R $\geq$ 1K) Pulse in min. width = 15ns Level in, asserted edge (rise or fall), 0.4 to 2.4v in less than 1us.

All inputs normally provided with diode clamps to +5v. May be replaced with pull-up resistors to +5v for open collector drivers.

Device Address	Normally set for 63, selectable.
Priority Controls	ISR normally set for bit 6, selectable Interrupt trap address normally set for 44, (45,46), selectable.
Function Output Pulses	EP0, EP1, EP2, EP3 EP3 also clears operator flag. Output pulses negative going, 10 TTL unit load fan out, pulse width normally set for lus, may be changed by changing RC network. Pulse generators, standard 74121's. Positive pulses may be chosen by staple arrangement.
Power Requirements	+5v at 460 ma

1.2 Operation:

The operator functions as a source of data only. As a source, it may participate in any instruction which references it as a source device address. There is no suggested mnemonic for the operator, but it is recommended that the user select a mnemonic that suitable represents the external device interfaced to the operator. For purposes of this manual only, GI will be used as the mnemonic. Typical instructions for data transfers or tests are:

FAST	BASE	MACHINE CODE
GI TO AX	RR GI,AX	63 0000 11
GI TO ID 0	RMID GI,0	63 0011 06 000000
IF GI ETZ GO TO 100	JC GI,ETZ,100	63 0100 03 000100

The operator contains a ready flag which is connected to FTB33 and therefore, may be sensed via

SKIP IF GI [NOT] IRDY	SF GI,[NOT] IRDY	63 100[1/0]02

The two external status inputs may also be sensed via

SKIP IF GI [NOT] EF1	63 001 [1/0] 02
SKIP IF GI [NOT] EF2	63 010 [1/0] 02

The operator's flag may be cleared under program control by the function output command

CLIF TO GI	FO CLIF,GI	02 1000 63

This command also generates external pulse EP3. Pulses EP0, EP1, and EP2 may be generated via

EP0 TO GI	02 0001 63
EP1 TO GI	02 0010 63
EP2 TO GI	02 0100 63

The input flag is automatically cleared on power up or down, and by depressing the START key.

The device has a complete interrupt system connection. The ISR bit is normally connected to bit 6 for factory test purposes and may be changed by the user (see Appendix B). An address of 44, (45,46) is normally generated when an interrupt occurs. This address may be easily changed by the user (see Appendix B).

1.3 Programming:

The device operator is often used to interface a Digital Volt Meter to the GRI-909. A DVM will require a start conversion function and provide a conversion done or ready flag. We will also assume that the DVM has an over range indicator which will be connected to external flag input 1 (EF1). The mnemonics we will assign will be:

```
DVM  = 63          (DVM #1,63)
GTFS = 2           (GTFS #2,200)  ; greater than full scale
```

A program driven service routine to digitize a point and return the four BCD digits in AX might look like this:

```
DVMS:  CLL  ; clear over range indicator
       STRT CLIF TO DVM  ; take a reading
       SKIP IF DVM IRDY  ; wait for done
       I .-2 TO SC
       DVM TO AX
       SKIP IF DVM NOT GTFS  ; over range?
       STL                   ; yes, set link
       NOP
       TRP TO SC  ; exit
```

The BCD value in AX will now probably need to be converted to a binary integer and possible scaled. A conversion to binary integer format would be accomplished by a subroutine such as @SBI (BCD to integer).

CHAPTER II

APPLICATIONS

2.0 The gate input card will service a great range of devices for data input to a GRI-909. In most cases, all that will be necessary is proper choice of staple arrangements for positive or negative level inputs on flags and status lines (see Appendix B). The data line inputs are set up to handle only positive assertion logic. If negative assertion logic is used, the result of the operator may be 1's complemented while it is being read into another system register, e.g.

```
C GI TO AX      63 0010 11
```

will invert the data value automatically. The user may also increment the value as it is read in from the GI and thereby store the negative of the value (2's complement). Thus,

```
GI P1 TO I 0      63 0110 06
                  000000
```

will store the negative of the binary value read from GI if negative logic data lines are used.

There are four independent one shots (74121's) on GI to permit the user to select a variety of pulse widths for function commands. They are nominally set at the factory for 1.0us and negative polarity. If the user desires a different set of pulse widths or polarity, see Appendix B for instructions on changing the RC timing networks. The user should remember that a pulse width in excess of 1.76 us will cause the control pulse to possibly overlap the next instruction after the function output command that generated the pulse.

This may or may not be of consequence to the user, depending upon the action the device connected to GI takes on receipt of this function pulse.

All connections to the board are made via the standard 48-pin I/O cable plug and cable clamp assembly, S40-216. Ribbon cable, twisted pair, or miniature coax may be used. Cable shields may be terminated on one of the screws that fastens the cable clamp assembly to the board. Grounding is important and so is the cable length because the inputs on GI have no signal conditioning. Cable lengths should be kept less than twenty feet and every ground connection must be used. Each signal has an adjacent ground to permit running alternate wire grounds in a ribbon cable. Lines may be terminated at the device end to both +5 and ground as long as there is sufficient drive to activate the GI inputs or sufficient drive available from GI outputs. Table 2-1 is a listing of the external connections and their pin numbers.

TABLE 2-1

SIGNAL		PIN	GND	
IOH (LSB)	DATA IN	A	1	
I1H	"	B	2	
I2H	"	C	3	
I3H	"	D	4	
I4H	"	F	6	
I5H	"	H	7	
I6H	"	J	8	
I7H	"	K	9	
I8H	"	M	11	
I9H	"	N	12	
I10H	"	P	13	
I11H	"	R	14	
I12H	"	S	15	
I13H	"	T	16	
I14H	"	U	17	
I15H (MSB)	"	V	18	
FSPH(L)	FLAG SET IN	W	19	
EF1H(L)	STATUS 1 IN	X	20	
EF2H(L)	STATUS 2 IN	Y	21	
EPOL(H)	FUNC. PULSE 0 OUT	c	25	
EP1L(H)	FUNC. PULSE 1 OUT	b	24	
EP2L(H)	FUNC. PULSE 2 OUT	a	23	
EP3L(H)	FUNC. PULSE 3 OUT	z	22	(clear flag)

H = POSITIVE ASSERTION
L = LOW (GND) ASSERTION

H(L) = POSITIVE OR LOW ASSERTION (SEE APPENDIX B)

APPENDIX A

INSTALLATION

The GI device operator uses the interrupt system and therefore requires priority chain jumpers (S40-215) to be inserted in positions SE-5 and SF-6 in all vacant slots between the lefthand side of the machine, as viewed from the rear, and the GI board.

External connections are made to the operator via a 48-pin I/O connector and cable clamp assembly (S40-216 with S40-204 contacts). See Chapter 2 for signal connections.

Power must be turned off for insertion or withdrawal of any board, and the user should wait about 20 seconds after turning power off before withdrawing or inserting any board to give the $\pm$A (28VDC) voltages a chance to discharge.

APPENDIX B

DEVICE ADDRESS AND INTERRUPT SELECTION

Device Address Selection:

The device address selection consists of a dual row of staples marked "1" and "0" surrounding decoders (7430) in positions A1 (DAB decode) and L1 (SAB decode). To set an address in a board, insert staples in Row "1" for those SAB or DAB bits which are to be decoded as 1's. Insert staples in Row "0" for those SAB or DAB bits which are to be decoded as 0's. The example shown is for an address of 65_8. See Table B-1.

Device Interrupt Control:

Some devices provide for a choice of interrupt status bit and interrupt address generation. Where the interrupt status bit is to be chosen, the same SB and DB bits must be chosen. Interrupt address generation provides for up to four 1's to be generated on any of the 16 DB lines. For example, assume that the desired interrupt address for a device is 45_8, 46_8, 47_8. Only the first address of the group need be generated, and this will be the address that the SC is stored in when the interrupt occurs. The generated address plus 1 (46_8) will be the location in which program operation resumes after the interrupt. To generate 45_8, we need threee 1's generated, e.g.:

$$45_8 = 100101_2$$

DB bits 0, 2, 5 must be connected to the address generator gates. Note that one of the four gates is not required and is, therefore, left open.

The wiring of interrupt functions is described with each device manual in a tabular form.

NOTE: All device operators are set for a specific device address and interrupt controls at the factory in order to facilitate testing of the boards. The user may alter these addresses if he desires by following the instructions in the device manual. In systems where multiples of the same operator are used, the user must, of course, change the addresses and interrupt controls.

The interrupt controls, however, need not all be different. The same status bit, for example, is often assigned to a group of like devices. For example, 5 general output registers are put into a system. They may all be assigned to the same status bit, but each one will generate a unique interrupt address. When all boards are on the same status bit level, there is a hardware priority imposed by the order in which the boards are plugged into the rear of the GRI-909. This priority is determined by the PINL-POUTL chain and runs from left to right (highest to lowest) looking at the rear of the machine.

The Gate Input Card (GI) has provisions for user selection of interrupt status bit, interrupt address generation, pulse widths for external function pulses (4), external flag polarity selection, external status flag polarity selection, and clamp type selection on all inputs (diode or resistor pull up). The following tables describe the modifications which may be made to GI by the user.

Interrupt Status Bit Selection

Pick 1 DB and corresponding SB bit

SB bit	jumper area F	pick 1 line
DB bit	jumper area E	pick 1 line (same as SB bit)

(Set at factory for SB6H, DB6L)

Interrupt Address Generation

Address Generator Outputs TO DB lines

pad A		pick up to 4
B		
	(Set at factory for 44_8)	
C		
	(DB5L, DB2L)	
D		

Pulse Width Control of Function Pulses

PULSE	RT	CT	
EPOL	R28	C11	Do Not Use R32
EP1L	R29	C12	" R33
EP2L	R30	C13	" R34
EP3L	R31	C14	" R35

See Table B-2 normally set for 1us, R_T = 15K, C_T = 100pf

External Flag Set Pulse Polarity

POS GOING PULSE OR EDGE	CUT STAPLE e	INSERT STAPLE f
NEG GOING PULSE OR EDGE	CUT STAPLE f	INSERT STAPLE e

Normally set for pos polarity

External Sense Lines

POS LEVELS (+5v)

EF1H	CUT STAPLE c	INSERT STAPLE d
EF2H	CUT STAPLE a	INSERT STAPLE b

NEG LEVELS (0v)

EF1L	CUT STAPLE d	INSERT STAPLE c
EF2L	CUT STAPLE b	INSERT STAPLE a

Normally set for pos levels

External Pulses

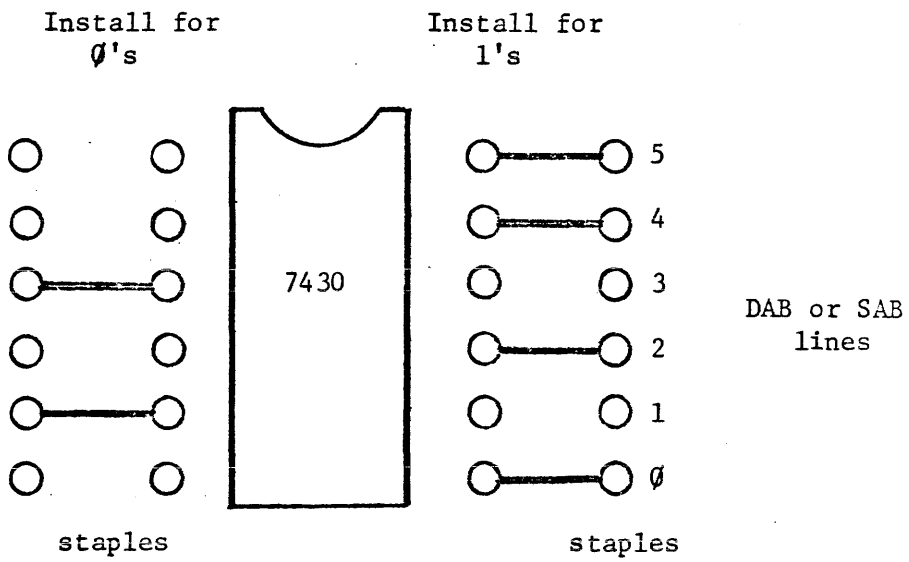
POS PULSES (+5v)

EP0H	CUT STAPLE j	INSERT STAPLE h
EP1H	CUT STAPLE l	INSERT STAPLE k
EP2H	CUT STAPLE n	INSERT STAPLE m
EP3H	CUT STAPLE r	INSERT STAPLE p

Example Address = 65_8

DAB/SAB 5 4 3 2 1 Ø

1 1 0 1 0 1



A1-destination address (DAB)
L1-source address (SAB)

VARIABLE ADDRESS SELECTION

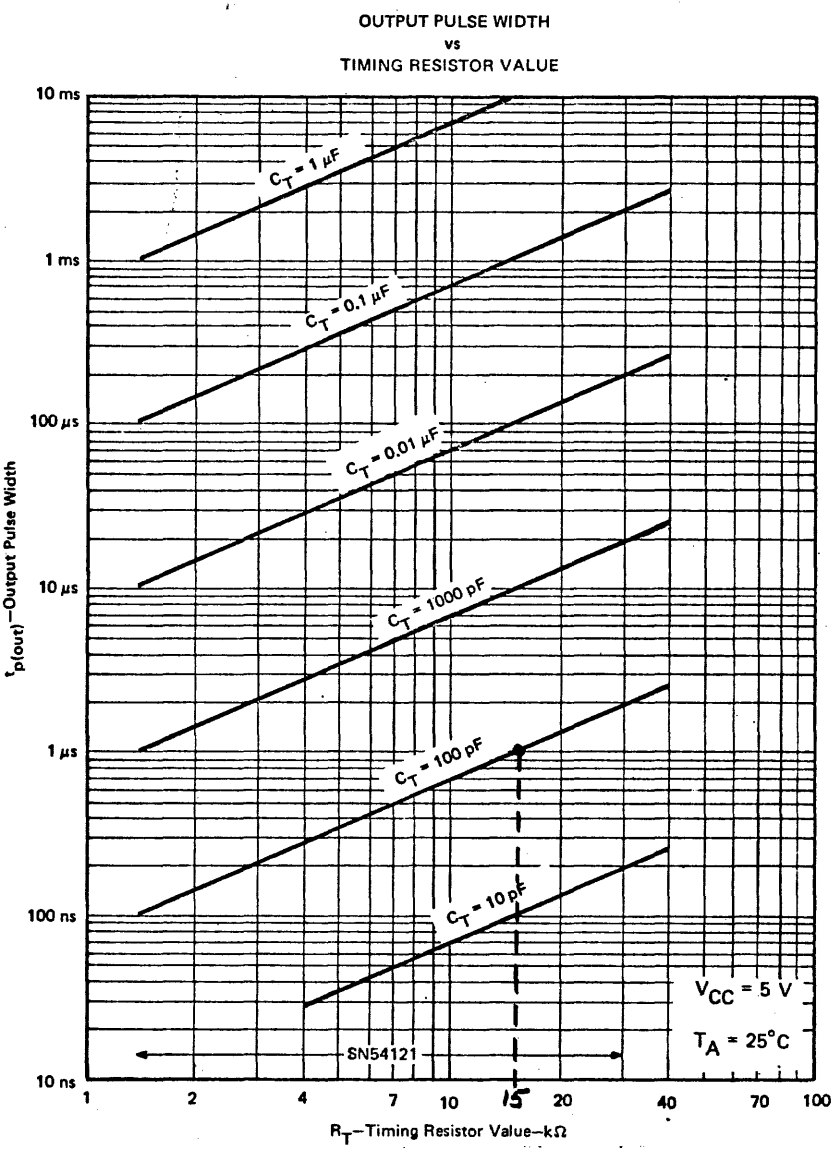

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE
10 ms
1 ms
100 µs
10 µs
1 µs
100 ns
10 ns
$t_{p(out)}$—Output Pulse Width
C_T = 1 µF
C_T = 0.1 µF
C_T = 0.01 µF
C_T = 1000 pF
C_T = 100 pF
C_T = 10 pF
V_{CC} = 5 V
T_A = 25°C
SN54121
1
2
4
7
10
15
20
40
70
100
R_T—Timing Resistor Value—kΩ

TABLE B-2

NEG PULSES (0v)

EP0L	CUT STAPLE h	INSERT STAPLE j
EP1L	CUT STAPLE k	INSERT STAPLE 1
EP2L	CUT STAPLE m	INSERT STAPLE n
EP3L	CUT STAPLE p	INSERT STAPLE r

Normally set for pos pulses

External Flag Clamp*

+12v swings from $R_S \geq$ 1K - Z9 = GRC-3 diode (1N914)

Open collector drive - Z9 = pull-up resistor

Pull down - Z20 $\geq$ 220 ohms (optional)

External Sense Line Clamps*

EF1 +12v swings from $R_S \geq$ 1K - Z17 = GRC-3 Diode (1N914)

Open collector drive Z17 = pull-up resistor

EF2 +12v swings from $R_S \geq$ 1K Z18 = GRC-3 Diode (1N914)

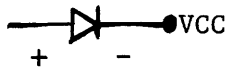
Open collector drive Z18 = pull-up resistor

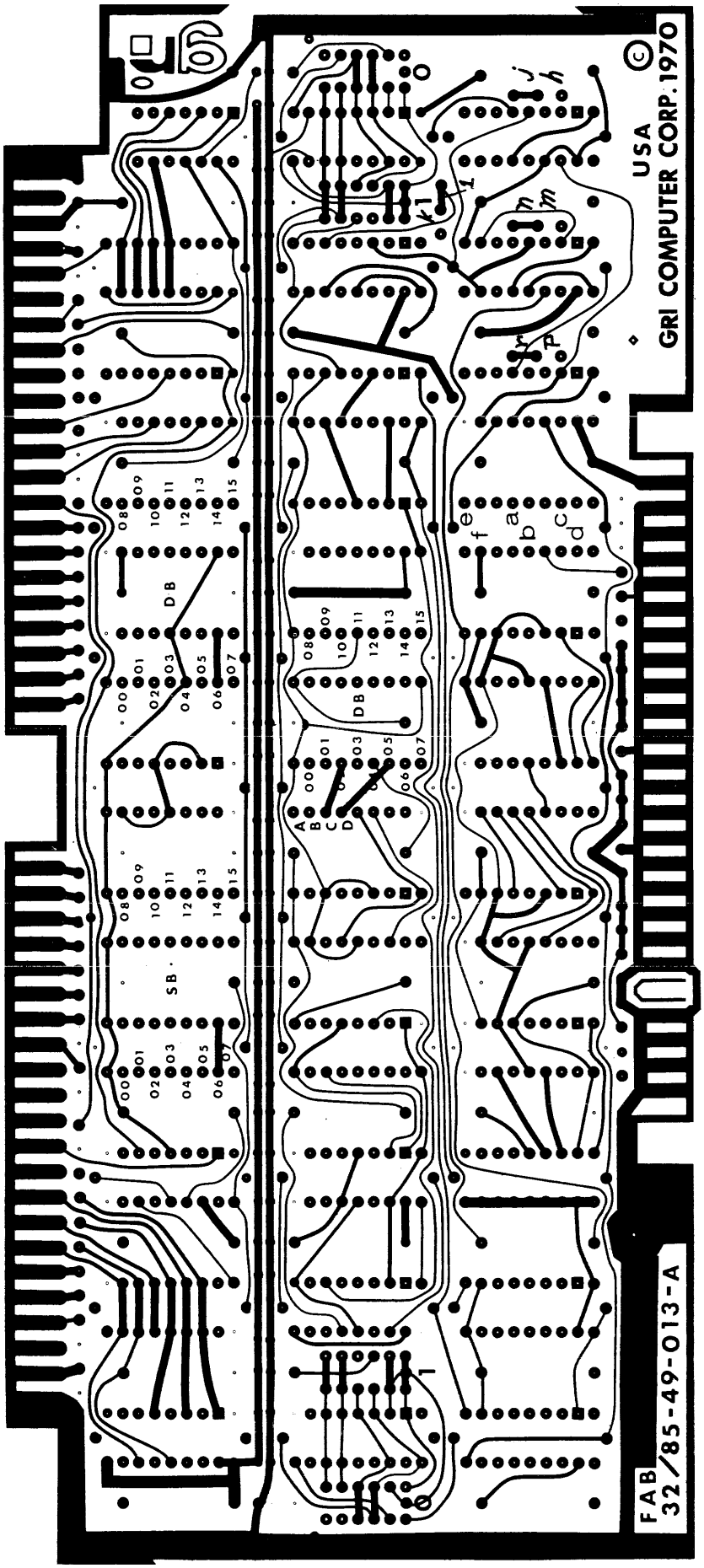
Data Line Clamps*

+12 swings from $R_S \geq$ 1K Z1-Z16 inclusive = GRC3 diodes

Open collector drive Z1-Z16 inclusive = pull-up resistors

*Observe polarity marks if diodes are used

+5v clamps 

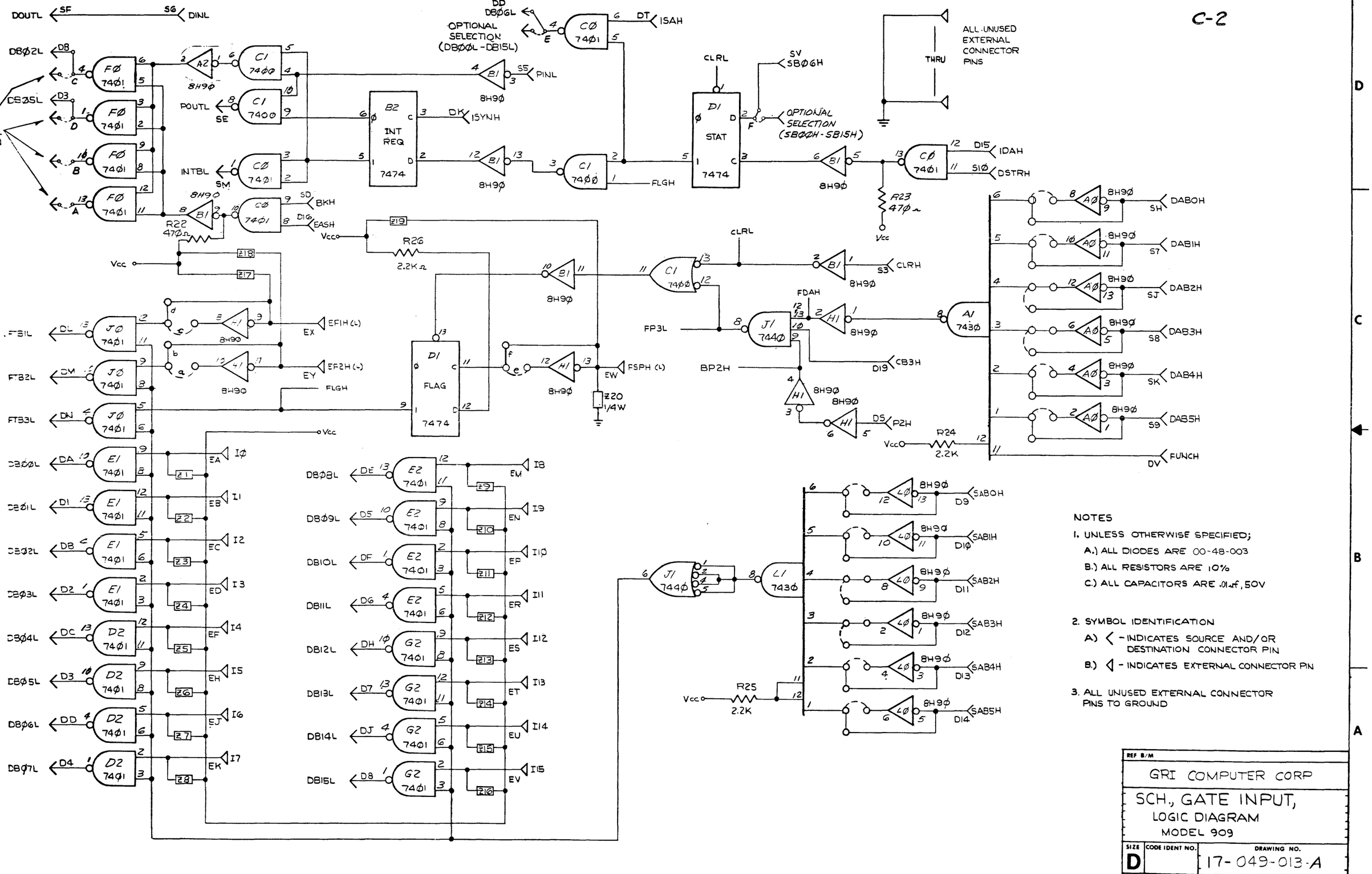


Selectable Jumpers

Standard Setting Shown

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED

C-2



NOTES

1. UNLESS OTHERWISE SPECIFIED;
   - A.) ALL DIODES ARE 00-48-003
   - B.) ALL RESISTORS ARE 10%
   - C.) ALL CAPACITORS ARE .01μf, 50V
2. SYMBOL IDENTIFICATION
   - A) < - INDICATES SOURCE AND/OR DESTINATION CONNECTOR PIN
   - B.) ◁ - INDICATES EXTERNAL CONNECTOR PIN
3. ALL UNUSED EXTERNAL CONNECTOR PINS TO GROUND

REF B/M

GRI COMPUTER CORP

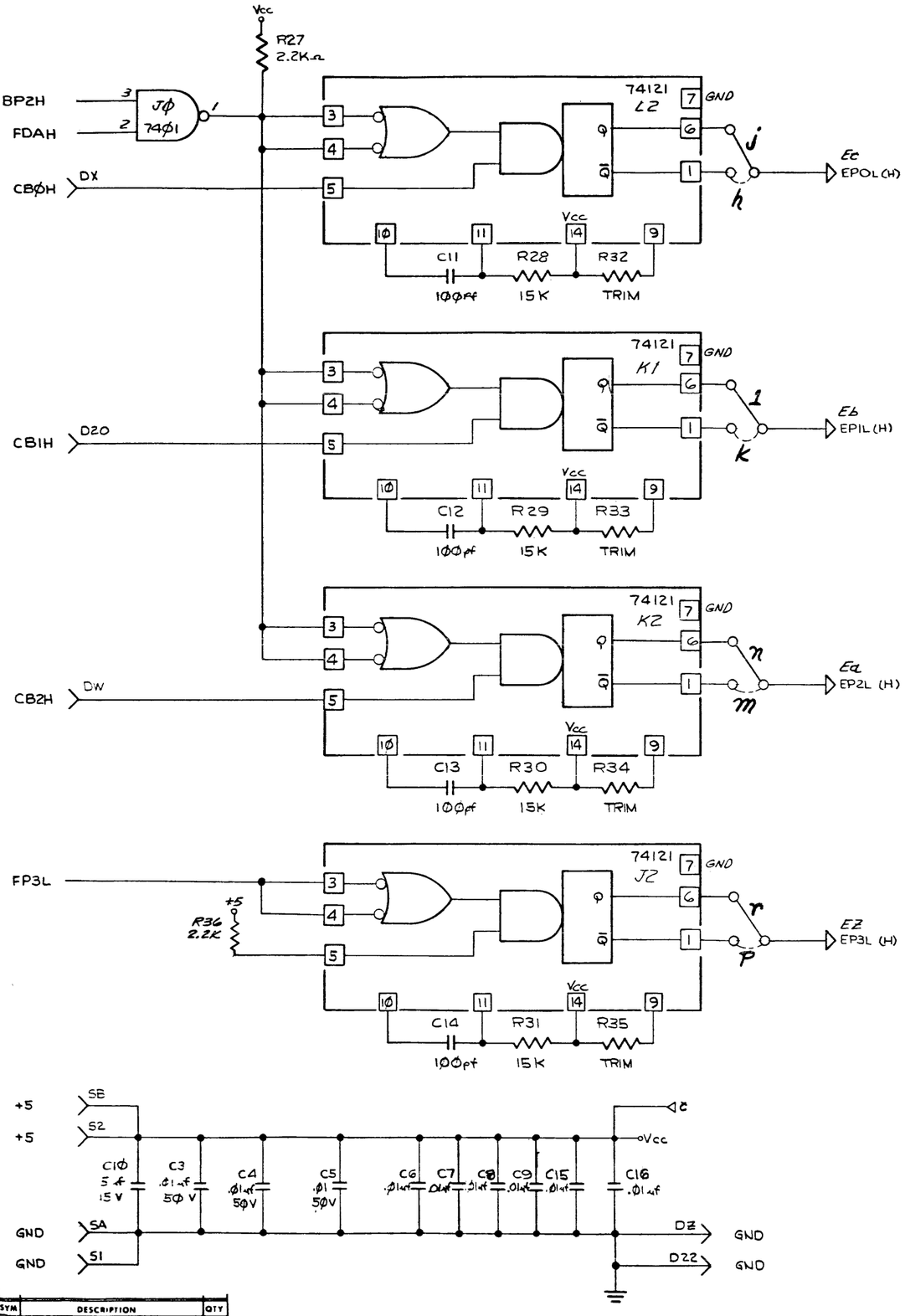
SCH., GATE INPUT, LOGIC DIAGRAM MODEL 909

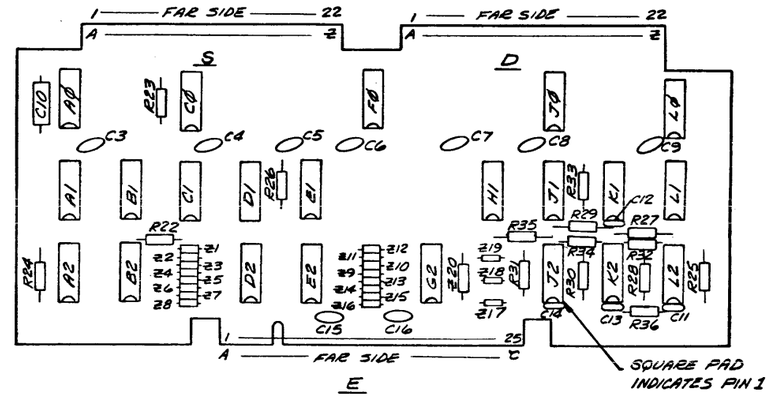
SIZE	CODE IDENT NO.	DRAWING NO.
D		17-049-013-A

SCALE NONE

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
—	-	SEE SHT ONE FOR REVISIONS	—	——

C-3





SYM	DESCRIPTION	QTY
	HOLE LEGEND	

REF B/M

GRI COMPUTER CORP

SCH., GATE INPUT, LOGIC DIAGRAM

MODEL 909

SIZE	CODE IDENT NO.	DRAWING NO.
D		17-049-013-A
SCALE NONE	UNIT WT	SHEET 2 OF 2

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