DOCUMENT CHANGE NOTICE C

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Document Affected	3000AF21-T Small System Digital Outputs	3010, 3010/2
Section Affected	Digital I/O in Theory Manuals	
Publications No.	3000AF21-T	
Reason:	Error in Vendor's Documentation	

Changes:

On page 1, second paragraph under "Functional Description", exchange the references to "one" bits and "zero" bits. A "zero" bit in the data byte transferred sets the corresponding flip-flop which turns on the relay driver, providing a ground return on the associated control line. A "one" bit in the data byte transferred resets the corresponding flip-flop.

On page 6, in the last paragraph in the right-hand column, change "CL000 through CL070" to read "CL001 through CL071", and exchange the references to "one" and "zero" data bits.

On page 8, in Fig. 4, change the reference to the transistor to read, " '1' data bit = OFF".

SMALL SYSTEM DIGITAL OUTPUTS

TABLE OF CONTENTS

SMALL SYSTEM DIGITAL OUTPUTS

INTRODUCTION

The Small System Digital Outputs hardware provides a means by which the system program can control the operation of process indicators, relays, solenoids, stepping motors, etc. Up to 16 output points may be controlled using the Small System Digital Output hardware. These outputs may take the form of latching contacts, momentary contacts, or pulse-train.

The status of the 16 output points is controlled by two 8-bit data bytes stored in memory. The data bytes are transferred to the digital outputs system by two Write Data (WD) Instructions. A single Output Command instruction initializes the digital output control circuits. The first Write Data instruction following an Output Command transfers the most significant eight bits to control eight digital outputs. The lower eight bits are transferred by a second Write Data instruction to the remaining eight digital outputs. Subsequent Write Data instructions are presumed to transfer alternate upper and lower bytes. A "one" bit in the data byte transferred energizes the corresponding output relay and closes its contact pair or enables an output pulse train. A "zero" bit de-energizes the relay and opens its contact pair or disables the output pulse-train.

Functional Description

Fig. 1 illustrates the Small System Digital outputs hardware in block diagram form. This figure illustrates the basic signal flow and lists the model numbers of the functional modules that make up the subsystem. All Small System Digital Outputs hardware modules are normally located within the Central System Cabinet (CSC).

The 4DP3000AF2102 Control Line Module consists of a standard 9.75 inch by 10.5 inch mother board. The board may be installed in any available slot on the Computer's Multiplexer Bus. The Control Line Module is normally assigned address X'71', however, this address may be changed by jumper wiring on the mother board. The Control Line Module provides 16 output lines for application to the 4DP3010AF24xx Buffer Relays in the 4DP3010AF3302 Digital Termination Assembly. Each of the 16 output lines is controlled by an individual flip-flop and relay driver circuit in the Control Line Module. The status of the flip-flops and relay drivers are controlled by 8-bit data bytes transferred from core memory by two Write Data Instructions. A "one" bit in the data byte transferred sets the corresponding flip-flop which turns on the relay driver, providing a ground on the associated control line. In the on condition, the relay driver is capable of returning up to +200 milliamps to the common return. A "zero" bit in the data byte transferred resets the corresponding flip-flop which turns off the relay driver providing an open on the associated control line. In the off condition, the relay driver is capable of withstanding up to +30V with respect to the common return. In this manner, the state of the control line will be maintained until changed by the program.

The 3010AF3302 Digital Termination Assembly permits connections to the process via screw-type terminals and provides card slots for Buffer Relay boards that adapt the Control Line Module outputs to the process. The output can be a latching circuit, momentary pulsing circuit, or timed pulse-train by plugging in the desired Buffered Relay boards (4DP3010AF24xx). Each Buffer Relay board contains 8 digital output circuits. The basic Digital Termination Assembly permits 16 circuit terminations. This assembly will support add-on terminations which can be expanded in 16 circuit increments up to a maximum of 80 circuits using the 4DP3010AF3304 Output Adder Assemblies. Each 16 circuit termination, however, requires a corresponding Control Line Module.

Examples of the types of Buffer Relay Boards are listed below:

Model Number	Description
3010AF2401	Buffer relays (contact outputs - 8 pt, 100VA Hg wetted). These circuits are shown on GE drawing PX3600IHSK1.
3010AF2402	Buffer relays (contact output) light duty (8 pt, 10 watts). These circuits are shown on GE drawing PX3600IHSL1.
Special	Buffer relays (contact output) 8 pt, 100VA latching or momentary.
Special	Solid State Switch Output, 8 pt, (ext. source 5-50 VDC, 250ma max).
Special	AC Output Switch, 8 pt, 120 VAC, "TRIACS".

These Buffer Relays are powered by a 4DP3010AL3501 (1 amp.) or 4DP3010AL3801 (5 amp.) 12 VDC Power Supply.

References

In addition to the Theory of Operation described in this publication, the following documents are provided to support the Small System Digital Outputs hardware:

- Functional Schematics

  Output Control Module - 70D102007 (Previously 70B113243 or FS21)

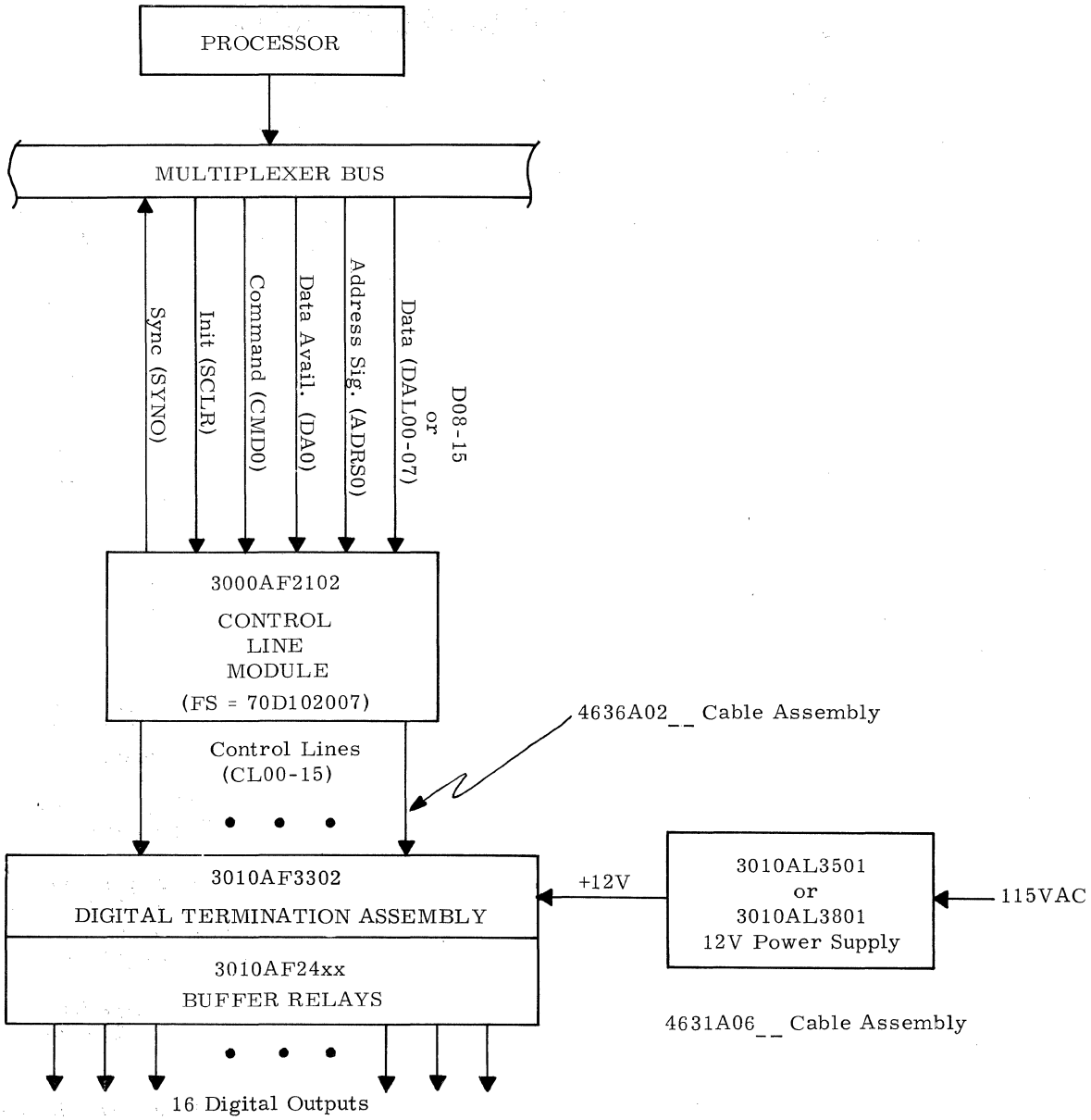

Fig. 1 Small System Digital Outputs

3010AF2401, 100VA Hg wetted Buffer Relay Board - PX3600IHSK1

3010AF2402, Light Duty (10 watts) Buffer Relay Board - PX3600IHSL1

- Maintenance

  3000AF21-M Publication located in the Digital I/O section of the GE-PAC* 3010 Computer Maintenance Manual.

- Hardware Location, Address, and System Connections

  System Configuration Drawing - Unique for each system (Referenced on the System Model List - 4DP0005ASID)

- Reference Manuals

  GE-PAC 30/3010

  Reference Manual - GET-6047

  Systems Interface Manual - PCP-126

  GE-PAC 3010/2

  Central Processor Reference Manual - GET-6174

- Illustrated Parts

  Illustrated Parts section of the GE-PAC 3010 Computer Maintenance Manual. (Control Line Module mother board assembly is

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32-048204. Parts for the Buffer Relay printed wiring boards are provided on the schematic for the board.)

- 12 Volt Power Supply

  Refer to the System Power Section of the GE-PAC 3010 Computer Maintenance Manual.

- Wire Lists

  Digital Output Termination Assembly - 70A121687

  Cable, Control Line Module to Termination assembly (4636A02xxx) - 70A122003P2

  Cable, Power (4631A01xxx) - 70A121175

> NOTE
>
> The last three digits (xxx) of cable model numbers correspond to the cable length in feet.

- Test Program

  Control Line Module Test - 70A112466

Options

ADDRESS

The address for the Small System Digital Outputs hardware is normally wired for X'71'. This address may be selected for any address from X'00' to X'FF' by changing the position of wire jumpers on the Control Line Module. The only restriction is that the address selected must not duplicate the address of any other I/O Controller on the Multiplexer Bus.

The logic elements which select and decode the address are shown on sheet 1 of the Control Line Module functional schematic. The address is selected by means of wire wrap jumpers at locations 02 and 03 on the Control Line Module mother board. Table 1 shows the function of each jumper pin and lists examples of the actual connections for several different addresses including the normal address, X'71'.

D. B. LOC	PIN NUMBER	LEVEL	HEXA-DECIMAL WEIGHT	SIGNAL MNE-MONIC*	EXAMPLES OF DEVICE ADDRESSING		
					X'4C'	X'2B'	X'71'
02	61 — 71	1	8	DAL00	61 TO 51	61 TO 51	61 TO 51
	51	0					
	31 — 41	1	4	DAL01	31 TO 41	31 TO 21	31 TO 41
	21	0					
	60 — 70	1	2	DAL02	60 TO 50	60 TO 70	60 TO 70
	50	0					
	30 — 40	1	1	DAL03	30 TO 20	30 TO 20	30 TO 40
	20	0					
03	61 — 71	1	8	DAL04	61 TO 71	61 TO 71	61 TO 51
	51	0					
	31 — 41	1	4	DAL05	31 TO 41	31 TO 21	31 TO 21
	21	0					
	60 — 70	1	2	DAL06	60 TO 50	60 TO 70	60 TO 50
	50	0					
	30 — 40	1	1	DAL07	30 TO 20	30 TO 20	30 TO 40
	20	0					

*In 3010/2 systems these signals correspond to D080 through D150 on the Mux Bus.

Table 1 Address Selection

The address of the module, as shipped from the factory, is listed in the System Configuration drawing supplied with each system.

TERMINATION BOARDS

As previously described in the Functional Description, various types of Buffer Relay boards may be inserted in the Digital Termination Assembly. Each board contains 8 output digital output circuits. Therefore, two boards may be selected for each Control Line Module. The actual boards implemented and their location in a system are shown on the System Configuration drawing. This drawing also specifies the screw termination designation for each digital output signal to the process.

BASIC OPERATION

In normal operation of the Small System Digital Outputs hardware, a 16-bit memory location is used to store the image (1 for enabled or closed, 0 for disabled or open) of the 16 digital output control signals. An Output Command (OCR) instruction is executed to reset the digital output control logic and clear the 16 storage register flip-flops associated with the 16 digital outputs. Two Write Data (WD) instructions are then executed to transfer the two 8-bit bytes of memory to the 16 storage registers, thereby, controlling the status of the 16 digital outputs. There are no interrupts associated with the digital output operation.

The following program illustrates a typical instruction sequence:

OCR, R1, R4	Reset Control logic (R4 may contain anything)
WD, R1, LOC	Transfer first 8 bit image byte
WD, R1, LOC+1	Transfer second 8 bit image byte

R1 contains the Control Line Module address.

The detailed operation of the digital output hardware during the execution of each of these commands is described in the following paragraphs. Most of this discussion is written for use with the functional schematic for the Control Line Module. A dictionary of the mnemonics used in this functional schematic is provided in Table 2. Understanding the meaning of these mnemonics will be of assistance in understanding the operation of the digital outputs hardware.

MNEMONIC	MEANING	FUNCTIONAL SCHEMATIC LOCATION
ADDL	Output from the Set Side of the Address Register	1N8 (coordinates) / 1P8 (sheet)
ADRS0	Address Signal from Processor	1P8
AG001 through AG071	High Inputs to Address NAND Gate	1H1 through 1H8
ASYN1A	Address Synchronization	1P2
CL000 through CL150	Control Lines to External Equipment	3C9 through 3P9
CMD0	Command Pulse from Processor	2A5
DA0	Data Available Pulse from Processor	2A4
DAL000 through DAL070 (D080 thru D150 on 3010/2)	Data Available Lines	1A1 through 1A8
DG1	Data Gate for First Eight Bits in Sixteen-Bit Register	1P6
DG2	Data Gate for Last Eight Bits in Sixteen-Bit Register	1P5
SCLR0	Initialize Pulse from Processor	2A7
SCLR0A	System Clear for First Eight Bits in Sixteen-Bit Register	2P7
SCLR0B	System Clear for Last Eight Bits in Sixteen-Bit Register	2L8

Table 2 Control Line Module Mnemonic Dictionary

Multiplexer Bus Interface

As previously described, the Small System Digital Outputs hardware communicates with the processor via the Multiplexer Bus. The Control Line Module printed wiring board may be inserted into any available card slot in the Multiplexer Bus. The Digital Outputs hardware responds to the Multiplexer Bus control signals generated as the result of the execution of Output Command (OC) instructions, Write Data (WD) instructions, or the Initialize function.

The Multiplexer Bus interface lines used by the Digital Outputs hardware are:

Function	Mnemonic	Direction (Processor → Control Line Module)
Data Lines	*DAL00:07	→
Address Signal	ADRS	→
Data Available Pulse	DA	→
Command Pulse (OUT)	CMD	→
Initialize	SCLR	→
Synchronize	SYN	←

*In 3010/2 systems these signals are labeled D080:150.

The data lines carry the status of both the address and the data bits used to control the digital output signals. The Address Signal is enabled when the Data Lines contain address information. The Data Available Pulse is enabled when the Data Lines contain information to control the status of the digital outputs. The Command Pulse is enabled during the execution of the Output Command instruction. The Initialize signal is enabled when the INITialize pushbutton is pressed. The Synchronize signal is generated within the Control Line Module in response to an ADRS, DA, or CMD control signal from the processor.

These signals are connected to the Control Line Module mother board by the Field 0 connector. These signals are at 0 volts (±.5V) for true at the input of the Control Line Module. Pin numbers associated with these connections are shown on sheet 4 of the Control Line Module functional schematic.

Out Command (OC) Instruction

The Out Command instruction is executed by the processor to reset the digital output control logic and to clear the storage register associated with the 16 digital outputs. In this manner, the Out Command initializes the Control Line Module prior to receipt of the two Write Data Instructions.

Fig. 2 illustrates the basic timing associated with the Out Command instruction. This timing diagram specifies the sheet numbers and coordinates of the functional schematic for the Control Line Module where the logic associated with the signals is illustrated.

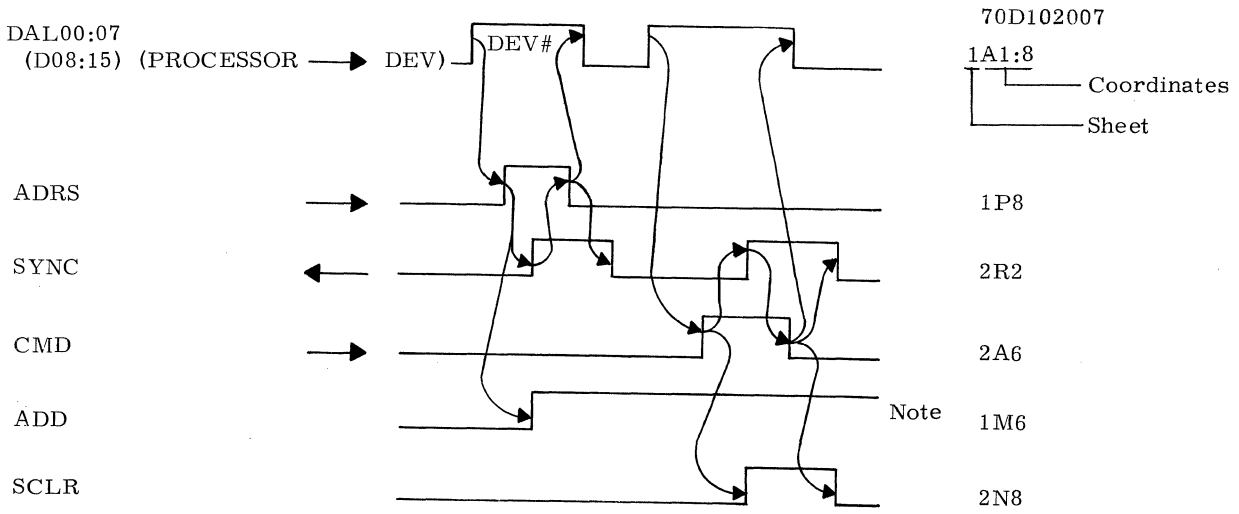
When the processor applies the correct address of the Control Line Module on the Data Available Lines (DAL00 thru DAL07 or D08 thru D15 in 3010/2 systems), all high inputs are applied to the Address NAND gate as shown on sheet 1, coordinates K2 (1K2) of the functional schematic. The low output (DVADD0) from this gate is inverted producing a high pulse (ASYN0S) to one input of the NAND gate at 1N3.

The ADRS pulse is applied from the processor to the other input of the NAND gate at 1N3, during the time ASYN0A is enabled. This NAND gate is then enabled and the resulting low output (ASYN0) DC sets the Address flip-flop at 1M6 and enables the Synchronizing signal (SYN0) back to the processor. The Synchronizing signal remains enabled until the ADRS signal is disabled by the processor. The Address flip-flop at 1M6 remains in the set state generating the ADD1 signal until a different module is addressed (i.e., until ADRS0A at 1M5 is enabled) or the Initialize function from the processor is enabled (SCLR1).

Next, as a result of the Out Command Instruction execution, the CMD signal from the processor is enabled. This signal, in conjunction with the ADD1 signal generated by the address, enables the two NAND gates at 2F6. The outputs from these two NAND gates perform the following functions:

1. Enables the synchronization signal (SYN0) back to the processor.
2. Enables the SCLR0A signal at 2R7 which DC clears the lower 8 Holding Register flip-flops on sheet 3. Resetting these flip-flops disables the CL000 thru CL070 Control Lines.
3. Enables the SCLR0B signal at 2K8 which DC clears the upper 8 Holding Register flip-flops on sheet 3 associated with the CL080 thru CL150 Control Lines.
4. Clears the DG1, DG2 Control flip-flop at 2H5. Clearing this flip-flop ensures that during the next WD instruction, the 8 bit data byte received will be steered to the Holding Register flip-flops associated with Control Lines CL000 thru CL070.

The processor then removes the CMD signal, disabling the signals described above to complete execution of the OC command.



NOTE 1. ADD is disabled by next ADRS when a different device number address is preset or by Initialize.

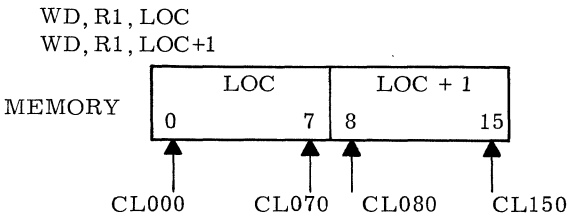
2. Signals not to time scale.

Fig. 2 Out Command Instruction Timing

Write Data (WD) Instruction

Write Data instructions are executed to transfer the image of the digital outputs from a 16-bit memory location. Write Data instructions, when executed, transfer the memory image to a Holding Register in the Control Line Module which will maintain the status of the digital outputs until updated by a subsequent WD or cleared by an OC instruction. Each WD instruction executed transfers one 8-bit byte of data. Therefore, two WD instructions must be executed to transfer the memory image for the 16 digital output signals.

Executing two WD instructions, following an OC instruction, Initialize, or following prior execution of WD instructions executed in pairs, controls the digital outputs as shown below:



Digital Output Control Lines
(a "one" enables the digital output, a "zero" disables the output)

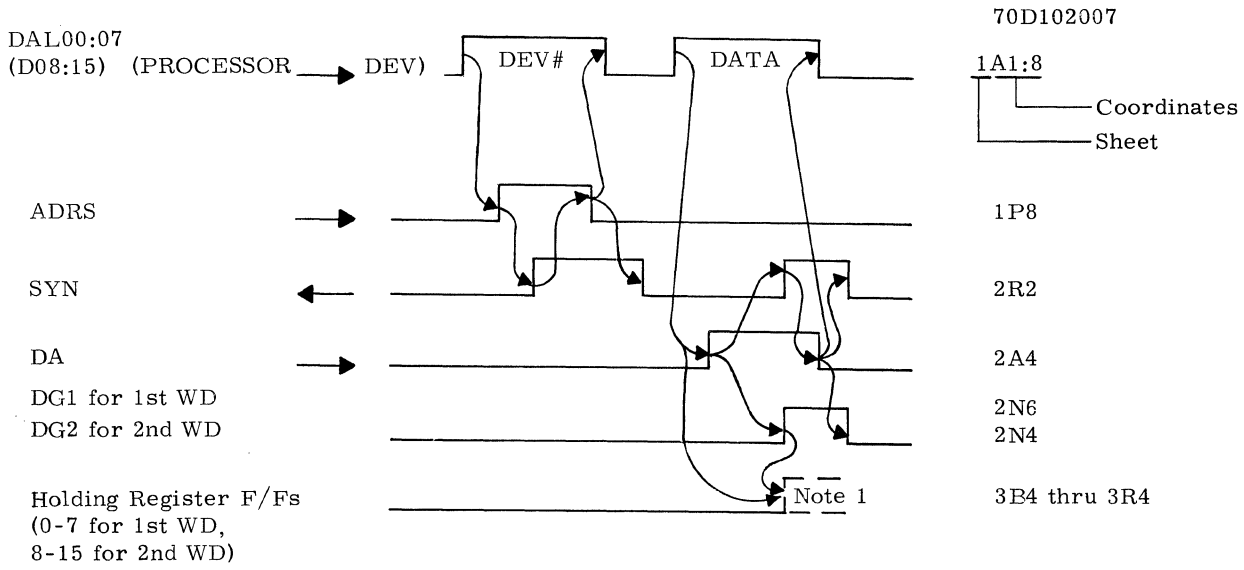
Fig. 3 illustrates the basic timing associated with the WD Instruction execution.

Executing the WD instruction applies the address on the Data Available Lines and an ADRS pulse which sets the Address flip-flop at 1M6 and enables the Synchronizing signal (SYN0) back to the processor, in the same manner described for the OC instruction. The Synchronizing signal remains enabled until the ADRS pulse is removed. Setting the Address flip-flop at 1M6 generates the ADD1 signal.

After the address has been applied to the Control Line Module, the WD instruction applies an 8 bit byte of control data on the Data Available Lines (DAL00, 07) along with a Data Available pulse (DA).

The DA pulse from the Processor is inverted and applied to one input of the NAND gate on 2F4. Since ADD1 is at the other input, the gate is enabled. The resultant low output is buffered and generates the SYN0 signal back to the Processor. The low output is also inverted generating a high pulse which is applied to the T input of the flip-flop on 2H5 and to one input of the NAND gate on 2K6. The trailing edge of the pulse toggles the flip-flop. Assuming the flip-flop was reset by a previous OC instruction, the flip-flop is set by the toggle. However, since the flip-flop was reset when the DA pulse is enabled, the NAND gate is enabled generating the DG1 pulse.

The byte of control data, on the Data Available Lines (DAL000 through DAL070) is applied to the input of the first eight bits of the sixteen-bit Holding Register, shown on sheet 3. DG1 toggles the T input to the eight flip-flops and the byte of data is transferred to the Output Control Lines, CL000 through CL070, via a resistor-transistor network. A "one" data bit turns the transistor on providing a ground on the associated Output Control Line. A "zero" data bit



NOTE 1. A "1" data bit sets the corresponding flip-flop. A "0" data bit resets the corresponding flip-flop.

2. Not to time scale.

Fig. 3 Write Data Instruction Timing

turns the transistor off providing an open on the associated Output Control Line.

The Control Lines are connected via a cable to the Buffer Relay boards in the Digital Termination Assembly. A Control Line, when enabled, will energize the corresponding output buffer relay or enable the output pulse train. The process is connected to the Buffer Relay contacts via screw-type terminals. Fig. 4 illustrates the operation of the Holding Register, output transistor, and Buffer Relay circuit.

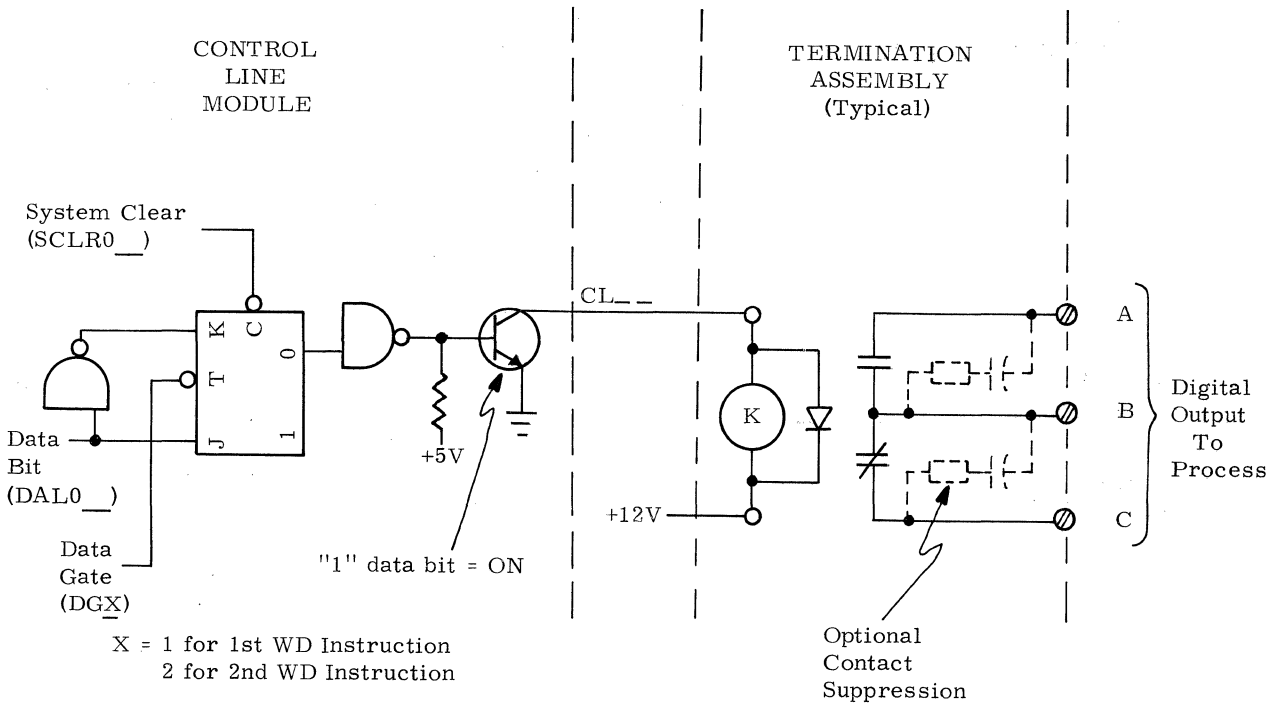
When the DA pulse is removed by the processor, the Synchronizing and DG1 signals are disabled to end the WD operation. The Holding Register flip-flops and Control Lines will remain in the state specified by the control data bits.

A second WD instruction addressed to the Control Line Module will operate in the same manner as the first WD instruction described above, except that the DG1/DG2 control flip-flop on 2H5 will be set during execution and toggled to clear. Since the flip-flop is set, the NAND gate at 2K5 will be enabled. The resultant output produces a DG2 pulse. This DG2 pulse toggles the T inputs of the second eight flip-flops in the Holding Register. The byte of control data is transferred via a resistor transistor network to Control Lines CL080 through CL150. In this manner, the second WD instruction executed controls the digital output contacts associated with Control Lines CL080 through CL150.

If another WD instruction was executed, the 8-bit data byte would again control the CL000 through CL070 lines. In this manner, the above cycle can be repeated by executing two WD instructions in succession.

Initialize

Pressing the INITialize switch on the console applies a SCLR0 pulse to the Control Line Module. This SCLR0 pulse resets the 16 bit Holding Register, the Address flip-flop, and the DG1/DG2 Control flip-flop (2H5). The SCLR0 pulse is applied to the input of the inverter on 2C7. The resulting pulse (SCLR1) resets the Address flip-flop on 1M6. SCLR1 is inverted to produce SCLR0A and SCLR0B. SCLR0A clears the DG1/DG2 Control flip-flop on 2H5 and the first eight flip-flops in the sixteen-bit Holding Register. SCLR0B clears the second eight flip-flops in the sixteen-bit Holding Register.



One Of 16

Fig. 4 Digital Output Circuit