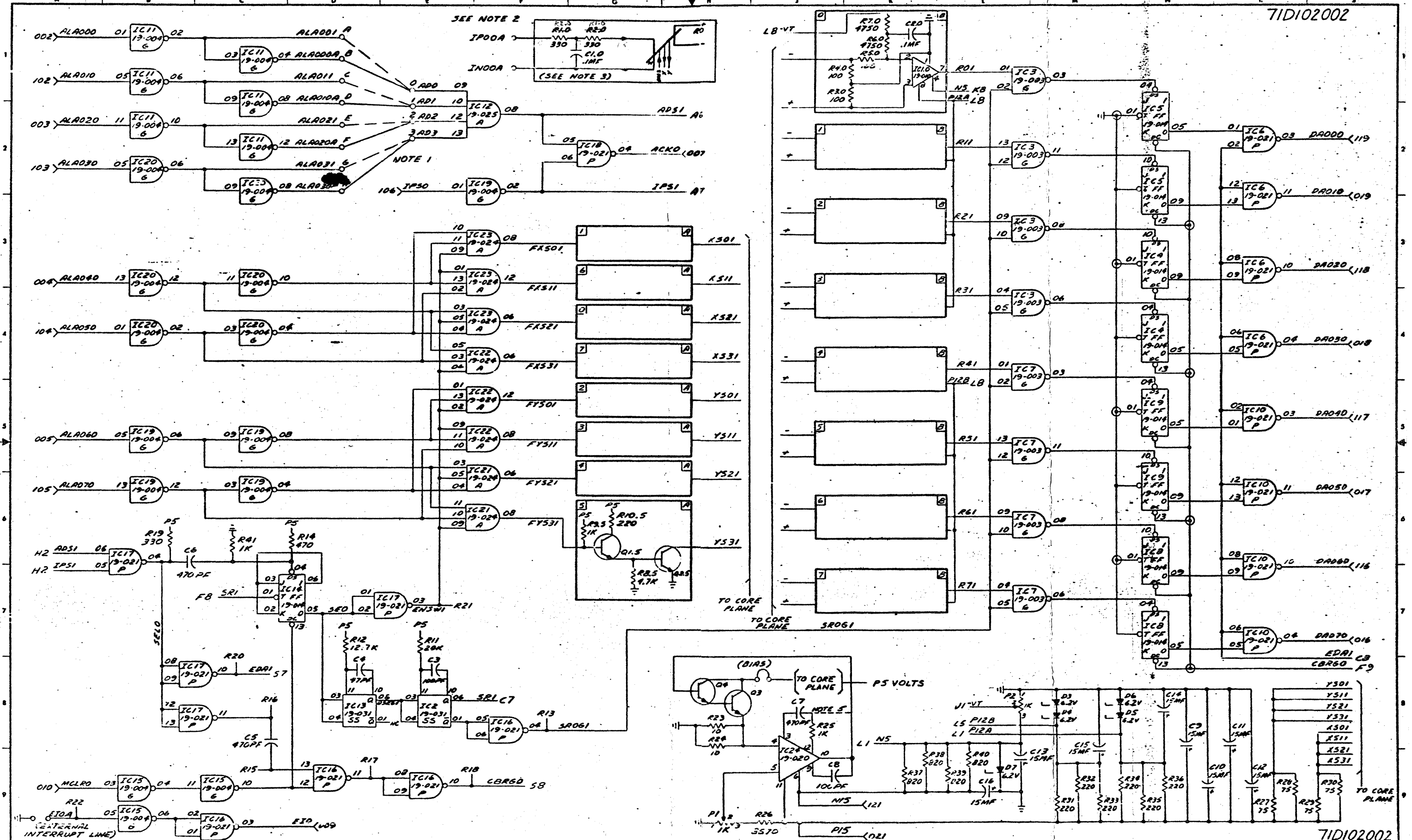


SYSTEM BDR FOR SUN STUDS, INC.

DRAWING NUMBER	DRAWING DESCRIPTION	REVISION DWG PL	TAB NAME
71D 102 002	DIG IN MODULE LOGIC		PROCESS DIGITAL I/O



NOTES

1. NORMALLY STRAPPED FOR ADDRESS 0.
2. USER'S INPUTS (1 OF 128) SEE SHEET 2.
3. LINE FILTER 1 OF 128 R10 TO R127, R20 TO R2127, C10 TO C1127.
4. SEE SHEET 2 FOR REVISION INFORMATION
5. IF IC24 IS 19-037 OPAMP C8, R25 ARE NOT EQUIPPED, C7 IS 22 PF AND IS WIRED BETWEEN PINS 03 & 10 ON IC24.

ISSUED 7-26-70

DESIGNED BY D. BARKER, R. E. SAGER, D. M. YOUNG, R. E. JONES

CHECKED BY D. BARKER, R. E. SAGER, D. M. YOUNG, R. E. JONES

DATE 7-26-70

TIME 10:00

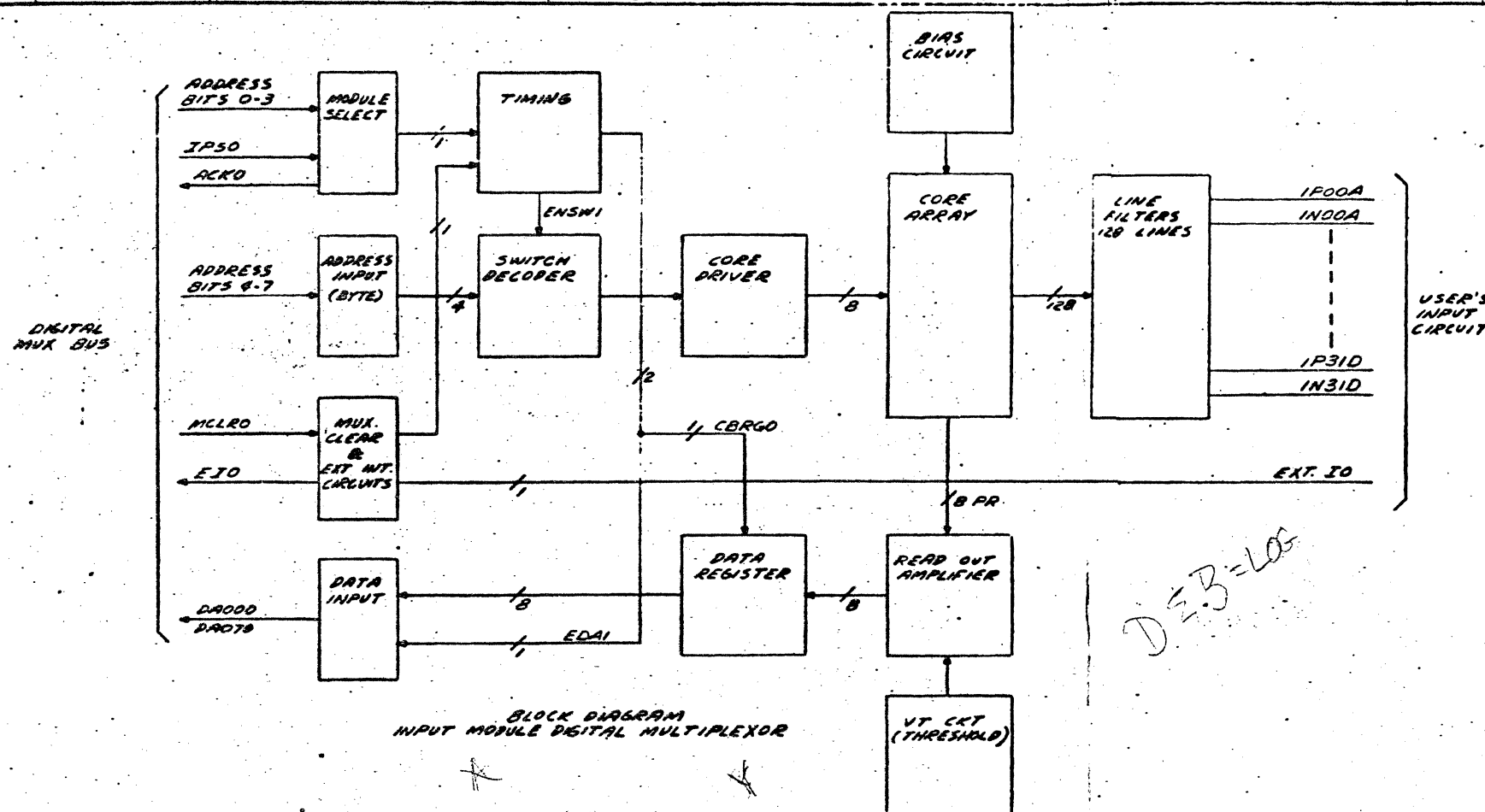
PROJECT 03061

REVISION 02-159400000

71D102002

71D102002

ADDED SH. 3
 R1 R3 918 1-4-71 R0
 ADDED NOTE 5 TO SH
 1. ADDED NOTE 2 TO
 SH. 3. SH. 2 CHANGED
 IC PIN 12-16 L. C. 12-
 M. 7. 1. 2. CHANGED 12-11-
 IC20 LOC C2 CHANGED
 DIODE DESIG. DS 106
 LOC M8
 R1 R3 996 1-4-71 R0
 CH. 1. AREA 12. 7K
 RESISTOR WAS 12.5K
 R1 R3 1124 1-4-71 R0



22	GND	P5
21	GND	P5
20	N15	P15
19	DA000	DA000
18	DA020	DA030
17	DA040	DA050
16	DA060	DA070
15	GND	GND
14		
13		
12		
11		
10		MCLR0
09		ETO
08		
07		ACK0
06		
05	ALA070	ALA060
04	ALA050	ALA040
03	ALA030	ALA020
02	ALA010	ALA000
01	GND	P5
00	GND	P5

BACK PANEL MAP

CONN. A			CONN. B			CONN. C			CONN. D		
P	N		P	N		P	N		P	N	
00	IP00A	IN00A	0	IP00B	IN00B	00	IP00C	IN00C	0	IP00D	IN00D
01	IP01A	IN01A	01	IP01B	IN01B	01	IP01C	IN01C	01	IP01D	IN01D
02	IP02A	IN02A	02	IP02B	IN02B	02	IP02C	IN02C	02	IP02D	IN02D
03	IP03A	IN03A	03	IP03B	IN03B	03	IP03C	IN03C	03	IP03D	IN03D
04	IP04A	IN04A	04	IP04B	IN04B	04	IP04C	IN04C	04	IP04D	IN04D
05	IP05A	IN05A	05	IP05B	IN05B	05	IP05C	IN05C	05	IP05D	IN05D
06	IP06A	IN06A	06	IP06B	IN06B	06	IP06C	IN06C	06	IP06D	IN06D
07	IP07A	IN07A	07	IP07B	IN07B	07	IP07C	IN07C	07	IP07D	IN07D
08	IP08A	IN08A	08	IP08B	IN08B	08	IP08C	IN08C	08	IP08D	IN08D
09	IP09A	IN09A	09	IP09B	IN09B	09	IP09C	IN09C	09	IP09D	IN09D
10	IP10A	IN10A	10	IP10B	IN10B	10	IP10C	IN10C	10	IP10D	IN10D
11	IP11A	IN11A	11	IP11B	IN11B	11	IP11C	IN11C	11	IP11D	IN11D
12	IP12A	IN12A	12	IP12B	IN12B	12	IP12C	IN12C	12	IP12D	IN12D
13	IP13A	IN13A	13	IP13B	IN13B	13	IP13C	IN13C	13	IP13D	IN13D
14	IP14A	IN14A	14	IP14B	IN14B	14	IP14C	IN14C	14	IP14D	IN14D
15	IP15A	IN15A	15	IP15B	IN15B	15	IP15C	IN15C	15	IP15D	IN15D
16	IP16A	IN16A	16	IP16B	IN16B	16	IP16C	IN16C	16	IP16D	IN16D
17	IP17A	IN17A	17	IP17B	IN17B	17	IP17C	IN17C	17	IP17D	IN17D
18	IP18A	IN18A	18	IP18B	IN18B	18	IP18C	IN18C	18	IP18D	IN18D
19	IP19A	IN19A	19	IP19B	IN19B	19	IP19C	IN19C	19	IP19D	IN19D
20	IP20A	IN20A	20	IP20B	IN20B	20	IP20C	IN20C	20	IP20D	IN20D
21	IP21A	IN21A	21	IP21B	IN21B	21	IP21C	IN21C	21	IP21D	IN21D
22	IP22A	IN22A	22	IP22B	IN22B	22	IP22C	IN22C	22	IP22D	IN22D
23	IP23A	IN23A	23	IP23B	IN23B	23	IP23C	IN23C	23	IP23D	IN23D
24	IP24A	IN24A	24	IP24B	IN24B	24	IP24C	IN24C	24	IP24D	IN24D
25	IP25A	IN25A	25	IP25B	IN25B	25	IP25C	IN25C	25	IP25D	IN25D
26	IP26A	IN26A	26	IP26B	IN26B	26	IP26C	IN26C	26	IP26D	IN26D
27	IP27A	IN27A	27	IP27B	IN27B	27	IP27C	IN27C	27	IP27D	IN27D
28	IP28A	IN28A	28	IP28B	IN28B	28	IP28C	IN28C	28	IP28D	IN28D
29	IP29A	IN29A	29	IP29B	IN29B	29	IP29C	IN29C	29	IP29D	IN29D
30	IP30A	IN30A	30	IP30B	IN30B	30	IP30C	IN30C	30	IP30D	IN30D
31	IP31A	IN31A	31	IP31B	IN31B	31	IP31C	IN31C	31	IP31D	IN31D

INPUT MODULE CONNECTORS

DIGITAL ADDRESS

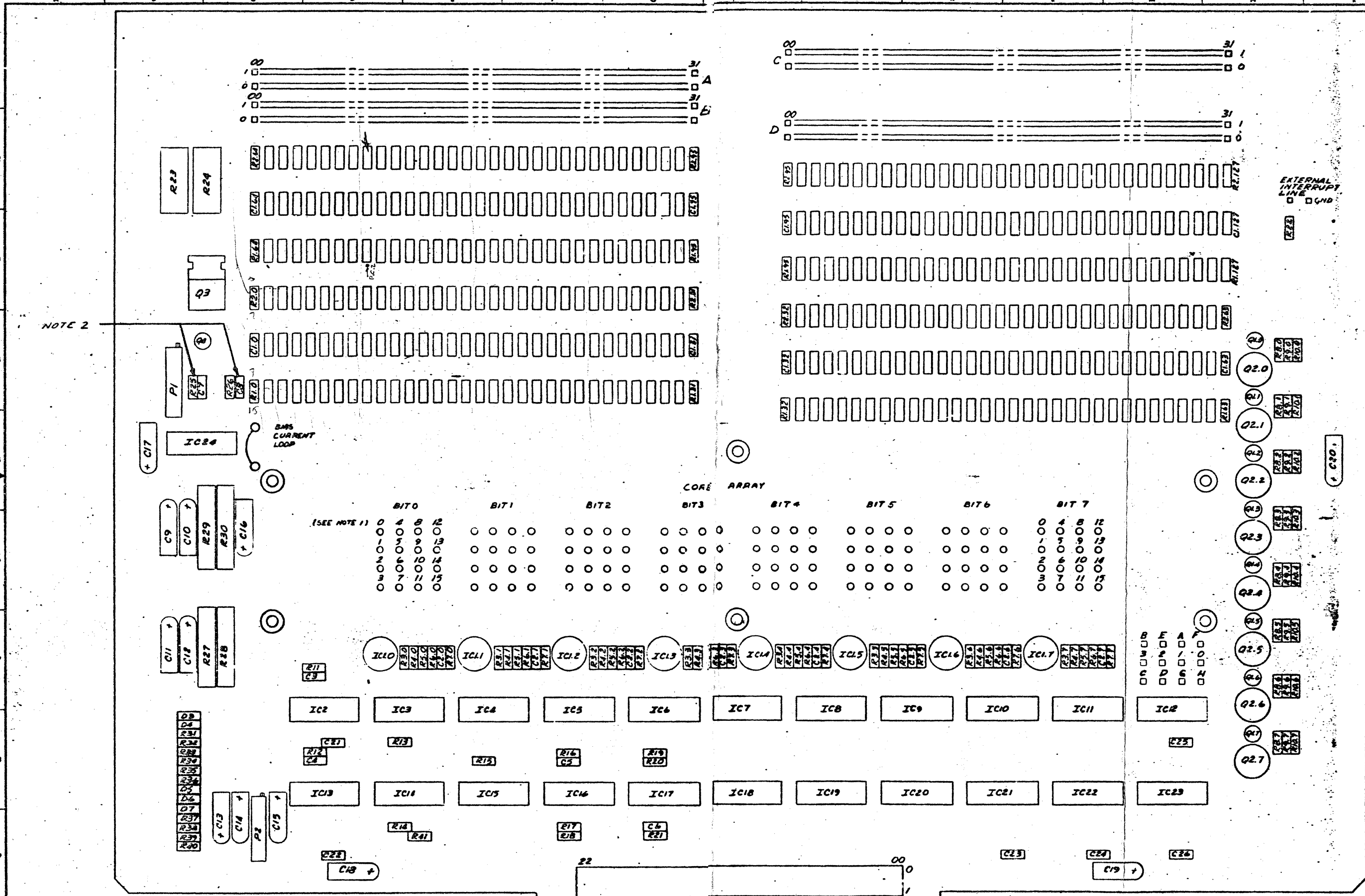
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0	0	1	0	2
0	0	1	1	3
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0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

71D102002

NOTES

NAME	DATE	DATE	TITLE FUNCTIONAL SCHEMATIC
DATE	DATE	DATE	DIGITAL MULTIPLEXOR
CHK	CHK	CHK	INPUT MODULE
ENG	ENG	ENG	
SYS TEST	SYS TEST	SYS TEST	03061
DR ENG	DR ENG	DR ENG	02-15913008 2-3





NOTE 2

(SEE NOTE 1)

NOTES
 1. 0 TO 15 DENOTES BYTE NUMBER.
 2. R25, AND C8 ARE NOT USED ON 35-20 R03 AND HIGHER REVISIONS

NAME	TITLE	DATE	TITLE
	DRAFT		COMPONENT LOCATOR
	CHK		DIGITAL MULTIPLEXOR
	ENGR		INPUT MODULE
	DR ENG		03061
			02-159 R03D08
			3-3