GENERAL ELECTRIC

70A111158

PRINT DIST. K7-20	CONTROL LINE MODULE INSTALLATION SPECIFICATION	CONT. ON 1 SH. NO. 0 (02-060120)

GENERAL NOTES

F.C.F.

FMF: GE-PAC 30

APPROVED BY: E A White DATE: Mar 16, 70

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
A1	ANI-038 REV SHTS 0, 1	J Linic 7-27-71			

REISSUED

A Dodie

A1 Jul 27, '71

Made By	Issue Date	PROCESS	Dwg. No.	Sh. No.
E. WHITE, MARCH 10, 1970	Mar 17, 1970	COMPUTER PHOENIX, ARIZ.	70A111158 Cont. on 1	0

PCE 20A 7-62

TITLE CONTROL LINE MODULE
INSTALLATION SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-060A20)

REVISIONS

A1

1. UNPACKING

When this module is shipped with a Processor, it is installed in the chassis so there is no special unpacking procedure. However, if the Control Line Module is shipped as an expansion unit, unpack it carefully and check for breakage and damage to components.

2. PHYSICAL CHARACTERISTICS

This module consists of a standard 9-3/4 inch by 10-1/2 inch mother-board and associated cable.

3. LOCATION

The mother-board connects into any I/O slot in the Processor or expansion chassis.

4. SAFEGUARDS

To prevent damage to personnel or equipment, make sure that the AC power is off while installing this equipment.

5. CABLES

Standard 17-069F04 cables are provided in locations 40, 41, 42, and 43 of the mother-board. The cables are stranded 28 gauge twisted pair wire. Table 1 shows the cable layout for this module.

6. DEVICE ADDRESSING

The device address for this module is X'71'. This address may be changed by changing the position of the straps in positions 02 and 03 of the mother-board. See Figure 1 for possible changes.

7. INSTALLATION CHECK

To determine if the Control Line Module has been installed correctly and is functioning properly, run the test program 70A112467

PRINTS TO

TABLE 1 CABLE CONNECTIONS

Lead Designations	Terminals
CL150	11-42
CL140	10-42
CL130	70-43
CL120	60-43
CL110	50-43
CL100	40-43
CL090	30-43
CL080	20-43
CL070	10-43
CL060	71-43
CL050	61-43
CL040	51-43
CL030	41-43
CL020	31-43
CL010	21-43
CL000	11-43

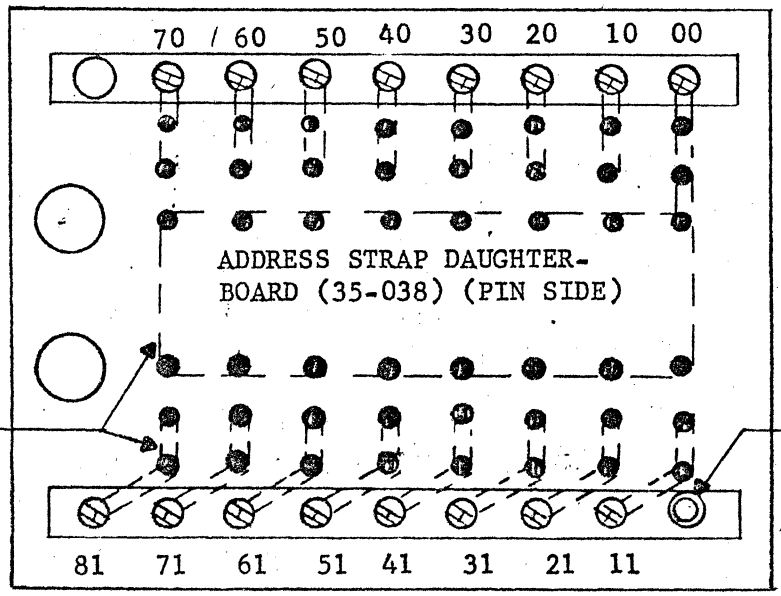
TITLE CONTROL LINE MODULE
INSTALLATION SPECIFICATION

FIRST MADE FOR GE-PAC 30 (02-060A20)

REVISIONS

Figure 1 Strap Daughter Board Device Addressing

D.B. LOC	PIN NUMBER	LEVEL	HEXADECIMAL WEIGHT	EXAMPLES OF DEVICE ADDRESSING X'4C'	X'2B'
02	61 — — — — — — — 71 — — — — — — — — 51	1 0	8	61 TO 51	61 TO 51
	31 — — — — — — — 41 — — — — — — — — 21	1 0	4	31 TO 41	31 TO 21
	60 — — — — — — — 70 — — — — — — — — 50	1 0	2	60 TO 50	60 TO 70
	30 — — — — — — — 40 — — — — — — — — 20	1 0	1	30 TO 20	30 TO 20
03	61 — — — — — — — 71 — — — — — — — — 51	1 0	8	61 TO 71	61 TO 71
	31 — — — — — — — 41 — — — — — — — — 21	1 0	4	31 TO 41	31 TO 21
	60 — — — — — — — 70 — — — — — — — — 50	1 0	2	60 TO 50	60 TO 70
	30 — — — — — — — 40 — — — — — — — — 20	1 0	1	30 TO 20	30 TO 20



PRINTS TO

GENERAL ELECTRIC

70A111245

PRINT DIST. K7-21

CONTROL LINE MODULE
MAINTENANCE SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-060A21)

GENERAL NOTES

F.C.F.
FMF: GE-PAC 30

APPROVED BY: E. G. White DATE: Mar 16, 70

REVISION STATUS

V.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				

REISSUED

Made By
E. WHITE, MARCH 10, 1970

Issue Date
Mar. 17, 1970

PROCESS
COMPUTER
PHOENIX, ARIZ.

Dwg. No. 70A111245
Cont. on 1 Sh. No. 0

1. INTRODUCTION

The Control Line Module, Part Number 02-069, transfers sixteen bits of data from the Processor to an external device under program control. The module has provisions for storing the information in a sixteen0bit register until it is updated. The register is cleared prior to inserting new data.

2. BLOCK DIAGRAM

The block diagram of the Control Line Module is shown on Drawing 70B113243. As shown in the block diagram, an Output Command is sent from the Processor to reset the sixteen-bit register. The Processor sends control data via Data Available Lines, DA1000 through DAL070, to the input of eight bits of the sixteen-bit register. Upon receiving a Write Instruction from the Processor, the data is transferred to Control Lines CL00 through CL070.

The Processor sends control data via Data Available Lines DAL000 through DAL070 to the second eight bits of the sixteen-bit register. When the second Write Instruction from the Processor arrives, this data is transferred to Control Lines CL080 through CL150.

3. FUNCTIONAL DIAGRAM ANALYSIS

The functional diagrams of the Control Line Module are on Drawing 70B113243.

3.1 Addressing Input

When the Processor sends the correct address of the module via Data Available Lines DAL000 through DAL070, the output is strapped in such a way as to present all highs at the inputs to the Address NAND gate on 70B113243-1K2. The low output from this gate is inverted to produce a high pulse, ASYN0A, which is applied to one input of the NAND gate on 1N3.

The Processor sends an ADRS0 pulse to the input to the inverter on 1P8 at the same time it sends the correct address to the module. This ADRS0 pulse is inverted and ADRS1 is applied at the other input of the NAND gate on 1N3. The gate is enabled and the resulting low sets the Address flip-flop on 1M6 to produce ADD1.

3.2 Control Data

The Processor sends two consecutive DA0 pulses to the module. The first DA0 from the Processor is inverted and applied at one input to the NAND gate on 2F4. Since ADD1 is at the other input, the gate is enabled. The resultant low output is buffered and sends SYN0 to the Processor. The low output is also inverted and the high pulse is sent to the T input to the flip-flop on 2H5 and to one input of the NAND gate on 2K6. The lagging edge of the pulse sets the flip-

flop. However, since the 0-side output from the flip-flop is high when the pulse is high, the NAND gate is enabled. The resultant low output is inverted to produce a DG1 pulse.

The Processor presents a byte of control data, via Data Available Lines DAL000A through DAL070A, to the input of the first eight bits of the sixteen-bit register. DG1 toggles the T input to the eight flip-flops and the byte of data is transferred to the output Control Lines, CL000 through CL070, via a resistor-transistor network. The data to Control Lines CL000 through CL070 is available to external equipment on cable connectors.

The second DA0 pulse from the Processor is inverted and applied at one input to the NAND gate on 2F4. Since ADD1 is on the other input, the gate is enabled. The resulting low output is buffered and sends SYN0 to the Processor. The low output from the NAND gate is inverted and a high pulse is applied at the T-input to the flip-flop on 2H5 and to one input of the NAND gate on 2K4. The lagging edge of the pulse resets the flip-flop. However, since the pulse is high at the same time as the 1-side output from the flip-flop is high, the NAND gate of 2K4 is enabled. The resultant low is inverted to produce a DG2 pulse.

The Processor presents a byte of data to the second eight inputs of the sixteen-bit register. DG2 toggles the T-inputs of the second eight flip-flops in the register. The byte of control data is transferred via a resistor transistor network to Control Lines CL080 through CL150. The data on the control lines is available to external equipment on cable connectors. Active (low) signals on the DA1000A through DAL070A lines produce a ground on the associated control line.

3.3 Initialization

When the INITIALIZE pushbutton on the Processor is depressed, a SCLR0 pulse is applied to the input of the inverter on 2C7. This pulse is inverted to produce SCLR1 which resets the Address flip-flop on 1M6. SCLR1 is inverted to produce SCLR0A and SCLR0B. SCLR0A clears the flip-flop on 2H6 and the first eight flip-flops in the sixteen-bit register. SCLR0B clears the second eight flip-flops in the sixteen-bit register.

4. MNEMONICS LIST

This section contains the mnemonics, meanings, and locations on 70B113243 of the various signals that are used in the Control Line Module.

MNEMONIC	MEANING	LOCATION
ADDL	Output from the Set Side of the Address Register	1N8
ADRS0	Address Signal from Processor	1P8
AG001 through AG071	High Inputs to Address NAND Gate	1H1 through 1H8
ASYN1A	Address Synchronization	1P2
CL000 through CL150	Control Lines to External Equipment	3C9 through 3P9
CMD0	Command Pulse from Processor	2A5
DA0	Data Available Pulse from Processor	2A4
DAL000 through DAL070	Data Available Lines	1A1 through 1A8
DG1	Data Gate for First Eight Bits in Sixteen-Bit Register	1P6
DG2	Data Gate for Last Eight Bits in Sixteen-Bit Register	1P5
SCLR0	Initialize Pulse from Processor	2A7
SCLR0A	System Clear for First Eight Bits in Sixteen-Bit Register	2P7
SCLR0B	System Clear for Last Eight Bits in Sixteen-Bit Register	2L8

GENERAL ELECTRIC

70A110448

PRINT DIST.: K7-15

PROGRAMMING SPECIFICATION
CONTROL LINE/RELAY CLOSURE

CONT. ON 1 SH. NO. 0

GENERAL NOTES

F.C.F.
FMF:

APPROVED BY: Lucy A. Miller DATE: 12-10-71

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	Issue				

REISSUED

A	Issued										

Made By: J. Lima/LAP

Issue Date: DEC 16 1971

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A110448
Cont. on 1 Sh. No. 0

TITLE PROGRAMMING SPECIFICATION
CONTROL LINE/RELAY CLOSURE

FIRST MADE FOR GE-PAC 30

REVISIONS

1. INTRODUCTION

These modules are interfaces designed to transfer two bytes of control information from a GE-PAC 30 processor to a user's external equipment (Control Line) or to sixteen reed relays (Relay Closure). The significance of the 16 bits of data is entirely dependent upon the user's equipment.

Device number 'X'71' is normally assigned to the Control Line module; X'08' is normally assigned to the Relay Closure module.

2. STATUS AND COMMAND BYTES

No status byte exists for either device. Any Output Command (actual bit configuration does not matter) resets the steering on either device so that the next Write instruction will affect the upper 8 bits.

3. INITIALIZATION

Depressing INITIALIZE on the processor will reset the Write steering and clear all sixteen control lines.

4. PROGRAMMING CONSIDERATIONS

The 16 control bits are transferred to either device by two Write Data instructions. The first Write transfers the upper 8 bits; the second transfers the lower 8 bits. The steering is reset following the second Write. The control bits remain available to the external equipment until updated by another pair of writes.

For the Relay Closure module, a one-bit in the data closes the contacts; a zero-bit opens them.

For the Control Line module, a one-bit in the data produces a logical zero output level; a zero-bit produces a logical one output level.

K7-15

PRINTS TO

GENERAL ELECTRIC

70A1108A9

ENT DIST. KT-12

CONTROL LINE MODULE INFORMATION DWG (32-048A12) CONT. ON 1 SH NO. 0

GENERAL NOTES

F.C.F.

FMT: GE-PAC 30

APPROVED BY: C. A. Cole DATE: Oct 27, 69

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
A	ISSUE				
A1	ADD-ON REV SHTS 0, 1, 2	J. LIMA 7-27-71			

REISSUED

A	Issue										
A1	Jul 29, 71										

Made By E. WHITE

Issue Date Oct 29, 1969

PROCESS COMPUTER PHOENIX, ARIZ.

Dwg. No. 70A1108A9 Cont. on 1 Sh. No.

REVISIONS

A11

CONTROL LINE MODULE

1.0 General Description

This module provides a means of activating 16 external devices such as indicators, relays, solenoids, stepping motors, etc.

Each of the 16 control lines has its own storage register and buffer driver stage.

In the normal operation of this module, a 16-bit memory location is used to store the image of the 16 control lines. The images may be transferred to the control line module by executing two 'Write Data' instructions from the two bytes of the memory image.

The module contains logic control for automatically steering the two bytes of data to the 16 control lines.

A single 'Output Command' instruction will reset the control logic and reset all 16 control line registers.

2.0 Interface Specifications

The output lines each consist of a collector output from a common emitter connected transistor stage. In the 'ON' condition, the collector can sink up to +200ma to ground. In the 'OFF' condition, the collector can take up to +30 VDC.

When driving inductive loads, negative going transients should be removed by using a suppressor diode across the load.

3.0 Programming Considerations

Strap options provide for any Dev # selection from X'00' to X'FF'.

Two 'Write Data' instructions are used to transfer the two-byte memory image to the control line storage registers.

An 'Output Command' will reset the control logic and clear all 16 storage registers. The following will serve to demonstrate the typical instructions.

```
OCR, R1, R4        INITIALIZE I/O  (R4 may have anything in it)
WD, R1, LOC        TRANSFER FIRST    image byte.
WD, R1, LOC + 1    TRANSFER SECOND   image byte.
```

See 70A112467 for Test Program Information.

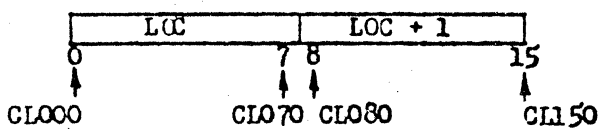
PRINTS TO

1.0 Mechanical Considerations

The control line module consists of one mother board which may be plugged into any I/O slot in the expansion card file. The control line outputs are accessible through Daughter board cable connectors, (35-038 DB's), at locations 42 & 43 on the mother board. The following table shows cable connections:

LEAD DESIG	TERMINAL
CL150	11-42
CL140	10-42
CL130	70-43
CL120	60-43
CL110	50-43
CL100	40-43
CL090	30-43
CL080	20-43
CL070	10-43
CL060	71-43
CL050	61-43
CL040	51-43
CL030	41-43
CL020	31-43
CL010	21-43
CL000	11-43

MEMORY LOC



A 'one' bit transferred to the control line module will cause the associated control line to be grounded.

GENERAL ELECTRIC

7CA110858

PH. & T DIST. K7-12

CONTROL LINE MODULE
PRODUCT SPECIFICATION

CONT. ON 1 SH. NO. 0
(02-060A19)

GENERAL NOTES

F.C.F.
FMT: GE-PAC 30

APPROVED BY: _____ DATE: _____

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
C	REV. SH 1, ADDED SH 0	[illegible]			
[illegible]	2, & 3 PER AN-6WL N- 44-017	2-4-70			
C1	AN6058 REVISIONS 0, 1, & 2				

REISSUED
C April 29 1970
C1 8-26-71

Made By W. Wong

Issue Date April 29 1970

PROCESS
COMPUTER
PHOENIX, ARIZ.

Dwg. No. 70A110858
Cont. on 1 Sh. No. 0

PCE 20A 7-62

1. DOCUMENTATION

Shipped with Product

1 each	70A111245	Maintenance Spec.
1 each	70A111158	Installation Spec.
1 each	70A112467	Test Program
1 each	70B113243	Logic Schematic

2. PARTS LIST

Part Number 70A104048G.74 (02-060) consists of the following:

1 each	32-084	Control Line Module (MB)
2 each	069F04	Cables

3. DIMENSIONS

Mother-Board:	9.75" x 10.5"
Cable Length:	12' (open end)

4. WEIGHT

3 pounds including cable

5. POWER

5.1 Interface Board: +5 volt $\pm$ 10% @ .75 amps

6. ENVIRONMENTAL DATA

6.1	Temperature:	0° to 50°C
6.2	Humidity:	Equals or exceeds Processor
6.3	Vibration:	Equals or exceeds Processor

7. DESCRIPTION

The 70A104048G.74 (02-060) Control Line Module provides sixteen control lines of 200 ma and 30V capability, each with its own storage register. The image of the control lines is stored in two consecutive bytes of memory.

7. DESCRIPTION (Cont'd)

The control line states are updated by executing two Write Data (WD) instructions from the two bytes of memory.

8. ACCEPTANCE TEST

The Interface board must successfully perform the designated test program (70A112467) in order to be considered operational. This program should run under prescribed environmental variations.

9.0 Application Information

9.1 General Description

In the normal operation of the Control Line Module, a sixteen-bit memory location is used to store the image of the sixteen control lines. The images may be transferred to the Control Line Module by executing two Write Data Instructions from the two bytes of the memory image. This module contains logic control for automatically steering the two bytes of data to the control lines. Each output line has its own storage register to maintain the state of the line until updating is desired. This module provides a means for operating medium power external devices such as indicators, relays, solenoids, and stepping motors under program control.

This module is useful whenever it is desired to control devices which require up to 200 milliamps to operate. The device will respond only to the WD (Write Data) Instruction. Interrupt circuitry is not provided on the module.

A ONE bit in the memory will be represented as an on transistor (ground) on the associated control line. A ZERO in memory will be represented by a non-conducting transistor.

9.2 Outputs

Each output line consists of an open collector output from a common emitter connected transistor stage as shown in Figure 1.

Output Specifications

Identical to 2N3646 transistor

Maximum OFF Voltage = (Sustain) 15 volts

Breakdown Voltage = 40 volts

The base drive to this circuit is approximately 10 milliamps which will support an 1_C of approximately 200 milliamps with V_{CE} of 0.5 volts.

When driving inductive loads, negative going transients should be removed by using a suppressor diode across the load. Cable length should be considered when suppression is necessary.

9.3 Connector Layout

Standard 17-069F04 (Twelve foot open-ended) cables are provided. For connector assignments, see the Installation Specification 70A111158.

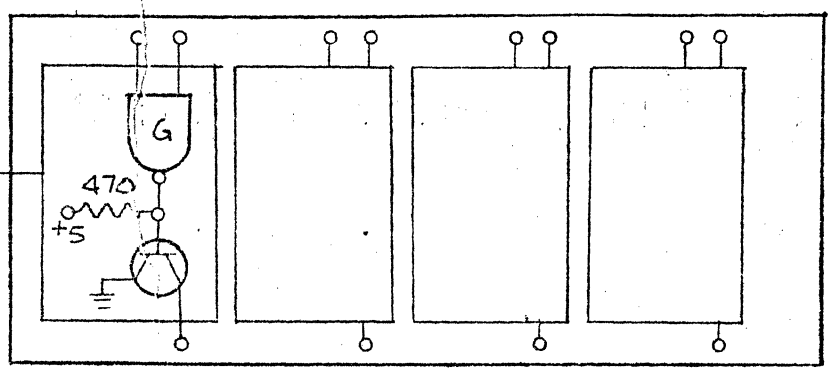


FIG. 1
OUTPUT CIRCUIT

U

PRINTS TO

GENERAL ELECTRIC

PROCESS COMPUTERS
PHOENIX ARIZONA

TITLE FUNCTIONAL SCHEMATIC
CONTROL LINE MODULE

DRAWING NUMBER 70B113243 | CONT 0A | PAGE 0

FIRST MADE FOR GE-PAC 30

(FS21)

REVISION STATUS

REV.	RECORD OF CHANGE	REV. DATE & NAME	REV.	RECORD OF CHANGE	REV. DATE & NAME
D	ISSUED				
E	REV. SH. 2 & 0A PER AN	Lasforasso			
[illegible]	6WDW-44-014	DEC 24, '69			
E1	REV. SH. 0A & 2 PER	J. J. Cowens			
[illegible]	AN 6WDW-44-019	APR. 20, 70			

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D	Issued
E	Jan 12, 1970
E1	May 14, 1970

REISSUED

(FS21)

MADE BY [illegible] 28 AUG 69

APPROVAL E. [illegible] Sept 9, 69

ISSUED September 11, 1969

REV. D

DWG. NO. 70B113243 | CONT 0A | PAGE 0

PRINTS TO: K7-08

PCS 2002

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE FUNCTIONAL SCHEMATIC	DWG NO (FS21)
APPLIED PRACTICES	SURFACES	TOLERANCES FRACTIONS	TOLERANCES DEC PLACES	TOLERANCES ANGLES	PROCESS COMPUTER PHOENIX	CONTROL LINE MODULE	70B13243
	V	±	±	±		FOR GE-PAC 30 SERIES	CONT ON SHEET 1 DRN NO 0A

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SHEET INDEX SUPPORTING INFORMATION	0A	1	2	3	4																
FUNCTIONAL SCHEMATIC	1	1	2	2	4																
	2	1	2	3	4																
	3	1	2	2	4																
EACK PANEL MAP	4	1	1	1	1																
BLOCK DIAGRAM	5	-	2	2	2																
	ISSUE DATE	12-16-67	11-15-68	7-7-69	11-27-70																

SUPPORTING INFORMATION

CATEGORY	PART NO.
MOTHER BOARD ASSEMBLY	52-0748804

SHEET INDEX NOTES:

1. CHANGES ON THIS DRAWING SHALL REQUIRE ONLY THE REISSUE OF SHEETS AFFECTED.
2. THE ISSUE OF THIS SHEET SHALL DETERMINE THE LATEST ISSUE OF THIS DRAWING.
3. IN THE EVENT THAT THE REVISION LEVEL STAMPED ON THE PWB DOES NOT CORRESPOND TO THAT IN THE SUPPORTING INFORMATION TABLE, PLEASE REQUEST SCHEMATIC OF THE CORRECT REVISION LEVEL FROM "GENERAL ELECTRIC COMPANY 40 FEDERAL ST. WEST LYNN, MASSACHUSETTS 01905".

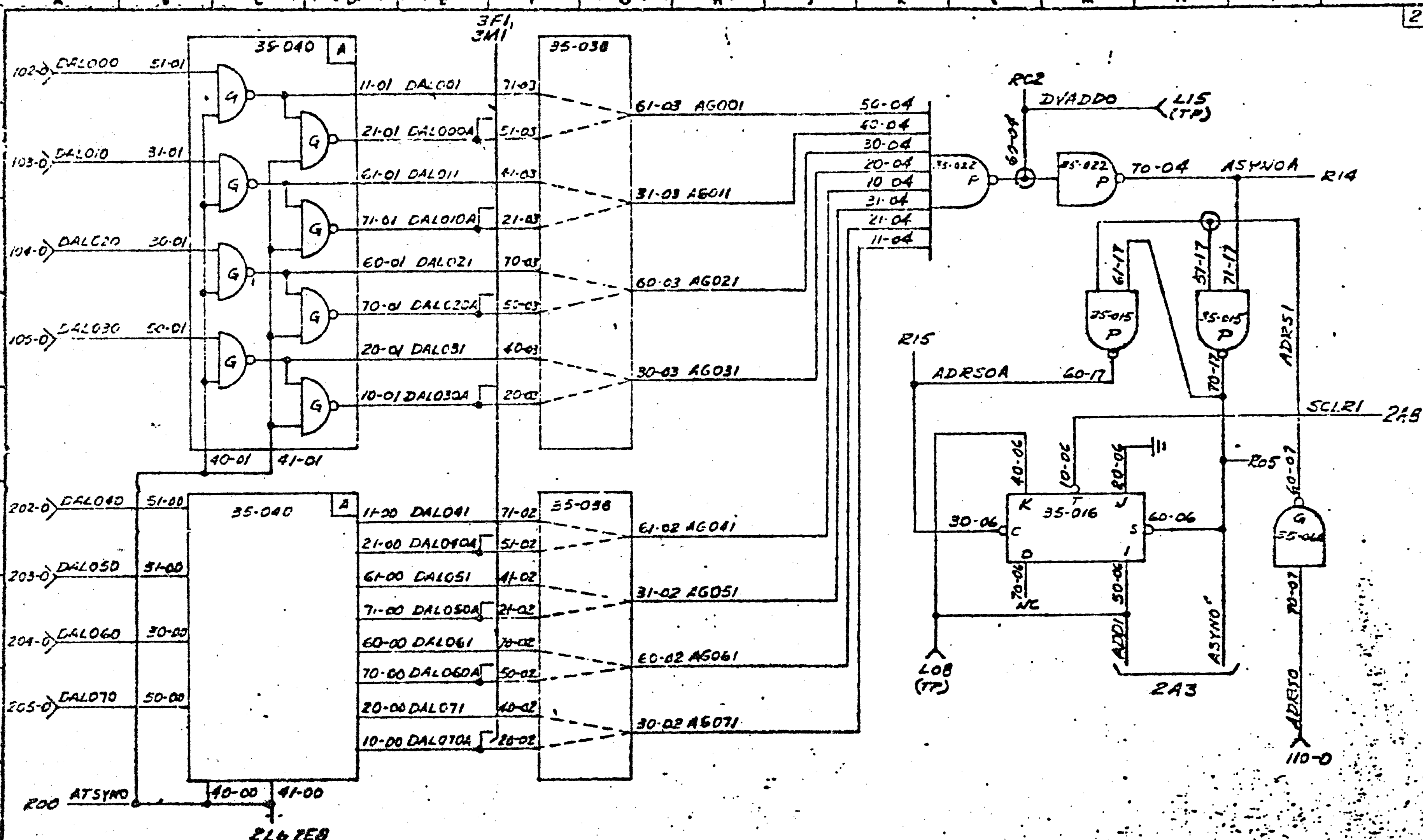
MADE BY	28 AUG 69	APPROVAL		ECO		REV	D		E1				DWG NO (FS21) 70B113243
ISSUED	Sept 11, 1969			CHNG			E						CONT ON SHEET 1 DRN NO 0A

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING				
APPLIED PRACTICES	SURFACES	TOLERANCES: FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC
CONTROL LINE MODULE
GE-PAC 30

DWG NO (FS21) 70B113243
CONT ON SHEET 2 SH NO 1



28 AUG 69
Sept 11, 1969

REV. D

DWG NO (FS21) 70B113243
CONT ON SHEET 2 SH NO 1

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING

APPLIED PRACTICES	SURFACES	FRACTIONS	DECIMALS	ANGLES
	√	±	±	±

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTIONAL SCHEMATIC COMPUTER PROJECT (FS21)
CONTROL LINE MODULE
70B113243
FMP GE-PAC 30 FCP
CONT ON SHEET 3 SH NO 2

2

R04
C04
470pf
R03

ASYNO
30-05
50-05
40-05
35-022 P
R13
60-05
35-022 P
70-05
SYNO
115-0

IN8

ADDI
51-15
71-15
35-015 P
70-15
111-0 DA0
50-07
35-060 G
40-07

71-07
35-060 G
21-07

51-13
61-13
35-015 P
60-13
R12
61-11
35-015 P
60-11
R22
DG2

J S 1
11-06 T
35-016
K C 0
51-06
71-06
L09 (TP)
L10 (TP)

210-0 CMAD0
30-07
35-060 G
20-07
61-15
35-015 P
60-15
11-37
20-37
35-020 P
21-37

71-13
35-015 P
70-13
R10
71-11
51-11
35-015 P
70-11
R21
DG1
3A5
L11 (TP)
31-06

117-0 SCLR0
31-07
35-060 G
21-07
70-37
35-020 P
71-37
10-37
R11
SCLR0A
ATSYNO
1A9

R16
IR5 SCLRI
60-37
35-020 P
61-37
SCLR0B
3J9

MADE BY
28 AUG 69
APPROVAL
DES
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Sept 11, 1969

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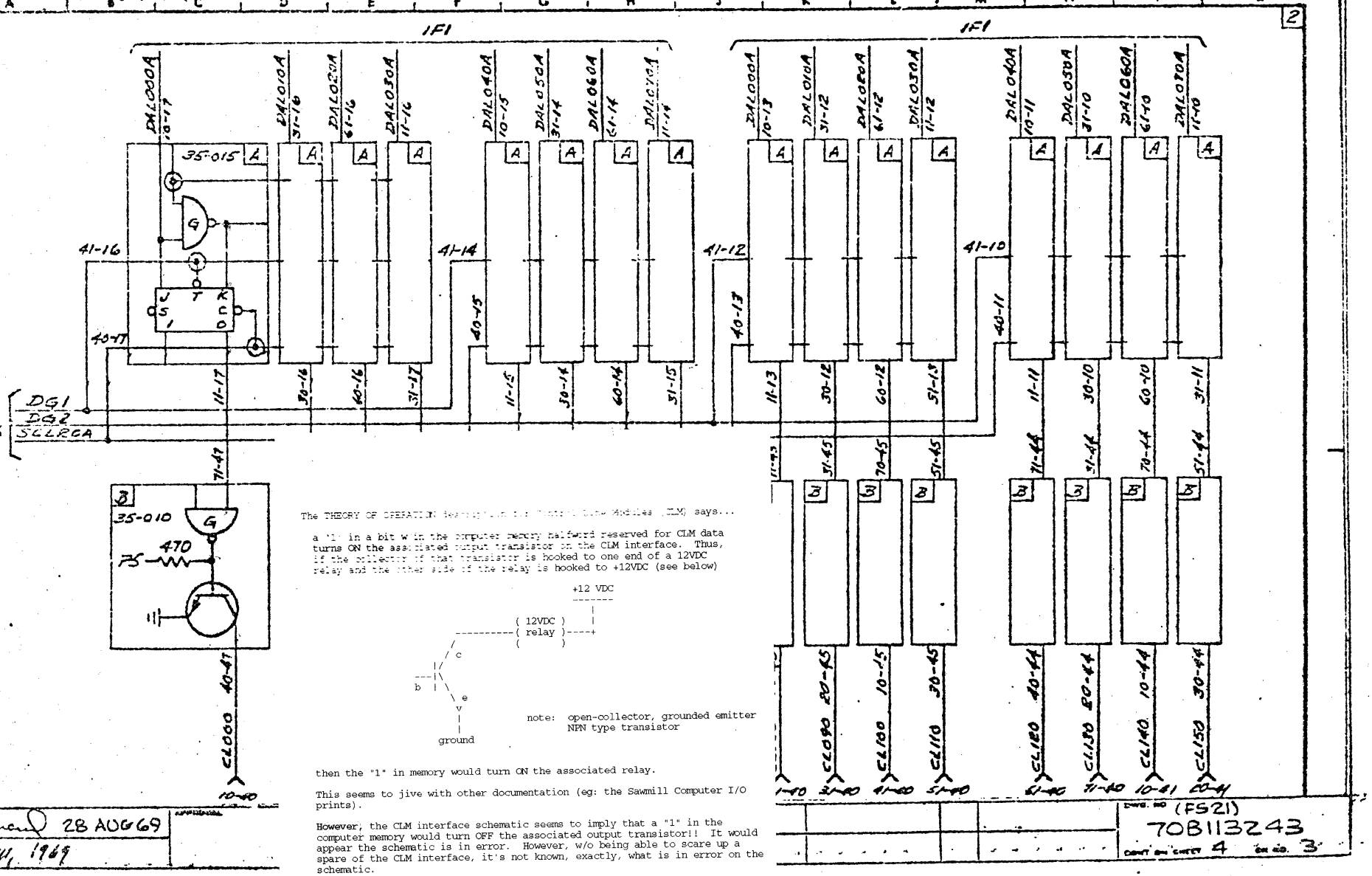
DWG NO (FS21)
70B113243
CONT ON SHEET 3 SH NO 2

GENERAL ELECTRIC
PROCESS COMPUTER
PHOENIX

TITLE FUNCTION SCHEMATIC
CONTROL LINE MODULE
FOR GE-PAC 30

DWG NO (FS21)
70B113243

SCALE OF SHEET 4. DWG NO. 3



The THEORY OF OPERATION [illegible] Control Line Modules (CLM) says...

a "1" in a bit w in the computer memory halfword reserved for CLM data turns ON the associated output transistor in the CLM interface. Thus, if the collector of that transistor is hooked to one end of a 12VDC relay and the other side of the relay is hooked to +12VDC (see below)

note: open-collector, grounded emitter NPN type transistor

then the "1" in memory would turn ON the associated relay.

This seems to jive with other documentation (eg: the Sawmill Computer I/O prints).

However, the CLM interface schematic seems to imply that a "1" in the computer memory would turn OFF the associated output transistor!! It would appear the schematic is in error. However, w/o being able to scare up a spare of the CLM interface, it's not known, exactly, what is in error on the schematic.

DRAWN BY J. [illegible] 28 AUG 69
APPROVED Sept 11, 1969

DWG NO (FS21)
70B113243
SHEET 4 DWG NO. 3

DIST.		UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING					GENERAL ELECTRIC	TITLE	DWG NO
		APPLIED PRACTICES	SURFACES	FRACTIONS	DECIMALS	ANGLES	PROCESS COMPUTER PHOENIX	FUNCTIONAL SCHEMATIC CONTROL LINE MODULE	(FS21) 70B113243
			√	±	±	±		GE-PAC 30	CONT ON SHEET 5 SH NO 4

BACK PANEL MAP

CONN POS / MOT'H. BD / VERT. POS		HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS			HORIZ POS		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
1	22																		
	21																		
	20																		
	19																		
	18																		
	17																		
	16																		
	15																		
	14																		
	13																		
	12																		
	11																		
	10																		
	09																		
	08																		
	07																		
	06																		
	05																		
	04																		
	03																		
	02																		
	01																		
	00																		
0	22		P5	GND															
	21																		
	20																		
	19																		
	18																		
	17		SCLRO																
	16																		
	15		SYNO																
	14																		
	13																		
	12																		
	11		DRO																
	10		ADR50	CMDO															
	09																		
	08																		
	07																		
	06																		
	05		DAL030	DAL070															
	04		DAL020	DAL060															
	03		DAL010	DAL050															
	02		DAL000	DAL040															
	01																		
	00		P5	GND															

MADE BY		APPROVAL	DSG	REV	DWG NO
J. [illegible]	28 AUG 69			D	(FS21) 70B113243
ISSUED Sept 11, 1969			CHKD		CONT ON SHEET 5 SH NO 4