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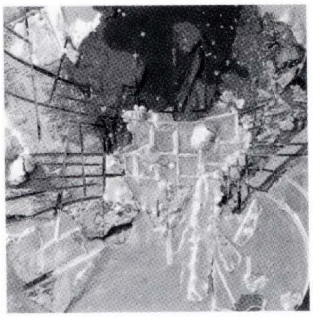

The Issue's Cover:
Fluctuation by Hirofumi OHKUMA

In quantum mechanics, at any given time, particles existing in a small area have an equal probability of being found at any of their possible locations and are traveling at various speeds. Particles are in constant random motion.

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• Takeshi Imamura

This paper reviews the fabrication technology developed for Josephson integrated circuits and describes the techniques used in the standard process for various circuit elements including Nb/AlO_x/Nb junctions. These process techniques were verified based on the characteristics of the 8K-bit cell array chips fabricated for process evaluation as being applicable to Josephson circuits that include several thousand junctions. Without the process technology based on the reliable Nb/AlO_x/Nb junctions, the recently demonstrated ultrahigh-speed operation of Josephson integrated circuits would not have been possible. This paper also introduces advanced process techniques developed for future Josephson LSI application.

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Josephson Integrated Circuits II High-Speed Digital Circuits

• Shinya Hasuo

Josephson junctions with Nb/AlO_x/Nb structures have made it possible to fabricate a variety of high-speed circuits, including an 8-bit digital signal processor and 4K-bit memory.

These circuits operate at ultrafast speeds and consume less power than any high-speed semiconductor circuits. An interface circuit which issues the signal from Josephson circuits to semiconductor circuits has also been fabricated. In short, it is possible to fabricate all components necessary for constructing a Josephson computer. Now the high-speed operation of the Josephson computer must be demonstrated.

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Josephson Integrated Circuits III A Single-Chip SQUID Magnetometer

• Norio Fujimaki

Superconducting Quantum Interference Devices (SQUIDs) can measure magnetic fields as low as femto tesla and have been used for biomagnetism, resource surveying, and physical or geophysical measurement. Unlike the conventional SQUID, the single-chip SQUID is the first device that intergrates both a SQUID sensor and a feedback circuit on the same chip. This reduces the number of external cables. Also, the output can be processed with Josephson digital circuits in the cryogenic environment. These advantages open up the possibility of constructing a multichannel system with an array of more than 100 SQUIDs, which is required to measure a magnetic field map in detail.

UDC 621.383.52
FUJITSU Sci. Tech. J., **27**, 1, pp. 84-91(1991)

High-Speed Monolithic GaInAs Twin PIN Photodiodes for Coherent Optical Receivers

• Masao Makiuchi • Hisashi Hamaguchi • Osamu Wada

Monolithic GaInAs twin PIN photodiodes were fabricated to realize excellent dual-detector balanced optical receivers in coherent optical communication systems. Introducing a backilluminated, flip-chip structure gives these photodiodes a small junction capacitance of 80 fF, a quantum efficiency of 75 percent at a wavelength of 1.54 μm, and a cutoff frequency better than 15 GHz. An optical input power level as high as 8 mW is obtained.

A large fiber alignment tolerance of 60 μm is achieved by integrating InP microlenses. The common-mode rejection ratio is better than −30 dB at a frequency of up to 10 GHz. The performance demonstrated is well suited to high-speed optical coherent communication systems.

UDC 621.391.6:621.395.4
FUJITSU Sci. Tech. J., **27**, 1, pp. 92-106(1991)

SONET System for North America

• Masahiro Shinbashi • Akihiko Ichikawa • Kenji Sato

In 1988, the Phase I standard of Synchronous Optical Network (SONET) was established by ANSI. Standards committees are planning for Phase II, which defines the functions for maintenance and operations, and which will be generally standardized in late 1990.

Fujitsu produced the Fiber Loop Multiplexer (FLM) series conforming to the Phase I standard for the Regional Bell Operating Companies (RBOCs) before its competitors. The FLM was well received.

This paper describes the SONET systems created by Fujitsu, Fujitsu's plan to upgrade to Phase II, and the key technologies used in the product.

UDC 681.327.5:681.621.83
FUJITSU Sci. Tech. J., **27**, 1, pp. 107-114(1991)

Conductive Fur Brush Charging of a Dielectric Surface

• Masahiro Wanou • Masatoshi Kimura

Charging of a dielectric surface without corona discharge has been achieved using a conductive fur brush to which an electrical potential of several hundred volts is applied. In this method, it was observed that brush charging is accomplished by direct charge transfer, gas discharge, and triboelectric charging. Direct charge transfer, the primary charging process, was analyzed using an ohmic contact model. The charged potential is nearly proportional to that of the brush. When the charging time exceeds 0.3 seconds, the charged potential on the surface of the photoreceptor saturates at almost the potential of the brush. Brush charging is, therefore, useful as a low-voltage charging technique.

UDC 681.7.03
FUJITSU Sci. Tech. J., **27**, 1, pp. 115-131(1991)

Design of Organic Nonlinear Optical Materials for Electro-Optic and All Optical Devices by Computer Simulation

• Testsuzo Yoshimura

This paper investigate the use of organic materials for nonlinear optical devices as a means to providing a breakthrough in optical nonlinearities. For electro-optic devices, an improvement in second-order nonlinearity 10-100 times as large as that of $LiNbO_3$ is needed.

For all-optical devices, an improvement in the third-order nonlinearity over 10 times as large as that of ordinary polydiacetylene (PDA) is required. To achieve these objectives, several organic materials were designed based on newly proposed guidelines requiring that the balance between wave function overlap and separation (or difference) be optimized. Computer simulations show that the objectives may be attainable by controlling the wave function and forming quantum wells through adjusting donor and acceptor substitution sites in one-dimensional conjugated systems.

UDC 621.3.049.75.002.2:681.32
FUJITSU Sci. Tech. J., **27**, 1, pp. 132-140(1991)

CIM System for PC Board Design and Manufacture

• Tsuyoshi Kobayashi • Hideaki Kuwabara

The importance of computer-integrated manufacture (CIM) in the design and manufacturing of printed circuit boards (PC boards) is widely acknowledged. It is difficult to increase the efficiency of schematic design, pattern layout design, or manufacturing using CAD/CAM separately. This paper discusses the construction of a PC board CIM system for use as a key system in a company. It describes the background and scope of CIM, and explains the concept of CIM construction, showing examples. It also introduces the automated drawing input system for PC board design and the supporting system for mounting the parts. This system is advanced technology related to CIM construction.

UDC 624.04:681.32
FUJITSU Sci. Tech. J., **27**, 1, pp. 141-146(1991)

High-Speed Structural Analysis Program: POPLAS® / FEM5 on Supercomputer

• Yasuhiro Komori • Katsuhiko Akahori

This paper describes the high-speed processing achieved by the development of the structural analysis program POPLAS®/FEM5 (called FEM5) on the multiple-pipeline architecture of the FUJITSU VP-series supercomputer.

The CPU time has been reduced by using a method of solving simultaneous linear equations that takes advantage of performance capabilities of a supercomputer. This method is combined with a matrix column-row exchange method. Concentrated vector tuning is also used.

The I/O time has been reduced by developing original I/O processing. As a result, FEM5 has achieved superlative high-level, high-speed processing in the structural analysis field.

UDC 538.945:621.3.049.771

Josephson Integrated Circuits I Fabrication Technology

• Takeshi Imamura *(Manuscript received September 3, 1990)*

This paper reviews the fabrication technology developed for Josephson integrated circuits and describes the techniques used in the standard process for various circuit elements including Nb/AlO_x/Nb junctions. These process techniques were verified based on the characteristics of the 8K-bit cell array chips fabricated for process evaluation as being applicable to Josephson circuits that include several thousand junctions. Without the process technology based on the reliable Nb/AlO_x/Nb junctions, the recently demonstrated ultrahigh-speed operation of Josephson integrated circuits would not have been possible. This paper also introduces advanced process techniques developed for future Josephson LSI application.

1. Introduction

Superconductivity has been studied ever since 1911[1]. Although current flow without power consumption in electronics applications is certainly appealing, it took another fifty years before the application of superconductivity to electronics finally began. This is because the microscopic theory of superconductivity has unknown for a long time. Without a theoretical basis, it was difficult to develop superconducting devices. Such difficulties were solved by two theoretical innovations introduced around 1960. One is the quantum theory of superconductivity proposed by Bardeen, Cooper, and Schrieffer in 1957[2]. The other is the superconducting tunneling phenomenon theoretically predicted by Josephson in 1962[3]. This effect, called Josephson effect, was experimentally verified in 1963[4]. Based on such development in theoretical study, the application of superconductivity to electronics has begun in earnest[5)-7]. The various types of proposed superconducting devices are divided into three groups: the cryotron[8], Josephson junction devices[9], and superconducting three-terminal devices[10]. Among them, only the Josephson junction features high-speed performance, which has been experimentally demonstrated. Much effort has been focused on Josephson circuit technology. Even now, the application of Josephson junctions is limited to such applications as voltage standard[11], magnetic sensor for medical use[12)-14], and a mixer for radio astronomy[15)-16]. Discrete Josephson devices have been used in these applications. The integrated circuits for digital application remain in the research stage for two reasons: the ultrahigh performance not possible with semiconductors has not been readily demonstrated using Josephson LSI chips, and even a small superconducting digital computing system requires the further development of such peripheral technologies as packaging and cooling. Recently, however, significant progress has been made in Josephson circuit technology[17)-19]. We expect to introduce a small-scale superconducting computing system in the near future.

The Josephson junction devices use the superconducting tunneling effect, and, theoretically, should achieve high-speed, low-power operation not possible with semiconductors[20),21]. Since the mid-1960s, IBM has spearheaded Josephson device research[5)-7]. During the mid-1970s to early 1980s, many organiza-

tions also joined the race to develop a Josephson computer[22)-27)]. This work stopped abruptly when IBM ended its Josephson computer project in September 1983[28)] for two reasons. First, Josephson circuits were not much faster than semiconductor circuits. Secondly, it was difficult to develop a high-speed cache memory. Ever since IBM lost its enthusiasm for developing Josephson junctions for digital applications, others have followed in kind. Research in Japan, however, has continued all along. One of the problems posed by Josephson junctions used at that time was the instability of the junction materials – lead alloys[29)-31)]. For one thing, the critical current of the junction increased with time during storage at room temperature. For another, the scattering of critical current was too large, even for junctions on the same chip, making it very difficult to manufacture LSI circuits.

The introduction of reliable niobium (Nb/AlO_x/Nb) junctions at the end of 1983 to replace the obsolete lead-alloy junctions changed the picture dramatically. The Nb/AlO_x/Nb junction as developed by Gurvitch et al[32)]. was further improved by Morohashi et al[33),34)]. The introduction of niobium junctions solved most of the problems hindering process reliability. Many kinds of fabricated logic and memory circuits could operate at much higher speeds than semiconductor circuits. Recently, a Josephson gate established a 1.5-ps gate delay at a power dissipation of only 12 μw[35)]. The world's first Josephson microprocessor operated at a clock frequency of 770 MHz[36)]. An 8-bit digital signal processor with 6 300 gates operated at 1 GHz[37)]. Josephson digital circuit technology was also applied to the superconducting quantum interference device (SQUID) magnetometer[12)-14)], where the Josephson junction had been used as an analog magnetic sensor. This enabled us to develop a single-chip SQUID including a feedback circuit[38)]. These developments have been made possible by the high quality and excellent uniformity of junction characteristics.

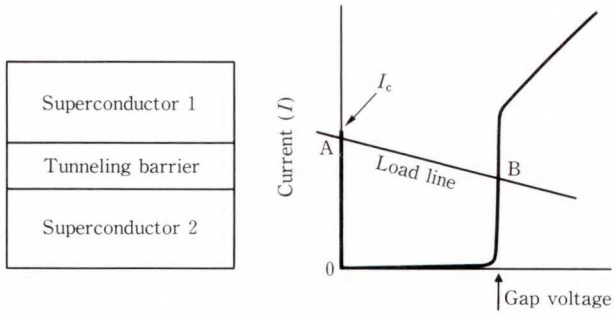
This paper (Part I) reviews recent developments in Josephson circuit technology achieved by our laboratories, and describes the fabrication technology of Josephson circuits based on Nb/AlO_x/Nb junctions. Part II[19)] describes the high-speed performance of fabricated Josephson integrated circuits, and Part III[39)] describes the breakthrough made in SQUID magnetometers.

Chapter 2 of this paper (Part I) reviews the Josephson junction materials investigated thus far. Chapter 3 describes the standard fabrication process using Nb/AlO_x/Nb junctions. Chapter 4 describes the advanced process technology being developed for future Josephson LSI application. In conclusion, chapter 5 summarizes this paper.

2. Junction materials

The Josephson junction is made of a thin tunneling barrier sandwiched between two superconducting films called the base and counter electrodes. See references 40 and 41 for the principles of Josephson junction. Figure 1a) shows a cross section of the junction, and 1b) shows the current-voltage (I - V) characteristic. The maximum superconducting tunneling current is called critical current (I_c). When the bias current exceeds I_c, the junction switches from zero-voltage state A to voltage state B. Thus, I_c is one of the most important device parameters used in circuit design. In most Josephson junctions, the tunneling barrier is as thin as a few nanometers. Since I_c decreases exponentially with the barrier thickness, barrier formation integrity is essential for obtaining good junctions.

Circuit fabrication requires the use of stable, uniform, high-quality, and reproducible junctions.



a) Structure of Josephson junction

b) I-V characteristics

Fig. 1 –Principles of the Josephson junction.

1) Stable

The junction characteristic is stable against thermal cycling between 4.2 K and room temperature. Stability during long-term storage at room temperature is also crucial.

2) Uniform

I_c variation is small (typically less than ten percent) for junctions on a chip.

3) High-quality

Small leakage current in the sub-gap voltage region for the I-V characteristic. Parameter V_m is normally used to determine junction quality, as described later.

4) Reproducible

Expected junction characteristics, particularly the cririca current, are reproducible through the process.

Throughout the 1970s, lead alloy materials have been used as junction electrode materials. Native oxide grown by plasma oxidation was used for the junction barrier[29]. Much effort has been focused on improving the reliability of lead-alloy junctions[42)-45)]. By the early 1980s, however, it became clear that unreliable lead-alloy junctions could not provide the Josephson integrated circuits required[31]. For example, I_c of the junction continues changing during long-term storage even at room temperature, and excessive I_c variation hinders integrated circuit operation. Moreover, the initial junction yield is not high enough to facilitate use in circuits. Typically, one percent of the junctions is initially shorted. Such unreliable characteristics are due to large-grained, corrosive, and mechanically soft lead-alloy electrodes.

Much work has gone into replacing lead-alloy electrodes with such refractory materials as Nb and NbN[46], which are much more fine-grained, hard, and stable. Table 1 lists the "all-refractory" junctions reported thus far. "All-refractory" means that both the base and counter electrodes are made of refractory materials. The sequence indicated by slashes (/) refers to "counter electrode/barrier/base electrode". V_g is the gap voltage, and V_m is the quality parameter defined by the product of the critical current and subgap resistance at 2 mV. Recently, V_m for NbN junctions has been defined at 3 mV because the Nb junction has larger V_g than Nb junctions. Junctions to be used in Josephson integrated circuits require V_m exceeding ~30 mV to afford a wide circuit's operating margin enough for practical use.

Table 1. All-refractory Josephson Junctions

Junction	V_g (mV)	V_m Note 1) (mV)	Ref.
Nb/oxide/Nb	2.8	6-8	47, 51
Nb/Au/oxide/Nb	2.6	26	54
Nb/*a*-Si/Nb	2.8	28	55-58
Nb/AlO_x/Nb	2.8-2.9	40-70	32, 33
Nb/ZrO_x/Nb	2.8	50	59
Nb/YbO_x/Nb	2.8	15	60
Nb/TaO_x/Nb	2.8	25	61
Nb/Si_xN_y/Nb	2.8	16	62
NbN/oxide/NbN	4.0-4.4	15-25	63, 64
NbN/*a*-Si/NbN	4.4	10-12	65, 66
Nb/p-Ge/NbN	4.0	35-48	68
NbN/MgO/NbN	5.1-5.4	45-50 Note 2)	70-73

Note 1) : V_m defined at 2 mV.
Note 2) : V_m defined at 3 mV.

In early studies, Nb was used for the base electrode alone, and the Nb_2O_5 barrier enjoyed some success[47)-50)]. Attempts to use all-refractory junctions, however, were less than successful. High-quality junctions feasible for circuit applications were difficult to fabricate, and V_m was less than 10 mV[47),51)]. The subgap conductance was too large for use in circuits. This means that the tunneling barrier contains pinholes, inducing leakage current, apparently due to the chemical reaction between the Nb counter electrode and Nb_2O_5 barrier. Studies on the interface between the Nb electrode and oxide barrier[52),53)] resulted in a thin Au layer being introduced to minimize subgap conductance[54]. The highest attainable V_m (26 mV) still proved insufficient for use in Josephson LSI.

Studies on artificial barrier materials other than native Nb_2O_5 have been challenged. "Artificial" refers to the intentional depositing of barrier materials on the base electrode. Studies on barrier materials that react less at the interface with Nb electrodes have tended to take one of two approaches: Using a semiconductor barrier or using a metal oxide barrier. In the first approach, an amorphous silicon barrier offered

the best characteristics V_m = 28 mV)[55)-58)]. With the second approach, some of the many metals studied were found to function as good junction barriers when adequately oxidized[32),59)-62)]. Among them, the AlO_x barrier has outstanding quality[32),33)]. V_m reproducibly exceeds 40 mV while I_c uniformity and controllability are far superior to those of any other refractory junctions. Not surprisingly, recent developments in Josephson circuits have proceeded almost exclusively using $Nb/AlO_x/Nb$ junctions.

A possible Nb alternative also receiving much attention has been NbN[46)]. The use of NbN, which has a higher critical temperature, results in large V_g and smaller subgap conductance. NbN is also less chemically reactive than Nb and less sensitive to oxygen contaminants – both advantages in making high-quality junctions – but the coherence length of NbN is shorter than Nb, necessitating the formation of a thinner tunneling barrier on NbN. The greater penetration depth in NbN also reduces the junction's switching sensitivity. Of the many barrier materials used for junctions with NbN electrodes[63)-74)], MgO has shown the highest quality – V_m of 45 mV to 50 mV[70),71)]. Junction quality generally depends on the critical current density, particularly in NbN/MgO/NbN junctions. Thus, the V_m in Table 1 is selected from junctions with a practical current density greater than 1 000 A/cm^2.

The all-refractory junctions used to fabricate a variety of logic and memory circuits thus far are $Nb/AlO_x/Nb$[17),18)], NbN/oxide/NbN[75)], and NbN/MgO/NbN[76)]. Most Josephson circuits, however, have been made of $Nb/AlO_x/Nb$. We have made significant progress in Josephson circuit technology development based on $Nb/AlO_x/Nb$ junctions, mainly due to their high quality and reproducibility.

The following chapters also introduce fabrication using the $Nb/AlO_x/Nb$ junctions developed in our laboratories. After a brief description of the standard integrated circuit fabrication process, this paper discusses the advanced techniques developed for future Josephson LSI application.

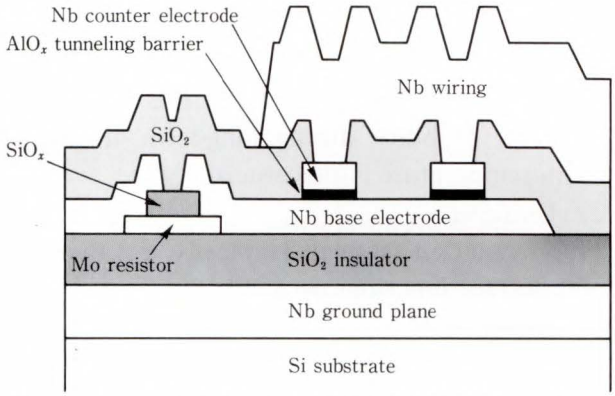


Fig. 2 – Integrated circuits with $Nb/AlO_x/Nb$ Josephson junctions.

3. Standard process

3.1 Outline

Josephson integrated circuits consist of the $Nb/AlO_x/Nb$ Josephson junctions, SiO_2 insulators, Mo resistors, Nb ground plane, and Nb wiring, usually formed in nine to eleven layers on Si substrates[77)]. Each layer is patterned through a photoresist mask by reactive ion etching (RIE).

As shown in the typical cross section in Fig. 2, Josephson circuits are usually fabricated above a superconducting ground plane. The Nb wiring formed above the ground plane composes a superconducting strip line. This is necessary to enable high-speed signal transmission between adjacent junctions. Resistors that are used as loads or as damping resistors[78)] in junction switching contact the base electrode. Contact holes are formed in insulators above the junction counter electrodes to ensure electrical contact with subsequent wiring. The contacts between the base electrode and ground plane, which are not shown in Fig. 2, are necessary for Josephson circuits. Contact is enabled by the base electrode through a hole in the insulation layer above the ground plane. In logic circuits designed using the MVTL gate family[79)], wiring is set in the top layer. In memory and some types of logic circuits, two additional layers are formed on the wiring, i.e. insulators and control lines.

Table 2 lists the layer materials and thicknesses. Nb, Al, Mo and SiO_2 are deposited by sputtering under the conditions listed in Table 3. The SiO_x used as a protective (P) layer for Mo resistors during RIE of the Nb base electrode is

Table 2. Circuit layers

Layer		Material	Thickness (nm)
GP	Ground plane	Nb	300
I_1	Insulation	SiO_2	300
R	Resistor	Mo	100
P	Resistor protection	SiO or SiO_x	100
B	Base electrode	Nb	200
–	Tunneling barrier	AlO_x-Al	7
C	Counter electrode	Nb	100-200
I_2	Insulation	SiO_2	400
WR	Wiring	Nb	600
I_3	Insulation	SiO_2	800
CL	Control line	Nb	1 000

Table 3. Metal and insulation layer sputtering

Material	Ar pressure (Pa)	Deposition rate (nm/min)
Nb	1.3-2.3	200
Al	1.3	8
Mo	0.67	130
SiO_2	1.3	8

Table 4. Metal and insulation layer patterning

Material	Reactive gas	Pressure (Pa)	Power density (W/cm^2)
Nb	CF_4 (5-20 % O_2)	2.7-6.7	0.10
Al	Ar	0.7	0.15
Mo	CF_4 (5 % O_2)	6.7	0.10
SiO_2	CHF_3 (0-15% O_2)	2.0	0.20

deposited by evaporating SiO in an oxygen atmosphere[80]. All layers except the P layer are patterned by RIE. Table 4 lists the reactive gases used in RIE. Because Al and AlO_x are not etched by reactive CF_4 and CHF_3, they act as an etching stopper. The thin AlO_x-Al barrier is removed by Ar sputter etching. The SiO_x used for the P layer is patterned by lift off[31].

Although the key process in Josephson LSI development is producing high-quality junctions, the other circuit elements are also important. These elements include the insulation layer, superconducting wiring resistors, and contacts between two Nb layers. The following sections briefly describe the standard fabrication process optimized for Nb/AlO_x/Nb junctions, SiO_2 insulators, Nb wirings, contacts, and Mo resistor. The final section evaluates the standard process

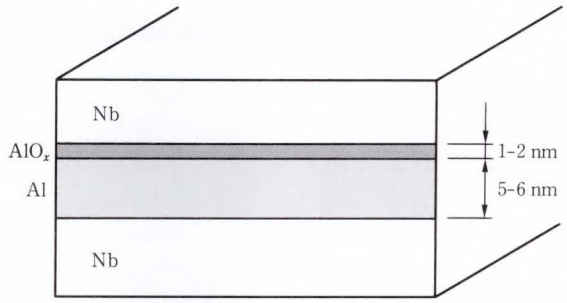


Fig. 3 –Nb/AlO_x/Nb Josephson junction.

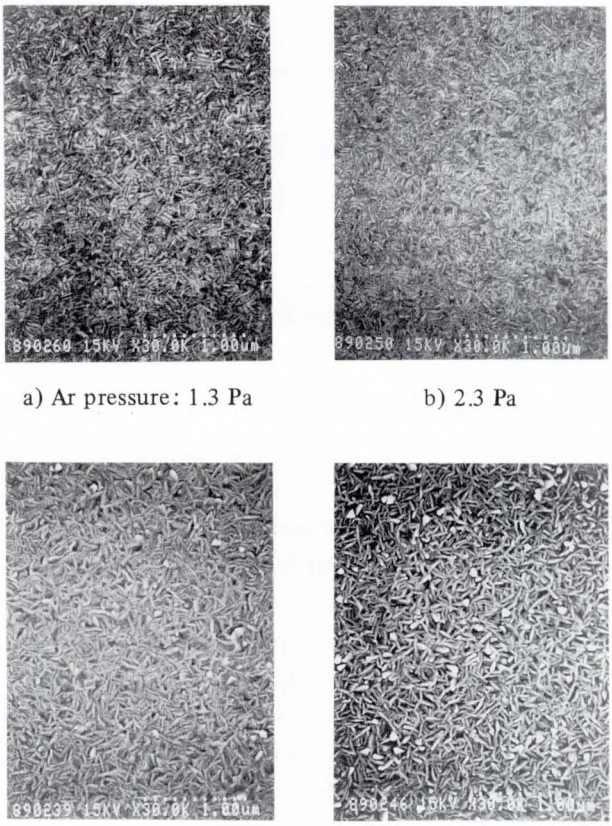
in full vertical structures from the ground plane to the control line, both at 300 K and 4.2 K.

3.2 Nb/AlO_x/Nb junctions

3.2.1 Excellence of Nb/AlO_x/Nb junctions

Figure 3 shows a cross section of the Nb/AlO_x/Nb junction used in the standard process. The required junction characteristics are stability, uniformity, reproducibility, and high quality as described in Chap. 2. On these characteristics, the Nb/AlO_x/Nb junctions offer the best I-V characteristics among all refractory junctions. This excellence of the Nb/AlO_x/Nb junctions is due to the following four properties. First is the stability of refractory Nb with its fine-grain, smooth surface. Second is the affinity of the thin Al to the underlying Nb. An Al layer a few nanometers thick can wet the Nb surface[81)-84)]. Third is the integrity of the AlO_x barrier formed on Al. The uniform AlO_x 2 nm thick is reproduced by introducing oxygen into a vacuum chamber. Fourth is that the AlO_x barrier is not damaged by the subsequent deposition of the counter Nb electrode. In addition to these inherent material properties, the development of the whole wafer process[32),55)] is vital to enhance junction process reliability. In this process, the Nb/AlO_x/Nb multilayered structure is deposited in a vacuum run to eliminate contaminants around the junction barrier.

To reproduce high-quality Nb/AlO_x/Nb junctions, we have optimized the various process parameters listed in Tables 3 and 4. In particular, the deposition of the Nb/AlO_x/Nb trilayer structure is essential to obtaining high-quality junctions. The depositing parameters of Nb and Al were observed to affect the junction charac-



a) Ar pressure: 1.3 Pa

b) 2.3 Pa

c) 3.3 Pa

d) 4.0 Pa

Fig. 4—SEM photographs of Nb films deposited at different Ar pressures. Film thickness is 600 nm.

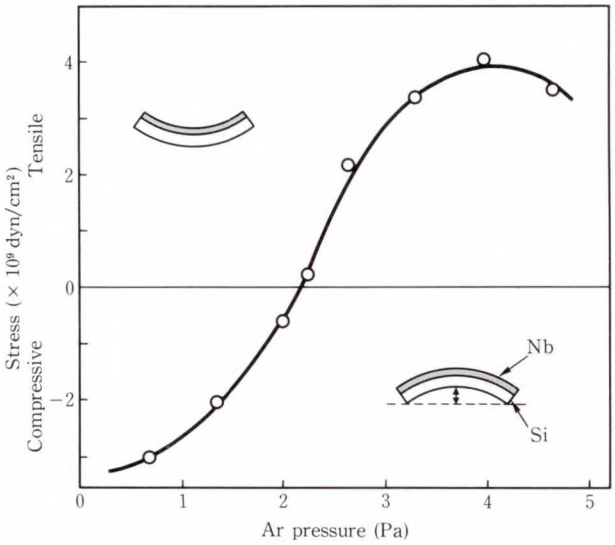


Fig. 5—Nb film stress versus Ar pressure during sputtering.

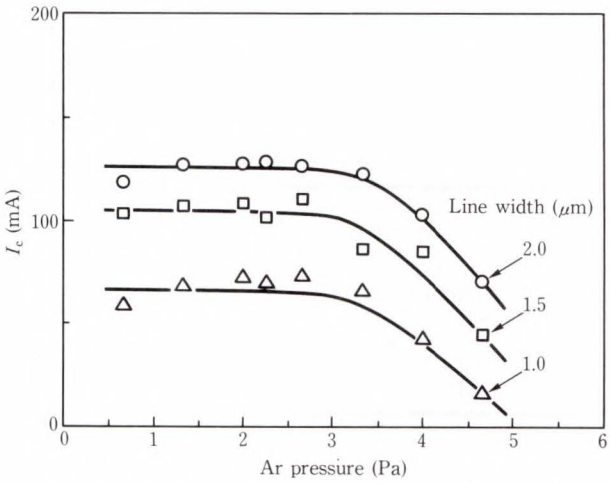


Fig. 6—Critical current I_c of Nb wirings versus Ar pressure.

teristics. Reference to details on optimization is made in some papers[34),85)-87)]. The following subsections briefly describe two points affecting the junction characteristics: the quality of Nb electrode[85)] and the coverage of thin Al on Nb[86),87)]. The standard process for junctions and their characteristics is described below.

3.2.2 Nb electrodes

The Nb electrodes were deposited with dc and rf magnetron sputtering. A comparison of the junction characteristics concluded that junctions with dc-sputtered Nb are superior to those with rf-sputtered Nb[34)]. This difference is due to the interdiffusion between the lower Nb and thin Al layers. Based on these results, our research has focused on optimizing the parameters of dc-sputtered Nb.

The film characteristics of dc-sputtered Nb were studied in terms of surface morphology, stress, crystal structure, and superconductivity. These characteristics change depending on the sputtering parameters, typically on the Ar pressure.

Sputtered Nb film has a columnar structure with polycrystalline grains, where the Nb(110) plane is oriented in parallel to the substrate surface. Figure 4 compares scanning electron microscopy (SEM) photographs of Nb deposited at different Ar pressures. The surface morphology of sputtered Nb features a fine filamentous texture. At higher Ar pressures, however, the surface morphology deteriorates as small grains of increased density appear in the texture. Figure 5 shows the intrinsic stress of sputtered Nb changes as a function of Ar pressure. The

stress changes from compressive to tensile as the Ar pressure increases. At around 2.3 Pa, stress-free Nb is obtained. Figure 6 shows the superconducting critical current of 600-nm Nb wiring as a function of the Ar pressure. The superconductivity of Nb film gradually deteriorates above a threshold Ar pressure of 3 Pa.

When considering the surface morpholgy and superconductivity of sputtered Nb, films deposited at low Ar pressures are regarded more suitable for junction electrodes. Based on these results, the Ar pressure for the standard process was fixed at 1.3 Pa, although it is a little compressive. For the characteristics of junctions larger than 1 μm, however, we observed no effects caused by the compressive stress of Nb film. To make junctions smaller than 1 μm, the use of stress-free Nb was considered crucial to achieving high-guality junctions, as described in Sec. 4.1.

3.2.3 Coverage of Al on Nb

Since Al is several nanometers thick, its coverage on the underlying Nb is critical to grow a uniform AlO_x barrier without pinholes. The coverage of thin Al on Nb was studied by using X-ray photoelectron spectroscopy (XPS)[86),87)]. Figure 7 compares the Al 2p spectra for Al/Nb/Si of different Al thicknesses. Spectra are normalized by the peak height of Al oxide. For Al thicker than 2.1 nm, a peak of elemental Al is clearly observed. Figure 8 compares the Nb 3d spectra for the same samples. For Al thicker than 2.1 nm, peaks of Nb_2O_5 disappear, and only the elemental Nb peaks remain. Figure 9 summarizes the film growth of thin Al on Nb based on the values above, with XPS studies on Al/Si samples also indicated. For Al thinner than 1.4 nm, the Al is completely oxidized, and underlying Nb is partly oxidized. For Al thicker than 2.8 nm, the Nb surface is compeletely covered by elemental Al. Consequently, the Nb is not oxidized. The Al formed on Nb should be thicker than 2.8 nm

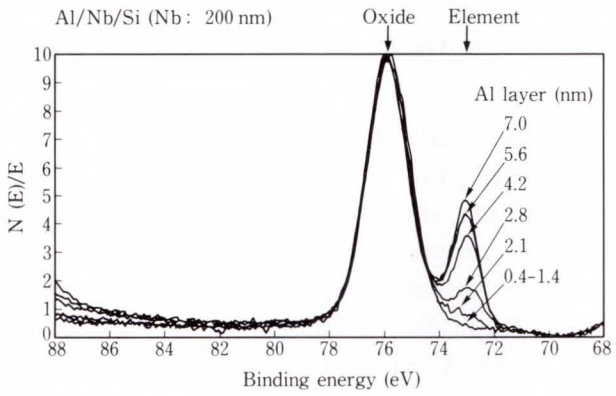


Fig. 7—Al 2p spectra for air-oxidized Al/Nb/Si.

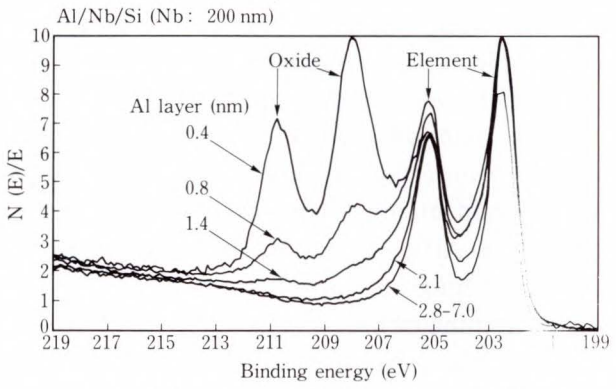


Fig. 8—Nb 3d spectra for air-oxidized Al/Nb/Si.

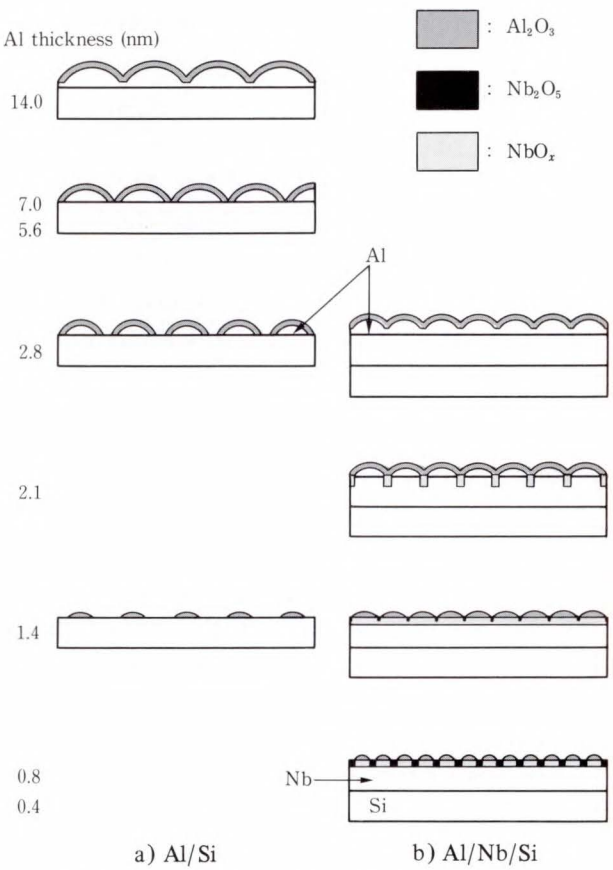


Fig. 9—Film growth of Al deposited on Nb.

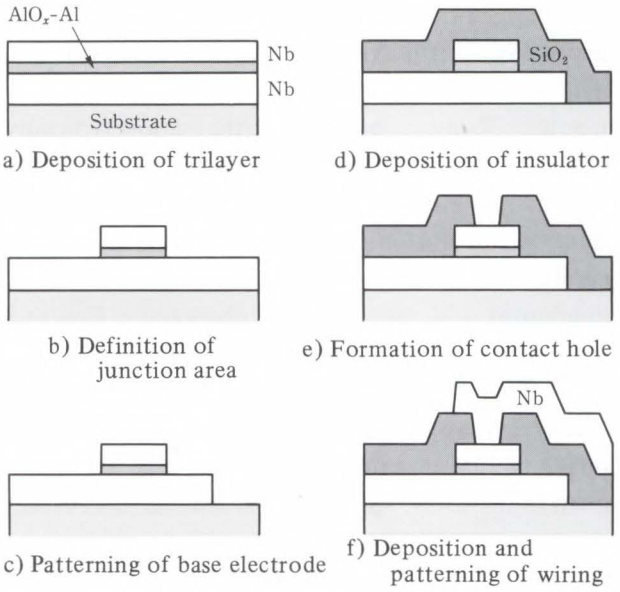


Fig. 10—Nb/AlO_x/Nb Josephson junction process sequence.

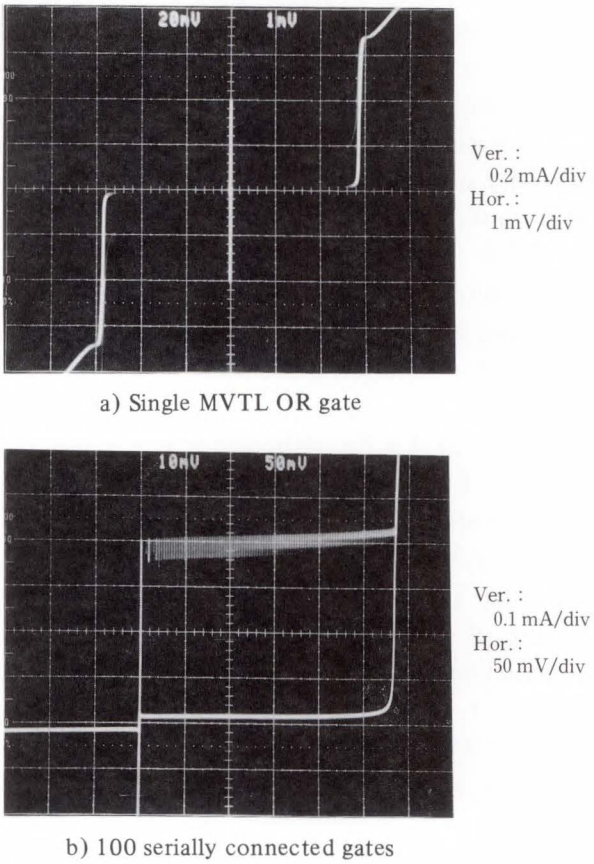


Fig. 11—I-V characteristics.

to obtain a clean Al/Nb interface. Conversely, when Al is deposited on Si, Al thicker than 7 nm can cover the Si surface. This indicates the affinity of Al to Nb is much better than that to Si. This enables formation of a thin Al barrier on Nb.

The I-V characteristics were examined for junctions of different Al thicknesses. Good characteristics were obtained for Al 2.8-10 nm thick. For Al thicker than 10 nm, the I-V characteristics gradually deteriorate due to the proximity effect on the Al/Nb interface. Based on these results, a standard Al thickness of 7 nm was established.

3.2.4 Junction process

Item a) to f) in Fig. 10 indicate the sequence of Nb/AlO_x/Nb junction fabrication.

a) Deposition of trilayer

Before trilayer (Nb/AlO_x/Nb) deposition, substrates are etched by Ar sputtering to contact the Nb ground plane through contact holes. The trilayer is then deposited by sputtering on the substrates attached to a holder cooled by circulating water. To ensure good thermal contact, copper backing plates and indium foils are used as spacers between the substrates and holder. The base pressure is less than 2×10^{-5} Pa. After the Nb base electrode and 7-nm Al barrier are sequentially deposited, Ar + 10%O_2 gas is introduced into the chamber to form a thin oxide 2 nm thick on the Al. The junction's critical current density (j_c), depends on the pressure (usually 50-200 Pa) and oxidation time (typically 30-60 min). j_c ranges of 500-20 000 A/cm^2. When j_c is designed at 2 000 A/cm^2, the averages of j_c range of 1 500-2 500 A/cm^2 for different waters. After oxidation, the Nb counter electrode is deposited on the AlO_x barrier. Next, the trilayer is trimmed into a device structure.

b) Definition of junction area

The junction area is defined by patterning the Nb counter electrode. In RIE, AlO_x and Al act as good etching stops against CF_4 gas. The remaining AlO_x-Al barrier is removed by Ar sputter etching.

c) Patterning of base electrode

The lower Nb is then etched into a base electrode pattern with CF_4.

d) Deposition of insulator

Junctions are covered with an SiO_2 insulation layer. Section 3.3 describes the sputtering of SiO_2.

e) Formation of contact holes

Contact holes above the counter electrodes are formed in the SiO_2 by RIE with CHF_3.

f) Deposition and patterning of wiring

Nb is deposited and patterned as a wiring layer.

3.2.5 Junction characteristics

The j_c uniformity is sufficient for circuit application. The standard deviation of j_c is about three percent for 2-μm-square junctions on a chip. The variation of j_c in different fabricated waters increases even in the same lot.

Figure 11 shows the I-V characteristics of modified variable threshold logic (VMTL) gates[79]. The gate junction is paired, 2.5 μm and 4.0 μm in diameter. The gap voltage is 2.9 mV. Quality parameter V_m exceeds 50 mV. The maximum-to-minimum spread of the critical current is ±5% for 100 gates.

$Nb/AlO_x/Nb$ junctions are very stable in thermal cycles between 4.2 K and 300 K, and in storage at room temperature. The I-V characteristics do not change during the first few years of storage, but are affected by annealing. Figure 12 shows changes in j_c and V_m after 60 minutes of annealing in nitrogen at different temperatures. The junction starts deteriorating with annealing above 200 °C. Critical current density begins decreasing after annealing at 175 °C. These changes are considered caused by the change in AlO_x composition and/or the interdiffusion of Al and Nb[34),83),88)].

Deterioration due to annealing is one of the most critical problems regarding the reliability of $Nb/AlO_x/Nb$ junctions. This makes it difficult to further develop Josephson circuit technology for two reasons. One is that the margin in process temperature is not very large; 175 °C is only 55 °C higher than the typical resist baking temperature. The other is that the annealing characteristic limits the application of various semiconductor process techniques.

Thus, the annealing characteristics should be improved for further development in Josephson circuit technology[89)].

3.3 SiO_2 insulators

In lead-alloy Josephson circuits, SiO or SiO_x films were used for insulation layers[31)], but the integrity of such films is not sufficient for Nb circuits. Figure 13 shows the breakdown voltage in SiO and SiO_x[90)]. The insulator is 300 nm thick, and the electrode is 4 mm square. Using sputtered Nb for the upper electrode reduces the

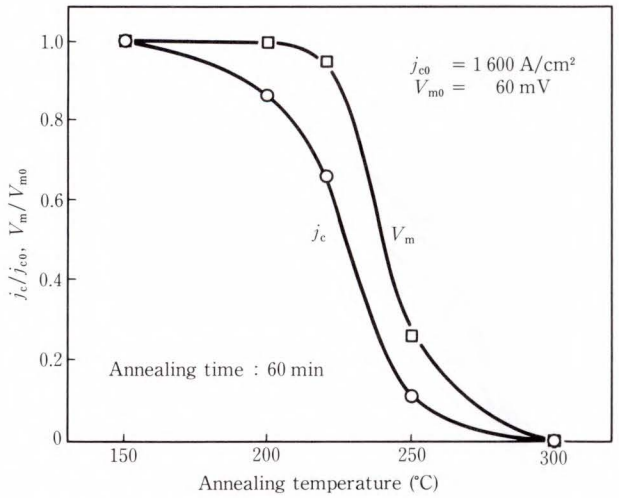


Fig. 12—Deterioration of Josephson junctions after annealing.

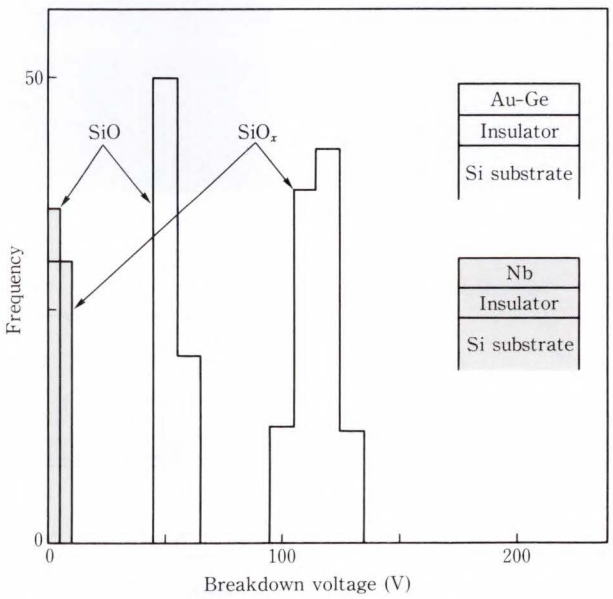


Fig. 13—Breakdown voltage in 300-nm SiO and SiO_x films.

breakdown voltage to almost zero due to microcracks induced by heat or stress during refractory Nb deposition.

Sputtered SiO_2 was used as an insulator in $Nb/AlO_x/Nb$ Josephson circuits[77),90)]. The breakdown voltage in sputtered SiO_2 (see Fig. 14) exceeds 200 V even when Nb is used for the upper electrode. When Nb is used for both upper and lower electrodes, the breakdown voltage of the sandwiched SiO_2 is reduced to one third the above value, though still exceeding 50 V. This is high enough for use in practical Josephson integrated circuits, where the junction voltage is only 3 mV. The deterioration of SiO_2 deposited on Nb is due to the differences in the initial SiO_2 film growth between on Si and on Nb.

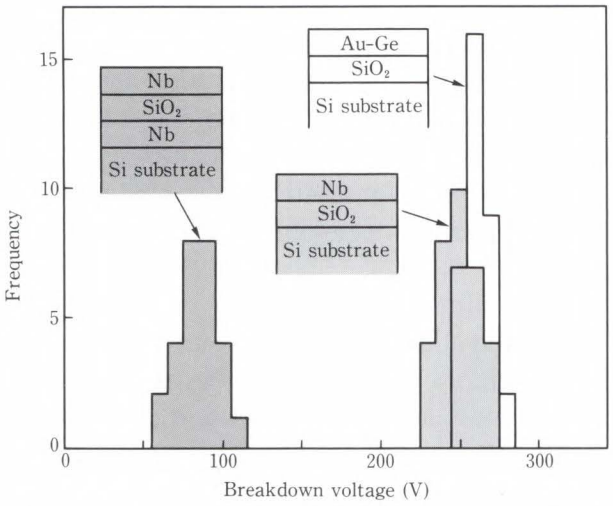
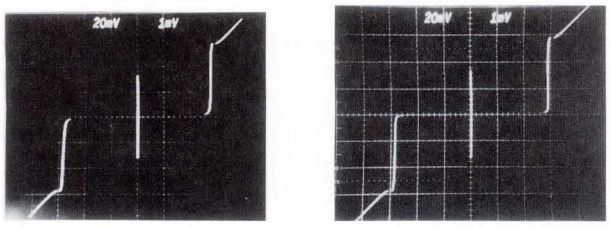
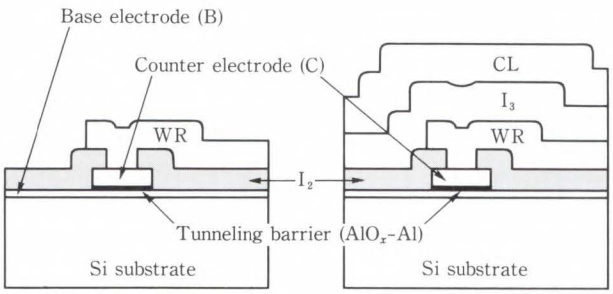


Fig. 14—Breakdown voltage in 300-nm sputtered SiO_2 films.



Ver.: 0.2 mA/div Hor.: 1 mV/div



a) Without I_3 and CL layers b) With I_3 and CL layers

Fig. 15—I-V characteristics and cross sections for junctions.

The $Nb/AlO_x/Nb$ junction deteriorates when annealed at temperatures exceeding 200 °C. When depositing SiO_2 on the junctions, thoroughly cooling the substrates during SiO_2 sputtering becomes critical for protecting the junctions against thermal damage. For this purpose, the deposition rate of SiO_2 was reduced to 8 nm/min. During sputtering, the substrates were attached to a water-cooled holder with indium foils. Through these measures, the application of SiO_2 in the junction process was found to cause no deterioration in the junction characteristics. Figure 15 compares junctions with and without an 800-nm SiO_2 insulation layer (I_3). The junction quality (V_m) exceeds 40 mV for both junctions. No deterioration in the characteristics were observed after depositing a thick layer of SiO_2 on the junctions. Based on these results, sputtered SiO_2 has been applied in the standard Josephson circuit process. The use of sputtered SiO_2 resulted in a significantly improved production yield for Josephson circuits. This was demonstrated in the yield evaluation for 8K-bit cell array chips[91)], as described in Sec. 3.7.

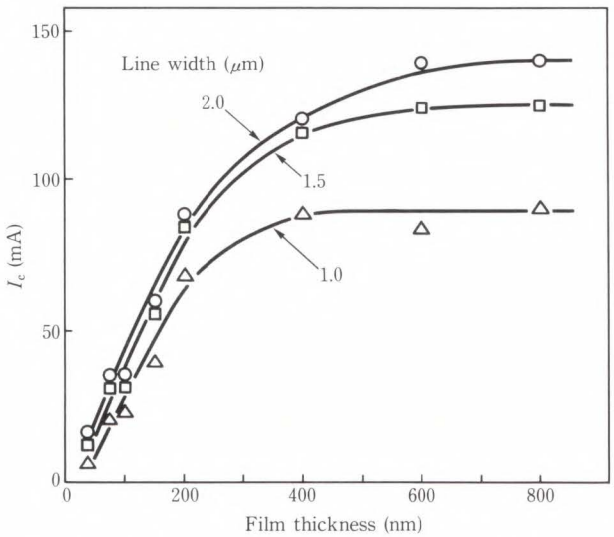


Fig. 16—Critical current I_c of Nb wiring lines[77)].

3.4 Nb wiring

In Josephson circuits, superconducting Nb is used for the wiring. As circuits become more densely integrated, long, narrow wiring lines are needed for circuit construction. Figure 16[77] shows the superconducting critical current (I_c) measured for Nb wiring. The lines are 1.0-2.0 μm wide and 10.88 mm long. For films thicker than 400 nm, I_c only depends on line width, not film thickness. For films thinner than 200 nm, however, I_c changes linearly with the thickness, apparently due to supercurrent flowing in the film surface up to the London penetration depth[40].

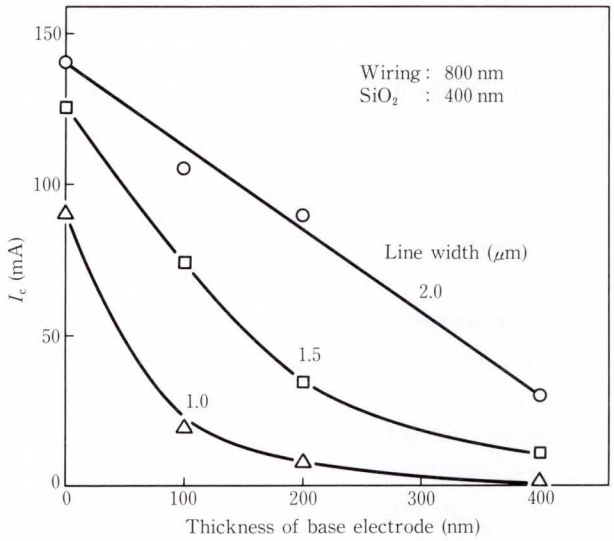


Fig. 17—I_c of wirings versus the thickness of underlaying Nb base electrode.

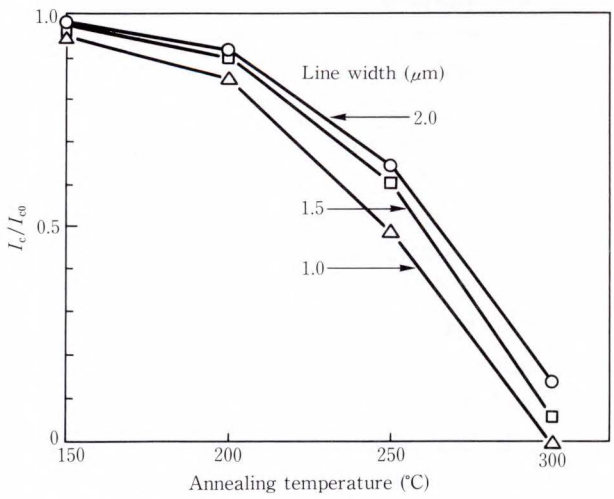


Fig. 18—Changes in I_c of wiring after annealing.

The I_c of Nb wiring is much greater than the current level of Josephson gates (typically less than 1 mA). In actual circuits, however, Nb wiring should run over steps of underlying layers. The I_c decreases steeply with the thickness of underlying layers (see Fig. 17). This is due to an effectively decreased film thickness at steps. Thus, the I_c of wiring at steps will be enhanced by improving the Nb coverage at steps. This was actually verified by applying bias-sputtered Nb to wiring as described in Sec. 4.4.

Another problem posed by Nb wiring is its annealing characteristics[85]. The I_c of wiring decreases with the annealing temperature as shown in Fig. 18, even when annealed in nitrogen. The reduction in I_c was observed to be closely related to the oxygen diffusion in Nb[85),89].

3.5 Contacts

Josephson circuits require contacts between two Nb electrodes. With increased circuit integration, smaller contacts with higher critical currents are needed. Contacts are made through holes formed in the insulating SiO_2 layers. The critical current of 200 serially connected contacts is plotted in terms of the contact area shown in Fig. 19[77]. Before Nb wiring deposi-

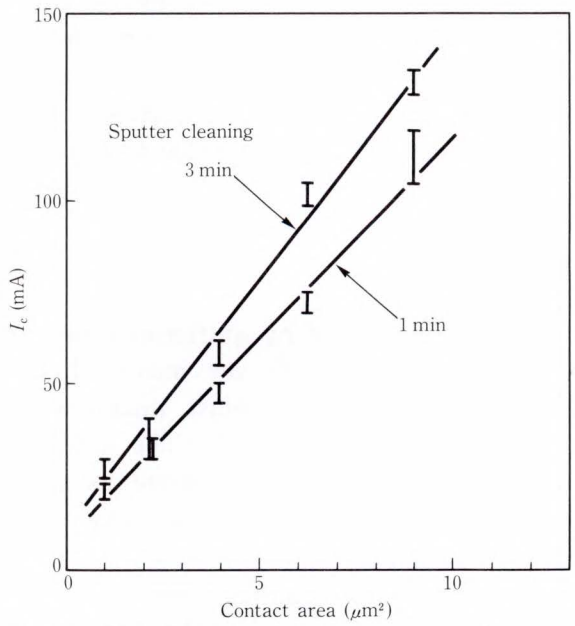


Fig. 19—Critical current I_c in contacts formed between Nb electrodes[77].

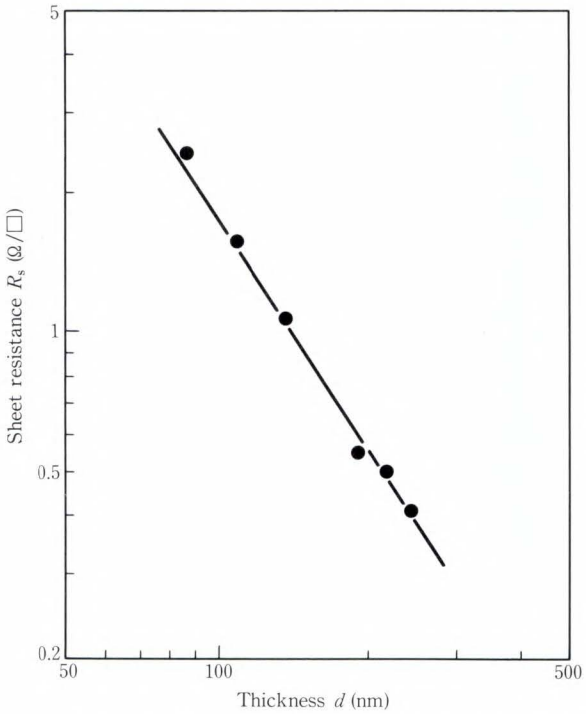


Fig. 20—Sheet resistance in Mo resistors.

tion, the Nb base electrode is cleaned by Ar sputtering at 1.3 Pa for one to three minutes to remove the native oxide formed on Nb. The sputtering power density was 1.9 W/cm^2. The base electrode is 200 nm thick and the wiring layer 800 nm thick. The critical current for contacts changes almost linearly with the contact area. Even for small contacts 1.0 μm square, the 20-mA critical current is much larger than the current flow in actual circuits. Also note that such contacts face the same problem as the wiring: I_c deterioration due to annealing. Section 4.4 describes how the annealing stability of contacts has been improved.

3.6 Mo resistors

Mo films deposited by sputtering form resistors. Figure 20[77] shows the measured sheet resistance (R_s) plotted against thickness (d). R_s is proportional to $d^{-1.6}$. The spread of resistance on a wafer is as small as several percent, and the contact resistance between Mo and Nb is negligible.

The Mo resistor requires a protective layer of SiO_x, which is patterned by lift-off. The damping resistor used in the gates makes it

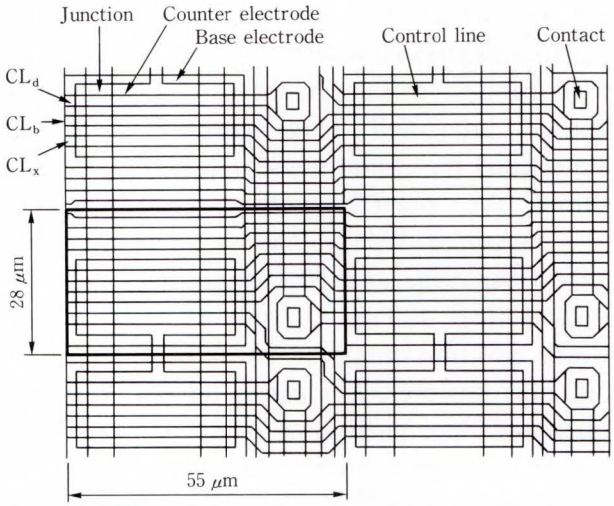


Fig. 21—Cell layout for the 8K-bit memory cell array chip. The unit cell is indicated by a bold rectangle.

difficult to reduce the gate size. Because the SiO_x lift-off enforces a rather large patterning margin. Thus we are developing new resistor material to make the protective layer of SiO_x unnecessary.

3.7 Process evaluation

The previous sections described the independent evaluation of the elements composing Josephson circuits. In actual circuits, however, such evaluations are not independent, but affect each other in complex ways. Thus, it is necessary to evaluate the characteristics of each element in full vertical structures, including the layers from the ground plane to the control lines. For this purpose, we have evaluated 8K-bit memory cell array chips from the early stages of our Josephson research[31]. The junctions tested thus far are lead-alloy (Pb-Bi/Pb-In-Au) junctions, Pb-Bi/Nb junctions, and Nb/AlO_x/Nb junctions[77),91].

The tested cell is a 2-junction interferometer with three control lines (see Fig. 21). The junction size is 5 x 14 μm^2 and the minimum line width is 2 μm. Figure 22 shows the fabricated 5 x 5 mm^2 cell array chip containing 8 192 cells and 87 pads. The fabricated chips were tested at two stages. First, the chip yield was measured at room temperature by using an automatic prober. Table 5 lists the test items.

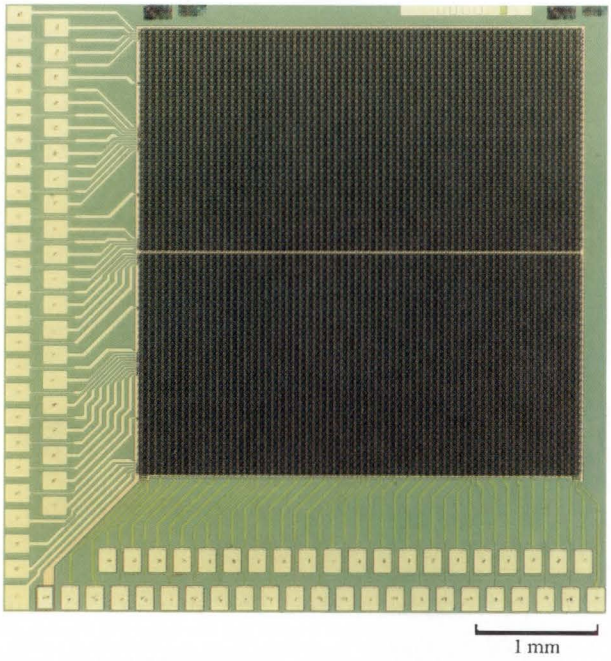


Fig. 22—Microphotograph of the fabricated 8K-bit memory cell array.

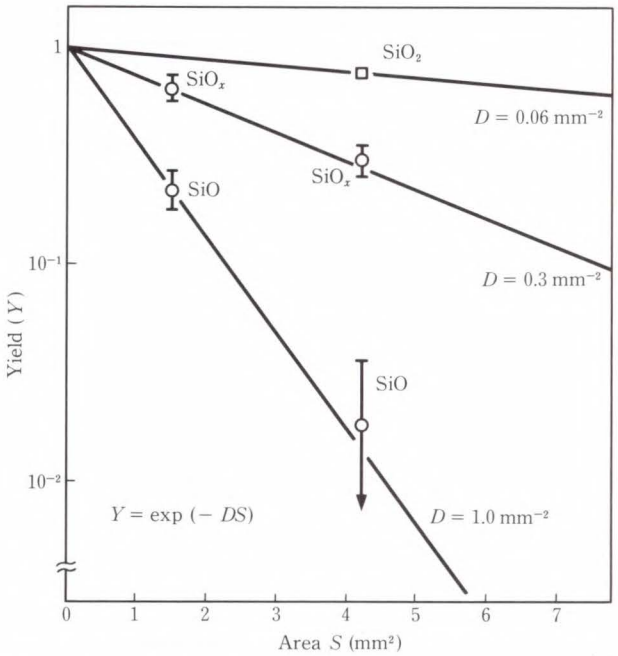


Fig. 23—Yield of the insulation checks versus the area of the insulators.

Table 5. Tested items in the prober test at room temperature

	Item	Content	Combinations of pads
Continuity check	SA	SQUID array	36
	CL	Control line	32
		Total	68
Insulation check	SG	SQUID array-GP	20
	CC	CL_i-CL_j	20
	SC	SQUID array-CL_i	48
	CG	CL_i-GP	12
		Total	100

Table 6. Yields for the tested items

Junction	Insulator	Yield (%) SA	CL	SG	CC	SC	CG
Nb/AlO_x/Nb	SiO_x	86	0	40	0	0	44
	SiO_2	94	12	77	17	15	83

Table 7. Yields for combinations of the tested items

Junction	Insulator	Yield (%) SA*	CL*	No. of perfect chips
Pb-Bi/Pb-In-Au	SiO_x	0	0	0
Pb-Bi/Nb	SiO_x	9	0	0
Nb/AlO_x/Nb	SiO_2	52	10	6

The continuity of the interconnecting wiring was checked for 68 combinations of selected pads, and the insulation of the insulating layers was checked for 100 combinations. Secondly, the I-V characteristics were measured for the chips selected through room-temperature testing. The yield of cells without shorted junctions was evaluated, as well as variations in the cells' I_c.

Table 6 lists the yields for checks made during the room-temperature testing. By using SiO_2, the yields are significantly improved. Figure 23 shows the yield of the insulation check plotted in terms of the area of the insulators sandwiched by two electrodes. Plots of SiO_2 were obtained for the Nb/AlO_x/Nb junctions, and plots of SiO_x and SiO were obtained for the Pb-Bi/Pb-In-Au junctions. The defect density (D) of the insulators was obtained from the slope of plots: 0.06 mm^{-2} for SiO_2, 0.3 mm^{-2} for SiO_x, and 1.0 mm^{-2} for SiO. These results are consistent with the breakdown voltages for SiO_2, SiO_x and SiO.

The total yield for the SQUID array and control line (SA* and CL*) are calculated by the yield obtained for related checks;

SA* = SA × SG × SC,

CL* = CL × CC × SC × SG.

Table 8. Failure rates of the Nb/AlO_x/Nb cells

Chip No.	No. of cells	No. of shorted cells	Failure rate (%)
1	8 192	2	0.024
2	8 192	0	0
3	8 192	4	0.048
4	8 192	0	0
5	8 192	0	0
6	8 192	2	0.024
Total	49 152	8	0.016

Table 9. Average cell failure rates for three kinds of the junction material

Junctions	No. of cells measured	No. of shorted cells	Failure rate (%)
Pb-Bi/Pb-In-Au	24 576	260	1.06
Pb-Bi/Nb	65 536	83	0.13
Nb/AlO_x/Nb	49 152	8	0.016

Table 7 lists SA* and CL*, along with the results for the Pb-Bi/Pb-In-Au and Pb-In-Au/Nb junctions. The yield for Nb/AlO_x/Nb junctions proved sufficiently high to obtain six perfect chips among the 64 tested.

The low-temperature characteristics were measured for the selected six chips. Eight cells were observed to be shorted in 49 152 cells (see Table 8). Thus, three of the six chips had no cell failure. The average cell failure rate was 0.016 percent. From these results, we estimated a practical yield of 27 percent for the 8K-bit cells.

Table 9 compares the cell failure rates for the three kinds of junction materials. The use of refractory Nb for the base and counter electrodes decreases the failure rate by one order.

Figure 24 shows the I_c distribution of 8 192 cells. All cells are within the range of ±13%, and the standard deviation of I_c distribution is 3.3 percent.

The evaluation of the 8K-bit cell array chips demonstrated that our standard process is feasible to Josephson integrated circuits including several thousand junctions.

4. Advanced processes

The standard process described in the previous chapter enables high-speed operation of Josephson logic and memory circuits described in Part II[19] to be verified. Josephson device potential is very high, however, current circuit design and process techniques remain relatively primitive when compared to semiconductor devices. To keep pace with semiconductor device development, Josephson circuit process technology must be further developed to achieve higher circuit density and enhance process reliability, for example. Four advanced process techniques have been recently developed: the fabrication of submicrometer junctions[92),93)] three-dimensional Josephson circuits[92),94),95)], anodization to characterize the thin tunneling barrier[96),97)], and bias-sputtered Nb applied to wiring[98)]. The microstructure of Nb/AlO_x/Nb junctions was also studied by using transmission electron microscopy (TEM)[99)].

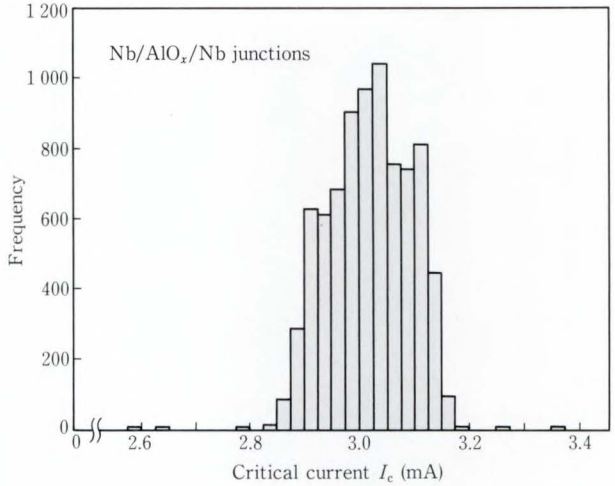
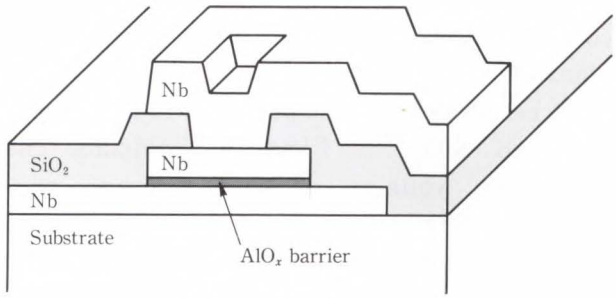


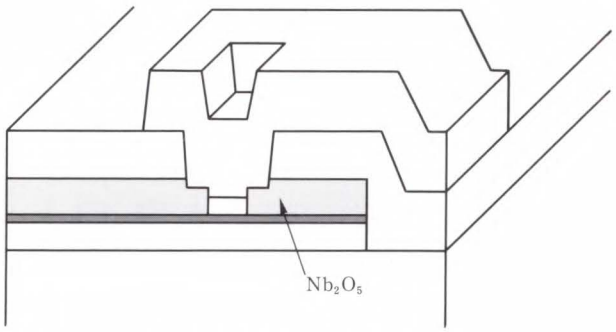
Fig. 24—I_c distribution for 8 192 cells on a chip.

4.1 Submicrometer junction

Figure 25 compares the cross section of the conventional junction with a new junction structure developed through miniaturization[92),93)]. A contact hole in the insulator is formed above the junction in the conventional structure. A submicron junction is difficult to make because the contact hole size must be smaller than the junction size. In the new structure, the junction area is defined by anodizing the Nb counter electrode. The anodized film thickness is *in-situ* monitored by the anodization profile methods[97)] described in Sec. 4.3. The anodized Nb, also

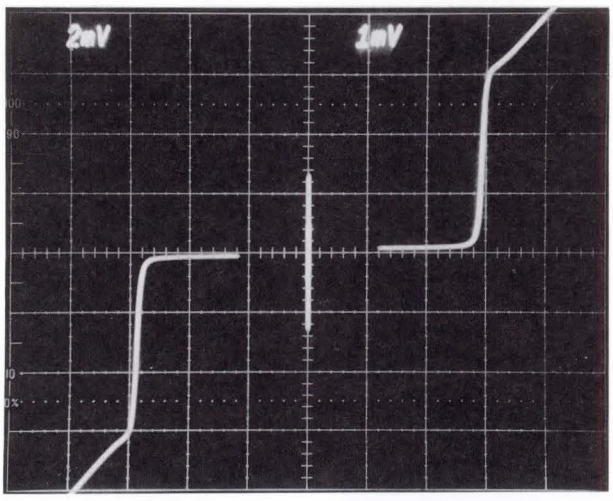


a) Conventional process



b) Self-aligned process

Fig. 25—Josephson junction.



Ver.: 20 μA/div Hor.: 1 mV/div

Fig. 26—I-V characteristics in the 0.7-μm-sequare $Nb/AlO_x/Nb$ junction.

acting as an insulator between the base electrode and wiring, enables formation of self-aligned contact holes. Thus, a small junction can be defined independently of the contact hole size.

Figure 26 shows an I-V characteristic for a

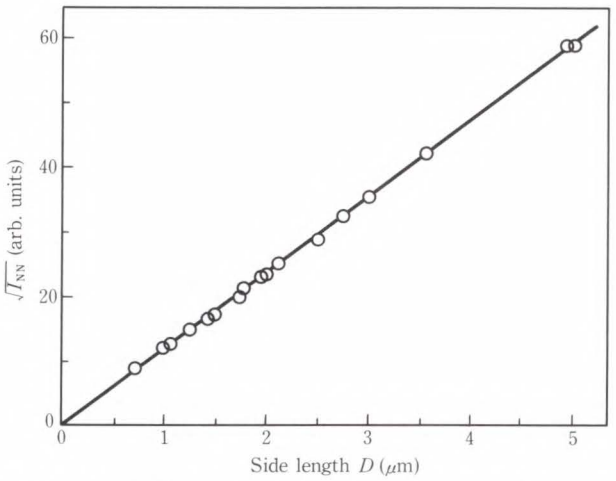


Fig. 27—Linearity of the tunneling current and the junction area. I_{NN} is the tunneling current at 4 mV, and D is the side length of square junctions.

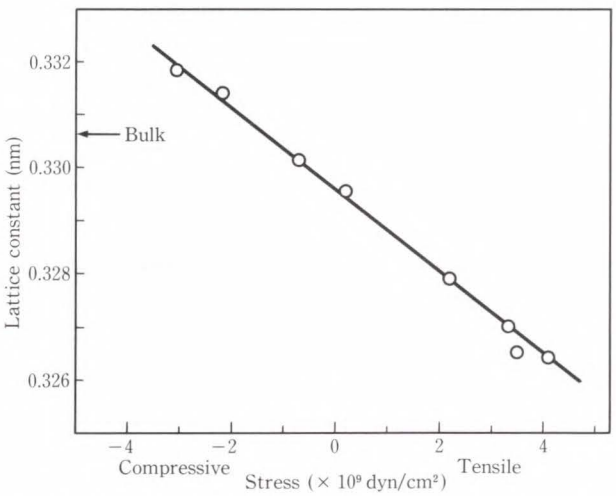


Fig. 28—Lattice constant versus stress of sputtered Nb[103].

0.7-μm-square junction. The junction has one excellent characteristic: V_m exceeds 30 mV. Here, electron beam lithography is used to make the resist pattern defining the junction area. The tunneling current at 4 mV is plotted against the junction size shown in Fig. 27. Linearity is observed for junction sizes of 0.7-5 μm. Pattern deviation in the junction size is estimated at only 0.02 μm.

To achieve high-quality submicron junctions, another technical problem had to be solved — the intrinsic stress in Nb film[100]. Sputtered Nb film reportedly contains stress apparently related to the junction characteristics[101]. Such stress

varies with the Ar pressure during sputtering (see Fig. 5). Stress-free Nb attained by optimizing the Ar pressure was used for junction electrodes to make submicrometer junctions[93]. The high-quality characteristics are due to the use of stress-free Nb electrodes.

The stress observed was related to the microscopic crystal structure of sputtered Nb. The lattice constant of Nb is plotted against the film stress in Fig. 28[102]. The linear relationship indicates that the crystal structure of Nb is distorted in proportion to the stress. How Nb stress deteriorates small-junction quality is not yet clear, but stress relaxation was observed during Nb film patterning[102]. As shown in Fig. 29, the lattice constant of compressive and tensile Nb clearly changes when the film is patterned, and shifts more markedly as the pattern size decreases. In contrast, stress-free Nb exhibits no change. These results suggest that film stress relaxes at the periphery in patterned Nb, thus adversely affecting small-junction quality.

4.2 Planarization and three-dimensional circuits

As mentioned before, the sputtered SiO_2 insulator helps improve the production yield of Josephson circuits. But, SiO_2 integrity is not yet sufficient to increase circuit integration to the VLSI level. This is mainly due to the poor step coverage of SiO_2 deposited on the patterned Nb. Planarizing the step of the underlying layer must be developed. One possiblity is to use bias-sputtered SiO_2[103]. Figure 30 compares the breakdown voltages of sputtered and bias-sputtered SiO_2 deposited on the patterned Nb[95]. The breakdown voltage, increased by a factor of 2 or 3, indicates the improved step coverage of bias-sputtered SiO_2. The production

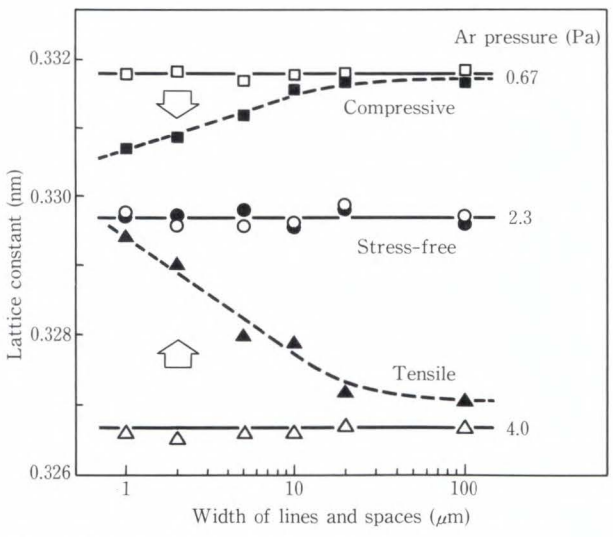


Fig. 29—Changes in the Nb lattice constant during patterning (Hollow symbols: before patterning, solid symbols; after patterning).

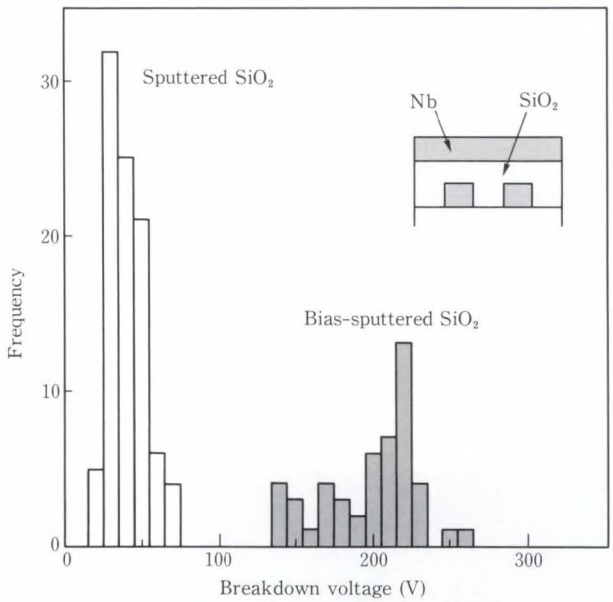
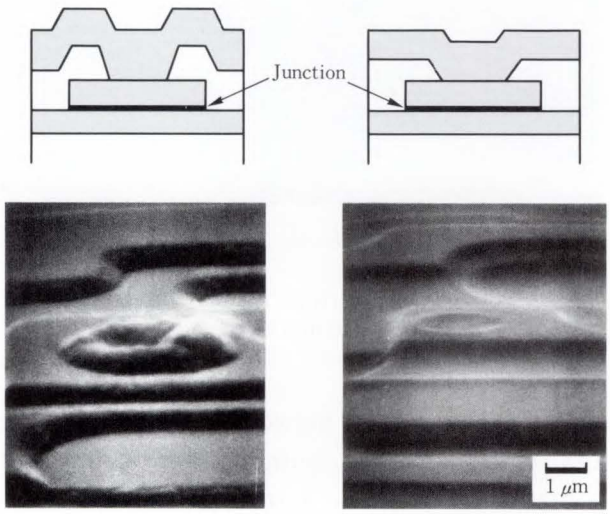


Fig. 30—Breakdown voltages of sputtered and bias sputtered SiO_2 films deposited on patterned Nb films.

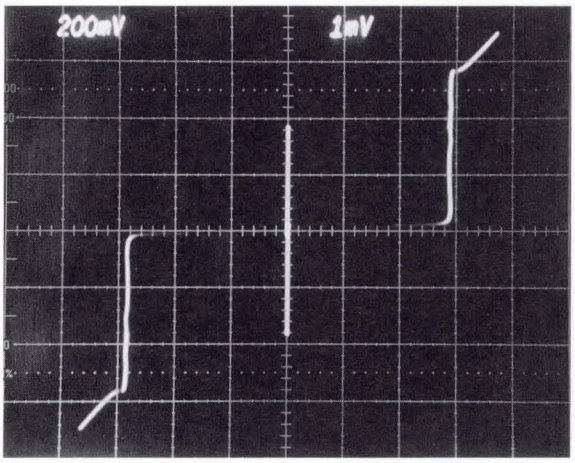


a) Sputtered SiO_2 b) Bias-sputtered SiO_2

Fig. 31—SEM photographs of junctions.

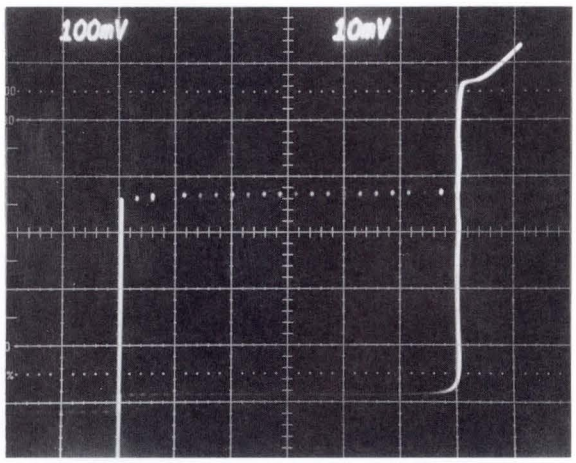
yield was verified as being improved by changing the insulator from sputtered to bias-sputtered SiO_2.

Figure 31 shows SEM photographs of junctions made with sputtered SiO_2 and bias-sputtered SiO_2; the steps of underlying Nb



Ver. : 2 mA/div Hor. : 1 mV/div

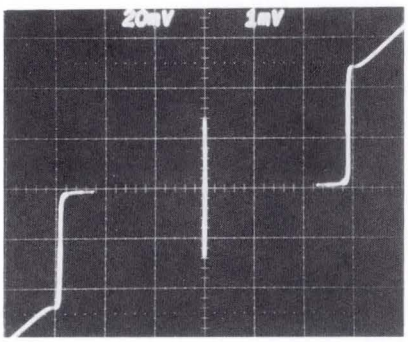
a) Single junction



Ver. : 1 mA/div Hor. : 10 mV/div

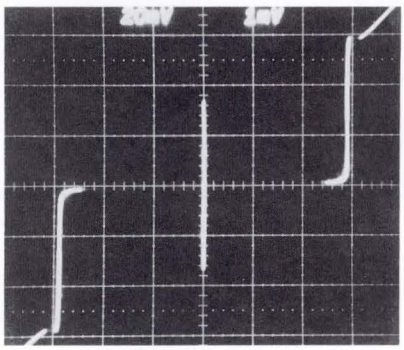
b) 20-junction chain

Fig. 32—I-V characteristics of junctions planarized with bias-sputtered SiO_2.



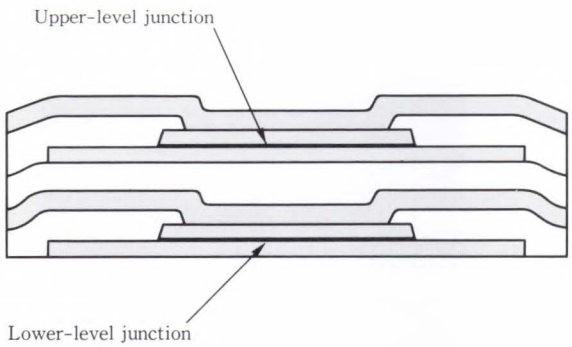
Upper-level junction

Ver. : 0.2 mA/div
Hor. : 1 mV/div

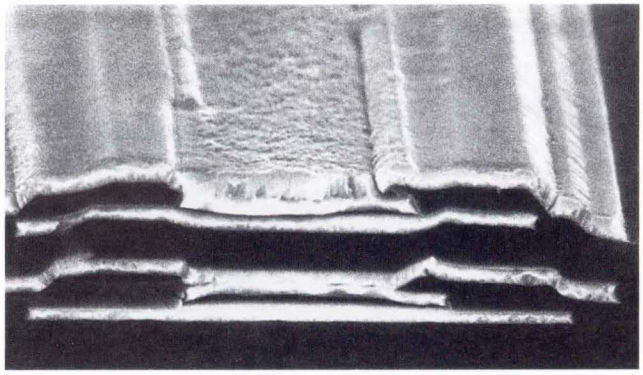


Lower-level junction

a) I-V characteristics



Cross section



SEM photograph

1 μm

b) Stacked junctions

Fig. 33—Vertically stacked junctions.

electrodes are planarized to obtain a smoother device surface. Figure 32 shows the I-V characteristics of the junctions planarized with bias-sputtered SiO_2. Although bias-sputtering accompanies additional ion bombardment, no deterioration was observed in the I-V characteristics.

We tried to stack other junctions above the junctions planarized by using bias-sputtered SiO_2[94]. Figure 33 shows a cross section of the vertically stacked junction, and the I-V characteristics for the upper-level and the lower-level junctions. By using 600-nm bias-sputtered SiO_2, high-quality characteristics could be obtained, even for the upper-level junctions.

Planarization increases the possibilities of developing three-dimensional Josephson circuits[17]. A gate array including 10 584 gates was fabricated as a test device for the first three-dimensional Josephson circuits (see Fig. 34). The upper-level and lower-level circuits both contain 5-K Josephson gates. Figure 35 shows an SEM photograph of the vertically stacked gate array. A common ground plane is sandwiched between the lower- and upper-level circuits. Lower-level gates are set upside down to the upper-level gates. The high quality of the 252-gate chains was verified for both the upper- and lower-level gates (see Fig. 36).

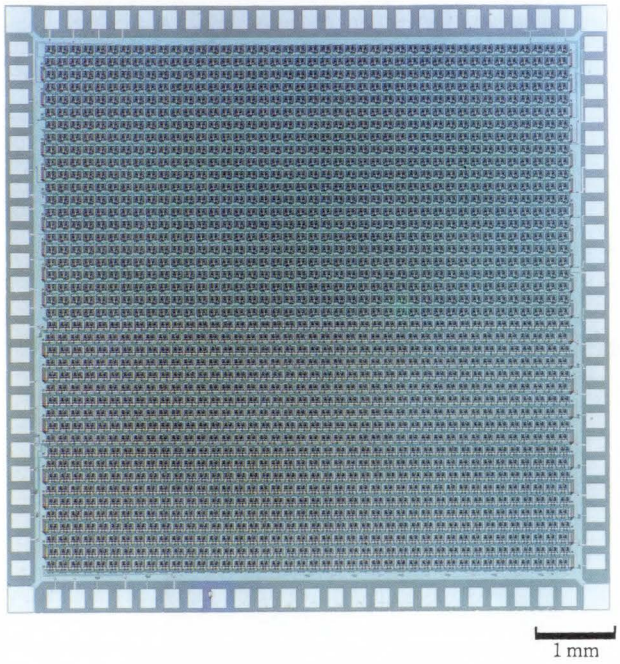


Fig. 34—Three-dimensional 10-Kgate array chip, 7.8 mm square. A 5 292 gates are integrated in both upper- and lower-level circuits.

4.3 Junction barrier diagnosis

Josephson junction characteristics largely depend on the formation of a uniform, high-quality tunneling barrier. Since the Josephson effect only appears at such low temperatures as 4.2 K, junctions cannot really be evaluated until processing is completed. It is also difficult to diagnose the thin AlO_x-Al barrier using conventional analytical methods because the barrier is very thin and sandwiched between two Nb electrodes. These are serious problems hindering the

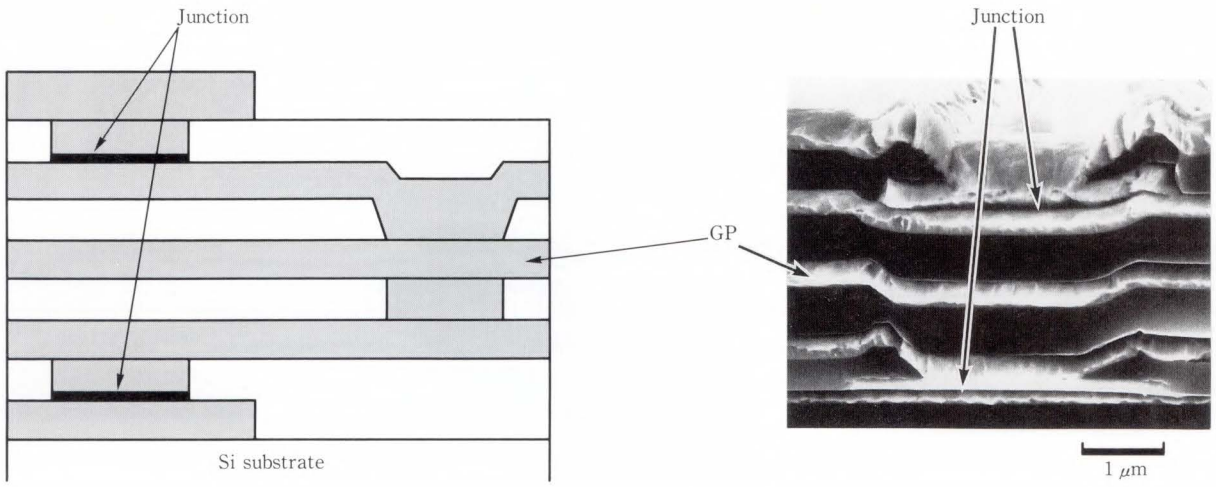
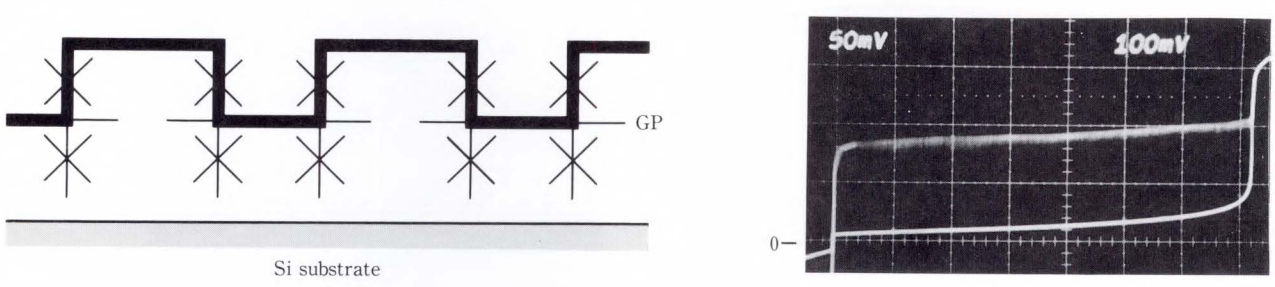
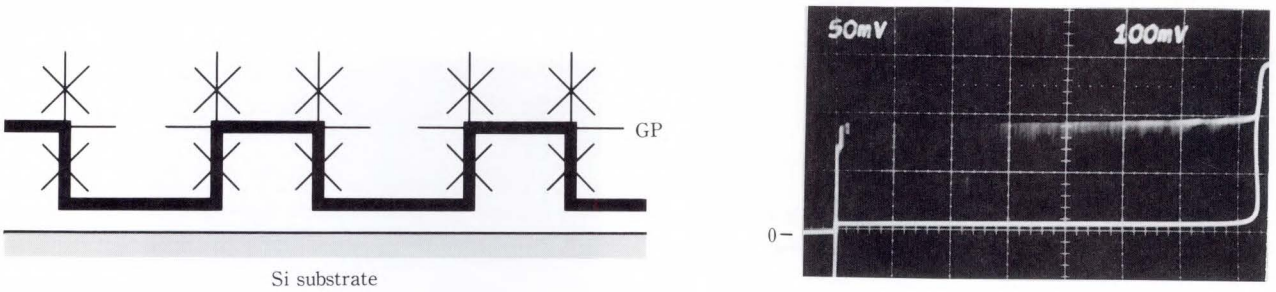


Fig. 35—SEM photograph of a vertically stacked gate array.



a) Upper-level circuit



Ver. : 0.5 mA/div Hor. : 100 mV/div

b) Lower-level circuit

Fig.36—Wiring diagram and I-V characteristics for 252-gate chain.

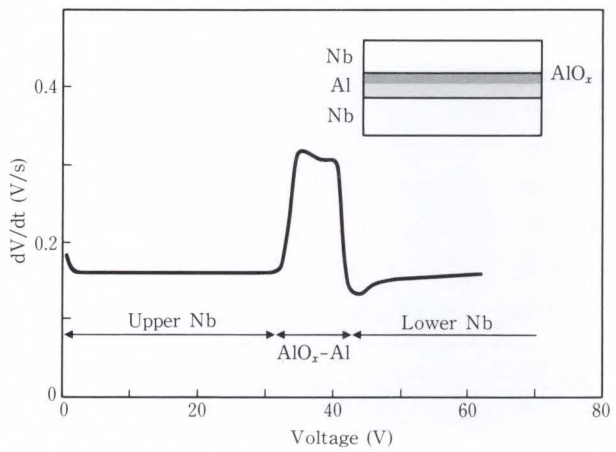


Fig. 37—Anodization profile for a Nb/AlO_x/Nb junction. The upper Nb and Al layers are 30 nm and 7 nm thick.

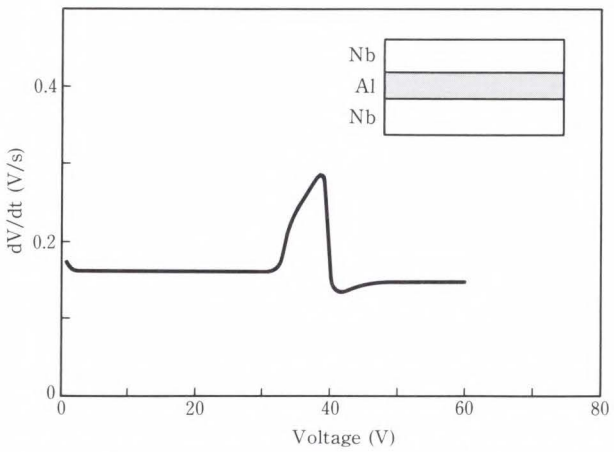


Fig. 38—Anodization profile for a Nb/Al/Nb structure.

development of improved Josephson process techniques.

An anodization profile[104] proposed for evaluating multilayered structures was applied to Nb/AlO_x/Nb junction structures[96),97)]. Many junction structures were studied by using the anodization profiles. Figure 37 shows an anodization profile for the Nb/AlO_x/Nb junction. The anodization proceeds in proportion to the voltage: 0.85 nm/V for Nb and 0.88 nm/V for Al. From the profile, the sharpness of interfaces in multilayered structures can be estimated within an accuracy of 0.5 nm. Such a precise analysis is not possible by using conventional methods of analysis.

Figure 38 shows a profile of the Nb/Al/Nb structure. Without the AlO_x, diffusion between the upper Nb and Al is clearly observed. As evident in Figs. 37 and 38, AlO_x prevents the

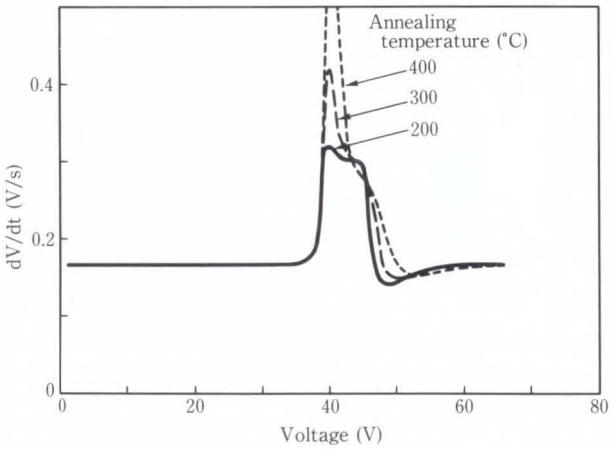


Fig. 39—Anodization profiles of $Nb/AlO_x/Nb$ junctions annealed for 30 min.

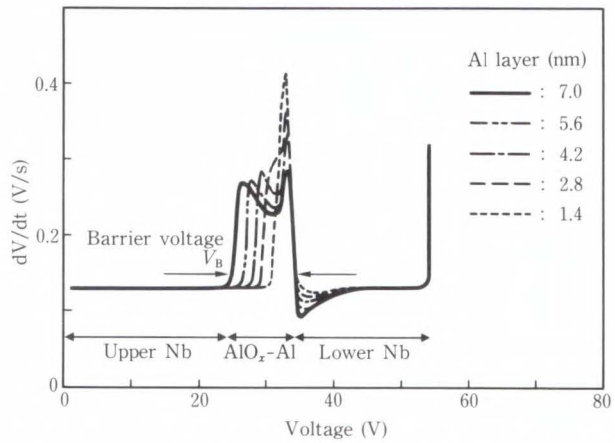


Fig. 41—Anodization profiles of $Nb/AlO_x/Nb$ junctions with five different Al thicknesses. The upper and lower Nb are 30 nm and 15 nm thick.

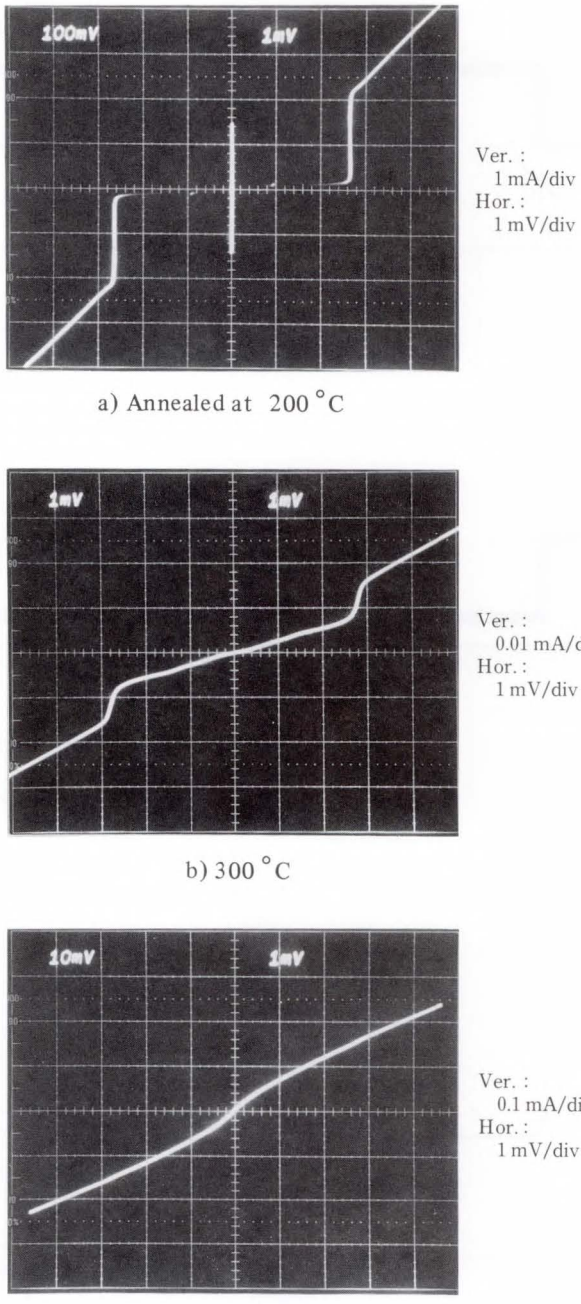


Fig. 40—I-V characteristics of junctions.

diffusion of Al and the upper Nb. In other words, the AlO_x barrier is not damaged during deposition of the upper Nb.

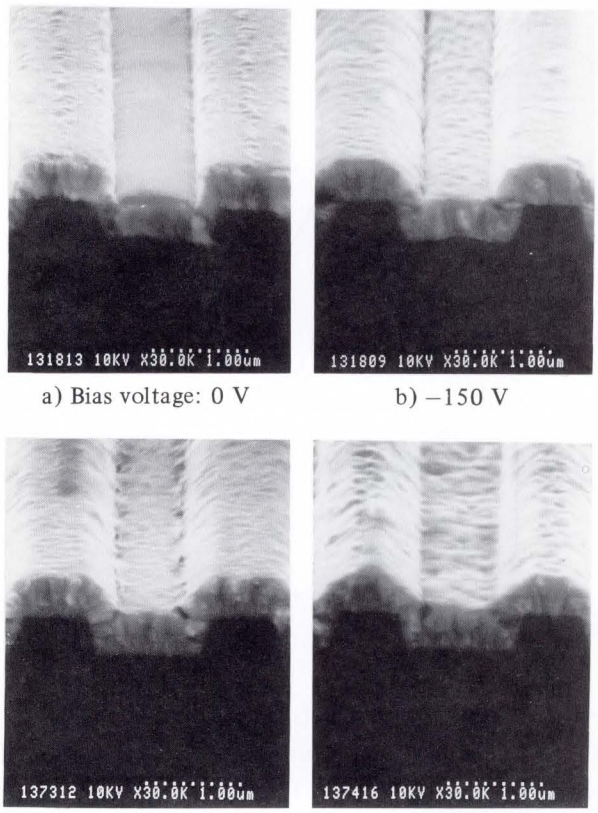
Figure 39 compares the anodization profiles for annealed junctions. By annealing, two changes occur in the profiles. One is the diffusion between Al and the lower Nb. The other is the increased peak height of AlO_x. Figure 40 shows the I-V characteristics of annealed junctions. Changes in the characteristics feature a reduced I_c and increased leakage current. Both changes are related to changes in the anodization profiles.

Figure 41 compares the anodization profiles with Al from 1.4 nm to 7.0 nm thick. Al barriers as small as a few nanometers thick can definitely be observed. From the barrier anodization voltage width (V_B), we can calculate the thickness of Al to be oxidized into AlO_x as about 1 nm[105].

The anodization profile has been verified as an effective tool for accurately analyzing junction barriers with high precision.

4.4 Bias-sputtered Nb for wiring

Using Nb wiring in Josephson circuits poses



a) Bias voltage: 0 V b) −150 V

c) −200 V d) −300 V

Fig. 42—Cross-sectional SEM photographs of Nb deposited on SiO_2 steps. Nb and SiO_2 are 500 nm thick.

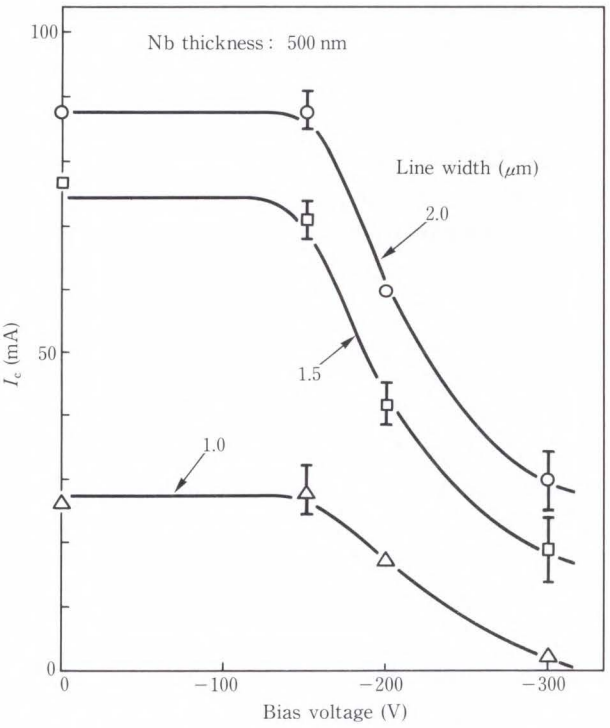


Fig. 43—Critical current I_c of bias-sputtered Nb films.

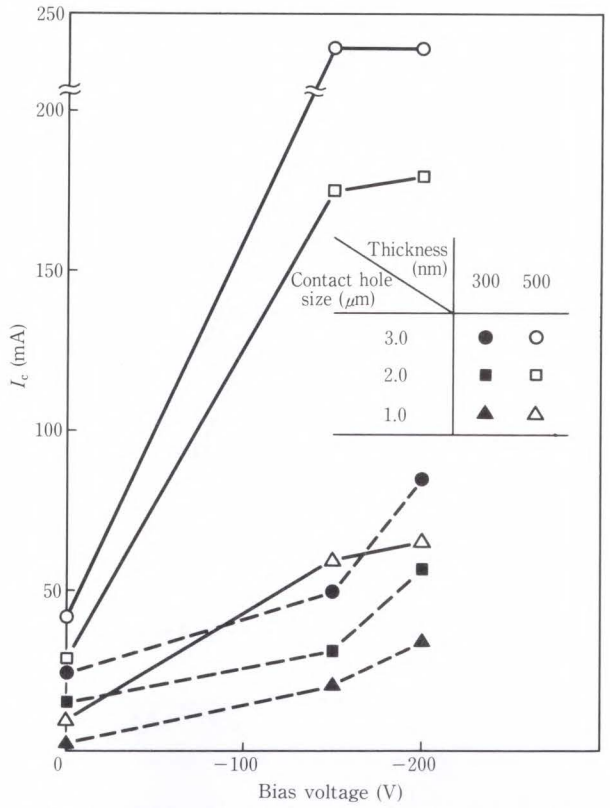


Fig. 44—Critical current I_c of contacts versus bias voltage during Nb sputtering.

two problems: reduced I_c of wiring at steps and after annealing. This is due to the effectively reduced thickness of Nb wiring running over the steps. To enhance Nb wiring reliability, we developed bias-sputtered Nb for wiring in circuits[98]. The step coverage of Nb is improved by adding the bias voltage during sputtering (see Fig. 42). Figure 43 shows the superconducting critical current (I_c) of bias-sputtered Nb film. For bias voltage less than −150 V, the deterioration in superconducting characteristics is negligible. Based on these rusults, bias-sputtered Nb was applied to the wiring used in Josephson circuits. We confirmed that the $Nb/AlO_x/Nb$ junction was not affected by using the bias-sputtered Nb. The characteristics of contacts were also improved before and after annealing. The wiring running over the steps also showed improvement in terms of their superconducting characteristics.

Figure 44 shows the I_c of contacts as a function of the bias voltage during wiring sputtering. The Nb base electrode is 200 nm thick, the SiO_2 insulator is 300 nm thick, and the Nb wiring is

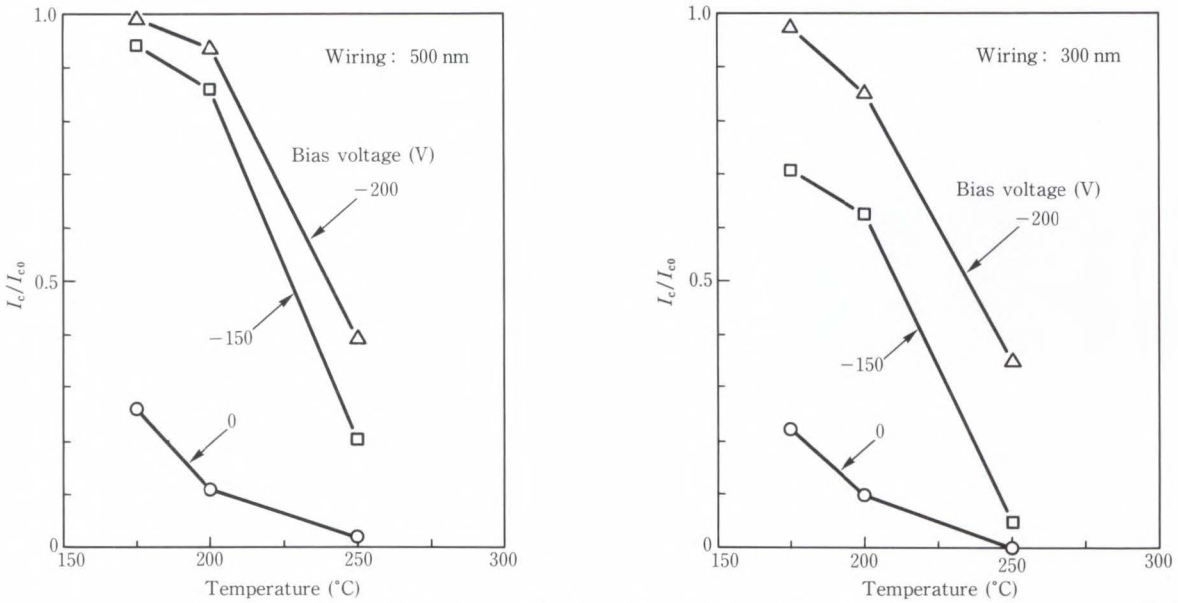


Fig. 45—Changes in I_c of contact after annealing.

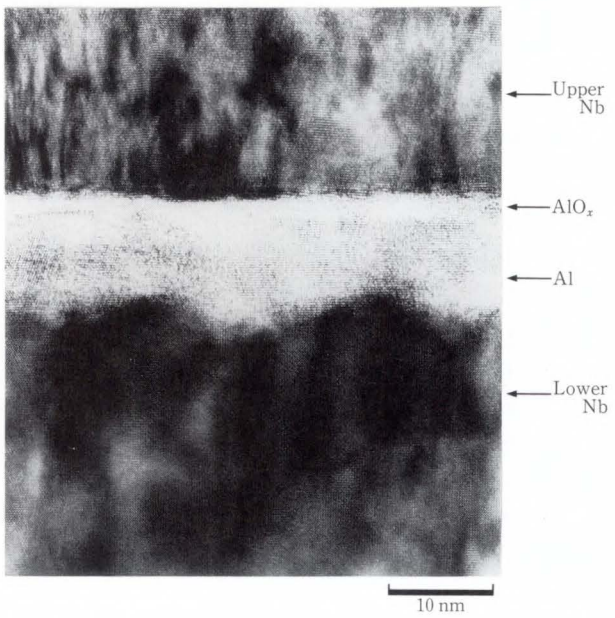


Fig. 46—Lattice image of $Nb/AlO_x/Nb$ junction structure.

300 nm to 500 nm thick. By applying bias voltage, I_c is increased by factors of 2 to 10. In addition, the contacts with bias-sputtered Nb were observed to be stable against annealing. Figure 45 shows changes in I_c after annealing. The I_c decreases with the annealing temperature. The contacts with bias-sputtered Nb, however, are much more stable than those with sputtered Nb. These improvements in contact characteristics before and after annealing are due to the effectively increased Nb thickness at the steps. Thus, the bias-sputtered Nb offers promise for wiring use in Josephson LSI application.

4.5 Cross-sectional TEM observation of junction structures

The microstructures of the $Nb/AlO_x/Nb$ junction were studied through cross-sectional TEM observation[99]. Figure 46 shows the lattice image of the $Nb/AlO_x/Nb$ junction structure. The upper and lower Nb are 20-200 nm, with Al 14 nm thick. From the lattice image, two interesting pieces of information were obtained. One is the crystallization of Nb and Al (thin Al as well as Nb are polycrystalline films with columnar structures). Most grains are oriented to a certain plane; Nb(110) planes are parallel to the substrate. The orientation of Nb(110) is consistent with the results obtained by X-ray diffraction. Al is also oriented to the (111) plane. Thus, the crystalline Al grown on Nb is considered critical to producing high-quality junctions. Also note that the upper Nb features a good crystalline structure just above the AlO_x barrier. This indicates that diffusion did not occur between the upper Nb and AlO_x barrier.

The other piece of information obtained concerns the Al and Nb interfaces. The interface between the lower Nb and Al is rough and wavy

due to the rough surface of the lower Nb. The other interface between the upper Nb and AlO_x is sharp and clear. This indicates that Al planarizes the lower Nb surface. Consequently, the planarized Al surface is considered essential to growing an AlO_x barrier without pinholes.

The TEM studies indicated that a material combination of Nb, Al and AlO_x is nearly ideal for the Josephson junctions.

5. Conclusion

This paper reviewed the fabrication technology developed in our laboratories for Josephson integrated circuits, and described the techniques used in the standard process for various circuits elements, $Nb/AlO_x/Nb$ junctions, SiO_2 insulators, Nb wiring, contacts, and Mo resistors. The key process to producing Josephson circuits is obtaining reliable and high-quality junctions. The characteristics of $Nb/AlO_x/Nb$ junctions were found to satisfy these requirements almost perfectly. Therefore, a combination of Nb, Al and AlO_x is deemed the best one for Josephson junctions. This paper also described how process techniques were verified as being practical for Josephson circuits that include several thousand junctions, based on the characteristics of the 8K-bit cell array chips fabricated for process evaluation. Without the process technology based on the reliable $Nb/AlO_x/Nb$ junctions, the ultra-high-speed operations recently achieved in Josephson integrated circuits would not have been possible. This paper also introduced the advanced process technology developed for future Josephson LSI application. These techniques satisfy demanding requirements to enhance circuit integration and improve process reliability even more.

Existing Josephson process technology was developed by several researchers. Although this technology may appear primitive when compared to semiconductor technology, the high-speed and low-power operation made possible when using Josephson logic and memory circuits are not possible with semiconductors. This verifies the potential application of $Nb/AlO_x/Nb$ Josephson junctions as digital devices in future high-speed computers. Based on the $Nb/AlO_x/Nb$ junction technology, Josephson computer development may now be seriously undertaken. To achieve this lofty goal, many technical breakthroughs in process technology must be made, particularly in terms of reliability and uniformity. Perhaps a greater research effort should be initiated in the field of superconductive electronics.

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Josephson Integrated Circuits II High-Speed Digital Circuits

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Josephson junctions with $Nb/AlO_x/Nb$ structures have made it possible to fabricate a variety of high-speed circuits, including an 8-bit digital signal processor and 4K-bit memory. These circuits operate at ultrafast speeds and consume less power than any high-speed semiconductor circuits. An interface circuit which issues the signal from Josephson circuits to semiconductor circuits has also been fabricated. In short, it is possible to fabricate all components necessary for constructing a Josephson computer. Now the high-speed operation of the Josephson computer must be demonstrated.

1. Introduction

The development of the niobium junction ($Nb/AlO_x/Nb$) for Josephson integrated circuits has changed what appeared to be a closed future to one with great potential. As described in the previous part of this paper[1], niobium junctions have solved most problems caused by the poor characteristics of lead-alloy junctions[2]. The niobium junction is very stable against thermal cycling and long-term storage. The scattering of critical current is quite small, and various circuits have been made possible with niobium junctions. These circuits operate much faster than those using lead-alloy junctions.

When using lead-alloy junctions, critical current was widely scattered and the integrated circuit speed was limited to that of the slowest junction. Josephson integrated circuits are inherently faster than semiconductor devices, although actually fabricated circuits were not as fast as expected. The inherent nature of Josephson junctions could not be fully utilized with lead-alloy junctions. The uniformity of niobium junctions has, however, made it possible to realize the potential performance capabilities of Josephson junctions, such as the fastest gate operating at a switching time of 1.5 ps/gate[3]. An integrated circuit with a few thousand gates operates on a clock frequency above 1 GHz[4),5]. High-speed logic circuits with a few thousand gates and 4K-bit memory[6] have been developed.

This paper describes the recent progress made in Josephson digital circuit development at our laboratories, using $Nb/AlO_x/Nb$ junctions. Chapter 2 describes the principles of circuit operation. Chapter 3 introduces the high-speed gate family based on modified variable threshold logic (MVTL)[7]. Chapter 4 covers the key techniques for fabricating high-speed circuits. Chapter 5 details a variety of high-speed logic circuits. Chapter 6 introduces the memory circuits. Chapter 7 describes the interfacing between Josephson and semiconductor circuits. Chapter 8 describes the progress being made in Josephson computer development. In conclusion, chapter 9 summarizes this paper.

2. Basic principles of Josephson digital circuits

The main features of the Josephson junction are high-speed switching (1-10 ps/gate), low-power consumption (1-10 μW/gate), and low-dispersion signal transmission (at about 100 μm/ps). Figure 1 shows the relationship between the switching time and power consumption for different high-speed logic gates, clearly indicating the high-speed, low-power capability of the

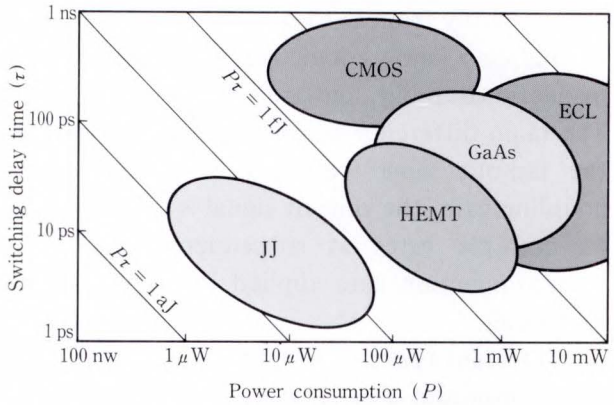
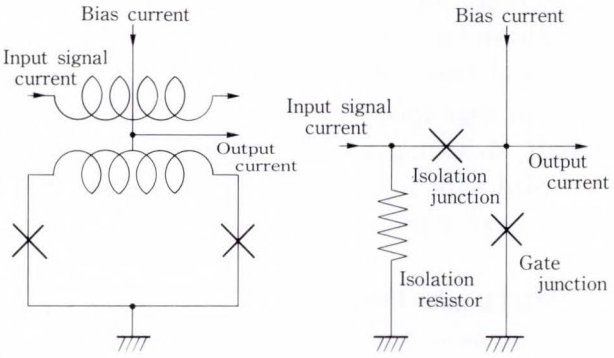
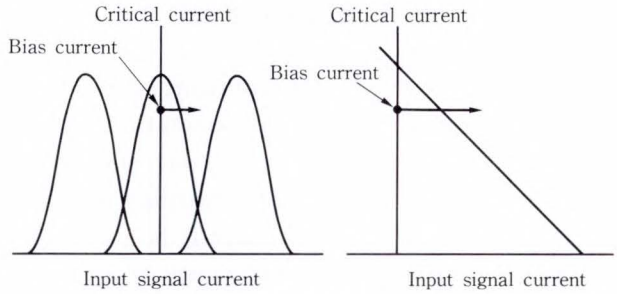


Fig. 1—Relationship of switching time and power consumption for different high-speed logic gates.



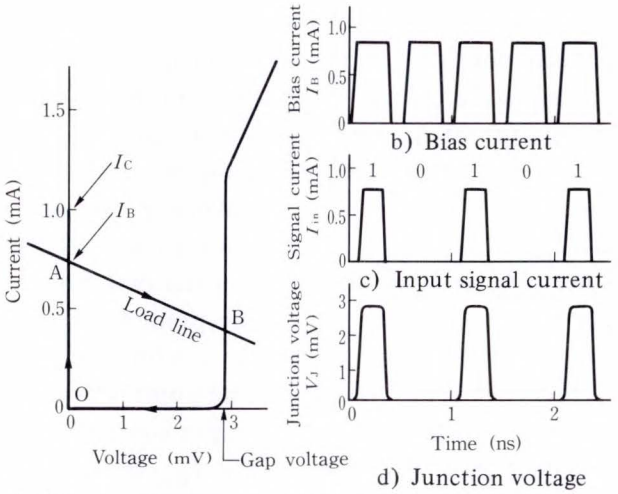
a) Magnetic-coupling gate b) Current-injection gate

Fig. 2—Equivalent circuits.



a) Magnetic-coupling gate b) Current-injection gate

Fig. 3—Threshold characteristics.



a) Current-voltage characteristics

Fig. 4—Computer simulated switching operation of Josephson logic gate.

Josephson logic gates. Due to these attractive features, Josephson junctions are expected to be used in ultrahigh-speed computers.

The Josephson logic gate operates differently than a semiconductor gate. The most important difference is that the Josephson gate switches in latching mode, while the semiconductor gate only changes its state when an input signal is applied. The Josephson gate, however, does not return to its initial state after the input signal is turned off, and is supplied by pulses rather than the dc power, with the frequency of the pulses determining the clock frequency. The supply current flowing through the gate is called bias current.

Josephson logic gates are classified into magnetic-coupling and current-injection. Figure 2 shows typical examples. Figure 3 shows the threshold characteristics of these gates. Figure 2a) shows the equivalent circuit of a magnetic-coupling gate with two junctions. Input signal current is applied to superconducting inductance coupled to another inductance loop in which two junctions are connected. The magnetic field caused by input signal current reduces the critical current of the gate {see Fig. 3a)}. When the bias current exceeds the reduced critical current, the gate switches from the superconducting state to the voltage state. Figure 2 b) shows the equivalent circuit of a current-injection gate. Input signal current is applied to the gate junction. The input current causes the gate junction to switch to the voltage state {see Fig. 3b)}, but the gate junction cannot isolate the input signal current from that output. Thus, an additional junction (isolation junction) and a resistor (isolation resistor) are connected to

the gate junction to prevent the input signal current from flowing to the output terminal.

Figure 4 shows computer-simulated waveforms of Josephson logic gate operation for the magnetic-coupling gate. Figure 4a) shows the operating point movement regarding the I-V characteristics. When bias current is applied to the gate, the operating point moves from origin O to point A, where the gate enters the standby state for switching to voltage state B.

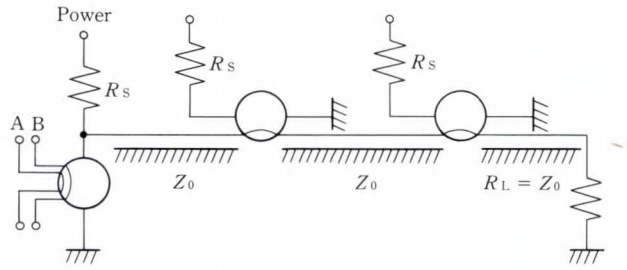
Figure 4b) shows the waveform of bias current I_B, 4c) input signal current I_{in}, and 4d) junction voltage V_J. When I_B is smaller than critical current I_C, the junction is in the zero voltage state (at operating point A). When input signal current I_{in} is applied to the gate, it generates a magnetic field that couples to the gate inductance and reduces I_C. When I_C becomes less than I_B, the gate switches to the voltage state (operating point B). After the switching to the voltage state, the operating point stays at B, even if I_{in} is removed. The gate can only be reset by decreasing I_B. The operating point goes from O to A to B to O. When the input signal is zero, I_C does not decrease below I_B, so nothing happens at A. O is only returned to when I_B is turned off. Consequently, the operating point moves simply from O to A to O.

Figure 5 shows logic circuits consisting of magnetic-coupling and current-injection gates. The main difference between these circuits is in the fan-out signal coupling. In the magnetic-coupling gate, the output signal is issued serially to multiple gates at subsequent stages. The current-injection gate applied its output signals in parallel.

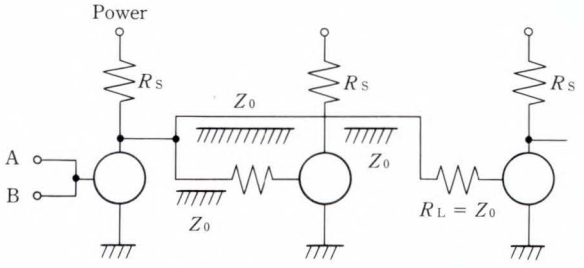
Different types of Josephson logic gates have been proposed (see Fig. 6)[8)-22)]. Some gates have been replaced by newly developed and improved gates. Josephson interferometer logic (JIL)[9)], Josephson threshold logic (JHTL)[12)], 4-junction logic (4JL)[16)], resistor coupled Josephson logic (RCJL)[20)], and modified variable threshold logic (MVTL)[22)] gates are now being used in high-speed circuits. Among these, the fastest switching speed (1.5 ps/gate) has been recorded with the MVTL OR gate[3)] as described in the next chapter.

3. MVTL gate family[22)-24)]

Josephson logic circuits usually consist of OR and AND gates operated in a dual-rail configuration[14)] because an inverter cannot be constructed without a timing signal. The

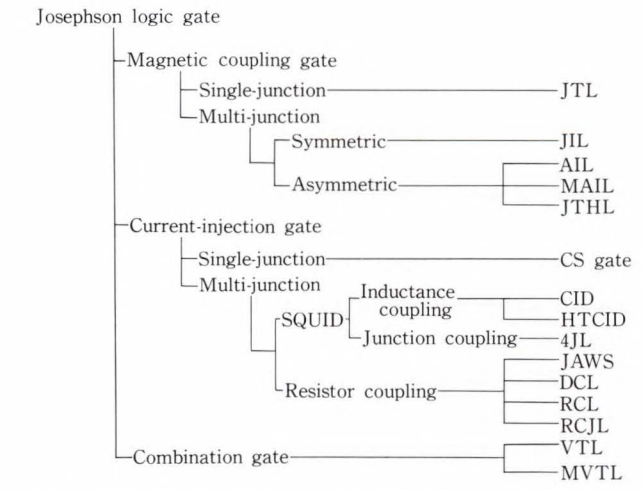


a) Magnetic-coupling gate



b) Current-injection gate

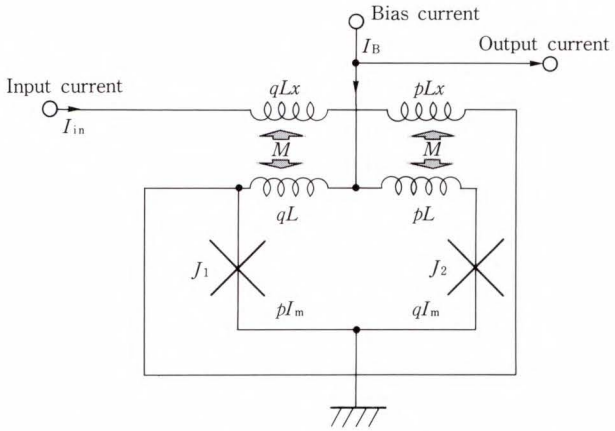
Fig. 5—Logic circuits.



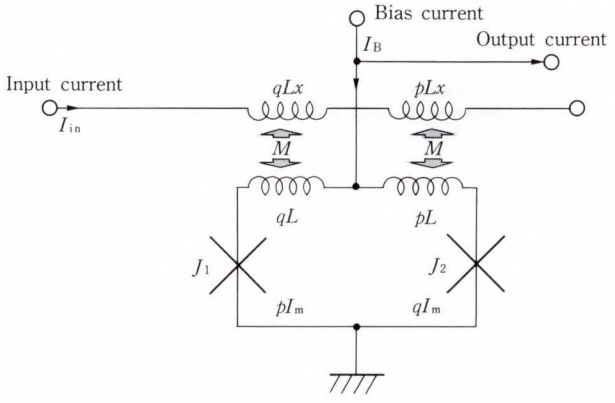
JTL : Josephson tunneling logic[8)]
JIL : Josephson interferometer logic[9)]
AIL : asymmetric interferometer logic[10)]
MAIL : magnetically-coupled asymmetric interferometer logic[11)]
JTHL : Josephson threshold logic[12)]
CS gate : current switched gate[13)]
CID : current injection device[14)]
HTCID : high tolerance current injection device[15)]
4JL : four-junction logic[16)]
JAWS : Josephson atto weber switch[17)]
DCL : direct coupled logic[18)]
RCL : resistor coupled logic[19)]
RCJL : resistor coupled Josephson logic[20)]
VTL : varible threshold logic[21)]
MVTL : modified variable threshold logic[22)]

Fig. 6—Classification of Josephson logic gates.

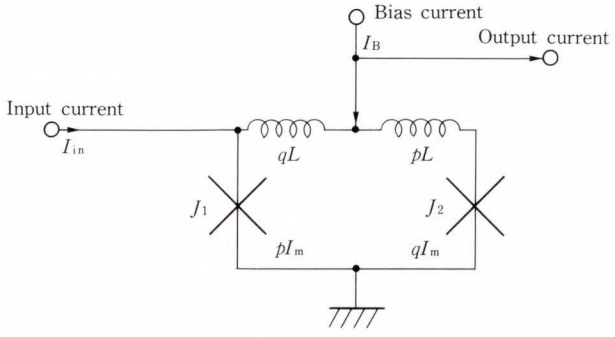
AND gate is usually driven by the output signals of OR gates because the AND gate cannot isolate the output signal from the input signal by itself. The MVTL gate family consists of OR, AND, and 2/3 majority (MJ) gates. The timed inverter (TI) is sometimes combined with an OR gate and another single junction. This chapter discusses the members of the MVTL gate family.



a) Basic structure for the MVTL OR gate, whose input current both couples to the interferometer magnetically and it is injected.



b) Gate with a magnetic coupling only



c) Gate with current injection

Fig. 7—Equivalent circuits for three coupling structures.

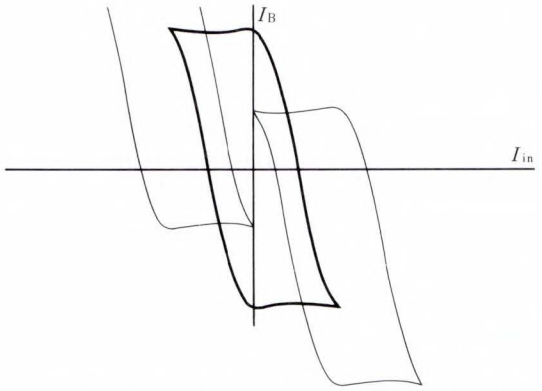
3.1 MVTL OR gate

The MVTL OR gate is the most important member of the Josephson logic gate family because it operates both as an OR gate and an isolator between input and output. The TI structure also includes an OR gate.

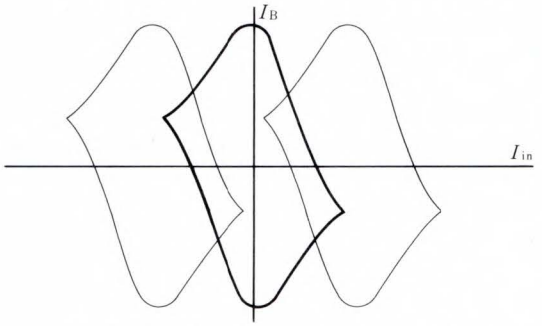
Figure 7a) shows the equivalent circuit of the basic MVTL OR gate. It is an asymmetric interferometer or 2-junction superconducting quantum interference device (SQUID), consisting of two Josephson junctions J_1 and J_2 and inductance L. The critical current of J_1 is pI_m and that of J_2 is qI_m, where $p + q = 1$ and I_m is the maximum supercurrent of the interferometer. Inductance L is magnetically coupled to control line inductance L_x through mutual inductance M. Bias current I_B is applied to the point between left branch inductance qL and right-branch inductance pL, thus ensuring that the upper limit of the bias current is at its maximum, I_m. The input signal current is fed through inductance L_x and applied to the interferometer. Thus, the signal current flows through magnetically coupled control line L_x and is applied to the interferometer. Figure 8a) shows the threshold curves of the gate shown in Fig. 7a). The bold line shows the main mode of threshold. The lighter lines show the modes including flux quantum Φ_0 ($= h/2e = 2.07 \times 10^{-15}$ Wb, where e is the electron charge and h the Plank's constant) in the superconducting loop.

Figures 7b) and 8b) respectively show a simple magnetic coupling structure and its threshold curve, while Figs. 7c) and 8c) show the current injection structure and its threshold curve for reference. As shown in the threshold curves of Fig. 8, the slope of the curve becomes steep when both magnetic coupling and current injection are made. The slope of the MVTL gate increases at a factor of about 1.6 so that a smaller signal can be used to switch the gate instead of only using magnetic coupling or current injection.

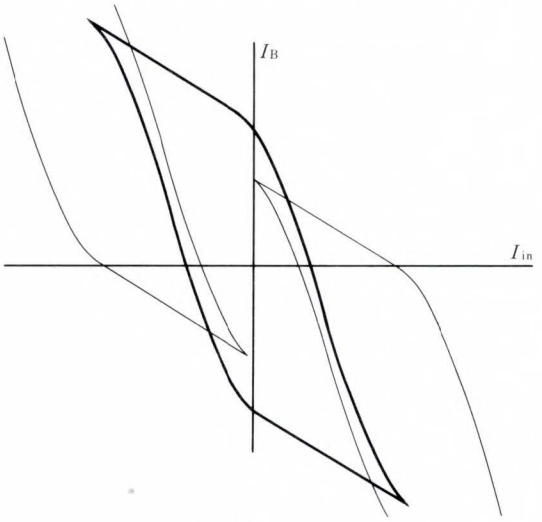
The gate shown in Fig. 7a) cannot isolate the input signal from the output one because the input signal current flows directly from the output terminal. Therefore, an extra junction J_3 and resistor R_i are added to the actual MVTL



a) Basic structure for the MVTL OR gate

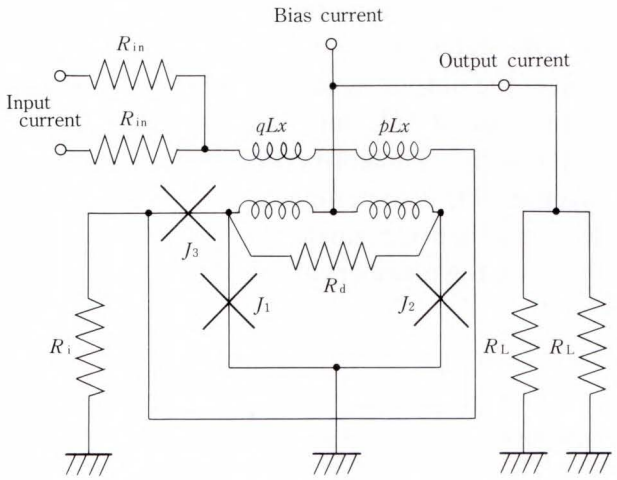


b) Gate with a magnetic coupling only

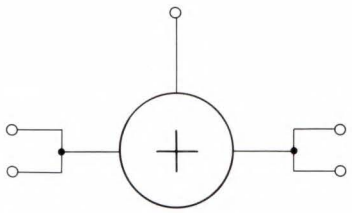


c) Gate with current injection

Fig. 8—Threshold curves for coupling schemes shown in Fig. 7. q/p is chosen to be 3 for the three structures.



a) Equivalent circuit



b) Its symbol

Fig. 9—MVTL OR gate.

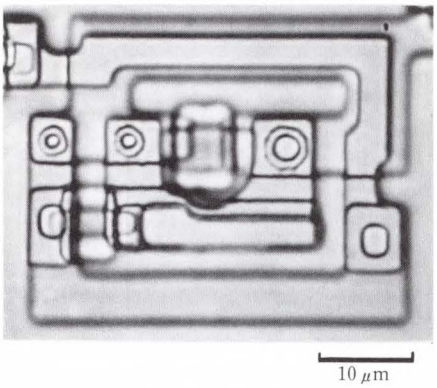
Table 1. OR gate design parameters

Parameter	Optimized value
I_m	0.4 mA
q/p	3
LI_m/Φ_0	1.0
L	5.2 pH
M	0.8 L
L_x	3-5 L
R_i	1 Ω
R_d	1.8 Ω

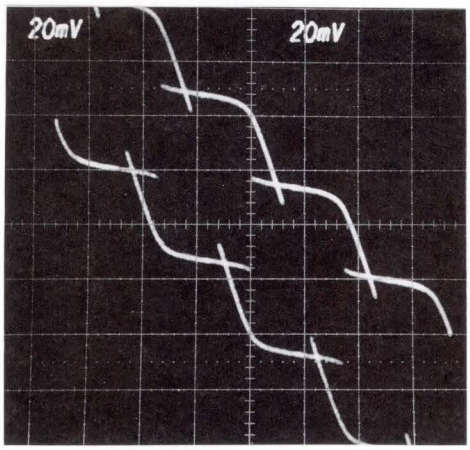
Φ_0: flux quantum (2.07×10^{-15} Wb)

OR gate as shown in Fig. 9. Input signals are added and fed through inductance L_x and injected into the interferometer through isolation junction J_3.

Junctions J_1 and J_2 switch due to the bias and input signal current being applied, while the operating point crosses the threshold value of the interferometer. The bias current then flows through J_3 and R_i to ground. J_3 is switched to the voltage state and most of the bias current flows to load resistor R_L. After the gate switches to the voltage state, the input current flows through R_i to ground, thus isolating input and output signals. Reference 22 details the MVTL gate design, and is not included here. Table 1 lists the optimized design parameters.



a) Photomicrograph



Ver.: I_B 0.2 mA/div Hor.: I_{in} 0.2 mA/div)

b) Experimentally obtained threshold curve
Curves should be compared with those of Fig. 8a)

Fig. 10—MVTL OR gate.

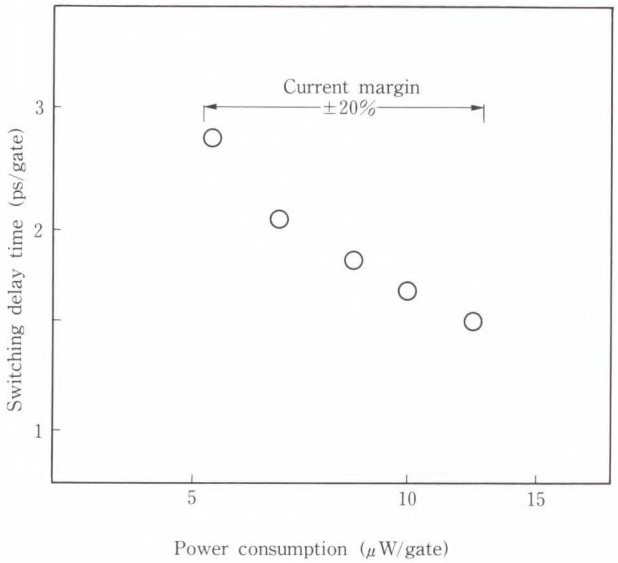


Fig. 11—Power-delay relationship of MVTL OR gate with a minimum junction diameter of 1.2 μm[3].

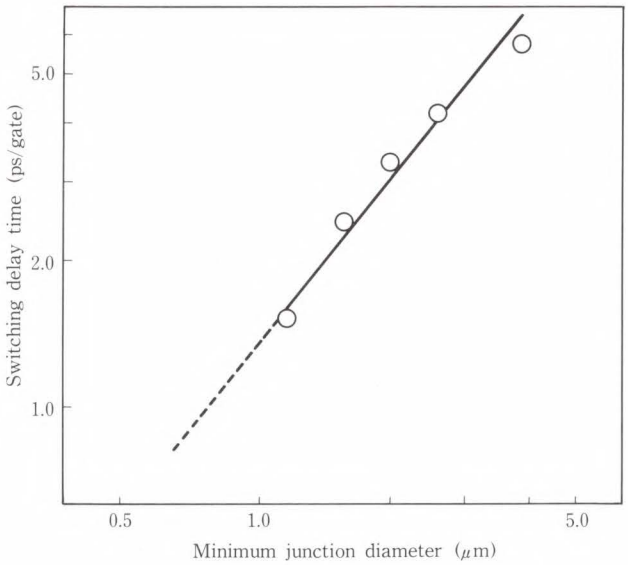
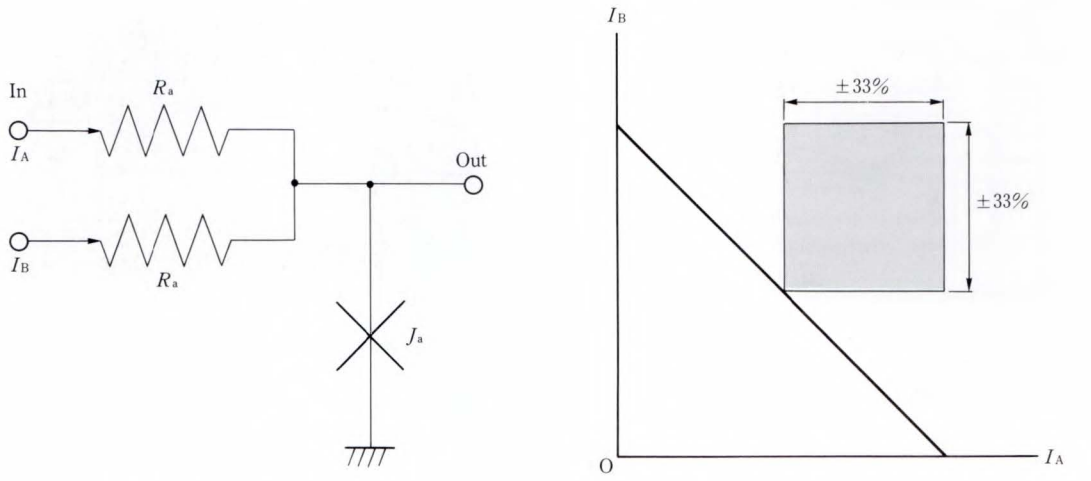


Fig. 12—Relationship between fastest gate delay and minimum junction diameter of MVTL OR gate.

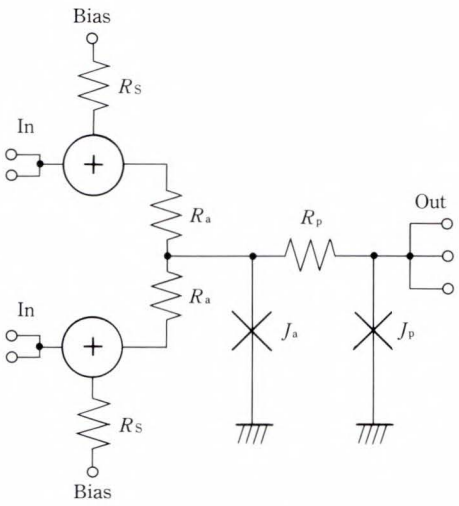
Figure 10 shows the OR gate and experimentally obtained threshold curve. This curve was obtained for a special gate without isolation junction J_3 and isolation resistor R_i as shown in Fig. 7a), and should be compared with the theoretical curve of Fig. 8a). The actual gate has three Josephson junctions J_1, J_2, and J_3 with respective diameters of 2.5, 4, and 2.5 μm. The gate with the minimum junction diameter of 2.5 μm is 31 x 41 μm^2. The switching delay, measured with a 100-stage gate chain, operates at 4.2 ps/gate[24]. Operating speed was increased by reducing the junction diameter. Five types of MVTL OR gates with different junction sizes have already been fabricated. The minimum junction diameter was changed from 4 μm to 1.2 μm. The fastest gate speed (1.5 ps/gate) was obtained using a gate with a minimum junction diameter of 1.2 μm[3]. This speed was achieved under a power consumption condition of 12 μW/gate. Figure 11 shows the power-delay relationship of this gate. It also shows that the 3 ps/gate speed can be achieved even during low-power operation at 5 μW/gate.



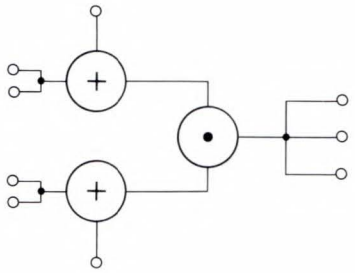
a) Equivalent circuit

b) Threshold curve for input currents I_A and I_B

Fig. 13—Single junction AND.



a) Equivalent circuit



b) Its symbol

Fig. 14—2OR-AND gate (unit cell).

Figure 12 shows the relationship between the fastest gate delay and minimum junction diameter for five MVTL OR gates with different minimum junction sizes[3),22)-27)]. Note that Josephson logic gates can attain a gate delay of less than 2 ps/gate without using submicron technology. This is an advantage of Josephson devices because submicron or even quarter-micron technology is essential for semiconductor devices in achieving speeds up to 10 ps/gate. Figure 12 suggests that a sub-ps/gate delay may be achieved by fabricating a gate with junctions 0.7-μm in minimum diameter.

3.2 MVTL gate family[22)-24)]

An AND gate is constructed with single junction J_a as shown in Fig. 13a). Critical current I_{J_a} of junction J_a is designed so that J_a can be switched at the summation of two input currents for total current exceeding critical current I_{J_a}. The operating margin for the input current is ±33% {see Fig. 13b)}. When the critical current varies ±20%, the operating margin becomes ±14%. To prevent the operating margin from decreasing, this AND gate receives no bias current and cannot provide isolation. As a result, the AND gate is always used behind the OR gate, called the 2OR-AND gate or unit cell, in the OR-AND combination shown in Fig. 14.

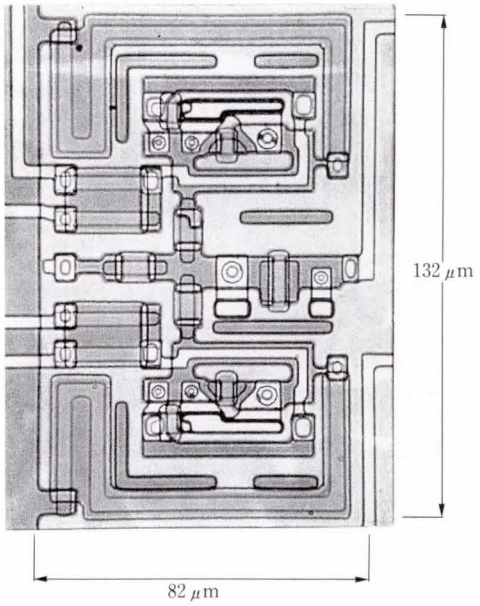


Fig. 15—Photomicrograph of 2OR-AND gate.

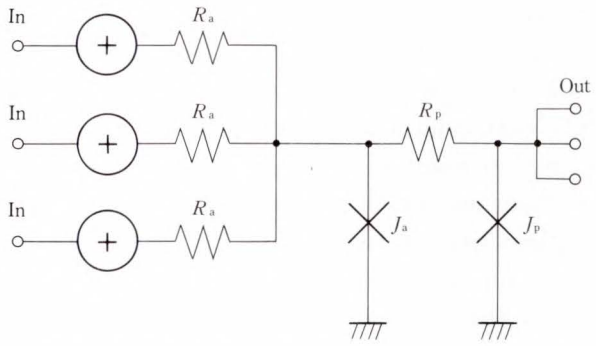


Fig. 16—Equivalent circuit of 2/3 majority gate.

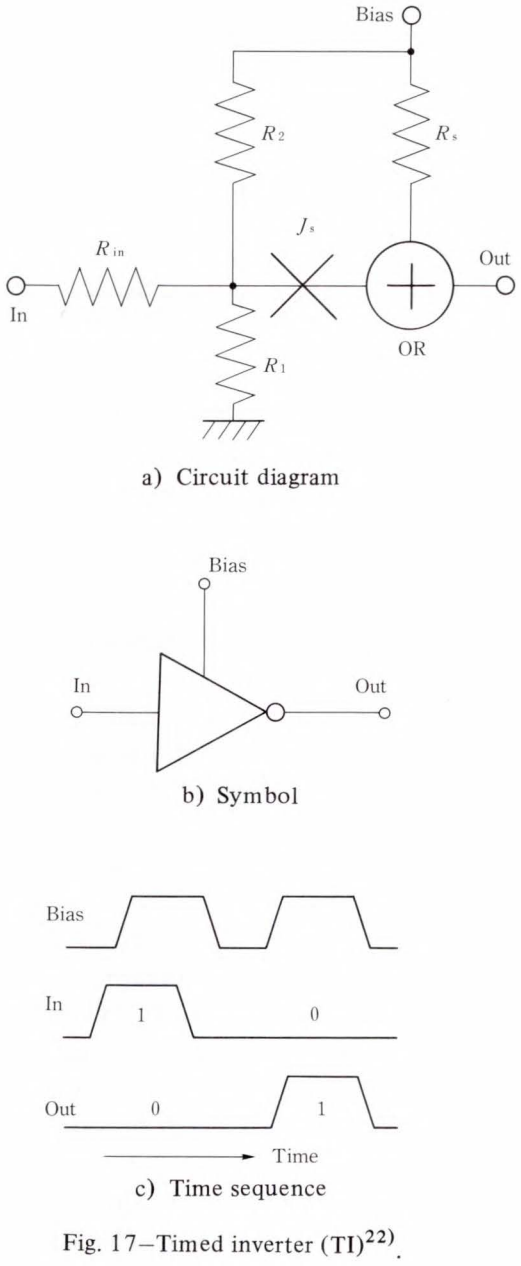


Fig. 17—Timed inverter (TI)[22].

To prevent J_a from being switched by leakage current from the next-stage gate, J_a has resistor R_p and a junction J_p. The critical current of J_p equals that of J_1 of the OR gate. This is small enough to minimize current loss through J_p when switching to the voltage state. Figure 15 shows a unit cell fabricated with a minimum junction diameter of 2.5 μm. The unit cell is 82 μm x 132 μm^2 in size with a gate delay of 11.5 ps[24]. The delay time for the gate with a minimum junction diameter of 4 μm is 16 ps[23].

In an LSI logic circuit, the carry signal of a full adder can only be obtained by using a 2/3 majority (MJ) gate. The 2/3 MJ gate in the MVTL gate family is basically the same as the unit cell, but has another OR gate connected at junction J_a. The 2/3 MJ gate is constructed by adding an OR gate (see Fig. 16). The operating speed of the 2/3 MJ gate was evaluated at 21 ps[23] for a minimum junction diameter of 4 μm.

The latching characteristics of the Josephson junction make it impossible to fabricate inverters. The Josephson logic gate requires a timing signal for inversion, and the inverter gate must be constructed with a timing signal. This type of gate is called a timed inverter (TI) (see Fig. 17)[22]. The TI operates correctly when signal current is applied before the bias current

Table 2. MVTL gate family performance

Gate \ JJ dia (μm)	4.0	2.5	2.0	1.5	1.2
OR	5.6	4.2	3.3	2.5	1.5
2OR-AND (unit cell)	16.0	11.5	–	–	–
3OR-AND (majority)	21.0	–	–	–	–

Unit: ps/gate or ps/unit cell

rises.

Table 2 summarizes the delay times obtained for different feature sizes[3),21)-27)]. The TI delay is not listed here because a timing signal is required and the gate delay depends on the signal timing.

4. Key techniques for fabricating high-speed circuits

Josephson devices operate more differently than semiconductor devices and require specific techniques to make full use of their performance potential. The fabrication of $Nb/AlO_x/Nb$ junction detailed in this paper[1)] was a measure breakthrough.

Another important technique is the high-speed gate with a sufficient operating margin for constructing high-speed circuits. This also requires a gate family consisting of several kinds of gates with different functions, such as the MVTL gate family described previously. The MVTL gate has a large operating margin and high sensitivity to input signal current, and can attain ultra-fast switching speed. The MVTL gate family facilitates the design of any kind of circuit because it enables a systematic circuit layout.

Two important techniques needed for high-speed circuits in addition to the $Nb/AlO_x/Nb$ junction and the MVTL gate family are dual-rail logic and the 3-phase powering system.

4.1 Dual-rail logic

In semiconductor devices, output 0 is easily obtained for an input of 1. In contrast, the Josephson device outputs 1 when 1 is input because it has no inversion function. Thus, semiconductor circuits cannot simply be replaced by Josephson devices. This requires special circuits and what is called dual-rail logic[14)].

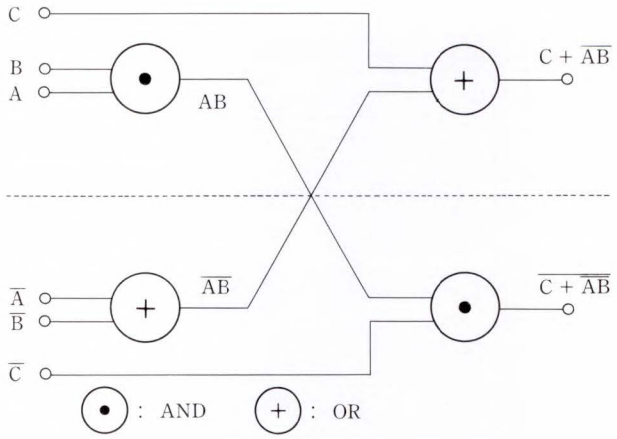
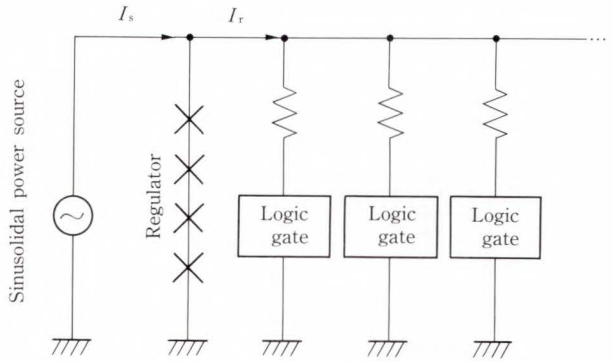


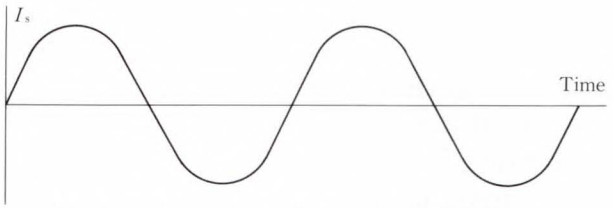
Fig. 18—Circuit construction of $C + \overline{AB}$.

True and complementary signals are always provided for the dual-rail logic circuit. For example, $C + \overline{AB}$ is constructed with dual-rail logic (see Fig. 18). Only true signals A, B, and C are used on the upper plane of the circuit, while only complementary signals $\overline{A}$, $\overline{B}$, and $\overline{C}$ are used as input on the lower plane. Circuits for the upper and lower planes are set in a true and complementary relationship, that is, an OR gate is used on the upper plane instead of an AND gate on the lower plane and vice versa. When a complementary signal is needed in the true circuit, it is taken from the complementary circuit. Any circuit can be made without using an inverter. Even though dual-rail logic doubles the number of gates, it is usually used in Josephson LSI circuits due to the simple circuitry.

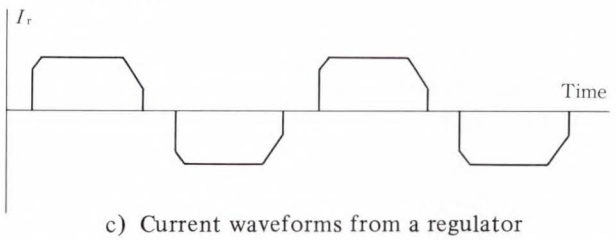
A TI gate is sometimes used because a complementary signal is necessary for an input signal, even in dual-rail logic. We usually use TI gates at the leading edge of the bias current, and use 3-phase powering as described in the next section. The TI gates can be used three times in one clock cycle. The TI gates used in dual-rail logic circuits do not double the number of gates because only true signals are needed for output in each powering stage. Combining dual-rail logic and TI gates requires about 1.5 times as many gates as required by semiconductor circuits.



a) Circuit diagram



b) Current waveform from a sinusoidal current source

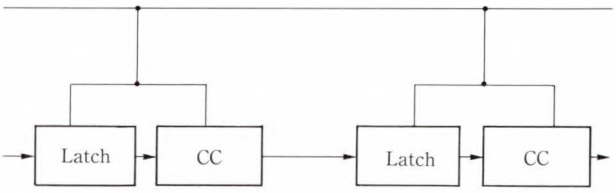


c) Current waveforms from a regulator

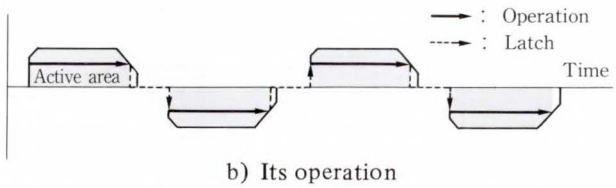
Fig. 19—Alternate current powering with single-phase power supply.

4.2 Three-phase powering system

Josephson logic gates operate in latching mode, with the gate switching to the voltage state only when an input signal is applied. Once switched, the gate does not return to the zero-voltage state, even after the input signal is turned off. Therefore the power supply driving Josephson logic gates must be turned off to reset the gate in each clock cycle. Alternate current power is used for this purpose[28)-30)]. Sinusoidal ac power is supplied from an external source and is reformed as trapezoidal ac power by using a regulator circuit. The regulator usually consists of four Josephson junctions connected in series. Figure 19 shows how the regulator usually consists of four Josephson junctions connected in series. Figure 19 shows how the regulator generates the clipped top waveform of the bias current. Logic operation is executed



a) Circuit configuration with latch circuits



b) Its operation

Fig. 20—Alternate current powering system with single-phase power supply.

in the flat part of the source power.

Due to symmetrical current-voltage characteristics of Josephson junctions, positive and negative bias current can be used for logic operation. A latch circuit is used to retain information when bias current changes from positive to negative or vice versa[31)-34)]. The information is stored in the form of persistent current in the superconducting loop without any bias current.

Figure 20 shows the circuit construction with an ac power supply. The conventional combinational circuit (CC) is accompanied by a latch circuit. The information from the previous clock cycle is stored in the latch when ac bias current changes its polarity, and is transferred to the adjacent CC during the changing period to the next clock cycle. The latch consists of superconducing flip-flops that temporarily store the information. There are other problems in using ac power, such as CCs not being activated when power is in transition. To increase the clock frequency, we must reduce the transient time. This reduction would result in a malfunction caused by punch-through[35)-37)], however. Another problem is posed by the polarity of bias current being reversed in each clock cycle so that the information stored in the latch cannot be directly used in the next CC. In addition, a latch consisting of magnetically coupled devices would increase the size of the circuit.

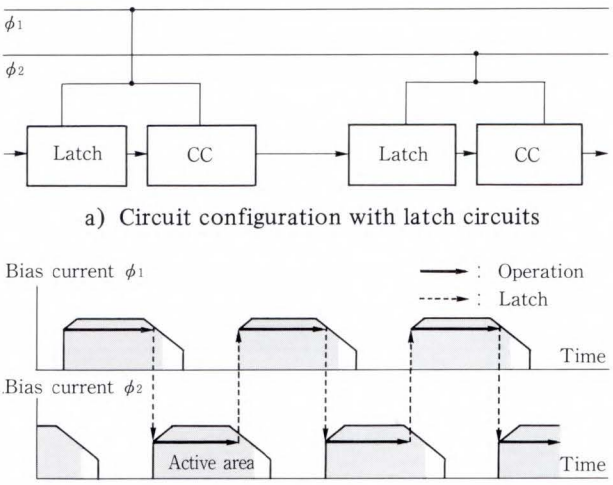


Fig. 21—Two-phase monopolar powering system.

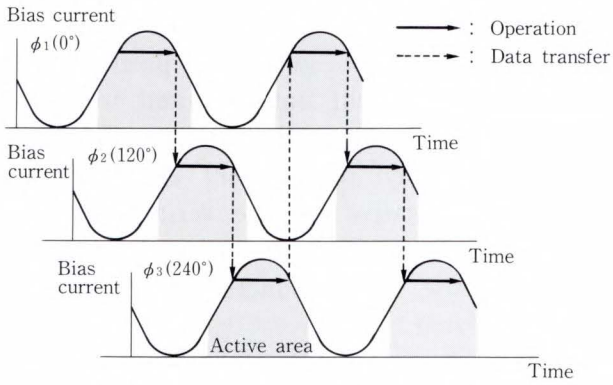


Fig. 22—Logic operation with three-phase sinusoidal power supply.

Different types of multi-phase monopolar powering have been proposed to resolved the problems encountered in ac or bipolar powering. Figure 21 shows 2-phase monopolar powering[38]. The two regulated monopolar power supplies ϕ_1 and ϕ_2 are 180° out of phase. At the leading edge of ϕ_1, the latch in phase ϕ_1 reads the output of the CC in phase ϕ_2 and information is transferred to the CC in ϕ_1. Logic operation is executed under ϕ_1 and terminated before ϕ_2 begins to rise. After output is realized by the latch in ϕ_2, the CC in ϕ_1 and the latch in ϕ_1 enter the idle state when ϕ_1 is off. This powering system has several advantages. Logic operation is continued alternately in ϕ_1 and ϕ_2. The shaded areas in Fig. 21 indicate the active times when logic operation is executed. In this way, there is

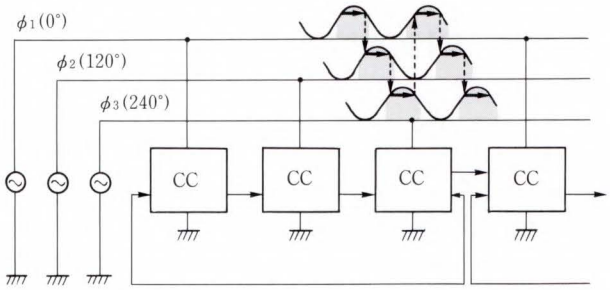


Fig. 23—Three-phase monopolar powering with sinusoidal waves.

no idle time so that the system can operate faster than with ac power. The latch can consist of current-injection gates because the polarity of bias current is not reversed and the latch can be made smaller.

We have developed a 3-phase powering system. Three sinusoidal waveforms with dc offset are used, with each being 120° out of phase. Figure 22 shows the logic operation using this system. When logic operation is executed and completed in phase ϕ_1, data is transferred to the circuits driven by phase ϕ_2 and processed there. After ϕ_2 is completed, data is sent to the circuits driven by ϕ_3. Data is retransferred from circuits in ϕ_3 to those in ϕ_1. This completes one clock cycle in 3-phase powering. This system requires no latch because processed data is transfeered as ϕ_1, ϕ_2, ϕ_3, ϕ_1, ..., without wasting time. In three-phase powering, racing does not occur. This is a significant advantage over 2-phase powering. Figure 23 shows that the circuit configuration with 3-phase sinusoidal powering. The TI can also be used more frequently than in 2-phase powering. The input signal must be followed by bias current in the TI. This requirement is satisfied at every rise of the next clock cycle power.

The 3-phase sinusoidal waveform has an important effect not possible with the single-phase or multi-phase trapezoidal waveform. The 3-phase sinusoidal waveform reduces deviation in the ground voltage, which is vital to the high-speed operation of Josephson circuit. Bias current flows through contacts and is terminated at the common superconducting ground plane. If the total current through

the ground plane changes drastically over time, a time variation is caused in the voltage level of the ground plane, which, in turn, may cause a logic gate malfunction because the output voltage of the Josephson logic gate is only 2.8 mV. The clock frequency is on the order of 1 GHz, and the total supply current for the chip is about 1 A. The time variation of ground voltage V_{gr} is given by $L\,(dI/dt)$, where L is stray inductance and I is supply current. For L of 50 pH, a typical value of flip-chip bonding, V_{gr} becomes 0.3 V. This is much larger than the signal voltage of 2.8 mV from the Josephson circuits. By using the 3-phase sinusoidal waveform, however, the total current to the ground plane does not change with time. As a result, the ground level is not affected by power supply changes. This is a significant advantage of the high-speed operation of Josephson logic circuits. Powering with a sinusoidal waveform results in a duty ratio of active time a little less than that with trapezoidal waveforms, although the duty ratio is only reduced by about ten percent, and is not critical to circuit operation.

5. High-speed logic circuits

Various high-speed Josephson LSIs have been recently developed. These include a 4-bit processor[39], a 4-chip 4-bit computer[40], and 1 K-bit memory[41], all using niobium junctions.

The MVTL gate family has been used to fabricate various logic circuits. These include an 8-bit shift register[42], 16-bit arithmetic logic unit (ALU)[43], 4-bit microprocessor[44], 4-bit processor[4], and 8-bit digital signal processor (DSP)[5]. The following sections describe the performance of these circuits.

5.1 Shift register[42]

We designed an 8-bit shift register with SHIFT, LOAD, HOLD, and CLEAR functions. Figure 24 shows a circuit diagram of the 1-bit shift register. The OR, 2OR-AND, and TI symbols are defined in Figs. 9b), 14b), and 17b).

$S \cdot DS + L \cdot DL + H \cdot T_{\phi_3}$ denotes the output of the 1-bit shift register, and S, L and H denote

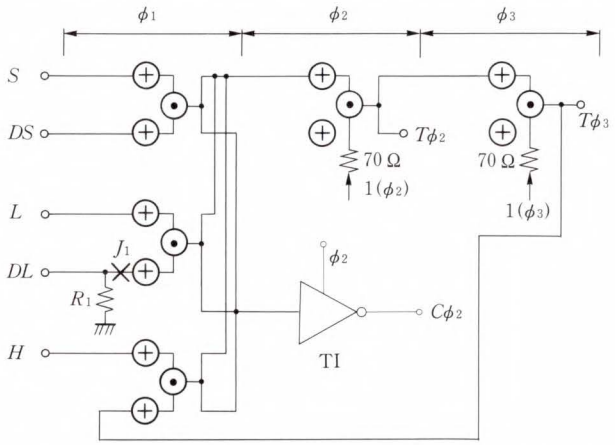


Fig. 24—One-bit shift register circuit. Input resistor R_{in} for the OR gate and TI and supply resistor R_s for the OR gates are omitted.

the control signals used for SHIFT, LOAD, and HOLD. DS and DL denote the data used for SHIFT and LOAD. T_{ϕ_3} denotes the output data for the 1-bit shift register from the preceding ϕ_3 phase power clock, and is used for HOLD. Such AND operations as $S \cdot DS$, $L \cdot DL$, and $H \cdot T_{\phi_3}$ are executed using 2OR-AND gates powered by ϕ_1 (see Fig. 24).

In the 2OR-AND gates powered by ϕ_2 and ϕ_3, one connecting line of each AND gate is not connected to the OR gate, but is connected through a 70 Ω resistor to the power bus. These AND gates are used to amplify the current for a fan-out of 2.

A circuit consisting of resistor R_1 and Josephson junction J_1 makes a 1-shot pulse by switching J_1 when the data for LOAD DL rises. If the pulse width of DL is longer than one clock cycle, this circuit transfers the data for only one clock.

This shift register outputs T_{ϕ_2}, T_{ϕ_3}, and C_{ϕ_2}. T and C denote true and complement. ϕ_2 and ϕ_3 represent their power phases. Other power phase output can also be easily obtained by slightly modifying the circuit.

Figure 25 shows the 8-bit shift register, which consists of the eight 1-bit shift registers shown in Fig. 24. When 1 is applied to S, the contents of each 1-bit shift register are transferred to the next register to the right. The DS of each bit is given by output T_{ϕ_3} of the preceding bit.

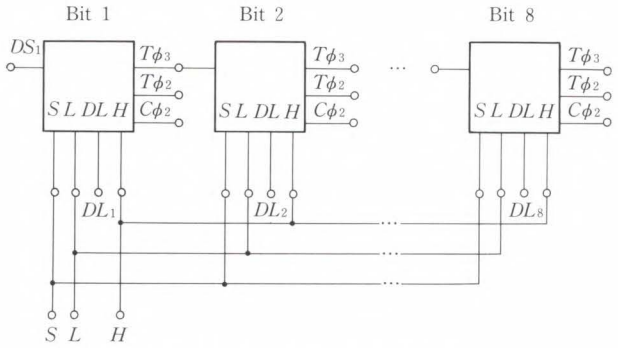


Fig. 25—Eight-bit shift register.

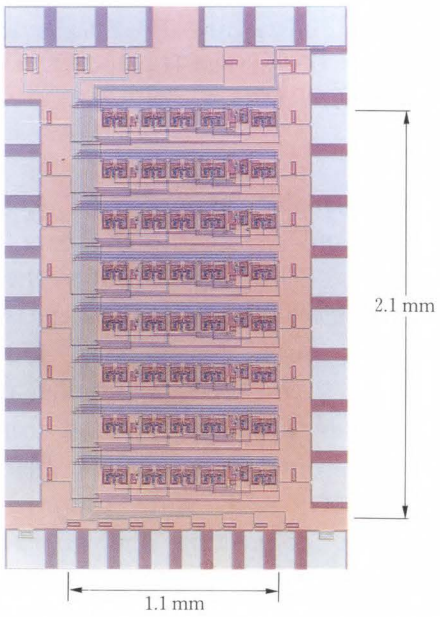


Fig. 26—Fabricated 8-bit shift register chip.

The DS for bit 1 is given externally by DS_1. When 1 is applied to L, LOAD is executed. In this operation, data from DL_1 to DL_8 is applied in all bits in parallel. When 1 is applied to H, HOLD is executed. The data for each bit is held from one clock to the next. When 0 is applied to all three control signals, the output of all bits becomes 0 after the CLEAR operation.

The 8-bit shift register was fabricated using $Nb/AlO_x/Nb$ junctions, Mo resistors, and SiO_2 insulation, that is, the standard process described in another part of this paper[1]. The minimum diameter of the junction is 2.5 μm. The critical current density of 1 700 A/cm^2 is about 20 percent less than the design value of 2 100 A/cm^2. Figure 26 shows the fabricated

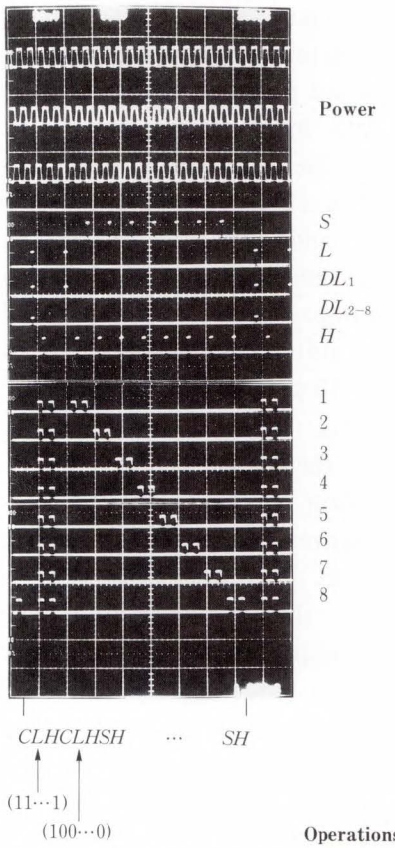


Fig. 27—Function tests of SHIFT, LOAD, HOLD, and CLEAR operations.

chip. The circuit area is 1.1 x 2.1 mm^2 and contains 112 gates. There is a total of 328 Josephson junctions and 516 resistors. The total power consumption was 1.8 mW.

Figure 27 shows the results of testing the shift register function using an 80-μs clock. All functions operated correctly. SHIFT operation was executed with clocks up to 2.3 GHz (430 ps) as shown in Fig. 28. By applying 1 to S and DS_1 continuously with a unit step pulse, the output of bit 1 was set to 1 and that of bit 8 was set to 1 after eight clock cycles. The operating margin of the power bus was only a point at 2.3 GHz for the SHIFT operation. For 500-MHz clock operation, it was ±8%.

A pseudorandom bit sequence generator was also developed[45]. The circuit is constructed with nine stages of the 1-bit shift register with its output being fed back to stage 5 through an exclusive-OR gate. This generator can generate a pseudorandom number with a 511-bit sequence. Correct operation was also confirmed

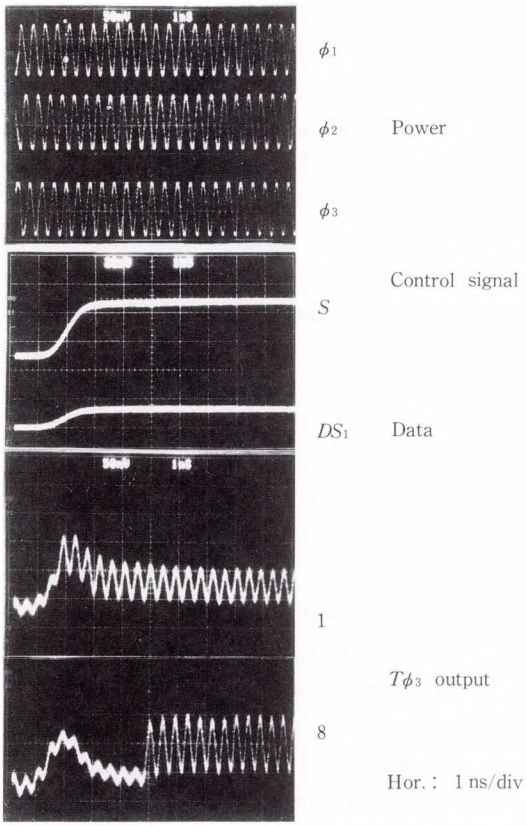


Fig. 28—Measured SHIFT operation with 2.3 GHz (430 ps) clock.

up to 2.2 GHz.

5.2 Arithmetic Logic Unit: ALU[43)]

The ALU is a key processor component. The ALU designed with the MVTL gates performs 12 functions (see Table 3). Three-bit control signals S_0, S_1, and S_2, and one carry signal C_{in} from the previous stage are used to determine operation. By using different combinations of these four signals, the ALU performs eight arithmetic functions and four logic functions.

A unique block layout was developed to achieve these functions using the MVTL 2OR-AND unit cell. The unit cell executes logic operation $(A + B) \cdot (C + D)$, and the ALU diagram layout is designed based on this operation. Figure 29 shows a 1-bit ALU consisting of 18 unit cells. Because dual-rail logic is used, complementary signals for both control and data are required. A_n and B_n are input signals, and F_n is the output data signal.

Output terminals for the carry signal of

Table 3. ALU functions

No.	Signal S_2	S_1	S_0	C_{in}	Out
1	0	0	0	0	A
2	0	0	0	1	A + 1
3	0	0	1	0	A + B
4	0	0	1	1	A + B + 1
5	0	1	0	0	A − B − 1
6	0	1	0	1	A − B
7	0	1	1	0	A − 1
8	0	1	1	1	A
9	1	0	0	×	$A \vee B$
10	1	0	1	×	$A \oplus B$
11	1	1	0	×	$A \wedge B$
12	1	1	1	×	$\overline{A}$

× : Don't care

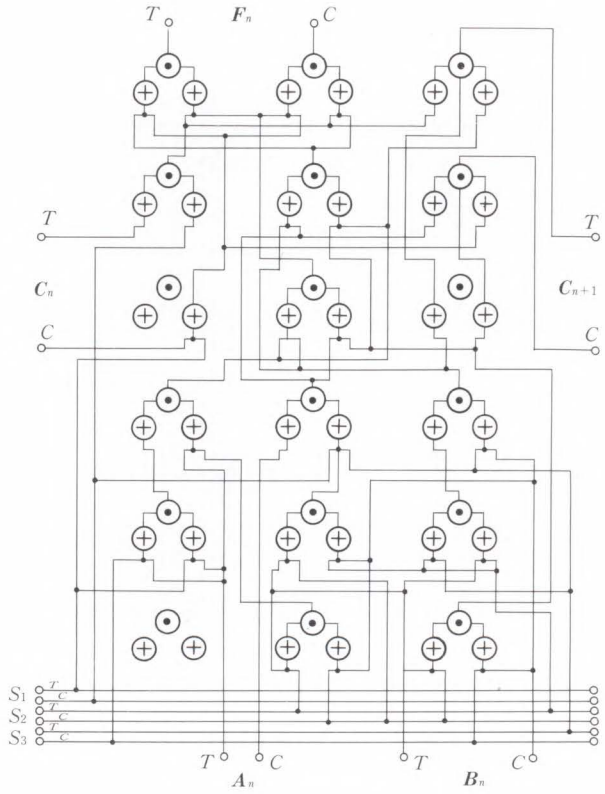


Fig. 29—One-bit ALU diagram.

the 1-bit block shown in Fig. 29 are laid out for easy connection to the input terminals of the next block. This block can be used as a simple 1-bit slice ALU. When blocks are arranged serially, the input and output terminals are connected with the shortest possible wiring,

resulting in a multiple-bit ALU using the ripple carry.

Figure 30 shows a 1-bit ALU composed of unit cells. The arrangement of cells and interconnecting lines corresponds to the diagram in Fig. 29. The carry signal flows from left to right. The minimum diameter of the junction is 2.5 μm. The circuit area for the 1-bit ALU, enclosed in dashed line in Fig. 30, is $480 \times 800\ \mu m^2$. The area includes 18 unit cells, power buses for the OR gates, and the interconnecting lines. The power bus is 22 μm wide, and provides stable power. A 2-layer superconductive metal was used for the interconnecting lines. Line width and spacing are both 4 μm. Contact holes are $2 \times 2\ \mu m^2$.

The multiple-bit ALU consists of 1-bit ALUs connected side by side. Figure 31 shows a fabricated chip whose circuit area is $8.2 \times 0.85\ mm^2$. The sixteen 1-bit ALU blocks are connected serially. The total number of gates is 900. The critical current density ($2\,600\ A/cm^2$) of the Josephson junction is slightly higher than the optimum design value of $2\,100\ A/cm^2$.

We confirmed correct circuit operation with a low-frequency clock (1 kHz). To measure the critical path delay, we set the ALU in adder mode. The critical path delay is the sum of carry propagation delays from bits 1 to 16 when (000 ... 01) + (111 ... 11) is executed, and the shortest delay measured was 860 ps. The critical path of the ALU includes 83 stages of OR and AND gates, and the total length of superconducting lines between the unit cells is 13 mm. The propagation delay in the 13 mm lines was calculated as 95 ps. From these values, the average gate delay was estimated to be 9.2 ps per gate. Thus, we succeeded in demonstrating sub-10 ps gate operation in an actual circuit with reasonable fan-in and fan-out for the first time. Since the total power consumed was 10.1 mW, the average power consumed per gate was 11.3 μW.

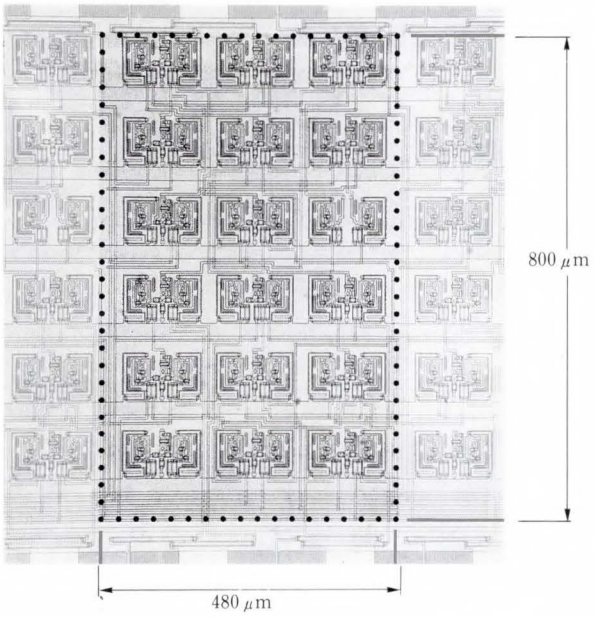


Fig. 30—One-bit ALU.

5.3 Four-bit microprocessor[44]

We newly fabricated a 4-bit microprocessor in the world's first application of Josephson devices to a microprocessor. This development confirms the ultra-fast operation of Josephson circuits at the LSI level. Chip functions similar to those of the Am 2901 Microprocessor made by Advanced Micro Devices Inc.[46] were selected because this microprocessor is considered the standard 4-bit microprocessor slice. A GaAs version of the Am 2901 Microprocessor has also been developed[47]. Consequently, the capabili-

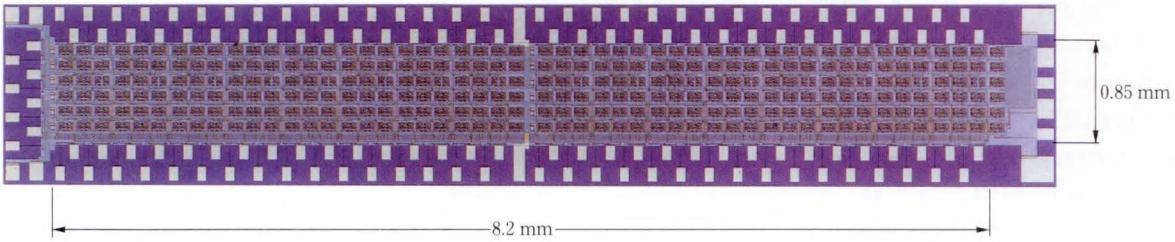


Fig. 31—Sixteen-bit ALU.

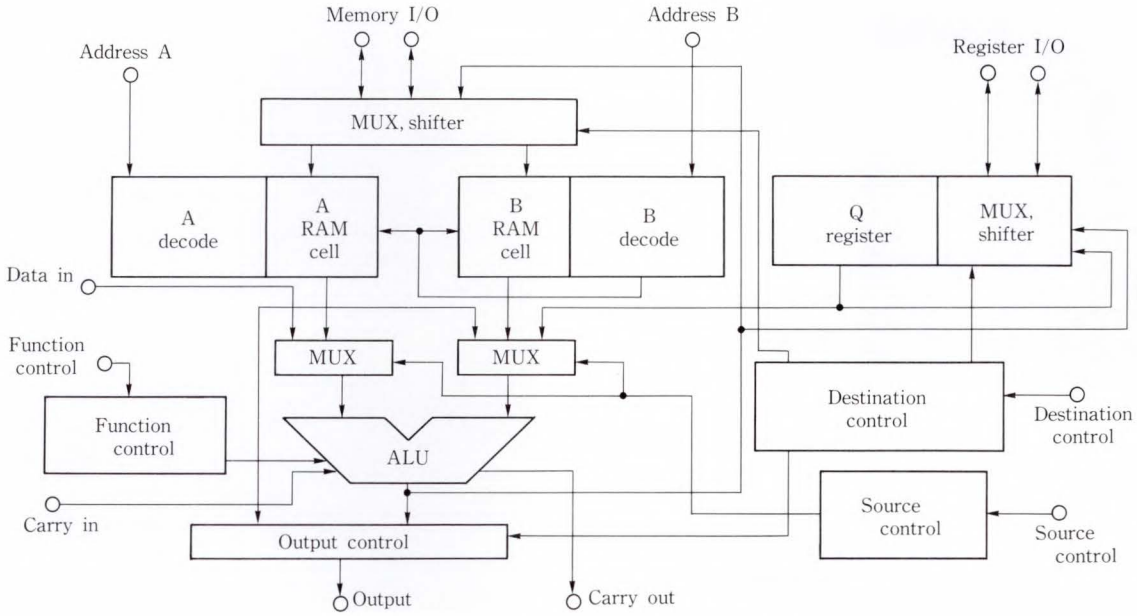


Fig. 32—Four-bit microprocessor diagram.

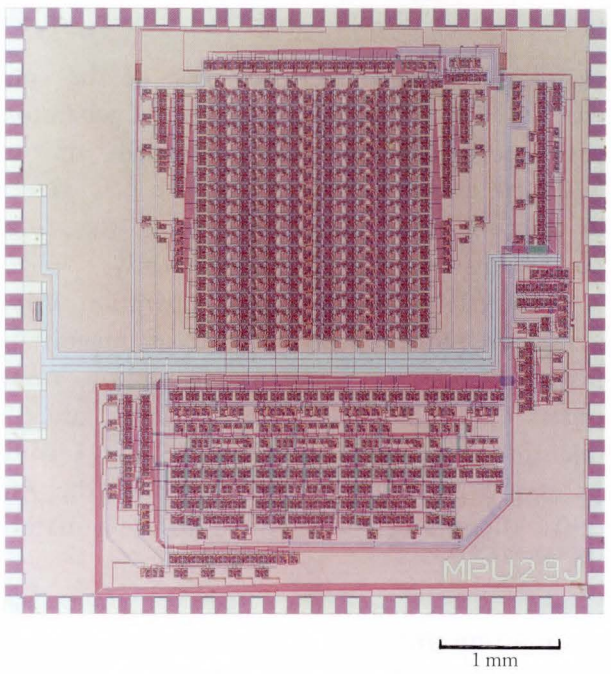


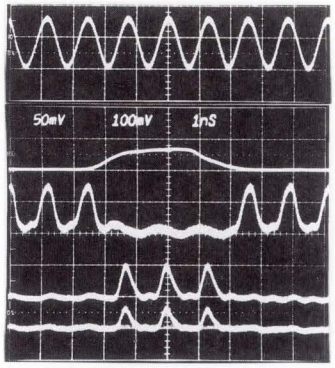
Fig. 33—Four-bit microprocessor.

ties of the Josephson microprocessor can now be compared with those of semiconductor microprocessors having the same functions, and the performance potential of Josephson circuits can be clarified.

Figure 32 diagrams the Josephson microprocessor we designed. This microprocessor features a dual memory set used as 16-word by 4-bit 2-port RAM with a RAM shifter, 8-function ALU, Q register, and several controllers. This circuit is driven by 3-phase power ϕ_1, ϕ_2, and ϕ_3. Dual-rail logic was used in the ALU and the controllers of the microprocessor, and complementary signals are made from the input signals with TIs powered by ϕ_1. Decoding is run in gates powered by ϕ_1, memory data reading powered by ϕ_2, and data modification and writing powered by ϕ_3.

Both the minimum junction diameter and line width are 2.5 μm. The interconnecting lines are 4 μm wide. Figure 33 shows the chip. The basic gate is the MVTL, and there are a total of 1 841 gates.

The critical path of the carry signal is transmitted from the least significant bit (LSB) to the most significant bit (MSB) in the ALU, then the sum signal is transferred from the ALU to RAM. Forty-one gates are required to switch sequentially along the path, with an interconnecting line length of 15 mm. MVTL gates operate with a sub-10 ps gate delay in the actual circuits as previously described, and the propagation delay in the interconnecting lines is about 8 ps/mm. The critical path delay time may be roughly estimated about 0.5 ns, and a sinusoidal power duty ratio is about 1/2. Thus, the maximum clock frequency was estimated at 1 GHz.



Power : 5 mW/chip
(3.6 μW/gate)

Carry in

Output LSB

Output MSB

Memory I/O MSB

Hor. : 1ns/div

Fig. 34—Operation waveforms of the 4-bit microprocessor.

Table 4. Four-bit microprocessor performance

Device	Maximum clock (MHz)	Power dissipation (W)
Si	30	1.4
GaAs	72	2.2
Josephson	770	0.005

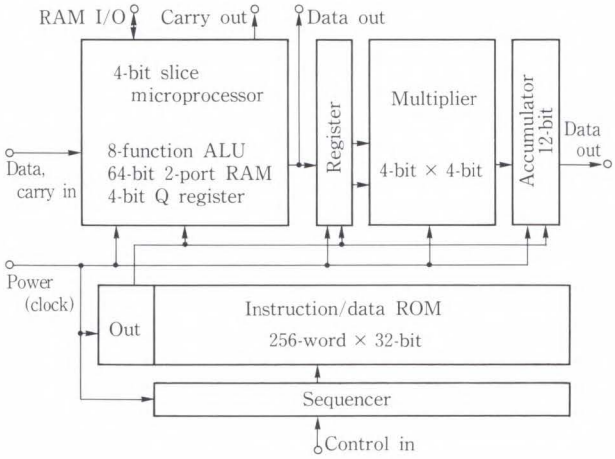


Fig. 35—Four-bit processor diagram.

The critical current density of the fabricated Josephson junction was 2 300 A/cm^2, which is slightly higher than the optimum designed value of 2 100 A/cm^2. The measured operating margin was ±34% for the MVTL OR gate and ±32% for the unit cell. All functions and source combinations were confirmed with an operating margin of ±16% at a clock frequency up to 100 MHz, which is the maximum clock frequency of the word pattern generator.

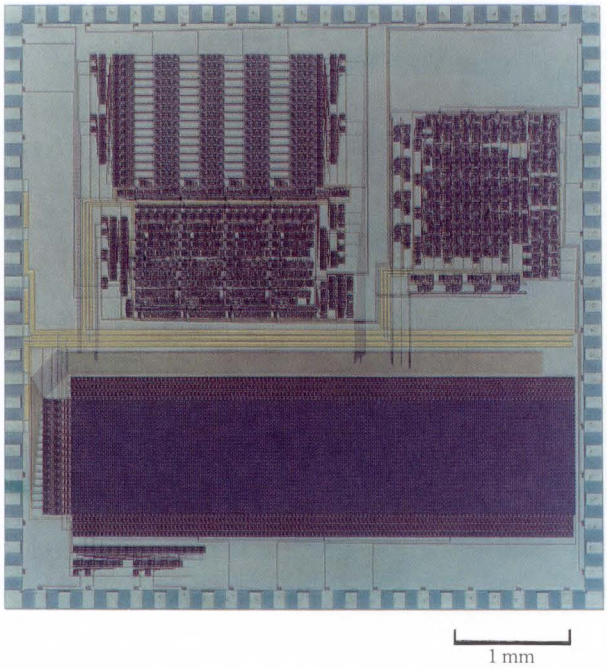


Fig. 36—Four-bit processor.

Operation along the critical path of the chip was tested using the high-speed pulse generator, with correct operation confirmed up to 770 MHz as shown in Fig. 34. The gate power dissipation was 3.6 μW/gate, and the total power consumed by the chip was 5 mW.

Josephson microprocessor operation using a clock frequency one order of magnitude faster than, and power consumption three orders of magnitude less than a semiconductor microprocessor were confirmed. Table 4 compares the performance capabilities of the Am 2901 Microprocessor for three different materials[44),46),47)].

5.4 Four-bit processor[4)]

The microprocessor was expanded into a more complete processor by adding a 4-bit multiplier, a 12-bit accumulator, 8 K-bit instruction ROM, and a sequencer. Figure 35 diagrams the 4-bit processor. Figure 36 shows the fabricated chip. The minimum junction diameter was reduced from 2.5 μm to 1.5 μm and, accordingly, the gates and memory cells were made smaller. Consequently, the Am 2901 Microprocessor was reduced in size from 5 × 5 mm^2 to about 2 × 2 mm^2. Thus, the

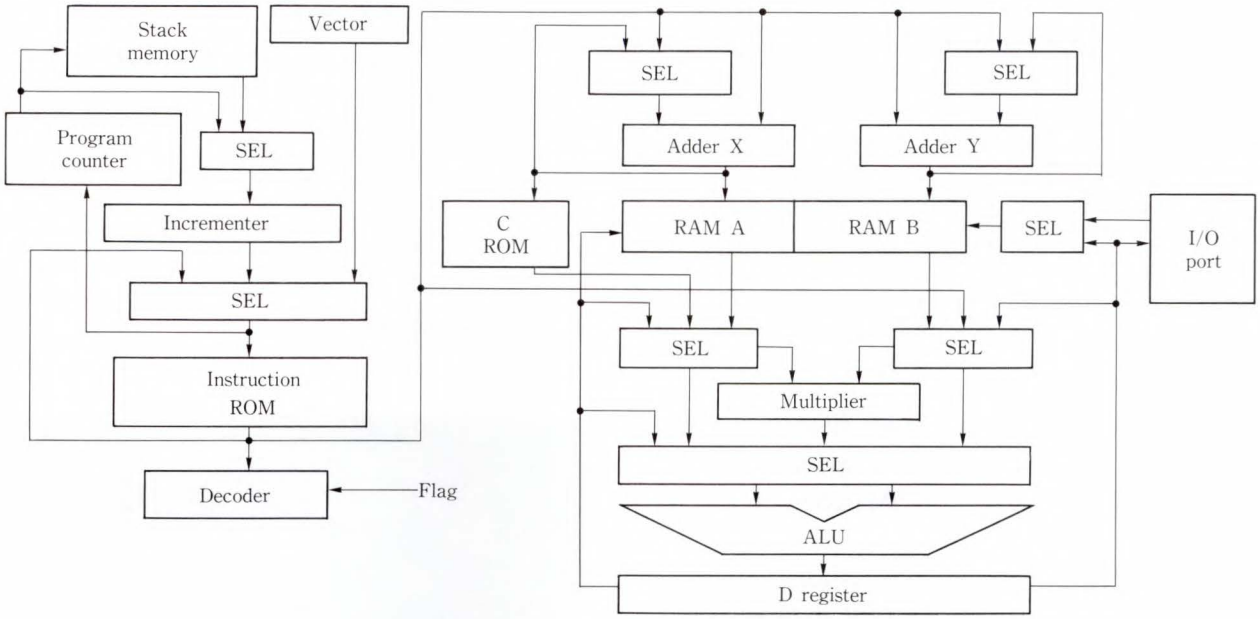


Fig. 37—Eight-bit DSP diagram.

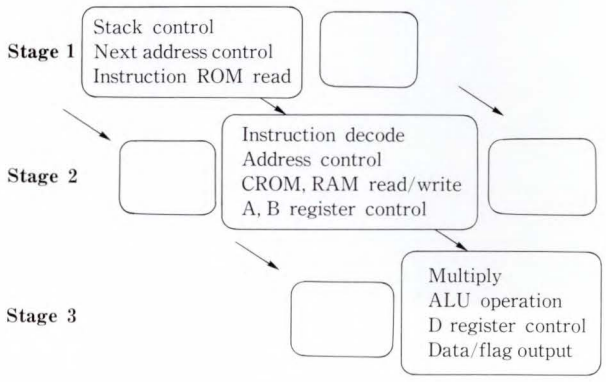


Fig. 38—DSP processing sequence.

integration of all components, including 3 056 gates, on a chip 5 x 5 mm^2 was made possible.

The ROM access time was 100 ps for the far-end ROM cell. The multiplication time was 200 ps for operation along the multiplier critical path. Correct 4-bit microprocessor operation was also confirmed along the critical path up to a clock frequency of 1.1 GHz. The maximum clock frequency increased due to the 1.5-μm technology employed to reduce the microprocessor size. The power dissipation of the chip was 6.1 mW. Because the multiplier, microprocessor and ROM are operated by different phases of three pipelines, the multiplier and ROM are fast enough to be operated at a clock frequency of 1.1 GHz. Thus, the operating speed of the chip is limited by the clock frequency of the microprocessor.

5.5 Eight-bit Digital Signal Processor: DSP[5)]

We have designed an 8-bit DSP to achieve high-speed system-level performance. The DSP includes a multiplier, ALU, instruction ROM, coefficient ROM, two data RAMs, a sequencer, and other control circuits. The DSP performs the same functions as commercially available DPSs and offers comparable performance capabilities.

Figure 37 diagrams the DSP. The architecture is based on that of the Si DSP[48)]. Figure 38 shows the 3-stage pipeline processing sequence. Both the 8 x 8 bit multiplier and 13-bit ALU are active in the third stage. The DSP thus completes a series of multiply-add operations and a multiply-add operation using previously added data once every machine cycle. With this design, the data processing rate using previous data is the same as the internal machine clock frequency.

Data memory consists of two 16-word by 8-bit RAMs, RAM A and RAM B. Each has its own addressing circuits. Program ROM (IROM) is 64 words by 24 bits. Each 24-bit

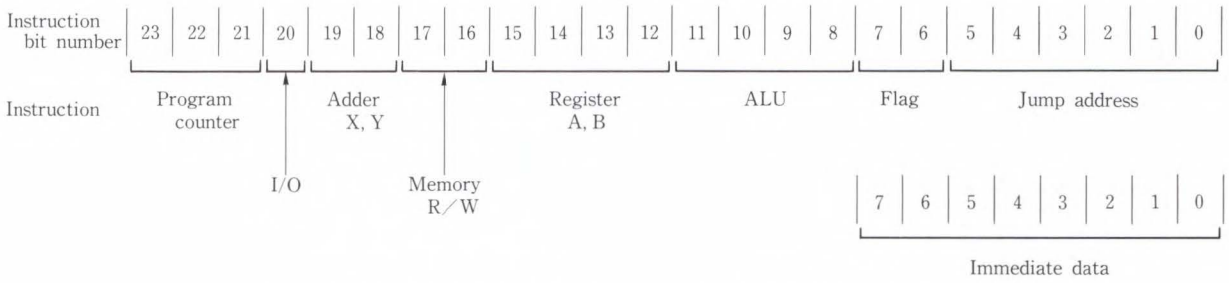


Fig. 39—24-bit instruction code format and immediate data format.

instruction is divided into seven fields as shown in Fig. 39. The DSP contains a special 16-word by 8-bit memory area (CROM) for coefficient storage.

The I/O port of this DSP consists of data registers and a controller. Output data is stored with an independent external clock. This port helps interface the high-clock-speed Josephson DSP with low-clock-speed semiconductor systems.

Such Josephson devices, as the $69 \times 52\ \mu m^2$ unit cell for the logic gate, $26 \times 16\ \mu m^2$ ROM cell, and $133 \times 48\ \mu m^2$ data RAM are built into this DSP. The MVTL OR gate in the unit cell occupies $26 \times 21\ \mu m^2$. Each data RAM cell stores data in a superconducting persistent current, and has a sense amplifier to increase the operating margin. The minimum junction diameter is 1.5 μm and the minimum line width is 2 μm. The 2-layer superconducting interconnections are 3 μm wide with 2 μm spacing.

Figure 40 shows the DSP chip. To reduce the level of complexity, both the multiplier and ALU use the ripple carry method. Table 5 lists the chip specifications. There are 6 300 gates and the chip is $5 \times 5\ mm^2$ in size.

The operating speed of each circuit in the DSP was measured. The carry propagation delay in the multiplier was 240 ps. Forty gates must switch sequentially along a 3.6 mm path. Because the propagation delay is 8 ps/mm, the average gate delay is estimated at 5.3 ps/gate. For the ALU, the delay was 410 ps. The critical path in the ALU is the carry propagation route in adder mode, and 44 gates must switch sequentially along a 4.2-mm path. The average delay is estimated at 7 ps/gate.

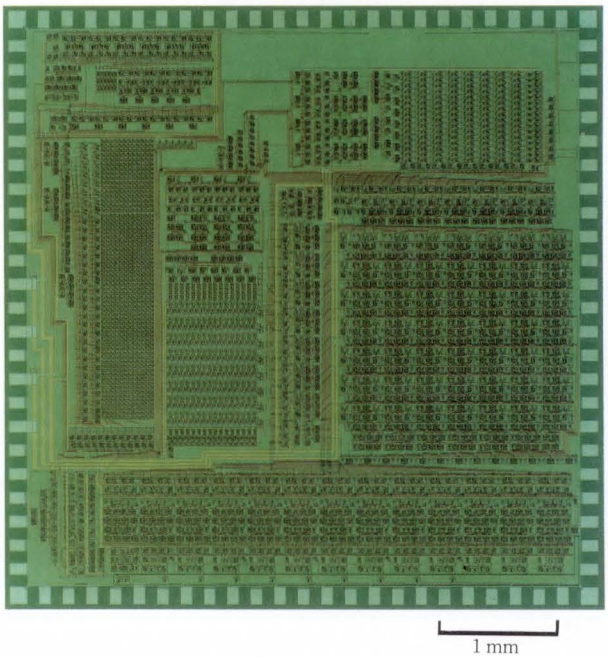


Fig. 40—Eight-bit DSP.

Table 5. DSP chip specification

Item		Specification
Gates		6 300
Josephson junctions		23 000
Minimum-junction size		1.5 μm
ROM	Instruction	64-word x 24-bit
	Coefficient	16-word x 8-bit
Data RAM		16-word x 8-bit x 2
Multiplier		8-bit x 8-bit
ALU		13-bit, 16 functions
Chip size		5.0 mm x 5.0 mm

The access time of the far-end IROM was 200 ps, and that of the RAM cells was 130 ps.

The internal machine cycle is limited by the stage 3 pipeline. Both multiplication and

addition are completed in this stage. The total delay of both multiplier and ALU is 650 ps. The maximum clock frequency is estimated at 1 GHz with sufficient margin for an interconnection propagation delay between the component so that a nonparallel processing speed of 1 GOPS (Giga-Operation Per Second) can be attained. This is 100 times faster than the conventional CMOS DSP, with about one tenth the power consumption[48].

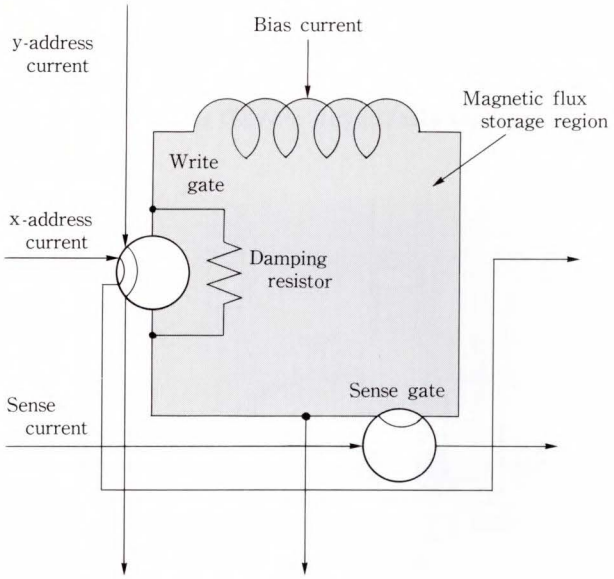


Fig. 41—Conventional memory cell.

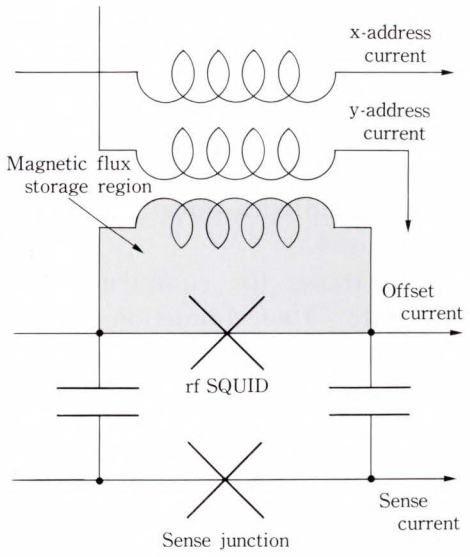
6. Memory circuits[6]

It was once considered that high-speed Josephson cache memory capacity up to the 4 K-bit level was too difficult to achieve[49]. No one actually built a memory circuit with sub-ns access time until 1988. We discarded conventional memory in an attempt to develop a completely new memory circuit with a new memory cell, decoder, and driver circuit.

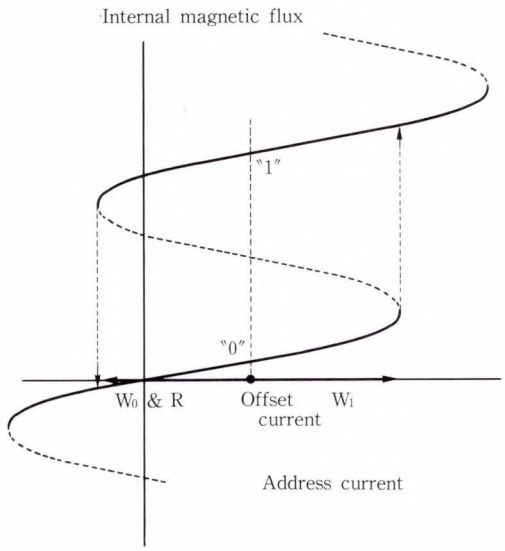
Figure 41 shows the circuit diagram of a conventional memory cell, with which 1 K-bit memory circuits were fabricated. Access time as fast as 570 ps has been reported[41]. The development of higher-density memory was complicated due to the difficulty in reducing the cell size used in conventional memory design. Other problems were posed by the small fan-in and fan-out of Josephson gates and their lack of sufficient drivability. To solve these problems, a new memory circuit with a 4 K-word by 1-bit configuration was developed[6].

6.1 Memory cell

We developed a capacitively coupled memory cell in which information is stored as a superconducting persistent current in an rf SQUID. The rf SQUID is a superconduct-



a) Equivalent circuit



b) Memory operation on internal flux vs external flux curve (W_1 denotes write 1, and W_0 & R denotes write 0 and read)

Fig. 42—Capacitively coupled memory cell.

ing loop with one Josephson junction. The cell consists of one rf SQUID, a sense junction, and two capacitors as shown in Fig. 42a). Information is read by the sense junction connected to the rf SQUID through the capacitors. One memory cell is selected by two magnetically coupled control lines.

The following describes memory cell operation and Fig. 42b) shows the relationship between internal flux Φ_i and the external flux caused by the x- and y-address currents. The regions with a positive slope (bold line) are stable, and negative-slope regions (dashed line) are unstable. Thus, two stable states, denoted by quantum states 0 and 1, exist for the properly shifted point of the address current with an offset current. The states correspond to binary 0 and 1. The address current is positive for writing 1 and negative for writing 0. For reading, negative-polarity address current is applied and the sense junction is biased below the critical current. When 1 is stored in the rf SQUID, it goes from quantum state 1 to quantum state 0. A small pulse appears across the junction of the rf SQUID when it changes the states. The pulse voltage multiplied by the pulse width almost equals the value of flux quantum Φ_0. For example, a pulse voltage of 200 μV with a 10-ps duration appears across the junction. This pulse is transferred to the sense junction, causing sense junction voltage transition. Although the read operation is destructive, rewriting is done immediately after reading.

6.2 Decoder circuit

There are two ways to construct a decoder: using AND gates or using OR gates. The advantages of AND gates are that timing pulses are not needed. But more gates should be used than when using OR gates because the multiple-input AND gate is not practical for Josephson AND gates. The disadvantages of OR gates are that timing pulses are needed and the circuit becomes more complex. We have successfully constructed a decoder with AND gates. To reduce the number of logic stages needed for decoding, we developed an AND gate with

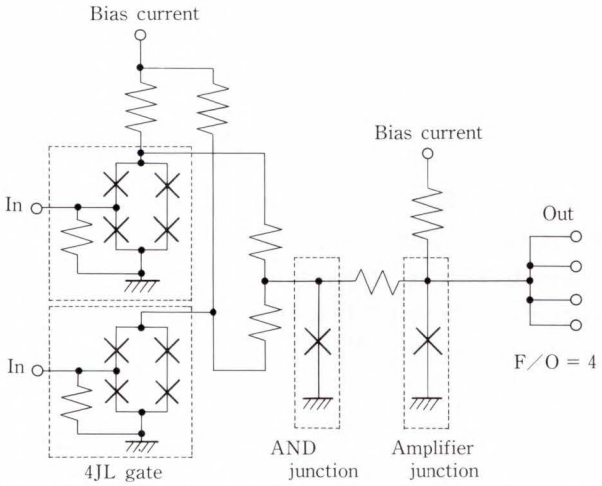


Fig. 43—Equivalent circuit of AND gate for decoder.

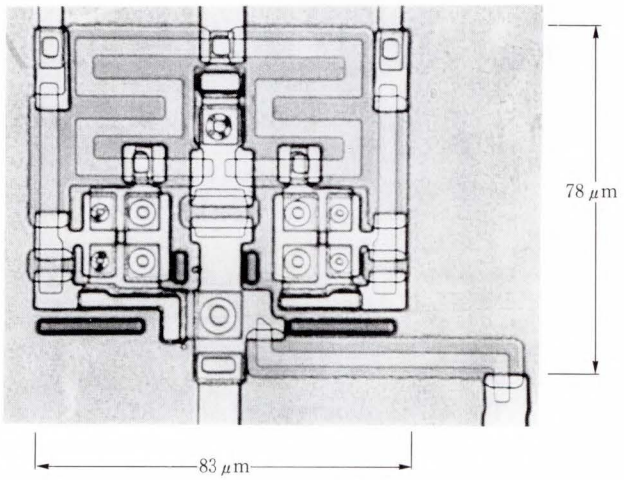


Fig. 44—AND gate.

a fan-out of 4. A 6-bit to 64-bit decoder that selects 64 address lines with 6-bit address signals can be constructed with three AND gate stages with a fan-out of 4.

Figure 43 shows the equivalent circuit of the AND gate. Two 4-junction logic (4JL) gates are used to isolate the input and output of the previous gate. One junction is used as an AND gate that operates like a member of the MVTL gate family. The output current is amplified by the other single junction, which was biased independently of the 4JL gates, and the fan-out was increased from 2 to 4.

Figure 44 shows the fabricated gate, 83 x 78 μm^2 in size, with a 4 μm line width. We designed a 6-bit to 64-bit decoder with

this AND gate and confirmed its correct operation. The decoding time was measured at 90 ps, which is the fastest decoding time yet recorded.

6.3 Driver circuit

Since memory cells were arranged in a 64-by-64 configuration, each driver gate had to drive 64 cells connected in series. The drive line can be considered a transmission line, provided the propagation delay time for one memory cell is less than the rise time of the drive current. This condition is usually satisfied because the propagation delay time is less than 1 ps and the rise time exceeds 10 ps. For matched transmission line, drive current I_d is given by V_0/Z_0, where V_0 is an output voltage of the driver gate and Z_0 is the characteristic impedance of the drive line. Since Z_0 was 18 Ω and I_d is 0.6 mA in our cell design, the output voltage of the driver should be 10.8 mV, which is about 4 times the gap voltage of the Nb/AlO_x/Nb junction.

Since simple series-connected junctions do not switch simultaneously, it was considered too difficult to obtain an output voltage larger than the gap voltage of one junction, that is, 2.8 mV for the Nb/AlO_x/Nb junction. We have developed a gate that generates a voltage higher than the gap voltage. Figure 45 shows the circuit configuration. The gate consists of two branches, each consisting of four junctions and one resistor connected in series. The bias current is supplied to the gate midway between the two branches. The critical current of junctions and the resistance are designed to be equal for both branches. The next chapter describes the principles of the gate operation.

This driver circuit was fabricated to include 64 memory cells. The measured rise time at the far end of the drive line was 60 ps.

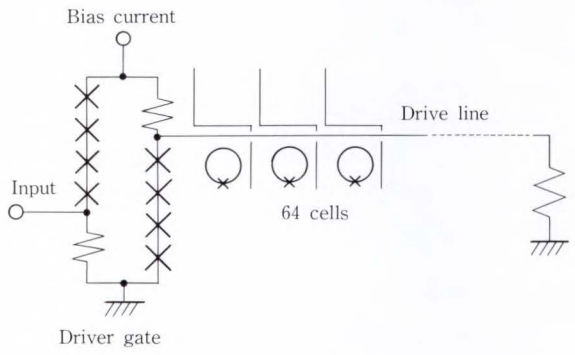


Fig. 45—Equivalent circuit of driver gate. A cell drive line is also shown. The critical current of all junctions is 4.2 mA. The resistance for each of the two resistors is 1.5 Ω.

6.4 Memory operation

Figure 46 shows the 4 K-bit memory designed and fabricated with the circuits described above. The minimum junction diameter is 2.5 μm and the minimum line width 4 μm. Each memory cell is 83 × 83 μm^2 in size. A rather large cell was used to verify memory circuit feasibility without using sophisticated process technology. The chip is 7.7 × 7.7 mm^2 in size and includes 14 468 junctions. The measured access time was 590 ps, and the chip power dissipation was 19 mW.

7. Interfacing

Josephson logic circuits operate at a clock frequency above 1 GHz and their logic swing is less than 3 mV. Two factors dictate the need for interface circuits between the Josephson and semiconductor circuits. One factor is

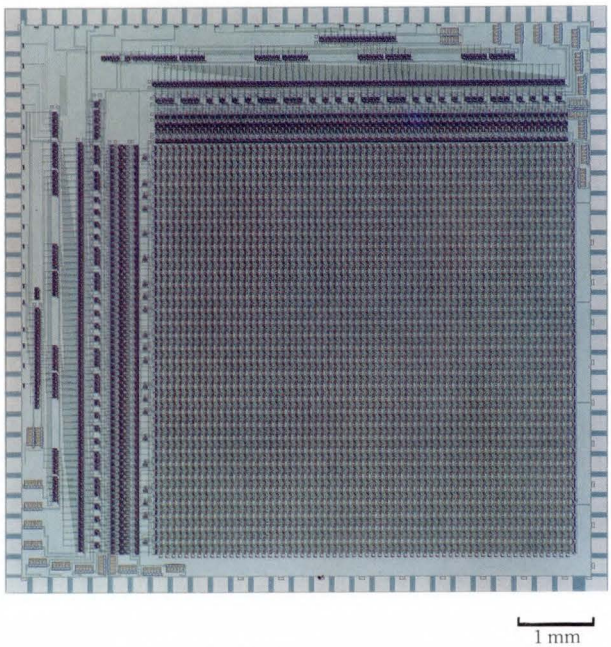


Fig. 46—4 K-bit memory circuit.

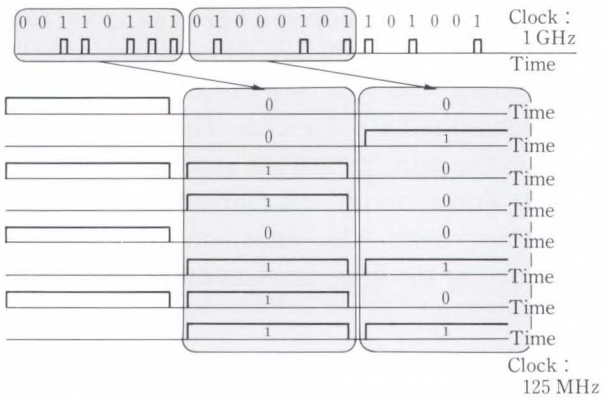


Fig. 47—Serial-parallel converter operation principle. 1 GHz outputs from Josephson circuits are converted into 8-bit parallel signals with a clock frequency of 125 MHz.

amplifying the output voltage from the 3 mV of the Josephson circuit to the 1 V needed to drive semiconductor circuits at room temperature. The other factor is converting the clock frequency from 1 GHz to 100 MHz. Simply reducing the clock frequency will cause information to be lost in a Josephson system. Consequently, we decided to convert the serial output signal from the Josephson system into a low-frequency parallel output called a serial-parallel converter. Figure 47 illustrates the conversion.

The following sections describe the two interface circuits.

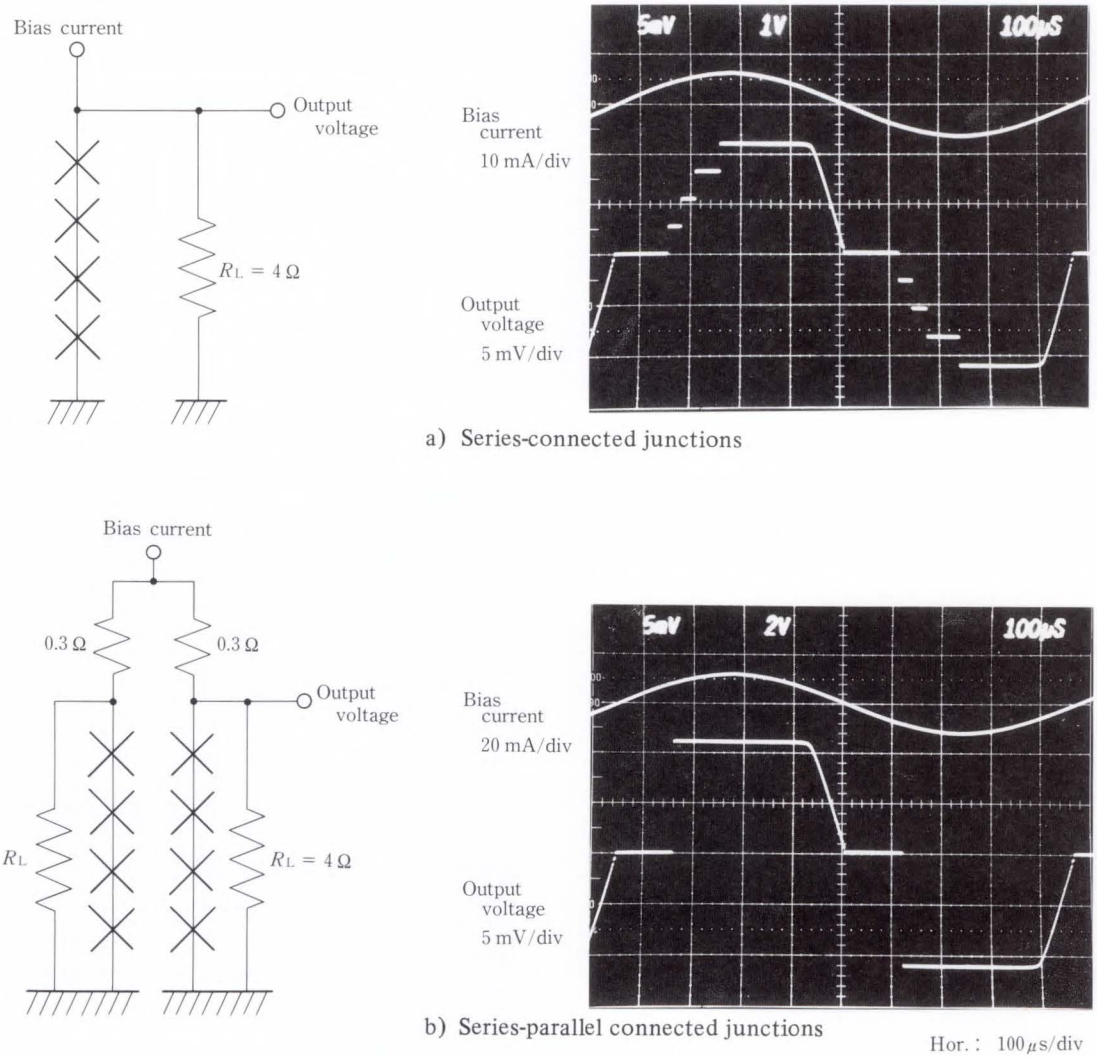


Fig. 48—Voltage waveforms across junctions driven by sinusoidal current.

7.1 High-voltage driver[50)]

The output of a Josephson logic gate consisting of $Nb/AlO_x/Nb$ junctions is only 2.8 mV, and is determined by the gap voltage of the junction. It would seem easy to obtain a voltage higher than the gap voltage with series-connected junctions, but this is true only for series-connected junctions without a load resistor. Even in such a case, the scattering of critical currents should be small. When a load resistor is connected to series-connected junctions, the junctions do not switch simultaneously. Figure 48a) shows the voltage output across four series-connected junctions with a load resistor. A voltage step appears for each junction switching to the voltage state. When one of the four junctions switches to the voltage state, current flowing through a series-connected junction decreases because some bias current flows to the load resistor. Thus, bias current should be increased to switch the next junction to the voltage state. After switching, the current for the series-connected junction decreases again. Consequently, steps appear in the voltage across the junctions as shown in Fig. 48a). Thus, the simple series-connected junctions cannot be applied to an interface circuit for driving semiconductor circuits.

This problem was solved by connecting the series-connected junctions in parallel. Figure 48b) shows the voltage across the junctions. Four series-connected junctions are connected in parallel, and load resistors are connected to the junctions. No step occurs and four times the gap voltage V_g of the junction is obtained. The series-parallel connected junctions switch simultaneously because the bias current flows equally to both branches, and after the bias current increases, the junction with the smallest critical current, for example, in the left branch, switches to the voltage state, then some current flowing through the left branch is transferred to the right branch, causing an overdrive current for junctions in the right branches. Consequently, all junctions switch almost simultaneously to the voltage state. The bias current is transferred again to the left branch, and the remaining

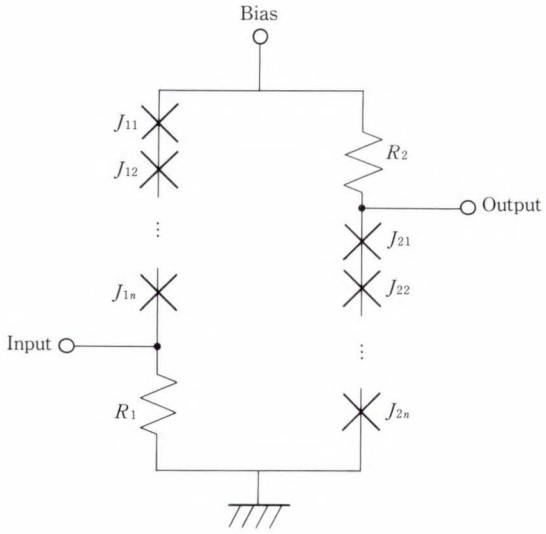


Fig. 49—Equivalent circuit for the high-voltage gate interfacing Josephson junctions and semiconductors.

junctions switch to the voltage state. After all junctions switch to the voltage state, bias current is transferred to the load resistors. This switching is done within a few tens of ps. The series-connected junctions can be applied to a gate, which should have an output voltage higher than the junction gap voltage.

We designed a high-voltage gate using series-parallel junctions as shown in Fig. 49. The only difference between this structure and that shown in Fig. 48b) is the location of the resistor. Junctions J_{11} to J_{1n} serve as isolation junctions. Resistor R_1 functions both as branch and isolation resistors. After the isolation junctions switch, input current flows to resistor R_1, to isolate both input and output. The circuit is designed so that the critical current in all junctions J_{11} to J_{1n} and J_{21} to J_{2n} is equal. Resistors R_1 and R_2 are usually equal, resulting in a large bias margin. The current gain (or gradient of the threshold curve) is set to 1. Note that the voltage gain is 4.

We applied this high-voltage gate with four junctions in each branch to supply 4 V_g output voltage, to the driver circuit of the previously mentioned 4 K-bit memory. We also designed a high-voltage gate with 52 junctions in each branch to build a Josephson driver gate, and obtained output voltage of 150 mV. Because

this voltage is insufficient for driving a semiconductor circuit at room temperature, the output voltage of the driver gate was applied to a high electron mobility transistor (HEMT) immersed in liquid helium as shown in Fig. 50. The HEMT had a gate length of 1 μm and a gate width of 50 μm, and operated in depletion mode. Transconductance g_m increased from 200 mS/mm to 300 mS/mm when cooled from 300 K to 4.2 K. Although the threshold voltage shifted about 0.4 V, the HEMT maintained its depletion characteristics.

Figure 51 shows the interface circuit in which the Josephson driver gate and HEMT driver are combined. The upper trace is the bias current of the Josephson driver and the middle trace is the input current. Both are negative. The lower trace is the output voltage of 0.9 V from the HEMT. The HEMT was biased with dc voltage of 4 V. When input current was applied to the driver gate, a positive output voltage was obtained, then inverted by the HEMT. An output voltage swing of 0.9 V is sufficient to drive semiconductor circuits. By estimating the switching speed of this interface circuit through computer simulation, the rise time of the output voltage from the HEMT was confirmed at about 100 ps. This means that the high-voltage gate is suitable for use in an interface circuit.

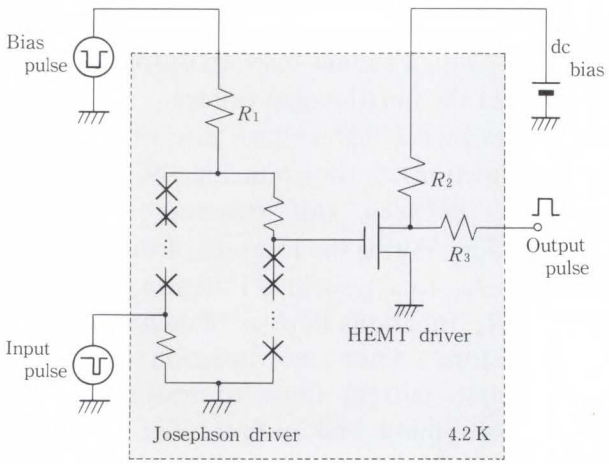


Fig. 50—Interface circuit for converting 3 mV output to 1 V. It consists of Josephson and HEMT drivers.

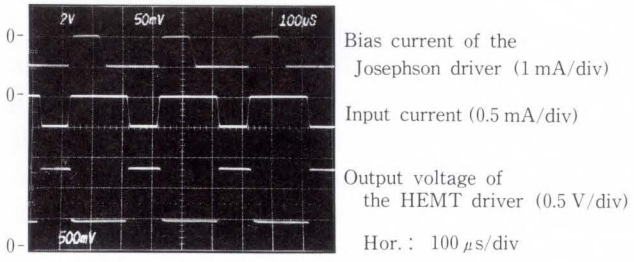


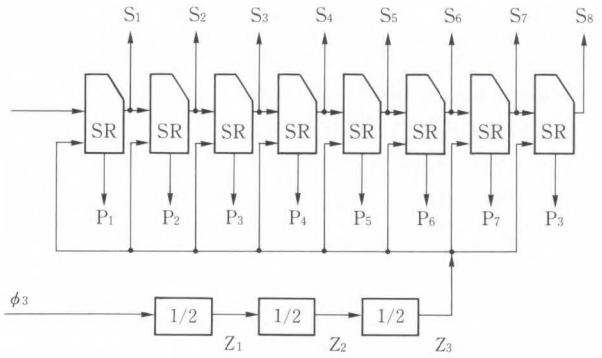
Fig. 51—Interface circuit operation.

7.2 Serial-parallel converter[51)]

We designed an 8-bit serial-parallel converter consisting of a 1/8-prescaler that generates a pulse every eight clocks, and an 8-bit shift register.

The 1/2-prescaler generates a pulse when the number of input pulses is even, that is, it outputs one pulse for every two input pulses. Connecting three 1/2-prescalers in cascade forms a 1/8-prescaler.

The shift register is almost identical to the one previously described. Figure 52 shows the 8-bit serial-parallel converter. Figure 53



S_n: Output from the 1-bit shift register in each bit.
P_n: Parallel output available only when timing signal is applied.
Z_n: Output from 1/2 prescaler.

Fig. 52—Eight-bit serial parallel converter diagram.

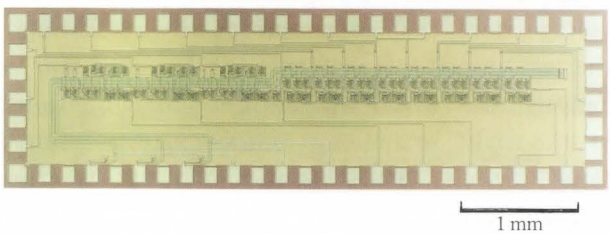


Fig. 53—Serial parallel converter.

shows the fabricated converter, which is 5.1×1.5 mm^2 in size, and which contains 92 MVTL gates. Correct operation was confirmed at low frequency, and the circuit was tested at high frequency. Figure 54 shows the operation waveforms at 1.3 GHz. The upper trace is the bias current waveform at phase ϕ_3. The second is a timing pulse Z_3 obtained from the 1/8-prescaler. The middle eight traces, S_n (n = 1-8), are output voltages from the shift register in each stage. Because the timing pulse from the prescaler was used as an input signal to the shift register, input is applied every eight clocks. The input signal was shifted from the lower to higher stages. The lower eight traces, P_n (n = 1-8), are parallel output signals from the shift register in response to a timing signal. The timing pulse was supplied from the prescaler. Thus, the output (100000001000 ...) from the 1.3 GHz clock circuit was converted to an 8-bit parallel signal with 160 MHz operation. Note the test circuit should include a circuit prolonging the 8-bit parallel output pulses for the duration of reduced clock frequency (about 6 ns in this case). Even so, a prolongation circuit can certainly be built with Josephson gates.

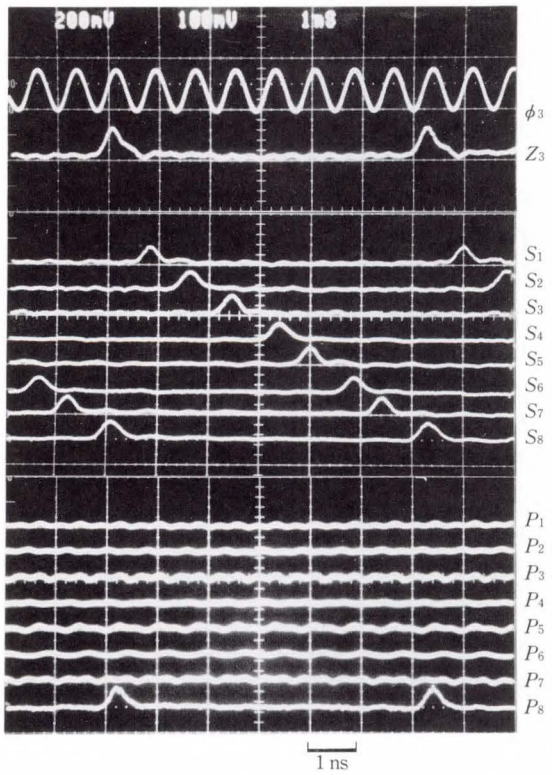


Fig. 54—Waveforms measured at 1.3 GHz.

8. Progress toward the Josephson computer

The introduction of the Nb/AlO_x/Nb junction completely changed the nature of Josephson integrated circuits. The stability, uniformity, reliability, and reproducibility of these junctions finally made it possible to create a variety of high-speed Josephson integrated circuits. The next step is to install these circuits in a cryogenic refrigerator to demonstrate their high-speed performance at the system level.

So, what lies ahead for Josephson integrated circuits?

8.1 Josephson computer

We know that it is possible to fabricate all components needed for Josephson computer – logic, memory, and interface circuits. Although their level of integration hardly matches that of semiconductor circuits Josephson integrated circuits operate much faster than semiconductors. This is because it is difficult to fabricate large-scale memory, such as 1 M-bit or 4 M-bit, with Josephson junctions, and thus the memory hierarchy of the Josephson computer appears similar to the 3-stage structure shown in Fig. 55. The Josephson memory will operate at 1 GHz, which is the same clock frequency as for logic circuits. Such semiconductor memory as 256 K-bit SRAM and 1 M-bit DRAM is used to store the information needed for calculation

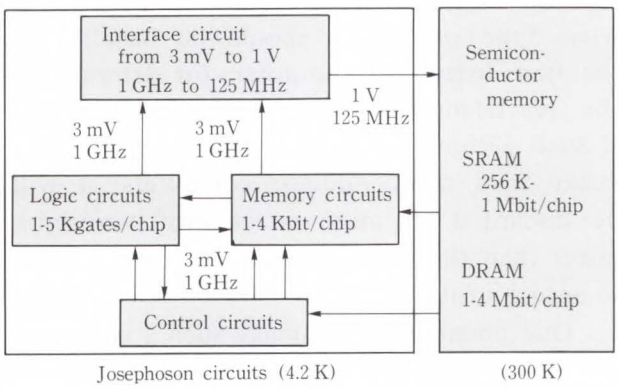


Fig. 55—Josephson computer diagram.

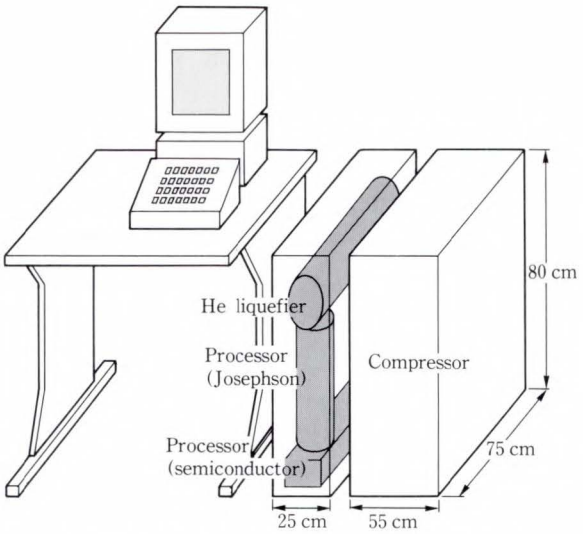


Fig. 56—Small-scale Josephson computer.

by the Josephson computer.

To develop a prototype Josephson computer, components must be installed in a cryogenic refrigerator, which looks very like a conventional semiconductor workstation, as shown in Fig. 56, but which requires a compressor to liquefy helium gas through cooling. The compressor can also be set up in a separate room, if necessary.

The first Josephson computer will not be as large is a semiconductor computer, but will be much faster. The smaller scale is not caused by technological problems, but is due to the relatively small amount of time and money expended on Josephson computer development projects around the world. After the first Josephson computer is introduced, the scale of this type of computer will certainly increase.

The most important point to consider is what type of system should be installed in the first Josephson computer, for determining the practicality of the Josephson computer. If such a computer is only two or three times faster than semiconductor computers, it will be discarded. It must be at least ten times faster than the fastest semiconductor computer to ensure a future.

One possibility is to make such a computer a special-purpose one for SQUID signal processing, for example. The SQUID is used

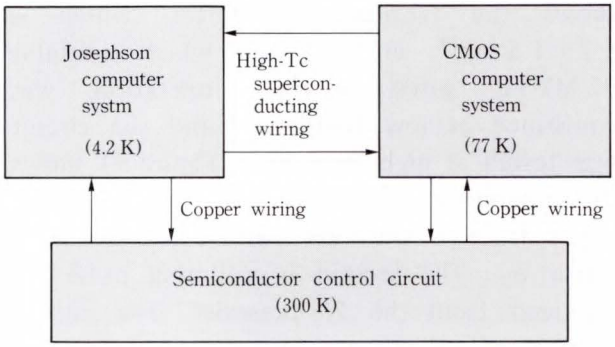


Fig. 57—Hybrid computer system.

to measure an extremely faint magnetic field. Magnetic field from the human body can be detected with the SQUID for obtaining magnetic cardiograms. To determine magnetic field distribution in the body, a large number of channels of SQUID are required, because the magnetic fields in many places should be measured simultaneously. For a 1 000-channel system, several thousands of cables would be needed to connect the chips in the cryogenic container and the electronic circuits at room temperature. As described in the following, a SQUID system can be integrated with a feedback circuit on a single chip[52),53)]. By using such a chip, information that is easy to process using the Josephson computer can be obtained in digital form from the SQUID, and thus the number of cables can be remarkably reduced.

8.2 Hybrid computer

The use of high-Tc superconducting materials in interconnecting wiring between circuit boards would enable development of a hybrid computer system consisting of Josephson devices and cooled CMOS (see Fig. 57). In such a computer system, large-scale signal processing would be done by the CMOS computer, while high-speed processing would be done by the Josephson computer. Both computers would be connected with high-Tc superconducting transmission lines. One way to promote the actual development of the Josephson computer may be to install Josephson devices as components of large-scale computer.

The Josephson computer previously described is also a kind of hybrid computer

because large-scale memory operates at room temperature. In such a computer system, semiconductor circuits must be installed very close to the Josephson circuits. This is important for signal transmission between both types of circuits. It is already possible to make a cryogenic container in which signal transmission is possible within 5 cm between room temperature and the temperature of liquid helium[54].

9. Conclusion

This paper has described our recent progress in Josephson integrated circuit development. Rapid progress has been made ever since niobium replaced lead alloys as the junction material. It is now possible to fabricate such circuits as processors, memory, and interfaces between Josephson and semiconductor circuits.

The early 1980s were troubling times for engineers working on fabricated lead-alloy circuits that seldom worked as intended. Moreover, such difficulties as a low fabrication yield, the large scattering of critical currents for junctions, unstable junction characteristics, and malfunctions due to flax trapping and punch-through, were very annoying. These difficulties were considered fatal to attempts being made to develop a Josephson computer. Although we introduced the niobium junction in 1984, it was difficult to obtain a good junction during the early stages of development. On the other hand, after successfully developing an effective fabrication process, the junctions were impressively stable, reliable, reproducible, and controllable. Thus, most problems were solved simultaneously and great promise emerged from great difficulty.

Part I of this paper details the use of niobium junctions. Niobium is possibly the best material for Josephson junctions, much as silicon is the best material for transistors because both are single-atom materials. Because compound or alloy materials are difficult to use with electron devices, the pairing of niobium and aluminum is more effective than could have possibly been expected.

We developed the MVTL gate and 3-phase powering for high-speed circuits. The MVTL offers many excellent features, the most important being high speed and a large operating margin. The 1.5 ps/gate is the world's fastest gate delay. We now plan to develop a subps/gate with MVTL. Three-phase powering is ideally suited to Josephson junctions operation. Three-phase powering makes it possible to ensure a smooth stream of data, which is vital for ultra-fast circuit operation.

Without the key techniques described in this paper, it would not be possible to create Josephson junction high-speed circuts. The next step is to install chips in a cryogenic refrigerator to demonstrate their high performance capabilities at the system level.

To build a Josephson computer, new techniques for packaging and refrigeration must be developed. Packaging technique is very important in terms of building an ultra-fast computer because it determines system speed. Although little is known about multi-chip operation, the development of a high-speed multi-chip packaging is essential. Refrigeration is also important for the Josephson computer. For this reason, a closed-cycle refrigeration system that is quiet, small and highly efficient must also be developed. We are now developing these techniques toward the realization of the world's first Josephson computer.

10. Acknowledgement

This paper contains information complied on high-speed digital circuits developed at our laboratories during the last five years. The people mainly responsible for developing these circuits include Messrs. N. Fujimaki (MVTL gate and shift register), H. Suzuki (4 K-bit memory and high-voltage driver), S. Kotani (16-bit ALU, 4-bit microprocessor, 4-bit processor, and 8-bit DSP), S. Ohara (serial-parallel converter), and A. Inoue (8-bit DSP).

The decision to replace the junction material in 1984 was a decisive turning point for us in our progress toward Josephson computer development. The introduction of the niobium junction gave ultra-fast computers a new life. None of this would have been possible, however, without the enthusiasm and effort of my colleagues Messrs. T. Imamura, N. Fujimaki,

S. Morohashi, H. Tamura, H. Suzuki, H. Hoko, S. Kotani, S. Ohara, A. Yoshida, and A. Inoue. The author wishes to thank these people for the honor and pleasure of working with them during the most exciting period in the history of Josephson computer development.

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Josephson Integrated Circuits III
A Single-Chip SQUID Magnetometer

• Norio Fujimaki *(Manuscript received September 3, 1990)*

Superconducting Quantum Interference Devices (SQUIDs) can measure magnetic fields as low as femto tesla and have been used for biomagnetism, resource surveying, and physical or geophysical measurement. Unlike the conventional SQUID, the single-chip SQUID is the first device that intergrates both a SQUID sensor and a feedback circuit on the same chip. This reduces the number of external cables. Also, the output can be processed with Josephson digital circuits in the cryogenic environment. These advantages open up the possibility of constructing a multichannel system with an array of more than 100 SQUIDs, which is required to measure a magnetic field map in detail.

1. Introduction

The superconducting quantum interference device is a superconducting ring that includes Josephson junctions. It can be used as a magnetic sensor with high sensitivity. From early on, two types of SQUIDs (rf SQUID and dc SQUID) has been used[1]. The rf SQUID is a superconducting ring that has an inductance and a Josephson junction. It is coupled to an LC resonator and is fed with an rf current. The dc SQUID consists of a superconducting inductance and two Josephson junctions. It is biased with direct current. Recently the dc SQUID has been more commonly used for practical applications, because of its higher sensitivity.

The SQUID can measure magnetic fields as low as femto tesla (fT). Other magnetic sensors, such as the Hall effect device and flux gate, cannot measure magnetic fields at less than 100 pico tesla (pT). Thus, the SQUID is an indispensable device for measuring magnetic fields in the range between 100 pT and 1 fT. It has been widely used for biomagnetism[2)-4)], susceptometer, and geophysical measurement[5]. Other applications[4),6)] are resource surveying, nondestructive measurement of magnetic impurity in products, gravity wave detection, and monopole detection.

Rapid progress has occurred in the area of biomagnetism[4),7)]. Many researchers have measured magnetic fields from the brain, heart, and other tissues. The construction of a SQUID sensor array which measures the magnetic field map more quickly would be highly desirable. The SQUID array is called a multichannel SQUID.

In the continuing attempts to construct a multichannel system, the single-chip SQUID[8] is a promising device. It enables us to construct more than 100 channels. This paper reviews the principle of operation, design and performance of the single-chip SQUID.

2. Target

2.1 Multichannel requirements

For biomagnetic applications, a multichannel SQUID system is desirable for measuring the magnetic field map. Recently many efforts have been made to increase the number of channels, i.e. the number of sensors in the array, as shown in Fig. 1. BTI developed 5-channel (1984), 7-channel (1987), and 37-channel (1989) systems. Helsinki University of Technology has made 7-channel (1987) and 24-channel (1989) systems. Siemens made a 37-channel system in 1989. Nevertheless, a still larger number of channels are said to be necessary for practical application. Extrapolations were discussed by

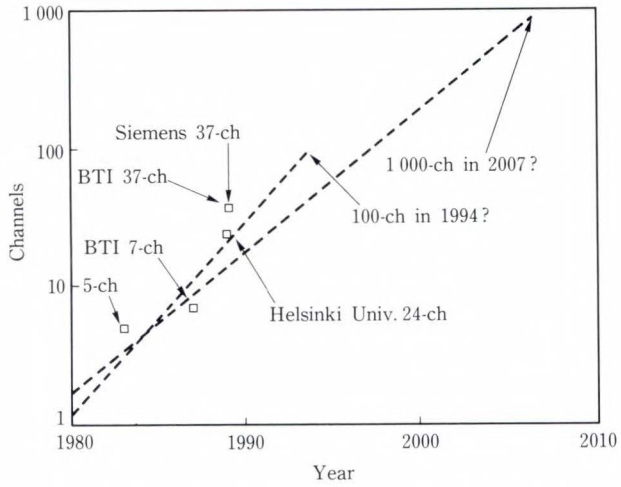


Fig. 1—The evolution of the number of channels[9].

Hämäläinen[9] and other participants at the 7th International Conference on Biomagnetism as shown in Fig. 1. Many more projects on a multichannel SQUID have been undertaken by other companies and research organizations.

It is not yet known what would be the sufficient number of channels. As the magnetic field map is used to calculate current sources in tissues, further research on the inverse problem[2),7)] might give an answer concerning the sufficient number of channels required. The following discussion is only a simple estimation that we are able to make at this point in time. Let us assume that the brain is a sphere with the radius of 10 cm, and its upper surface area is about 600 cm^2. In order to cover this whole area with pickup coils at each 2 cm mesh point, the number of channels required would be 150. From this simple estimation, we imagine that 100 channels or even 1 000 channels might be required for future applications.

As the number of channels increases, the number of cables required to connect the room temperature electronics and the SQUID sensors in the cryogenic environment (usually liquid helium) increases too. This causes larger heat flow and larger crosstalk between cables. The former causes a higher level of liquid helium consumption. Let us take an example, 1 W heat flowing from 300 K to 4.2 K through copper lines 1 m long and with 6.6 mm^2 cross-sectional area[10]. This would be equivalent to

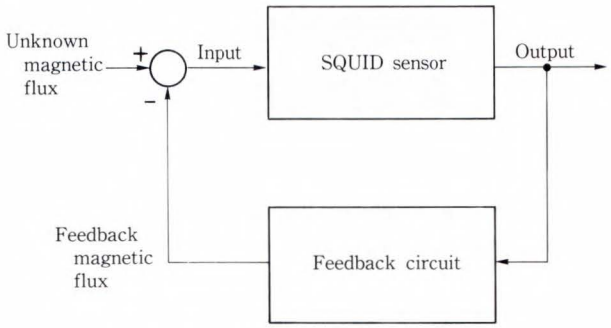


Fig. 2—Block diagram of the SQUID.

210 thin copper cables of 0.2 mm in diameter. The 1 W heat flow consumes 1.4 litres liquid helium in an hour.

When using a closed-cycle refrigerator to supply liquid helium for the SQUID system, a larger heat flow requires greater refrigeration power. For example, the cooling of 1 W requires more than 1 kW refrigeration power.

2.2 Fundamental operation of SQUID

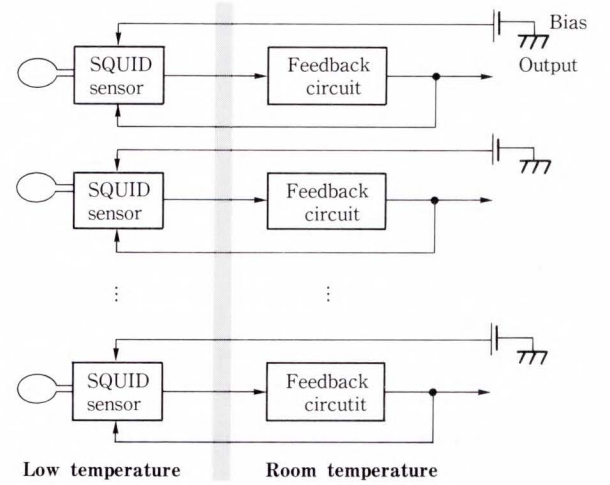
A SQUID sensor is operated in a feedback loop[1] as shown in Fig. 2. The SQUID sensor receives an input magnetic flux and produces an output. The feedback circuit receives this output, and returns the feedback flux to the SQUID sensor. The feedback flux is given with the polarity changed in order to cancel the unknown magnetic flux. The feedback loop thus maintains the sum of the unknown flux and the feedback flux at zero. We can ascertain the unknown flux by measuring the feedback flux. This null method enables us to measure the unkown magnetic flux without being affected by nonlinearity of the sensor, or additional amplifier drift.

2.3 Analog SQUID

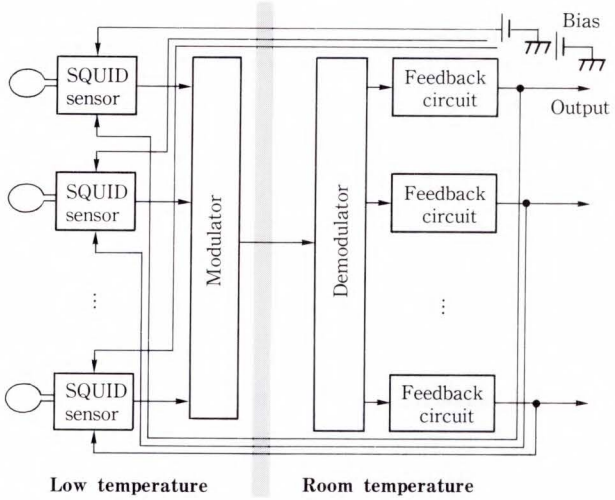
The analog SQUID means a conventional dc or rf SQUID, where the output is an analog voltage. The analog feedback circuit receives the output, and gives a feedback flux to the SQUID sensor.

2.3.1 Parallel method

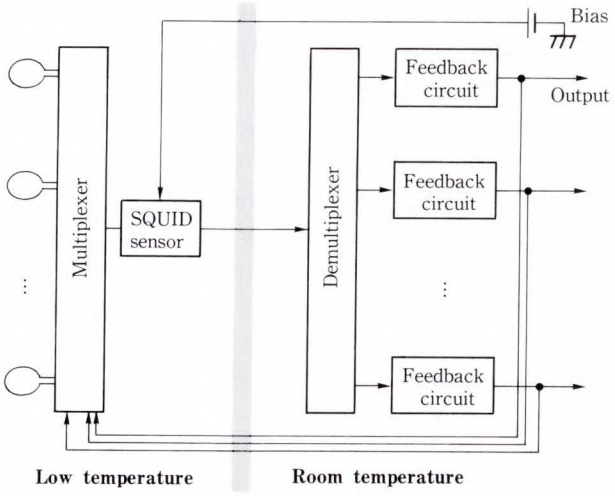
Until now, all practical multichannel systems have been constructed by arranging many analog SQUIDs in parallel as shown in Fig. 3a). With



a) Parallel method



b) Frequency division multiplex



c) Time division multiplex

Fig. 3—Multichannel system with the conventional dc SQUID.

this parallel method, each sensor requires a feedback circuit[4), 11)] which means a large amount of electronics operating at room temperature. Each dc SQUID requires cables for transmitting bias, output, and modulation or feedback. For these signals, each requires three pairs of cables. Each pair consists of one signal cable and one ground cable twisted together. So, for an n-channel SQUID system in the parallel method, $6n$ cables are required. If n is 100, the number of cables would be 600. On the basis of the previous estimation of heat flow, 600 cables would cause about 3 W heat flow. This indicates that if we wanted to construct a multichannel system with more than 100 channels in the parallel method, heat flow might be a serious problem.

2.3.2 Frequency division multiplex

To overcome this problem, the frequency division multiplex method[12)] has been proposed and tested as shown in Fig. 3b). In this method, the dc SQUIDs are modulated at different frequencies to each other. The modulated output voltages are transmitted through a single output cable. They are demodulated by the electronics operating at room temperature. This method reduces the number of output cables for multichannel SQUID systems based on the conventional dc SQUID technology. In this case, the maximum number of channels is limited by the amount of crosstalk caused by nonlinearity of the SQUID.

2.3.3 Time division multiplex

The time division multiplex method[12)] has also been proposed, as shown in Fig. 3c). In this method, many pickup coils and one SQUID are used. The superconducting multiplexer selects one of the pickup coils and connects it to the SQUID sensor.

In this method, the multiplexer is required to maintain the superconducting state in the selected connection line and to break the superconducting state for those lines not in use. One possible candidate device for this multiplexing operation is a superconducting thin film which is heated by the light that is conducted by an optical fiber. Another candidate is a superconducting three-terminal device, which can select a superconducting or normal state by

changing the gate voltage. This method requires further study of these multiplexing devices.

2.4 Digital SQUID

Another approach is the digital SQUID[8), 13)], which is described in this paper.

2.4.1 Definition of digital SQUID

The digital SQUID is also operated in a feedback loop as shown in Fig. 2. But, unlike the analog SQUID, the output of the SQUID sensor is a pulse sequence. The digital feedback circuit receives this output pulse and gives a feedback flux to the SQUID sensor. This is called a digital feedback loop. The sensor with pulse output can be called a digital SQUID sensor.

2.4.2 Advantages of digital SQUID

The digital feedback loop has the following two advantages.

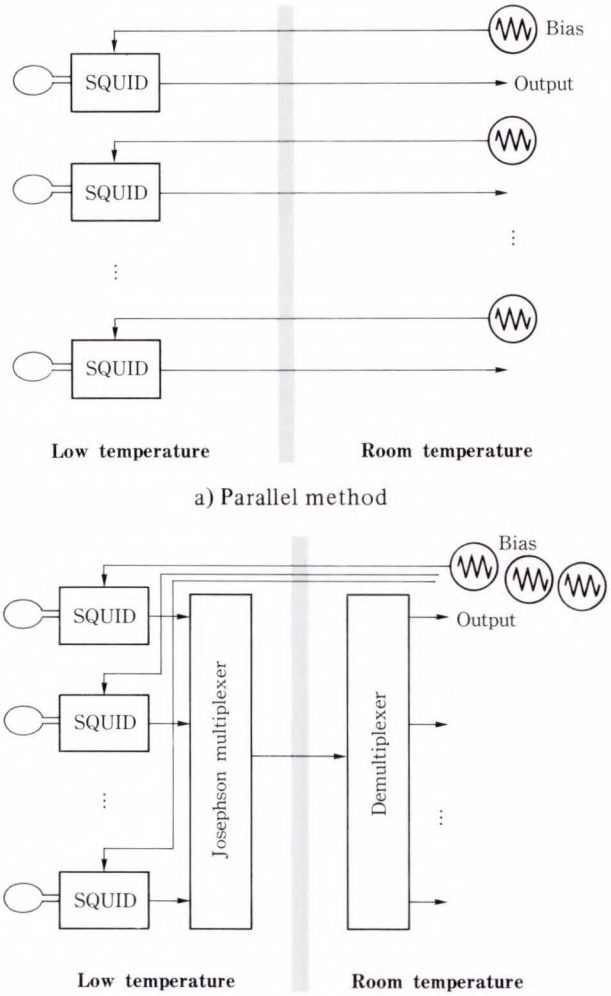
1) The signal-to-noise ratio of the output becomes high

The output cable connecting the SQUID chip in the cryogenic environment and the electronics at room temperature is typically a few meters long. In the analog feedback loop, the output voltage to be resolved is of the order of $nV/Hz^{1/2}$ and therefore very sensitive to environmental noise. In the digital feedback loop, the output pulse amplitude is typically mV. Besides, it is only necessary to ascertain whether or not there is a pulse.

2) The output pulse can be processed by Josephson circuits in the cryogenic environment

First, this enables us to integrate the digital feedback circuit into the SQUID chip, thus creating a single-chip SQUID. In contrast to this, the analog feedback circuit requires a lock-in-amplifier which is not easy to integrate into the cryogenic chip because of the restricted performance of the superconducting analog circuit.

As the single-chip SQUID has a fully integrated feedback circuit, a cable for an external feedback loop is not necessary. Each single-chip SQUID requires one cable for bias and one cable for output. Due to the high signal-to-noise ratio of the output pulse, a common ground can be used. If we construct a system with n channels, as shown in Fig. 4a), the number of cables is



a) Parallel method

b) Time division multiplex

Fig. 4—Multichannel system with the single-chip SQUID.

$2n$. This is 1/3 of the number required by the parallel method with analog SQUID.

Secondly, as the output is a pulse, it becomes possible to process this by Josephson digital circuits in the cryogenic environment. The stable and reproducible operation of Josephson digital circuits have been reported[14)]. For example, if we used a Josephson multiplexer, a time division multiplex could be made[15)], as shown in Fig. 4b). The outputs from many single-chip SQUIDs go to the Josephson multiplexer to be arranged in time division on a single output cable.

3. Digital SQUID sensor

3.1 Principle of operation

In order to produce the pulse sequence in the cryogenic environment, A/D conversion is

necessary. The simplest way to do this is to use a Josephson comparator which receives the unkown magnetic flux and produces a comparator output[8].

3.1.1 Josephson comparator

Figure 5 shows the Josephson comparator. It is a 2-junction interferometer. This comparator is used in the single-chip SQUID. It receives the unkown magnetic flux and produces a comparator output in the form of a pulse sequence. The dc SQUID is also a 2-junction interferometer. But unlike the dc SQUID, the comparator has no shunt resistor with Josephson junction and has a definite hysteretic I-V curve as shown in Fig. 6. When the bias current is lower than the threshold value, the comparator is in the zero voltage state. When the bias current is increased beyond the threshold value, it switches to the finite voltage state of the order of mV. The finite voltage state is maintained until the bias is lowered to less than the value, I_{min}. It is typically much smaller than the threshold value.

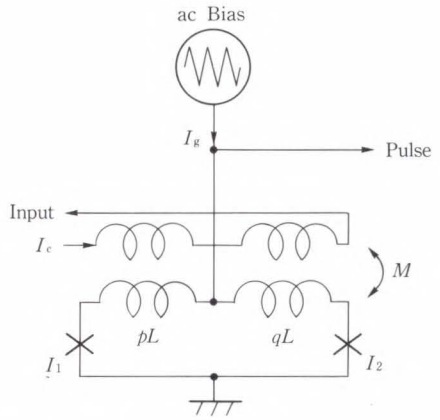


Fig. 5—Circuit of a Josephson comparator. It is a 2-junction interferometer without shunt resistor.

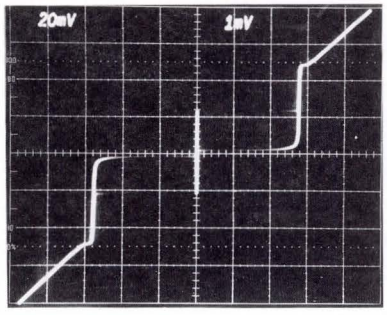
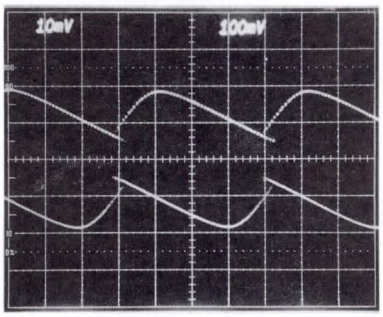


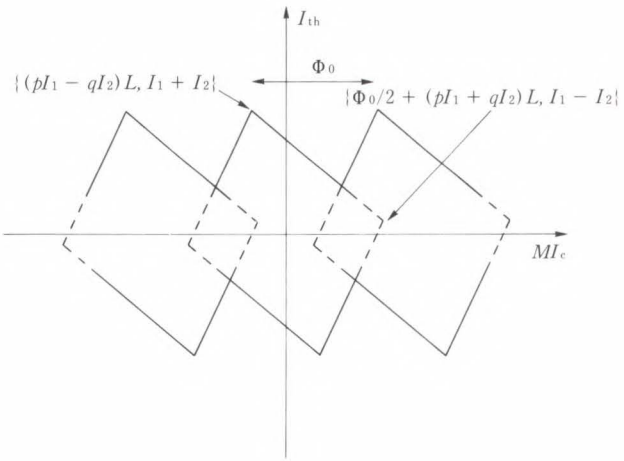
Fig. 6—I-V curve of the Josephson comparator.

1) Threshold curve

The threshold value of the Josephson comparator is a function of the input magnetic flux or the current I_c flowing through a magnetically coupled line. Figure 7 shows the threshold curves of the 2-junction interferometer. It consists of the same closed shapes placed periodically along the horizontal axis. The periodicity is the flux quantum Φ_0 which is defined by Planck's constant over twice the electron's charge, $h/(2e)$, and is $2\,067 \times 10^{-15}$ Wb. Each closed curve is called a mode and is numbered thus -1-mode, 0-mode, 1-mode, etc. When the operating point is in m-mode, almost m flux quanta are entered in the interferometer. The theoretical curve on the bending line approximation is shown in Fig. 7b).



a) Measured



b) Theoretical (Theoretical curve is based on bending line approximation)

Fig. 7—Threshold curve of the Josephson comparator.

When the operating point crosses the solid threshold curve in Fig. 7b), the interferometer switches from the zero voltage state to the finite voltage state. On the other hand, when it crosses the dashed curve, the interferometer changes its state from one mode to another.

The shape of the threshold curve depends on the critical currents (I_1 and I_2) of the Josephson junctions, the inductance L, and the ratio of right and left inductances, q/p $(p+q=1)$[16]. The coordinates of the two points shown in Fig. 7b) are exact values. The curve is symmetrical about its origin. The exact whole curve can be obtained to calculate the maximum bias current I_g using the following two static equations. The first equation is Kirchhoff's law.

$$I_g = I_1 \sin\phi_1 + I_2 \sin\phi_2 . \qquad \ldots\ldots (1)$$

The second equation is the quantum condition. The increase of the phase of the superconducting order parameter is permitted by only two times integer n along the superconducting closed loop. There are phase differences of ϕ_1 and ϕ_2 at the two Josephson junctions. In the superconductors, the phase change is expressed by the following equation,

$$\nabla\phi - \frac{2\pi}{\Phi_0} A = \mu_0 \lambda_L^2 \left(\frac{2\pi}{\Phi_0}\right) i, \qquad \ldots (2)$$

where A is the vector potential, μ_0 is the permeability in vacuum, λ_L is the London penetration length (85 nm for Niobium), i is the current density. The current density is negligibly small in the region far inside the superconductor. Then, by integrating Equation (2) on the path far inside the interferometer ring, we obtain the next quantum condition,

$$\phi_1 - \phi_2 + \frac{2\pi}{\Phi_0}\Phi = 2n\pi,$$

$$\Phi = pLI_1 \sin\phi_1 - qLI_2 \sin\phi_2 - MI_c, \qquad (3)$$

where Φ is the magnetic flux interlinked in the interferometer ring.

2) Operation

The alternating current (ac) bias is applied to the 2-junction interferometer. The bias amplitude is adjusted to the threshold value at the vertical axis as shown in Fig. 8. When the input is positive, the interferometer produces positive pulses. When the input is negative, a negative pulse sequence is produced. The pulse shape is definite due to the hysteretic I-V curve shown in Fig. 6. So, the interferometer discriminates between the positive and negative input. It operates as a comparator.

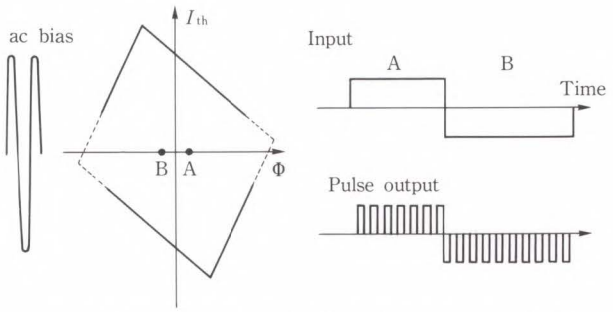


Fig. 8—Operation of the Josephson comparator.

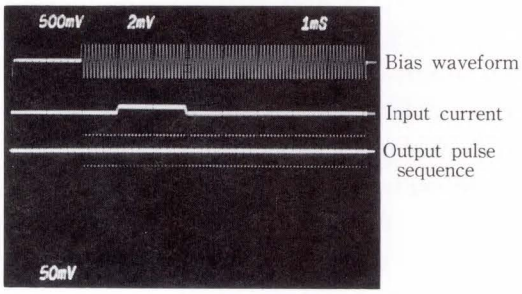


Fig. 9—Measured operation of the Josephson comparator.

The above is true for a large input. When the input is small, however, the fluctuation effect, such as thermal noise or external noise, should be considered. Due to this, even when the input was positive, a negative pulse sometimes appeared as shown in Fig. 9.

As the photograph was taken of the oscilloscope during many scans, the intensity represents the probability of the pulse occurrence. Higher intensity means higher switching probability. Therefore, the comparator output is not determined strictly by the input flux; only the switching probability is determined by the input flux. The switching probabilities, p^+ for positive polarity and p^- for negative polarity, changes from zero to one in a smooth curve as shown in Fig. 10a). As a result, the average number of positive pulses minus the number of negative pulses, $p^+ - p^-$, becomes a smooth curve. Due to

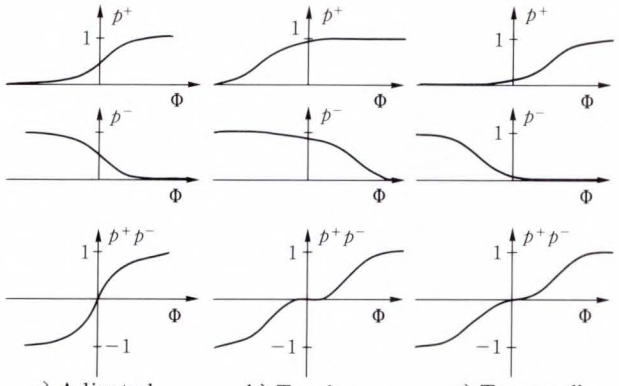


Fig. 10—The switching probability p^+ for positive bias, p^- for negative bias, and their difference $p^+ - p^-$, for three bias amplitudes.

the smoothness of the curve, it is not necessary to adjust the bias amplitude exactly to one point of the threshold value. However, it is necessary to adjust the bias amplitude to about one percent. If the bias amplitude is too large or too small, the interferometer becomes insensitive to small flux, as shown in Figs. 10b) and c). The derivative, $\partial p/\partial \Phi$, determines the sensitivity of the SQUID sensor and the response speed. Larger $\partial p/\partial \Phi$ gives higher sensitivity and a faster response speed, which will be discussed later.

Some other variations in the operation of the 2-junction interferometer can be considered. In the above discussions, the operating point moves along the vertical axis with bipolar ac bias. But it is possible to move the operating point along an axis other than the vertical. It is also possible to use monopolar ac bias. Further, the modulation of the input current with a different frequency enables us to operate it avoiding the insensitive region by sacrificing the response speed.

3.1.2 Other methods of pulse output

Other methods of digitalization have been reported. In the first report on the digital SQUID[13], the operations of receiving signals and comparation were divided into two components, a dc SQUID and a Josephson comparator, which were integrated on the same chip. In this method, the dc SQUID receives the unknown magnetic flux and produces an analog voltage. The comparator receives it and produces a pulse sequence. This is sent to the digital counter at room temperature, which produces feedback flux and sends it back to the dc SQUID. This method enables us to design optimally for each operation, but it requires two interferometers with dc bias and ac bias, respectively. The noise was limited by the dc SQUID, not by the comparator.

Another comparator called DCFP or QFP[17] has been proposed and tested. It is a 2-junction interferometer contained in a closed superconducting ring. Its output is not a voltage, but a magnetic flux. When an excitation current is applied, it changes the small input flux to a large magnetic flux with the same polarity. To receive the magnetic flux change, a superconducting storage loop circuit has been proposed[18]. This is required to control the shape of the short voltage pulse and to control the transient response for stable operation. It has similarities with the superconducting feedback circuit described in this paper, but the operation is different. Further research will be required to characterize this device for use as a magnetic sensor.

In the following sections, we restrict ourselves to a discussion of the simplest digital SQUID sensor, the Josephson comparator, which receives the input flux directly.

3.2 Sensitivity

3.2.1 Switching probability

In the case of the analog SQUID, the thermal noise appears as a noise voltage on the output[1),11)]. The output is the sum of a voltage due to the input flux and a voltage due to the thermal noise. In the case of the digital SQUID, the output is a pulse sequence and the thermal noise appears as a fluctuation of the output pulse. If we suppose there is positive input flux without noise, the digital SQUID sensor produces a positive pulse and no negative pulse at each bias clock. But, the real SQUID does have thermal noise, and as discussed in Subsec. 3.1.1, a positive pulse is sometimes lost and a negative pulse is sometimes produced as shown in Fig. 11. The input flux only determines the probability of pulse occurrence. Switching probability, p of the digital SQUID sensor can

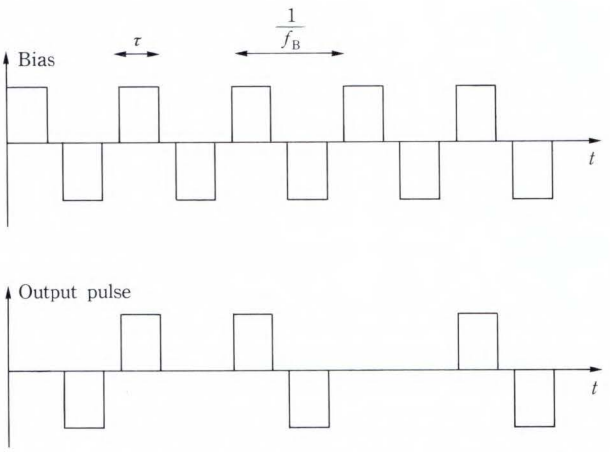


Fig. 11—The bias waveform and the output pulse of the Josephson comparator.

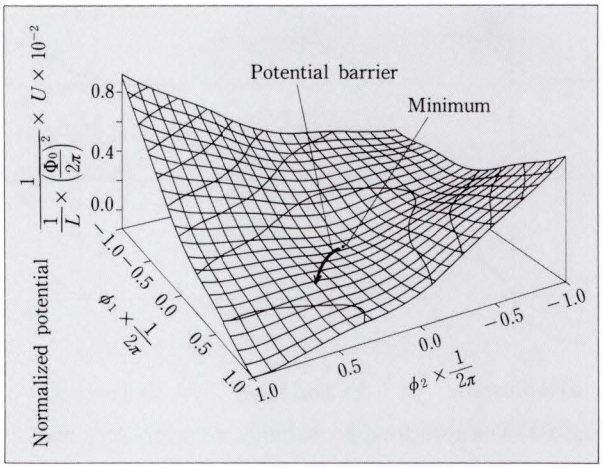


Fig. 12—A potential $U(\phi_1, \phi_2)$ calculated numerically for parameters of $LI_0 = 0.33\Phi_0$, $\Phi = 0$, $p = 0$, $q = 1$, and $I_g/I_0 = 1$.

be obtained as follows[19].

The characteristics of the ideal Josephson junction is expressed by the following Josephson equations[20],

$$i = I_0 \sin\phi, \qquad \cdots\cdots\cdots\cdots (4)$$

$$v = \frac{\Phi_0}{2\pi} \frac{d\phi}{dt}, \qquad \cdots\cdots\cdots (5)$$

where i is the current and I_0 is the critical current of the Josephson junction, v is the voltage of the junction, ϕ is the phase difference of the order parameter in the Josephson junction. The real Josephson junction has a junction capacitance and a conductance in parallel. Then, the circuit equations of the SQUID sensor are

$$\left(\frac{\Phi_0}{2\pi}\right)^2 \left(C \frac{d^2\phi_1}{dt^2} + G \frac{d\phi_1}{dt}\right) = -\frac{\partial U}{\partial \phi_1}$$

$$\left(\frac{\Phi_0}{2\pi}\right)^2 \left(C \frac{d^2\phi_2}{dt^2} + G \frac{d\phi_2}{dt}\right) = -\frac{\partial U}{\partial \phi_2}, \qquad (6)$$

where the potential U[16] is expressed by

$$U(\phi_1, \phi_2) = \frac{\Phi_0 I_0}{2\pi} \left\{(2 - \cos\phi_1 - \cos\phi_2) - \phi_1 \left(p \frac{I_g}{I_0} + \frac{\Phi}{LI_0}\right) - \phi_2 \left(q \frac{I_g}{I_0} - \frac{\Phi}{LI_0}\right) + \frac{\Phi_0}{4\pi LI_0} (\phi_1 - \phi_2)^2\right\}, \qquad \cdots\cdots (7)$$

where we assume two Josephson junctions in the digital SQUID sensor have the same critical current I_0, capacitance C, and conductance G. These equations are the same as those for the motion of a ball in 2-dimensional potential $U(\phi_1, \phi_2)$[20]. A potential map for a certain bias current I_g is shown in Fig. 12. When a positive I_g is applied, the potential decreases along the $(p\phi_1 + q\phi_2)$ axis with undulation due to the $\cos\phi$ term in the potential Equation (7). For small bias I_g, the potential has periodical local minima. In the mechanical analog, the ball is trapped in one of the minima. As the bias is increased, the potential barrier becomes smaller. If there is no noise, the ball remains in the minimum. When the bias current is applied beyond the threshold value, the potential barrier is lost and the ball starts to move continuously toward the lower potential. Phases ϕ_1 and ϕ_2 increases continuously. From the Josephson Equation (5), we can see that this corresponds to the finite voltage state. In this case, the digital SQUID sensor switches from the zero voltage state to the finite voltage state.

Due to thermal noise, the ball moves randomly in the neighborhood of the potential minimum. Even when the bias current is lower than the threshold value, it has a finite probability of overcoming the potential barrier. This probability p is the switching probability of the digital SQUID sensor.

According to the mechanical analog, the hysteretic I-V curve can be understood as follows. As we do not shunt the Josephson junctions with low resistors, there is only a small loss. Then, once the ball has overcome the

potential barrier, it continues to fall toward the lower potential. Due to the ball's inertia, the voltage state is maintained until the bias decreases below the low value, I_{min}. Due to the hysteresis, the digital SQUID sensor produces a definite pulse.

In the following discussion, we assume that the bias waveform is a pulse as shown in Fig. 11. The switching probability was obtained on the basis of the transition state method[21] for one dimensional consideration as

$$p_0 = e^{-\frac{\Delta U}{kT}}, \quad \cdots\cdots\cdots (8)$$

$$p = 1 - (1 - p_0)^{f_p \tau}, \quad \cdots\cdots (9)$$

where ΔU is the potential barrier, k is the Boltzmann constant, T is the temperature, f_p is the Josephson's plasma frequency $\{= (1/2\pi)\sqrt{2\pi I_0/(\Phi_0 C)}\}$, and τ is the bias pulse width.

Equations (8) and (9) lead us to the following reasoning. The ball in the mechanical analog oscillates in the potential minimum with a frequency of the Josephson plasma frequency f_p. At every oscillation, the ball attempts to overcome the potential barrier. p_0 is the probability of overcoming the potential barrier, ΔU, at each attempt of the Josephson oscillation. $f_p \tau$ attempts determine the probability of switching p in one bias clock.

When operating in a feedback loop, the input flux is around zero; this is sufficient data for us to calculate the probability at zero input. The potential barrier ΔU can be obtained by numerical calculation of Euation (7). Using Equations (8) and (9), the switching probability p vs the normalized bias amplitude i_g is calculated as shown in Fig. 13. The numerical calculation of the $\partial p/\partial \Phi$ is also shown in Fig. 14.

In the above discussion, the probability was obtained by the approximation of one-dimensional transition state method. By extending the transition state method[21] to the two-dimensional lossless case, we obtain

$$p_0 = f_p \frac{\alpha_1 \alpha_2}{\gamma_2} e^{-\frac{\Delta U}{kT}}, \quad \cdots\cdots (10)$$

$$p = 1 - e^{-p_0 \tau}, \quad \cdots\cdots\cdots (11)$$

where α_1 and α_2 are the square roots of curvatures in the two orthogonal axes at the potential minimum, and γ_2 is the square root of curvature at the saddle point of the potential barrier along the axis normal to the ball's overcoming movement. But the calculated result is nearly the same as that shown in Figs. 13 and 14. There is a

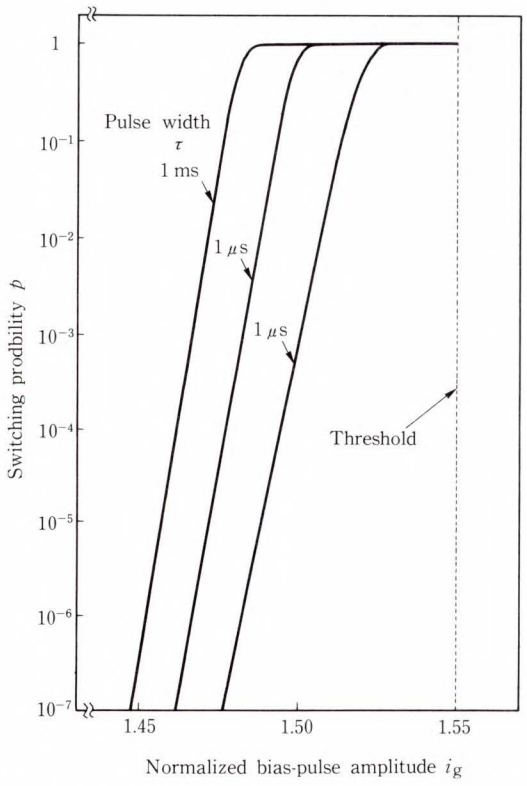


Fig. 13—Calculated switching probability vs normalized bias amplitude i_g ($= I_g/I_0$).

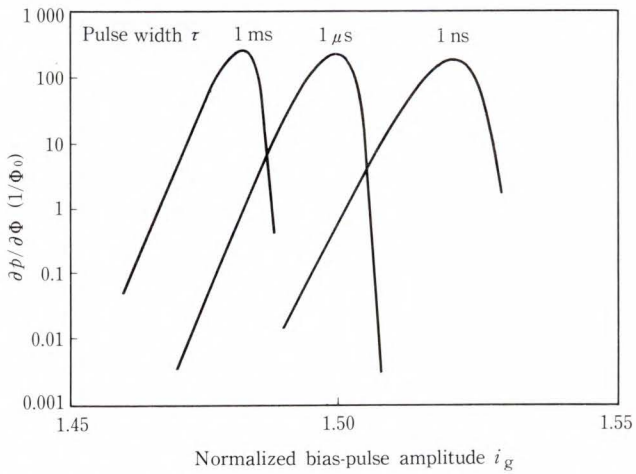


Fig. 14—Calculated $\partial p/\partial \Phi$ vs normalized bias amplitude i_g.

result of about ten percent change in the minimum flux spectral density.

3.2.2 Power spectral density of output pulse

For simplicity, we suppose the output pulse is a delta function. The output waveform $x(t)$ is written as

$$x(t) = \sum_{n=-\infty}^{\infty} \left[x_n^+ \delta(t - nT_B) - x_n^- \delta\{t - (n + \frac{1}{2})T_B\} \right], \quad T_B = \frac{1}{f_B}, \quad \ldots (12)$$

$$\overline{x_n^{\pm}} = p_n^{\pm}, \quad \ldots\ldots\ldots (13)$$

where bar means the ensemble average. This approximation causes an error in the spectrum only at a frequency higher than the bias frequency f_B. When we want to know the Fourier component at a low frequency region less than the bias frequency f_B, this approximation is not problematic. The ensemble average of the Fourier component of the output pulse in the time period of T, X_T and the power spectral density S_x can be obtained by the following equations,

$$X_T(f) = \int_{-T/2}^{T/2} x(t) e^{-i\omega t} dt, \ \omega = 2\pi f, \quad (14)$$

$$S_x(f) = \lim_{T\to\infty} \frac{\overline{2|X_T(f)|^2}}{T}, \quad \ldots (15)$$

where S_x is defined for positive frequency f. If the bias amplitude and the signal flux do not vary with time, the switching probability $p_n^{\pm}$ is independent of n. This instance is dealt with in Ref. 19. Now we wish to consider a more general instance, where a small signal flux $\Phi_s(t)$ is applied. Then, the switching probability depends on time as expressed by

$$p_n^{\pm} \simeq p \pm \left(\frac{\partial p}{\partial \Phi}\right) \hat{\Phi}_s(nT_B). \quad \ldots (16)$$

The quantity $\hat{\Phi}_s$ is defined by

$$\hat{\Phi}_s(t) = \frac{1}{\tau} \int_{-\tau/2}^{\tau/2} \Phi_s(t + t') dt', \quad \ldots (17)$$

which has the following Fourier transform.

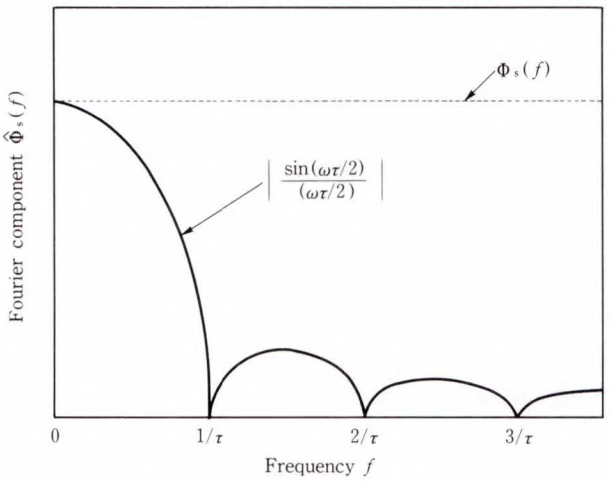


Fig. 15—The relation between $\hat{\Phi}_s$ and Φ_s.

$$\hat{\Phi}_s(f) = \frac{\sin(\omega\tau/2)}{(\omega\tau/2)} \Phi_s(f), \quad \ldots (18)$$

$\hat{\Phi}_s$ is the average of Φ_s at each time. The average is calculated by the time period of bias pulse width τ. This comes from the fact that the switching probability p is determined by all of the attempts in a bias clock. This averaging effect reduces the high frequency component of the signal flux spectral density. The reduction is a factor of $\{\sin(\omega\tau/2)/(\omega\tau/2)\}^2$ as shown in Fig. 15.

From Equations (12) to (16), we obtain the power spectral density of the output pulse X as follows.

$$S_x(f) = 4f_B p(1-p) - 4f_B \left(\frac{\partial p}{\partial \Phi}\right) \phi_{\hat{\Phi}}(0) + 8f_B^2 p^2 \sum_{n=-\infty}^{\infty} \delta\{f - (2n+1)f_B\} + 4f_B^2 p^2 \left(\frac{\partial p}{\partial \Phi}\right)^2 \sum_{n=-\infty}^{\infty} S_{\hat{\Phi}}(f + 2nf_B), \quad (19)$$

where $\phi_{\hat{\Phi}}$ is the autocorrelation function of the $\hat{\Phi}_s$. $S_{\hat{\Phi}}$ is the power spectral density of $\hat{\Phi}_s$. In the right side of Equation (19), the first and third terms represent the thermal noise. The second term comes from the probability change due to the signal flux. This is small compared with the first term, if the signal is small enough. The fourth term comes from the signal flux.

Equation (19) shows the following important points.

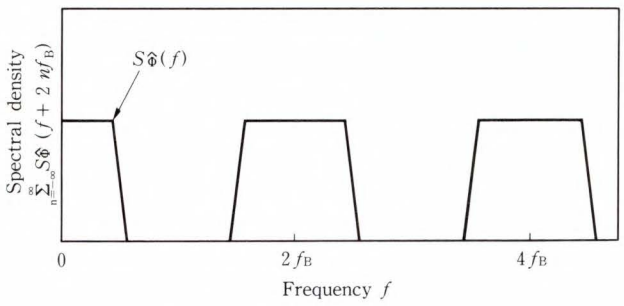


Fig. 16—Spectral density with aliasing effect.

1) Thermal noise appears as white noise in the frequency region below the bias frequency f_B. It is represented by the first term on the right of Equation (19).
2) Signal flux spectrum appears in the output, as multiplied by the factor of $\{\sin(\omega\tau/2)/(\omega\tau/2)\}^2$, due to the averaging effect.
3) Signal spectrum appears periodically in the output spectral density, with the period of $2f_B$ as shown in Fig. 16. This is the same as the aliasing effect that appeared in sampling. The digital SQUID sensor operates as a sampler.

3.2.3 Thermal-noise-limited sensitivity

The biomagnetic signal has frequency components from 0.1 Hz to 1 000 Hz, while the bias frequency is typically from 1 MHz to 100 MHz. It is sufficient for us to attend to the component at a frequency lower than the bias frequency f_B only. In this case, the relationship between the spectral density of the output pulse and the signal flux is expressed by the coefficient $4f_B^2(\partial p/\partial\Phi)^2$ of the fourth term on the right side of Equation (19).

By dividing the thermal noise $4f_B p(1-p)$ by the above coefficient, we obtain the equivalent flux spectral density of the thermal noise as follows[19].

$$S_\Phi = \frac{p(1-p)}{f_B\left(\frac{\partial p}{\partial\Phi}\right)^2} . \quad \cdots\cdots\cdots\cdots (20)$$

As we cannot detect a signal flux smaller than this spectral density, this is the fundamental limit on the sensitivity of the SQUID sensor. It is determined by the switching probability p and its derivative $\partial p/\partial\Phi$. Figure 17 shows the numerical calculation for interferometer inductance L of 6.9 pH and temperature at 4.2 K. Larger L gives lower sensitivity. For example, the minimum flux spectral density was obtained as $3\times10^{-6}\Phi_0/\mathrm{Hz}^{1/2}$ for 6.9 pH with the bias pulse width of 1 ns and bias frequency at 1 MHz. However, for 15 pH it becomes as large as $5\times10^{-6}\Phi_0/\mathrm{Hz}^{1/2}$.

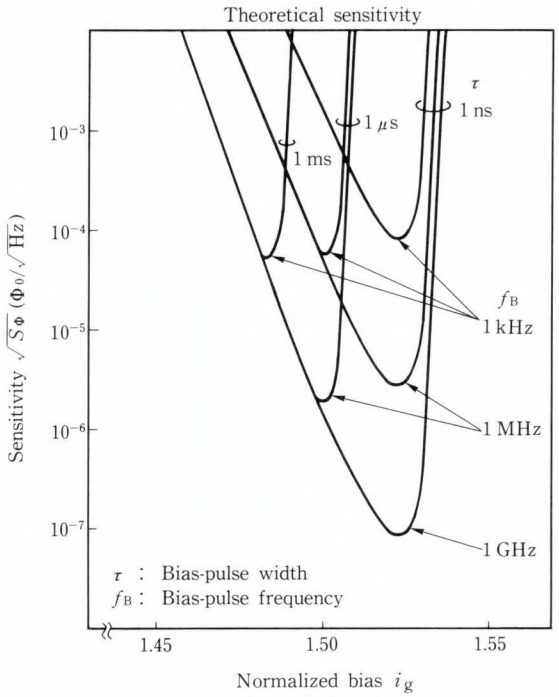


Fig. 17—Calculated square root of flux spectral density $S_\Phi^{1/2}$ vs normalized bias amplitude i_g.

The potential barrier ΔU cannot be expressed analytically. But, if we confine ourselves to the small inductance, an approximate expression can be obtained. In the limit of zero inductance, the 2-junction interferometer can be used as a single Josephson junction. In this case, ΔU, and therefore, p, $\partial p/\partial\Phi$, and S_Φ can be expressed analytically. The minimum flux sensitivity is expressed as follows[19].

$$S_\Phi|_{\min} = K\frac{\Phi_0^{2/3}}{f_B}\left(\frac{kT}{I_0}\right)^{4/3},$$

$$K = \left[\frac{1}{6\pi\left[-ln\left\{(-1/f_p\tau)ln(1-p_m)\right\}\right]}\right]^{2/3} \times \frac{p_m}{(1-p_m)\left\{ln(1-p_m)\right\}^2} \quad \cdots (21)$$

The minimum condition is obtained for the bias amplitude that has a switching probability of p_m (= 0.79). The value K is 0.05-0.13 for τ of 10^{-3}-10^{-9} s and can be considered as nearly constant. Equation (21) gives $1.4 \times 10^{-6}\ \Phi_0/\mathrm{Hz}^{1/2}$, which is about half of the numerically calculated result shown in Fig. 17. This is the approximation error. However, Equation (21) is useful as it allows us to know the rough dependence of the sensitivity on parameters. The flux spectral density is inversely proportional to the bias frequency. It is also proportional to four-thirds of the temperature and is inversely proportional to four-thirds of the critical current. This temperature dependence might seem ridiculous, but it is due to the nonlinear dependence of the switching probability, and its flux derivative.

When the temperature is much decreased or the bias frequency much increased, the thermal noise lowers. But it is limited by another condition called the quantum limit.

3.2.4 External noise effect

External noise contributes to the flux spectral density. If it is larger than the thermal noise, the sensitivity becomes limited by the external noise. The external noise can enter both as input flux and as bias fluctuation. As for the input flux, this has already been treated by the second and the fourth terms in Equation (19). When there is a fluctuation on the bias, it can be treated in the same way. By adding the bias fluctuation effect to the probability, Equation (16) is replaced by

$$p_n^{\pm} \simeq p \pm \left(\frac{\partial p}{\partial \Phi}\right)\hat{\Phi}(nT_B) \pm \left(\frac{\partial p}{\partial i_g}\right)\hat{i}_g(nT_B). \quad \cdots\cdots\cdots\cdots (22)$$

The term $\hat{i}_g$ is defined in the same way as in Equations (17) and (18). The frequency component of the bias noise power at high frequency is also reduced by the factor $\{\sin(\omega\tau/2)/(\omega\tau/2)\}^2$ due to the averaging effect. The spectral density of the output pulse is obtained as

$$\begin{aligned} S_x(f) = {} & 4f_B p(1-p) - 4f_B\left(\frac{\partial p}{\partial \Phi}\right)^2 \phi\hat{\Phi}(0) \\ & - 4f_B\left(\frac{\partial p}{\partial i_g}\right)^2 \phi\hat{i}_g(0) \\ & + 8f_B^2 p^2 \sum_{n=-\infty}^{\infty} \partial\{f-(2n+1)f_B\} \\ & + 4f_B^2\left(\frac{\partial p}{\partial \Phi}\right)^2 \sum_{n=-\infty}^{\infty} S_{\hat{\Phi}}(f+2nf_B) \\ & + 4f_B^2\left(\frac{\partial p}{\partial i_g}\right)^2 \sum_{n=-\infty}^{\infty} S_{\hat{i}_g}(f+2nf_B). \end{aligned} \quad (23)$$

The bias noise also suffers the averaging effect and the aliasing effect, as with the input flux noise. It appears in the equivalent flux spectral density as multiplied by $(\partial p/\partial\Phi)^2/(\partial p/\partial i_g)^2$. Roughly speaking, it is the slope of the threshold curve and is about $(1/L)^2$.

In order to suppress external noise, the bias and the signal with a frequency component higher than f_B should be cut with a low-pass filter.

3.3 Structure

In its early use[1], the Josephson junction was made by means of point contact. But now, for practical use, SQUID sensors have been made using thin film technology. Figure 18 shows the sensor structure. It is the same as that of the dc SQUID proposed by Ketchen[22], except that it has no shunt resistor. The structure is a superconducting thin film transformer. It has a single-turn superconducting inductance covered by multi-turn squre coils above the first

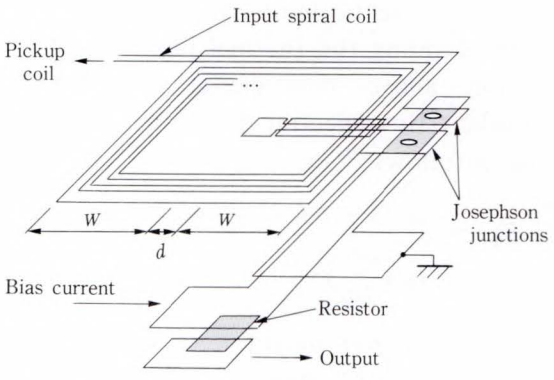


Fig. 18—Structure of the SQUID sensor.

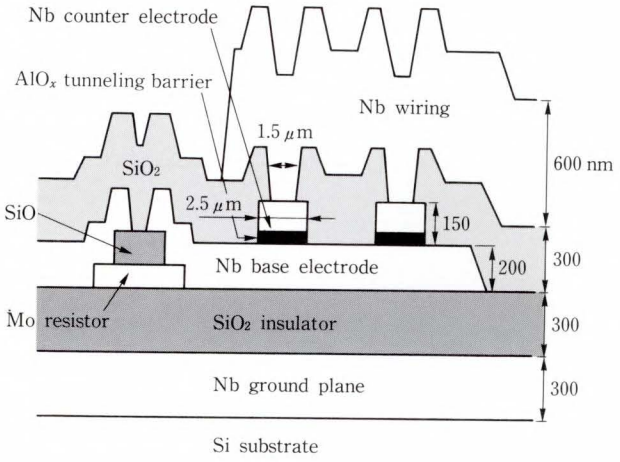
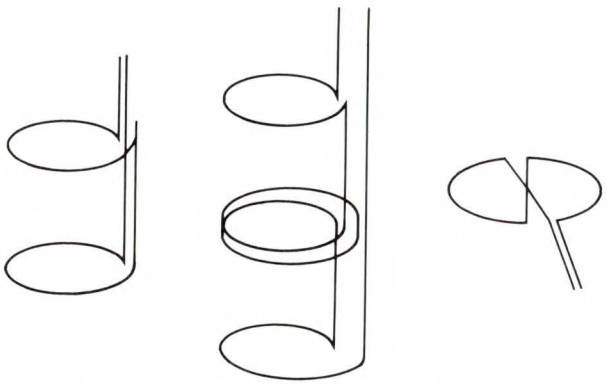


Fig. 19—Cross-sectional view of the multilayer structure.



a) First order b) Second order c) Planar first order

Fig. 20—Three kinds of pickup coils of gradiometer.

coil. These layers can be turned upside down. The multi-turn coil is called the input coil.

The sensor is made by multilayer fabrication in the same process as the Josephson digital circuits[14]. The cross-sectional view is shown in Fig. 19. The self and mutual inductances are calculated by the following equations[22].

$$L = 1.25\,\mu_0 d, \qquad \ldots\ldots\ldots (24)$$

$$M \simeq nL, \qquad \ldots\ldots\ldots (25)$$

$$L_{\text{in}} = n^2 L + L_s, \qquad \ldots\ldots\ldots (26)$$

where n is the number of turns. Equation (24) is valid for w/d much larger than 1. L_s comes from the flux uncoupled to the SQUID inductance L. This is the flux interlinked in the insulator between the multi-turn coil and the SQUID's single-turn coil. L_s is calculated by the following equation of the superconducting strip line.

$$L_s = \frac{\mu_0 (h + \lambda_{L_1}{}^* + \lambda_{L_2}{}^*) l_s}{Kw},$$

$$\lambda_{L_i}{}^* = \lambda_{L_i} \coth\left(\frac{\lambda_{L_i}}{t_i}\right),\ i = 1.2, \qquad (27)$$

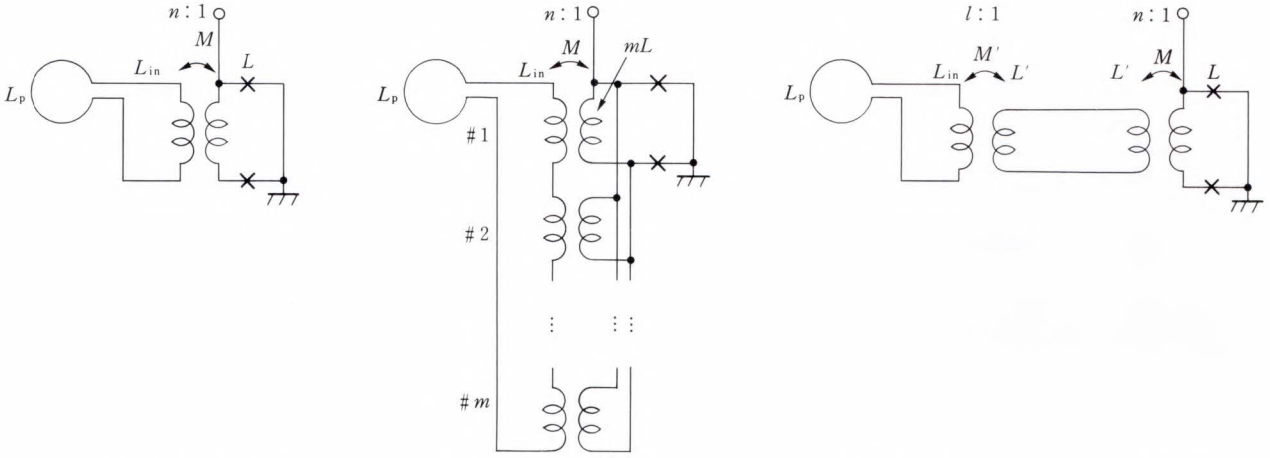
where h is the thickness of the insulator, w is the width of the multi-turn coil, K is the fringe factor[23], t_i and λ_{L_i} are the thickness and London penetration depth of the single-turn coil ($i = 1$), and the multi-turn coil ($i = 2$), respectively. l_s is the length of the multi-turn coil. The fringe factor K can be approximated by $(1 + 4h/w)$[24]. Typically, L_s is much smaller than $n^2 L$, the coupling coeffient k^2 can be as high as 0.9.

3.4 Coupling to the input flux

3.4.1 Pickup coil

The superconducting pickup coil receives the unknown magnetic field. It is made with superconducting wires or thin film line patterns[2]. Typically, their dimensions are 2 cm or 3 cm in diameter. The magnetic field measured is of the order of 10 fT, which is about six orders lower in magnitude than the environmental magnetic field fluctuation. To pick up this low magnetic flux, electromagnetically and magnetically shielded room are used. But, because it is not easy to obtain the shielding factor of 10^6 by them, a gradiometer is commonly used[4]. The first order gradiometer has two coils placed in parallel which are anti-wound to each other as shown in Fig. 20a). It is insensitive to the uniform field and is more sensitive to the field varying in space. As the signal source is placed near the pickup coil, and the source of the environmental field is generally far from the pickup coil, the environmental field varies more slowly than the signal field that is being measured. So, the gradiometer less sensitive to the environmental field. The second order gradiometer shown in Fig. 20b) is also used to obtain higher suppression of the environmental field, but is less sensitive. Usually, the coil imbalance can be made as small as 1/1 000.

Typical gradiometer coils have been made by winding a superconducting wire around a



a) Direct connection b) Fractional-turn c) Use of intermediate transformer

Fig. 21—Various methods for inductance matching.

cylinder. The planar coil configuration with superconducting wires as shown in Fig. 20c) has also been proposed and tested.

For strict balance of the gradiometer coil, it is useful to make the coil with the lithography technique. Some authors reported that the pick-up coil was integrated on the same chip[13),25)]. Nakanishi[25)] reported that a couple of dc SQUID magnetometer chips with a single-turn pickup coil were used, and in this case their output data is subtracted to suppress the environmental field.

3.4.2 Direct connection

In many cases, the pickup coil is connected to the input coil of the SQUID as shown in Fig. 21a). To maximize the transmitted flux, the input inductance L_{in} is designed to be the same as that of the pickup coil L_p. The pickup coil has a relatively large inductance of the order of 1 μH. However, the thin film SQUID inductance is designed to be from 10 pH to 100 pH. In order to match these inductance differences, the number of turns n has been designed as typically a few tens or 100.

The maximum transmission coefficient, which is defined as the ratio of the flux interlinked with the SQUID sensor Φ to the flux interlinked with the pickup coil Φ_p is obtained as

$$\frac{\Phi}{\Phi_p} = \frac{1}{2}\sqrt{\frac{L}{L_{in}}} \simeq \frac{1}{2n}, (L_p = L_{in}). \qquad (28)$$

As the input coil is shunted by the pickup coil, the inductance of the interferometer becomes $L\{1 - M^2/(L_{in} + L_p)\}$ instead of L.

3.4.3 Fractional-turn

The fractional-turn type has been proposed and tested as an alternative to using one superconducting inductance[26)]. The inductance of the SQUID sensor is divided into many coils as shown in Fig. 21b). The maximum flux is transmitted, when the next equation is satisfied.

$$L_p = L_{in} \simeq m^2 n^2 L. \qquad \ldots\ldots (29)$$

The transmission coefficient is

$$\frac{\Phi}{\Phi_p} = \frac{1}{2}\sqrt{\frac{L}{L_{in}}} \simeq \frac{1}{2mn}. \qquad \ldots (30)$$

Compared with the direct connection, this method helps reduce the number of input coil turns n.

The fractional-turn type is reported to have a resonance problem, because the many-turn coils have a larger parasitic capacitance[26)]. The resonance deforms the I-V characteristics of the dc SQUID and decreases the sensitivity. In this case, a Josephson junction is shunted by a low resistor, and the I-V curve is non-hysteretic. But in the case of the digital SQUID, the interferometer has no shunt resistor and its I-V curve has a large hysteresis as shown in Fig. 6. As the interferometer is used to switch

from the zero voltage state to the finite voltage state with a larger load resistor, the operation is not affected by the resonance.

3.4.4 Intermediate transformer

Another alternative is the intermediate superconducting transformer, as shown in Fig. 21c). The next condition does not maximize the transmission coefficient, but is near to this maximum condition.

$$L_p = L_{in} \simeq l^2 L' \simeq l^2 n^2 L. \quad \ldots\ldots (31)$$

The transmission coefficient is expressed as

$$\frac{\Phi}{\Phi_p} = \frac{1}{4}\sqrt{\frac{L}{L_{in}}} \simeq \frac{1}{4ln}. \quad \ldots\ldots (32)$$

The use of the intermediate transformer reduces the transmission coefficient by a factor of 2. But the transformer is capable of adjusting the input inductance without changing the SQUID sensor. Knuutila[27] reported that the intermediate transformer is used to attach the input coil, made on a different substrate, to the SQUID chip.

4. Digital feedback loop

4.1 Principle of operation

The digital SQUID sensor is operated in a digital feedback loop. In this loop, the digital feedback circuit receives a pulse sequence and produces a feedback flux. The transmission function of the feedback circuit relates to the response speed of the feedback loop. A simple choice in this case is integration.

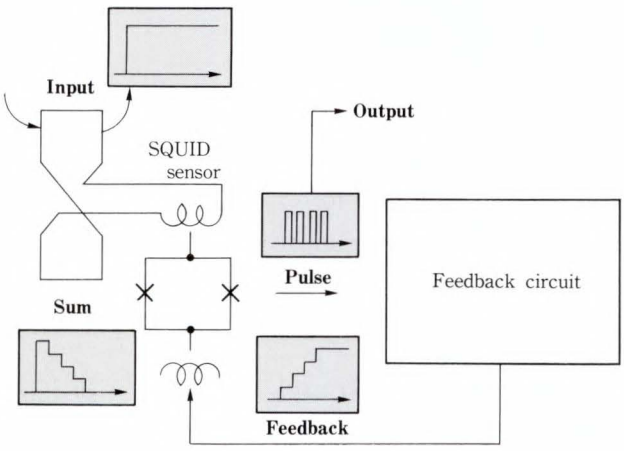


Fig. 22—Operation of the digital SQUID.

In this case, the digital feedback circuit is designed to operate as an up/down counter[8), 13)]. Figure 22 illustrates the feedback operation. If the input rises in a step function, the SQUID sensor produces positive pulses. The feedback circuit counts this pulse sequence and sends back the feedback flux to the SQUID sensor with negative polarity. The SQUID sensor receives both the input flux and feedback flux. The SQUID sensor measures the input flux minus the feedback flux. This decreases as the feedback flux increases. When it becomes zero, the SQUID sensor stops producing a positive pulse. To be precise, the SQUID sensor produces both positive and negative pulses with equal probability, and the average feedback flux does not increase any more. In this way, the feedback loop operates to maintain the total input flux at zero. We can know the input flux by measuring the pulse sequence. For example, there are four positive pulses in Fig. 22, so we know the input is four times the quantized flux. This scheme is the same as that of the delta modulation[28)].

When the input is cancelled by the feedback flux, the sensor produces both positive and negative output pulses with the same polarity, typically adjusted in the range from 0.5 to 0.8. That can be changed by adjusting the bias amplitude as discussed in Subsec. 3.2.1.

The dynamic range of the SQUID operation is limited by the capacity of the feedback circuit to count the pulse. To measure the input waveform with adequate resolution, a dynamic range of 10^3 seems to be sufficient. But in the practical measurement of biomagnetism, the presence of external noise means that a larger dynamic range is necessary. The dynamic range of 2^{18}, that is, about 5×10^5, will be sufficient.

4.2 Response speed

4.2.1 Maximum slew rate

1) Fixed step size

Response speed depends on the quantized feedback flux $\Delta\Phi$ and the bias frequency f_B.

When the input flux rises in a step function with the amplitude much larger than the noise level, the feedback flux increases at a constant rate as shown in Fig. 22. This rate is the maximum slew rate[8] and is expressed as $\Delta\Phi f_B$. It can be increased by increasing the bias frequency or the quantized feedback flux. But, if the quantized flux is larger than the noise level of the sensor, the quantization error will limit the sensitivity. In order to obtain high sensitivity, the quantized feedback flux should be near the noise level of the SQUID sensor. However, it is possible to increase the maximum slew rate, by sacrificing the sensitivity.

2) Adaptive modulation

To improve the slew rate without sacrificing the sensitivity, the use of variable step size, or adaptive modulation, has been used and tested[28),29)]. In this method, the quantity of the quantized feedback flux is changed by the characteristics of the pulse sequence. If only a positive pulse continuously arrives, this means that a large positive signal flux is applied to the SQUID sensor. In this instance, the quantity of the feedback flux for each arriving pulse is increased. Experimentally this method has been shown to improve the maximum slew rate by three orders of magnitude. This has been done using the external digital feedback loop, but it could be replaced by Josephson logic circuits.

4.2.2 Cutoff frequency

Due to the aliasing effect discussed in Subsec. 3.2.2, the output pulse has the signal flux spectrum shifted by integer times twice f_B. But the bias frequency is typically more than 1 MHz and is much higher than the signal band width which typically ranges from 0.1 Hz to 1 000 Hz. So, when we confine ourselves to the low frequency region below the bias frequency and small signal, the SQUID sensor is equivalent to a linear transducer with the transfer function of $2f_B\,(\partial p/\partial\Phi)$ as shown in Equation (19). Thus, a block diagram of the feedback circuit can be drawn as shown in Fig. 23. The relationship between the input flux $\Phi_s - \Phi_{FB}$ and the output pulse X is obtained as

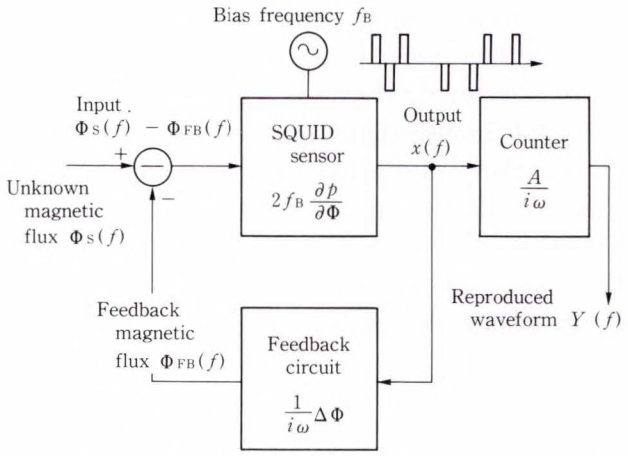


Fig. 23—Block diagram of the digital SQUID for small input flux. Only the frequency component below the bias frequency f_B is considered.

$$X(\omega) = 2f_B\left(\frac{\partial p}{\partial \Phi}\right)\left\{\Phi_s(\omega) - \Phi_{FB}(\omega)\right\} . \quad \ldots\ldots\ldots\ldots (33)$$

The feedback circuit operates as a counter and is expressed as

$$\Phi_{FB}(\omega) = \frac{\Delta\Phi}{i\omega} X(\omega) . \quad \ldots\ldots (34)$$

Substituting Equation (34) into Equation (33), we obtain

$$\Phi_{FB}(\omega) = \frac{\Phi_s(\omega)}{1 + i\omega/\omega_c} ,$$

$$\omega_c = 2f_B \Delta\Phi \frac{\partial p}{\partial \Phi} . \quad \ldots\ldots\ldots (35)$$

If we count the output pulse at room temperature, the counted result Y is proportional to Φ_{FB} and is expressed as

$$Y(\omega) = \frac{A}{\Delta\Phi}\Phi_{FB}(\omega) = \frac{A}{\Delta\Phi}\frac{\Phi_s(\omega)}{1 + i\omega/\omega_c} , \quad \ldots (36)$$

where A is a unit quantity for one pulse. If we use a D/A converter to measure the counted result A is the 1-bit output voltage of the D/A converter.

This shows that the feedback system operates as a first-order low-pass filter. The cutoff frequency is $\Delta\Phi f_B\{(1/\pi)(\partial p/\partial\Phi)\}$.

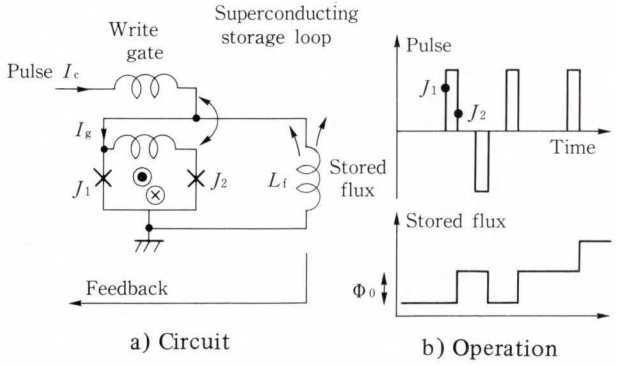


Fig. 24—Superconducting feedback circuit.

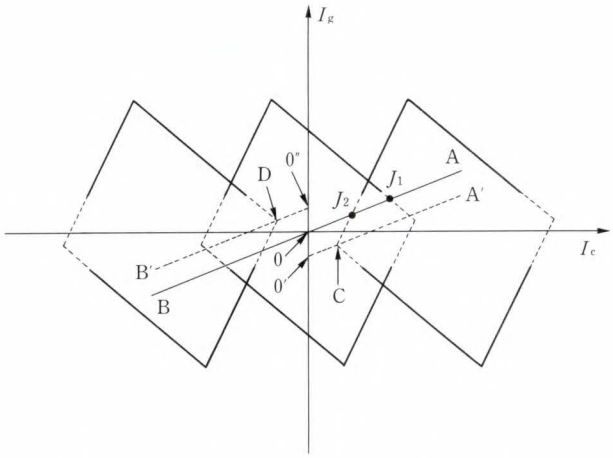


Fig. 25—The operating trajectory on the threshold curve of the write gate.

5. Single-chip SQUID

5.1 Superconducting feedback circuit

The digital feedback circuit can be made with an up/down counter and a digital-to-analog converter as discussed in Sec. 4.1. It can be realized with room temperature electronics or cryogenic electronics, as for Josephson logic circuits. However, a further alternative method has been proposed and tested[8]. In this method, the operation of pulse counting is done by placing a quantum flux in the storage loop. Figure 24a) shows the circuit. A superconducting inductance and write gate of a 2-junction interferometer form a loop for flux storage.

5.1.1 Flux quantization

This method utilizes flux quantization[30]. In the superconducting loop, the magnetic flux is quantized. The flux is permitted when,

$$\Phi = n\Phi_0 , \qquad \ldots\ldots\ldots (37)$$

where n is an integer. In a superconducting loop including Josephson junction, or interferometer, the above quantization condition reappears as,

$$\frac{\Phi_0}{2\pi}\phi + \Phi = n\Phi_0 , \qquad \ldots\ldots (38)$$

where ϕ is the phase difference of the Josephson junction or the interferometer. Due to the limitation of dynamic range by the write gate operation, the first term is less than $\Phi_0/40$, as discussed in the next subsection. For practical applications, this small difference of less than one quantized flux is not a problem. In the case of exact measurement requiring an estimate of this difference, it is possible to calibrate the value.

5.1.2 Write gate

The write gate[8] in Fig. 24a) is a 2-junction interferometer. It is used to add flux quantum when a pulse arrives. Its operation is shown in Fig. 24b). Figure 25 shows the threshold curve of the write gate. When the pulse comes from the sensor, the pulse current flows through a magnetically coupled control line and is then injected at the left end of the interferometer inductance. The operating point moves from the origin to point A in Fig. 25. As the operating point crosses the threshold curve, it changes its state from the zero mode to the first mode. At this point, the left Josephson junction J_1 switches transiently and as a result, nearly one flux quantum enters the interferometer. When the pulse falls, the point returns to the origin. In this case, when the operating point crosses the dashed curve of the first mode, the right Josephson junction J_2 switches transiently, and the flux quantum is transferred to the superconducting loop. When the operating point returns to the origin, the stored flux is exactly one flux quantum.

To be precise, the operating point does not return exactly to origin 0. Due to the nonlinear inductance of the write gate having a Josephson junction, the stored flux is slightly different from the flux quantum. The difference is expressed by Equation (38). However, it is

small, because the loop inductance is of the order of 10 μH and is much larger than the interferometer inductance of about 10 pH. When the critical current flows, the first term in the left side of Equation (38) becomes $\Phi_0/4$. But, even when the maximum number of flux quanta is stored in the loop, the maximum circulating current is about 1/10 of the critical current of the write gate as discussed in the next subsection. In this instance, the error is less than 1/40 of the flux quantum, and can be neglected in usual use.

5.1.3 Dynamic range

The dynamic range is the same as the maximum number of flux quanta. The capacity of storing flux quanta is determined by the following effect. When one flux quantum enters the superconducting storage loop, the flux is maintained in the loop by the external current. The current shifts the operating point trajectory along the vertical axis. As the number of the positive stored flux increases, the trajectory is shifted down. When it becomes the dashed line 0'A' in Fig. 25, it crosses point C. At this point, the interferometer can add no more flux quanta. Actually, in this case, when the pulse rises, J_1 switches transiently and nearly one flux quantum enters the interferometer, but when the pulse falls, the same J_1 switches transiently and the flux moves back to the left. No flux is added in the superconducting storage loop. On the other hand, when many negative pulses continue, the operating point shifts upward and if it crosses point D, no more negative flux quantum can be added. The maximum circulating current I_{mc}, which is defined as the point when no more flux can be added, is value 00'. It is determined by the write gate design and is typically 0.02 mA. The maximum amount of stored flux is denoted by $L_f I_{mc}/\Phi_0$. For example, 10^5 for L_f of 10 μH[31].

5.2 Chip design

The single-chip SQUID consists of a digital SQUID sensor and a superconducting feedback circuit as shown in Fig. 26. The quantized

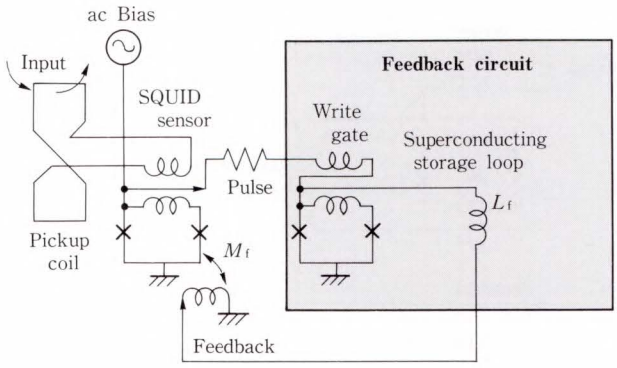


Fig. 26—Circuit of the single-chip SQUID.

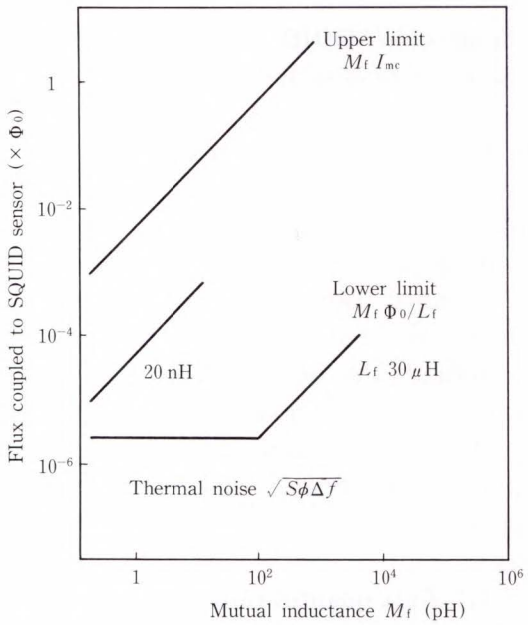


Fig. 27—Cover range of the single-chip SQUID.

Table 1. Parameter dependence of the performance of the single-chip SQUID

Item	Specification
Sensitivity	$\Delta\Phi \simeq \sqrt{S_\phi \Delta f}$
Dynamic range	$M_f I_{mc}/\Delta\Phi$
Response speed	
Slew rate[note)]	$\Delta\Phi f_B$
Cutoff frequency	$\Delta\Phi f_B(\frac{1}{\pi}\frac{\partial p}{\partial \Phi})$

Note: Constant step size: $\Delta\Phi = (M_f/L_f)\Phi_0$.

feedback flux per one pulse is $\Delta\Phi$. It can be adjusted by designing mutual inductance M_f. Figure 27 shows the coverage of the single-chip SQUID as a function of M_f, with a parameter of the inductance L_f of the storage

loop. The upper limit is $M_f I_{mc}/\Phi_0$. The lower limit is determined by the quantized flux or the thermal noise.

Table 1 summarizes the parameter dependences of the sensitivity, the dynamic range, the slew rate, and the cutoff frequency discussed in Sec. 4. The sensitivity is determined by the larger values of the noise level and the quantized flux. They are designed to be nearly the same. The dynamic range is the same as the maximum amount of flux quanta that can be stored in the storage loop. The slew rate and the cutoff frequency can be increased by increasing the bias frequency and the quantized feedback flux. The cutoff frequency is also proportional to the flux derivative of the switching probability, $\partial p/\partial \Phi$, which, in turn, depends on the bias amplitude, the bias pulse width, the critical current of the Josephson junctions, the attempt frequency, the inductance of the sensor, and the operating temperature as discussed in Subsec. 3.2.1.

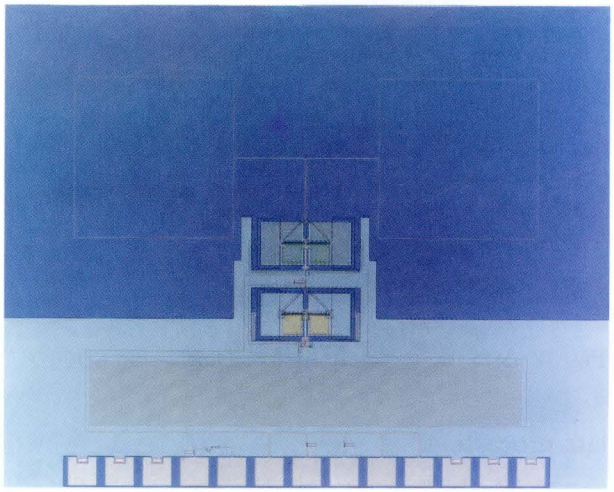


Fig. 28—Photograph of the single-chip SQUID.

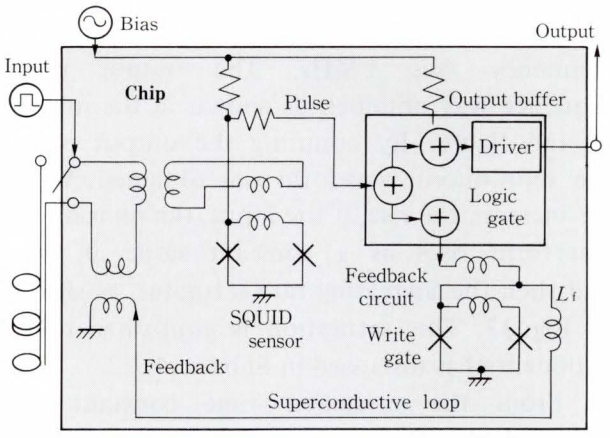


Fig. 29—Circuit of the improved single-chip SQUID.

5.2.1 First chip

The first chip[8] includes a figure-of-eight coil shown in Fig. 28. The circuit in the chip is the same as that shown in Fig. 26. The storage inductance L_f is 20 nH. It is made with a superconducting strip line with a width of 5 μm on the ground plane. The length is 13 cm. The dynamic range is about 200, which is too small to be used in practical applications, but is sufficient to investigate the fundamental operation. The sensitivity was obtained as $7 \times 10^{-5}\ \Phi_0/\mathrm{Hz}^{1/2}$ with the bias frequency at 500 kHz. This value is worse than the theoretical value of $4 \times 10^{-6}\ \Phi_0/\mathrm{Hz}^{1/2}$. The cause of this is believed to be external noise. But, for the first time, a digital SQUID sensor with a superconducting feedback circuit integrated on the same chip has been successfully operated.

5.2.2 Improved chip

Improved performance, and the practical use of SQUID in the field of biomagnetism, were the aims in mind when the second chip was designed and tested[31]. The improved chip circuit is shown in Fig. 29. Figure 30 is a photomicrograph of the chip. The pickup coil is not contained in the same chip. It is intended that the superconducting wire of the first or second gradiometer pickup coil will be attached to the chip pads.

The intermediate transformer is used to match the input inductance to the pickup coil. The feedback transformer is also used to adjust the quantized feedback flux $\Delta\Phi$ to be $5.6 \times 10^{-6}\ \Phi_0$.

The storage loop inductance was increased to about 30 μH. It was realized by 32 coils without any ground plane. The theoretical dynamic range is 1.7×10^5. Because the circuit has no ground plane, it might suffer from the external magnetic field or the stored flux-produces a magnetic field. To prevent this, the 32 coils are arranged as shown in Fig. 31.

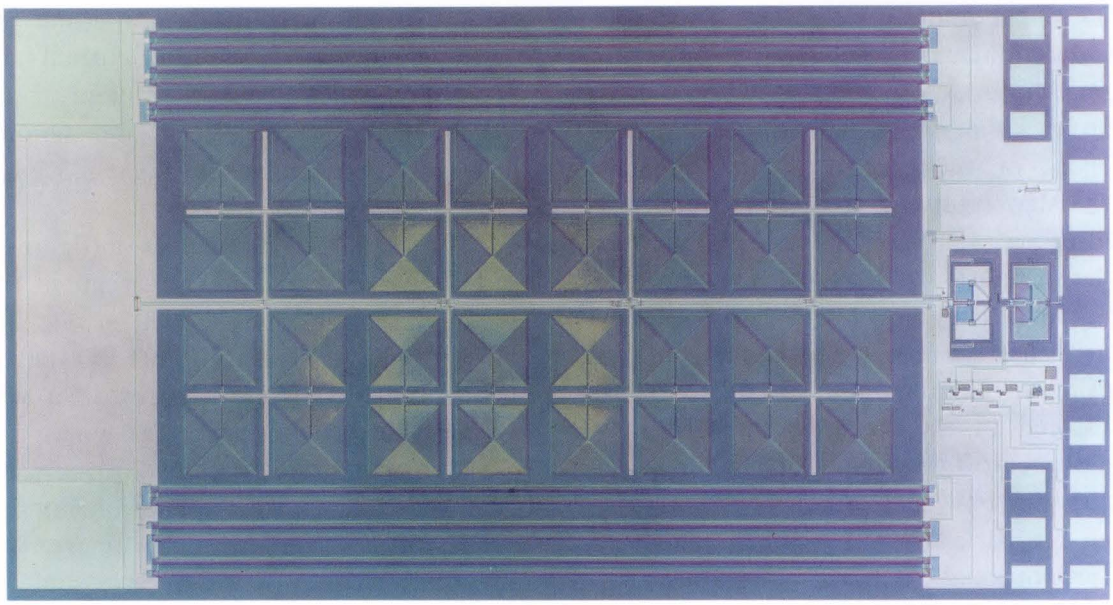


Fig. 30—Photograph of the improved single-chip SQUID.

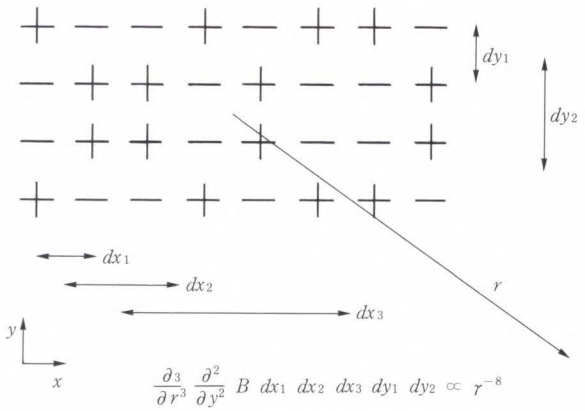


Fig. 31—An arrangement of the 32 coils of the superconducting storage inductance.

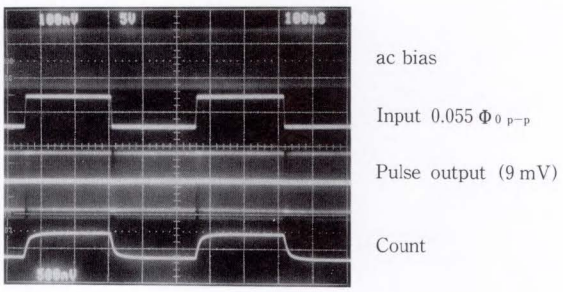


Fig. 32—Measured operation of the single-chip SQUID.

The field produced is proportional to r^{-8} where r is the distance from the center of the coils to the origin of the field. By simple estimation, the coils produce only 10 fT at a point about 2 cm far from the coil, even when the storage loop holds 10^5 flux quanta.

The Josephson logic gates are used in the same chip. The gates are one of the MVTL gate family[24] and a driver gate. The gates in this chip are used only as an output buffer which prevents the SQUID sensor from suffering form the external noise coming through the output cable. In the future it will be possible to add more complex logic circuits, for more data processing.

5.3 Performance

Figure 32 shows the results of our experiments[31]. The rectangular waveform current is applied to the chip as an input. The bias frequency was 1 MHz. The output pulse sequence was obtained as shown in the middle of the figure. By counting the output pulse, the reproduced waveform was obtained. When we increase the rise of the input, the reproduced waveform rises as a constant slope at first, and then the increasing rate saturates, as shown in Fig. 33. This saturation is confirmed to be exponential as discussed in Subsec. 4.2.2.

From the measured time constant, we obtained the flux derivative of the switching probability. The switching probability itself

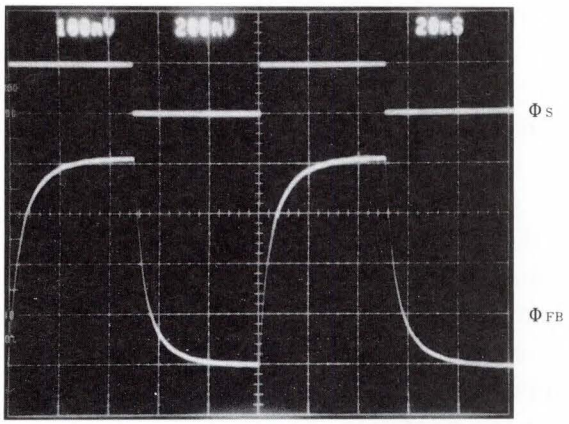


Fig. 33—Enlarged photograph of the reproduced waveform in Fig. 32.

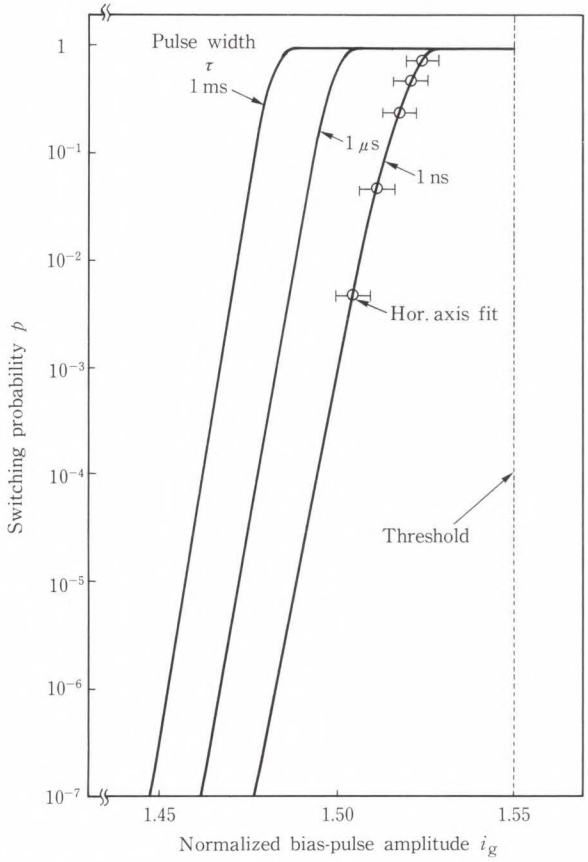


Fig. 34—Measured switching probability p vs normalized bias amplitude i_g.

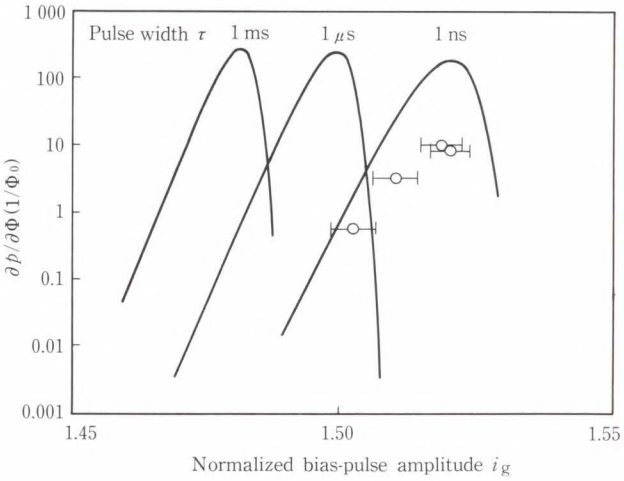


Fig. 35—Measured $\partial p/\partial \Phi$ vs normalized bias amplitude i_g.

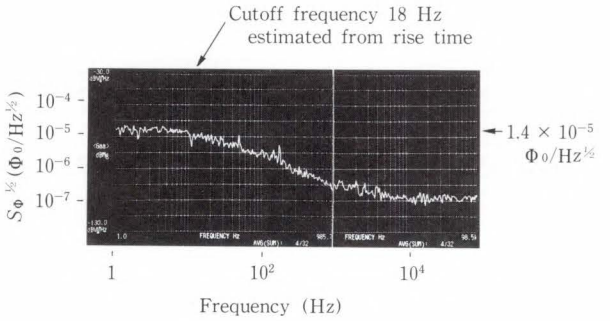


Fig. 36—Measured flux spectral density.

has been measured by changing the bias amplitude. The measured p and $\partial p/\partial \Phi$ are plotted in Figs. 34 and 35. In the experiment, the bias was applied as a rectangular pulse waveform having a slight ringing with a peak at the rise of the pulse. The experimental data fits with the theoretical curve with 1 ns pulse width at one point, as shown in Fig. 34. The theoretical calculation in Figs. 13 and 14 shows that the shape of p and $\partial p/\partial \Phi$ curve does not depend on τ, but only shifts along the horizontal axis. The reason for the difference between the experimental data and the theoretical calculation is not yet known. Some external noise might contribute to this difference, but further study of this is required.

Figure 36 shows the measured flux spectral density. It has a constant level of $1.4 \times 10^{-5}\ \Phi_0/\mathrm{Hz}^{1/2}$ at low frequency. It decreases at a rate of 20 dB/decade at higher frequency. It is in agreement with the response speed of the feedback loop with 18 Hz. The results of the experiment are summarized in Table 2.

The sensitivity and the response speed are improved by increasing the bias frequency as discussed in Secs. 3 and 4. From the above data, the performance at 100 MHz is estimated

Table 2. Comparison of the experimental and the theoretical performance of the single-chip SQUID

Performance	Experiment	Theory
Bias frequency	1 MHz	1 MHz
Dynamic range	$\pm 2 \times 10^4$	$\pm 1.7 \times 10^5$
Sensitivity	$1.4 \times 10^{-5}\,\Phi_0/\mathrm{Hz}^{1/2}$	$2.7 \times 10^{-6}\,\Phi_0/\mathrm{Hz}^{1/2}$
Response speed		
Maximum slew rate	$4\,\Phi_0$/s	$5.6\,\Phi_0$/s
Cut off frequency	18 Hz	320 Hz

Table 3. Comparison of the expected performance of the single-chip SQUID and the top performance of the dc SQUID

Performance	Single-chip SQUID	dc SQUID
Bias frequency	100 MHz	dc
Dynamic range	$\pm 10^5$	$\pm 10^6$
Sinsitivity note)	$3 \times 10^{-7}\,\Phi_0/\mathrm{Hz}^{1/2}$	10^{-6} - $10^{-7}\,\Phi_0/\mathrm{Hz}^{1/2}$
Response speed		
Maximum slew rate	$400\,\Phi_0$/s	$10^6\,\Phi_0$/s
Cut off frequency	1.8 kHz	–

Note: Constant step size.

and compared with the best performance of the dc SQUID shown in Table 3. The dynamic range and the sensitivity are the theoretical values. The response speed is extrapolated from the 1 MHz experimental results. The digital SQUID has the same level of sensitivity and dynamic range as the dc SQUID. For practical use in biomagnetism, the sensitivity of the conventional dc SQUID is of the order of $10^{-6}\,\Phi_0/\mathrm{Hz}^{1/2}$. Therefore, a bias frequency of 10 MHz should be sufficient. As for the response speed, the digital SQUID with fixed step size is slow compared with the dc SQUID. This is due to the fact that the feedback flux increases by one quantized flux at most in one clock cycle. To improve the slew rate, it is possible to use the variable step size or the adaptive modulation as described in article 2) of Subsec. 4.2.1.

5.4 Unsolved problems

Two problems remain unsolved. They are flux trap and crosstalk. The flux trapped in the feedback circuit reduces the dynamic range. The write gate has been improved and is now free of flux trapping. The persistent current in the superconducting storage loop, due to trapped flux, can be reset by heating with the resistor. However, in the sensor itself it is not easy to remove trapped flux. The static trapped flux can be cancelled by the internal feedback operation, although this reduces the dynamic range. However, the movement of the trapped flux produces extra noise in the sensor. That is a serious problem.

Crosstalk is becoming the greatest obstacle to attempts to increase the bias frequency of the digital SQUID. The sensitivity and the response speed can be enhanced by increasing the bias frequency. Typically, when we increase the bias frequency higher than 1 MHz, crosstalk affects the SQUID performance. Crosstalk alters the operating point of the sensor or the other circuit element, and causes the wrong circuit operation. For much higher frequency, the multiple reflection of the pulse and its crosstalk determine the switching probability. When this occurs, the switching probability does not depend on the signal but on the former clock output. In the worst case, the SQUID becomes insensitive to the signal.

If the above two problems, flux trap and crosstalk, are solved, the theoretical sensitivity and response speed of the single-chip SQUID can be obtained.

Recently, the digital SQUID sensor has been operated with an external feedback loop, a room temperature digital counter and a D/A converter, to measure biomagnetism[32]. The magnetic field produced by the heart has been measured with sufficient signal-to-noise ratio[33]. These results show that the digital SQUID can be effectively used for biomagnetic purposes.

5.5 Future prospects

Figure 37 shows a future target of the multichannel SQUID system using the single-chip SQUID. As the feedback loop is included in

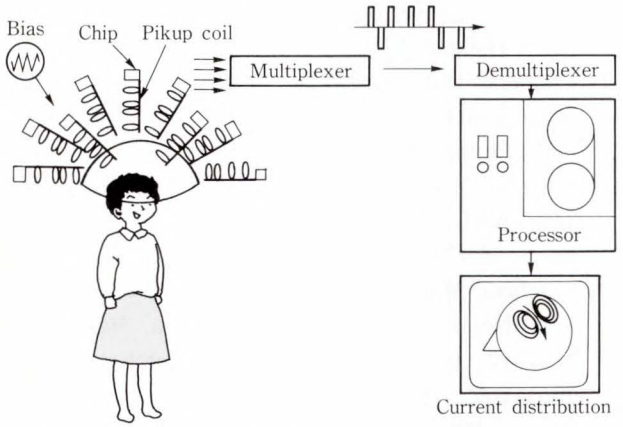


Fig. 37—A future target of the multichannel system.

each chip, there is no need for an external feedback loop between the cryogenic environment and room temperature electronics. This helps suppress external noise, and suppress the possible crosstalk between the cables of each channel. Also, as the output is a pulse sequence, unlike the conventional analog SQUID, the signal-to-noise ratio is enhanced. The use of the Josephson logic gate or buffer gate on the output terminal is particularly useful in preventing external noise from coming from the output cable.

The major advantage of the internal feedback circuit is the reduction in the number of cables required. The single-chip SQUID requires only a bias line and an output line. When n channels are operated in parallel, the required number of cables is only $2n$ whereas the analog dc SQUID requires $6n$.

Processing with Josephson digital circuits will be possible, as the multiplexer and the adaptive modulation seem to be promising candidates. There is also the possibility of reducing the number of cables to less than $2n$. If we use the Josephson multiplexer, the number of output cables can be decreased. If all of the SQUID output is multiplexed on a single output cable, then the total number of cables will be $n + 1$. If the bias can be adjusted by some method or circuit in the cryogenic environment, one bias line might be all that is needed. Then, the number of cables would be only one bias line and one output line, except for some multiplexer control lines.

6. Conclusion

This paper reviews the digital SQUID. Unlike the conventional analog SQUID, the digital SQUID produces a pulse sequence. Combining the new superconducting feedback circuit, the digital SQUID sensor and the feedback loop are integrated on a single chip. This reduces the number of cables connecting the room temperature electronics and the cryogenic chip. It enables us to construct a multichannel system with more than 100 channels for measuring a biomagnetic field map. Further, it will be possible to combine Josephson digital circuits and have the data processing of the SQUID outputs in the cryogenic environment. Although the chip performance has been improved, some problems still remain. But the experimental data up to now shows that the single-chip SQUID is a promising device for constructing a multichannel system.

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High-Speed Monolithic GaInAs Twin PIN Photodiodes for Coherent Optical Receivers

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Monolithic GaInAs twin PIN photodiodes were fabricated to realize excellent dual-detector balanced optical receivers in coherent optical communication systems. Introducing a back-illuminated, flip-chip structure gives these photodiodes a small junction capacitance of 80 fF, a quantum efficiency of 75 percent at a wavelength of 1.54 μm, and a cutoff frequency better than 15 GHz. An optical input power level as high as 8 mW is obtained. A large fiber alignment tolerance of 60 μm is achieved by integrating InP microlenses. The common-mode rejection ratio is better than −30 dB at a frequency of up to 10 GHz. The performance demonstrated is well suited to high-speed optical coherent communication systems.

1. Introduction

Coherent optical transmission techniques are very important for lightwave communication systems because they significantly improve the receiver sensitivity and enable very high-density wavelength division multiplexing transmission. The key to this technique is coherent optical reception by optical heterodyne detection using a local oscillator and a photodiode. Since the sensitivity increases with local oscillator power, photodiodes must also be capable of accepting high optical power.

Achieving an operating speed of several Gbit/s requires the following: New optical sources such as semiconductor DFB lasers having high optical power (>10 mW) and a very narrow spectrum (<1 MHz) for the local oscillator, and new photodiodes having a high-speed response (>10 GHz) at high optical power injection (>5 mW).

In designing highly sensitive coherent optical receivers, care must be taken when using a local oscillator laser because optical power fluctuation of the laser becomes a noise source for the receiver.

To suppress this laser intensity noise, dual-detector balanced optical receivers (DBORs) are often used[1),2)]. Key components of the DBOR are two photodiodes and a 3-dB directional optical coupler. If the photocurrents in the two photodiodes are exactly equal, the noise due to laser intensity fluctuation is canceled by subtracting the two photocurrents.

For this reason, it is required that the quantum efficiency, capacitance, and frequency response of the two photodiodes be well matched.

Two photodiodes acquiring by monolithic integration; twin PIN photodiodes should be very convenient for achieving this requirement. The authors have already reported the first monolithic twin PIN photodiodes integrating two surface-illuminated photodiodes[3)]. The authors have also demonstrated that monolithic integration is very effective for achieving well matched characteristics.

On the other hand, several authors have reported the fabrication of monolithic devices integrating an optical waveguide coupler, a semiconductor laser and photodiodes for

coherent transmission systems[4)-6)]. Although the use of such monolithic devices is desirable in the future, it is very important to obtain key components which can be used now to construct high-performance DBORs operating at several Gbit/s.

Previous twin PIN photodiodes[3)], however, are insufficient for high-speed response, high optical power detection and large fiber alignment tolerance. And these characteristics are critical for constructing the practical key components for DBORs.

In this work, we have developed new twin PIN photodiodes satisfying all the above-mentioned requirements.

2. Design

Figure 1 shows the basic DBOR circuit. To obtain high-performance optical receivers having sensitivities close to the quantum noise limit, the photodiodes must have the following characteristics: High quantum efficiency, small junction capacitance, good optical coupling efficiency, and the endurance for high optical power injection. The characteristics of the two photodiodes must be matched to prevent any imbalance that decreases sensitivity.

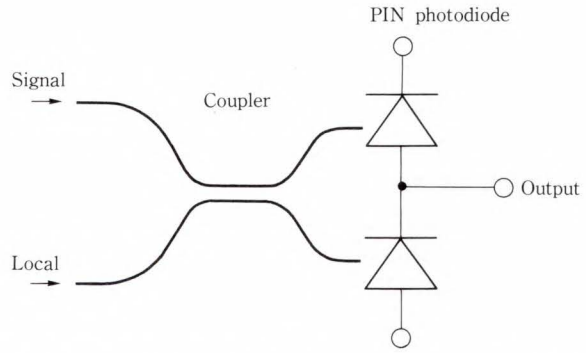

Fig. 1—Dual-detector balanced optical receiver (DBOR).

To meet the above requirements, the authors introduced a monolithic InP microlens[7)], a back-illuminated photodiode structure, and flip-chip bonding[8)].

Figure 2 shows the twin PIN photodiodes[9)], which were integrated on a semi-insulating (SI) InP substrate for electrical isolation.

The light signal is fed into the junction from the substrate side (back-illuminated). The InP microlens yields a large tolerance to optical misalignment and good optical coupling efficiency. Introducing metal bumps for flip-chip bonding eliminates the need to use bonding wire, and hence eliminates degradation due to the inductance of the bonding wire.

To obtain well matched characteristics, a symmetrical layout was used for the interconnecting metal. The circular bump is for the electrical signal output and the square bumps are for the bias supply.

To design the junction structure of the twin PIN photodiodes precisely, the cutoff frequency and quantum efficiency of the back-illuminated

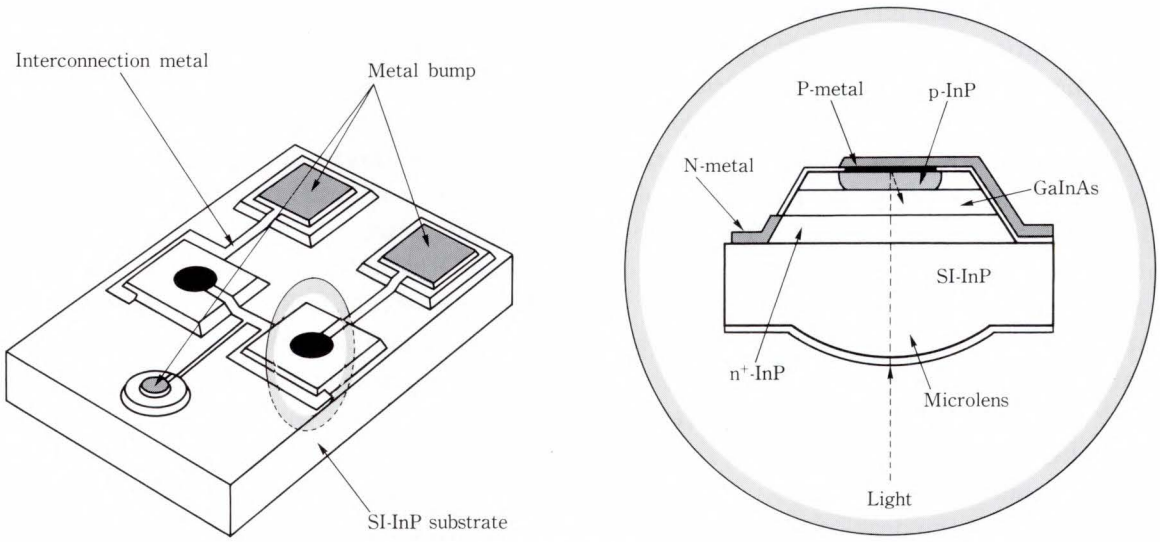

Fig. 2—Twin PIN photodiodes.

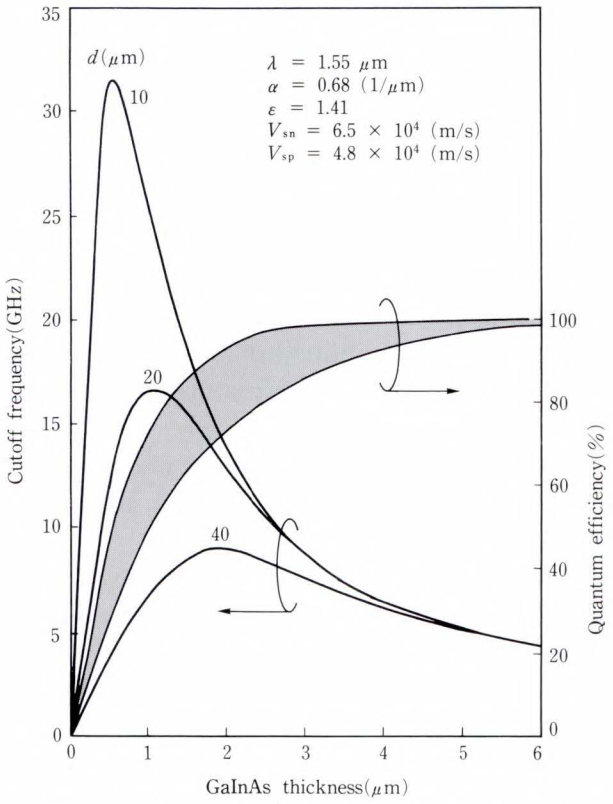

Fig. 3—Cutoff frequency and quantum efficiency as a function of GaInAs thickness. d is the PIN junction diameter, α is the absorption coefficient of InGaAs at a 1.55-μm wavelength, ϵ is the dielectric constant of GaInAs, V_{sn} is the electron velocity, and V_{sp} is the hole velocity.

twin PIN photodiodes was calculated as a function of the photoabsorption layer (GaInAs) thickness by solving continuity equations[10] (see Fig. 3).

The following parameters[11] were assumed for GaInAs: absorption coefficient, $\alpha = 0.68$ (1/μm) (at wavelength $\lambda = 1.55 = m$); dielectric constant, $\epsilon = 14.1$; electron saturation velocity, $V_{sn} = 6.5 \times 10^4$ (m/s); and hole saturation velocity, $V_{sp} = 4.8 \times 10^4$ (m/s). The three solid curved lines show the cutoff frequencies. Parameter d is the diameter of the PIN junction and was calculated from 10 μm to 40 μm.

The left side of the peak of the three curves is mainly subjected to an RC time constant consisting of the photodiode junction capacitance {see Equation (A1) of Appendix} and its 50-Ω load resistance.

The right side of the peak of the three curves is mainly subjected to the carrier transit time between electrodes, determined by the electron and hole velocity.

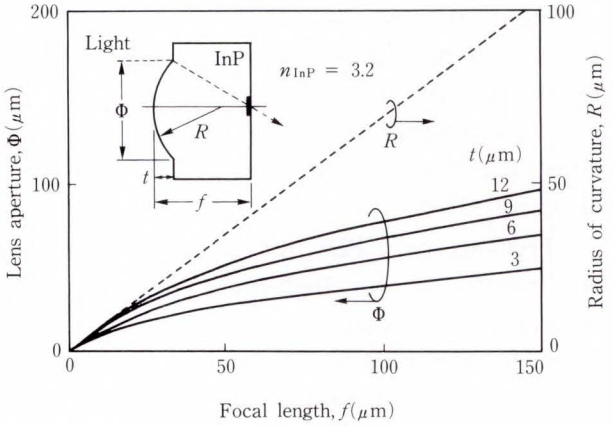

Fig. 4—Relationship between focal length (f), lens aperture (Φ), radius of curvature (R), and thickness (t) of the microlens.

The shaped area shows quantum efficiency. The lower boundary is determined by the single optical path in the thickness of GaInAs. The upper boundary is determined by considering the complete reflection of incident light at the P-metal surface. This shaded area is only achieved by a back-illuminated photodiodes structure in which a high quantum efficiency can be obtained with thinner GaInAs.

On the other hand, to make the photodiode able to operate at high speed under high optical power injection, it is important to reduce the GaInAs thickness so that the space charge effect[10),12] is suppressed. Space charges can be accumulated in the photo-absorption layer at high optical power injection. This decreases the internal electric field and therefore slows down carrier velocity.

Taking this effect into account, the GaInAs thickness was designed to be 1.4 μm for a junction diameter of 20 μm. A cutoff frequency of 16 GHz and a quantum efficiency in a range from 62 percent to 84 percent is expected.

To obtain a large fiber alignment tolerance, the InP microlens was designed using simple ray optics theory[13]. Given the focal length (f) and refractive index (n_{InP}) of the InP microlens, the radius of curvature (R) can be found from $R = f(n_{InP} - 1)/n_{InP}$. The lens aperture is given by $\Phi = 2\sqrt{(2Rt - t^2)}$, where t is the micro-

lens thickness.

Figure 4 shows the results for a refractive index of 3.2.

The focal length corresponds to the thickness of the InP substrate. To get a fiber alignment tolerance of better than 50 μm, which is required for stable optical coupling, the lens aperture was set to 80 μm and the microlens thickness was 9 μm. The substrate was about 130 μm thick. Taking into account the 20-μm PIN junction diameter, the substrate thickness can vary by ±25 μm and the lens thickness can vary by ±2 μm.

3. Twin PIN photodiode fabrication

In fabricating the photodiodes, the authors started by selective Zn diffusion to form the 20-μm-diameter PIN junction. Au/AuZn p-contacts are formed by evaporation and alloying, then the slanted mesa structure is made by Ar ion beam etching.

The authors formed Au/AuGe n-contacts on the mesa slope, followed by formation of the interconnection metal by evaporating Au/Ti on SiN film. AuSn/Pt/Ti metal bumps were formed after passivation film deposition. The substrate was then thinned, and two 80-μm lenses were fabricated[14] as shown in Fig. 5.

Resist patterning and deformation by heating were performed, followed by Ar-ion beam etching, while the wafer was rotated. The purpose of the last step was to deposit a SiN antireflection film using plasma CVD.

The photodiode layer consists of an n-InP ($n \fallingdotseq 1 \times 10^{16}$ cm^{-3}) top layer 1 μm thick, an n$^-$-GaInAs ($n < 1 \times 10^{15}$ cm^{-3}) absorption layer 1.4 μm thick, and an n$^+$-InP ($n \fallingdotseq 2 \times 10^{17}$ cm^{-3}) contact layer 1.5 μm thick grown on a semi-insulating (SI) InP substrate with a (100) plane.

Figure 6 shows the twin PIN photodiodes flip-chip-bonded directly to Au bonding pads formed on a ceramic mount 0.85 x 1.3 mm^2. The center-to-center separation of the two microlens was 125 μm. The chip was 300 x 250 μm.

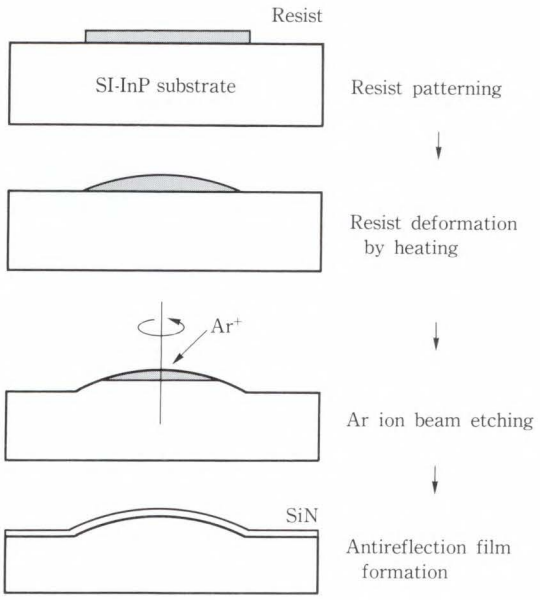

Fig. 5—InP microlens fabrication[14].

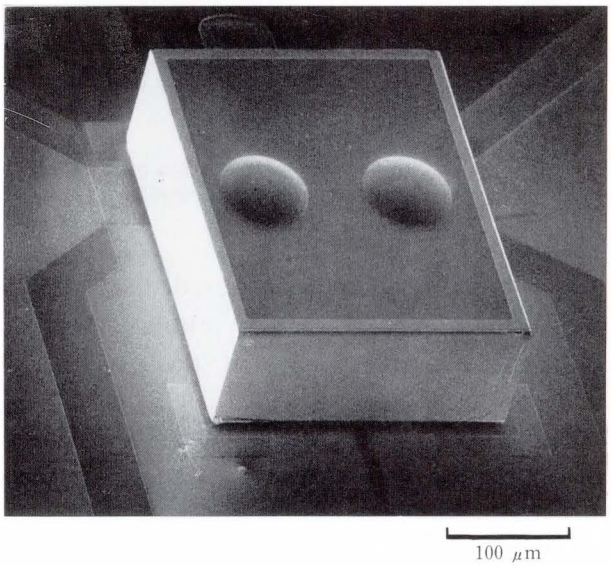

Fig. 6—Twin PIN photodiodes flip-chip-bonded to a ceramic substrate.

4. Characteristics

Figure 7 shows the photosensitivity profile measured by scanning a single-mode fiber having a tapered hemispherical lens at the end of the fiber (radius of lens curvature: about 20 μm).

The fiber alignment tolerance defined by permitting 0.5-dB coupling loss was as large as 60 μm, despite the small PIN junction diameter of 20 μm. At the center of this profile,

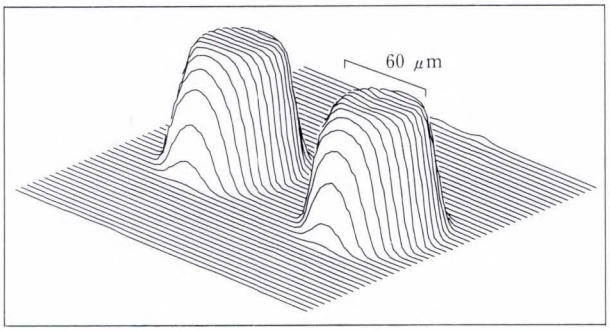

Fig. 7—Photosensitivity profile.

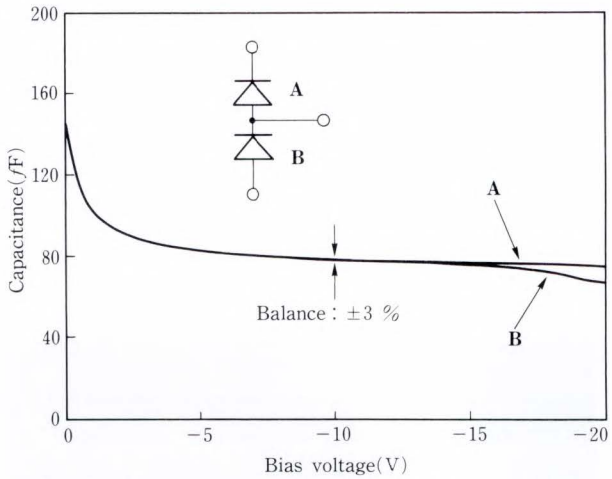

Fig. 8—Photodiode capacitance versus bias voltage measured before flip-chip bonding.

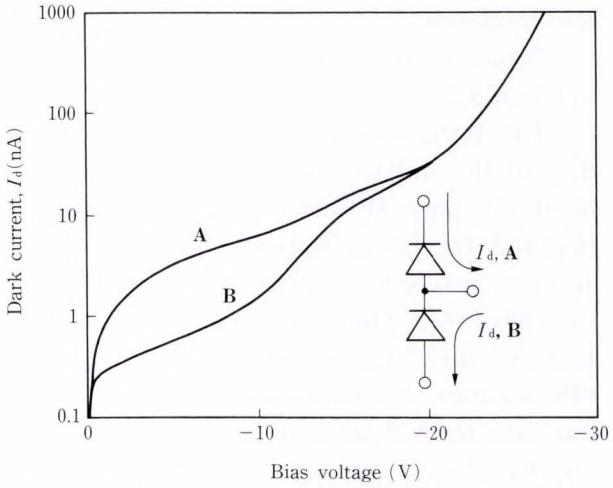

Fig. 9—Dark current versus bias voltage measured after flip-chip bonding.

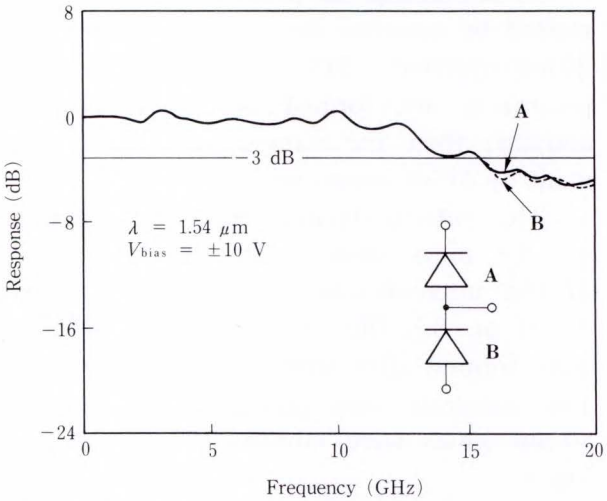

Fig. 10—Frequency response characteristics monitored for an optical input signal having a wavelength of 1.54 μm.

the quantum efficiency exceeded 75 percent at a 1.54-μm wavelength. The mismatch between the quantum efficiencies of the photodiodes was within 1.4 percent.

Figure 8 shows the junction capacitances as a function of the applied voltage, measured before flip-chip bonding.

The values of 80 *f*F and 78 *f*F at −10 V are matched to within ±3%. With these closely matched, the small capacitances are due to the symmetrical layout and the extremely small PIN junction area. The value of 80 *f*F is thought to be due to the intrinsic PIN junction capacitance (60 *f*F) and the stray capacitance (20 *f*F) between the interconnection metal and the n^+-InP contact layer.

Figure 9 shows dark current (I_d) as a function of the applied voltage, measured after flip-chip bonding.

The dark currents around 10 V were 6 nA and 1.5 nA for photodiodes **A** and **B** (labeled in the inset). The slightly larger current for photodiode **A** is assumed to be due to substrate leakage. This imbalance presents no problem in practical use because it has minimal effect in higher bit rate coherent systems that exceed 1 Gbit/s.

Figure 10 shows the frequency responses measured using the optical heterodyne technique.

The optical power fed into one photodiode was about 350 μW at a wavelength of 1.54 μm and at applied voltages of ±10 V. The load resistance of the twin PIN photodiodes was 50 Ω. An excellent balance was achieved between the two photodiodes' responses. The

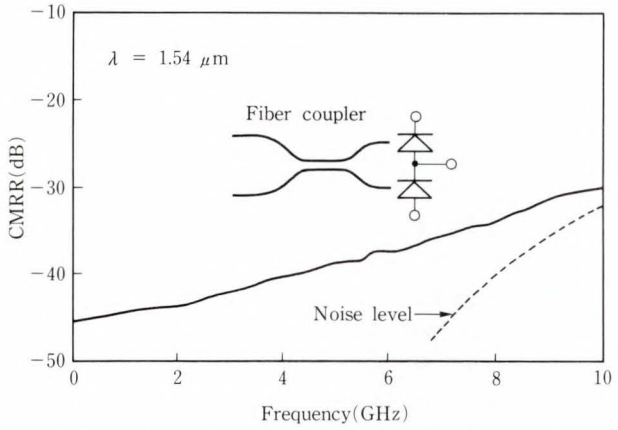

Fig. 11—Common-mode rejection ratio (CMRR) as a function of frequency.

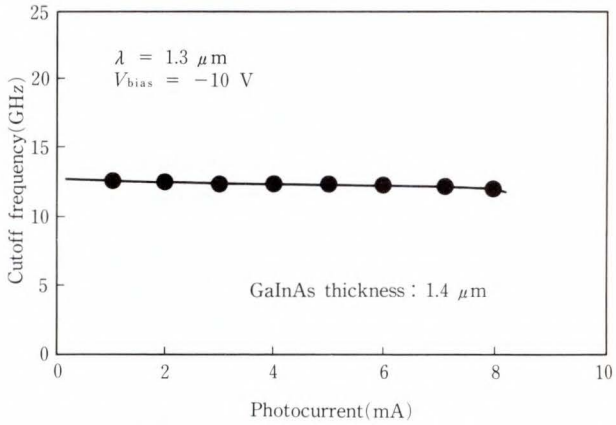

Fig. 12—Cutoff frequency as a function of photocurrent for optical input having a wavelength of 1.3 μm.

cutoff frequency was above 15 GHz. The measured cutoff frequency is almost equal to the calculated value of 16 GHz (see Fig. 3).

Many chips showed the same frequency responses, indicating excellent reproducibility. This shows the importance of flip-chip bonding in fabricating high-speed photodetectors.

To confirm the suppression of excess intensity noise generated by the local oscillator, the common-mode rejection ratio (CMRR) was measured using a conventional optical fiber coupler.

Figure 11 shows the CMRR measured using an intensity-modulated DFB laser having a wavelength of 1.54 μm. Optical power of about 650 μW was fed into one port of the fiber coupler. Although data was limited by the noise in the measurement system, a CMRR of better than −30 dB was achieved at up to 10 GHz.

In a previous paper[7], the authors reported a CMRR of −30 dB at up to 7 GHz and a cutoff frequency of 13.5 GHz using similar twin PIN photodiodes bonded to a ceramic mount. However, this mount did not have a symmetrical metallization pattern layout.

This shows that the mount for flip-chip bonding must also have a symmetrical layout to improve the CMRR.

Figure 12 shows the cutoff frequencies as a function of photocurrent for one photodiode measured with a semiconductor laser having a wavelength of 1.3 μm. The cutoff frequency was about 12 GHz at photocurrents greater than 8 mA under a 10-V bias. The maximum injection power (P_{in}) can be calculated by $P_{in} = (h\nu/e) \times I_p$, where h is Plank's constant, ν is the frequency of the injection light, and I_p is the photocurrent of the photodiode. From this equation, the photocurrent of 8 mA corresponds to the detected optical power of about 8 mW.

This high optical power detection was achieved by introducing the back-illuminated structure and optimizing the photo-absorption layer thickness. In the photo-absorption layer, a high quantum efficiency and suppression of the space charge effect are simultaneously achieved.

5. Conclusion

The authors designed and fabricated flip-chip, twin PIN photodiodes which can be used to construct high-performance coherent transmission systems.

The two photodiodes were integrated with a back-illuminated, lens structure having symmetrical layout. The twin PIN photodiodes satisfied the requirements of high-speed response, high optical power detection and a large fiber alignment tolerance.

The cutoff frequencies were better than 15 GHz. The optical power acceptability was more than 8 mW as measured at a wavelength of 1.3 μm. The fiber alignment tolerance was as large as 60 μm, despite the small PIN junction

diameter of 20 μm. The quantum efficiencies and junction capacitances of the photodiodes were 75 percent at a wavelength of 1.54 μm and 80 *f*F for one photodiode.

These characteristics were closely matched between two integrated photodiodes.

A common-mode rejection ratio of better than −30 dB at up to 10 GHz was achieved. These results demonstrate the importance of the present flip-chip, back-illuminated structure with symmetrical layout. This device is well suited to applications in high-performance coherent DBORs.

6. Appendix

The single-junction capacitance (C_{PIN}) of the twin PIN photodiode, considering the fringing field, is given by

$$C_{PIN} = \frac{\epsilon \epsilon_0 \pi d^2}{4W} + \epsilon \epsilon_0 d \left\{ ln\left(\frac{4\pi d}{W}\right)\left(1 + \frac{T}{2W}\right) - 1 \right\} + \frac{2\pi \epsilon \epsilon_0 dT}{W} ln\left(1 + \frac{2W}{T}\right). \quad (A1)$$

Where ϵ is the dielectric constant of GaInAs, ϵ_0 is 8.854×10^{-12} F/m, d is the diameter of the PIN junction, W is the thickness of GaInAs, and T is the thickness of the p-type region.

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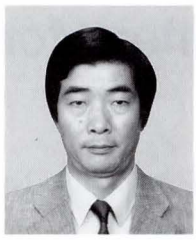

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SONET System for North America

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In 1988, the Phase I standard of Synchronous Optical Network (SONET) was established by ANSI. Standards committees are planning for Phase II, which defines the functions for maintenance and operations, and which will be generally standardized in late 1990.
Fujitsu produced the Fiber Loop Multiplexer (FLM) series conforming to the Phase I standard for the Regional Bell Operating Companies (RBOCs) before its competitors. The FLM was well received.
This paper describes the SONET systems created by Fujitsu, Fujitsu's plan to upgrade to Phase II, and the key technologies used in the product.

1. Introduction

The development of Broadband Integrated Services Digital Network (BISDN) is increasing the pace of network reconstruction all over the world.

In North America, the multiplexing hierarchy of DS1 (1.544 Mbit/s), DS2 (6.312 Mbit/s), and DS3 (44.736 Mbit/s) has been standardized. However, multiplexing hierarchies exceeding DS3 are generally proprietary. Fujitsu has designed and manufactured optical transmission system products having optical rates of 135 Mbit/s[1], 405 Mbit/s[2], 810 Mbit/s[3] and 1.8 Gbit/s. Fujitsu has placed these products on the market.

The ANSI T1 committee has initiated an effort for standardizing a multiplexing hierarchy exceeding DS3. The ANSI T1 committee includes representatives from manufacturing, Local Exchange Carrier (LEC) and Interexchange Carrier (IXC) companies. In 1988, it established the ANSI T1.105 standard under the name of "SONET"[4] coordinated closely with the international standards body, CCITT. This standard, called "SONET Phase I", specifies functions which allow multivendor, mid-span, optical interconnects which transport traffic, or in SONET terms, the payload.

In addition, in February, 1990, the first draft of the SONET Phase II specifications were completed. The specifications provide for mid-span meets of Data Communication Channel (DCC) protocols, new mappings and Phase I clarification. Standards are scheduled to be submitted for approval this year.

This paper describes Fujitsu's approach to provide a total SONET transport system. It covers the key technologies of Fujitsu's new optical transmission systems with Optical Carrier Levels OC-1 (51.84 Mbit/s), OC-3 (155.52 Mbit/s), OC-12 (622.08 Mbit/s) and OC-48 (2 488.32 Mbit/s) of the SONET multiplexing hierarchy.

This paper also outlines the following Fujitsu SONET products: The FLM 50/150 with OC-1 and OC-3 optical line interfaces and the FLM 600 with an OC-12 optical line interface already in production.

2. System outline

The Fujitsu SONET FLM optical digital multiplexer systems conform to the SONET hierarchy for North America. These systems operate at the OC-1, OC-3, OC-12, and OC-48 rates and can be used to form a SONET network.

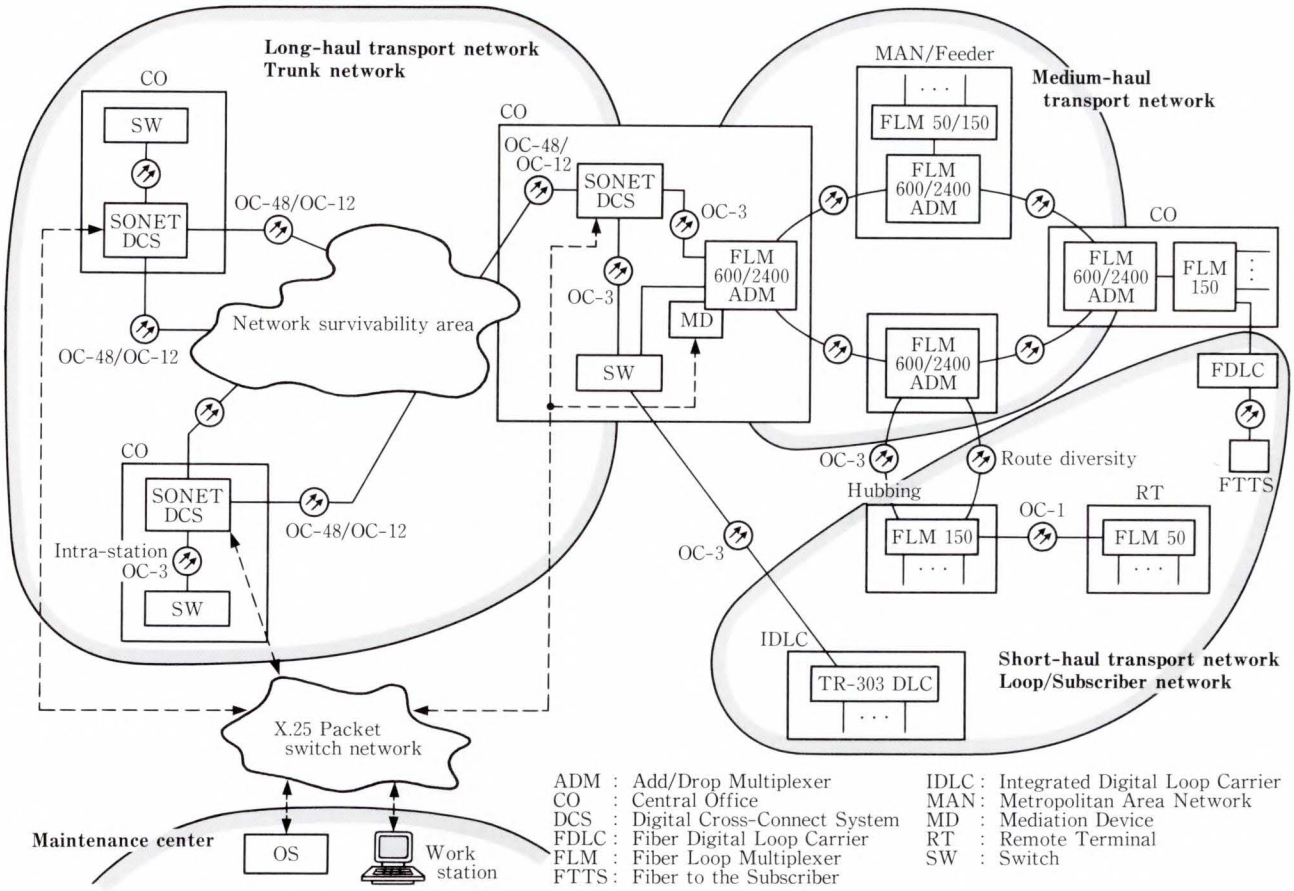


Fig. 1—System application for SONET.

2.1 System application

Most applications for Fujitsu's asynchronous optical transmission equipment were previously in point-to-point networks. For long-distance trunk lines, optical repeating equipment was placed between the terminals. Lines were extended, dropped, and inserted by back-to-back terminal installations using hard wiring.

An expanding network has increasing need for such services as Broadband ISDN, ring applications by the Add/Drop Multiplexers (ADMs), and digital cross-connect systems (DCSs). These features provide high quality, network survivability, and self-healing attributes in addition to traditional transmission capability[5].

To cope with the various and increasing services required by customers, the operating companies need to have a network which can be flexibly configured remotely according to the customers' requirements. This is the reason why a synchronous multiplexing format, such as SONET, was developed.

The mid-span meet capability was developed to allow multi-vendor networks to be created which include the signal transport and Operation, Administration, Maintenance and Provisioning (OAM&P) functions required from the operating companies[6),7)].

With this background, the ANSI T1 committee and CCITT are accelerating the standardization of SONET which enables mid-span meet.

Fujitsu is developing the FLM series SONET products to provide for flexible implementations of the requirements described above. Figure 1 is an example of the SONET network application that the FLM series can offer.

2.2 SONET FLM series

Fujitsu's FLM series was introduced to support the total SONET system approach

Table 1. System parameters of FLM series

Item	FLM 50	FLM 150	FLM 600
Line rate	51.84 Mbit/s (OC-1 or STS-1)	155.52 Mbit/s (OC-3 or STS-3*)	622.08 Mbit/s (OC-12)
Transmission capacity	672 telephone channels	2 016 telephone channels	8 064 telephone channels
Multiplexing	Positive/negative synchronization, byte interleaving		
Tributary	DS1 x 28 (2-system)	DS1 x 84 DS3 x 3 STS-1* x 3	DS3 x 12 STS-1* x 12 STS-3* x 4 OC-3* x 4
Mapping	VT 1.5 asynchronous mapping floating VT 1.5 bit synchronous mapping floating DS3 direct mapping		DS3 direct mapping STS-1 byte interleave multiplexer
Line code	Scrambled-NRZ		
Light wavelength	1.31 μm	1.31 μm or 1.55 μm	
Optical source	FP LD	1.31 μm: FP LD 1.55 μm: DFB	1.31 μm: FP LD or DFB 1.55 μm: DFB
Optical detector	Ge-APD	1.31 μm: Ge-APD 1.55 μm: InGaAs-APD	
Protection	Low-speed: 1 : 7 High-speed: 1 + 1, power duplication		Low-speed: 1 : 4 High-speed: 1 + 1 Power duplication
Switching scheme	Forced, auto, manual (Lock-in, lock-out, features)		
Switching time	Less than 60 ms (BER exceeds 10^{-3} at line rate)		
Supervisory	TBOS, Parallel**, NMA (TL-1 interface), FJT proprietary interface***		
Orderwire	2-wire** or 4-wire		
External environmental alarm (input/output)	Alarm: 8 items,	Status: 4 items,	Control: 4 items
Craftperson interface Performance monitor Physical inventory Control Alarm/status Provisioning	ASCII terminal (1 200-baud) Low-speed/high-speed bit error, OOF counts Plug-in unit data Loopback, switching Summary/detailed alarm, status monitor Provision of all-plug-in units		
Synchronization	External reference input: 2 inputs (primary & secondary) External reference output: 2 outputs (primary & secondary)		

*: Future option **: It is provided for FLM 50/150 only.
***: This interface is used for connection to Fujitsu SV system (FAMS: Fujitsu Alarm & Maintenance System) and is provided for FLM 50/150 only.

in the North America transmission market. As first generation products, Fujitsu is supplying the FLM 50/150, FLM 600 and FLM 2400.

Table 1 lists the system parameters of the FLM series and Fig 2 shows the system hierarchy. As shown in Fig. 2, entire SONET hierarchies can be constructed from combinations of the three types of FLM systems. The following shows an overview of each FLM configuration.

2.2.1 FLM 50/150

The FLM 50/150 is an optical transmission

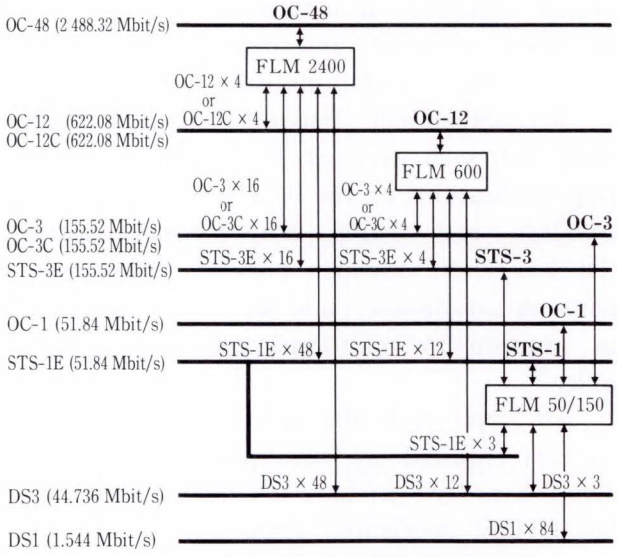


Fig. 2—Hierarchy for SONET FLM series.

system used primarily in the loop network. The product features an integrated floating virtual tributary (VT) or M13 multiplexer permitting flexible networks. Other features include an operating temperature range from −40 °C to +65 °C, compact packaging, and reduced power drain for installation in a cabinet.

The main components the FLM 50/150 are as follows:

1) Terminal
2) ADM-Linear
3) ADM-Ring
4) Fiber Hubbing (50 Mbit/s Fiber Extension)
5) M13/STS-1 Multiplexer.

2.2.2 FLM 600

The FLM 600 is a 600 Mbit/s optical transmission system used primarily in the interoffice or trunk network. This equipment can be used to transport asynchronous DS3 signals in the same manner as conventional Fuditsu asychronous optical systems, such as the 405/810 Mbit/s line terminal equipment. This enables the operating companies to immediately deploy the FLM 600 with the capability for future expansion. The FML 600 can be upgraded to the FLM 2400 without affecting traffic.

The main components of the FLM 600 are as follows:

1) Terminal
2) ADM-Linear
3) ADM-Ring
4) Fiber Hubbing (150 Mbit/s Fiber Extension).

2.2.3 FLM 2400

In the trunking system, ultra high-speed optical systems with advanced network survivability technologies should be introduced.

The FLM 2400 is a 2.4-Gbit/s optical transmission system to be used in the next generation of trunk network. The FLM 2400 system will be supplied with a 1:n protection switching capability.

As described in Subsect. 2.2.2 the Flm 2400 can be constructed by upgrading the FLM 600 or is available as a stand-alone FLM 2400 LTE.

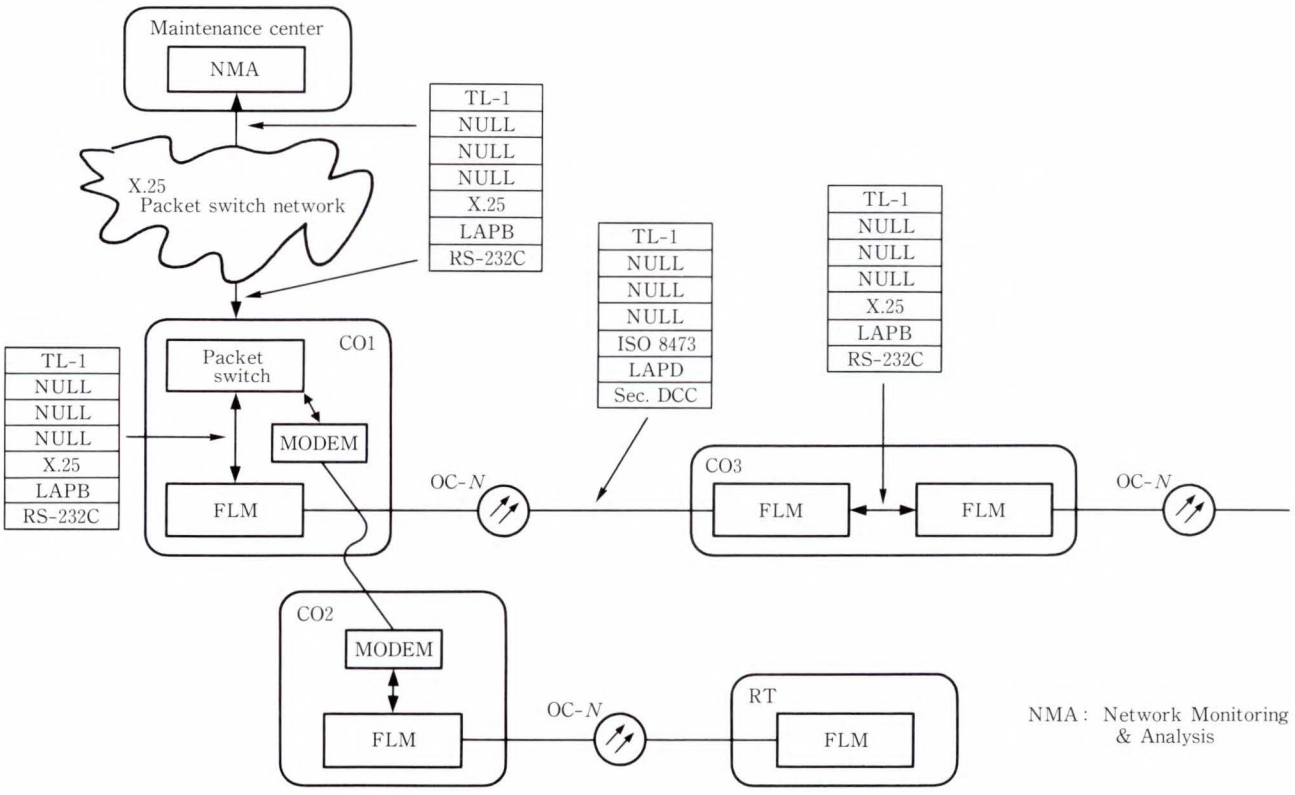


Fig. 3—Current operating system.

3. Operations support

3.1 Current operational support systems

The requirements for supporting SONET have not been completely standardized and are under discussion at T1 and CCITT. Because the industry is in transition from earlier asychronous optical systems to SONET systems, we must consider connecting SONET equipment to existing operations systems (OSs) which support asynchronous systems.

Accordingly, this section describes current practices for connection to the network monitoring & analysis (NMA) OS deployed by the RBOCs in North America. NMA is used to record and retrieve information on alarms and the status and performance data of network elements (NEs).

It is difficult for Fujitsu to undertake the primary development of the interface for connection to NMA alone. Fujitsu must work on this stage of development with its customers and Bell Communications Research (Bellcore).

The block diagram in Fig. 3 shows the connection from NMA to the FLM series being developed by Fujitsu. Methods of making such connections are now being discussed with the RBOCs and Bellcore.

3.2 SONET operating systems/SONET Phase II upgrade

The SONET Phase I standard established the necessary specifications to ensure a traffic mid-span meet. By this we mean that it is possible to transmit traffic (DS1s, DS3, etc.) from a network element from one manufacturer to another. This is analogous to the situation of building a network which contains M13 multiplexers from different suppliers. DS1s are reliably multiplexed and demultiplexed but many of the desired operation support features are not standardized and therefore not available.

SONET Phase II was to finish the specifications of the protocols and messages used to communicate OAM&P information over the SONET Phase II interface. Figure 4 illustrates the protocols and where they exist in the network. The DCC refers to the embedded operations channel (EOC) in the SONET interface (the NE-to-NE link). The local communica-

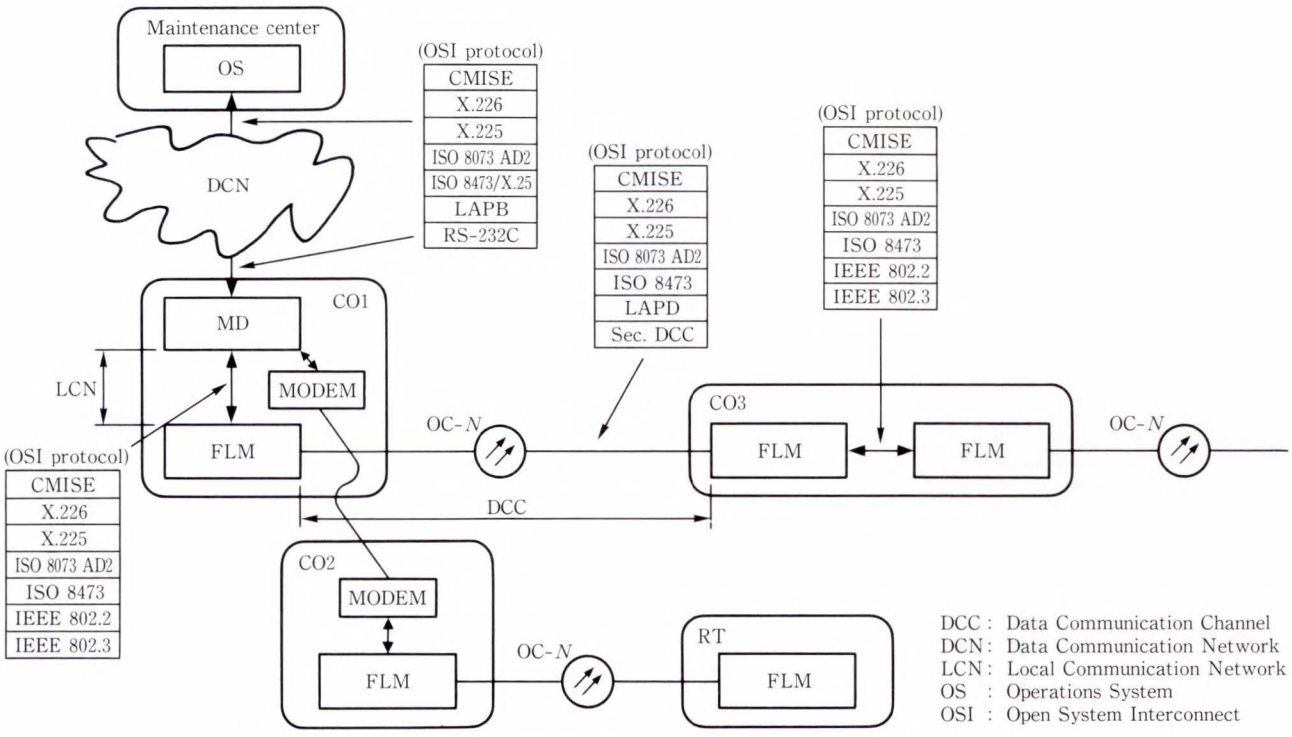


Fig. 4—SONET operating system.

tions network (LCN) refers to the local area network interface used to communicate between the NE and the OSs. As shown in the figure, a mediation device can be used to convert the local area network protocol used in the LCN to the protocol required by the OS. Notice also that all of the upper layers (layers 4 to 7) are the same for all protocol stacks. SONET was released in these phases because one is able to migrate from Phases I to II and beyond by replacing the read only memories (ROMs) or by downloading software.

Unfortunately, the T1 committee did not complete the specifications of the CMISE messages to be used over the DCC in the Phase II specifications. However, an agreement was reached on the protocol stacks. It is anticipated that the first set of messages will be available in the first half of 1991. This will allow suppliers to implement the necessary protocols and update the messages when appropriate.

For the next several years, SONET interfaces will most likely communicate using transaction language 1 (TL-1) messages. This is because many of the customers' OSs only accept TL-1 and will not be in a position to accept CMISE messages for several years. Translation from abstract syntax notation 1 (ASN.1) to TL-1 is not practical in the smaller network elements which implement many of the SONET interfaces. Therefore development of ASN.1, even though it may be standardized, will be outpaced by the development of OSs which can accept the new message format.

4. Equipment design

4.1 FLM 50/150

This equipment multiplexes the North America DS1 and DS3 signals into the synchronous transport signal level 1 or level 3 (STS-1 or STS-3 shown in Fig. 5) of the SONET frame format, for transmission at the optical level of OC-1 or OC-3.

Figure 6 is a block diagram of the FLM 150.

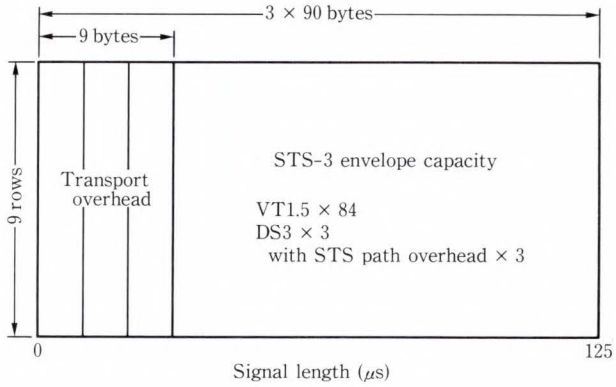


Fig. 5—STS-3 (155.52 Mbit/s) frame structure.

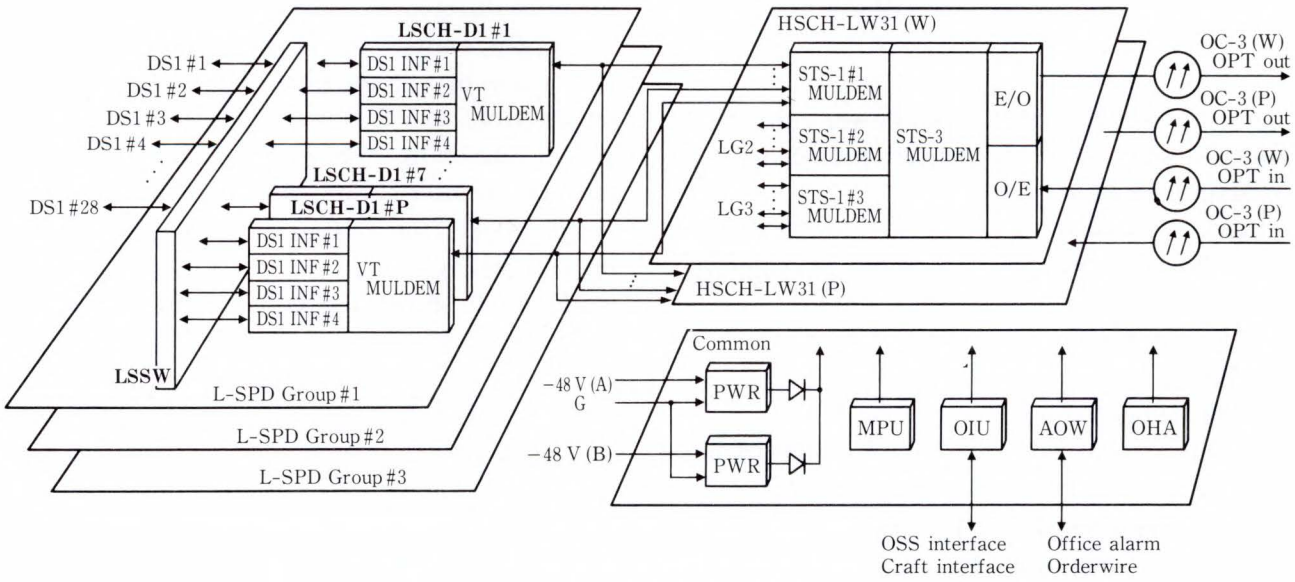


Fig. 6—Block diagram of FLM 150.

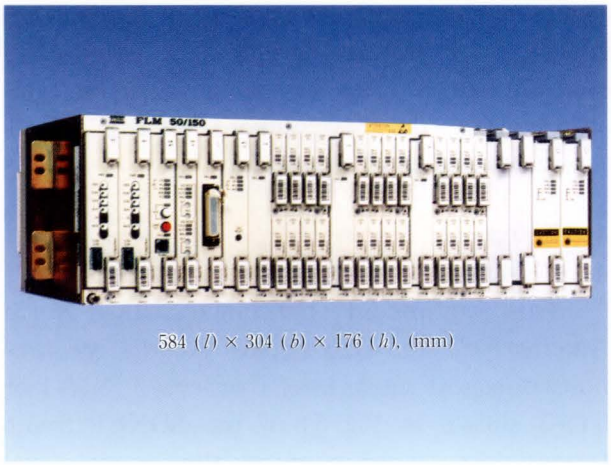


Fig. 7—FLM 50/150.

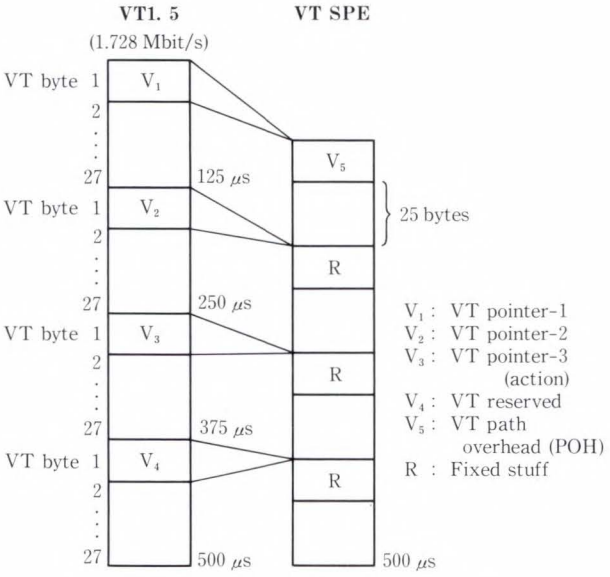


Fig. 8—VT1.5 superframe structure.

Figure 7 shows the front view. Power consumption is 72 watts when 84 DS1s are provided.

1) Mapping and pointer action

The FLM 50/150 uses the floating VT and DS3 asynchronous mapping to support the following payloads:

1) DS1 asynchronous
2) DS1 bit-synchronous
3) DS3 asynchronous.

Figure 8 shows the VT1.5 superframe structure. The FLM 50/150 has the following SONET characteristics: Enabling a positive bit stuffing operation to absorb the offset of input frequency in asynchronous signals,

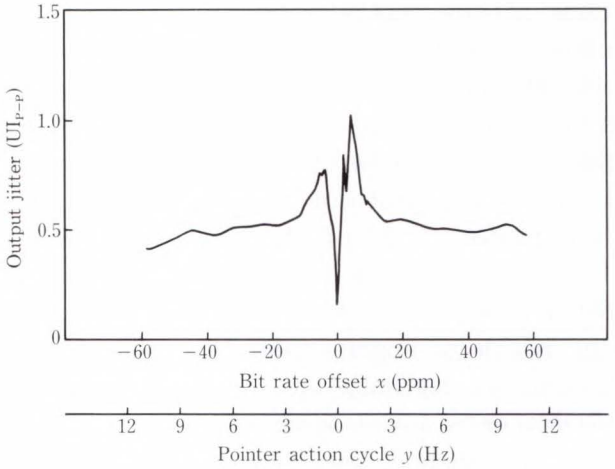


Fig. 9—DS1 bit-synchronous output jitter.

Table 2. Output jitter and DPLL parameters

	DPLL design
Sampling frequency (MHz)	49.408 (1.544 x 32)
Buffer stages	72
DPLL counter value	256
Output jitter (UI_{p-p})	1.05

and pointer action operations to absorb the fluctuation of synchronous timing.

This timing fluctuation is due to the jitter/wander from the building integrated timing supply (BITS) or external synchronous circuits in the NEs, and also plesiochronous operation spanning different synchronous islands.

A gap exists with a maximum of 3 bytes in a cycle of 125 μs when extracting the DS1 signals from a VT format. If a pointer action occurs, one more byte gap is added. The byte gap at a pointer action, which occurs in a slow cycle, affects the output jitter of DS1s from the equipment.

Figure 9 shows the DS1 output jitter with VT pointer actions occurring in a bit-synchronous mapping.

A digital phase-locked loop (DPLL)[8] with low cut-off frequency characteristics was utilized to achieve these results. Table 2 shows the output jitter and DPLL parameters.

This jitter was produced by changing the input bit rate in the bit-synchronous floating

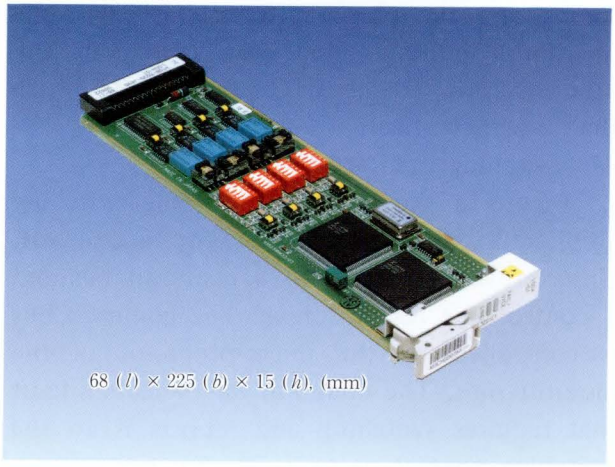
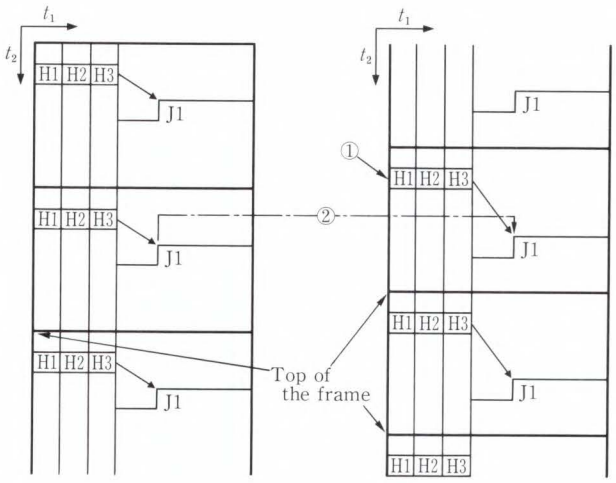


Fig. 10—DS1s channel unit (LSCH-D1).



①: Insert the pointer value indicating the timing of input J1.
②: Send data without delay after receiving it.

Fig. 11—STS pointer processing (normal operation).

mode and causing VT pointer actions.

Because there is a maximum of 500 (2-ms cycle) pointer actions per second, the average frequency of the VT pointer action y when the DS1 frequency is dislocated by x ppm is

$y = 0.193\ x$ (Hz).

According to the Bellcore specifications, the output jitter shall be no more than 1.5 UI peak-to-peak[9]. The above-mentioned DPLL satisfies this requirement.

2) Minimization of equipment

To minimize the size of the equipment, Fujitsu developed the following:

i) Large scale integration (LSI) circuits for the mapping functions (five 12 000-gate CMOS ASICs, one ECL ASIC)

ii) Modular optical/electrical converter (O/E, E/O)

iii) Surface mount technology (SMT) DS1 channel unit.

Since the sub-STS signals are transmitted via VT groups (VTGs) at 6.912 Mbit/s (equivalent to 4 DS1s) when multiplexing DS1 signals into the SONET frame, four channels were mounted on one DS1 tributary unit for minimum size.

Two LSIs (12 000 gates each and packaged in a Quad Flat Package) are used to multiplex/demultiplex four DS1s into a VT group. Functions included in this LSI are mapping the DS1s into floating VT1.5s and multiplexing the VT1.5s into a VT group. Figure 10 is a photo of the channel unit.

3) Hubbing

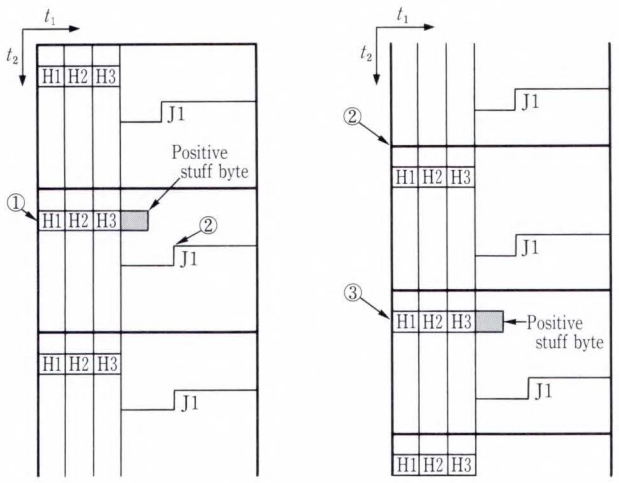
Hubbing is an application where one STS-1 SPE from an OC-3 is transmitted to an OC-1 without terminating the path as shown in Fig. 1.

When an STS-1 in the incoming OC-3 signal is taken out and placed into the OC-1 signal to be sent to a remote station, the data delay must be minimized for all frequency offsets (e.g. offset of input frequency and output frequency) and data slips must not occur. This equipment minimizes the data delay and eliminates slips through the use of STS pointers and enables all frequency offsets to be absorbed.

The left side of Fig. 11 shows the STS-1 frame format of the input optical signal. The right side shows the frame format of the output optical signal. The frame moves from t_1 to t_2. J1 in the figure is the first byte of the STS synchronous payload envelope (STS SPE).

To send an STS SPE without delay, the J1 byte (top of STS SPE) is mapped from the frame of the input optical signal to the frame of the output optical signal simultaneously. At the same time, a new STS pointer value is written to locate the start of the outgoing SPE.

The equipment can cope with any frequency offset. To do this, the equipment continually



①: Receiving pointer value with increment bits inverted.
②: Detect the phase difference between the input J1 and the output frame.
③: Invert the increment bits (new pointer value).

Fig. 12—STS pointer processing (with pointer action).

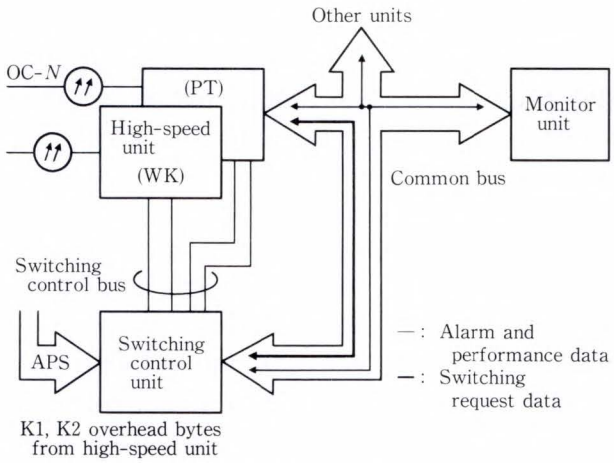


Fig. 13—Switching architecture.

supervises the SPE timing of the input optical signal and the frame timing of the optical signal to be sent by controlling the pointer value. (When the equipment detects a phase difference of eight or more bits in the buffer memory by using a phase comparator, the pointer value is incremented or decremented in the output optical signal.) Figure 12 shows an example of incrementing the pointer for in an incoming optical signal.

For the pointer to be incremented, the J1 timing phase differs by eight bits. If the phase of the frame of the output optical signal is compared with the phase of the transmit J1 timing and the phase difference is eight bits or more, the equipment can increment the pointer value at the next frame and absorb the frequency offset.

4) Switching architecture

Figure 13 shows the optical line switching architecture. Each box in the figure is one unit. Units are connected with a common bus and a control line for switching. The common bus is controlled by the micro-processor of the monitor unit. The common bus detects a fault that requires switching and reports it to the switching control unit. It functions as a fault monitor, performance monitor, and maintenance control unit.

The processor detects and processes the cause of switching in cycles of 10 ms or less to allow switching within 50 ms. It reports other performance data in a slower cycle. A multi-task operating system is installed in the monitor micro-processor and a timer-interrupt is used independently of the operating system to activate 10-ms processing decisions.

In addition, the micro-processor in the switching control unit independently controls automatic protection switch (APS) according the protocol used over the K1 and K2 overhead bytes in conjection with the remote station.

5) Temperature requirements

Transmission systems such as the FL 50/150 when used in the loop area are often required to operate in uncontrolled environments. In the U.S., the range of expected temperatures inside a cabinet, pedestal, or other enclosure used to house the equipment, generally ranges from $-40°C$ to $+65°C$[10]. To withstand large temperature ranges, the FLM 50/150 is manufactured by temperature-screening on a component basis.

A 100-cycle temperature test implemented by Fujitsu and Bellcore has demonstrated that the equipment meets all specifications over the larger temperature range.

4.2 FLM 600

The FLM 600 equipment converts an OC-12 signal into DS3, STS-1 or STS-3 tributaries and vice versa.

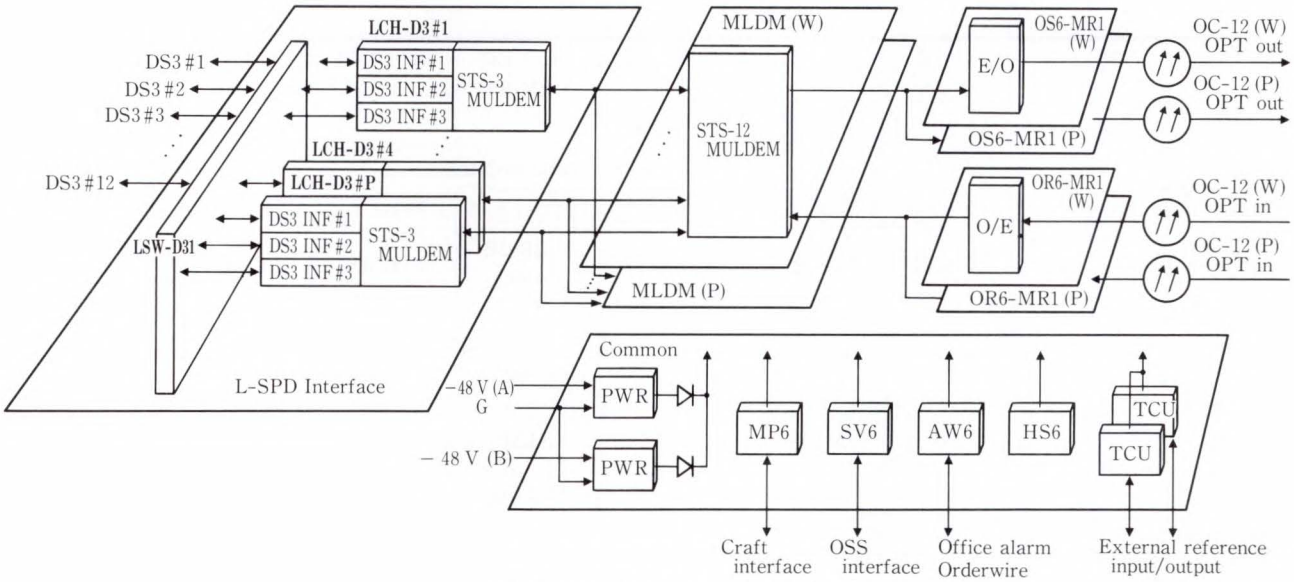


Fig. 14—Block diagram of FLM 600.

Figure 14 is a block diagram of the FLM 600 terminal equipment. MUX/DMUX, the optical sending and optical receiving units have a 1 + 1 redundancy. The tributary units consist of four working units and one protection unit operating in a 1:4 redundant structure. The high-speed units and the switching system in the tributary units are designed to operate independently to improve system reliability.

Most circuits are designed in LSIs. Principally eight parallel signals are used to handle the SONET frame format in the MUX/DMUX unit having 622.08-Mbit/s capacity. Therefore the maximum frequency of the parallel lines is 77.76 Mbit/s to enable stable operation and reduce power demand. The 622.08-Mbit/s high-speed signals are processed from parallel to serial and in reverse in the optical send and recieve units. This high-speed conversion is accomplished with state-of-the-art GaAs-ICs, which also reduce power demand.

Figure 15 shows the FLM 600 LTE. The power requirement is 114 watts when fully loaded. Up to four terminals can be mounted in a 7-foot rack. No fans are required due to the low power consumption of the equipment.

Fujitsu is planning a flexible system architecture having various tributary interfaces including an upgrade from the FLM 600 to FLM 2400. This transmission system, operating at OC-48, is also being developed as one of the FLM series.

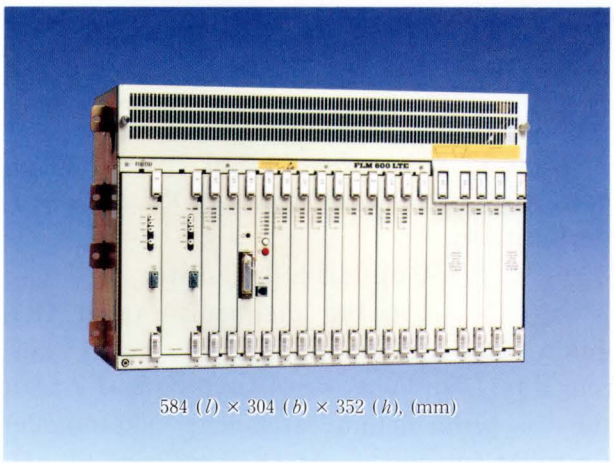


Fig. 15—FLM 600 LTE.

4.3 Optical interface

For the SONET optical interface, it is essential that the interface conforms to the criteria for mid-span meets and environmental conditions at an installation site.

Minimization, low power consumption, and adaptability to the larger temperature ranges are required for loop systems with OC-1 or OC-3 interfaces. In trunking systems with OC-12 or OC-48 interfaces, ultra high-speed devices and the modulation method are key technologies.

This section focuses on the OC-1, OC-3, and OC-12 interfaces.

Table 3. FLM50/150/600 optical path design

Item \ OC level	OC-1 IR 1.31 μm	OC-3 IR 1.31 μm	OC-3 LR 1.31 μm	OC-3 LR 1.55 μm	OC-12 IR 1.31 μm	OC-12 LR 1.31 μm	OC-12 LR 1.55 μm
Line rate (Mbit/s)	51.84	155.52			622.08		
Line code	Scrambled-NRZ						
Center wavelength (nm)	1 270-1 340	1 270-1 340	1 285-1 330	1 525-1 575	1 291-1 333	1 300-1 320	1 525-1575
Spectral width (nm)	7 (RMS)	7 (RMS)	4 (RMS)	1 (20 dB down)	4 (RMS)	2 (RMS)	1 (20 dB down)
Optical power (dBm)	−15	−15	−2	−4	−15	−3	
Minimum receiving level (dBm)	−30	−30		−39	−30	−31	−32
LD type	MLM	MLM	MLM	SLM	MLM	MLM or SLM	SLM
APD type	Ge	Ge	Ge	InGaAs	Ge	Ge	InGaAs
Power penalty (dB)	1	1			1		
Cable dispersion (ps/nm)	100	100	160	2 000	80	110	1 500
Max span (km)	15	15	40	100	15	40	80

RMS: Root Mean Square MLM: Multi-Longitudinal Mode SLM: Single-Longitudinal Mode

4.3.1 Optical path design

Table 3 gives the optical path design parameters conforming to the SONET Phase I specifications.

1) FLM 50/150 optical path design

At OC-1, using the intermediate reach (IR) option, data can be transmitted over 15 km using a 1.31-μm Fabry-Perot laser diode (FP-LD) and a germanimum avalanche photodiode (Ge-APD) detector[11]. At OC-3 utilizing FP-LD and APD for both the 1.31-μm IR option and 1.31-μm long-reach (LR) option, data can be transmitted over 15 km with IR or 40 km with the LR 1.31 μm. At OC-3 using the 1.55-μm LR option, data can be transmitted over 100 km using a distributed feedback laser diode (DFB-LD)[12] and InGaAs-APD.

In the 1.31-μm systems of OC-1 and OC-3, since optical fiber dispersion is small, the distance is restricted only by optical fiber loss. In the 1.55-μm system at OC-3 using a non-dispersion shifted fiber whose dispersion per kilometer is 20 ps/nm, the total system dispersion for 100 km is 2 000 ps/nm. Therefore the power penalty is set to 1 dB due to the fiber dispersion. For this power penalty, the side mode suppression ratio of the 1.55-μm DFB-LD must be 30 dB or more.

2) FLM 600 optical path design

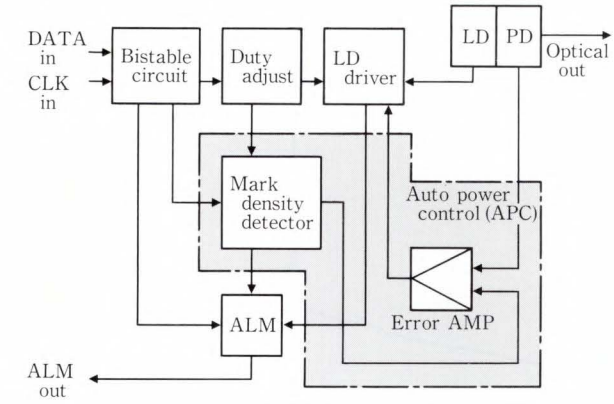
With the 1.31-μm IR otpion of OC-12, 15-km transmission can be achieved with 1.31-μm FP-LD and Ge-APD. The 1.31-μm LR option of OC-12 provides 40-km transmission utilizing a 1.31-μm DFB-LD and Ge-APD. With the 1.55-μm LR option of OC-12, up to 80-km transmission is accomplished with a 1.55-μm DFB-LD and InGaAs-APD. With the 1.31-μm and 1.55-μm IR/LR options of OC-12, the power penalty is set to 1 dB due to the fiber dispersion.

4.3.2 Optical module design

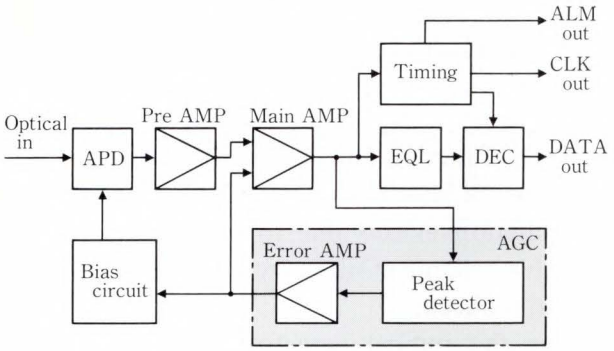
In the FLM 50/150/600 systems, optical modules are being designed according to the fiber span length. The 1.31-μm IR optical module at OC-1 and OC-3 levels is designed without a Peltier cooling element for temperature conditions from −40°C to +65°C to reduce the power cinsumption.

This section describes the minimum-size optical modules for LR OC-3 (1.55 μm) and for LR OC-12 (1.31 μm) used for trunk lines.

Figure 16 is a block diagram of the electrical/optical converter (E/O) module and the optical/electrical converter (O/E) module.



a) E/O module



b) O/E module

Fig. 16—OC-1, 3, 12 module block diagram.

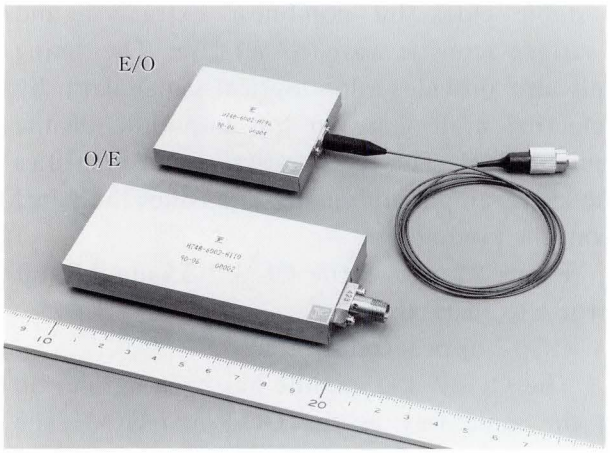


Fig. 17—OC-3 1.55 μm E/O, O/E module.

Figure 17 is a photo of the E/O module containing the DFB-LD and the O/E module used in the OC-3 1.55-μm LR option.

Figure 18 is the E/O and O/E module used in the OC-12 1.31-μm LR option.

1) OC-1/OC-3 optical transmitter

To cope with high-density module mounting,

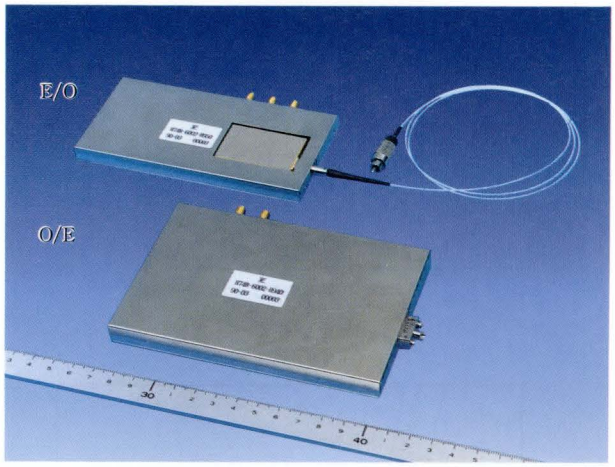


Fig. 18—OC-12 1.31 μm E/O, O/E module.

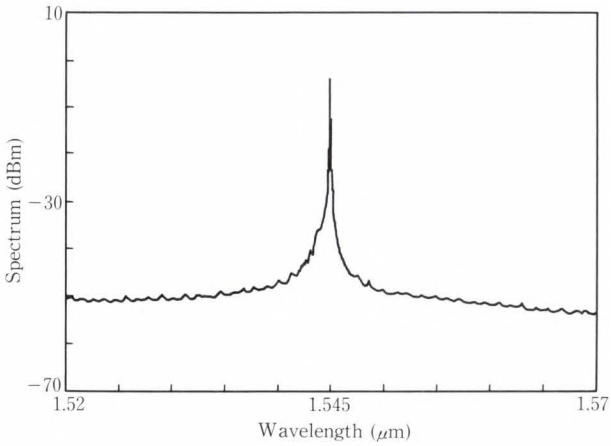


Fig. 19—OC-3 optical output spectrum.

the size of each functional block needs to be minimized. However, minimizing the LD module in the optical send-receive unit was restricted by its shape.

To minimize the transmitter, Fujitsu has developed an LD module by applying the following technology to the drive circuit:

i) Integrated circuits (ICs) using Si-bipolar processes (Two ICs)

ii) Reduction of heat resistance by utilizing ceramic substrates

The pulse width of the input data is controlled by a bistable circuit and duty-cycle adjustment circuit. The LD drive unit drives the LD with the required current. The automatic power control (APC) circuit stabilizes the optical output power. The APC circuit amplifies the

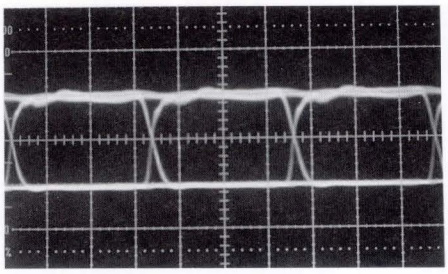


Fig. 20—OC-3 optical output waveform.

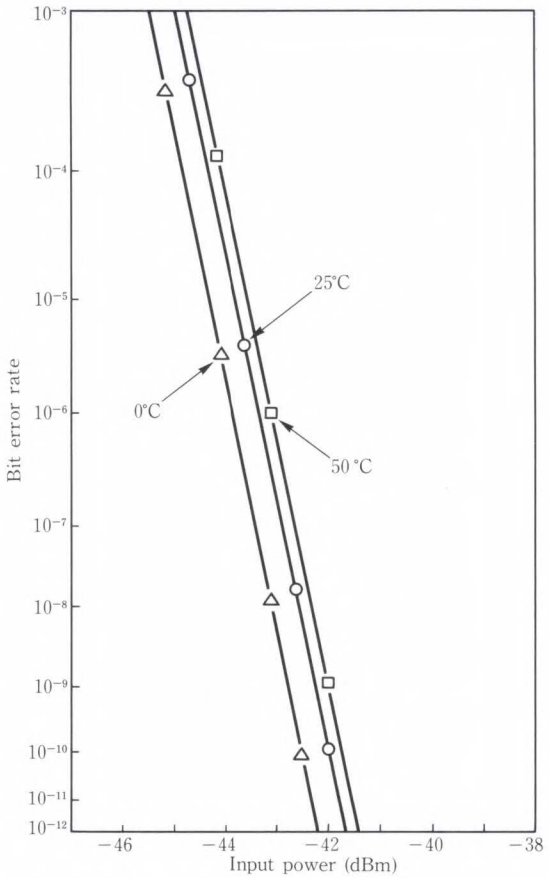


Fig. 21—OC-3 LR (1.55 μm) bit error rate characteristics.

transmitter optical signal detected by the photodiode monitor and stabilizes the optical output power by feedback control. This module also has an LD current alarm function for detecting excessive LD current.

Figure 19 shows the optical output spectrum characteristics of the DFB-LD module using an OC-3 1.55-μm LR option.

Figure 20 shows the optical output waveform at OC-3, 1.55-μm LR.

2) OC-1/OC-3 optical receiver

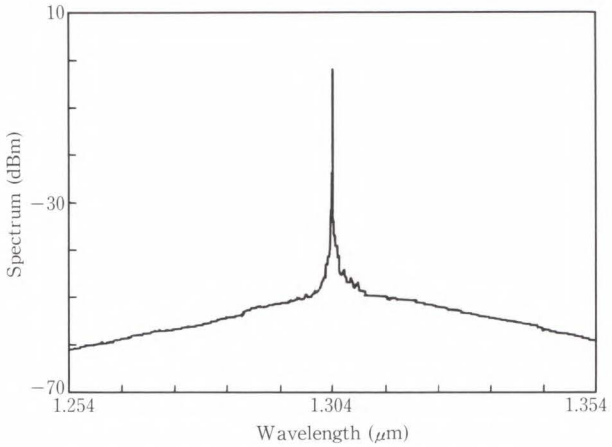


Fig. 22—OC-12 optical output spectrum.

Each function block consists of the appropriate Si-bipolar process ICs. In addition, the radiation effects due to modules mounted on highly reliable miniaturized ceramic substrate are also reduced.

For the optical detector, Ge-APD is used for the 1.31-μm option and InGaAs-APD is used for 1.55 μm. The current from the APD is amplified to the required level by a preamplifier and main amplifier. The timing unit regenerates a stable clock by non-linear extraction and a surface acoustic wave (SAW) filter. The timing unit also provides a low optical signal alarm by detecting a decrease in the amplitude of the timing signal. The regenerative circuit identifies the signal amplified equally and issues the signal from the module.

Figure 21 shows the OC-3 1.55-μm LR bit error rate characteristics.

3) OC-12 optical transmitter

The OC-12 LD module has been minimized in the same way as the OC-1 and OC-3. The block diagram of the E/O module is the same as that of the OC-1 and OC-3.

Figure 22 shows the optical output spectrum of the DFB-LD module in the OC-12 1.31-μm LR. Figure 23 shows the OC-12 1.31-μm optical output waveform.

4) OC-12 optical receiver

Each block consists of the appropriate Si-bipolar process ICs in the OC-12 module in the same way as the OC-1 and OC-3. The

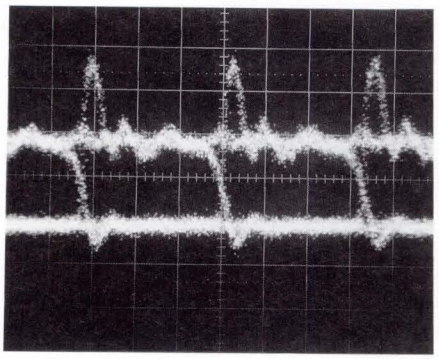


Fig. 23—OC-12 optical output waveform.

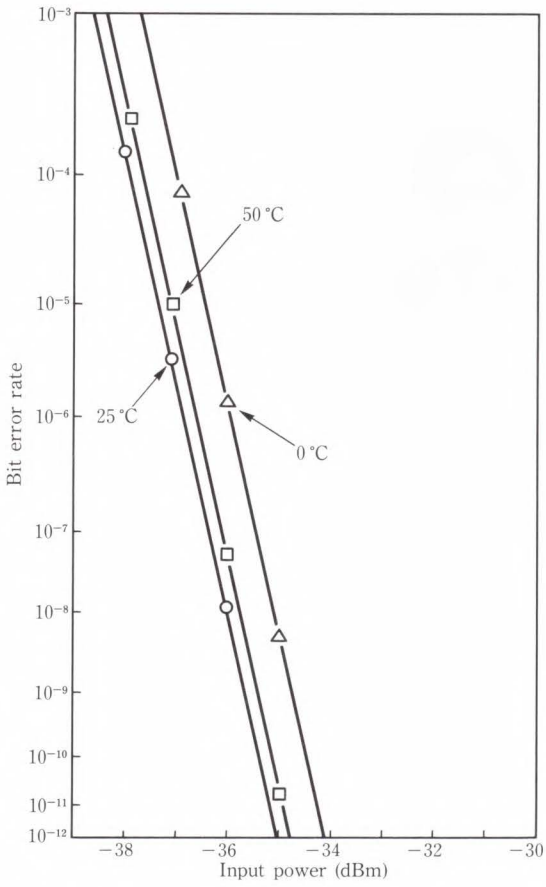


Fig. 24—OC-12 LR (1.31 μm) bit error rate characteristics.

block diagram of the O/E module is the same as that of the OC-1 and OC-3.

Figure 24 shows the OC-12 1.31-μm LR bit error rate characteristics.

5. Conclusion

Fujitsu has developed and delivered the FLM 50/150 and FLM 600 terminal equipment conforming to the SONET Phase I specification to RBOCs ahead of its rivals. A Phase II package is being developed to upgrade existing Phase I products to conform to Phase II standards. In addition, the FLM architecture will have enhancements to conform with future standards. To construct more flexible SONET networks in the future, an optical ADM, ring, and integrated digital loop carrier (IDLC) must be developed. The basic specifications and technology are common all over the world. Therefore, Fujitsu will provide the international market with SONET products, referred to in CCITT as synchronous digital hierarchy (SDH). Accomplishing this requires the mass production of gigabit optical and LSI technology. It is also important to review with the customers the operation, control, and maintenance functions, including Phase II and beyond.

SONET systems are developing towards the subscriber and inhouse delivery of broadband ISDN. Further study and development are required to greatly reduce system costs for the economical introduction of these advanced services.

Fujitsu intends to promote a total SONET approach in line with its goal of becoming a world lead in the field.

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Conductive Fur Brush Charging of a Dielectric Surface

• Masahiro Wanou • Masatoshi Kimura *(Manuscript received September 12, 1990)*

Charging of a dielectric surface without corona discharge has been achieved using a conductive fur brush to which an electrical potential of several hundred volts is applied. In this method, it was observed that brush charging is accomplished by direct charge transfer, gas discharge, and triboelectric charging. Direct charge transfer, the primary charging process, was analyzed using an ohmic contact model. The charged potential is nearly proportional to that of the brush. When the charging time exceeds 0.3 seconds, the charged potential on the surface of the photoreceptor saturates at almost the potential of the brush. Brush charging is, therefore, useful as a low-voltage charging technique.

1. Introduction

Corona charging is a well-developed technique, and is generally used in electrophotography[1),2)]. However, the corona charging device requires several thousand volts to produce corona emission; also, it generates ozone, which can damage other devices such as photoreceptors. Therefore, a new low voltage charging method is required.

It is known that a conductive brush maintained at several hundred volts and placed in contact with a dielectric surface can transfer its charge to the dielectric. However, there is no detailed report available on brush charging. Also, although transfer using a low voltage to create a charge pattern on a dielectric layer has been studied for electrography[3),4)]. These studies investigated the amount of charge applied from styli less than 100 μm in diameter.

Fujitsu has analytically and experimentally investigated conductive fur brush charging. Brush charging experiments were carried out with Mylar film and photoreceptors.

2. Brush charging model[5)]

A conductive fur brush maintained at several hundred volts and placed in contact with a dielectric surface can apply its charge to the dielectric surface. In this method, there are three charging processes. These are: direct charge transfer due to contact between the brush fiber and dielectric surface, charge transfer by gas discharge in the small air gap between the fiber tips and surface, and triboelectric charging. The triboelectric charge depends on the surfaces of the two materials that rub together[6)] and is less than the charges due to the other two processes. Therefore, direct charge transfer and gas discharge only were analyzed.

2.1 Direct charge transfer

A model and its equivalent circuit for brush charging are shown in Figs. 1 and 2 respectively. In the equivalent circuit the conductive brush is regarded as a resistor, the dielectric layer as a capacitor, and the brush-dielectric interface as a capacitor in parallel with a resistor. For simplicity, the brush-dielectric interface is treated as an ohmic contact.

During charging, a real charge q_r flows through the contact region of the brush fiber and dielectric and is deposited on the surface of the dielectric. Charge q_c is induced at the small air gap between the fiber tip and dielectric surface. Charge q_d is the sum of the induced charge q_c, real charge q_r, and initial charge on

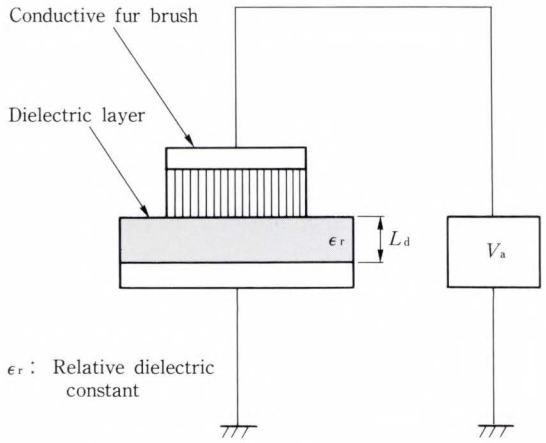

Fig. 1—Brush charging model.

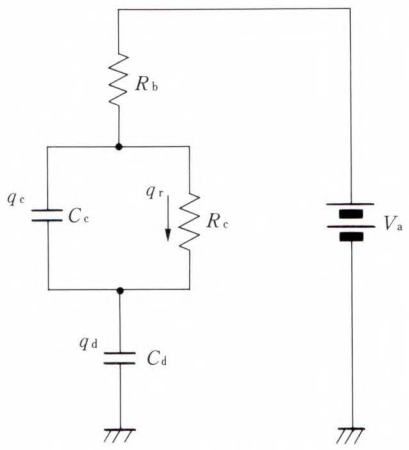

Fig. 2—Equivalent circuit.

the dielectric surface q_0. After the dielectric leaves the brush, the real charge q_r and the intial charge q_0 remain on the surface to form the surface potential of the dielectric.

In the equivalent circuit, the following equation is derived assuming that the initial values of q_c and q_r are zero.

$$q_r = q_d - q_c - q_0. \quad \ldots\ldots\ldots (1)$$

The voltage across the brush-dielectric interface is as follows:

$$R_c \frac{dq_r}{dt} = \frac{q_c}{C_c}, \quad \ldots\ldots\ldots\ldots (2)$$

where R_c is the resistance of the contact region and C_c is the capacitance of the small air gap. Potential V_a applied to the brush can be represented by:

$$V_a = R_b \frac{dq_d}{dt} + R_c \frac{dq_r}{dt} + \frac{q_d}{C_d} \ldots\ldots (3)$$

Substituting Equation (1) with Equation (3), gives:

$$V_a = R_b \frac{d}{dt}(q_c + q_r + q_0) + R_c \frac{dq_r}{dt} + \frac{q_c + q_r + q_0}{C_d} \ldots\ldots\ldots\ldots (4)$$

Also, by substituting Equation (2) with Equation (4) and rearranging, the following differential equation for q_r is obtained:

$$A \frac{d^2 q_r}{dt^2} + B \frac{dq_r}{dt} + q_r = C_d V_a - q_0, \quad \ldots (5)$$

Where $A = C_c C_d R_b R_c$,
$B = C_c R_c + C_d R_b + C_d R_c$.

It is assumed that q_0 is zero prior to charging. For further simplification, since R_b is low compared to R_c, brush resistivity R_b is ignored. By solving Equation (5) for q_r and substituting $R_b = 0$ and $q_0 = 0$, the charge applied to the dielectric is as follows:

$$q_r = C_d V_a \left[1 - \exp\left\{-\frac{t}{R_c(C_c + C_d)}\right\}\right]. \quad \ldots\ldots\ldots (6)$$

The equation for surface potential V_s then becomes:

$$V_s = V_a \left[1 - \exp\left\{-\frac{t}{R_c(C_c + C_d)}\right\}\right]. \quad (7)$$

2.2 Charge transfer by gas discharge

When the brush potential exceeds the breakdown voltage, a gas discharge takes place in the air gap between the brush fiber tips and dielectric surface. As the gas discharge proceeds, charge accumulates on the dielectric surface, reducing the potential across the brush-dielectric interface. The gas discharge is extinguished when the gap potential falls below the minimum value required to sustain the discharge. After extinction, the direct charge transfer discussed in the preceding section takes place. Since the gas discharge occurs in a very short time, the

charge due to the gas discharge is regarded as only an initial charge in the direct charge transfer process.

The extinction voltage between the brush and the ground plane of the dielectric V_{ex} is given by the following empirical equation[7]:

$$V_{ex} = V_{gex} + E_a \frac{L_d}{\epsilon_r} , \quad \ldots\ldots\ldots\ldots (8)$$

where V_{gex} is the extinction voltage of the air gap between the brush and dielectric surface, and E_a is the electric field on the dielectric surface. The gas discharge is extinguished when the potential on the dielectric surface reaches $V_{se} = V_a - V_{ex}$. Therefore, it is assumed that the dielectric has an initial charge $q_0 = C_d V_{se}$ on its surface prior to the direct charge transfer.

By solving the differential Equation (5) for q_r using the initial charge q_0, and by ignoring the small R_b, the charge and surface potential on the dielectric is as follows:

$$q_r = C_d \left[V_a - V_{ex} \exp \left\{ - \frac{t}{R_c(C_c + C_d)} \right\} \right] , \quad \ldots\ldots\ldots\ldots (9)$$

$$V_s = V_a - V_{ex} \exp \left\{ - \frac{t}{R_c(C_c + C_d)} \right\} . \quad \ldots\ldots\ldots\ldots (10)$$

3. Experiment

Figure 3 shows the experimental setup. A Mylar film and selenium-coated drum are used as electroreceptors. Aluminized Mylar films of 25-μm, 50-μm, and 75-μm thickness are mounted on a grounded metal drum. A conductive fur brush roll or bar brush is placed in contact with the surface of the electroreceptor. The conductive fur brush roll (32 mm diameter) consists of a metal core and conductive rayon fiber. The bar brush consists of a metal plate and conductive fiber. The values of the brush parameter were determined experimentally. The brush fiber density is 155 fibers per square millimeter. The diameter of the fibers is 10 μm, and the resistivity is 10^3 Ω·cm. A voltage of approximately −500 V to +700 V is applied to the brush. The probe of a surface potential meter is positioned over the drum. The probe output can be displayed visually on an X-Y plotter, or it can be digitized and stored for analysis.

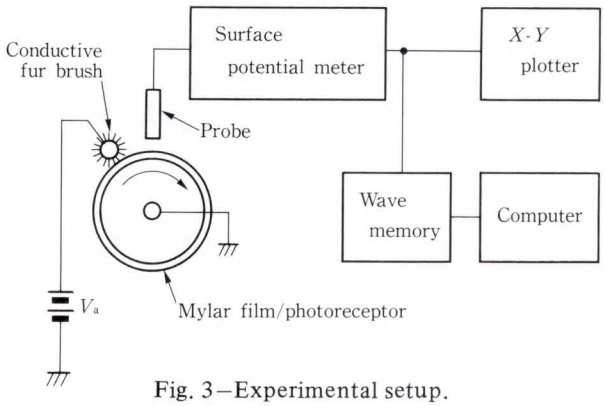

Fig. 3—Experimental setup.

The conductive brush roll was used to charge the Mylar film. The brush is maintained at a selected constant potential, and transfers a charge to the Mylar surface. The brush is rotated at 500 rpm to achieve charging with good uniformity. The drum is rotated at a surface velocity of 190 mm/s. Since the Mylar has a high resistivity, there is no charge decay. Therefore, a charge accumulates during multiple rotations of the drum. The charging time is controlled by controlling the number of drum rotations. The charge potential on the Mylar is measured using surface potential meter.

The photoreceptor drum was charged by the conductive bar brush. The bar brush is placed in static contact with the Se-Te drum surface. The measurement is made in the same way as for the Mylar except that the photoreceptor drum measurement is made in the dark.

4. Results and discussion

4.1 Triboelectric charge

Figure 4 shows the relationship between the surface potential V_s on the Mylar film and the charging time when the brush potential is fixed at zero. Figure 4 shows that V_s decreases with charging time. Even though the brush is grounded, a charge flows through the brush-dielectric interface. This charge flow is caused by the triboelectric phenomena. The magnitude

of the triboelectric charge is determined by the surface states of the materials rubbing against each other[6]. Therefore, the surface potential V_s increases with the thickness of the Mylar film L_d.

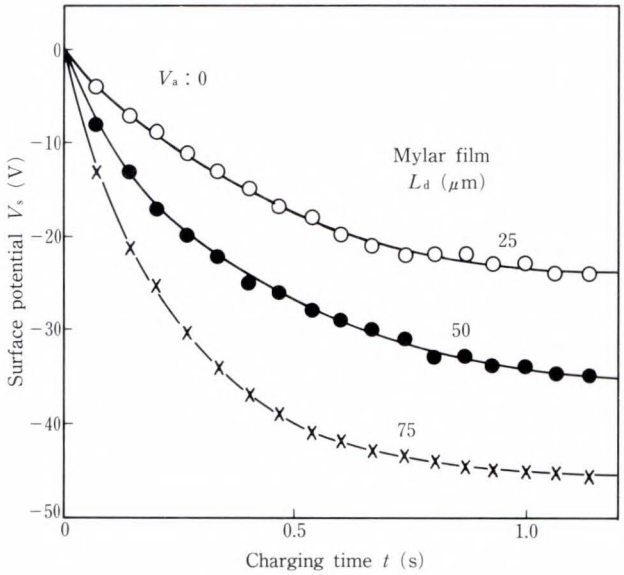

Fig. 4—Triboelectric charge for Mylar of various thickness.

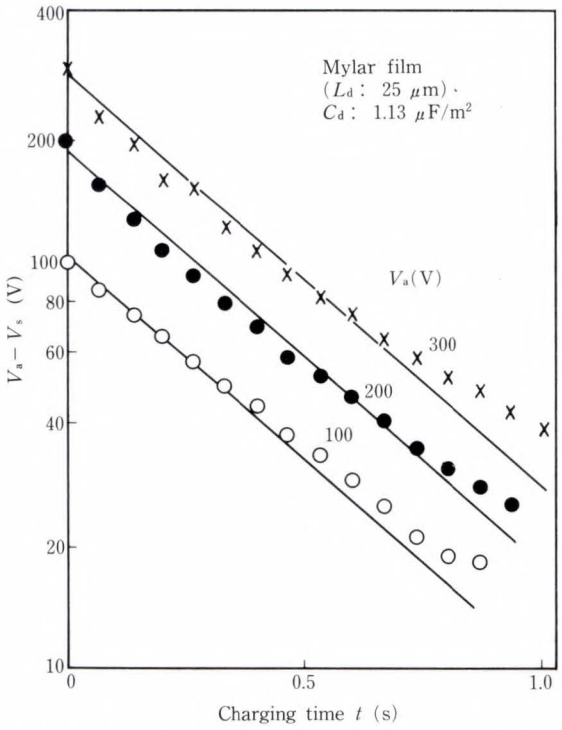

Fig. 5—Relationship between $V_a - V_s$ and charging time for direct charge transfer.

In the following discussions, the triboelectric charge was eliminated from the experimental results in order to investigate the charge transfer process.

4.2 Direct charge transfer

This section discusses the direct charge transfer process without gas discharge. By rearranging Equation (7), $V_a - V_s$ can be represented as:

$$V_a - V_s = V_a \exp\left\{-\frac{t}{R_c(C_c + C_d)}\right\} . \quad (11)$$

This shows that the logarithm of $V_a - V_s$ is a linear function of the charging time. Figure 5 shows the relationship between $V_a - V_s$ and the charging time when the parameter is the brush potential V_a, and the Mylar film thickness L_d is 25 μm. Figure 5 shows that the logarithm of $V_a - V_s$ decreases linearly with an increasing charging time and that the slopes of these lines are the same. The charging time constant of Equation (11) can be obtained from the slope of these lines and was found to be 380 ms. The capacitance of the dielectric C_d can be calculated from the Mylar film thickness L_d and its relative dielectric constant ($\epsilon_r = 3.2$). Capacitance C_c was measured at 0.18 μF/m^2 in the experimental setup. Using these values, resistance $R_c = 2.9 \times 10^5$ ohm-m^2.

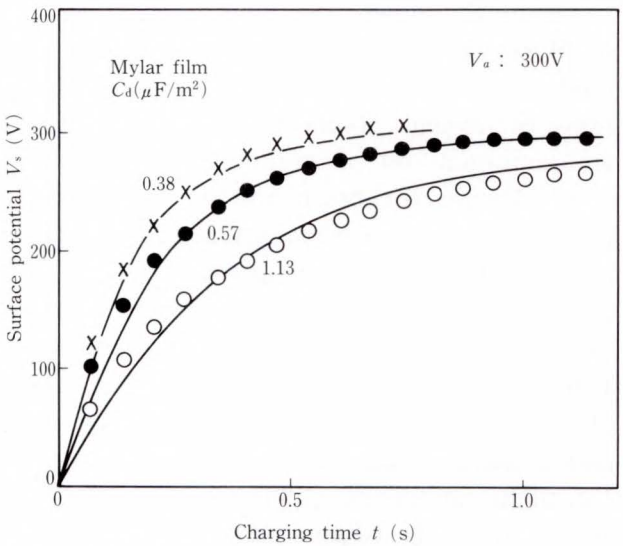

Fig. 6—Surface potential as a function of charging time.

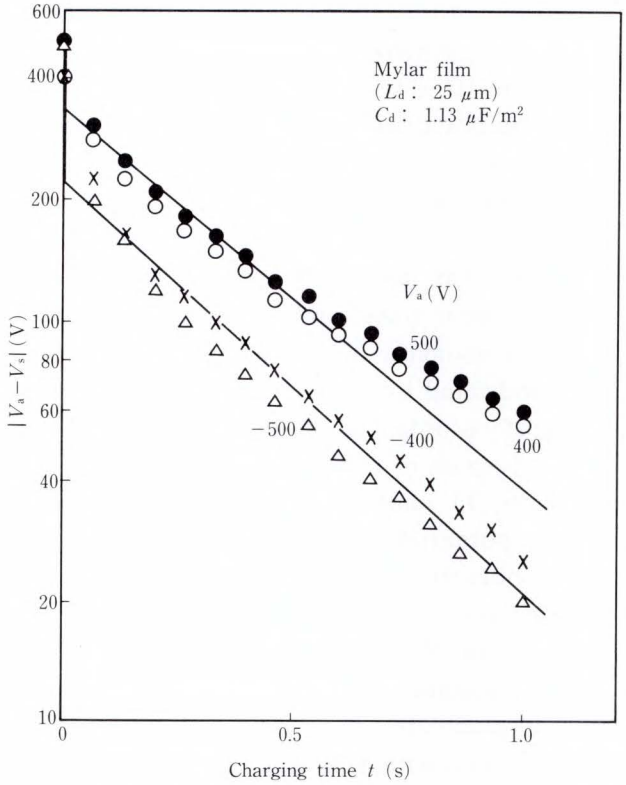

Fig. 7—Relationship between $V_a - V_s$ and charging time for gas discharge process.

Figure 6 shows the surface potential V_s as a function of the charging time for three different values of dielectric C_d when the brush potential V_a is 300 V. The solid lines indicate the results of computation when $R_c = 2.9 \times 10^5$; these results agree well with the experimental results when the charging time is longer than 0.3 seconds. However, the experimental data deviates from the solid line when the charging time is shorter than 0.3 seconds. This deviation seems to be caused by nonuniformity of R_c. R_c is believed to be influenced by the electric field (increasing with a decreasing electric field).

4.3 Charge transfer by gas discharge

Figure 7 shows the relationship between the absolute value of $V_a - V_s$ and the charging time when the Mylar film is 25 μm thick (C_d = 1.13 μF/m^2). The potential applied to the brush is high enough to cause gas discharge. The plots for the same polarity of V_a are almost the same, and their slopes are the same as the slopes of the direct charge transfer plots

Table 1. Extinction voltage

Mylar thickness (μm)	Extinction voltage: V_{ex} (V)	
	V_a: Positive	V_a: Negative
25	350	-220
50	395	-263
75	430	-277

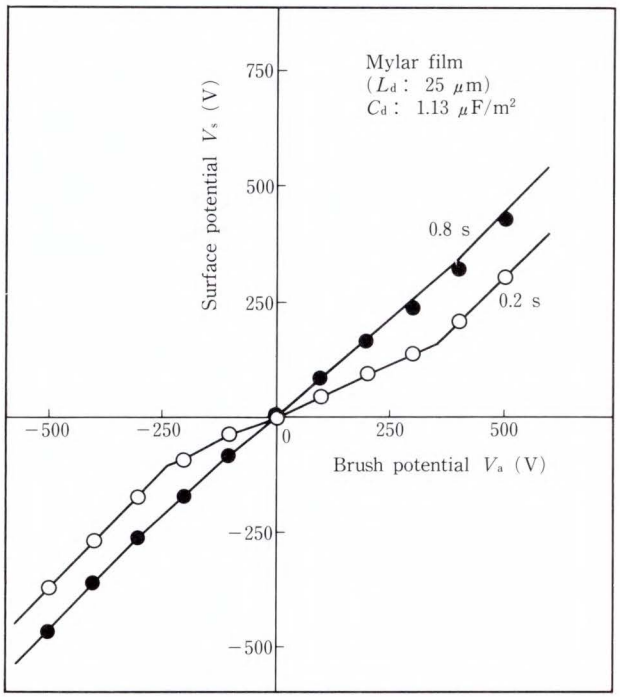

Fig. 8—Relationship between surface potential and brush potential.

shown in Fig. 5. As soon as V_a is applied, gas discharge occurs and charge is deposited on the Maylar film. At the beginning of the charging process (t = 0), $V_a - V_s$ rapidly decreases to the extinction voltage U_{ex}. Figure 7 shows that V_{ex} = 350 V for a positive brush potential, and V_{ex} = −220 V for a negative brush potential. Since the amount of electron emission with a negative brush potential is greater than that with positive brush potential, V_{ex} for a negative V_a is lower than that for a positive V_a. From further experiments, V_{ex} for Mylar films 50-μm and 75-μm thick were obtained (see Table 1).

Figure 8 shows the relationship between the surface potential and the brush potential for two different charging times as calculated from Equations (7) and (10) . The figure shows that

for a charging time of 0.8 seconds, the two potentials are nearly the same at all points and the plot is an almost straight line. For a charging time of 0.2 seconds the potential difference is much greater and the plot has three distinct stages. These results agree well with the experimental results. The equations can be used to determine the surface potential V_s for a given V_a, C_d, and charging time.

4.4 Charging of photoreceptor[8)]

A bar brush (see Fig. 9) was used for an experiment in charging the photoreceptor. The bar brush is a simpler charging device than the conductive brush roll; however, charging with a bar brush tends to increase nonuniformity of charge potential.

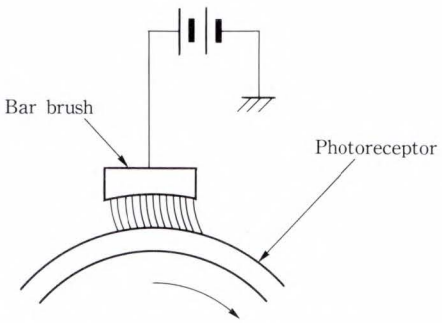

Fig. 9—Bar brush charger used to charge photoreceptor.

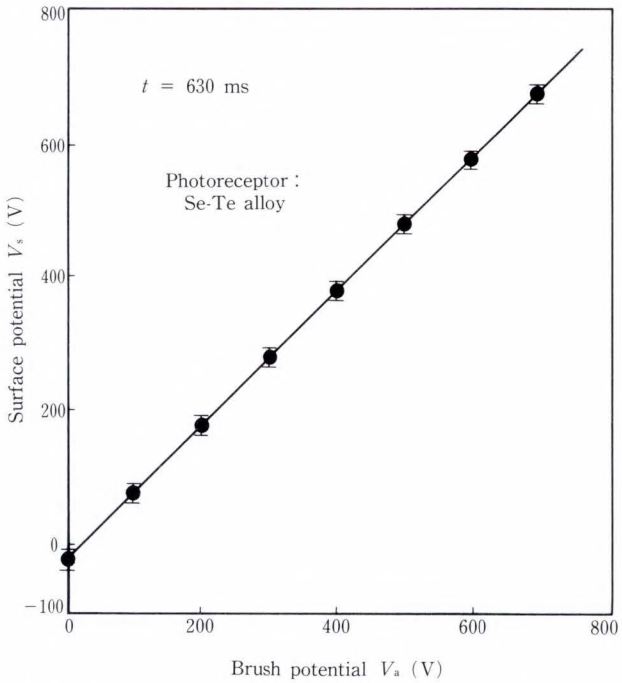

Fig. 10—Relationship between surface potential on selenium photoreceptor and brush potential.

Figure 10 shows the relationship between the brush potential V_a, and the surface potential on the Se-Te drum V_s in the saturated state. The relationship is linear, and V_a is nearly the same as V_s. The nonuniformity of charge potential was measured in the direction of photoreceptor travel and is represented as $\pm 3\sigma$ (σ is the standard deviation). The nonuniformity is indicated by the vertical bars in the graph. The surface potential V_s is slightly negative at $V_a = 0$ because of triboelectrification.

Figure 11 shows the relationship between surface potential and charging time when the brush potential V_a is fixed at 600 V. The charging time is controlled by changing the bar brush width. When the charging time is longer than 0.3 seconds, the surface potential V_s saturates to reach almost V_a. The nonuniformity in charging represented by $\pm 3\sigma$ is indicated by the vertical bars in the graph. Nonuniformity decreases with increasing charging time and becomes less than 50 V when the charging time exceeds 0.3 seconds. The nonuniformity in corona charging is almost 50 V; therefore, the brush charging method is suitable for electrophotography.

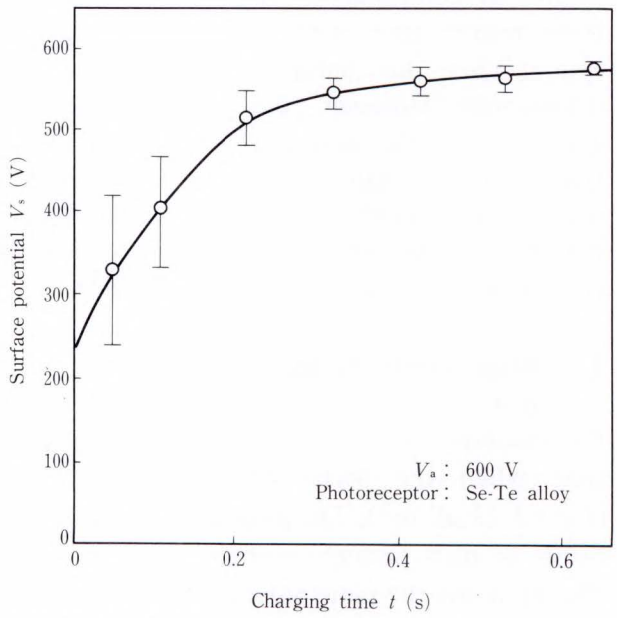

Fig. 11—Surface potential as a function of charging time for selenium photoreceptor.

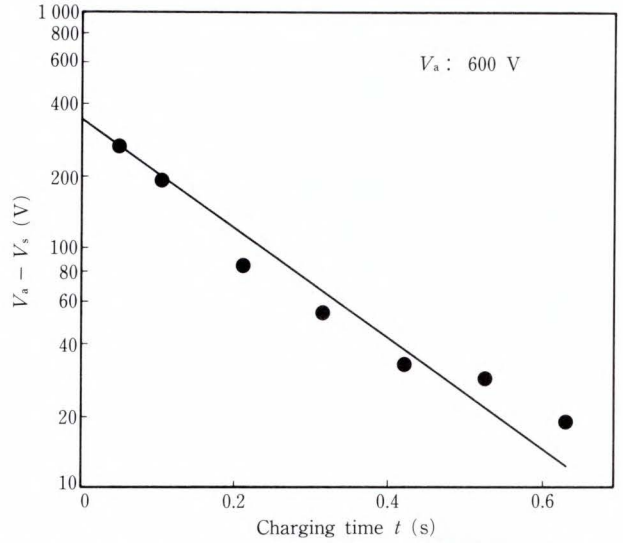

Fig. 12—Relationship between $V_a - V_s$ and charging time for selenium photoreceptor.

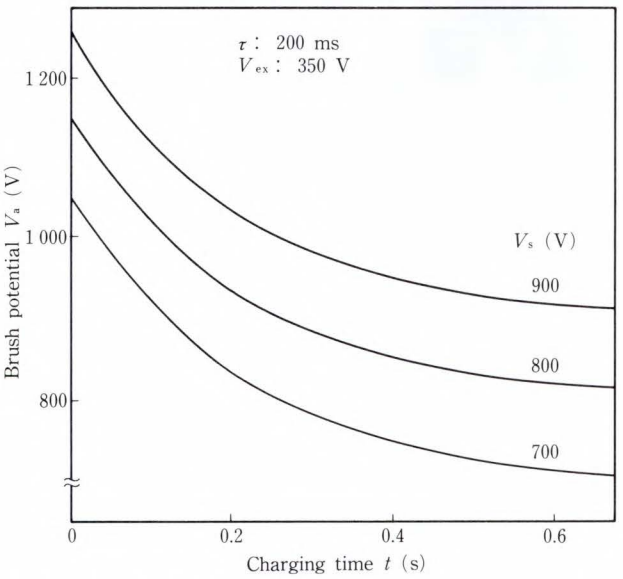

Fig. 13—Relationship between brush potential and charging time for selenium photoreceptor.

Figure 12 shows the relationship between the charging time and $V_a - V_s$ as calculated from the relationship shown in Fig. 11. Air breakdown occurs when the brush potential reaches 600 V. Therefore, Equation (10) applies to the charging process. The extinction voltage of gas discharge V_{ex} is obtained from the intercept of the vertical axis of the graph and is 350 V. The time constant of charging, $\tau = R_c (C_c + C_d)$, is obtained from the slope of the line and is 200 ms.

Figure 13 shows the relationship between the charging time and brush potential. This figure can be used to determine the required surface potential on the Se-Te drum for electrophotographic recording. The graph was drawn using Equation (10) with $\tau = 200$ ms and $V_{ex} = 350$ V (from Fig. 12). This graph can also be used to determine the brush potential V_a for given charging time and surface potential.

5. Conclusion

Studies on the charging process and characteristics of conductive fur brush charging led to the following conclusions:

A conductive fur brush can apply both positive and negative charges to a dielectric surface. The charged potential is nearly proportional to that of the brush.

Charge is deposited on the dielectric surface by three processes: triboelectric charging, direct charge transfer, and gas discharge.

The direct charge transfer process can be described using an ohmic model. The charged potential is a function of the brush potential, charging time, dielectric capacitance, contact capacitance, and contact resistance.

In the gas discharge process, the charged potential depends on the extinction voltage of gas discharge.

Nonuniformity of charged potential on a photoreceptor is less than 50 V when the charging time is longer than 0.3 seconds. The brush charging method is suitable for use in electrophotography.

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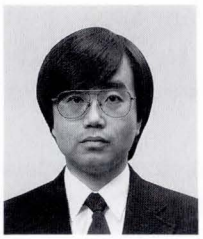

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Design of Organic Nonlinear Optical Materials for Electro-Optic and All-Optical Devices by Computer Simulation

• Tetsuzo Yoshimura

(Manuscript received September 6, 1990)

This paper investigates the use of organic materials for nonlinear optical devices as a means to providing a breakthrough in optical nonlinearities. For electro-optic devices, an improvement in second-order nonlinearity 10-100 times as large as that of $LiNbO_3$ is needed. For all-optical devices, an improvement in the third-order nonlinearity over 10 times as large as that of ordinary polydiacetylene (PDA) is required. To achieve these objectives, several organic materials were designed based on newly proposed guidelines requiring that the balance between wave function overlap and separation (or difference) be optimized. Computer simulations show that the objectives may be attainable by controlling the wave function and forming quantum wells through adjusting donor and acceptor substitution sites in one-dimensional conjugated systems.

1. Introduction

Nonlinear optical devices such as electro-optic (EO) devices, all-optical devices, and optical ICs consisting of these devices are important in optical communication, optical information processing, and other optical systems. However, practical nonlinear optical devices have not yet been fabricated due to a lack of nonlinear optical materials with high-performance.

Organic materials with conjugated systems have attracted interest because of their large optical nonlinearity[1)-5)]. This nonlinearity is expected to be superior to that of conventional inorganic materials such as $LiNbO_3$ (LN) and the multiple quantum wells (MQWs) of compound semiconductors. However, despite much work on organic materials, no notable improvements in optical nonlinearities have been made.

The author's motivation on this research is to make a break-through in the nonlinear optical properties of organic materials and to clarify the potential of the organic materials for EO and all-optical devices.

2. Nonlinear optical phenomena

Nonlinear optical phenomena can be understood using the spring analogy in Figs. 1a) to c)[6)]. In a spring, displacement x is proportional to external force F. With increasing F, the spring stretches rapidly with a nonlinear relationship between x and F. Nonlinear optical phenomena can be similarly described by replacing x with polarization P and F with electric field E. When E is small, P is proportional to E. With increasing E, the contribution of the E^2 or E^3 term becomes dominant. The E^2 and E^3 terms induce second-order and third-order nonlinear optical effects (see Table 1). The Pockels effect, in which the refractive index changes linearly with an applied electric field, is a second-order nonlinear effect and is used by EO devices. The optical Kerr effect, in which the refractive

index changes linearly with incident light intensity, is a third-order nonlinear effect and is used by all-optical devices.

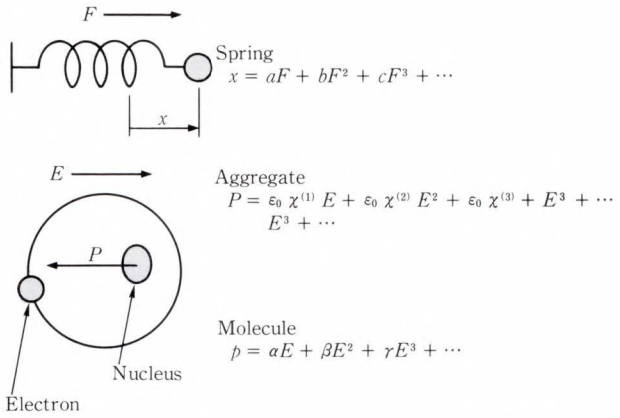
Measures of second- and third-order optical nonlinearities for a molecule are given by molecular second- and third-order nonlinear susceptibilities β and γ. For aggregates of many molecules, macroscopic second- and third-order optical nonlinearities can be given by second- and third-order nonlinear susceptibilities $\chi^{(2)}$ and $\chi^{(3)}$. When the intermolecular interaction is weak, $\chi^{(2)}$ is approximately the sum of βs of molecules in a unit volume[7]. Similarly, $\chi^{(3)}$ is the sum of γs. Electro-optic coefficient r, which is proportional to $\chi^{(2)}$, is usually used as the measure for Pockels effect.

The relationship between E and P can be translated into the electronic potential energy vs. polarization curve {see Fig. 1b) and c)}. When E and P are linearly related, the potential energy curve is parabolic. This corresponds to the fact that the potential energy of a spring is proportional to x^2. When nonlinear terms predominate, the potential energy curve deviates from the parabola.

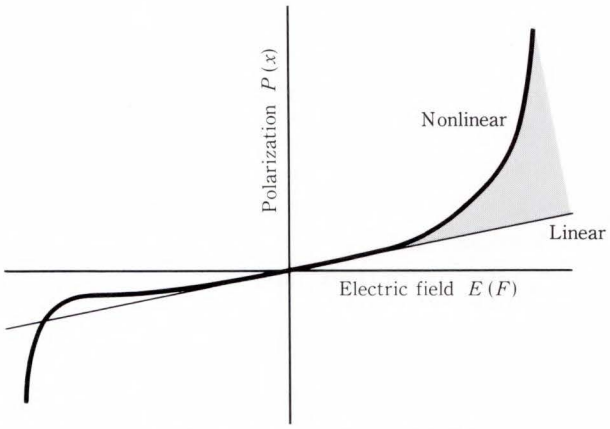
In general, the potential curve deviation becomes large in highly polarizable systems. Figure 2 illustrates electron-cloud polarizations induced by an electric field. In dielectric materials such as LN, electronic polarization is not large because electrons are localized near atoms, regarded as a strong spring. In semiconductors, electron clouds are widely spread, regarded as a weak spring. Therefore, compared to dielectric materials, large electronic polarization is attainable. Organic materials, especially long-chain molecules, have electrons delocalized one-dimensionally, i.e. they are regarded as natural quantum wires. The one-dimensional characteristics lead to effcient electronic polarization induced by an electric field along the direction of the chain. This is why the organic materials seem promising for nonlinear optical devices.

Table 1. Nonlinear optical phenomena for EO and all-optical devices

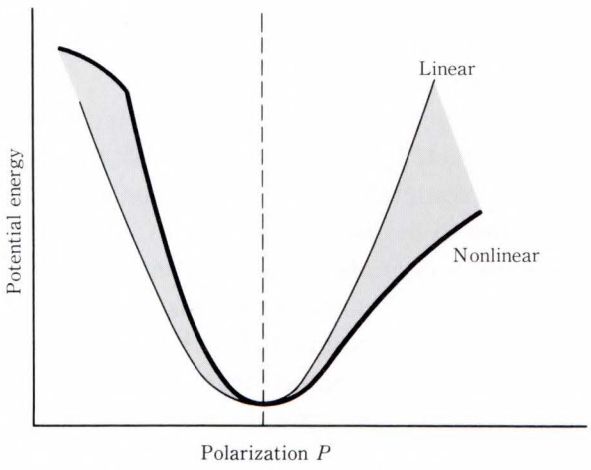
Order		Effect	Devices	Measure
Second	E^2	Pockels	EO	$\beta\ \chi^{(2)}\ r$
Third	E^3	Optical Kerr	All-optical	$\gamma\ \chi^{(3)}$



a) Spring analogy of nonlinear optical phenomena



b) Polarization vs. electric field



c) Potential energy vs. polarization

Fig. 1—Nonlinear optical phenomena.

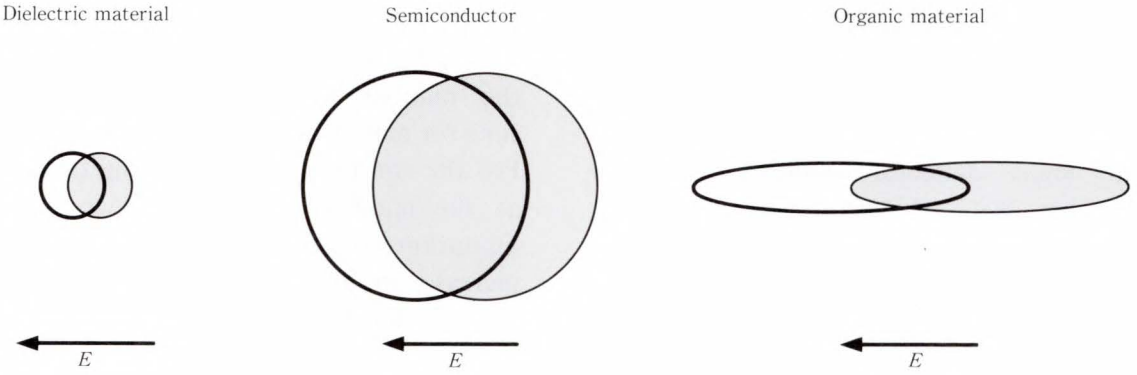


Fig. 2—Why organic materials are promising.

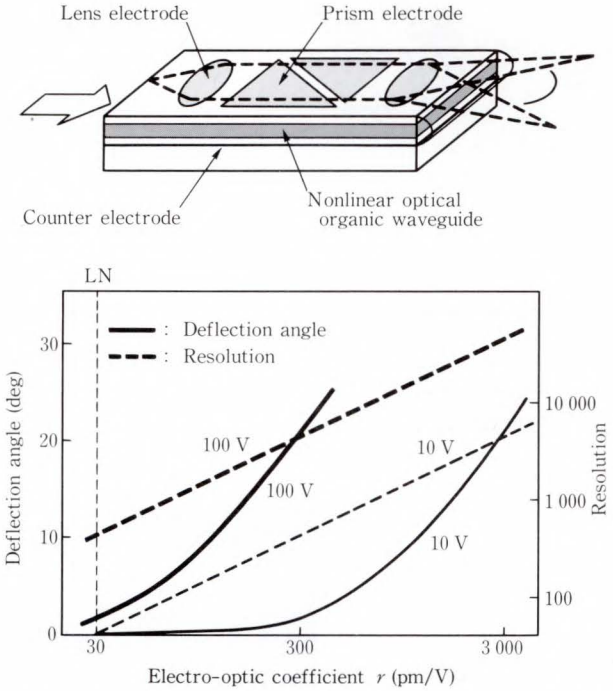


Fig. 3—Integrated optical waveguide deflector, and the calculated dependence of the deflection angle and resolution on electro-optic coefficient r. The prism electrode is 8 mm long and 5 mm wide, and the gap between prism and counter electrodes is 5 μm.

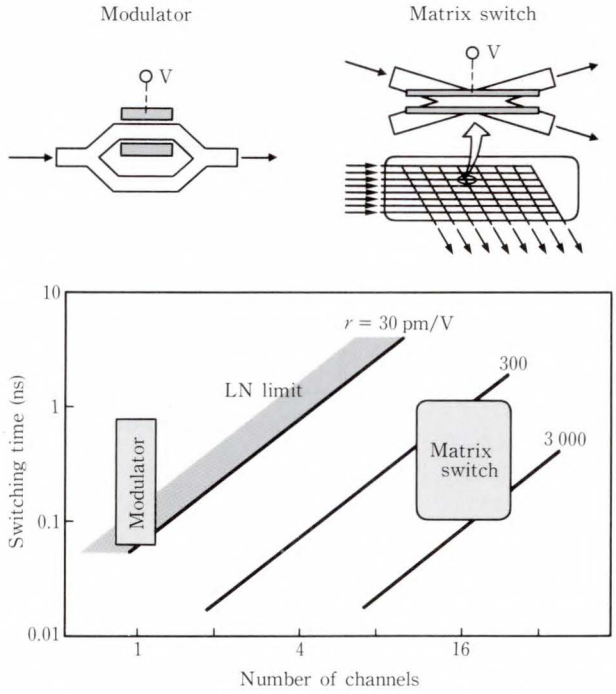


Fig. 4—Matrix optical switches and modulators, and correlation between the number of channels and switching time.

3. State-of-the-art nonlinear optical materials and their objective

3.1 EO device materials

Figures 3 and 4 show typical EO devices. Our goal is to have devices widely used in optical systems. At present, most EO devices are fabricated using LN. Because the optical nonlinearity of LN is insufficient, except for the optical modulator, current device characteristics do not come close to accomplishing the objective.

Figure 3 gives an example of the integrated optical waveguide deflector proposed in this paper. The deflector consists of a nonlinear optical organic waveguide 5 μm thick inserted between the counter and prism electrodes 8 mm long and 5 mm wide. By controlling the voltage applied to the prism electrodes, we can induce waveguide prisms with a variable refractive index. It is then possible to scan the light beam in the waveguide. The calculated dependence of the deflection angle and re-

solution on the electro-optic coefficient r is shown in Fig. 3. When r is about 30 pm/V, which equals the r of LN, the deflection angle is only a few degrees even when 100 V is applied. Many deflector applications require a deflection angle of several tens of degrees, however, and resolution of more than thousands of points. To attain the objective, a material with an r of about 300 pm/V to 3 000 pm/V, i.e. 10 times to 100 times that of LN, is required.

Figure 4 shows the correlation between the number of channels and the switching time for matrix optical switches and modulators. For the constant r, the switching time increases as the number of channels increases due to limitations on the speed of the circuitry. An increase in the number of channels causes the individual constituent switch to be small,

Electro-optic materials	$LiNbO_3$	Pendant-attached polymer	Molecular crystal	Conjugated polymer
r (pm/V)	30	50	430	?
Processability	Commercially available	Very good	Poor	Good
Development phase		Device fabrication	Material preparation	Material design

Fig. 5—Second-order nonlinear optical materials for EO devices[8].

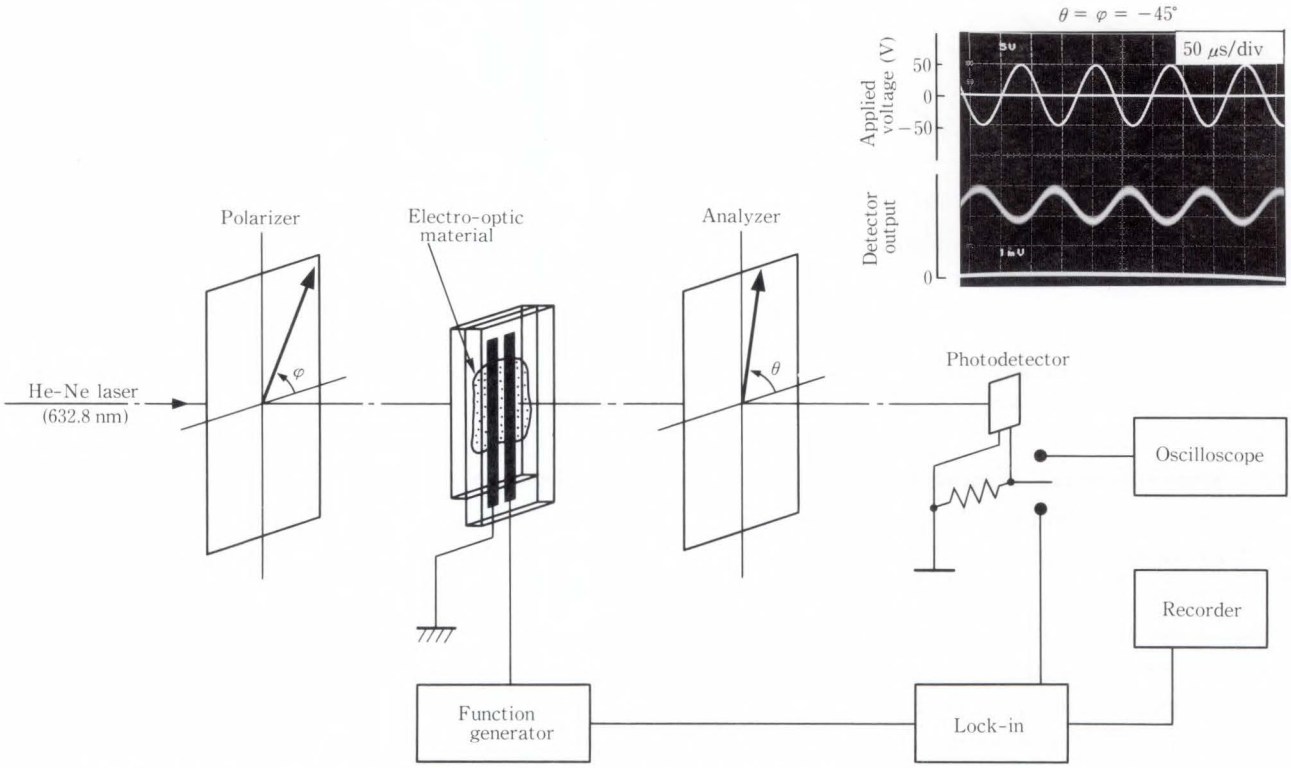


Fig. 6—Measurement system for AC modulation method and the typical light modulation signal for SPCD thin-film crystal.

resulting in an increase in the drive voltage, which slows the circuit speed. The LN limit is roughly determined in reference to the present circuit performance and a wafer several inches in diameter. Dynamic optical interconnections for broadband optical communications may require matrix optical switches with more than 16 channels operating at a bit rate exceeding 10 GHz. Thus, to reach the objective for matrix optical switches, an r 10 times to 100 times as large as that of LN is required.

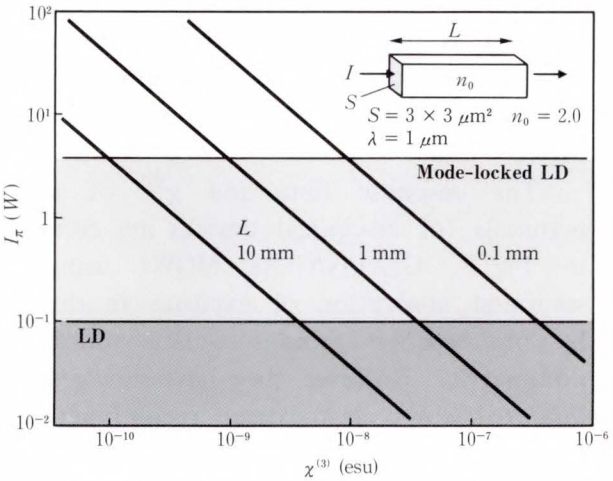
The electro-optic coefficients of EO materials are compared in Fig. 5[8]. Organic materials can be classified into pendant-attached polymers, molecular crystals, and conjugated polymers. For molecular crystals, in the initial period of research, the author developed crystal-growth techniques for styrylpyridinium cyanine dye (SPCD) and 2-methyl-4-nitroaniline (MNA). The purpose was to study the Pockels effects in demonstrating the usefulness of organic materials as EO materials[9)-11)]. In 1987, using the AC modulation method (see Fig. 6), the author found the SPCD thin-film crystal had an r of 430 pm/V, about 14 times that of LN[9]. To the author's knowledge, this is the largest value ever observed in an organic material. The results demonstrated the possible use of organic materials in EO devices. Since 1987, however, despite the promising molecular crystal MNBA (4'-nitrobenzylidene-3-acetamino-4-methoxyaniline)[12] developed by Toray, no molecular crystals have exceeded 430 pm/V. This suggests that the limit of r in ordinary molecular crystals is about ten times r (LN). For the pendant-attached polymers[13)-16)], r is smaller than that for molecular crystals at present. However they can be easily formed by spin-coating into thin films of high optical quality. In principle, by improving the molecular alignment, it may be possible to achieve an r of the same level as that of the molecuar crystals, that is, ten times r (LN).

As mentioned above, the electro-optic coefficient of about 10 times r (LN), which is the lower limit of the proposal, seems possible using the molecular crystals and pendant-attached polymers. Device fabrication using these materials is one approach. However, to further improve the Pockels effect, another material, conjugated polymers like polydiacetylene (PDA), should be selected. PDA is regarded as a natural one-dimensional system (quantum wire), more favorable to inducing a larger oscillator strength[17] than two- or three-dimensional systems. It has long variable wave functions offering a greatly enhanced Pockels effect.

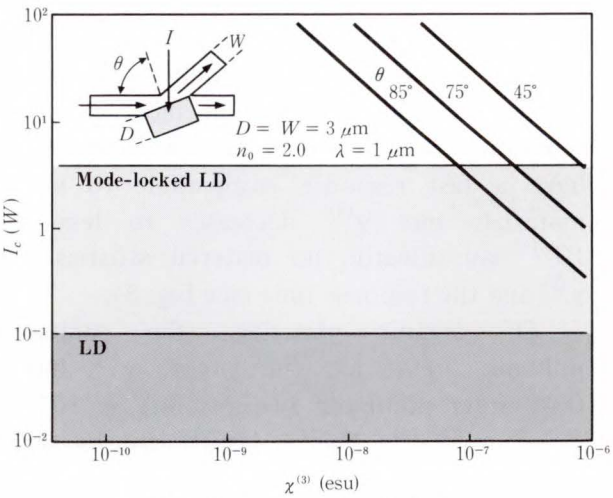
3.2 All-optical device materials

Figures 7a) and b) show the correlation between $\chi^{(3)}$ and light powers I_π and I_c required to operate of all-optical devices.

Here, I_π and I_c are given by



a) Bistable optical devices and all-optical phase modulators



b) Nonlinear interface devices

Fig. 7—Correlations between $\chi^{(3)}$ and the light power required for device operation.

$$I_\pi = (3000/32\pi^2)S\lambda n_0^2/(L\chi^{(3)}),$$
$$I_c = (3000/16\pi^2)(1-\sin\theta)DWn_0^2/(\chi^{(3)}\cos\theta).$$

S is the waveguide cross-sectional area, λ the wavelength of incident light in a vacuum, n_0 the refractive index in the dark, L the light path length, θ the incident angle of propagating light in the waveguide, and $D \times W$ the area exposed by controlling the light. Sizes are given in centimeters and $\chi^{(3)}$ is in esu. The advantage of all-optical systems is high speed, e.g. a response time of less than 10 ps. Therefore the light path length in the device must be less than about 0.15 mm because the light propagating speed, c/n_0, is 0.15 mm/10 ps in a medium when n_0 equals 2. Assuming operations with laser diodes (LDs) or mode-locked LDs, bistable optical devices and optical phase modulators need $\chi^{(3)}$ exceeding 10^{-8} esu. Nonlinear interface devices require $\chi^{(3)}$ exceeding 10^{-7} esu.

The response time and $\chi^{(3)}$ of typical materials for all-optical devices are compared in Fig. 8. GaAlAs/GaAs MQWs using the saturated absorption of excitons in shielding by photocarriers exhibit a large third-order nonlinearity. However, they have slow response due to slow photocarrier recombination[18]. In contrast, organic materials have a fast response of a few picoseconds or less, but a small $\chi^{(3)}$. Semiconductor-doped glasses show a property in between GaAlAs/GaAs MQWs and organic materials. Note that $\chi^{(3)}$ and the response time are extremely sensitive to resonant conditions[19),20]. In fact, in an off-resonant condition, the GaAlAs/GaAs MQWs have a fast response comparable to organic materials but $\chi^{(3)}$ decreases to less than 10^{-10} esu. Clearly, no material satisfies both $\chi^{(3)}$ and the response time (see Fig. 8).

Of organic materials, the conjugated polymer, PDA, has the largest $\chi^{(3)}$, but its third-order nonlinear susceptibility is 10^{-9} to 10^{-10} esu[21)-23)]. This is insufficient by several orders of magnitude for practical application to all-optical devices operating with LDs. Thus, for the optical Kerr effect, an improvement of at least ten times is necessary.

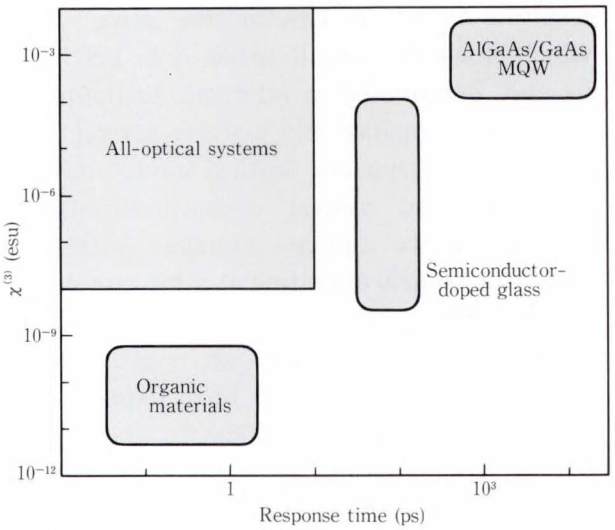


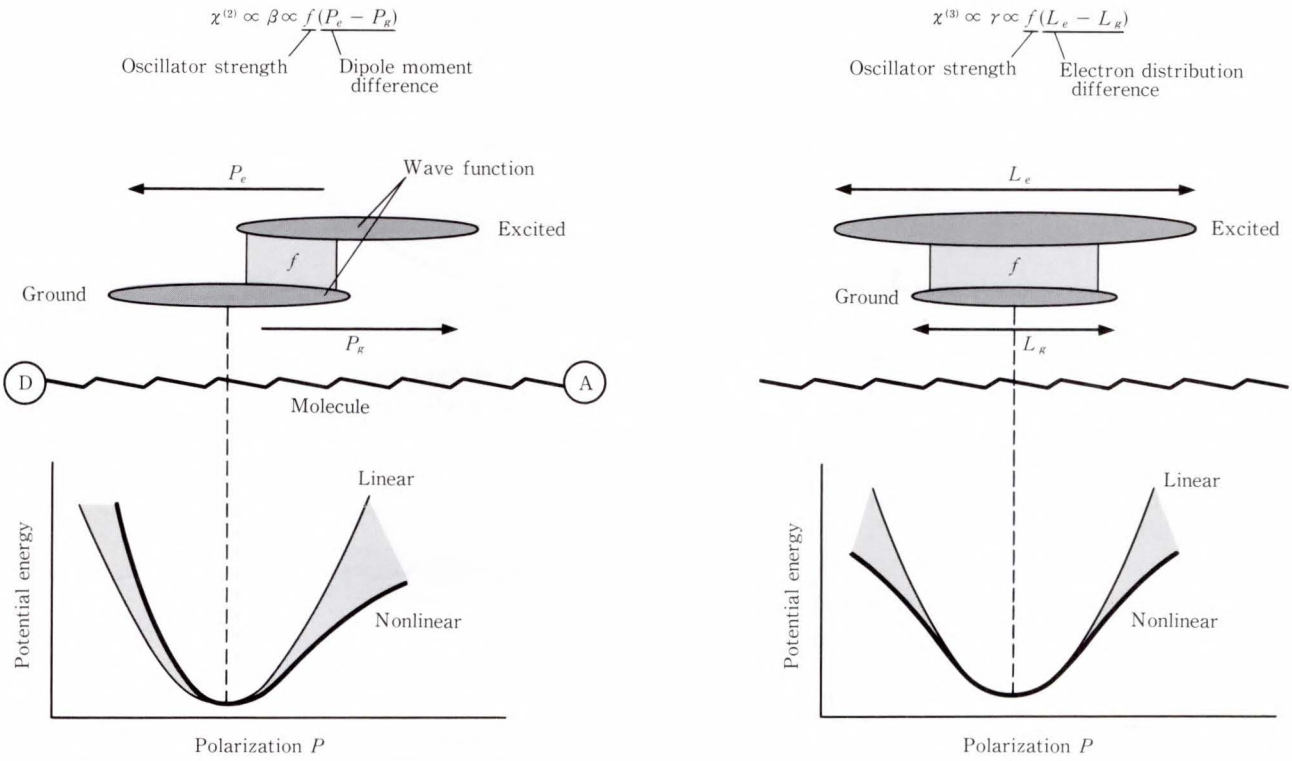
Fig. 8—Third-order nonlinear optical materials for all-optical devices.

From sections 3.1 and 3.2, the author concluded that the work should focus on improving second- and third-order nonlinear optical properties 10 times to 100 times using one-dimensional conjugated systems.

4. Qualitative guidelines for improving optical nonlinearities

Figure 9 shows the microscopic origins[6),24)] of second- and third-order optical nonlinearities. As mentioned in chapter 2, the potential energy curve for linear systems is parabolic. In nonlinear systems, however, it is not. This induces a variety of nonlinear phenomena. To induce second-order nonlinearity, the potential curve deviation must be asymmetric {see Fig. 9a)}. For third-order nonlinearity, symmetry does not matter {see Fig. 9b)}. The larger the potential curve deviation from the parabola, the larger the induced nonlinear optical effects.

The driving force for this potential curve deformation is explained in terms of the shape of the wave function {see Figs. 9a) and b)}. Here, consider the ground state and one excited state, that is, a two-level model, for simplicity. Introducing a perturbation of incident light or applied voltage to a molecule induces mixing the excited and ground state wave functions, deforming the potential curve. Therefore,



a) Second-order b) Third-order

Fig. 9—Microscopic origins for second- and third-order optical nonlinearities.

the first approach to improving optical nonlinearity lies in promoting the mixing rate of ground and excited states, i.e. promoting the oscillator strength f between the ground and excited states. Here, $f \propto <e \mid r \mid g>^2$, which can be increased by promoting the wave function overlap between the ground and excited states. However, only increasing the wave function mixing rate is not in itself sufficient to increase the potential curve deformation. For example, when the ground and excited state wave functions have a similar shape, mixing the wave function results only in a small change in electron distribution. Consequently, there is only a small potential curve deformation. Another approach to improving optical nonlinearity is promoting the wave function difference between the ground and excited states.

The following guidelines were derived:

Second-order nonlinearity

1) Promote wave function overlap between the ground and excited states, increasing oscillator strength $f \propto <e \mid r \mid g>^2$.
2) Promote wave function separation between the ground and excited states, increasing dipole moment difference $P_e - P_g$, where $P_e = <e \mid r \mid e>$ and $P_g = <g \mid r \mid g>$.

Second-order nonlinearity would then be proportional to the product of f and $P_e - P_g$, consistent with the two-level model expression for molecular second-order nonlinear susceptibility,

$$\beta \propto f(P_e - P_g). \quad \ldots\ldots\ldots\ldots (1)$$

Third-order nonlinearity

1) Promote wave function overlap between the ground and excited states, increasing the oscillator strength $f \propto <e \mid r \mid g>^2$.
2) Promote wave function differences between the ground and excited states, increasing $L_e - L_g$ where L_e and L_g are measures of wave function distribution.

Third-order nonlinearity would then be proportional to the product of f and $L_e - L_g$. As shown in Fig. 10, considering one excited state, $\mid e>$, which has a major transition matrix element with the ground state $\mid g>$ and neglect-

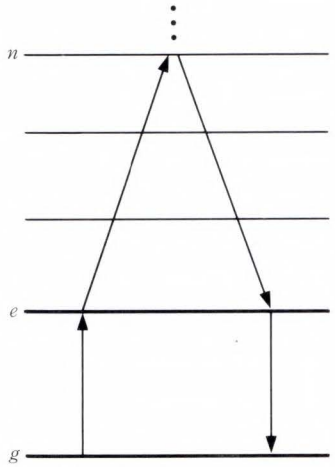


Fig. 10—Ground g and excited e states. e has a large transition matrix element with the ground state. n is the other excited state.

ing the energy denominator, molecular third-order nonlinear susceptibility is roughly expressed as

$$\gamma \propto \sum_{n} <g \mid r \mid e><e \mid r \mid n><n \mid r \mid e> <e \mid r \mid g>$$

$$\approx <g \mid r \mid e><e \mid r^2 \mid e><e \mid r \mid g>.$$

Then, assuming, $<e \mid r^2 \mid e> \propto L_e - L_g$, the difference in expected values of r^2 between ground and excited states, on the analogy of $P_e - P_g$ in β, we obtain

$$\gamma \propto f(L_e - L_g). \quad \ldots\ldots\ldots (2)$$

This is consistent with our qualitative guidelines.

For both second- and third-order nonlinearity, however, note that f and $P_e - P_g$, or f and $L_e - L_g$ are not independent, but are a tradeoff. It is concluded that the balance of the wave function overlap and wave function separation (or difference) must be considered simultaneously in optimizing nonlinear optical effects.

5. Simulation of optical nonlinearity in newly designed organic materials

Given the guidelines in chapter 4, the author designed several molecules with PDA structures, and simulated second- and third-order optical nonlinearities.

5.1 EO device materials[25)-27)]

Figure 11 shows three wave function shapes.

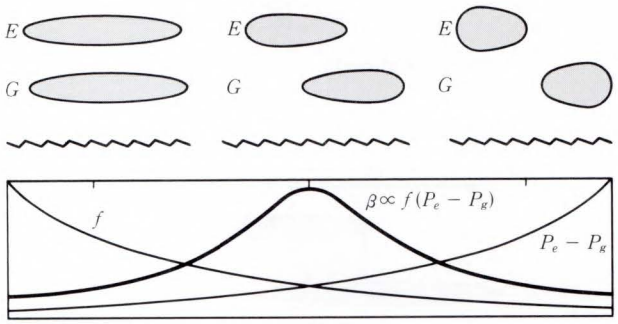


Fig. 11—Relationship between second-order optical nonlinearity and wave function separation.

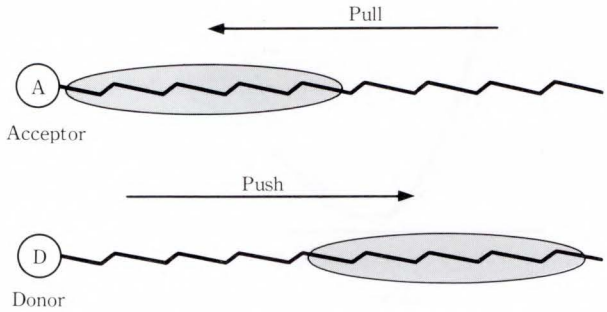


Fig. 12—Push- and pull-effects of donor (D) and acceptor (A). Donors push electrons and acceptors pull electrons when excited by light.

Wave function separation between the excited and ground states increases from left to right and wave function overlap between the two states decreases, i.e. $P_e - P_g$ increases and f decreases in a tradeoff. β is expected to have its maximum in an intermediate wave function condition as suggested in chapter 4. To obtain such a wave function shape, the author tried controlling the wave function by adjusting the donor and acceptor substitution sites, as well as the molecular chain length, using push- and pull-effects of donors and acceptors (see Fig. 12).

Figure 13 shows the new molecules, designed by Fujitsu's Assistance of New Chemistry for Original Research (ANCHOR)[28)]. These molecules have a PDA structure and an acetylenic backbone. NH_2 is the donor (D) and NO_2 the acceptor (A). DA, DAAD, and DDAA are types of donor and acceptor substitution, and the numbers following them indicate

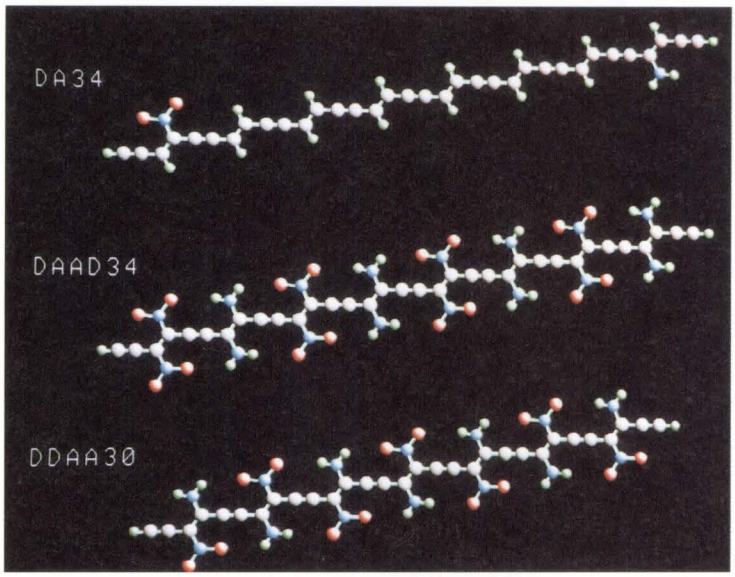


Fig. 13—New molecules designed by ANCHOR. White balls are carbon atoms, blue balls are nitrogen atoms, red balls are oxygen atoms and green balls are hydrogen atoms.

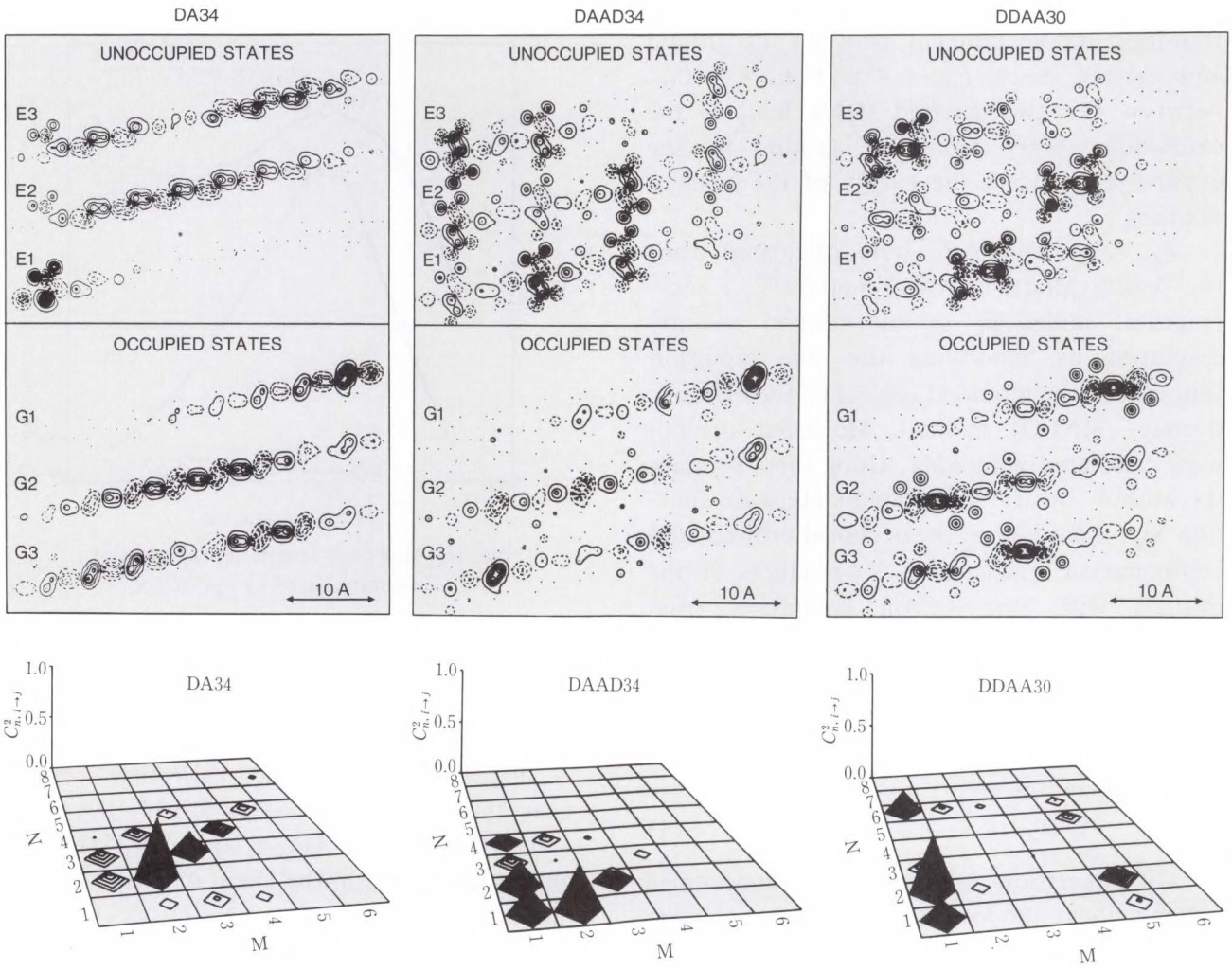


Fig. 14—Contour diagrams of molecular orbitals near the Fermi surface in plane z-0.6 Å (0.06 nm) and $C^2_{n,i\to j}$ for the first excited states. G denotes occupied orbitals and E unoccupied orbitals. G1 is HOMO and E1 is LUMO. M denotes the occupied molecular orbitals GM (M = 1,2, ..., 6) and N unoccupied molecular orbitals EN (N = 1, 2, ..., 8). The height of the pyramid indicates C_n, $GM \to EN^2$.

the number of carbon sites (N_c) in the conjugated chain.

β for the Pockels effect corresponding to the chain direction is calculated based on Ward's expression[29],

$$\beta = -\frac{e^3}{2\hbar^2}\left\{\sum_{\substack{g\neq n'\\ n\neq g\\ n\neq n'}} P_{gn'}P_{n'n}P_{ng} \times \right.$$

$$\times \frac{3\omega_{n'g}\omega_{ng}+\omega^2}{(\omega_{n'g}^2-\omega^2)(\omega_{ng}^2-\omega^2)} +$$

$$\left. + \sum_n P_{gn}^2 \Delta P_n \frac{3\omega_{ng}^2+\omega^2}{(\omega_{ng}^2-\omega^2)^2}\right\}. \quad \ldots (3)$$

Here, $\Delta P_n = P_n - P_g, P_{gn} = <g \mid r \mid n>$ is the transition dipole moment between the ground and excited states. $P_{nn'} = <n \mid r \mid n'>$ is that between the two excited states. $\hbar\omega_{ng}$ is the excitation energy from the ground to the excited state. $\hbar\omega$ is the energy of the incident photons.

P_{gn}, $P_{nn'}$ and ΔP_n were calculated using the Austin Model 1 (AM1) method[30], a semi-empirical molecular orbital method recently developed by modifying the core repulsion function in the modified neglect of the diatomic overlap (MNDO) method. Molecular orbitals were calculated with AM1. Using these orbitals, the author constructed ground state wave function Ψ_g, a product of the occupied orbitals, and configuration functions $\chi_{i\to j}$, products of the orbitals with one-electron excitation from occupied orbital i to unoccupied orbital j. Excited states Ψ_n, expressed as linear combinations of configuration functions, Equation (4), were determined by single-excitation configuration interaction (SCI)[31].

$$\Psi_n = \sum_{i,j} C_{n,i\to j}\chi_{i\to j} . \quad \ldots\ldots\ldots\ldots (4)$$

CI calculation involved eight unoccupied orbitals above the lowest unoccupied molecular orbital (LUMO) and six occupied orbitals below the highest occupied molecular orbital (HOMO). Using Ψ_g and Ψ_n, P_{gn}, $P_{nn'}$ and ΔP_n were calculated.

MNA was used as the standard molecule.

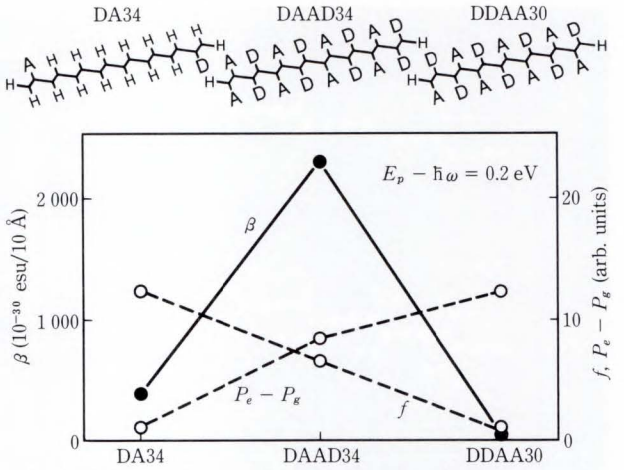


Fig. 15—β, P_e - P_g, and f of DA34, DAAD34, and DDAA30.
β is normalized by the molecular length. E_p is the exicitation energy for the first excited state.

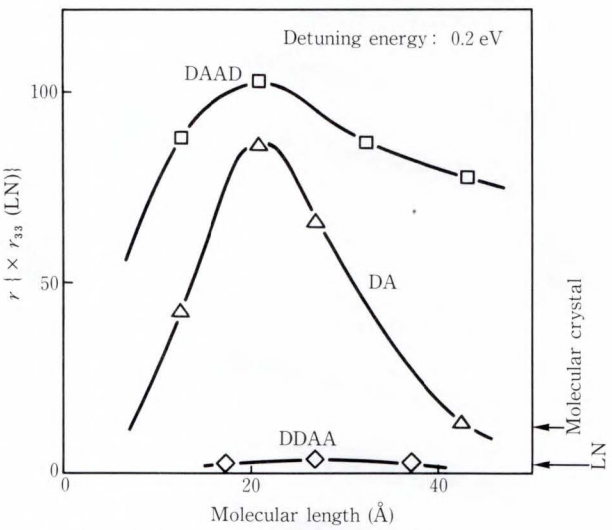


Fig. 16—Molecular length dependences of r.
r is normalized by r_{33} of LN.

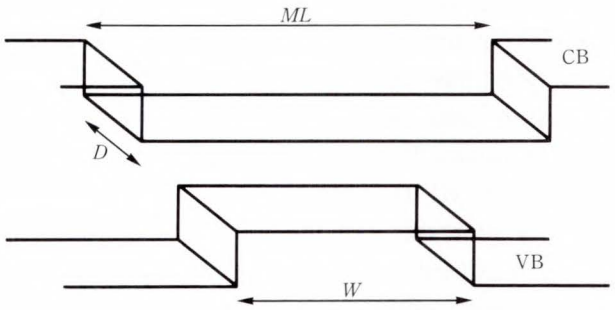
From the calculation, $\beta = 13 \times 10^{-30}$ esu at 1.06 μm. This agrees fairly well with the 12×10^{-30} esu reported by Garito et al[32].

Figure 14 shows the molecular orbitals near the Fermi surface for DA34, DAAD34, and DDAA30. In DA34 and DAAD34, the charge separation in the chain direction appears mainly in the HOMO and LUMO. In other molecular orbitals, electrons in molecules tend to be delocalized. In DDAA30, however, as in LUMO, E2 and E3 orbitals also exhibit considerable charge separation. In Fig. 14, $C_{n,i\to j}^2$ for the first excited state is also shown.

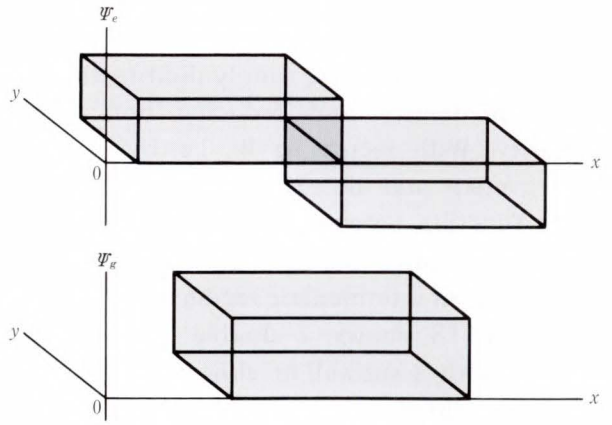
$C_{n,i\to j}$ represents the fraction of the configuration function involved in Ψ_n, Equation (4). Combining these results with shape of the molecular orbitals clarifies the wave function shape. In DA34, the G1 → E1 component, corresponding to the LUMO-to-HOMO transition, is extremely small. The wave function separation then becomes small corresponding to the wave function condition on the left side in Fig. 11. In DAAD34, finite G1 → EN and GM → E1 components appear, resulting in a considerable wave function separation corresponding to the condition in the center in Fig. 11. In DDAA30, G1 → EN components predominate and, furthermore, the EN orbital exhibits considerable charge separation, inducing the large wave function separation like on the right in Fig. 11. Wave function separations increase in the order of DA34, DAAD34, and DDAA30.

Figure 15 shows the calculated molecular second-order nonlinear susceptibilities per 10 Å (1 nm) of molecular length for DA34, DAAD34, and DDAA30. As expected, $P_e - P_g$ increases and f decreases in the order of DA34, DAAD34, and DDAA30. β becomes maximum in between for DAAD34. This parallels the tendency of the qualitative guideline (see Fig. 11), and indicates that the balance between $P_e - P_g$ and f is important in improving β.

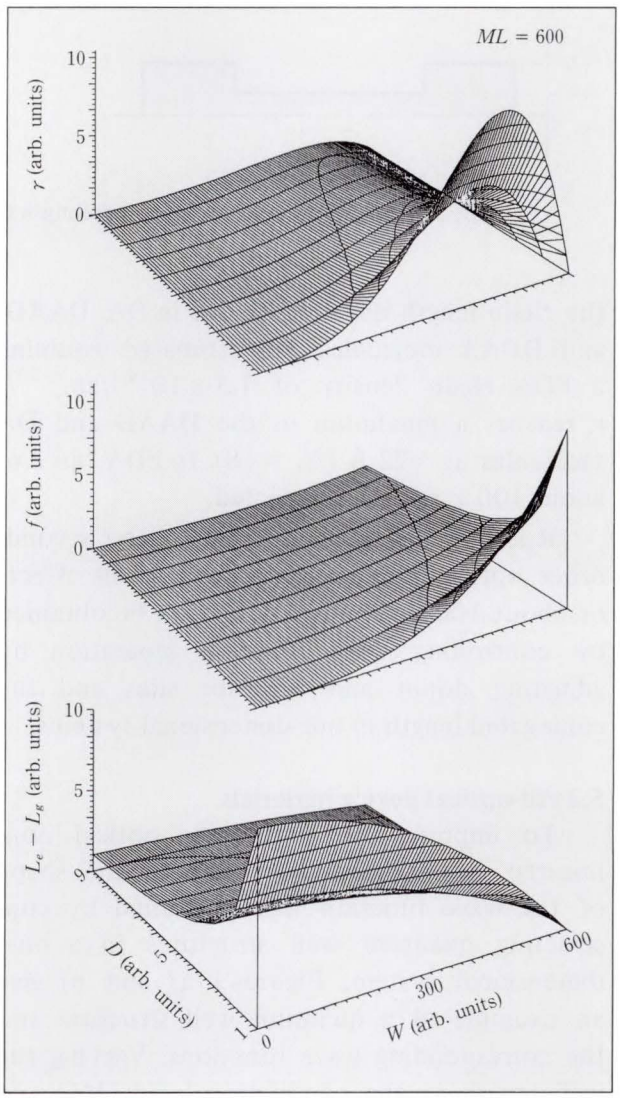
In addition, it was also found that the molecular length affects the wave function shape and that adjusting the length effectively improves nonlinear effects. Figure 16 shows



a) Example of quantum well structure

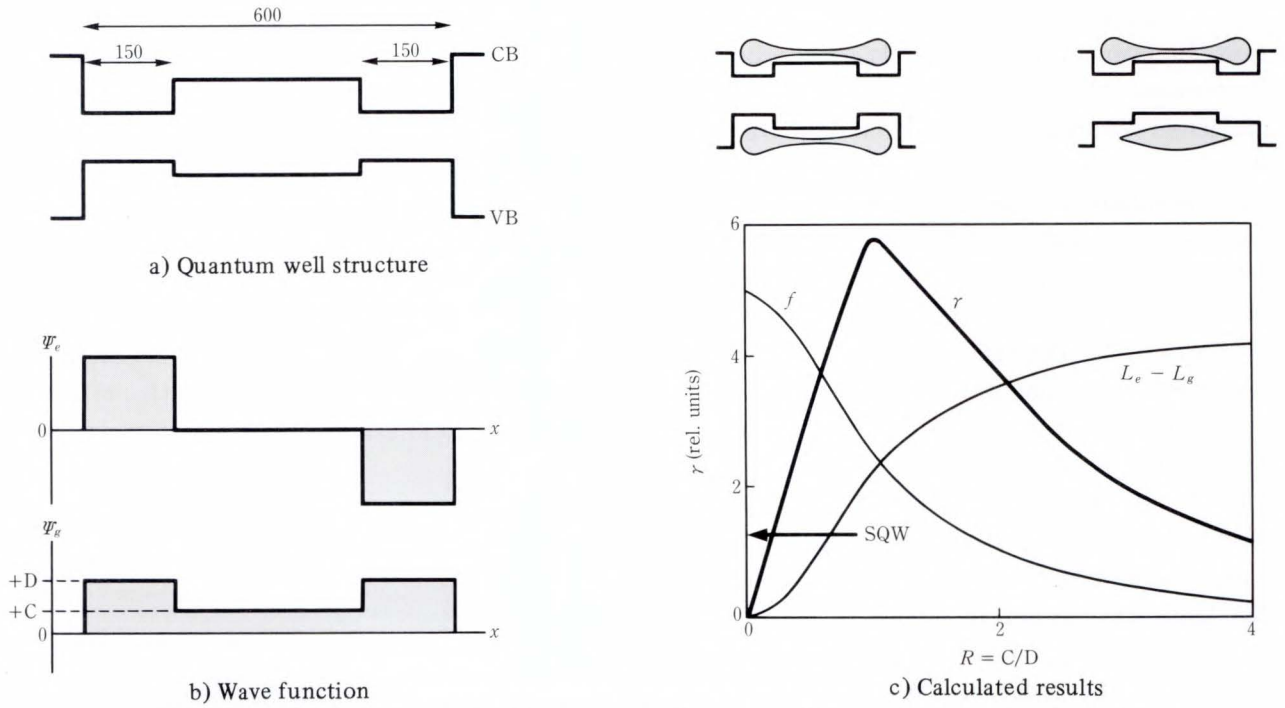


b) Corresponding wave function



c) γ, f and L_e - L_g

Fig. 17—Enhancement of γ by controlling wave function shapes with quantum well structure.



a) Quantum well structure

b) Wave function

c) Calculated results

Fig. 18—Enhancement of γ by controlling wave function shape with double quantum well structure.

the chain length dependence of r in DA, DAAD, and DDAA molecules. r is estimated assuming a PDA chain density of 1.3×10^{14} l/cm^2 [33]. r reaches a maximum in the DAAD and DA molecules at ~22 Å ($N_c = 18$). In PDA, an r of about $100 \times r$ (LN) is expected.

It is therefore concluded that a large second-order optical nonlinearity (the Pockels effect) of about 100 times that of LN can be obtained by controlling wave function separation by adjusting donor and acceptor sites and the conjugated length in one-dimensional systems.

5.2 All-optical device materials

To improve the third-order optical nonlinearty (the optical Kerr effect), the shape of the wave function was controlled by constructing quantum well structures in a one-dimensional system. Figures 17a) and b) give an example of a quantum well structure and the corresponding wave functions. Varying the well length in the conduction band (ML) and that in the valence band (W) adjusts the wave function difference between the ground and excited states. D is the well width. Reducing D changes the system from being two- to one-dimensional. γ per unit length for the light polarization with the well length direction was calculated from Equation (2). For simplicity, it was assumed that the ground state wave function has even parity, the excited wave function odd parity, and wave functions are square waves. The results are shown in Fig. 17c). With reduced D, both $L_e - L_g$ and f increase, then γ increases rapidly. This clearly indicates that the one-dimensional system is better than a two-dimensional system for introducing large optical nonlinearity (see chapter 2). That is, a wave function extent perpendicular to the direction of light polarization contributes little to optical nonlinearity, simply diluting the wave function density and reducing optical nonlinearity. With increasing W, i.e. by increasing the overlap and decreasing the difference in wave function between the ground and excited states, f increases and $L_e - L_g$ decreases, with γ peaking at an intermediate region in W.

Figure 18 shows a double quantum well (DQW) with a subwell at either side. The wave function difference is controlled by the difference in well depth between the conduction and valence bands. With increasing well depth,

the wave function tends to localize on either side. The calculated values of γ, $L_e - L_g$, and f are shown in Fig. 18c) as a function of $R = C/D$. R is a measurement of the wave function extent in the valence band as defined in Fig. 18b). With increasing R, $L_e - L_g$ increases and f decreases. γ peaks at an intermediate region in R of about 1 when the balance between the overlap and difference of wave functions is optimum. In this case, γ is improved about five times over that for a single quantum well (SQW). It was also found that further confinement of electrons in three or more subwells would make it possible to enhance γ more than ten times.

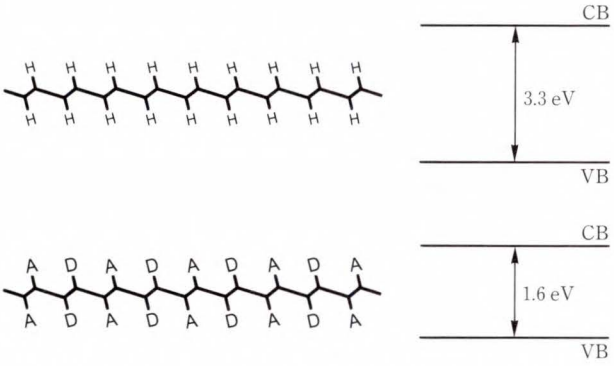


Fig. 19—Band gap control in PDA by donor and acceptor substitution.

5.3 Quantum well formation in PDA

To apply the materials in sections 5.1 and 5.2 to practical devices, it is necessary to fabricate the materials as a thin film. This involves constructing quantum well structures in one-dimensional PDA chains to make PDA thin-film crystals.

Recently, the author found from molecular orbital calculation that the energy gap of PDA can be reduced when donors and acceptors are substituted in the DAAD type[26] (see Fig. 19). Using this effect, the author expected to insert many DAAD molecules into the PDA chain, constructing a one-dimensional MQW (see Fig. 20)[8),34)]. This structure enables DAAD molecules to be aligned perfectly, which is favorable to attaining a large Pockels effect.

Using energy gap narrowing, it should be possible to form quantum wells in PDA by modulating the energy gap with selective substitutions of donors and acceptors into the PDA chain[24),34)]. The DQW with two wells 14 Å (1.4 nm) long designed by ANCHOR is shown in Fig. 21 together with an SQW. Quantum wells are formed in PDA with 38 carbon sites. Areas with donor and acceptor substitution are wells, and areas with hydrogen

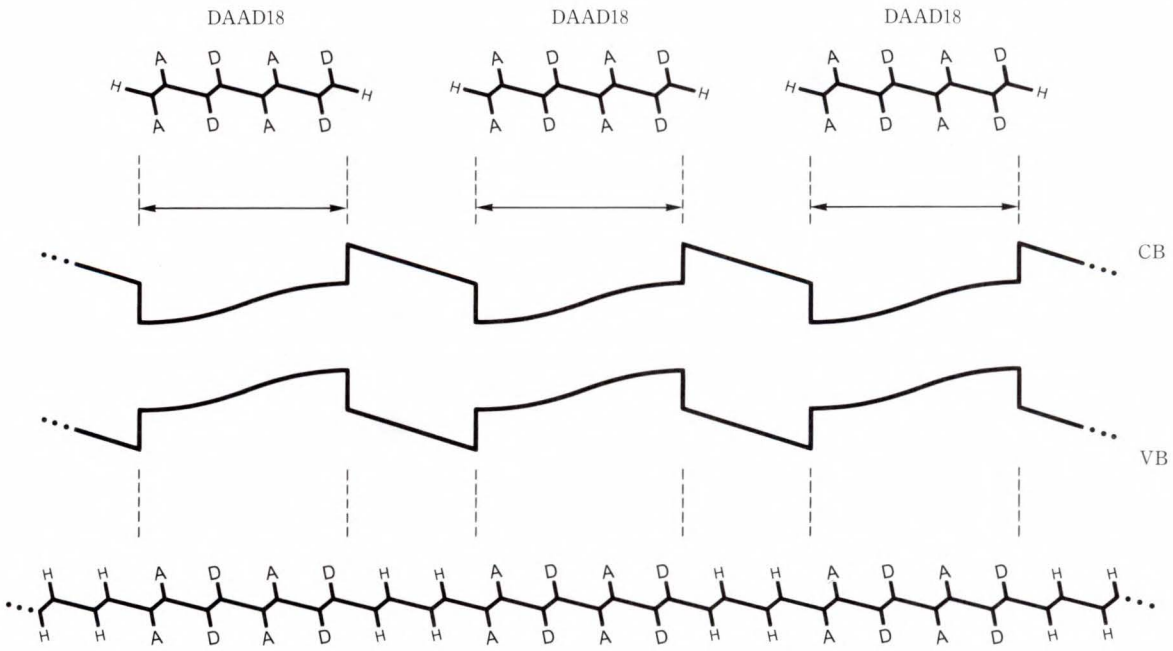
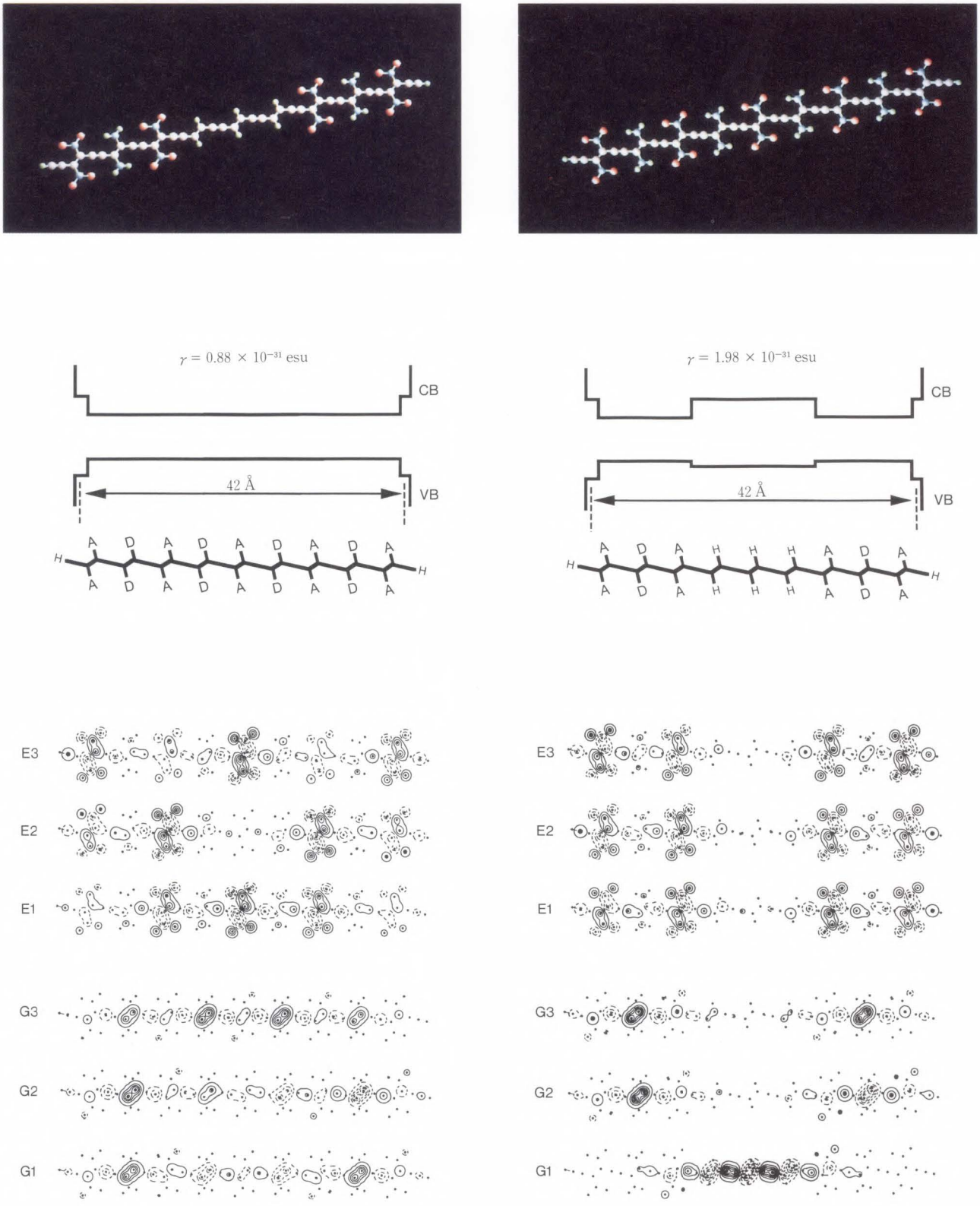


Fig. 20—Multiple quantum well formation in PDA. Wells can be regarded as DAAD18 molecules inserted in a PDA chain.



a) SQW b) DQW

Fig. 21—SQW and DQW structures designed by ANCHOR and their molecular orbitals.

substitution are barriers. The energy gap in the well region is about 1.6 eV, about one half of that in the barrier region. Molecular orbitals show that, in the SQW, electrons are spread throughout the molecular chain. In the DQW, electrons tend to be confined to both sides of the molecular chain. Here, note that, although electrons for unoccupied orbitals are localized on both sides in all E1, E2, and E3 orbitals, for occupied orbitals, electrons are in the barrier region in the G3 orbital. This suggests that the wave function tends to delocalize throughout the chain more in the valence band than in the conduction band, reproducing the condition in Fig. 18.

γ was calculated by AM1 molecular orbital calculation using the following formula:

$$\gamma = \frac{e^4}{4\hbar^3} \left\{ \sum_{\substack{n \\ n' \\ n''}} P_{gn} P_{nn'} P_{n'n''} P_{n''g} \times \right.$$

$$\left. \times \frac{1}{(\omega_{ng} - \omega)(\omega_{n'g} - 2\omega)(\omega_{n''g} - \omega)} \right\} . \quad \ldots\ldots\ldots (5)$$

The expression neglects antiresonant terms. This is because calculations were done at a deturning energy of 0.2 eV from the first excited state, which induces a large resonant enhancement in γ. As expected, γ in the DQW is more than twice that in the SQW. This indicates that it may be possible to improve third-order optical nonlinearity by adjusting the well structures.

6. Projections

Research on artificial materials, like PDA or other conjugated systems with the MQWs above, has far-reaching consequences. If a way is developed to stack a monomer on a monomer with direction control, the donor- and acceptor-substitution locations and the conjugated length could be controlled. Organic molecular beam epitaxy[35], organic chemical vapor deposition under electric field[36], and molecular layer deposition (MLD)[37], in which films grow through self-terminated monomolecular growth steps, are promising techniques for making artificial materials. It is also worthwhile to make actual EO devices using available pendant-attached polymers or molecular crystals.

In addition to controlling the wave function as described in this paper, another approach, i.e. sharpening the absorption band[38], is also important for improving optical nonlinearities by resonant enhancement. The uniformity of the conjugated length in materials is important in sharpening the absorption band, as is reducing the exciton-phonon coupling strength. Bound excitons or exciton confinements in quantum wells in one-dimensional systems may be a way to sharpen absorption bands.

Research on organic nonlinear optics involves two fields, physics and chemistry. A deficiency in either will halve progress. The author believes that, to succeed in developing the full potential of organic nonlinear materials and devices, close cooperation of physicists and chemists is essnetial.

7. Conclusion

The author investigated the use of organic materials in EO and all-optical devices, and looked for a way to make a breakthrough to a new understanding of nonlinear optical properties. First, the author clarified the goal to fabricate practical devices for optical systems. It was found that second-order optical nonlinearity must be improved by 10 times to 100 times over that of LN and that third-order nonlinearity must be improved more than 10 times over that of ordinary PDA. The authors derived qualitative guidelines for improving optical nonlinearities, i.e. that the balance between the overlap and separation (or difference) of wave functions must be optimized. Based on these guidelines, the author designed several organic materials using ANCHOR[28]. From computer simulations, it was found that organic materials have the potential to reach the goal by controlling the wave function and forming wells through adjusting the donor and acceptor substitution sites.

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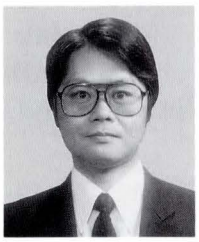

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CIM System for PC Board Design and Manufacture

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The importance of computer-integrated manufacture (CIM) in the design and manufacturing of printed circuit boards (PC boards) is widely acknowledged. It is difficult to increase the efficiency of schematic design, pattern layout design, or manufacturing using CAD/CAM separately. This paper discusses the construction of a PC board CIM system for use as a key system in a company. It describes the background and scope of CIM, and explains the concept of CIM construction, showing examples. It also introduces the automated drawing input system for PC board design and the supporting system for mounting the parts. This system is advanced technology related to CIM construction.

1. Introduction

PC board CAD/CAM is a prerequisite for the construction of PC board CIM. This chapter gives a background on the use of PC board CAD/CAM.

Competition is keen in the field of PC board design and manufacturing. Readily identifiable products are required and the time required for the entire process from product planning to shipment must be reduced to market products sooner.

High-density mounting for PC boards using surface mounting technology has made considerable progress. The number of parts per PC board has increased, and the patterns have become more complex. At present, up to 1 600 parts are used for an analog PC board. In the near future, pattern layouts using about 3 000 parts will appear. The pattern is about 0.1 mm wide. This increase in the number of parts complicates the management of parts lists related to the calculation of weight and cost. It is difficult to manage the mounting of the parts, and manual processing is almost impossible.

Separate systematization including schematic design and artwork has reached the limit for increasing efficiency and reducing the time required for the entire process. The system is used for the entire process from schematic design to drilling, assembly, and testing the PC board. It is necessary to construct a PC board CIM system for the design and manufacture of PC boards. The system must integrate CAD/CAM systems that cover systems from the schematic design system to the manufacturing system (artwork, mounting, etc.). Also, it has to link the three departments: Design department using PC board CAD, production department, and manufacturing department.

This paper discusses the basic ideas of constructing a PC board CIM system, and then explains the system of analog PC boards of the ICAD/PCB[Note)] as an example.

Note: ICAD/PCB (integrated Computer-Aided Design and manufacturing system/Printed Circuit Board) is the system for PC board design and manufacture in ICAD[1)], which is Fujitsu's CAD/CAM system. Fujitsu developed this system based on the technology accumulated through designing PC boards for computers and communication equipment. Fujitsu has expanded the system in cooperation with its customers.

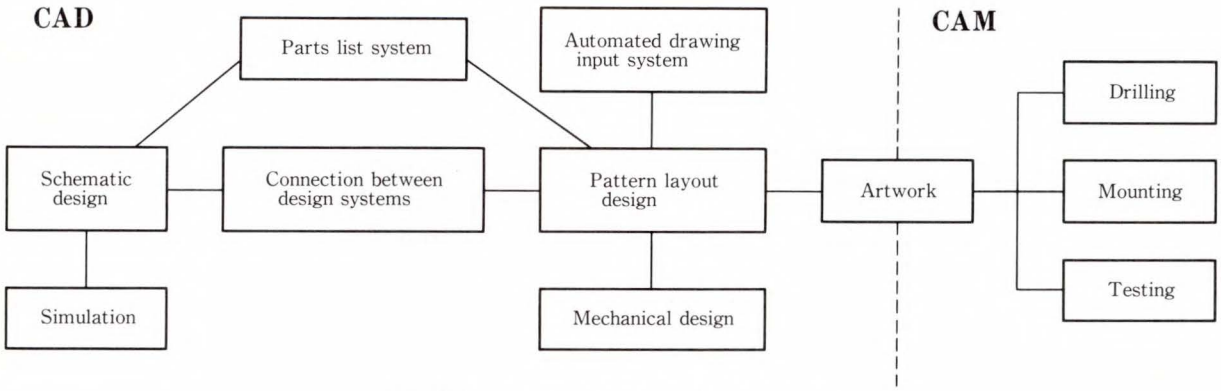


Fig. 1—Structure of PC board CIM system.

2. Structure of the PC board CIM system

Figure 1 shows the structure of the PC board CIM system. The core components of the system are the schematic design system and the pattern layout design system. These systems are closely connected with the information of nets and parts. The CAM systems are artwork, drilling, and mounting, etc. The PC board CIM must be linked to the other CAD/CAM systems, such as the parts list system, simulation, and mechanical design and mounting.

The ICAD/PCB almost covers these requirements, and facilitates the construction of CIM.

3. The basic idea of CIM construction

The following four points are important for constructing a PC board CIM system.

1) Supporting a flexible design flow

It is essential not to fix the design flow of processes such as schematic design, pattern layout design, and PC board manufacture. The system must support a flexible design flow.

2) Gradually applying the system

The system should be implemented in stages, based on the flexible design flow, without changing the current system rapidly.

3) Integration using a system link

The system should integrate the related CAD/CAM systems, such as the parts list system and mechanical CAD system.

4) Applying CAM to the assembly process

The system should be able to support not only outputting NC data for artwork and drilling, but also the assembly and test processes[2].

3.1 Supporting a flexible design flow

PC boards are designed and manufactured in several stages, e.g., primary trial manufacture, secondary trial manufacture, trial manufacture for mass production, and mass production. This cycle is repeated in a short time. Schematic design often changes during pattern layout design. Pattern layout design may be started before schematic design is completed.

The relationship between in-house design and subcontracted design also varies. The information passed to subcontractors may be rough schematic sketches or the schematic diagram and the net list generated by CAD. The subcontractors may deliver data in the gerber format after pattern layout or data of the PC board (patterns, parts, and net information). The design may change in the company while the subcontractors are working on the design.

As indicated, schematic design and pattern layout design are usually parallel processes. In-house design is also performed in parallel with subcontracted design. An integrated system for PC board CIM must accommodate a flexible design flow and be able to collate design information. That is, the system must be able to collate schematic diagrams with pattern layouts.

The patterns of design and verification generated by the ICAD/PCB are shown in Fig. 2.

1) The information of nets and parts is extracted after the schematic diagram is completed, and the pattern layout is started

using the extracted information.

2) The pattern layout is designed first. When the schematic diagram is completed, the information of nets is incorporated into the pattern layout.

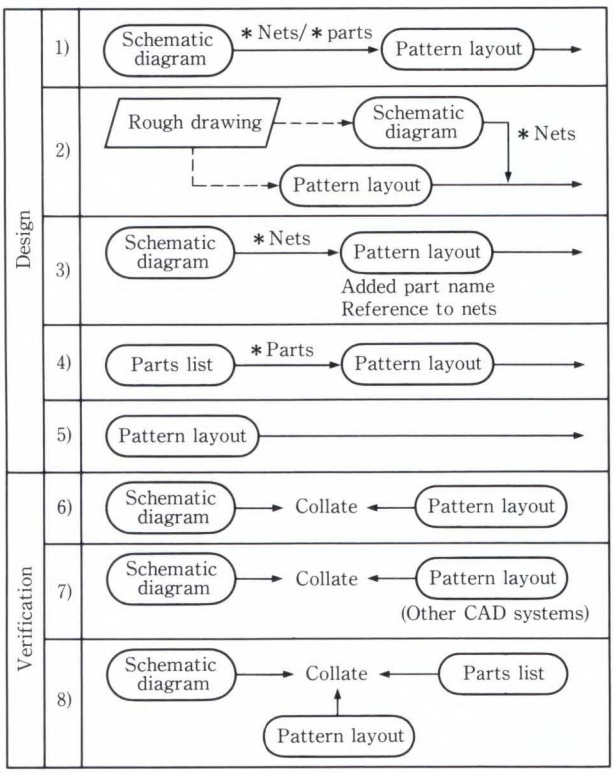


Fig. 2—Flexible design flow and some collations.

3) The pattern layout is designed using only the nets of the schematic diagram. Then, the part names are added while designing the pattern layout, and the related nets are incorporated when the parts are assigned.

4) The information of parts is extracted from the parts list system, and the pattern layout is started using the extracted information.

5) The pattern layout is designed without preparing a schematic diagram.

6) The schematic diagram is collated with the pattern layout.

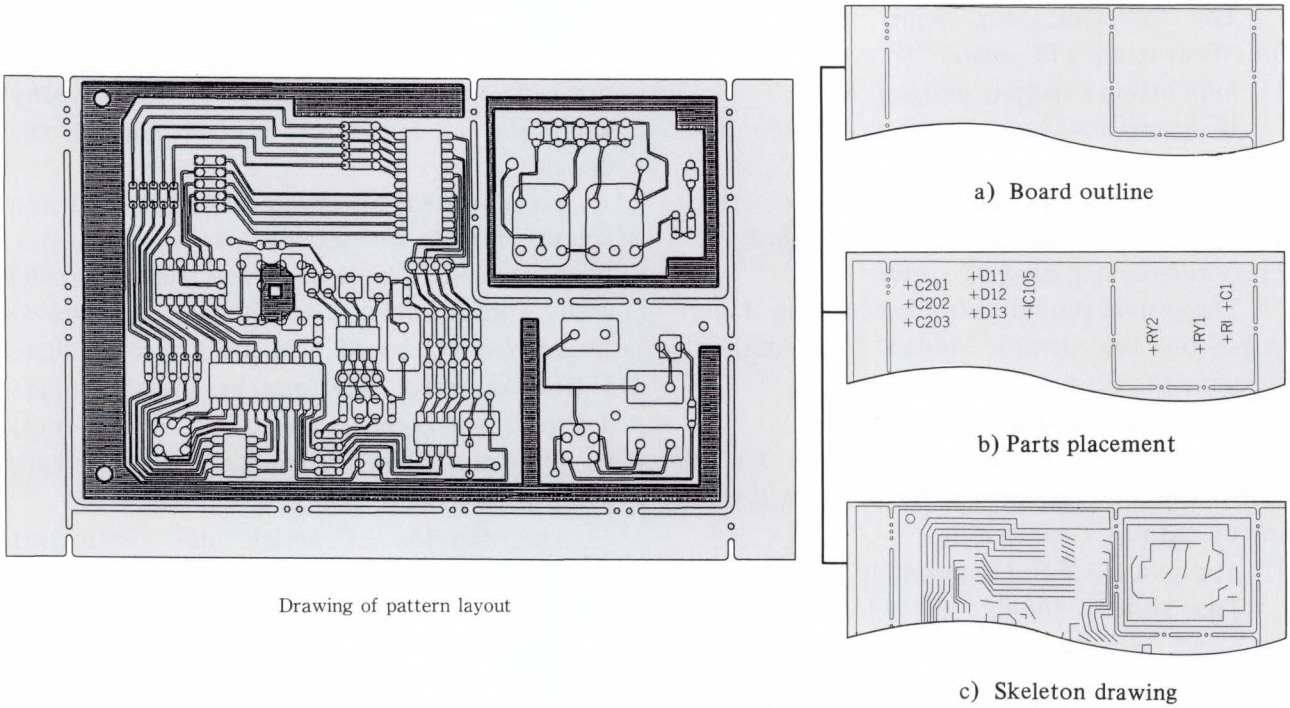
7) The schematic diagram designed in the company is collated with the pattern layout designed by a subcontractor using another CAD system.

8) The schematic diagram, pattern layout, and parts list are collated (a triple collation).

3.2 Gradually applying the system

The following method is generally used to design the pattern layout for PC boards.

The pattern layout is drawn by subcontractors by hand. The drawing is then digitized with the CAD system because it is difficult



Drawing of pattern layout

a) Board outline

b) Parts placement

c) Skeleton drawing

Fig. 3—Three types of drawings prepared by hand.

to design analog pattern layout automatically. CIM construction will not succeed if the current design work is changed rapidly. It is important to introduce the system gradually, utilizing the current design work. The ICAD/PCB enables the separate use of individual subsystems, such as the schematic design system, pattern layout design system, and manufacturing system.

This paper introduces the system for drawing input. This is an automated drawing input system for PC boards, for gradually applying the system considering the actual design conditions. With such a system, drawings of pattern layout are made by hand using a pencil and plotting paper. The drawings prepared by hand are classified into three types (see Fig. 3).

1) Board outline
2) Drawing containing part name and the cordinates (parts placement)
3) Drawing of only the paths of the pattern (skeleton drawing)

In the digitized system, these drawings are designed in the same way as drawings done by hand. This enables design to continue without placing a burden on the new system. These drawings are input by a scanner, and are converted to CAD data after segment and character recognition. For a skeleton drawing, the program automatically performs width adjustment and teardropping. In this way, the skeleton drawing is converted into the pattern drawing.

The ICAD/PCB pattern layout editor must correct segments of the drawing done by hand that are indistinct and cannot be recognized (about 2 percent in normal operation). After the pattern layout data is generated, ICAD/PCB is used to complete the design by editing and modifying the data. The processing time, compared with that for the digitizing system, can be greatly reduced (see Fig. 4). For example, it is possible to reduce the time required by accepting drawings prepared by hand from subcontractors for use with the automated drawing input system.

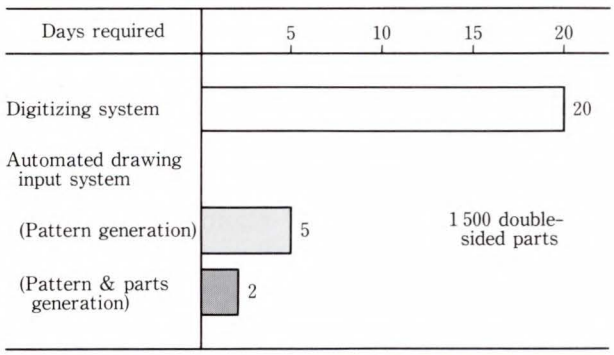


Fig. 4—Days required for drawing input (example).

3.3 Integration using a system link

It is important when constructing the PC board CIM system to integrate the related CAD/CAM systems. For this reason, the system should open the interface to read and write to the ICAD/PCB database. Use the database as the nucleus of the PC board CIM system or system linked with other systems.

3.3.1 Parts list system

The operations linking three systems and parts library have increased (see Fig. 5).

For example, this link enables the following processing.

1) Automatic parts selection considering the cost and delivery data based on the constants and rating determined by the schematic design
2) Using the schematic diagram database to automatically generate a parts list
3) Pattern layout design can also be started based on the parts information for each pattern layout.
4) The following can be performed realtime during schematic design:
   i) Estimating the weight of the PC board
   ii) Calculating the cost
   iii) Estimating the rate of insertion

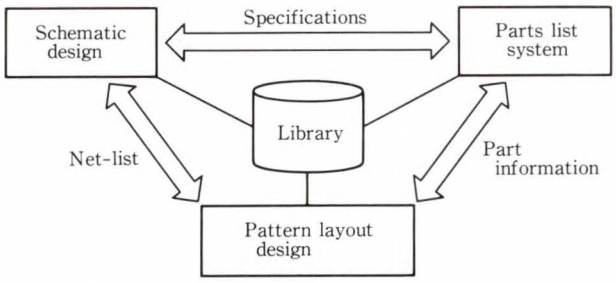


Fig. 5—System linked by parts list system.

Such information is useful for designers.

3.3.2 Other CAD systems

Many companies use a combination of two or more PC board CAD systems. Even if a company uses a single CAD system, related companies often use different CAD systems. The following are examples of the link required for the PC board CIM system.

1) Acquiring information of artwork based on gerber data
2) Collating the schematic diagrams designed in-house with the pattern layouts designed by subcontractors, based on a net file.
3) Acquiring parts information of another CAD system based on the parts list.

3.3.3 Mechanical CAD system

As high-density mounting has progressed, the outlines of PC boards have become more complex. For this reason, the outlines of PC boards are usually designed by mechanical CAD, and the data is incorporated into a PC board CAD. The following method is under examination: To return the data to mechanical CAD after PC board design, and use it for mechanical design.

3.4 Applying CAM to the assembly process

Constructing a PC board CIM system expands the range of CAM. Formerly, the main process performed by CAM was outputting NC data for artwork and drilling. Now, to reduce the time required, CAM should be applied to the assembly process. In the assembly process, experts manually generate parts mounting data, checking the machine characteristics, CAD data, and parts information. This is done to attain the following:

1) To prevent the destruction of parts
2) To reduce the time taken for mounting parts
3) To improve the ratio of machine operation

In the future, the number of parts will increase because of high-density mounting. The manual generation of data will become difficult. Support by the CAM system will be indispensable. The supporting system for mounting the parts with the ICAD/PCB satisfies these requirements, and enables the automated generation of data in the assembly process.

Table 1. Performance of parts mounting system (example)

Number of parts on PC board	Performed by	Data-generation time (hour)	Parts mounting time (s)
560	Expert	16	147
	ICAD/PCB	3	148
800	Expert	23	190
	ICAD/PCB	3	193

Table 1 shows an example that compares the work by an expert with the performance of the parts mounting system. This table indicates that the results of this system are equivalent to those of the expert. Furthermore, the time taken to generate data using this system is much less than the time taken by the expert.

4. Advanced technology related to CIM construction

The essential points of CIM construction have been explained above. This chapter concerns the technology of the automated drawing input system and the supporting system for mounting the parts, which have been mentioned as examples.

4.1 Automated drawing input system for PC boards

4.1.1 System outline

To reduce the time required for initial input to CAD, an automated drawing input system that combines the ICAD/PCB and the FADCS (Fujitsu Advanced Drawing Capture System)[3] was developed for analog pattern layout. Priority was given to the following:

1) Enabling accurate recognition
2) Preventing CAD data from increasing

Figure 6 shows the configuration of this system. First, the skeleton drawing and parts arrangement drawing based on the drawing notation is input using a scanner. Then, it is passed as image data to the recognition unit. This unit performs vectorization and character recognition. The vectorization process automatically selects a mode to extract the center

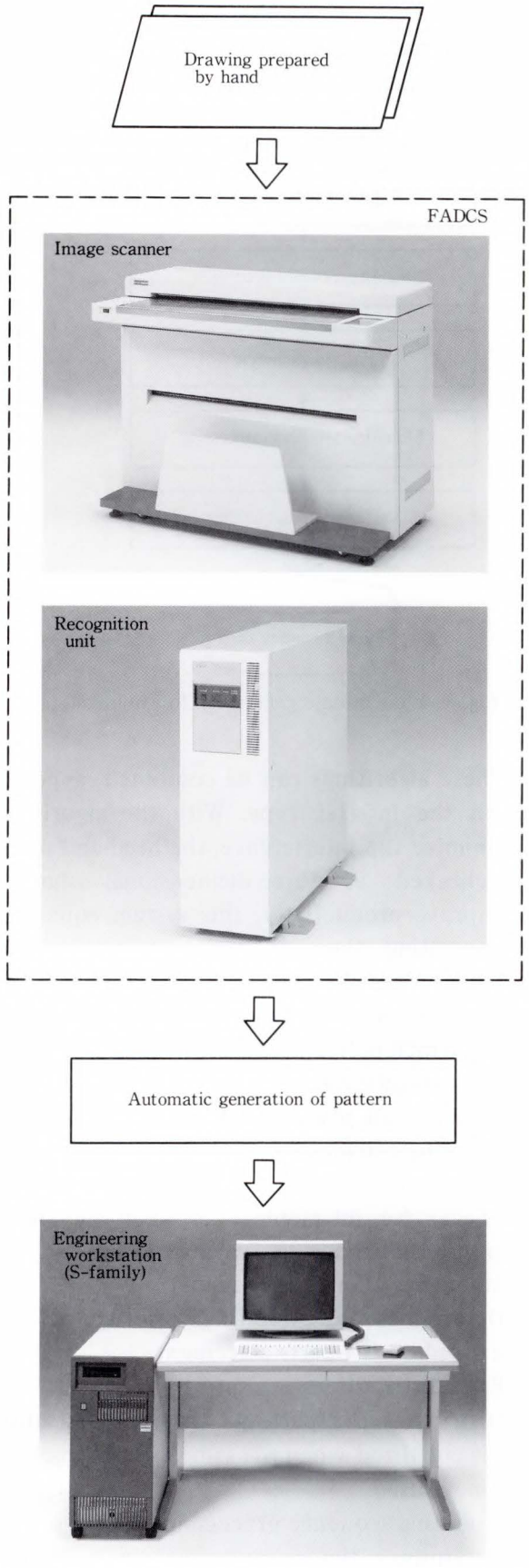


Fig. 6—Automated drawing input system for PC boards.

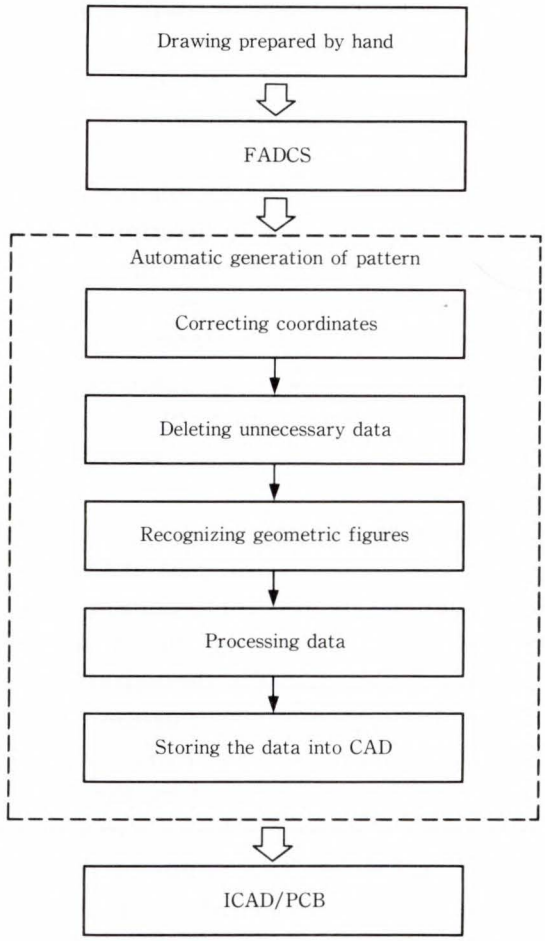


Fig. 7—Flow of pattern generation.

line or contour of the pattern. The character recognition process identifies the characters and symbols in the configuration drawing. The vector data and the character recognition results are sent to the computer.

The program for pattern generation processes the data processed by the recognition unit. The data is stored as pattern layout data in the ICAD/PCB. The ICAD/PCB checks the connection and clearance of the pattern layout data automatically. It confirms and corrects the data interactively, and designs the analog pattern layout.

4.1.2 The pattern generation process

To apply the automated drawing input system to PC board design, automatic pattern generation performs the processing shown in Fig. 7. Each step is outlined after the figure.

1) Correcting coordinates

Corrects dislocation or inclination on the

pattern drawing that occurs during input by the scanner. Adjusts the coordinates between the classified drawings (skeleton drawing, parts placement, and board outline).

2) Deleting unnecessary data

Before recognition, deletes the noise caused by dirt on the drawing or description errors, such as an irregular segment on a curve.

3) Recognizing geometric figures

To reduce the input pattern layout data, identifies straight lines, circles, and arcs based on the vector data obtained by the FADCS. Corrects their connections to identify them as smooth data.

4) Processing data

Reads the shape of the part indicated by the part number in the configuration drawing from the parts library of the ICAD/PCB. Generates the part data for the pattern layout based on the obtained information. At this time, generates a land at each pin position of the part, which is determined by the position and direction of the part. For a pattern path, rounds the endpoints and points of inflection at the center of the lands and generates through-holes at the open endpoints. In this way, makes adjustments between the drawings. Finally, adjusts the width of the identified pattern, planes the surface, and smoothes and teardrops the pattern.

5) Storing the data into CAD

Stores the data of the recognized and processed pattern and parts in the ICAD/PCB database.

4.2 Supporting system for mounting the parts

4.2.1 System outline

The parts mounting system aims at reducing the time taken for parts mounting. The following algorithms for parts mounting with the ICAD/PCB are used for this purpose:

1) Minimizing the movement of the head table (basic algorithm)
2) Minimizing the movement of the cassette
3) Minimizing the interference between the head and parts
4) Minimizing the head rotation
5) Minimizing the pitch change

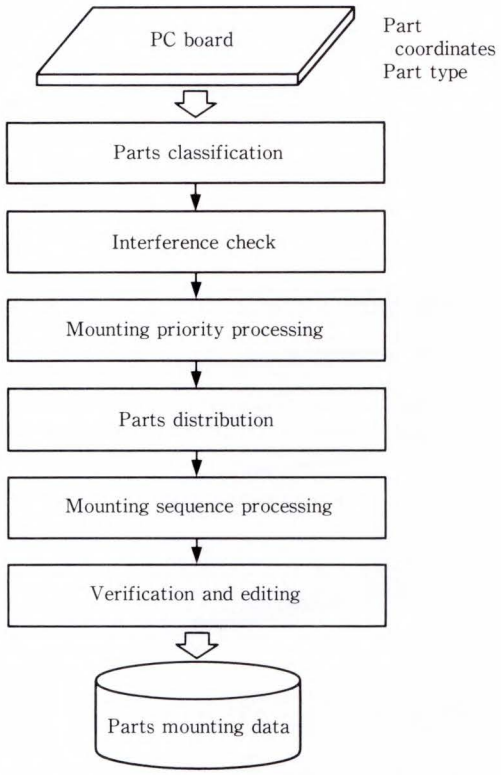


Fig. 8—Flow of data generation for mounting.

These algorithms can be combined, depending on the inserter type. With the algorithm to minimize the interference, the head and parts are checked as three-diemensional shapes. To improve productivity, this system equalizes the operating time of each inserter in the assembly process.

Figure 8 shows the configuration of this system, which performs the following:

1) Parts classification

Classifies all parts mounted on a PC board based on their shapes and specifications.

2) Interference check

Checks for interference between the parts and inserter head during parts mounting.

3) Mounting priority processing

Determines the mounting priority of the parts based on the parts placement.

4) Parts distribution

Distributes the parts so that the assembly time is equalized when the same type of inserter machine is used.

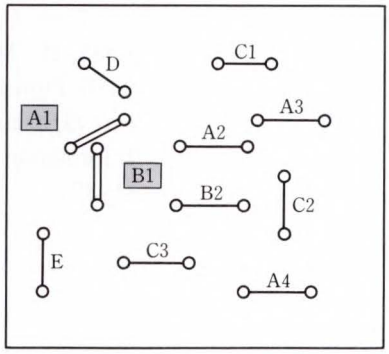
5) Mounting sequence processing

Determines the parts mounting sequence based on the specific algorithm for reducing

a) Structure of assemble line

Type of parts	Quantity
A	4
B	2
C	3
D	1
E	1

b) Parts information



c) Parts placement

Inserter machine No.1	Inserter machine No.2
B × 2	A × 4
D × 1	C × 3
E × 1	

d) Parts distribution

Fig. 9—Model of data generation for mounting.

the time taken for mounting the parts.

6) Verification and editing

Verifies the mounting time and the imbalance in the operating time between the inserter machines, based on the mounting sequence and the operation characteristics of the inserter machines.

4.2.2 Procedure for generating data for mounting

This section explains the procedure for generating data for mounting, using the model shown in Fig. 9 as an example.

The model consists of two inserter machines of the same type. Five types of parts and eleven parts are specified. The mounting tact of each machine is 0.8 s and 0.4 s per part.

First, an interference check is made based on the following information:

1) Placement of the parts mounted on the PC board
2) Head shape when the head catches on a part registered in the machine library
3) Shape of parts in the parts library

When parts A1 and B1 will interfere, the mounting priority processing generates information in the part priority table whereby part B1 has priority over part A1.

The distribution of parts types is based on the quantity of parts and the placement information. For parts distribution processing, the parts priority and the performance ratio of the mounting tact are considered. Since the tact ratio of the two inserter machines is 2:1, the parts distribution ratio is set to 1:2. The distribution results are generated in the sequence table for parts mounting. After the parts have been assigned to the inserter machines, the mounting sequence is determined for each sequence table, considering the parts placement information, parts priority, and operating characteristics of the machines.

Finally, the mounting time for each machine is verified to equalize the operating time.

This model uses two inserter machines of the same type. Any number of machines can be used.

5. Conclusion

Technological innovation is keen in the field of PC board design and manufacturing. It is necessary to reduce the time required for these processes. For this reason, the demand for the PC board CIM system will increase.

This paper discussed the basic idea of the PC board CIM system, giving examples of the ICAD/PCB. It is important to use the CAD/CAM system as the nucleus in this system. It is also important to establish the database

management technology used for centrally managing the technical information, such as parts lists, parts attributes, drawings, and technical documents. It is also necessary to establish the network technology that enables information to be transferred smoothly between related departments.

Fujitsu will acquire the related technology and enhance the ICAD/PCB as the nucleus of the PC board CIM system.

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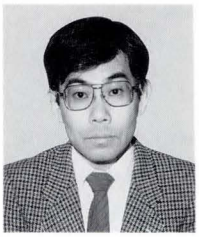

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High-Speed Structural Analysis Program: POPLAS®/FEM5 on Supercomputer

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This paper describes the high-speed processing achieved by the development of the structural analysis program POPLAS®/FEM5 (called FEM5) on the multiple-pipeline architecture of the FUJITSU VP-series supercomputer.

The CPU time has been reduced by using a method of solving simultaneous linear equations that takes advantage of performance capabilities of a supercomputer. This method is combined with a matrix column-row exchange method. Concentrated vector tuning is also used. The I/O time has been reduced by developing original I/O processing. As a result, FEM5 has achieved superlative high-level, high-speed processing in the structural analysis field.

1. Introduction

With the increase of more advanced, more complicated products in recent years, the range of processes subject to simulations in product development has extended. The scale of these processes has become larger, and the need for supercomputers[1),2)] has grown. In the structural analysis field, there is a great demand to reduce the time necessary for product development. For example, company A, a Fujitsu VP user, asked Fujitsu to improve the performance of structural analysis program FEM5 based on finite element method, with a technique that utilizes the performance of the FUJITSU VP-series, so that FEM5 can solve large-scale problems.

Fujitsu has developed and provided FEM5, which operates on computers ranging from supercomputers to workstations. Two hundred and fifty copies of FEM5 have been distributed.

For our development of high-speed processing by FEM5 on a supercomputer, the target performance for FEM5 was specified based on the requirements of company A as follows: FEM5 can solve a problem with about 15 000 degrees of freedom (matrix size: 15 000×15 000) requiring CPU time and elapsed time that are 0.8 to 1.2 times as long as those taken for the general-purpose structural analysis program "α", the famous fastest general-purpose program.

2. Problems

In converting a commercial structural analysis program for use on a supercomputer, the scalar version of the source program, the version which is used on general-purpose computers, is copied as is onto the supercomputer. Then this source code is vectorized using an automatic vectorizing FORTRAN compiler. Alternatively, more often the source program is subjected to vector tuning by hand and tested.

An algorithm such as that for solving simultaneous linear equations, exchanging the columns and rows of a matrix, etc., that fully takes advantage of the performance of a supercomputer has not been applied to a commercial structural program. Also, no programming technique that takes full advantage of the performance capabilities has been examined on the application program side. The CPU time and I/O time have not been reduced effectively.

2.1 Reduction of CPU time

Effectively reducing the CPU time on a supercomputer requires the following:

1) Employing a method of solving simultaneous linear equations that takes advantage of the performance of the supercomputer CPU
2) Combining the solution method with a matrix column-row exchange method to maximize the performance
3) Improving the vectorization ratio through concentrated vector tuning efforts

2.2 Reduction of I/O time

To reduce I/O time effectively on a supercomputer, a new method for an application program must be developed for the following reasons:

1) There is a method that depends on the specific hardware, whereas none of the methods operate on the standard hardware configuration.
2) There is no general method to reduce the I/O time. For each application, the best method must be developed with the characteristics of the application taken into account.

3. Developed techniques

The following new techniques have been developed. They reduce the CPU time and I/O time to make full use of the performance of a supercomputer, instead of simply using the scalar version of the source program of FEM5 on the supercomputer.

1) Block skyline method
2) GPS method (Norman E. Gibbs, William G. Poole. Jr, and Paul K. Stockmeyer method)[3] combined with the block skyline method
3) Concentrated vector tuning
4) Design of parallel I/O functions and combination with the block skyline method

3.1 Choice of the block skyline method

There are some methods for solving linear simultaneous equations, such as the band matrix method, the block skyline method, the active column method, and the CG method (the conjugate gradient method). The block skyline method and the CG method are known for taking advantage of the CPU performance of a supercomputer.

The algorithm for the block skyline method solves linear simultaneous equations while reducing the related columns for each column of the matrix. When the block skyline method is written in FORTRAN, a multi nested Do-loop source program is obtained. When the FORTRAN program is compiled with the automatic vectorizing FORTRAN compiler for a supercomputer, an object module with an extremely high vectorization ratio is obtained.

The CG method also takes advantage of the CPU performance of a supercomputer. A prototype was produced and evaluated with a real problem (honeycomb-structure car parts). Although the prototype sometimes resulted in outstanding CPU performance, the results showed that unstable convergence occurred for some data. Therefore, the CG method was not adopted for a commercial general-purpose program.

This is why the block skyline method was adopted. The block skyline method is outlined below:

1) Only the upper right triangular portion of a matrix is handled, because matrices handled in linear structure analysis are symmetric.
2) The area up to the nonzero element (called the skyline) that is farthest from the diago-

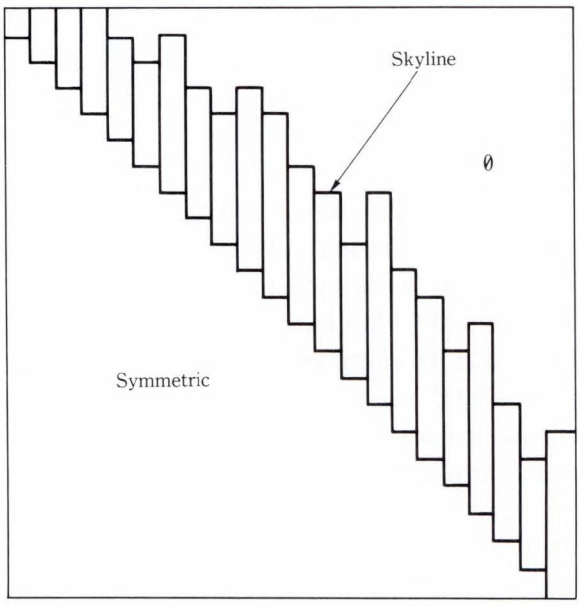
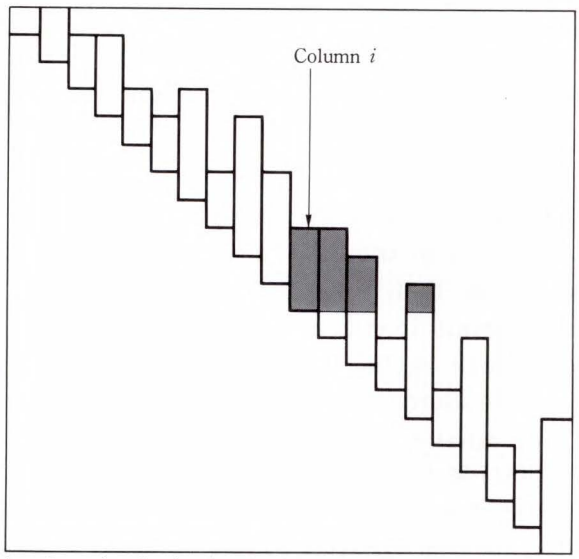


Fig. 1—Skyline.

nal element is handled (see Fig. 1).

3) Forward reduction and back-substitution are performed for each column of a matrix (see Fig. 2).

4) I/O operations are performed between an external storage unit and main storage for each group of columns (called a block) (see Fig. 3).



(e.g. foward reduction for the ith column)

Fig. 2—Operation for each column in a matrix.

3.2 GPS method combined with block skyline method

Only nonzero elements of the matrix proc-

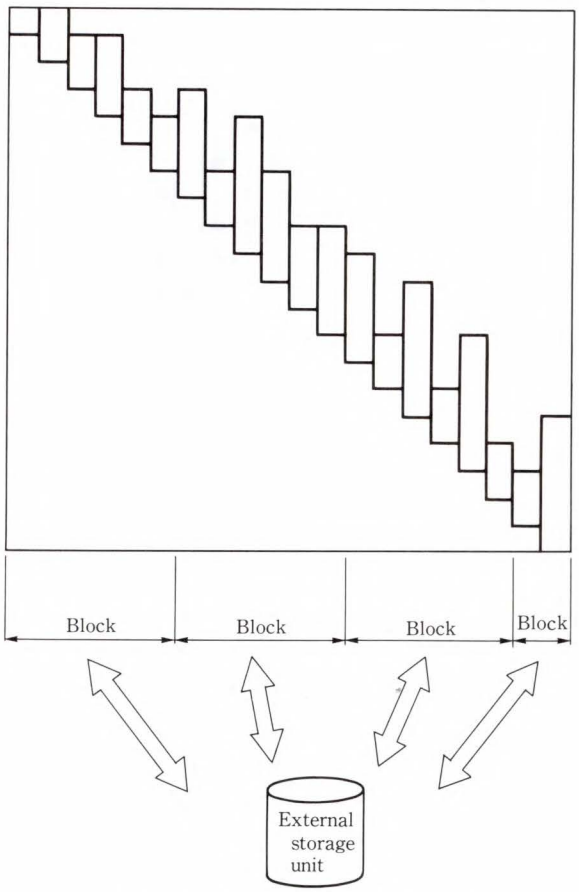
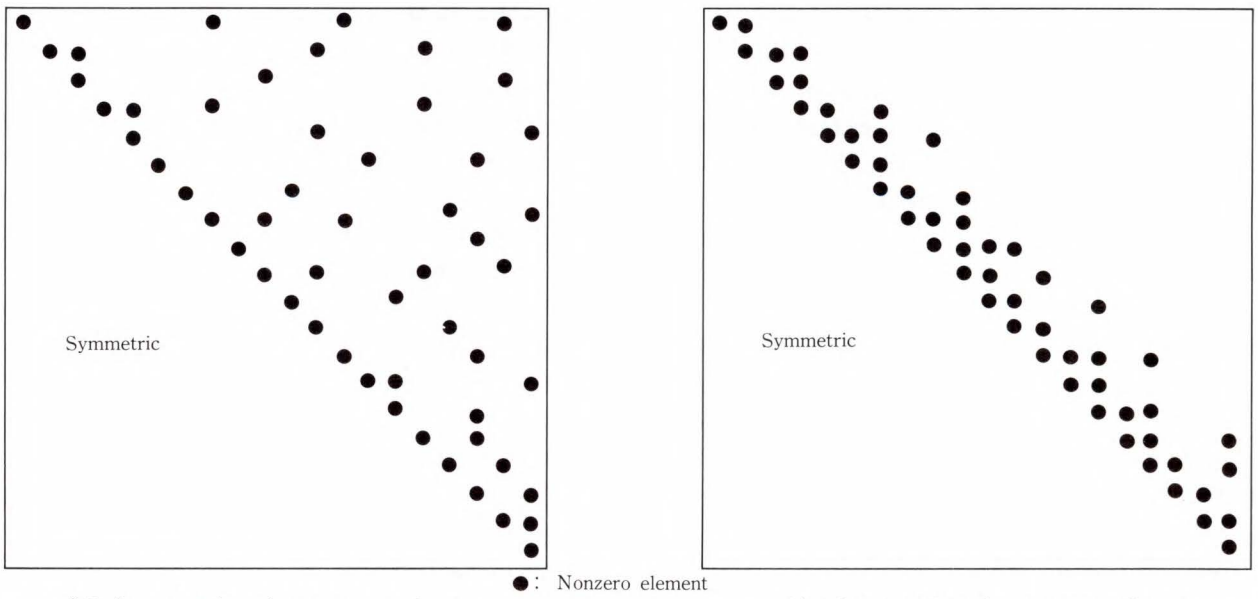


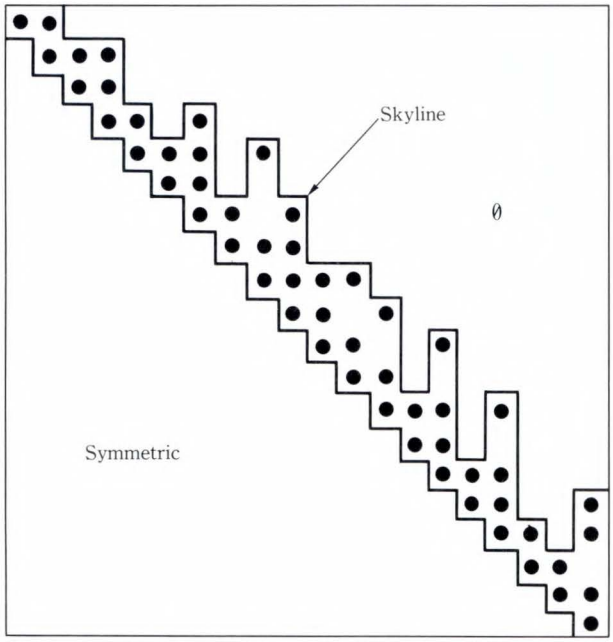
Fig. 3—I/O processing for each block.



a) Before matrix column-row exchange

b) After matrix column-row exchange

Fig. 4—Matrix column-row exchange.



GPS minimizes the area between the skyline and diagonal elements

Fig. 5—Feature of the GPS method.

essed in structural analysis can be collected near the diagonal element in a column-row exchange (see Fig. 4). Some column-row exchange methods are available. To reduce the CPU time and I/O time effectively, a method fit for the simultaneous linear equations solver is needed.

The algorithm of the GPS method is characterized by its ability to minimize the area between the skyline and the diagonal element. This characteristic enables a matrix to be generated so that the number of operations in the block skyline method and the quantity of I/O data between main storage and the external storage unit can be minimized (see Fig. 5). Therefore, the GPS method was adopted as the method that could maximize the performance of the block skyline method.

GPS processing is outlined below:

1) The apexes of both ends in the longitudinal direction of element division are selected.
2) The level (distance from the apex) of each node is determined.
3) The level structure that minimizes the number of nodes of the same level is selected by repeating steps 1) and 2).
4) Nodes are numbered in the order of the level.

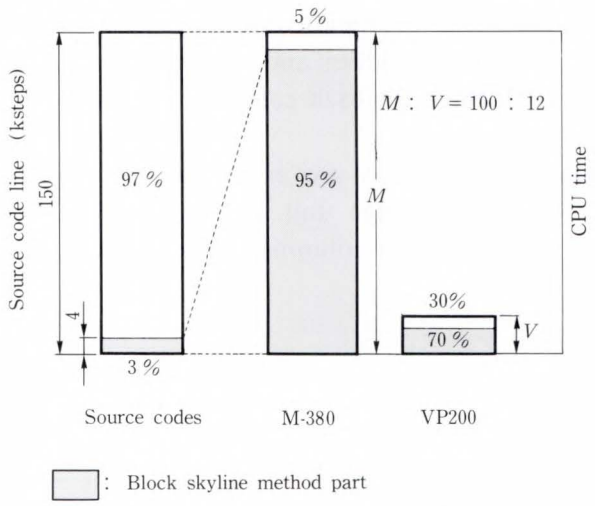


Fig. 6—Distribution of CPU time.

3.3 Concentrated vector tuning

Analysis of the CPU time using a real problem shows that, for a problem whose matrix size is about 15 000 x 15 000, about three percent (block skyline method part: 4 ksteps) of the entire source code takes up about 95 percent of the total CPU time in a scalar computer FUJITSU M-380 (see Fig. 6).

Therefore, the CPU time can be greatly reduced by concentrating vector tuning efforts on the block skyline method part of the source code (For example, expanding DO-loops, exchanging indices of nested DO-loops).

In the final results, the ratio of the total CPU time of M-380 to that of FUJITSU VP200 was 100 to 12 (see Fig. 6). This ratio exactly represents the effect of vectorization because the VP200 has the same scalar performance as the M-380.

3.4 Parallel I/O function combined with block skyline method

In the block skyline method, the data (two blocks) necessary for forward reduction and back substitution which is performed for each column of a matrix is stored in a work area in main storage. If the data is in more than two blocks, it is necessary to transfer them to an external storage unit to perform direct I/O processing of each block, and to transfer the blocks necessary for operation to main storage (see Fig. 7). For a problem whose matrix size is

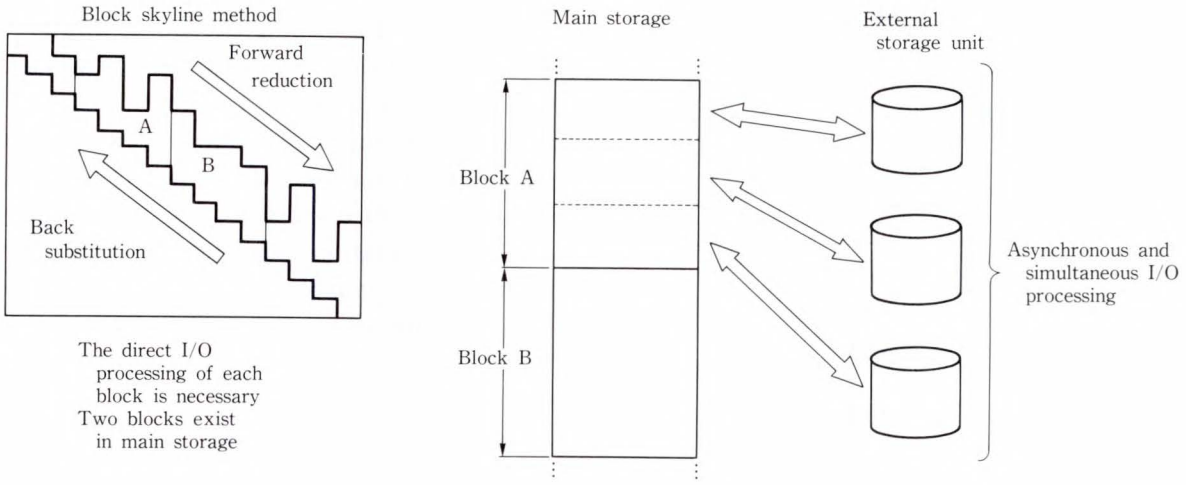


Fig. 7—Block skyline method and parallel I/O method.

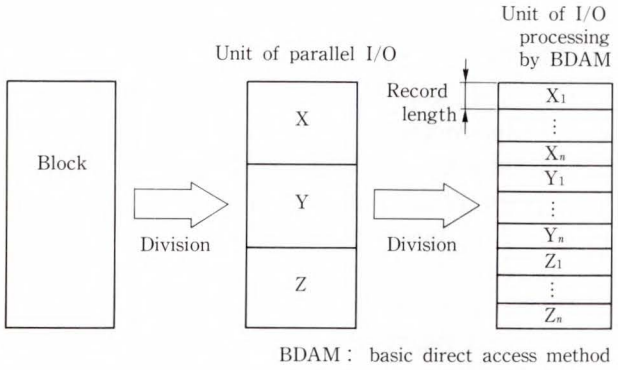


Fig. 8—Block division.

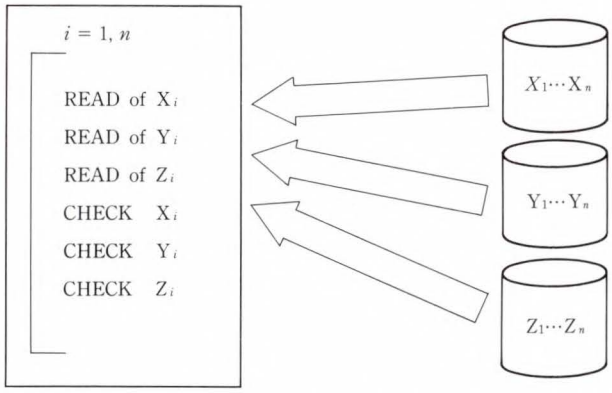


Fig. 9—Parallel I/O routine.

about 15 000 x 15 000, the area between the skyline and the diagonal element is 40 Mbytes and much I/O data is generated.

The block skyline method is characterized by its I/O operation which is performed in block units. This characteristic was used to develop an original parallel I/O function (see Fig. 7). This function divides a block into subblocks and performs subblock I/O operations for multiple external storage units simultaneously and asynchronously.

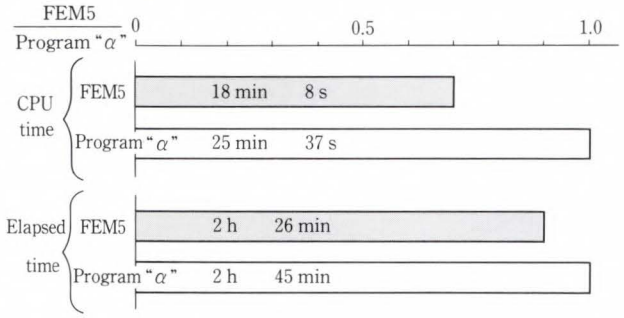
Figure 8 shows how a block is divided. Figure 9 shows the processing performed by the parallel I/O routine.

Because I/O operations are performed simultaneously for multiple external storage units, the number of subblocks that constitute a block and number of paths for the channels that are to operate concurrently must be increased. Independent channel paths must be assigned to the storage units. Otherwise channels will compete and the I/O time will not be effectively reduced.

In FEM5, the number of subblocks varies from 1 to 10 so that FEM5 can flexibly adapt itself to the hardware configuration of a user system. In actual user operations, the number is usually 4.

4. Results

The FEM5 program developed using the above methods has been tested with seven samples of car structural analysis data (matrix size: 5 202 x 5 202 to 21 826 x 21 826) on the FUJITSU VP100 system of company A. The results show that the CPU time is 18 minutes and 8 seconds and that the elapsed time is 2 hours



Computer : VP100
A total of seven samples of data
(matrix size : 5 202 × 5 202 to 21 826 × 21 826)

Fig. 10—Survey data of CPU time and elapsed time.

26 minutes (total of seven samples of data). On the other hand, program "α" required the CPU time of 25 minutes 37 seconds, and the elapsed time of 2 hours 45 minutes for the same samples of data. Thus, assuming the CPU and elapsed time for program "α" to be 1, respectively, the results show a CPU time of 0.7, and elapsed time of 0.9. These values satisfy the requirements (see Fig. 10). As of August 1990, the CPU time and the elapsed time are less than those obtained by any other general-purpose finite element analysis program in the world.

5. Conclusion

The development of FEM5 has reduced the CPU time and I/O time resulting in high-speed processing by FEM5 on a supercomputer. To reduce the I/O time, a new parallel I/O function has also been developed. The application of the parallel I/O function to other programs has revealed that it can be used as a general-purpose function to reduce the I/O time in a batch type technical calculation program. The same function has been available as a high-speed I/O function in the library of the Fujitsu FORTRAN77 EX V11 compiler for general users since September 1990.

Fujitsu plans to continue this technical development according to the performance of the supercomputer hardware functions (such as expanded high-speed data space and virtual I/O features), and to achieve faster processing.

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