M E M O R A N D U M

TO: DISTRIBUTION DATE: September 20, 1983

FROM: Dave Nudelman DN

SUBJ: Central Logic Bus Interface
Manual Specification

There will be a meeting to review the Central Logic Bus Interface Manual Specification on Monday, September 26, 1983, at 11:00 a.m. in the Engineering Conference Room.

Please review this document before the meeting and be ready to discuss it. If you are unable to attend the meeting and have comments on the CLB spec, please call me at x438 or send someone from your group to the meeting.

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FORTUNE SYSTEMS CORPORATION

CENTRAL LOGIC BUS
INTRERFACE MANUAL

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Section 1

General Description

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This document describes the Central Logic Bus (CLB) of the Fortune Systems 32/16 computer . It is divided into four parts ; Section 1 which provides a general description of the Central Logic Bus ; Section 2 which provides mechanical specifications , Section 3 which provides logical specifications , and Section 4 which defines electrical specifications . Figure 1 , at the end of this section , shows the Central Logic Bus connector and pinouts .

The ~~mecinal~~ mechanical specification includes a description of the size of the option boards , the location of connectors , and the numbering of pins on the connector . The logical interface discusses the various siginals on the CLB and their rules of protocol and timing . The electrical specification includes voltage levels , D.C (current) asnd A.C. (capacitance) loading .

Additional documents which should be procured as supplements to this document are as follows :

CPU, MMU , Motherboard Hardware Spec
Hardware Design Specification Basic System
In-House Software Documentation Guidelines
Power Supply Specification
Printed Circuit Layout Guidelines
Voltage Sense Module Hardware Design Specification

The CLB is the primary control and data transfer path within the Fortune system central logic subassembly. The major logic components such as processor, memory subsystem, and device controllers are interconnected through the CLB (The memory array cards interface to the memory controller, which is in turn connected to the CLB) .

The CLB was targeted to support a set of devices with a high aggregate transfer rate: 6 MHz 68000 CPU (24 Mb/s), Ethernet port (10 Mb/s), high speed Winchester disks (5-10 Mb/s), and bit-mapped display (15 Mb/s).

The CLB is a system bus, not a processor bus. It is based on synchronous system timing, with multi-master control of transfers, and with centralized arbitration logic. Each master (processor or DMA controller) ordinarily holds the CLB just long enough for one trasfer of a byte or word to or from some CLB address. Bus arbitration is pipelined one cycle ahead to eliminate delay switching from master to master. Synchronous timing control permits simple control logic in each master.

The basic bus timing is generated by a bus subsystem controller. Certain types of access may involve cycles which are extended by one or more bus cycles, such as a byte write when using ECC with memory.

Because the processor is the most latency-sensitive device, the arbitrator assumes that the processor is about to use the next cycle, and enables the processor's address buffers by default. This technique saves one clock cycle in the usual case of continual processor memory references since the processor gives no early warning that it is about to use the bus. The arbitration logic processes the DMA requests in parallel during each clock cycle and determunes which controller has the highest priority. This way the arbitration amounts to a binary decision: the processor, or "the other". The identity of "the other" will have been set during the preceding bus clock time. Once the processor has granted the bus, the timing is the same as any other device.

Slave devices are of two kinds: "fast," and "slow". Ordinarily, the main system memory (RAM) is the only fast device. All of the internal and standard CLB option card I/O device registers are slow devices.

The processor may be slowed down but must not be stopped during disk and network activity,. Other devices in the system such as serial ports must each have service at least once per millisecond. With one COMM/A option plus the built-in port, if all the serial ports are at 9600 baud, this amounts to six such devices , since full-duplex transfers are possible. Both disk and Ethernet transfers can take in excess of one millisecond of continuous transfer time, causing unrecoverable lost data overruns on the serial ports. The disk and Ethernet transfers can get overruns/underruns occasionally, but with human interfaces this is not acceptable .

These devices have very low latency times since heavy local buffering is not used. Full buffering has negative system throughput implications , since the system latency to get at a data block would have to include an added transfer time from the buffer to main memory. Also, too much buffering on high speed devices causes an undesirable stuttering effect since the data burst from each device draining its buffer causes the next device to fill its buffer.

The combination of tight latency and high throughput requirements dictated that the CLB is not simply a buffered copy of the processor chip pins. These requirements can easily be met with a multi-ported memory architecture, as long as the memory cycle time is less than one-half of the processor cycle time. This is desirable to avoid heavy interference from as few as one of the DMA devices transferring.

In contrast , memory cycle times as long as 0.8 times the processor cycle time would give adequate performance under heavy disk/Ethernet load, but could not also accommodate display traffic. During the design of the CLB it was determined that DMA cycles would not be shorter than 3/4 of a processor cycle. For this reason, the display was separately buffered. As a result, any memory system that can satisfy the processor's access time requirements without wait states can also meet the cycle time demands of the DMA load expected.

For slower devices such as floppy disks the fully buffered approach is reasonable. Analysis of the 68000instruction code sequences for block transfers shows the effective bus overhead of the software transfer is about 2.3 times the bus overhead of a true DMA transfer (as seen by the part of the processor not involved in the transfer). Of this amount a factor of 2 is applied since true DMA transfers (to devices on a private controller bus) only take one memory cycle for each word moved while memory-to-memory block transfers take two cycles per word. The remaining factor 1.15 is is applied since the best usable code sequences for block transfers only use about 85% of the bus cycles for data. The remainder are instruction fetches.

The issue of whether the serial ports should be DMA or not is not based on data transfer rates but on the amount of read-time intelligence needed for the various protocols and on the pre-interrupt overhead of the processor. SIO latency and throughput requirements are modest, when compared to disk or Ethernet. The buffered disk or network ports only give one interrupt per block transfer, and a buffered display gives no interrupts at all.

Main memory is implemented using 64K-bit MOS dynamic memory devices in the memory array. The array cards interface to, and are controlled by , the memory subsystem controller which provides timing signals,and address multiplexing. Each array card provides 128 Kbytes or 256 Kbytes of memory, and up to 4 array cards may be plugged into the system.

The memory controller contains all of the logic needed to interface the memory array cards to the CLB. This includes the address decode and multiplexing logic, refresh control, and optional error correcting logic. The controller contains several error save registers that are accessible to the processor in I/O address space. These registers allow the operating system to record the failing memory location, isolate the error to a single memory chip, and verify that the error correcting logic is working properly.

The memory system performance is optimized (together with the CLB arbitrator) around 16-bit word read operations by the processor, since the vast majority of all system memory cycles will be processor instruction and data fetches. A 16-bit processor write operation, or any 16-bit operation from other bus masters, proceeds at full processor/device speed. The memory controller also allows 8-bit byte write operations.

FUNCTION	NMEMONIC	PIN & STATE		MNEMONIC	FUNCTION
+12 Volt Power	+12 volts	1	2	+12 volts	+12 Volt Power
-12 Volt Power	-12 volts	3	4	-12 volts	-12 Volt Power
+5 Volt Power	+5 volts	5	6	+5 volts	+5 Volt Power
Siginal Ground	ground	7	8	CLBA1+	CLB Address 1
CLB Address 2	CLBA2+	9	10	CLBA3+	CLB Address 3
CLB Address 4	CLBA4+	11	12	CLBA5+	CLB Address 5
CLB Address 6	CLBA6+	13	14	CLBA7+	CLB Address 7
CLB Address 8	CLBA8+	15	16	CLBA9+	CLB Address 9
CLB Address 10	CLBA10+	17	18	CLBA11+	CLB Address 11
CLB Address 12	CLBA12+	19	20	CLBA13+	CLB Address 13
CLB Address 14	CLBA14+	21	22	CLBA15+	CLB Address 15
CLB Address 16	CLBA16+	23	24	CLBA17+	CLB Address 17
CLB Address 18	CLBA18+	25	26	CLBA19+	CLB Address 19
CLB Address 20	CLBA20+	27	28	CLBA21+	CLB Address 21
CLB Address 22	CLBA22+	29	30	CLBA23+	CLB Address 23
+12V (for CRT only)	+12v	31	32	+12v	+12V (for CRT only)
Signal Ground	ground	33	34	CLBD0+	CLB Data 0
CLB Data 1	CLBD1+	35	36	CLBD2+	CLB Data 2
CLB Data 3	CLBD3+	37	38	CLBD4+	CLB Data 4
CLB Data 5	CLBD5+	39	40	CLBD6+	CLB Data 6
CLB Data 7	CLBD7+	41	42	CLBD8+	CLB Data 8
CLB Data 9	CLBD9+	43	44	CLBD10+	CLB Data 10
CLB Data 11	CLBD11+	45	46	CLBD12+	CLB Data 12
CLB Data 13	CLBD13+	47	48	CLBD14+	CLB Data 14
CLB Data 15	CLBD15+	49	50	ground	Signal Ground
System Reset	CLBRESET-	51	52	spare	
	spare	53	54	CLBIO3-	CLB Int. Req. 3
CLB Int. Req. 4	CLBIO4-	55	56	T2+	
CLB Read/Write	CLBR/W	57	58	CLBAS-	CLB Address Strobe
CLB Upr. Data Strobe	CLBUDS-	59	60	CLBLDS-	CLB Lwr. Data Strobe
Signal Ground	ground	61	62	CLBCLK+	CLB Clock
Signal Ground	ground	63	64	spare	
CLB Data Bus Error	CLBPERR-	65	66	CLBPFL-	CLB Power Fail
CLB Int. Ack. In 3	CLBINTACKI3-	67	68	CLBINTACKO3-	CLB Int. Ack. Out 3
CLB Int. Ack. In 4	CLBINTACKI3-	69	70	CLBINTACKO4-	CLB Int. Ack. Out 4
CLB Bus Request	CLBBR-	71	72	CLBBG-	CLB Bus Grant
CLB Board Present	CLBPRESENT-	73	74	CLBIOS-	CLB I/O Select
+5 Volt Power	+5 volts	75	76	+5 volts	+5 Volt Power
Signal Ground	ground	77	78	ground	Signal Ground
Signal Ground	ground	79	80	ground	Signal Ground

Figure 1. CENTRAL LOGIC BUS CONNECTOR PINOUT

SECTION 2

MECHANICAL SPECIFICATIONS

This section describes the mechanical specifications of the CLB .

Connector

The connector used is a 2x40 pin PC edge connector with 0.1" pin spacing . Typical part number for the connector (mounted on the mother board) is Amp # 530843-9 .

Board Dimensions

Physical dimensions for the I/O board is shown in figure 2 . (Fortune drawing # 1000443 , page 9)

Physical demensions for the I/O plate are shown in figure 3 . (page 10)

Physical example of a I/O board , a I/O Plate and a Piggyback board are shown in figure 4. (page 11)

Physical dimensions for the mother board is shown in figure 5. (Fortune drawing # 1001176 , page 12)

Example of the air flow in the 32/16 is shown in figure 6. (page 13)

Physical example of a Fortune 32/16 system is shown in figures 7 (page 14), 8 (page 15), and 9 (page 16).

Fabrication Notes

The following fabrication notes apply to the board shown in figure 2 .

1. Materal : fl-gfm .062 c 1/1 AIA or equivalent .

2. Holes : Copper plate all holes (unless otherwise specified in hole schedule) to a minimum thickness of .001 . Upon plating the holes , the surface will have a total copper thickness of two ounces .

3. all holes are to be drilled from component side and within .003 of pad center with no breakout . Finished diameter to be within +.003-.002 unless otherwise specified .

4. Tooling holes are to be drilled to within .002 of center . They will be unplated .

5. Maximun allowable line reduction due to pits , dents , and nicks to be 30%

6. Any line run or pad shall not vary in with or diameter more than +.003-.002 due to processing .

7. Minimum annular ring to be .004.

8. Registration between patterns shall not exceed + or - .005 when measured across any diagonal .

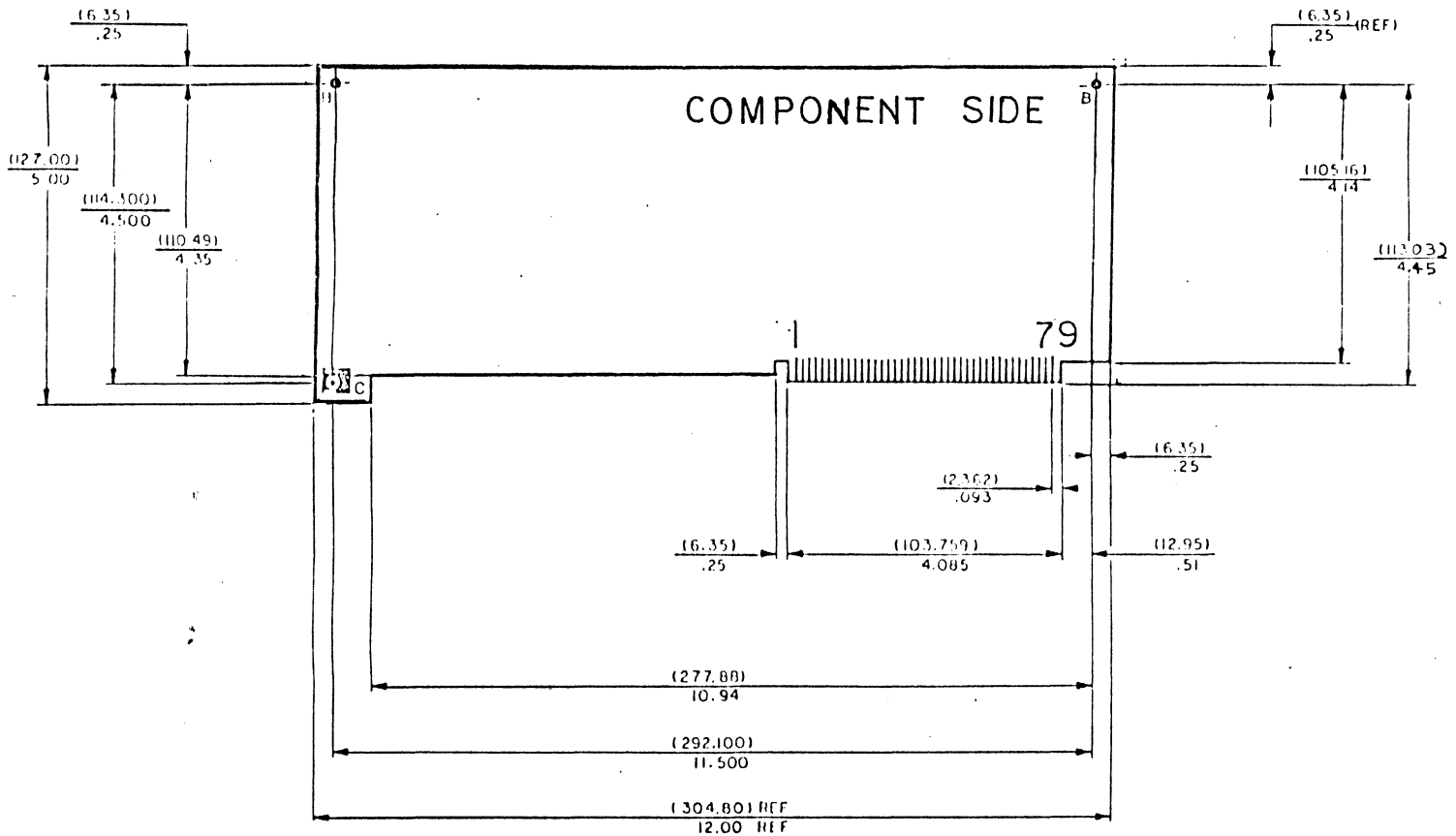
9. Finish : 60/40 tin/lead plate to a total thickness of .0003/.0007 (maximum allowable deviation of tin lead composition to be 50/50).

10. Reflow is required . The tin/lead will be bright and shiny and pulled down to base laminate with all line edges covered.

11. Connector finigers : .000015 minimun gold plate over .000100 minimum low stress nickel . Blades to be beveled 30 deg. x .025 to .031 both sides and 45 deg. x .062 both ends .

12. All interior corner radii to be .06 nominal . All finished boards shall be marked with manufacturer's logo and board type designation as specified by UL which meets flammability rating of 94V-2 or better.

13. Apply solder mask to both sides using white expoxy ink to component side .


(6.35)
.25
(6.35) (REF)
.25
COMPONENT SIDE
B
(127.00)
5.00
(114.300)
4.500
(110.49)
4.35
(105.16)
4.14
(113.03)
4.45
1
79
C
(6.35)
.25
(2.362)
.093
(6.35)
.25
(103.759)
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(292.100)
11.500
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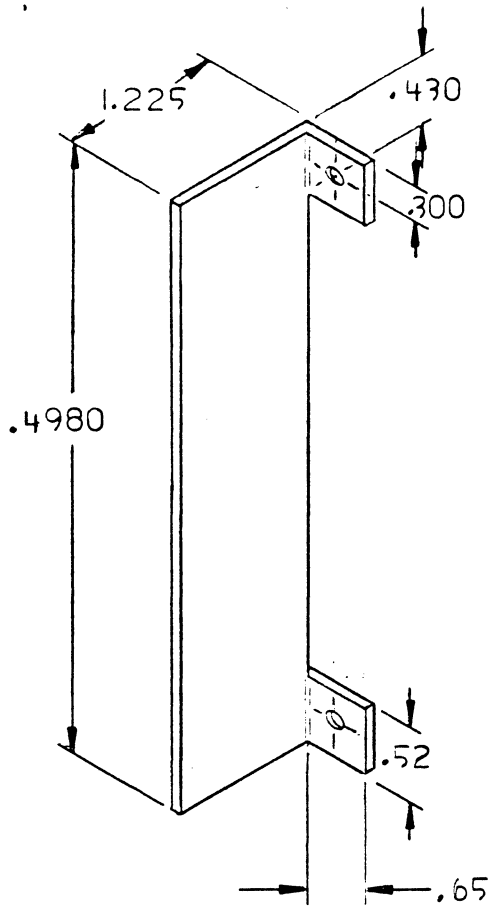
12.00 REF



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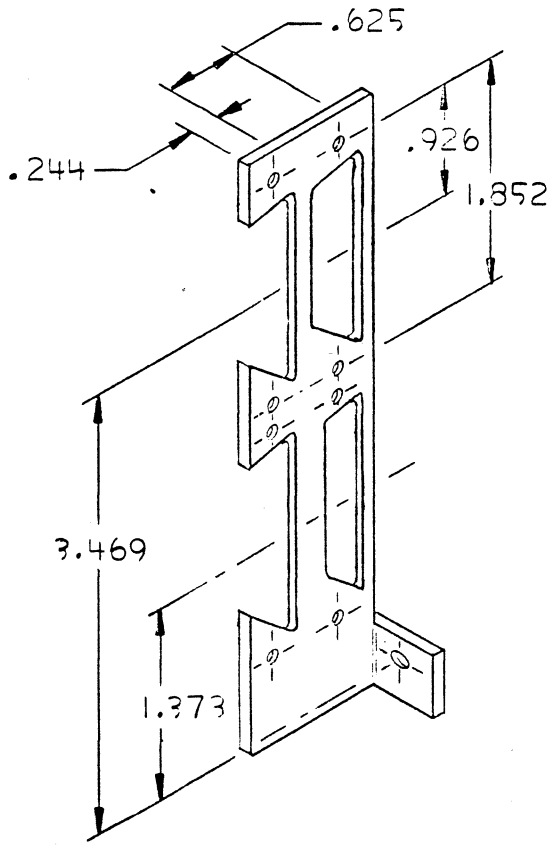
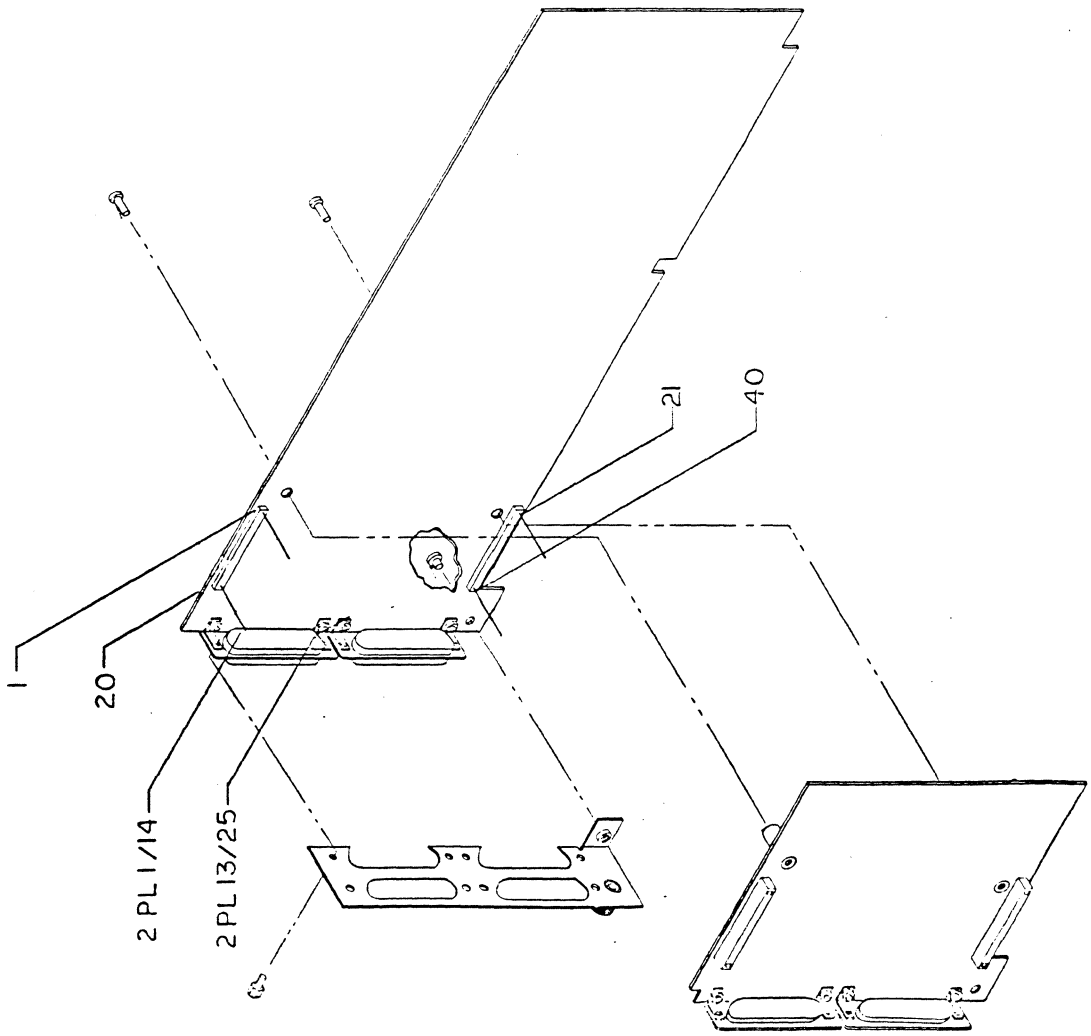
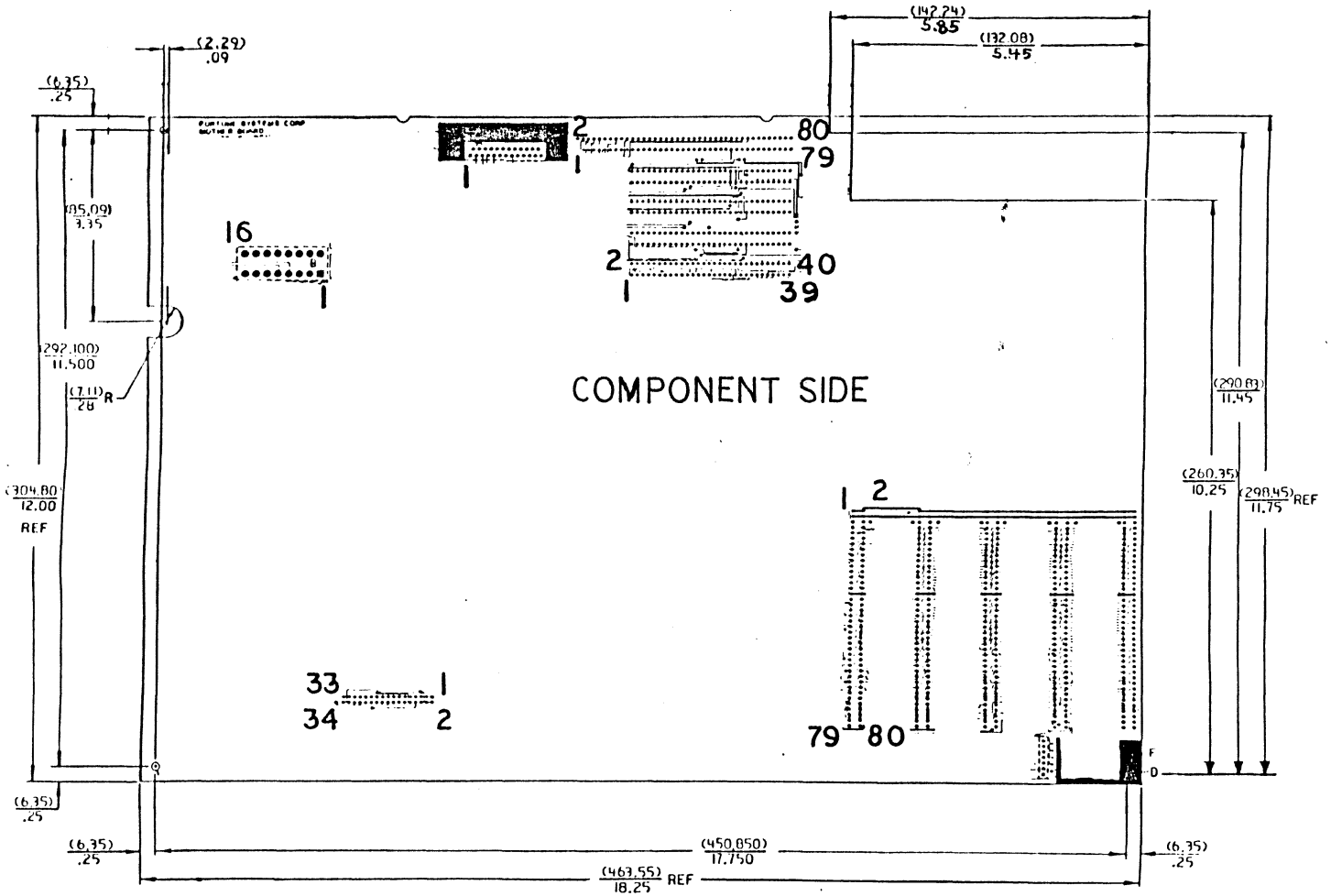


-04
ALL OTHER
FEATURES SAME
AS -01 EXCEPT
UPPER TAB
NOT REQD.


1
20
2 PL 1/14
2 PL 13/25
21
40


(142.24)
5.85
(132.08)
5.45
(2.29)
.09
(6.35)
.25
(85.09)
3.35
16
1
2
1
80
79
2
1
40
39
(292.100)
11.500
(7.11)
.28
R
COMPONENT SIDE
(290.83)
11.45
(304.80)
12.00
REF
(260.35)
10.25
(298.45)
11.75
REF
1
2
33
34
1
2
79
80
F
D
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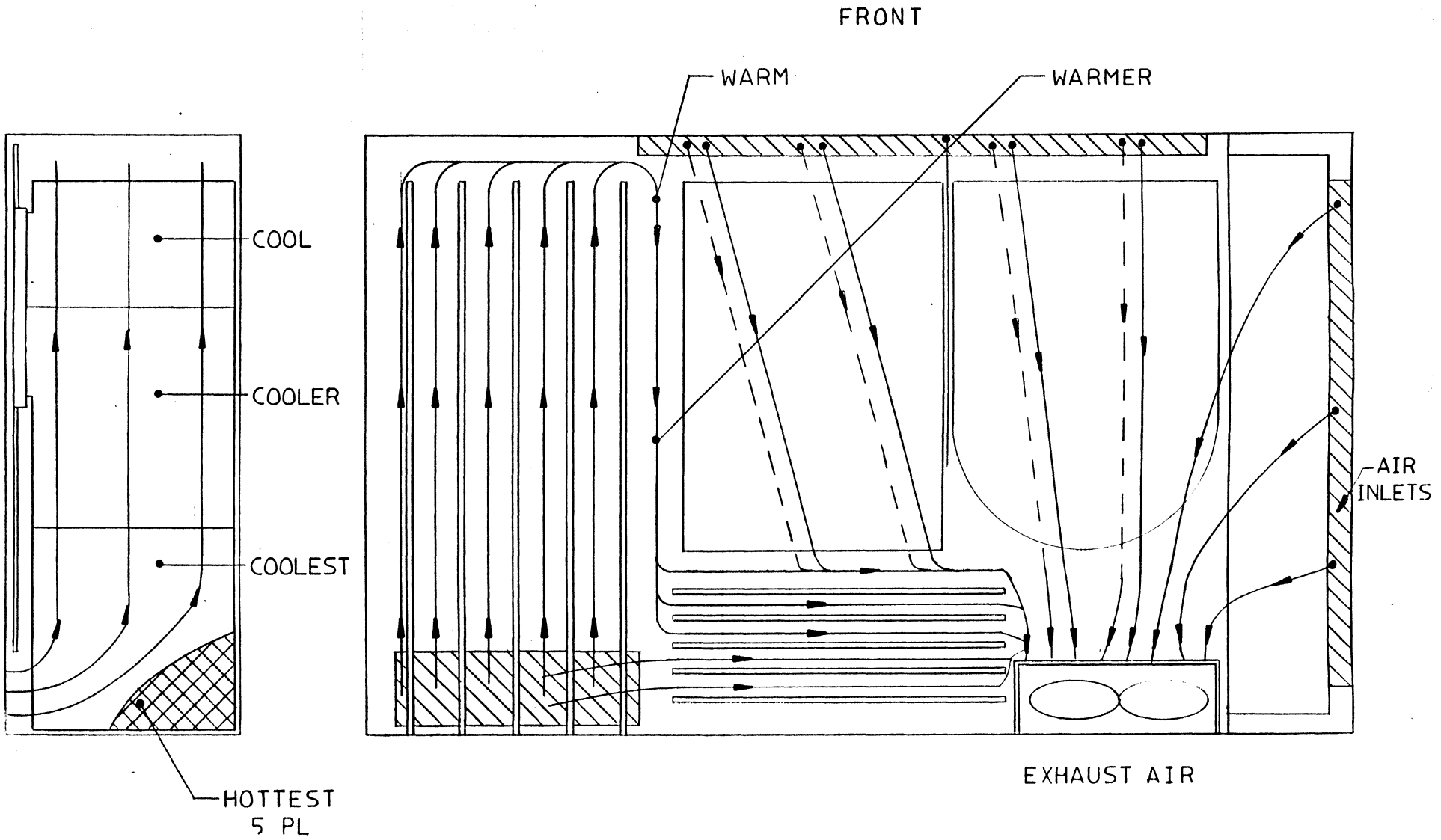
17.750
(6.35)
.25
(463.55)
18.25
REF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COOL
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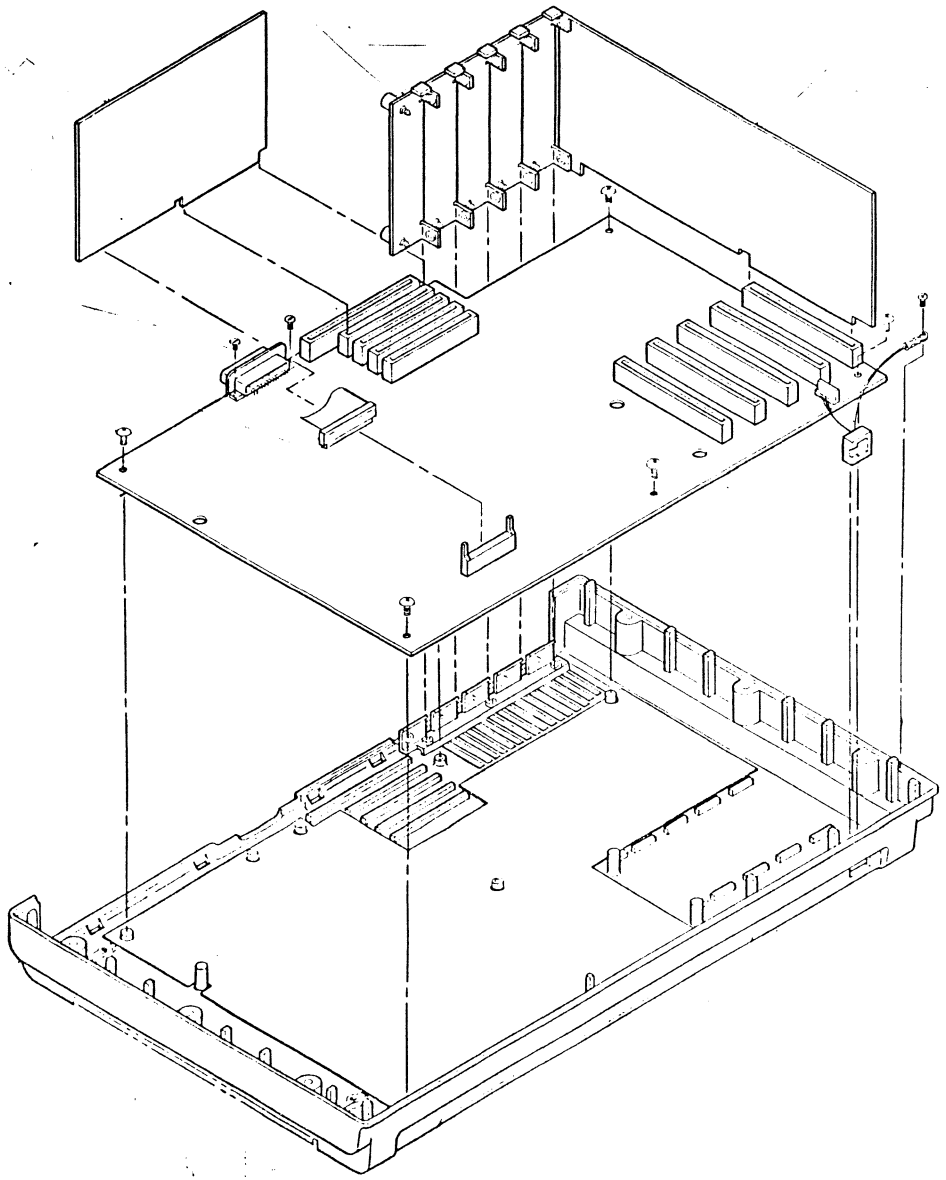
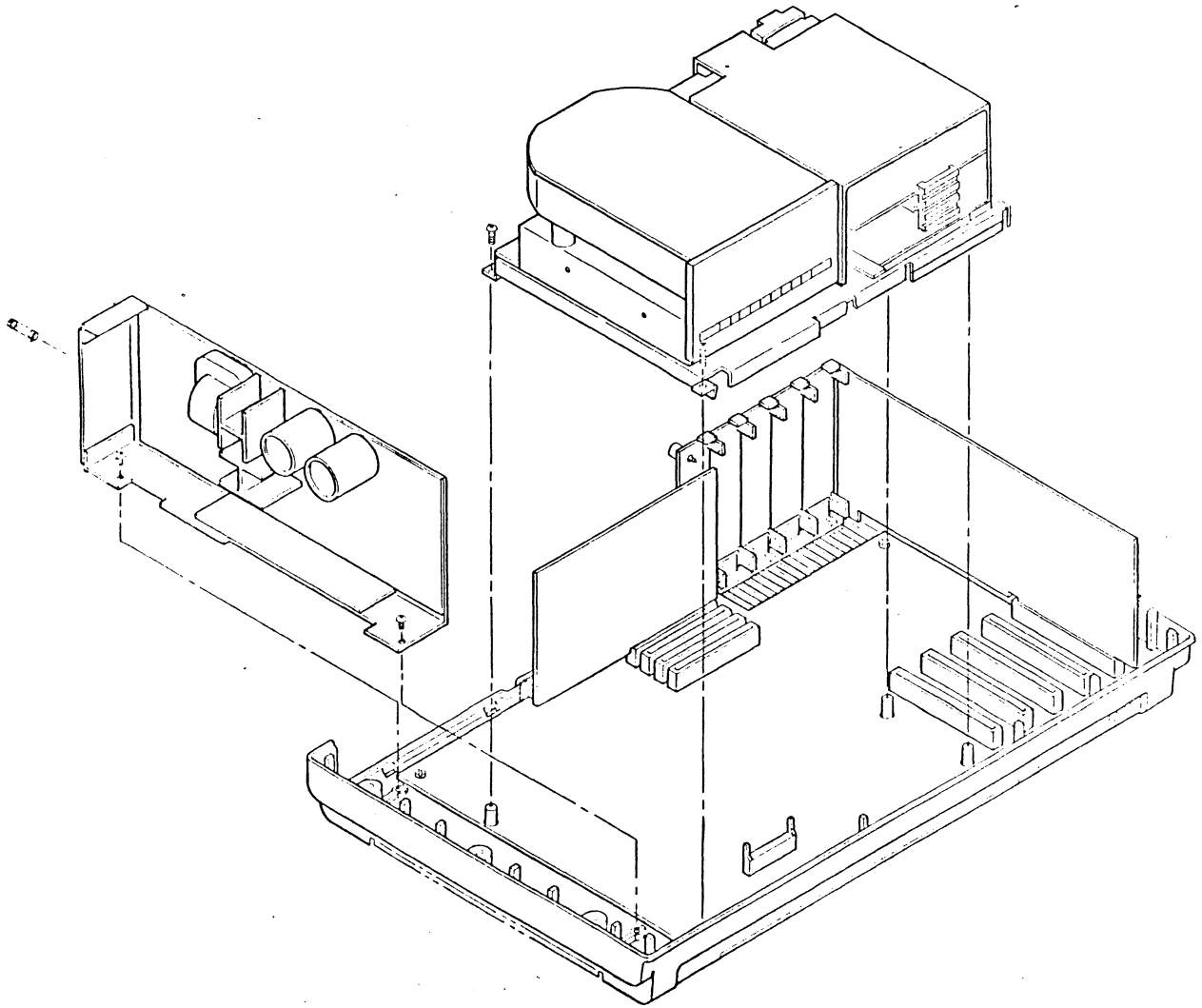
AIR
INLETS
EXHAUST AIR
HOTTEST
5 PL



FORTUNE SYSTEMS CORP
SAN CARLOS, CA 94070

SUB-ASSEMBLY
CPU

SIZE D | 10000045/10



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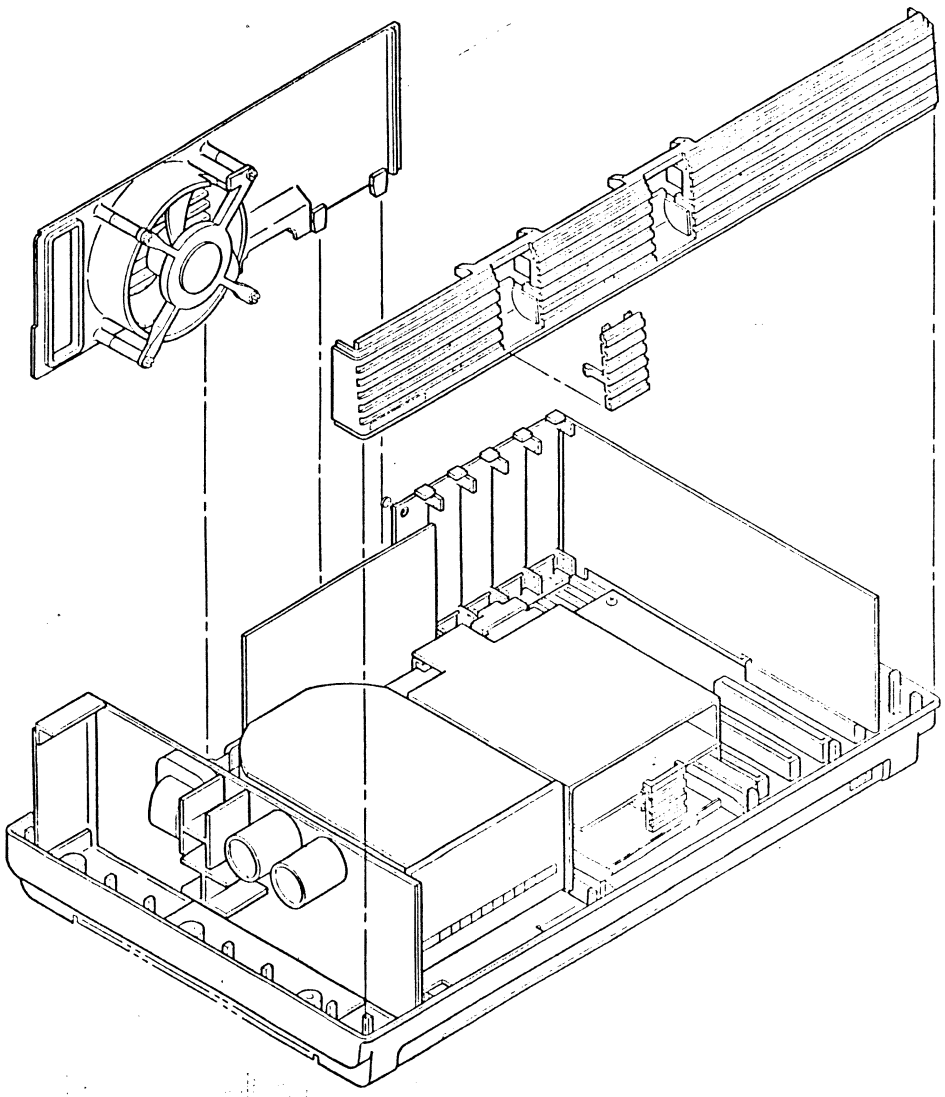
SAN CARLOS, CA

SUB-ASSEMBLY
CPU

D 10000-



FORTUNE SYSTEMS CORP
SAN CARLOS CA 94070

SUB-ASSEMBLY
CPU

SIZE D | 1000049 | REV 10

SCALE 1/2 | SHEET 2

SECTION 3

Logical Specification

The following paragraphs define each of the siginal lines on the CLB. Eather a + or a - follows the name of each siginal , and indicates a positive true (+) or a negative true (-) condition . Figures 7-11 present the relative timing considerations . Numbers in brackets [n] show the corresponding pin number .

CLBA1+ to CLBA23+ [8-30]

These 23 lines are used by the bus master device to select the slave device address to transfer to or from which data will be transferred . This can be either a memory location or a device register . For the 32/16 cpu CLBA21+ ,CLBA22+ and CLBA23+ are tied together .

The 24th address bit, A0, is specified by the presence of one or both of UDS and LDS (Upper/Lower Data Strobe). This is defined later under CLBUDS- , CLBLDS- .

Bus addresses between 0000000 hex and 1FFFFF hex are assumed to be RAM or fast devices , and use the fast ram timing. Addresses between 780000 hex and 7FFFFF hex are assumed to be slow I/O devices, and use the special slow I/O timing.

During interrupt acknowledge cycles, A1 - A3 contain the interrupt level number being acknowledged, and A4 - A23 are all ones.

CLBD0+ to CLBD15+ [34-49]

These 16 lines transfer data between master and slave devices . For word transfers, all 16 lines are used. For byte transfers, CLBD8 - CLBD15 are used for even addresses (CLBUDS active), and CLBD0 - CLBD7 are used for odd addresses (CLBLDS active).

CLBAS- [58]

Bus address strobe is used by the master to indicate to the slave that valid addresses, device address decodes, and read/write controls are present on the bus. Slow-cycle devices that must know before CLBUDS/CLBLDS that they are going to be accessed may use address strobe as an indication. See note 1.

CLBIOS - [74]

This line is unique to each of the five option slots (A-E), and indicates (when CLBAS is true) that the address on CLBA1+ to CLBA23+ is selecting the range of addresses assigned to the particular option slot. The CLBIOS- lines are valid only with CLBAS- active (low). The I/O Select line for option slot "A" is true for addresses between 7A0000 hex and 7AFFFF hex , for option slot "B" the addresses are from 7B0000 hex to 7BFFFF hex , etc. Each option thus has a 64 Kbyte address space for software driver ROMS, buffer RAMs, and various I/O register addresses. The only fixed addresses within this range are for the beginning of the software driver ROM, which must begin at relative location zero (7n0000 hex where n=slot A, B, C, D, or E) within the option slot's address space. See note 1 . See note 1.

CLBUDS- , CLBLDS- [59 ,60]

CLBUDS- (upper data strobe) and CLBLDS- (lower data strobe) are used by the bus master to indicate to the addressed slave device that the transfer is to begin. For fast (RAM) cycles, CLBUDS-/CLBLDS- will be presented concurrently with CLBAS+ . For slow (I/O register) cycles, CLBUDS-/CLBLDS- will be preceded and followed by CLBAS+ . Refer to the timming figures for the correct timing of these siginals . See note 1.

CLBR/W- [57]

This signal indicates that the current bus cycle is either a "read "or a " write " . When low , it indicates a transfer of data from the current bus master to the addressed slave device. When high , it indicates a transfer data from the slave device to bus master . For byte trasfers (only one of CLBUDS or CLBLDS are true), the content of the unaddressed byte of the CLB DATA lines is unspecified. See note 1.

CLBI03-,CLBI04- [54 , 55]

These low-true levels indicate an interrupt request to the 68000 CPU on priority levels 3 and 4, respectively. These are "wired-OR" connections, and should be driven

CLBINTACKI3-,CLBINTACKI4- [67 , 69]

These two low-true signals are input to an I/O controller to indicate that ; the CPU is acknowledging an interrupt on priority level 3 or 4, and signal that the device controller should place an interrupt vector on CLBD0 - CLBD7 if this device was requesting an interrupt. A daisy-chain priority scheme is used with board slot E having top priority and board slot A having lowest priority. See Interrupt Acknowledge Protocol section .

CLBINTACK03-, CLBINTACK04- [68 , 70]

If the signals (CLBINTACKI3- , CLBINTACKI4-) are received and the device controller was not requesting an interrupt on priority level 3 or 4, respectively, the corresponding CLBINTACKxx- line should be asserted so that devices in option slots further down the daisy-chain can respond to the interrupt acknowledgement. See Interrupt Acknowledge Protocol section .

CLBBR0- to CLBR4- [71]

This low-true signal indicates to the bus arbitration circuitry that the device is requesting to become bus master. This signal is not wired-OR, and is unique to the option slot. CLBBR4- is highest priority while CLBBRO- is lowest priority. This signal must be asserted synchronously with CLBCLK.

CLBBG0- to CLBG4- [72]

This low-true signal is unique to each option slot, and is asserted by the system bus arbitrator when this option has ; requested to be bus master, the option is the highest priority device requesting, and the bus is available. The device controller must immediately place onto the bus the DMA address, address strobe, upper and/or lower data strobe, write (if a write cycle), and data (if a write cycle). The option board with the highest interrupt priority has the lowest priority in becoming the bus master. The option board with the lowest interrupt priority has the highest priority to becoming the bus master. This signal is synchronous with bus clock.

SIGINAL	SLOT
CLBR0-/CLBG0-	E
CLBR1-/CLBG1-	D
CLBR2-/CLBG2-	C
CLBR3-/CLBG3-	B
CLBR4-/CLBG4-	A

CLBPERR- [65]

This low-true signal is sampled by the bus master during a DMA READ to determine if the data on the CLB DATA BUS has had a data error that has not been corrected by the system . See the DMA read timing figure .

CLBCLK+ [62]

This 5.5296 MHz square wave generates the timing signals in the device controller to maintain synchronous characteristics required for conforming to the various bus protocols. All control signals (execpt as noted) sent to or from a device on the CLB must be synchronous with clock. The only exception is the interrupt request lines (CLBIO3- and CLBIO4-) which may be asynchronous since the CPU contains synchronizers for these signals. Note that some signals are referenced to the positive going edge of the clock siginal , while others are referenced to the negative going edge. Refer to the timing diagrams for specifics on each siginal . See note 1.

CLBRESET- [51]

This low-true signal indicates that the I/O device controller should reset itself to a known and consistent state. Reset must clear any interrupt requests or bus request, and must cause the device control logic to cease actively driving the bus (address, data, and controls). If there is a vlotage senes module in the system then see the power fail timing figure .

CLBPRESENT- [73]

This pin must be connected to logic ground on the device option board. It signals to the CPU and the interrupt acknowledge daisy-chain circuitry that there is an option board plugged into this slot.

CLBPFL- [66]

This low-true signal provides a warning that a power fail condition is about to occur. This signal will become active about 5 msec prior to actual power failure. This signal is used by any device (disk, tape) that requires early warning so they may complete a write , and so they will not start a write with this condition . This siginal may go down and back up a number of times before power failure . If there is a vlotage senes module in the system then see the power fail timing figure 10 page 21.

CLBSPARE [52 , 53 , 64]

These signal pins are not currently connected. They are reserved for future definition by Fortune Systems Corporation.

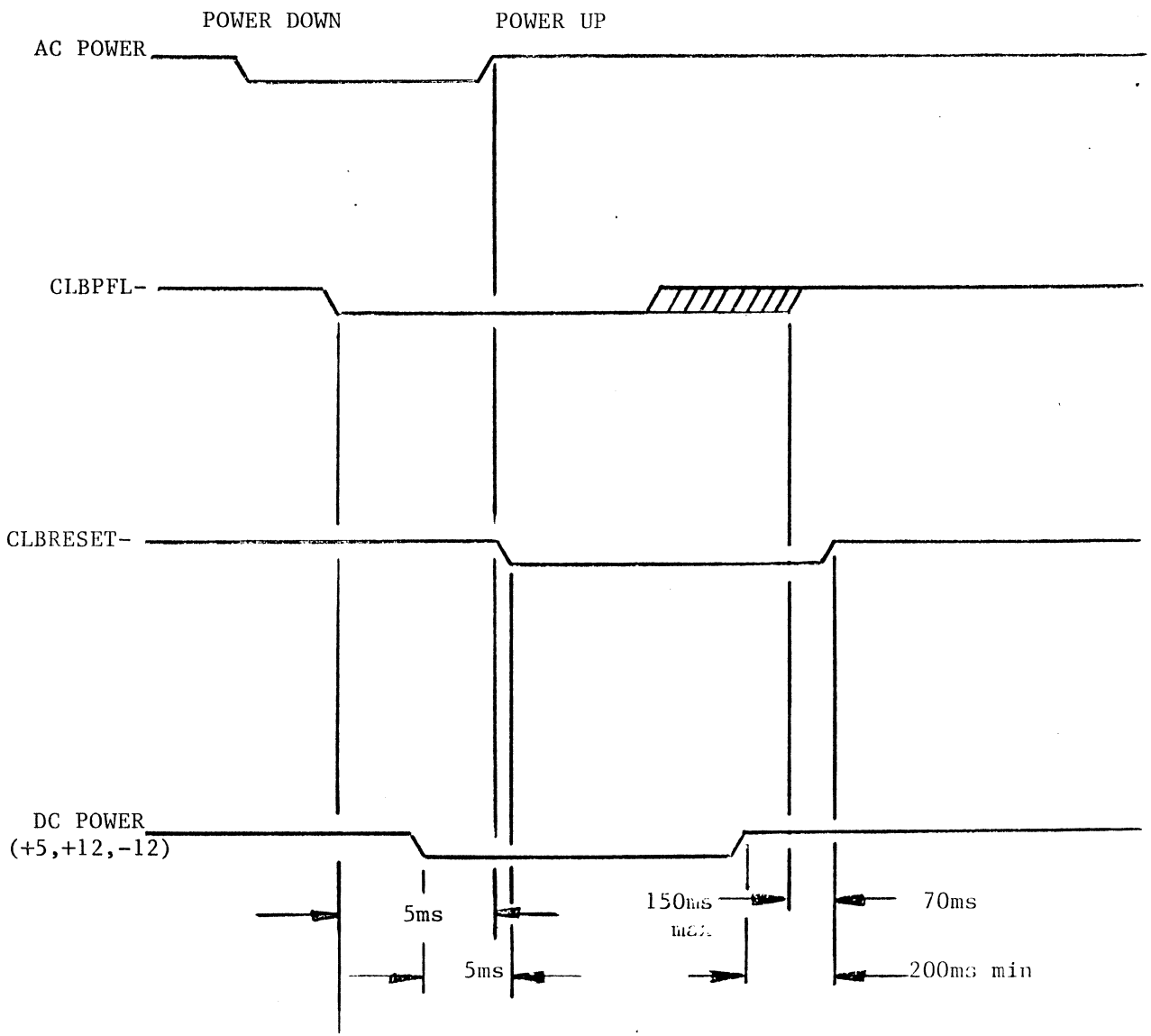
+5, +/-12,GROUND [56 , 75 , 76 , 1 , 2 , 3 , 4 , 7 , 31 , 32 , 33 , 50 , 61 , 63 , 77 , 78 , 79 , 80]

These signals supply operating voltages for the device controller option boards. There are nine connections for ground, four for +5 volts, and two each for +/-12, thus ensuring a noise-free environment on the option board. Each of the like signals should be connected in a mesh configuratior on the option board to further reduce the possibility of unwanted noise. Note see I/O Power Distribution section .

T2+ [56]

This siginal , Timing pulse 2 , is not to be used by I/O boards .

(NOTE 1 See section on Recivers, Drivers , and Termination .)


POWER DOWN
POWER UP
AC POWER
CLBPFL-
CLBRESET-
DC POWER
(+5,+12,-12)
5ms
5ms
150ms
70ms
200ms min

Interrupt Acknowledge Protocol

The interrupt protocol on the CLB allows asynchronous interrupts to be issued by I/O controllers to the microprocessor at any time. Interrupt acknowledge timing is a synchronous process initiated by the microprocessor. The interrupt acknowledge sequence is as follows:

1. Interrupt request is recived by the processor. The processor will compare the interrupt level in the status register and wait for the current instruction to complete . If the priorty of the pending interrupt is greater than the processor priority , the processor will then ask for a CLB cycle .

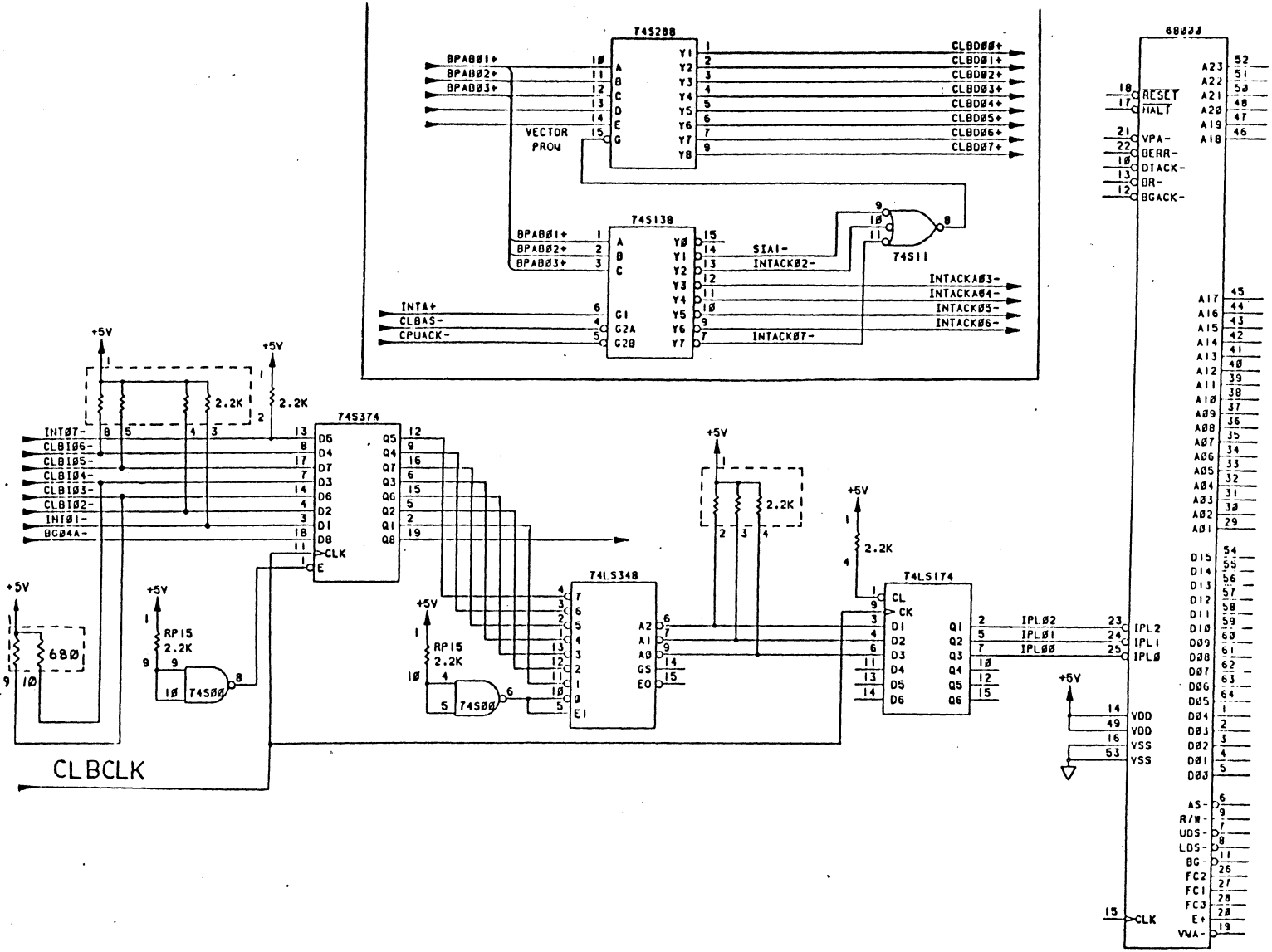
2. The CLBR/W line will become active (high) as late as CLB cycle 1 depending on what the previous process happened to be across the CLB. This line high conditions the CLB for a read (interrupt vector) from an interrupting I/O controller.

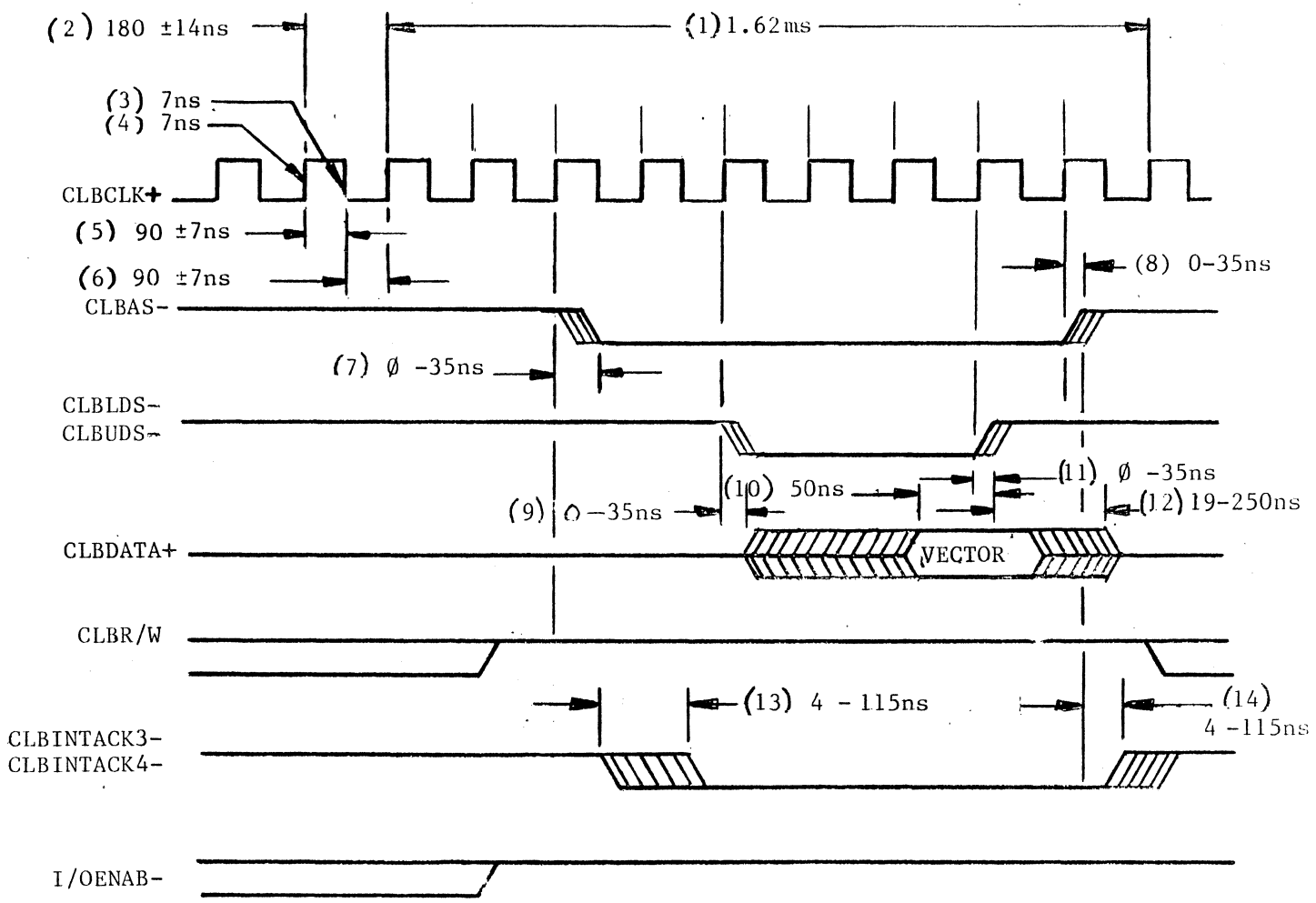
3. During CLB cycle 2, CLBAS-, CLBINTACK3- or CLBINTACK4- become active (low) and I/OENAB- becomes active (high). Each I/O controller upon detection of CLBAS- becoming active determines whether to block CLBINTACK3- or CLBINTACK4- or to pass it on to the next I/O controller with lower priority. While CLBAS- is active , no I/O controller is allowed to block CLBINTACK3- or CLBINTACK4- signal unless the controler is the one intrrupting.

4. For the decision required above , and with the worst case of four I/O controller boards prior to the last I/O controller board (25 ns delay maximum per board), CLBINTACK3- or CLBINTACK4- will be valid at the beginning of CLB cycle 4.

5. During CLB cycle 4, CLBLDS- and CLBUDS- will become active(low). The I/O controller that had blocked the CLBINTACK3- or CLBINTACK4- must place its interrupt vector on CLBD0 to CLBD7 no later than 20ns into CLB cycle 6. The interrupt vector must remain on CLBD0 tc CLBD7 until at least 19 ns after CLBUDS- or CLBLDS- becomes inactive and no later than the middle of CLB cycle 7.

6. At the beginning of CLB cycle 8, CLBAS-, CLBINTACK3- or CLBINTACK4-, and I/OENAB- become inactive. The interrupt acknowledge process is now complete.


74S288
VECTOR PROM
74S138
74S11
SIAI-
INTACKØ2-
INTACKA Ø3-
INTACKA Ø4-
INTACKØ5-
INTACKØ6-
INTACKØ7-
INTA+
CLBAS-
CPUACK-
BPAØØ1+
BPAØØ2+
BPAØØ3+
CLBDØØ+
CLBDØ1+
CLBDØ2+
CLBDØ3+
CLBDØ4+
CLBDØ5+
CLBDØ6+
CLBDØ7+
68ØØØ
RESET
HALT
VPA-
BERR-
DTACK-
BR-
BGACK-
74S374
74LS348
74LS174
74S11
74S2Ø
RP15
2.2K
68Ø
+5V
INTØ7-
CLBIØ6-
CLBIØ5-
CLBIØ4-
CLBIØ3-
CLBIØ2-
INTØ1-
BGØ4A-
CLK
E
IPLØ2
IPLØ1
IPLØØ
IPL2
IPL1
IPLØ
VDD
VSS
AS-
R/W-
UDS-
LDS-
BG-
FC2
FC1
FC3
E+
VMA-
CLBCLK


(2) 180 ±14ns
(1) 1.62ms
(3) 7ns
(4) 7ns
CLBCLK+
(5) 90 ±7ns
(6) 90 ±7ns
(8) 0-35ns
CLBAS-
(7) Ø -35ns
CLBLDS-
CLBUDS-
(11) Ø -35ns
(10) 50ns
(12) 19-250ns
(9) 0 -35ns
CLBDATA+
VECTOR
CLBR/W
(13) 4 - 115ns
(14)
4 -115ns
CLBINTACK3-
CLBINTACK4-
I/OENAB-

	Symbol	Parameter	Min.	TYP.	Max.
(1)	tia	Interrupt Acknowledge Time	1.49ms	1.62ms	1.75ms
(2)	tcy	Clock Cycle	164ns	180ns	194ns
(3)	tcf	Clock Fall Time	-----	----	7ns
(4)	tcr	Clock Rise Time	-----	----	7ns
(5)	tch	Clock With High	83ns	90ns	97ns
(6)	tcl	Clock With Low	83ns	90ns	97ns
(7)	tchasl	Clock High to Address Strobe Low	0ns	----	35ns
(8)	tchash	Clock HIGH to Address Strobe High	0ns	----	35ns
(9)	tchdsl	Clock High to Data Strobe Low	0ns	----	35ns
(10)	tdvdsh	Data Valid to Data Strobe High	50ns	----	----
(11)	tchdsh	Clock High to Data Strobe High	0ns	----	35ns
(12)	tdshdi	Data Strobe High to Data Invalid	19ns	----	250ns
(13)	taslil	Adress Strobe Low to Int. Ack. Low	4ns	----	115ns
(14)	tasiii	Adress Strobe Inactive to Int. Invalid	4ns	----	115ns
(15)	tdmawcy	DMA Write Cycle Time	498ns	540ns	582ns
(16)	tbgav	Bus Grant to Address Valid	0ns	----	25ns
(17)	tclai	Clock low to Address Invalid	20ns	----	70ns
(18)	tbgas	Bus Grant to Address Strobe	0ns	----	20ns
(19)	tclash	Clock Low to Address Strobe high	0ns	----	70ns
(20)	tbgdsv	Bus Grant to Data Strobe Valid	0ns	----	20ns
(21)	tcldsi	Clock Low to Data Strobe Invalid	0ns	----	70ns
(22)	tbgrwv	Bus Grant to Read Write Valid	0ns	----	20ns
(23)	tclrwi	Clock Low to Read Write Invalid	0ns	----	70ns
(24)	tbgdv	Bus Grant to Data Valid	0ns	----	65ns
(25)	tcldi	Clock Low to Data Invalid	20ns	----	70ns
(26)	tchbr	Clock High to Bus Request	0ns	----	25ns
(27)	tchbri	Clock High to Bus Request Invalid	0ns	----	25ns
(28)	tchbg	Clock High to Bus Grant	0ns	----	25ns
(29)	tchdgi	Clock High to Bus Grant Invalid	0ns	----	25ns
(30)	tdmarcy	DMA Read Cycle Time	498ns	540ns	582ns
(31)	tdvcl	Data Valid to Clock Low	37ns	----	----
(32)	tdsldi	Data Strobe Low to Data Invalid	15ns	----	----
(33)	tbecl	Bus Error to Clock Low	10ns	----	----
(34)	tiorcy	I/O Read Cycle Time	1.49ms	1.62ms	1.75ms
(35)	tchav	Clock High to Address Valid	0ns	----	80ns
(36)	tav	Address Valid	1.16ms	----	1.53ms
(37)	tavasl	Address Valid to Address Strobe Low	76ns	----	229ns
(38)	tasldsl	Address Strobe Low to Data Strobe Low	293ns	----	423ns
(39)	tasl	Address Strobe Low	949ns	----	1.2ms
(40)	tdsl	Data Strobe low	457ns	----	617ns
(41)	tchioel	Clock High to I/O Select Low	0ns	----	50ns
(42)	tchioeh	Clock High to I/O Select High	0ns	----	50ns
(43)	tioel	I/O Select Low	934ns	----	1.21ms
(44)	tiowcy	I/O Write Cycle Time	1.49ms	1.62ms	1.75ms
(45)	tashrwi	Address Strobe High to Data CLBR/W Invalid	0ns	----	35ns
(46)	tchrwv	Clock High to Read Write Valid	0ns	----	120ns
(47)	trwv	Read Write Valid	1.03ms	----	1.43ms
(48)	tdsldv	Data Strobe low to Data Valid	0ns	----	15ns
(49)	tashdi	Address Strobe High to Data Invalid	0ns	----	35ns
(50)	tchdv	Clock High to Data Valid	0ns	----	45ns
(51)	tdv	Data Valid	949ns	----	1.23ms
(52)	tdshdi	Data Strobe High to Data Invalid	145ns	----	250ns

Table 1. Timming Parameters

To maximize total system performance and minimize latency to other devices, the configuration of DMA devices must be limited to a maximum system aggregate throughput of 2.35 Mbyte/second peak, with a maximum for any single device of 1.3 Mbyte/second. By placing the highest transfer rate devices in the lowest numbered slots (slot "A" has the highest DMA priority), the bus bandwidth will be balanced, the CPU will continue to have about 15% available cycles during worst-case peak transfers, and the maximum latency experienced by any DMA device will be less than two words of data at its transfer rate. For any permitted combination of device rates a double buffer will suffice for the DMA device.)

This configuration assumes that DMA transfers are always word transfers to/from fast memory (main system RAM), and that each transfer takes three bus clock cycles (540 ns). Note that is the default cycle time of the RAM. While it is possible for a DMA controller to execute a byte transfer or to access slow I/O space, such accesses are not permitted by the general bus rules. Any system configuration which includes a DMA controller which violates these rules must be approved by Fortune Engineering on a case-by-case basis.

The DMA transfer sequence is as follows:

1. The controller must synchronize the requests of its devices to the system bus clock.

2. Synchronous with and between 0-25 ns after the rising edge of bus clock (CLBCLK+), the DMA controller must assert CLBBRx- (CLB cycle 0).

3. At least 50 ns before the next CLBCLK+, the address, control, and (in the case of a write) the data must be presented to the inputs of 74S series bus drives . The outputs become enabled onto the bus when CLBBGx- becomes active.

4. Between 0-35 ns after some CLBCLK+ (which one depends on bus latency with higher priority devices), the bus arbitrator will assert CLBBGx- to the DMA controller slot. The DMA controler will then immediately place the address, controls, and (if a write) data on the bus (CLB cycle 1).

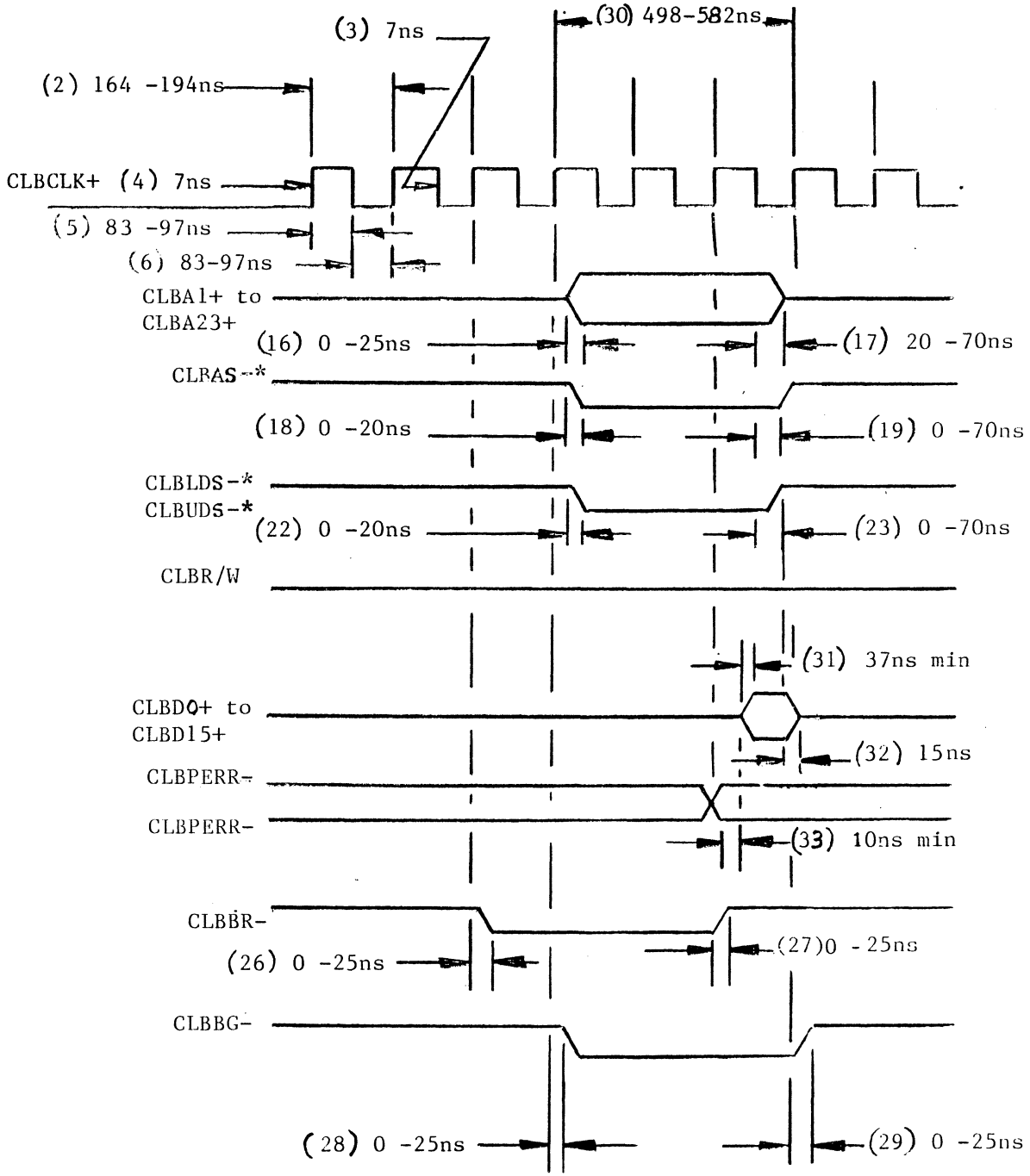
5. Between 0-25 ns after the second CLBCLK+ from the assertion of CLBBGx-, the DMA controller will de-assert CLBBRx- (CLK cycle 3) for a minimum of one clock cycle.

6. For read operations, read data will become valid on the CLBD 37 ns (minimum) prior to the trailing clock edge during CLB cycle 3. The DMA controller will use this trailing edge to clock the data into its internal data register. CLBPERR- will become valid 10 ns (minium) prior to the same trailing clock edge. CLBPERR- is sampled at this edge by the DMA controller to determine if the data on the CLBD is correct and valid.

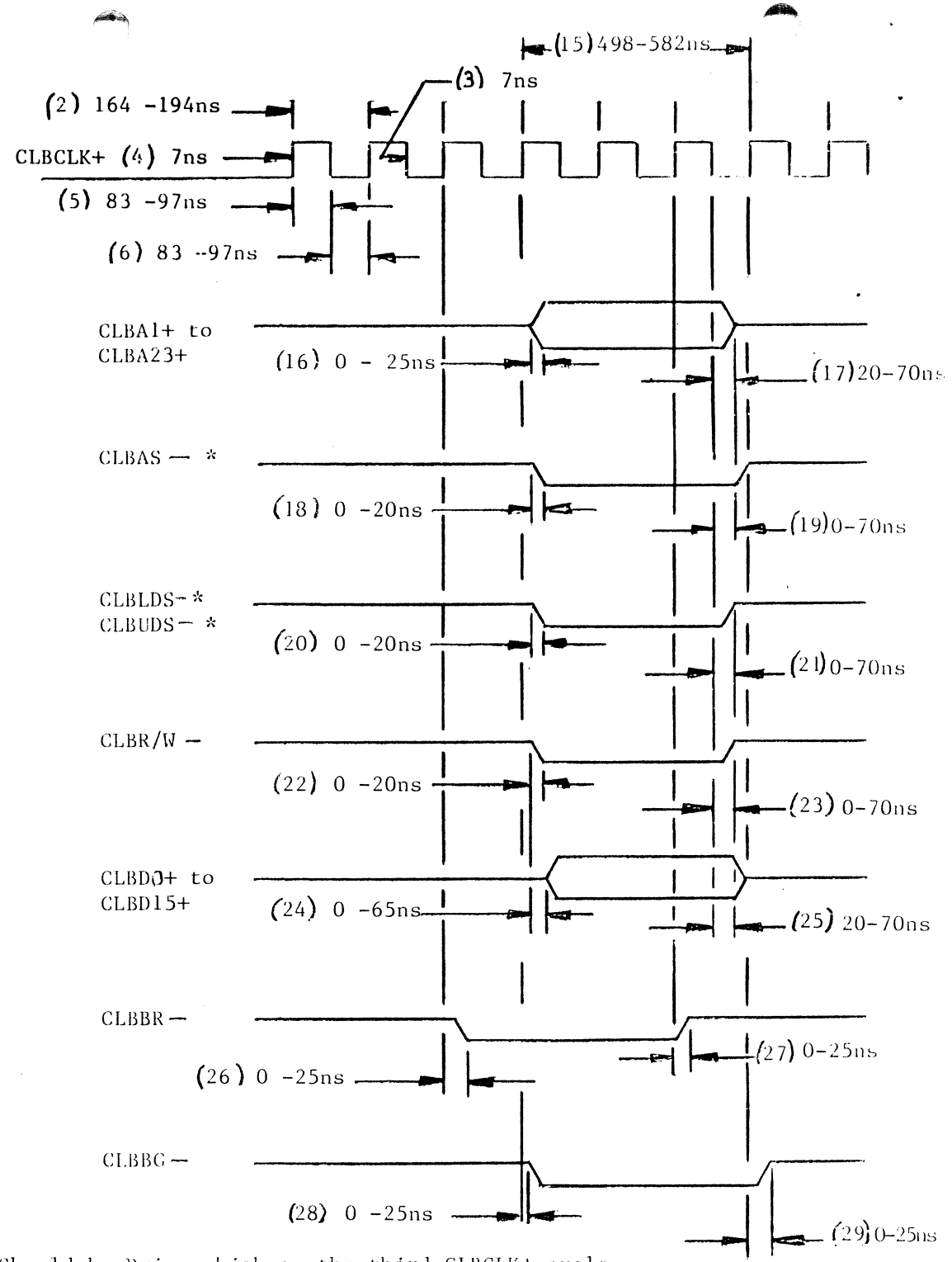
7. By the end of clock cycle 3, all CLB lines driven by the DMA controller must be disabled.

8. Between 0-35 ns after the same CLBCLK+ referred to in step 5, the bus arbitrator will de-assert CLBBGx- (in response to CLBBRx- going away at the previous CLBCLK+).

9. The bus is now idle, and the next CPU or DMA cycle can start as soon as the next CLBCLK+.



*Should be driven high on the third CLBCLK+ cycle



* Should be Driven high on the third CLBCLK+ cycle

Extended Option Addressing

As defined above, each option slot is assigned a fixed 64 Kbytes of address space, which will be in the "slow cycle" area of the system bus address space. There is one megabyte of unallocated "fast" address space and 1.5 megabyte of unallocated "slow" space left in the system bus address space with the maximum RAM and all five option slots installed. This address space may be assigned to selected device controllers, such as large bit-mapped displays, by the following mechanism:

The controller must contain an on-board base address register and an address decode comparator. At system reset time, the device controller must disable the extended address space selector, and wait for system software (usually contained in the device ROM, however) to write to the base address register. From then on, the device will respond to any address within the range covered by its base register and by the size of the allocated address space.

I/O Read/Write Protocol

The Read/Write protocol for the CLB is conventional and does not impose as fast a timing requirement as the DMA cycle . Reda and write operations require nine CLB cycles for each word read or written to main memory and should not be used to transfer large blocks of data . Where large amounts of data are to be transferred DMA control should be employed .

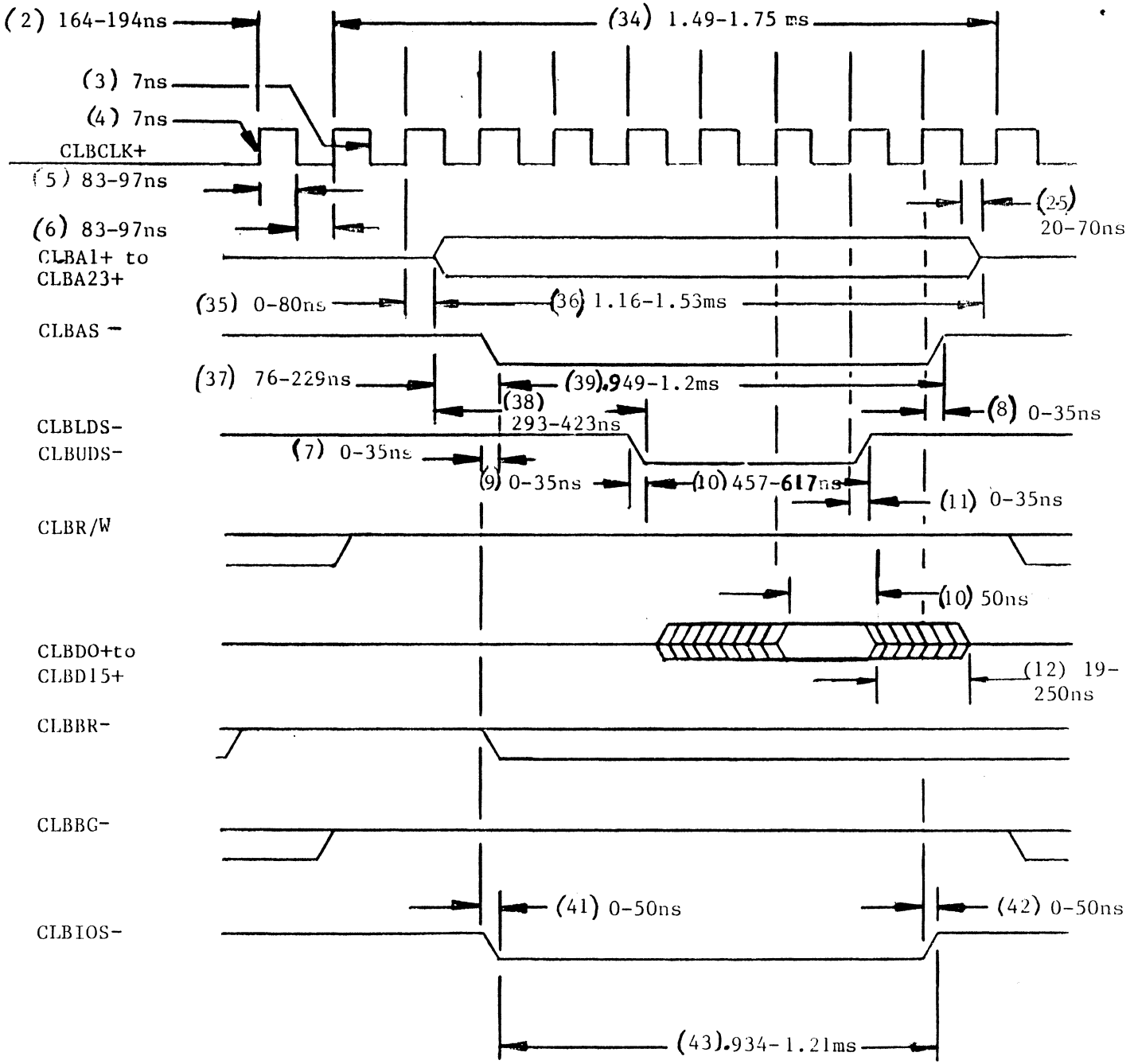
The Read/Write operation is defined as follows :

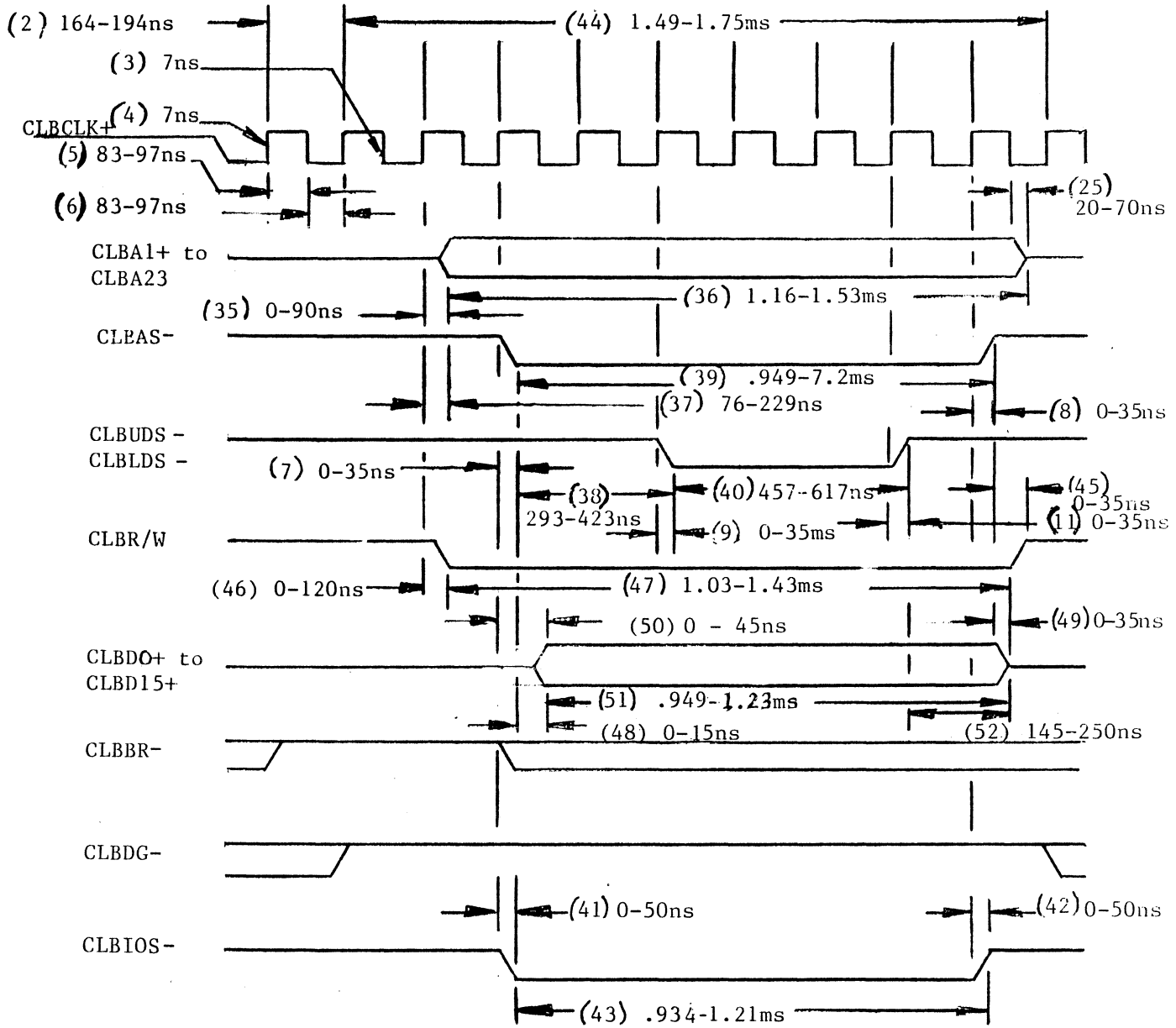
1. The CLBR/W line will be high during the first CLB cycle . If the cycle is to be a write cycle the the CLBR/W line will go low in the second CLB cycle .

2. From 0ns to 90ns after the rising edge of the second CLB cycle the address lines become stable . These lines should be decoded prior to the address strobe (CLBAS-) which occures from 0ns to 35ns after the rising edge of the third CLB cycle . This siginals the beginning of the I/O cycle .

3. In the case of a I/O write the data will be presented to the bus at about the same time that CLBAS- becomes stable . This is from 325ns to 395ns prior to CLBLDS- and CLBUDS-, and will remain stable from 145ns to 250 ns after CLBLDS- and CLBUDS- go away . This timing allows extra time for slow controllers . In the case of a I/O read data must be presented to the bus no later than 0ns to 20ns into CLB cycle 6 and must remain stable from 19ns to 55ns after CLBLDS- and CLBUDS- go away .

4. From 0ns to 35ns into CLB cycle 8 the address strobe is removed which siginals the completion of the I/O cycle .


(2) 164-194ns
(34) 1.49-1.75 ms
(3) 7ns
(4) 7ns
CLBCLK+
(5) 83-97ns
(25) 20-70ns
(6) 83-97ns
CLBA1+ to CLBA23+
(35) 0-80ns
(36) 1.16-1.53ms
CLBAS -
(37) 76-229ns
(39).949-1.2ms
(38) 293-423ns
(8) 0-35ns
CLBLDS-
CLBUDS-
(7) 0-35ns
(9) 0-35ns
(10) 457-617ns
(11) 0-35ns
CLBR/W
(10) 50ns
CLBDO+to CLBD15+
(12) 19-250ns
CLBBR-
CLBBG-
(41) 0-50ns
(42) 0-50ns
CLBIOS-
(43).934-1.21ms


(2) 164-194ns
(44) 1.49-1.75ms
(3) 7ns
(4) 7ns
CLBCLK+
(5) 83-97ns
(6) 83-97ns
(25) 20-70ns
CLBA1+ to CLBA23
(35) 0-90ns
(36) 1.16-1.53ms
CLEAS-
(39) .949-7.2ms
(37) 76-229ns
(8) 0-35ns
CLBUDS -
CLBLDS -
(7) 0-35ns
(38) 293-423ns
(40) 457-617ns
(45) 0-35ns
(9) 0-35ms
(11) 0-35ns
CLBR/W
(46) 0-120ns
(47) 1.03-1.43ms
(50) 0 - 45ns
(49) 0-35ns
CLBDO+ to CLBD15+
(51) .949-1.23ms
(48) 0-15ns
(52) 145-250ns
CLBBR-
CLBDG-
(41) 0-50ns
(42) 0-50ns
CLBIOS-
(43) .934-1.21ms

Section 4

Electrial Specifications

Bus DC Parameters

DC parameters for the various siginals on the bus are shown in Table 2.

Table 2. DC Parameters

	Output Signal Drive of Controller				Input Siginal Requirements of Controller			
Bidirectional Signals	High State Voh Min.	High State Ioh Max.	Low State Vol Min.	Low State Iol Max.	High State Vih Min.	High State Iih Max.	Low State Vil Min.	Low State Iil Max.
CLBA1-CLBA23	+2.4V	-6 mA	+.5 V	24mA	+2V	-1 mA	+ .5V	4 mA
CLBUDS,CLBLDS CLBD0-CLBD15 CLBR/W,CLBAS	+2.4V	-10mA	+.5 V	24mA I/O 64mA DMA	+2V	-1 mA	+ .5V	2 mA
Output Siginals								
CLBINTACKI3,4 CLBPRESENT CLBBR0-CLBBR4	+2.4V	-.5mA	+.5 V	4mA				
CLBIO3 CLBIO4	+2.4V	-2 mA	+.5 V	24mA				
Input Siginals								
CLBIOS CLBINTACKO3,4 CLBPERR					+2V	-1 mA	+ .8V	6 mA

Recivers , Drivers , and Termination

Siginals (CLBUDS-, CLBLDS-, CLBAS-,CLBIOS-, CLBCLK+, AND CLBR/W that cross a connector should be buffered with a Schmitt-Trigger buffer . At no time should a clocked device (EXP. 74s74) be put on a CLB control line . The stripline from the I/O connector to the buffer should be as short as possable (less than 4 in).

Typical bus drivers generate siginals that drive the bus from S244 devices .

The CLB has no termination networks on it . The address and data lines do not have any pull up resistors on them . There are 2.2k pull ups on the CLBAS-, CLBLDS-, CLBUDS- , CLBR/W-, all CLBBR lines, T2-,and all CLBPRESENT- lines . There is a 680 ohm pull up on the CLBIO3- and CLBIO4- lines .

The characteristic impedance on all I/O boards should be on the order of 50 ohms.

I/O Power Distribution

Power should not drop more than 50mV on the mother board from the power connector to the I/O connectors . The power should also not drop more than 50 mV on the I/O card from I/O connector to the back plate . Power supply limits should be noted and accounted for . See table 3 for the power consumption of a 32/16 system . Note that there are three types of power supplies in the feild see table 4.

	+5V	+12V	-12V
Mother Board	8.00		
256K Ram (1)	1.60		
Hard Disk Controler	3.05		
Hard Disc Drive	.75		
Keyboard	.18		
Flex Disc Drive	.45		

TABLE 3

power supply 1	22 amps at +5V 4 amps at +12V
power supply 2	28 amps at +5V 4 amps at +12V
power supply 3	32 amps at +5V 5 amps at +12V

TABLE 4