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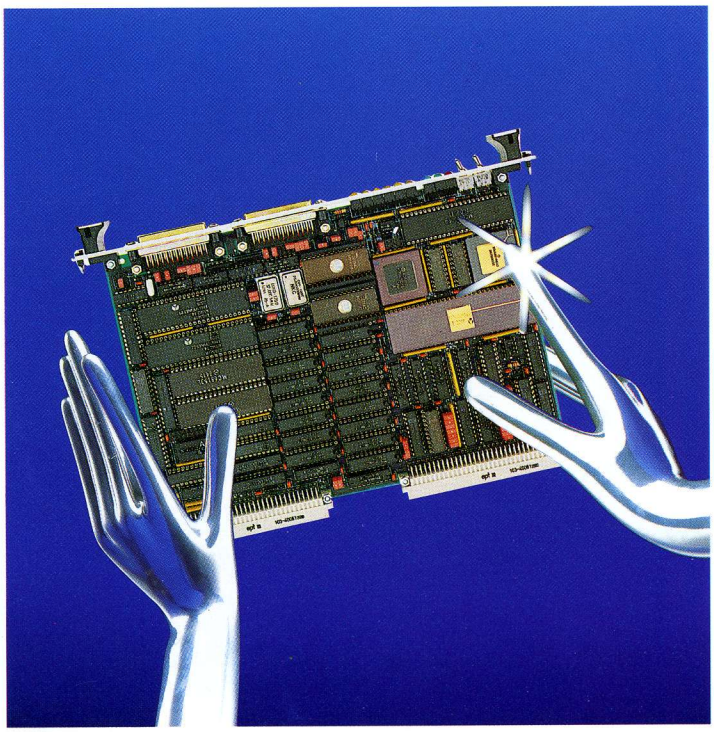
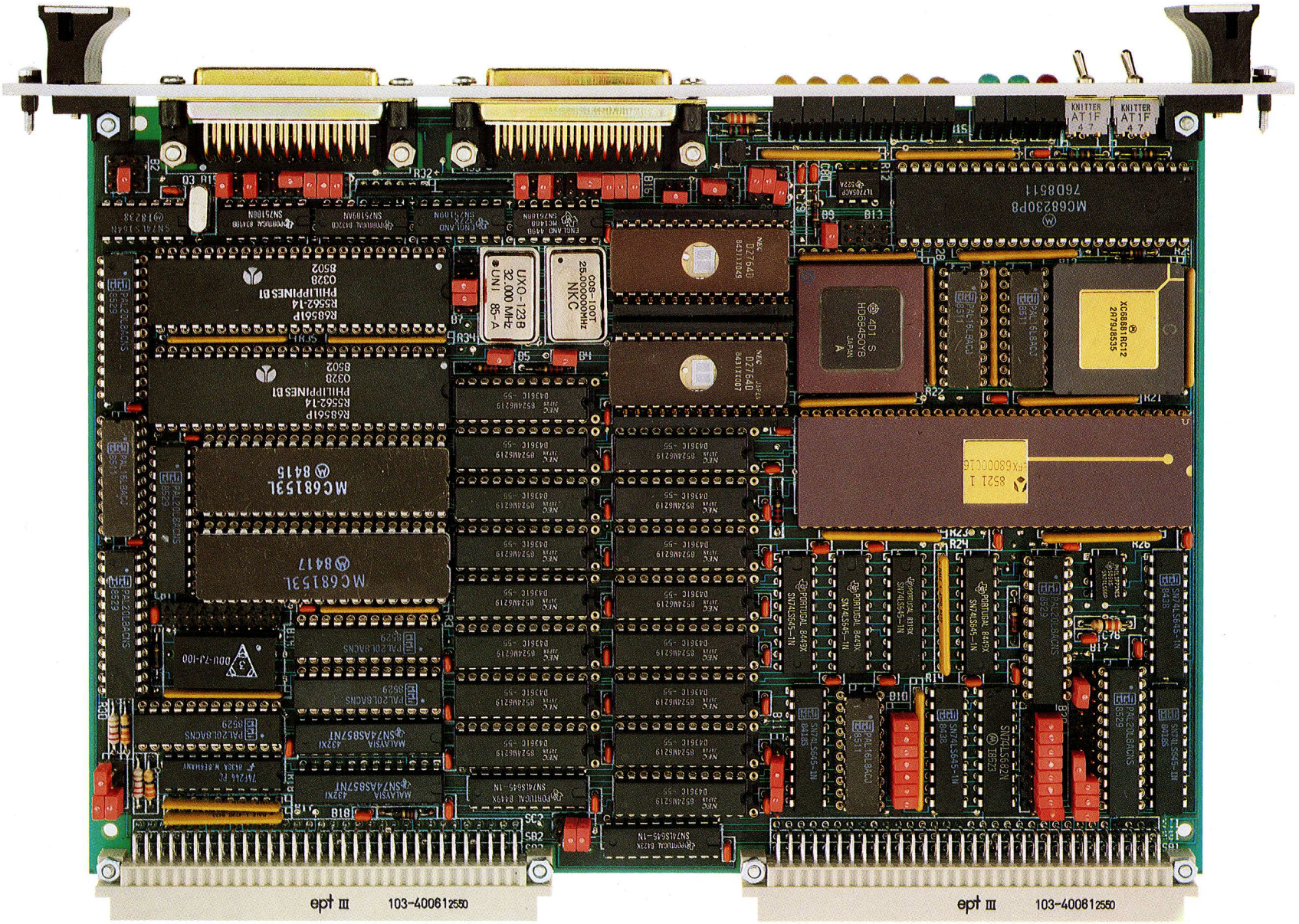


System 68000 VME
SYS68K/CPU-5

16MHz CPU Board with Floating Point Co-Processor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General Description

The SYS68K/CPU-5 boards are high speed computer boards built around the 68000/68010 CPU and the ultra fast Floating Point Co-Processor 68881.

Zero wait state operation is performed at 16.7 MHz CPU clock frequency by accessing the 128 Kbyte high speed static RAM.

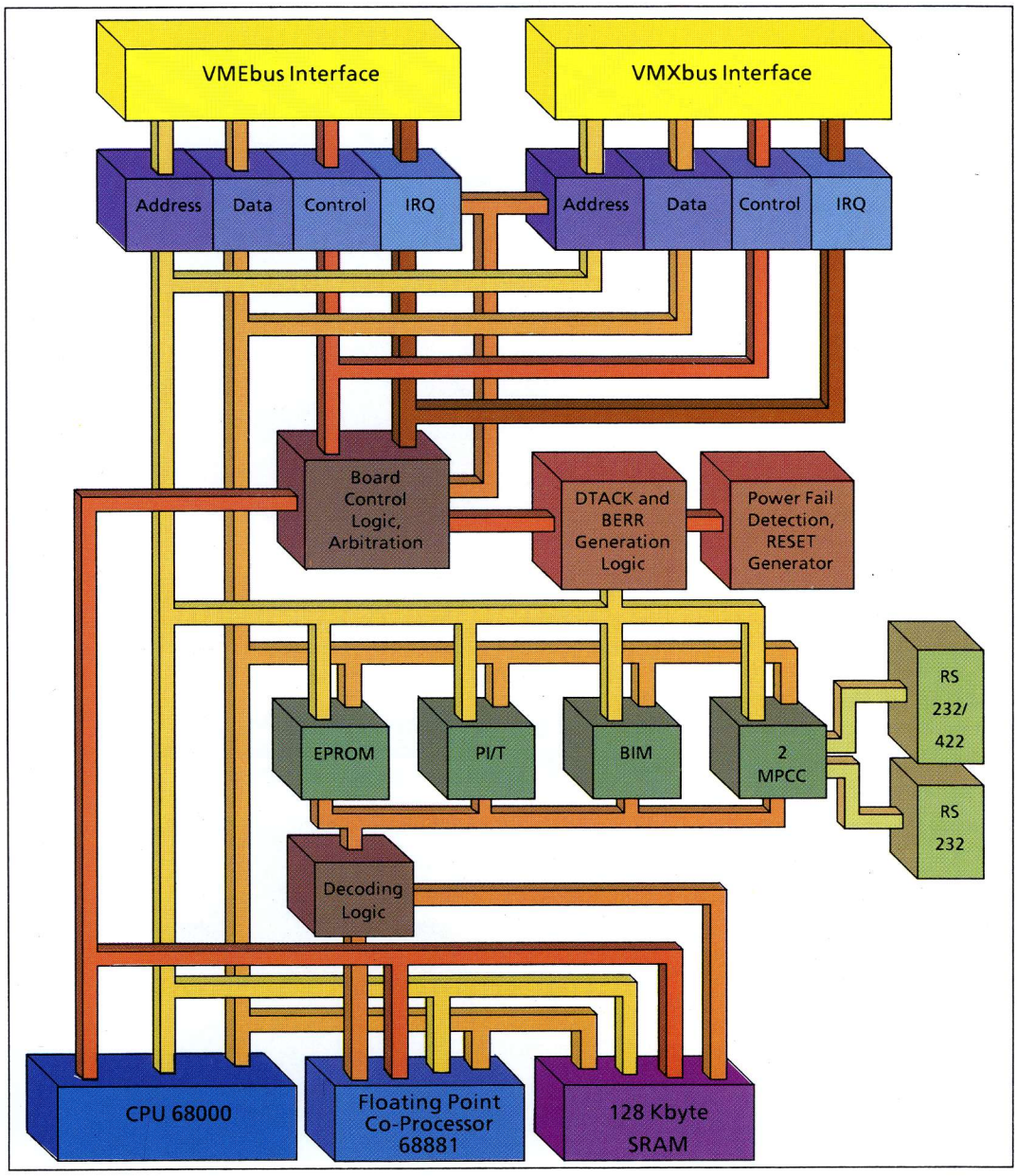
The installed four channel DMA Controller is capable of transferring data from memory to memory or from the two serial interfaces to memory.

One Parallel Interface and Timer Module offers a software programmable timer as well as VMEbus exception signal handling.

The implemented VMEbus interface is fully VMEbus and IEEE P1014 compatible and includes a one level arbiter.

The primary VMXbus interface completes the board and offers optimized multiprocessing support.

The block diagram shows the board structure of the CPU-5 in detail.



Block Diagram of CPU-5A

SYS68K/CPU-5A Features

- 68000 CPU with 16.7MHz clock frequency.
- 68881 Floating Point Co-Processor with 16.7MHz clock frequency.
- 68450 DMA Controller with 8MHz clock frequency.
- 68561 Multi Protocol Communications Controllers with two RS232 compatible interfaces.
- 68230 Parallel Interface and Timer Module with 8MHz clock frequency.
- 128 Kbytes of zero wait state static RAM.
- 4 EPROM sockets for system and/or user programs.
- All on-board interrupt requests are software programmable (level and vector).
- Each VMEbus IRQ (1-7) can be enabled or disabled via software through the PI/T.
- Single level arbiter.
- VMEbus interface (A24:D8,D16; A16:D8,D16).
- VMXbus primary master interface (A24:D16).
- Self-contained operating firmware that provides debug, one line assembly/disassembly and I/O control functions.
- 9 Status LED's, RESET and ABORT function switch.
- High level real time operating systems available.

Table 1 shows the global memory layout of the CPU-5 board:

Table 1 CPU-5 Memory Layout

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	Static RAM on CPU-5A/5V (128Kbyte)
020000 to xxxxxx	VME or VMXbus Addresses
xxxxxx to EFFFFF	VMX or VMEbus Addresses
F00000 to F7FFFF	SYSTEM and USER EPROM Area
F80000 to F8FFFF	LOCAL I/O Devices
F90000 to FEFFFF	VMEbus Addresses
FF0000 to FFFFFF	Short I/O VMEbus Addresses

Different Features of the SYS68K/CPU-5V

- 68010 CPU with 12.5MHz clock frequency.
- 68881 Floating Point Co-Processor with 12.5MHz clock frequency.

The SRAM, EPROM, and the Floating Point Co-Processor are communicating to the DMAC and the CPU via their buffered bus.

1. 68000/68010 Central Processing Unit

The high performance 68010 CPU with its upgrated 68000 instruction set and virtual memory support offers a total of 16M Bytes of addressable memory through its 24 address signals. The fully asynchronous 16 bit data bus allows high speed data transfer to/from the on-board, VME- or VMXbus memory and I/O areas.

The SYS68K/CPU-5A uses a 16.7MHz 68000 processor while the CPU-5V uses a 12.5MHz 68010 CPU. Both CPU-5 versions are running constantly without any wait states out of the 128 KByte of static RAM.

2. The Floating Point Co-Processor:

The 68881 Floating Point Co-Processor is a full implementation of the IEEE Standard P754 for Floating Point Arithmetic (Draft 10.0).

A set of 8 general Floating Point Data Registers, supporting full 80 bit extended precision are available for arithmetic operations such as:

Add	Sin, cosine, hyperbolic sin and cosine
Subtract	Tangent, cotangent, hyperbolic tangent and cotangent
Multiply	e EXP(x)
Divide	e EXP(x–1)
Compare	E EXP(xtract (4))
Scale Exponent	ln (x), ln (x+1)
Modulo	log 10 (x), log 2 (x)
Conditional branches	
Absolute value	2 EXP(x), 10 EXP (x)
	Square root
	Conditional Trap (32)

The FPCP supports the following date types:

Byte, Word and Long Integers

Simgle, Double and Extended Precision Real Numbers

Packed BCD String Real Numbers

The SYS68K/CPU-5A is fitted with a 16.7MHz, while CPU-5V uses a 12.5MHz FPCP.

3. The Static RAM

Zero wait state operation for the CPU and the DMAC at 12.5 or 16.7MHz clock frequency is provided by using the 16 static RAM's.

128 Kbyte of SRAM with a maximum access time of 55ns is provided on each CPU-5 board for program and/or data storage.

4. The SYSTEM and the USER Area

The CPU-5 contains four sockets for JEDEC compatible EPROM devices. Two 27128 devices are used for the SYS68K/CPU-5 DEBUGGER firmware (included in the shipment).

The following table lists the usable EPROM types for each area:

Device	Organization	TOTAL Capacity
2764	8K x 8	32 Kbyte
27128	16K x 8	64 Kbyte
27256	32K x 8	128 Kbyte
27512	64K x 8	256 Kbyte

The access time for both areas is jumper selectable in the range of 100-400ns to adapt different EPROM access times.

5. 68450 Direct Memory Access Controller

A high-speed DMA Controller with 8MHz clock frequency is used on the board to move data on the local, VMX- and the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.

The DMAC has a maximum data transfer speed of 4 MBytes per second. Time critical programs can thus be loaded into the local RAM via the DMAC, which allows number cruncher applications without the time overhead through the VME/VMXbus. This also results in a lower bus load.

The 68450 is connected to the two serial interface channels to optimise serial communication (if required).

6. 68561 Multi-Protocol Communication Controllers

The CPU-5 boards contains two serial interfaces for communication to a terminal and/or printer/host computer.

The MPCC offers different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.

Protocols:

- IBM binary synchronous (ASCII or EBCDIC).
- Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECMA 16 etc.)
- Synchronous Bit oriented protocols (SDLC, HDLC, ADCCP, X.25).

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.

The I/O signal assignment of the 4 input and 4 output signal per channel to the 25 pin D-Sub-connectors on the front panel is jumper selectable.

The MPCC is able to force an interrupt with 3 different software programmable vectors to the CPU.

7. The Local Control

The Parallel Interface and Timer Module (PI/T) with its 8MHz clock frequency allows an optical status display through six yellow status LEDs mounted on the front panel.

Each interrupt request level from the VMEbus can be enabled or disabled independent from each other through the CPU (dynamically). The VMEbus signals ACFAIL and SYSFAIL are monitored through the 3rd PI/T port.

The bus release functions described in the VMEbus section are also software programmable.

The PI/T includes a 24-bit programmable timer with a 5 bit prescaler. This timer may be used for measuring time delays or as a watchdog timer.

8. The Interrupt Structure

The CPU-5 contains two Bus Interrupter Modules to provide a flexible interrupt structure for multi-processor applications.

Each on-board interrupt request is software programmable to one of the IRQ levels of the CPU. The vector is also free software programmable.

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Each on-board interrupt request is software programmable to one of the IRQ levels of the CPU. The vector is also free software programmable.

The following table lists all the on-board interrupt sources:

Interrupt	Device
ABORT	SWITCH
TIMER	PI/T
Serial I/O 1	MPCC 1
Serial I/O 2	MPCC 2
DMAC	DMAC
ACFAIL	VMEbus
SYSFAIL	VMEbus
IRQVMX	VMXbus

The VMXbus interrupt request is routed into the on-board IRQ structure to offer maximum flexibility (software programmable level and vector).

The VMEbus interrupt requests can be dynamically enabled or disabled to the CPU through the PI/T device. This allows dynamic adaption for high end multi-processor environments because each of the IRQ's (1-7) can be selected separately under run time of the CPU (no jumper settings are required).

9. The VMXbus Interface

The CPU-5 board contains a primary VMXbus interface with a jumper selectable access address range in the whole address space of 16M bytes.

24 address lines and 16 data lines are supported from the VMXbus interface. The early DTACK option can be used to speed up the access cycles.

10. The VMEbus Interface

The implemented interface supports 24 address, 16 data, 6 address modifiers and all the control signals.

The transfer of 8 and 16 bit (A24: D8, D16) is supported.

Software programmable bus release functions allow flexible adjustment to the various application dependent requirements.

ROR	Release on Request
RBCLR	Release on Bus Clear
RAT	Release after Time-Out
RWD	Release when Done

The single level arbiter included on the board simplifies installation of the CPU-5 into a VMEbus environment.

The Debug Firmware Features of the FORCEbug

- Powerful Command Set including:
  - Test facilities
  - Debugging tools
  - Up/down load utilities
- Line assembler/disassembler fully supporting all 68020 and 68010 opcodes and addressing modes
- Full support of floating point co-processor
- Macro facility for FORCEbug commands
- Recall of last input line using Control A
- System timer with 10msec clock tics

General Description

FORCEbug is an EPROM resident debugging package for the SYS68K/CPU-5. It features test facilities, debugging tools, a powerful line assembler/disassembler for the 68000/68010 as well as for the 68881 co-processor and a macro facility for use with all FORCEbug commands.

The test facilities allow the user to test and debug hardware on the external bus as well as to prove functionality of all onboard devices.

The debugging tools are well suited to down-load programs from a host computer and debug them on the board. Included is breakpoint setting, single stepping, tracing, display and change of all processor registers and memory contents.

With the macro facility, several FORCEbug commands can be combined in one command name and then executed together. It also allows parameter substitution for up to eight parameters.

FORCEbug takes approx. 32Kbytes of EPROM space and resides in two 27128 EPROMs. Additionally, approx. 8Kbytes of read/write memory are used by FORCEbug for vector and parameter storage.

Command Summary

1. Block Commands:

BF	Fill block of memory with constant value.
BM	Move block of memory.
BS	Search a block of memory for constant value.
BT	Test a block of memory.
BV	Verify two blocks of memory.

2. Memory Commands:

M	Display/change memory including line assembly, disassembly.
MD	Display memory contents in Hex and ASCII.
MS	Set memory to a constant value or string.

3. System Facilities:

COLD	Cold start the monitor.
TIME	Enable/disable display of the run time of user programs.
TM	Transparent Mode via Port 2.
PA	Attach a serial printer to Port 2,3
NP	Detach the serial printer from Port 2,3

4. Debugging Tools:

BP	Set/remove/display breakpoints.
DR	Display formatted registers.
G	Start user program at address.
RM	Display/set processor register.
RL	Set register list to be displayed by DF command and during trace.
T	Trace continuous.
TC	Set trace count.

5. Macro Facility:

DIR	Display list of defined Macros.
KILL	Delete all defined Macros.
LIST	List Macro contents.
MACRO	Define a Macro.
MLOAD	Load Macros from memory.
MSAVE	Save Macros in memory.
REN	Rename Macro

6. Up/downloading:

LOAD	Load SREC from port to memory.
SEND	Dump SREC from memory to port.

Specifications of the SYS68K/CPU-5 Boards

Microprocessors	68000 CPU 16.7MHz on CPU-5A 68010 CPU 12.5MHz on CPU-5V
Floating Point Co-Processor	68881 FPCP 16.7MHz on CPU-5A 68881 FPCP 12.5MHz on CPU-5V
SRAM	128 Kbyte of zero wait state static RAM (16.7MHz operation)
EPROM	4 Sockets for JEDEC compatible EPROM's 256 Kbyte (max)
CONTROL	68230 PI/T for interrupt control and timer function
DMA Controller	68450 DMAC 8MHz
Serial I/O	68561 MPCC with software programmable protocolls and baud rate 2 serial interfaces RS232 compatible
Interrupts	All on-board interrupts are software programmable on level and vector. Off-board interrupts can be enabled/disabled via software (dynamically)
VMXbus	Primary VMXbus interface: A24:D16, early DTACK option
VMEbus	VMEbus interface A24: D8, D16 A16: D8, D16 IRQ handler (1-7 dynamically) Single level arbiter Requester (0-3 static)
Firmware	32 Kbytes of firmware called SYS68K/CPU-5 DEBUGGER
Power Requirements	+ 5V/5.0A(max) +12V/200mA(max) −12V/200mA(max)
Operating Temperature	0 to +50 degrees C
Storage Temperature	−50 to +85 degrees C
Relative Humidity	0–95% (non-condensing)
Board Dimensions	Double Eurocard 234x160mm (9.2x6.3")

Ordering Information

SYS68K/CPU-5A Part No. 100501	16.7MHz 68000 CPU board with Floating Point Co-Processor (16.7MHz) and debugger software, HUM and SUM included.
SYS68K/CPU-5V Part No. 100502	12.5MHz 68010 CPU-board with Floating Point Co-Processor (12.5MHz) and debugger software, HUM and SUM included.
SYS68K/CPU-5 UM Part No. 800078	User's Manual for CPU-5A/-5V.

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